GreenPAK
Programmable Mixed-signal Matrix

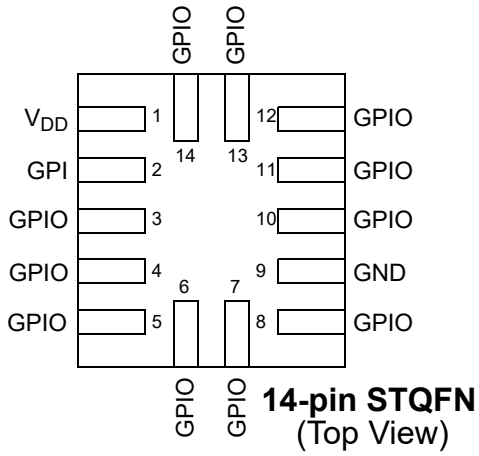
Features

- Logic & Mixed Signal Circuits
- Highly Versatile Macrocells
- Read Back Protection (Read Lock)
- 1.8 V (±5 %) to 5 V (±10 %) Supply
- Operating Temperature Range: -40 °C to 85 °C
- RoHS Compliant / Halogen-Free
- 14-pin STQFN: 2 x 2.2 x 0.55 mm, 0.4 mm pitch

Applications

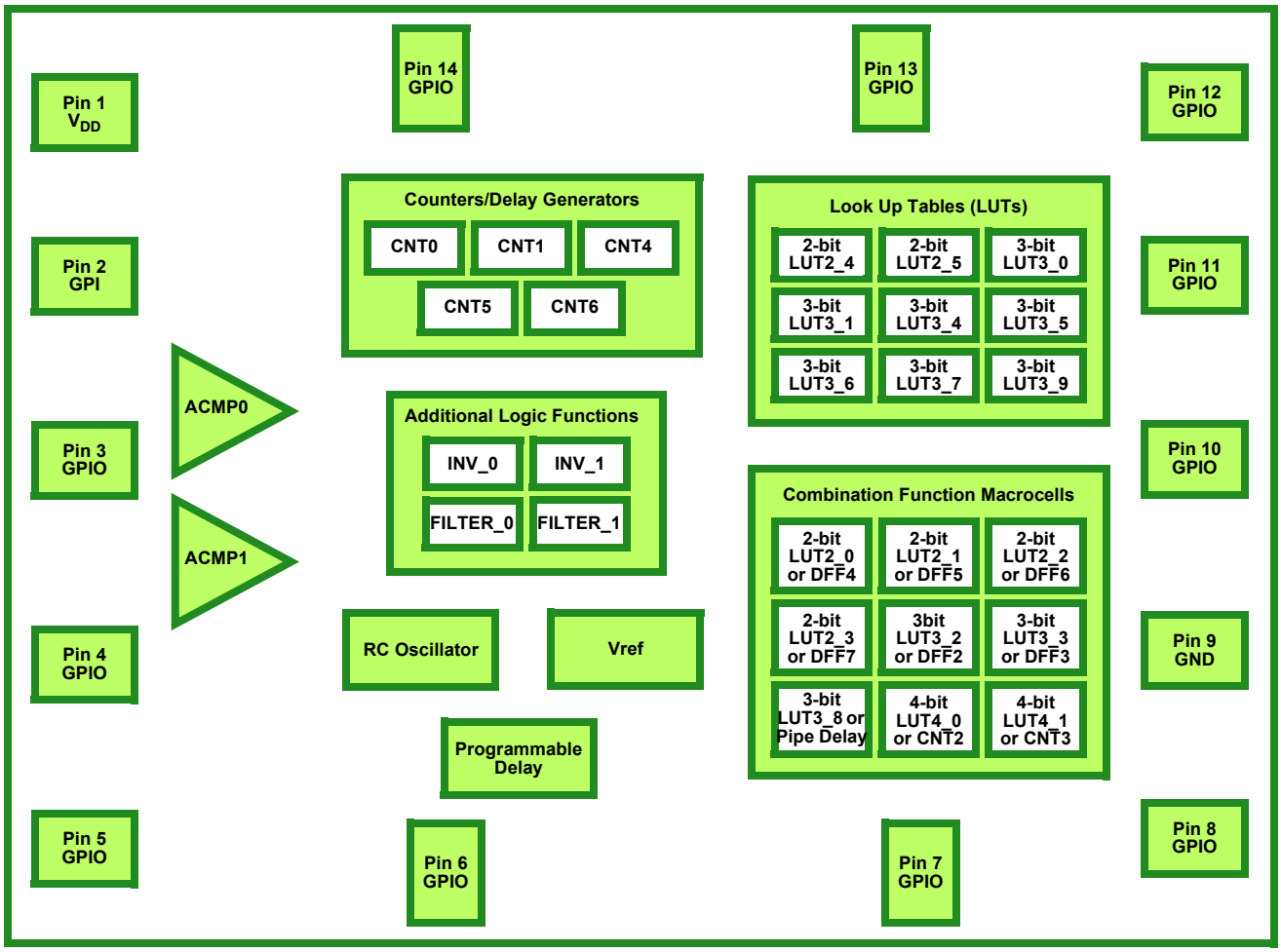
- Personal Computers and Servers
- PC Peripherals
- Consumer Electronics
- Data Communications Equipment
- Handheld and Portable Electronics

Pin Configuration



14-pin STQFN
(Top View)

Block Diagram



1.0 Overview

The SLG46169 provides a small, low power component for commonly used mixed-signal functions. The user creates their circuit design by programming the one time Non-Volatile Memory (NVM) to configure the interconnect logic, the I/O Pins and the macrocells of the SLG46169. This highly versatile device allows a wide variety of mixed-signal functions to be designed within a very small, low power single integrated circuit. The macrocells in the device include the following:

- Two Analog Comparators (ACMP)
- Two Voltage References (Vref)
- Nine Combinatorial Look Up Tables (LUTs)
  - Two 2-bit LUTs
  - Seven 3-bit LUTs
- Nine Combination Function Macrocells
  - Four Selectable DFF/Latch or 2-bit LUTs
  - Two Selectable DFF/Latch or 3-bit LUTs
  - One Selectable Pipe Delay or 3-bit LUT
  - Two Selectable CNT/DLY or 4-bit LUTs
- Five Counter / Delay Generators (CNT/DLY)
  - One 14-bit delay/counter
  - One 14-bit delay/counter with external clock/reset
  - Three 8-bit delays/counters
- Pipe Delay – 16 stage/3 output (Part of Combination Function Macrocell)
- Programmable Delay
- Additional Logic Functions – 2 Inverters / 2 Deglitch Filters
- RC Oscillator (RC OSC)

2.0 Pin Description

2.1 Functional and Programming Pin Description

Pin #	Pin Name	Function	Programming Function
1	V_{DD}	Power Supply	Power Supply
2	GPI	General Purpose Input	V_{PP} (Programming Voltage)
3	GPIO	General Purpose I/O	N/A
4	GPIO	General Purpose I/O with OE	N/A
5	GPIO	General Purpose I/O or Analog Comparator 0 (+)	N/A
6	GPIO	General Purpose I/O with OE or Analog Comparator 0 (-)	N/A
7	GPIO	General Purpose I/O with OE	N/A
8	GPIO	General Purpose I/O or Analog Comparator 1 (+)	N/A
9	GND	Ground	Ground
10	GPIO	General Purpose I/O with OE	Programming Mode Control
11	GPIO	General Purpose I/O	Programming ID Pin
12	GPIO	General Purpose I/O with OE	Programming SDIO Pin
13	GPIO	General Purpose I/O with OE and Vref output (VREF)	Programming SRDWB Pin
14	GPIO	General Purpose I/O or External Clock Input	Programming SCL Pin

3.0 User Programmability

Non-volatile memory (NVM) is used to configure the SLG46169's connection matrix routing and macrocells. The NVM is One-Time-Programmable (OTP). However, Renesas Electronics Corporation's GreenPAK development tools can be used to configure the connection matrix and macrocells, without programming the NVM, to allow on-chip emulation. This configuration will remain active on the device as long as it remains powered and can be re-written as needed to facilitate rapid design changes.

When a design is ready for in-circuit testing, the same GreenPAK development tools can be used to program the NVM and create samples for small quantity builds. Once the NVM is programmed, the device will retain this configuration for the duration of its lifetime.

Once the design is finalized, the design file can be forwarded to Renesas Electronics Corporation to integrate into the production process.

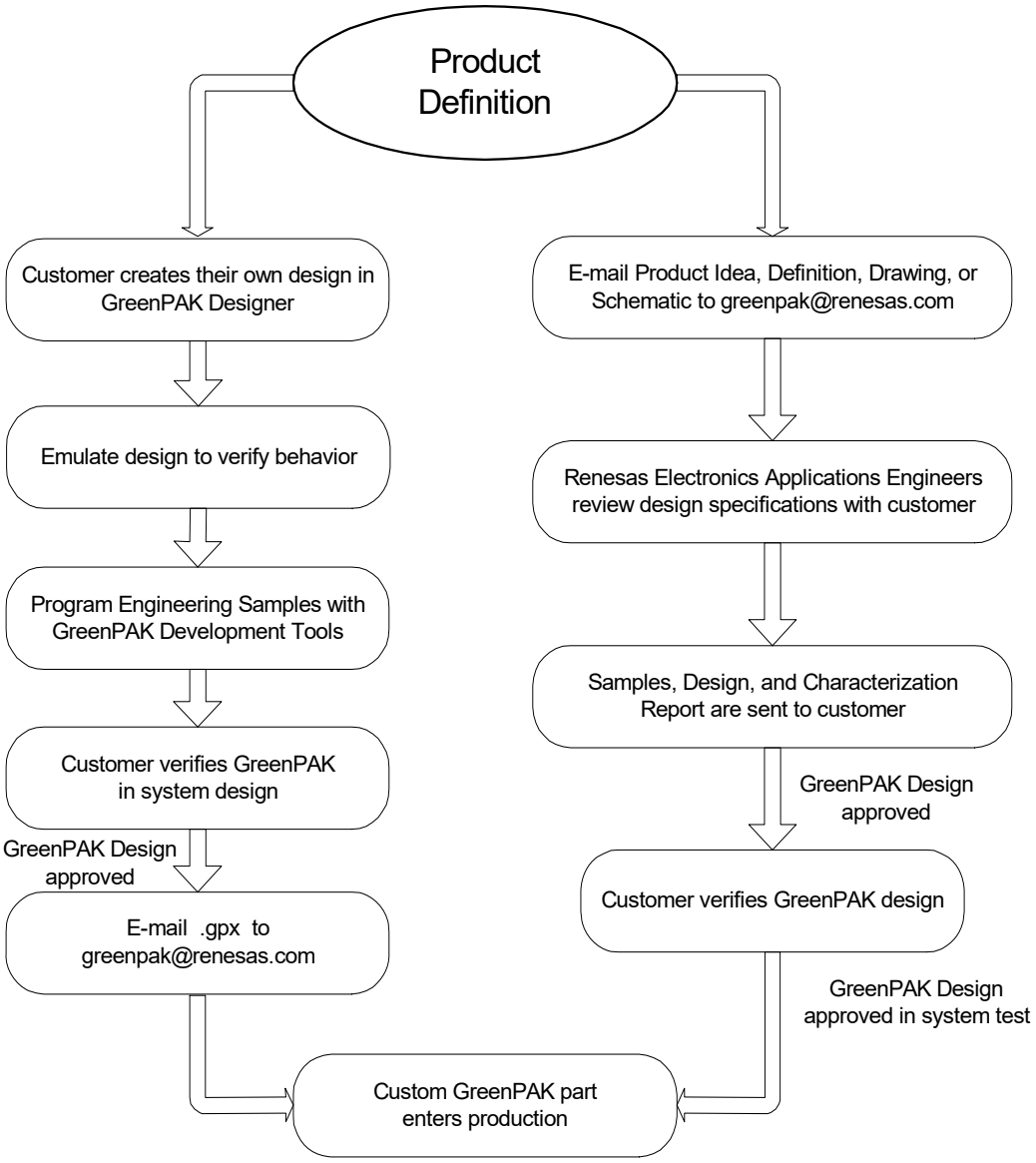


Figure 1. Steps to create a custom Renesas Electronics Corporation GreenPAK device

4.0 Ordering Information

Part Number	Type
SLG46169V	14-pin STQFN
SLG46169VTR	14-pin STQFN - Tape and Reel (3k units)

Note 1: Use SLG46169V to order. Shipments are automatically in Tape and Reel.

Note 2: "TR" suffix is no longer used. It is a legacy naming convention shown here only for informational purposes.

5.0 Electrical Specifications

5.1 Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
Supply Voltage on V_{DD} relative to GND		-0.5	7	V
DC Input Voltage		GND - 0.5	V_{DD} + 0.5	V
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	8	mA
	Push-Pull 2x	--	10	
	OD 1x	--	8	
	OD 2x	--	12	
	OD 4x	--	25	
Current at Input Pin		-1.0	1.0	mA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

5.2 Electrical Characteristics (1.8 V ±5 % V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.71	1.80	1.89	V
T_A	Operating Temperature		-40	25	85	°C
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.1	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.100	--	--	V
		Logic Input with Schmitt Trigger	1.270	--	--	V
		Low-Level Logic Input	0.980	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	0.690	V
		Logic Input with Schmitt Trigger	--	--	0.440	V
		Low-Level Logic Input	--	--	0.520	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, Open Drain PMOS 1X, I_{OH} = 100 µA	1.690	1.789	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 100 µA	1.700	1.794	--	V

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 100 µA	--	0.008	0.030	V
		Push-Pull 2X, I_{OL}= 100 µA	--	0.004	0.010	V
		Open Drain NMOS 1X, I_{OL}= 100 µA	--	0.005	0.020	V
		Open Drain NMOS 2X, I_{OL}= 100 µA	--	0.003	0.010	V
		Open Drain NMOS 4X, I_{OL}= 100 µA	--	0.003	0.004	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, $V_{OH} = V_{DD}$ - 0.2 V	1.066	1.703	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, $V_{OH} = V_{DD}$ - 0.2 V	2.216	3.406	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.15 V	0.917	1.689	--	mA
		Push-Pull 2X, V_{OL} = 0.15 V	1.834	3.378	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.15 V	1.375	2.534	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.15 V	2.750	5.068	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.15 V	5.500	10.136	--	mA
I_{VDD}	Maximum Average or DC Current Through V_{DD} Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	84	mA
		T_J = 110 °C	--	--	40	mA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: $V_{IN} = V_{DD}$	--	1	--	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: $V_{IN} = V_{DD}$	--	100	--	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: $V_{IN} = V_{DD}$	--	10	--	kΩ
C_{VDD}	Decoupling Capacitor	Capacitor Value at V_{DD}	--	0.1	--	µF

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.3 Electrical Characteristics (3.3 V ±10 % V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
T_A	Operating Temperature		-40	25	85	°C
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	1.780	--	--	V
		Logic Input with Schmitt Trigger	2.130	--	--	V
		Low-Level Logic Input	1.130	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.210	V
		Logic Input with Schmitt Trigger	--	--	0.950	V
		Low-Level Logic Input	--	--	0.690	V
I_{LKG}	Input Leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 3 mA	2.735	3.120	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 3 mA	2.870	3.210	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 3 mA	--	0.130	0.228	V
		Push-Pull 2X, I_{OL}= 3 mA	--	0.060	0.108	V
		Open Drain NMOS 1X, I_{OL}= 3 mA	--	0.080	0.147	V
		Open Drain NMOS 2X, I_{OL}= 3 mA	--	0.040	0.080	V
		Open Drain NMOS 4X, I_{OL}= 3 mA	--	0.027	0.034	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	6.045	12.080	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	11.522	24.160	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	4.875	8.244	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	9.750	16.488	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	7.313	12.370	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	14.541	24.740	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.4 V	25.801	49.480	--	mA
I_{VDD}	Maximum Average or DC Current Through V_{DD} Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	84	mA
		T_J = 110 °C	--	--	40	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{VDD}	Decoupling Capacitor	Capacitor Value at V_{DD}	--	0.1	--	μF

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.4 Electrical Characteristics (5 V ±10 % V_{DD})

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5.0	5.5	V
T_A	Operating Temperature		-40	25	85	°C
V_{ACMP}	ACMP Input Voltage Range	Positive Input	0	--	V_{DD}	V
		Negative Input	0	--	1.2	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	2.640	--	--	V
		Logic Input with Schmitt Trigger	3.160	--	--	V
		Low-Level Logic Input	1.230	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input	--	--	1.840	V
		Logic Input with Schmitt Trigger	--	--	1.510	V
		Low-Level Logic Input	--	--	0.780	V
I_{LGK}	Input leakage (Absolute Value)		--	1	1000	nA
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X,Open Drain PMOS 1X, I_{OH} = 5 mA	4.190	4.780	--	V
		Push-Pull 2X, Open Drain PMOS 2X, I_{OH} = 5 mA	4.320	4.890	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}= 5 mA	--	0.157	0.270	V
		Push-Pull 2X, I_{OL}= 5 mA	--	0.076	0.130	V
		Open Drain NMOS 1X, I_{OL}= 5 mA	--	0.102	0.180	V
		Open Drain NMOS 2X, I_{OL}= 5 mA	--	0.051	0.110	V
		Open Drain NMOS 4X, I_{OL}= 5 mA	--	0.035	0.045	V
I_{OH}	HIGH-Level Output Current (see Note 1)	Push-Pull 1X, Open Drain PMOS 1X, V_{OH} = 2.4 V	22.080	34.040	--	mA
		Push-Pull 2X, Open Drain PMOS 2X, V_{OH} = 2.4 V	41.690	68.080	--	mA
I_{OL}	LOW-Level Output Current (see Note 1)	Push-Pull 1X, V_{OL} = 0.4 V	7.215	11.580	--	mA
		Push-Pull 2X, V_{OL} = 0.4 V	13.831	23.160	--	mA
		Open Drain NMOS 1X, V_{OL} = 0.4 V	10.820	17.380	--	mA
		Open Drain NMOS 2X, V_{OL} = 0.4 V	17.343	34.760	--	mA
		Open Drain NMOS 4X Drive, V_{OL} = 0.4 V	30.964	69.520	--	mA
I_{VDD}	Maximum Average or DC Current Through V_{DD} Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	45	mA
		T_J = 110 °C	--	--	22	mA
I_{GND}	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T_J = 85 °C	--	--	84	mA
		T_J = 110 °C	--	--	40	mA

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	V_{DD}+0.3	V
T_{SU}	Startup Time	From V_{DD} rising past PON_{THR}	--	0.3	--	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.180	1.353	1.516	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.730	0.914	1.103	V
R_{PULL}	Pull Up or Pull Down Resistance	1 M for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	1	--	MΩ
		100 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	100	--	kΩ
		10 k for Pull Up: V_{IN} = GND; for Pull Down: V_{IN} = V_{DD}	--	10	--	kΩ
C_{VDD}	Decoupling Capacitor	Capacitor Value at V_{DD}	--	0.1	--	μF

Note 1: DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
Note 2: The GreenPAK's power rails are divided in two sides. Pins 2, 3, 4, 5, 6, 7 and 8 are connected to one side, pins 10, 11, 12, 13 and 14 to another.

5.5 IDD Estimator

Table 1. Typical Current estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
I	Current	Chip Quiescent	0.29	0.54	0.84	µA
		Vref	64	78	75	µA
		Vref Buffer (each)	0.5	12	12	µA
		OSC 25 kHz, predivide = 1	3.4	5.1	7	µA
		OSC 2 MHz, predivide = 1	44	85	135	µA
		OSC 2 MHz, predivide = 8	23	33	41	µA
		1x push-pull + 4 pF @ 25 kHz	0.4	5	16	µA
		1x push-pull + 4 pF @ 2 MHz	22	47	106	µA
		1st ACMP used (includes Vref)	73	86	81	µA
		Each additional ACMP add	3.7	4.1	4.8	µA

5.6 Timing Estimator

Table 2. Typical Delay estimated for each macrocell

Symbol	Parameter	Note	V_{DD} = 1.8 V		V_{DD} = 3.3 V		V_{DD} = 5.0 V		Unit
			rising	falling	rising	falling	rising	falling	
tpd	Delay	Digital input to PP 1X	42	45	17	19	12	13	ns
tpd	Delay	Digital Input with Schmitt Trigger to PP 1X	42	43	16	17	18	12	ns
tpd	Delay	Low Voltage Digital input to PP 1X	45	428	17	177	12	120	ns
tpd	Delay	Digital input to PMOS	42	-	17	-	12	-	ns
tpd	Delay	Digital input to NMOS	-	80	-	27	-	18	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 1	53	-	21	-	15	-	ns
tpd	Delay	Output enable from pin, OE Hi-Z to 0	50	-	20	-	14	-	ns
tpd	Delay	LUT2bit(LATCH)	34	33	14	13	10	9	ns
tpd	Delay	LATCH(LUT2bit)	30	34	14	13	10	9	ns
tpd	Delay	LUT3bit(LATCH)	38	37	18	15	13	10	ns
tpd	Delay	LATCH+nRESET(LUT3bit)	45	42	21	17	15	12	ns
tpd	Delay	LUT4bit	28	33	14	13	10	9	ns
tpd	Delay	LUT2bt	19	26	10	10	7	7	ns
tpd	Delay	LUT3bit	28	34	14	13	10	9	ns
tpd	Delay	CNT/DLY	40	38	18	15	13	11	ns
tpd	Delay	P_DLY1C	380	377	166	163	123	120	ns
tpd	Delay	P_DLY2C	720	718	314	312	233	231	ns
tpd	Delay	P_DLY3C	1061	1060	462	460	343	341	ns
tpd	Delay	P_DLY4C	1396	1400	609	609	451	451	ns
tpd	Delay	Filter	200	200	78	78	53	53	ns
tpd	Delay	ACMP (5mV across inputs)	3000	3000	2000	2000	2000	2000	ns
tw	width	I/O with 1X push pull (min transmitted)	20	20	20	20	20	20	ns
tw	width	filter (min transmitted)	150	150	55	55	35	35	ns

5.7 Typical Counter/Delay Offset Measurements

Table 3. Typical Counter/Delay Offset Measurements

Parameter	RC OSC Freq	RC OSC Power	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
offset	25 kHz	auto	19	14	12	µs
offset	2 MHz	auto	7	4	4	µs
frequency settling time	25 kHz	auto	19	14	12	µs
frequency settling time	2 MHz	auto	14	14	14	µs
variable (CLK period)	25 kHz	forced	0-40	0-40	0-40	µs
variable (CLK period)	2 MHz	forced	0-0.5	0-0.5	0-0.5	µs
tpd (non-delayed edge)	25 kHz/ 2 MHz	either	35	14	10	ns

5.8 Expected Delays and Widths

Table 4. Expected Delays and Widths for Programmable Delay (typical)

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time1	Width, 1 cell	mode:(any)edge detect, edge detect output	325	150	110	ns
time1	Width, 2 cell	mode:(any)edge detect, edge detect output	740	300	225	ns
time1	Width, 3 cell	mode:(any)edge detect, edge detect output	1020	450	340	ns
time1	Width, 4 cell	mode:(any)edge detect, edge detect output	1350	600	450	ns
time2	Delay, 1 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 2 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 3 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time2	Delay, 4 cell	mode:(any)edge detect, edge detect output	44	18	14	ns
time1	Width, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	340	150	110	ns
time1	Width, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	670	300	220	ns
time1	Width, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	1000	450	335	ns
time1	Width, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	1340	600	450	ns
time2	Delay, 1 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 2 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 3 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 4 cell	mode: delayed (any)edge detect, delayed edge detect output	570	220	140	ns
time2	Delay, 1 cell	mode: both edge delay, edge detect output	382	375	126	ns
time2	Delay, 2 cell	mode: both edge delay, edge detect output	713	169	237	ns
time2	Delay, 3 cell	mode: both edge delay, edge detect output	1045	318	350	ns
time2	Delay, 4 cell	mode: both edge delay, edge detect output	1370	466	460	ns
time2	Delay, 1 cell	mode: both edge delay, delayed edge detect output	900	613	250	ns
time2	Delay, 2 cell	mode: both edge delay, delayed edge detect output	1250	520	360	ns

Table 4. Expected Delays and Widths for Programmable Delay (typical)

Symbol	Parameter	Note	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
time2	Delay, 3 cell	mode: both edge delay, delayed edge detect output	1600	680	480	ns
time2	Delay, 4 cell	mode: both edge delay, delayed edge detect output	1900	815	600	ns

5.9 Typical Pulse Width Performance

Table 5. Typical Pulse Width Performance

Parameter	V_{DD} = 1.8 V	V_{DD} = 3.3 V	V_{DD} = 5.0 V	Unit
Filtered Pulse Width for Filter 0 and Filter 1	< 150	< 55	< 35	ns

5.10 OSC Specifications

Table 6. 25 kHz RC OSC frequency limits

Power Supply Range (V_{DD}) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Minimum Value, kHz	Maximum Value, kHz	Minimum Value, kHz	Maximum Value, kHz
1.8 V ±5 %	24.044	25.969	19.924	29.122
3.3 V ±10 %	24.395	25.609	20.383	28.363
5 V ±10 %	24.297	25.702	20.371	28.337
2.5 V ... 4.5 V	24.163	25.873	20.288	28.397
1.71 V… 5.5 V	23.506	28.006	19.381	29.378

Table 7. 25 kHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (V_{DD}) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-3.82 %	3.88 %	-20.30 %	16.49 %
3.3 V ±10 %	-2.42 %	2.44 %	-18.47 %	13.45 %
5 V ±10 %	-2.81 %	2.81 %	-18.52 %	13.35 %
2.5 V ... 4.5 V	-3.35 %	3.49 %	-18.85 %	13.58 %
1.71 V… 5.5 V	-5.98 %	12.02 %	-22.48 %	17.51 %

5.10.1 2 MHz RC Oscillator

Table 8. 2 MHz RC OSC frequency limits

Power Supply Range (V_{DD}) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Minimum Value, MHz	Maximum Value, MHz	Minimum Value, MHz	Maximum Value, MHz
1.8 V ±5 %	1.855	2.137	1.583	2.395
3.3 V ±10 %	1.903	2.097	1.557	2.350
5 V ±10 %	1.892	2.106	1.550	2.347
2.5 V ... 4.5 V	1.879	2.125	1.541	2.372
1.71 V… 5.5 V	1.754	2.197	1.450	2.541

Table 9. 2 MHz RC OSC frequency error (error calculated relative to nominal value)

Power Supply Range (V_{DD}) V	Temperature Range			
	+25 °C		-40 °C ... +85 °C	
	Error (% at Minimum)	Error (% at Maximum)	Error (% at Minimum)	Error (% at Maximum)
1.8 V ±5 %	-7.26 %	6.85 %	-20.83 %	19.73 %
3.3 V ±10 %	-4.85 %	4.83 %	-22.15 %	17.49 %
5 V ±10 %	-5.38 %	5.30 %	-22.49 %	17.33 %
2.5 V ... 4.5 V	-6.07 %	6.27 %	-22.96 %	18.59 %
1.71 V… 5.5 V	-12.28 %	9.84 %	-27.52 %	27.07 %

5.10.2 OSC Power On delay

Table 10. Oscillators Power On delay at T=(-40..+85) °C, DLY/CNT Counter data = 100; RC OSC power setting: "Auto Power On"

Power Supply Range (V_{DD}) V	RC OSC 2 MHz		RC OSC 25 kHz	
	Typical Value, µs	Maximum Value, µs	Typical Value, µs	Maximum Value, µs
1.71	8.80	12.78	19.34	24.22
1.80	8.26	12.07	18.80	24.37
1.89	7.76	11.47	18.28	23.99
2.50	5.76	8.57	15.45	19.91
2.70	5.42	7.86	14.64	18.85
3.00	5.10	7.24	13.58	17.80
3.30	4.90	7.14	12.52	16.96
3.60	4.79	7.22	11.36	16.20
4.20	4.69	7.33	9.58	12.69
4.50	4.66	7.22	8.83	11.51
5.00	4.60	7.12	7.69	9.79
5.50	4.54	7.00	6.75	8.45

5.11 ACMP Specifications

Table 11. ACMP Specifications

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
V_{ACMP}	ACMP Input Voltage Range	Positive Input	V_{DD} = 1.8 V ± 5 %	0	--	V_{DD}	V
		Negative Input		0	--	1.1	V
		Positive Input	V_{DD} = 3.3 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
		Positive Input	V_{DD} = 5.0 V ± 10 %	0	--	V_{DD}	V
		Negative Input		0	--	1.2	V
V_{offset}	ACMP Input Offset Voltage	Low Bandwidth - Enable, Vhys = 0 mV, Gain = 1, Vref = 1000 mV, V_{DD} = (1.71..5.5) V	T = 25 °C	-6.2	--	7.5	mV
			T = (-40..85) °C	-14.1	--	15.2	mV
		Low Bandwidth - Disable, Vhys = 0 mV, Gain =1, Vref = 1000 mV, V_{DD} = (1.71..5.5) V	T = 25 °C	-6.5	--	7.5	mV
			T = (-40..85) °C	-8.3	--	10.1	mV
$V_{boffset}$	ACMP Buffer Input Offset Voltage	V_{DD} = (1.71..5.5) V	T = 25 °C	-28.2	--	16.3	mV
t_{start}	ACMP Start Time	Hysteresis: disable; Low bandwidth: disable; IN+ Gain: disable; IN+ source: PIN4 (Pull Up 10k); IN- source: 50 mV	T = 25 °C V_{DD} = (1.71..5.5) V	--	47.1	101.5	µS
			T = (-40..85) °C V_{DD} = (1.71..5.5) V	--	47.0	113.3	µS
V_{HYS}	Built-in Hysteresis	V_{HYS} = 25 mV $V_{IL} = V_{IN} - V_{HYS}/2$ $V_{IH} = V_{IN} + V_{HYS}/2$	LB - Enabled, T = 25 °C	0.0	--	33.1	mV
			LB - Disabled, T = 25 °C	0.0	--	35.4	mV
		V_{HYS} = 50 mV $V_{IL} = V_{IN} - V_{HYS}/2$ $V_{IH} = V_{IN} + V_{HYS}/2$	LB - Enabled, T = 25 °C	7.1	--	51.7	mV
			LB - Disabled, T = 25 °C	9.8	--	60.4	mV
		V_{HYS} = 200 mV $V_{IL} = V_{IN} - V_{HYS}/2$ $V_{IH} = V_{IN} + V_{HYS}/2$	LB - Enabled, T = 25 °C	77.5	--	228.4	mV
			LB - Disabled, T = 25 °C	91.2	--	223.5	mV
		V_{HYS} = 25 mV $V_{IL} = V_{IN} - V_{HYS}/2$ $V_{IH} = V_{IN} + V_{HYS}/2$	LB - Enabled, T = (-40…+85) °C	0.0	--	46.7	mV
			LB - Disabled, T = (-40…+85) °C	0.0	--	46.5	mV
		V_{HYS} = 50 mV $V_{IL} = V_{IN} - V_{HYS}/2$ $V_{IH} = V_{IN} + V_{HYS}/2$	LB - Enabled, T = (-40…+85) °C	0.0	--	160.2	mV
			LB - Disabled, T = (-40…+85) °C	0.0	--	121.5	mV
		V_{HYS} = 200 mV $V_{IL} = V_{IN} - V_{HYS}/2$ $V_{IH} = V_{IN} + V_{HYS}/2$	LB - Enabled, T = (-40…+85) °C	24.2	--	261.1	mV
			LB - Disabled, T = (-40…+85) °C	25.0	--	325.3	mV

Symbol	Parameter	Description/Note	Conditions	Min.	Typ.	Max.	Unit
R_{sin}	Series Input Resistance	Gain = 1x		--	100.0	--	MΩ
		Gain = 0.5x		--	1.0	--	MΩ
		Gain = 0.33x		--	0.8	--	MΩ
		Gain = 0.25x		--	1.0	--	MΩ
PROP	Propagation Delay, Response Time	Low Bandwidth - Disable, Gain = 1, V_{DD}=(1.71..3.3) V, Overdrive=2 mV	Low to High, T = 25 °C	--	2.87	5.69	µS
			High to Low, T = 25 °C	--	2.79	5.12	µS
G	Gain error (including threshold and internal Vref error), T = (-40…+85) °C	G = 1, V_{DD} = (1.71..5.5) V	Vref = (50…1200) mV	--	1	--	
		G = 0.5, V_{DD} = (1.71..5.5) V		-1.25 %	--	0.95 %	
		G = 0.33, V_{DD} = (1.71..5.5) V		-1.79 %	--	1.39 %	
		G = 0.25, V_{DD} = (1.71..5.5) V		-2.18 %	--	1.57 %	
Vref	Internal Vref error, Vref = (50...1200) mV	V_{DD} = (1.71..5.5) V	T = 25 °C	-1.91 %	--	1.79 %	
			T = (-40…+85) °C	-7.87 %	--	5.58 %	

6.0 Summary of Macrocell Function

6.1 I/O Pins

- Digital Input (low voltage or normal voltage, with or without Schmitt Trigger)
- Open Drain Outputs
- Push Pull Outputs
- Analog I/O
- 10 kΩ/100 kΩ/1 MΩ pull-up/pull-down resistors
- 40 mA Open Drain 4X Drive output

6.2 Connection Matrix

- Digital matrix for circuit connections based on user design

6.3 Analog Comparators (2 total)

- Selectable hysteresis 0 mV/25 mV/50 mV/200 mV
- Bandwidth control
- Selectable gain

6.4 Voltage Reference

- Used for references on Analog Comparators
- Can also be driven to external pins

6.5 Combinational Logic Look Up Tables (LUTs – 9 total)

- Two 2-bit Lookup Tables
- Seven 3-bit Lookup Tables

6.6 Combination Function Macrocells (9 total)

- Four Selectable DFF/Latch or 2-bit LUTs
- Two Selectable DFF/Latch or 3-bit LUTs
- One Selectable Pipe Delay or 3-bit LUT
- Two Selectable CNT/DLY or 4-bit LUTs

6.7 Delays/Counters (5 total)

- Two 14-bit delay/counters: Range 1-16384 clock cycles
- Three 8-bit delays/counters: Range 1-255 clock cycles

6.8 Pipe Delay (Part of Combination Function Macrocell)

- 16 stage / 3 output
- One 1 stage fixed output
- Two 1-16 stage selectable outputs.

6.9 Programmable Delay

- 150 ns/300 ns/450 ns /600 ns @ 3.3 V
- Includes Edge Detection function

6.10 Additional Logic Functions (4 total)

- Two Inverter macrocells
- Two Deglitch filter macrocells

6.11 RC Oscillator

- 25 kHz and 2 MHz selectable frequency
- First stage divider (4): OSC/1, OSC/2, OSC/4, and OSC/8
- Second stage divider (5): OSC/1, OSC/4, selectable (OSC/8, OSC/12, OSC/24, or OSC/64), OSC/3, and additional OSC/3 (from selectable output)

7.0 I/O Pins

The SLG46169 has a total of 12 multi-function I/O pins which can function as either a user defined Input or Output, as well as serving as a special function (such as outputting the voltage reference), or serving as a signal for programming of the on-chip Non Volatile Memory (NVM).

Normal Mode pin definitions are as follows:

- Pin 1: V_{DD} power supply
- Pin 2: general purpose input
- Pin 3: general purpose input or output
- Pin 4: general purpose input or output with OE
- Pin 5: general purpose input or output or analog comparator 0(+)
- Pin 6: general purpose input or output with OE or analog comparator 0(-)
- Pin 7: general purpose input or output with OE
- Pin 8: general purpose input or output or analog comparator 1(+)
- Pin 9: ground
- Pin 10: general purpose input or output with OE
- Pin 11: general purpose input or output
- Pin 12: general purpose input or output with OE
- Pin 13: general purpose input or output with OE and Vref output (VREF)
- Pin 14: general purpose input or output or external clock input

Programming Mode pin definitions are as follows:

- Pin1: V_{DD} power supply
- Pin 2: V_{PP} programming voltage
- Pin 9: ground
- Pin 10: programming mode control
- Pin 11: programming ID pin
- Pin 12: programming SDIO pin
- Pin 13: programming SRDWB pin
- Pin 14: programming SCL pin

Of the 12 user defined I/O pins on the SLG46169, all but one of the pins (Pin 2) can serve as both digital input and digital output. Pin 2 can only serve as a digital input pin.

7.1 Input Modes

Each I/O pin can be configured as a digital input pin with/without buffered Schmitt Trigger, or can also be configured as a low voltage digital input. Pins 5, 6 and 8 can also be configured to serve as analog inputs to the on-chip comparators. Pins 12 and 13 can also be configured as analog reference voltage outputs.

7.2 Output Modes

Pins 3, 4, 5, 6, 7, 8, 10, 11, 12, 13 and 14 can all be configured as digital output pins.

7.3 Pull Up/Down Resistors

All I/O pins have the option for user selectable resistors connected to the input structure. The selectable values on these resistors are 10 kΩ, 100 kΩ and 1 MΩ. In the case of Pin 2, the resistors are fixed to a pull-down configuration. In the case of all other I/O pins, the internal resistors can be configured as either pull-up or pull-downs.

7.4 I/O Register Settings

7.4.1 PIN 2 Register Settings

Table 12. PIN 2 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 2 Mode Control	<830:829>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 2 Pull Down Resistor Value Selection	<832:831>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor

7.4.2 PIN 3 Register Settings

Table 13. PIN 3 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 3 Mode Control	<842:840>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
PIN 3 Pull Up/Down Resistor Value Selection	<844:843>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 3 Pull Up/Down Resistor Selection	<845>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 3 Driver Strength Selection	<846>	0: 1X 1: 2X

7.4.3 PIN 4 Register Settings

Table 14. PIN 4 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 4 Mode Control (sig_pin4_oe =0)	<848:847>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 4 Mode Control (sig_pin4_oe =1)	<850:849>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 4 Pull Up/Down Resistor Value Selection	<852:851>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 4 Pull Up/Down Resistor Selection	<853>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.4 PIN 5 Register Settings

Table 15. PIN 5 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 5 Mode Control	<856:854>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
PIN 5 Pull Up/Down Resistor Value Selection	<858:857>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 5 Pull Up/Down Resistor Selection	<859>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 5 Driver Strength Selection	<860>	0: 1X 1: 2X

7.4.5 PIN 6 Register Settings

Table 16. PIN 6 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 6 Mode Control (sig_pin6_oe =0)	<862:861>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
PIN 6 Mode Control (sig_pin6_oe =1)	<864:863>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 6 Pull Up/Down Resistor Value Selection	<866:865>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 6 Pull Up/Down Resistor Selection	<867>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.6 PIN 7 Register Settings

Table 17. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Mode Control (sig_pin7_oe =0)	<876:875>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 7 Mode Control (sig_pin7_oe =1)	<878:877>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

Table 17. PIN 7 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 7 Pull Up/Down Resistor Value Selection	<880:879>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 7 Pull Up/Down Resistor Selection	<881>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.7 PIN 8 Register Settings

Table 18. PIN 8 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 8 Mode Control	<884:882>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
PIN 8 Pull Up/Down Resistor Value Selection	<886:885>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 8 Pull Up/Down Resistor Selection	<887>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 8 Driver Strength Selection	<888>	0: 1X 1: 2X
PIN 8 4X Drive (4X, NMOS Open Drain) Selection	<889>	0: 4X Drive Off 1: 4X Drive On (if <884:882> = '101')

7.4.8 PIN 10 Register Settings

Table 19. PIN 10 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 10 Mode Control (sig_pin10_oe =0)	<920:919>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
PIN 10 Mode Control (sig_pin10_oe =1)	<922:921>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 10 Pull Up/Down Resistor Value Selection	<924:923>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 10 Pull Up/Down Resistor Selection	<925>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.9 PIN 11 Register Settings

Table 20. PIN 11 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 11 Mode Control	<928:926>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
PIN 11 Pull Up/Down Resistor Value Selection	<930:929>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 11 Pull Up/Down Resistor Selection	<931>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 11 Driver Strength Selection	<932>	0: 1X 1: 2X

7.4.10 PIN 12 Register Settings

Table 21. PIN 12 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 12 Mode Control (sig_pin12_oe =0)	<934:933>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
PIN 12 Mode Control (sig_pin12_oe =1)	<936:935>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 12 Pull Up/Down Resistor Value Selection	<938:937>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 12 Pull Up/Down Resistor Selection	<939>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.11 PIN 13 Register Settings

Table 22. PIN 13 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 13 Mode Control (sig_pin13_oe =0)	<941:940>	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
PIN 13 Mode Control (sig_pin13_oe =1)	<943:942>	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
PIN 13 Pull Up/Down Resistor Value Selection	<945:944>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 13 Pull Up/Down Resistor Selection	<946>	0: Pull Down Resistor 1: Pull Up Resistor

7.4.12 PIN 14 Register Settings

Table 23. PIN 14 Register Settings

Signal Function	Register Bit Address	Register Definition
PIN 14 Mode Control	<949:947>	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
PIN 14 Pull Up/Down Resistor Value Selection	<951:950>	00: Floating 01: 10 kΩ Resistor 10: 100 kΩ Resistor 11: 1 MΩ Resistor
PIN 14 Pull Up/Down Resistor Selection	<952>	0: Pull Down Resistor 1: Pull Up Resistor
PIN 14 Driver Strength Selection	<953>	0: 1X 1: 2X

7.5 GPI Structure

7.5.1 GPI Structure (for Pin 2)

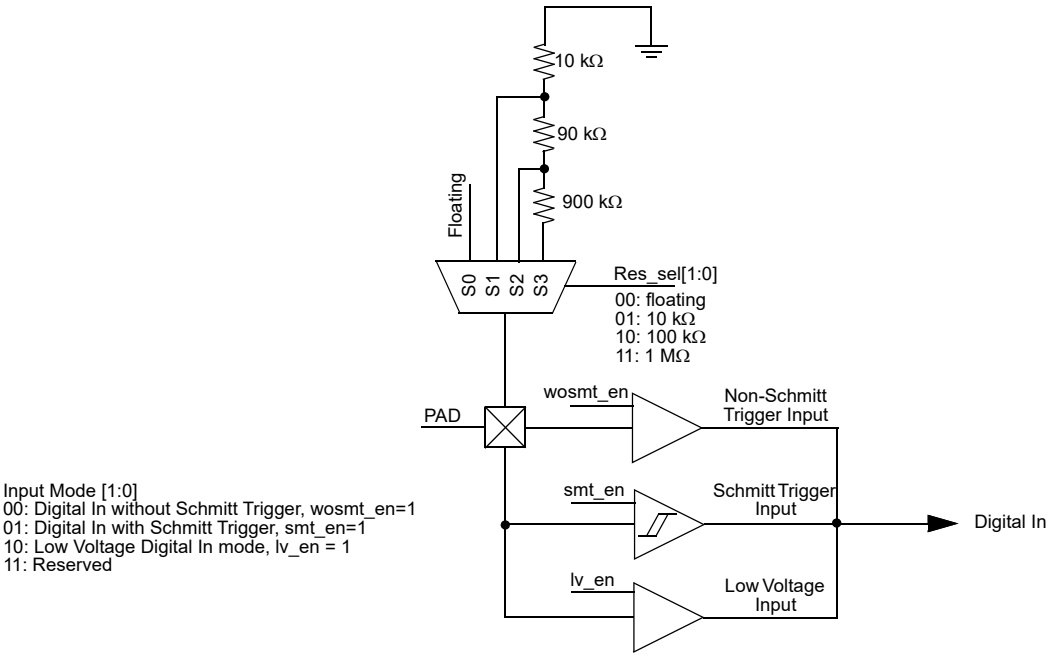


Figure 2. PIN 2 GPI Structure Diagram

7.6 Matrix OE IO Structure

7.6.1 Matrix OE IO Structure (for Pins 4, 6, 7, 10, 12, 13)

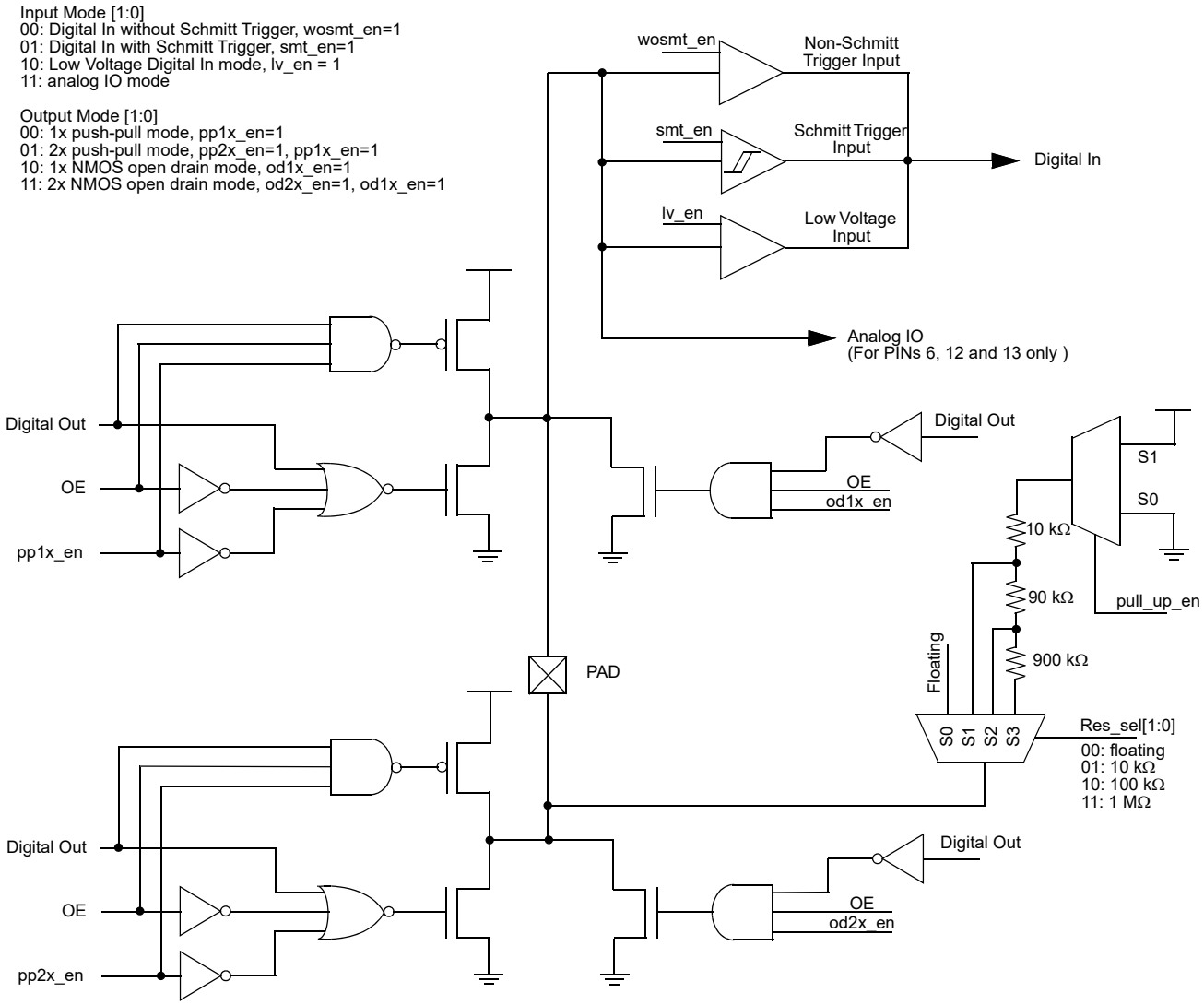


Figure 3. Matrix OE IO Structure Diagram

7.7 Register OE IO Structure

7.7.1 Register OE IO Structure (for Pins 3, 5, 11, 14)

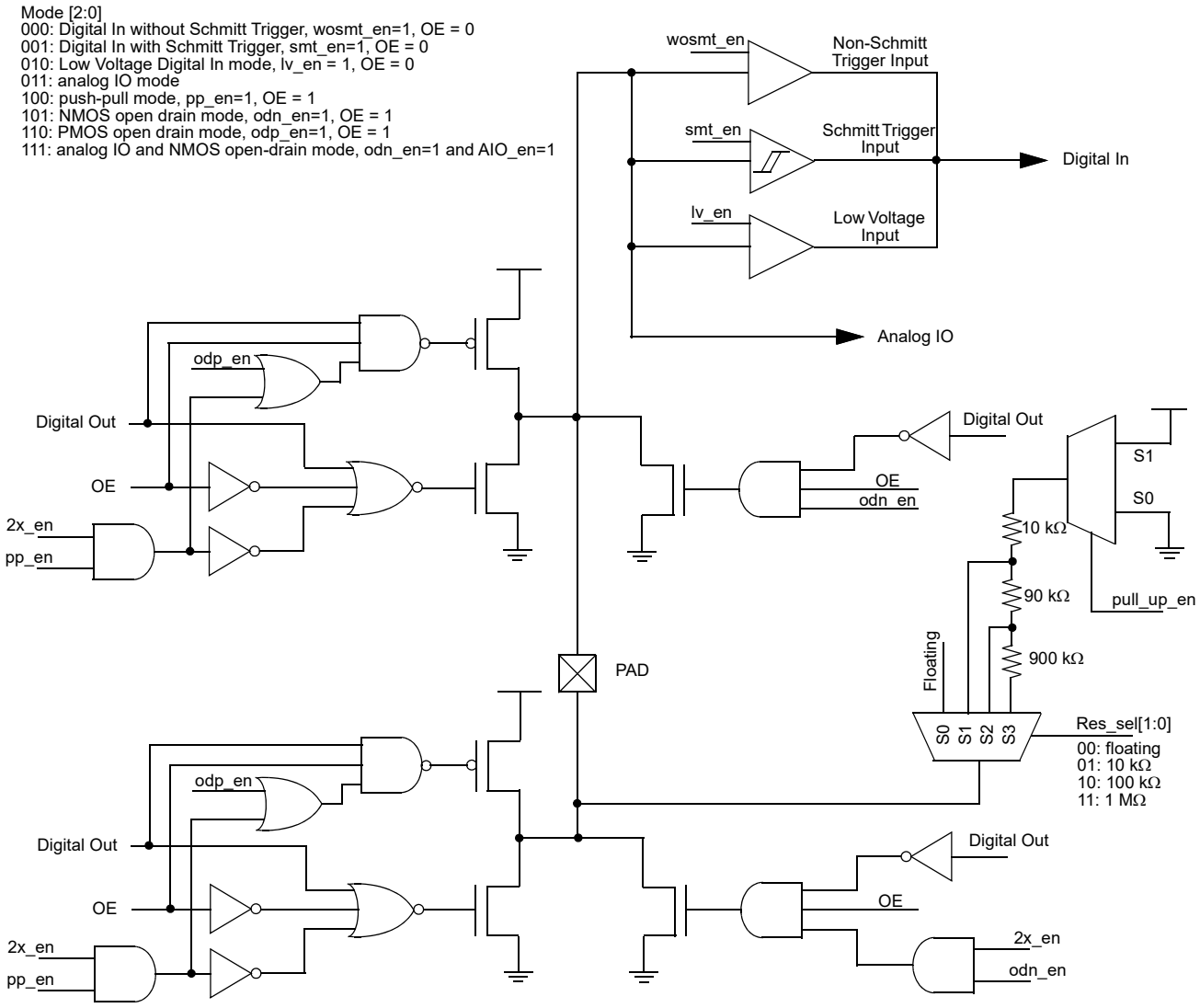


Figure 4. Register OE IO Structure Diagram

7.8 Register OE IO Structure with 4X Drive

7.8.1 Register OE IO Structure with 4X Drive (for Pin 8)

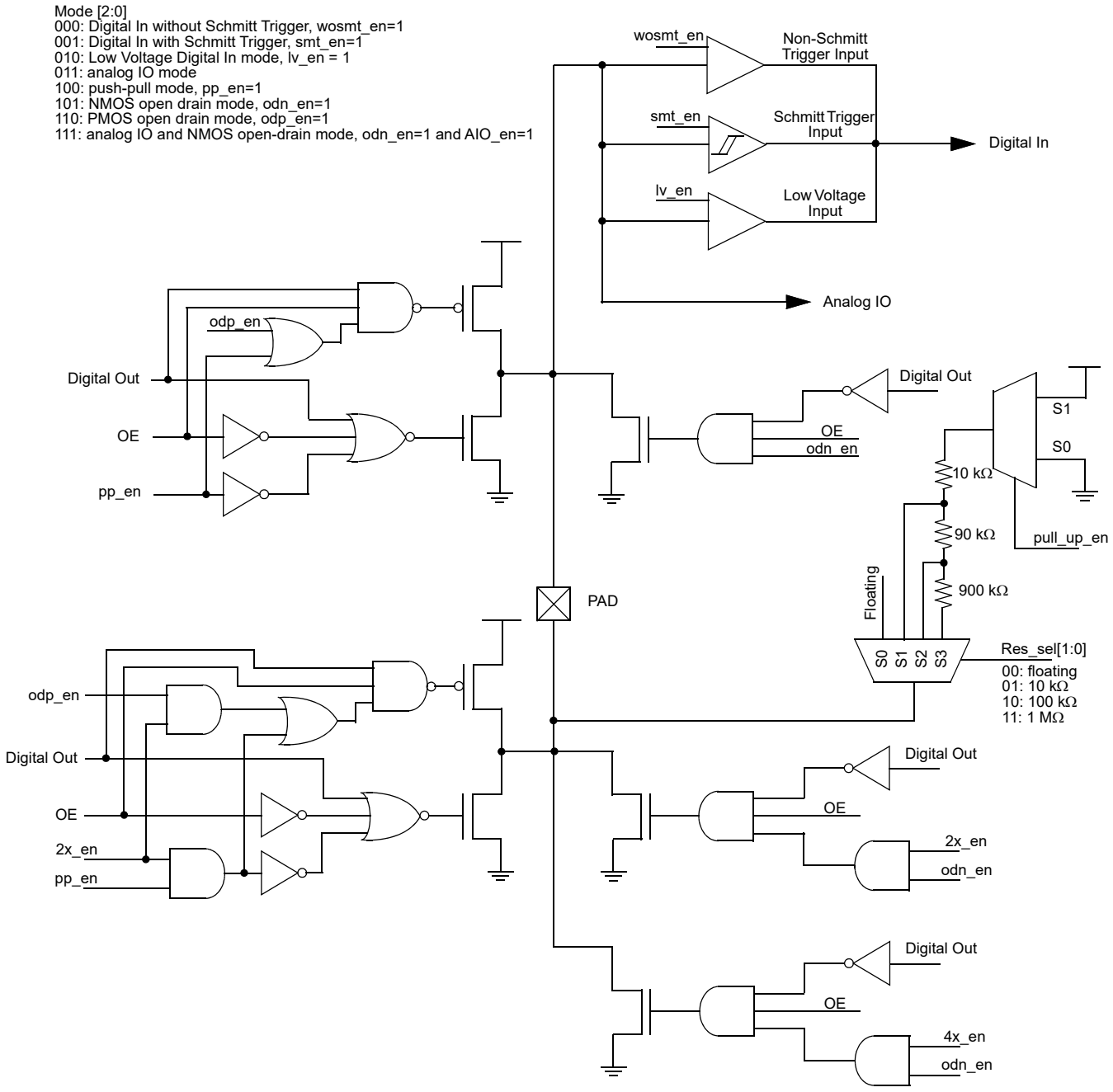


Figure 5. Register OE IO with 4X Drive Structure Diagram

8.0 Connection Matrix

The Connection Matrix in the SLG46169 is used to create the internal routing for internal functions of the device once it is programmed. The registers are programmed from the one-time NVM cell during Test Mode Operation. All of the connection point for each logic cell within the SLG46169 has a specific digital bit code assigned to it that is either set to active “High” or inactive “Low” based on the design that is created. Once the 1024 register bits within the SLG46169 are programmed a fully custom circuit will be created.

The Connection Matrix has 64 inputs and 92 outputs. Each of the 64 inputs to the Connection Matrix is hard-wired to a particular source macrocell, including I/O pins, LUTs, analog comparators, other digital resources and V_{DD} and GND. The input to a digital macrocell uses a 6-bit register to select one of these 64 input lines.

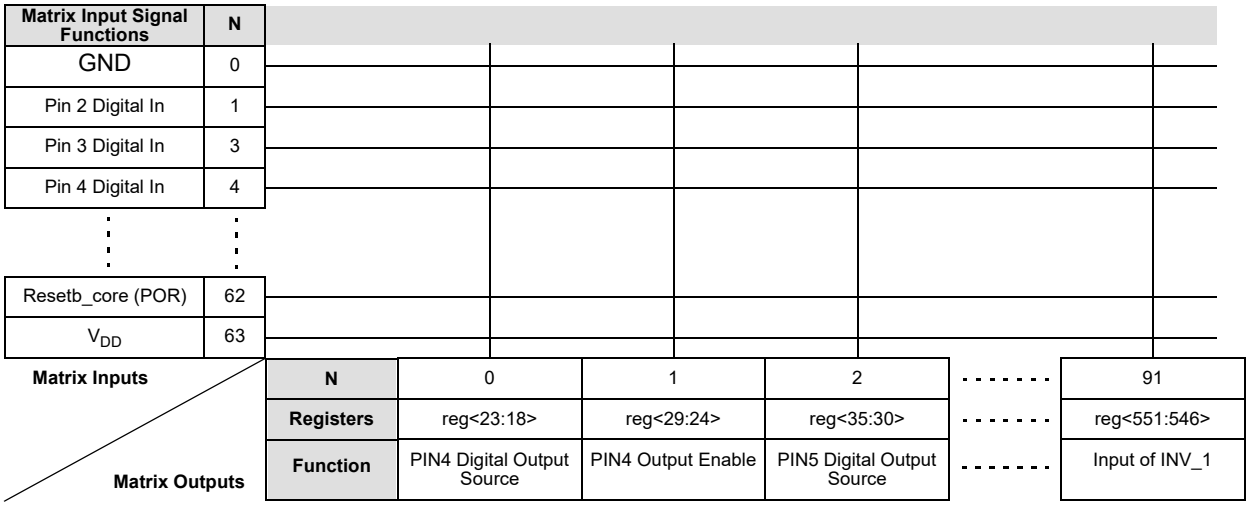


Figure 6. Connection Matrix

8.1 Matrix Input Table

Table 24. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
0	GND	0	0	0	0	0	0
1	pin2 digital input	0	0	0	0	0	1
2	Reserved	0	0	0	0	1	0
3	pin3 digital input	0	0	0	0	1	1
4	pin4 digital input	0	0	0	1	0	0
5	pin5 digital input	0	0	0	1	0	1
6	pin6 digital input	0	0	0	1	1	0
7	Reserved	0	0	0	1	1	1
8	pin7 digital input	0	0	1	0	0	0
9	pin8 digital input	0	0	1	0	0	1
10	ACMP_0 output	0	0	1	0	1	0
11	ACMP_1 output	0	0	1	0	1	1
12	Reserved	0	0	1	1	0	0
13	CNT_DLY0(14bit) output	0	0	1	1	0	1
14	CNT_DLY1(14bit with ext CK/Reset) output	0	0	1	1	1	0
15	CNT_DLY4(8 bit) output	0	0	1	1	1	1
16	CNT_DLY5(8 bit) output	0	1	0	0	0	0
17	CNT_DLY6(8 bit) output	0	1	0	0	0	1
18	Reserved	0	1	0	0	1	0
19	Inverting of DFF/LATCH_2 output	0	1	0	0	1	1
20	GND (spare)	0	1	0	1	0	0
21	Inverting of DFF/LATCH_3 output	0	1	0	1	0	1
22	LUT4_0 output (CNT_DLY2 output (8 bit w/ ext CK and reset))	0	1	0	1	1	0
23	LUT4_1 output (CNT_DLY3 output (8 bit w/ ext CK and reset))	0	1	0	1	1	1
24	LUT3_0 output	0	1	1	0	0	0
25	LUT3_1 output	0	1	1	0	0	1
26	LUT3_2 output (DFF/LATCH_2 output with nRST or nSET)	0	1	1	0	1	0
27	LUT3_3 output (DFF/LATCH_3 output with nRST or nSET)	0	1	1	0	1	1
28	LUT3_4 output	0	1	1	1	0	0
29	LUT3_5 output	0	1	1	1	0	1
30	LUT3_6 output	0	1	1	1	1	0
31	LUT3_7 output	0	1	1	1	1	1
32	LUT3_8 output(1st stage pipe 1 delay output)	1	0	0	0	0	0
33	LUT2_0 output (DFF/LATCH_4 output)	1	0	0	0	0	1
34	LUT2_1 output (DFF/LATCH_5 output)	1	0	0	0	1	0
35	LUT2_2 output (DFF/LATCH_6 output)	1	0	0	0	1	1
36	LUT2_3 output (DFF/LATCH_7 output)	1	0	0	1	0	0
37	LUT2_4 output	1	0	0	1	0	1

Table 24. Matrix Input Table

N	Matrix Input Signal Function	Matrix Decode					
		5	4	3	2	1	0
38	LUT2_5 output	1	0	0	1	1	0
39	LUT3_9 output	1	0	0	1	1	1
40	pipe1 delay output0	1	0	1	0	0	0
41	pipe1 delay output1	1	0	1	0	0	1
42	filter_0 output	1	0	1	0	1	0
43	Edge detect output	1	0	1	0	1	1
44	Programmable delay with edge detector output	1	0	1	1	0	0
45	internal oscillator output	1	0	1	1	0	1
46	internal oscillator divided by 4 output	1	0	1	1	1	0
47	internal oscillator divided by 8, 12, 24, 64 output selection	1	0	1	1	1	1
48	internal oscillator divided by 3 output	1	1	0	0	0	0
49	matrix input <47> divided by 3	1	1	0	0	0	1
50	Reserved	1	1	0	0	1	0
51	Reserved	1	1	0	0	1	1
52	Reserved	1	1	0	1	0	0
53	Reserved	1	1	0	1	0	1
54	pin10 digital input	1	1	0	1	1	0
55	pin11 digital input	1	1	0	1	1	1
56	pin12 digital input	1	1	1	0	0	0
57	pin13 digital input	1	1	1	0	0	1
58	pin14 digital input	1	1	1	0	1	0
59	out of INV_0 gate	1	1	1	0	1	1
60	out of INV_1 gate	1	1	1	1	0	0
61	filter_1 output	1	1	1	1	0	1
62	Resetb_core (POR) as matrix input	1	1	1	1	1	0
63	V_{DD}	1	1	1	1	1	1

8.2 Matrix Output Table

Table 25. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<5:0>	Reserved	0
reg<11:6>	Reserved	1
reg<17:12>	Matrix Out: PIN3 Digital Output Source	2
reg<23:18>	Matrix Out: PIN4 Digital Output Source	3
reg<29:24>	Matrix Out: Output Enable of PIN4	4
reg<35:30>	Matrix Out: PIN5 Digital Output Source	5
reg<41:36>	Matrix Out: PIN6 Digital Output Source	6
reg<47:42>	Matrix Out: Output Enable of PIN6	7
reg<53:48>	Reserved	8
reg<59:54>	Matrix Out: PIN7 Digital Output Source	9
reg<65:60>	Matrix Out: Output Enable of PIN7	10
reg<71:66>	Matrix Out: PIN8 Digital Output Source (4X Drive)	11
reg<77:72>	Matrix Out: PDB (Power Down) for ACMP0	12
reg<83:78>	Matrix Out: PDB (Power Down) for ACMP1	13
reg<89:84>	Reserved	14
reg<95:90>	Matrix Out: Input for Delay0 or Counter0 External Clock	15
reg<101:96>	Matrix Out: Input for Delay1 or Counter1 Reset Input	16
reg<107:102>	Matrix Out: Input for Counter1 External Clock or Delay1 External Clock	17
reg<113:108>	Matrix Out: Input for Delay4 or Counter4 External Clock	18
reg<119:114>	Matrix Out: Input for Delay5 or Counter5 External Clock	19
reg<125:120>	Matrix Out: Input for Delay6 or Counter6 External Clock	20
reg<131:126>	Matrix Out: Input for Filter_0	21
reg<137:132>	Matrix Out: Input for Filter_1	22
reg<143:138>	Reserved	23
reg<149:144>	Matrix Out: In0 of LUT3_9	24
reg<155:150>	Matrix Out: In1 of LUT3_9	25
reg<161:156>	Matrix Out: In2 of LUT3_9	26
reg<167:162>	Matrix Out: In0 of LUT4_0 or Input for Counter2 (Delay2) External Clock	27
reg<173:168>	Matrix Out: In1 of LUT4_0 or Input for Delay2 (Counter2 Reset Input)	28
reg<179:174>	Matrix Out: In2 of LUT4_0	29
reg<185:180>	Matrix Out: In3 of LUT4_0	30
reg<191:186>	Matrix Out: In0 of LUT4_1 or Input for Counter3 (Delay3) External Clock	31
reg<197:192>	Matrix Out: In1 of LUT4_1 or Input for Delay3 (Counter3 Reset Input)	32
reg<203:198>	Matrix Out: In2 of LUT4_1	33
reg<209:204>	Matrix Out: In3 of LUT4_1	34
reg<215:210>	Matrix Out: In0 of LUT3_0	35
reg<221:216>	Matrix Out: In1 of LUT3_0	36
reg<227:222>	Matrix Out: In2 of LUT3_0	37

Table 25. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<233:228>	Matrix Out: In0 of LUT3_1	38
reg<239:234>	Matrix Out: In1 of LUT3_1	39
reg<245:240>	Matrix Out: In2 of LUT3_1	40
reg<251:246>	Matrix Out: In0 of LUT3_2 or Clock Input of DFF2	41
reg<257:252>	Matrix Out: In1 of LUT3_2 or Data Input of DFF2	42
reg<263:258>	Matrix Out: In2 of LUT3_2 or nRST (nSET) Input of DFF2	43
reg<269:264>	Matrix Out: In0 of LUT3_3 or Clock Input of DFF3	44
reg<275:270>	Matrix Out: In1 of LUT3_3 or Data Input of DFF3	45
reg<281:276>	Matrix Out: In2 of LUT3_3 or nRST (nSET) of DFF3	46
reg<287:282>	Matrix Out: In0 of LUT3_4	47
reg<293:288>	Matrix Out: In1 of LUT3_4	48
reg<299:294>	Matrix Out: In2 of LUT3_4	49
reg<305:300>	Matrix Out: In0 of LUT3_5	50
reg<311:306>	Matrix Out: In1 of LUT3_5	51
reg<317:312>	Matrix Out: In2 of LUT3_5	52
reg<323:318>	Matrix Out: In0 of LUT3_6	53
reg<329:324>	Matrix Out: In1 of LUT3_6	54
reg<335:330>	Matrix Out: In2 of LUT3_6	55
reg<341:336>	Matrix Out: In0 of LUT3_7	56
reg<347:342>	Matrix Out: In1 of LUT3_7	57
reg<353:348>	Matrix Out: In2 of LUT3_7	58
reg<359:354>	Matrix Out: In0 of LUT3_8 or Input of Pipe Delay	59
reg<365:360>	Matrix Out: In1 of LUT3_8 or nRST of Pipe Delay	60
reg<371:366>	Matrix Out: In2 of LUT3_8 or Clock of Pipe Delay	61
reg<377:372>	Matrix Out: In0 of LUT2_0 or Clock Input of DFF4	62
reg<383:378>	Matrix Out: In1 of LUT2_0 or Data Input of DFF4	63
reg<389:384>	Matrix Out: In0 of LUT2_1 or Clock Input of DFF5	64
reg<395:390>	Matrix Out: In1 of LUT2_1 or Data Input of DFF5	65
reg<401:396>	Matrix Out: In0 of LUT2_2 or Clock Input of DFF6	66
reg<407:402>	Matrix Out: In1 of LUT2_2 or Data Input of DFF6	67
reg<413:408>	Matrix Out: In0 of LUT2_3 or Clock Input of DFF7	68
reg<419:414>	Matrix Out: In1 of LUT2_3 or Data Input of DFF7	69
reg<425:420>	Matrix Out: In0 of LUT2_4	70
reg<431:426>	Matrix Out: In1 of LUT2_4	71
reg<437:432>	Matrix Out: In0 of LUT2_5	72
reg<443:438>	Matrix Out: In1 of LUT2_5	73
reg<449:444>	Matrix Out: Input for Programmable Delay & Edge Detector	74
reg<455:450>	Matrix Out: Power Down for Osc	75
reg<461:456>	Reserved	76

Table 25. Matrix Output Table

Register Bit Address	Matrix Output Signal Function	Matrix Output Number
reg<467:462>	Reserved	77
reg<473:468>	Reserved	78
reg<479:474>	Reserved	79
reg<485:480>	Reserved	80
reg<491:486>	Reserved	81
reg<497:492>	Matrix Out: Pin10 Digital Output Source	82
reg<503:498>	Matrix Out: Pin10 Output Enable	83
reg<509:504>	Matrix Out: Pin11 Digital Output Source	84
reg<515:510>	Matrix Out: Pin12 Digital Output Source	85
reg<521:516>	Matrix Out: Pin12 Output Enable	86
reg<527:522>	Matrix Out: Pin13 Digital Output Source	87
reg<533:528>	Matrix Out: Pin13 Output Enable	88
reg<539:534>	Matrix Out: Pin14 Digital Output Source	89
reg<545:540>	Matrix Out: Input of INV_0 Gate	90
reg<551:546>	Matrix Out: Input of INV_1 Gate	91

9.0 Combinatorial Logic

Combinatorial logic is supported via nine Lookup Tables (LUTs) within the SLG46169. There are two 2-bit LUTs and seven 3-bit LUTs. The device also includes eight Combination Function Macrocells that can be used as LUTs. For more details, please see Section *10.0 Combination Function Macrocells*.

Inputs/Outputs for the nine LUTs are configured from the connection matrix with specific logic functions being defined by the state of NVM bits. The outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR).

9.1 2-Bit LUT

The two 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

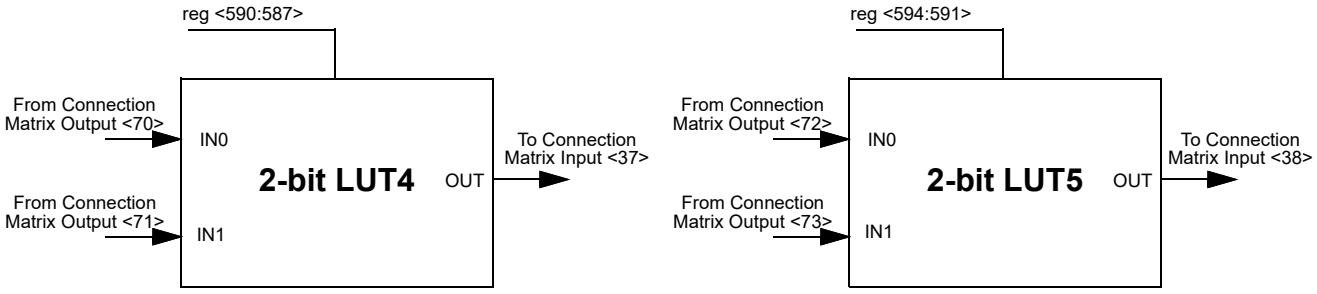


Figure 7. 2-bit LUTs

Table 26. 2-bit LUT4 Truth Table

IN1	IN0	OUT
0	0	reg <587>
0	1	reg <588>
1	0	reg <589>
1	1	reg <590>

Table 27. 2-bit LUT5 Truth Table

IN1	IN0	OUT
0	0	reg <591>
0	1	reg <592>
1	0	reg <593>
1	1	reg <594>

Each 2-bit LUT uses a 4-bit register signal to define their output functions;

2-Bit LUT4 is defined by reg<590:587>

2-Bit LUT5 is defined by reg<594:591>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the two 2-bit LUT logic cells.

Table 28. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

9.2 3-Bit LUT

The seven 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix.

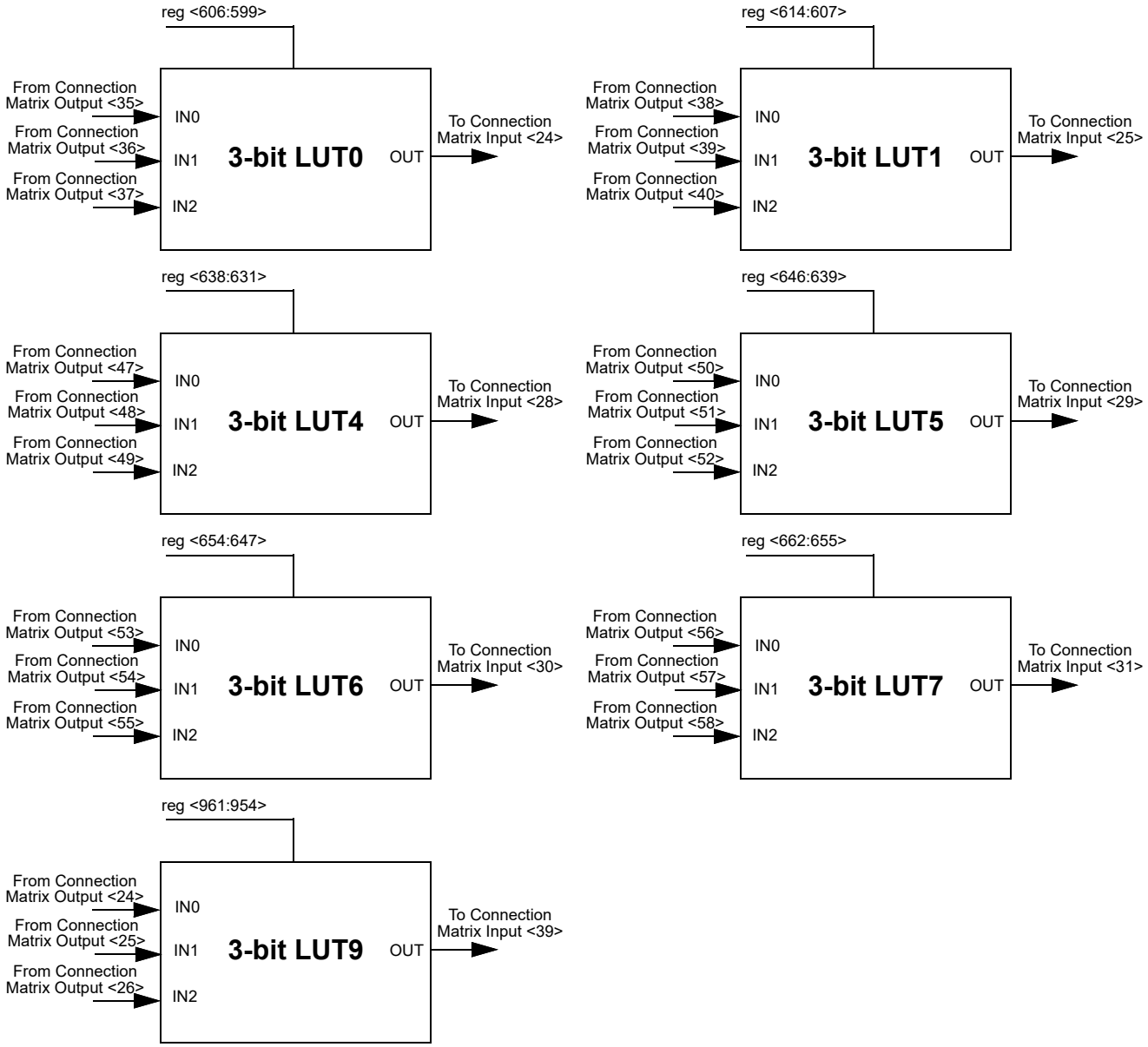


Figure 8. 3-bit LUTs

Table 29. 3-bit LUT0 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <599>
0	0	1	reg <600>
0	1	0	reg <601>
0	1	1	reg <602>
1	0	0	reg <603>
1	0	1	reg <604>
1	1	0	reg <605>
1	1	1	reg <606>

Table 30. 3-bit LUT1 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <607>
0	0	1	reg <608>
0	1	0	reg <609>
0	1	1	reg <610>
1	0	0	reg <611>
1	0	1	reg <612>
1	1	0	reg <613>
1	1	1	reg <614>

Table 31. 3-bit LUT4 Truth Table

IN2	IN1	IN0	OUT
0	0	0	reg <631>
0	0	1	reg <632>
0	1	0	reg <633>
0	1	1	reg <634>
1	0	0	reg <635>
1	0	1	reg <636>
1	1	0	reg <637>
1	1	1	reg <638>

Table 32. 3-bit LUT5 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <639>
0	0	1	reg <640>
0	1	0	reg <641>
0	1	1	reg <642>
1	0	0	reg <643>
1	0	1	reg <644>
1	1	0	reg <645>
1	1	1	reg <646>

Table 33. 3-bit LUT6 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <647>
0	0	1	reg <648>
0	1	0	reg <649>
0	1	1	reg <650>
1	0	0	reg <651>
1	0	1	reg <652>
1	1	0	reg <653>
1	1	1	reg <654>

Table 34. 3-bit LUT7 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <655>
0	0	1	reg <656>
0	1	0	reg <657>
0	1	1	reg <658>
1	0	0	reg <659>
1	0	1	reg <660>
1	1	0	reg <661>
1	1	1	reg <662>

Table 35. 3-bit LUT9 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <954>
0	0	1	reg <955>
0	1	0	reg <956>
0	1	1	reg <957>
1	0	0	reg <958>
1	0	1	reg <959>
1	1	0	reg <960>
1	1	1	reg <961>

Each 3-bit LUT uses a 8-bit register signal to define their output functions;

3-Bit LUT0 is defined by reg<606:599>

3-Bit LUT1 is defined by reg<614:607>

3-Bit LUT4 is defined by reg<638:631>

3-Bit LUT5 is defined by reg<646:639>

3-Bit LUT6 is defined by reg<654:647>

3-Bit LUT7 is defined by reg<662:655>

3-Bit LUT9 is defined by reg<961:954>

The table below shows the register bits for the standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR) that can be created within each of the six 3-bit LUT logic cells.

Table 36. 3-bit LUT Standard Digital Functions.

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	1	0	0	1	0	1	1	0
XNOR-3	0	1	1	0	1	0	0	1

10.0 Combination Function Macrocells

The SLG46169 has nine combination function macrocells that can serve more than one logic or timing function. In each case, they can serve as a Look Up Table (LUT), or as another logic or timing function. See the list below for the functions that can be implemented in these macrocells;

- Four macrocells that can serve as either 2-bit LUTs or as D Flip Flops.
- Two macrocells that can serve as either 3-bit LUTs or as D Flip Flops.
- One macrocell that can serve as either 3-bit LUT or as Pipe Delay
- Two macrocells that can serve as either 4-bit LUTs or as 8-Bit Counter / Delays

Inputs/Outputs for the nine combination function macrocells are configured from the connection matrix with specific logic functions being defined by the state of NVM bits.

When used as a LUT to implement combinatorial logic functions, the outputs of the LUTs can be configured to any user defined function, including the following standard digital logic devices (AND, NAND, OR, NOR, XOR, XNOR, Inverter, Buffer and MUX for 3-bit and 4-bit LUTs).

When used as a D Flip Flop / Latch, the source and destination of the inputs and outputs for the DFF/Latches are configured from the connection matrix. All DFF/Latch macrocells have user selection for initial state, and all have the option to connect both the Q and Q Bar outputs to the connection matrix. The macrocells DFF2, DFF3 have an additional input from the matrix that can serve as a nSet or nReset function to the macrocell.

The operation of the D Flip-Flop and Latch will follow the functional descriptions below:

DFF: CLK is rising edge triggered, then Q = D; otherwise Q will not change

Latch: if CLK = 0, then Q = D

10.1 2-Bit LUT or D Flip Flop Macrocells

There are four macrocells that can serve as either 2-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 2-bit LUTs each take in two input signals from the connection matrix and produce a single output, which goes back into the connection

matrix. When used to implement D Flip Flop function, the two input signals from the connection matrix go to the data (d) and clock (clk) inputs for the Flip Flop, with the output going back to the connection matrix.

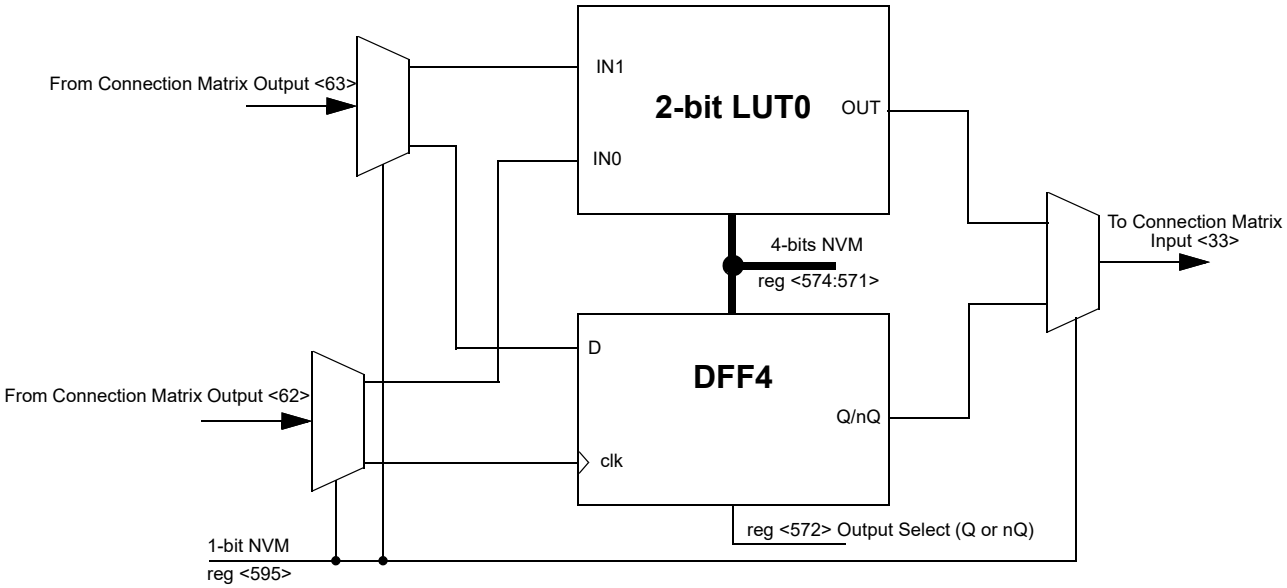


Figure 9. 2-bit LUT0 or DFF4

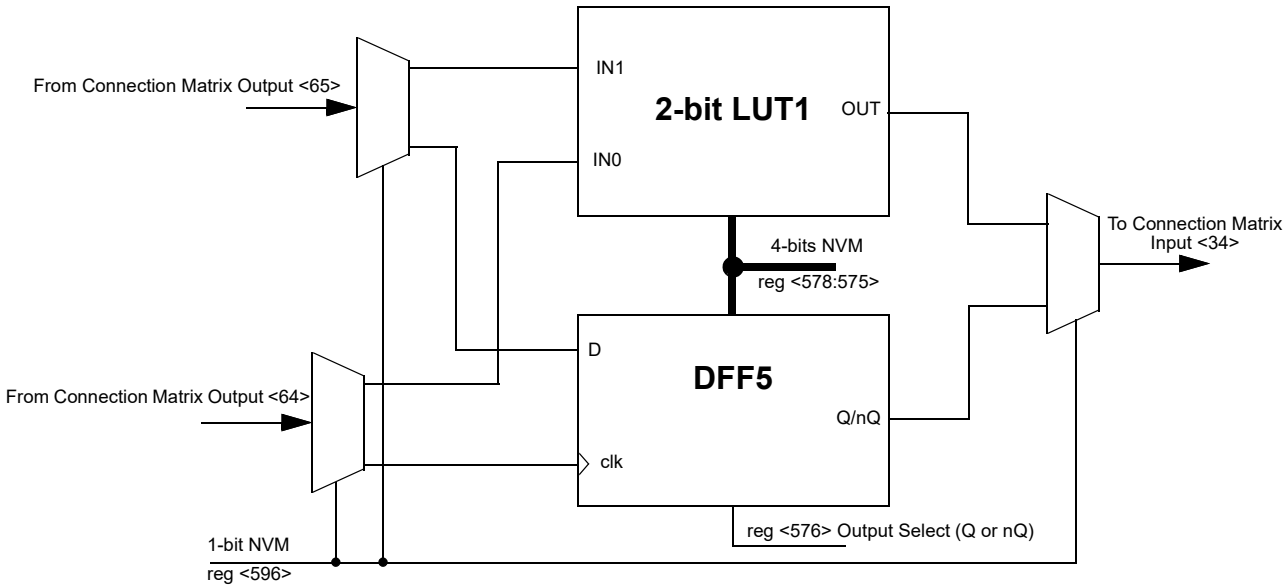


Figure 10. 2-bit LUT1 or DFF5

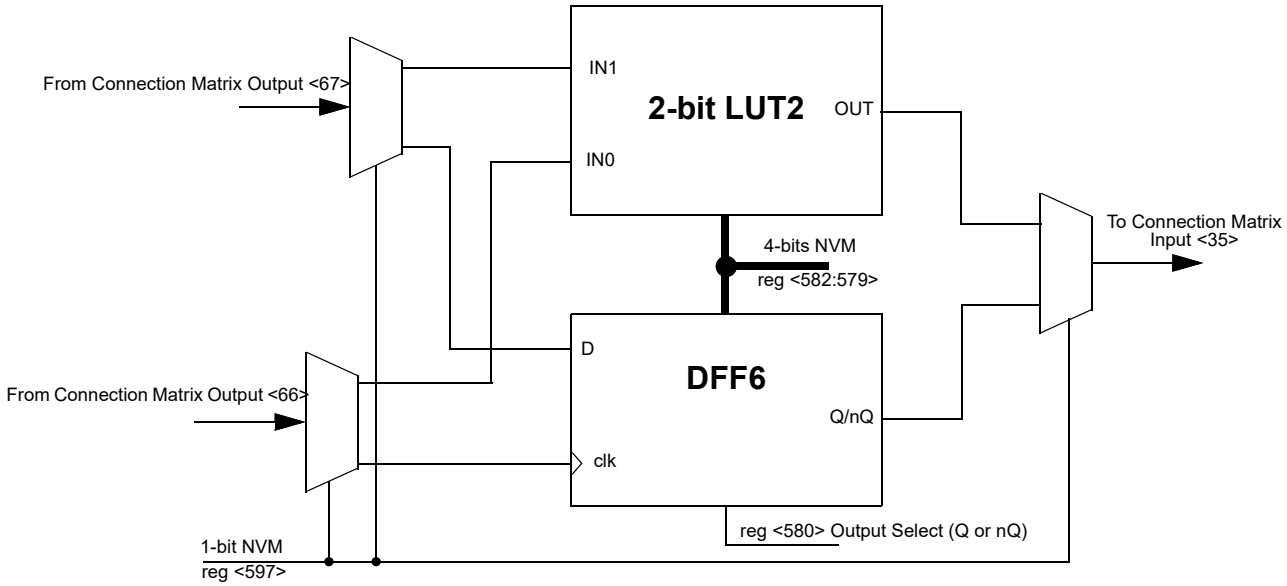


Figure 11. 2-bit LUT2 or DFF6

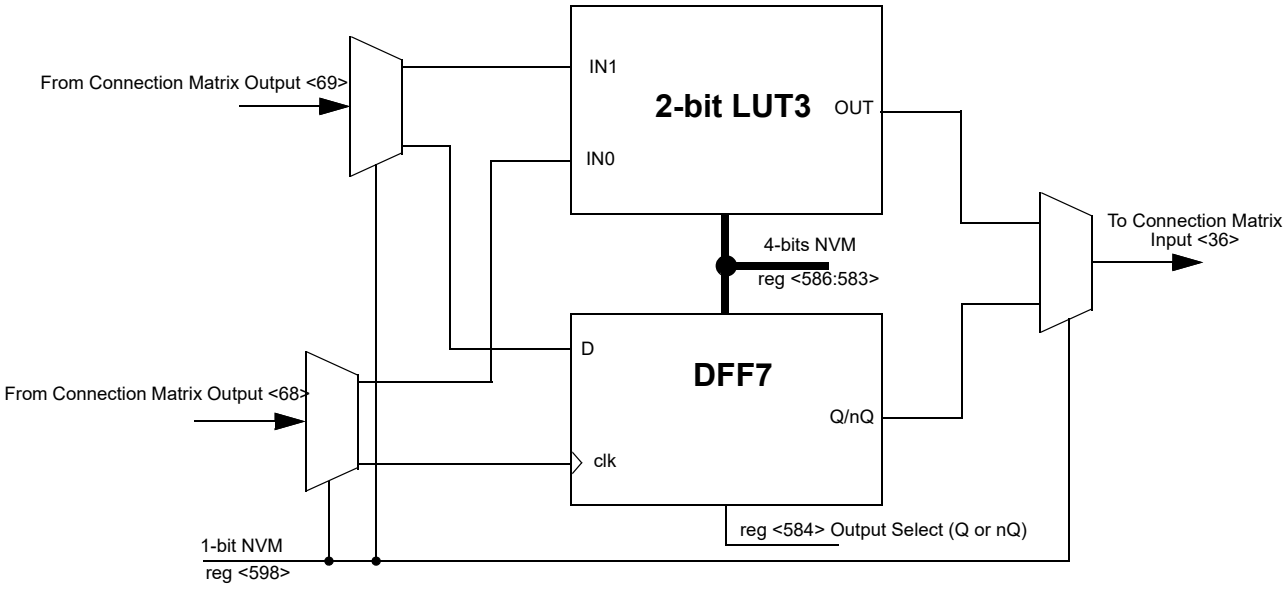


Figure 12. 2-bit LUT3 or DFF7

10.1.1 2-Bit LUT or D Flip Flop Macrocells Used as 2-Bit LUTs

Table 37. 2-bit LUT0 Truth Table.

IN1	IN0	OUT
0	0	reg <571>
0	1	reg <572>
1	0	reg <573>
1	1	reg <574>

Table 38. 2-bit LUT1 Truth Table.

IN1	IN0	OUT
0	0	reg <575>
0	1	reg <576>
1	0	reg <577>
1	1	reg <578>

Table 39. 2-bit LUT2 Truth Table.

IN1	IN0	OUT
0	0	reg <579>
0	1	reg <580>
1	0	reg <581>
1	1	reg <582>

Table 40. 2-bit LUT3 Truth Table.

IN1	IN0	OUT
0	0	reg <583>
0	1	reg <584>
1	0	reg <585>
1	1	reg <586>

Each Macrocell, when programmed for a LUT function, uses a 4-bit register to define their output function:

2-Bit LUT0 is defined by reg<574:571>

2-Bit LUT1 is defined by reg<578:575>

2-Bit LUT2 is defined by reg<582:579>

2-Bit LUT3 is defined by reg<586:583>

Table 41. 2-bit LUT Standard Digital Functions

Function	MSB			LSB
AND-2	1	0	0	0
NAND-2	0	1	1	1
OR-2	1	1	1	0
NOR-2	0	0	0	1
XOR-2	0	1	1	0
XNOR-2	1	0	0	1

10.1.2 2-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 42. DFF4 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_0 or DFF4 Select	<595>	0: LUT2_0 1: DFF4
DFF4 or Latch Select	<571>	0: DFF function 1: Latch function
DFF4 Output Select	<572>	0: Q output 1: nQ output
DFF4 Initial Polarity Select	<573>	0: Low 1: High

Table 43. DFF5 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_1 or DFF5 Select	<596>	0: LUT2_1 1: DFF5
Select or Latch select	<575>	0: DFF function 1: Latch function
DFF5 Output Select	<576>	0: Q output 1: nQ output
DFF5 Initial Polarity Select	<577>	0: Low 1: High

Table 44. DFF6 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_2 or DFF6 Select	<597>	0: LUT2_2 1: DFF6
DFF6 or Latch Select	<579>	0: DFF function 1: Latch function
DFF6 Output Select	<580>	0: Q output 1: nQ output
DFF6 Initial Polarity Select	<581>	0: Low 1: High

Table 45. DFF7 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT2_3 or DFF7 Select	<598>	0: LUT2_3 1: DFF7
DFF7 or Latch Select	<583>	0: DFF function 1: Latch function
DFF7 Output Select	<584>	0: Q output 1: nQ output
DFF7 Initial Polarity Select	<585>	0: Low 1: High

10.2 3-Bit LUT or D Flip Flop with Set/Reset Macrocells

There are two macrocells that can serve as either 3-bit LUTs or as D Flip Flops. When used to implement LUT functions, the 3-bit LUTs each take in three input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement D Flip Flop function, the three input signals from the connection matrix go to the data (D) and clock (clk) and Set/Reset (nRST/nSET) inputs for the Flip Flop, with the output going back to the connection matrix.

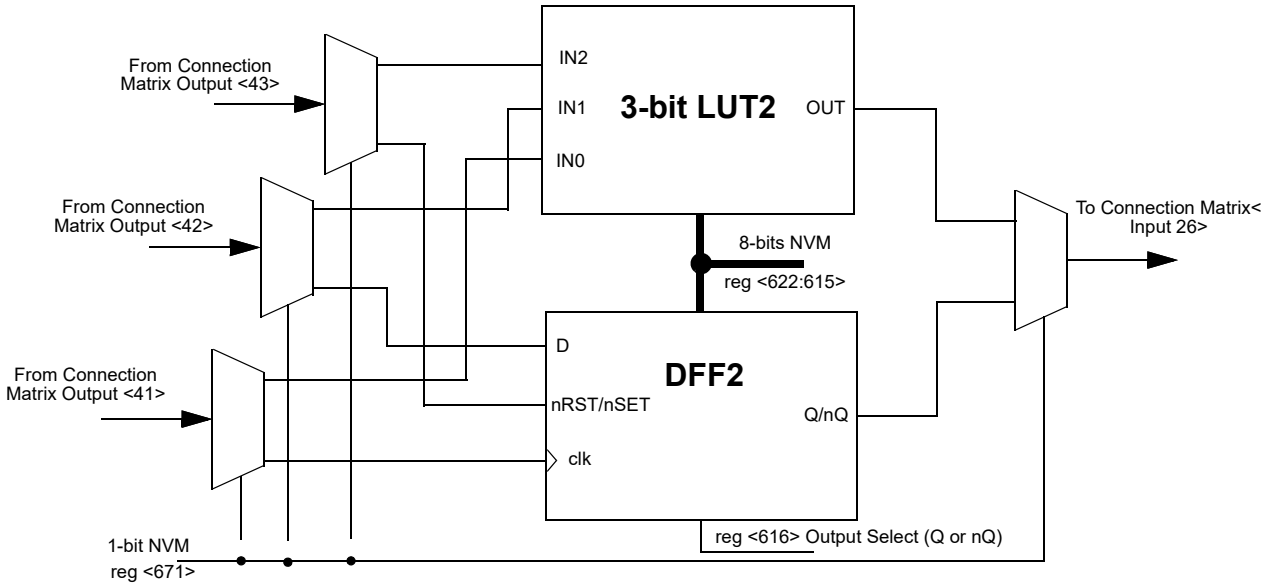


Figure 13. 3-bit LUT2 or DFF2

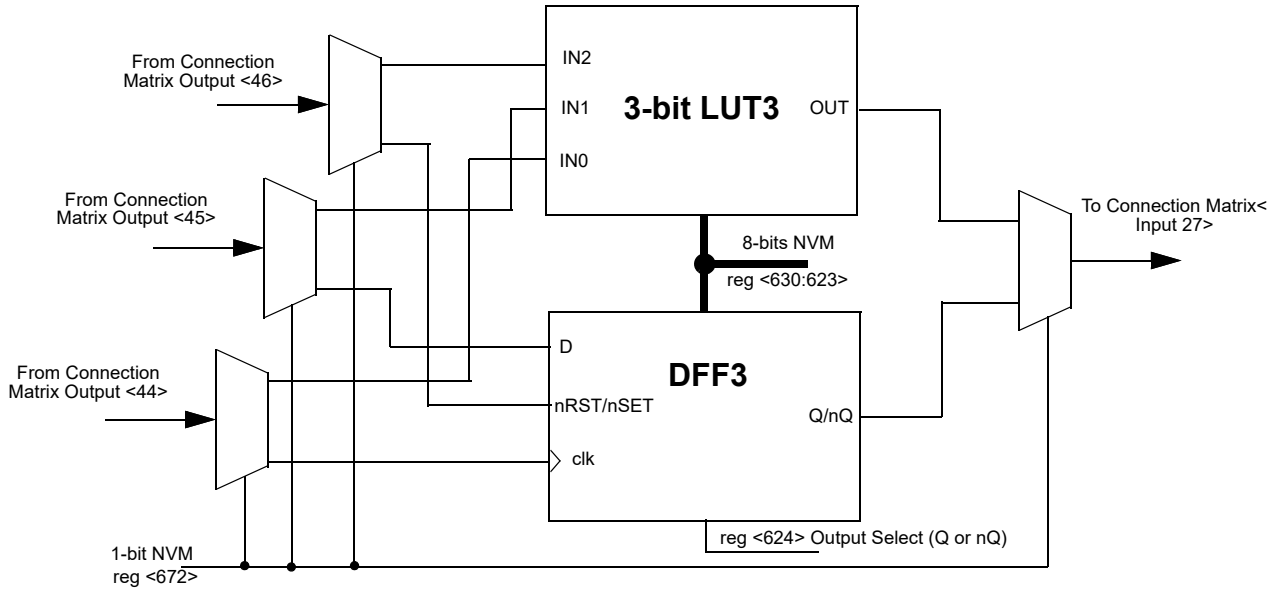


Figure 14. 3-bit LUT3 or DFF3

10.2.1 3-Bit LUT or D Flip Flop Macrocells Used as 3-Bit LUTs

Table 46. 3-bit LUT2 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <615>
0	0	1	reg <616>
0	1	0	reg <617>
0	1	1	reg <618>
1	0	0	reg <619>
1	0	1	reg <620>
1	1	0	reg <621>
1	1	1	reg <622>

Table 47. 3-bit LUT3 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <623>
0	0	1	reg <624>
0	1	0	reg <625>
0	1	1	reg <626>
1	0	0	reg <627>
1	0	1	reg <628>
1	1	0	reg <629>
1	1	1	reg <630>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT2 is defined by reg<622:615>

3-Bit LUT3 is defined by reg<630:623>

10.2.2 3-Bit LUT or D Flip Flop Macrocells Used as D Flip Flop Register Settings

Table 48. DFF2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_2 or DFF2 Select	reg<671>	0: LUT3_2 1: DFF2
DFF2 or Latch Select	reg<615>	0: DFF function 1: Latch function
DFF2 Output Select	reg<616>	0: Q output 1: nQ output
DFF2 nRST/nSET Select	reg<617>	1: nSET from matrix out 0: nRST from matrix out
DFF2 Initial Polarity Select	reg<618>	0: Low 1: High

Table 49. DFF3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_3 or DFF3 Select	reg<672>	0: LUT3_3 1: DFF3
DFF3 or Latch Select	reg<623>	0: DFF function 1: Latch function
DFF3 Output Select	reg<624>	0: Q output 1: nQ output
DFF3 nRST/nSET Select	reg<625>	1: nSET from matrix out 0: nRST from matrix out
DFF3 Initial Polarity Select	reg<626>	0: Low 1: High

10.3 3-Bit LUT or Pipe Delay Macrocell

There is one macrocell that can serve as either a 3-bit LUT or as a Pipe Delay.

When used to implement LUT functions, the 3-bit LUT takes in three input signals from the connection matrix and produces a single output, which goes back into the connection matrix.

When used as a pipe delay, there are three inputs signals from the matrix, Input (IN), Clock (CLK) and Reset (RST). The pipe delay cell is built from 16 D Flip-Flop logic cells that provide the three delay options, two of which are user selectable. The DFF cells are tied in series where the output (Q) of each delay cell goes to the next DFF cell. The first delay option (ONE PIPE OUT) is fixed at the output of the first flip-flop stage. The other two outputs (OUT0 and OUT1) provide user selectable options for 1 – 16 stages of delay There are delay output points for each set of the OUT0 and OUT1 outputs to a 4-input mux that is controlled by reg <666:663> for OUT0 and reg <670:667> for OUT1. The 4-input mux is used to control the selection of the amount of delay.

The overall time of the delay is based on the clock used in the SLG46169 design. Each DFF cell has a time delay of the inverse of the clock time (either external clock or the RC Oscillator within the SLG46169). The sum of the number of DFF cells used will be the total time delay of the Pipe Delay logic cell.

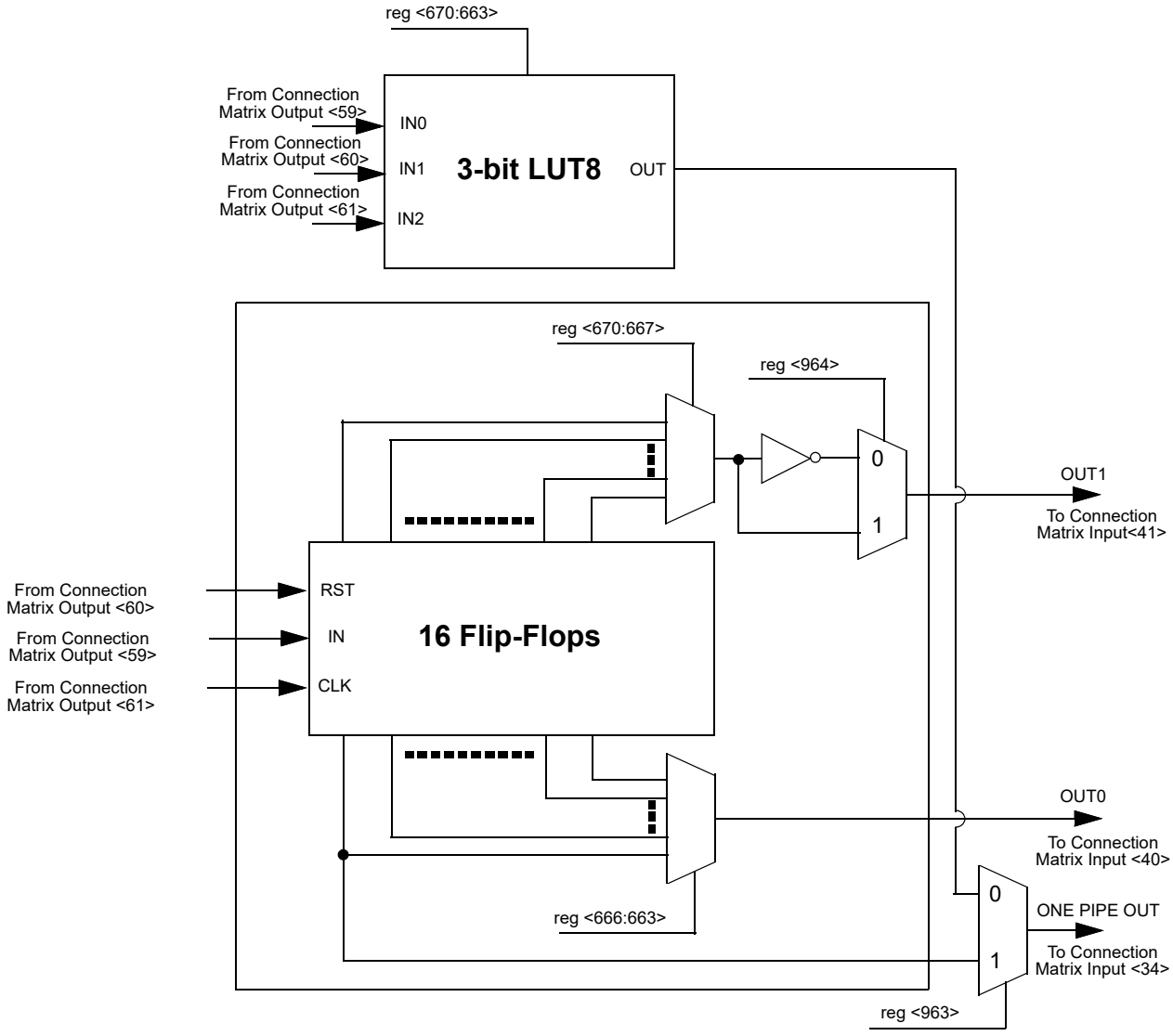


Figure 15. 3-bit LUT8 or Pipe Delay

10.3.1 3-Bit LUT or Pipe Delay Macrocells Used as 3-Bit LUTs

Table 50. 3-bit LUT8 Truth Table.

IN2	IN1	IN0	OUT
0	0	0	reg <663>
0	0	1	reg <664>
0	1	0	reg <665>
0	1	1	reg <666>
1	0	0	reg <667>
1	0	1	reg <668>
1	1	0	reg <669>
1	1	1	reg <670>

Each Macrocell, when programmed for a LUT function, uses a 8-bit register to define their output function:

3-Bit LUT8 is defined by reg<670:663>

Table 51. 3-bit LUT Standard Digital Functions

Function	MSB							LSB
AND-3	1	0	0	0	0	0	0	0
NAND-3	0	1	1	1	1	1	1	1
OR-3	1	1	1	1	1	1	1	0
NOR-3	0	0	0	0	0	0	0	1
XOR-3	0	0	0	1	0	1	1	0
XNOR-3	1	1	1	0	1	0	0	1

10.3.2 3-Bit LUT or Pipe Delay Macrocells Used as Pipe Delay Register Settings

Table 52. Pipe Delay Register Settings

Signal Function	Register Bit Address	Register Definition
LUT3_8 or Pipe Delay Output Select	reg<963>	0: LUT3_8 1: 1 Pipe Delay Output
OUT0 select	reg<666:663>	
OUT1 select	reg<670:667>	
Pipe delay OUT1 Polarity Select Bit	reg<964>	0: Non-inverted 1: Inverted

10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells

There are two macrocells that can serve as either 4-bit LUTs or as Counter / Delays. When used to implement LUT functions, the 4-bit LUTs each take in four input signals from the connection matrix and produce a single output, which goes back into the connection matrix. When used to implement 8-Bit Counter / Delays function, two of the four input signals from the connection matrix go to the external clock (ext_clk) and reset (DLY_in/CNT_Reset) for the counter/delay, with the output going back to the connection matrix. For timing diagrams refer to section *13.1 CNT/DLY Timing Diagrams*.

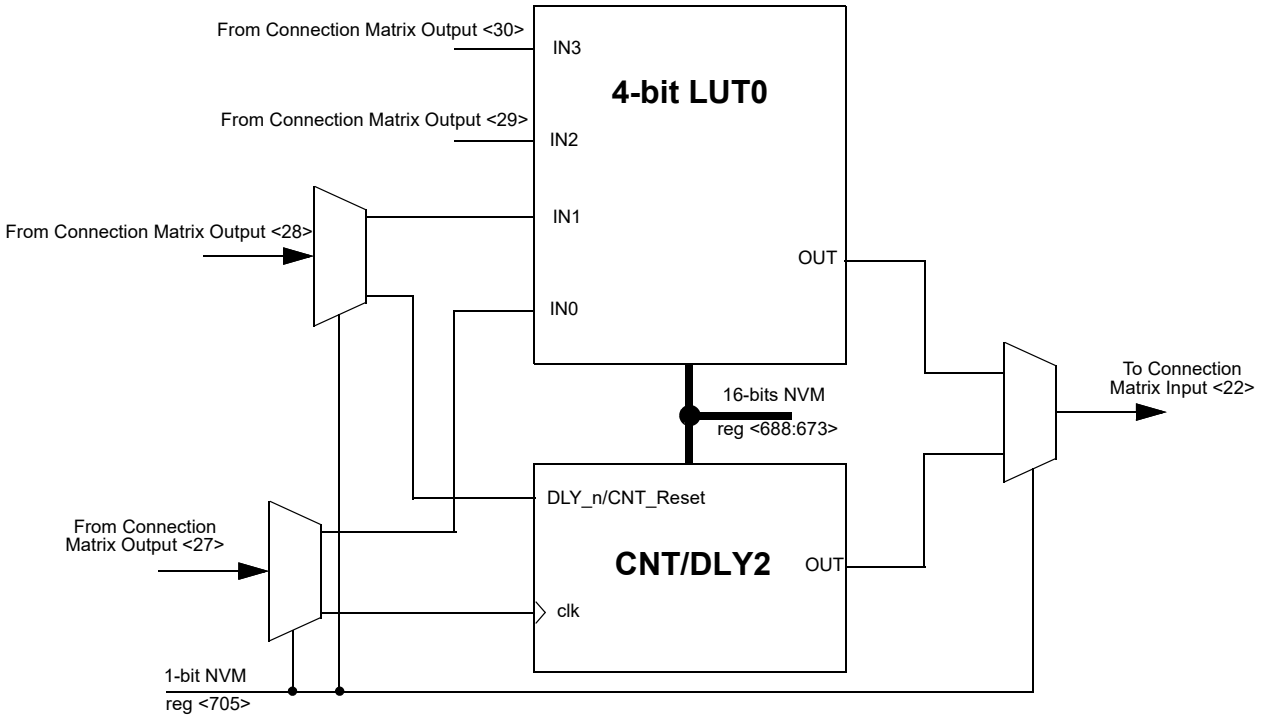


Figure 16. 4-bit LUT0 or CNT/DLY2

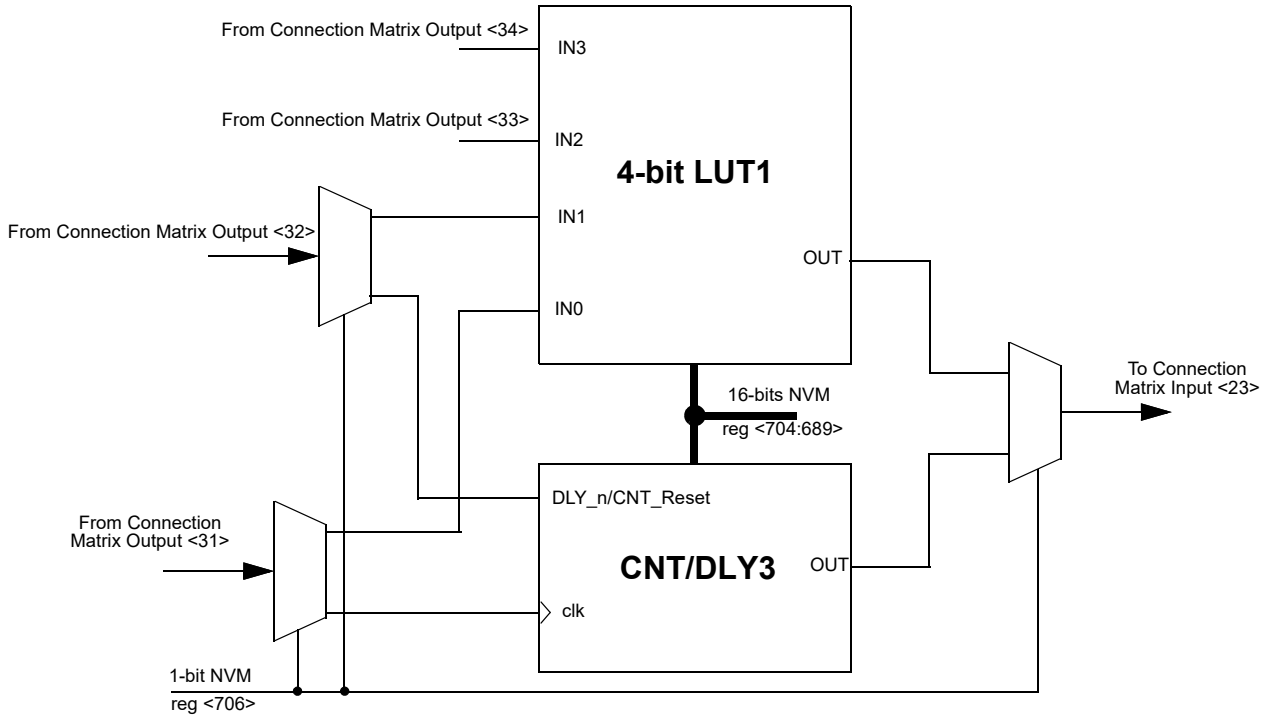


Figure 17. 4-bit LUT1 or CNT/DLY3

10.4.1 4-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 4-Bit LUTs

Table 53. 4-bit LUT0 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <673>
0	0	0	1	reg <674>
0	0	1	0	reg <675>
0	0	1	1	reg <676>
0	1	0	0	reg <677>
0	1	0	1	reg <678>
0	1	1	0	reg <679>
0	1	1	1	reg <680>
1	0	0	0	reg <681>
1	0	0	1	reg <682>
1	0	1	0	reg <683>
1	0	1	1	reg <684>
1	1	0	0	reg <685>
1	1	0	1	reg <686>
1	1	1	0	reg <687>
1	1	1	1	reg <688>

Table 54. 4-bit LUT1 Truth Table.

IN3	IN2	IN1	IN0	OUT
0	0	0	0	reg <689>
0	0	0	1	reg <690>
0	0	1	0	reg <691>
0	0	1	1	reg <692>
0	1	0	0	reg <693>
0	1	0	1	reg <694>
0	1	1	0	reg <695>
0	1	1	1	reg <696>
1	0	0	0	reg <697>
1	0	0	1	reg <698>
1	0	1	0	reg <699>
1	0	1	1	reg <700>
1	1	0	0	reg <701>
1	1	0	1	reg <702>
1	1	1	0	reg <703>
1	1	1	1	reg <704>

Each Macrocell, when programmed for a LUT function, uses a 16-bit register to define their output function:

4-Bit LUT0 is defined by reg<688:673>

4-Bit LUT1 is defined by reg<704:689>

Table 55. 4-bit LUT Standard Digital Functions.

Function	MSB															LSB
AND-4	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
NAND-4	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
OR-4	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
NOR-4	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
XOR-4	0	1	1	0	1	0	0	1	1	1	0	0	1	1	1	0
XNOR-4	1	0	0	1	0	1	1	0	0	0	1	1	0	0	0	1

10.4.2 4-Bit LUT or 8-Bit Counter / Delay Macrocells Used as 8-Bit Counter / Delay Register Settings

Table 56. CNT/DLY2 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_0 or Counter2 Select	reg<705>	0: LUT4_0 1: Counter2
Counter/delay2 Mode Selection	reg<673>	0: Delay Mode 1: Counter Mode
Counter/delay2 Clock Source Select	reg<676:674>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock / 8 111: Counter1 Overflow
Counter/delay2 Control Data	reg<684:677>	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay2 Mode Select or asynchronous counter reset	reg<686:685>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset

Table 57. CNT/DLY3 Register Settings

Signal Function	Register Bit Address	Register Definition
LUT4_1 or Counter3 Select	reg<706>	0: LUT4_1 1: Counter3
Counter/delay3 Mode Selection	reg<689>	0: Delay Mode 1: Counter Mode
Counter/delay3 Clock Source Select	reg<692:690>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock / 8 111: Counter2 Overflow
Counter/delay3 Control Data	reg<700:693>	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay3 Mode Select or asynchronous counter reset	reg<702:701>	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset

11.0 Analog Comparators (ACMP)

There are two Analog Comparator (ACMP) macrocells in the SLG46169. In order for the ACMP cells to be used in a GreenPAK design, the power up signals (ACMP0_pdb, ACMP1_pdb) need to be active. By connecting to signals coming from the Connection Matrix, it is possible to have each ACMP be on continuously, off continuously, or switched on periodically based on a digital signal coming from the Connection Matrix. When ACMP is powered down, output is low.

Each of the ACMP cells has a positive input signal that can be provided by a variety of external sources, and can also have a selectable gain stage before connection to the analog comparator. Each of the ACMP cells has a negative input signal that is either created from an internal VREF or provided by way of the external sources.

PWR UP = 1 => ACMP is powered up.
PWR UP = 0 => ACMP is powered down.

During powerup, the ACMP output will remain low, and then become valid 120 μs (max) after POR signal goes high. If Low Bandwidth option enabled, then the ACMP output initializes in the high state.

Vref accuracy is optimized near 1000 mV selection.

Input bias current < 1 nA (typ). The Gain divider is unbuffered and consists of 1 MΩ resistors. IN- voltage range: 0 - 1.2 V. Can use Vref selection $V_{DD}/4$ and $V_{DD}/3$ to maintain this input range.

For high input impedance when using the gain divider (x0.25, x0.33, x0.5), it is possible to use the input buffer. However, this will affect input voltage range, see *Figure 18.* . It also will add the offset in a range of -24.5 mV to 12.6 mV. It is not recommended to use the input buffer when the gain divider is not used. .

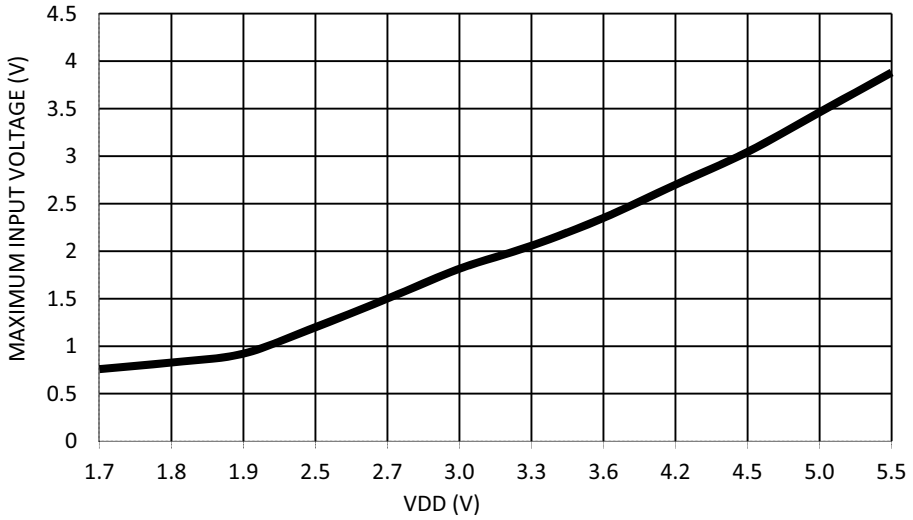


Figure 18. Maximum Analog Buffer Input Voltage vs. V_{DD}

Note: the input buffer gain depends on V_{DD}, see Figure 19. .

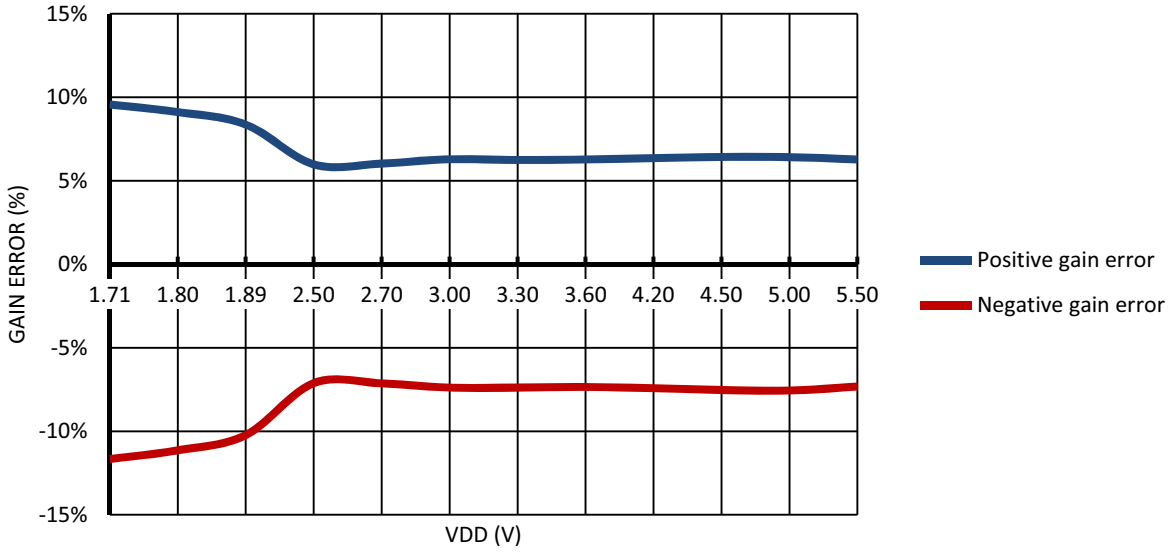


Figure 19. Input Buffer Gain Error vs. V_{DD}

Each of the ACMP cells has a selection for the bandwidth of the input signal, which can be used to save power when low bandwidth signals are input into the analog comparator.

Low bandwidth: For V_{DD} 1.8 V or less, this option will connect a low pass filter with 180 kHz upper frequency. And if input frequency > 200 kHz, the output will retain its previous value.

Enabling the Analog buffer will influence the ACMP response time.

Note that power supply control options have influence on Analog macrocells operation.

Note: Any ACMP powered ON enables the BandGap circuit as well, and an analog voltage will appear on Vref (even when Force BandGap is disabled).

Each cell also has a hysteresis selection, to offer hysteresis of 0 mV, 25 mV, 50 mV or 200 mV.

Hysteresis: Input signal hysteresis options are disable, 25 mV, 50 mV, 200 mV.

Note: $V_{IL} = V_{IN} - V_{HYS}/2$, $V_{IH} = V_{IN} + V_{HYS}/2$.

ACMP0 IN+ options are pin 5, buffered PIN 5, V_{DD}
ACMP1 IN+ options are pin 8, buffered PIN 8, ACMP0 IN+

11.1 ACMP0 Block Diagram

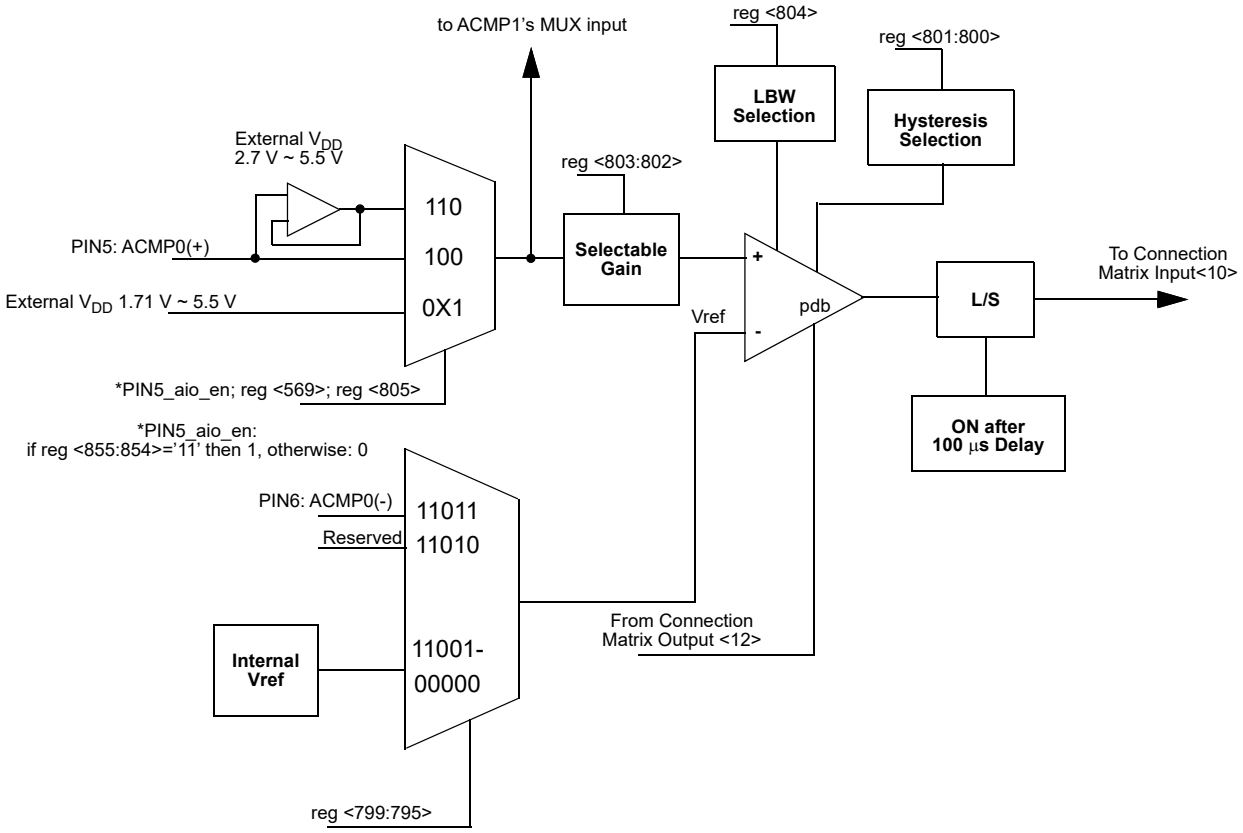


Figure 20. ACMP0 Block Diagram

11.2 ACMP0 Register Settings

Table 58. ACMP0 Register Settings

Signal Function	Register Bit Address	Register Definition
Analog Buffer at ACMP0 Enable	reg<569>	1: Enable Analog Buffer 0: Disable Analog Buffer
ACMP0 In Voltage Select	reg<799:795>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: Reserved 11011: EXT_VREF(PIN6)
ACMP0 Hysteresis Enable	reg<801:800>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP0 Positive Input Divider	reg<803:802>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP0 Low Bandwidth (Max: 1 MHz) Enable	reg<804>	1: On 0: Off
ACMP0 Positive Input Source Select V_{DD}	reg<805>	0: Disable 1: Enable

11.3 ACMP1 Block Diagram

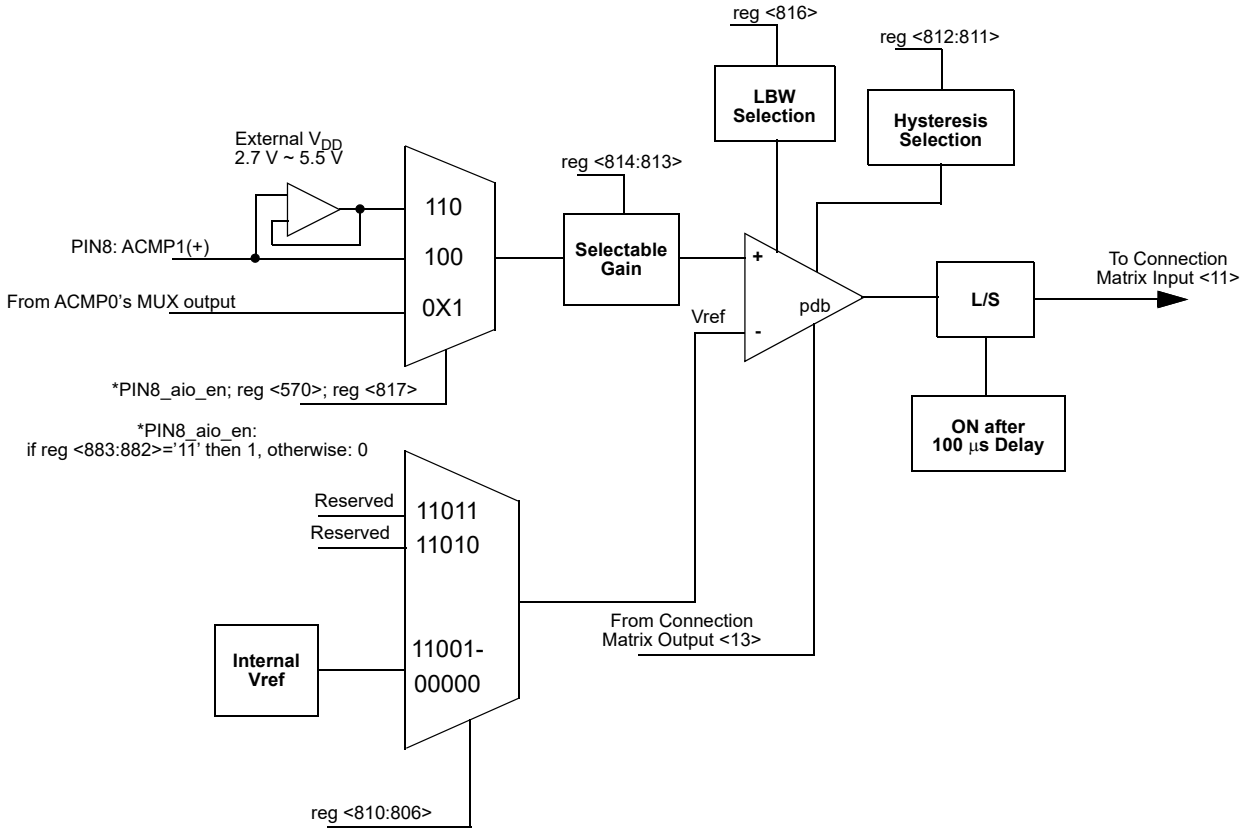


Figure 21. ACMP1 Block Diagram

11.4 ACMP1 Register Settings

Table 59. ACMP1 Register Settings

Signal Function	Register Bit Address	Register Definition
Analog Buffer at ACMP1 Enable	reg<570>	1: Enable Analog Buffer 0: Disable Analog Buffer
ACMP1 Negative Input Voltage Select	reg<810:806>	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: $V_{DD}/3$ 11001: $V_{DD}/4$ 11010: Reserved 11011: Reserved
ACMP1 Hysteresis Enable	reg<812:811>	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
ACMP1 Positive Input Divider	reg<814:813>	00: 1.00X 01: 0.50X 10: 0.33X 11: 0.25X
ACMP1 Low Bandwidth (Max: 1 MHz) Enable	reg<816>	0: Off 1: On
ACMP1 Positive Input Source Select PIN5	reg<817>	0: Disable 1: Enable

12.0 Digital Storage Elements (DFFs/Latches)

There are six Combination Function macrocells that can be used to implement D-Flip Flop or Latch functions. Please see Section *10.1 2-Bit LUT or D Flip Flop Macrocells* and Section *10.2 3-Bit LUT or D Flip Flop with Set/Reset Macrocells* for the description of this Combination Function macrocell.

12.1 Initial Polarity Operations

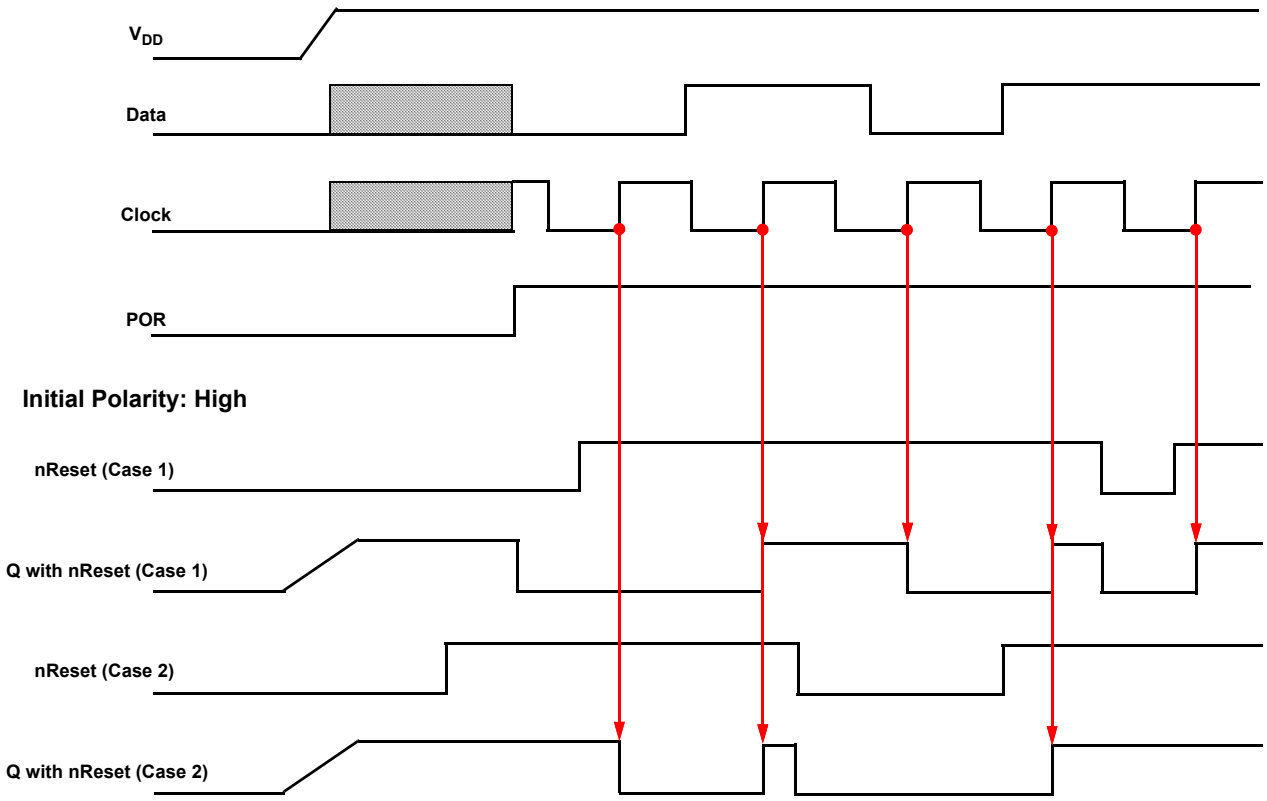


Figure 22. DFF Polarity Operations

13.0 Counters/Delay Generators (CNT/DLY)

There are five configurable counters/delay generators in the SLG46169. Two of these counters/delay generators (CNT/DLY 0 and 1) are 14-bit, and three of the counters/delay generators (CNT/DLY 4, 5, 6) are 8-bit. For flexibility, each of these macrocells has a large selection of internal and external clock sources, as well as the option to chain from the output of the previous (N-1) CNT/DLY macrocell, to implement longer count / delay circuits.

One of the counter/delay generator macrocells (CNT/DLY 1) has two inputs from the connection matrix, one for Delay Input/Reset Input (Delay_In/Reset_In), and one for an external counter/clock source. Four of the counter/delay generator macrocells (CNT/DLY 0, 4, 5, 6) have one input from the connection matrix, which has a shared function of either a Delay Input or an external clock input.

CNT/DLY6 has one extra output on which a short pulse will be generated according to the configured edge on the input signal if detected.

Note that there are also two Combination Function Macrocells that can implement either 4-bit LUTs or 8-bit counter / delays, For more information please see Section *10.4 4-Bit LUT or 8- Bit Counter / Delay Macrocells*.

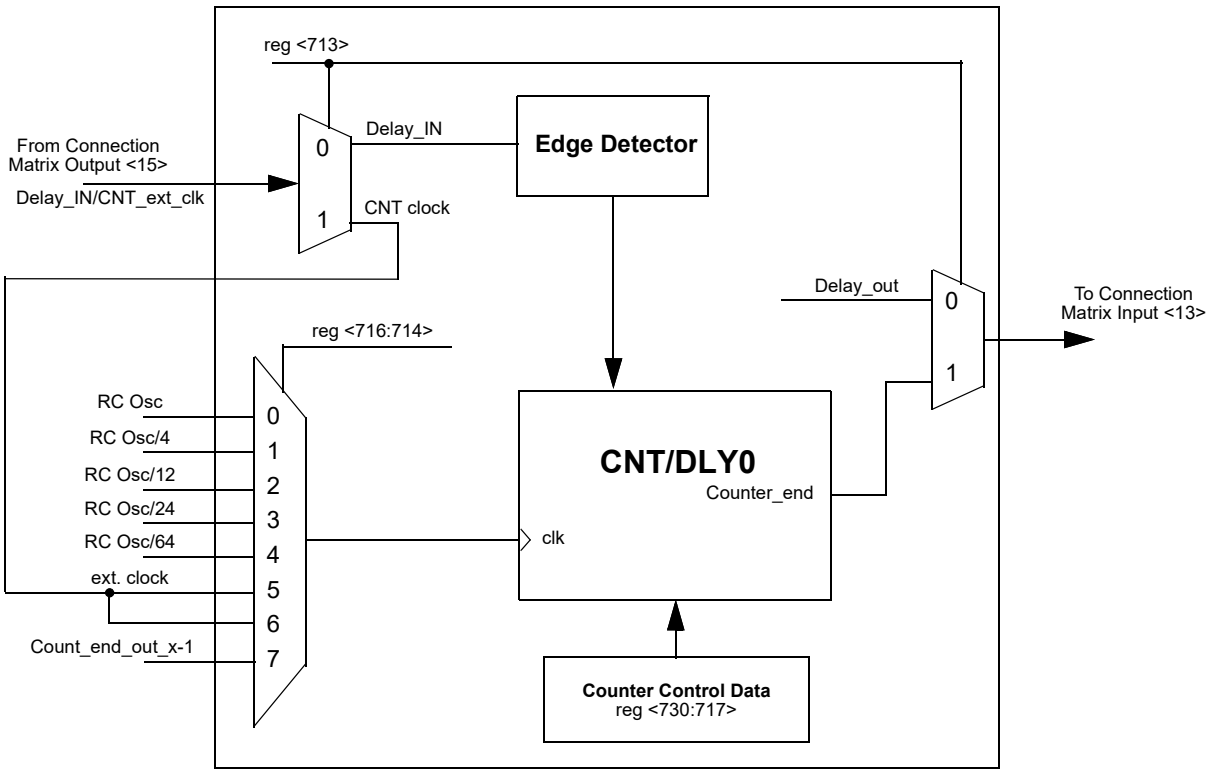


Figure 23. CNT/DLY0

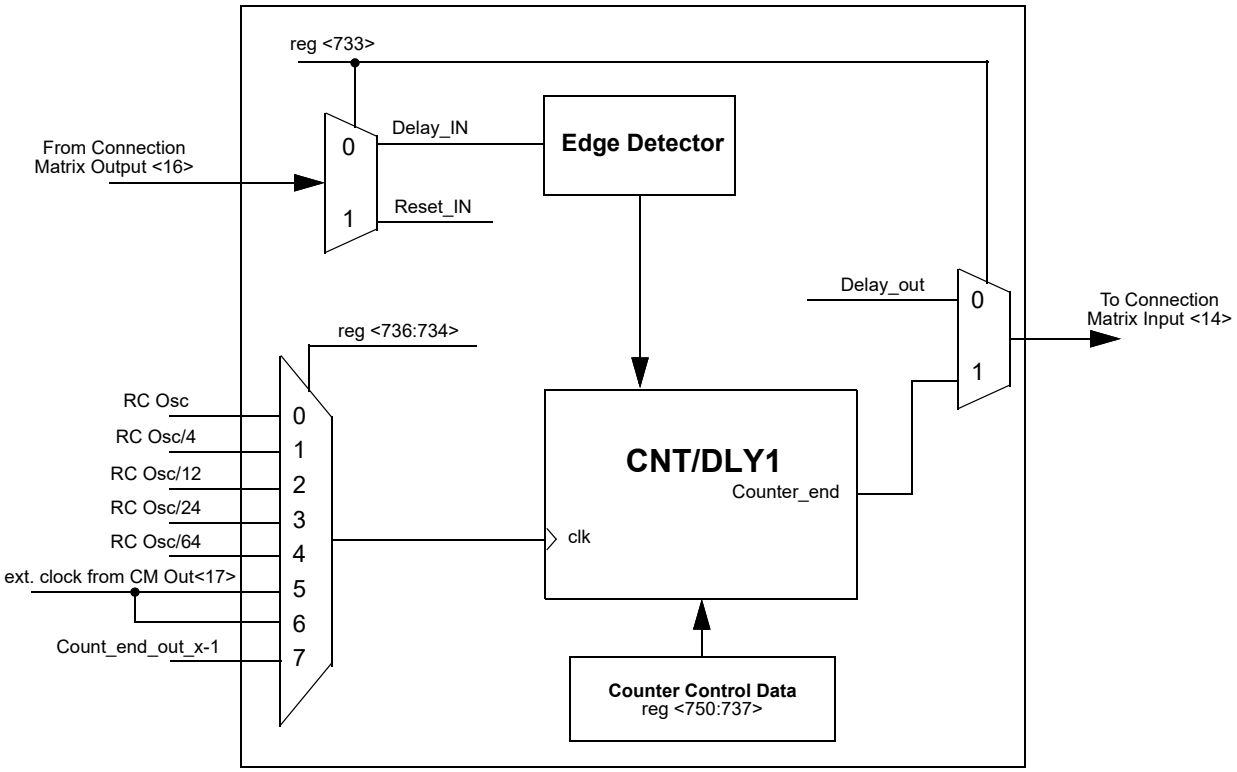


Figure 24. CNT/DLY1

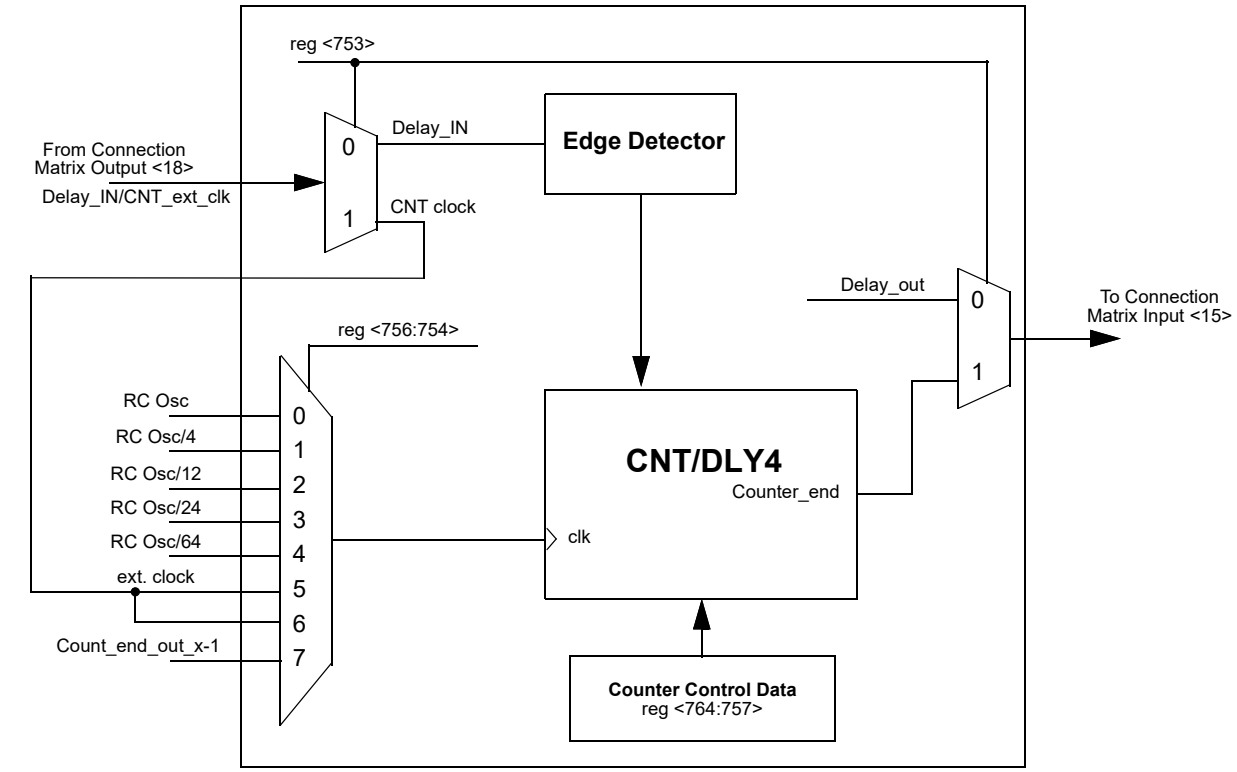


Figure 25. CNT/DLY4

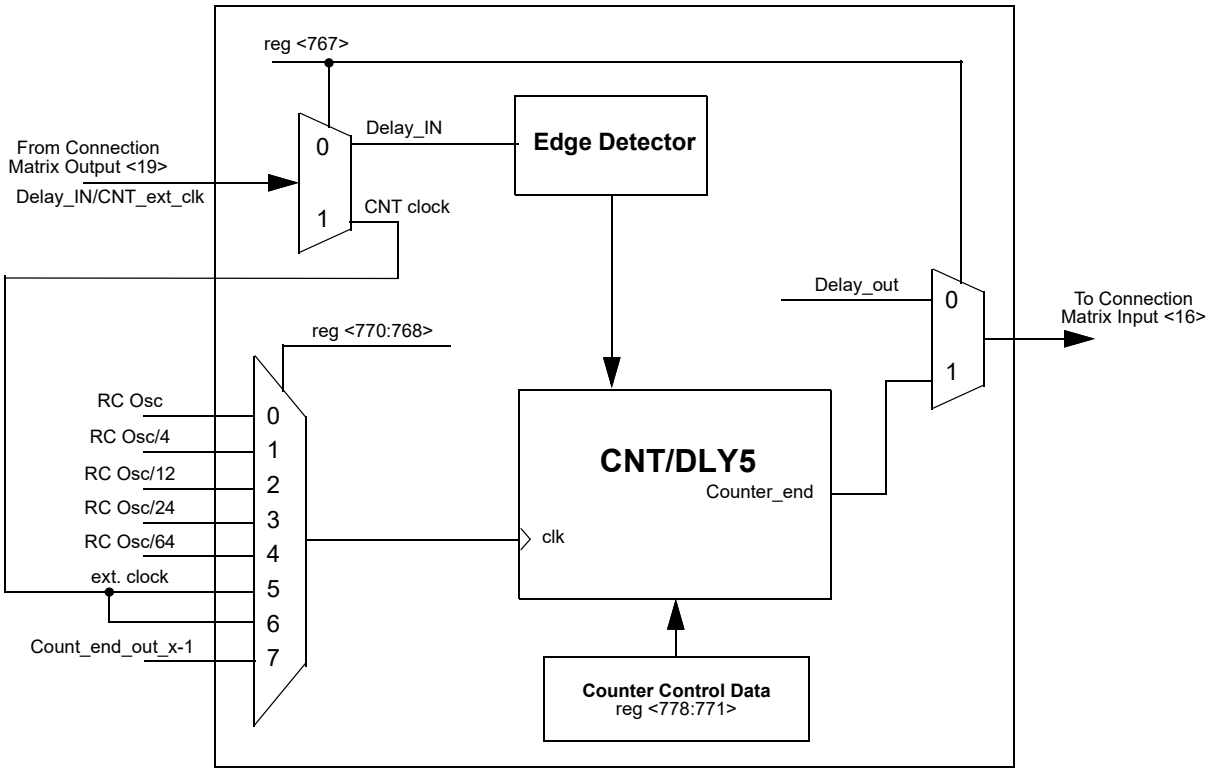


Figure 26. CNT/DLY5

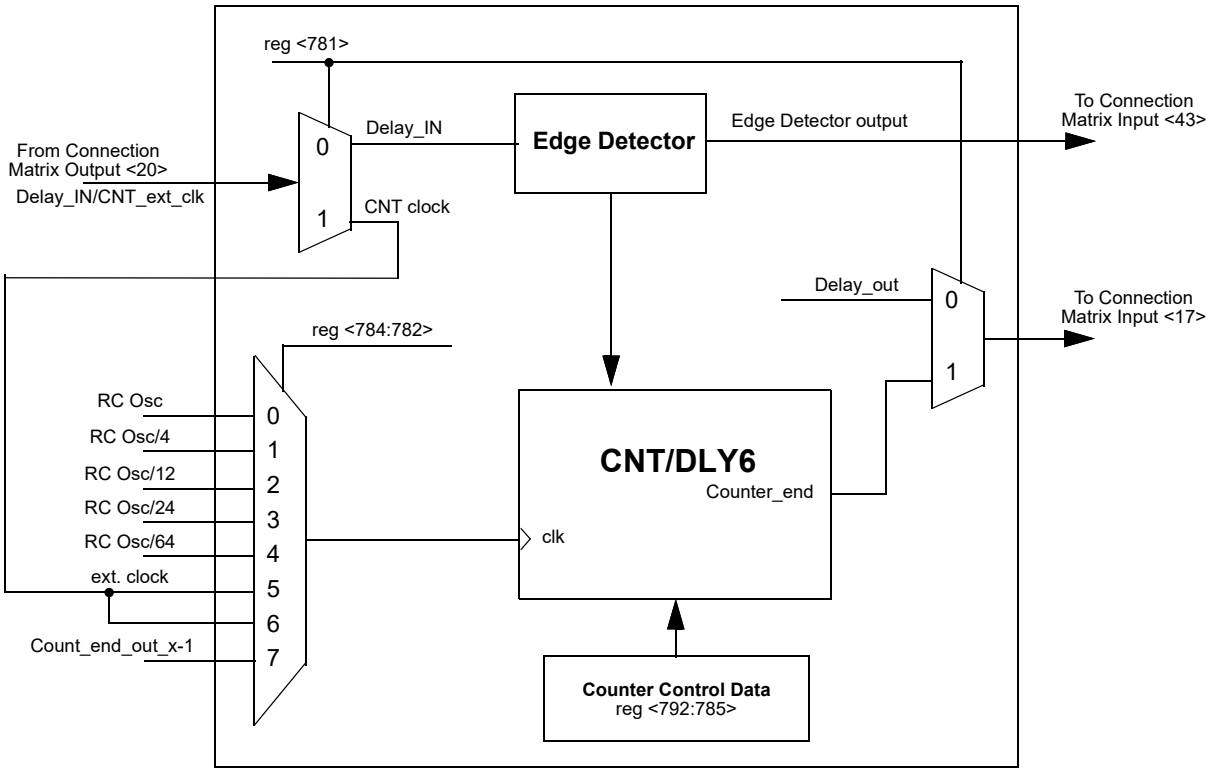


Figure 27. CNT/DLY6

13.1 CNT/DLY Timing Diagrams

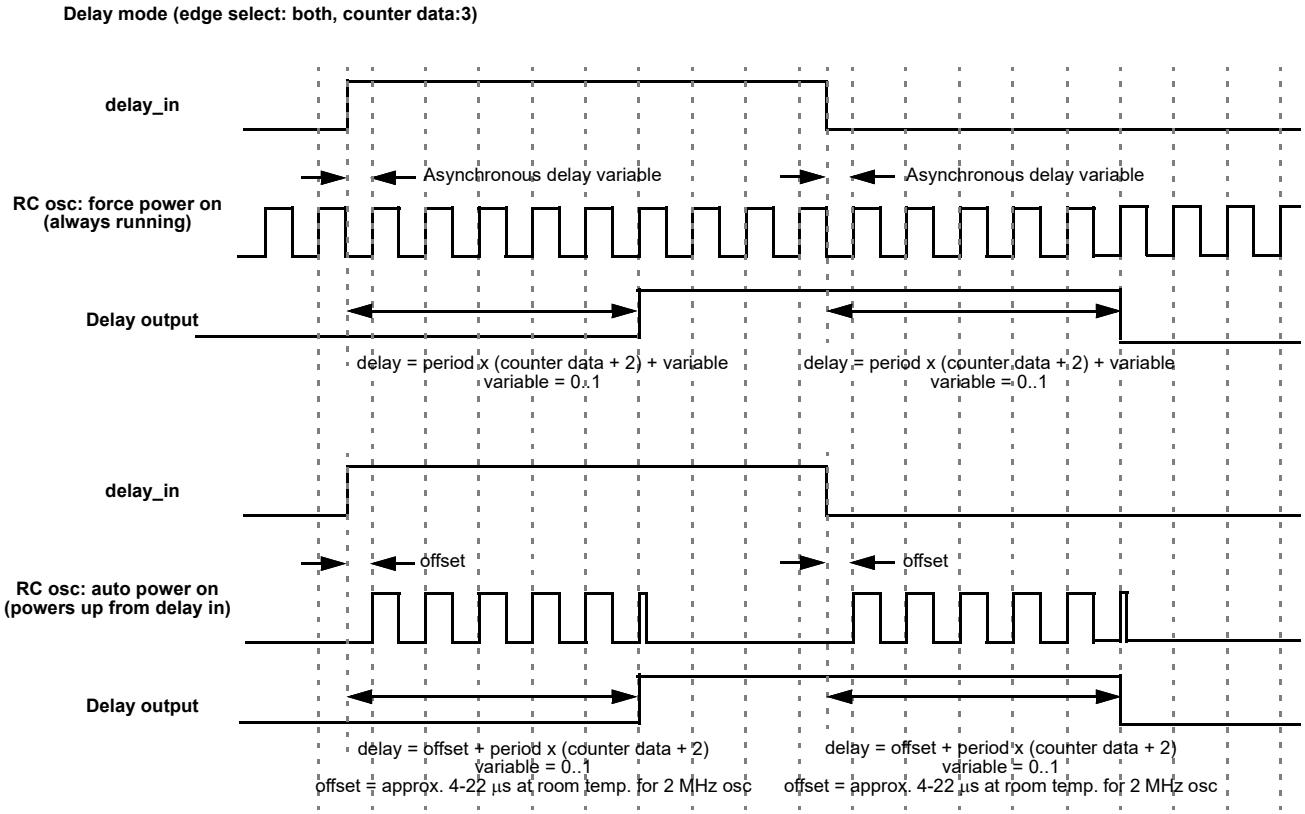


Figure 28. Delay Mode Timing

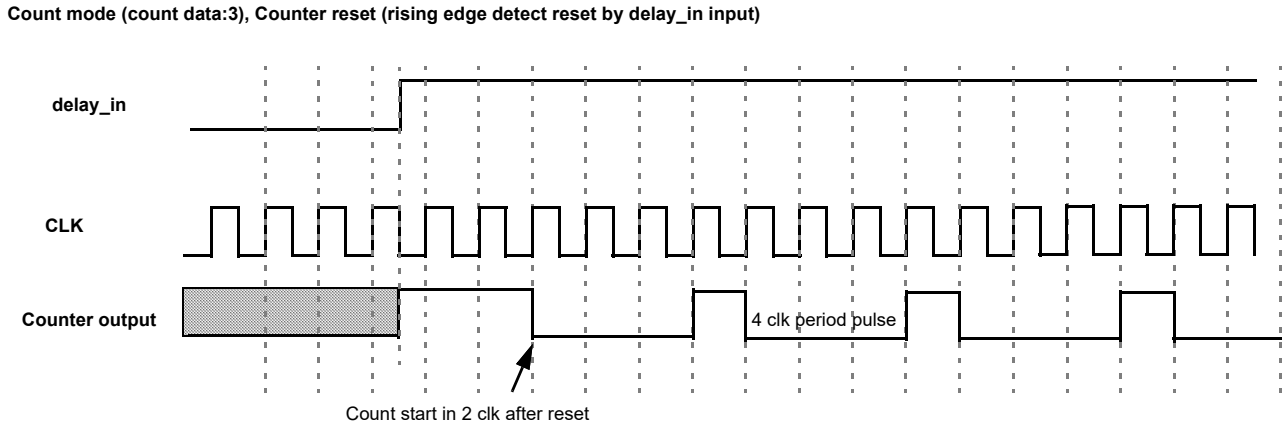


Figure 29. Counter Mode Timing

13.2 CNT/DLY0 Register Settings

Table 60. CNT/DLY0 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay0 Mode Select	reg<713>	0: Delay Mode 1: Counter Mode
Counter/Delay0 Clock Source Select (external clock is only for counter mode)	reg<716:714>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter6 Overflow
Counter0 Control Data/Delay0 Time Control	reg<730:717>	1-16384: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay0 Mode Select	reg<732:731>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

13.3 CNT/DLY1 Register Settings

Table 61. CNT/DLY1 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay1 Mode Select	reg<733>	0: Delay Mode 1: Counter Mode
Counter/Delay1 Clock Source select	reg<736:734>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter0 Overflow
Counter1 Control Data/Delay1 Time Control	reg<750:737>	1-16384: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay1 Mode Select or asynchronous counter reset	reg<752:751>	00: Delay on both falling and rising edges (for delay & counter reset) 01: Delay on falling edge only (for delay & counter reset) 10: Delay on rising edge only (for delay & counter reset) 11: No delay on either falling or rising edges / high level reset for counter mode

13.4 CNT/DLY4 Register Settings

Table 62. CNT/DLY4 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay4 Mode Select	reg<753>	0: Delay Mode 1: Counter Mode
Counter/Delay4 Clock Source Select (external clock is only for counter mode)	reg<756:754>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Reserved
Counter4 Control Data/Delay4 Time Control	reg<764:757>	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay4 Mode Select	reg<766:765>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

13.5 CNT/DLY5 Register Settings

Table 63. CNT/DLY5 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay5 Mode Select	reg<767>	0: Delay Mode 1: Counter Mode
Counter/Delay5 Clock Source Select (external clock is only for counter mode)	reg<770:768>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter4 Overflow
Counter5 Control Data/Delay5 Time Control	reg<778:771>	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay5 Mode Select	reg<780:779>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

13.6 CNT/DLY6 Register Settings

Table 64. CNT/DLY6 Register Settings

Signal Function	Register Bit Address	Register Definition
Counter/Delay6 Mode Select	reg<781>	0: Delay Mode 1: Counter Mode
Counter/Delay6 Clock Source Select (external clock is only for counter mode)	reg<784:782>	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: Reserved 111: Counter5 Overflow
Counter6 Control Data/Delay6 Time Control	reg<792:785>	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
Delay6 Mode Select	reg<794:793>	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

14.0 Pipe Delay (PD)

The SLG46169 has a pipe delay logic cell that is shared with the 3-bit LUT8 in one of the Combination Function macrocells. The user can select one of these functions to use in a design, but not both. Please see Section *10.3 3-Bit LUT or Pipe Delay Macrocell* for the description of this Combination Function macrocell.

15.0 Programmable Delay / Edge Detector

The SLG46169 has a programmable time delay logic cell available that can generate a delay that is selectable from one of four timings (time1) configured in the GreenPAK Designer. The programmable time delay cell can generate one of four different delay patterns, rising edge detection, falling edge detection, both edge detection and both edge delay. These four patterns can be further modified with the addition of delayed edge detection, which adds an extra unit of delay as well as glitch rejection during the delay period. See the timing diagrams below for further information.

Note: *The input signal must be longer than the delay, otherwise it will be filtered out.*

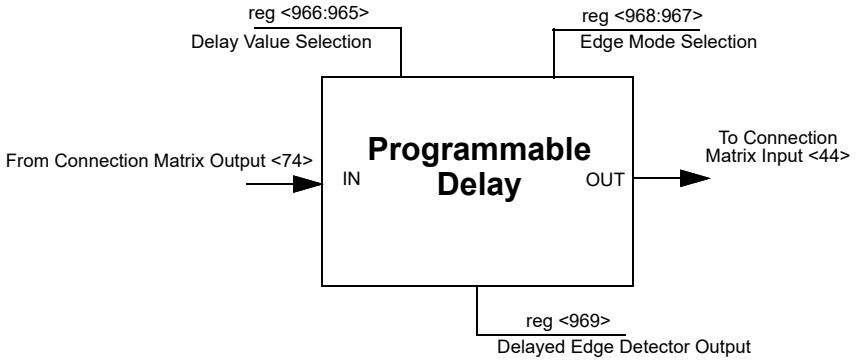


Figure 30. Programmable Delay

15.1 Programmable Delay Timing Diagram - Edge Detector Output

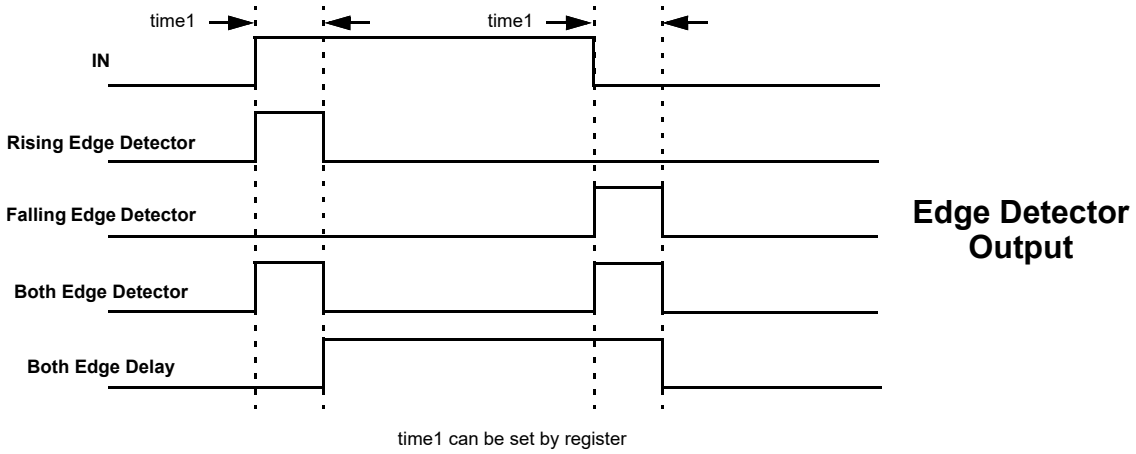


Figure 31. Edge Detector Output

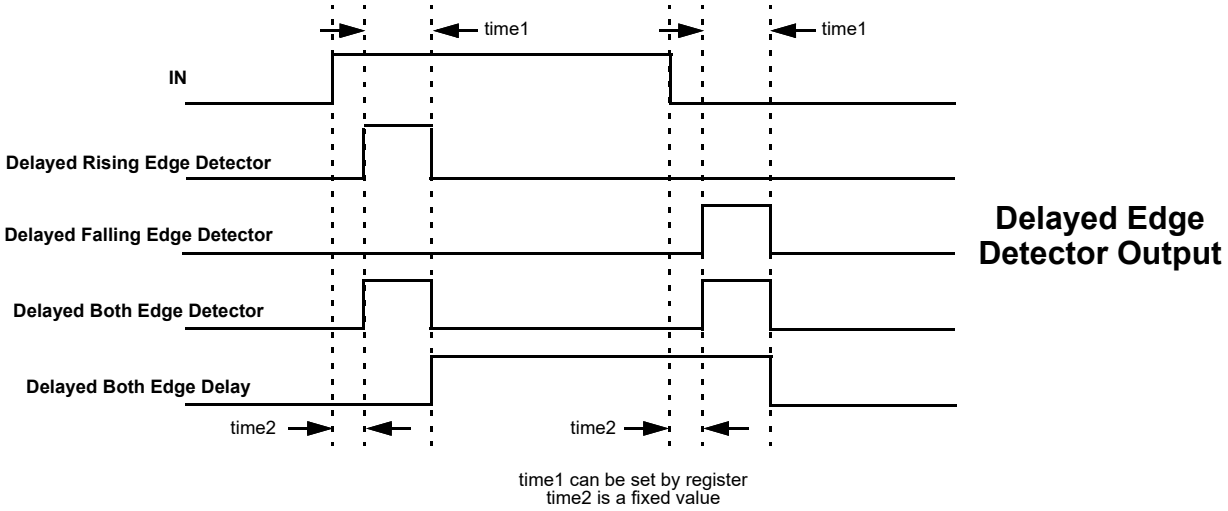


Figure 32. Delayed Edge Detector Output

Note: For delays and widths refer to Table 4.

15.2 Programmable Delay Timing Diagram - Glitch Filtering For Edge Detector Output

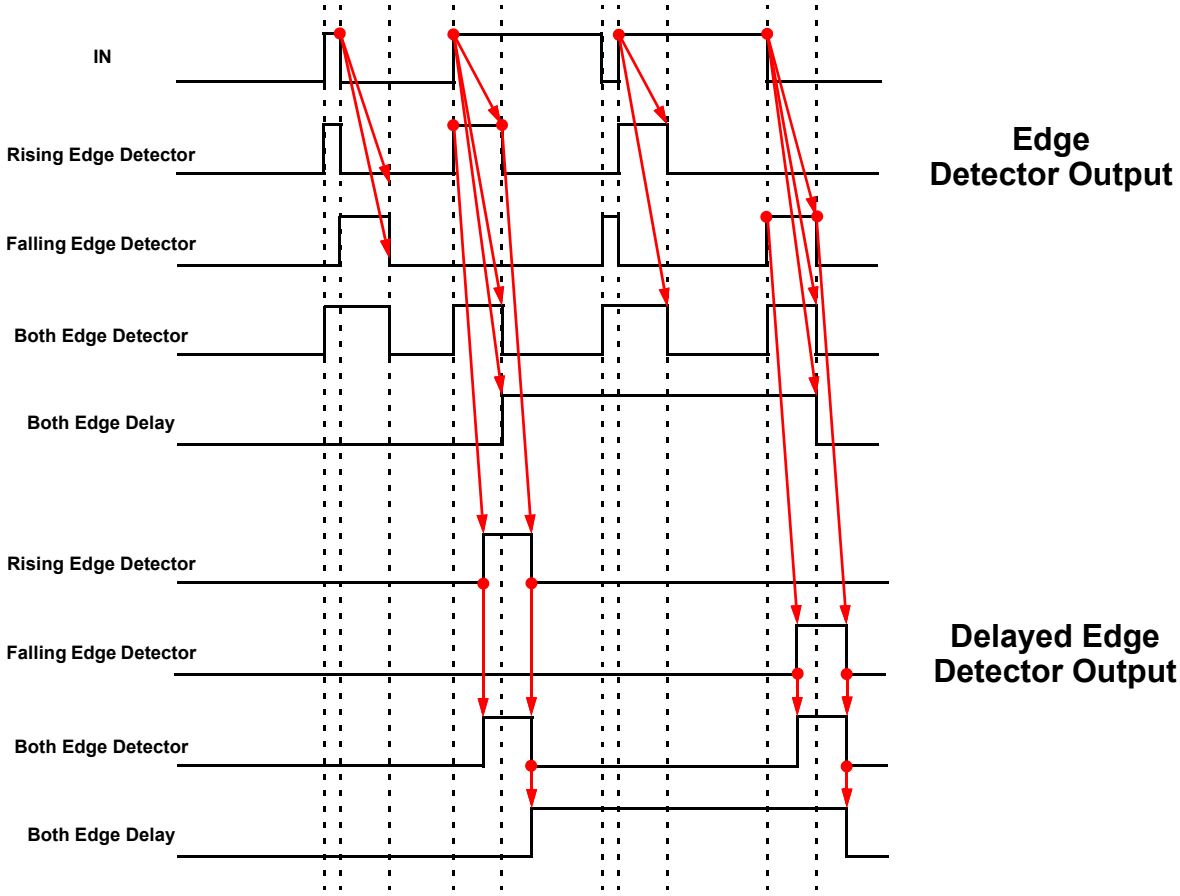


Figure 33. Glitch Filtering for Edge Detector Output

15.3 Programmable Delay Register Settings

Table 65. Programmable Delay Register Settings

Signal Function	Register Bit Address	Register Definition
Delay value select for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	reg<966:965>	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
Select the edge mode of programmable delay & edge detector	reg<968:967>	00: Rising Edge Detector 01: Falling Edge Detector 10: Both Edge Detector 11: Both Edge Delay
Select edge detector output mode	reg<969>	0: Non-Delayed Output 1: Delayed Output

16.0 Additional Logic Functions

The SLG46169 has four additional logic functions that are connected directly to the Connection Matrix inputs and outputs. There are two inverters, which can switch the polarity of any Connection Matrix signal, and there are also two deglitch filters.

16.1 Inverter 0 (INV_0 Gate)

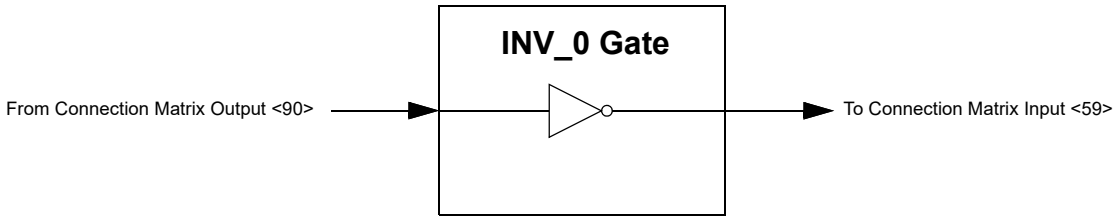


Figure 34. INV_0 Gate

16.2 Inverter 1 (INV_1 Gate)

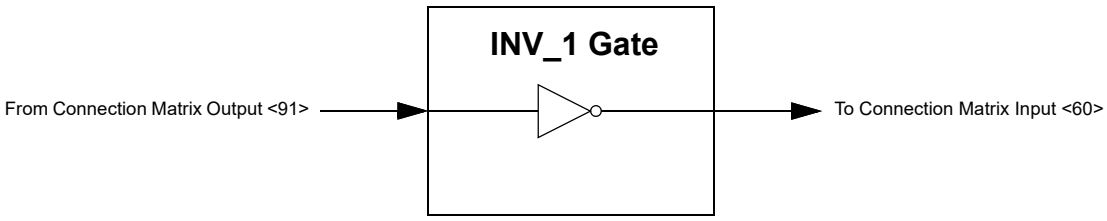


Figure 35. INV_1 Gate

16.3 Deglitch Filter

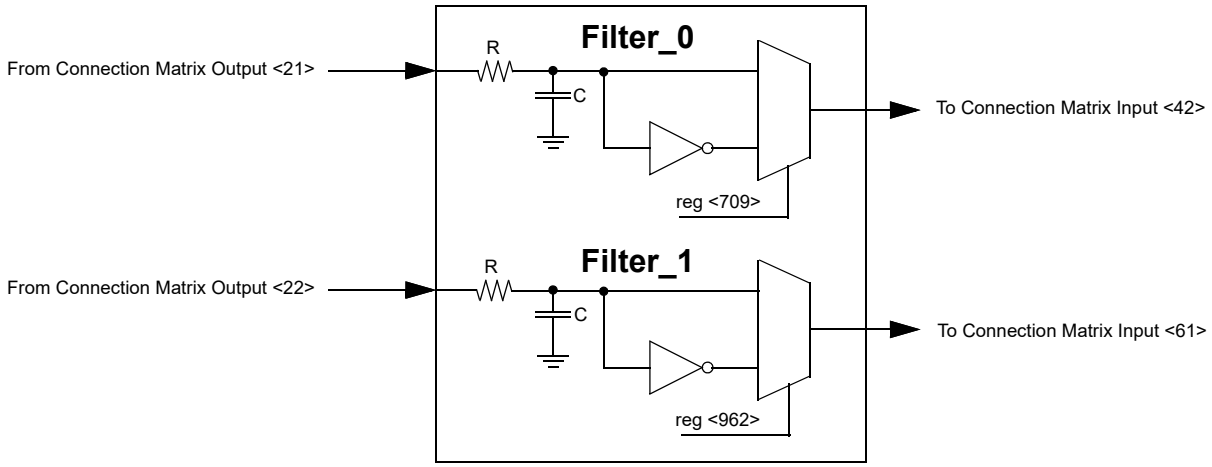


Figure 36. Deglitch Filter

17.0 Voltage Reference (VREF)

17.1 Voltage Reference Overview

The SLG46169 has a Voltage Reference Macrocell to provide references to the two analog comparators. This macrocell can supply a user selection of fixed voltage references, /3 and /4 reference off of the V_{DD} power supply to the device, and externally supplied voltage references from PIN 6. The macrocell also has the option to output reference voltages on PIN 12 and PIN 13. See table below for the available selections for each analog comparator. Also see *Figure 37.* below, which shows the reference output structure.

17.2 VREF Selection Table

Table 66. VREF Selection Table.

SEL<4:0>	ACMP0_VREF	ACMP1_VREF
11011	PIN 6: ACMP0(-)	Reserved
11001	V_{DD} / 4	V_{DD} / 4
11000	V_{DD} / 3	V_{DD} / 3
10111	1.20	1.20
10110	1.15	1.15
10101	1.10	1.10
10100	1.05	1.05
10011	1.00	1.00
10010	0.95	0.95
10001	0.90	0.90
10000	0.85	0.85
01111	0.80	0.80
01110	0.75	0.75
01101	0.70	0.70
01100	0.65	0.65
01011	0.60	0.60
01010	0.55	0.55
01001	0.50	0.50
01000	0.45	0.45
00111	0.40	0.40
00110	0.35	0.35
00101	0.30	0.30
00100	0.25	0.25
00011	0.20	0.20
00010	0.15	0.15
00001	0.10	0.10
00000	0.05	0.05

V_{DD}	Practial VREF Range	Note
2.0 V - 5.5 V	50 mV ~1.2 V	
1.7 V - 2.0 V	50 mV ~1.1 V	Do not operte above 1.1 V

17.3 VREF Block Diagram

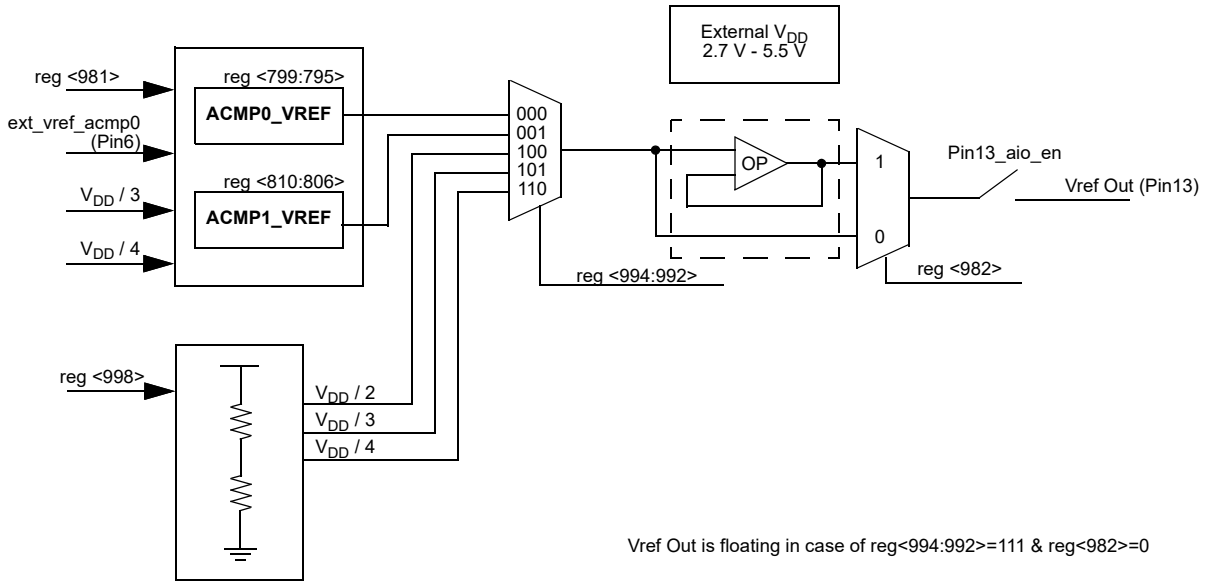


Figure 37. Voltage Reference Block Diagram

18.0 RC Oscillator (RC Osc)

18.1 RC Oscillator Overview

The SLG46169 has two internal RC oscillators, one that runs at 25 kHz and one that runs at 2 MHz. The user can select one of these fundamental frequencies for the RC OSC Macrocell, or the fundamental frequency can also come from an external clock input (PIN 14). There are two divider stages that allow the user flexibility for introducing clock signals on various Connection Matrix Input lines. The first stage divider allows the selection of /1, /2, /4 or /8 divide down frequency from the fundamental. The second stage divider has an input of one frequency from the first stage divider, and outputs five different frequencies on Connection Matrix Input lines <45>, <46>, <47>, <48>, and <49>. See *Figure 38.* below for details of the frequencies for each of these five Connection Matrix Inputs.

If PWR DOWN input of oscillator is LOW, the oscillator will be turned on. If PWR DOWN input of oscillator is HIGH the oscillator will be turned off. The PWR DOWN signal has the highest priority.

The user can select two OSC POWER MODEs (reg<707>):

- If **AUTO POWER ON** <0> is selected, the OSC will run when the SLG46169 is powered on.
- If **FORCE POWER ON** <1> is selected, the OSC will run only when any macrocell that uses OSC is powered on.

OSC can be turned on by:

- Register control (force power on)
- Delay mode, when delay requires OSC
- CNT

18.2 RC OSC Block Diagram

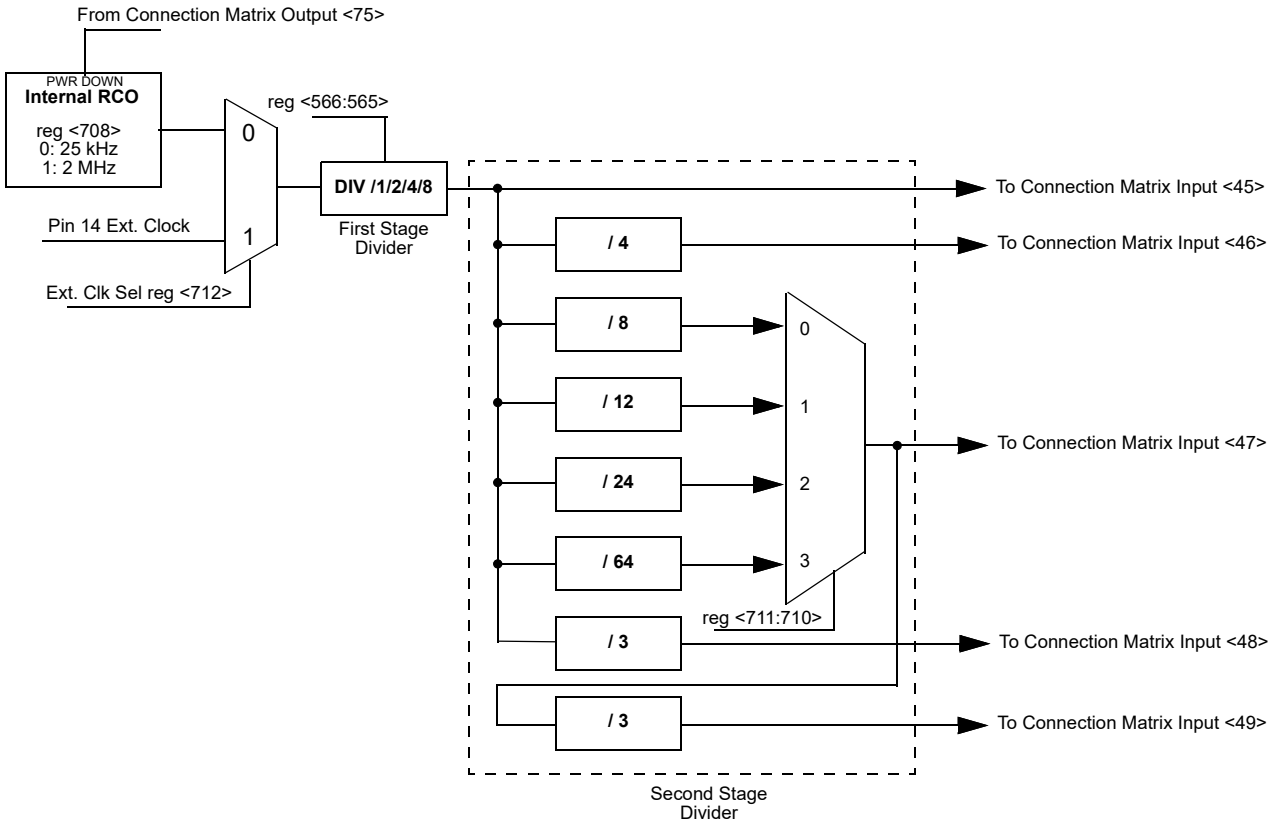


Figure 38. RC OSC Block Diagram

18.3 Oscillator Power On delay

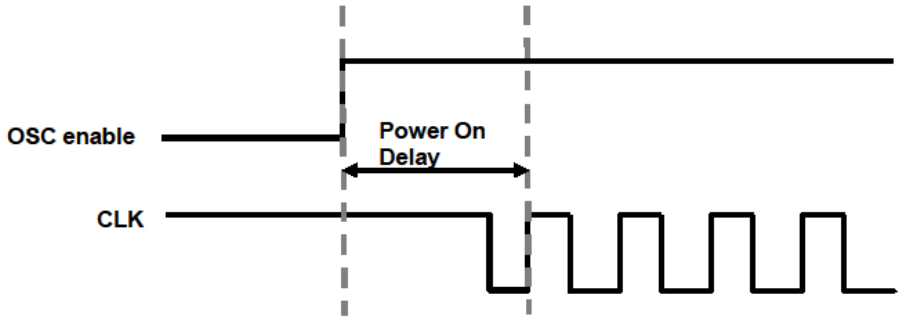


Figure 39. Oscillator Startup Diagram

Note 1: OSC power mode: "Auto Power On".

Note 2: 'OSC enable' signal appears when any macrocell that uses OSC is powered on.

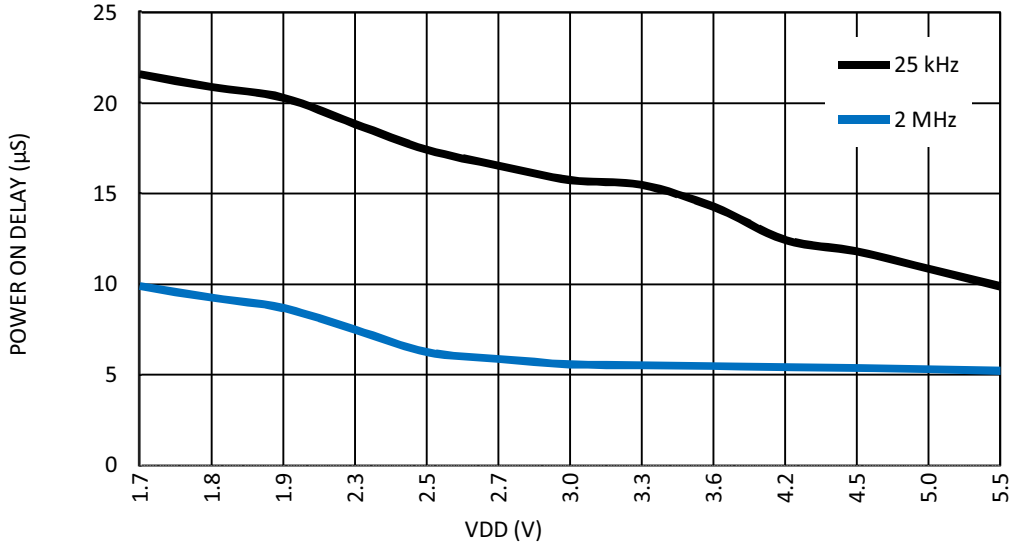


Figure 40. RC Oscillator Maximum Power On Delay vs. V_{DD} at room temperature

18.4 Oscillator Accuracy

Note: OSC power setting: Force Power On; Clock to matrix input - enable; Bandgap: turn on by register - enable.

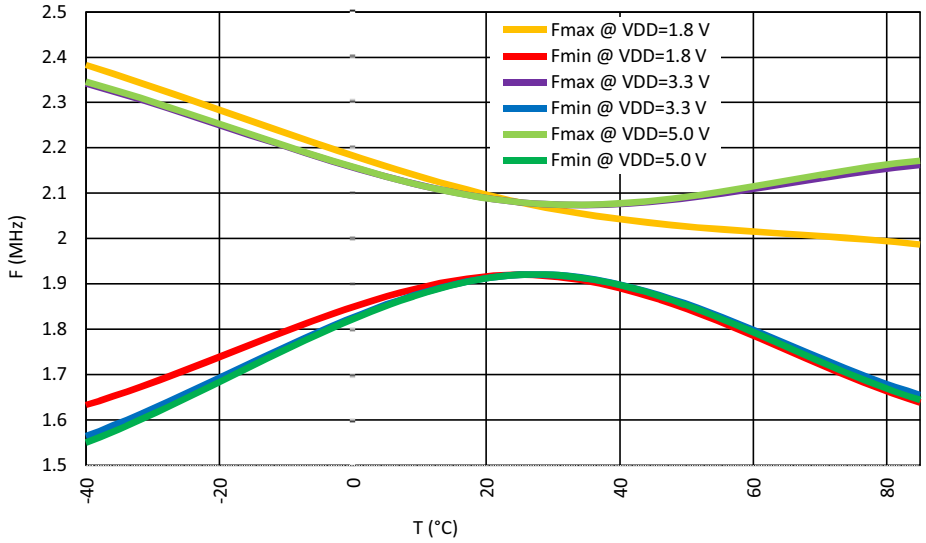


Figure 41. RC Oscillator Frequency vs. Temperature, RC OSC0=2 MHz

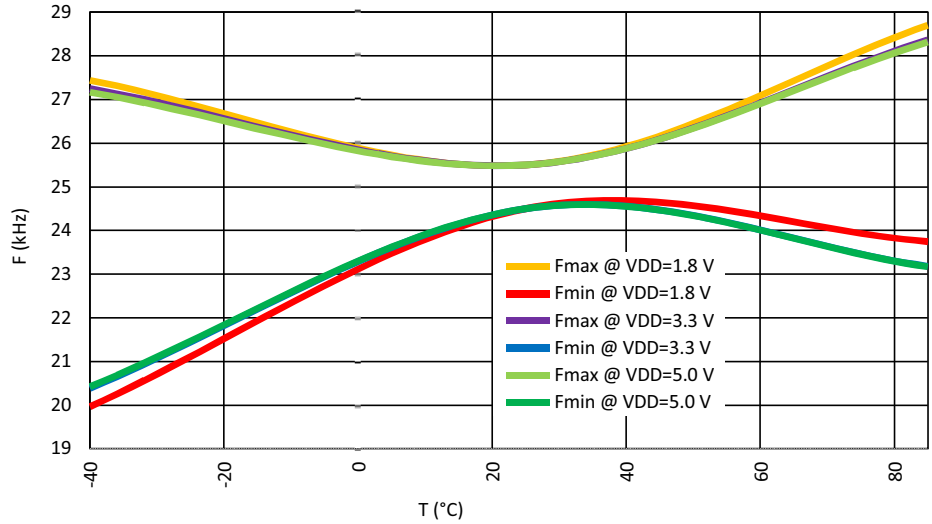


Figure 42. RC Oscillator Frequency vs. Temperature, RC OSC0=25 kHz

Note: For more information see section 5.10 OSC Specifications.

19.0 Power On Reset (POR)

19.1 POR Overview

The Power On Reset (POR) Macrocell will produce a high or “1” signal as an output when the device power supply (V_{DD}) rises to approximately 1.4 V. The typical internal delay for POR to release POR_IO will be 1 ms + α depending on the power slope, because there is adaptive power-up sequence. The next internal signal will be POR_CORE and then POR_IO_DLY, each of which is further delayed by approximately 1 µs. The rise of POR_IO_DLY will trigger the I/O pins to exit tri-state, and the device will become active.

19.2 POR Timing Diagram

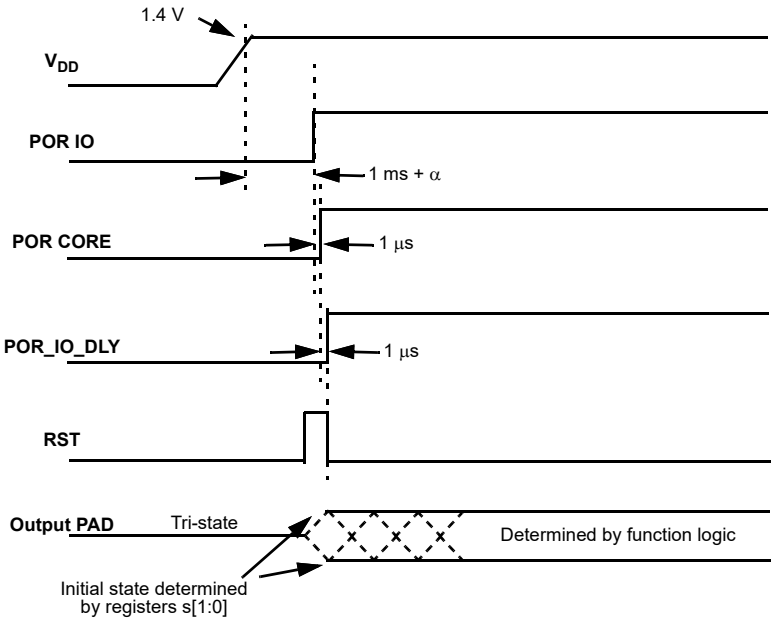


Figure 43. POR Timing Diagram

19.2.1 Initialization

All internal macrocells by default have initial low level. Starting from indicated powerup time of 1.15 V - 1.6 V, macrocells in GPAK3 are powered on while forced to the reset state, All outputs are in Hi-Z and chip starts loading data from NVM. Then the reset signal is released for internal macrocells and they start to initialize according to the following sequence:

1. Input PINs, ACMP, pull up/down;
2. LUTs;
3. DFFs, Delays/Counters, Pipe Delay;
4. POR output to matrix;
5. Output PIN corresponds to the internal logic

The VREF output pin driving signal can precede POR output signal going high by 3 µs - 5 µs. The POR signal going high indicates the mentioned powerup sequence is complete.

Note: The maximum voltage applied to any PIN should not be higher than the V_{DD} level. There are ESD Diodes between PIN –> V_{DD} and PIN –> GND on each PIN. So if the input signal applied to PIN is higher than V_{DD}, then current will sink through the diode to V_{DD}. Exceeding V_{DD} results in leakage current on the input PIN, and V_{DD} will be pulled up, following the voltage on the input PIN.There is no effect from input pin when input voltage is applied at the same time as V_{DD}.

19.2.2 Power Down

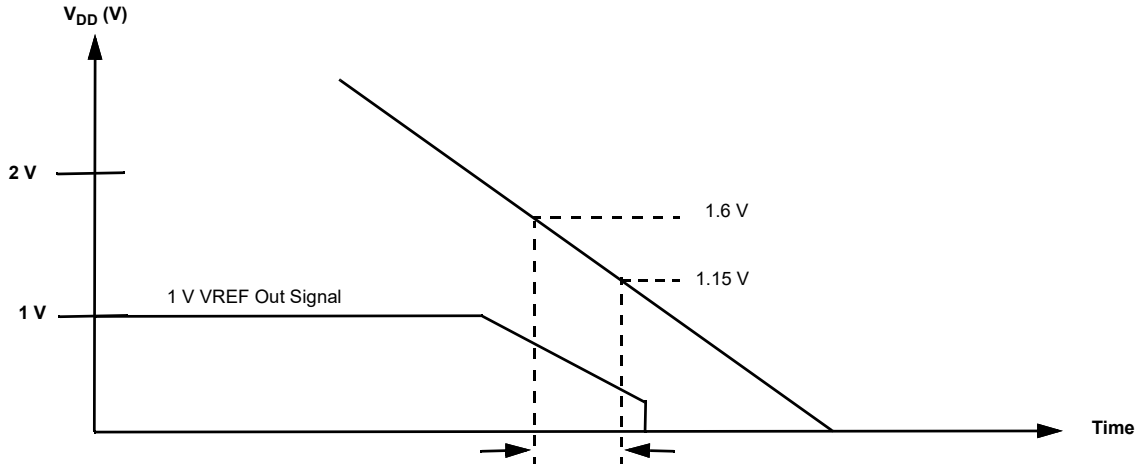


Figure 44. Power Down

During powerdown, macrocells in SLG46169 are powered off and logic macrocells may switch states after falling below 1.4 V. The I/O buffers are disabled when POR goes low at V_{DD}~1 V. Please note that during a slow rampdown, outputs can possibly switch state during this time.

20.0 Appendix A - SLG46169 Register Definition

Register Bit Address	Signal Function	Register Bit Definition
reg<5:0>	Reserved	
reg<11:6>	Reserved	
reg<17:12>	Matrix Out	PIN3 Digital Output Source
reg<23:18>	Matrix Out	PIN4 Digital Output Source
reg<29:24>	Matrix Out	Output Enable of PIN4
reg<35:30>	Matrix Out	PIN5 Digital Output Source
reg<41:36>	Matrix Out	PIN6 Digital Output Source
reg<47:42>	Matrix Out	Output Enable of PIN6
reg<53:48>	Reserved	
reg<59:54>	Matrix Out	PIN7 Digital Output Source
reg<65:60>	Matrix Out	Output Enable of PIN7
reg<71:66>	Matrix Out	PIN8 Digital Output Source (4X Drive)
reg<77:72>	Matrix Out	pdb (power down) for ACMP0
reg<83:78>	Matrix Out	pdb (power down) for ACMP1
reg<89:84>	Reserved	
reg<95:90>	Matrix Out	Input for delay0 or Counter0 external clock
reg<101:96>	Matrix Out	Input for delay1 or counter1 reset input
reg<107:102>	Matrix Out	Input for Counter1 external clock or delay1 external clock
reg<113:108>	Matrix Out	Input for delay4 or Counter4 external clock
reg<119:114>	Matrix Out	Input for delay5 or Counter5 external clock
reg<125:120>	Matrix Out	Input for delay6 or Counter6 external clock
reg<131:126>	Matrix Out	Input for filter_0
reg<137:132>	Matrix Out	Input for filter_1
reg<143:138>	Reserved	
reg<149:144>	Matrix Out	In0 of LUT3_9
reg<155:150>	Matrix Out	In1 of LUT3_9
reg<161:156>	Matrix Out	In2 of LUT3_9
reg<167:162>	Matrix Out	In0 of LUT4_0 or Input for Counter2(delay2) external clock
reg<173:168>	Matrix Out	In1 of LUT4_0 or Input for delay2(counter2 reset input)
reg<179:174>	Matrix Out	In2 of LUT4_0
reg<185:180>	Matrix Out	In3 of LUT4_0
reg<191:186>	Matrix Out	In0 of LUT4_1 or Input for Counter3(delay3) external clock
reg<197:192>	Matrix Out	In1 of LUT4_1 or Input for delay3(counter3 reset input)
reg<203:198>	Matrix Out	In2 of LUT4_1

Register Bit Address	Signal Function	Register Bit Definition
reg<209:204>	Matrix Out	In3 of LUT4_1
reg<215:210>	Matrix Out	In0 of LUT3_0
reg<221:216>	Matrix Out	In1 of LUT3_0
reg<227:222>	Matrix Out	In2 of LUT3_0
reg<233:228>	Matrix Out	In0 of LUT3_1
reg<239:234>	Matrix Out	In1 of LUT3_1
reg<245:240>	Matrix Out	In2 of LUT3_1
reg<251:246>	Matrix Out	In0 of LUT3_2 or Clock Input of DFF2
reg<257:252>	Matrix Out	In1 of LUT3_2 or Data Input of DFF2
reg<263:258>	Matrix Out	In2 of LUT3_2 or Resetb Input of DFF2
reg<269:264>	Matrix Out	In0 of LUT3_3 or Clock Input of DFF3
reg<275:270>	Matrix Out	In1 of LUT3_3 or Data Input of DFF3
reg<281:276>	Matrix Out	In2 of LUT3_3 or Resetb (Setb) of DFF3
reg<287:282>	Matrix Out	In0 of LUT3_4
reg<293:288>	Matrix Out	In1 of LUT3_4
reg<299:294>	Matrix Out	In2 of LUT3_4
reg<305:300>	Matrix Out	In0 of LUT3_5
reg<311:306>	Matrix Out	In1 of LUT3_5
reg<317:312>	Matrix Out	In2 of LUT3_5
reg<323:318>	Matrix Out	In0 of LUT3_6
reg<329:324>	Matrix Out	In1 of LUT3_6
reg<335:330>	Matrix Out	In2 of LUT3_6
reg<341:336>	Matrix Out	In0 of LUT3_7
reg<347:342>	Matrix Out	In1 of LUT3_7
reg<353:348>	Matrix Out	In2 of LUT3_7
reg<359:354>	Matrix Out	In0 of LUT3_8 or Input of Pipe delay
reg<365:360>	Matrix Out	In1 of LUT3_8 or Resetb of Pipe delay
reg<371:366>	Matrix Out	In2 of LUT3_8 or Clock of Pipe delay
reg<377:372>	Matrix Out	In0 of LUT2_0 or Clock Input of DFF4
reg<383:378>	Matrix Out	In1 of LUT2_0 or Data Input of DFF4
reg<389:384>	Matrix Out	In0 of LUT2_1 or Clock Input of DFF5
reg<395:390>	Matrix Out	In1 of LUT2_1 or Data Input of DFF5
reg<401:396>	Matrix Out	In0 of LUT2_2 or Clock Input of DFF6
reg<407:402>	Matrix Out	In1 of LUT2_2 or Data Input of DFF6
reg<413:408>	Matrix Out	In0 of LUT2_3 or Clock Input of DFF7
reg<419:414>	Matrix Out	In1 of LUT2_3 or Data Input of DFF7
reg<425:420>	Matrix Out	In0 of LUT2_4
reg<431:426>	Matrix Out	In1 of LUT2_4
reg<437:432>	Matrix Out	In0 of LUT2_5
reg<443:438>	Matrix Out	In1 of LUT2_5
reg<449:444>	Matrix Out	Input for programmable delay & edge detector
reg<455:450>	Matrix Out	Power down for osc

Register Bit Address	Signal Function	Register Bit Definition
reg<461:456>	Reserved	
reg<467:462>	Reserved	
reg<473:468>	Reserved	
reg<479:474>	Reserved	
reg<485:480>	Reserved	
reg<491:486>	Reserved	
reg<497:492>	Matrix Out	Pin10 Digital Output Source
reg<503:498>	Matrix Out	Pin10 Output Enable
reg<509:504>	Matrix Out	Pin11 Digital Output Source
reg<515:510>	Matrix Out	Pin12 Digital Output Source
reg<521:516>	Matrix Out	Pin12 Output Enable
reg<527:522>	Matrix Out	Pin13 Digital Output Source
reg<533:528>	Matrix Out	Pin13 Output Enable
reg<539:534>	Matrix Out	Pin14 Digital Output Source
reg<545:540>	Matrix Out	Input of INV_0
reg<551:546>	Matrix Out	Input of INV_1
reg<556:552>	Reserved	
reg<558:557>	Reserved	
reg<560:559>	Reserved	
reg<561>	Reserved	
reg<562>	Reserved	
reg<563>	Reserved	
reg<564>	V_{DD} bypass enable	0: Regulator auto on 1: Regulator off (V_{DD} bypass)
reg<566:565>	OSC clock pre-divider	00: Div1 01: Div2 10: Div4 11: Div8
reg<568:567>	Reserved	Reserved
reg<569>	Analog buffer at ACMP0 enable	0: Disable analog buffer 1: Enable analog buffer
reg<570>	Analog buffer at ACMP1 enable	0: Disable analog buffer 1: Enable analog buffer

Register Bit Address	Signal Function	Register Bit Definition
reg<574:571>	LUT2_0 Data (if reg.<595>=0) or DFF4 / Latch Select	
	reg<571> DFF4 or Latch select	0: DFF function 1: Latch function
	reg<572> DFF4 output select	0: Q output 1: nQ output
	reg<573> DFF4 initial polarity select	0: Low 1: High
reg<578:575>	LUT2_1 Data (if reg.<596>=0) or DFF5 / Latch Select	
	reg<575> DFF5 or Latch select	0: DFF function 1: Latch function
	reg<576> DFF5 output select	0: Q output 1: nQ output
	reg<577> DFF5 initial polarity select	0: Low 1: High
reg<582:579>	LUT2_2 Data (if reg.<597>=0) or DFF6 / Latch Select	
	reg<579> DFF6 or Latch select	0: DFF function 1: Latch function
	reg<580> DFF6 output select	0: Q output 1: nQ output
	reg<581> DFF6 initial polarity select	0: Low 1: High
reg<586:583>	LUT2_3 Data (if reg.<598>=0) or DFF7 / Latch Select	
	reg<583> DFF7 or Latch select	0: DFF function 1: Latch function
	reg<584> DFF7 output select	0: Q output 1: nQ output
	reg<585> DFF7 initial polarity select	0: Low 1: High
reg<590:587>	LUT2_4 data	
reg<594:591>	LUT2_5 data	
reg<595>	LUT2_0 or DFF4 select	0: LUT2_0 1: DFF4
reg<596>	LUT2_1 or DFF5 select	0: LUT2_1 1: DFF5
reg<597>	LUT2_2 or DFF6 select	0: LUT2_2 1: DFF6
reg<598>	LUT2_3 or DFF7 select	0: LUT2_3 1: DFF7
reg<606:599>	LUT3_0 data	
reg<614:607>	LUT3_1 data	
reg<622:615>	LUT3_2 Data (if reg.<671>=0) or DFF2 / Latch Select)	
	reg<615> DFF2 or Latch select	0: DFF function 1: Latch function
	reg<616> DFF2 output select	0: Q output 1: nQ output
	reg<617> DFF2 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
	reg<618> DFF2 initial polarity select	0: Low 1: High

Register Bit Address	Signal Function	Register Bit Definition
reg<630:623>	LUT3_3 Data (if reg.<672>=0) or DFF3 / Latch Select	
	reg<623> DFF3 or Latch select	0: DFF function 1: Latch function
	reg<624> DFF3 output select	0: Q output 1: nQ output
	reg<625> DFF3 rstb/setb select	0: resetb from matrix output 1: setb from matrix output
	reg<626> DFF3 initial polarity select	0: Low 1: High
reg<638:631>	LUT3_4 data	
reg<646:639>	LUT3_5 data	
reg<654:647>	LUT3_6 data	
reg<662:655>	LUT3_7 data	
reg<670:663>	LUT3_8 data or pipe number select	
	reg<666:663>: OUT0 select	
	reg<670:667>: OUT1 select	
reg<671>	LUT3_2 or DFF2 select	0: LUT3_2 1: DFF2
reg<672>	LUT3_3 or DFF3 select	0: LUT3_3 1: DFF3
reg<688:673>	LUT4_0 data or Counter / Delay 2 mode selection	
	reg<673> Counter/delay2 mode selection	0: Delay Mode 1: Counter Mode
	reg<676:674> Counter/delay2 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter1 Overflow
	reg<684:677> Counter/delay2 Control Data	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
	reg<686:685> Delay2 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset

Register Bit Address	Signal Function	Register Bit Definition
reg<704:689>	LUT4_1 data or Counter / Delay 3 mode selection	
	reg<689> Counter/delay3 mode selection	0: Delay Mode 1: Counter Mode
	reg<692:690> Counter/delay3 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter2 Overflow
	reg<700:693> Counter/delay3 Control Data	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
	reg<702:701> Delay3 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset
reg<705>	LUT4_0 or Counter2 select	0: LUT4_0 1: Counter2
reg<706>	LUT4_1 or Counter3 select	0: LUT4_1 1: Counter3
reg<707>	Force RC oscillator on	0: Auto Power on 1: Force Power on
reg<708>	RC Oscillator frequency control	0: 25 k 1: 2 M
reg<709>	Filter_0 output polarity select	0: Filter_0 output 1: Filter_0 output inverted
reg<711:710>	Internal Oscillator frequency divider control	00: OSC/8 01: OSC/12 10: OSC/24 11: OSC/64
reg<712>	External Clock Source Select	0: Internal Oscillator 1: External Clock from Pin20
reg<713>	Counter/delay0 mode selection	0: Delay Mode 1: Counter Mode
reg<716:714>	Counter/delay0 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter6 Overflow
reg<730:717>	Counter0 Control Data/Delay0 Time Control	1-16384: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
reg<732:731>	Delay0 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges

Register Bit Address	Signal Function	Register Bit Definition
reg<733>	Counter/delay1 mode selection	0: Delay Mode 1: Counter Mode
reg<736:734>	Counter/delay1 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter0 Overflow
reg<750:737>	Counter1 Control Data/Delay1 Time Control	1-16384: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
reg<752:751>	Delay1 Mode Select or asynchronous counter reset	00: on both falling and rising edges (for delay & counter reset) 01: on falling edge only (for delay & counter reset) 10: on rising edge only (for delay & counter reset) 11: no delay on either falling or rising edges / high level reset for counter mode
reg<753>	Counter/delay4 mode selection	0: Delay Mode 1: Counter Mode
reg<756:754>	Counter/delay4 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter3 Overflow
reg<764:757>	Counter4 Control Data/Delay4 Time Control	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
reg<766:765>	Delay4 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<767>	Counter/delay5 mode selection	0: Delay Mode 1: Counter Mode
reg<770:768>	Counter/delay5 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter4 Overflow
reg<778:771>	Counter5 Control Data/Delay5 Time Control	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
reg<780:779>	Delay5 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<781>	Counter/Delay6 output source select	0: Delay Output 1: Counter Output

Register Bit Address	Signal Function	Register Bit Definition
reg<784:782>	Counter/delay6 Clock Source select	000: Internal OSC Clock 001: OSC/4 010: OSC/12 011: OSC/24 100: OSC/64 101: External Clock 110: External Clock/8 111: Counter5 Overflow
reg<792:785>	Counter6 Control Data/Delay6 Time Control	1-256: (delay time = (counter data + 2 + variable)/freq), where 0 < variable < 1
reg<794:793>	Delay6 Mode Select	00: Delay on both falling and rising edges 01: Delay on falling edge only 10: Delay on rising edge only 11: No delay on either falling or rising edges
reg<799:795>	ACMP0 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: Reserved 11011: EXT_VREF(PIN6)
reg<801:800>	ACMP0 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
reg<803:802>	ACMP0 positive Input divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X
reg<804>	ACMP0 low bandwidth (Max: 1 MHz) enable	0: off 1: on
reg<805>	ACMP0 positive input source select V_{DD}	0: Disabled 1: Enabled
reg<810:806>	ACMP1 IN voltage select	00000: 50 mV 00001: 100 mV 00010: 150 mV 00011: 200 mV 00100: 250 mV 00101: 300 mV 00110: 350 mV 00111: 400 mV 01000: 450 mV 01001: 500 mV 01010: 550 mV 01011: 600 mV 01100: 650 mV 01101: 700 mV 01110: 750 mV 01111: 800 mV 10000: 850 mV 10001: 900 mV 10010: 950 mV 10011: 1 V 10100: 1.05 V 10101: 1.1 V 10110: 1.15 V 10111: 1.2 V 11000: V_{DD}/3 11001: V_{DD}/4 11010: Reserved 11011: Reserved

Register Bit Address	Signal Function	Register Bit Definition
reg<812:811>	ACMP1 hysteresis Enable	00: Disabled (0 mV) 01: Enabled (25 mV) 10: Enabled (50 mV) 11: Enabled (200 mV)
reg<814:813>	ACMP1 positive Input divider	00: 1.0X 01: 0.5X 10: 0.33X 11: 0.25X
reg<815>	Reserved	must be set to 0
reg<816>	ACMP1 low bandwidth (typ: Max.1 Mhz) enable	0: off 1: on
reg<817>	ACMP1 positive input source select PIN6	0: Disabled 1: Enabled
reg<822:818>	Reserved	
reg<824:823>	Reserved	
reg<826:825>	Reserved	
reg<827>	Reserved	
reg<828>	Reserved	
reg<830:829>	PIN2 mode control	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
reg<832:831>	PIN2 pull down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<834:833>	Reserved	
reg<836:835>	Reserved	
reg<838:837>	Reserved	
reg<839>	Reserved	
reg<842:840>	PIN3 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
reg<844:843>	PIN3 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<845>	PIN3 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<846>	PIN3 driver strength selection	0: 1X 1: 2X
reg<848:847>	PIN4 mode control (sig_pin4_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved

Register Bit Address	Signal Function	Register Bit Definition
reg<850:849>	PIN4 mode control (sig_pin4_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
reg<852:851>	PIN4 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<853>	PIN4 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<856:854>	PIN5 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
reg<858:857>	PIN5 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<859>	PIN5 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<860>	PIN5 driver strength selection	0: 1X 1: 2X
reg<862:861>	PIN6 mode control (sig_pin6_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
reg<864:863>	PIN6 mode control (sig_pin6_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
reg<866:865>	PIN6 pull up/down resistor value selection	00: Floating 01: 10 10: 100 K 11: 1 M
reg<867>	PIN6 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<870:868>	Reserved	
reg<872:871>	Reserved	
reg<873>	Reserved	
reg<874>	Reserved	
reg<876:875>	PIN7 mode control (sig_pin7_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
reg<878:877>	PIN7 mode control (sig_pin7_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

Register Bit Address	Signal Function	Register Bit Definition
reg<880:879>	PIN7 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<881>	PIN7 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<884:882>	PIN8 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Analog Input/Output 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Analog Input & Open Drain
reg<886:885>	PIN8 pull up/down resistor value selection	00: Floating 01: 10K 10: 100K 11: 1M
reg<887>	PIN8 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<888>	PIN8 driver strength selection	0: 1X 1: 2X
reg<889>	PIN8 4X Drive(4X, NMOS open drain) selection	0: 4X Drive off 1: 4X Drive on (if reg<884:882> = 101)
reg<892:890>	Reserved	
reg<894:893>	Reserved	
reg<895>	Reserved	
reg<896>	Reserved	
reg<897>	Reserved	
reg<899:898>	Reserved	
reg<901:900>	Reserved	
reg<903:902>	Reserved	
reg<904>	Reserved	
reg<906:905>	Reserved	
reg<908:907>	Reserved	
reg<910:909>	Reserved	
reg<911>	Reserved	
reg<914:912>	Reserved	
reg<916:915>	Reserved	
reg<917>	Reserved	
reg<918>	Reserved	

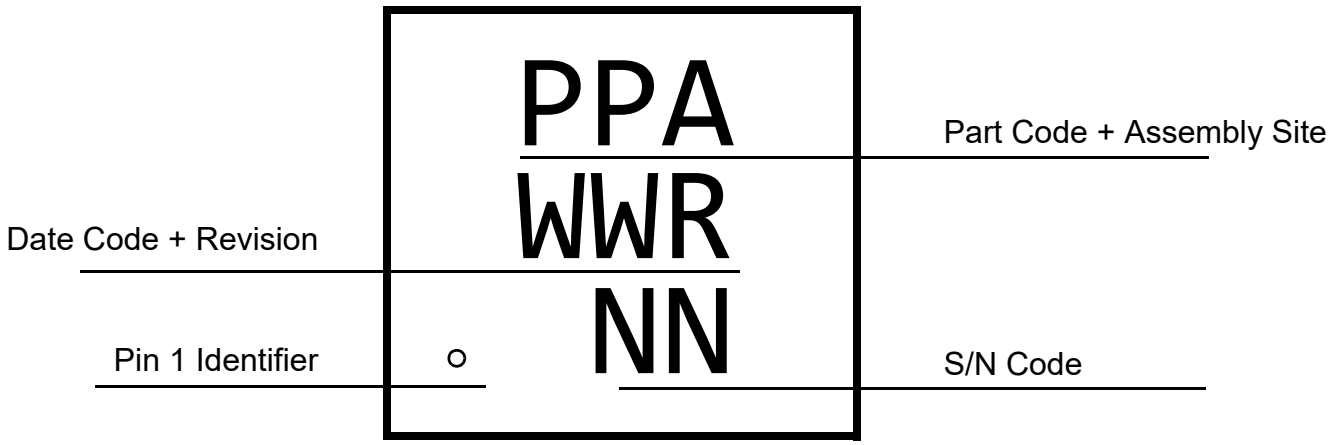
Register Bit Address	Signal Function	Register Bit Definition
reg<920:919>	PIN10 mode control (sig_pin10_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Reserved
reg<922:921>	PIN10 mode control (sig_pin10_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
reg<924:923>	PIN10 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<925>	PIN10 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<928:926>	PIN11 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
reg<930:929>	PIN11 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<931>	PIN11 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<932>	PIN11 driver strength selection	0: 1X 1: 2X
reg<934:933>	PIN12 mode control (sig_pin12_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
reg<936:935>	PIN12 mode control (sig_pin12_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X
reg<938:937>	PIN12 pull up/down resistor value selection	00: Floating 01: 10 K 10: 100 K 11: 1 M
reg<939>	PIN12 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<941:940>	PIN13 mode control (sig_pin13_oe =0)	00: Digital Input without Schmitt Trigger 01: Digital Input with Schmitt Trigger 10: Low Voltage Digital Input 11: Analog Input/Output
reg<943:942>	PIN13 mode control (sig_pin13_oe =1)	00: Push Pull 1X 01: Push Pull 2X 10: Open Drain NMOS 1X 11: Open Drain NMOS 2X

Register Bit Address	Signal Function	Register Bit Definition
reg<945:944>	PIN13 pull up/down resistor value selection	00: Floating 01: 10K 10: 100K 11: 1M
reg<946>	PIN13 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<949:947>	PIN14 mode control	000: Digital Input without Schmitt Trigger 001: Digital Input with Schmitt Trigger 010: Low Voltage Digital Input 011: Reserved 100: Push Pull 101: Open Drain NMOS 110: Open Drain PMOS 111: Open Drain NMOS
reg<951:950>	PIN14 pull up/down resistor value selection	00: Floating 01: 10K 10: 100K 11: 1M
reg<952>	PIN14 pull up/down resistor select	0: pull down resistor enable 1: pull up resistor enable
reg<953>	PIN14 driver strength selection	0: 1X 1: 2X
reg<961:954>	LUT3_9 data	
reg<962>	Filter_1 output polarity select	0: Filter_1 output 1: Filter_1 output inverted
reg<963>	LUT3_8 or pipe delay output select	0: LUT3_8 1: 1pipe delay output
reg<964>	Pipe delay OUT1 polarity select bit	0: non-inverted 1: inverted
reg<966:965>	Delay value select for programmable delay & edge detector (V_{DD} = 3.3 V, typical condition)	00: 125 ns 01: 250 ns 10: 375 ns 11: 500 ns
reg<968:967>	Select the edge mode of programmable delay & edge detector	00: rising edge detector 01: falling edge detector 10: both edge detector 11: both edge delay
reg<969>	Select edge detector output mode	0: edge detector output 1: delayed edge detector output
reg<977:970>	8-bit pattern id	
reg<978>	GPIO quick charge enable	0: Disable 1: Enable
reg<979>	NVM data read disable	0: Disable (program data can be read) 1: Enable (Program data cannot be read)
reg<980>	NVM power down	0: None (or programming enable) 1: Power Down (or programming disable)
reg<981>	Force bandgap on	0: Auto-mode 1: Enable
reg<982>	VREF Output Active Buffer Control	0: Disabled (bypass Active Buffer) 1: Enabled
reg<983>	Reserved	
reg<991:984>	Reserved	

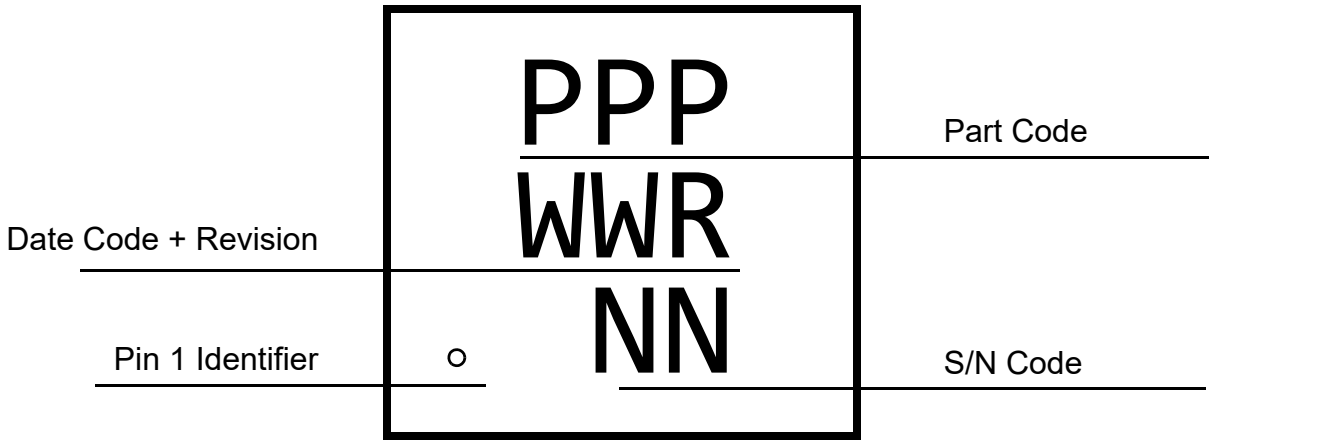
Register Bit Address	Signal Function	Register Bit Definition
reg<994:992>	VREF Output Source Select	000: ACMP0 reference voltage 001: ACMP1 reference voltage 100: $V_{DD}/2$ 101: $V_{DD}/3$ 110: $V_{DD}/4$ 111: Hi-Z
reg<997:995>	Reserved	
reg<998>	Power Divider Power	0: Power down 1: Power On
reg<999>	POR Auto Power detect	0: Enable 1: Disable
reg<1000>	Charge pump for analog macrocell enable (when V_{DD} <=2.7 V turn on)	0: Disable (automatic on/off control) 1: Enable (always on)
reg<1002:1001>	Reserved	
reg<1007:1003>	Reserved	
reg<1013:1008>	Reserved	
Reg<1015:1014>	Reserved	
reg<1023:1016>	Reserved	

21.0 Package Top Marking System Definition

21.1 Before February 1, 2021

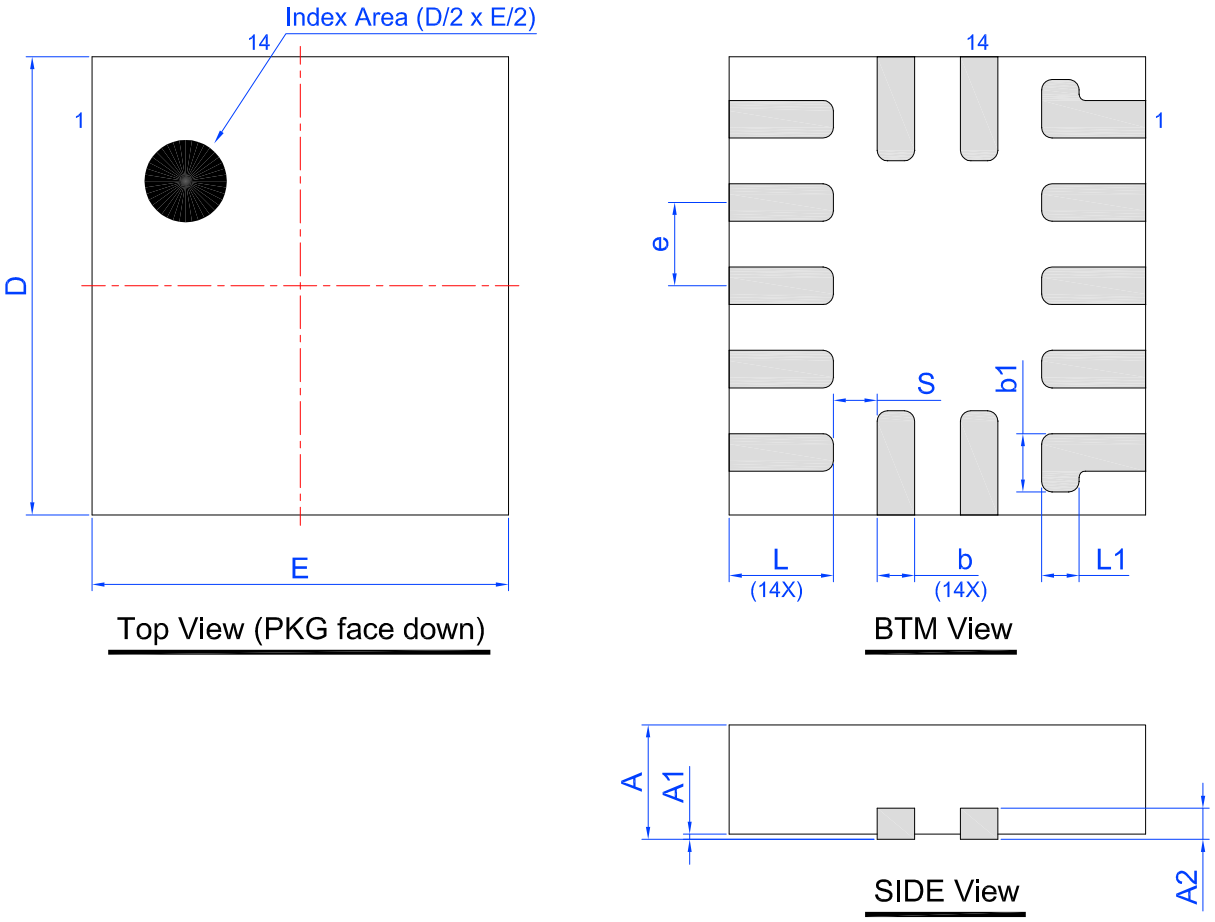


21.2 After February 1, 2021



22.0 Package Drawing and Dimensions

STQFN 14L 2 x 2.2 mm 0.4P COL Package
JEDEC MO-220, Variation WECE



Unit: mm

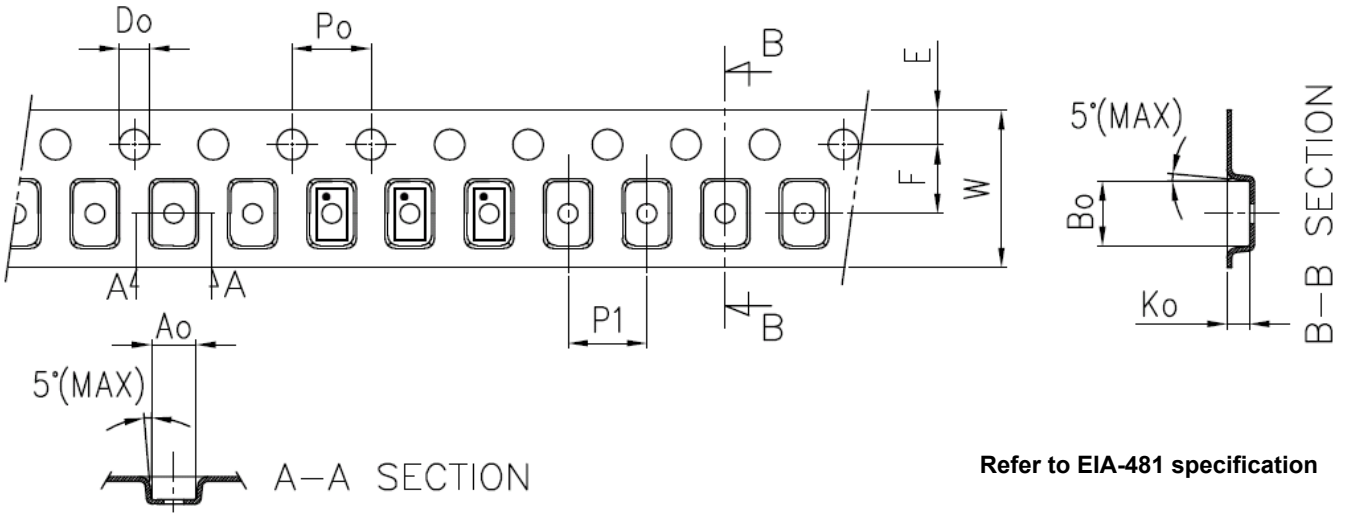
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.15	2.20	2.25
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.45	0.50	0.55
b	0.13	0.18	0.23	S	0.21 TYP		
e	0.40 BSC			b1	0.28 TYP		
				L1	0.18 TYP		

23.0 Tape and Reel Specifications

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 2x2.2 mm 0.4P COL	14	2 x 2.2 x 0.55	3,000	3,000	178 / 60	100	400	100	400	8	4

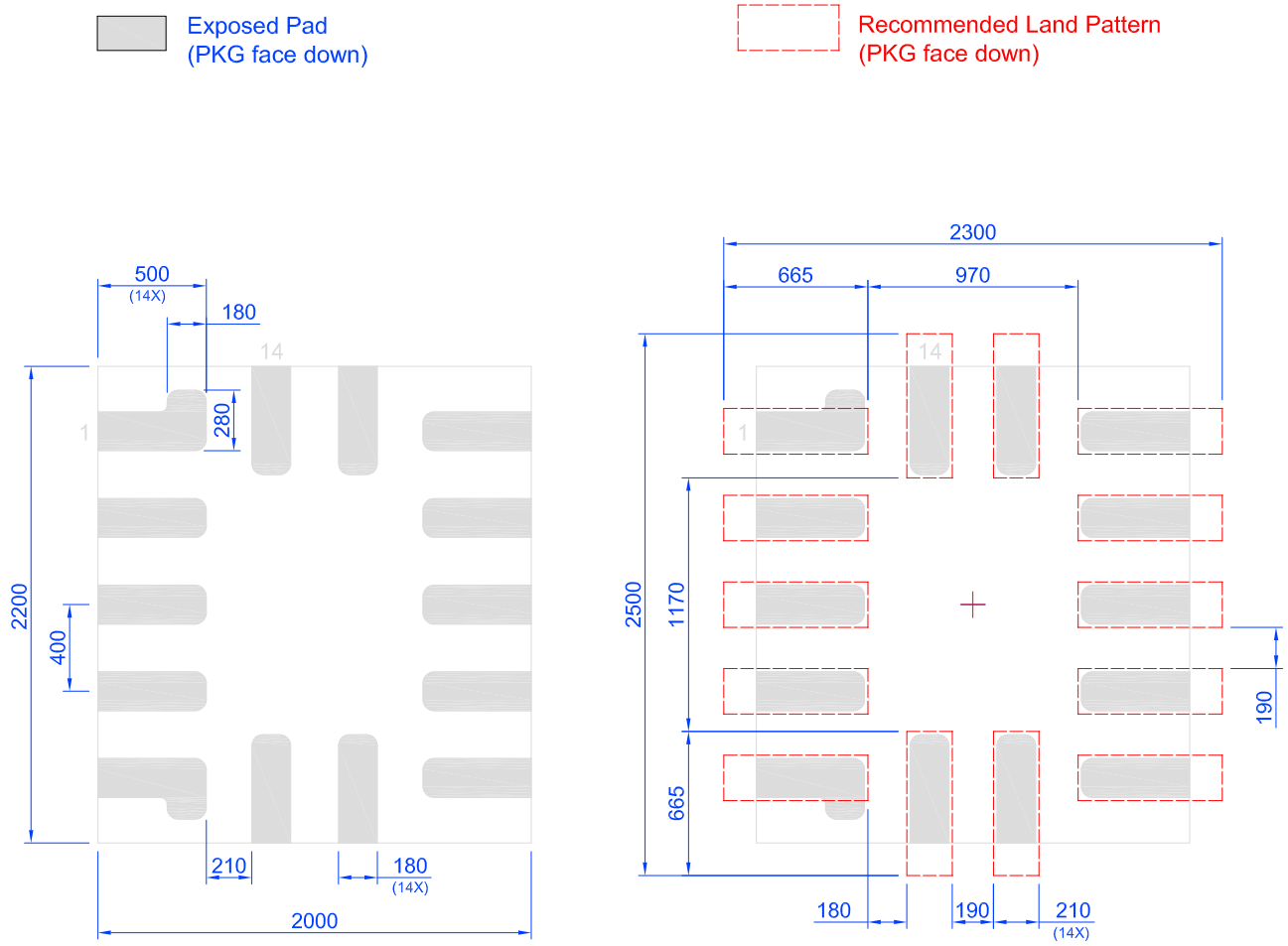
23.1 Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 2x2.2 mm 0.4P COL	2.2	2.35	0.8	4	4	1.5	1.75	3.5	8



Refer to EIA-481 specification

24.0 Recommended Landing Pattern



Unit:um

25.0 Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.42 mm^3 (nominal). More information can be found at www.jedec.org.

26.0 Revision History

Date	Version	Change
8/14/2023	1.12	Updated tables Electrical Characteristics Fixed typos
3/10/2023	1.11	Added notes to section Ordering Information
3/4/2022	1.10	Added R_{PUP} and R_{PDWN} in section Electrical Specifications Renesas rebranding Updated tables CNT/DLY Register Settings Corrected registers [684:677], [700:693], [730:717], [750:737], [764:757], [778:771], [792:785] in Appendix A - SLG46169 Register Definition
2/2/2021	1.09	Updated section Package Top Marking System Definition
10/30/2019	1.08	Added pre front page Updated last page with disclaimer and contacts
4/16/2019	1.07	Updated Chip Quiescent Value
5/10/2018	1.06	Fixed ACMP's hysteresis formula
12/4/2017	1.05	Fixed typos
10/10/2017	1.04	Updated Electrical Spec Fixed typos
7/5/2017	1.03	Updated Electrical Spec
4/13/2017	1.02	Fixed typos Updated Silego Website & Support Updated Section Programmable Delay / Edge Detector
10/20/2016	1.01	Removed references to GPAK families
9/28/2016	1.00	Production Release

RoHS Compliance

Renesas Electronics Corporation's suppliers certify that its products are in compliance with the requirements of Directive 2011/65/EU of the European Parliament on the restriction of the use of certain hazardous substances in electrical and electronic equipment. RoHS certificates from our suppliers are available on request.

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