

SLG5NT1533V

20 mΩ, Fast Turn On, 2.5 A Load Switch with Discharge

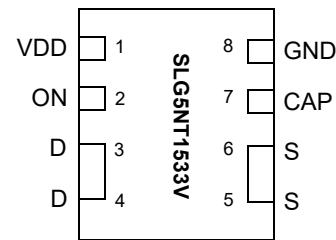
General Description

The SLG5NT1533V is a 20 mΩ 2.5 A single-channel load switch with configurable slew rate control. The device can enable fast power rail turn on with big cap loading. Internal circuit limits max inrush current to prevent device damage. The product is packaged in an ultra-small 1.0 x 1.6 mm package.

Features

- 1.0 x 1.6 x 0.55 mm FC-STDFN package (2 fused pins for drain and 2 fused pins for source)
- Logic level ON pin capable of supporting 0.85 V CMOS Logic
- Discharged Load when off
- Fast Turn On time
 - 32 μs, $C_{SLEW} = 0.1 \text{ nF}$, $C_{LOAD} = 1 \text{ μF}$, $I_{DS} = 100 \text{ mA}$
 - 102 μs, $C_{SLEW} = 0.5 \text{ nF}$, $C_{LOAD} = 10 \text{ μF}$, $I_{DS} = 2.5 \text{ A}$
- Low $R_{DS(ON)}$ while supporting 2.5 A
 - 20 mΩ, $V_{DD} = 5 \text{ V}$, $V_D = 1 \text{ V}$
 - 27.5 mΩ, $V_{DD} = 3.3 \text{ V}$, $V_D = 1 \text{ V}$
- Pb-Free / Halogen-Free / RoHS compliant
- Operating Temperature: -40 °C to 85°C
- Operating Voltage: 2.5 V to 5.5 V
- Power Rail Switching $V_D = 0.85 \text{ V}$ to $V_D = V_{DD} - 1.5 \text{ V}$

Pin Configuration

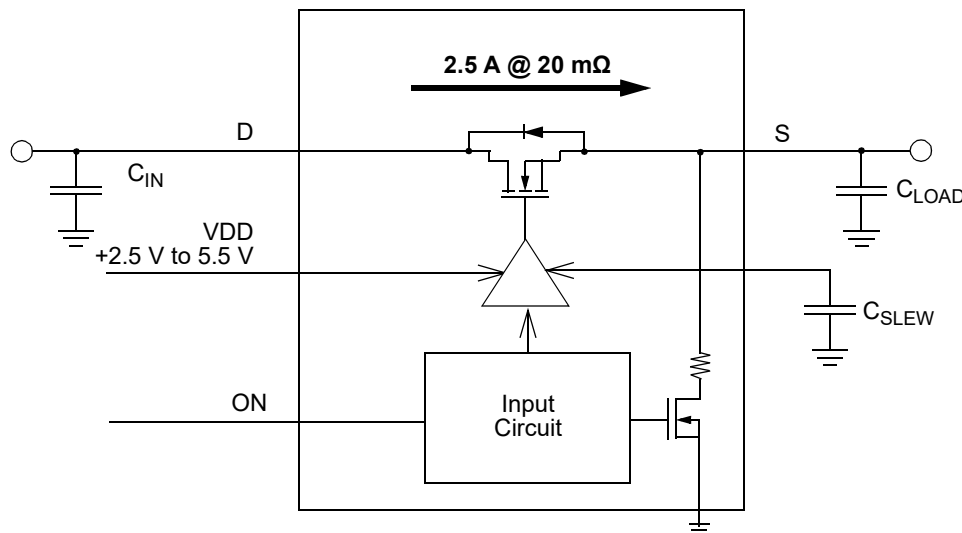


8-pin FC-STDFN (Top View)

Applications

- Fast Turn On/Off power rail switching with big load capacitance
- Frequent wake & sleep power cycle
- Mobile devices and portable devices

Block Diagram



SLG5NT1533V

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Pin Description

| Pin # | Pin Name | Type | Pin Description |
|-------|----------|--------|--|
| 1 | VDD | PWR | VDD supplies the power for the operation of the load switch and internal control circuitry. Bypass the VDD pin to GND with a 0.1 μF (or larger) capacitor. |
| 2 | ON | Input | A low-to-high transition on this pin initiates the operation of the SLG5NT1533V's state machine. ON is a CMOS input with ON_V _{IL} < 0.3 V and ON_V _{IH} > 0.85 V thresholds. While there is an internal pull-down circuit to GND (~4 MΩ), connect this pin directly to a general-purpose output (GPO) of a microcontroller, an application processor, or a system controller. |
| 3, 4 | D | MOSFET | Drain terminal connection of the n-channel MOSFET (2 pins fused for V _D). Connect at least a low-ESR 0.1 μF capacitor from this pin to ground. Capacitors used at V _D should be rated at 10 V or higher. |
| 5, 6 | S | MOSFET | Source terminal connection of the n-channel MOSFET (2 pins fused for V _S). Connect a low-ESR capacitor from this pin to ground and consult the Electrical Characteristics table for recommended C _{LOAD} range. Capacitors used at V _S should be rated at 10 V or higher. |
| 7 | CAP | Input | A low-ESR, stable dielectric, ceramic surface-mount capacitor connected from CAP pin to GND sets the V _S slew rate and overall turn-on time of the SLG5NT1533V. Capacitors at CAP pin should be rated at 10 V or higher. |
| 8 | GND | GND | Ground connection. Connect this pin to system analog or power ground plane. |

Ordering Information

| Part Number | Type | Production Flow |
|---------------|-----------------------------|-----------------------------|
| SLG5NT1533V | FC-STDFN 8L | Industrial, -40 °C to 85 °C |
| SLG5NT1533VTR | FC-STDFN 8L (Tape and Reel) | Industrial, -40 °C to 85 °C |

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Absolute Maximum Ratings

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|--------------------------|-----------------------------------|--|------|------|-----------------|------|
| V _{DD} | Power Supply | | -- | -- | 7 | V |
| V _D to GND | Load Switch Input Voltage to GND | | -0.3 | -- | V _{DD} | V |
| V _S to GND | Load Switch Output Voltage to GND | | -0.3 | -- | V _D | V |
| ON and CAP to GND | ON and CAP Pin Voltages to GND | | -0.3 | -- | V _{DD} | V |
| T _S | Storage Temperature | | -65 | -- | 150 | °C |
| T _J | Junction Temperature | | -- | -- | 150 | °C |
| ESD _{HBM} | ESD Protection | Human Body Model | 2000 | -- | -- | V |
| MSL | Moisture Sensitivity Level | | 1 | | | |
| θ _{JA} | Thermal Resistance | 1.6 x 1 mm, 8L STDFN; Determined using 1 in ² , 1 oz. copper pads under each VD and VS terminals and FR4 pcb material | -- | 75 | -- | °C/W |
| W _{DIS} | Package Power Dissipation | | -- | -- | 0.4 | W |
| MOSFET IDS _{PK} | Peak Current from Drain to Source | For no more than 20 μs with 1% duty cycle | -- | -- | 25.0 | A |
| | | For no more than 50 μs with 1% duty cycle | -- | -- | 12.5 | A |
| | | For no more than 1 ms with 1% duty cycle | -- | -- | 3.5 | A |

Note: Stresses greater than those listed under "Absolute Maximum Ratings" may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Electrical Characteristics

T_A = -40 °C to 85 °C. Typical values are at T_A = 25 °C unless otherwise noted.

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|-------------------|--------------------------------------|--|------|------|-----------------------|------|
| V _{DD} | Power Supply Voltage | -40 °C to 85 °C | 2.5 | -- | 5.5 | V |
| I _{DD} | Power Supply Current (PIN 1) | when OFF | -- | -- | 1 | μA |
| | | when ON, No load | -- | -- | 10 | μA |
| RDS _{ON} | ON Resistance, T _A = 25°C | V _{DD} = 5 V, V _D = 1.0 V, V _{DD} - V _D = 4.0 V, R _{LOAD} = 0.5 Ω | -- | 20 | 24 | mΩ |
| | | V _{DD} = 3.3 V, V _D = 1.0 V, V _{DD} - V _D = 2.3 V, R _{LOAD} = 0.5 Ω | -- | 27.5 | 31 | mΩ |
| | ON Resistance, T _A = 70°C | V _{DD} = 5 V, V _D = 1.0 V, V _{DD} - V _D = 4.0 V, R _{LOAD} = 0.5 Ω | -- | 23.5 | 27 | mΩ |
| | | V _{DD} = 3.3 V, V _D = 1.0 V, V _{DD} - V _D = 2.3 V, R _{LOAD} = 0.5 Ω | -- | 31 | 35 | mΩ |
| | ON Resistance, T _A = 85°C | V _{DD} = 5 V, V _D = 1.0 V, V _{DD} - V _D = 4.0 V, R _{LOAD} = 0.5 Ω | -- | 24.5 | 28 | mΩ |
| | | V _{DD} = 3.3 V, V _D = 1.0 V, V _{DD} - V _D = 2.3 V, R _{LOAD} = 0.5 Ω | -- | 33 | 37 | mΩ |
| MOSFET IDS | Current from D to S | Continuous, V _D = 0.85 V to 3.3 V | -- | -- | 2.5 | A |
| V _D | Drain Voltage | | 0.85 | -- | V _{DD} - 1.5 | V |

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Electrical Characteristics (continued)

T_A = -40 °C to 85 °C. Typical values are at T_A = 25 °C unless otherwise noted.

| Parameter | Description | Conditions | Min. | Typ. | Max. | Unit |
|-------------------------|--------------------------------------|---|--|------|-----------------|------|
| T _{ON_Delay} | ON Delay Time | 50% ON to 10% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{SLEW} = 0.1 nF | -- | 12 | 15 | μs |
| | | 50% ON to 10% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{SLEW} = 0.5 nF | -- | 32 | 35 | μs |
| T _{Total_ON} | Total Turn On Time | 50% ON to 90% V _S | Set by External C _{SLEW} ¹ | | | μs |
| | | 50% ON to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 1 μF, I _{DS} = 50 mA, C _{SLEW} = 0.1 nF | -- | 32 | 39 | μs |
| | | 50% ON to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 1 μF, I _{DS} = 100 mA, C _{SLEW} = 0.1 nF | -- | 32 | 39 | μs |
| | | 50% ON to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 4.7 μF, I _{DS} = 2.5 A, C _{SLEW} = 0.5 nF | -- | 102 | 123 | μs |
| | | 50% ON to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 10 μF, I _{DS} = 2.5 A, C _{SLEW} = 0.5 nF | -- | 102 | 123 | μs |
| V _{S(SR)} | Slew Rate | 10% V _S to 90% V _S | Set by External C _{SLEW} ¹ | | | V/ms |
| | | 10% V _S to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 1 μF, I _{DS} = 50 mA, C _{SLEW} = 0.1 nF | -- | 65 | 78 | V/ms |
| | | 10% V _S to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 1 μF, I _{DS} = 100 mA, C _{SLEW} = 0.1 nF | -- | 65 | 78 | V/ms |
| | | 10% V _S to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 4.7 μF, I _{DS} = 2.5 A, C _{SLEW} = 0.5 nF | -- | 13 | 16 | V/ms |
| | | 10% V _S to 90% V _S , V _{DD} = 5 V, V _D = 1.0 V, C _{LOAD} = 10 μF, I _{DS} = 2.5 A, C _{SLEW} = 0.5 nF | -- | 13.5 | 16.5 | V/ms |
| C _{LOAD} | Output Load Capacitance | C _{LOAD} connected from S to GND | -- | -- | 10 | μF |
| R _{DISCHRG} | Discharge Resistance | | 100 | 150 | 300 | Ω |
| ON_V _{IH} | High Input Voltage on ON pin | | 0.85 | -- | V _{DD} | V |
| ON_V _{IL} | Low Input Voltage on ON pin | | -0.3 | 0 | 0.3 | V |
| T _{OFF_Delay} | OFF Delay Time | 50% ON to V _S Fall Start, no C _{LOAD} , R _{LOAD} = 20 Ω, V _{DD} = 5 V, V _D = 1.0 V, No C _{SLEW} | -- | 120 | 150 | μs |
| THERM _{OFF} | Thermal shutoff turn-off temperature | Programmable, automatic shutoff temperature | -- | 125 | -- | °C |
| THERM _{OFFACC} | Thermal Sensor Accuracy | | -- | -- | ±20 | % |
| THERM _{DT} | Thermal Disable Time | Thermal sensor disable for the ON rising edge to 100 μs. Prevent thermal shutdown from inrush current | -- | -- | 100 | μs |

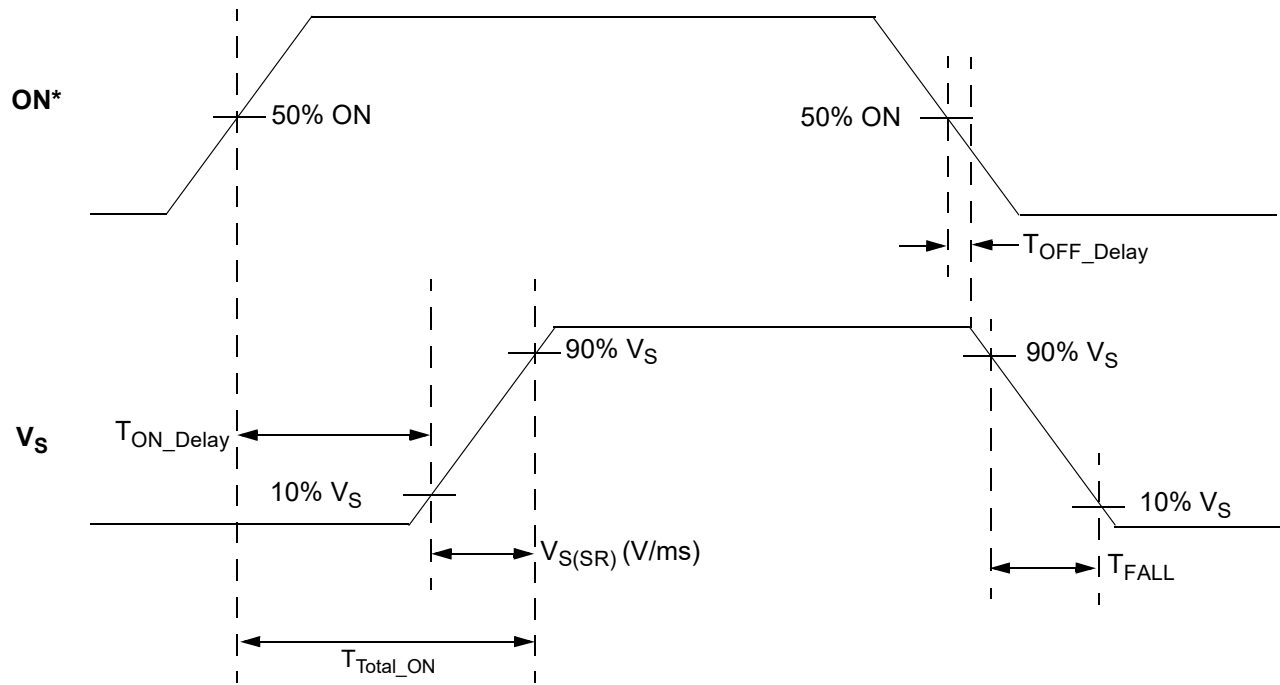
Notes:

1. Refer to typical timing parameter vs. C_{SLEW} performance charts for additional information when available.

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T_{ON_Delay} , $V_{S(SR)}$, and T_{Total_ON} Timing Details



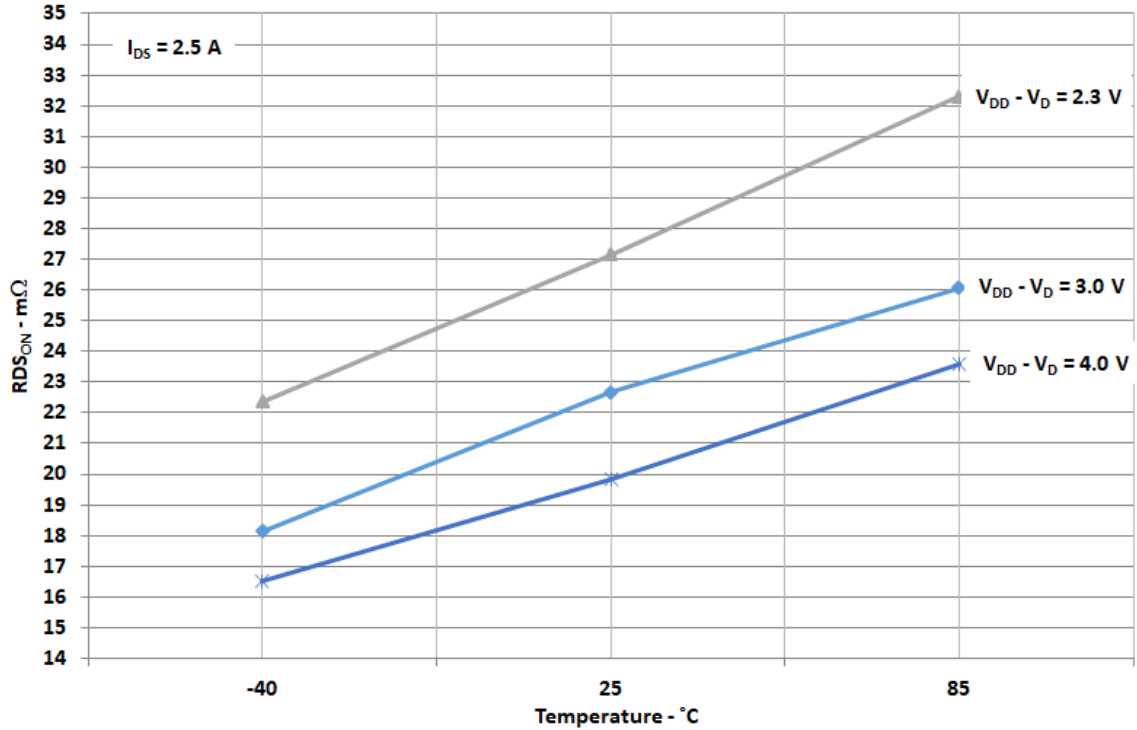
Note: * Rise and Fall times of the ON signal are 100 ns

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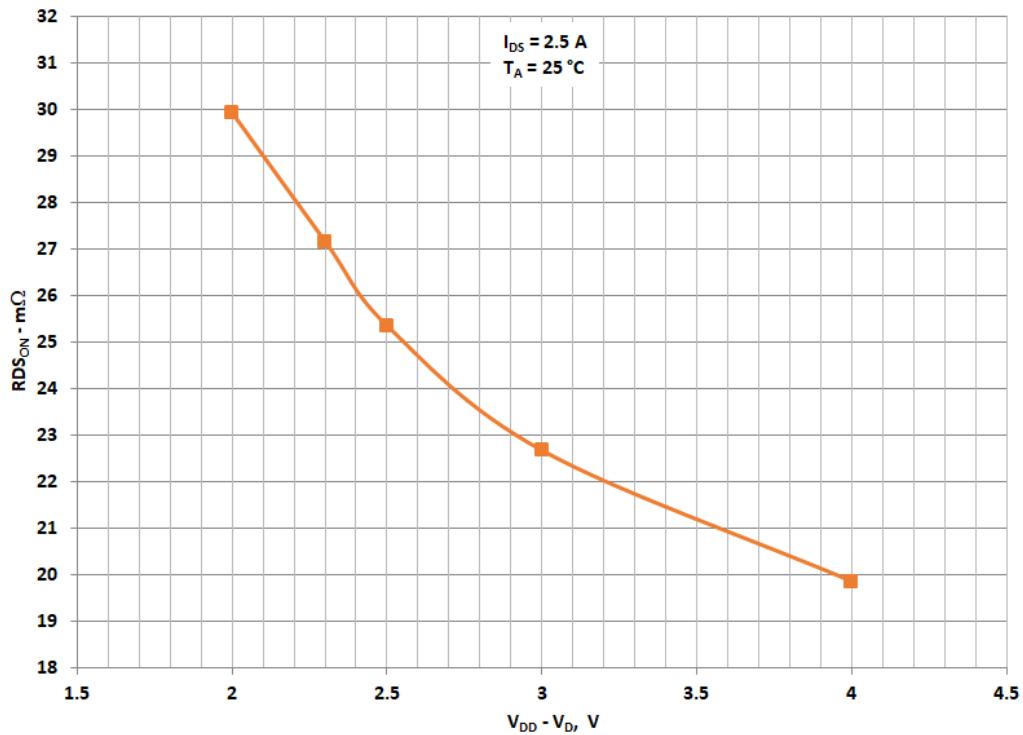
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Typical Performance Characteristics

RDS_{ON} vs. Temperature and V_{DD} - V_D



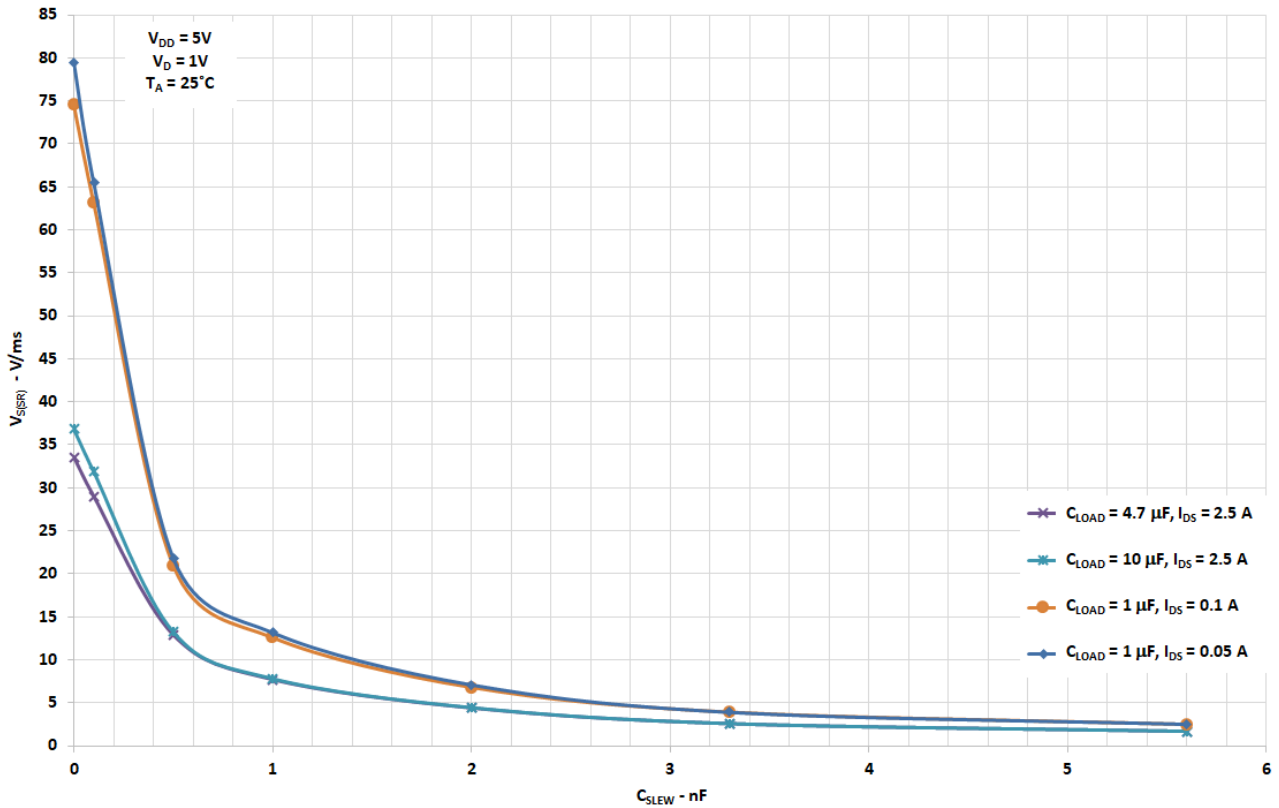
RDS_{ON} vs. V_{DD} - V_D



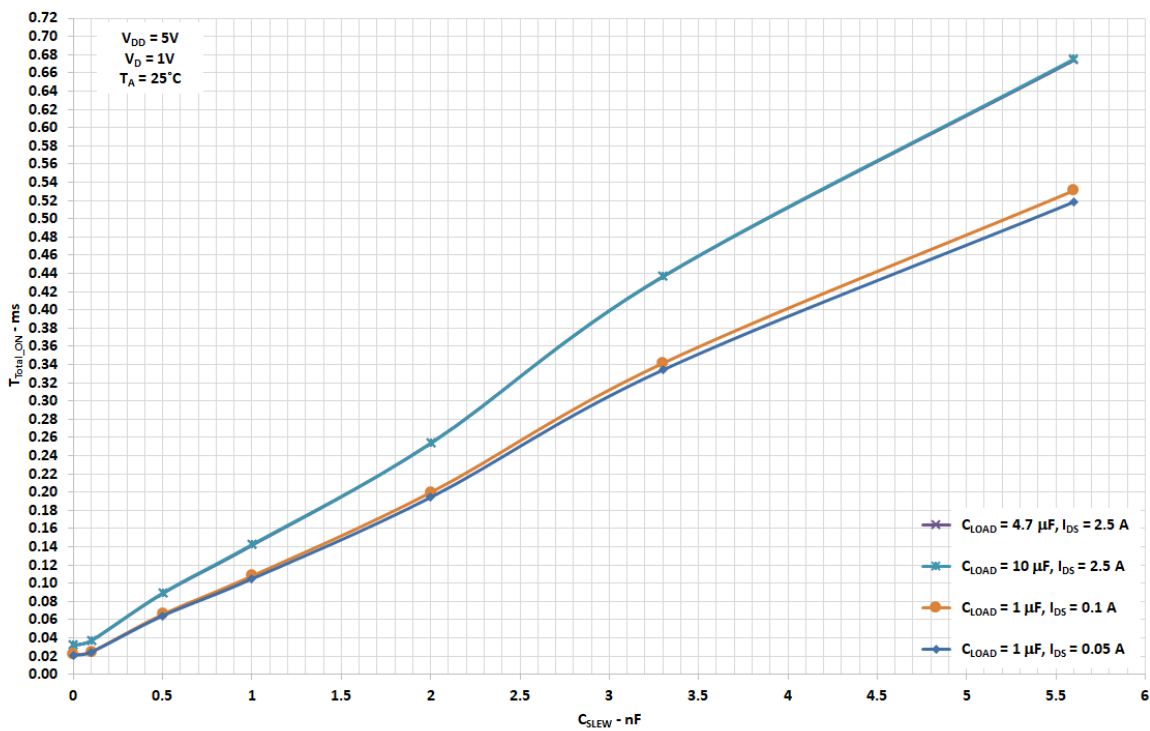
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V_S Slew Rate vs. C_{SLEW}



T_{Total_ON} vs. C_{SLEW}



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SLG5NT1533V Power-Up/Power-Down Sequence Considerations

A nominal power-up sequence is to apply V_{DD} first, followed by V_D only after V_{DD} is $> 90\%$ of final V_{DD} , and finally toggling the ON pin LOW-to-HIGH after V_D is at least 90% of its final value.

A nominal power-down sequence is the power-up sequence in reverse order.

If V_{DD} and V_D are applied at the same time, a voltage glitch may appear on the output pin at V_S . To prevent glitches at the output, it is recommended to connect at least a 1 μF capacitor from the S pin to GND and to keep the V_{DD} and V_D ramp times higher than 2 ms.

If the ON pin is toggled HIGH before V_{DD} and V_D have reached their steady-state values the load switch timing parameters may differ from datasheet specifications.

Power Dissipation

The junction temperature of the SLG5NT1533V depends on different factors such as board layout, ambient temperature, and other environmental factors. The primary contributor to the increase in the junction temperature of the SLG5NT1533V is the power dissipation of its power MOSFET. Its power dissipation and the junction temperature in nominal operating mode can be calculated using the following equations:

$$PD = (R_{DS_{ON}} \times I_{DS}^2) + (V_{DD} \times I_{DD})$$

where:

PD = Power dissipation, in Watts (W)

$R_{DS_{ON}}$ = Power MOSFET ON resistance, in Ohms (Ω)

I_{DS} = Output current, in Amps (A)

V_{DD} = Power supply voltage applied to the SLG5NT1533V, in Volts (V)

I_{DD} = Power supply current of the SLG5NT1533V at V_{DD} , in Amps (A)

and

$$T_J = PD \times \theta_{JA} + T_A$$

where:

T_J = Junction temperature, in Celsius degrees ($^{\circ}\text{C}$)

θ_{JA} = Package thermal resistance, in Celsius degrees per Watt ($^{\circ}\text{C}/\text{W}$) = 75 $^{\circ}\text{C}/\text{W}$ for the SLG5NT1533V's STDFN package.

T_A = Ambient temperature, in Celsius degrees ($^{\circ}\text{C}$)

For more information on GreenFET load switch features, please visit our website and see App Note "AN-1068 GreenFET and High Voltage GreenFET Load Switch Basics".

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Layout Guidelines:

1. The VDD pin needs a 0.1μF (or larger) external capacitor to smooth pulses from the power supply. Locate this capacitor as close as possible to the SLG5NT1533V's pin 1.
2. Since the D and S pins dissipate most of the heat generated during high-load current operation, it is highly recommended to make power traces as short, direct, and wide as possible. A good practice is to make power traces with absolute minimum widths of 15 mils (0.381 mm) per Ampere. A representative layout, shown in [Figure 1](#), illustrates proper techniques for heat to transfer as efficiently as possible out of the device;
3. To minimize the effects of parasitic trace inductance on normal operation, it is recommended to connect input C_{IN} and output C_{LOAD} low-ESR capacitors as close as possible to the SLG5NT1533V's D and S pins;
4. The GND pin should be connected to system analog or power ground plane.
5. 2 oz. copper is recommended for high current operation.

SLG5NT1533V Evaluation Board:

A GFET3 Evaluation Board for SLG5NT1533V is designed according to the statements above and is illustrated on [Figure 1](#). Please note that evaluation board has D_Sense and S_Sense pads. They cannot carry high currents and dedicated only for RDS_{ON} evaluation.

Please solder your SLG5NT1533V here

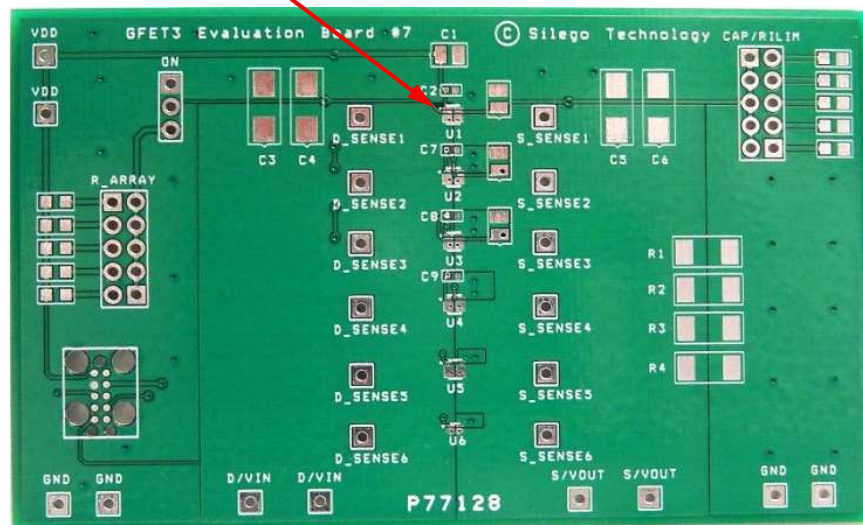


Figure 1. SLG5NT1533V Evaluation Board

SLG5NT1533V

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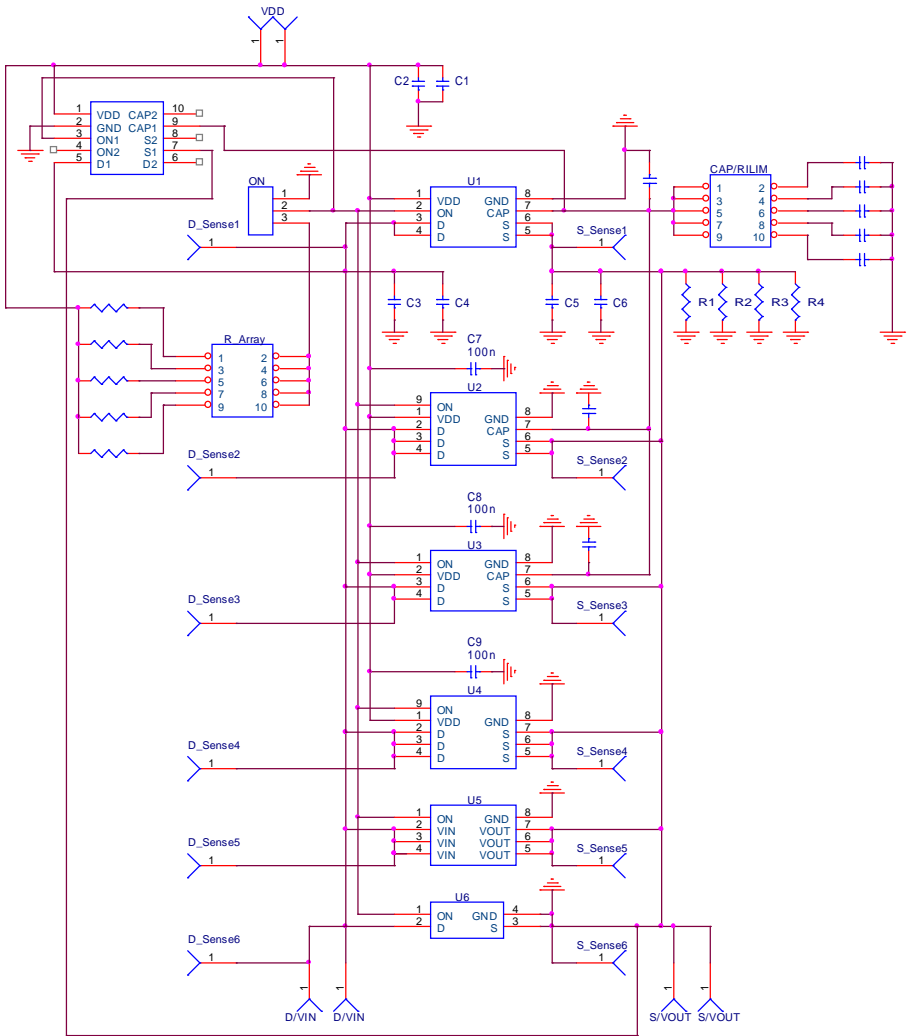


Figure 2. SLG5NT1533V Evaluation Board Connection Circuit

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Basic Test Setup and Connections

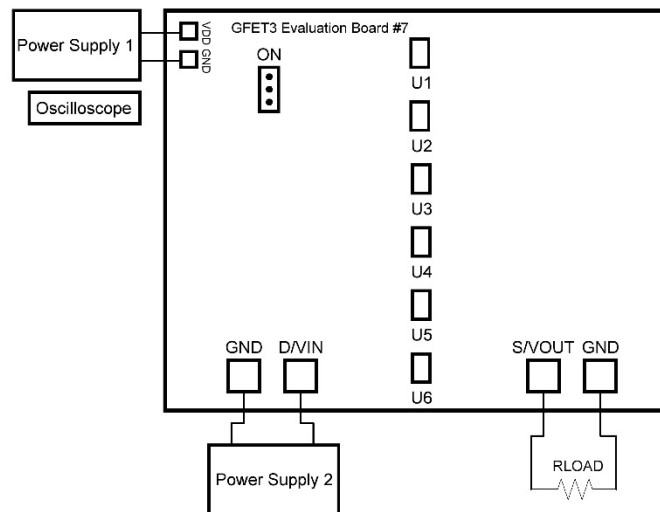


Figure 3. SLG5NT1533V Evaluation Board Connection Circuit

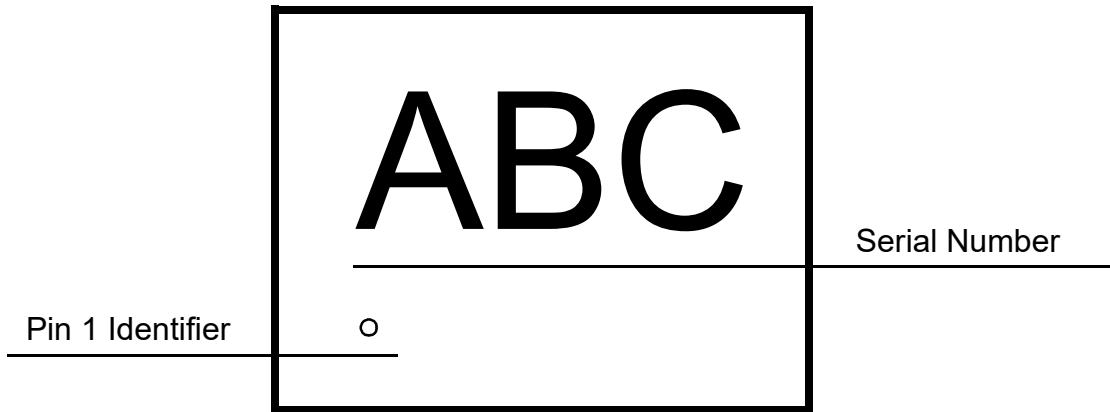
EVB Configuration

1. Connect oscilloscope probes to D/VIN, S/VOUT, ON, etc.;
2. Turn on Power Supply 1 and set desired V_{DD} from 2.5 V...5.5 V range;
3. Turn on Power Supply 2 and set desired V_D from 0.85 V... $V_{DD} - 1.5$ V range;
4. Toggle the ON signal High or Low to observe SLG5NT1533V operation.

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Package Top Marking System Definition



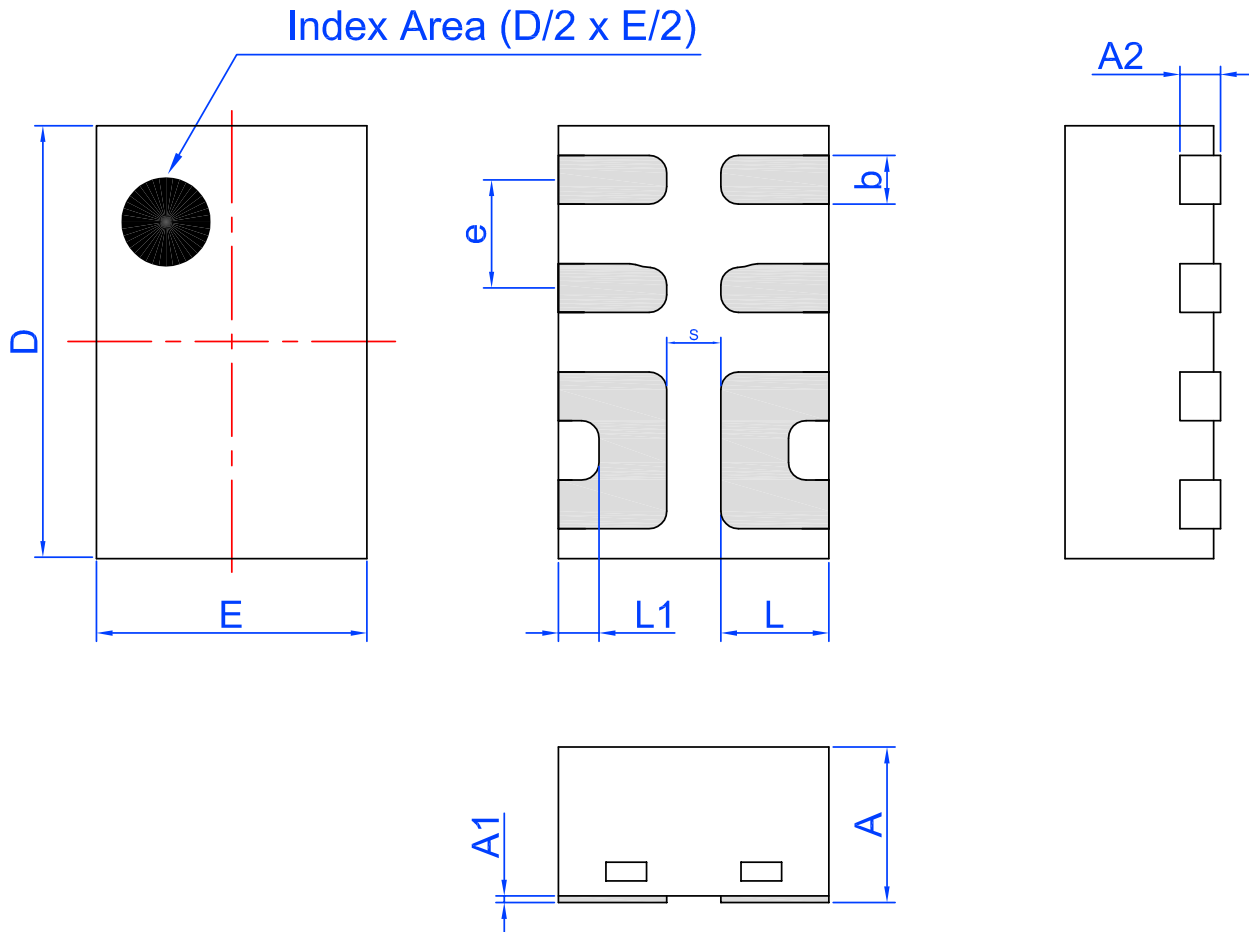
Each character in Serial Number field can be alphanumeric A-Z

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Package Drawing and Dimensions

8 Lead STDFN Package 1.0 x 1.6 mm (Fused Lead)



Unit: mm

| Symbol | Min | Nom. | Max | Symbol | Min | Nom. | Max |
|--------|----------|------|-------|--------|---------|------|------|
| A | 0.50 | 0.55 | 0.60 | D | 1.55 | 1.60 | 1.65 |
| A1 | 0.005 | - | 0.060 | E | 0.95 | 1.00 | 1.05 |
| A2 | 0.10 | 0.15 | 0.20 | L | 0.35 | 0.40 | 0.45 |
| b | 0.13 | 0.18 | 0.23 | L1 | 0.10 | 0.15 | 0.20 |
| e | 0.40 BSC | | | S | 0.2 REF | | |

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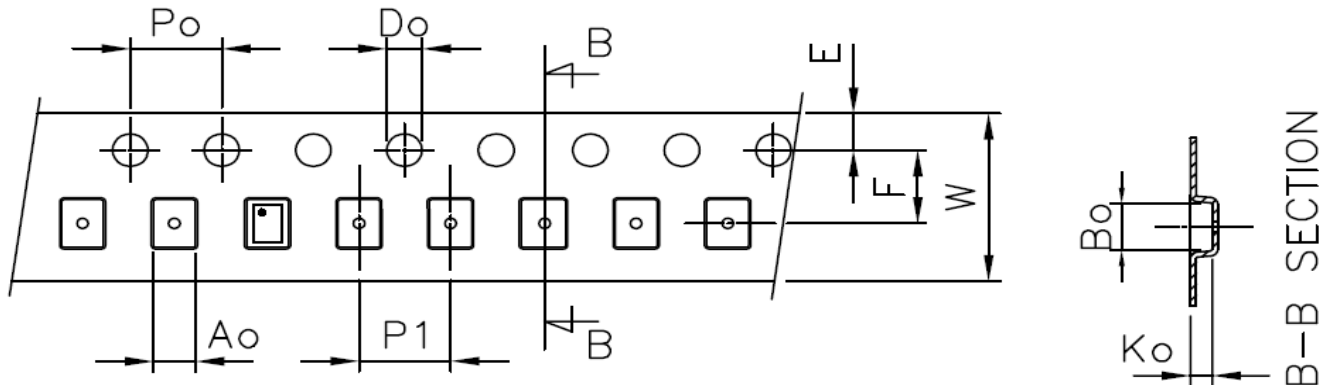
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Tape and Reel Specifications

| Package Type | # of Pins | Nominal Package Size [mm] | Max Units | | Reel & Hub Size [mm] | Leader (min) | | Trailer (min) | | Tape Width [mm] | Part Pitch [mm] |
|---|-----------|---------------------------|-----------|---------|----------------------|--------------|-------------|---------------|-------------|-----------------|-----------------|
| | | | per Reel | per Box | | Pockets | Length [mm] | Pockets | Length [mm] | | |
| STDFN 8L 1x1.6mm 0.4P FC Green | 8 | 1.0 x 1.6 x 0.55 | 3,000 | 3,000 | 178 / 60 | 100 | 400 | 100 | 400 | 8 | 4 |

Carrier Tape Drawing and Dimensions

| Package Type | Pocket BTM Length | Pocket BTM Width | Pocket Depth | Index Hole Pitch | Pocket Pitch | Index Hole Diameter | Index Hole to Tape Edge | Index Hole to Pocket Center | Tape Width |
|---|-------------------|------------------|--------------|------------------|--------------|---------------------|-------------------------|-----------------------------|------------|
| | A0 | B0 | K0 | P0 | P1 | D0 | E | F | W |
| STDFN 8L 1x1.6mm 0.4P FC Green | 1.12 | 1.72 | 0.7 | 4 | 4 | 1.55 | 1.75 | 3.5 | 8 |



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 0.88 mm³ (nominal). More information can be found at www.jedec.org.

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Revision History

| Date | Version | Change |
|------------|---------|---|
| 2/3/2022 | 1.07 | Updated Company name and logo Fixed typos |
| 11/26/2018 | 1.06 | Added Junction Temperature to Abs Max Table |
| 11/8/2018 | 1.05 | Updated Style and formatting Updated Abs, Max and Electrical Characteristics tables Added Applications information Added Layout Guidelines |
| 8/14/2015 | 1.04 | Add support for 0.85 VD |
| 4/22/2015 | 1.03 | Removed TBD from Timing Diagram |
| 4/20/2015 | 1.02 | Fixed Block Diagram (added Discharge Resistor) |
| 9/15/2014 | 1.01 | Added MSL |
| 6/16/2014 | 1.0 | Production release |

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