VR Enable and Discharge

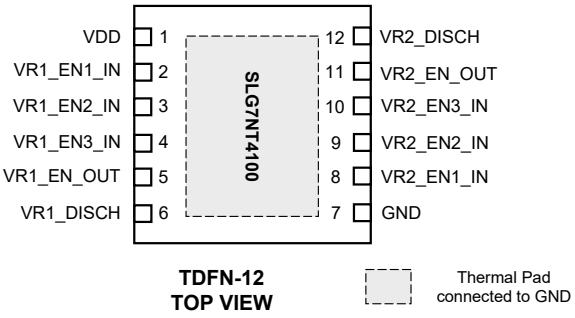
General Description

Renesas SLG7NT4100 is a low power and small form device. The SoC is housed in a 2.5mm x 2.5mm TDFN package which is optimal for using with small devices.

Features

- Low Power Consumption
- 3.3V Supply Voltage
- RoHS Compliant / Halogen-Free
- Pb-Free TDFN-12 Package

Pin Configuration

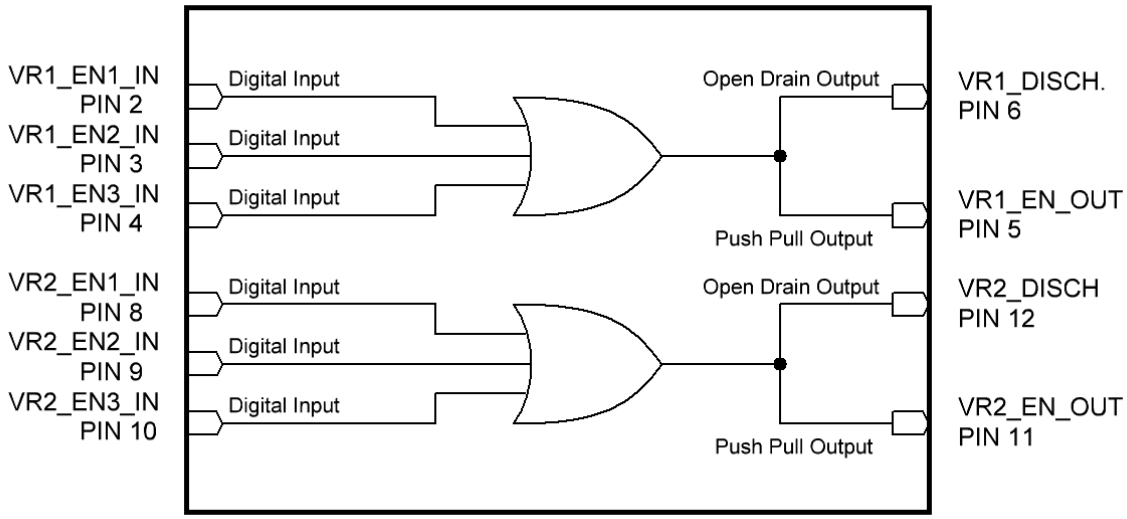


TDFN-12
TOP VIEW

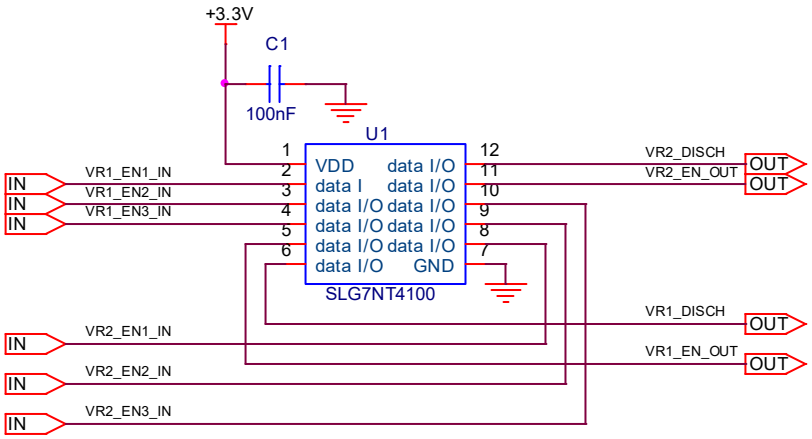
Output Summary

- 2 Outputs – Open Drain 2X current
- 2 Outputs – Push Pull

Block Diagram



Typical Application Circuit



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	Power	Supply Voltage
2	VR1_EN1_IN	Input	Digital Input
3	VR1_EN2_IN	Input	Digital Input
4	VR1_EN3_IN	Input	Digital Input
5	VR1_EN_OUT	Output	Push Pull
6	VR1_DISCH	Output	Open Drain 2x current
7	GND	GND	Ground
8	VR2_EN1_IN	Input	Digital Input
9	VR2_EN2_IN	Input	Digital Input
10	VR2_EN3_IN	Input	Digital Input
11	VR2_EN_OUT	Output	Push Pull
12	VR2_DISCH	Output	Open Drain 2x current
Exposed Bottom Pad	Exposed Bottom Pad	GND	Ground

Ordering Information

Part Number	Package Type
SLG7NT4100V	V = TDFN-12
SLG7NT4100VTR	VTR = TDFN-12 - Tape and Reel (3k units)

Absolute Maximum Conditions

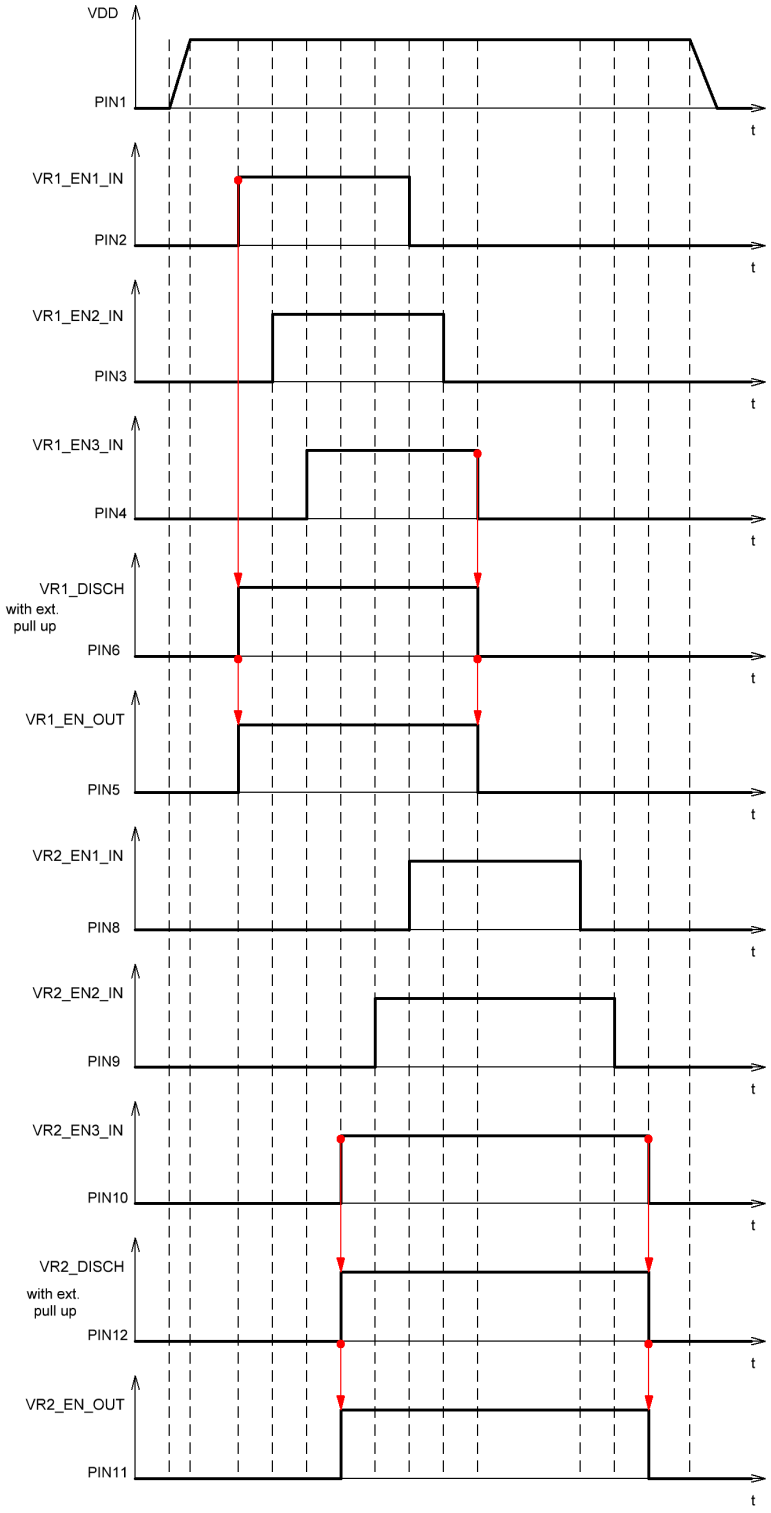
Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	150	°C
Junction temperature	--	150	°C

Electrical Characteristics

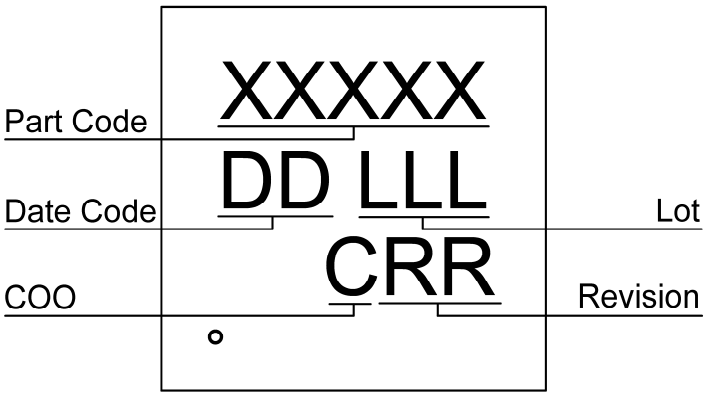
(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		3.0	3.3	3.6	V
I_Q	Quiescent Current	Static inputs and outputs	--	1	--	µA
T_A	Operating Temperature		-40	25	85	°C
I_L	Input Leakage Current	Leakage Current for Digital Inputs or outputs in High impedance state	-100	--	100	nA
V_{IH}	HIGH-Level Input Voltage	Logic Input at VDD=3.3V	1.8	--	--	V
V_{IL}	LOW-Level Input Voltage	Logic Input at VDD=3.3V	--	--	1.1	V
V_{OH}	Output Voltage High	Push Pull Logic Level Output at VDD=3.3V, I_{OH}=3mA	2.1	--	--	V
V_{OL}	Output Voltage Low	Push Pull Logic Level Output at VDD=3.3V, I_{OL}=3mA	--	--	0.81	V
V_{OL}	Output Voltage Low	Open Drain Logic Level Output at VDD=3.3V, I_{OL}=10mA, 2X Drive	--	--	0.252	V
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD	V
I_{OL}	LOW-Level Output Current	Push Pull Current at, V_{OL}=0.4V	--	1	--	mA
I_{OL}	LOW-Level Output Current	Open Drain Current at V_{OL}=0.4V, 2X Drive	28	--	--	mA
T_{SU}	Start up Time	After VDD reaches 1.6V	--	7	--	ms

Timing Diagrams



Package Top Marking

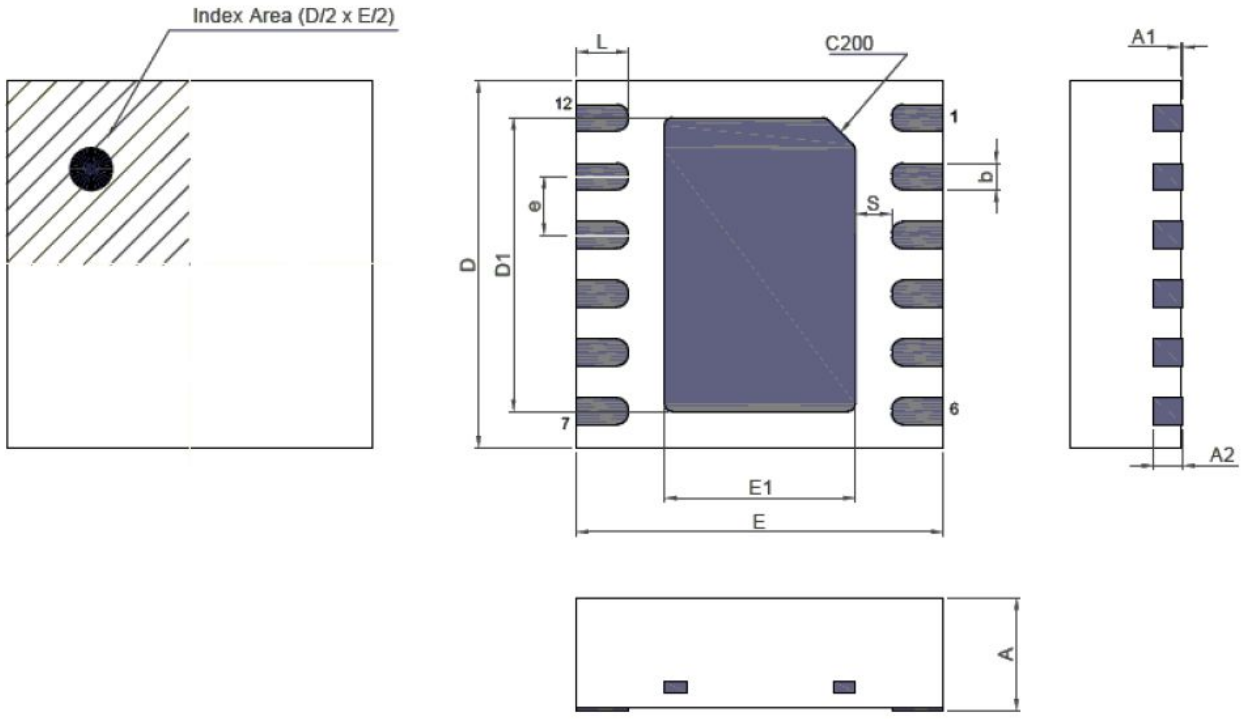


XXXXX – Part Code Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Part Code	Revision	Date
1.02	02	4100V	AB	02/25/2022

Package Drawing and Dimensions

12 Lead TDFN Package
JEDEC MO-229, Variation WDDE



Unit: mm

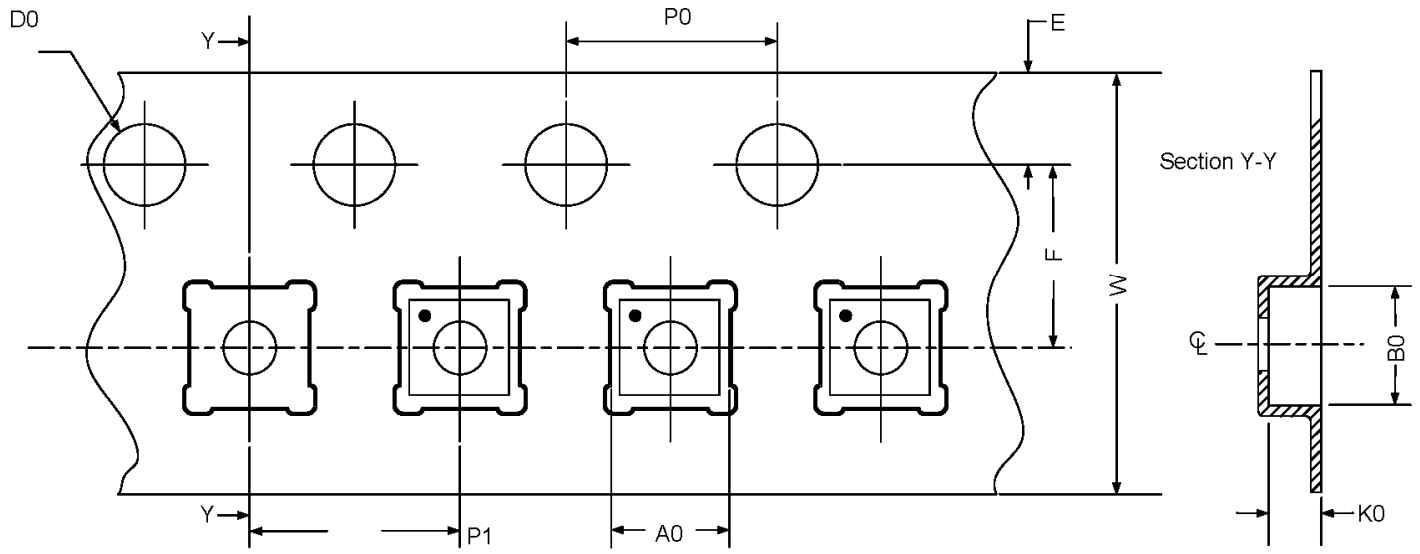
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.70	0.75	0.80	D1	1.95	2.00	2.05
A1	0.005	-	0.060	E1	1.25	1.30	1.35
A2	0.15	0.20	0.25	e	0.40 BSC		
b	0.13	0.18	0.23	L	0.30	0.35	0.40
D	2.45	2.50	2.55	S	0.18	-	-
E	2.45	2.50	2.55				

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
TDFN 12L 2.5x2.5mm 0.4P Green	12	2.5x2.5x0.75	3000	3000	178/60	42	168	42	168	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
TDFN 12L 2.5x2.5mm 0.4P Green	2.75	2.75	1.05	4	4	1.55	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 4.6875 mm^3 (nominal). More information can be found at www.jedec.org.

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