SLG7RN46359

GreenPAK ™

RZ/T2H Reference device: Power sequencer

General Description

Renesas SLG7RN46359 is a low power and small form device. The SoC is housed in a 1.6mm x 2.0mm STQFN package which is optimal for using with small devices.

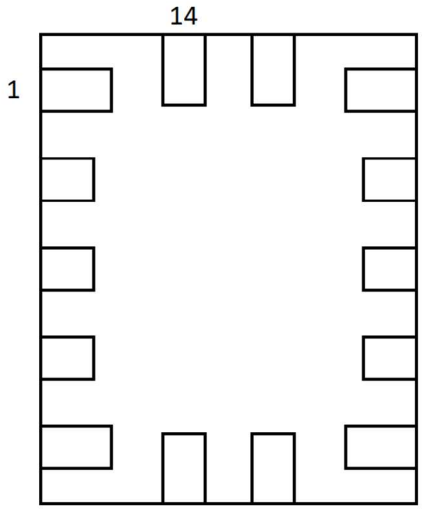
Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 14 Package

Output Summary

3 Outputs - Open Drain NMOS 1X
4 Outputs - Push Pull 1X

Pin Configuration

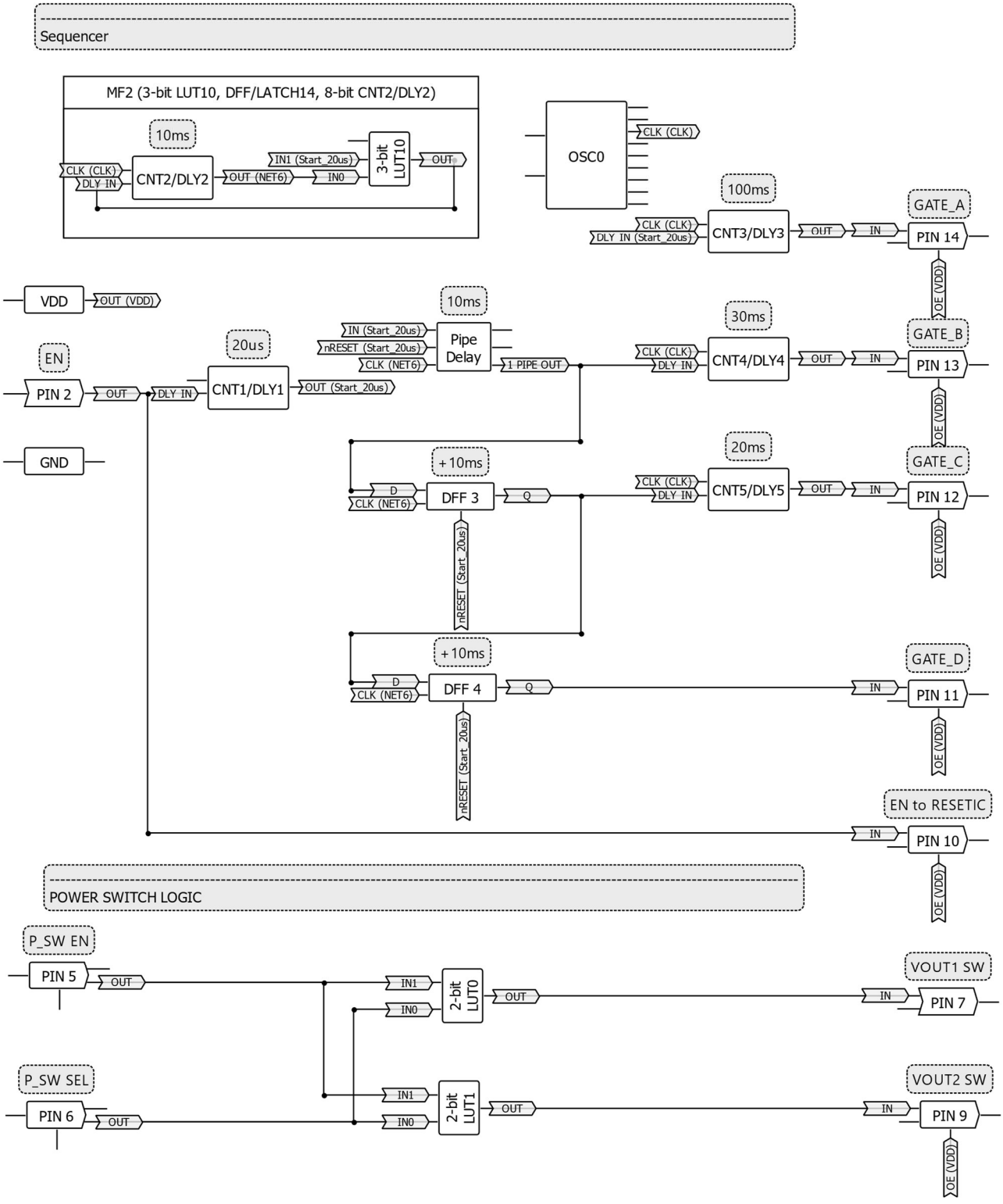


14-pin STQFN (Top View)

Pin name

Pin #	Pin name	Pin #	Pin name
1	VDD	8	GND
2	EN	9	VOUT2 SW
3	NC	10	EN to RESETIC
4	NC	11	GATE_D
5	P_SW EN	12	GATE_C
6	P_SW SEL	13	GATE_B
7	VOUT1 SW	14	GATE_A

Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	VDD	PWR	Supply Voltage	--
2	EN	Digital Input	Digital Input without Schmitt trigger	1MΩ pulldown
3	NC	--	Keep Floating or Connect to GND	--
4	NC	--	Keep Floating or Connect to GND	--
5	P_SW EN	Digital Input	Low Voltage Digital Input	1MΩ pulldown
6	P_SW SEL	Digital Input	Low Voltage Digital Input	1MΩ pulldown
7	VOUT1 SW	Digital Output	Open Drain NMOS 1X	floating
8	GND	GND	Ground	--
9	VOUT2 SW	Digital Output	Open Drain NMOS 1X	floating
10	EN to RESETIC	Digital Output	Open Drain NMOS 1X	floating
11	GATE_D	Digital Output	Push Pull 1X	floating
12	GATE_C	Digital Output	Push Pull 1X	floating
13	GATE_B	Digital Output	Push Pull 1X	floating
14	GATE_A	Digital Output	Push Pull 1X	floating

Ordering Information

Part Number	Package Type
SLG7RN46359V	14-pin STQFN
SLG7RN46359V	14-pin STQFN - Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter		Min.	Max.	Unit
V_{HIGH} to GND		-0.3	7	V
Voltage at Input Pin		GND-0.5V	V_{DD}+0.5V	V
Maximum Average or DC Current (Through V_{DD} or GND pin)		--	90	mA
Maximum Average or DC Current (Through pin)	Push-Pull 1x	--	11	mA
	OD 1x	--	11	
Current at Input Pin		-1.0	1.0	mA
Input leakage Current (Absolute Value)		--	1000	nA
Storage Temperature Range		-65	150	°C
Junction Temperature		--	150	°C
ESD Protection (Human Body Model)		2000	--	V
ESD Protection (Charged Device Model)		1300	--	V
Moisture Sensitivity Level		1		

Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		4.5	5	5.5	V
T_A	Operating Temperature		-40	25	85	°C
C_{VDD}	Capacitor Value at VDD		--	0.1	--	µF
C_{IN}	Input Capacitance		--	4	--	pF
I_Q	Quiescent Current	Static inputs and floating outputs. PINs 2,5,6 are LOW	--	1	--	µA
V_O	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
V_{IH}	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
		Low-Level Logic Input	1.25	--	VDD+0.3	V
V_{IL}	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
		Low-Level Logic Input	GND-0.3	--	0.5	V
V_{OH}	HIGH-Level Output Voltage	Push-Pull 1X, I_{OH}=5mA at VDD=5.0V	4.16	--	--	V
V_{OL}	LOW-Level Output Voltage	Push-Pull 1X, I_{OL}=5mA, at VDD=5.0V	--	--	0.270	V
		Open Drain NMOS 1X, I_{OL}=5mA, at VDD=5.0V	--	--	0.107	V
I_{OH}	HIGH-Level Output Current (Note 1)	Push-Pull 1X, V_{OH}=2.4V at VDD=5.0V	20.42	--	--	mA
I_{OL}	LOW-Level Output Current (Note 1)	Push-Pull 1X, V_{OL}=0.4V, at VDD=5.0V	7.36	--	--	mA
		Open Drain NMOS 1X, V_{OL}=0.4V, at VDD=5.0V	17.90	--	--	mA
R_{PULL_DOWN}	Internal Pull Down Resistance	Pull down on PINs 2, 5, 6	--	1	--	MΩ
T_{DLY1}	Delay1 Time	At temperature 25°C	20	21	24	µs
		At temperature -40 +85°C (Note 3)	20	21	27	µs
T_{DLY2}	Delay2 Time	At temperature 25°C	10.14	10.49	11.50	ms
		At temperature -40 +85°C (Note 3)	10.03	10.49	12.22	ms

T_{DLY3}	Delay3 Time	At temperature 25°C	99.06	100.34	102.28	ms
		At temperature -40 +85°C (Note 3)	97.98	100.34	109.34	ms
T_{DLY4}	Delay4 Time	At temperature 25°C	29.47	30.02	31.23	ms
		At temperature -40 +85°C (Note 3)	29.15	30.02	33.33	ms
T_{DLY5}	Delay5 Time	At temperature 25°C	19.81	20.26	21.36	ms
		At temperature -40 +85°C (Note 3)	19.59	20.26	22.78	ms
T_{SU}	Startup Time	From VDD rising past PON_{THR}	--	1	2	ms
PON_{THR}	Power On Threshold	V_{DD} Level Required to Start Up the Chip	1.6	1.85	2.05	V
$POFF_{THR}$	Power Off Threshold	V_{DD} Level Required to Switch Off the Chip	0.85	1.25	1.5	V

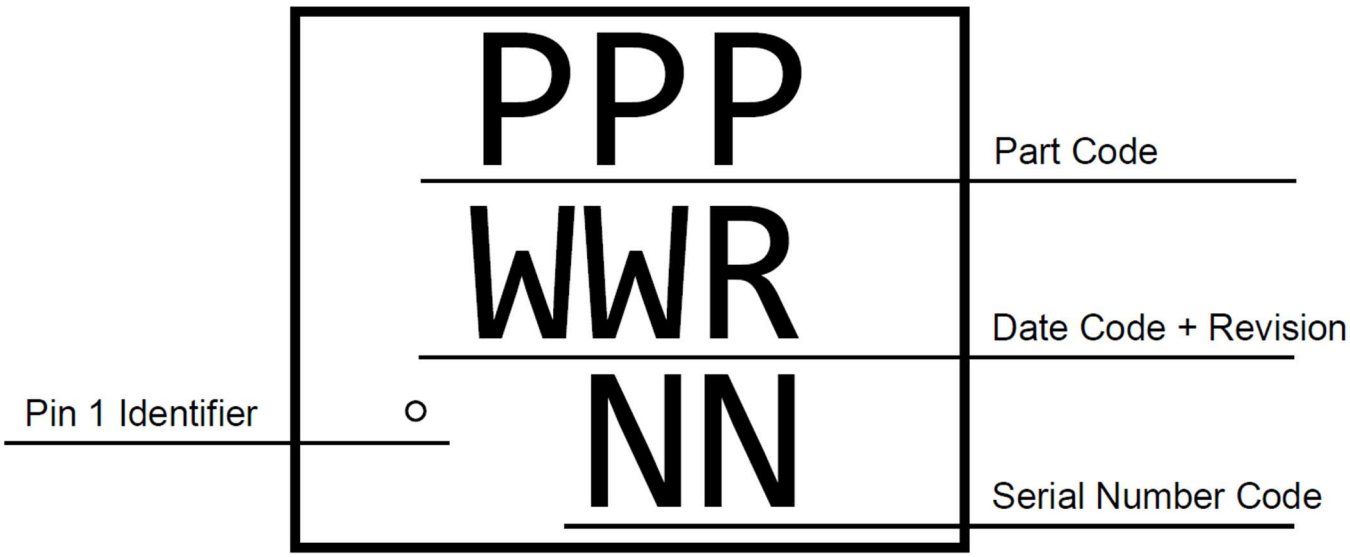
Note:
1. DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
2. The GreenPAK's power rails are divided in two sides.
3. Guaranteed by Design.

Truth Tables

2-bit LUT0		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	1
1	1	0

2-bit LUT1		
IN1	IN0	OUT
0	0	0
0	1	0
1	0	1
1	1	1

Package Top Marking



Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	002	U	0x5085104E			03/15/2023

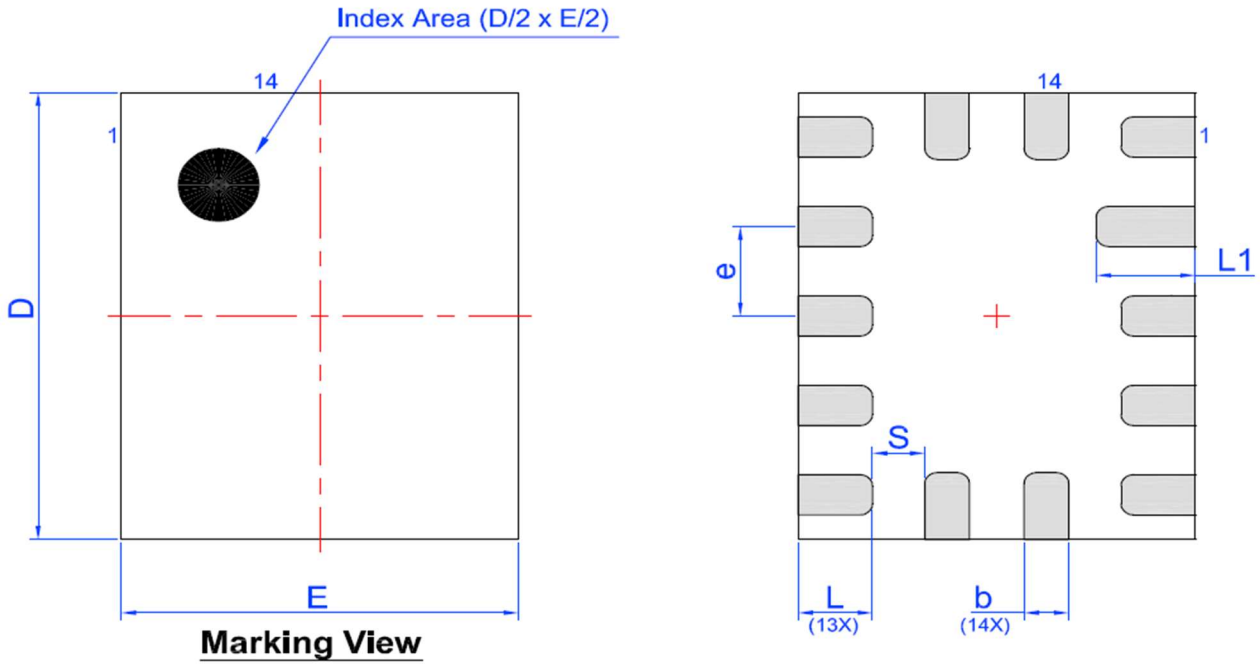
Lock coverage for this part is indicated by √, from one of the following options:

√	Unlocked
	Partly lock read (mode 1)
	Partly lock read2 (mode 2)
	Partly lock read2/write (mode 3)
	All lock read (mode 4)
	All lock write (mode 5)
	All lock read/write (mode 6)

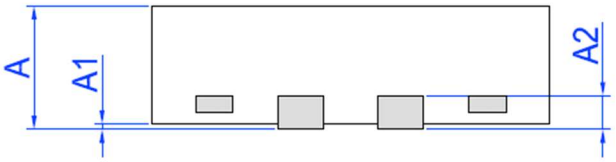
The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

Package Outlines

STQFN 14L 1.6 x 2.0 x 0.55 mm 0.4P FC Package
IC Net Weight: 0.0045 g



Marking View



Marking View

Unit: mm

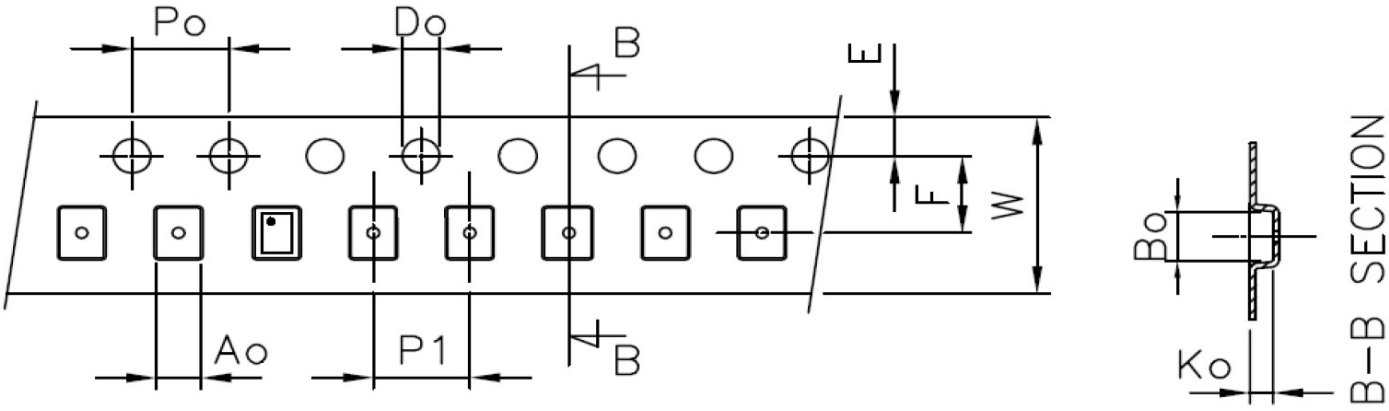
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	1.95	2.00	2.05
A1	0.005	-	0.050	E	1.55	1.60	1.65
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			S	0.21 REF		

Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 14L 1.6x2mm 0.4P FC Green	14	1.6x2.0x0.55	3000	3000	178 / 60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

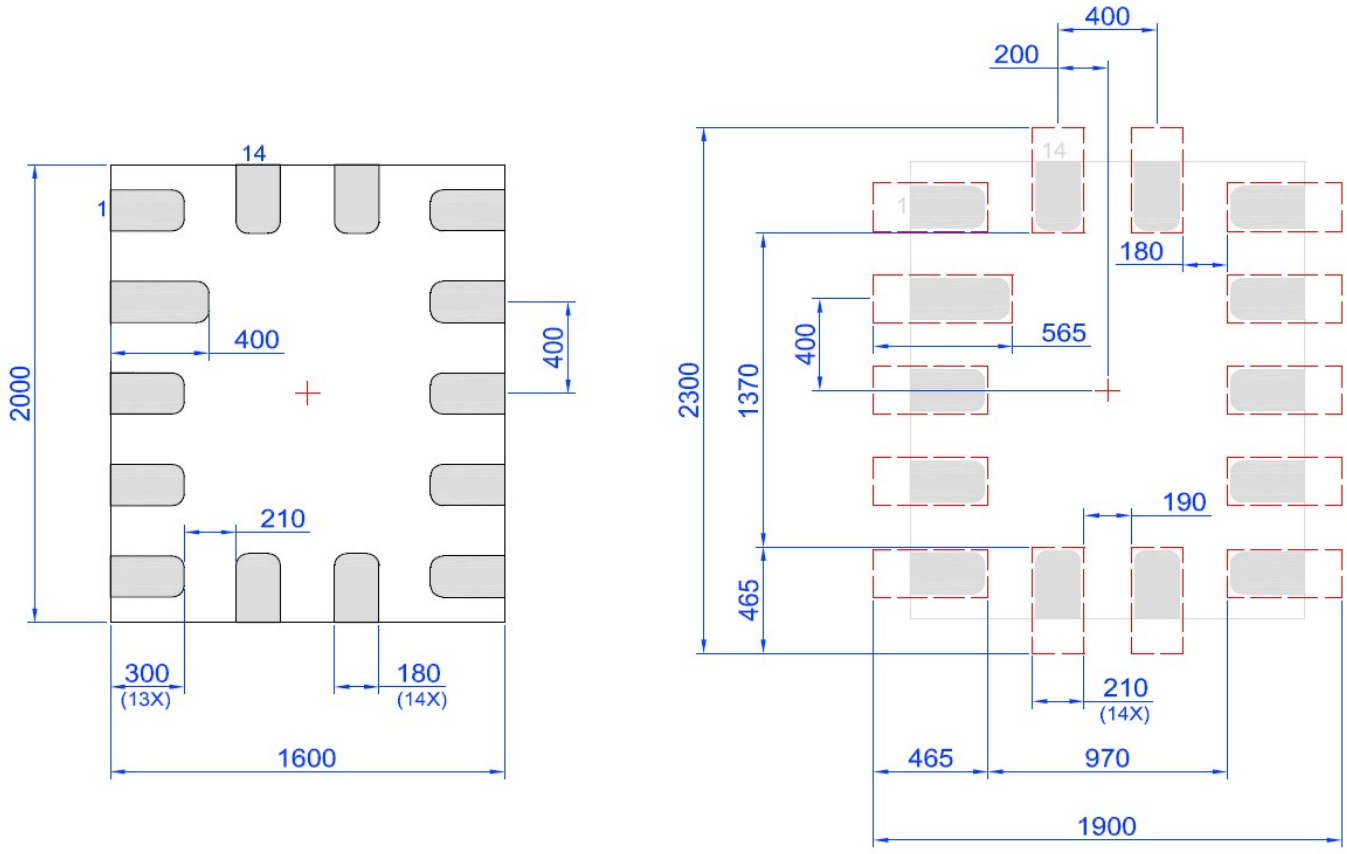
Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 14L 1.6x2 mm 0.4P FC Green	1.9	2.3	0.76	4	4	1.5	1.75	3.5	8



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 2.64 mm^3 (nominal) for STQFN 14L Package. More information can be found at www.jedec.org.

Layout Guidelines



Unit: um

Datasheet Revision History

Date	Version	Change
03/07/2023	0.10	New design for SLG46855 chip
03/15/2023	0.11	The PINs 5,6 mode were changed to Low voltage digital input

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