

## General Description

Renesas SLG7RN46383 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

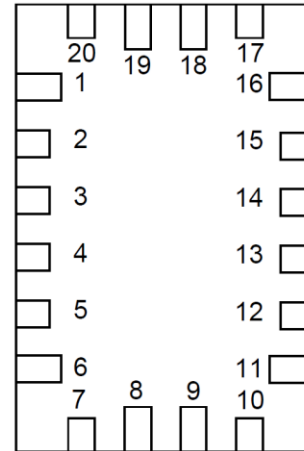
## Features

- Low Power Consumption
- Pb - Free / RoHS Compliant
- Halogen - Free
- STQFN - 20 Package

## Output Summary

2 Outputs - Open Drain NMOS 2X  
 1 Output - Push Pull 2X

## Pin Configuration

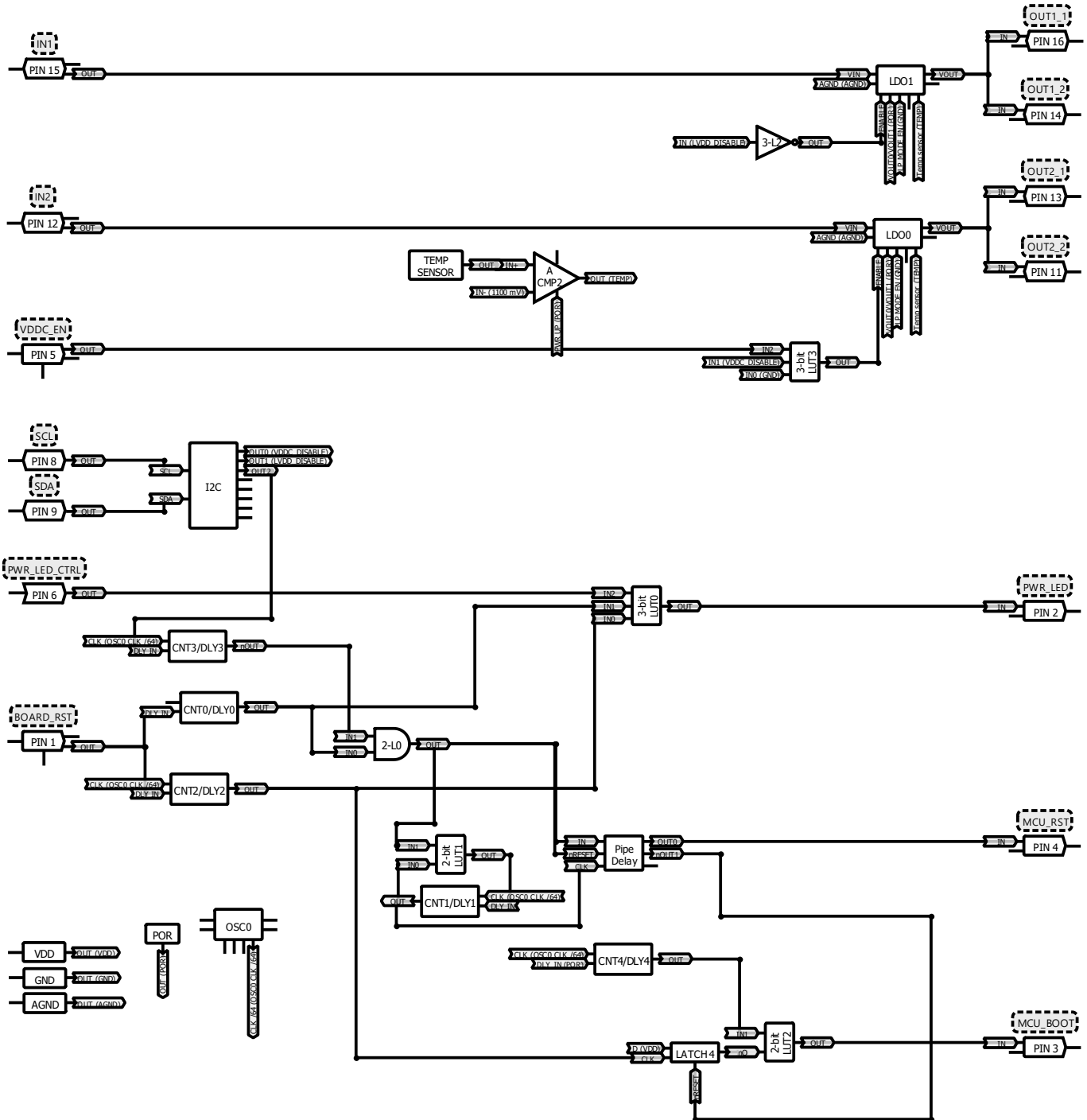


STQFN-20  
(Top view)

## Pin name

Pin #	Pin name	Pin #	Pin name
1	BOARD_RST	11	OUT2_2
2	PWR_LED	12	IN2
3	MCU_BOOT	13	OUT2_1
4	MCU_RST	14	OUT1_2
5	VDDC_EN	15	IN1
6	PWR_LED_CTRL	16	OUT1_1
7	VDD	17	AGND
8	SCL	18	NC
9	SDA	19	NC
10	NC	20	GND

### Block Diagram



### Pin Configuration

Pin #	Pin Name	Type	Pin Description	Internal Resistor
1	BOARD_RST	Digital Input	Digital Input with Schmitt trigger	10kΩ pullup
2	PWR_LED	Digital Output	Push Pull 2X	floating
3	MCU_BOOT	Digital Output	Open Drain NMOS 2X	floating
4	MCU_RST	Digital Output	Open Drain NMOS 2X	floating
5	VDDC_EN	Digital Input	Digital Input without Schmitt trigger	100kΩ pulldown
6	PWR_LED_CTRL	Digital Input	Digital Input without Schmitt trigger	100kΩ pulldown
7	VDD	PWR	Supply Voltage	--
8	SCL	Digital Input	Digital Input with Schmitt trigger	floating
9	SDA	Digital Input	Digital Input with Schmitt trigger	floating
10	NC	--	Keep Floating or Connect to GND	--
11	OUT2_2	Analog Output	LDO0 VOUT Analog Output	floating
12	IN2	Analog Input	LDO0 VIN Analog Input	floating
13	OUT2_1	Analog Output	LDO0 VOUT Analog Output	floating
14	OUT1_2	Analog Output	LDO1 VOUT Analog Output	floating
15	IN1	Analog Input	LDO1 VIN Analog Input	floating
16	OUT1_1	Analog Output	LDO1 VOUT Analog Output	floating
17	AGND	AGND	Ground	--
18	NC	--	Keep Floating or Connect to GND	--
19	NC	--	Keep Floating or Connect to GND	--
20	GND	GND	Ground	--

### Ordering Information

Part Number	Package Type
SLG7RN46383V	20-pin STQFN
SLG7RN46383V	20-pin STQFN - Tape and Reel (3k units)

### Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
Supply Voltage on VDD relative to GND	-0.3	7	V
DC Input Voltage	GND - 0.5V	VDD + 0.5V	V
Maximum Average or DC Current (Through pin)	Push-Pull 2x	43	mA
	OD 2x	65	
Current at Input Pin	-1.0	1.0	mA
Input leakage (Absolute Value)	--	1000	nA
Storage Temperature Range	-65	150	°C
Junction Temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

### Electrical Characteristics

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V <sub>DD</sub>	Supply Voltage		2.3	3.3	5.5	V
T <sub>A</sub>	Operating Temperature		-40	25	85	°C
C <sub>VDD</sub>	Capacitor Value at VDD		--	0.1	--	µF
C <sub>IN</sub>	Input Capacitance		--	4	--	pF
I <sub>Q</sub>	Quiescent Current	Static inputs and floating outputs PIN8 and PIN9 are HIGH	--	75	--	µA
V <sub>O</sub>	Maximal Voltage Applied to any PIN in High-Impedance State		--	--	VDD+0.3	V
I <sub>VDD</sub>	Maximum Average or DC Current Through VDD Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	73	mA
		T <sub>J</sub> = 110°C	--	--	35	mA
I <sub>GND</sub>	Maximum Average or DC Current Through GND Pin (Per chip side, see Note 2)	T <sub>J</sub> = 85°C	--	--	152	mA
		T <sub>J</sub> = 110°C	--	--	72	mA
V <sub>IH</sub>	HIGH-Level Input Voltage	Logic Input	0.7xVDD	--	VDD+0.3	V
		Logic Input with Schmitt Trigger	0.8xVDD	--	VDD+0.3	V
V <sub>IL</sub>	LOW-Level Input Voltage	Logic Input	GND-0.3	--	0.3xVDD	V
		Logic Input with Schmitt Trigger	GND-0.3	--	0.2xVDD	V
V <sub>OH</sub>	HIGH-Level Output Voltage	Push-Pull 2X, I <sub>OH</sub> =100µA at VDD=2.5V	2.29	2.50	--	V
		Push-Pull 2X, I <sub>OH</sub> =3mA at VDD=3.3V	2.87	3.21	--	V
		Push-Pull 2X, I <sub>OH</sub> =5mA at VDD=5.0V	4.32	4.89	--	V
V <sub>OL</sub>	LOW-Level Output Voltage	Push-Pull 2X, I <sub>OL</sub> =100µA, at VDD=2.5V	--	0.03	0.06	V
		Push-Pull 2X, I <sub>OL</sub> =3mA, at VDD=3.3V	--	0.06	0.11	V
		Push-Pull 2X, I <sub>OL</sub> =5mA, at VDD=5.0V	--	0.08	0.14	V
		Open Drain NMOS 2X, I <sub>OL</sub> =100µA, at VDD=2.5V	--	0.02	0.03	V

		Open Drain NMOS 2X, $I_{OL}=3mA$ , at $V_{DD}=3.3V$	--	0.04	0.08	V
		Open Drain NMOS 2X, $I_{OL}=5mA$ , at $V_{DD}=5.0V$	--	0.05	0.11	V
$I_{OH}$	HIGH-Level Output Current (Note 1)	Push-Pull 2X, $V_{OH}=V_{DD}-0.2V$ at $V_{DD}=2.5V$	2.22	3.41	--	mA
		Push-Pull 2X, $V_{OH}=2.4V$ at $V_{DD}=3.3V$	11.54	24.16	--	mA
		Push-Pull 2X, $V_{OH}=2.4V$ at $V_{DD}=5.0V$	41.46	68.08	--	mA
$I_{OL}$	LOW-Level Output Current (Note 1)	Push-Pull 2X, $V_{OL}=0.15V$ , at $V_{DD}=2.5V$	1.83	3.38	--	mA
		Push-Pull 2X, $V_{OL}=0.4V$ , at $V_{DD}=3.3V$	9.75	16.49	--	mA
		Push-Pull 2X, $V_{OL}=0.4V$ , at $V_{DD}=5.0V$	13.83	23.16	--	mA
		Open Drain NMOS 2X, $V_{OL}=0.15V$ , at $V_{DD}=2.5V$	2.75	5.07	--	mA
		Open Drain NMOS 2X, $V_{OL}=0.4V$ , at $V_{DD}=3.3V$	14.54	24.74	--	mA
		Open Drain NMOS 2X, $V_{OL}=0.4V$ , at $V_{DD}=5.0V$	17.34	34.76	--	mA
$R_{PULL\_UP}$	Internal Pull Up Resistance	Pull up on PIN 1	--	10	--	k $\Omega$
$R_{PULL\_DOWN}$	Internal Pull Down Resistance	Pull down on PINs 5, 6	--	100	--	k $\Omega$
$T_{DLY0}$	Delay0 Time	At temperature 25°C	39.6	41.0	41.8	ms
		At temperature -40 +85°C (Note 3)	37.9	41.0	44.2	ms
$T_{DLY1}$	Delay1 Time	At temperature 25°C	307.5	322.5	332.4	ms
		At temperature -40 +85°C (Note 3)	294.0	322.5	351.2	ms
$T_{DLY2}$	Delay2 Time	At temperature 25°C	1.94	2.01	2.05	s
		At temperature -40 +85°C (Note 3)	1.85	2.01	2.17	s
$T_{DLY3}$	Delay3 Time (one-shot mode)	At temperature 25°C	257.9	271.3	280.5	ms
		At temperature -40 +85°C (Note 3)	246.6	271.3	296.3	ms
$T_{DLY4}$	Delay4 Time	At temperature 25°C	2.54	2.62	2.67	s
		At temperature -40 +85°C (Note 3)	2.42	2.62	2.82	s
$V_{ACMP2}$	Analog Comparator2 Threshold Voltage	Low to High transition, at temperature 25°C	1087	--	1113	mV
		Low to High transition, at temperature -40 +85°C (Note 3)	1080	--	1113	mV
		High to Low transition, at temperature 25°C	1087	--	1112	mV
		High to Low transition, at temperature -40 +85°C (Note 3)	1080	--	1112	mV
LDO0	LDO0 output voltage	Vout0 voltage	--	1.10	--	V
		Vout1 voltage	--	1.10	--	V
LDO1	LDO1 output voltage	Vout0 voltage	--	1.80	--	V
		Vout1 voltage	--	1.80	--	V
$T_{SU}$	Startup Time	From VDD rising past $PON_{THR}$	--	1.3	--	ms
$PON_{THR}$	Power On Threshold	$V_{DD}$ Level Required to Start Up the Chip	1.34	1.55	1.74	V

POFF <sub>THR</sub>	Power Off Threshold	V <sub>DD</sub> Level Required to Switch Off the Chip	1.05	1.25	1.45	V
---------------------	---------------------	---	------	------	------	---

**Note:**

- DC or average current through any pin should not exceed value given in Absolute Maximum Conditions.
- The GreenPAK's power rails are divided in two sides. PINs 1, 2, 3, 4, 5 and 6 are connected to one side, PINs 8, 9, 10, 18 and 19 to another.
- Guaranteed by Design.

## I<sup>2</sup>C Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
F <sub>SCL</sub>	Clock Frequency, SCL	V <sub>DD</sub> = (2.3...5.5) V	--	--	400	kHz
t <sub>LOW</sub>	Clock Pulse Width Low	V <sub>DD</sub> = (2.3...5.5) V	1300	--	--	ns
t <sub>HIGH</sub>	Clock Pulse Width High	V <sub>DD</sub> = (2.3...5.5) V	600	--	--	ns
t <sub>i</sub>	Input Filter Spike Suppression (SCL, SDA)	V <sub>DD</sub> = 2.5V ± 8%	--	--	168	ns
		V <sub>DD</sub> = 3.3V ± 10%	--	--	157	ns
		V <sub>DD</sub> = 5.0V ± 10%	--	--	156	ns
t <sub>AA</sub>	Clock Low to Data Out Valid	V <sub>DD</sub> = (2.3...5.5) V	--	--	900	ns
t <sub>BUF</sub>	Bus Free Time between Stop and Start	V <sub>DD</sub> = (2.3...5.5) V	1300	--	--	ns
t <sub>HD_STA</sub>	Start Hold Time	V <sub>DD</sub> = (2.3...5.5) V	600	--	--	ns
t <sub>SU_STA</sub>	Start Set-up Time	V <sub>DD</sub> = (2.3...5.5) V	600	--	--	ns
t <sub>HD_DAT</sub>	Data Hold Time	V <sub>DD</sub> = (2.3...5.5) V	0	--	--	ns
t <sub>SU_DAT</sub>	Data Set-up Time	V <sub>DD</sub> = (2.3...5.5) V	100	--	--	ns
t <sub>R</sub>	Inputs Rise Time	V <sub>DD</sub> = (2.3...5.5) V	--	--	300	ns
t <sub>F</sub>	Inputs Fall Time	V <sub>DD</sub> = (2.3...5.5) V	--	--	300	ns
t <sub>SU_STO</sub>	Stop Set-up Time	V <sub>DD</sub> = (2.3...5.5) V	600	--	--	ns
t <sub>DH</sub>	Data Out Hold Time	V <sub>DD</sub> = (2.3...5.5) V	50	--	--	ns

## LDO Regulator Thermal Limitations

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
IC <sub>TL</sub>	Thermal Limitation	85 °C ambient, Total IC package	--	--	0.6	W
		70 °C ambient, Total IC package	--	--	0.8	W
		Max Watt per LDO <sup>1</sup>	--	--	0.5	W
Shutdown	Thermal Shutdown <sup>2</sup>		115	125	135	°C
	Thermal Shutdown Recovery		90	100	110	°C

**Note:**

- Please note that Max Watt LDO multiplied by number of LDOs can easily exceed the Max Watt for the total IC package. In this case an external resistor should be used on LDO Vin to lower the voltage drop across the LDO Regulator.
- Lower Thermal shutdown levels may be achieved by using the temperature sensor and comparator.

## LDO HP MODE Electrical Specifications

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
I <sub>OUT</sub>	Output Current Rating		--	--	300	mA
V <sub>IN</sub>	Voltage Input		2.3	--	V <sub>DD</sub>	V
V <sub>DO</sub>	Voltage Dropout		--	250	300	mV
ΔV <sub>OUT</sub>		over PVT of V <sub>OUT</sub> > 1.5 V	-3	--	+3	%

**FFPGADMOR2.0\_U8\_PWRCTRL\_0x08\_R1.0**

	Output Voltage Accuracy (see Note 1)	over PVT of $V_{OUT} \leq 1.5\text{ V}$	-60	--	+60	mV
$e_N$	Noise Voltage (rms)	10 Hz to 100 kHz	--	75	--	$\mu\text{V}$
PSRR	Power Supply Rejection Ratio (see Note 2)	100 Hz to 100 kHz	TBD	50	--	dB
CTRR	Crosstalk Rejection Ratio	LDO0 to LDO1 regulation perturbation, and LDO2 to LDO3 perturbation at 0 to 150 mA at 1 kHz at 1.8 V $V_{OUT}$	TBD	50	--	dB
$\Delta V_{LINE}$	Line Regulation	$V_{OUT} + 0.5\text{ V} < V_{IN} \leq 5.5\text{ V}$	-1%	--	+1%	%/V
$\Delta V_{LOAD}$	Load Regulation	$1\text{ mA} < I_{OUT} < 150\text{ mA}$	--	--	0.3	mV/ mA
$\Delta V_{TC}$	$V_{OUT}$ Temp Coefficient		--	100	--	ppm/ C
$C_{IN}$	External Input Capacitor (see Note 2)		2	--	--	$\mu\text{F}$
$C_{OUT}$	External Output Capacitor		4	--	--	$\mu\text{F}$
$t_{SS\_0}$	Soft Start Option 0 Time	$V_{OUT}$ 5% to 95%	-20%	10	+20%	V/ms
$t_{SS\_1}$	Soft Start Option 1 Time	$V_{OUT}$ 5% to 95%	-20%	20	+20%	V/ms
$t_{SS\_2}$	Soft Start Option 2 Time	$V_{OUT}$ 5% to 95%	-30%	1.25	+30%	V/ms
$t_{SS\_3}$	Soft Start Option 3 Time	$V_{OUT}$ 5% to 95%	-30%	2.50	+30%	V/ms
SC	Short Circuit Protection		TBD	TBD	TBD	mA
$t_{WAIT}$	Wait Time	Time from EN=1 to $V_{OUT}$ start rise	--	500	--	$\mu\text{s}$
$R_D$	Output Discharge Pull-down Resistance	EN=0, Dis_EN = 1	--	300	--	$\Omega$

**Note:**

1. Accuracy specifies all the effects of line regulation ( $\Delta V_{LINE}$ ), load regulation ( $\Delta V_{LOAD}$ ), and temperature coefficient ( $\Delta V_{TC}$ ),
2. X7R-type and X5R-type capacitors are recommended

**Chip address**

HEX	BIN	DEC
0x08	0001000	8

## I2C Description

### 1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<1867:1864>. The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of the data to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specific data byte to be read or written in the command. Figure 1 shows this basic command structure.

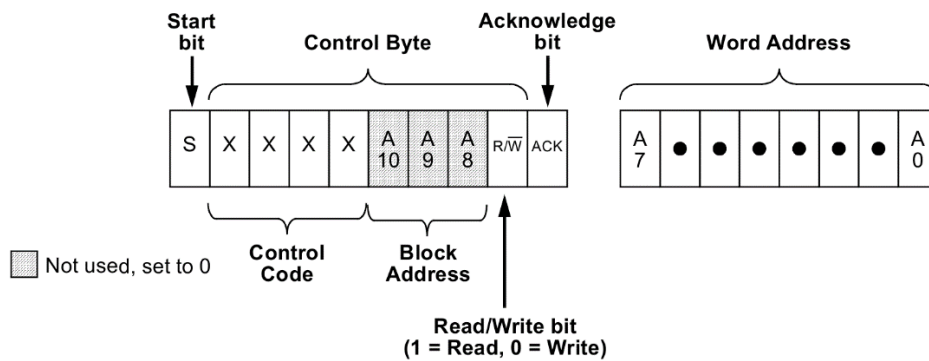


Figure1. I2C Basic Command Structure

### 2. I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

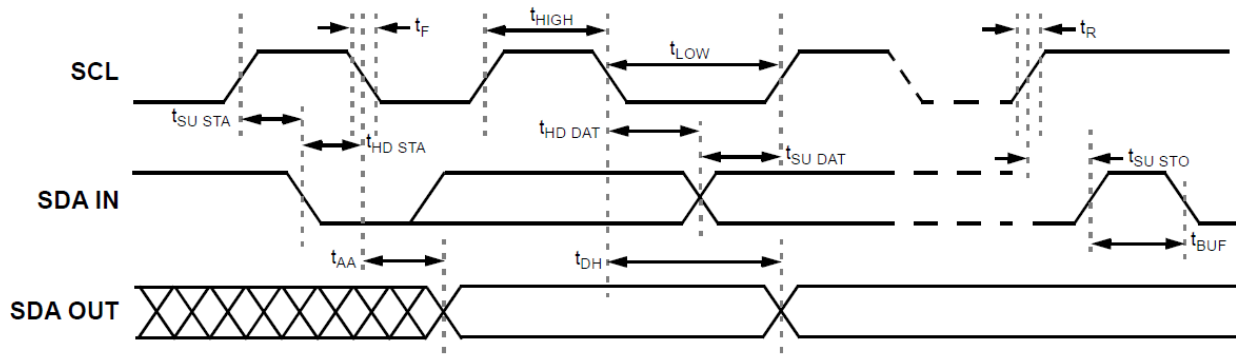


Figure2. I2C Serial General Timing



3. I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to “0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledge bit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG7RN46383 to the correct data byte to be written. After the SLG7RN46383 sends another Acknowledge bit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG7RN46383 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG7RN46383 generates the Acknowledge bit.

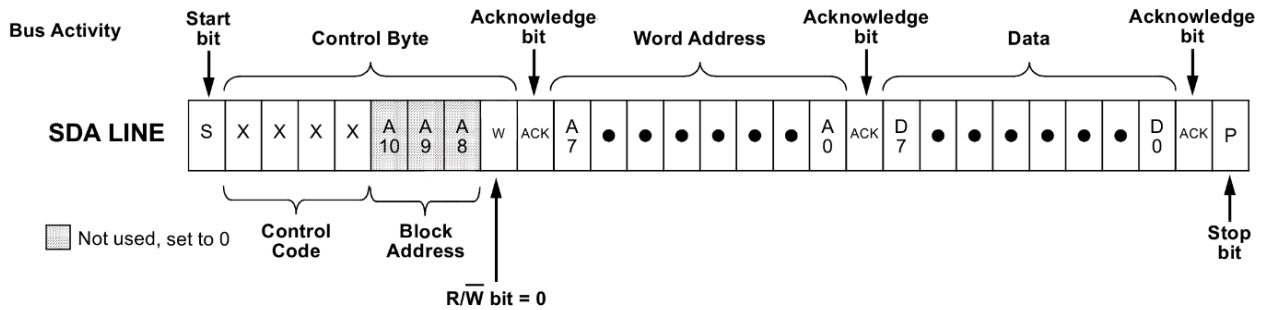


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with  $\overline{R/W}$  bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the same as the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the  $\overline{R/W}$  bit set to “1”, after which the SLG7RN46383 issues an Acknowledge bit, followed by the requested eight data bits.

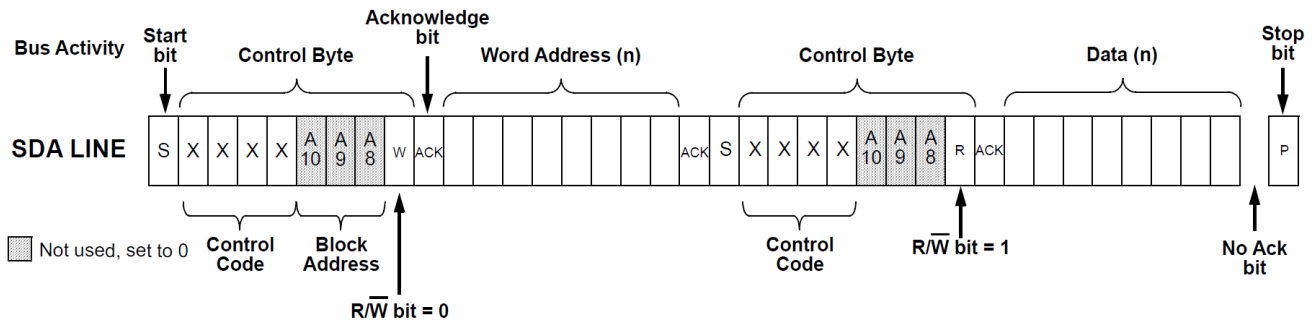
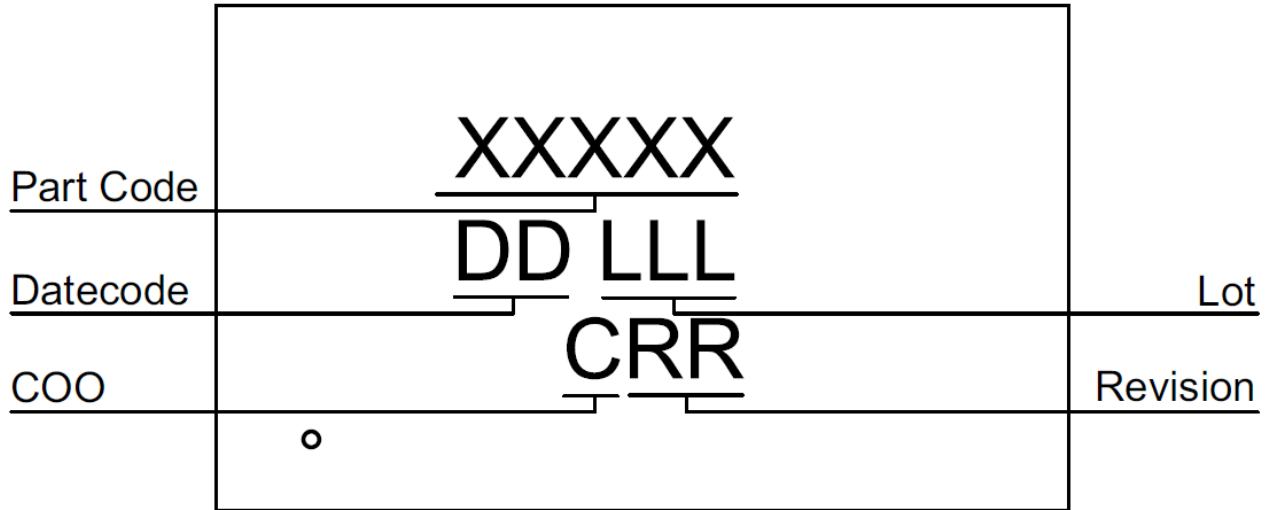


Figure4. I2C Random Read Command

#### Package Top Marking



- XXXXX – Part ID Field: identifies the specific device configuration
- DD – Date Code Field: Coded date of manufacture
- LLL – Lot Code: Designates Lot #
- C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
- RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Lock Status	Checksum	Part Code	Revision	Date
0.11	001	U	0x89B9C629	46383	AA	03/22/2023

Lock coverage for this part is indicated by  $\checkmark$ , from one of the following options:

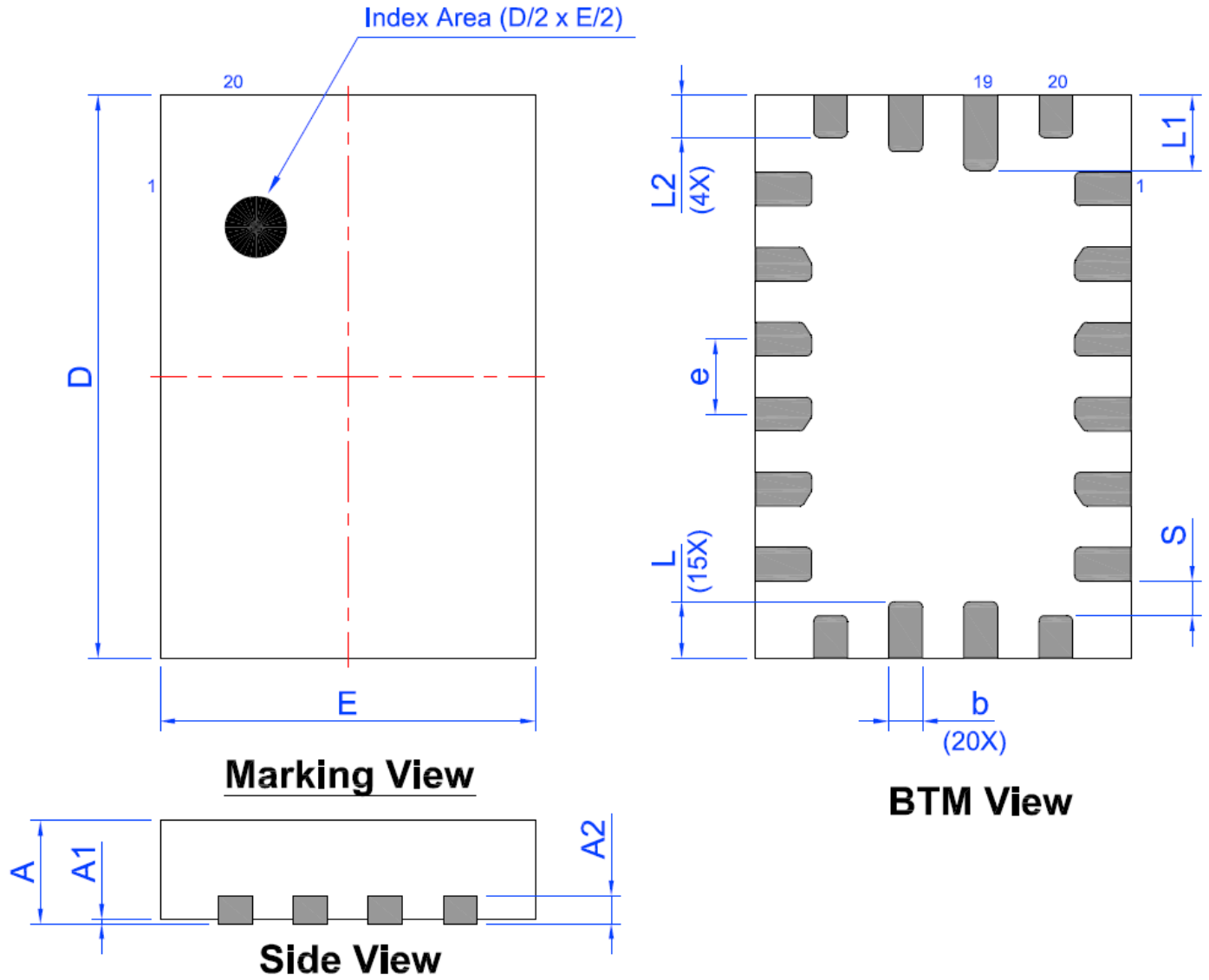
$\checkmark$	Unlocked
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for write all bits
	Locked for read and write bits <1535:0>
	Locked for read bits <1535:0> and write of all bits

The IC security bit is locked/set for code security for production unless otherwise specified. The Programming Code Number is not changed based on the choice of locked vs. unlocked status.

### Package Drawing and Dimensions

STQFN 20L 2x3mm 0.4P FCD Package

JEDEC MO-220, Variation WECE



Unit: mm

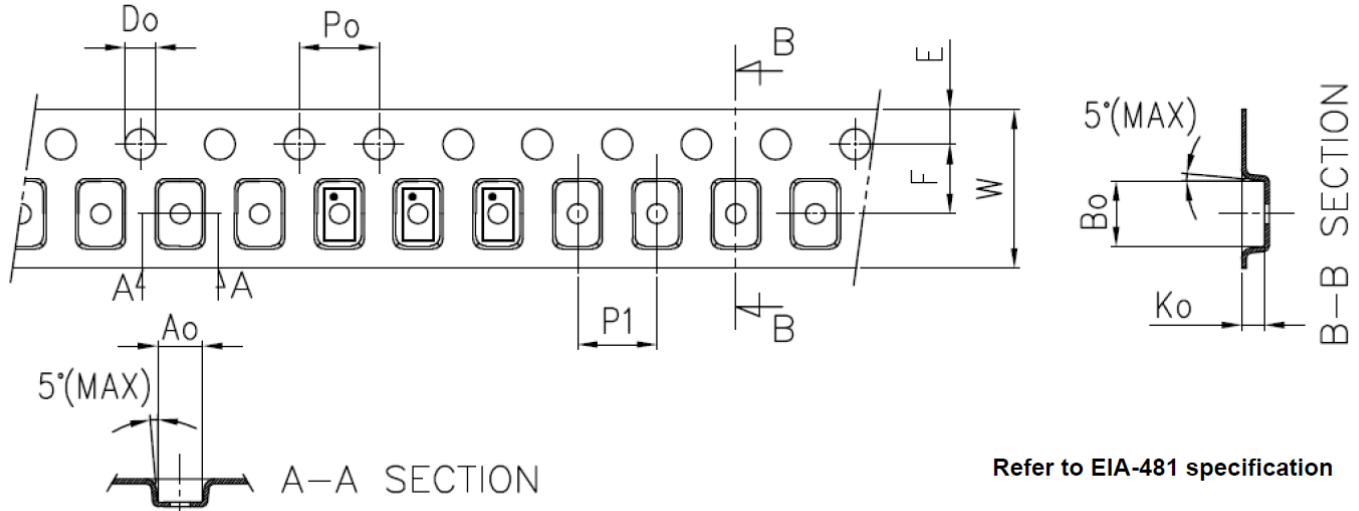
Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L	0.25	0.30	0.35
b	0.13	0.18	0.23	L1	0.35	0.40	0.45
e	0.40 BSC			L2	0.175	0.225	0.275
S	0.185 TYP						

### Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size [mm]	Max Units		Reel & Hub Size [mm]	Leader (min)		Trailer (min)		Tape Width [mm]	Part Pitch [mm]
			per Reel	per Box		Pockets	Length [mm]	Pockets	Length [mm]		
STQFN 20L 2x3mm 0.4P FCD	20	2 x 3 x 0.55	3000	3000	178/60	100	400	100	400	8	4

### Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length	Pocket BTM Width	Pocket Depth	Index Hole Pitch	Pocket Pitch	Index Hole Diameter	Index Hole to Tape Edge	Index Hole to Pocket Center	Tape Width
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P FCD	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8



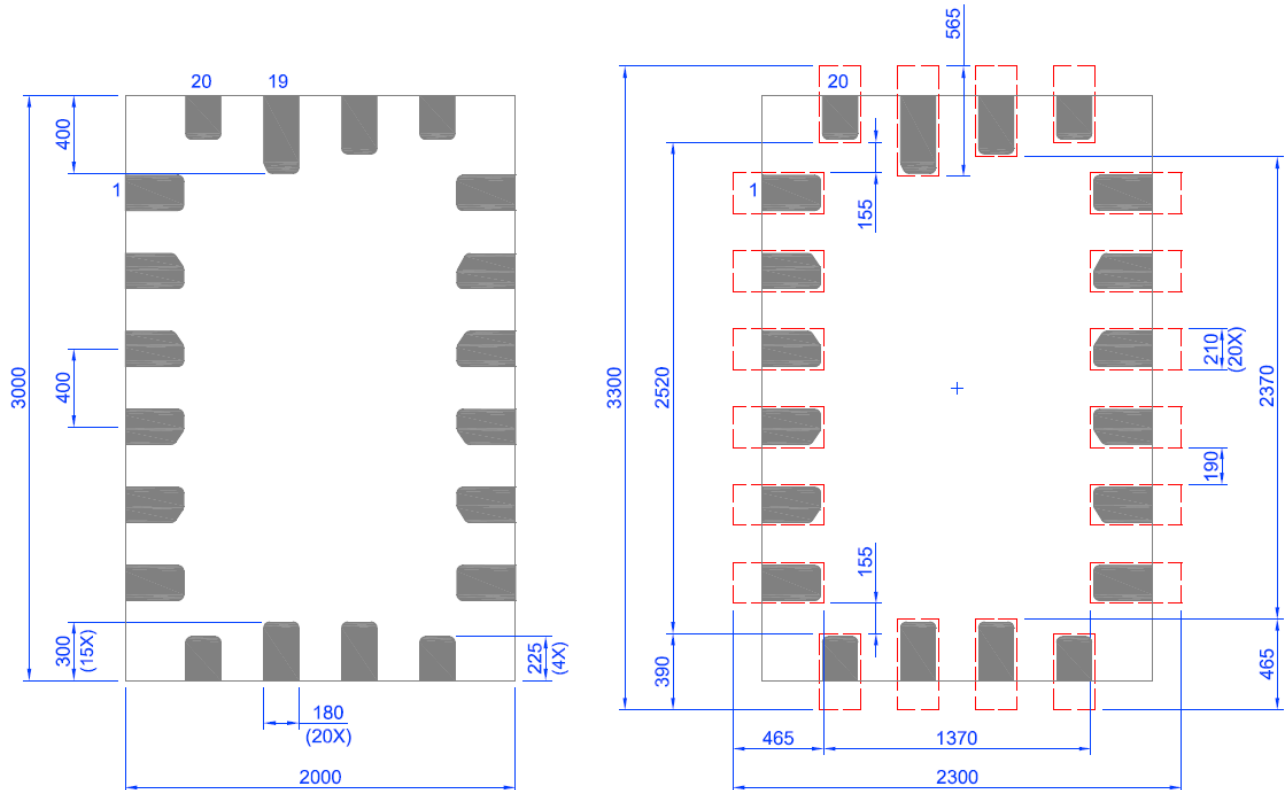
### Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.30 mm<sup>3</sup> (nominal). More information can be found at [www.jedec.org](http://www.jedec.org).

#### Recommended Land Pattern

 Exposed Pad  
(PKG face down)

 Recommended Land Pattern  
(PKG face down)



Unit:um

**Datasheet Revision History**

<b>Date</b>	<b>Version</b>	<b>Change</b>
03/14/2023	0.10	New design for SLG46582 chip
03/22/2023	0.11	Updated Device Revision Table

## IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

### Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,  
Koto-ku, Tokyo 135-0061, Japan  
[www.renesas.com](http://www.renesas.com)

### Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

### Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit [www.renesas.com/contact-us/](http://www.renesas.com/contact-us/).