28-Bit Configurable Registered Buffer for DDR2

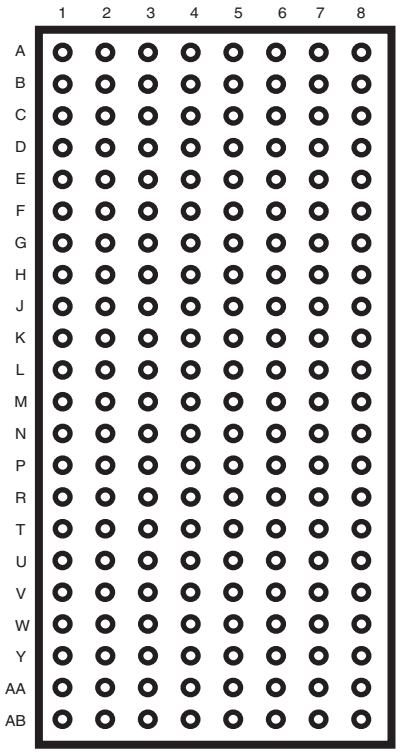
Recommended Application:

- DDR2 Memory Modules
- Provides complete DDR DIMM solution with ICS97U877
- Ideal for DDR2 400, 533 and 667

Product Features:

- 28-bit 1:2 registered buffer with parity check functionality
- Supports SSTL_18 JEDEC specification on data inputs and outputs
- Supports LVCMOS switching levels on CSGEN and RESET# inputs
- Low voltage operation V_{DD} = 1.7V to 1.9V
- Available in 176 BGA package
- Green packages available

Pin Configuration



176 Ball BGA
(Top View)

Functionality Truth Table

Inputs							Outputs			
RST#	DCS0#	DCS1#	CSGEN	CK	CK#	Dn, DODTn, DCKEn	Qn	QCS0#	QCS1#	QODT, QCKE
H	L	L	X	↑	↓	L	L	L	L	L
H	L	L	X	↑	↓	H	H	L	L	H
H	L	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	L	H	X	↑	↓	L	L	L	H	L
H	L	H	X	↑	↓	H	H	L	H	H
H	L	H	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	L	X	↑	↓	L	L	H	L	L
H	H	L	X	↑	↓	H	H	H	L	H
H	H	L	X	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	L	↑	↓	L	L	H	H	L
H	H	H	L	↑	↓	H	H	H	H	H
H	H	H	L	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
H	H	H	H	↑	↓	L	Q_0	H	H	L
H	H	H	H	↑	↓	H	Q_0	H	H	H
H	H	H	H	L or H	L or H	X	Q_0	Q_0	Q_0	Q_0
L	X or floating	X or floating	X or floating	X or floating	X or floating	X or floating	L	L	L	L

08/14/06

Ball Assignments

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6 (DCKE1)	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8 (DCKE0)	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A (QCKE1A)	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A QCKE0A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B (QCKE1B)
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B (QCKE0B)
J	DCS1#	QCS1A#	GND	GND	GND	GND	Q10B	Q9B
K	DCS0#	QCS0A#	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QCS0B#)	Q13B (QCS1B#)
M	CK3	RESET#	QERR#	V_{DD}	V_{DD}	V_{DD}	Q15B (QODT0B)	Q16B (QODT1B)
N	D15 (DODT0)	Q15A (QODT0A)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DODT1)	Q16A (Q0DT1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B
T	D18	Q19A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A	GND	GND	GND	GND	Q22A	Q23B
V	D20	Q23A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	VDD	Q28A	Q28B

1:2 Register A (C=0)

Note: NC denotes a no-connect (ball present but not connected to the die).

Ball Assignments

	1	2	3	4	5	6	7	8
A	D2	D1	C	GND	V_{REF}	GND	Q1A	Q1B
B	D4	D3	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q2A	Q2B
C	D6	D5	GND	GND	GND	GND	Q3A	Q3B
D	D8	D7	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q4A	Q4B
E	D9	Q6A	GND	GND	GND	GND	Q5A	Q5B
F	D10	Q8A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q7A	Q6B
G	D11	Q10A	GND	GND	GND	GND	Q9A	Q7B
H	D12	Q12A	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q11A	Q8B
J	D13 (DODT1)	Q13A (QODT1A)	GND	GND	GND	GND	Q10B	Q9B
K	D14 (DODT0)	Q14A (QODT0A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q12B	Q11B
L	CK	CSGEN	PAR_IN	GND	GND	GND	Q14B (QODT0B)	Q13B (QODT1B)
M	CK#	RESET#	QERR#	V_{DD}	V_{DD}	V_{DD}	Q15B (QCS0B#)	Q16B (QCS1B#)
N	D15 (DCS0#)	Q15A (QCS0#)	GND	GND	GND	GND	Q17B	Q18B
P	D16 (DCS1#)	Q16A (QCS1A#)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q19B	Q20B
R	D17	Q17A	GND	GND	GND	GND	Q18A	Q21B (QCKE0B)
T	D18	Q19	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q20A	Q22B
U	D19	Q21A (QCKE0A)	GND	GND	GND	GND	Q22A	Q23B (QCKE1B)
V	D20	Q23A (QCKE1A)	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q24A	Q24B
W	D21 (DCKE0)	D22	GND	GND	GND	GND	Q25A	Q25B
Y	D23 (DCKE1)	D24	V_{DD}	V_{DD}	V_{DD}	V_{DD}	Q26A	Q26B
AA	D25	D26	GND	GND	GND	GND	Q27A	Q27B
AB	D27	D28	NC	V_{DD}	V_{REF}	VDD	Q28A	Q28B

1:2 Register B (C=1)

Note: NC denotes a no-connect (ball present but not connected to the die).

08/14/06

General Description

This 28-bit 1:2 configurable registered buffer is designed for 1.7-V to 1.9-V VDD operation. All inputs are compatible with the JEDEC standard for SSTL_18, except the chip-select gate-enable (CSGEN), control (C), and reset (RESET) inputs, which are LVCMOS. All outputs are edge-controlled circuits optimized for unterminated DIMM loads, and meet SSTL_18 specifications, except the open-drain error (QERR) output.

The **ICSSSTUB32S868D** operates from a differential clock (CK and CK). Data are registered at the crossing of CK going high and CK going low. The device supports low-power standby operation. When RESET is low, the differential input receivers are disabled, and undriven (floating) data, clock, and reference voltage (VREF) inputs are allowed. In addition, when RESET is low, all registers are reset and all outputs are forced low except QERR. The LVCMOS RESET and C inputs always must be held at a valid logic high or low level. To ensure defined outputs from the register before a stable clock has been supplied, RESET must be held in the low state during power up. In the DDR2 RDIMM application, RESET is specified to be completely asynchronous with respect to CK and CK. Therefore, no timing relationship can be ensured between the two. When entering reset, the register will be cleared and the data outputs will be driven low quickly, relative to the time to disable the differential input receivers. However, when coming out of reset, the register will become active quickly, relative to the time to enable the differential input receivers. As long as the data inputs are low, and the clock is stable during the time from the low-to-high transition of RESET until the input receivers are fully enabled, the design of the **ICSSSTUB32S868D** must ensure that the outputs will remain low, thus ensuring no glitches on the output.

Inputs							Output
RST#	DCS0#	DCS1#	CK	CK#	Σ of inputs = H (D1 - D28)	PAR_IN†	QERR#‡
H	L	X	↑	↓	Even	L	H
H	L	X	↑	↓	Odd	L	L
H	L	X	↑	↓	Even	H	L
H	L	X	↑	↓	Odd	H	H
H	X	L	↑	↓	Even	L	H
H	X	L	↑	↓	Odd	L	L
H	X	L	↑	↓	Even	H	L
H	X	L	↑	↓	Odd	H	H
H	H	H	↑	↓	X	X	$QERR\#_0$ §
H	X	X	L or H	L or H	X	X	$QERR\#_0$
L	X or floating	X or floating	X or floating	X or floating	X	X or floating	H

† PAR_IN arrives one clock cycle after the data to which it applies.

‡ This transition assumes QERR# is high at the crossing of CK going high and CK# going low. If QERR# is low, it stays latches low for two clock cycles or until RST# is driven low.

§ If DCS0#, DCS1#, and CSGEN are driven high, the device is placed in low-power mode (LPM). If a parity error occurs on the clock cycle before the device enters the LPM and the QERR# output is driven low, it stays latches low for the LPM duration plus two clock cycles or until RST# is driven low.

08/14/06

General Description (Continued)

The **ICSSSTUB32S868D** includes a parity checking function. Parity, which arrives one cycle after the data input to which it applies, is checked on the PAR_IN input of the device. The corresponding QERR output signal for the data inputs is generated two clock cycles after the data, to which the QERR signal applies, is registered. The **ICSSSTUB32S868D** accepts a parity bit from the memory controller on the parity bit (PAR_IN) input, compares it with the data received on the DIMM-independent D-inputs (D1-D5, D7, D9-D12, D17-D28 when C = 0; or D1-D12, D17-D20, D22, D24-D28 when C = 1) and indicates whether a parity error has occurred on the open-drain QERR pin (active low). The convention is even parity, i.e., valid parity is defined as an even number of ones across the DIMM-independent data inputs combined with the parity input bit. To calculate parity, all DIMM-independent D-inputs must be tied to a known logic state. If an error occurs and the QERR output is driven low, it stays latched low for a minimum of two clock cycles or until RESET is driven low. If two or more consecutive parity errors occur, the QERR output is driven low and latched low for a clock duration equal to the parity error duration or until RESET is driven low. If a parity error occurs on the clock cycle before the device enters the low-power (LPM) and the QERR output is driven low, then it stays lateched low for the LPM duration plus two clock cycles or until RESET is driven low. The DIMM-dependent signals (DCKE0, DCKE1, DODT0, DODT1, DCS0 and DCS1) are not included in the parity check computation.

The C input controls the pinout configuration from register-A configuration (when low) to register-B configuration (when high). The C input should not be switched during normal operation. It should be hardwired to a valid low or high level to configure the register in the desired mode. The device also supports low-power active operation by monitoring both system chip select (DCS0 and DCS1) and CSGEN inputs and will gate the Qn outputs from changing states when CSGEN, DCS0, and DCS1 inputs are high. If CSGEN, DCS0 or DCS1 input is low, the Qn outputs will function normally. Also, if both DCS0 and DCS1 inputs are high, the device will gate the QERR output from changing states. If either DCS0 or DCS1 is low, the QERR output will function normally. The RESET input has priority over the DCS0 and DCS1 control and when driven low will force the Qn outputs low, and the QERR output high. If the chip-select control functionality is not desired, then the CSGEN input can be hard-wired to ground, in which case, the setup-time requirement for DCS0 and DCS1 would be the same as for the other D data inputs. To control the low-power mode with DCS0 and DCS1 only, then the CSGEN input should be pulled up to VDD through a pullup resistor. The two VREF pins (A1 and V1) are connected together internally by approximately 150 .. However, it is necessary to connect only one of the two VREF pins to the external VREF power supply. An unused VREF pin should be terminated with a VREF coupling capacitor.

Ball Assignment

Terminal name	Description	Electrical characteristics
GND	Ground	Ground input
V_{DD}	Power supply voltage	1.8-V nominal
V_{REF}	Input reference voltage	0.9-V nominal
CK	Positive master clock input	Differential input
CK#	Negative master clock input	Differential input
C	Configuration control inputs - Register A or Register B	LVCMOS inputs
RST#	Asynchronous reset input – resets registers and disables VREF data and clock differential-input receivers	LVCMOS input
CSGEN	Chip select gate enable – When high, D1-D28† inputs will be latched only when at least one chip select input is low during the rising edge of the clock. When low, theD1-D28† inputs will be latched and redriven on every rising edge of the clock.	LVCMOS input
D1-D28†	Data input – clocked in on the crossing of the rising edge of CK and the falling edge of CK#.	SSTL_18 input
DCS0#, DCS1#	Chip select inputs – These pins initiate DRAM address/command decodes, and as such at least one will be low when a valid address/command is present. The Register can be programmed to redrive all D inputs (CSGEN high) only when atleast one chip select input is low. If CSGEN, DCS0#, and DCS1# inputs are high, D1–D28† inputs will be disabled.	SSTL_18 input
DODT0, DODT1	The outputs of this register bit will not be suspended by the DC0# and DCS1# control.	SSTL_18 input
DCKE0, DCKE1	The outputs of this register bit will not be suspended by the DC0# and DCS1# control.	SSTL_18 input
PAR_IN	Parity input - arrives one clock cycle after the corresponding data input.	SSTL_18 input
Q1-Q28‡	Data outputs that are suspended by the DC0# and DCS1# control.	1.8-V CMOS outputs
QCS0#, QCS1#	Data output that will not be suspended by the DC0# and DCS1# control.	1.8-V CMOS output
QODT0, QODT1	Data output that will not be suspended by the DC0# and DCS1# control.	1.8-V CMOS output
QCKE0, QCKE1	Data output that will not be suspended by the DC0# and DCS1# control.	1.8-V CMOS output
QERR#	Output error bit - generated one clock cycle after the corresponding data output	Open-drain output
NC	No internal connection	

† Data inputs = D1-D5, D7, D9-D12, D17-D28 when C=0

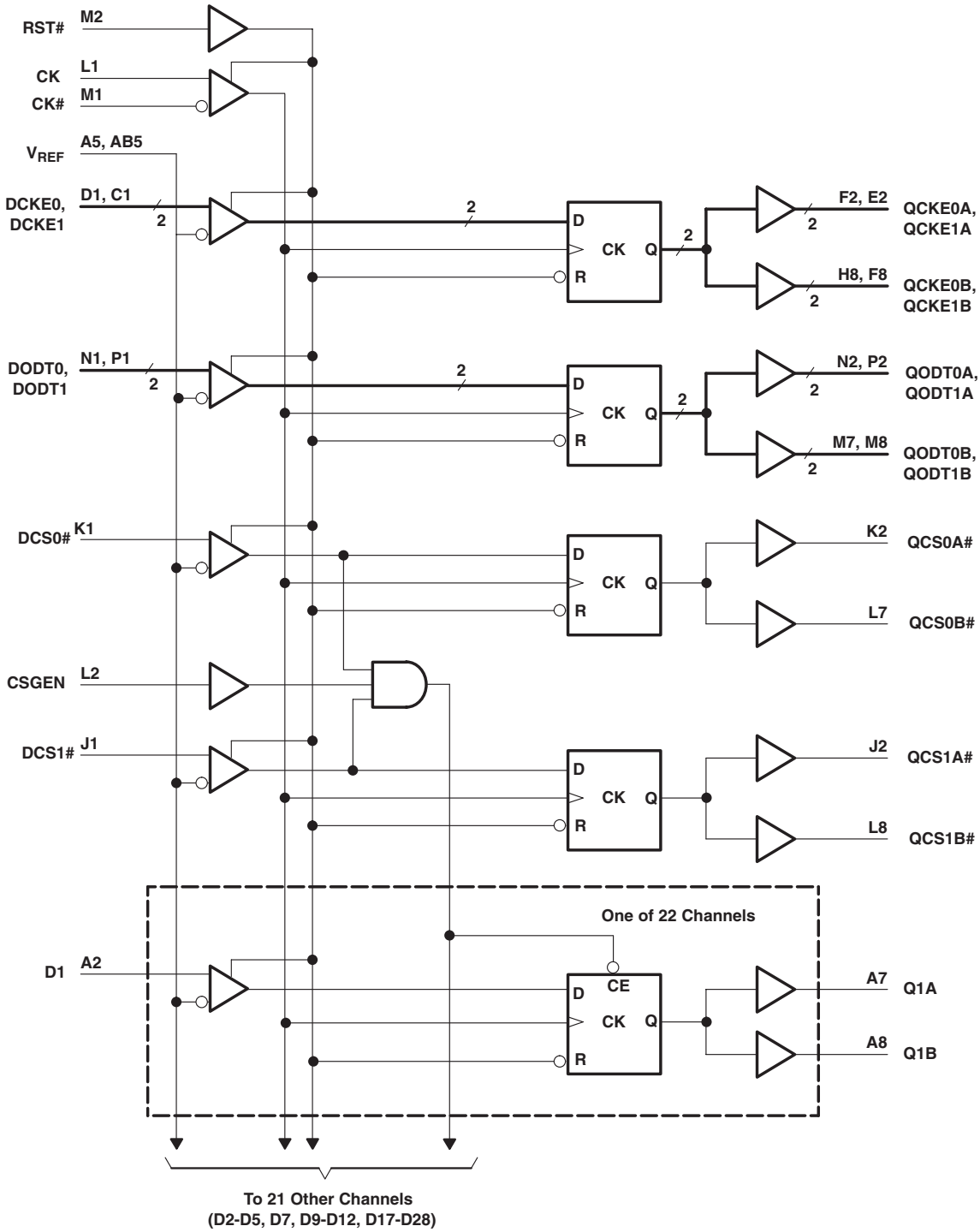
Data inputs = D1-D12, D17-D20, D22, D24-D28 when C=1

‡ Data outputs = Q1-Q5, Q7, Q9-Q12, Q17-Q28 when C=0

Data outputs = Q1-Q12, Q17-Q20, Q22, Q24-Q28 when C=1

08/14/06

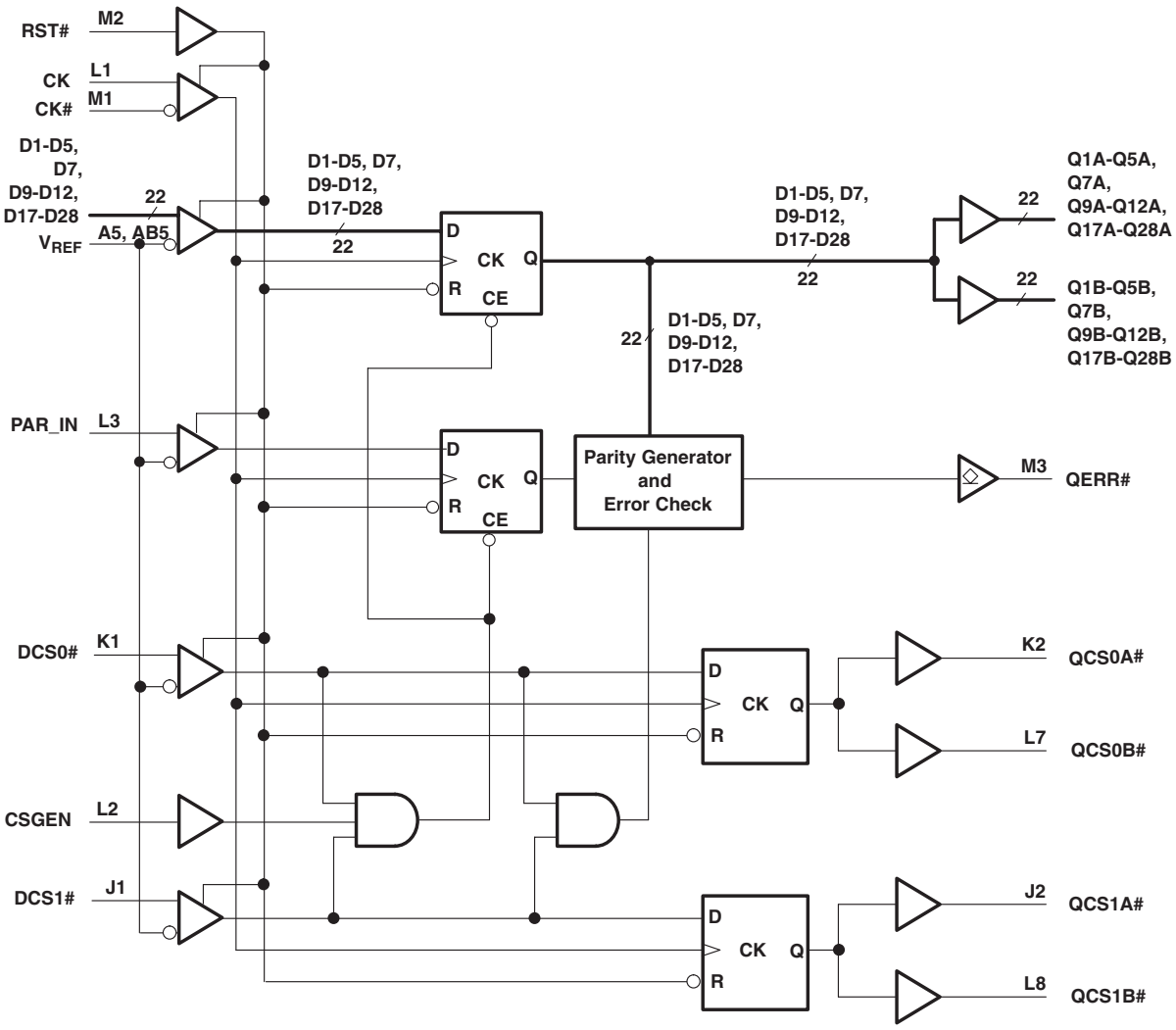
Block Diagram



Register A configuration with C= O; (positive logic)

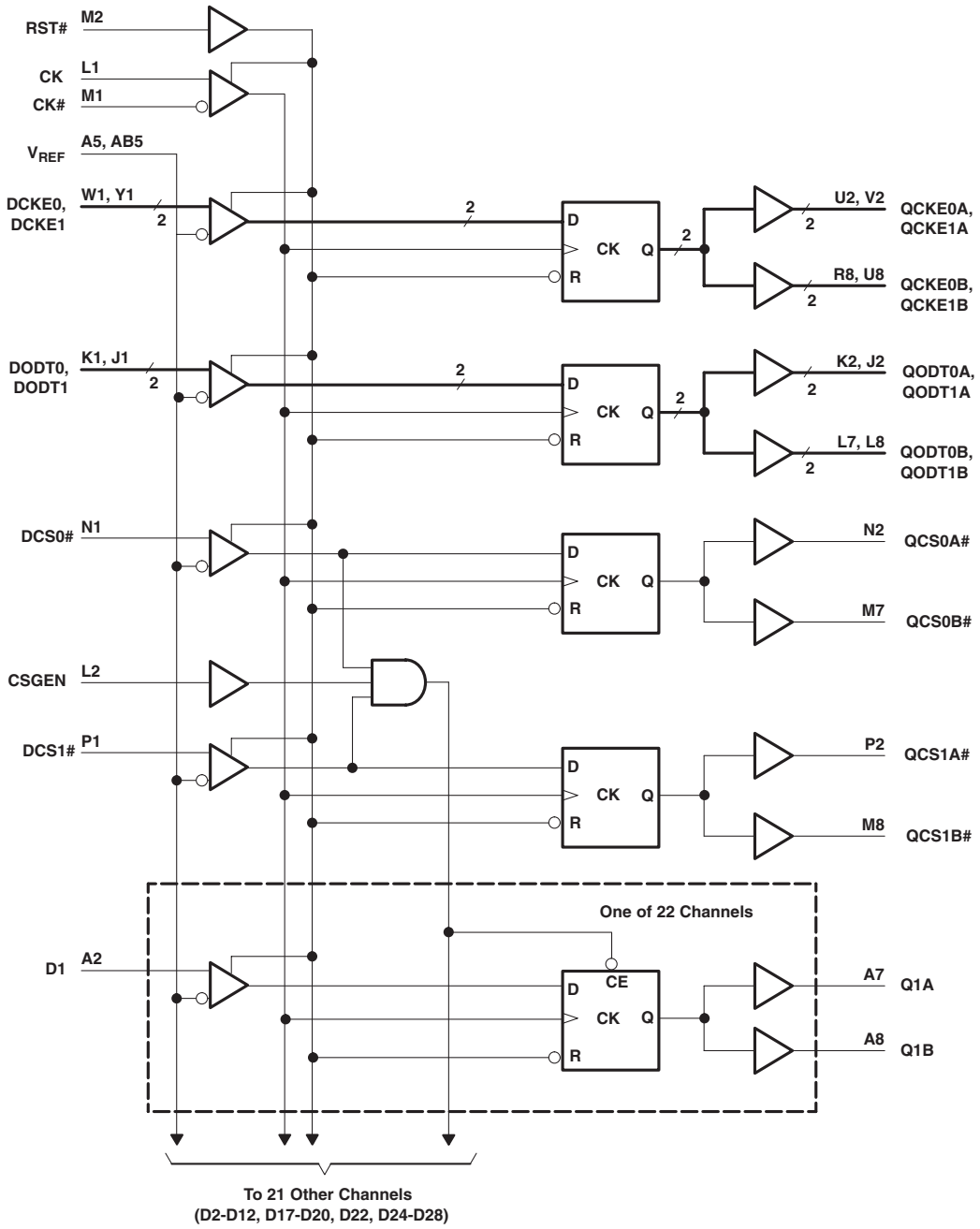
08/14/06

Parity Logic Diagram



Register A configuration with C= O; (positive logic)

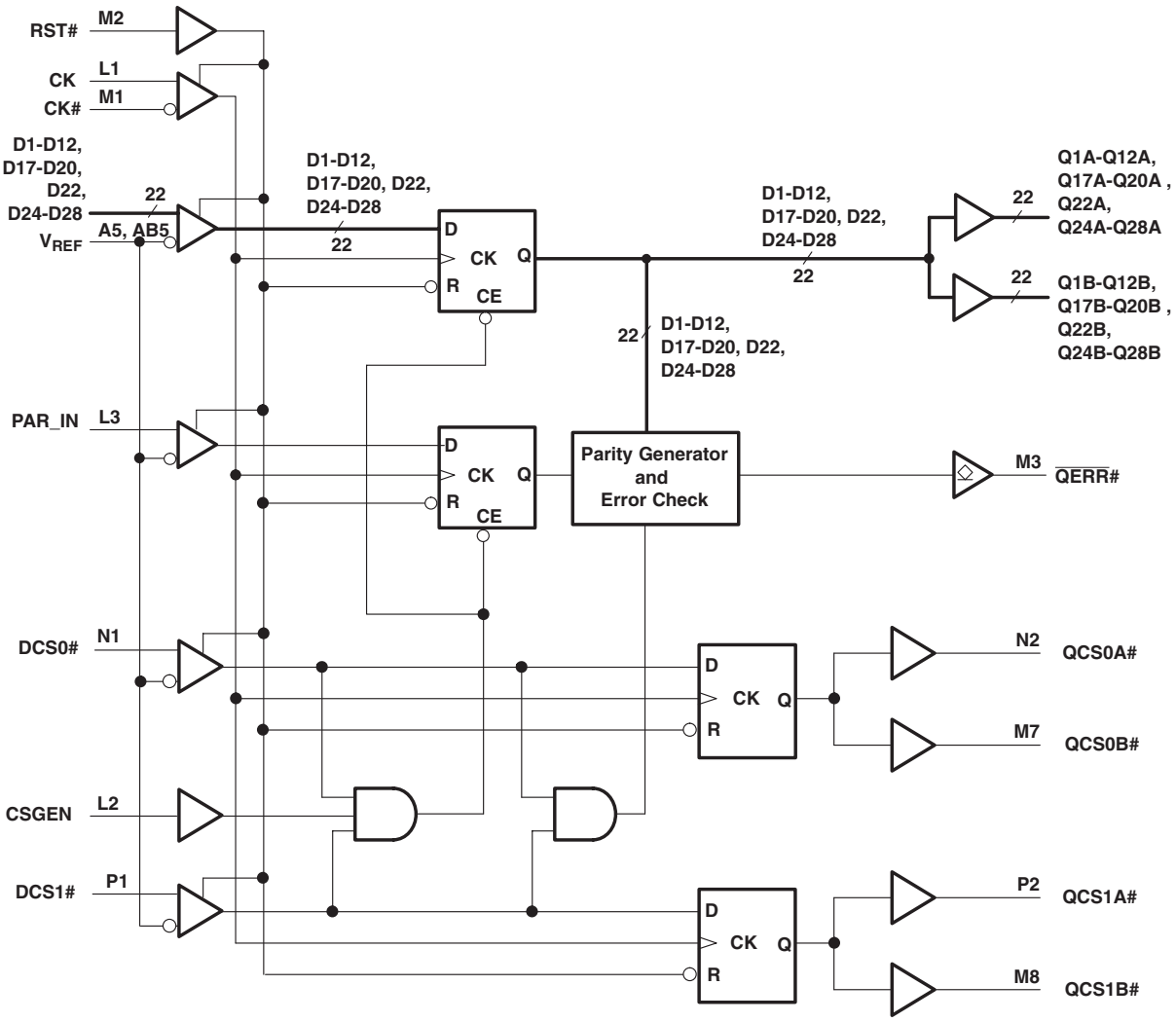
Block Diagram



Register B configuration with C= 1; (positive logic)

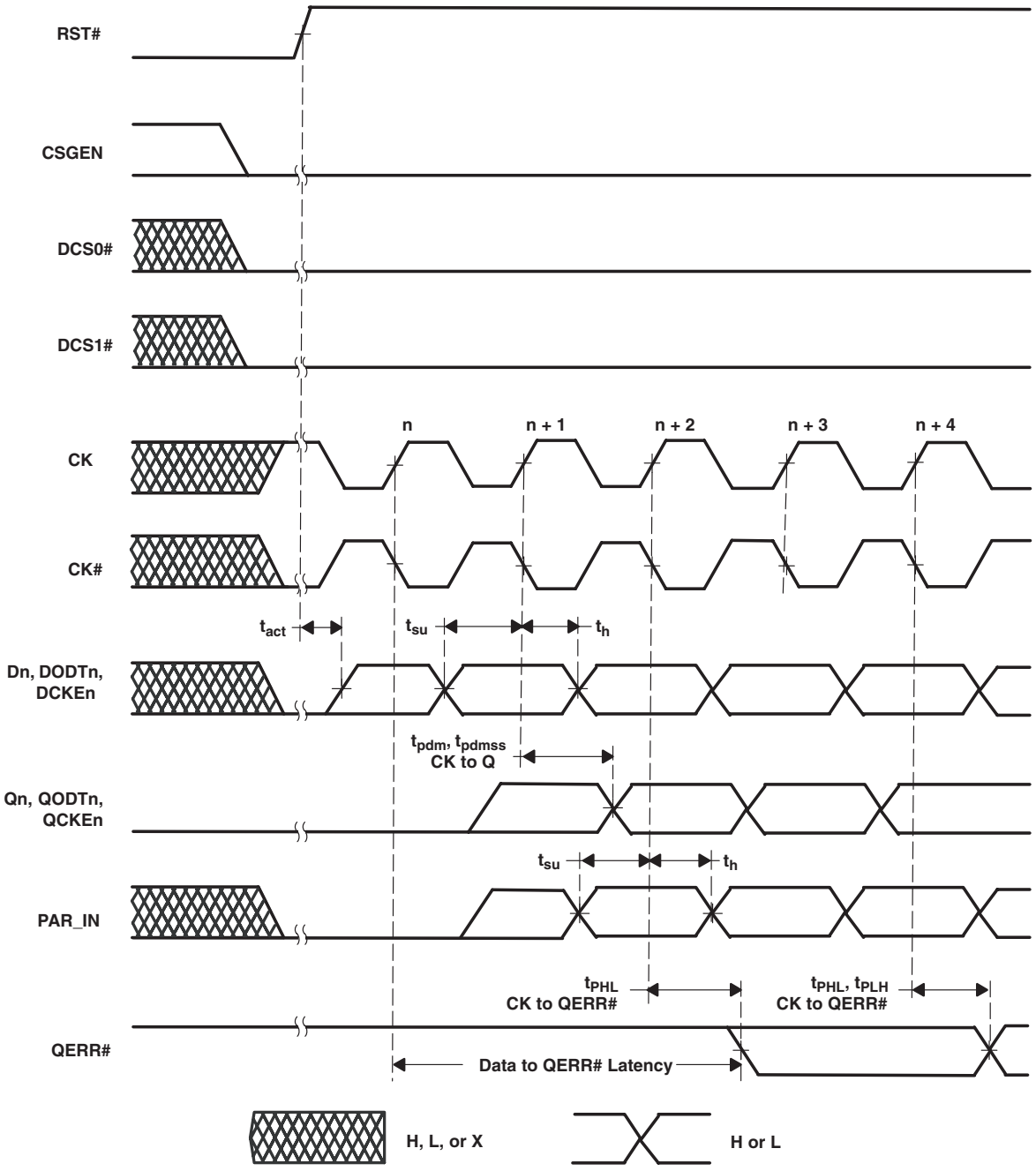
08/14/06

Parity Logic Diagram



Register B configuration with C= 1; (positive logic)

Register Timing

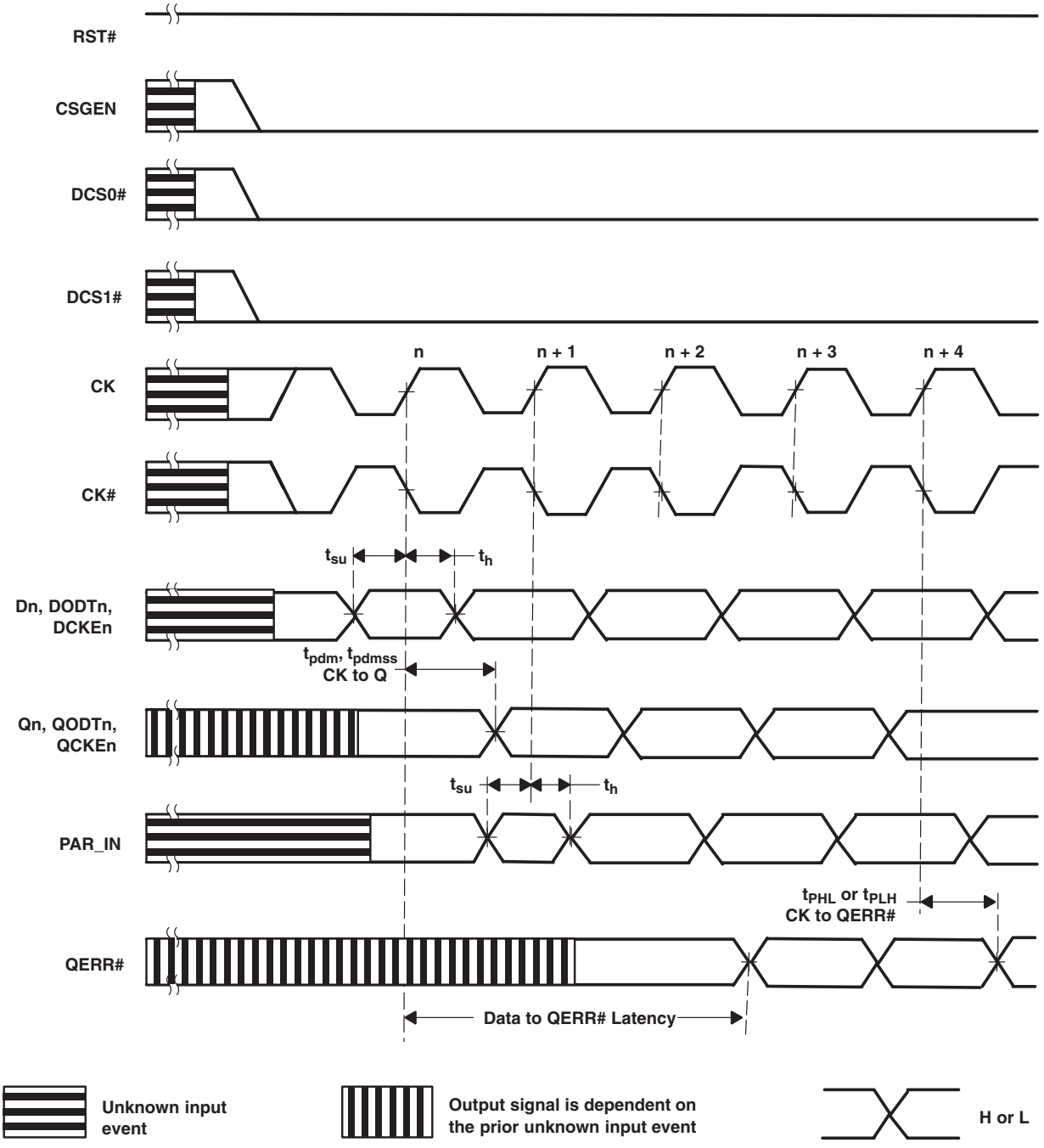


† After RESET# is switched from low to high, all data and PAR_IN input signals must be set and held low for a minimum time of tact max, to avoid false error.

‡ If the data is clocked in on the n clock pulse, the QERR# output sognal will be produced on the n+2 clock pulse and it will be valid on the n+3 clock pulse.

08/14/06

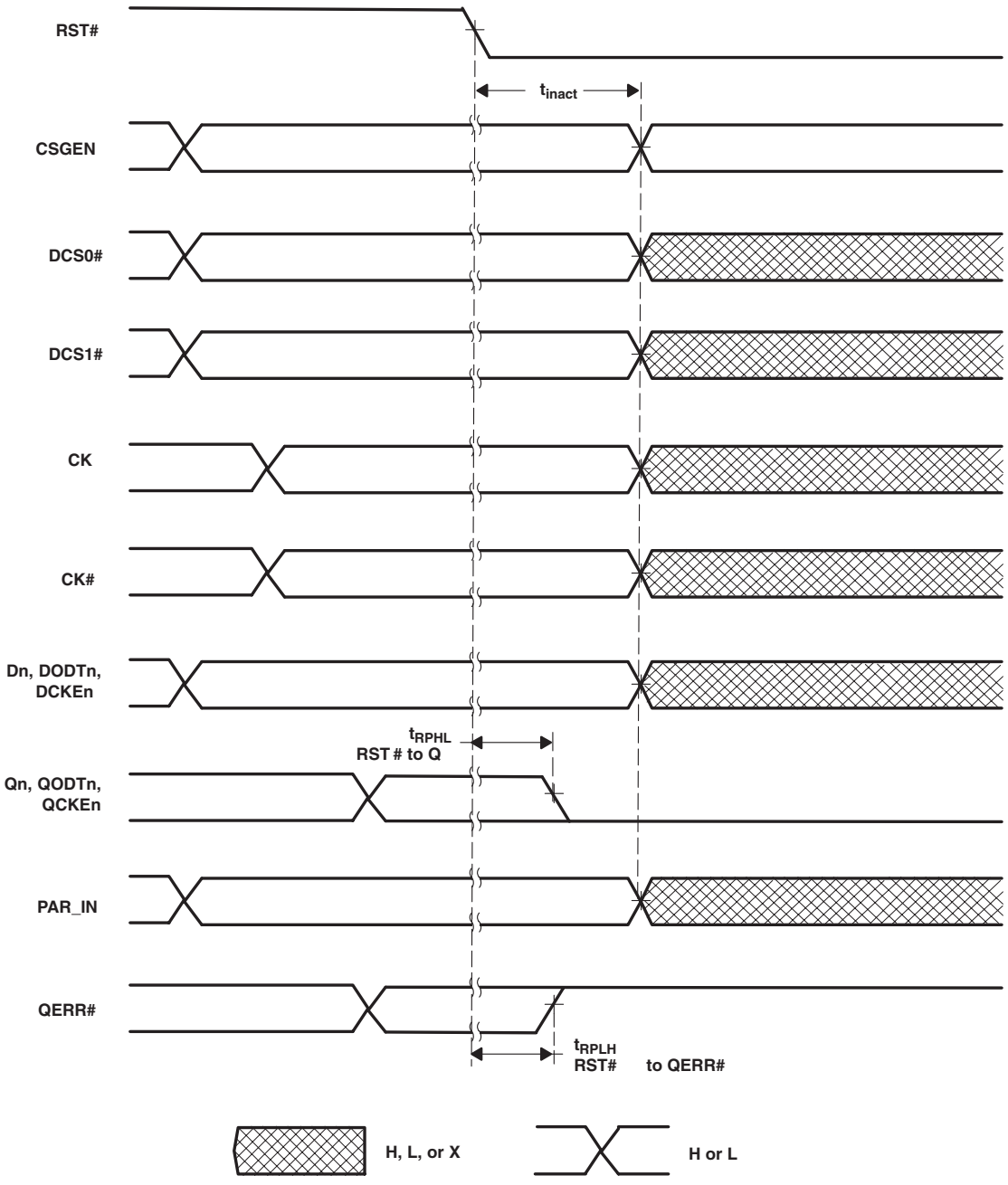
Register Timing



† If the data is clocked in on the n clock pulse, the QERR# output signal will be generated on the n + 2 clock pulse and it will be valid on the n + 3 clock pulse. If an error occurs and the QERR# output is driven low, it stays low for a minimum of two clock cycles or until RST# is driven low.

08/14/06

Register Timing



† After RST# is switched from high to low, all data and clock input signals must be held at valid logic levels (not floating) for a minimum time of t_{inact} max.

08/14/06

Absolute Maximum Ratings

Storage Temperature	–65°C to +150°C
Supply Voltage	-0.5 to 2.5V
Input Voltage[1]	-0.5 to VDD + 2.5V
Output Voltage[1,2]	-0.5 to VDDQ + 0.5
Input Clamp Current	±50 mA
Output Clamp Current	±50mA
Continuous Output Current	±50mA
VDDQ or GND Current/Pin	±100mA
Package Thermal Impedance[3]	36°C

Notes:
1. The input and output negative voltage ratings may be excluded if the input and output clamp ratings are observed.
2. This current will flow only when the output is in the high state level $V_O > V_{DDQ}$.
3. The package thermal impedance is calculated in accordance with JESD 51.

Stresses above those listed under *Absolute Maximum Ratings* may cause permanent damage to the device. These ratings are stress specifications only and functional operation of the device at these or any other conditions above those listed in the operational sections of the specifications is not implied. Exposure to absolute maximum rating conditions for extended periods may affect product reliability.

Recommended Operating Conditions

PARAMETER	DESCRIPTION		MIN	TYP	MAX	UNITS
V_{DD}	I/O Supply Voltage		1.7	1.8	1.9	V
V_{REF}	Reference Voltage		0.49 x V_{DD}	0.5 x V_{DD}	0.51 x V_{DD}	
V_{TT}	Termination Voltage		V_{REF} - 0.04	V_{REF}	V_{REF} + 0.04	
V_I	Input Voltage		0		V_{DD}	
$V_{IH\ (DC)}$	DC Input High Voltage	Data CSR#, and PAR_IN inputs	V_{REF} + 0.125			
$V_{IH\ (AC)}$	AC Input High Voltage		V_{REF} + 0.250			
$V_{IL\ (DC)}$	DC Input Low Voltage				V_{REF} - 0.125	
$V_{IL\ (DC)}$	AC Input Low Voltage				V_{REF} - 0.250	
V_{IH}	Input High Voltage Level	RESET#, C0, C1	0.65 x V_{DDQ}			
V_{IL}	Input Low Voltage Level				0.35 x V_{DDQ}	
V_{ICR}	Common mode Input Range	CLK, CLK#	0.675		1.125	
V_{ID}	Differential Input Voltage		0.600			
I_{OH}	High-Level Output Current				-16	mA
I_{OL}	Low-Level Output Current				16	
T_A	Operating Free-Air Temperature		0		70	°C

[1]Guaranteed by design, not 100% tested in production.

Note: Reset# and Cn inputs must be helf at valid logic levels (not floating) to ensure proper device operation. The differential inputs must not be floating unless Reset# is low.

Electrical Characteristics - DC

T_A = 0 - 70°C; V_{DD} = 2.5 +/-0.2V, V_{DDQ}=2.5 +/-0.2V; (unless otherwise stated)

SYMBOL	PARAMETERS	CONDITIONS		V_{DDQ}	MIN	TYP	MAX	UNITS
V_{OH}	Output HIGH voltage	I_{OH} = -16mA		1.7V	1.2			V
V_{OL}	Output LOW voltage						0.2	
		I_{OL} = 16mA		1.7V			0.5	
I_I	All Inputs	$V_I = V_{DD}$ or GND		1.9V			±5	µA
I_{DD}	Standby (Static)	RESET# = GND	I_O = 0	1.9V			200	µA
	Operating (Static)	$V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, RESET# = V_{DD}					80	mA
I_{DDD}	Dynamic operating (clock only)	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK# switching 50% duty cycle.	I_O = 0	1.8V		175		µ/clock MHz
I_{DDD}	Dynamic Operating (per each data input) 1:2 mode	RESET# = V_{DD}, $V_I = V_{IH(AC)}$ or $V_{IL(AC)}$, CLK and CLK# switching 50% duty cycle. One data input switching at half clock frequency, 50% duty cycle	I_O = 0	1.8V		200		µA/ clock MHz/data
C_i	Input capacitance, D_n, CSGEN, PAR_IN inputs	$V_I = V_{REF}$ ± 250 mV		1.8V	2.5		4	pF
	Input capacitance, DCS#$_n$[2]	$V_I = V_{REF}$ ± 250 mV	Single-die		2.5		4	pF
	Input capacitance, CK and CK# inputs[2]	V_{ICR} = 0.9V; $V_{I(PP)}$ = 600 mV	Single-die		2		3	pF
	Input capacitance, RESET# input	$V_I = V_{DD}$ or GND			Note 3		Note 3	pF

Notes:

1 - Guaranteed by design, not 100% tested in production.

2 - The vendor must choose to comply with either single-die or dual-die specification in accordance to the device implementatic

3 - The vendor must supply this value for full device description.

Output Buffer Characteristics

Output edge rates over recommended operating free-air temperature range (See figure 7)

PARAMETER	V_{DD} = 1.8V ± 0.1V		UNIT
	MIN	MAX	
dV/dt_r	1	4	V/ns
dV/dt_f	1	4	V/ns
dV/dt_Δ[1]	-	1	V/ns

1. Difference between dV/dt_r (rising edge rate) and dV/dt_f (falling edge rate)

Timing Requirements

(over recommended operating free-air temperature range, unless otherwise noted)

Symbol	Parameter		Min	Max	Unit
f_{clock}	Clock frequency		-	410	MHz
t_W	Pulse duration, CK, CK# HIGH or LOW		1	-	ns
t_{ACT}	Differential inputs active time (See Notes 1 and 2)		-	10	ns
t_{INACT}	Differential inputs inactive time (See Notes 1 and 3)		-	15	ns
t_{SU}	Setup time	DCS before CK↑, CK#↓, CSR# high; CSR# before CK↑, CK#↓, DCS# high	0.7	-	ns
	Setup time	DCS# before CK↑, CK#↓, CSR# low	0.5	-	ns
	Setup time	DODT, DCKE and data before CK↑, CK#↓	0.5	-	ns
	Setup time	PAR_IN before CK↑, CK#↓	0.5	-	ns
t_H	Hold time	DCS#, DODT, DCKE and data after CK↑, CK#↓	0.6	-	ns
	Hold time	PAR_IN after CK↑, CK#↓	0.5	-	ns

NOTE 1 This parameter is not necessarily production tested.

NOTE 2 V_{REF} must be held at a valid input voltage level and data inputs must be held low for a minimum time of t_{ACT} (max) after RESET# is taken high.

NOTE 3 V_{REF}, Data and clock inputs must be held at valid voltage levels (not floating) a minimum time of t_{INACT} (max) after RESET# is taken low.

Switching Characteristics

(over recommended operating free-air temperature range, unless otherwise noted)

Symbol	Parameter	Measurement Conditions	MIN	MAX	Units
fmax	Max input clock frequency		410		MHz
t_{PDM}	Propagation delay, single bit switching	CK↑ to CK#↓ Qn	1.2	1.9	ns
t_{LH}	Low to High propagation delay	CK↑ to CK#↓ to QERR#	1.2	3	ns
t_{HL}	High to low propagation delay	CK↑ to CK#↓ to QERR#	1	2.4	ns
t_{PDMSS}	Propagation delay simultaneous switching	CK↑ to CK#↓ Qn		2	ns
t_{PHL}	High to low propagation delay	Reset# ↓ to Qn↓		3	ns
t_{PLH}	Low to High propagation delay	Reset# ↓ to QERR#↑		3	ns

1. Guaranteed by design, not 100% tested in production.

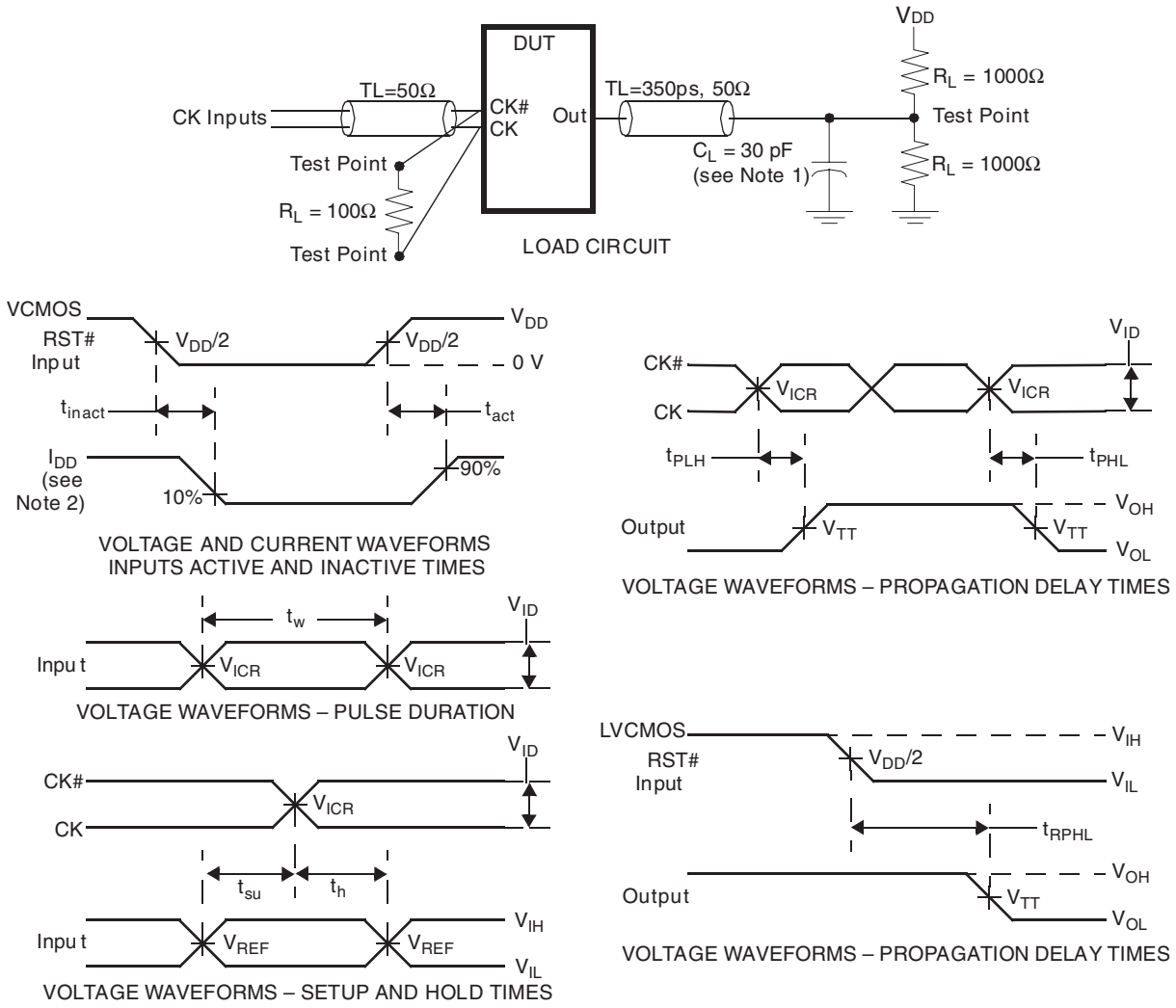


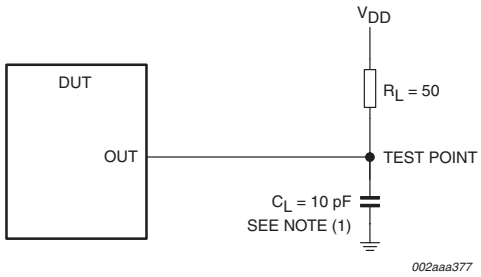
Figure 6— Parameter Measurement Information (V_{DD} = 1.8 V ±0.1 V)

Notes: 1. C_L incluces probe and jig capacitance.

2. I_{DD} tested with clock and data inputs held at V_{DD} or GND, and Io = 0mA.
3. All input pulses are supplied by generators having the following chareacteristics: PRR ≤10 MHz, Zo=50Ω, input slew rate = 1 V/ns ±20% (unless otherwise specified).
4. The outputs are measured one at a time with one transition per measurement.
5. $V_{REF} = V_{DD}/2$
6. $V_{IH} = V_{REF}$ + 250 mV (ac voltage levels) for differential inputs. $V_{IH} = V_{DD}$ for LVCMOS input.
7. $V_{IL} = V_{REF}$ - 250 mV (ac voltage levels) for differential inputs. V_{IL} = GND for LVCMOS input.
8. V_{ID} = 600 mV
9. t_{PLH} and t_{PHL} are the same as t_{PDM}.

Output slew rate measurement information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR 10 MHz; Z_o = 50 ; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 12 — Load circuit, HIGH-to-LOW slew measurement

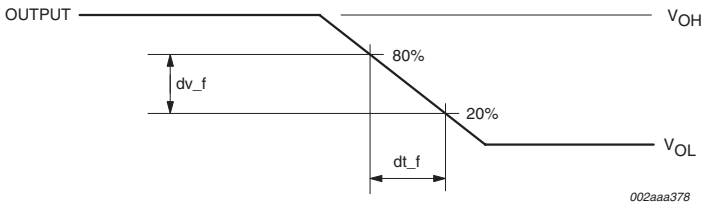
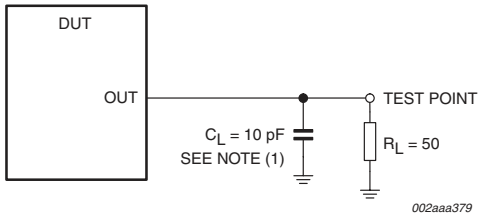


Figure 13 — Voltage waveforms, HIGH-to-LOW slew rate measurement



(1) C_L includes probe and jig capacitance.

Figure 14 — Load circuit, LOW-to-HIGH slew measurement

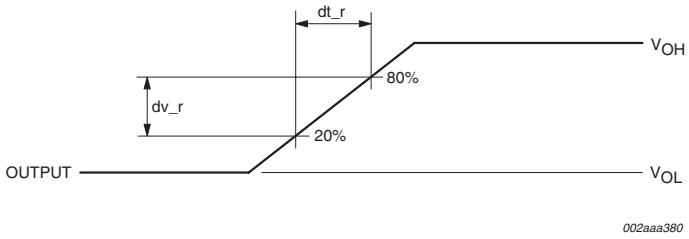
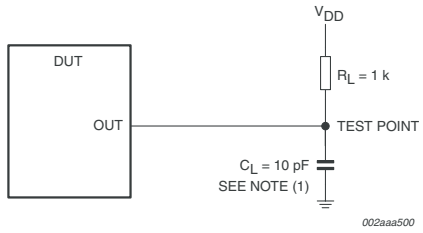


Figure 15 — Voltage waveforms, LOW-to-HIGH slew rate measurement

08/14/06

Error output load circuit and voltage measurement information (V_{DD} = 1.8 V ± 0.1 V)

All input pulses are supplied by generators having the following characteristics: PRR 10 MHz; Z_o = 50 ; input slew rate = 1 V/ns ± 20%, unless otherwise specified.



(1) C_L includes probe and jig capacitance.

Figure 16 — Load circuit, error output measurements

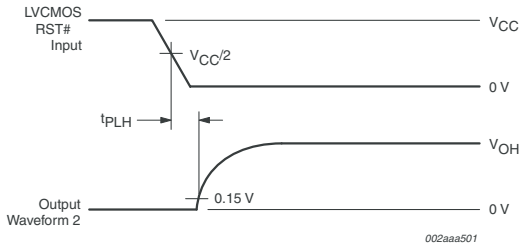


Figure 17 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to RST# input

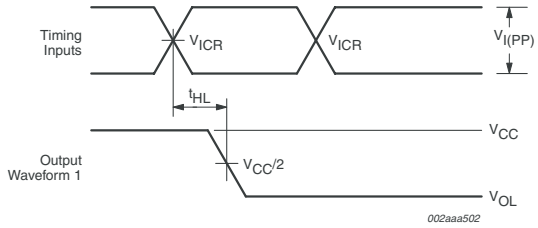


Figure 18 — Voltage waveforms, open-drain output HIGH-to-LOW transition time with respect to clock inputs

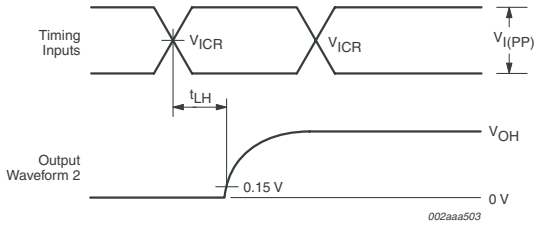
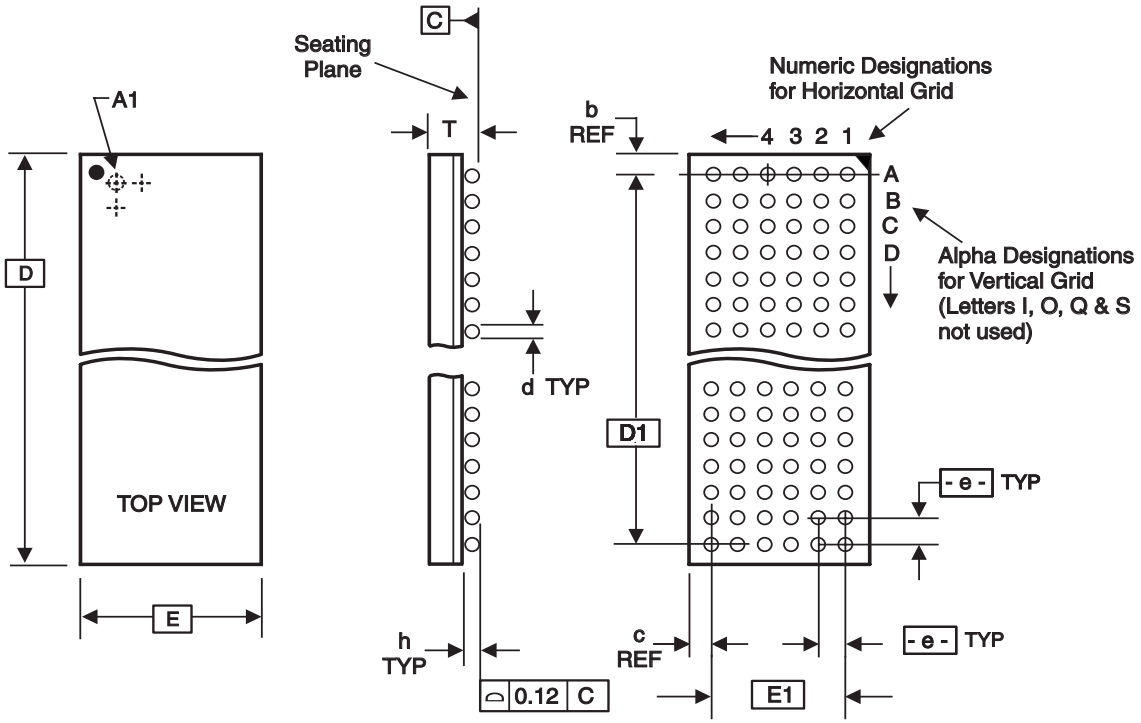


Figure 19 — Voltage waveforms, open-drain output LOW-to-HIGH transition time with respect to clock inputs



ALL DIMENSIONS IN MILLIMETERS

D	E	T Min/Max	e	----- BALL GRID ----- HORIZ	VERT	TOTAL	d Min/Max	h Min/Max	D1	E1	REF. DIMS b	c	
15.00 Bsc	6.00 Bsc	1.00/1.20	0.65 Bsc	8	22	176	0.35/0.45	0.25/0.35	13.65 Bsc	4.55 Bsc	0.675	0.725	***

Note: Ball grid total indicates maximum ball count for package. Lesser quantity may be used.

* Source Ref.: JEDEC Publication 95, MO-205*, MO-225**, MO-246***

10-0055

Ordering Information

ICSSSTUB32S868DH(LF)-

Example:

ICS XXXX y H (LF)- T

- **Designation for tape and reel packaging**
- **Lead Free, RoHS Compliant (Optional)**
- **Package Type**
  H = BGA
- **Revision Designator** (will not correlate with datasheet revision)
- **Device Type**
- **Prefix**
  ICS = Standard Device

08/14/06

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.