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Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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Not recommended
for new design

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**SWITCHING
N-CHANNEL POWER MOS FET
INDUSTRIAL USE**

DESCRIPTION

The μ PA1720 is N-Channel MOS Field Effect Transistor designed for DC / DC Converters and power management application of notebook computers.

FEATURES

- Low On-Resistance
 - $R_{DS(on)1} = 25.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 4.0 \text{ A)}$
 - $R_{DS(on)2} = 33.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 4.0 \text{ A)}$
 - $R_{DS(on)3} = 38.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 4.0 \text{ A)}$
- Low C_{iss} : $C_{iss} = 800 \text{ pF TYP.}$
- Built-in G-S Protection Diode
- Small and Surface Mount Package (Power SOP8)

ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1720G	Power SOP8

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, All terminals are connected.)

Drain to Source Voltage ($V_{GS} = 0$)	V_{DSS}	30	V
Gate to Source Voltage ($V_{DS} = 0$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 8	A
Drain Current (Pulse) ^{Note1}	$I_{D(pulse)}$	± 32	A
Total Power Dissipation (T _A = 25 °C) ^{Note2}	P_T	2.0	W
Single Avalanche Current ^{Note3}	I_{AS}	8.0	A
Single Avalanche Energy ^{Note3}	E_{AS}	6.4	mJ
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

Notes 1. $PW \leq 10 \mu s$, Duty cycle $\leq 1 \%$

2. Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$

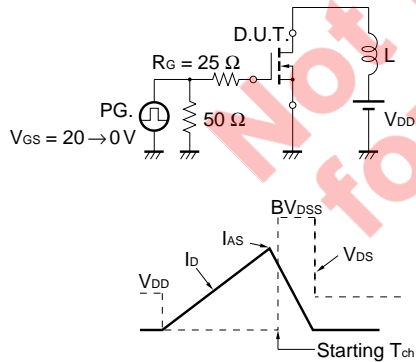
3. Starting $T_{ch} = 25 \text{ °C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

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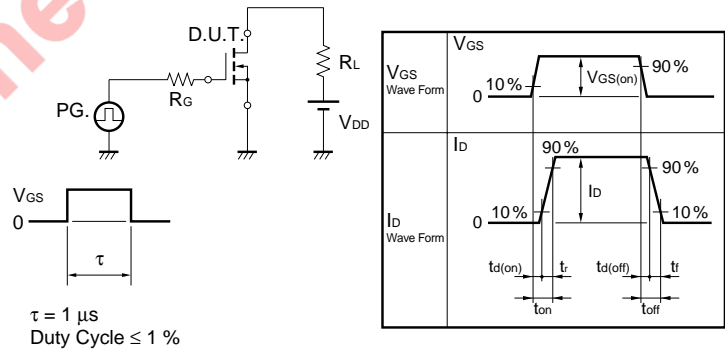
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 4.0 A		20.0	25.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 4.0 A		25.5	33.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 4.0 A		29.0	38.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 4.0 A	3.0	7.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iss}	V _{DS} = 10 V		800		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		250		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		96		pF
Turn-on Delay Time	t _{d(on)}	I _D = 4.0 A		20		ns
Rise Time	t _r	V _{GS(on)} = 10 V		80		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 15 V		40		ns
Fall Time	t _f	R _G = 10 Ω		40		ns
Total Gate Charge	Q _G	I _D = 8 A		14		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 24 V		2.3		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		3.6		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 8 A, V _{GS} = 0 V		0.86		V
Reverse Recovery Time	t _{rr}	I _F = 8 A, V _{GS} = 0 V		30		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		40		nC

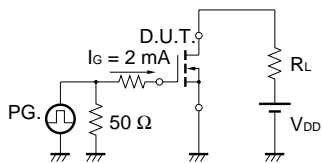
TEST CIRCUIT 1 AVALANCHE CAPABILITY



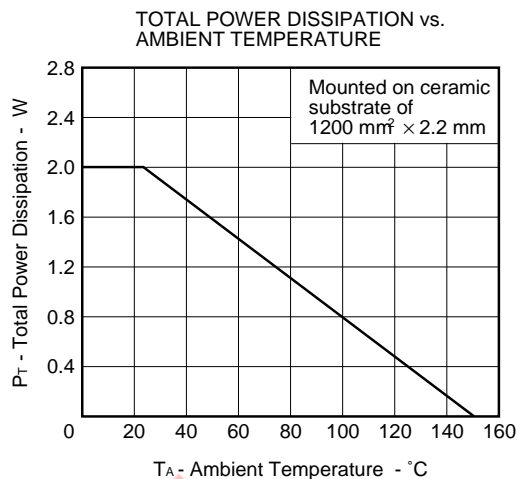
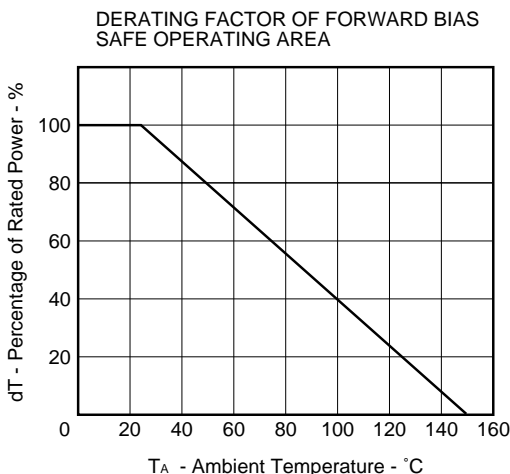
TEST CIRCUIT 2 SWITCHING TIME



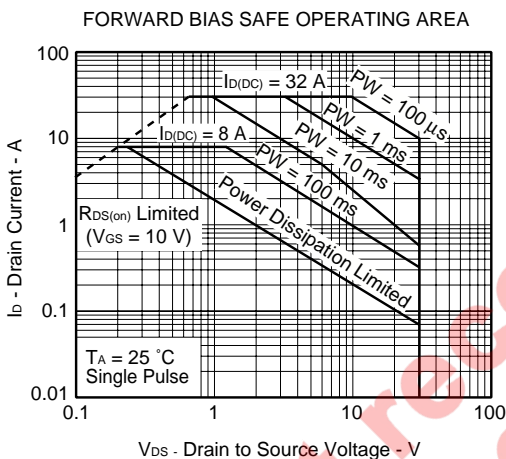
TEST CIRCUIT 3 GATE CHARGE



TYPICAL CHARACTERISTICS (T_A = 25 °C)

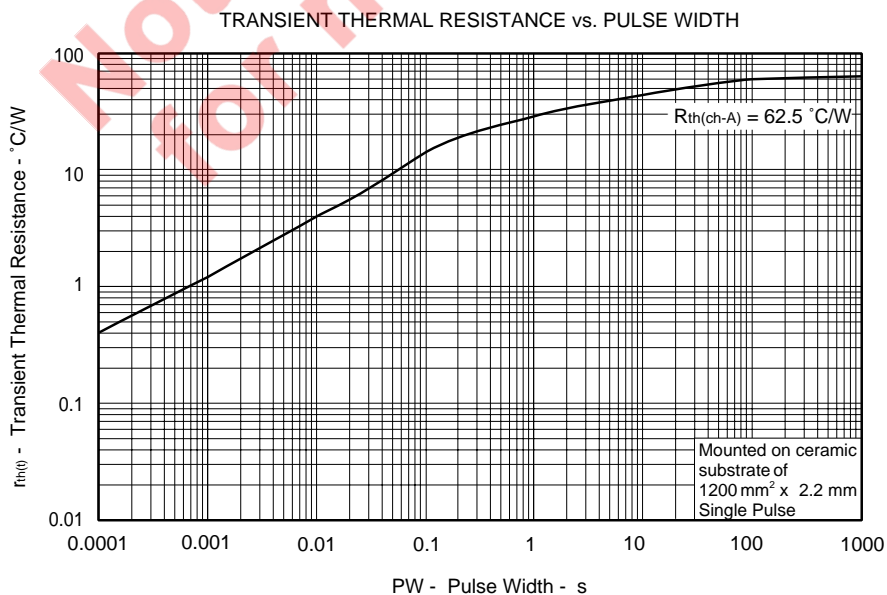


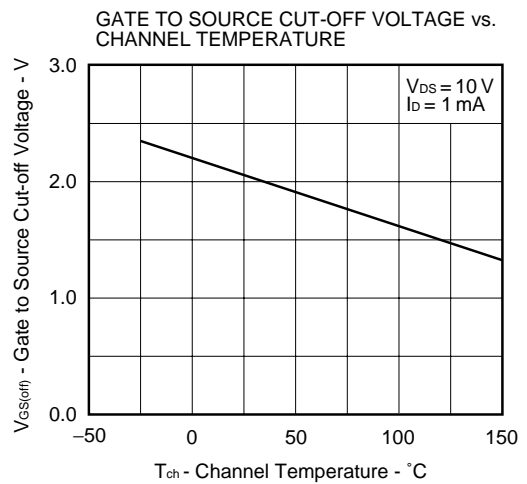
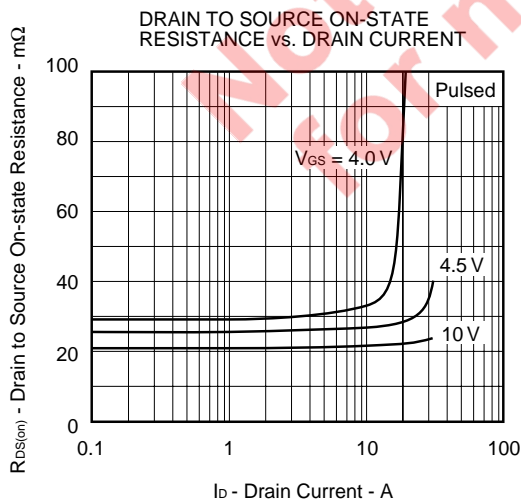
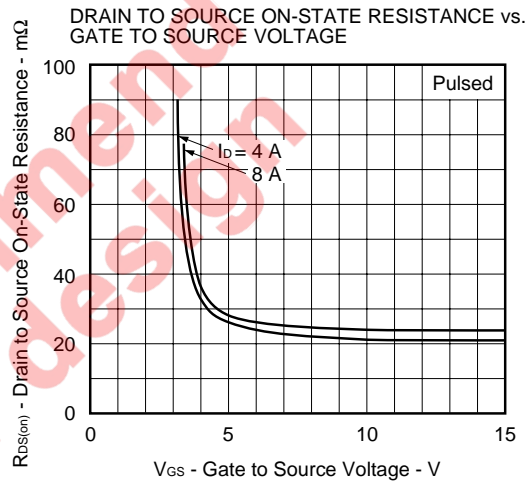
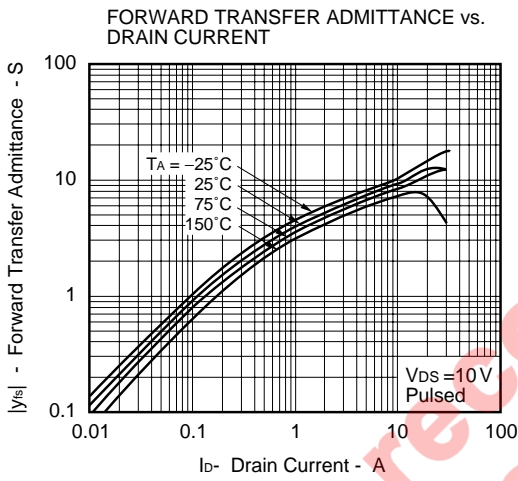
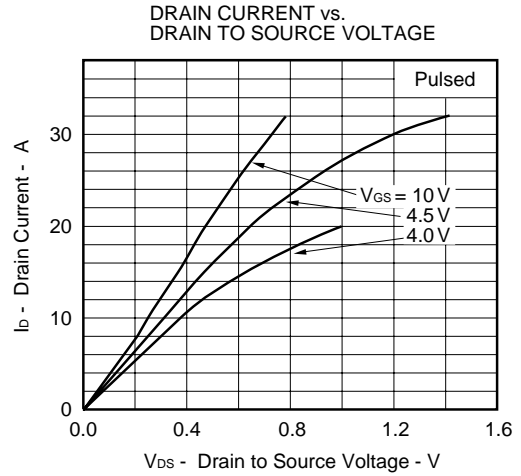
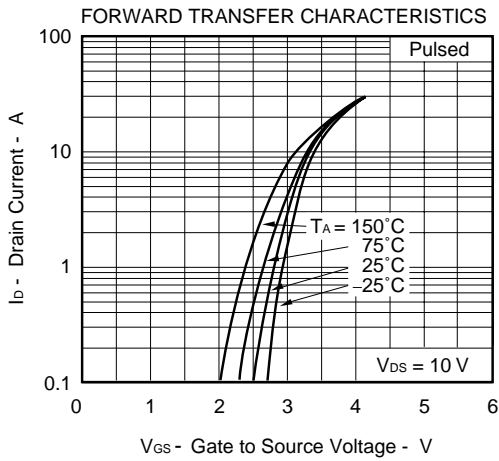
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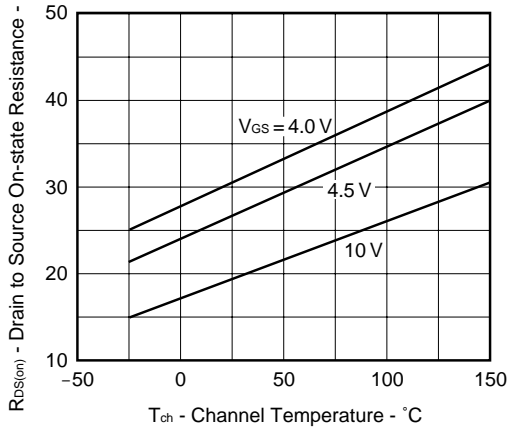
Remark Mounted on ceramic substrate of 1200 mm² × 2.2 mm

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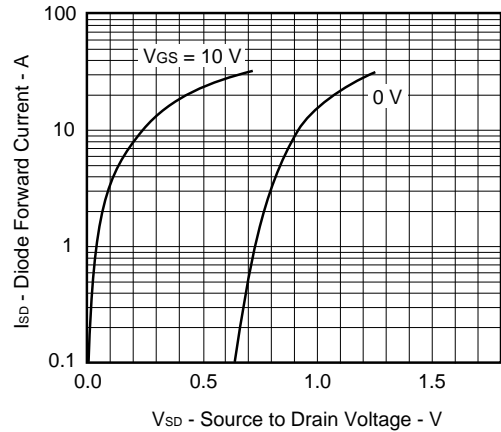




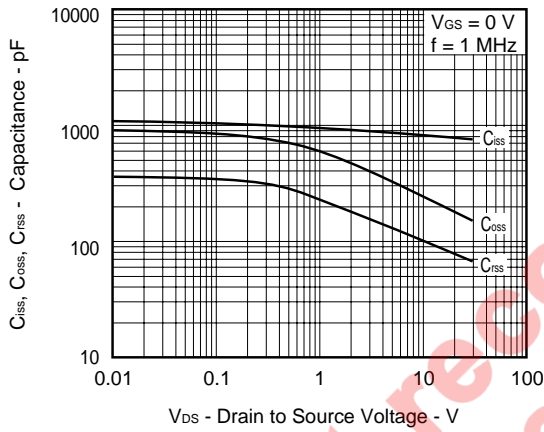
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



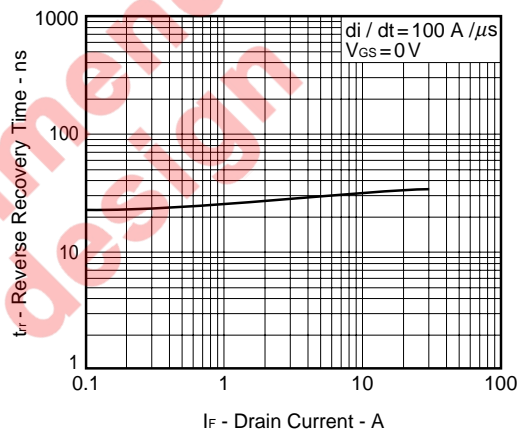
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



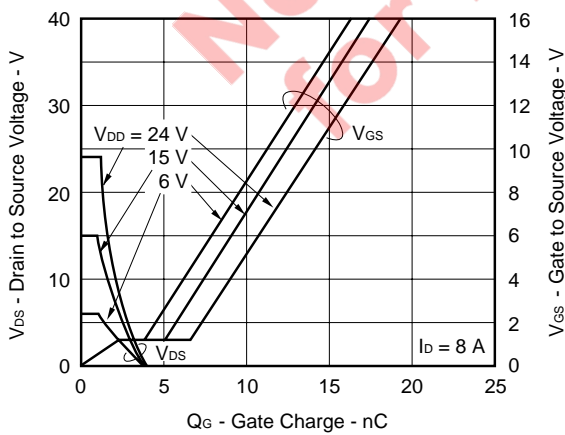
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE

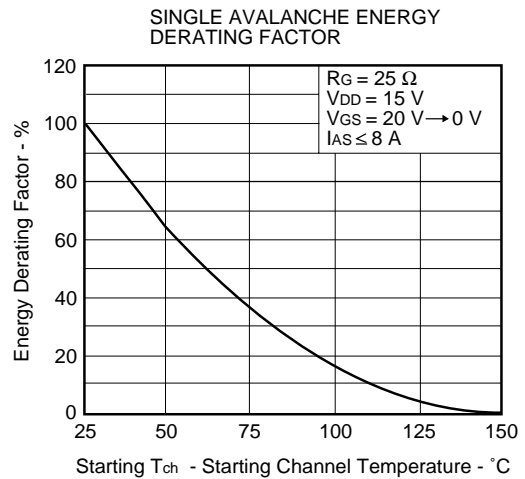
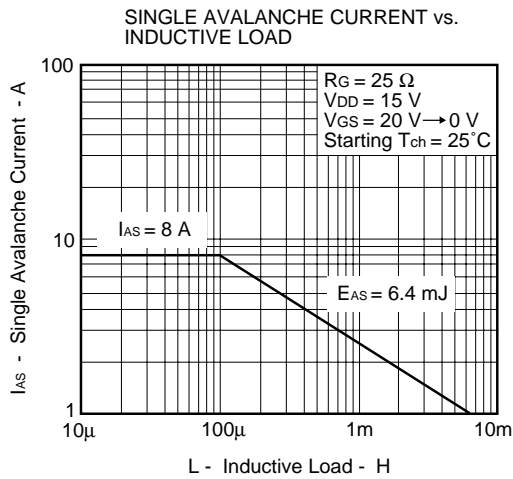


REVERSE RECOVERY TIME vs. DRAIN CURRENT



DYNAMIC INPUT/OUTPUT CHARACTERISTICS

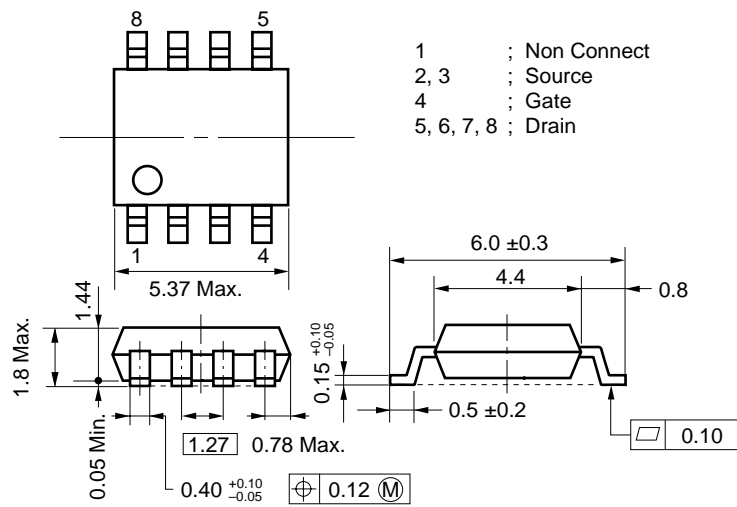




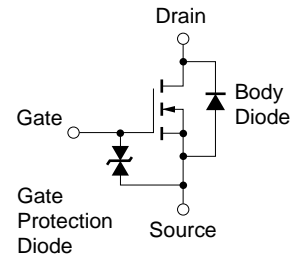
Not recommend
for new design

PACKAGE DRAWING (Unit : mm)

Power SOP8



EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

Not recommend for new design

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