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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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SWITCHING
DUAL N-CHANNEL POWER MOS FET
INDUSTRIAL USE

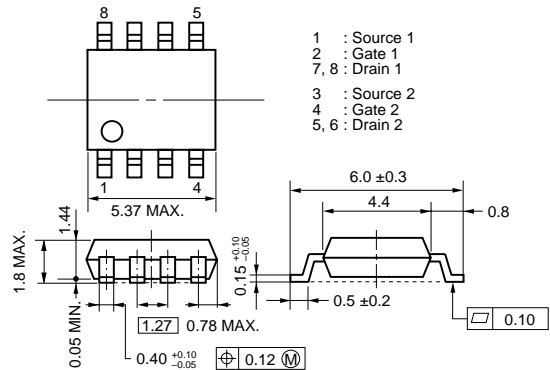
DESCRIPTION

The μ PA1763 is N-Channel MOS Field Effect Transistor designed for DC/DC Converters.

FEATURES

- Dual chip type
- Low on-resistance
 $R_{DS(on)1} = 47.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 2.3 \text{ A)}$
 $R_{DS(on)2} = 57.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 2.3 \text{ A)}$
 $R_{DS(on)3} = 66.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = 4.0 \text{ V, } I_D = 2.3 \text{ A)}$
- Low input capacitance
 $C_{iss} = 870 \text{ pF TYP.}$
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit : mm)



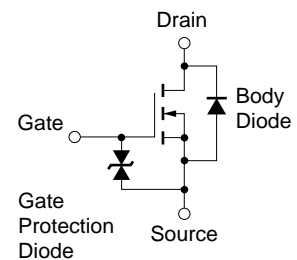
ORDERING INFORMATION

PART NUMBER	PACKAGE
μ PA1763G	Power SOP8

ABSOLUTE MAXIMUM RATINGS ($T_A = 25^\circ\text{C}$, All terminals are connected.)

Drain to Source Voltage	V_{DSS}	60	V
Gate to Source Voltage	V_{GSS}	±20	V
Drain Current (DC)	$I_{D(DC)}$	±4.5	A
Drain Current (pulse) ^{Note1}	$I_{D(pulse)}$	±18	A
Total Power Dissipation (1 unit) ^{Note2}	P_T	1.7	W
Total Power Dissipation (2 unit) ^{Note2}	P_T	2.0	W
Single Avalanche Current ^{Note3}	I_{AS}	4.5	A
Single Avalanche Energy ^{Note3}	E_{AS}	60	mJ
Channel Temperature	T_{ch}	150	°C
Storage Temperature	T_{stg}	-55 to + 150	°C

EQUIVALENT CIRCUIT
(1/2 Circuit)



- Notes**
1. $PW \leq 10 \mu\text{s}$, Duty cycle $\leq 1\%$
 2. $T_A = 25^\circ\text{C}$, Mounted on ceramic substrate of $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
 3. Starting $T_{ch} = 25^\circ\text{C}$, $R_G = 25 \Omega$, $V_{GS} = 20 \text{ V} \rightarrow 0 \text{ V}$

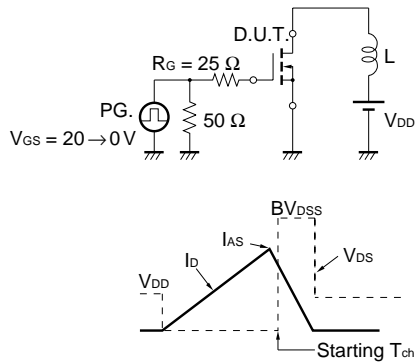
Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage Exceeding the rated voltage may be applied to this device.

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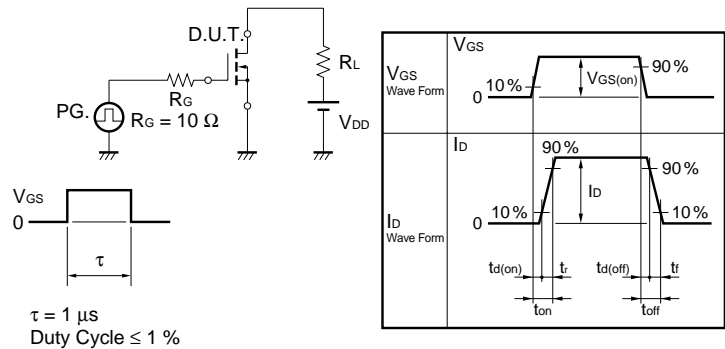
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, All terminals are connected.)

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Drain to Source On-state Resistance	R _{DS(on)1}	V _{GS} = 10 V, I _D = 2.3 A		37.0	47.0	mΩ
	R _{DS(on)2}	V _{GS} = 4.5 V, I _D = 2.3 A		45.0	57.0	mΩ
	R _{DS(on)3}	V _{GS} = 4.0 V, I _D = 2.3 A		49.0	66.0	mΩ
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5	2.0	2.5	V
Forward Transfer Admittance	y _{fs}	V _{DS} = 10 V, I _D = 2.3 A	3.0	6.0		S
Drain Leakage Current	I _{DSS}	V _{DS} = 60 V, V _{GS} = 0 V			10	μA
Gate to Source Leakage Current	I _{GSS}	V _{GS} = ±16 V, V _{DS} = 0 V			±10	μA
Input Capacitance	C _{iSS}	V _{DS} = 10 V		870		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V		150		pF
Reverse Transfer Capacitance	C _{rSS}	f = 1 MHz		80		pF
Turn-on Delay Time	t _{d(on)}	I _D = 2.3 A		11		ns
Rise Time	t _r	V _{GS(on)} = 10 V		40		ns
Turn-off Delay Time	t _{d(off)}	V _{DD} = 30 V		50		ns
Fall Time	t _f	R _G = 10 Ω		12		ns
Total Gate Charge	Q _G	I _D = 4.5 A		20		nC
Gate to Source Charge	Q _{GS}	V _{DD} = 48 V		3		nC
Gate to Drain Charge	Q _{GD}	V _{GS} = 10 V		5		nC
Body Diode Forward Voltage	V _{F(S-D)}	I _F = 4.5 A, V _{GS} = 0 V		0.80		V
Reverse Recovery Time	t _{rr}	I _F = 4.5 A, V _{GS} = 0 V		30		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		40		nC

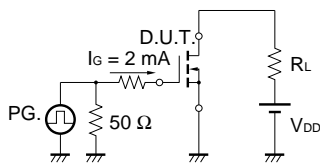
TEST CIRCUIT 1 AVALANCHE CAPABILITY



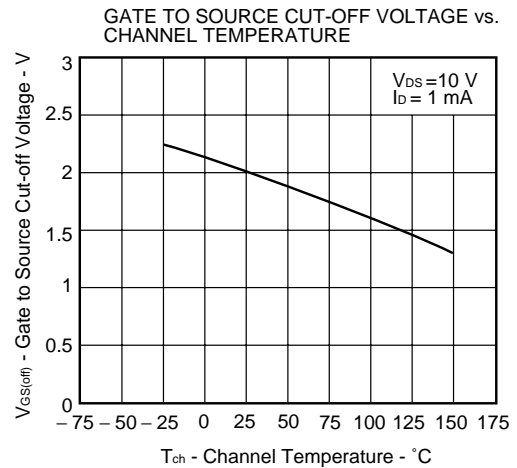
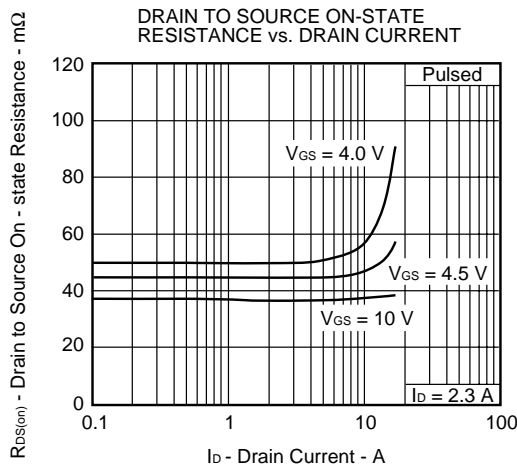
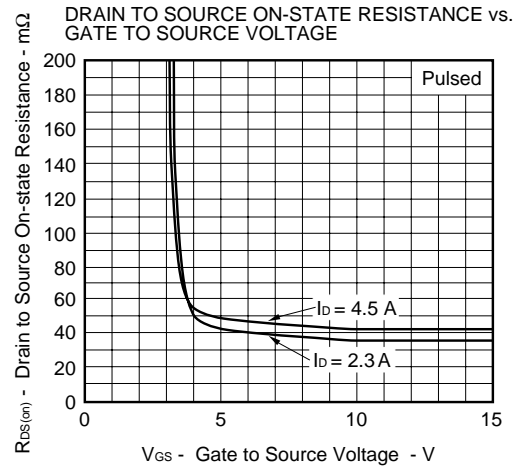
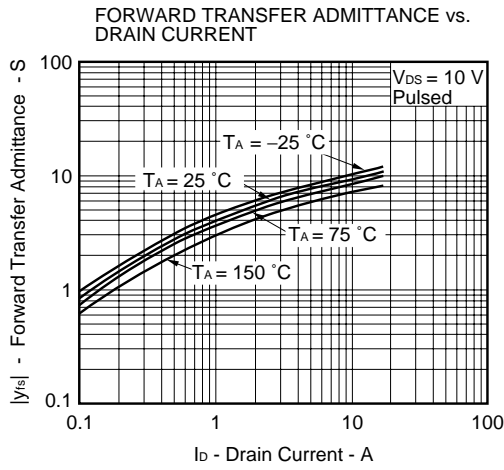
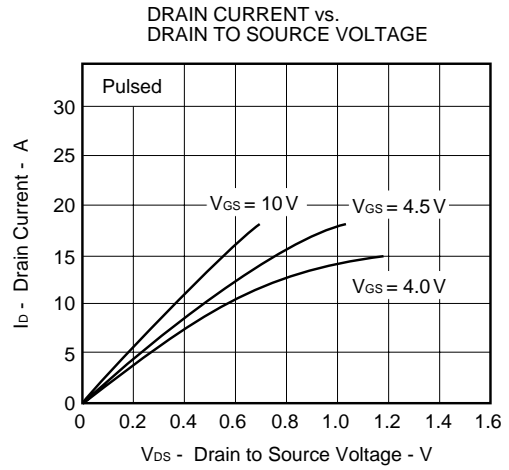
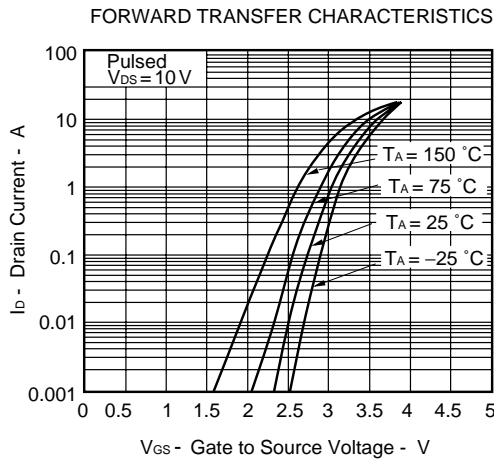
TEST CIRCUIT 2 SWITCHING TIME



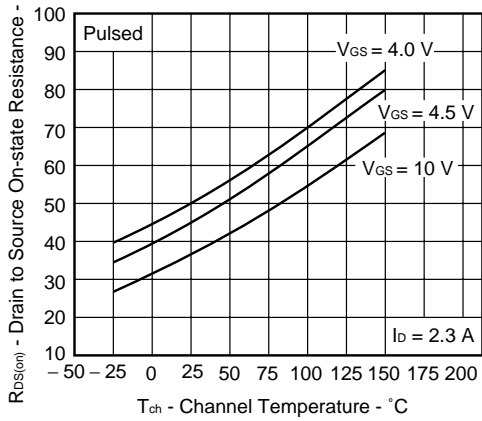
TEST CIRCUIT 3 GATE CHARGE



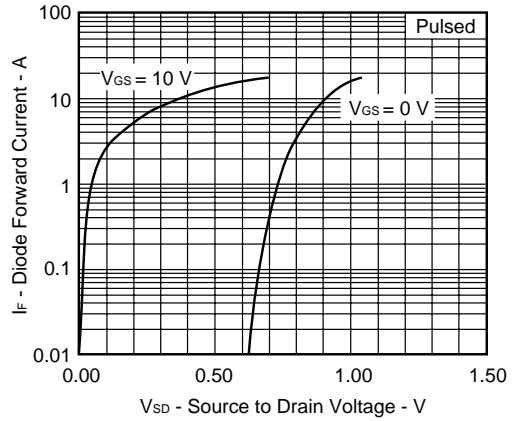
TYPICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)



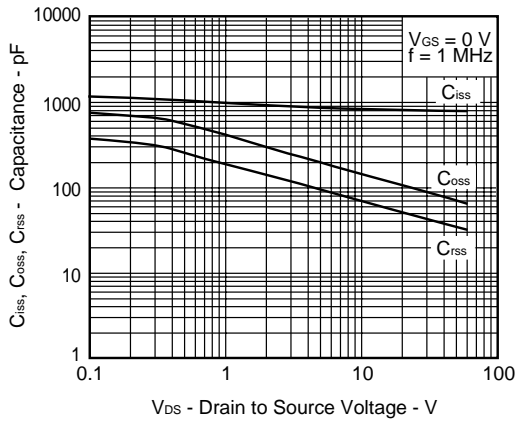
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



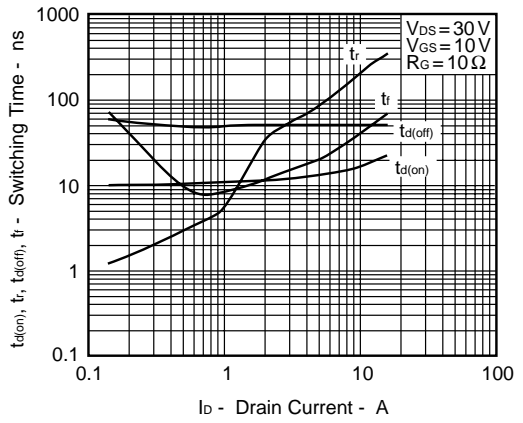
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



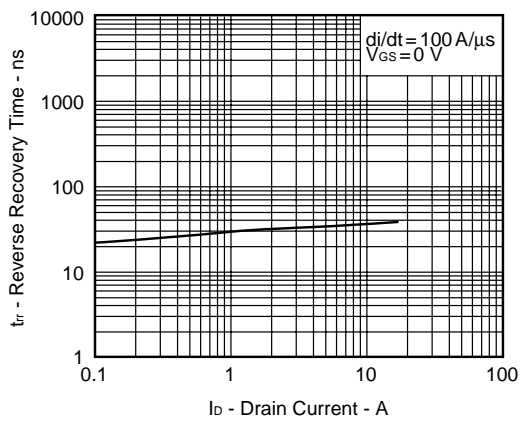
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



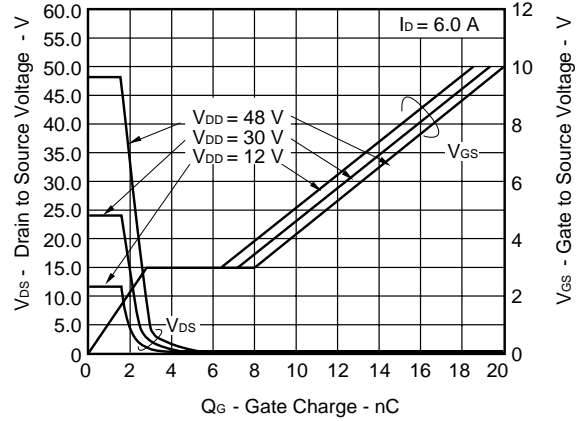
SWITCHING CHARACTERISTICS



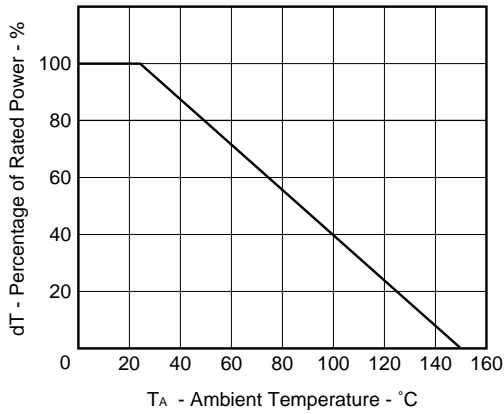
REVERSE RECOVERY TIME vs. DRAIN CURRENT



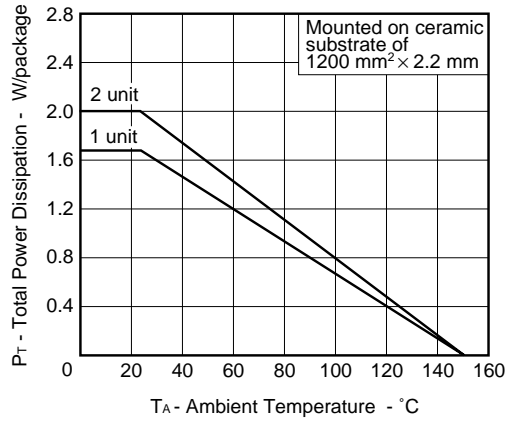
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA

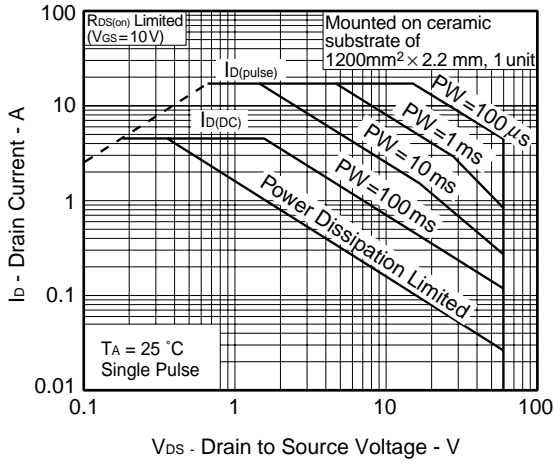


TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



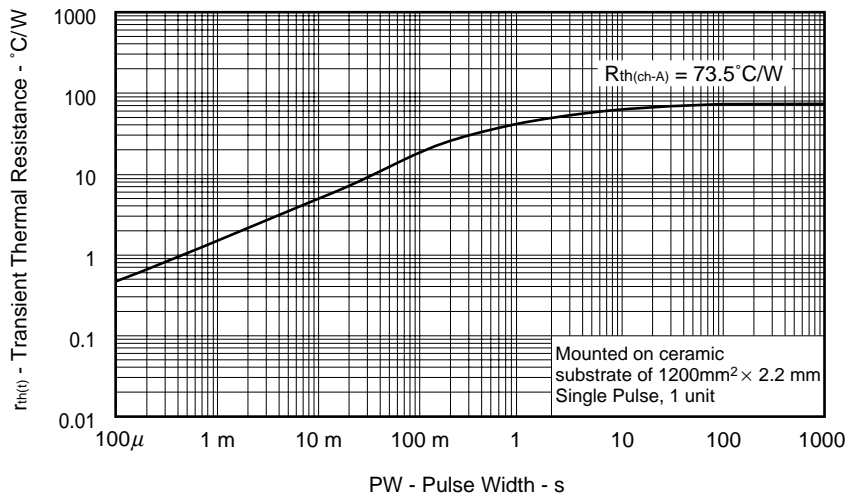
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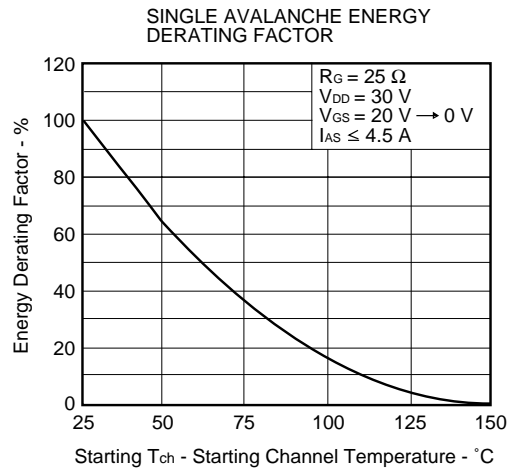
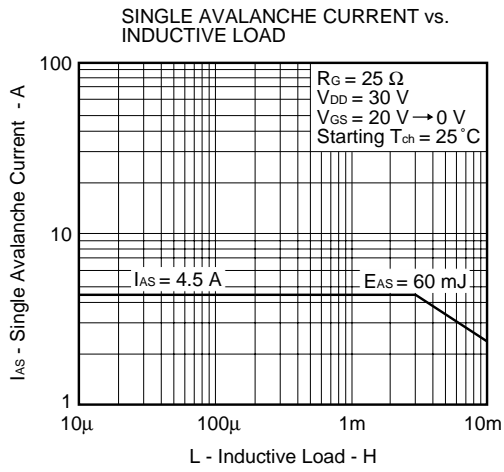
FORWARD BIAS SAFE OPERATING AREA



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TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH





[MEMO]

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