To our customers,

Old Company Name in Catalogs and Other Documents

On April 1st, 2010, NEC Electronics Corporation merged with Renesas Technology Corporation, and Renesas Electronics Corporation took over all the business of both companies. Therefore, although the old company name remains in this document, it is a valid Renesas Electronics document. We appreciate your understanding.

Renesas Electronics website: http://www.renesas.com

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (http://www.renesas.com)

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RENESAS

MOS FIELD EFFECT TRANSISTOR

Phase-out/Discontinued

μPA1790

SWITCHING
N-AND P-CHANNEL POWER MOS FET

DESCRIPTION

The μPA1790 is N-and P-Channel MOS Field Effect Transistor designed for motor driver applications.

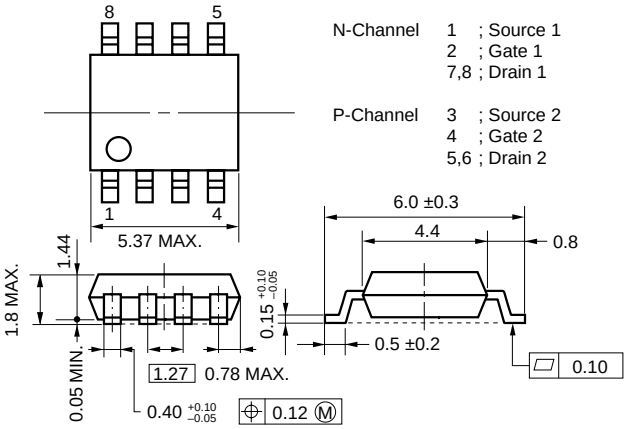
FEATURES

- Dual chip type
- Low on-state resistance
  - N-Channel $R_{DS(on)1}$ = 0.12 Ω TYP. (V_{GS} = 10 V, I_D = 0.5 A)
  - $R_{DS(on)2}$ = 0.19 Ω TYP. (V_{GS} = 4 V, I_D = 0.5 A)
  - P-Channel $R_{DS(on)1}$ = 0.45 Ω TYP. (V_{GS} = –10 V, I_D = –0.35 A)
  - $R_{DS(on)2}$ = 0.74 Ω TYP. (V_{GS} = –4 V, I_D = –0.35 A)
- Low input capacitance
  - N-Channel C_{iss} = 180 pF TYP.
  - P-Channel C_{iss} = 230 pF TYP.
- Built-in G-S protection diode
- Small and surface mount package (Power SOP8)

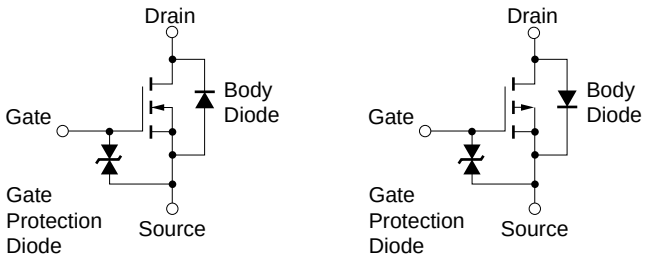
ORDERING INFORMATION

PART NUMBER	PACKAGE
μPA1790G	Power SOP8

PACKAGE DRAWING (Unit: mm)



EQUIVALENT CIRCUIT



Remarks 1. This product is designed for consumer application and isn't suitable for automotive application.

2. The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

Document No. G14320EJ2V0DS00 (2nd edition)
Date Published March 2002 NS CP(K)
Printed in Japan

The mark ★ shows major revised points.

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

	PARAMETER	SYMBOL	N-CHANNEL	P-CHANNEL	UNIT
	Drain to Source Voltage (V_{GS} = 0 V)	V_{DSS}	60	–60	V
	Gate to Source Voltage (V_{DS} = 0 V)	V_{GSS}	±20	∓20	V
	Drain Current (DC)	$I_{D(DC)}$	±1.0	∓0.7	A
	Drain Current (pulse) Note1	$I_{D(pulse)}$	±4.0	∓2.8	A
	Total Power Dissipation (1 unit) Note2	P_T	1.7		W
	Total Power Dissipation (2 unit) Note2	P_T	2.0		W
	Channel Temperature	T_{ch}	150		°C
	Storage Temperature	T_{stg}	–55 to +150		°C
★	Single Avalanche Current Note3	I_{AS}	0.5	–0.35	A
★	Single Avalanche Energy Note3	E_{AS}	0.02	0.01	mJ

Notes 1. PW ≤ 10 μs, Duty Cycle ≤ 1%

2. Mounted on ceramic substrate of 2000 mm^2 x 2.25 mm

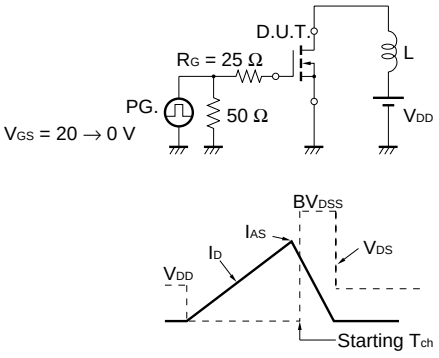
3. Starting T_{ch} = 25°C, V_{DD} = 30 V, R_G = 25 Ω , V_{GS} = 20 → 0 V

ELECTRICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

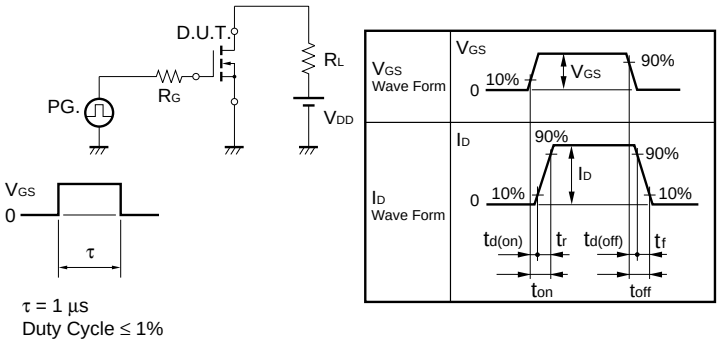
N-CHANNEL

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = 60 V, V_{GS} = 0 V			10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ±16 V, V_{DS} = 0 V			±10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = 10 V, I_D = 1 mA	1.0	1.7	2.5	V
Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = 10 V, I_D = 0.5 A	1.0	1.7		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = 10 V, I_D = 0.5 A		0.12	0.26	Ω
	$R_{DS(on)2}$	V_{GS} = 4 V, I_D = 0.5 A		0.19	0.34	Ω
Input Capacitance	C_{iss}	V_{DS} = 10 V		180		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		100		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		35		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = 30 V, I_D = 0.5 A		1		ns
Rise Time	t_r	V_{GS} = 10 V		1.4		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		23		ns
Fall Time	t_f			17		ns
Total Gate Charge	Q_G	V_{DD} = 48 V		8		nC
Gate to Source Charge	Q_{GS}	V_{GS} = 10 V		1		nC
Gate to Drain Charge	Q_{GD}	I_D = 1.0 A		3.5		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 1.0 A, V_{GS} = 0 V		0.75		V
Reverse Recovery Time	t_{rr}	I_F = 1.0 A, V_{GS} = 0 V		30		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		33		nC

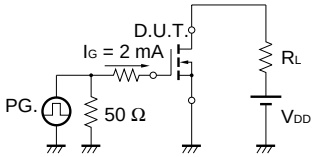
TEST CIRCUIT 1 AVALANCHE CAPABILITY



TEST CIRCUIT 2 SWITCHING TIME



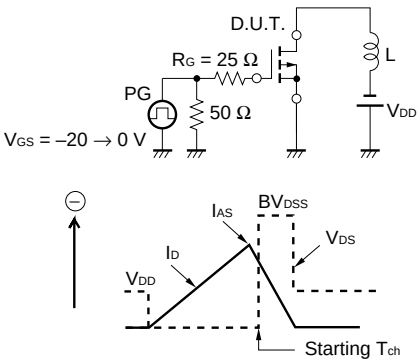
TEST CIRCUIT 3 GATE CHARGE



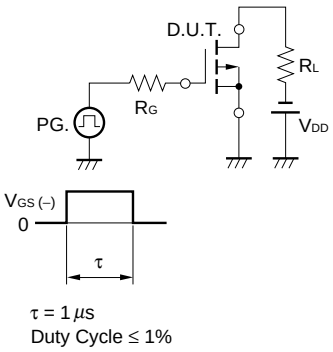
P-CHANNEL

CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	V_{DS} = –60 V, V_{GS} = 0 V			–10	μA
Gate Leakage Current	I_{GSS}	V_{GS} = ∓ 16 V, V_{DS} = 0 V			∓ 10	μA
Gate Cut-off Voltage	$V_{GS(off)}$	V_{DS} = –10 V, I_D = –1 mA	–1.0	–1.7	–2.5	V
★ Forward Transfer Admittance	$\|y_{fs}\|$	V_{DS} = –10 V, I_D = –0.35 A	0.5	0.9		S
Drain to Source On-state Resistance	$R_{DS(on)1}$	V_{GS} = –10 V, I_D = –0.35 A		0.45	0.6	Ω
	$R_{DS(on)2}$	V_{GS} = –4 V, I_D = –0.35 A		0.74	1.1	Ω
Input Capacitance	C_{iss}	V_{DS} = –10 V		230		pF
Output Capacitance	C_{oss}	V_{GS} = 0 V		100		pF
Reverse Transfer Capacitance	C_{rss}	f = 1 MHz		25		pF
Turn-on Delay Time	$t_{d(on)}$	V_{DD} = –30 V, I_D = –0.35 A		1.9		ns
Rise Time	t_r	V_{GS} = –10 V		1.7		ns
Turn-off Delay Time	$t_{d(off)}$	R_G = 10 Ω		30		ns
Fall Time	t_f			15		ns
Total Gate Charge	Q_G	V_{DD} = –48 V		7.6		nC
Gate to Source Charge	Q_{GS}	V_{GS} = –10 V		1		nC
Gate to Drain Charge	Q_{GD}	I_D = –0.7 A		2		nC
Body Diode Forward Voltage	$V_{F(S-D)}$	I_F = 0.7 A, V_{GS} = 0 V		0.85		V
Reverse Recovery Time	t_{rr}	I_F = 0.7 A, V_{GS} = 0 V		58		ns
Reverse Recovery Charge	Q_{rr}	di/dt = 100 A/μs		130		nC

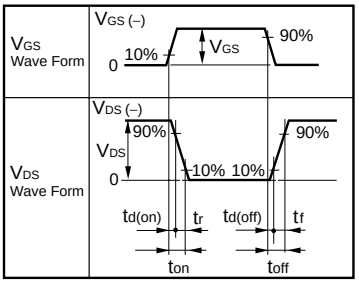
TEST CIRCUIT 1 AVALANCHE CAPABILITY



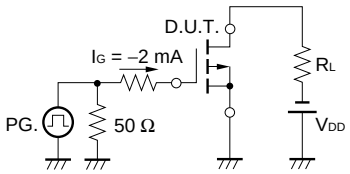
TEST CIRCUIT 2 SWITCHING TIME



τ = 1 μs
Duty Cycle ≤ 1%



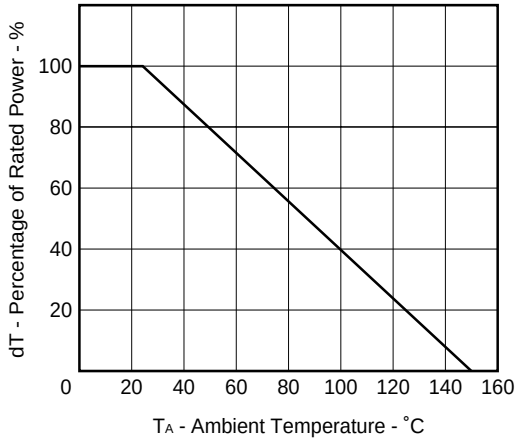
TEST CIRCUIT 3 GATE CHARGE



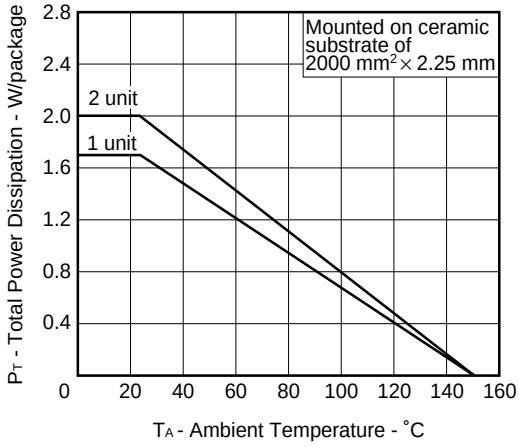
★ TYPICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

N-CHANNEL

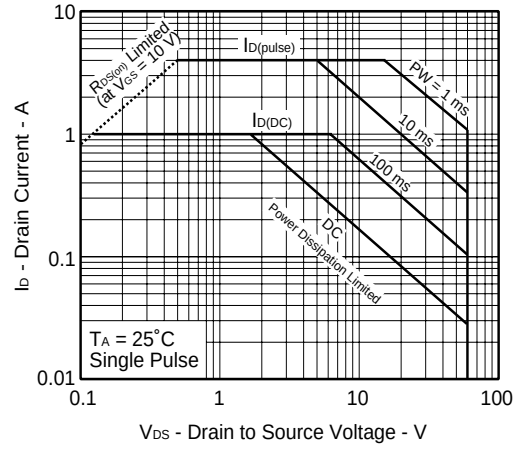
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



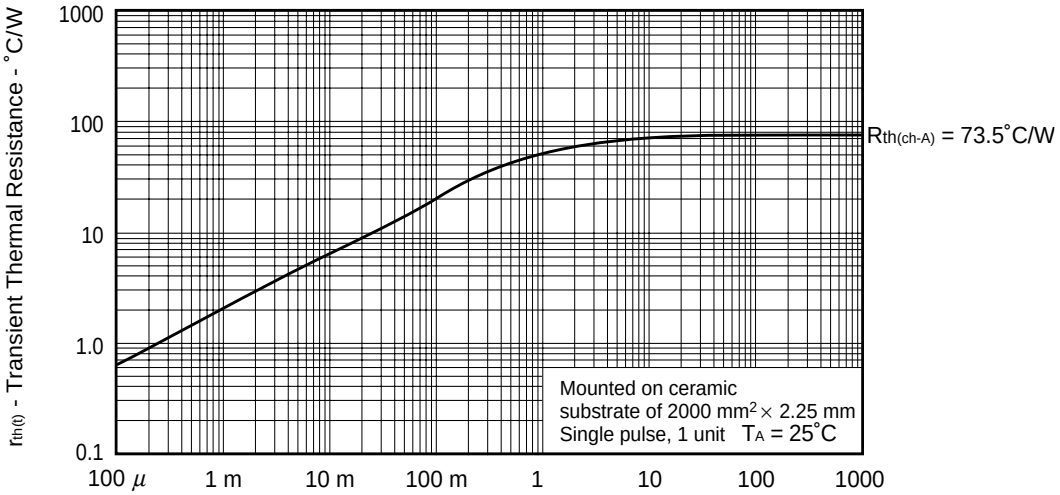
FORWARD BIAS SAFE OPERATING AREA



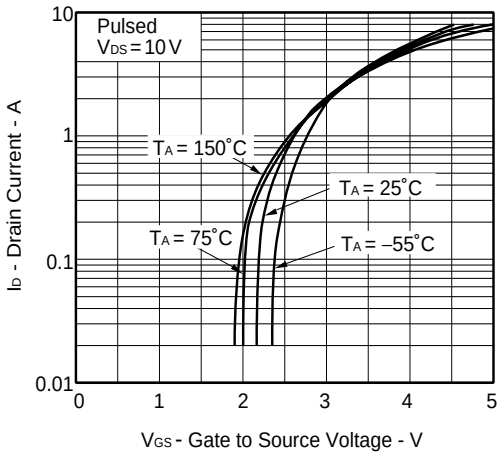
Remark

Mounted on ceramic substrate of 2000 mm^2 × 2.25 mm

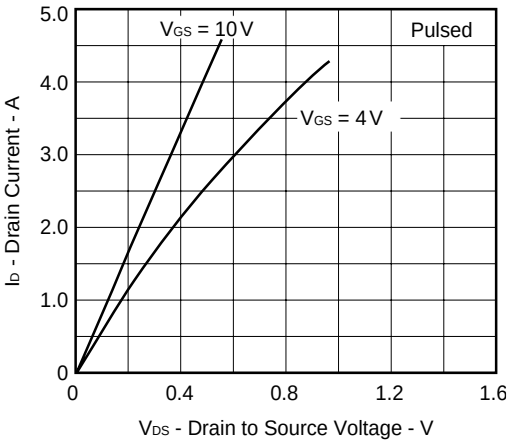
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



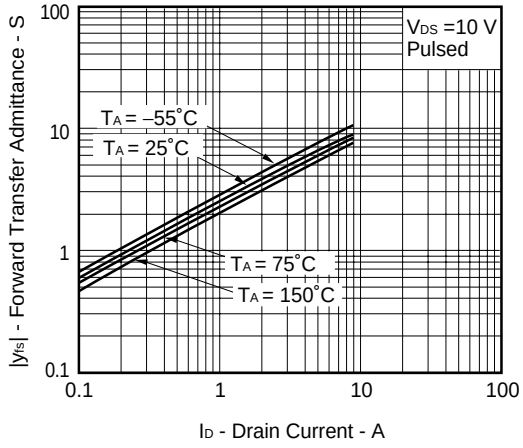
FORWARD TRANSFER CHARACTERISTICS



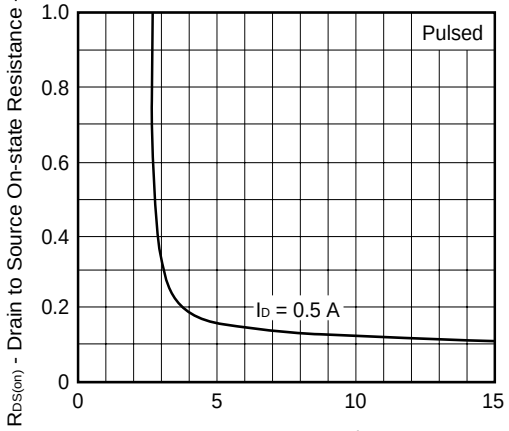
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



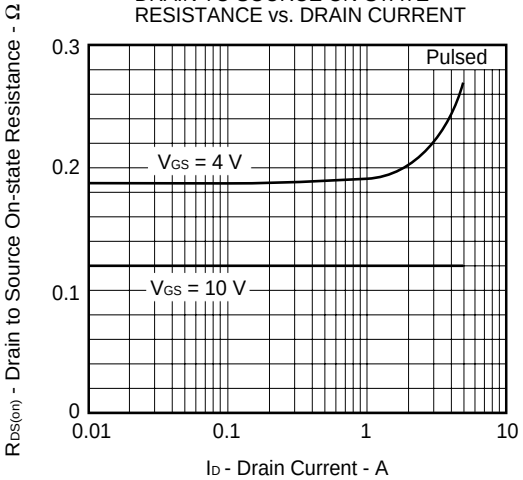
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



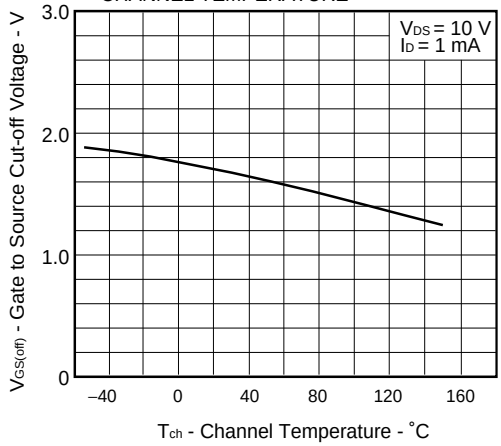
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



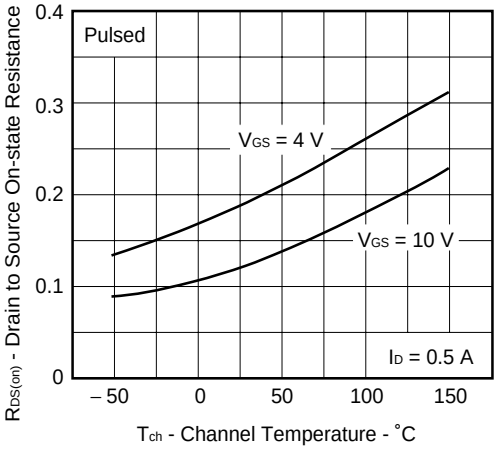
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



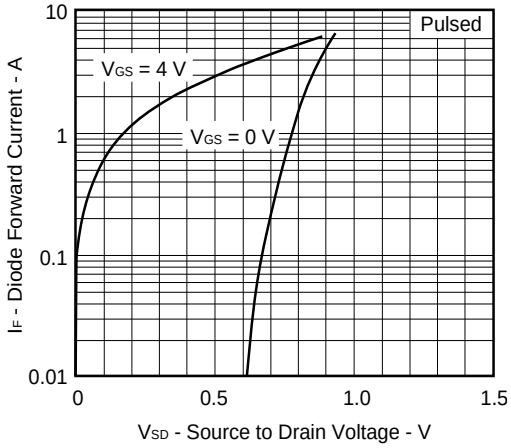
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



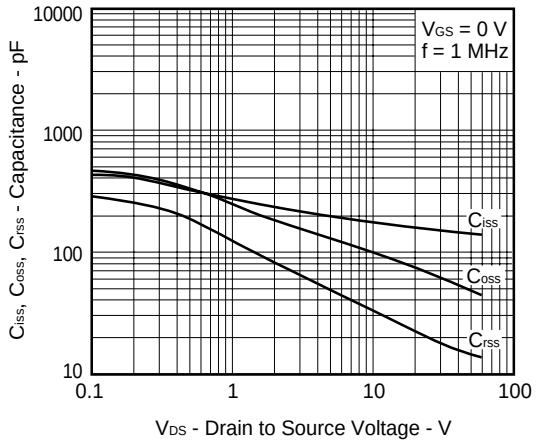
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



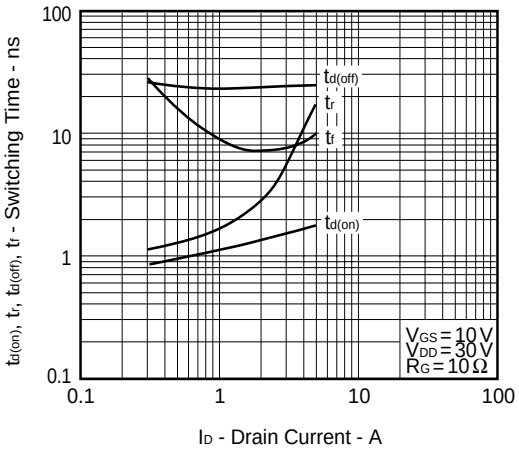
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



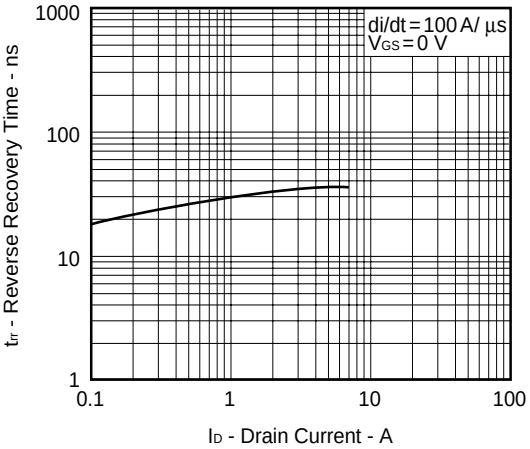
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



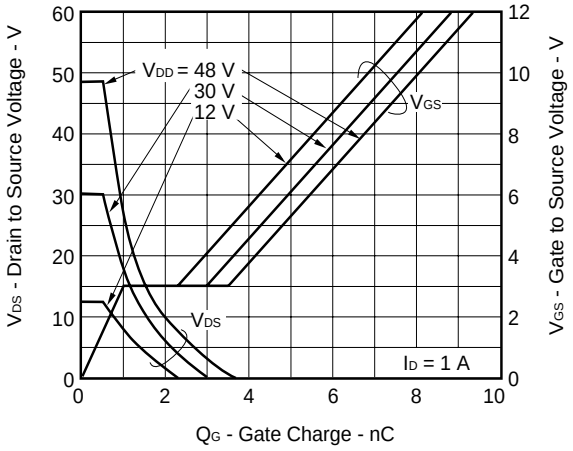
SWITCHING CHARACTERISTICS



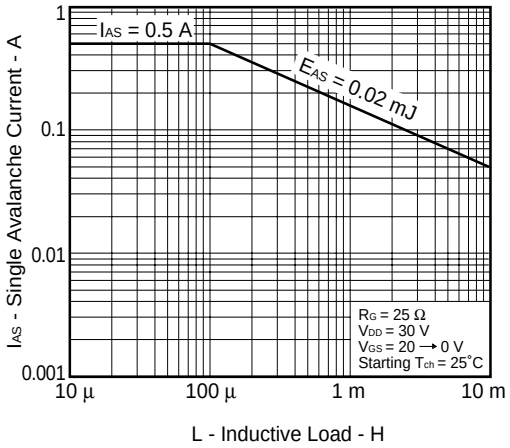
REVERSE RECOVERY TIME vs. DRAIN CURRENT



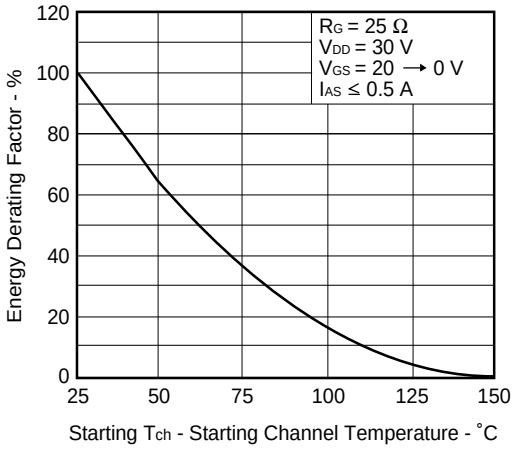
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



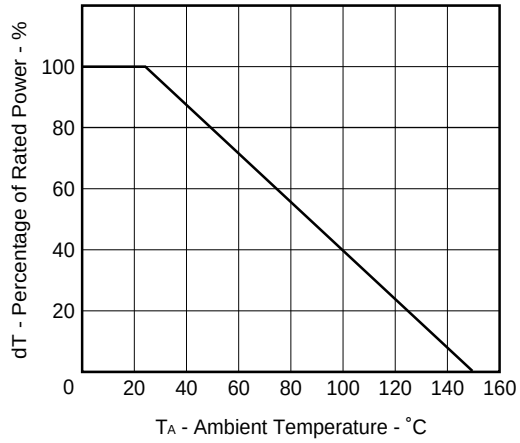
SINGLE AVALANCHE ENERGY
DERATING FACTOR



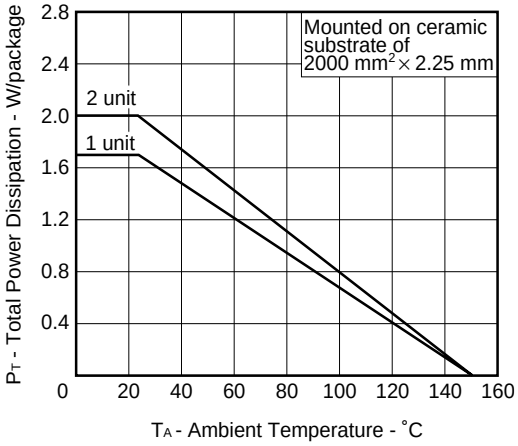
★ TYPICAL CHARACTERISTICS (T_A = 25°C, All terminals are connected.)

P-CHANNEL

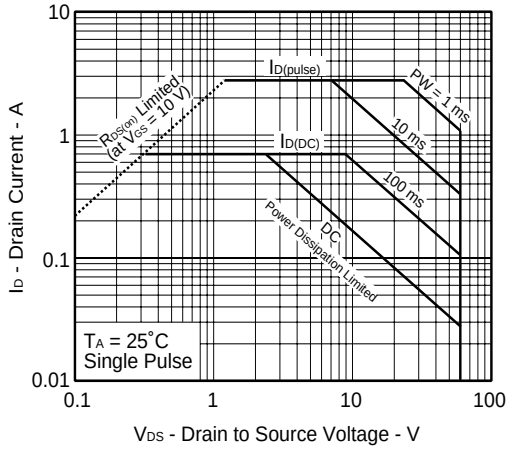
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



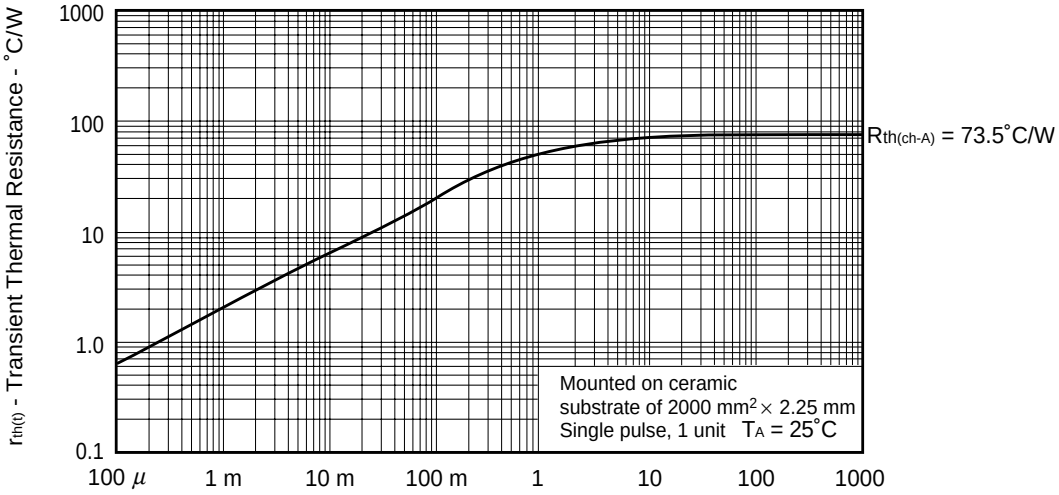
FORWARD BIAS SAFE OPERATING AREA



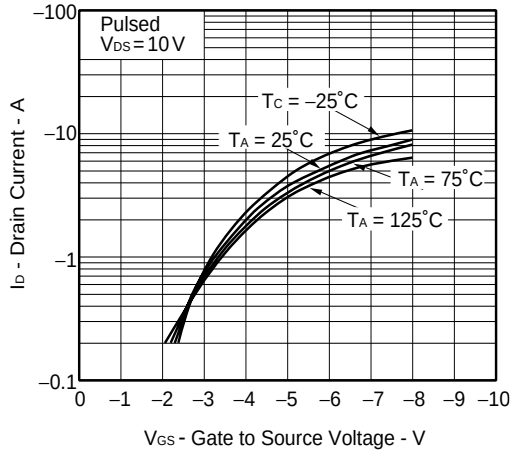
Remark

Mounted on ceramic substrate of 2000 mm^2 × 2.25 mm

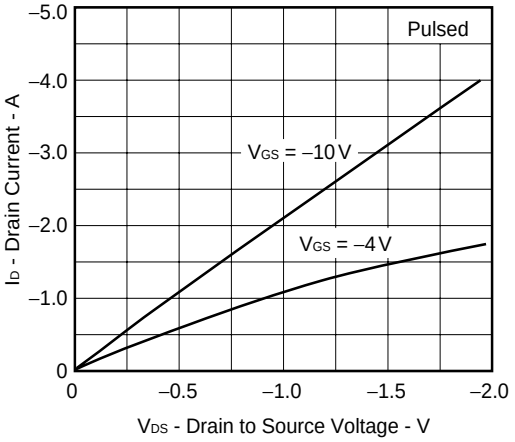
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



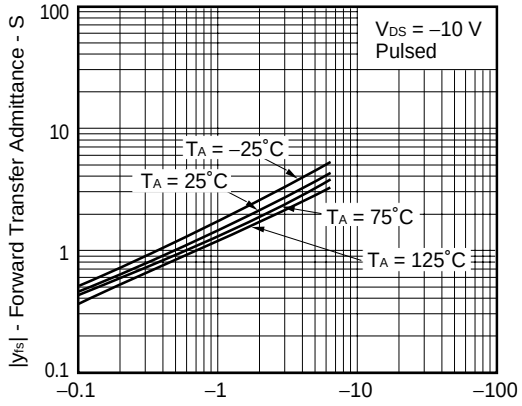
FORWARD TRANSFER CHARACTERISTICS



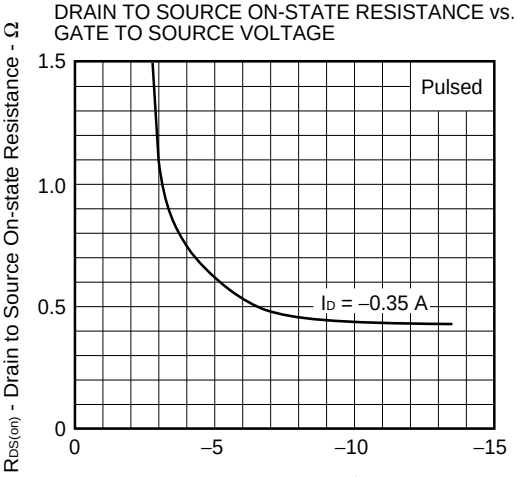
DRAIN CURRENT vs.
DRAIN TO SOURCE VOLTAGE



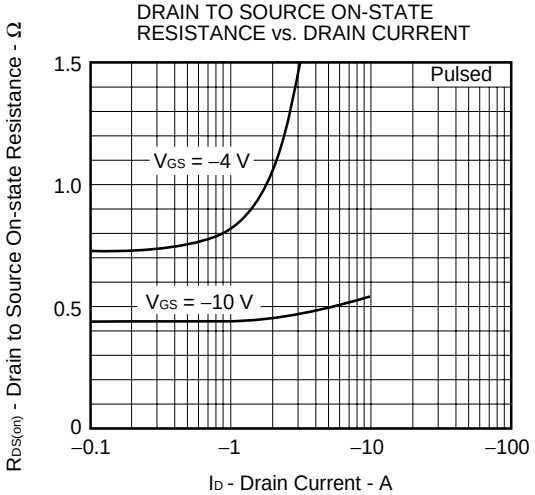
FORWARD TRANSFER ADMITTANCE vs.
DRAIN CURRENT



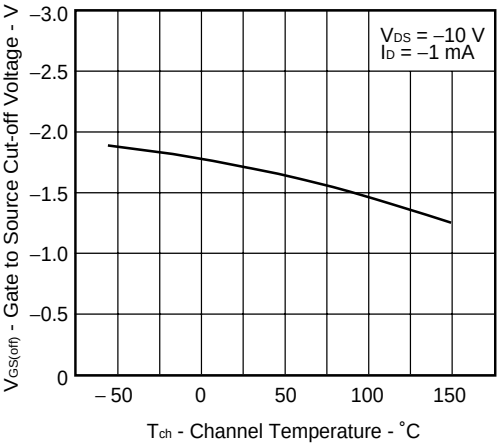
DRAIN TO SOURCE ON-STATE RESISTANCE vs.
GATE TO SOURCE VOLTAGE



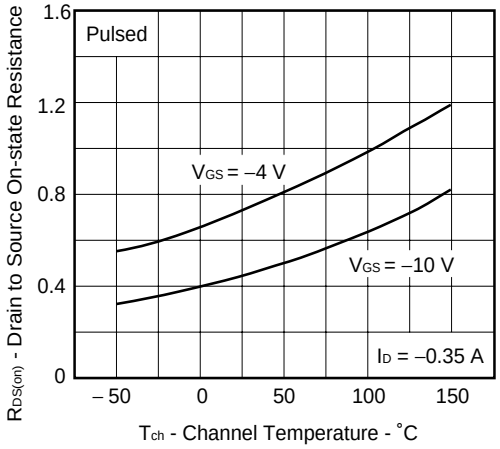
DRAIN TO SOURCE ON-STATE
RESISTANCE vs. DRAIN CURRENT



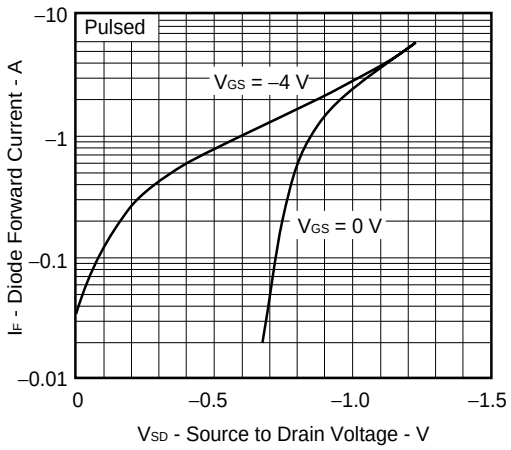
GATE TO SOURCE CUT-OFF VOLTAGE vs.
CHANNEL TEMPERATURE



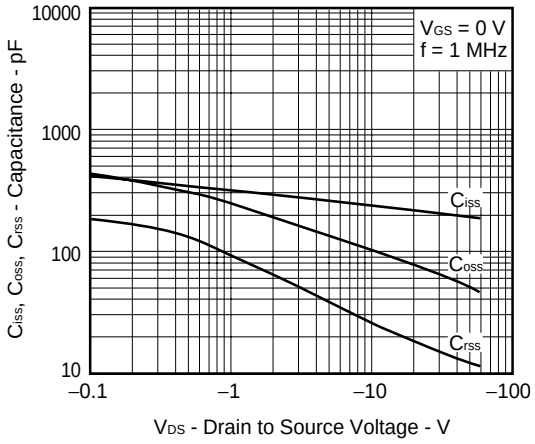
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



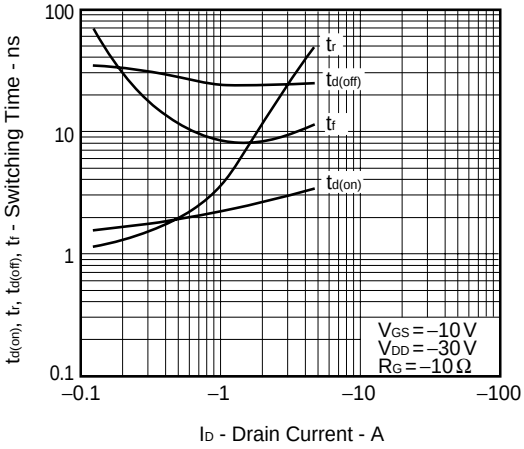
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



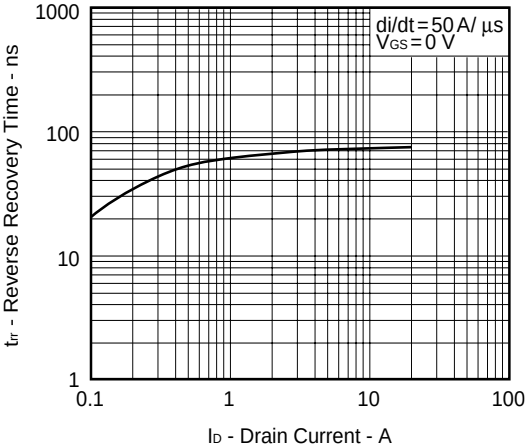
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



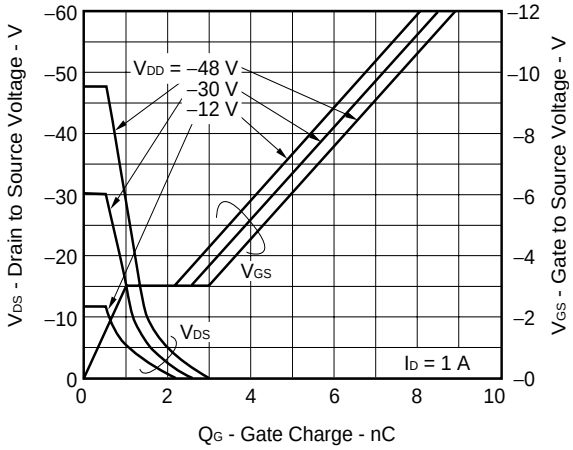
SWITCHING CHARACTERISTICS



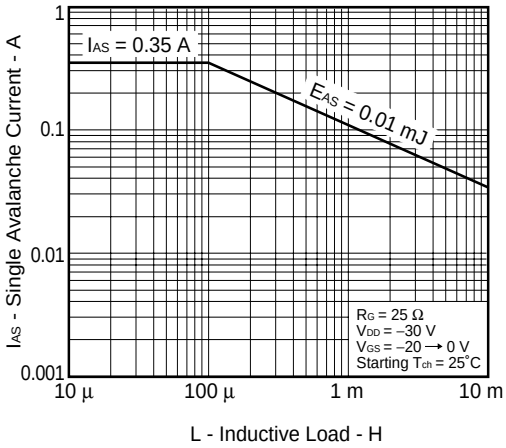
REVERSE RECOVERY TIME vs. DRAIN CURRENT



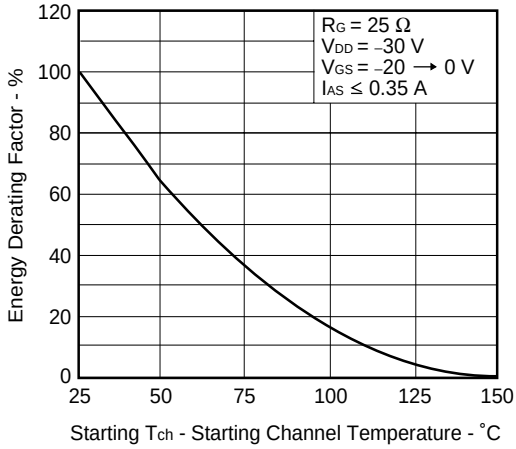
DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SINGLE AVALANCHE CURRENT vs.
INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY
DERATING FACTOR



[MEMO]

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