

To our customers,

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## Old Company Name in Catalogs and Other Documents

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April 1<sup>st</sup>, 2010  
Renesas Electronics Corporation

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SWITCHING  
P-CHANNEL POWER MOS FET

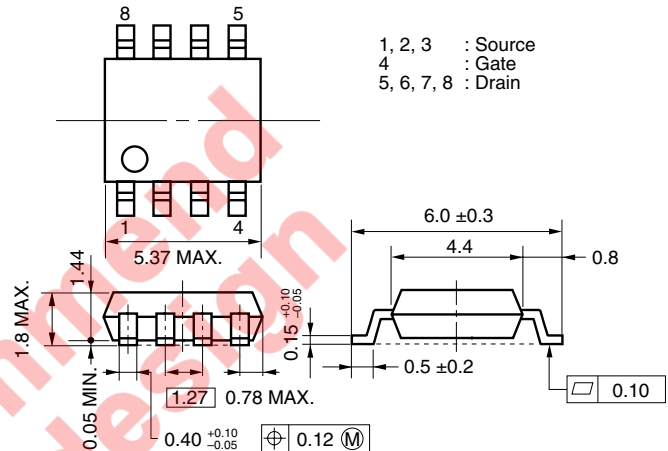
DESCRIPTION

The  $\mu$ PA2716GR is P-Channel MOS Field Effect Transistor designed for power management applications of notebook computers and Li-ion battery protection circuit.

FEATURES

- Low on-state resistance  
 $R_{DS(on)1} = 7.0 \text{ m}\Omega \text{ MAX. (} V_{GS} = -10 \text{ V, } I_D = -7.0 \text{ A)}$   
 $R_{DS(on)2} = 11.3 \text{ m}\Omega \text{ MAX. (} V_{GS} = -4.5 \text{ V, } I_D = -7.0 \text{ A)}$
- Low  $C_{iss}$ :  $C_{iss} = 3000 \text{ pF TYP.}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)

PACKAGE DRAWING (Unit: mm)



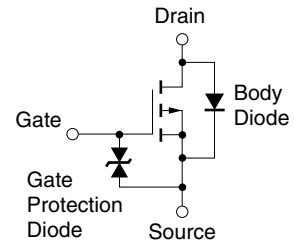
ORDERING INFORMATION

PART NUMBER	PACKAGE
$\mu$ PA2716GR	Power SOP8

ABSOLUTE MAXIMUM RATINGS ( $T_A = 25^\circ\text{C}$ , All terminals are connected.)

Drain to Source Voltage ( $V_{GS} = 0 \text{ V}$ )	$V_{DSS}$	-30	V
Gate to Source Voltage ( $V_{DS} = 0 \text{ V}$ )	$V_{GSS}$	±20	V
Drain Current (DC)	$I_{D(DC)}$	±14	A
Drain Current (pulse) <sup>Note1</sup>	$I_{D(pulse)}$	±140	A
Total Power Dissipation <sup>Note2</sup>	$P_{T1}$	2	W
Total Power Dissipation <sup>Note3</sup>	$P_{T2}$	2	W
Channel Temperature	$T_{ch}$	150	°C
Storage Temperature	$T_{stg}$	-55 to +150	°C
★ Single Avalanche Current <sup>Note4</sup>	$I_{AS}$	-14	A
Single Avalanche Energy <sup>Note4</sup>	$E_{AS}$	19.6	mJ

EQUIVALENT CIRCUIT



- Notes
1.  $PW \leq 10 \mu\text{s}$ , Duty Cycle  $\leq 1\%$
  2. Mounted on ceramic substrate of  $1200 \text{ mm}^2 \times 2.2 \text{ mm}$
  3. Mounted on glass epoxy board of  $25.4 \text{ mm} \times 25.4 \text{ mm} \times 0.8 \text{ mm}$ ,  $PW = 10 \text{ sec}$
  4. Starting  $T_{ch} = 25^\circ\text{C}$ ,  $V_{DD} = -15 \text{ V}$ ,  $R_G = 25 \Omega$ ,  $L = 100 \mu\text{H}$ ,  $V_{GS} = -20 \rightarrow 0 \text{ V}$

**Remark** The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

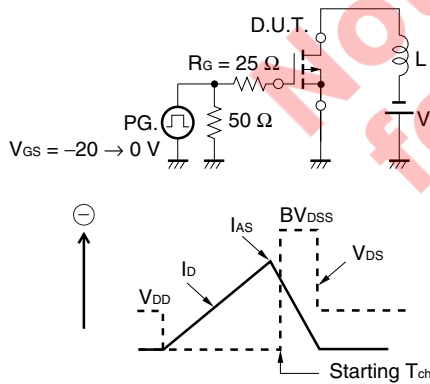
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**ELECTRICAL CHARACTERISTICS (T<sub>A</sub> = 25°C, All terminals are connected.)**

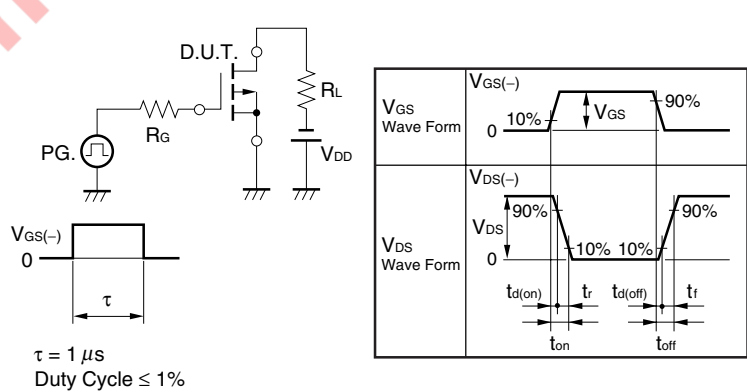
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I <sub>DSS</sub>	V <sub>DS</sub> = -30 V, V <sub>GS</sub> = 0 V			-1	μA
Gate Leakage Current	I <sub>GSS</sub>	V <sub>GS</sub> = ±20 V, V <sub>DS</sub> = 0 V			±10	μA
Gate Cut-off Voltage	V <sub>GS(off)</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -1 mA	-1.0		-2.5	V
Forward Transfer Admittance <sup>Note</sup>	y <sub>fs</sub>	V <sub>DS</sub> = -10 V, I <sub>D</sub> = -7.0 A	10			S
Drain to Source On-state Resistance <sup>Note</sup>	R <sub>DS(on)1</sub>	V <sub>GS</sub> = -10 V, I <sub>D</sub> = -7.0 A		5.5	7.0	mΩ
	R <sub>DS(on)2</sub>	V <sub>GS</sub> = -4.5 V, I <sub>D</sub> = -7.0 A		7.3	11.3	mΩ
	R <sub>DS(on)3</sub>	V <sub>GS</sub> = -4.0 V, I <sub>D</sub> = -7.0 A		8.3	13.5	mΩ
Input Capacitance	C <sub>iss</sub>	V <sub>DS</sub> = -10 V		3000		pF
Output Capacitance	C <sub>oss</sub>	V <sub>GS</sub> = 0 V		960		pF
Reverse Transfer Capacitance	C <sub>rss</sub>	f = 1 MHz		500		pF
Turn-on Delay Time	t <sub>d(on)</sub>	V <sub>DD</sub> = -15 V, I <sub>D</sub> = -7.0 A		14		ns
Rise Time	t <sub>r</sub>	V <sub>GS</sub> = -10 V		19		ns
Turn-off Delay Time	t <sub>d(off)</sub>	R <sub>G</sub> = 10 Ω		680		ns
Fall Time	t <sub>f</sub>			340		ns
Total Gate Charge	Q <sub>G</sub>	V <sub>DD</sub> = -24 V		95		nC
Gate to Source Charge	Q <sub>GS</sub>	V <sub>GS</sub> = -10 V		11		nC
Gate to Drain Charge	Q <sub>GD</sub>	I <sub>D</sub> = -14 A		25		nC
Body Diode Forward Voltage <sup>Note</sup>	V <sub>F(S-D)</sub>	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0 V		0.83		V
Reverse Recovery Time	t <sub>rr</sub>	I <sub>F</sub> = 14 A, V <sub>GS</sub> = 0 V		380		ns
Reverse Recovery Charge	Q <sub>rr</sub>	di/dt = 50 A/μs		690		nC

Note Pulsed

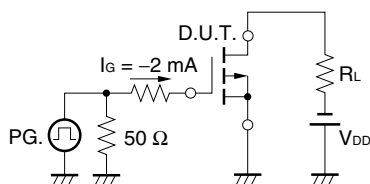
**TEST CIRCUIT 1 AVALANCHE CAPABILITY**



**TEST CIRCUIT 2 SWITCHING TIME**

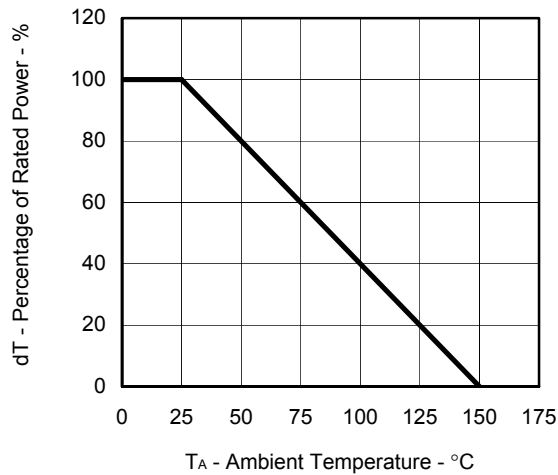


**TEST CIRCUIT 3 GATE CHARGE**

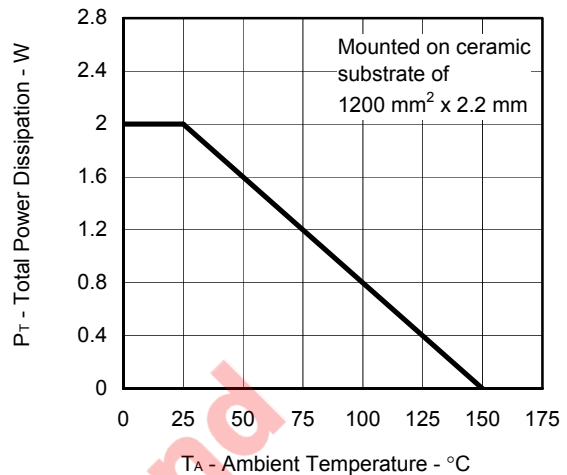


TYPICAL CHARACTERISTICS ( $T_A = 25^\circ\text{C}$ )

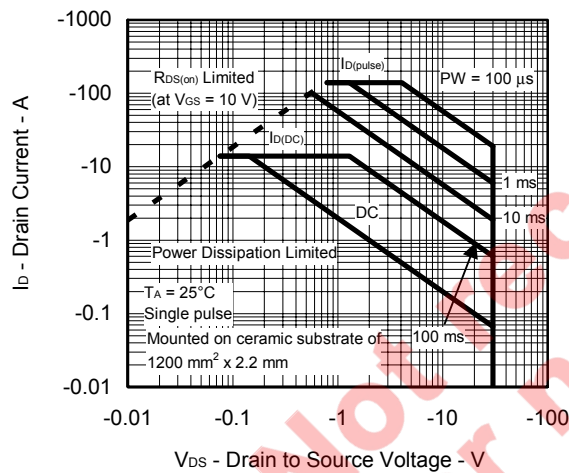
DERATING FACTOR OF FORWARD BIAS SAFE OPERATING AREA



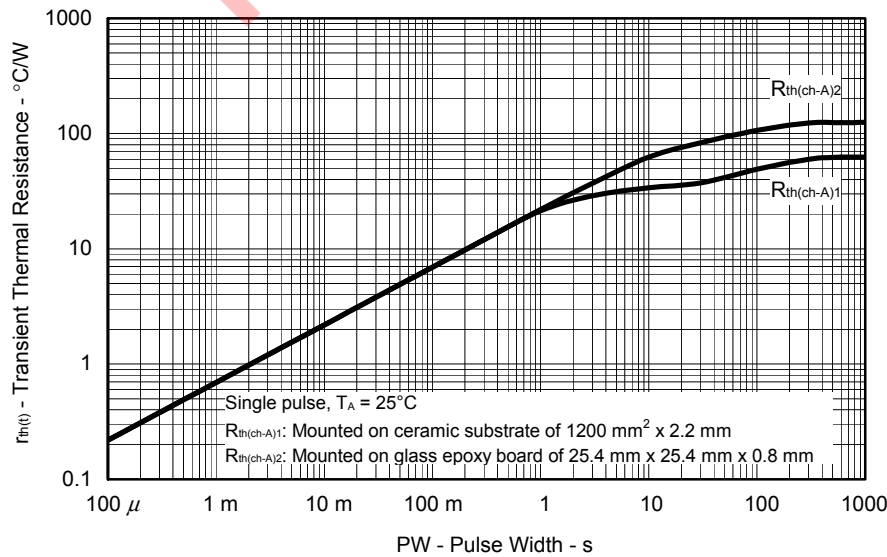
TOTAL POWER DISSIPATION vs. AMBIENT TEMPERATURE



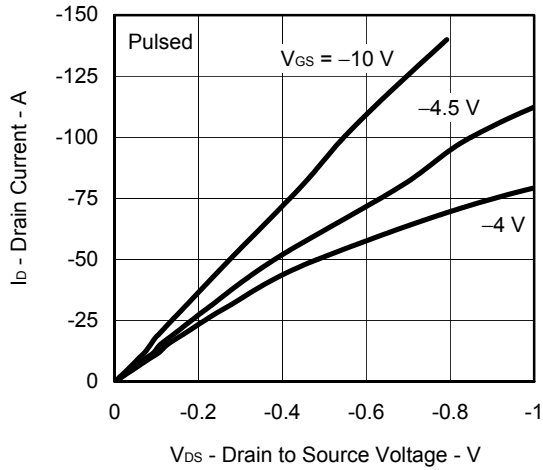
FORWARD BIAS SAFE OPERATING AREA



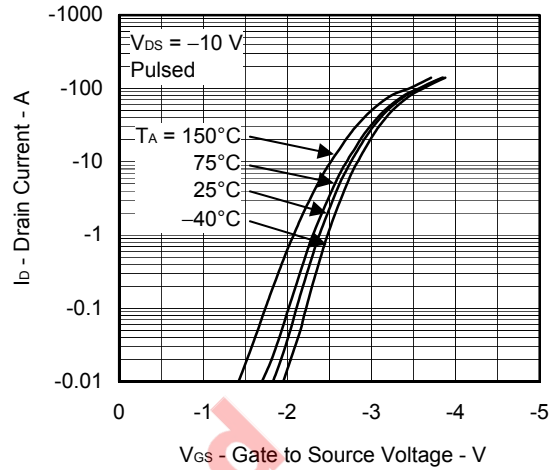
TRANSIENT THERMAL RESISTANCE vs. PULSE WIDTH



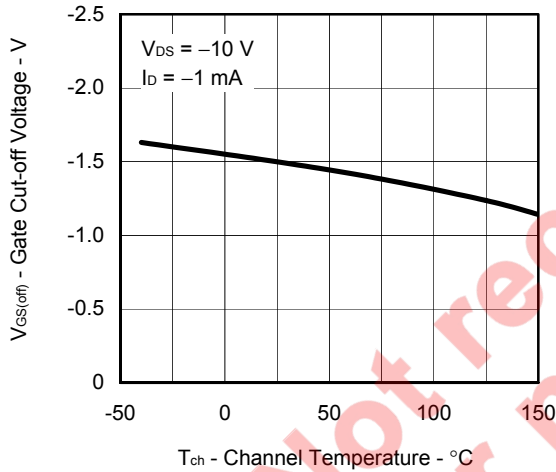
DRAIN CURRENT vs. DRAIN TO SOURCE VOLTAGE



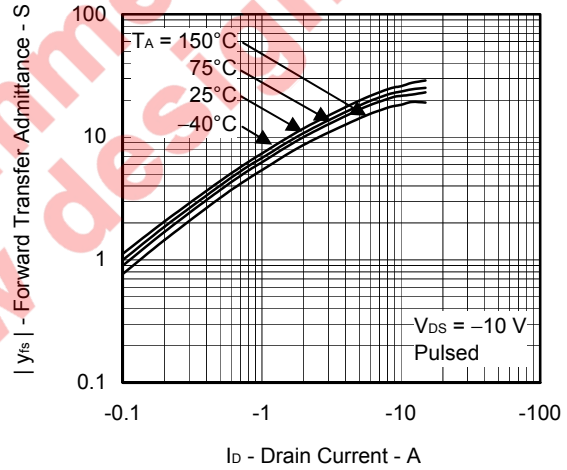
FORWARD TRANSFER CHARACTERISTICS



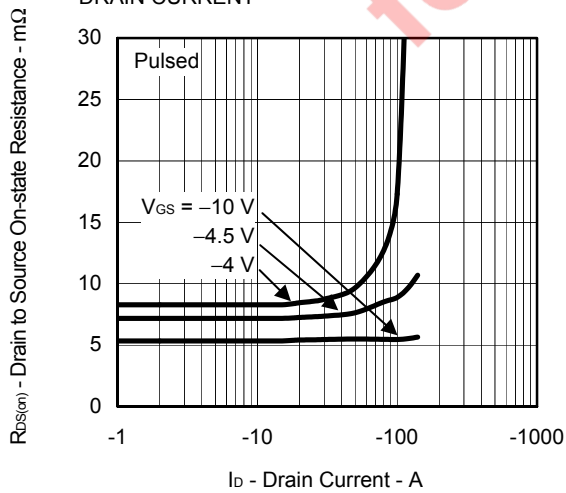
GATE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



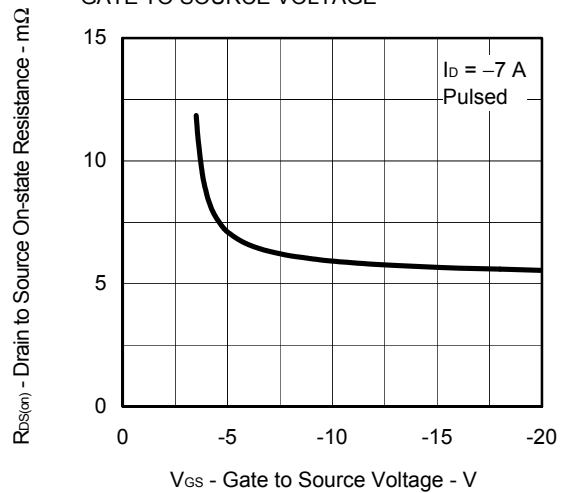
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



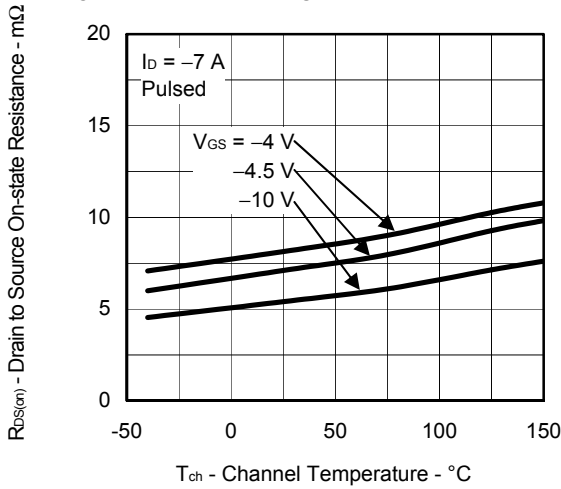
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



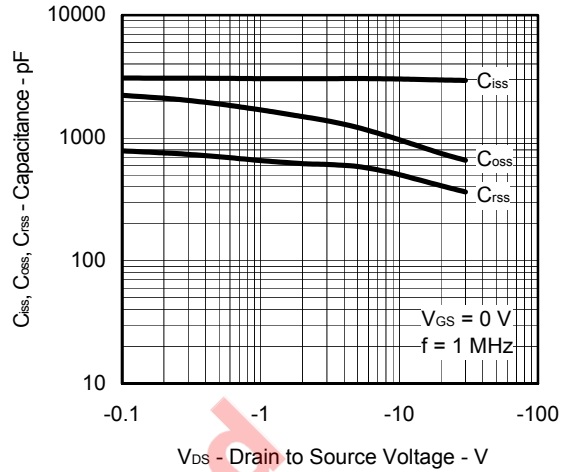
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



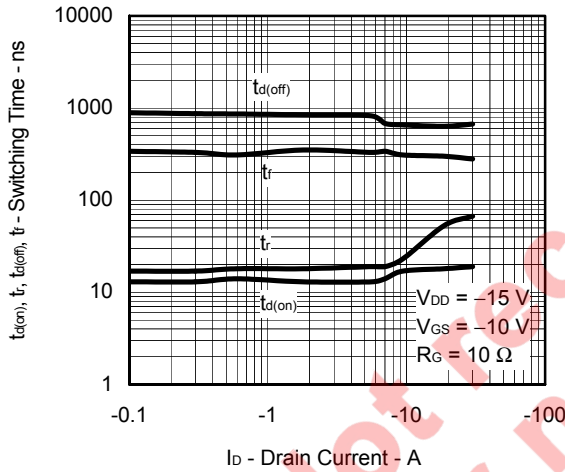
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



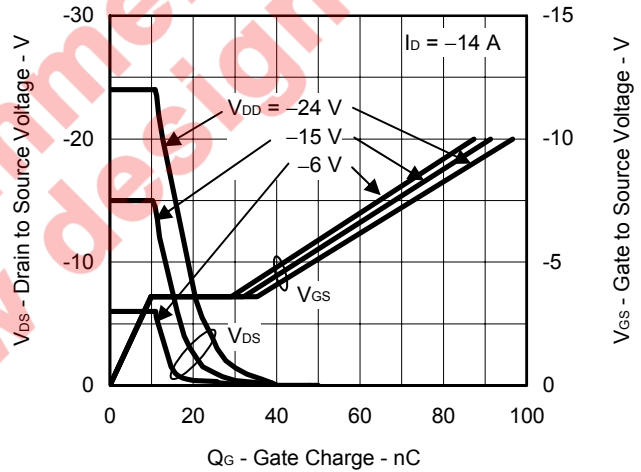
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



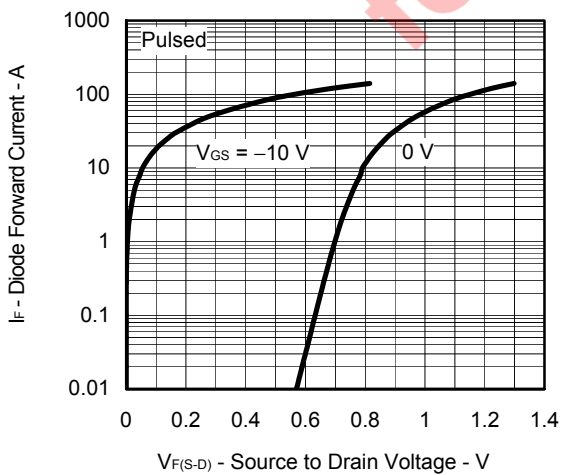
SWITCHING CHARACTERISTICS



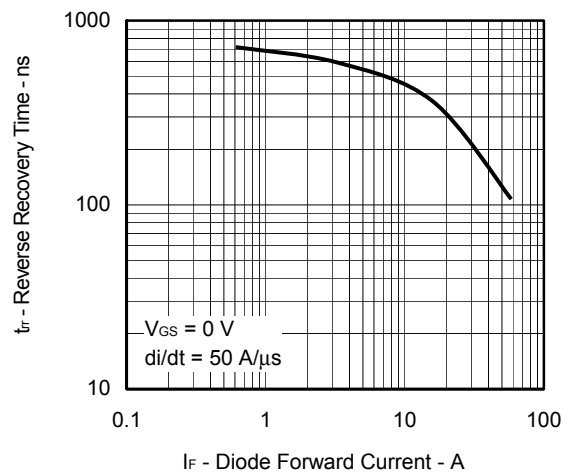
★ DYNAMIC INPUT/OUTPUT CHARACTERISTICS



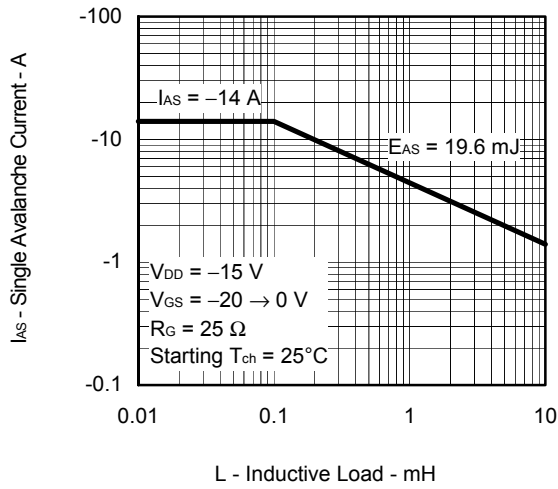
SOURCE TO DRAIN DIODE FORWARD VOLTAGE



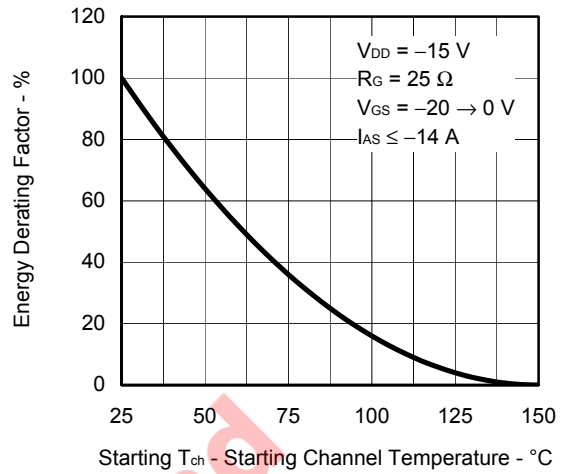
REVERSE RECOVERY TIME vs. DIODE FORWARD CURRENT



SINGLE AVALANCHE CURRENT vs. INDUCTIVE LOAD



SINGLE AVALANCHE ENERGY DERATING FACTOR



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