

To our customers,

Old Company Name in Catalogs and Other Documents

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Renesas Electronics website: <http://www.renesas.com>

April 1st, 2010
Renesas Electronics Corporation

Issued by: Renesas Electronics Corporation (<http://www.renesas.com>)

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MOS FIELD EFFECT TRANSISTOR μ PA2720AGR

SWITCHING N-CHANNEL POWER MOSFET

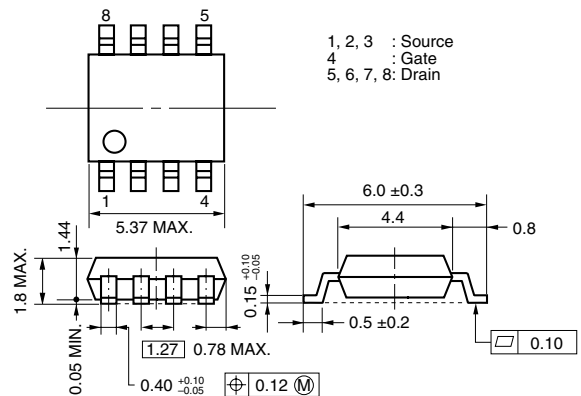
DESCRIPTION

The μ PA2720AGR is N-channel MOS Field Effect Transistor designed for power management applications of a notebook computer and Lithium-Ion battery protection circuit.

FEATURES

- Low on-state resistance
 $R_{DS(on)1} = 6.6 \text{ m}\Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 7 \text{ A)}$
 $R_{DS(on)2} = 14 \text{ m}\Omega \text{ MAX. (} V_{GS} = 5.0 \text{ V, } I_D = 7 \text{ A)}$
- Low input capacitance
 $C_{iss} = 3600 \text{ pF TYP. (} V_{DS} = 10 \text{ V, } V_{GS} = 0 \text{ V)}$
- Built-in gate protection diode
- Small and surface mount package (Power SOP8)
- RoHS Compliant

PACKAGE DRAWING (Unit: mm)



ORDERING INFORMATION

PART NUMBER	LEAD PLATING	PACKING	PACKAGE
μ PA2720AGR-E1-AT ^{Note}	Pure Sn	Tape 2500 p/reel	Power SOP8
μ PA2720AGR-E2-AT ^{Note}			0.08 g TYP.

Note Pb-free (This product does not contain Pb in external electrode and other parts.)

ABSOLUTE MAXIMUM RATINGS (T_A = 25°C, All terminals are connected.)

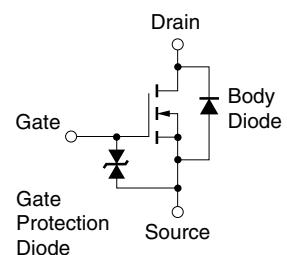
Drain to Source Voltage (V _{GS} = 0 V)	V _{DSS}	30	V
Gate to Source Voltage (V _{DS} = 0 V)	V _{GSS}	\pm 20	V
Drain Current (DC)	I _{D(DC)}	\pm 14	A
Drain Current (pulse) ^{Note1}	I _{D(pulse)}	\pm 150	A
Total Power Dissipation ^{Note2}	P _{T1}	1.1	W
Total Power Dissipation (PW = 10 sec) ^{Note2}	P _{T2}	2.5	W
Channel Temperature	T _{ch}	150	°C
Storage Temperature	T _{stg}	-55 to +150	°C
Single Avalanche Current ^{Note3}	I _{AS}	14	A
Single Avalanche Energy ^{Note3}	E _{AS}	19.6	mJ

Notes 1. PW \leq 10 μ s, Duty Cycle \leq 1%

2. Mounted on glass epoxy board of 25.4 mm x 25.4 mm x 0.8 mm

3. Starting T_{ch} = 25°C, V_{DD} = 15 V, R_G = 25 Ω , V_{GS} = 20 \rightarrow 0 V, L = 100 μ H

EQUIVALENT CIRCUIT



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

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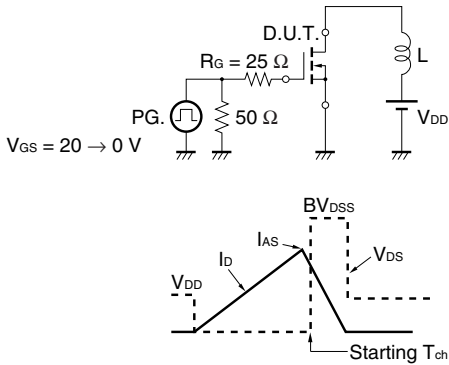
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ELECTRICAL CHARACTERISTICS (TA = 25°C, All terminals are connected.)

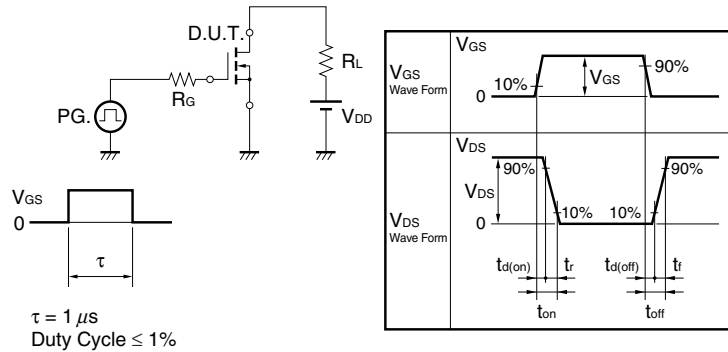
CHARACTERISTICS	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I _{DSS}	V _{DS} = 30 V, V _{GS} = 0 V			1	μA
Gate Leakage Current	I _{GSS}	V _{GS} = ±20 V, V _{DS} = 0 V			±10	μA
Gate to Source Cut-off Voltage	V _{GS(off)}	V _{DS} = 10 V, I _D = 1 mA	1.5		3.0	V
Forward Transfer Admittance ^{Note}	y _{fs}	V _{DS} = 10 V, I _D = 7 A	7			S
Drain to Source On-state Resistance ^{Note}	R _{DS(on)1}	V _{GS} = 10 V, I _D = 7 A		5.5	6.6	mΩ
	R _{DS(on)2}	V _{GS} = 5.0 V, I _D = 7 A		7.0	14	mΩ
Input Capacitance	C _{iss}	V _{DS} = 10 V,		3600		pF
Output Capacitance	C _{oss}	V _{GS} = 0 V,		490		pF
Reverse Transfer Capacitance	C _{rss}	f = 1 MHz		250		pF
Turn-on Delay Time	t _{d(on)}	V _{DD} = 15 V, I _D = 7 A,		22		ns
Rise Time	t _r	V _{GS} = 10 V,		22		ns
Turn-off Delay Time	t _{d(off)}	R _G = 10 Ω		73		ns
Fall Time	t _f			17		ns
Total Gate Charge	Q _G	V _{DD} = 15 V,		28		nC
Gate to Source Charge	Q _{GS}	V _{GS} = 5 V,		10		nC
Gate to Drain Charge	Q _{GD}	I _D = 14 A		11		nC
Body Diode Forward Voltage ^{Note}	V _{F(S-D)}	I _F = 14 A, V _{GS} = 0 V		0.8		V
Reverse Recovery Time	t _{rr}	I _F = 14 A, V _{GS} = 0 V,		31		ns
Reverse Recovery Charge	Q _{rr}	di/dt = 100 A/μs		25		nC

Note Pulsed

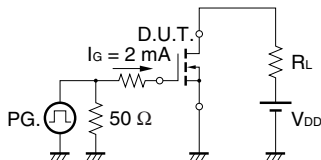
TEST CIRCUIT 1 AVALANCHE CAPABILITY



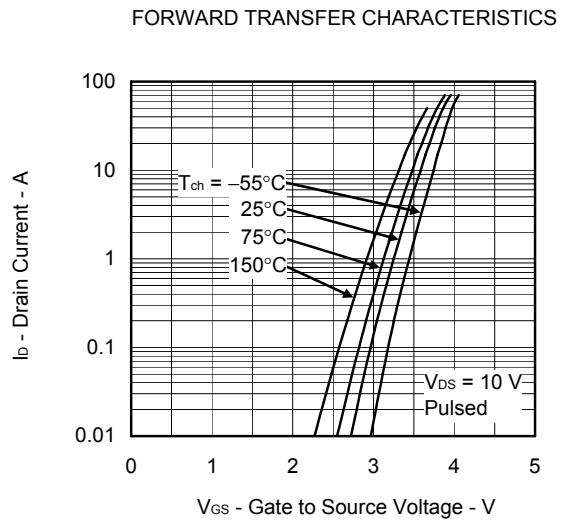
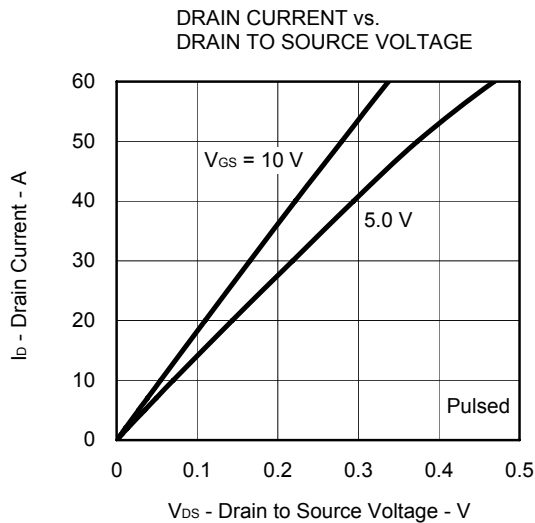
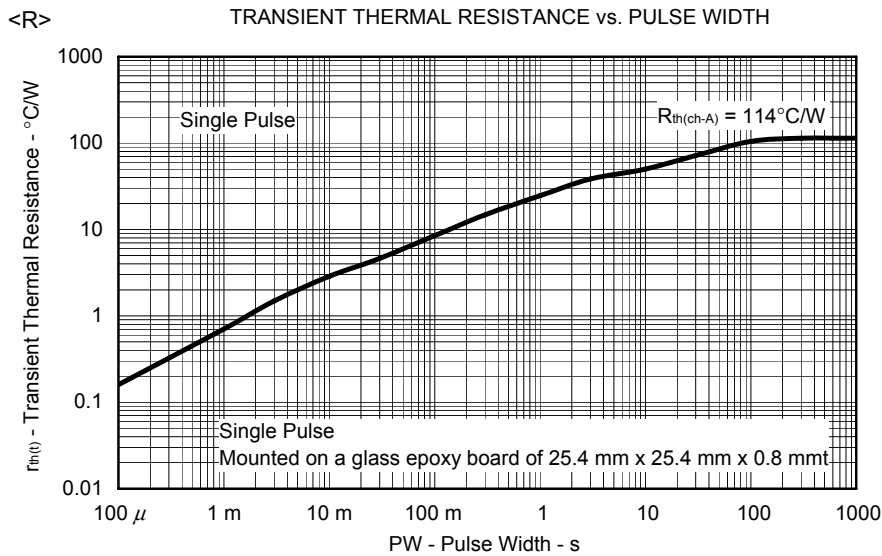
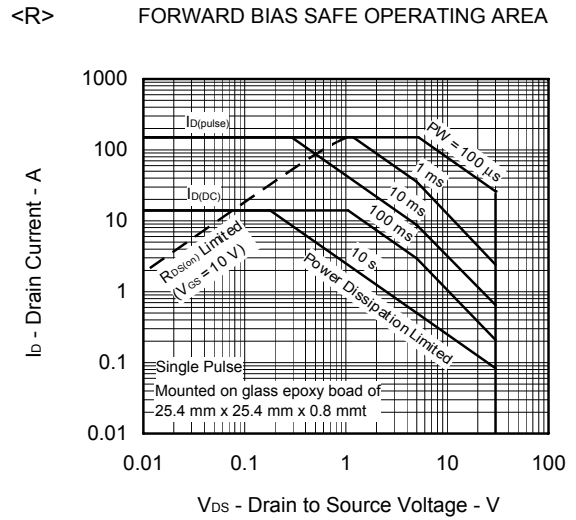
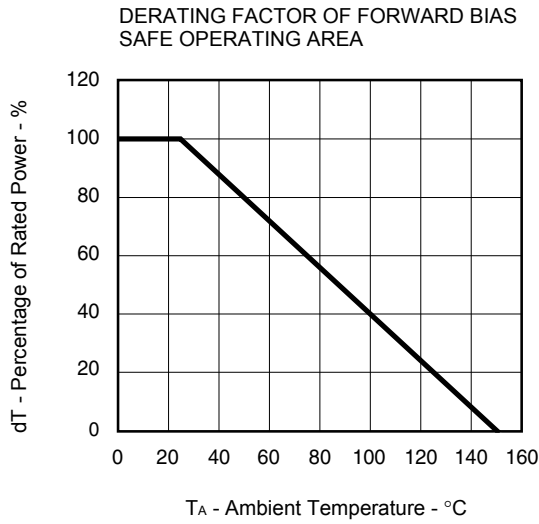
TEST CIRCUIT 2 SWITCHING TIME



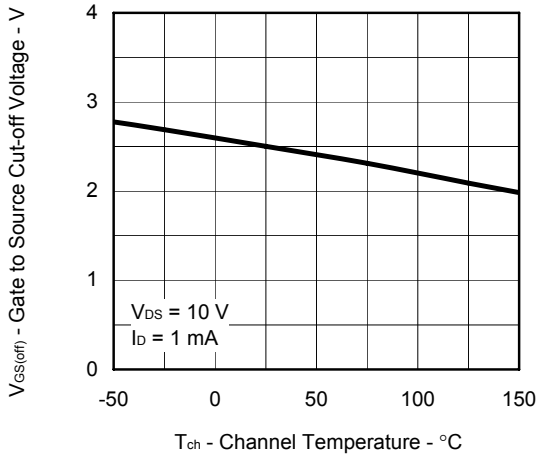
TEST CIRCUIT 3 GATE CHARGE



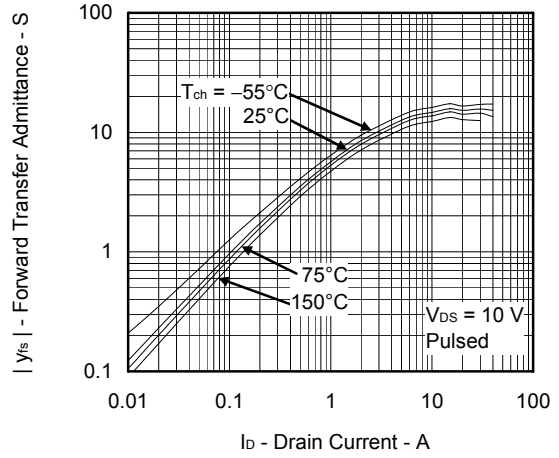
TYPICAL CHARACTERISTICS ($T_A = 25^\circ\text{C}$)



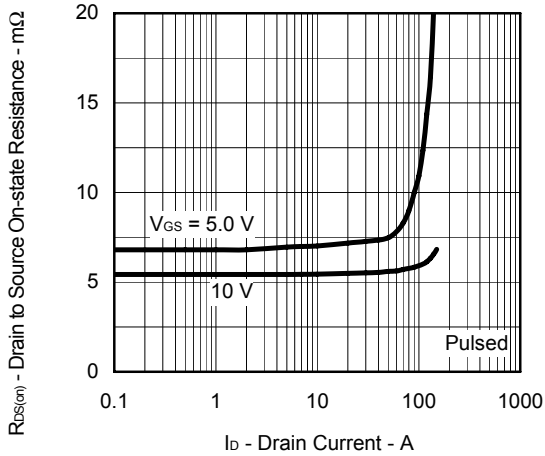
GATE TO SOURCE CUT-OFF VOLTAGE vs. CHANNEL TEMPERATURE



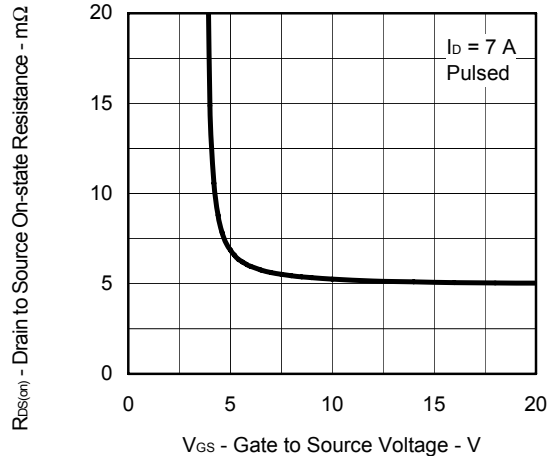
FORWARD TRANSFER ADMITTANCE vs. DRAIN CURRENT



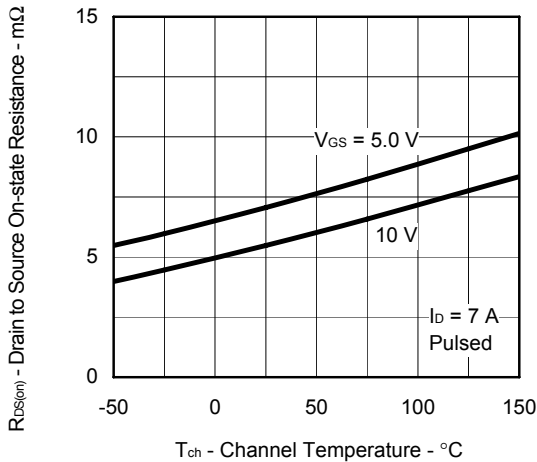
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



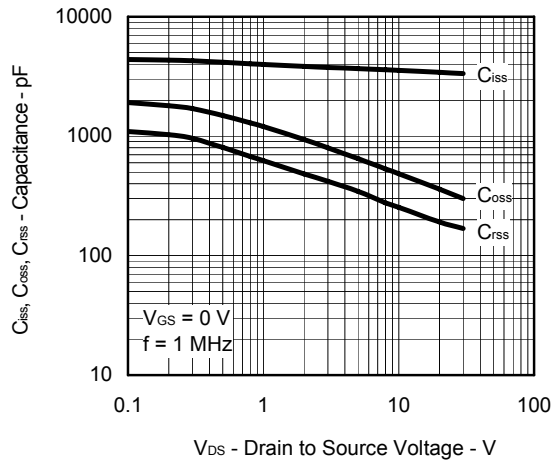
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



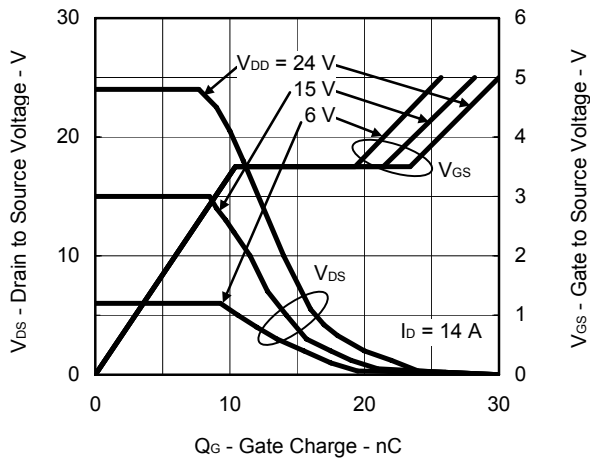
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



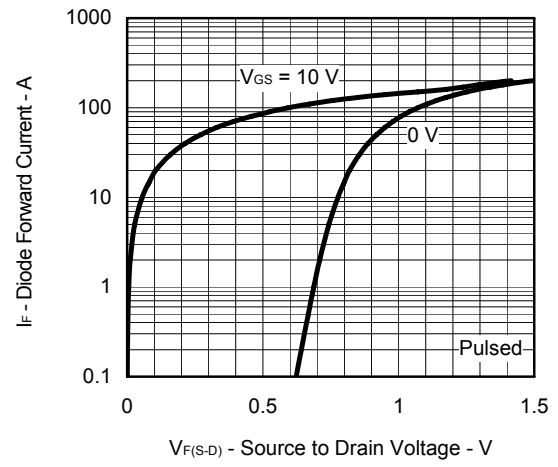
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



DYNAMIC INPUT/OUTPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE



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