

μPA672CT

R07DS1289EJ0200

Rev.2.00

Jul 24, 2015

N-CHANNEL MOSFET FOR SWITCHING

Description

The UPA672CT, N-channel vertical type MOSFET designed for general-purpose switch, is a device which can be driven directly by a 4.5 V power source.

Features

- Two MOSFET circuits
- Directly driven by a 4.5 V power source.
- Low on-state resistance
 - $R_{DS(on)1} = 2.7 \Omega \text{ MAX. (} V_{GS} = 10 \text{ V, } I_D = 100 \text{ mA)}$
 - $R_{DS(on)2} = 3.2 \Omega \text{ MAX. (} V_{GS} = 4.5 \text{ V, } I_D = 50 \text{ mA)}$

Ordering Information

Part Number	Lead Plating	Packing	Package
UPA672CT-T1-A/AT	-A:Sn-Bi , -AT:Pure Sn	3000p/Reel	SC-88 (6pSSP)

Remark "-AT" indicates Pb-free. This product does not contain Pb in external electrode and other parts.

Marking UA

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$)

Drain to Source Voltage ($V_{GS} = 0 \text{ V}$)	V_{DSS}	60	V
Gate to Source Voltage ($V_{DS} = 0 \text{ V}$)	V_{GSS}	± 20	V
Drain Current (DC)	$I_{D(DC)}$	± 100	mA
Drain Current (pulse) ^{Note}	$I_{D(pulse)}$	± 200	mA
Total Power Dissipation	P_T	200 (Total)	mW
Channel Temperature	T_{ch}	150	$^\circ\text{C}$
Storage Temperature	T_{stg}	-55 to +150	$^\circ\text{C}$

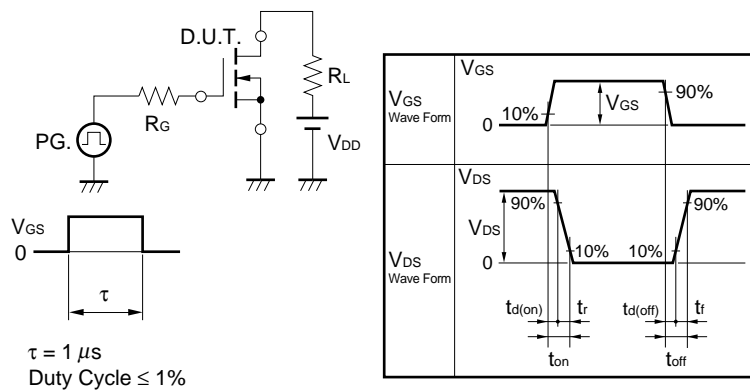
Note $PW \leq 10 \mu\text{s}$, Duty Cycle $\leq 1\%$

Electrical Characteristics (TA = 25°C)

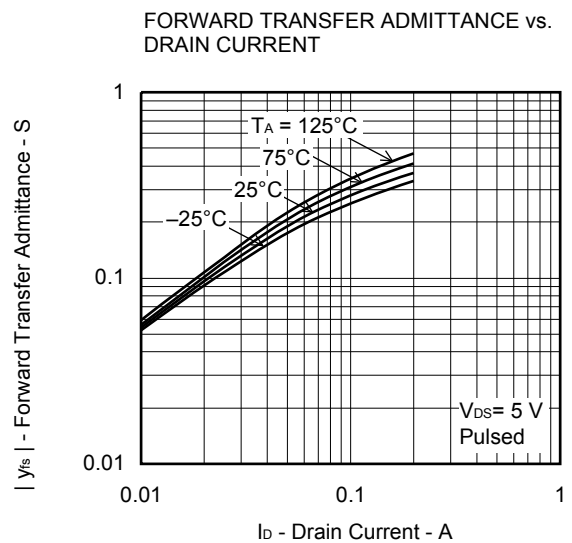
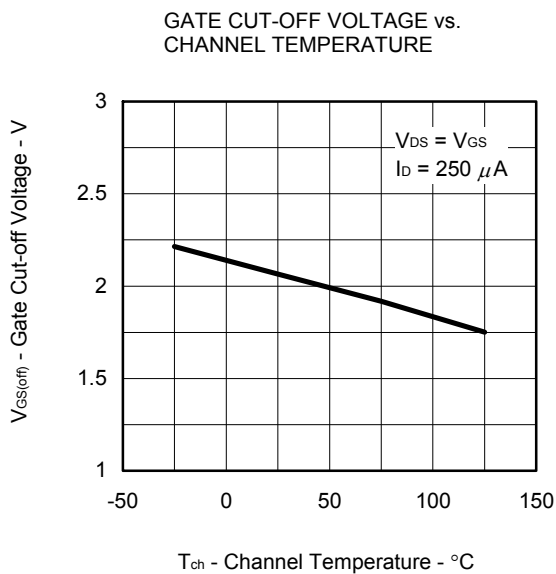
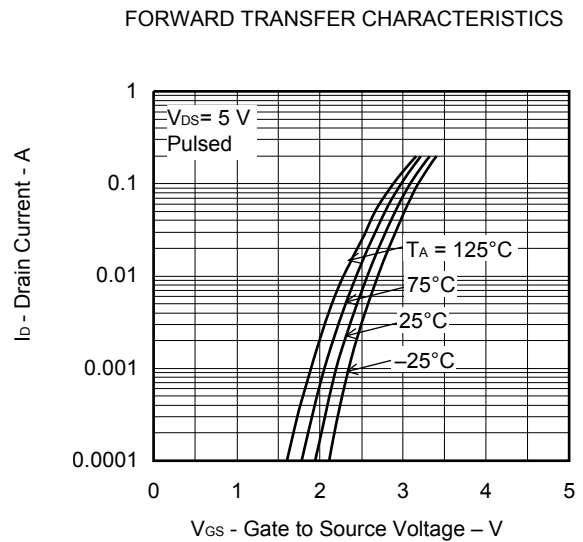
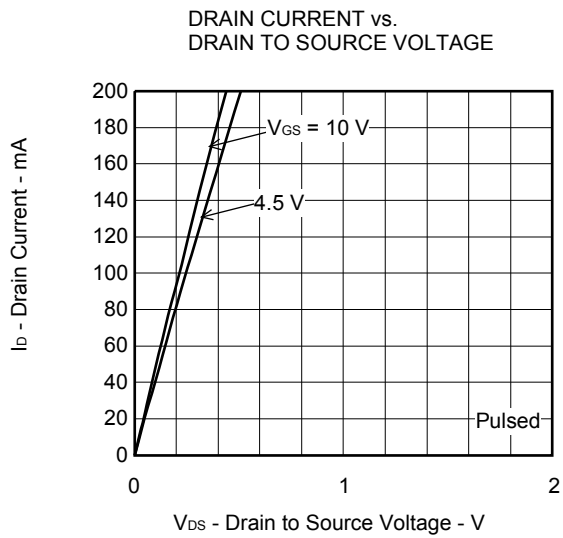
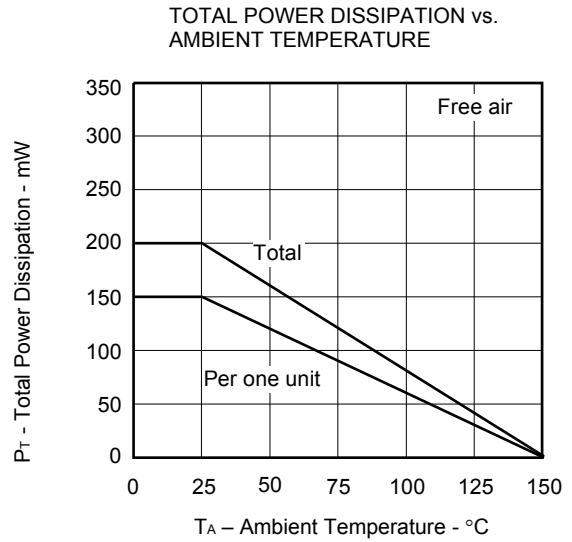
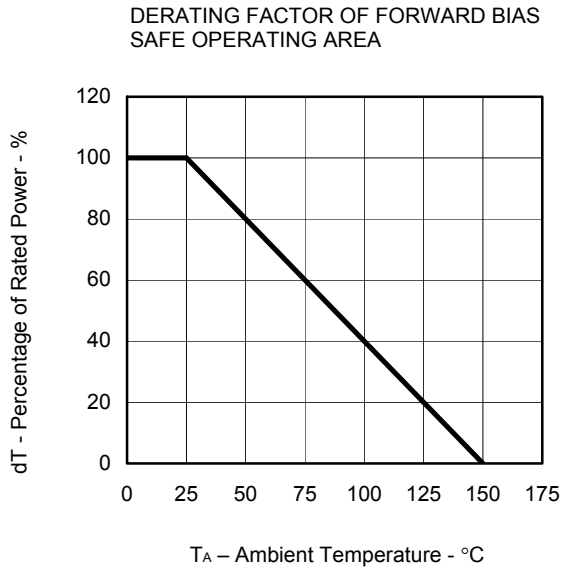
Characteristics	Symbol	Test Conditions	MIN.	TYP.	MAX.	UNIT
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = 60\text{ V}, V_{GS} = 0\text{ V}$			1	μA
Gate Leakage Current	I_{GSS}	$V_{GS} = \pm 20\text{ V}, V_{DS} = 0\text{ V}$			± 10	μA
Gate to Source Cut-off Voltage	$V_{GS(off)}$	$V_{DS} = V_{GS}, I_D = 250\ \mu\text{A}$	1.0		2.5	V
Forward Transfer Admittance Note	$ y_{fs} $	$V_{DS} = 10\text{ V}, I_D = 100\text{ mA}$	150			mS
Drain to Source On-state Resistance Note	$R_{DS(on)1}$	$V_{GS} = 10\text{ V}, I_D = 100\text{ mA}$		2.1	2.7	Ω
	$R_{DS(on)2}$	$V_{GS} = 4.5\text{ V}, I_D = 50\text{ mA}$		2.4	3.2	Ω
Input Capacitance	C_{iss}	$V_{DS} = 10\text{ V},$		20		pF
Output Capacitance	C_{oss}	$V_{GS} = 0\text{ V},$		9		pF
Reverse Transfer Capacitance	C_{rss}	$f = 1.0\text{ MHz}$		2		pF
Turn-on Delay Time	$t_{d(on)}$	$V_{DD} = 10\text{ V},$		16		ns
Rise Time	t_r	$I_D = 200\text{ mA},$		6.5		ns
Turn-off Delay Time	$t_{d(off)}$	$V_{GS} = 10\text{ V},$		82		ns
Fall Time	t_f	$R_G = 10\ \Omega$		32		ns
Total Gate Charge	Q_G	$I_D = 200\text{ mA}, V_{DD} = 25\text{ V}, V_{GS} = 10\text{ V}$		2		nC
Body Diode Forward Voltage Note	$V_{F(S-D)}$	$I_F = 200\text{ mA}, V_{GS} = 0\text{ V}$		0.86		V

Note Pulsed

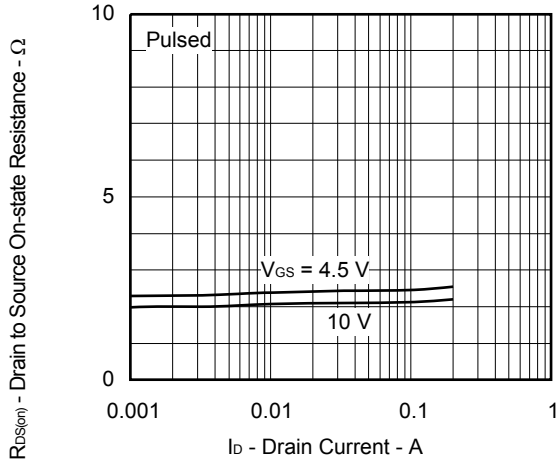
Test Circuit Switching Time



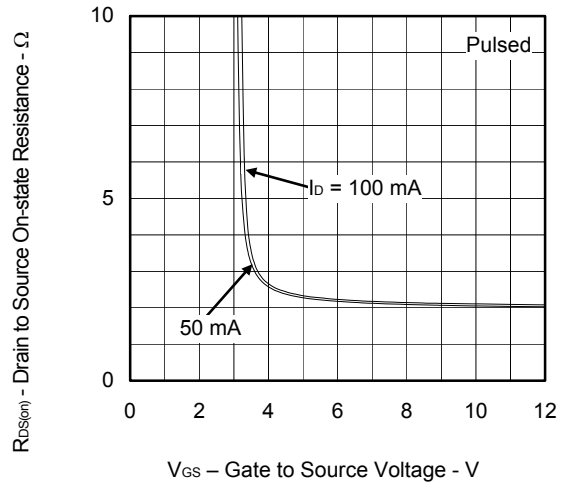
Typical Characteristics (T_A = 25°C)



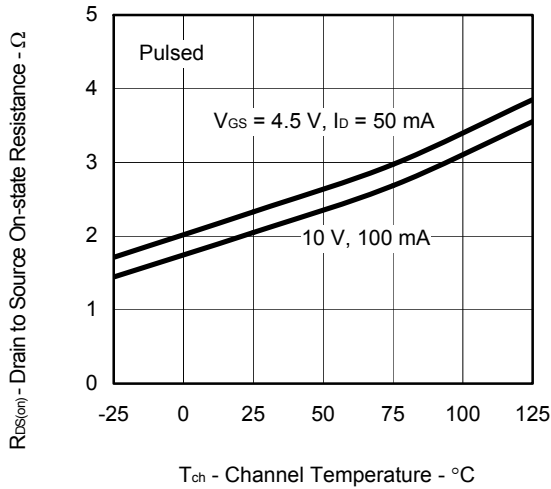
DRAIN TO SOURCE ON-STATE RESISTANCE vs. DRAIN CURRENT



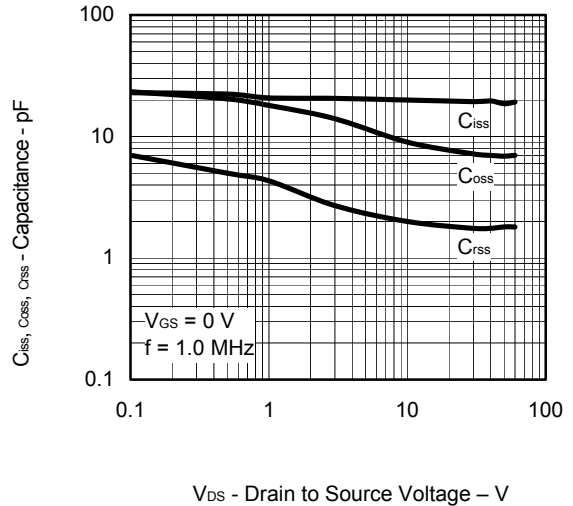
DRAIN TO SOURCE ON-STATE RESISTANCE vs. GATE TO SOURCE VOLTAGE



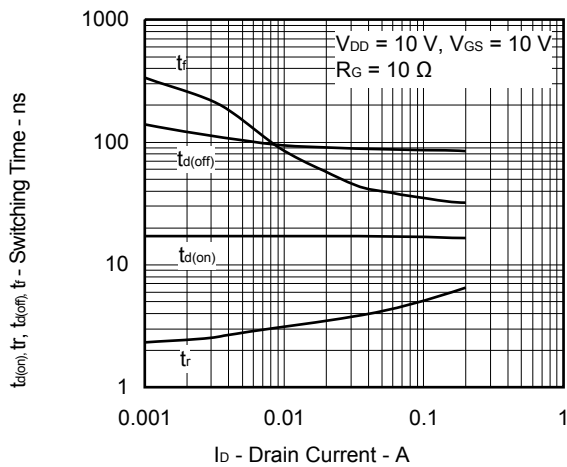
DRAIN TO SOURCE ON-STATE RESISTANCE vs. CHANNEL TEMPERATURE



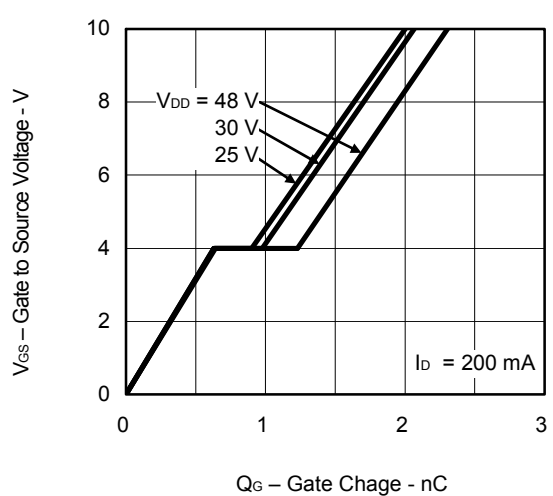
CAPACITANCE vs. DRAIN TO SOURCE VOLTAGE



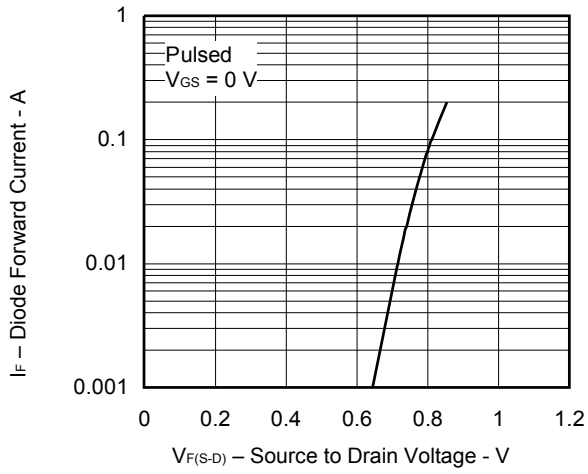
SWITCHING CHARACTERISTICS



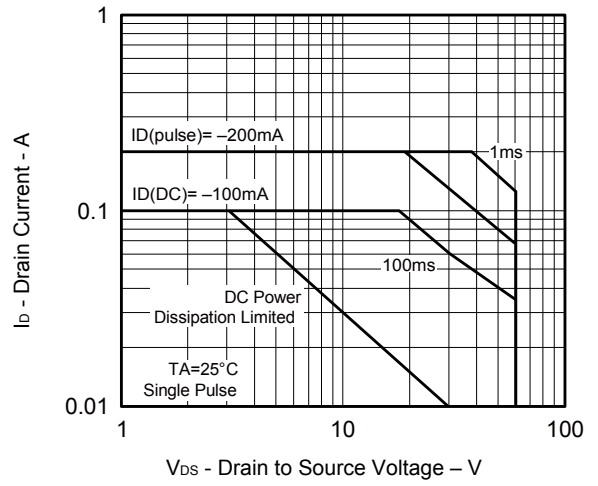
DYNAMIC INPUT CHARACTERISTICS



SOURCE TO DRAIN DIODE FORWARD VOLTAGE

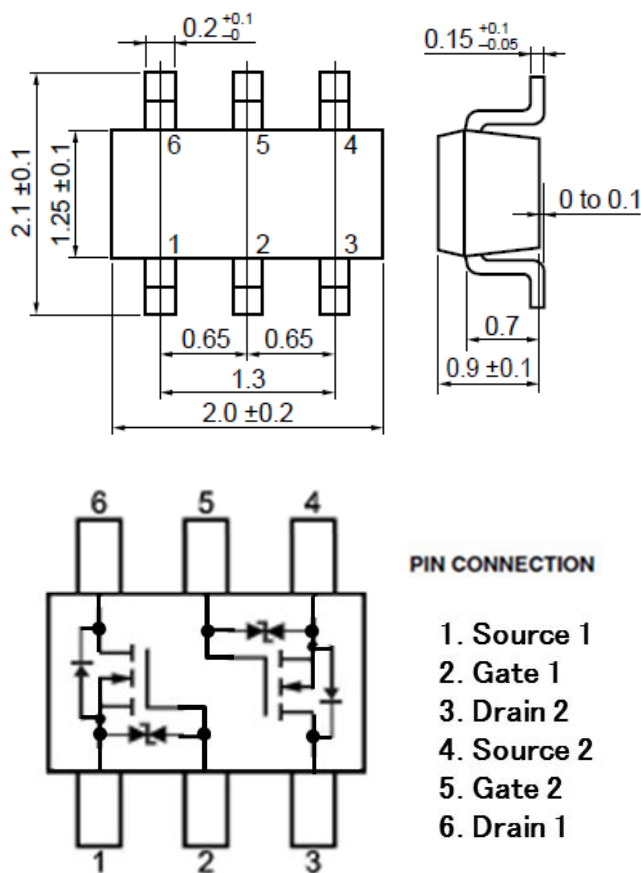


FORWARD BIAS SAFE OPERATING AREA

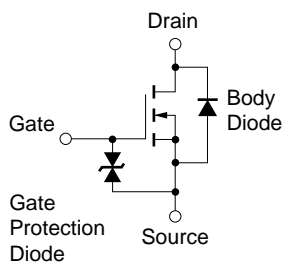


Package Drawings (Unit: mm)

SC-88 (6pSSP)



Equivalent Circuit



Remark The diode connected between the gate and source of the transistor serves as a protector against ESD. When this device actually used, an additional protection circuit is externally required if a voltage exceeding the rated voltage may be applied to this device.

	μPA672CT
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Rev.	Date	Description	
		Page	Summary
1.00	Sep , 2013	–	First Edition Issued
2.00	Jul, 2015	2	- Changed Electrical Characteristics - Changed Test Circuit Switching Time
		3, 4, 5	Changed all graphs

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Renesas Electronics America Inc.
2801 Scott Boulevard Santa Clara, CA 95050-2549, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6130

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-585-100, Fax: +44-1628-585-900

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709, Quantum Plaza, No.27 ZhichunLu Haidian District, Beijing 100191, P.R.China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, P. R. China 200333
Tel: +86-21-2226-0888, Fax: +86-21-2226-0899

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-8688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jin Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL II Stage, Indiranagar, Bangalore, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
12F., 234 Teheran-ro, Gangnam-Gu, Seoul, 135-080, Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5141