

μPC834, 4064

Low Power Consumption J-FET Input Quad Operational Amplifier

R03DS0153EJ0100
Rev.1.00
2019.11.12

DESCRIPTION

The μPC834 and 4064 are low power consumption versions operational amplifier of μPC804 and 4084 series with the general-purpose J-FET input. This revolutionary J-FET input operational amplifier realizes low power consumption of I_{CC} 800 μA TYP. and low voltage operation from ± 2 V. Owing to its J-FET input, the input impedance is high. The AC characteristics are also greatly improved compared to the conventional low power consumption operational amplifier. Therefore, it is ideal for application circuits such as amplifier circuits and active filters in various battery-operated electronic devices.

Depending on the operating ambient temperature, μPC834 is suitable for communication application while μPC4064 is suitable for general-purpose usage.

Along with this series of lineup, the dual type op-amp μPC832 and 4062 with same circuit configuration are also available.

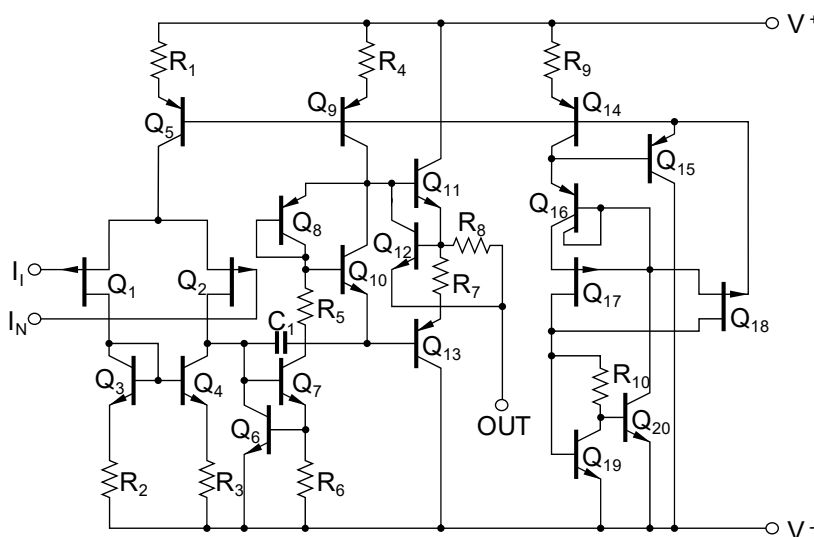
FEATURES

- Input Offset Voltage ±2 mV (TYP.)
- Input Bias Current 10 pA (TYP.)
- Slew Rate 3 V/μs (TYP.)
- Unity Gain Frequency 1 MHz (TYP.)
- Circuit Current 800 μA (TYP.)
- Operate from ±2 V
- Built-In Phase Compensation Circuit
- Built-In Output Short Circuit Protection
- Standard Quad Op-Amp terminal connection (pin compatible)

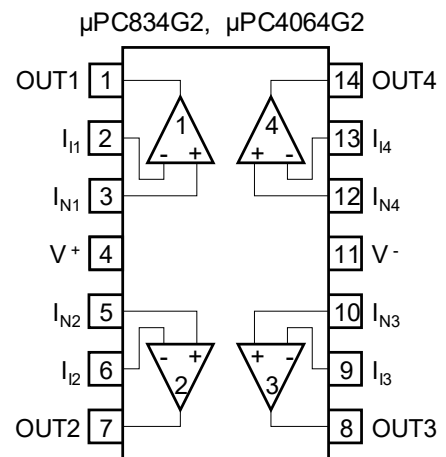
ORDERING INFORMATION

| Ordering Name | Package |
|---------------|--|
| μPC834G2-A | 14 pin plastic SOP (5.72 mm (225 mil)) |
| μPC4064G2-A | 14 pin plastic SOP (5.72 mm (225 mil)) |

EQUIVALENT CIRCUIT (1/4 Circuit)



PIN CONFIGURATION (Top View)



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

| PARAMETER | SYMBOL | μPC834G2 | μPC4064G2 | UNIT |
|--|----------------------------------|--|------------|------|
| Supply Voltage ^{Note1} | V ⁺ to V ⁻ | -0.3 to +36 | | V |
| Differential Input Voltage | V _{ID} | ±30 | | V |
| Input Voltage ^{Note2} | V _I | V ⁻ -0.3 to V ⁺ +0.3 | | V |
| Output Applied Voltage ^{Note3} | V _O | V ⁻ -0.3 to V ⁺ +0.3 | | V |
| Total Power Dissipation ^{Note4} | P _T | 550 | | mW |
| Output Short Circuit Duration ^{Note5} | | indefinite | | s |
| Operating Ambient Temperature | T _A | -40 to +85 | -20 to +80 | °C |
| Storage Temperature | T _{stg} | -55 to +125 | | °C |

- [Note]
- Note that reverse connections of the power supply may damage the ICs.
 - The input terminal must be applied within the input voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp input voltage must operate within the electrical characteristics range of input common-mode voltage.
 - The output terminal must be applied within the output voltage range to avoid deteriorating or damaging the device characteristic. Do not exceed the ratings including during transition state such as ON/OFF, etc. The Op-Amp output voltage must operate within the electrical characteristics range of maximum output voltage.
 - This is the value at T_A ≤ +25 °C. De-rate value at -5.5 mW/°C when T_A > 25 °C.
 - Please use the total loss and the de-rating value from Note 4.

RECOMMENDED OPERATING CONDITIONS

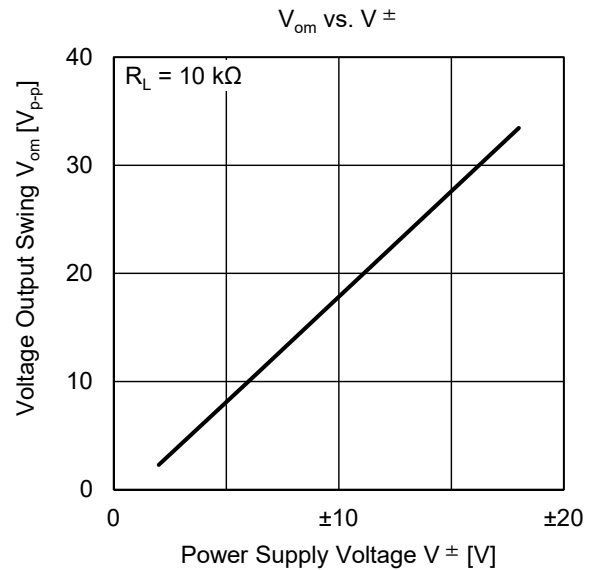
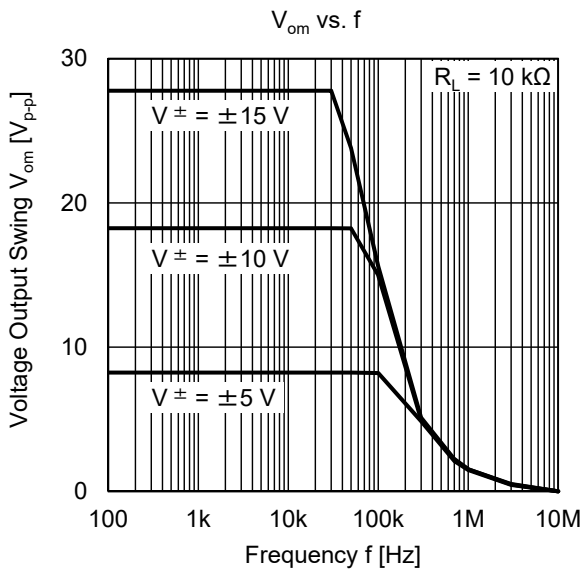
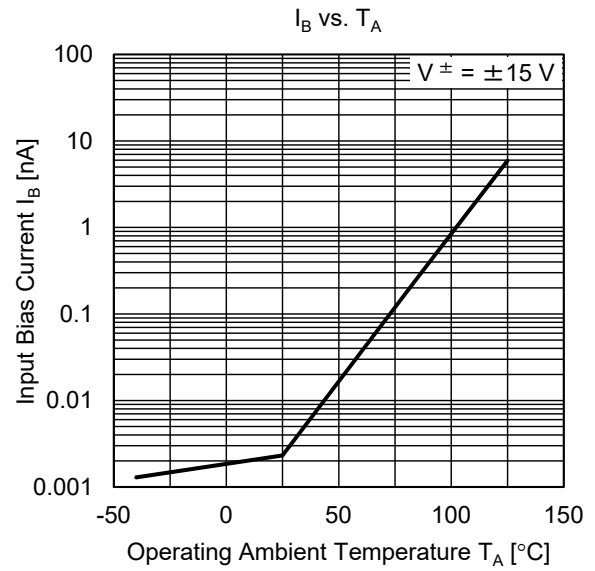
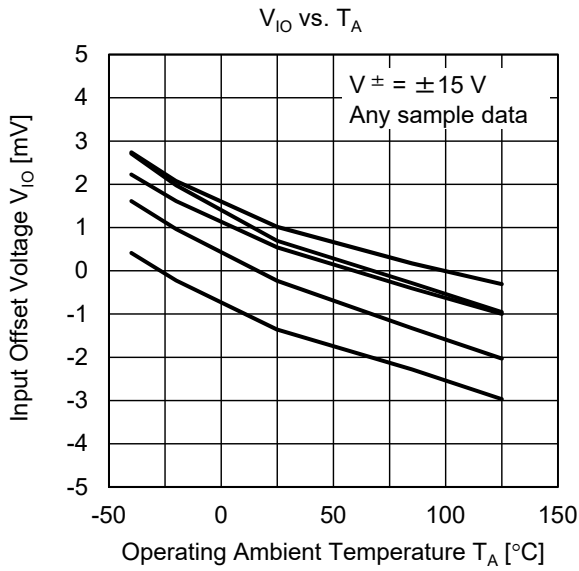
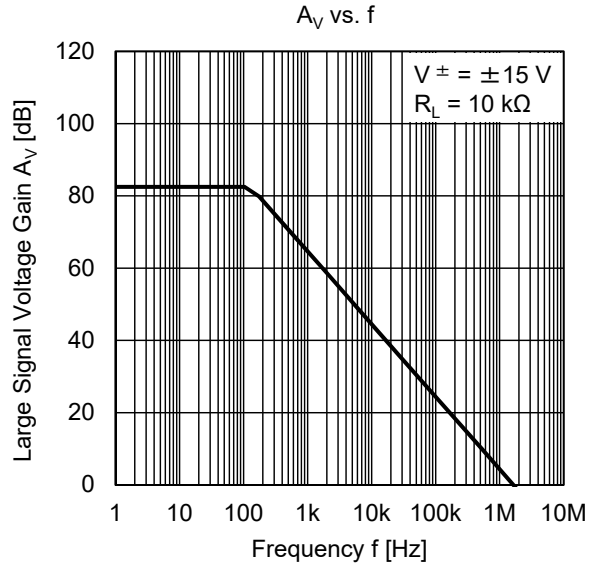
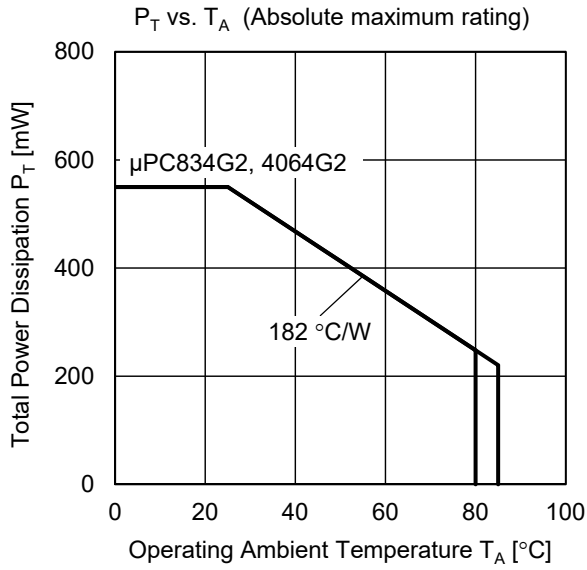
| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT |
|---|-----------------------|------|------|------|------|
| Power Supply Voltage | V [±] | ±2 | | ±16 | V |
| Output Current (SOURCE) | I _{O SOURCE} | | | 5 | mA |
| Output Current (SINK) | I _{O SINK} | | | 3.5 | mA |
| Load Capacitance (When A _V = +1) | C _L | | | 100 | pF |

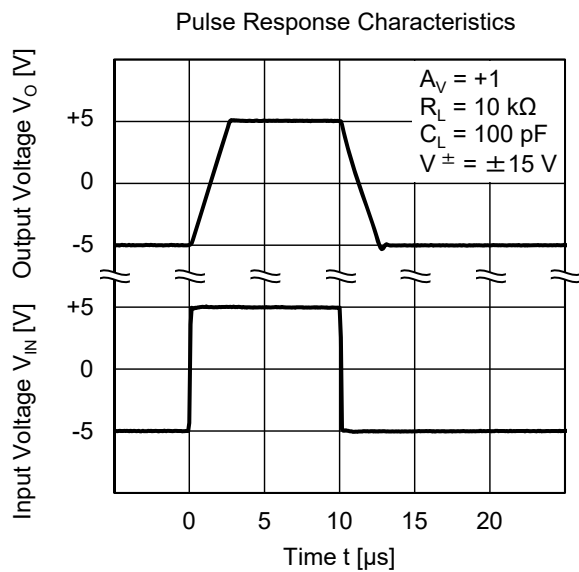
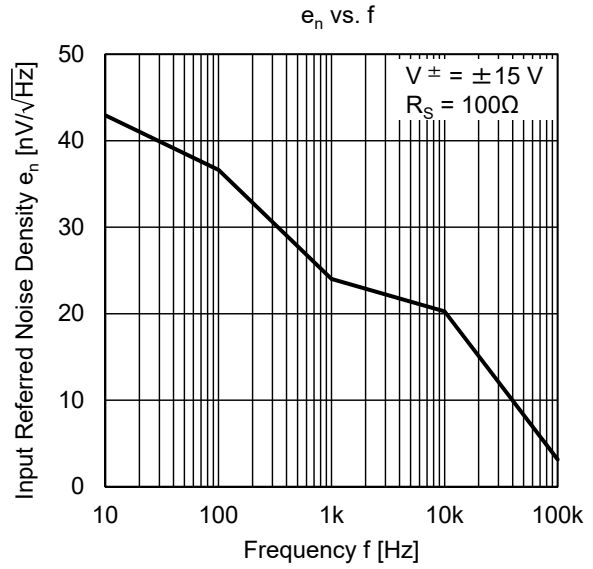
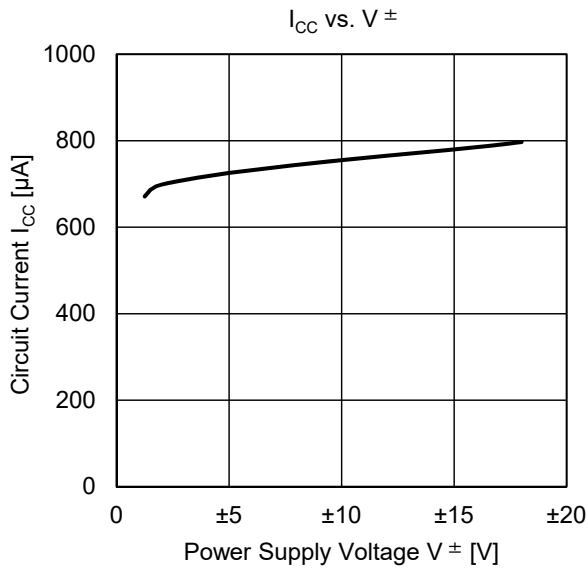
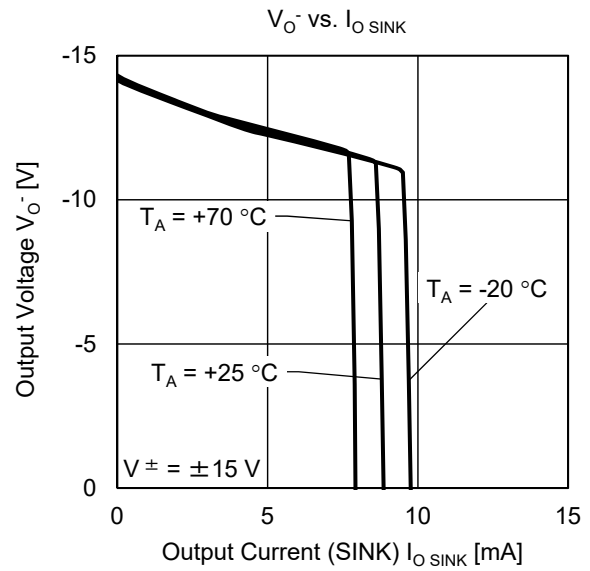
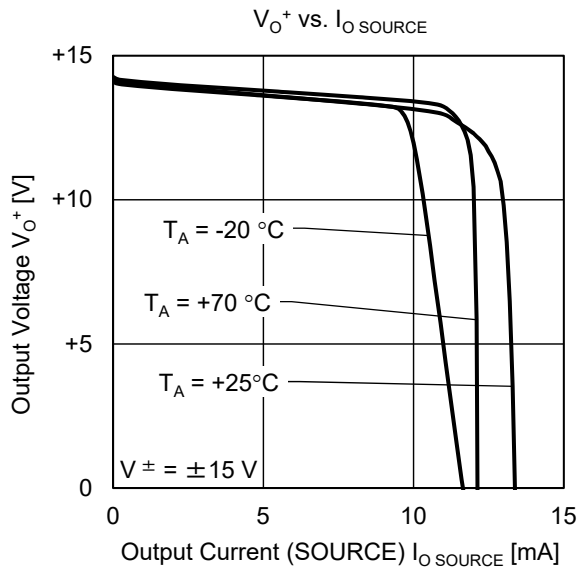
ELECTRICAL CHARACTERISTICS (T_A = 25 °C, V[±] = ±15 V)

| PARAMETER | SYMBOL | MIN. | TYP. | MAX. | UNIT | TEST CONDITION |
|---|----------------------|------|----------------|------|------------|---|
| Input Offset Voltage | V _{IO} | | ±2 | ±10 | mV | R _S ≤ 50 Ω |
| Input Offset Current | I _{IO} | | ±5 | ±50 | pA | |
| Input Bias Current ^{Note6} | I _B | | 10 | 100 | pA | |
| Large Signal Voltage Gain | A _V | 3000 | 9000 | | | R _L ≥ 10 kΩ, V _O = ±10 V |
| Circuit Current ^{Note7} | I _{CC} | | 800 | 1000 | μA | I _O = 0 A |
| Common Mode Rejection Ratio | CMR | 70 | 90 | | dB | |
| Supply Voltage Rejection Ratio | SVR | 70 | 90 | | dB | |
| Voltage Output Swing | V _{om} | ±12 | +14.0 -13.6 | | V | R _L ≥ 10 kΩ |
| Input Common-Mode Voltage Range | V _{ICM} | ±12 | +15 -13 | | V | |
| Slew Rate | SR | | 3 | | V/μs | A _V = 1 |
| Unity Gain Frequency | f _{unity} | | 1 | | MHz | |
| Input Referred Noise Voltage Density | e _n | | 30 | | nV/ √Hz | R _S = 100 Ω, f = 1 kHz |
| Channel Separation | | | 120 | | dB | |
| Input Offset Voltage | V _{IO} | | | ±15 | mV | R _S ≤ 50 Ω, T _A = -20 to +70 °C |
| Average V _{IO} Temperature Drift | ΔV _{IO} /ΔT | | ±10 | | μV/°C | T _A = -20 to +70 °C |
| Input Offset Current | I _{IO} | | | ±2 | nA | T _A = -20 to +70 °C |
| Input Bias Current ^{Note6} | I _B | | | 3.5 | nA | T _A = -20 to +70 °C |

- [Note] 6. The direction of the input bias current is the same direction that flows into the IC because the first stage is comprised of Pch J-FET. When T_J = 25 °C or higher, it increases exponentially with increase in temperature (please see I_B vs. T_A characteristics). During measurement, please kindly take care of T_J ≅ T_A
7. It is the current that flows into the internal circuit. This current flow is irrespective of the channel usage.

ELECTRICAL CHARACTERISTICS CURVE (T_A = 25 °C, TYP.) (REFERENCE VALUE)

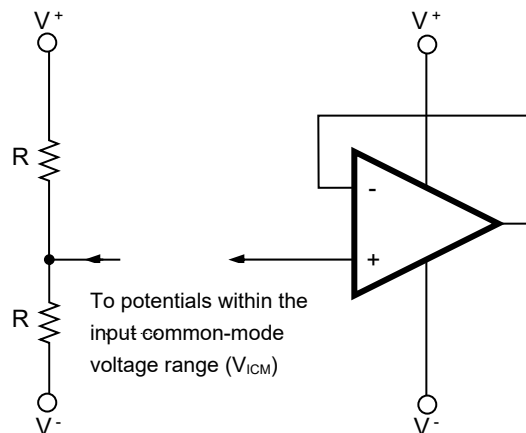




USE WITH PRECAUTIONS

- Managing unused circuits
If there is an unused circuit, the following connection is recommended.

Example of handling unused circuit



Note in this example, an intermediate voltage of V^+ and V^- is applied.

- Power Supply (Dual Power Supply / Single Power Supply)**

The op-amp operates when a predetermined voltage is applied between V^+ to V^- . Therefore, while it operates from a single power supply ($V^- = \text{GND}$), it is not possible to operate the input and output near GND. So please be careful of the common-mode input voltage range and maximum output voltage.

- Ratings of input/output pin voltage**

When the voltage of input/output pin exceeds the absolute maximum rating, the parasitic diode within the IC may conduct, causing characteristics degradation or damage. In addition, if the voltage of input pin is lower than V^- , or the voltage of output pin exceeds the power supply voltage, it is recommended to make a clamping circuit using a diode with low forward voltage (e.g.: Schottky diode) as protection.

- Input common-mode voltage range**

When the supply voltage does not meet the condition of electrical characteristics, the input common-mode voltage range is as follows.

$$V_{ICM} \text{ (TYP.): } V^- + 2 \text{ to } V^+ \text{ [V] (} T_A = 25 \text{ }^\circ\text{C)}$$

During designing, do include some margin by considering characteristic variations, temperature characteristics etc.

- Maximum Output Voltage**

When the supply voltage does not meet the condition of electrical characteristics, the TYP. value range of the maximum output voltage is as follows:

$$V_{om}^+ \text{ (TYP.): } V^+ - 1 \text{ [V] (} T_A = 25 \text{ }^\circ\text{C)}, V_{om}^- \text{ (TYP.): } V^- + 1.4 \text{ [V] (} T_A = 25 \text{ }^\circ\text{C)}$$

During designing, do include some margin by considering characteristic variations, temperature characteristics and so on. In addition, also note that the output voltage range (V_{om}^+ to V_{om}^-) will become narrow when the output current increases.

- Handling of ICs**

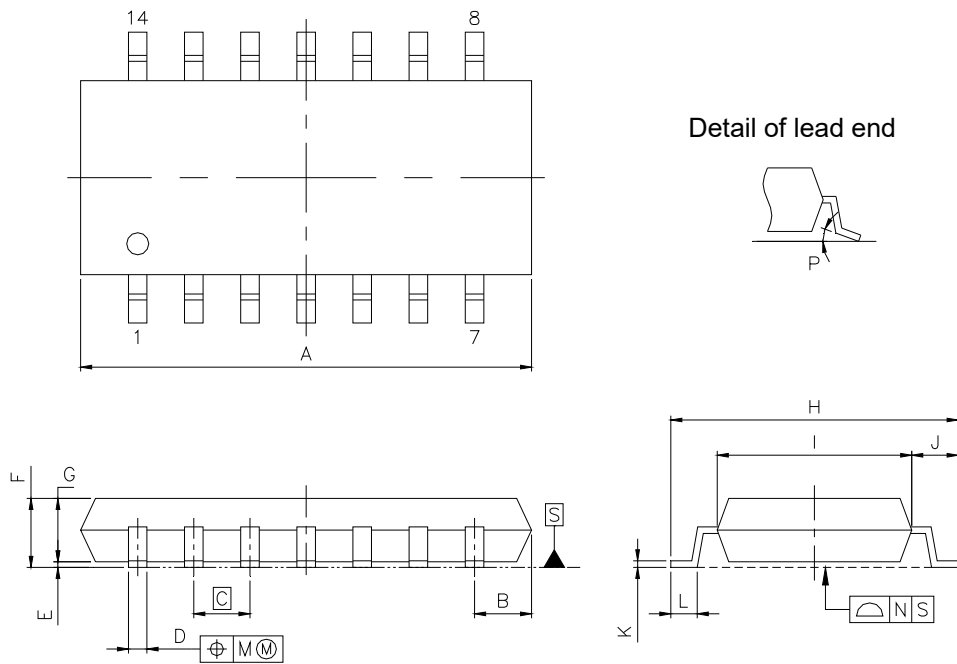
When stress is added to the ICs due to warpage or bending of a board, the characteristic may fluctuate due to piezoelectric (piezo) effect. Therefore, pay attention to warpage or bending of a board.

PACKAGE DRAWINGS

14-PIN PLASTIC SOP

| JEITA Package code | RENESAS code | Previous code | MASS (TYP.) [g] |
|--------------------|--------------|---------------|-----------------|
| P-SOP14-0225-1.27 | PRSP0014DI-A | P14GR-50-225B | 0.14 |

Unit: mm

**NOTE**

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

| ITEM | MILLIMETERS |
|------|--|
| A | 10.2 ±0.26 |
| B | 1.42 MAX |
| C | 1.27 (T.P.) |
| D | 0.42 ^{+0.08} _{-0.07} |
| E | 0.1 ±0.1 |
| F | 1.59 ^{+0.21} _{-0.2} |
| G | 1.49 |
| H | 6.5 ±0.2 |
| I | 4.4 ±0.1 |
| J | 1.1 ±0.16 |
| K | 0.17 ^{+0.08} _{-0.07} |
| L | 0.6 ±0.2 |
| M | 0.1 |
| N | 0.10 |
| P | 3° ^{+7°} _{-3°} |

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