To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD16443B

192-OUTPUT TFT-LCD SOURCE DRIVER (8 gray scales)

DESCRIPTION

The μPD16443B is a TFT-LCD source driver that can display eight gray scales. Digital data of 3 × 3 bits is input to this source driver, which is ideal for the displays of office machines. The μPD16443B internally consists of a 64 × 9 bit data register, 192 × 3 bit latch, and 192 8-value driver circuits. The output driver selects one of eight external power sources for output, according to the input data. With a panel having a color filter consisting of RGB vertical stripes, the μPD16443B can display as many as 512 colors.

FEATURES

- High-speed data transfer (f_{CLK} = 15 MHz MAX.)
- 3 bit (tone data) × 3 dot (RGB) input
- 8-value output function selecting one of eight external power sources
- Bidirectional data store function
- High output voltage: 20 V MAX.
- Suitable for high-density mounting (TCP)

Differences from the μPD16423:

- Shift register auto clear function added (Refer to description of CLK function in PIN FUNCTION.)
- Active edge of $\overline{\text{RESET}}$ changed (high → low active)

ORDERING INFORMATION

Part number	Package
μPD16443BN-×××	TCP (TAB package)
μPD16443BN-051	Standard TCP (180 μm pitch)

The TCP package is a custom model. For details, consult NEC.

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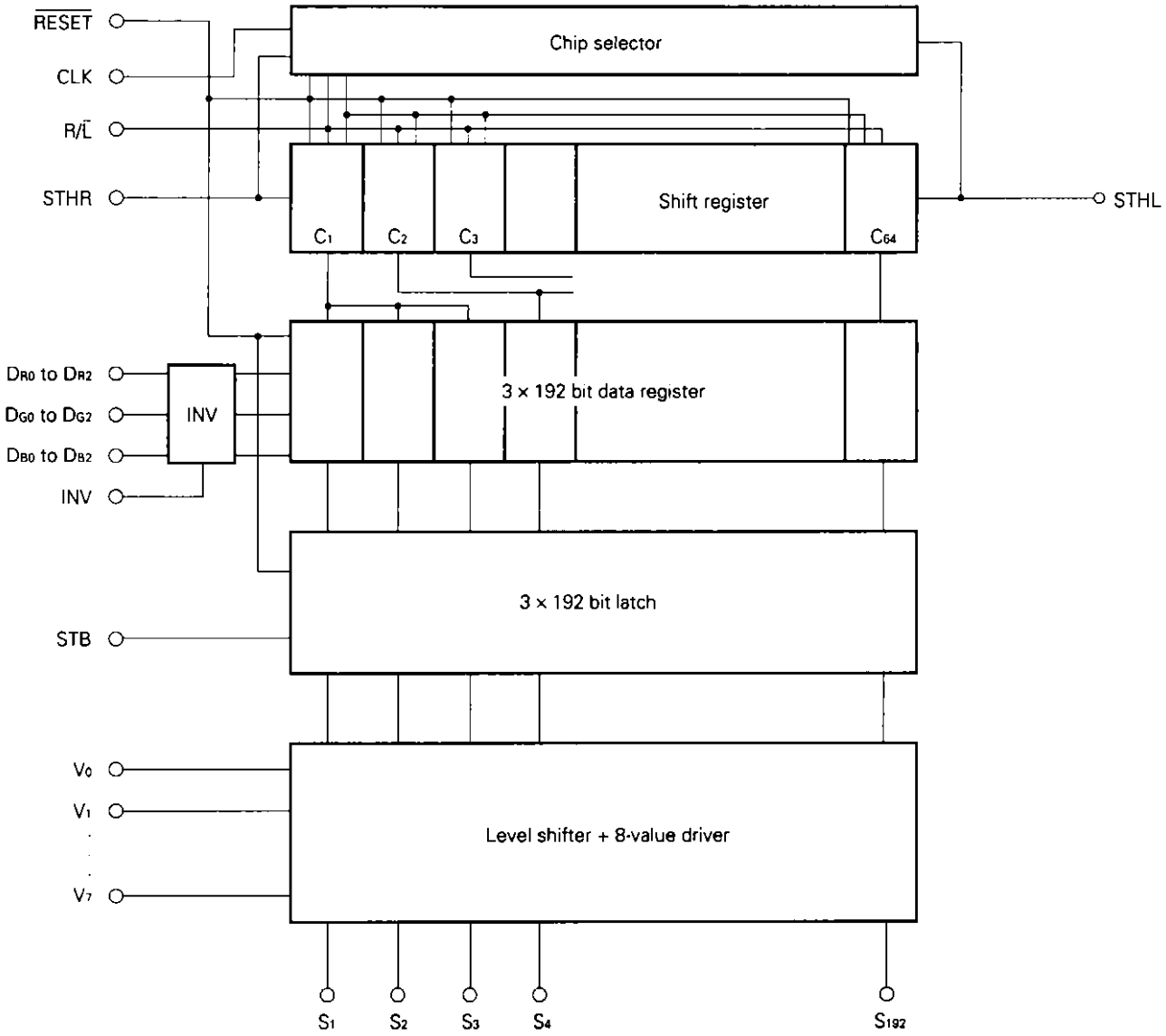
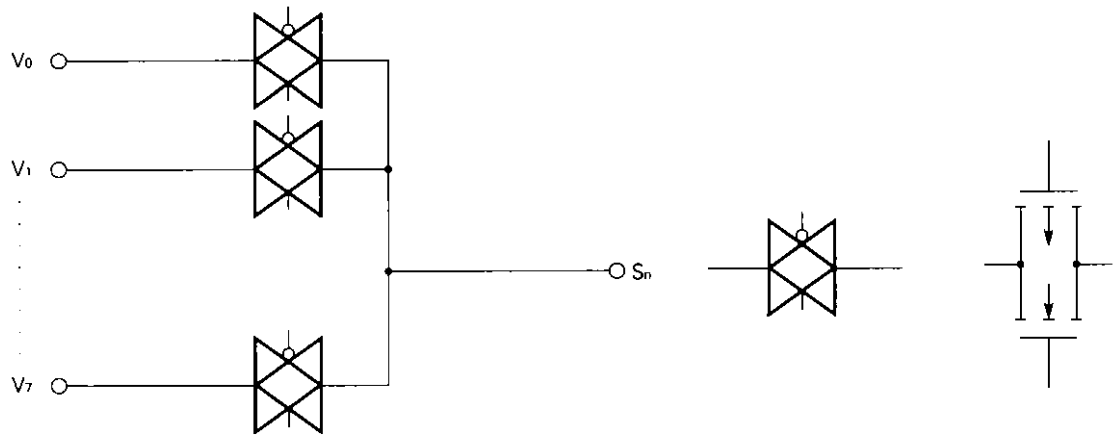
Date Published February 1995
Printed in Japan

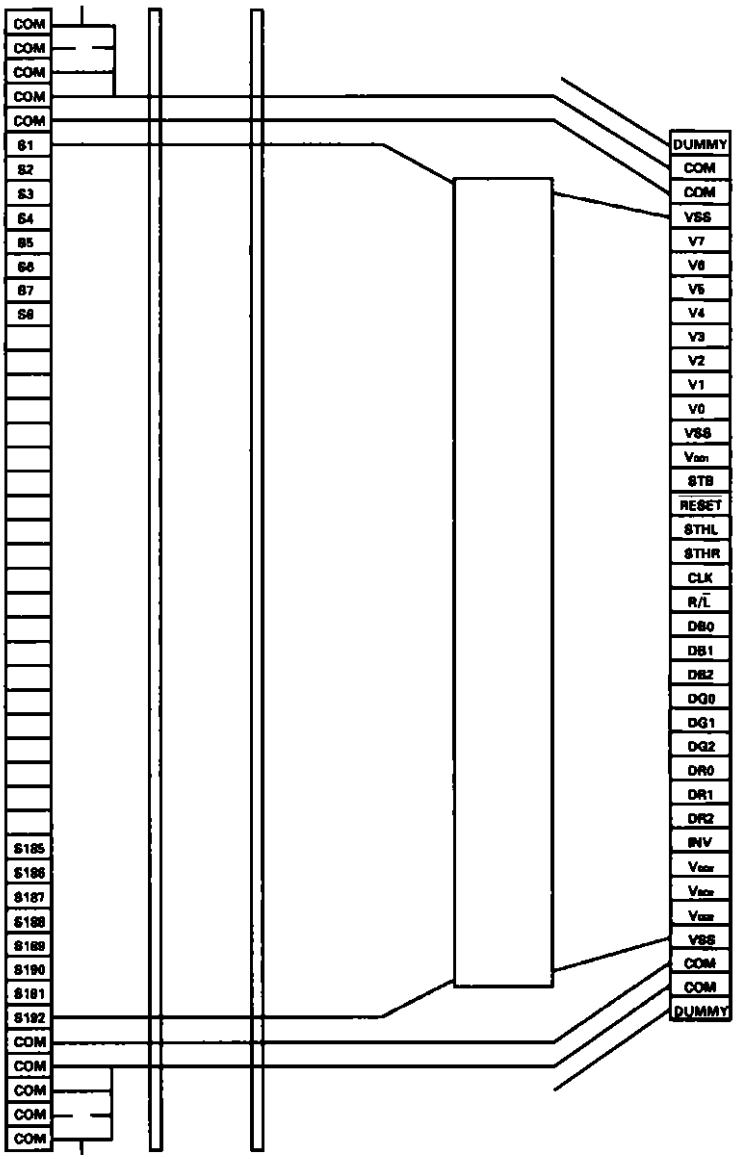
BLOCK DIAGRAM



EQUIVALENT CIRCUIT OF 8-VALUE DRIVER



STANDARD TCP PIN CONFGURATION (μPD16443BN-051)



Top view of copper foil

Caution: This figure does not specify the dimensions of TCP.

PIN FUNCTIONS

Pin Symbol	Pin Name	Description
S_1 to S_{192}	Driver output	Output one of the V_0 to V_7 levels
D_{R0} to D_{R2}	R data input	Input 9-bit data consisting of gray scale data (3 bits) × 3 (pixels RGB)
D_{G0} to D_{G2}	G data input	
D_{B0} to D_{B2}	B data input	
INV	Positive polarity inverting input	Input data is inverted and stored in data register when INV = H. However, data already stored is not affected.
R/$\overline{L}$	Shift direction select input	R/$\overline{L}$ = H: STHR input, $S_1 \rightarrow S_{192}$, STHL output R/$\overline{L}$ = L: STHL input, $S_{192} \rightarrow S_1$, STHR output
CLK	Clock input	Data input clock. Data is read to data register at falling edge of this clock. When start pulse is not input, contents of shift register are automatically cleared at rising edge of the 64th pulse after input of latch pulse. Start pulse output goes high at rising edge of 64th pulse, serving as start pulse for next stage. Output of start pulse goes low at rising edge of 65th pulse.
STHR	Right shift start pulse I/O	R/$\overline{L}$ = H: start pulse input pin R/$\overline{L}$ = L: start pulse output pin
STHL	Left shift start pulse I/O	R/$\overline{L}$ = H: start pulse output pin R/$\overline{L}$ = L: start pulse input pin
STB	Latch pulse input	Contents of data register are transferred to latch when STB = H, and tone level selected by gray scale data is output from driver output
$\overline{RESET}$	Reset input	Shift register, chip select circuit, and latch circuit are reset when this pin goes low. Be sure to reset the μPD16443B once when power is applied.
V_0 to V_7	Tone level power	$V_{SS2} \leq V_0$ to $V_7 \leq V_{DD2} - 1$ V
V_{DD1}	Logic power	5 V ± 5 %
V_{DD2}	Driver power	18 V MAX. (operating)
V_{SS1}	Logic ground	Connected to system ground
V_{SS2}	Driver ground	Connected to system ground

CORRESPONDENCE BETWEEN DATA INPUT AND DATA OUTPUT

Data format: 1 pixel data (3 bits) × RGB (3 bits) Input width: 9 bits

(1) R/$\overline{L}$ = H (right shift)

Output	S_1	S_2	S_3	.....	S_{19}
Data	D_{R0} D_{R1} D_{R2}	D_{G0} D_{G1} D_{G2}	D_{B0} D_{B1} D_{B2}	.....	D_{B0} D_{B1} D_{B2}

(2) R/$\overline{L}$ = L (left shift)

Output	S_{192}	S_{191}	S_{190}	.....	S_1
Data	D_{R0} D_{R1} D_{R2}	D_{G0} D_{G1} D_{G2}	D_{B0} D_{B1} D_{B2}	.....	D_{B0} D_{B1} D_{B2}

TONE LEVEL POWER SELECTION

Data			Driver Output	
D_{X0}	D_{X1}	D_{X2}	INV = L	INV = H
0	0	0	V_0	V_7
1	0	0	V_1	V_6
0	1	0	V_2	V_5
1	1	0	V_3	V_4
0	0	1	V_4	V_3
1	0	1	V_5	V_2
0	1	1	V_6	V_1
1	1	1	V_7	V_0

Caution The driver output is fixed to V_7 at reset, regardless of the level of the INV pin and data.

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Ratings	Unit
Logic Supply Voltage	V_{DD1}	−0.5 to +7.0	V
Logic Input Voltage	V_{IN}	−0.5 to V_{DD1}+0.5	V
Logic Output Voltage	V_{O1}	−0.5 to V_{DD1}+0.5	V
Driver Supply Voltage	V_{DD2}	−0.5 to +20	V
Driver Input Voltage	V_0 to V_7	−0.5 to V_{DD2}+0.5	V
Driver Output Voltage	V_{O2}	−0.5 to V_{DD2}+0.5	V
Driver Output Current	I_{O2}	±10	mA
Operating Temperature Range	T_A	−20 to +70	°C
Storage Temperature Range	T_{stg}	−40 to +125	°C

RECOMMENDED OPERATING RANGE (T_A = −20 to +70 °C, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}	4.75	5.0	5.25	V
High-Level Input Voltage	V_{IH}	0.7·V_{DD1}		V_{DD1}	V
Low-Level Input Voltage	V_{IL}	0		0.2·V_{DD1}	V
Driver Supply Voltage	V_{DD2}			18	V
Driver Input Voltage	V_0 to V_7	V_{SS}		V_{DD2} −1	V
Driver Output Voltage	V_{O2}	V_{SS}		V_{DD2} −1	V

Caution 1. Be sure to satisfy the following condition: $V_{SS} \le V_0$ to $V_7 \le V_{DD2} - 1$

2. Turn on power to V_{DD1}, logic signal, V_{DD2}, and V_0 to V_7 in this order. Turn off power in the reverse order.

ELECTRICAL CHARACTERISTICS (T_A = −20 to +70 °C, V_{DD1} = 5 V ±5 %, V_{DD2} = 18 V, V_{SS1} = V_{SS2} = 0 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
High-Level Output Voltage	V_{OH1}	Logic I_{OH1} = −1 mA	0.9·V_{DD}			V
Low-Level Output Voltage	V_{OL1}	Logic I_{OL1} = 1 mA			0.1·V_{DD1}	V
Driver Output ON Resistance	R_{ON}	$\lvert I_{O2} \rvert$ = 100 μA			5.0	kΩ
Logic Input Current	I_{IHL}	V_{IN} = V_{DD1} or V_{SS}			±1	μA
High-Level Input Voltage	V_{IH}		0.7·V_{DD1}			V
Low-Level Input Voltage	V_{IL}				0.2·V_{DD1}	V
Static Current Consumption	I_{DD1}	V_{DD1} pin, no load			40	μA
	I_{DD2}	V_{DD2} pin, no load			100	μA

SWITCHING CHARACTERISTICS

(T_A = –20 to +70 °C, V_{DD1} = 5 V ±5 %, V_{DD2} = 18 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6 ns)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Output Delay Time	t_{PHL1}	C_L = 20 pF	10		30	ns
	t_{PLH1}	C_L = 20 pF	10		30	ns
Driver Output Delay Time	t_{PHL2}	C_L = 300 pF			3	μs
	t_{PLH2}				3	μs
	t_{PHL3}	C_L = 300 pF			8	μs
	t_{PLH3}				8	μs
Maximum Clock Frequency	$f_{max.}$	Duty = 50 %, in cascade connection	15			MHz
Input Capacitance	C_{I1}	Logic other than STRH, STRL			15	pF
	C_{I2}	STRH, STRL			20	pF

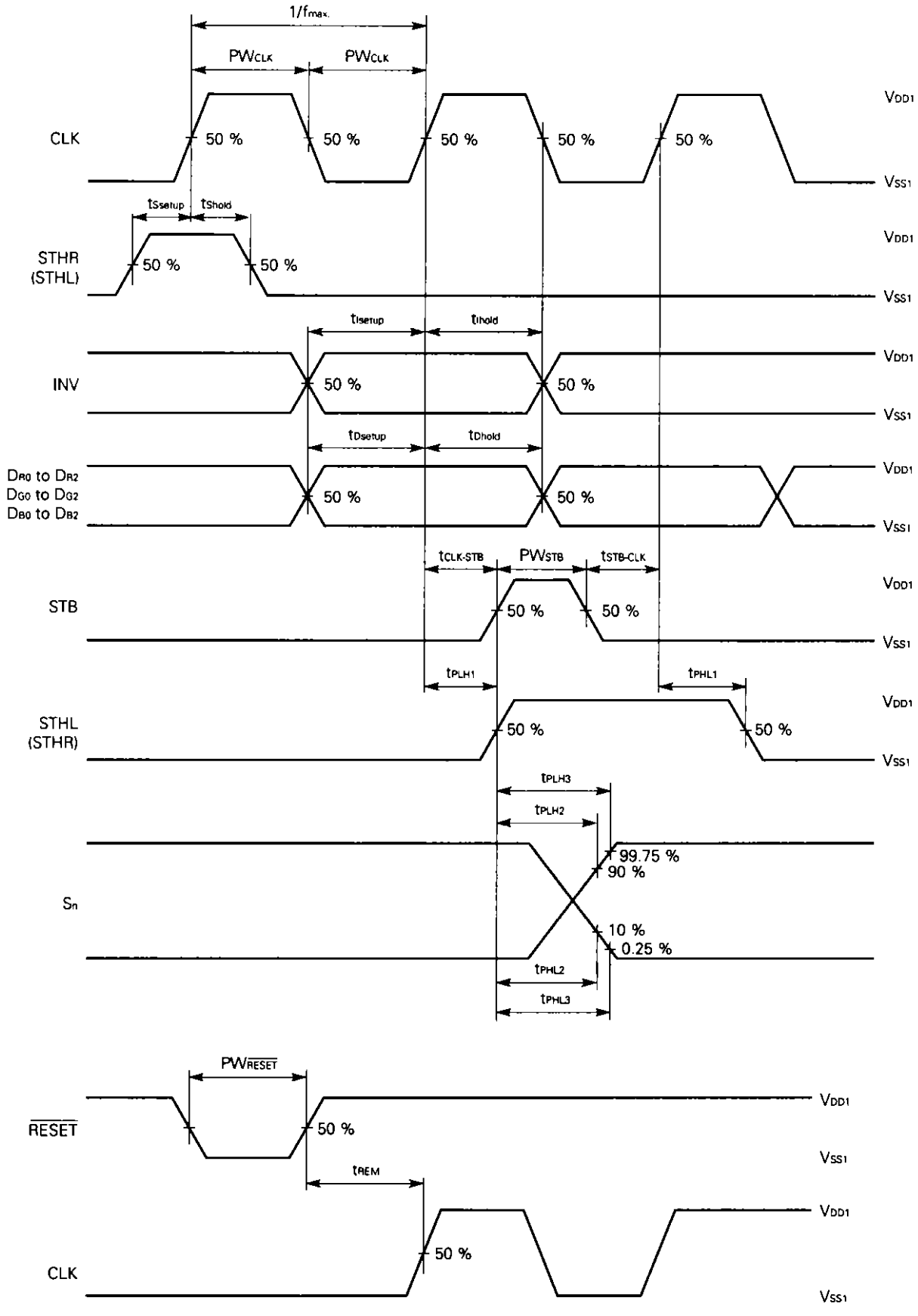
TIMING REQUIREMENTS

(T_A = –20 to +70 °C, V_{DD1} = 5 V ±5 %, V_{DD2} = 18 V, V_{SS1} = V_{SS2} = 0 V, t_r = t_f = 6 ns)

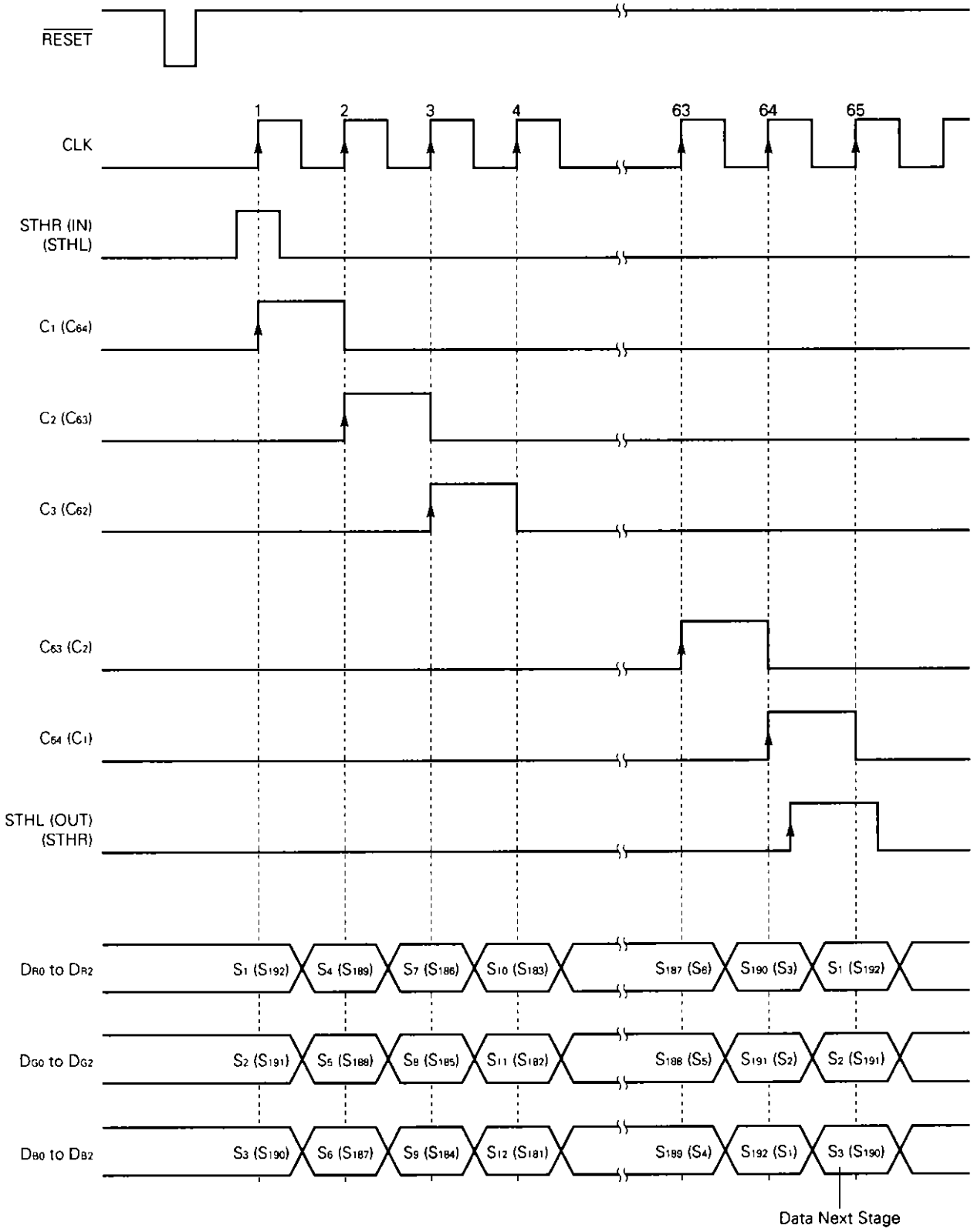
Parameter	Symbol	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLK}	30			ns
Strobe Pulse Width	PW_{STB}	30			ns
Reset Pulse Width	$PW_{\overline{RESET}}$	100			ns
Start Pulse Setup Time	t_{Ssetup}	30			ns
Start Pulse Hold Time	t_{Shold}	10			ns
Data Setup Time	t_{Dsetup}	30			ns
Data Hold Time	t_{Dhold}	30			ns
INV Setup Time	t_{Isetup}	30			ns
INV Hold Time	t_{Ihold}	30			ns
Reset Removal Time	t_{REM}	50			ns
Clock Strobe Time Interval	$t_{CLK-STB}$	30			ns
Strobe Clock Time Interval	$t_{STB-CLK}$	0			ns

Remark For the specifications of t_r and t_f, refer to SWITCHING CHARACTERISTIC WAVEFORMS.

SWITCHING CHARACTERISTIC WAVEFORMS



TIMING CHART



Caution Be sure to input one reset pulse when power is applied. When data is not stored for all outputs (there are some extra outputs), reset the μPD16443B before data transfer.

RECOMMENDED MOUNTING CONDITIONS

The following mounting conditions for the μPD16443B are recommended.
For any other mounting conditions, consult NEC.

Mounting Conditions	Mounting Method	Conditions
Thermocompression	Soldering	Heating tool: 300 to 350 °C, Time: 2 to 3 seconds, Pressure: 100 g (per piece)
	ACF (sheet adhesive agent)	Preliminary adhesion: 70 to 100 °C, Pressure: 3 to 8 kg/cm^2, Time: 3 to 5 seconds Actual adhesion: 165 to 180 °C, Pressure: 25 to 45 kg/cm^2, Time: 30 to 40 seconds (with Sumitomo Bakelite's anisotropic film SUMIZAC1003)

Caution 1. For the mounting conditions for the ACF, consult the ACF manufacturer before using the ACF.
2. Do not use two or more mounting methods in combination.

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	IEI-1212
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207

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