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April 1st, 2010
Renesas Electronics Corporation

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RENESAS

MOS INTEGRATED CIRCUIT

μPD16447

120-OUTPUT TFT LCD SOURCE DRIVER (NAVIGATION, AUTOMOBILE LCD-TV)

DESCRIPTION

The μPD16447 is a TFT liquid crystal panel source driver. It consists of a multiplexer circuit that supports various pixel arrangements, a shift register generating sampling timing, and two sample and hold circuits that sample an analog voltage. The two sample and hold circuits alternately sample and hold an analog voltage, improving the definition on the LCD panel. Simultaneous sampling or sequential sampling mode can be automatically selected according to the pixel arrangement on the LCD panel used, so that the μPD16447 can be employed in a wide range of applications including navigation systems and automobile LCD-TVs.

FEATURES

- Common inversion supported (maximum output voltage: 7.75 V, at V_{DD2} = 12 V)
- 5-V drive (supporting 882 × 240 dots)
  f_{max} = 5 MHz, V_{DD1} = 4.5 V
- Simultaneous/sequential sampling mode automatically selected according to pixel arrangement
  (Vertical stripe mosaic arrangement; simultaneous, delta arrangement; sequential)
- Two sample and hold circuits
- Small output deviation between pins (±50 mV MAX.)
- Internal multiplexer supporting many pixel arrangements such as stripe, mosaic, and delta arrangements
- Power-save circuit
- R/L pin for left/right shift selection
- For high-density mounting

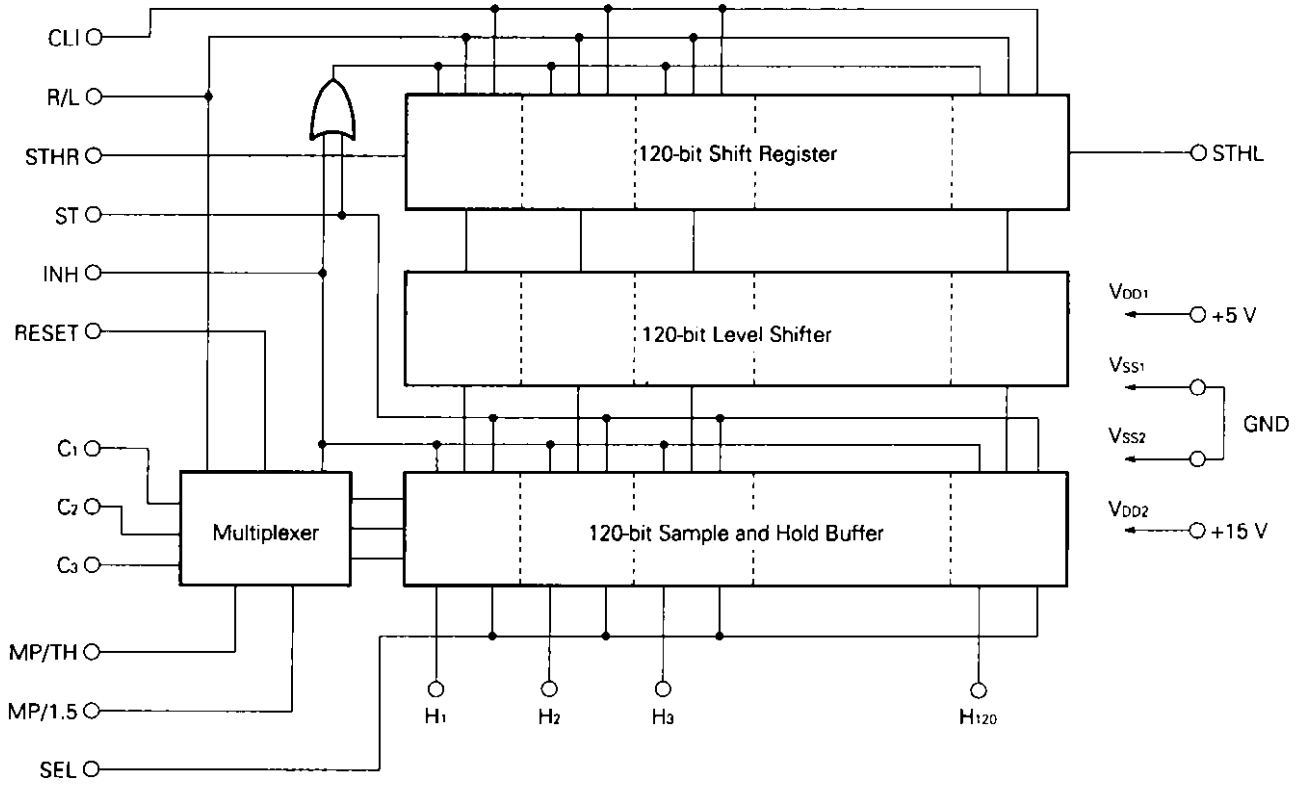
ORDERING INFORMATION

Parts Number	Package
μPD16447N-×××	TCP (TAB package)
μPD16447N-051	Standard TCP (200 μm OLB)

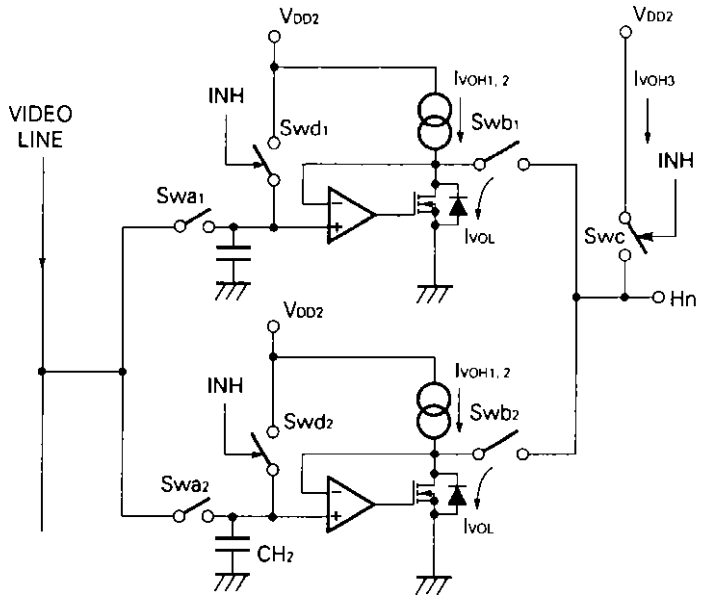
The TCP model is a custom product. For details, consult NEC.

Document No. IC-3499A
(O.D. No. IC-8932)
Date Published February 1995 P
Printed in Japan

BLOCK DIAGRAM



SAMPLE AND HOLD, AND OUTPUT CIRCUITS

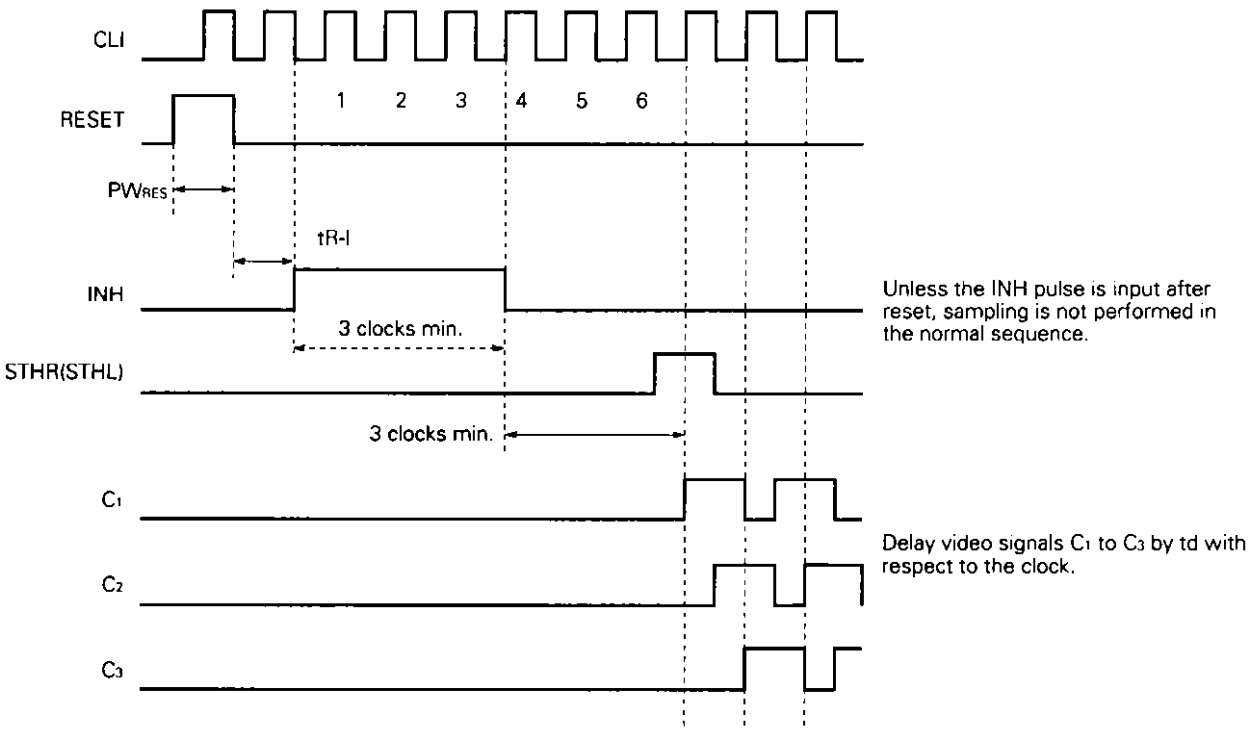


PIN FUNCTIONS

Pin Symbol	Pin Name	Description
C_1 to C_3	Video signal input	These pins input video signals R, G, and B.
H_1 to H_{120}	Video signal output	These pins output video signals, which have been sampled and held, during the horizontal period.
STHR STHL	Cascade I/O	These pins input/output the start pulse for sample and hold timing. STHR serves as the input pin and STHL serves as the output pin for right shift. For left shift, STHL serves as the input pin and STHR serves as the output pin.
SEL	Output hold current select input	This pin selects the high-level output current of the video signal (output hold current). H; I_{VOH} = –30 μA TYP. SEL = L; I_{VOH} = –8 μA TYP.
CLI	Shift clock input	The start pulse is read at rising edge of this signal. In sequential sampling mode, the sampling pulse SPn is generated at both the rising and falling edges of this signal. SPn is generated at either the rising or falling edge of this signal in simultaneous sampling mode (for details, refer to the TIMING CHART).
INH	Inhibit input	When this signal goes high, the video signal output is made high, and the pixels in the LCD panel are precharged. When it goes low, multiplexer and two sample and hold circuits are switched.
RESET	Reset input	When this signal goes high, the select counter of the multiplexer and the selectors of the two sample and hold circuits are reset. The multiplexer is turned off once it has been reset. Therefore, be sure to input one INH pulse before inputting a video signal. If a video signal is input without the INH pulse, sampling is not executed.
ST	Power-save input	When this signal goes high, all output video signals are made high, reducing the bias current of the analog circuit (during the vertical retrace line period).
MP/TH	Multiplexer selector input (1)	By using MP/TH and MP/1.5 in combination, the following three color filter arrangements can be supported: Mode / MP/TH / MP/1.5 Mosaic Arrangement / H / L Delta Arrangement / H / H Vertical Stripe Arrangement / L / L With the vertical stripe or mosaic arrangement, sampling is executed at the same time as video signal input/output. With the delta arrangement, sampling is sequentially executed. Do not select the combination of MP/TH = L and MP/1.5 = H.
MP/1.5	Multiplexer selector input (2)	
R/L	Shift direction select input	R/L = H; right shift: STHR → H_1 → H_{120} → STHL R/L = L; left shift: STHL → H_{120} → H_1 → STHR
V_{DD1}	Logic power	5 V ±10 %
V_{DD2}	Driver power	12 V
V_{SS}	Ground	Connect this pin to system ground.
$TEST_1$ to $TEST_3$	Test pins	Fix these pins to the L level.

Cautions

1. **Turn on power to V_{DD1}, logic input, V_{DD2}, and video signal input in this order, to prevent latchup. Turn off power in the reverse order. Observe this power sequence even during a transitional period.**
2. **The delay time of the clock and internal sampling pulse SHPn are designed to be about 15 to 30 ns (at V_{DD1} = 5 V, 25 °C). Delay the video input signal from the clock by this delay time.**
3. **Never change the video input signal during one sampling period. The maximum frequency of the video input of this product is 3.3 MHz. If a video signal with a higher frequency is input, the data may not be correctly displayed.**
4. **Insert a capacitor of 0.1 to 1 μF between V_{DD1} and V_{SS}, and V_{DD2} and V_{SS}. Unless the power supply is reinforced, the supply voltage may fluctuate, making the sampling voltage abnormal.**
5. **If noise is superimposed on the start pulse pin, the data may not be correctly displayed. For this reason, be sure to input the reset signal during the vertical blanking period.**
6. **If the start pulse width is extended by half the clock or longer, the sampling start timing SPH1 does not change from the normal timing; therefore, the sampling operation is performed normally.**
7. **The μPD16447 is designed to have logic frequency $f_{max.}$ = 5 MHz (5 V ±10%) on the assumption that it is used to drive an LCD panel of non-interlace, comb wiring with a maximum number of dots of 882 × 240. If this product is used with an LCD panel having a greater dot size, the LCD panel may malfunction or its display quality may be degraded.**
8. **The maximum operating temperature of this product is +85 °C. If this limit is exceeded, the REF value (output voltage) tends to decrease abruptly.**
9. **Recommended timing: For tR-I and PW_{RES}, refer to ELECTRICAL CHARACTERISTICS.**
   (The timing of the video signal inputs C_1 to C_3 is in sequential sampling mode.)



FUNCTIONAL DESCRIPTION

1. Multiplexer

This circuit selects video signals R, G, and B input to C_1, C_2, and C_3, respectively, according to the pixel arrangement of the LCD panel, and outputs the signals to H_1 through H_{120}. Vertical stripe, delta, or mosaic arrangement can be selected by using the MP/TH and MP/1.5 pins in combination.

(1) VERTICAL STRIPE ARRANGEMENT MODE (MP/TH = L, MP/1.5 = L)

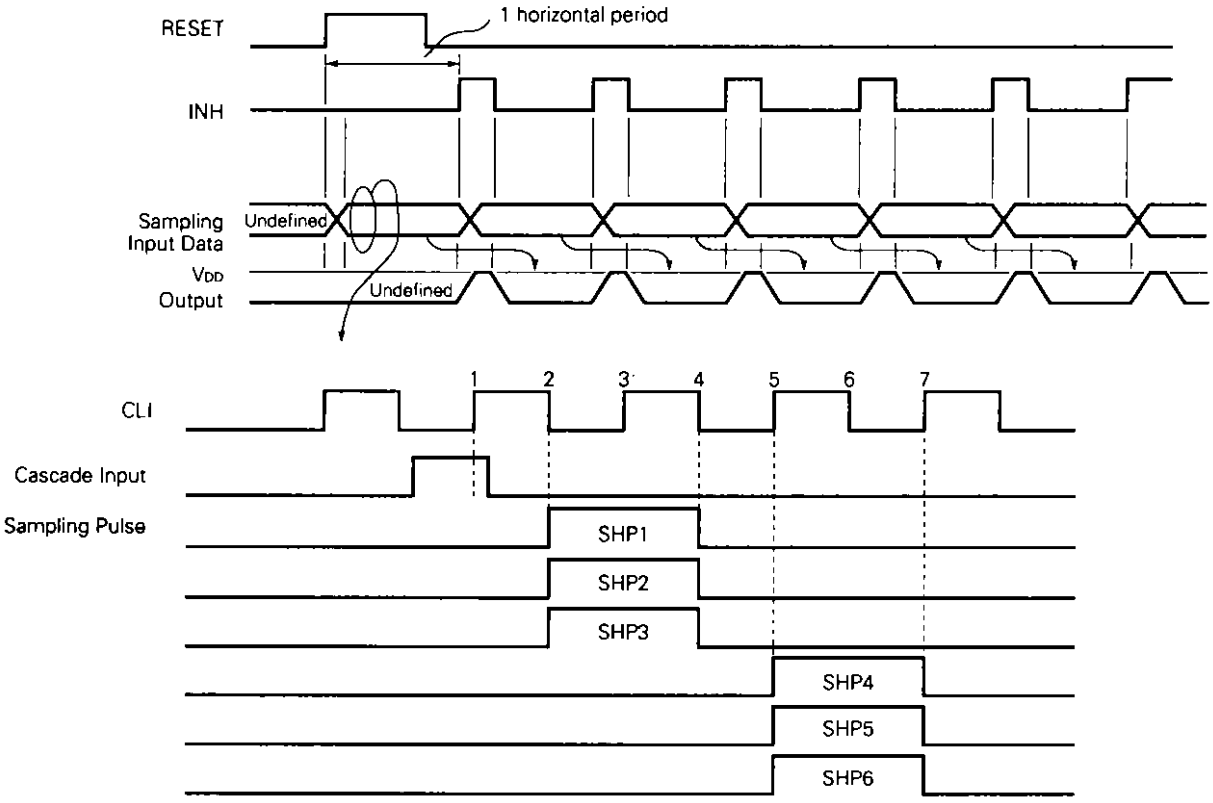
In this mode, the relation between the video signals C_1, C_2, and C_3, and output pins is as shown below. This mode is used to drive an LCD panel in the vertical stripe arrangement. In this mode, the multiplexer circuit is in the through state.

Relations between video signals C_1, C_2, and C_3, and output pins

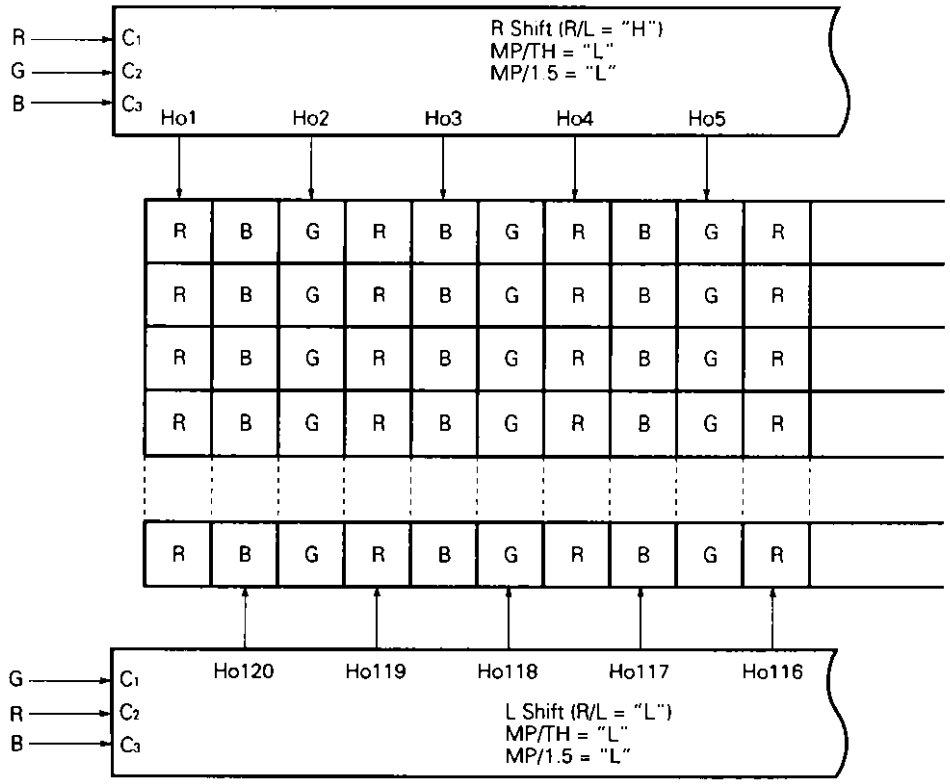
Line No. (No. of INHs)	RESET	INH	H_1 (H_{120})	H_2 (H_{119})	H_2 (H_{118})	H_2 (H_{117})		H_{119} (H_2)	H_{120} (H_1)
0	H	L	Undefined	→	→	→		→	→
1	L	L	Output C_1 (C_3)	Output C_2 (C_2)	Output C_3 (C_1)	Output C_1 (C_3)		Output C_2 (C_2)	Output C_3 (C_1)
2	L	L	Output C_1 (C_3)	Output C_2 (C_2)	Output C_3 (C_1)	Output C_1 (C_3)		Output C_2 (C_2)	Output C_3 (C_1)
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮

( ): for left shift

TIMING CHART



EXAMPLE OF MULTIPLEXER OPERATION IN STRIPE ARRANGEMENT MODE



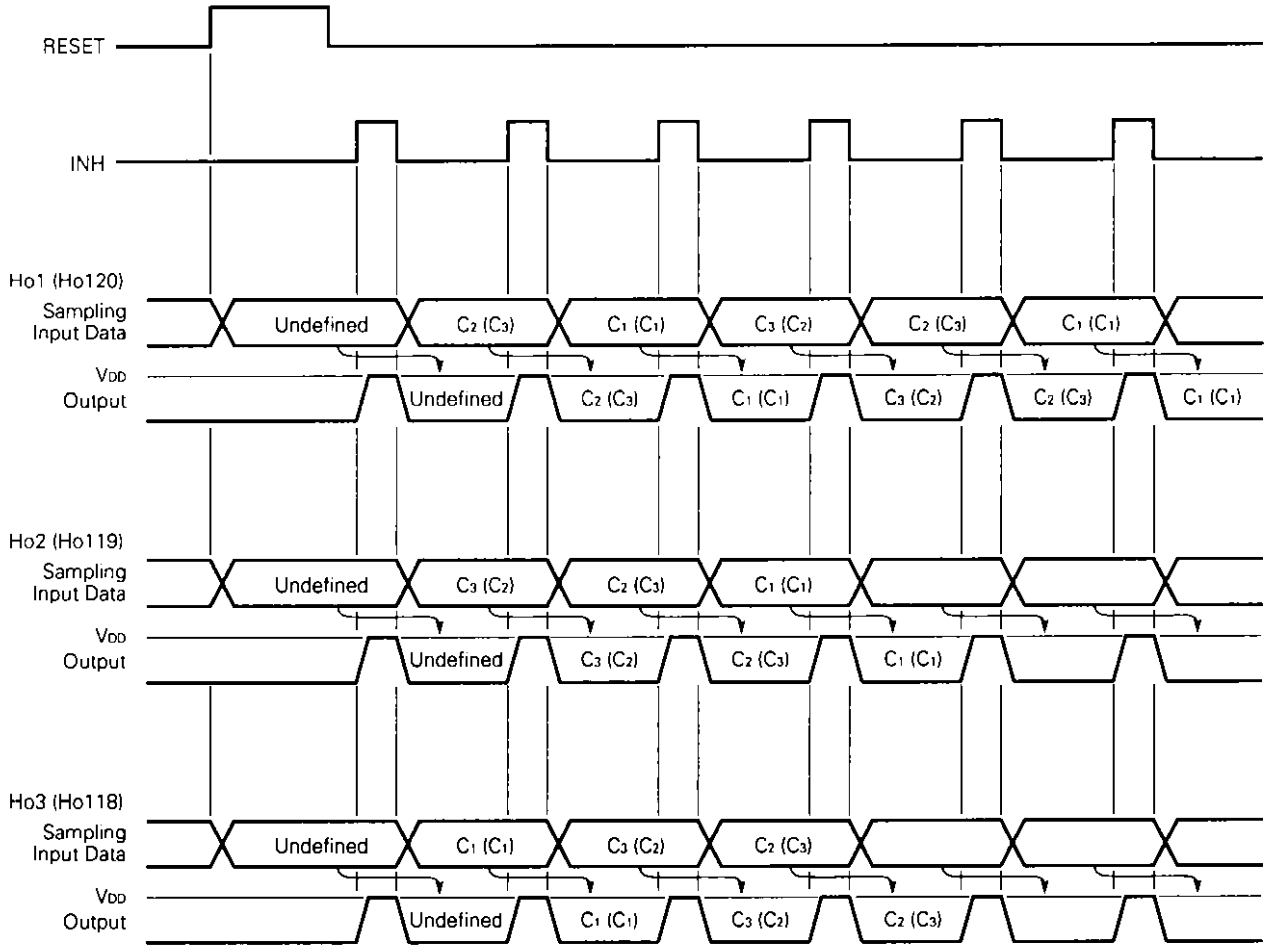
(2) DELTA ARRANGEMENT MODE (MP/TH = H, MP/1.5 = H)

Relations between video signals C_1, C_2, and C_3, and output pins

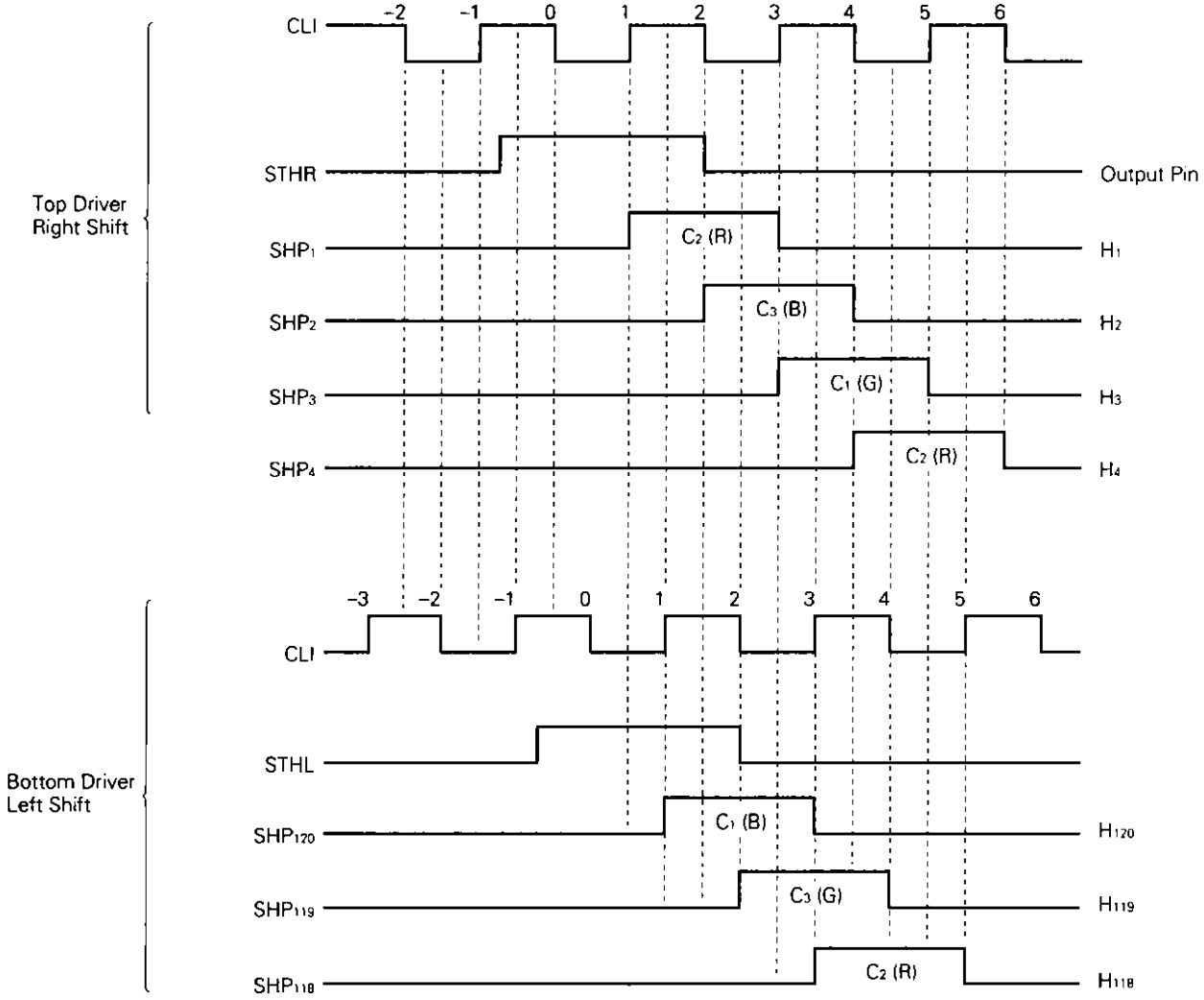
Line No. (No. of INHs)	RESET	INH	H_1 (H_{120})	H_2 (H_{119})	H_3 (H_{118})	H_4 (H_{117})		H_{119} (H_2)	H_{120} (H_1)
0	H	L	Undefined	←	←	←		←	←
1	L	L	Sampling C_2 (C_3)	Sampling C_3 (C_2)	Sampling C_1 (C_1)	Sampling C_2 (C_3)		Sampling C_3 (C_2)	Sampling C_1 (C_1)
2	L	L	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)		Output C_3 (C_2)	Output C_1 (C_1)
3	L	L	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)		Output C_2 (C_2)	Output C_3 (C_2)
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮

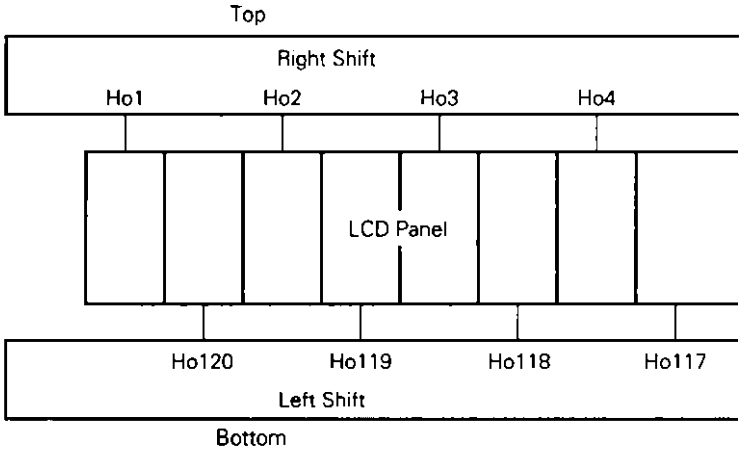
( ): for left shift

TIMING CHART

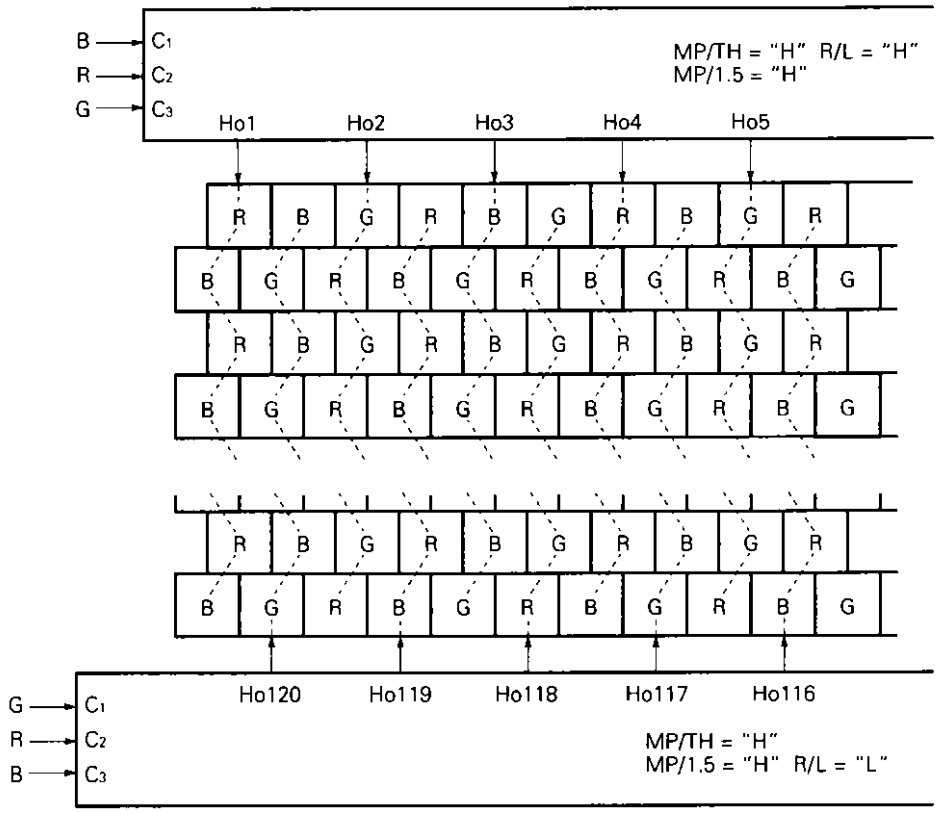


SEQUENTIAL SAMPLING





EXAMPLE OF MULTIPLEXER OPERATION IN MOSAIC ARRANGEMENT MODE



(3) MOSAIC ARRANGEMENT MODE (MP/TH = H, MP/1.5 = L)

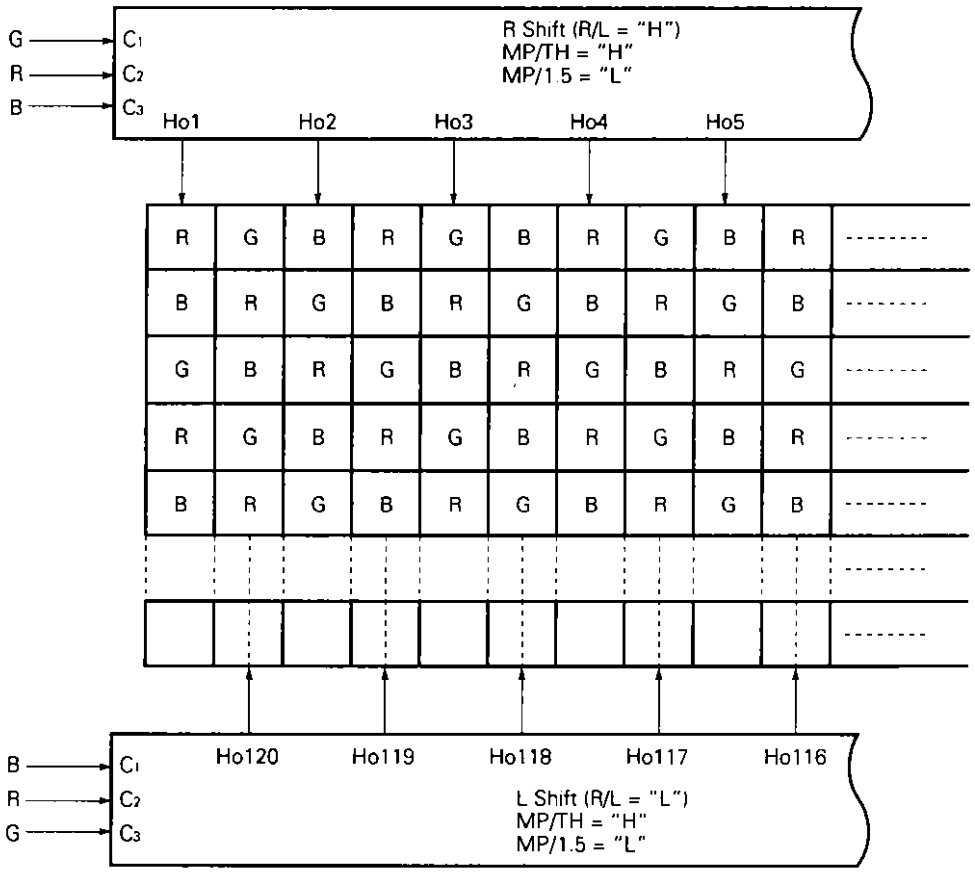
In this mode, the relation between video signals C_1, C_2, and C_3, and the output pins is as shown below. This mode is used to drive an LCD panel in the mosaic arrangement.

Relations between video signals C_1, C_2, C_3, and output pins

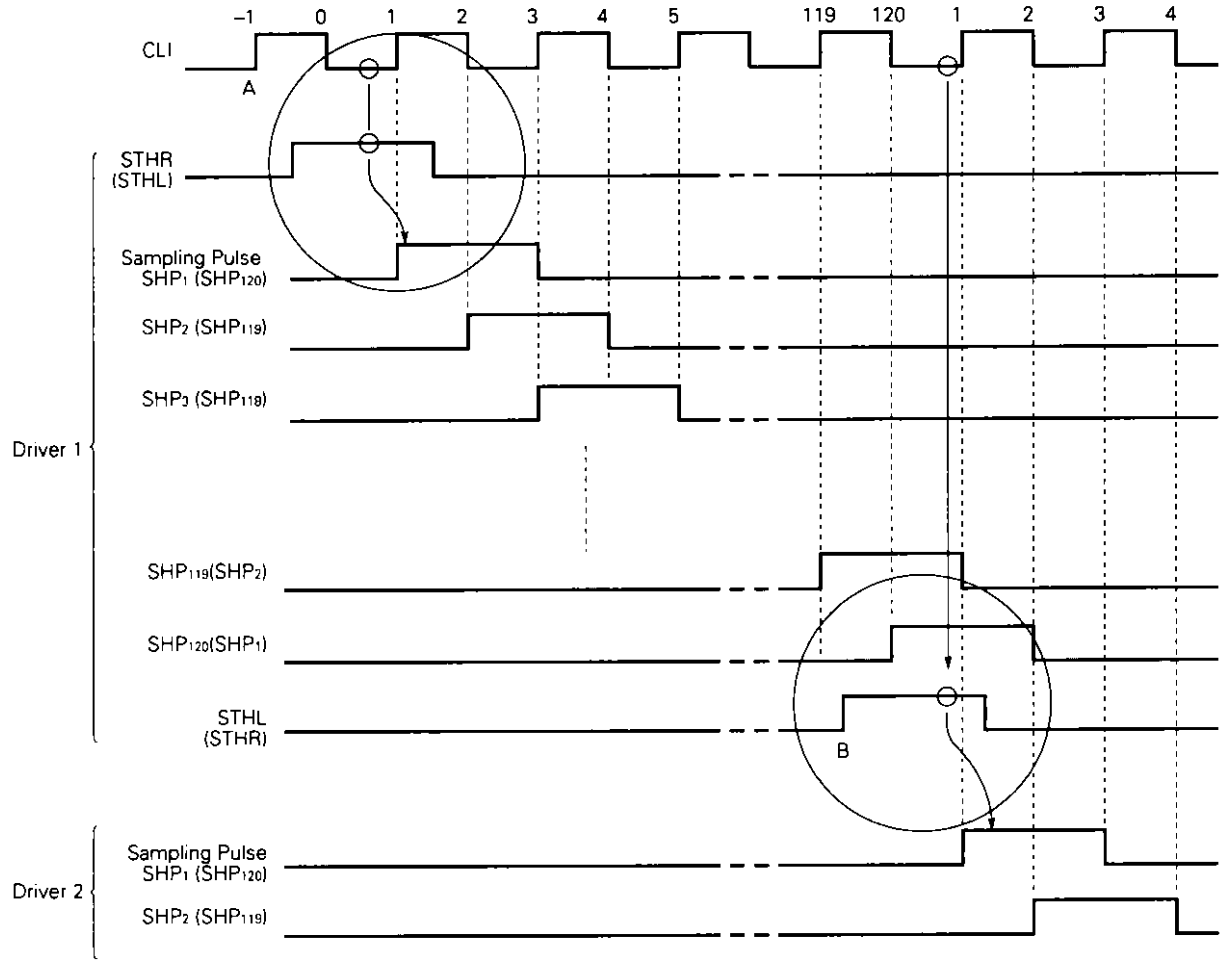
Line No. (INHs)	RESET	INH	H_1 (H_{120})	H_2 (H_{119})	H_3 (H_{118})	H_4 (H_{117})		H_{119} (H_2)	H_{120} (H_1)
0	H	L	Undefined	←	←	←		←	←
1	L	L	Sampling C_2 (C_3)	Sampling C_3 (C_2)	Sampling C_1 (C_1)	Sampling C_2 (C_3)		Sampling C_3 (C_2)	Sampling C_1 (C_1)
2	L	L	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)		Output C_3 (C_2)	Output C_1 (C_1)
3	L	L	Output C_3 (C_2)	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)		Output C_1 (C_1)	Output C_2 (C_3)
4	L	L	Output C_1 (C_1)	Output C_2 (C_3)	Output C_3 (C_2)	Output C_1 (C_1)		Output C_2 (C_3)	Output C_3 (C_2)
⋮	⋮	⋮	⋮	⋮	⋮	⋮		⋮	⋮

( ): for left shift

EXAMPLE OF MULTIPLEXER OPERATION IN MOSAIC ARRANGEMENT MODE

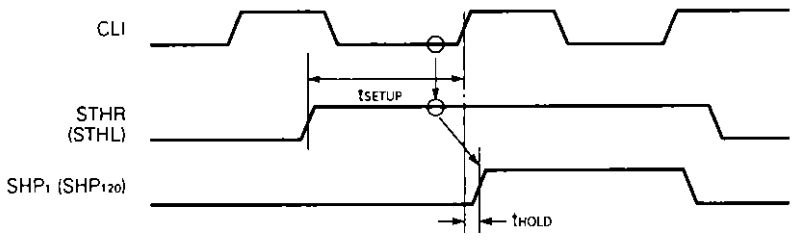


TIMING CHART (SEQUENTIAL SAMPLING)

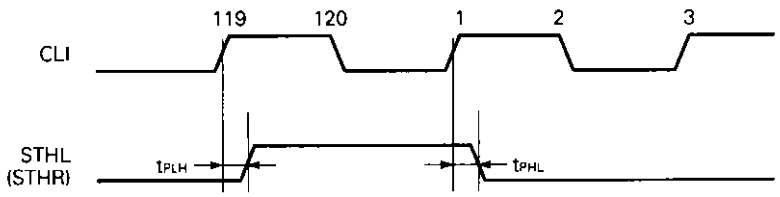


Remark The sampling pulse is set to the first stage of the shift register by the INH input. The shift register is started by the start trigger pulse that is generated when CL1 is low and STHR (STHL) is high, and is stopped when STHL (STHR) is output. STHR (STHL) is input three clocks after INH has fallen.

CASCADE INPUT TIMING (A of shift timing)

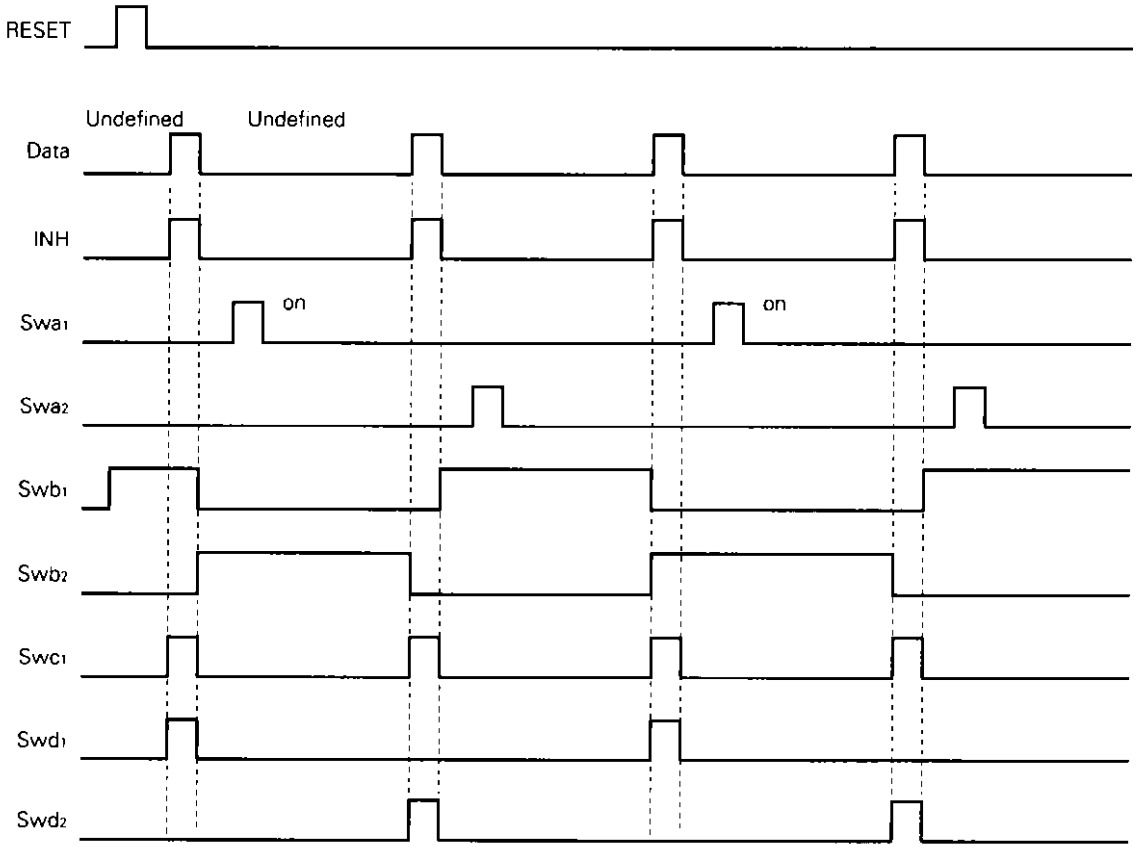


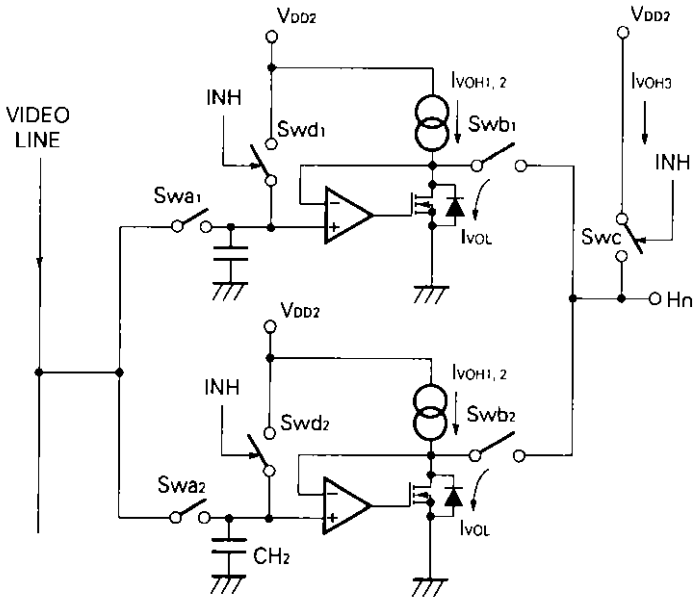
CASCADE OUTPUT TIMING (B of shift timing)



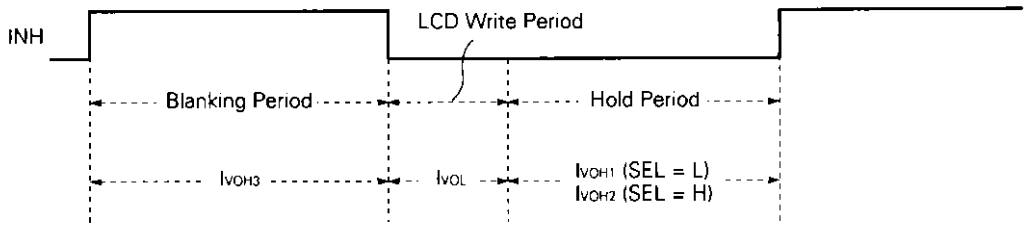
SAMPLE AND HOLD CIRCUITS

The sample and hold circuits execute a sample and hold operation on video signals C_1 through C_3 selected by the multiplexer in the timing shown below, by using two latches. Swa_1 and Swa_2 are reset by the RESET signal and change at the rising and falling of the INH signal.





The timing sequence of the output buffer is illustrated below. During the blanking period, the LCD is reset (charged) once to the V_{DD2} level by I_{VOH3}. Next, the sampling voltage is written to the LCD by the sink current I_{VOL}. When the specified voltage has been written, the LCD voltage is held by the source current I_{VOH1} (–8 μA typ.; SEL = L) or I_{VOH2} (–30 μA typ.; SEL = H), by using SEL (output current select input). SEL must be set to H or L in advance. I_{VOL} is automatically switched to I_{VOH1} or I_{VOH2}, but the timing of INH is determined by the load capacitance of the LCD and other factors and therefore must be determined according to the individual LCD panel used.



ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	Ratings	Unit
Logic Supply Voltage	V_{DD1}		−0.5 to +7.0	V
Driver Supply Voltage	V_{DD2}		−0.5 to +15	V
Logic Input Voltage	V_I		−0.5 to V_{DD1} + 0.5	V
Video Input Voltage	V_{VI}	C_1, C_2, C_3	−0.5 to V_{DD2} + 0.5	V
Logic Output Voltage	V_{O1}		−0.5 to V_{DD1} + 0.5	V
Video Output Voltage	V_{O2}		−0.5 to V_{DD2} + 0.5	V
Driver Output Current	I_{O2}		±10	mA
Operating Temperature	T_A		−20 to +85	°C
Storage Temperature	T_{stg}		−65 to +125	°C

RECOMMENDED OPERATING RANGE (T_A = −20 to +85 °C, V_{SS} = 0 V)

Parameter	Symbol	Conditions	MIN.	TYP.	MAX.	Unit
Logic Supply Voltage	V_{DD1}		4.5		5.5	V
Driver Supply Voltage	V_{DD2}				12	V
Driver Output Voltage	V_{O2}		V_{SS2} + 2.5		V_{DD2} − 2	V
High-level Input Voltage	V_{IH}		0.7 V_{DD1}		V_{DD1}	V
Low-level Input Voltage	V_{IL}		0		0.3 V_{DD1}	V

The elements are safe from damage and the functions work properly in the range T_A = −30 to +85 °C.

ELECTRICAL CHARACTERISTICS (T_A = –20 to +85 °C, V_{DD1} = 5 V ±10 %, V_{DD2} = 12 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Video Signal Maximum Output Voltage	V_{VOH}		V_{DD2} – 2.0	V_{DD2} – 0.8		V
Video Signal Minimum Output Voltage	V_{VOL}			1.45	2.5	V
Logic High-level Output Voltage	V_{LOH}	STHL, STHR pin I_{OH} = –1 mA	0.9·V_{DD1}			V
Logic Low-level Output Voltage	V_{LOL}	STHL, STHR pin I_{OL} = 1 mA			0.1·V_{DD1}	V
High-level Input Voltage	V_{IH}		0.7·V_{DD1}		V_{DD1}	V
Low-level Input Voltage	V_{IL}		0		0.3·V_{DD1}	V
Video Signal High-level Output Current 1	I_{VOH1}	INH = L, SEL = L V_{of} = 6 V, V_O = 8 V	–13	–8	–2	μA
Video Signal High-level Output Current 2	I_{VOH2}	INH = L, SEL = H V_{of} = 6 V, V_O = 8 V		–30		μA
Video Signal High-level Output Current 3	I_{VOH3}	INH = H V_{of} = 10 V			–0.3	mA
Video Signal Low-level Output Current	I_{VOL}	INH = L V_{of} = 11 V, V_O = 8 V	0.3			mA
Video Signal Minimum Input Voltage	V_{VIL}	T_A = 25 °C			1.5	V
Reference Voltage 1	V_{REF1}	V_{VI} = 2 V, T_A = 25 °C		1.99		V
Reference Voltage 2	V_{REF2}	V_{VI} = 6 V, T_A = 25 °C		5.97		V
Reference Voltage 3	V_{REF3}	V_{VI} = 10 V, T_A = 25 °C		9.97		V
Output Voltage deviation 1	ΔV_{VO1}	V_{VI} = 2 V, T_A = 25 °C			±50	mV
Output Voltage deviation 2	ΔV_{VO2}	V_{VI} = 6 V, T_A = 25 °C			±50	mV
Output Voltage deviation 3	ΔV_{VO3}	V_{VI} = 10 V, T_A = 25 °C			±50	mV
Logic Input Leakage Current	I_{LL}				±1	μA
Video Input Leakage Current	I_{VL}				±10	μA
Logic Dynamic Current Consumption	I_{DD1}	f_{CLK} = 5 MHz V_{VI} = 6 V, no load INH-duty = 4.5 %		1.0	2.5	mA
Driver Dynamic Current Consumption	I_{DD2}	f_{CLK} = 5 MHz INH = H, no load INH-duty = 4.5 %		2.7	5.0	mA

V_{of}; output applied voltage, V_o; output voltage under no load

REF values are typical values only. The output deviation is the on-chip guaranteed value.

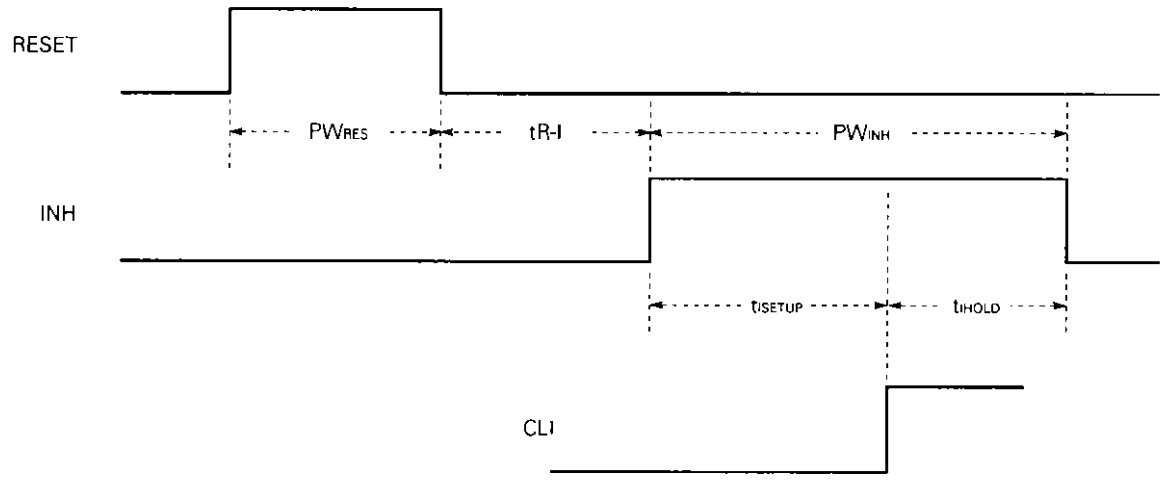
SWITCHING CHARACTERISTICS (T_A = −20 to +85 °C, V_{DD1} = 5 V ±10 %, V_{DD2} = 12 V, C_L = 20 pF)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Start Pulse Propagation Delay Time	t_{PHL}		10		120	ns
	t_{PLH}		10		120	ns
Maximum Clock Frequency	$f_{max.}$	Cascade connection	5			MHz
Logic Input Capacitance	C_{I1}	Other than STHL, STHR, T_A = 25 °C			15	pF
STHL, STHR Input Capacitance	C_{I2}	STHL, STHR, T_A = 25 °C			20	pF
Video Input Capacitance	C_{I3}	C_1 to C_3, V_{VI} = 6 V, T_A = 25 °C			30	pF

TIMING REQUIREMENTS (T_A = −20 to +85 °C, V_{DD1} = 5 V ±10 %, V_{DD2} = 12 V)

Parameter	Symbol	Condition	MIN.	TYP.	MAX.	Unit
Clock Pulse Width	PW_{CLI}	Duty = 50 %	100			ns
Start Pulse Setup Time	t_{SETUP}		80			ns
Start Pulse Hold Time	t_{HOLD}		10			ns
ST Pulse Width	PW_{ST}		100			ns
Reset Pulse Width	PW_{RES}		100			ns
INH Setup Time	t_{ISETUP}		300			ns
INH Hold Time	t_{IHOLD}		300			ns
Reset - INH Time	tR-I		100			ns

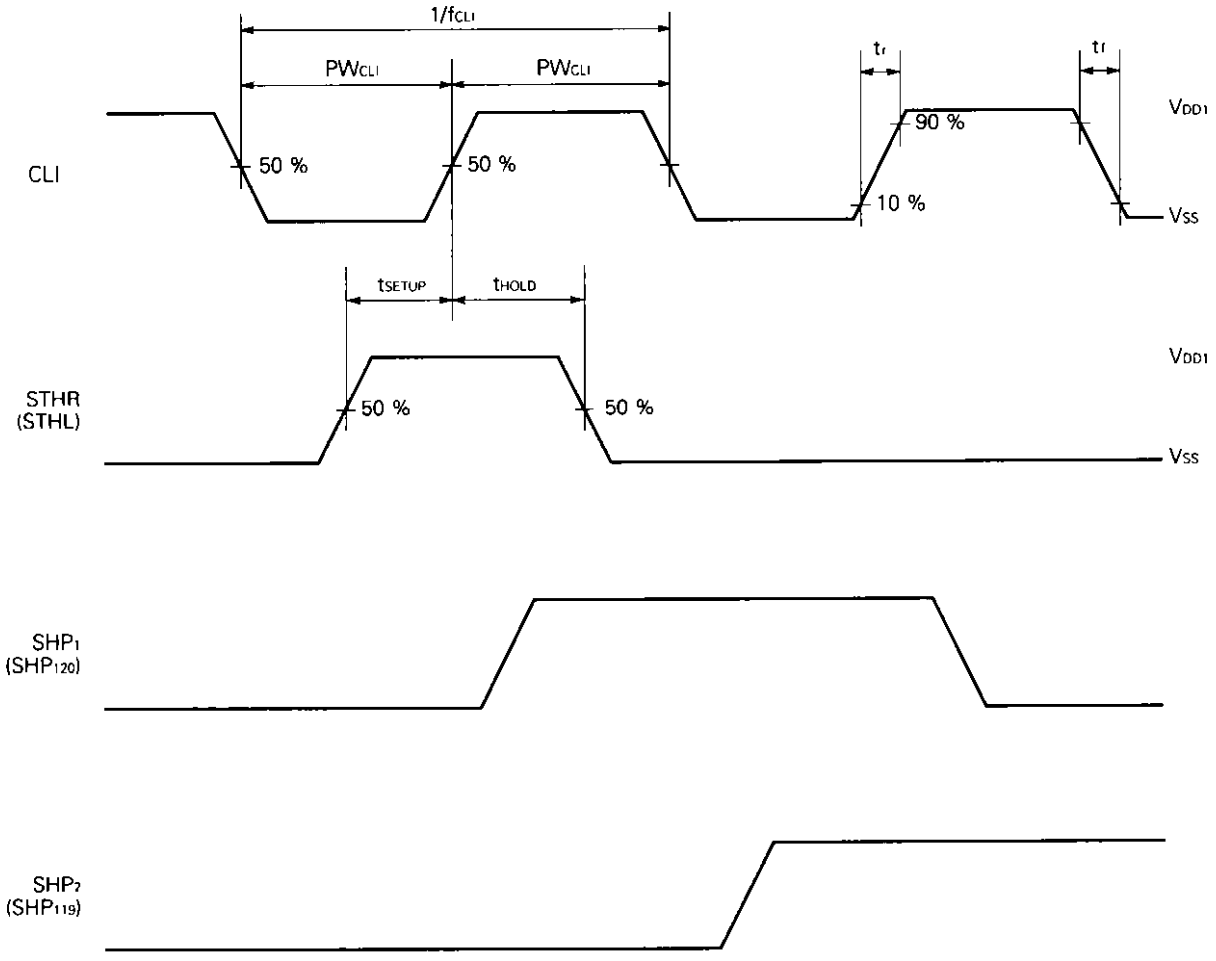
Keep the rise and fall times of all the digital signals to within t_r = t_f = 5 ns (10 % to 9 %). As an example, CLI is defined in the switching characteristic waveform diagram on the next page.



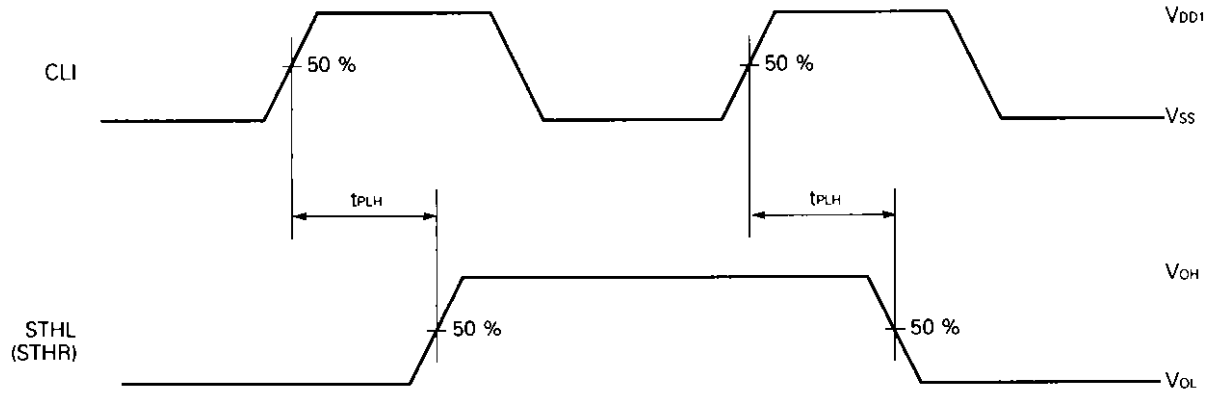
Make sure that the start INH pulse width PW_{INH} is at least three clocks.

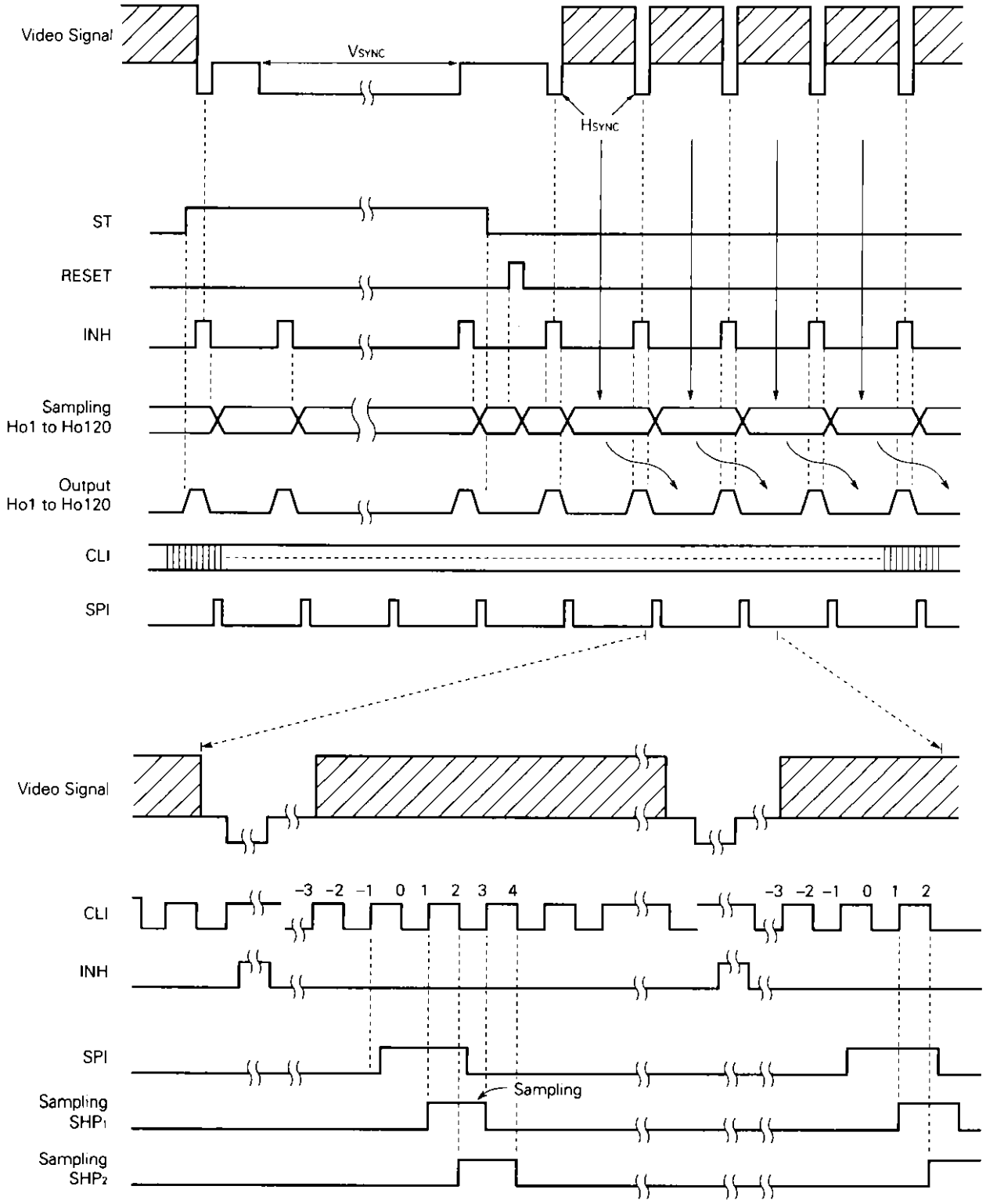
SWITCHING CHARACTERISTIC WAVEFORM

Start Pulse Input Timing



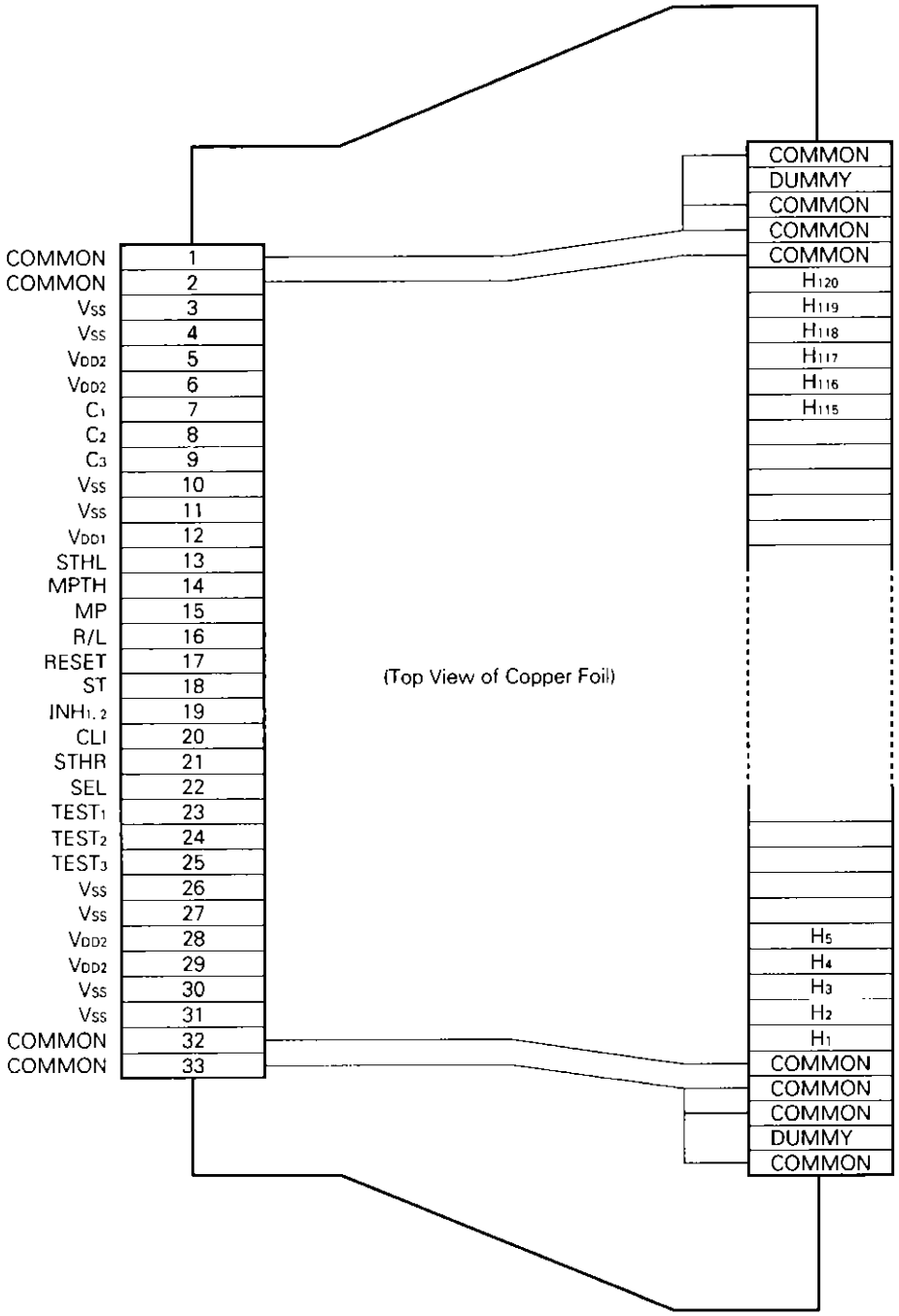
Start Pulse Output Timing





ST: By inputting this signal during the vertical blanking period, the power consumption can be reduced.

STANDARD TCP PIN CONFIGURATION (μPD16447N-051)



Caution This figure indicates the pin configuration of the standard TCP and does not specify the dimensions of the TCP.

RECOMMENDED MOUNTING CONDITIONS

The following mounting conditios for the μPD16447 are recommended.
For any other mounting conditions, consult NEC.

Mounting Conditions	Mounting Method	Conditions
Thermocompression	Soldering	Heating tool: 300 to 350 °C, Time: 2 to 3 seconds, Pressure: 100 g (per piece)
	ACF (sheet adhesive agent)	Preliminary adhesion: 70 to 100 °C, Pressure: 3 to 8 kg/cm^2, Time: 3 to 5 seconds Actual adhesion: 165 to 180 °C, Pressure: 25 to 45 kg/cm^2, Time: 30 to 40 seconds (with Sumitomo Bakelite's anisotropie film SUMIZAC1003)

Caution 1. For the mounting conditions for the ACF, consult the ACF manufacturer before using the ACF.
2. Do not use two or more mounting methods in combination.

REFERENCE

Document Name	Document No.
NEC semiconductor device reliability/quality control system.	IEI-1212
Quality grade on NEC semiconductor devices.	IEI-1209
Semiconductor device mounting technology manual.	IEI-1207

[MEMO]

[MEMO]