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RENESAS

MOS INTEGRATED CIRCUIT

μPD17134B, 17136B

SMALL GENERAL-PURPOSE 4 BIT SINGLE-CHIP MICROCONTROLLER

The μPD17134B and μPD17136B are 4-bit single-chip microcontrollers containing an 8-bit A/D converter (four channels), three timers, an AC zerocross detector, a power-on/power-down reset circuit, and a serial interface.

For the CPU, the μPD17134B and μPD17136B employ a 17K architecture using general registers. The new architecture allows operations to be performed directly on data memory, without involving accumulators as conventionally done. In addition, each instruction is 16 bits (one word) long, allowing programming to be done efficiently.

The μPD17P136B, a one-time PROM product, is available for program evaluation of the μPD17134B and μPD17136B and for small-scale production.

The μPD17134B and μPD17136B are products which achieves shorter oscillation settling time than the μPD17134A and μPD17136A. These products cannot be used in place of the μPD17134A and μPD17136A.

FEATURES

- 17K architecture : General registers
- Program memory (ROM)
  - μPD17134B : 2K bytes (1024 × 16 bits)
  - μPD17136B : 4K bytes (2048 × 16 bits)
- Data memory (RAM) : 112 × 4 bits
- External interrupt : 1 line (INT pin, with sensor input)
- Instruction execution time : 8 μs (at fcc = 2 MHz, RC oscillation[Note 1])
- 8-bit A/D converter : 4 channels
  Absolute accuracy: ±1.5 LSB or lower (V_{DD} = 5 V ±10 %)
- Timer function : 3 channels
- Serial interface : 1 channel (three-wire synchronous mode)
- Input/output pins : 22 pins (including one general input pin and one sensor input pin)
- Power-on/power-down reset circuit[Note 2]
- Operating supply voltage range : V_{DD} = 2.7 to 5.5 V

Notes 1. The capacitor for RC oscillation is contained in the μPD17136B.

2. The power-on/power-down reset may not be performed normally because the oscillation settling time is very short. In such a case, input the $\overline{\text{RESET}}$ signal using an external device.

This manual describes the μPD17136B unless otherwise specified.

The information in this document is subject to change without notice.

Document No. IC-3596
(O. D. No. IC-9083)
Date Published March 1995 P
Printed in Japan

APPLICATIONS

Controlling automatic focus lenses of cameras

ORDERING INFORMATION

Part number	Package
μPD17134BCT-xxx	28-pin plastic shrink DIP (400 mil)
μPD17134BGT-xxx	28-pin plastic SOP (375 mil)
μPD17136BCT-xxx	28-pin plastic shrink DIP (400 mil)
μPD17136BGT-xxx	28-pin plastic SOP (375 mil)

Remark xxx: ROM code number

DIFFERENCES BETWEEN μPD17134B SUBSERIES AND μPD17134A SUBSERIES

Item	μPD17134B	μPD17136B	μPD17134A	μPD17136A
Oscillation settling time	2 × 512/fcc		256 × 512/fcc	
Value in timer 1 modulo register when reset	01H		FFH	
Quality grade	Standard		Standard	• Standard • Special
One-time PROM product	μPD17P136B		μPD17P136A	

CHARACTERISTICS

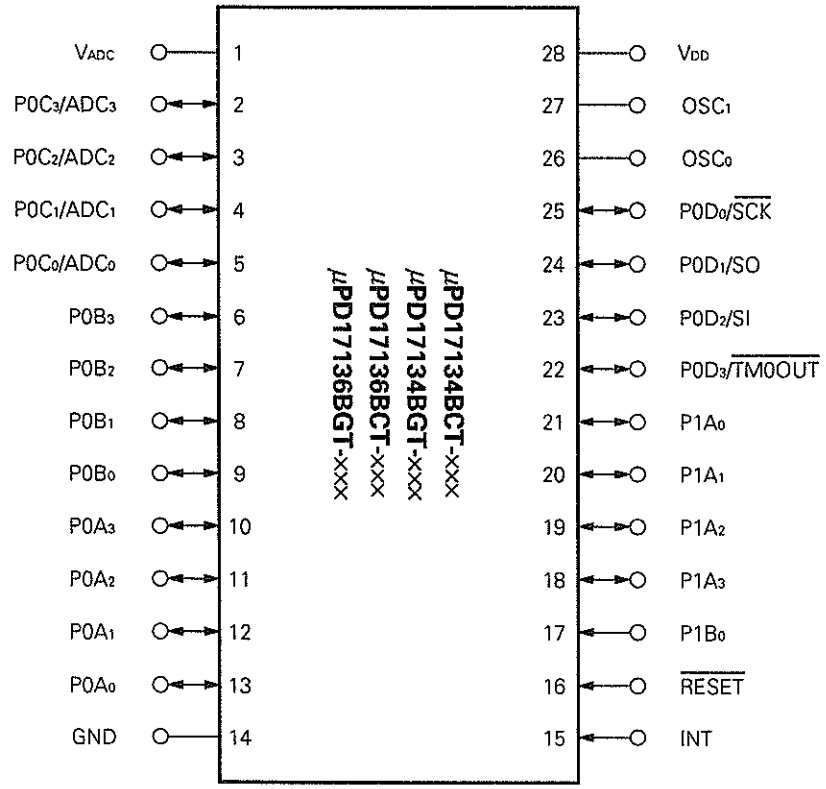
Item \ Product	μPD17134B	μPD17136B
ROM	2K bytes (1024 × 16 bits)	4K bytes (2048 × 16 bits)
RAM	112 × 4 bits (The stack is separate from data memory.)	
Stack	5 address stacks, 3 interrupt stacks	
Number of I/O ports	22 { • 20 I/O ports • 1 general input port • 1 sensor input port (INT pin[Note]) (also used for an interrupt or AC zerocross input)	
A/D converter input	4 channels (shared with ports) with an absolute accuracy of ±1.5 LSB or less at a power voltage 5 V ±10 %	
Timer	3 channels { • 2 channels for 8-bit timers (They can be used together as one 16-bit timer.) • 1 channel for a 7-bit basic interval timer (can be used as a watchdog timer)	
Serial interface	1 channel (3-wire type)	
Interrupt	• Up to 3 levels of multiple hardware interrupt • 1 external interrupt (INT) { • Shared with the input from the AC zerocross detection circuit • Detection of the rising edge, falling edge, or both edges can be selected. • With the sensor input • 4 internal interrupts { • Timer 0 (TM0) • Timer 1 (TM1) • Basic interval timer (BTM) • Serial interface (SIO)	
Execution time of an instruction	8 μs at f_{CC} = 2 MHz clock, RC oscillation	
Standby function	STOP/HALT	
Power-on/power-down reset circuit	Built-in (Can be used in an application circuit where V_{DD} is 4.5 to 5.5 V)	
Oscillation settling time	2 × 512/f_{CC}	
Operating supply voltage	• 2.7 V to 5.5 V • 4.5 V to 5.5 V (when the power-on/power-down reset functions are used)	
Package	• 28-pin plastic shrink DIP (400 mil) • 28-pin plastic SOP (375 mil)	
One-time PROM	μPD17P136B	

Note The INT pin can be used as an input pin (sensor input) when the external interrupt function is not used. The status of the pin is read with the INT flag of the control register, not with the port register.

Caution Although a PROM product is highly compatible with a masked ROM product in respect of functions, they differ in internal ROM circuits and part of electrical characteristics. Before changing the PROM product to the masked ROM product in an application system, evaluate the system carefully using the masked ROM product.

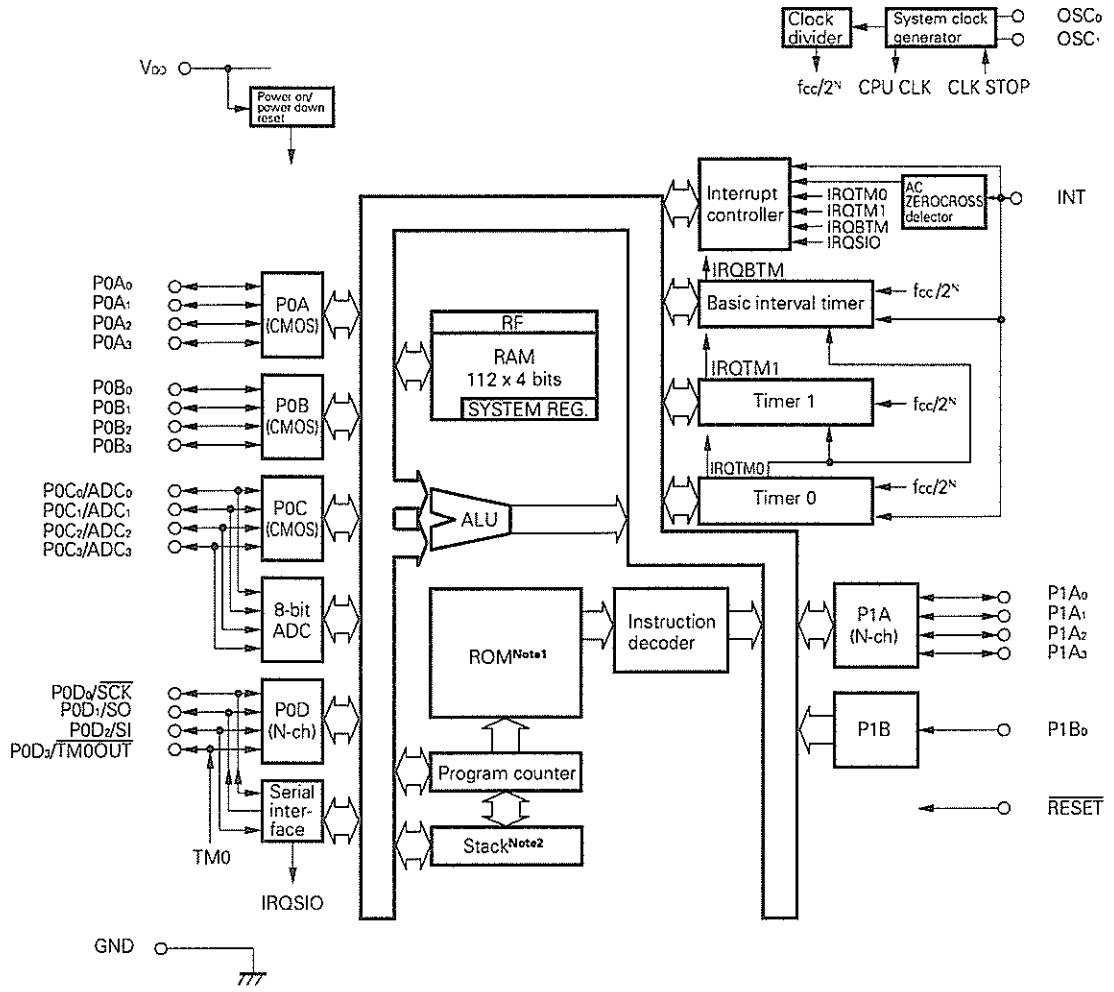
PIN CONFIGURATION (TOP VIEW)

28-pin plastic shrink DIP
28-pin plastic SOP



ADC0-ADC3	: Analog input	P1A0-P1A3	: Port 1A
GND	: Ground	P1B0	: Port 1B
INT	: External interrupt input	$\overline{\text{RESET}}$	: Reset input
OSC0, OSC1	: System clock oscillation	$\overline{\text{SCK}}$	: Serial clock input/output
P0A0-P0A3	: Port 0A	SI	: Serial data input
P0B0-P0B3	: Port 0B	SO	: Serial data output
P0C0-P0C3	: Port 0C	$\overline{\text{TM0OUT}}$	: Timer 0 output
P0D0-P0D3	: Port 0D	VADC	: Analog power supply
		VDD	: Power supply

BLOCK DIAGRAM



Remark The terms CMOS and N-ch in parentheses indicate the output form of the port.

CMOS : CMOS push-pull output

N-ch : N-channel open-drain output (Each pin can contain pull-up resistor as specified using a mask option.)

Notes 1. The ROM capacity of each product is as follows:

μPD17134B : 1024 × 16 bits

μPD17136B : 2048 × 16 bits

2. The stack capacity of each product is as follows:

μPD17134B : 5 × 10 bits

μPD17136B : 5 × 11 bits

CONTENTS

1. PINS

1.1 PIN FUNCTIONS

Pin No.	Pin name	Function	Output	After reset
1	V_{ADC}	Power voltage for the A/D converter and for the circuit generating reference voltage	Input	–

2 - 5	$P0C_3/ADC_3$ - $P0C_0/ADC_0$	Port 0C. Analog voltage is supplied to the A/D converter through these pins.
		• $P0C_3$ - $P0C_0$
		  • 4-bit input/output port
		  • Input/output setting allowed in units of 1 bit
		• ADC_3 - ADC_0
		  • Analog input for the A/D converter
			CMOS push-pull	Input (P0C)

6 - 9	$P0B_3$ - $P0B_0$	Port 0B • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	CMOS push-pull	Input
10 - 13	$P0A_3$ - $P0A_0$	Port 0A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by program in units of 4 bits	CMOS push-pull	Input
14	GND	Ground	–	–
15	INT	External interrupt request or sensor signal	–	Input
16	$\overline{RESET}$	System reset input pin • Pull-up resistor incorporation specifiable by mask option	–	Input
17	$P1B_0$	Port 1B • 1-bit input port • Pull-up resistor incorporation specifiable by mask option	Input	Input
18 - 21	$P1A_3$ - $P1A_0$	Port 1A • 4-bit input/output port • Input/output setting allowed in units of 4 bits • Pull-up resistor incorporation specifiable by mask option in units of 1 bit	N-ch open drain	Input

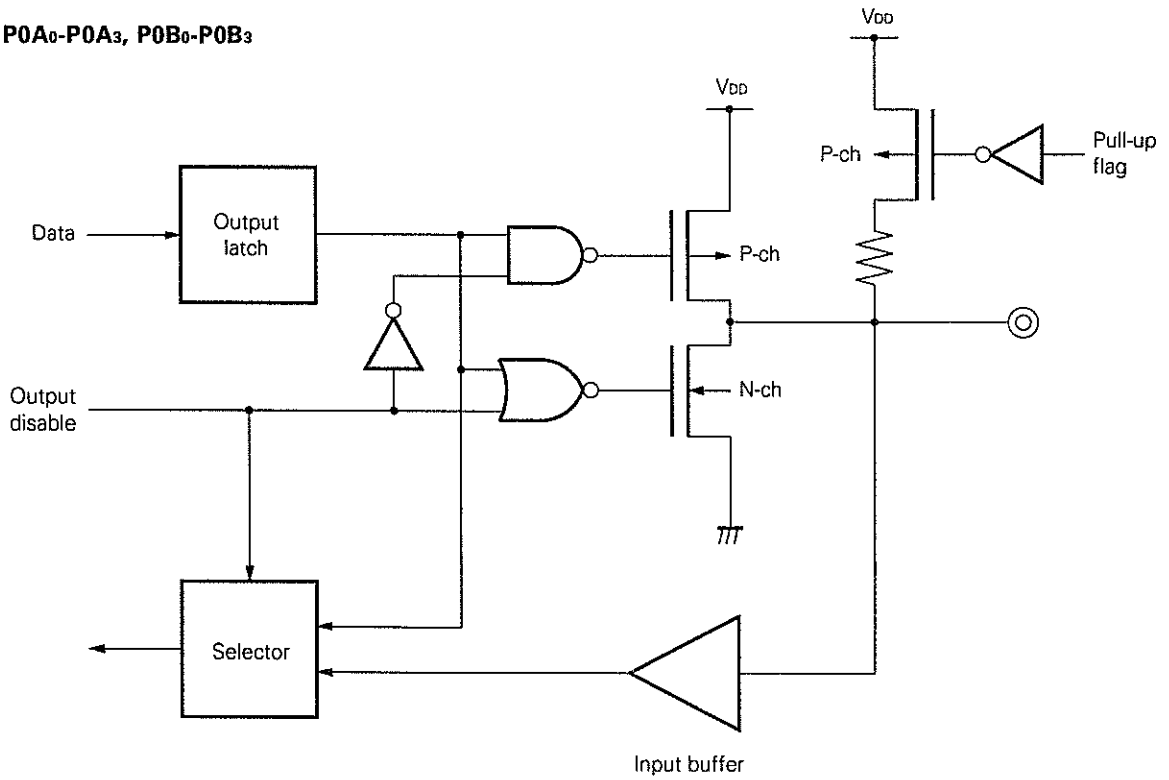
22	$P0D_3/\overline{TM0OUT}$	Pin for port 0D, timer 0 output, serial data input, serial data output, and serial clock input/output
		• Pull-up resistor incorporation specifiable by mask option in units of 1 bit
		• $P0D_3$ - $P0D_0$
		  • 4-bit input/output port
		  • Input/output setting allowed in units of 1 bit
		• $\overline{TM0OUT}$
		  • Timer 0 output
			N-ch open drain	Input (P0D)

23	$P0D_2/SI$	• SI • Serial data input		
24	$P0D_1/SO$	• SO • Serial data output		
25	$P0D_0/\overline{SCK}$	• $\overline{SCK}$ • Serial clock input/output		
26 27	OSC_0 OSC_1	For system clock oscillation Connect a resistor between OSC_0 and OSC_1.	–	–
28	V_{DD}	Power supply	–	–

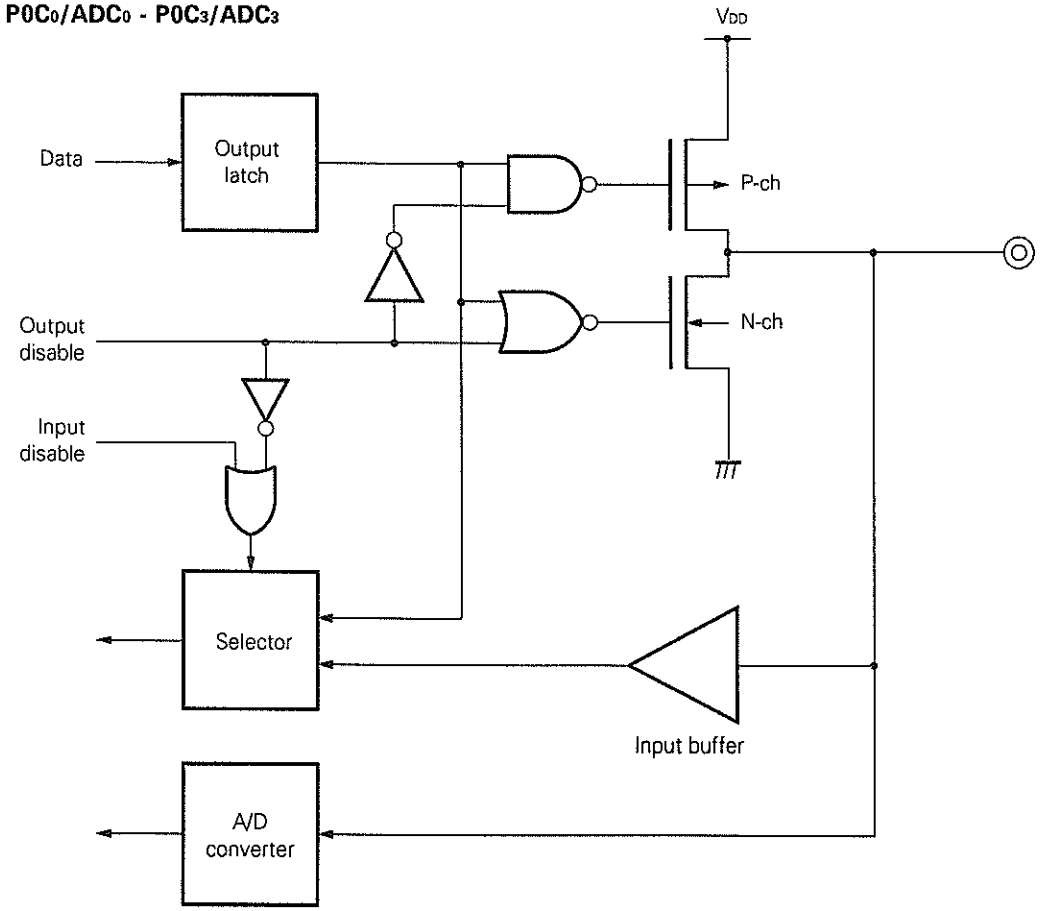
1.2 PIN EQUIVALENT CIRCUIT

Below are simplified diagrams of the input/output circuits for each pin.

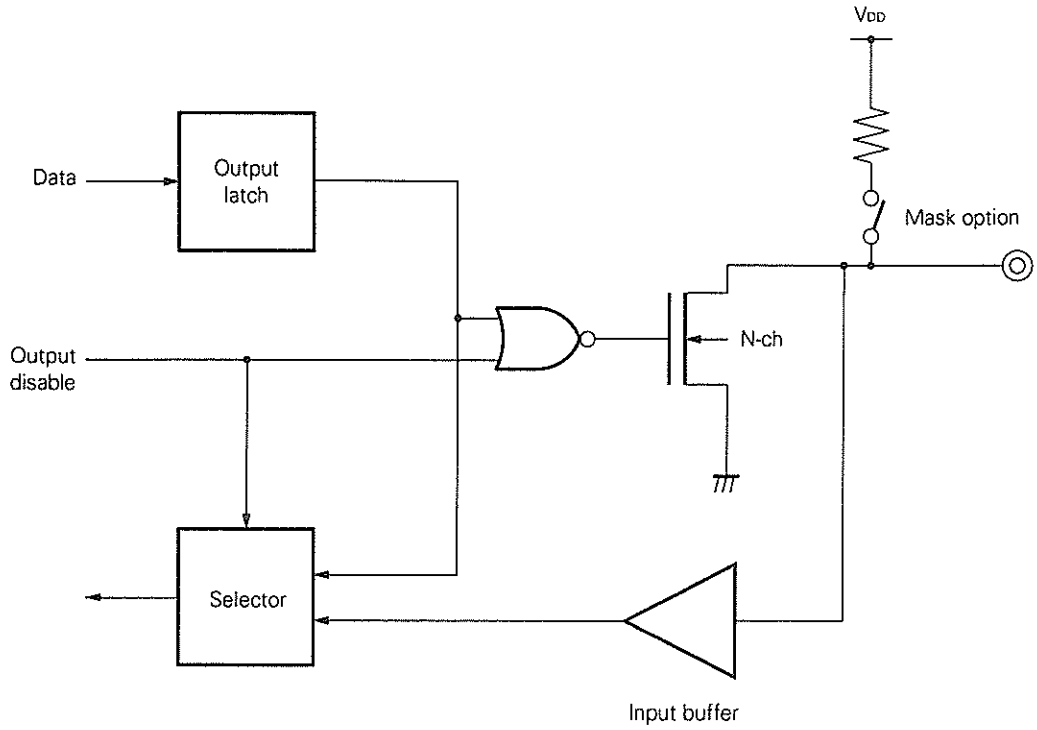
(1) $P0A_0$-$P0A_3$, $P0B_0$-$P0B_3$



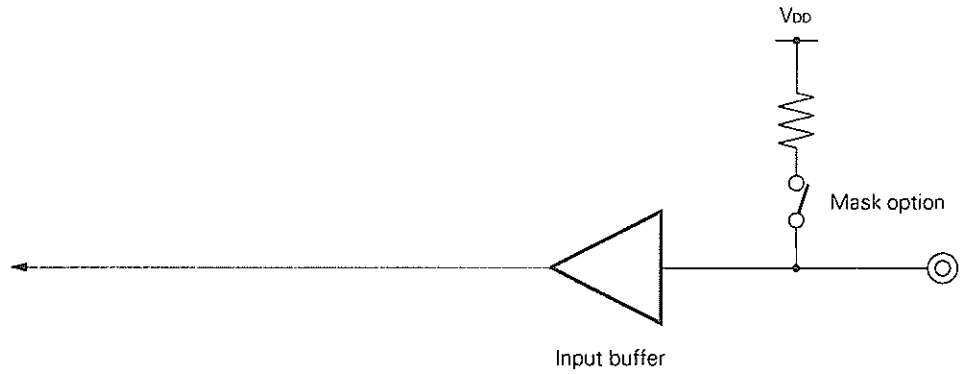
(2) $P0C_0$/ADC_0 - $P0C_3$/ADC_3



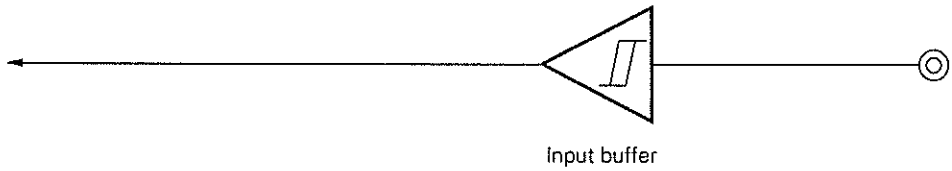
(3) $P0D_0$-$P0D_3$, $P1A_0$-$P1A_3$



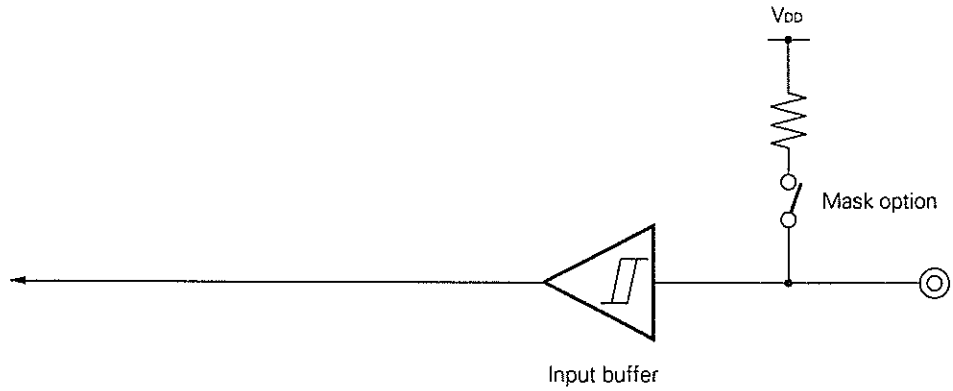
(4) $P1B_0$



(5) INT



(6) $\overline{\text{RESET}}$



1.3 HANDLING UNUSED PINS

Connect unused pins as follows:

Table 1-1 Handling Unused Pins

Pin			Recommended conditions and handling	
			Internal	External
Port	Input mode	P0A, P0B	Pull-up resistors that can be specified with the software are incorporated.	Leave open.
		P0C	—	Connect to V_{DD} or ground through resistors for each pin.[Note 1]
		P0D, P1A	Pull-up resistors that can be specified with the mask option are not incorporated.	Connect directly to ground.
			Pull-up resistors that can be specified with the mask option are incorporated.	Leave open.
		$P1B_0$[Note 2]	Pull-up resistors that can be specified with the mask option are not incorporated.	Connect directly to ground.
	Output mode	P0A, P0B, P0C (CMOS ports)	—	Leave open.
		P0D, P1A (N-ch open-drain port)	Outputs low level without pull-up resistors that can be specified with the mask option.	
			Outputs low level with pull-up resistors that can be specified with the mask option.	
External interrupt (INT)			Pull-up resistors that can be specified with the mask option are not incorporated.	Connect directly to V_{DD} or ground.
			Pull-up resistors that can be specified with the mask option are incorporated.	Leave open.
$\overline{RESET}$[Note 3]			Pull-up resistors that can be specified with the mask option are not incorporated.	Connect directly to V_{DD}.
			Pull-up resistors that can be specified with the mask option are incorporated.	
V_{ADC}			—	Connect directly to V_{DD}.

Notes 1. When a pin is pulled up to V_{DD} (connected to V_{DD} through a resistor) or pulled down to ground (connected to ground through a resistor) outside the chip, take the driving capacity and maximum current consumption of a port into consideration. When using high-resistance pull-up or pull-down resistors, apply appropriate countermeasures to ensure that noise is not attracted by the resistors. Although the optimum pull-up or pull-down resistor varies with the application circuit, in general, a resistor of 10 to 100 kilohms is suitable.

2. Since the $P1B_0$ pin is also used for setting the test mode, connect it directly to ground without incorporating a pull-up resistor that can be specified with the mask option, when the pin is not used.
3. When designing an application circuit which requires high reliability, be sure to design a circuit to which an external $\overline{RESET}$ signal can be input. Since the $\overline{RESET}$ pin is also used for setting the test mode, connect it to V_{DD} directly when not used.

Caution To fix the I/O mode, pull-up resistors that can be specified with the software, and output level of a pin, it is recommended that they should be specified repeatedly within a loop in a program.

1.4 NOTES ON USE OF THE $\overline{\text{RESET}}$ AND P1B0 PINS

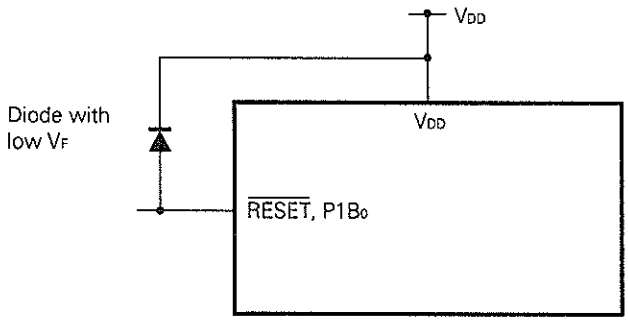
The $\overline{\text{RESET}}$ and P1B0 pins have the test mode selecting function for testing the internal operation of the μPD17136B (IC test), besides the functions shown in **Section 1.1.**

Applying a voltage exceeding V_{DD} to the $\overline{\text{RESET}}$ and/or P1B0 pin causes the μPD17136B to enter the test mode. When noise exceeding V_{DD} comes in during normal operation, the device is switched to the test mode.

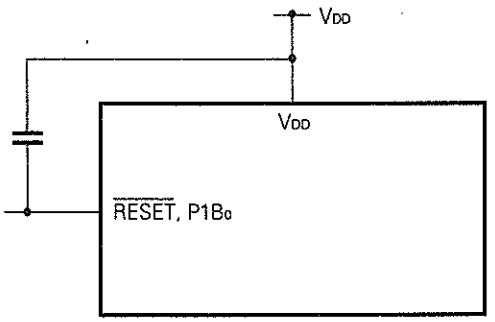
For example, if the wiring from the $\overline{\text{RESET}}$ or P1B0 pin is too long, noise may be induced on the wiring, causing this mode switching.

When installing the wiring, lay the wiring in such a way that noise is suppressed as much as possible. If noise yet arises, use an external part to suppress it as shown below.

- **Connect a diode with low V_F between the pin and V_{DD}.**



- **Connect a capacitor between the pin and V_{DD}.**



2. PROGRAM MEMORY (ROM)

Table 2-1 lists the program memory configuration for the μPD17134B and μPD17136B.

Table 2-1 Program Memory Configuration

Product	Program memory capacity	Address range
μPD17134B	2K bytes (1024 × 16 bits)	0000H – 03FFH
μPD17136B	4K bytes (2048 × 16 bits)	0000H – 07FFH

Program memory stores the program and the constant data table.

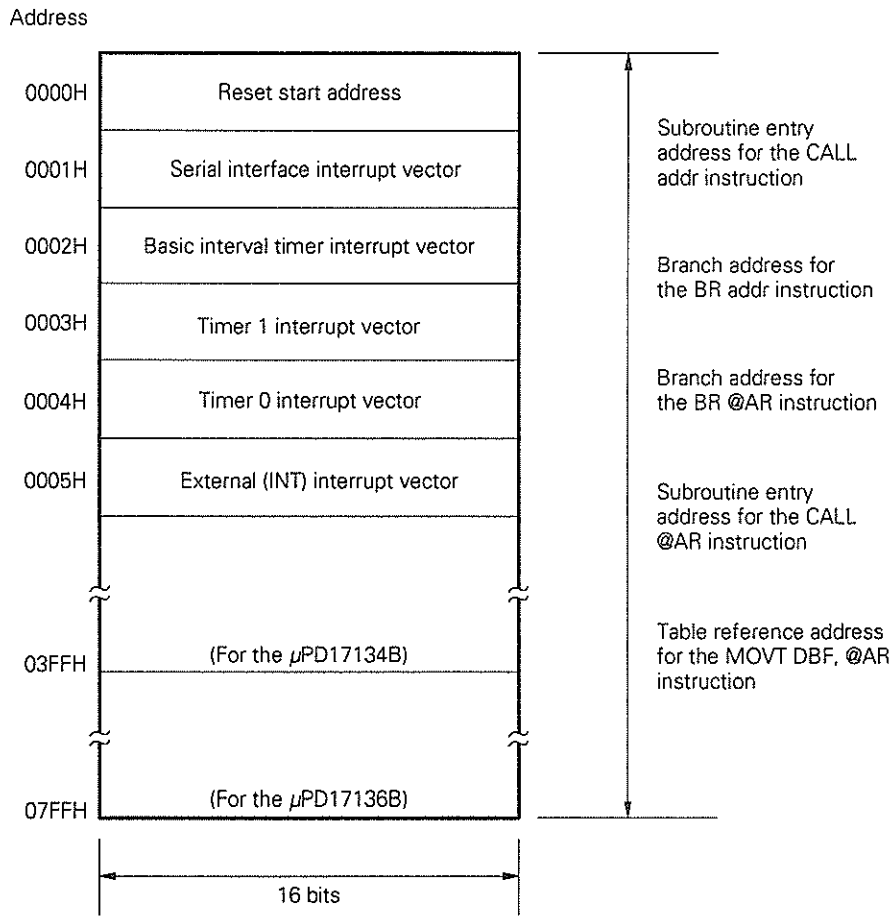
The program memory address is specified by the program counter.

The reset start address and interrupt vector addresses are assigned to program memory 0000H to 0005H.

2.1 PROGRAM MEMORY ORGANIZATION

Fig. 2-1 shows the program memory map. Branch instructions, subroutine calls, and table references can specify any address in program memory.

Fig. 2-1 Program Memory Map



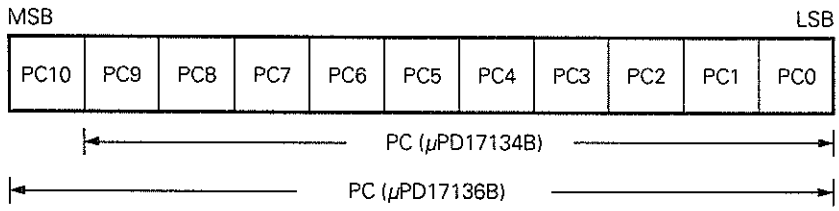
3. PROGRAM COUNTER (PC)

The program counter is used to specify an address in program memory.

3.1 PROGRAM COUNTER CONFIGURATION

The program counter of the μPD17134B is a 10-bit binary counter.
The program counter of the μPD17136B is a 11-bit binary counter.

Fig. 3-1 Program Counter



3.2 PROGRAM COUNTER OPERATION

Normally, the program counter is automatically incremented each time a command is executed. The memory address at which the next instruction to be executed is stored is assigned to the program counter under the following conditions: At reset; when a branch, subroutine call, return, or table referencing instruction is executed; or when an interrupt is received.

Fig. 3-2 Value of the Program Counter after an Instruction Is Executed

Instruction \ Program counter bit	Program counter value										
	PC10	PC9	PC8	PC7	PC6	PC5	PC4	PC3	PC2	PC1	PC0
During reset	0	0	0	0	0	0	0	0	0	0	0
BR addr CALL addr	Value set by addr										
BR @AR CALL @AR (MOVT DBF, @AR)	Value in the address register (AR)										
RET RETSK RETI	Value in the address stack location pointed to by the stack pointer (return address)										
During interrupt	Vector address for the interrupt										

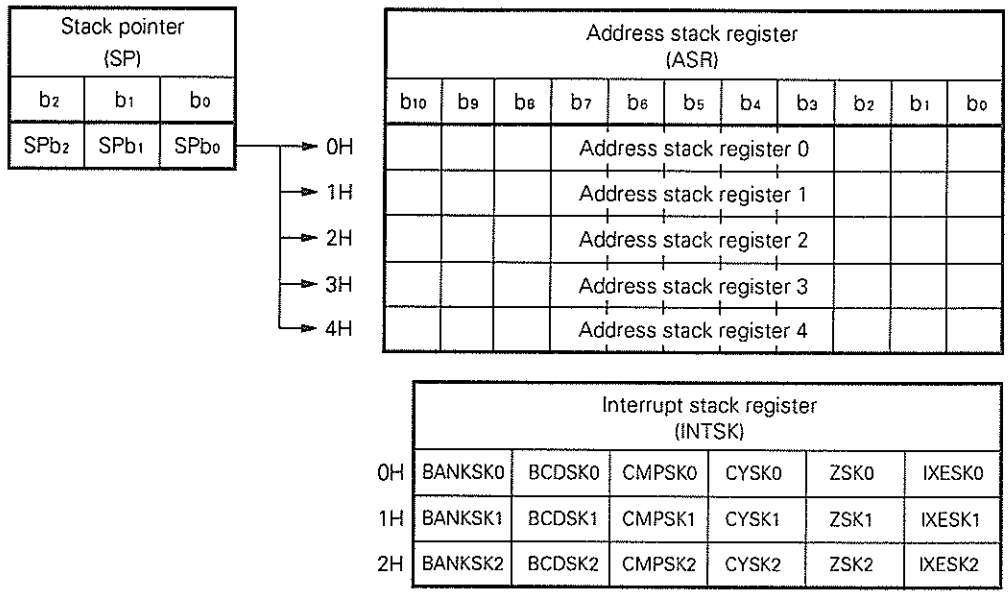
Remark The μPD17134B does not have PC10.

4. STACK

Fig. 4-1 shows the stack configuration. The stack consists of address stack registers and interrupt stack registers.

The stack is used to save the return address during execution of subroutine calls and table reference instructions. When an interrupt occurs, the program return address and the program status word (PSWORD) are automatically saved in the stack. Then, all bits of the bank and PSWORD are cleared to 0.

Fig. 4-1 Stack Configuration



Interrupt stack register (INTSK)

0H	BANKSK0	BCDSK0	CMPSK0	CYSK0	ZSK0	IXESK0
1H	BANKSK1	BCDSK1	CMPSK1	CYSK1	ZSK1	IXESK1
2H	BANKSK2	BCDSK2	CMPSK2	CYSK2	ZSK2	IXESK2

Remark The μPD17134B does not have b_{10}.

5. DATA MEMORY (RAM)

Data memory (RAM) stores data such as operation and control data. Data can be read from or written to data memory with an instruction during normal operation.

5.1 DATA MEMORY ORGANIZATION

Data memory locations have 7-bit addresses. The three high-order bits of each address are called the row address, and the four low-order bits are called the column address.

For example, the row address of address 1AH is 1H. The column address is 0AH.

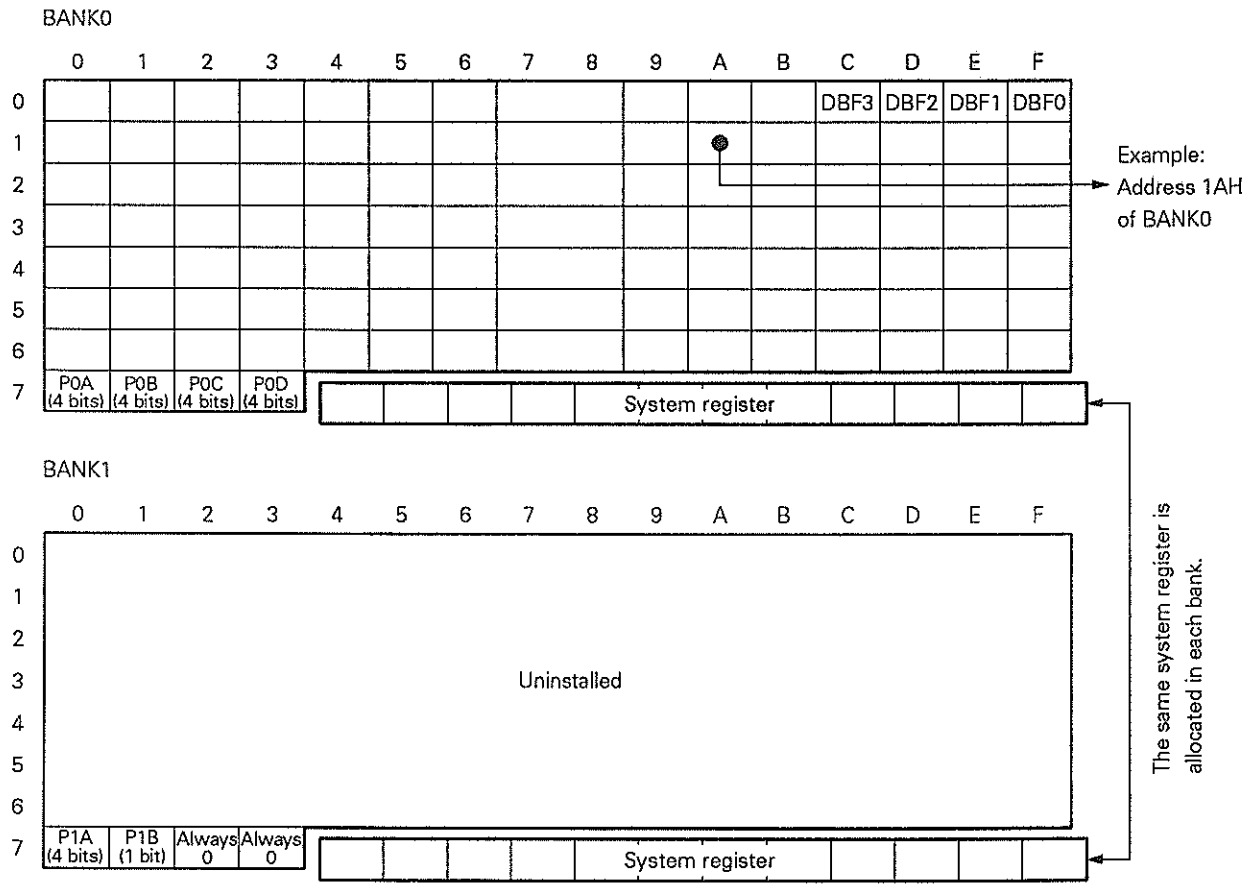
Each addressed memory location is 4-bits (one nibble) long.

Data memory contains an area to which the user is allowed to store data freely, as well as areas which are reserved for the use of specific functions.

The areas reserved for specific functions are as follows:

- System register (SYSREG) (See **Chapter 7.**)
- Data buffer (DBF) (See **Chapter 9.**)
- Port registers (See **Chapter 11.**)

Fig. 5-1 Organization of Data Memory



Caution There is no hardware installed at addresses 00H to 6FH of BANK1. Therefore, do not use this area. Any attempt to read this area will yield unpredictable results. Writing data to this area is invalid.

6. GENERAL REGISTER (GR)

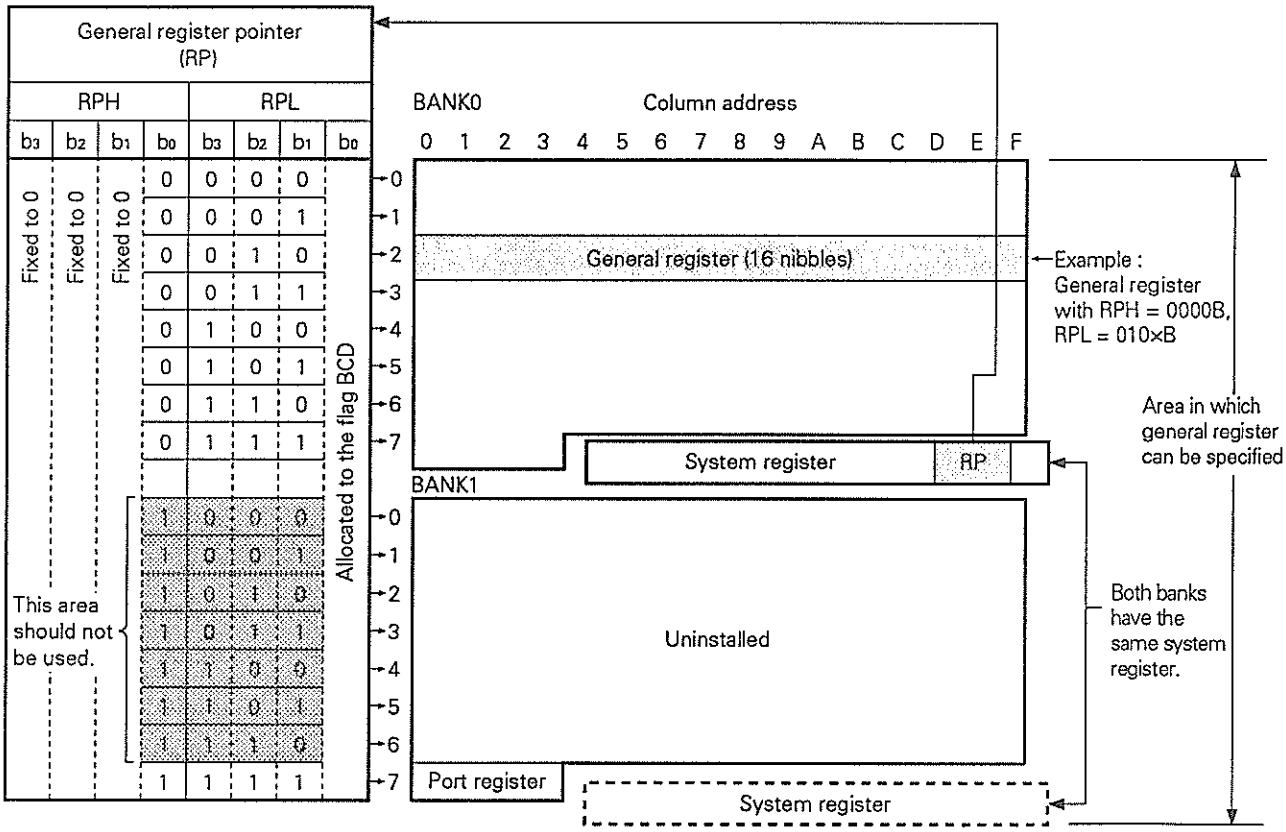
The general register, as the name implies, is a general register used for data transfer and manipulation. In the 17K series, the location of the general register is not fixed. The area used for the general register is in data memory, as specified by the general register pointer (RP). Thus, part of the data memory area can be specified as the general register as required, allowing data transfer in data memory and data memory manipulation to be performed with a single instruction.

6.1 GENERAL REGISTER POINTER (RP)

RP is a pointer used to specify part of data memory as the general register. In RP, specify a desired data memory bank and row address for the general register. RP consists of seven bits: 7DH (RPH), and the three high-order bits of 7EH (RPL) in the system register (see **Chapter 7**).

Set a bank in RPH, and a data memory row address in RPL.

Fig. 6-1 General Register Pointer Configuration



7. SYSTEM REGISTER (SYSREG)

The system register (SYSREG), located in data memory, is used for direct control of the CPU.

7.1 SYSTEM REGISTER CONFIGURATION

Fig. 7-1 shows the allocation address of the system register in data memory. As shown in Fig. 7-1, the system register is allocated in addresses 74H to 7FH of data memory, independently of the banks (BANK0, BANK1). This means that each bank has the same system register at addresses 74H to 7FH.

Since the system register is allocated in data memory, it can be manipulated using any of the instructions available for manipulating data memory. Therefore, it is also possible to put the system register in the general register.

Fig. 7-1 Allocation of System Register in Data Memory

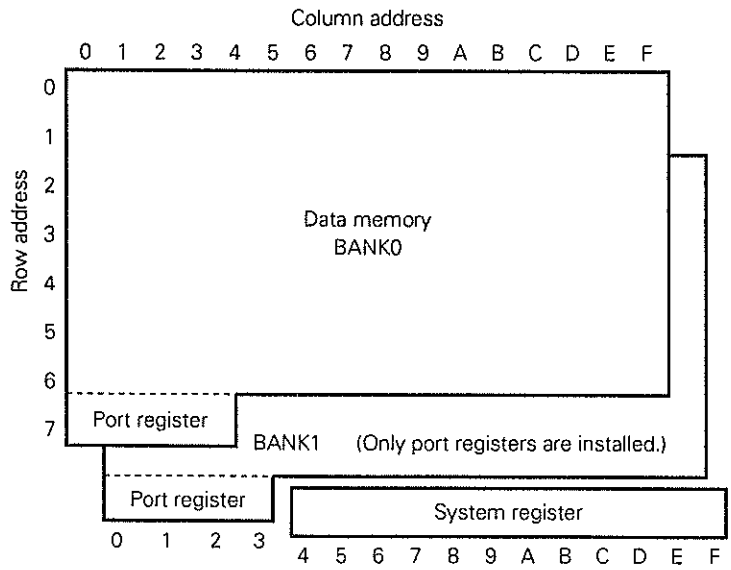


Fig. 7-2 shows the configuration of the system register. As shown in Fig. 7-2, the system register consists of the following seven registers.

- Address register (AR)
- Window register (WR)
- Bank register (BANK)
- Index register (IX)
- Data memory row address pointer (MP)
- General register pointer (RP)
- Program status word (PSW)

Fig. 7-2 System Register Configuration

Address	74H	75H	76H	77H	78H	79H	7AH	7BH	7CH	7DH	7EH	7FH
Name	Address register (AR)				Window register (WR)	Bank register (BANK)	Index register (IX) / Data memory row address pointer (MP)			General register pointer (RP)		Program status word (PSWORD)
Symbol	AR3	AR2[Note 1]	AR1	AR0	WR	BANK	IXH / MPH	IXM / MPL	IXL	RPH	RPL	PSW
Bit	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0
Data[Note 2]	0 0 0 0 (AR)	0 (AR)	(AR)	(AR)	↔	0 0 0 (BANK)	MPE 0 0 0 (MP)	(IX) (MP)	(IX)	0 0 0 (RP)	(RP)	BCD CMP CY Z IXE
Initial value when reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	Not defined	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Notes 1. For the μPD17134B, bit 2 of AR2 is fixed at 0.

2. A bit for which 0 is written is fixed at 0.

8. REGISTER FILE (RF)

The register file is a register used mainly for specifying conditions for peripheral hardware.

PEEK and POKE instructions or AS17K macro instructions SETn, CLRn, and INITFLG are used to set this register file.

8.1 REGISTER FILE CONFIGURATION

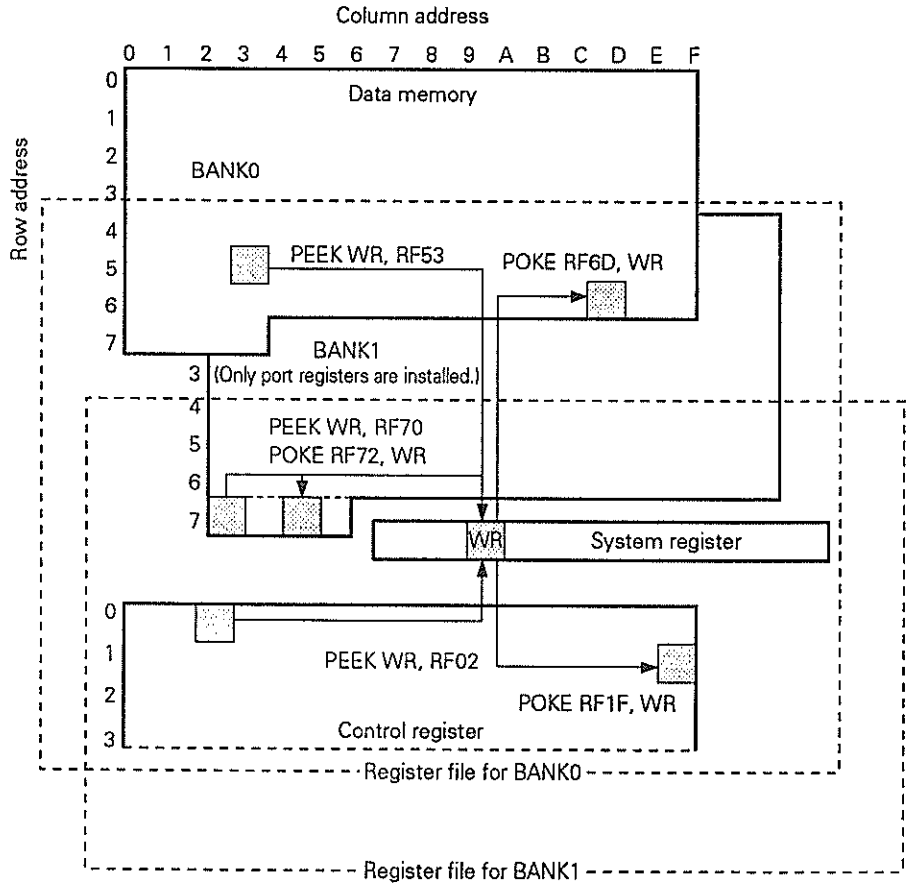
Fig. 8-1 shows the register file configuration and access to the register file using the PEEK and POKE instructions.

Control registers are allocated to addresses 00H to 3FH irrespective of banks.

Therefore, the accessible address range using the PEEK and POKE instructions are addresses 00H to 3FH for control registers and addresses 40H to 7FH specified with BANK, in general data memory. Memory corresponding to this range is called a register file.

Control registers in the in-circuit emulator IE-17K are allocated to addresses 80H to BFH in order to make debugging easy.

Fig. 8-1 Register File Configuration and Accessing the Register File Using the PEEK and POKE Instructions



8.2 CONTROL REGISTER

The control register consists of 64 nibbles (64 words by 4 bits) allocated to address locations 00H to 3FH in the register file. See **Fig. 21-2** for the configuration of the control register.

Only 26 nibbles in the control register are actually used. The remaining 38 nibbles are registers not used. Data should not be read from or written to these registers.

There are two types of control registers, both of which occupy one nibble of memory. One type is read/write (R/W), and the other is read-only (R).

Note that when the following read/write (R/W) flags are read, the read data is always 0.

- WDTRES (RF: 03H, bit 3)
- WDTEN (RF: 03H, bit 0)
- TM0RES (RF: 11H, bit 2)
- TM1RES (RF: 12H, bit 2)
- BTMRES (RE: 13H, bit 2)
- ADCSTRT (RF: 20H, bit 0)

Within the four bits of data in a nibble, there are bits which are fixed at 0 and will therefore always be read as 0. These bits remain fixed at 0 even when an attempt is made to write to them.

Attempting to read data in the unused register address area (38 nibbles) will yield unpredictable values. In addition, attempting to write to this area has no effect.

9. DATA BUFFER (DBF)

The data buffer consists of four nibbles allocated in addresses 0CH to 0FH in BANK0.

The data buffer acts as a data storage area for the CPU peripheral hardware (address register, serial interface, timer 0, timer 1, basic internal timer, and A/D converter) through use of the GET and PUT instructions. It also acts as data storage used for receiving and transferring data. By using the MOVT DBF, and @AR instructions, fixed data in program memory can be read into the data buffer.

9.1 DATA BUFFER CONFIGURATION

Fig. 9-1 shows the allocation of the data buffer in data memory.

As shown in Fig. 9-1, the data buffer is allocated in address locations 0CH to 0FH in BANK0 and consists of 4 nibbles (4 × 4 bits).

Fig. 9-1 Allocation of the Data Buffer

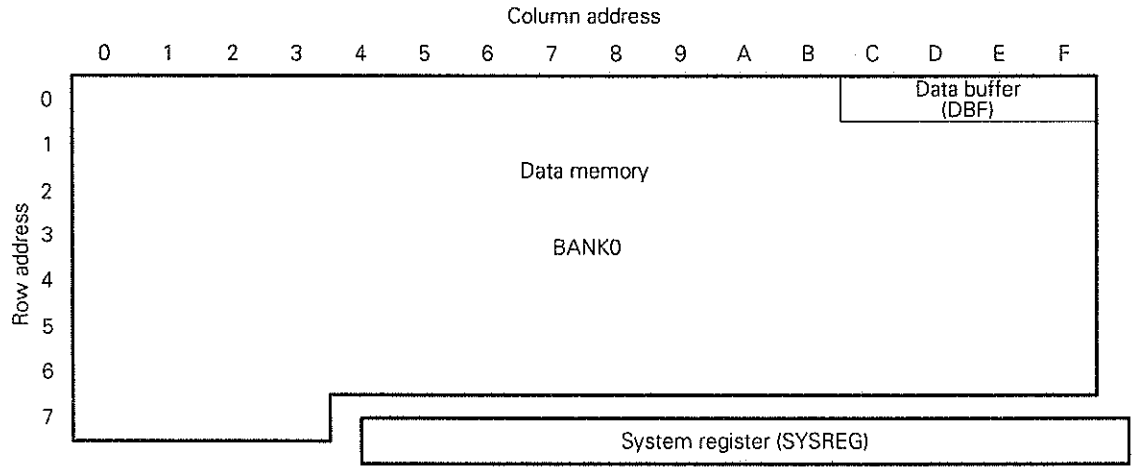


Fig. 9-2 shows the configuration of the data buffer. As shown in Fig. 9-2, the data buffer is made up of sixteen bits with its least significant bit in bit 0 of address 0FH and its most significant bit in bit 3 of address 0CH.

Fig. 9-2 Data Buffer Configuration

Data memory BANK0	Address	0CH				0DH				0EH				0FH			
	Bit	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0	b_3	b_2	b_1	b_0
Data buffer	Bit	b_{15}	b_{14}	b_{13}	b_{12}	b_{11}	b_{10}	b_9	b_8	b_7	b_6	b_5	b_4	b_3	b_2	b_1	b_0
	Symbol	DBF3				DBF2				DBF1				DBF0			
	Data	^ MSB v				Data											^ LSB v

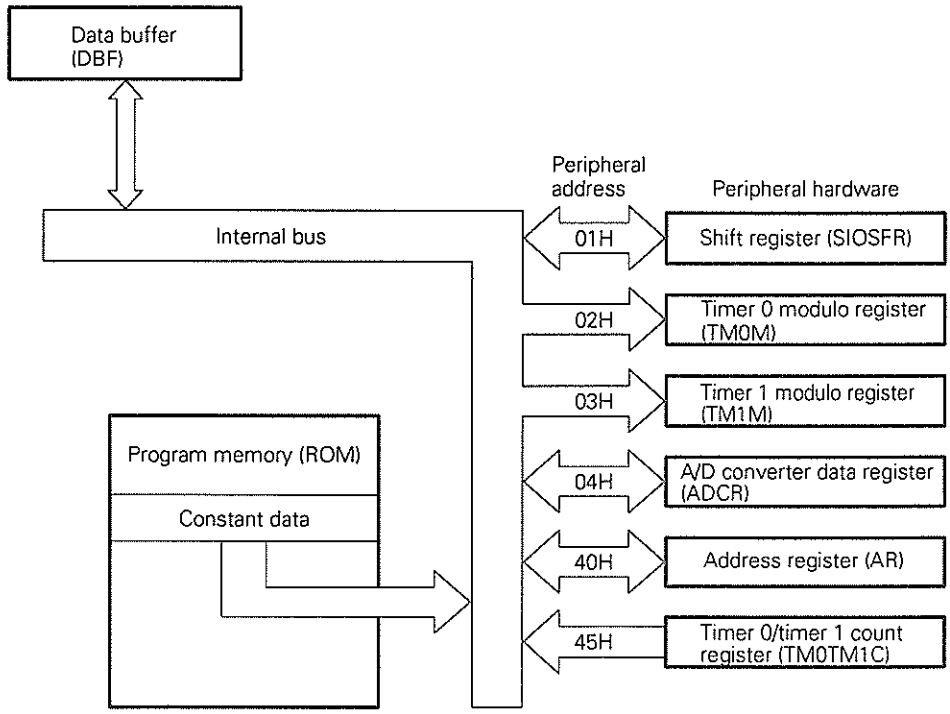
Because the data buffer is allocated in data memory, it can be used in any of the data memory manipulation instructions.

9.2 FUNCTIONS OF THE DATA BUFFER

The data buffer has two separate functions.

The data buffer is used for data transfer with peripheral hardware. The data buffer is also used for reading constant data in program memory. Fig. 9-3 shows the relationship between the data buffer and peripheral hardware.

Fig. 9-3 Relationship Between the Data Buffer and Peripheral Hardware



10. ALU BLOCK

The ALU is used for performing arithmetic operations, logical operations, bit evaluations, comparison evaluations, and rotations on 4-bit data.

10.1 ALU BLOCK CONFIGURATION

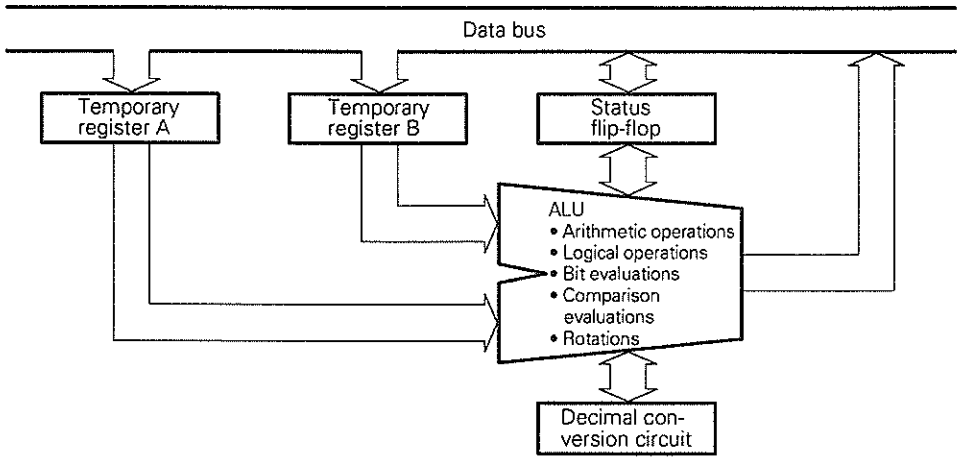
Fig. 10-1 shows the configuration of the ALU block.

As shown in Fig. 10-1, the ALU block consists of the main 4-bit data processor, temporary registers A and B, the status flip-flop for controlling the status of the ALU, and the decimal conversion circuit for use during arithmetic operations in BCD.

As shown in Fig. 10-1, the status flip-flop consists of the following flags: Zero flag flip-flop, carry flag flip-flop, compare flag flip-flop, and the BCD flag flip-flop.

Each flag in the status flip-flop corresponds directly to a flag in the program status word (PSWORD: addresses 7EH, 7FH) located in the system register. The flags in the program status word are the following: Zero flag (Z), carry flag (CY), compare flag (CMP), and the BCD flag (BCD).

Fig. 10-1 Configuration of the ALU



Address	7EH	7FH			
Name	Program status word (PSWORD)				
Bit	b_0	b_3	b_2	b_1	b_0
Flag	BCD	CMP	CY	Z	IXE

Status flip-flop			
BCD flag flip-flop	CMP flag flip-flop	CY flag flip-flop	Z flag flip-flop

Function outline
Indicates when the result of an arithmetic operation is 0.
Stores the borrow or carry from an arithmetic operation.
Used to indicate whether to store the result of an arithmetic operation.
Used to indicate whether to perform decimal correction for arithmetic operations.

11. PORTS

11.1 PORT 0A ($P0A_0$, $P0A_1$, $P0A_2$, $P0A_3$)

Port 0A is a 4-bit input/output port with an output latch. It is mapped into address 70H of BANK0 in data memory. The output format is CMOS push-pull output.

Input or output can be specified in units of four bits. Input/output is specified by P0AGIO (bit 0 at address 2CH) in the register file.

When P0AGIO is 0, each pin of port 0A is used as input port. If a read instruction is executed for the port register, pin statuses are read.

When P0AGIO is 1, each pin of port 0A is used as output port and the contents written in the output latch are output to pins. If a read instruction is executed when pins are output ports, the contents of the output latch, rather than pin statuses, are fetched.

Port 0A contains a software controlled pull-up resistor. P0AGPU (bit 0 at address 0CH) of the register file is used to determine whether port 0A contains the pull-up resistor. When P0AGPU is 1, all 4-bit pins are pulled up. If P0AGPU is 0, the pull-up resistor is not contained.

At reset, P0AGIO and P0AGPU are set to 0 and all P0A pins become input ports without a pull-up resistor. The contents of the port output latch are 0.

Table 11-1 Writing into and Reading from the Port Register (0.70H)

P0AGIO RF: 2CH, bit 0	Pin input/output	BANK0 70H	
		Write	Read
0	Input	Possible Write to the P0A latch	P0A pin status
1	Output		P0A latch contents

11.2 PORT 0B ($P0B_0$, $P0B_1$, $P0B_2$, $P0B_3$)

Port 0B is a 4-bit input/output port with an output latch. It is mapped into address 71H of BANK0 in data memory. The output format is CMOS push-pull output.

Input or output can be specified in 4-bit units. Input/ output is specified by P0BGIO (bit 1 at address 2CH) in the register file.

When P0BGIO is 0, all pins of port 0B are used as input ports. If a read instruction is executed for the port register, pin statuses are read.

When P0BGIO is 1, all pins of port 0B are used as output ports. The contents written in the output latch are output to pins. If a read instruction is executed when pins are used as output ports, the contents of the output latch, rather than pin statuses, are fetched.

Port 0B contains a software controlled pull-up resistor. P0BGPU (bit 1 at address 0CH) is used to determine whether or not port 0B contains a pull-up resistor. When P0BGPU is 1, all 4-bit pins are pulled up. When P0BGPU is 0, a pull-up resistor is not contained.

At reset, P0BGIO and P0BGPU are 0 and all P0B pins are input ports without a pull-up resistor. The value of the port 0B output latch is 0.

Table 11-2 Writing into and Reading from the Port Register (0.71H)

P0BGIO RF: 2CH, bit 1	Pin input/output	BANK0 71H	
		Write	Read
0	Input	Possible Write to the P0B latch	P0B pin status
1	Output		P0B latch contents

11.3 PORT 0C (P0C0/ADC0, P0C1/ADC1, P0C2/ADC2, P0C3/ADC3)

Port 0C is a 4-bit input/output port with an output latch. It is mapped into address 72H of BANK0 in data memory. The output format is CMOS push-pull output.

Input or output can be specified bit-by-bit. Input/output can be specified by P0CBIO0 to P0CBIO3 (address 1CH) in the register file.

If P0CBIOn is 0 (n = 0 to 3), the P0Cn pins are used as input port. If a data read instruction is executed for the port register, the pin statuses are read. If P0CBIOn is 1 (n = 0 to 3), the P0Cn pins are used as output port and the contents written in the output latch are output to pins. If a read instruction is executed when pins are used as output ports, the contents of the latch, rather than pin statuses, are fetched.

At reset, P0CBIO0 to P0CBIO3 are 0 and all P0C pins are input ports. The contents of the port output latch are 0.

Port 0C can also be used as an analog input to the A/D converter. P0C0IDI to P0C3IDI (1BH address) in the register file are used to switch the port and analog input pin.

If P0CnIDI is 0 (n = 0 to 3), the P0Cn/ADCn pin functions as a port. If P0CnIDI is 1 (n = 0 to 3), the P0Cn/ADCn pin functions as the analog input pin of the A/D converter.

ADCCH0 and ADCCH1 (bits 1 and 0 at address 22H) in the register file are used to select the input pin for A/D conversion.

To use P0C pins as A/D converter input pins, set P0CBIOn = 0 so that they are set as input ports. (See **Chapter 14.**)

At reset, P0CBIO0 to P0CBIO3, P0C0IDI to P0C3IDI, ADCCH0, and ADCCH1 are set to 0 and the P0C pins are used as input ports.

Table 11-3 Switching the Port and A/D Converter

(n = 0 to 3)

P0CnIDI RF: 1BH	P0CBIOn RF: 1CH	Function	BANK0 72H	
			Write	Read
0	0	Input port	Possible P0C latch	Pin status
	1	Output port	Possible P0C latch	P0C latch contents
1	0	A/D converter analog input[Note 1]	Possible P0C latch	P0C latch contents
	1	Output port and A/D converter analog input[Note 2]	Possible P0C latch	P0C latch contents

Notes 1. Normal setting when the pins are used as A/D converter analog input pins.

2. Functions as an output port. The analog input voltage is changed by the output from the port. To use the pins for analog input, be sure to set P0CBIOn to 0.

11.4 PORT 0D (P0D0/$\overline{SCK}$, P0D1/SO, P0D2/SI, P0D3/$\overline{TM0OUT}$)

Port 0D is a 4-bit input/output port with an output latch. It is mapped into address 73H of BANK0 in data memory. The output format is N-ch open-drain output. The mask option can be used to specify that a pin contain a pull-up resistor bit-by-bit.

Input or output can be specified bit-by-bit. Input/output is specified with P0DBIO0 to P0DBIO3 (address 2BH) in the register file.

If P0DBIOn is 0 (n = 0 to 3), the P0Dn pins are used as input port. Pin statuses are read if a data read instruction is executed for the port register. If P0DBIOn is 1, the P0Dn pins are used as output port and the value written in the output latch are output to pins. If a data read instruction is executed when pins are used as output ports, the output latch value, rather than pin statuses, is fetched.

At reset, P0DBIOn is set to 0 and all P0D pins become input ports. The contents of the port output latch become 0. The output latch contents remain unchanged even if P0DBIOn changes from 1 to 0.

Port 0D can also be used for serial interface input/output or timer 0 output. SIOEN (0BH bit 0) in the register file is used to switch ports (P0D0 to P0D2) to serial interface input/output ($\overline{SCK}$, SO, SI) and vice versa. TM0OSEL (bit 3 at address 0BH) in the register file is used to switch a port (P0D3) to timer 0 output ($\overline{TM0OUT}$) and vice versa. If TM0OSEL = 1 is selected, 1 is output at timer 0 reset. This output is inverted every time a timer 0 count value matches the modulo register contents.

Table 11-4 Register File Contents and Pin Functions

(n = 0 to 3)

Register file value			Pin function			
TM0OSEL RF: 0BH Bit 3	SIOEN RF: 0BH Bit 0	P0DBIOn RF: 2BH Bit n	P0D0/$\overline{SCK}$	P0D1/SO	P0D2/SI	P0D3/$\overline{TM0OUT}$
0	0	0	Input port			
		1	Output port			
	1	0	$\overline{SCK}$	SO	SI	Input port
		1				Output port
1	0	0	Input port			$\overline{TM0OUT}$
		1	Output port			
	1	0	$\overline{SCK}$	SO	SI	
		1				

Table 11-5 Contents Read from the Port Register (0.73H)

Port mode		Contents read from the port register (0.73H)
Input port		Pin status
Output port		Output latch contents
$\overline{SCK}$	An internal clock is selected as a serial clock.	Output latch contents
	An external clock is selected as a serial clock.	Pin status
SI		Pin status
SO		Not defined
$\overline{TM0OUT}$		Output latch contents

Caution Using the serial interface causes the output latch for the $P0D_1$/SO pin to be affected by the contents of the SIOSFR (shift register). So, reset the output latch before using the pin as output port.

11.5 PORT 1A ($P1A_0$, $P1A_1$, $P1A_2$, $P1A_3$)

Port 1A is a 4-bit input/output port with an output latch. It is mapped into address 70H of BANK1 in data memory. The output format is N-ch open-drain output. The mask option can be used to specify that a pin contain a pull-up resistor bit-by-bit.

Input or output can be specified in units of four bits. Input/output is specified by P1AGIO (bit 2 at address 2CH) in the register file.

When P1AGIO is 0, each pin of port 1A is used as input port. If a read instruction is executed for the port register, pin statuses are read. When P1AGIO is 1, each pin of port 1A is used as output port and the contents written in the output latch are output to pins. If a read instruction is executed when pins are output ports, the contents of the output latch, rather than pin statuses, are fetched.

At reset, P1AGIO is set to 0 and all P1A pins become input ports. The contents of the port output latch are 0.

Table 11-6 Writing into and Reading from the Port Register (1.70H)

(n = 0 to 3)

P1AGIOn RF: 2CH, bit 2	Pin input/output	BANK1 70H	
		Write	Read
0	Input	Possible	P1A pin status
1	Output	Write to the P1A latch	P1A latch contents

11.6 PORT 1B ($P1B_0$)

Port 1B is a 1-bit input-dedicated port. It is mapped into address 71H of BANK1 in data memory. The mask option can be used to specify that pull-up resistors be contained in $P1B_0$ pins.

Port 1B is the input-dedicated port. At reading, only the least significant bit is valid and a value is read into it. At writing, no value changes. Value 0 is always read into the three high-order bits of the port register.

12. 8-BIT TIMER COUNTER (TM0, TM1)

Timer 0 (TM0) and timer 1 (TM1) are available as 8 bit-timer counters.

By using the timer 0 counting signal as the timer 1 count pulse, these two 8-bit counters can be used as one 16-bit counter.

The timers are controlled by hardware operation with the PUT/GET instruction or by register operation with the PEEK/POKE instruction in the register file.

12.1 CONFIGURATION OF 8-BIT TIMER COUNTERS

Fig. 12-1 shows the configuration of the 8-bit timer counters. An 8-bit timer counter consists of an 8-bit counter register, 8-bit modulo register, comparator (compares counter register values and modulo register values), and selector (for count pulse selection).

Cautions 1. The modulo register is a write-only register.

2. The counter register is a read-only register.

Fig. 12-1 Configuration of the 8-Bit Timer Counters

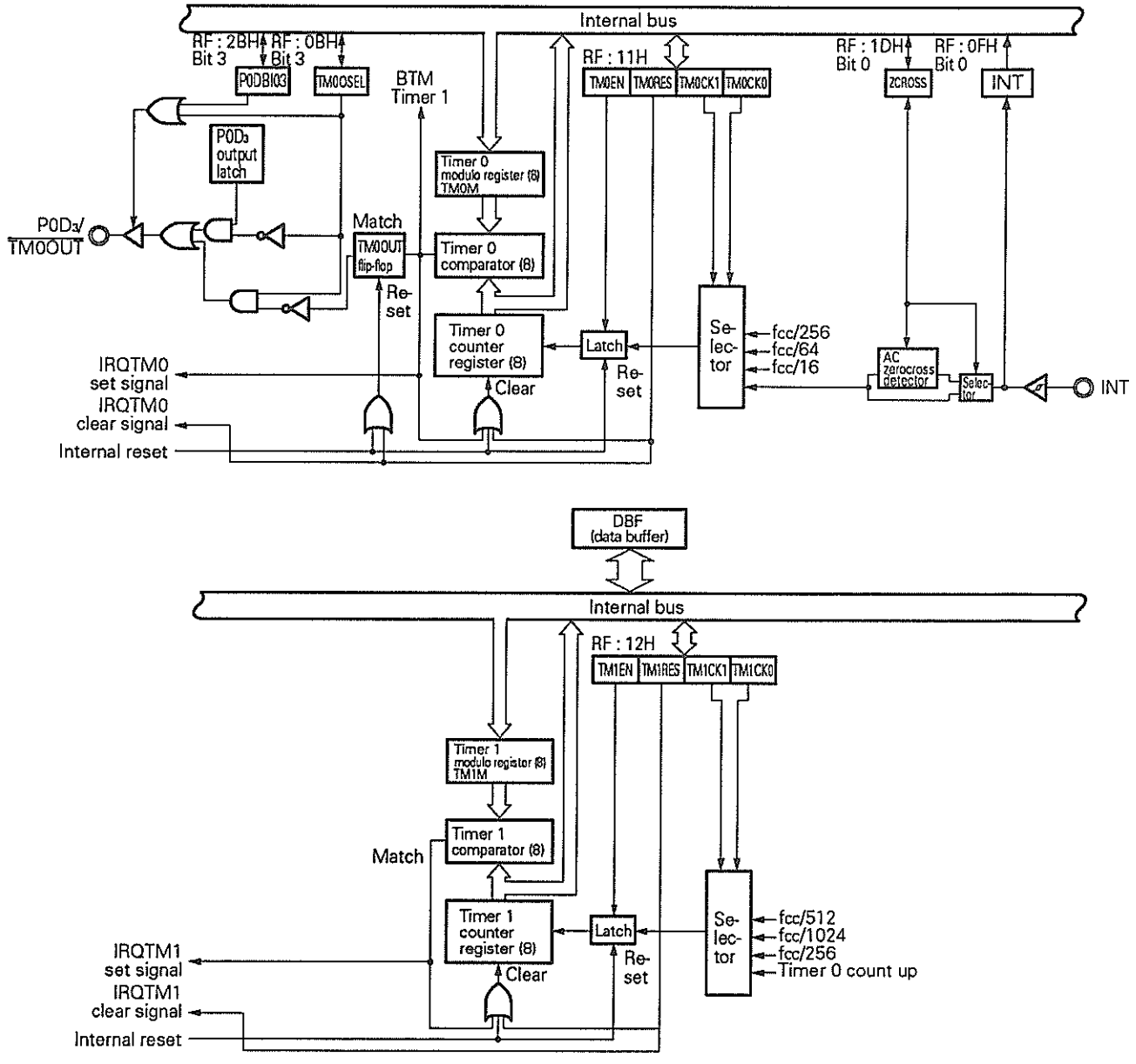


Fig. 12-2 Timer 0 Mode Register

RF: 11H

	Bit 3	Bit 2	Bit 1	Bit 0
	TM0EN	TM0RES	TM0CK1	TM0CK0
Read/write	R/W			
Initial value when reset	0	0	0	0

Read = R, write = W

TM0CK1	TM0CK0	Selects the count pulse of timer 0.
0	0	fcc/256
0	1	fcc/64
1	0	fcc/16
1	1	INT pin

TM0RES	Resets timer 0.
0	No effect on timer 0
1	The timer 0 count register and IRQTM0 are reset.

Remark TM0RES is automatically cleared to 0 after it is set to 1. 0 is always read.

TM0EN	Instruction to start timer 0.
0	Timer 0 stops counting.
1	Timer 0 starts counting.

Remark TM0EN can be used as the timer 0 status flag. (1: Counting, 0: Stopped counting)

Fig. 12-3 Timer 1 Mode Register

RF: 12H

	Bit 3	Bit 2	Bit 1	Bit 0
	TM1EN	TM1RES	TM1CK1	TM1CK0
Read/write	R/W			
Initial value when reset	1	0	0	0

Read = R, write = W

TM1CK1	TM1CK0	Selects the count pulse of timer 1.
0	0	fcc/512
0	1	fcc/1024
1	0	fcc/256
1	1	Count up signal from timer 0

TM1RES	Resets timer 1.
0	No effect on timer 1
1	The timer 1 count register and IRQTM1 are reset.

Remark TM1RES is automatically cleared to 0 after it is set to 1. 0 is always read.

TM1EN	Instruction to start timer 1
0	Timer 1 stops counting.
1	Timer 1 starts counting.

Remark TM1EN can be used as the timer 1 status flag. (1: Counting, 0: Stopped counting)

13. BASIC INTERVAL TIMER (BTM)

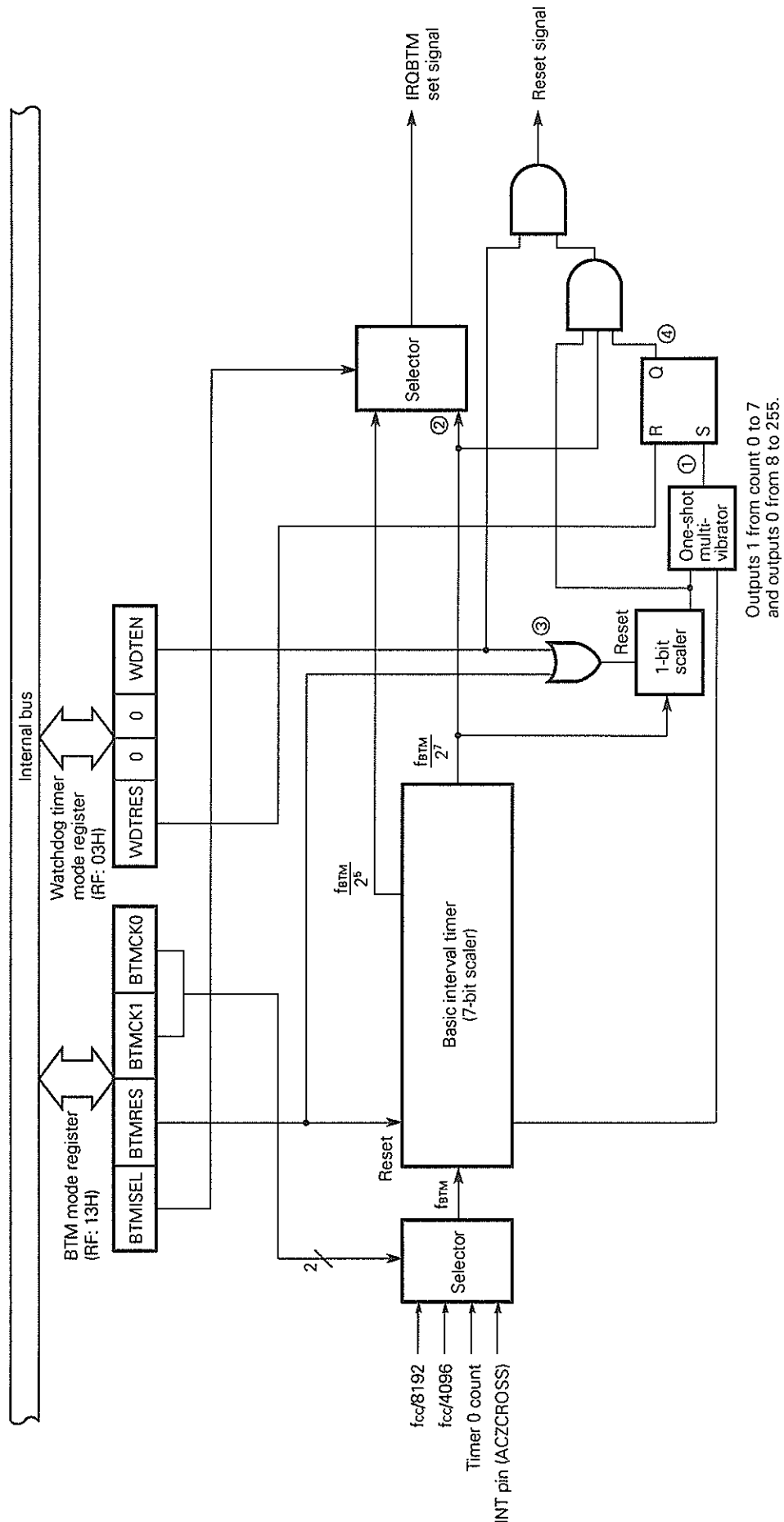
The μPD17136B provides a 7-bit basic interval timer. This timer has the following functions:

(1) Reference time generation
(2) Selection and counting of a wait time when standby mode is released
(3) Watchdog timer operation for detecting software errors (infinite loops, etc.)

13.1 CONFIGURATION OF THE BASIC INTERVAL TIMER

Fig. 13-1 shows the configuration of the basic interval timer.

Fig. 13-1 Configuration of the Basic Interval Timer



Remark ① to ④ in the figure indicate the signals in the timing chart in Fig. 13-4.

13.2 REGISTERS FOR CONTROLLING THE BASIC INTERVAL TIMER

The basic interval timer is controlled by the BTM mode register and watchdog timer mode register. Fig. 13-2 and 13-3 show the configurations of the registers.

Fig. 13-2 BTM Mode Register

RF: 13H

	Bit 3	Bit 2	Bit 1	Bit 0
	BTMISEL	BTMRES	BTMCK1	BTMCK0
Read/write	R/W			
Initial value when reset	0	0	0	0

Read = R, write = W

BTMCK1	BTMCK0	Selects the count pulse of the basic interval timer (BTM).
0	0	fcc/8192
0	1	fcc/4096
1	0	Timer 0 count up
1	1	INT pin (When ZCROSS = 1, information on the INT pin sent via the AC zerocross detection circuit)

BTMRES	Resets the basic interval timer (BTM).
0	Does not affect the basic interval timer (BTM).
1	Resets the counter of the basic interval timer (BTM).

Remark BTMRES is automatically cleared to 0 after it is set to 1. 0 is always read.

BTMISEL	Selects the interval time.
0	Sets the interval time for the 128-count pulse.
1	Sets the interval time for the 32-count pulse.

Fig. 13-3 Watchdog Timer Mode Register

RF: 03H

	Bit 3	Bit 2	Bit 1	Bit 0
	WDTRES	0	0	WDTEN
Read/write	R/W			
Initial value when reset	0	0	0	0

Read = R, write = W

WDTEN	Enables the watchdog timer function.
0	Puts the watchdog timer in stop status.
1	Starts watchdog timer operation.

Remarks 1. WDTEN cannot be cleared to 0 by the program.

2. WDTEN is automatically cleared to 0 after it is set to 1. 0 is always read.

WDTRES	Resets the watchdog timer.
0	Does not affect the watchdog timer.
1	Resets the flip-flop used to retain a BTM overflow carry used for the watchdog timer.

Remark WDTRES is automatically cleared to 0 after it is set to 1. 0 is always read.

13.3 WATCHDOG TIMER FUNCTION

13.3.1 Overview of the Watchdog Timer

The watchdog timer is a counter that generates a reset signal at constant intervals. When the generation of a reset signal is being disabled every time by the program, this function enables the system to be reset (starting from address 0000H) when the system hangs up (the watchdog timer is not reset within the expected time) for some reason, such as due to external noise.

Even if a program branches to an unexpected routine due to external noise and enters an infinite loop, the system can be recovered within a certain time by the reset signal that is generated by the watchdog timer.

13.3.2 Operation of the Watchdog Timer

If WDTEN is set to 1, the 1-bit scaler starts operating, causing the basic interval timer to operate as an 8-bit watchdog timer.

Once the watchdog timer runs, the watchdog timer function can be stopped only when the device is reset and WDTEN is cleared to 0.

A reset by the watchdog timer can be disabled in the following two ways:

(1) Repeating WDTRES setting in the program
(2) Repeating BTMRES setting in the program

For (1), it is necessary to set WDTRES while the watchdog timer count is between 8 and 191 (immediately before 192), as shown in Fig. 13-4. Therefore, the program must be written so that SET1 WDTRES is executed at least once in a shorter period than that required for the watchdog timer count to reach 184.

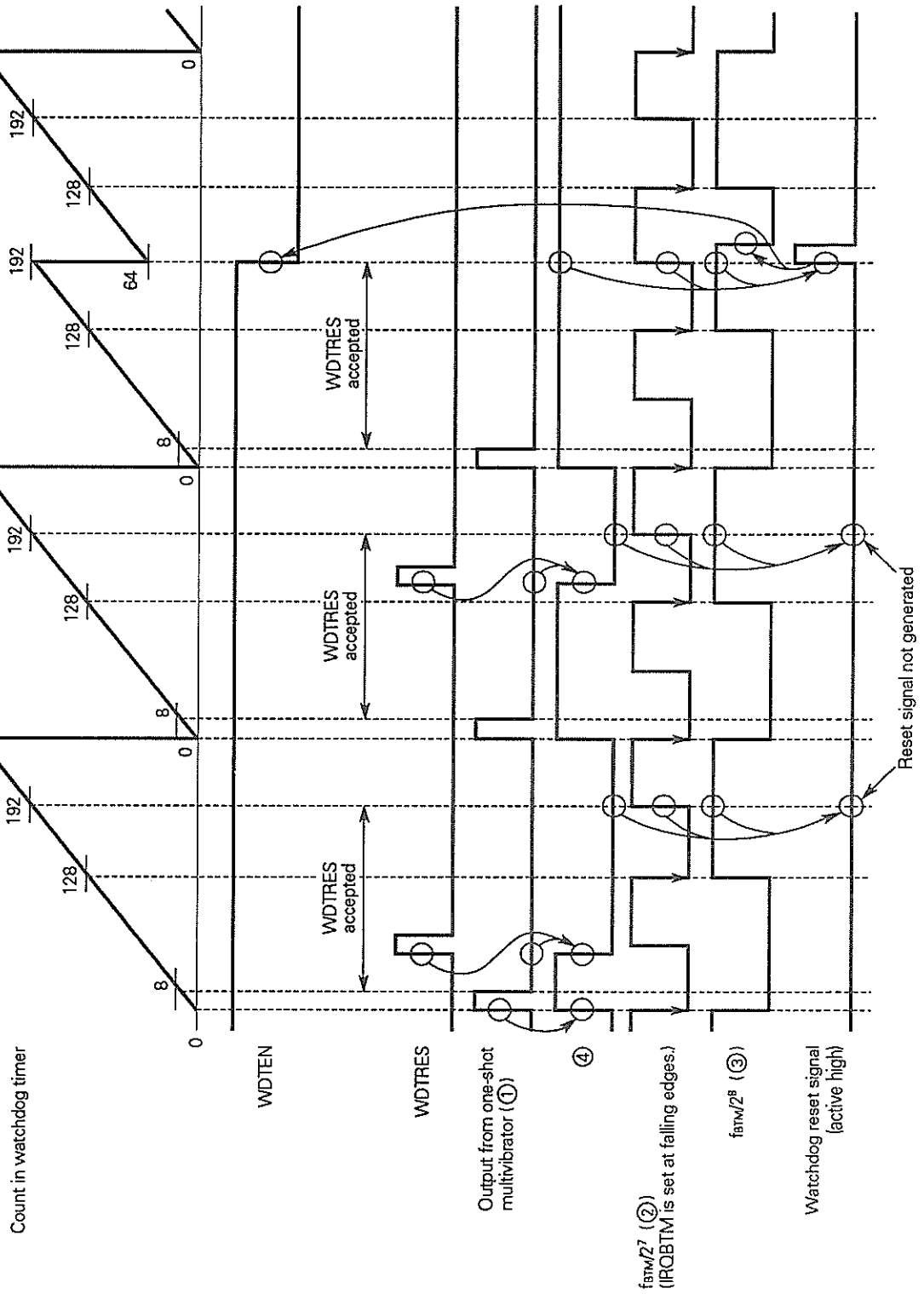
For (2), it is necessary to set BTMRES before the basic interval timer (BTM) count to reach 128. Therefore, the program must be written so that SET1 BTMRES is executed at least once in a shorter period than that required for the basic interval timer count to reach 128. However, using this method, interrupt handling by the basic interval timer is disabled.

Caution Setting WDTEN does not reset the basic interval timer. So, set BTMRES before setting WDTEN, to reset the basic interval timer.

Example

```
        ⋮
SET1    BTMRES
SET2    WDTEN, WDTRES
        ⋮
```

Fig. 13-4 Timing Chart for the Watchdog Timer (When the WDTRES Flag is Used)



14. A/D CONVERTER

μPD17136B contains an 8-bit resolution A/D converter with 4-channel analog input (P0C0/ADC0 - P0C3/ADC3).

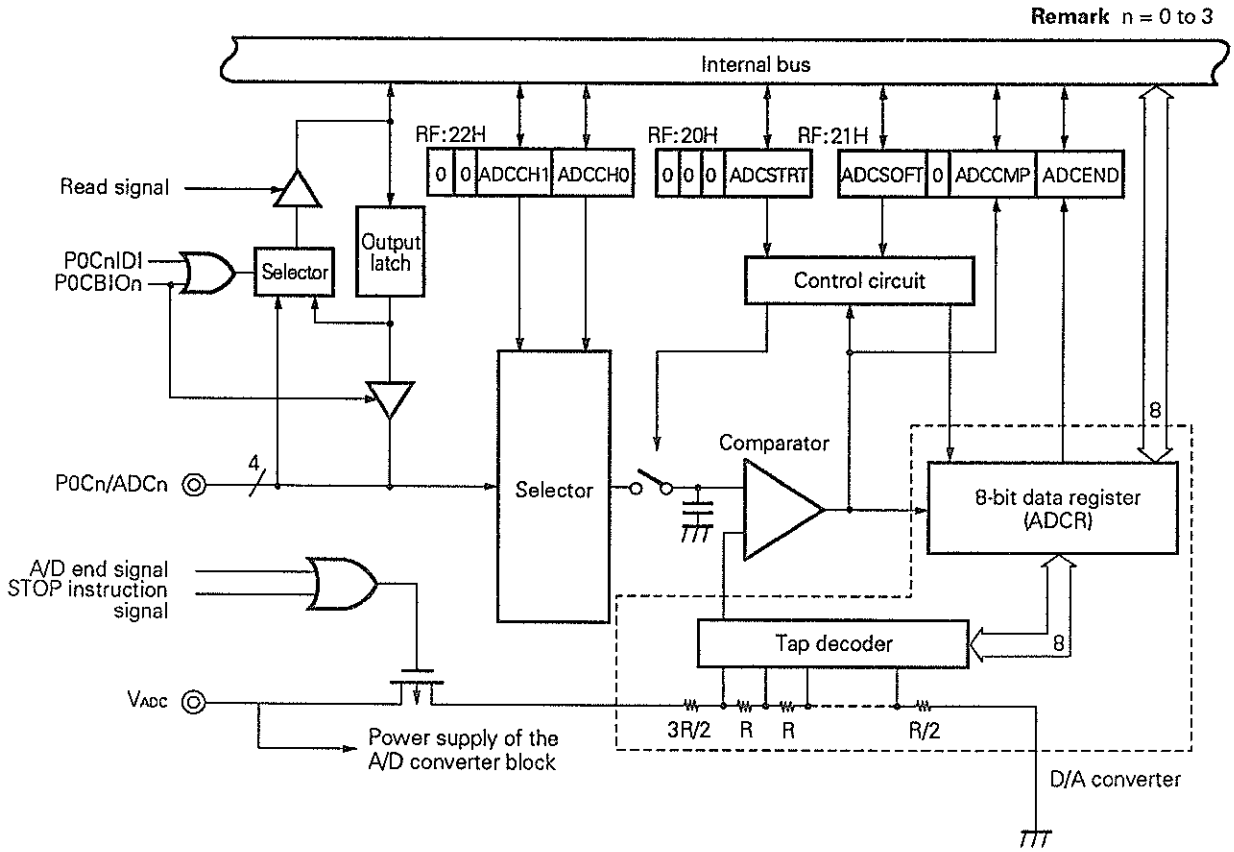
The A/D converter uses the successive approximation method. The following two operation modes are available:

① Continuous mode : 8-bit A/D conversion occurs starting at high-order bits.
② Single mode : Comparison occurs with an arbitrary voltage value set in the 8-bit data register.

14.1 A/D CONVERTER CONFIGURATION

Fig. 14-1 shows the A/D converter configuration.

Fig. 14-1 Block Diagram for the A/D Converter



Cautions 1. The 8-bit data register (ADCR) is cleared to 00H at the execution of STOP instruction.

2. Note that a current continues flowing between V_{ADC} and GND if a HALT instruction is executed during A/D conversion.

14.2 A/D CONVERTER FUNCTIONS

(1) ADC_0 - ADC_3 pins

These pins are used to input 4-channel analog voltage to the A/D converter. The A/D converter contains a sample hold circuit. Analog input voltage is internally retained during A/D conversion.

(2) V_{ADC} pin

This pin is used to input the reference voltage for the A/D converter and supply voltage of the A/D converter block.

A signal input to ADC_0 to ADC_3 is converted to a digital signal based on voltage applied across V_{ADC} and GND. To reduce the current consumption of the microcontroller, the A/D converter has a function for automatically stopping the current which flows into the V_{ADC} pin when the converter is not operating. Current flows into the V_{ADC} pin in the following cases.

① Continuous mode (ADCSOFT=0)
From when the ADCSTRT flag is set (1) until the ADCEND flag is set (1).

② Single mode (ADCSOFT=1)
From when the ADCSTRT flag is set (1) or from when a value of the 8-bit data register is written until the result of comparison by the comparator is written in the ADCCMP flag.

Caution A/D conversion stops if a HALT instruction is executed. Note that the V_{ADC} pin enter HALT mode while current is flowing. A/D conversion restarts when HALT mode is released. However, proper conversion results cannot be obtained because the value of ADCR is unpredictable.

Remark The A/D conversion stops when the STOP instruction is executed. The A/D converter is initialized and a current does not flow into the V_{ADC} pin. The A/D converter remains stopped after the STOP mode is released.

(3) 8-bit data register (ADCR)

In the continuous mode, this 8-bit data register stores A/D conversion results for successive approximation. It is read by the GET instruction. In the single mode, the data in this register is converted to analog voltage by the internal D/A converter and the comparator compares this voltage with an analog signal input from the ADCn pin. A value can be written in this register by using the PUT instruction.

(4) Comparator

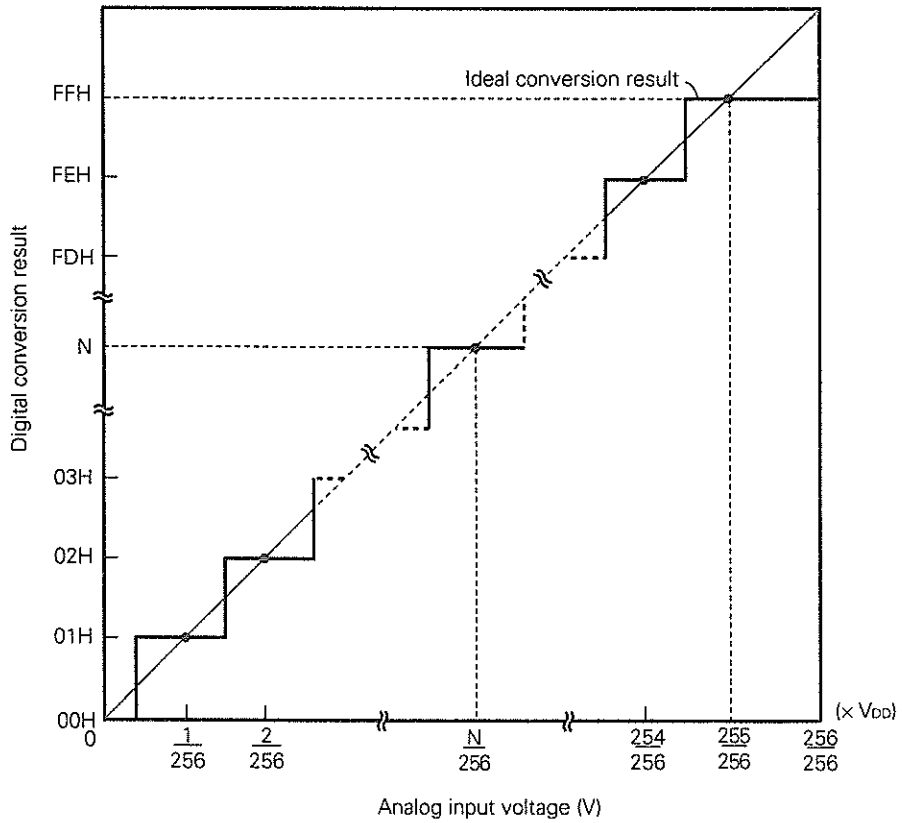
The comparator compares an analog input voltage with voltage output from the D/A converter. Value 1 is output if analog input voltage is higher. Value 0 is output if this voltage is lower. The comparison result is stored in the 8-bit data register (ADCR) in the continuous mode. It is stored in the ADCCMP flag in the single mode.

14.3 A/D CONVERTER OPERATION

The A/D converter operates in two modes: continuous mode and single mode. The mode can be switched by setting the ADCSOFT flag.

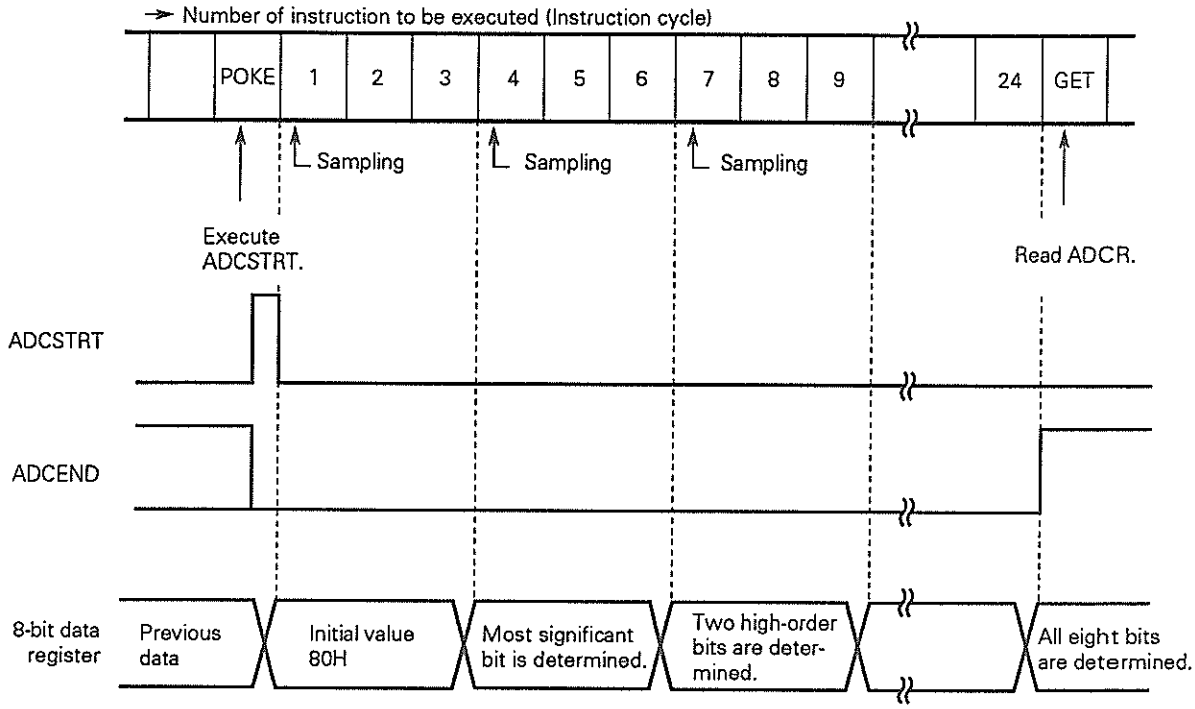
ADCSOFT	A/D converter operation mode
0	Continuous mode (A/D conversion)
1	Single mode (comparison)

Fig. 14-2 Relation between the Analog Input Voltage and Digital Conversion Result



(1) Continuous mode operation (A/D conversion) timing

Fig. 14-3 Continuous Mode Operation (A/D Conversion) Timing

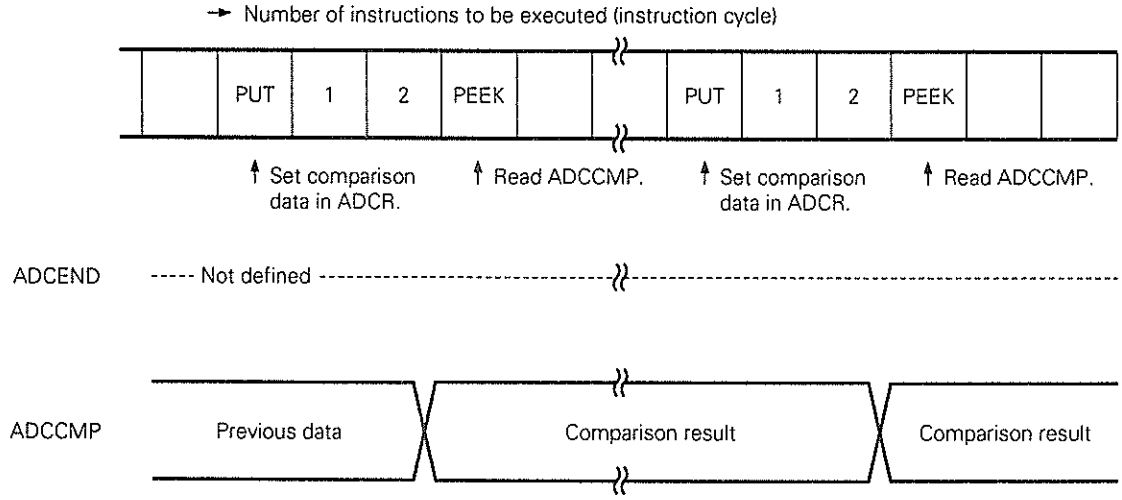


Caution Sampling is performed eight times for each A/D conversion. If the analog input voltage changes considerably during A/D conversion, accurate A/D conversion cannot be performed. To obtain accurate conversion, minimize any change in the analog input voltage during A/D conversion.

Time required for one sampling operation = 14/fcc (7 μs, at 2 MHz)
Sampling cycle period = 48/fcc (24 μs, at 2 MHz)

(2) Single mode operation (comparison) timing

Fig. 14-4 Single Mode Operation (Comparison) Timing



After data is set in ADCR (using the PUT instruction), the comparison result can be read after the third instruction.

Caution Before setting a value in ADCR, always set ADCSOFT to 1.
If ADCSOFT = 0, no value can be set in ADCR.
The PUT ADCR, DBF instruction is ineffective.

15. SERIAL INTERFACE (SIO)

The serial interface consists of an 8-bit shift register (SIOSFR), serial mode register, and serial clock counter. It is used for serial data input/output.

When SIOEN is set to 1, the pins of port 0D ($P0D_0/\overline{SCK}$, $P0D_1$/SO, $P0D_2$/SI) function as the pins of the serial interface. The serial interface operates in synchronization with the falling edge of the external or internal clock by setting SIOTS to 1. The detailed functions and operations are explained below.

15.1 FUNCTIONS OF THE SERIAL INTERFACE

This serial interface provides three signal lines: serial clock input pin ($\overline{SCK}$), serial data output pin (SO), and serial data input pin (SI). It allows 8 bits to be sent or received in synchronization with clocks. It can be connected to peripheral input/output devices using any method with a mode compatible to that used by the μPD7500 or 75X series.

(1) Serial clock

Three types of internal clocks and one type of external clock are able to be selected. If an internal clock is selected as a serial clock, it is automatically output to the $P0D_0/\overline{SCK}$ pin.

Table 15-1 Serial Clock

SIOCK1	SIOCK0	Serial clock to be selected
0	0	External clock input to the $\overline{SCK}$ pin
0	1	fcc/16
1	0	fcc/128
1	1	fcc/1024

(2) Transmission

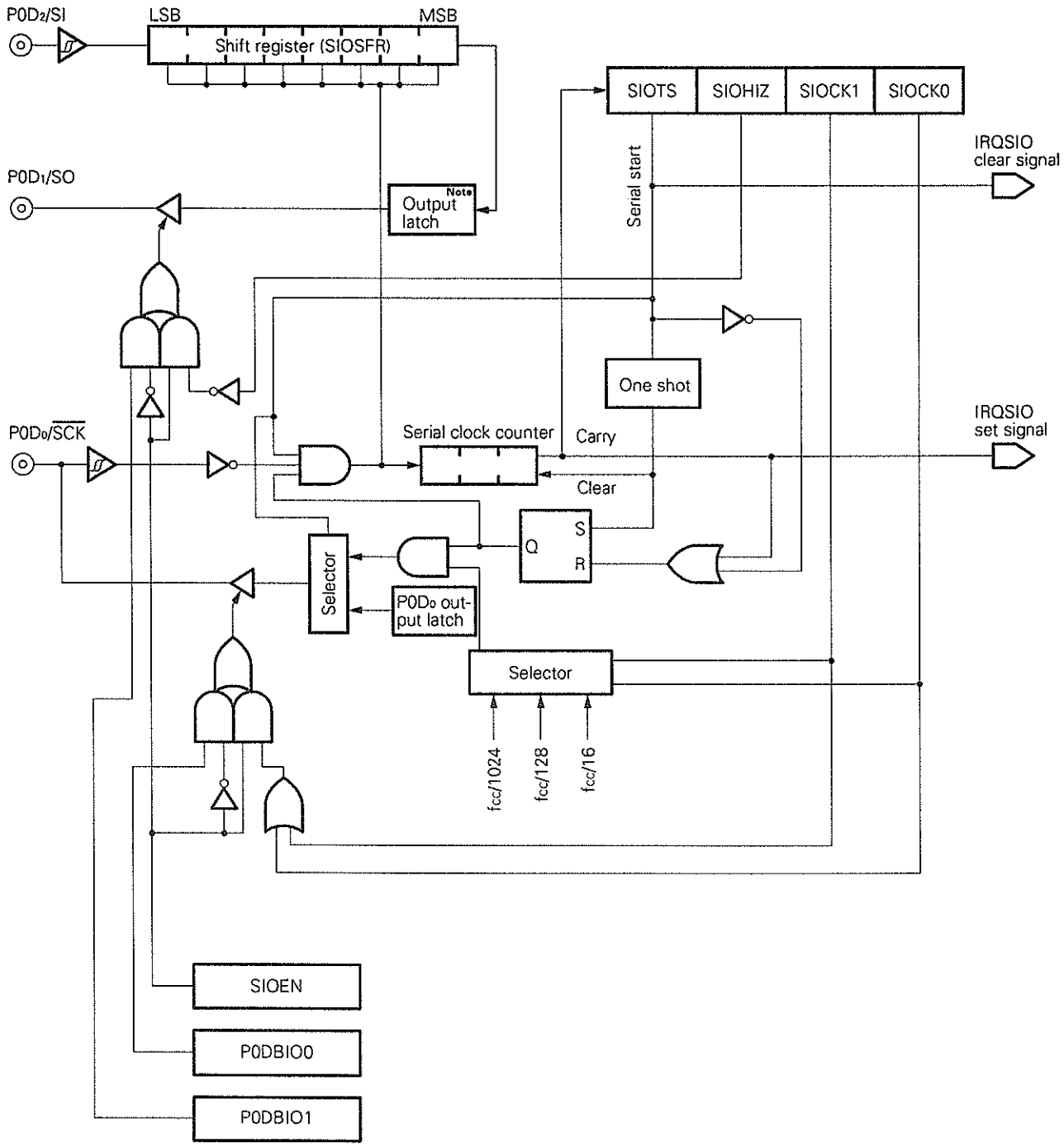
When SIOEN is set to 1, the pins of port 0D ($P0D_0/\overline{SCK}$, $P0D_1$/SO, $P0D_2$/SI) function as the pins of the serial interface. The serial interface operates in synchronization with the falling edge of the external or internal clock by setting SIOTS to 1. When SIOTS is set to 1, IRQSIO is automatically cleared.

Transmission starts from the most significant bit of the shift register in synchronization with the falling edge of the serial clock. SI pin information is stored in the shift register starting at the most significant bit in synchronization with the rising edge of the serial clock.

When the transmission of 8-bit data is completed, SIOTS is automatically cleared to 0 and IRQSIO is set to 1.

Remark Serial transmission starts only from the most significant bit of the shift register contents. It is not possible to start transmission from the least significant bit. SI pin status is always stored in the shift register in synchronization with the falling edge of the serial clock.

Fig. 15-1 Block Diagram of the Serial Interface



Note The output latch of the shift register is also used as that of the P0D1 pin. Therefore, executing an output instruction for the P0D1 pin changes the output latch status of the shift register.

15.2 3-WIRE SERIAL INTERFACE OPERATION MODES

Two modes can be used for the serial interface. If the serial interface function is selected, the P0D2/SI pin always takes in data in synchronization with the serial clock.

- 8-bit transmission and reception mode (simultaneous transmission and reception)
- 8-bit reception mode (with the SO pin in the high impedance status)

Table 15-2 Serial Interface Operation Mode

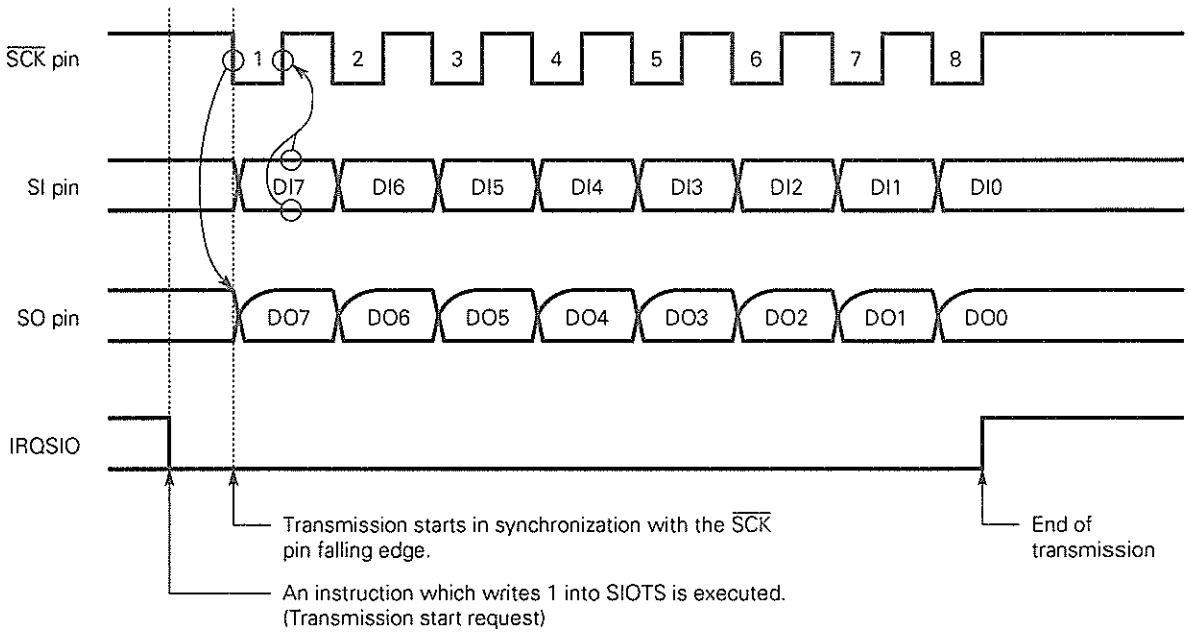
SIOEN	SIOHIZ	$P0D_2$/SI pin	$P0D_1$/SO pin	Serial interface operation mode
1	0	SI	SO	8-bit transmission and reception mode
1	1	SI	$P0D_1$ (input)	8-bit reception mode
0	×	$P0D_2$ (I/O)	$P0D_1$ (I/O)	General port mode

×: Don't care

(1) 8-bit transmission and reception mode (simultaneous transmission and reception)

Serial data input/output is controlled by a serial clock. The most significant bit of the shift register is output from the SO line with a falling edge of the serial clock ($\overline{SCK}$). The contents of the shift register is shifted one bit and at the same time, data on the SI line is loaded into the least significant bit of the shift register. The serial clock counter counts serial clock pulses. Every time it counts eight clocks, the internal interrupt request flag (IRQSIO) is set to 1.

Fig. 15-2 Timing of 8-Bit Transmission and Reception Mode (Simultaneous Transmission and Reception)



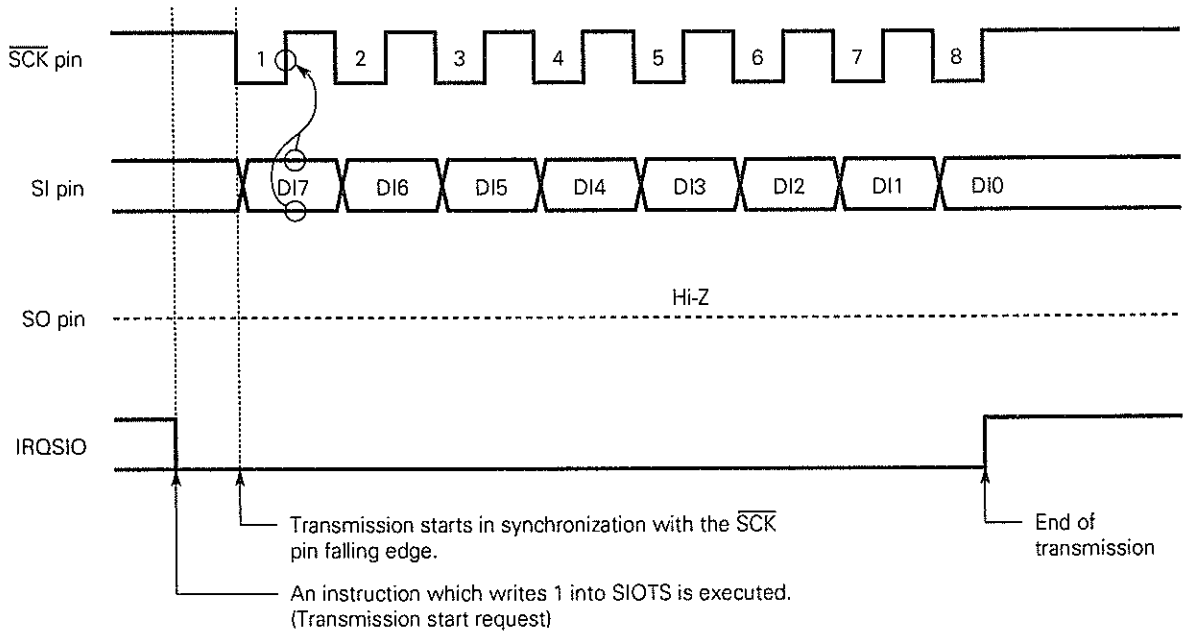
Remark DI : Input serial data
DO : Output serial data

(2) 8-bit reception mode (SO pin high impedance)

When SIOHIZ is 1, the P0D1/SO pin is in the high impedance status. If serial clock supply starts by writing 1 in SIOTS, only the reception function of the serial interface operates.

The P0D1/SO pin is in the high impedance status and can be used for input port (P0D1).

Fig. 15-3 Timing of 8-Bit Reception Mode



Remark DI : Input serial data

(3) Operation stop mode

If the value in SIOTS (RF: address 02H, bit 3) is 0, the serial interface enters operation stop mode. In this mode, no serial transfer occurs.

In this mode, the shift register does not perform shifting and can be used as an ordinary 8-bit register.

16. INTERRUPT FUNCTIONS

The μPD17136B has five interrupt sources: four internal interrupt functions and one external interrupt function. It can be used in various applications.

The interrupt control circuit of the μPD17136B has the features listed below. This circuit enables very high-speed interrupt handling.

(a) Used to determine whether an interrupt can be accepted with the interrupt mask enable flag (INTE) and interrupt enable flag (IPxxx).
(b) The interrupt request flag (IRQxxx) can be tested or cleared. (Interrupt generation can be checked by software.)
(c) Multiple interrupts are possible (up to three levels).
(d) Standby mode (STOP, HALT) can be released by an interrupt request. (Release conditions can be selected by the interrupt enable flag.)

Caution In interrupt handling, the bank register and the BCD, CMP, CY, Z, and IXE flags are saved in the stack automatically by the hardware for up to three levels of multiple interrupts. The DBF and WR are not saved by the hardware when peripheral hardware such as the timers or A/D converter is accessed in interrupt handling. It is recommended that the DBF and WR be saved in RAM by the software at the beginning of interrupt handling. Saved data can be loaded back into the DBF and WR immediately before the end of interrupt handling.

16.1 INTERRUPT SOURCE TYPES AND VECTOR ADDRESSES

For every interrupt in the μPD17136B, when the interrupt is accepted, a branch occurs to the vector address associated with the interrupt source. This method is called the vectored interrupt method. Table 16-1 lists the interrupt source types and vector addresses.

If two or more interrupt requests occur or multiple suspended interrupt requests are enabled at the same time, they are handled according to priorities shown in Table 16-1.

Table 16-1 Interrupt Source

Interrupt source	Priority	Vector address	IRQ flag	IP flag	IEG flag	Internal/ external	Remarks
INT pin (RF: 0FH, bit 0)	1	0005H	IRQ RF: 3FH, bit 0	IP RF: 2FH, bit 0	IEGMD0, 1 RF: 1FH	External INT	Rising edge or falling edge can be selected.
Timer 0	2	0004H	IRQTM0 RF: 3EH, bit 0	IPTM0 RF: 2FH, bit 1	–	Internal	
Timer 1	3	0003H	IRQTM1 RF: 3DH, bit 0	IPTM1 RF: 2FH, bit 2	–	Internal	
Basic interval timer	4	0002H	IRQBTM RF: 3CH, bit 0	IPBTM RF: 2FH, bit 3	–	Internal	
Serial interface	5	0001H	IRQSIO RF: 3BH, bit 0	IPSIO RF: 2EH, bit 0	–	Internal	

16.2 HARDWARE COMPONENTS OF THE INTERRUPT CONTROL CIRCUIT

The flags of the interrupt control circuit are explained below.

(1) Interrupt request flag and the interrupt enable flag

The interrupt request flag (IRQxxx) is set to 1 when an interrupt request occurs. When interrupt handling is executed, the flag is automatically cleared to 0.

An interrupt enable flag (IPxxx) is provided for each interrupt request flag. If the flag is 1, an interrupt is enabled. If it is 0, the interrupt is disabled.

(2) EI/DI instruction

The EI/DI instruction is used to determine whether an accepted interrupt is to be executed.

If the EI instruction is executed, the interrupt enable flag (INTE) for enabling is set. Since the INTE flag is not registered in the register file, flag status cannot be checked by instructions.

The DI instruction clears the INTE flag to 0 and disables all interrupts.

At reset the INTE flag is cleared to 0 and all interrupts are disabled.

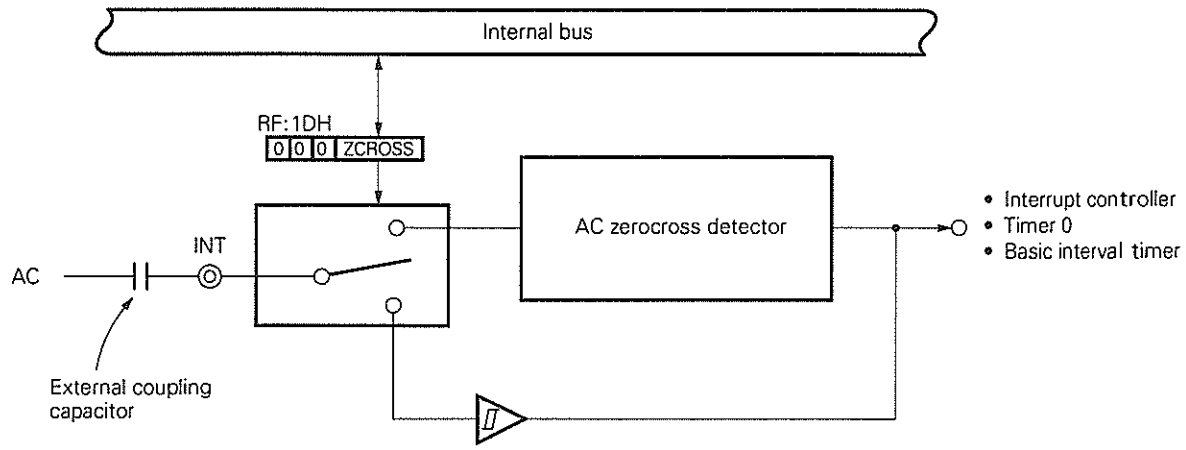
Table 16-2 Interrupt Request Flag and Interrupt Enable Flag

Interrupt request flag	Signal for setting the interrupt request flag	Interrupt enable flag
IRQ	Set by edge detection of an INT pin input signal. A detection edge is selected by IEGMD0 or IEGMD1.	IP
IRQTM0	Set by a match signal from timer 0.	IPTM0
IRQTM1	Set by a match signal from timer 1.	IPTM1
IRQBTM	Set by an overflow (reference time interval signal) from the basic interval timer.	IPBTM
IRQSIO	Set by a serial data transmission end signal from the serial interface.	IPSIO

17. AC ZEROCROSS DETECTOR

The INT pin is the interrupt signal input pin and timer count clock input pin. It also used as an AC zerocross detector input pin. This pin can be selected by writing 1 in ZCROSS (RF: 1DH bit 0).

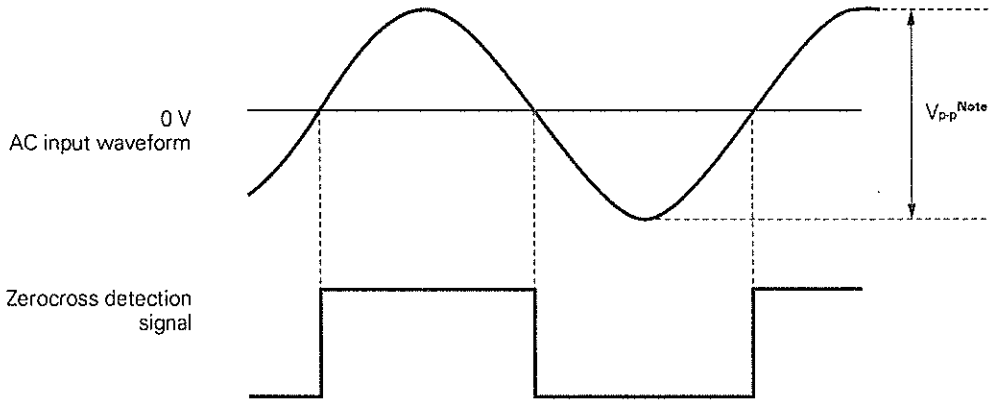
Fig. 17-1 Block Diagram for the AC Zerocross Detector



Caution When an AC zerocross detector is used, the current drain is slightly increased (typically by 15 μA). This is also true in standby mode. To limit the current drain, set ZCROSS to 0. Then, fix the input voltage at the INT pin to the high or low level.

The zerocross detector consists of a high gain amplifier which uses the self-bias method. It biases the input to the switching point and causes digital displacement in response to slight displacement of INT pin input. It detects changes of an AC signal from minus to plus and vice versa. This signal is input through the external coupling capacitor. The output signal changes from 0 to 1 and vice versa at each displacement point.

Fig. 17-2 Zerocross Detection Signal



Note When the INT pin is used as the input pin of the AC zerocross detector, the input voltage range must be 1.0 to 3.0 V_{p-p}. Since the AC zerocross detector cannot eliminate noise, input noise-free signals to the AC zerocross detector.

A pulse generated in the zerocross detector can be used as a timer 0 count pulse and basic interval timer count pulse in the same way as when the pulse does not go through the zerocross detector. The pulse is sent to the interrupt control circuit. Interrupt enable starts if an INT pin interrupt is enabled. To accept an interrupt, set IEGMD0 (RF: 1FH bit 0) and IEGMD1 (RF: 1FH bit 1) to select a signal rising edge, falling edge, or both rising and falling edges.

18. STANDBY FUNCTION

18.1 OVERVIEW OF THE STANDBY FUNCTION

The μPD17136B can reduce its current by using the standby function. The standby function supports STOP and HALT modes.

In the STOP mode, the system clock is stopped and the CPU current is reduced to almost only a leak current. This mode is useful in retaining data memory contents without operating the CPU.

In the HALT mode, the oscillation of the system clock continues. However, the system clock is not supplied to the CPU, stopping CPU operation. In this mode, current reduction is less than that in the STOP mode. However, since the system clock is oscillating, operation can be started immediately after the HALT mode is released. In both STOP and HALT modes, the statuses of the data memory, registers, and output latches of the output port used immediately before the standby mode is set are maintained (except STOP 0000B). Therefore, in order to lower consumption current for the entire system, input/output port statuses should be set beforehand.

Table 18-1 Standby Mode Status

		STOP mode	HALT mode
Programmed instruction		STOP instruction	HALT instruction
Clock oscillator		Oscillation stopped	Oscillation continued
Operation status	CPU	• Operation stopped	
	RAM	• The contents held immediately before setting standby mode are retained.	
	Port	• The status existing immediately before setting standby mode is retained.[Note]	
	TM0	• Operable only when the INT input is selected as the count pulse. • Stopped when the system clock is selected. (The count is retained.)	• Operable
	TM1	• Operation stopped. (The count is reset to 0.) (Count-up is also inhibited.)	• Operable
	BTM	• Operation stopped. (The count is retained.)	• Operable
	SIO	• Operable only when the external clock is selected as the serial clock.[Note]	• Operable
	A/D	• Operation stopped[Note] (ADCR ← 00H)	• Operable
	INT	• Operable	• Operable

Note When STOP 0000B is executed, all pins are set to input port mode even if the pins are used in dual-function mode.

Cautions 1. Always specify a NOP instruction immediately before STOP and HALT instructions.

2. When an interrupt request flag and the corresponding interrupt enable flag are both set, and the associated interrupt is specified as the standby mode release condition, the system does not enter the standby mode even if a STOP or HALT instruction is executed.

18.2 HALT MODE

18.2.1 Setting HALT Mode

Executing a HALT instruction sets HALT mode.

Operand $b_3b_2b_1b_0$ of the HALT instruction indicates the HALT mode release conditions.

Table 18-2 HALT Mode Release Conditions

Format: HALT $b_3b_2b_1b_0$B

Bit	HALT mode release conditions[Note 1]
b_3	When this bit is 1, release by IRQxxx is permitted.[Notes 2, 4]
b_2	Fixed at 0
b_1	When this bit is 1, forced release by IRQTM1 is permitted.[Notes 3, 4]
b_0	Fixed at 0

Notes 1. When HALT 0000B is specified, HALT mode can be released only by reset ($\overline{\text{RESET}}$ input or power-on/power-down reset).

2. IPxxx must be 1.

3. HALT mode is released regardless of the IPTM1 status.

4. If a HALT instruction is executed when IRQxxx = 1, the HALT instruction is ignored (treated as a NOP instruction), and HALT mode is not set.

18.2.2 Starting Address After HALT Mode is Released

The starting address depends on the release conditions and interrupt enable conditions.

Table 18-3 Starting Address After HALT Mode is Released

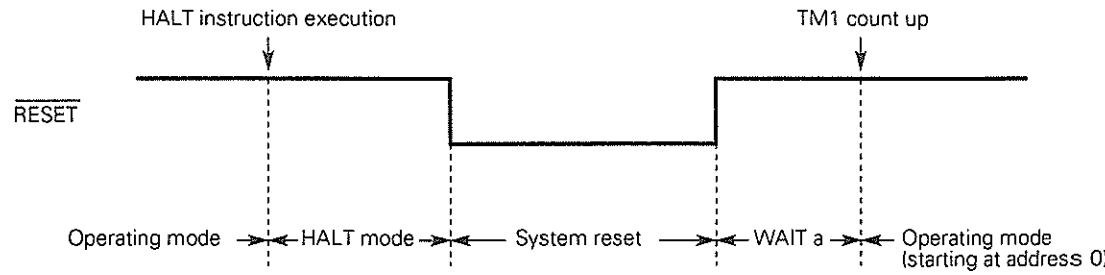
Release condition	Starting address after release
Reset[Note 1]	Address 0
IRQxxx[Note 2]	For DI, address subsequent to the HALT instruction
	For EI, interrupt vector (When more than one IRQxxx is set, the interrupt vector having the highest priority)

Notes 1. $\overline{\text{RESET}}$ input and power-on/power-down reset are valid.

2. Except when forced release is made with IRQTM1, IPxxx must be 1.

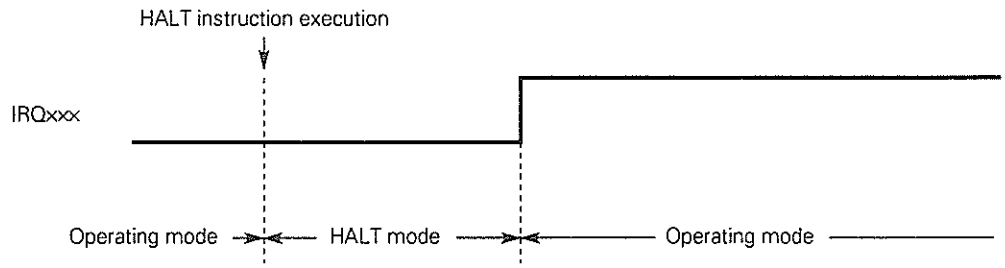
Fig. 18-1 Releasing HALT Mode

(a) Releasing HALT mode by $\overline{\text{RESET}}$ input

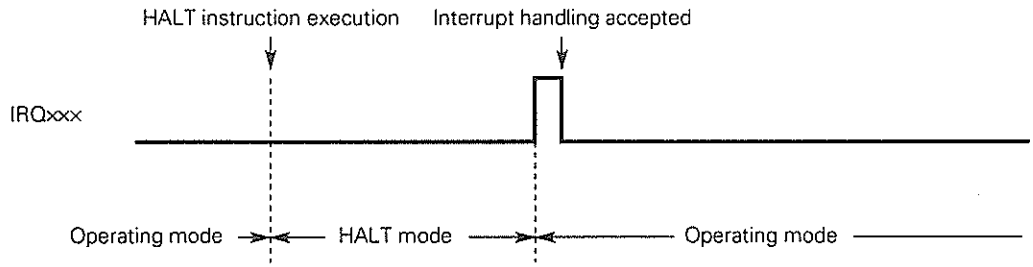


WAIT a : Wait time until TM1 counts 2 source clock pulses (system clock/512)
However, the wait time is the shortest when TM1 counts 0.5 source clock pulse because the TM1 count includes an error of the longest time minus 1.5 count.
$2 \times 512/f_{CC}$ (about 512 μs (the shortest time is about 128 μs) when f_{CC} is 2 MHz)

(b) Releasing HALT mode by IRQxxx (for DI)



(c) Releasing HALT mode by IRQxxx (for EI)



18.3 STOP MODE

18.3.1 Setting STOP Mode

Executing a STOP instruction results in STOP mode being set.

Operand $b_3b_2b_1b_0$ of the STOP instruction indicates the STOP mode release conditions.

Table 18-4 STOP Mode Release Conditions

Format: STOP $b_3b_2b_1b_0$B

Bit	STOP mode release condition[Note 1]
b_3	When this bit is 1, release by IRQxxx is permitted.[Note 2]
b_2	Fixed at 0
b_1	Fixed at 0
b_0	Fixed at 0

Notes 1. When STOP 0000B is specified, STOP mode can be released only with reset ($\overline{\text{RESET}}$ input or power-on/power-down reset). When STOP 0000B is executed, the microcomputer is initialized to the state existing immediately after the reset.

2. IPxxx must be 1. STOP mode cannot be released with IRQTM1.
If the STOP instruction is executed when IRQxxx = 1, the STOP instruction is ignored (treated as a NOP instruction), and STOP mode is not set.

18.3.2 Starting Address After STOP Mode is Released

The starting address depends on the release conditions and interrupt enable conditions.

Table 18-5 Starting Address After STOP Mode is Released

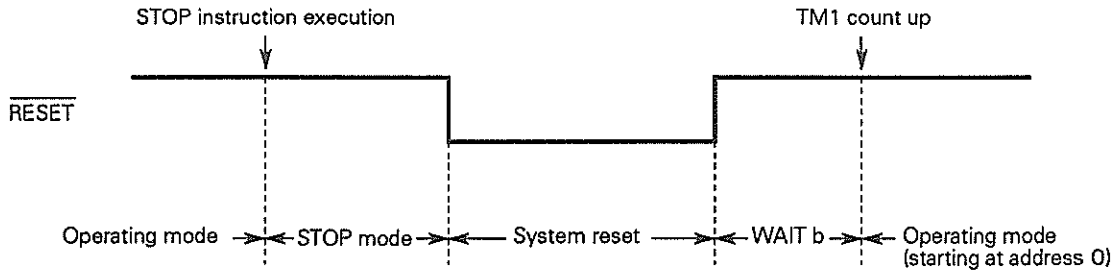
Release condition	Starting address after release
Reset[Note 1]	Address 0
IRQxxx[Note 2]	For DI, address subsequent to the STOP instruction
	For EI, interrupt vector (When more than one IRQxxx is set, the interrupt vector having the highest priority)

Notes 1. $\overline{\text{RESET}}$ input and power-on/power-down reset are valid.

2. IPxxx must be 1. STOP mode cannot be released with IRQTM1.

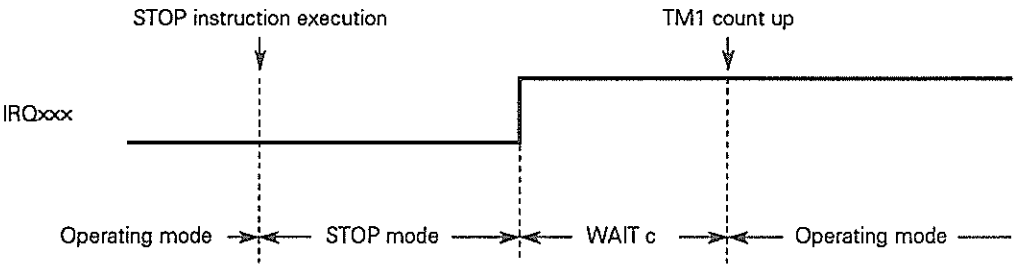
Fig. 18-2 Releasing STOP Mode

(a) Releasing STOP mode by $\overline{\text{RESET}}$ input



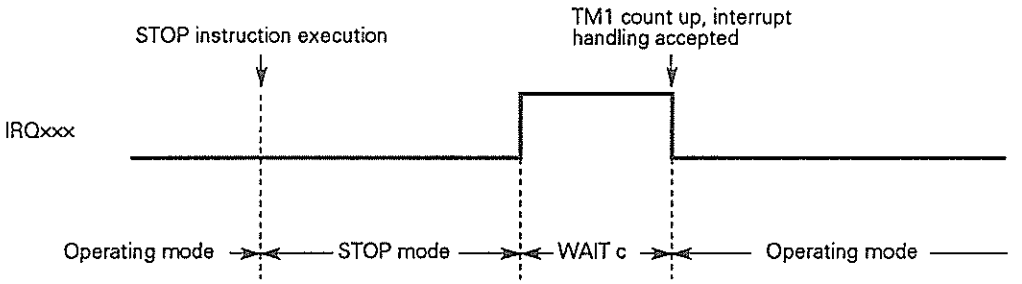
Wait b : Wait time until TM1 counts 2 source clock pulses (system clock/512)
However, the wait time is the shortest when TM1 counts 0.5 source clock pulse because the TM1 count includes an error of the longest time minus 1.5 count.
$2 \times 512/f_{CC} + \alpha$ (about 512 μs + α (the shortest time is about 128 μs + α) when f_{CC} is 2 MHz)
α : Oscillation development time

(b) Releasing STOP mode by IRQxxx (for DI)



Wait c : Wait time until TM1 counts (n+1) source clock pulses (system clock/m)
$(n+1) \times m/f_{CC} + \alpha$ (n and m are the values used immediately before STOP mode is set)
α : Oscillation development time

(c) Releasing STOP mode by IRQxxx (for EI)



Wait c : Wait time until TM1 counts (n+1) source clock pulses (system clock/m)
$(n+1) \times m/f_{CC} + \alpha$ (n and m are the values used immediately before STOP mode is set)
α : Oscillation development time

19. RESET

The μPD17136B provides the following four reset functions:

① Reset using $\overline{\text{RESET}}$ input
② Power-on/power-down reset at power-on or power voltage drop
③ Watchdog timer reset to prevent program crash
④ Address stack overflow or underflow reset

Power-on/power-down reset is valid only when the power voltage used is in the range of 4.5 to 5.5 V.

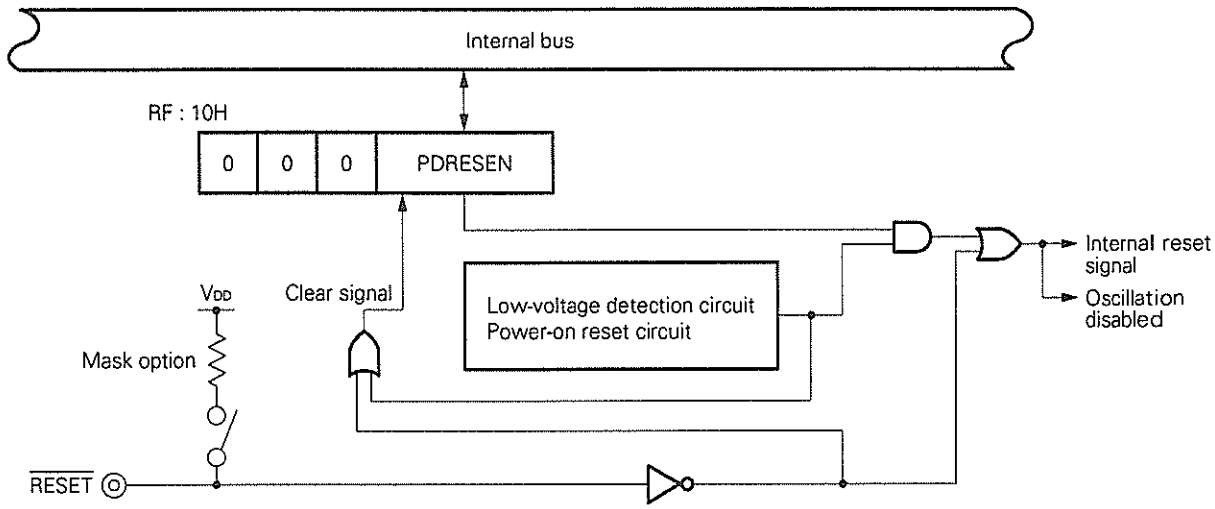
19.1 RESET FUNCTIONS

The reset functions are used to initialize device operations. The operations initialized depend on the reset type.

Table 19-1 Hardware Statuses after Reset

Hardware \ Reset type		• $\overline{\text{RESET}}$ input during operation • Incorporated power-on/power-down reset during operation	• $\overline{\text{RESET}}$ input in the standby mode • Incorporated power-on/power-down reset in the standby mode	• Watchdog timer overflow • Stack overflow or underflow
Program counter		0000H	0000H	0000H
Port	Input/output mode	Input	Input	Input
	Output latch	0	0	Not defined
General-purpose data memory	Other than DBF	Not defined	Statuses before reset are retained.	Not defined
	DBF	Not defined	Not defined	Not defined
System register	Other than WR	0	0	0
	WR	Not defined	Statuses before reset are retained.	Not defined
Control register		SP = 5H, IRQTM1 = 1, TM1EN = 1, IRQBTM = 0, and INT indicate the current status of the INT pin. The others are 0. See **Chapter 8.**		SP = 5H and INT indicate the current status of the INT pin. The others retain statuses before reset.
Timer 0 and timer 1	Count register	00H	00H	Timer 0: 00H Timer 1: Not defined
	Modulo register	01H	01H	01H
Basic interval timer binary counter		Not defined	Not defined	Not defined. (40H for watchdog timer overflow)
Serial interface shift register (SIOSFR)		Not defined	Statuses before reset are retained.	Not defined
A/D converter data register (ADCR)		00H	00H	00H

Fig. 19-1 Reset Block Configuration



19.2 RESETTING

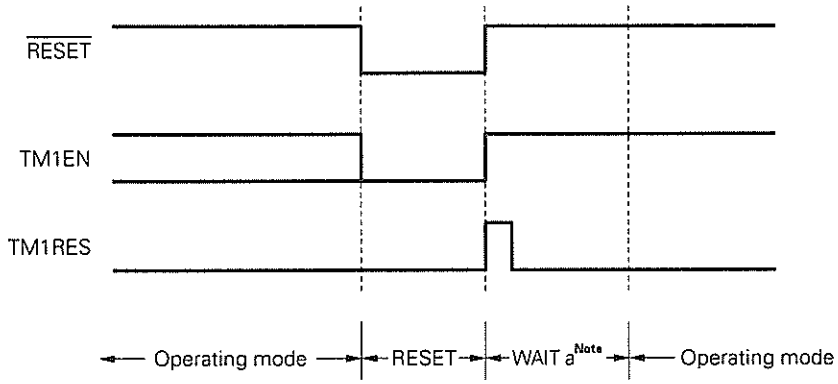
Operation when reset is caused by the $\overline{\text{RESET}}$ input is shown in Fig. 19-2.

If the $\overline{\text{RESET}}$ pin is set from low to high, system clock generation starts and an oscillation stability wait occurs with the timer 1. Program execution starts from address 0000H.

If power-on reset is used, the reset signals shown in Fig. 19-2 are internally generated. Operation is the same as that when reset is caused externally by the $\overline{\text{RESET}}$ input.

At watchdog timer overflow reset or stack overflow and underflow reset, oscillation stability wait time (WAIT a) does not occur. Operation starts from address 0000H after initial statuses are internally set.

Fig. 19-2 Resetting



Note This is oscillation stability wait time. Operating mode is set when timer 1 counts system clocks 512 × 2 times (about 512 μs (the shortest time is about 128 μs) when fcc is 2 MHz).

19.3 POWER-ON/POWER-DOWN RESET FUNCTION

The μPD17136B is provided with two reset functions to prevent malfunctions from occurring in the microcontroller. They are the power-on reset function and power-down reset function. The power-on reset function resets the microcontroller when it detects that power was turned on. The power-down reset function resets the microcontroller when it detects drops in the power voltage.

These functions are implemented by the power-voltage monitoring circuit whose operating voltage has a different range than the logic circuits in the microcontroller and the oscillation circuit (which stops oscillation at reset to put the microcontroller in a temporary stop state). Conditions required to enable these functions and their operations will be described next.

Caution When designing an application circuit which requires high reliability, do not design a reset function which depends only on a built-in power-on/power-down reset function. Be sure to design a circuit to which an external $\overline{\text{RESET}}$ signal can be input.

19.3.1 Conditions Required to Enable the Power-On Reset Function

This function is effective when used together with the power-down reset function.

The following conditions are required to validate the power-on reset function:

① The power voltage must be 4.5 to 5.5 V during normal operation, including the standby state.
② The power-down reset function must be enabled during normal operation, including the standby state.
③ The power voltage must rise from 0 V to the specified voltage.
④ The time it takes for the power voltage to rise from 0 to 2.7 V must be shorter than the oscillation stability wait time counted in timer 1. This takes about 512 μs (the shortest time is about 128 μs) when fcc is 2 MHz, which is equivalent to 512 × 2 pulses of the system clock.

Cautions 1. If the above conditions are not satisfied, the power-on reset function will not operate effectively. In this case, an external reset circuit needs to be added.

2. In the standby state, even if the power-down reset function operates normally, general-purpose data memory (except for DBF) retains data up to V_{DD} = 2.7 V. If, however, data is changed due to an external error, the data in memory is not guaranteed.

3. The power-on/power-down reset may not be performed normally because the oscillation settling time is very short. In such a case, input the $\overline{\text{RESET}}$ signal using an external device.

19.3.2 Description and Operation of the Power-On Reset Function

The power-on reset function resets the microcontroller when it detects that power was turned on in the hardware, regardless of the software state.

The power-on reset circuit operates under a lower voltage than the other internal circuits in the μPD17136B. It initializes the microcontroller regardless whether the oscillation circuit is operating. When the reset operation is terminated, timer 1 counts the number of oscillation pulses sent from the oscillator until it reaches the specified value. Within this period, oscillation becomes stable and the power voltage applied to the microcontroller enters the range (V_{DD} = 2.7 to 5.5 V) in which the microcontroller is guaranteed to operate.

When this period elapses, the microcontroller enters normal operation mode. Fig. 19-3 shows an example of the power-on reset operation.

Operation of the power-on reset circuit

① This circuit always monitors the voltage applied to the V_{DD} pin.

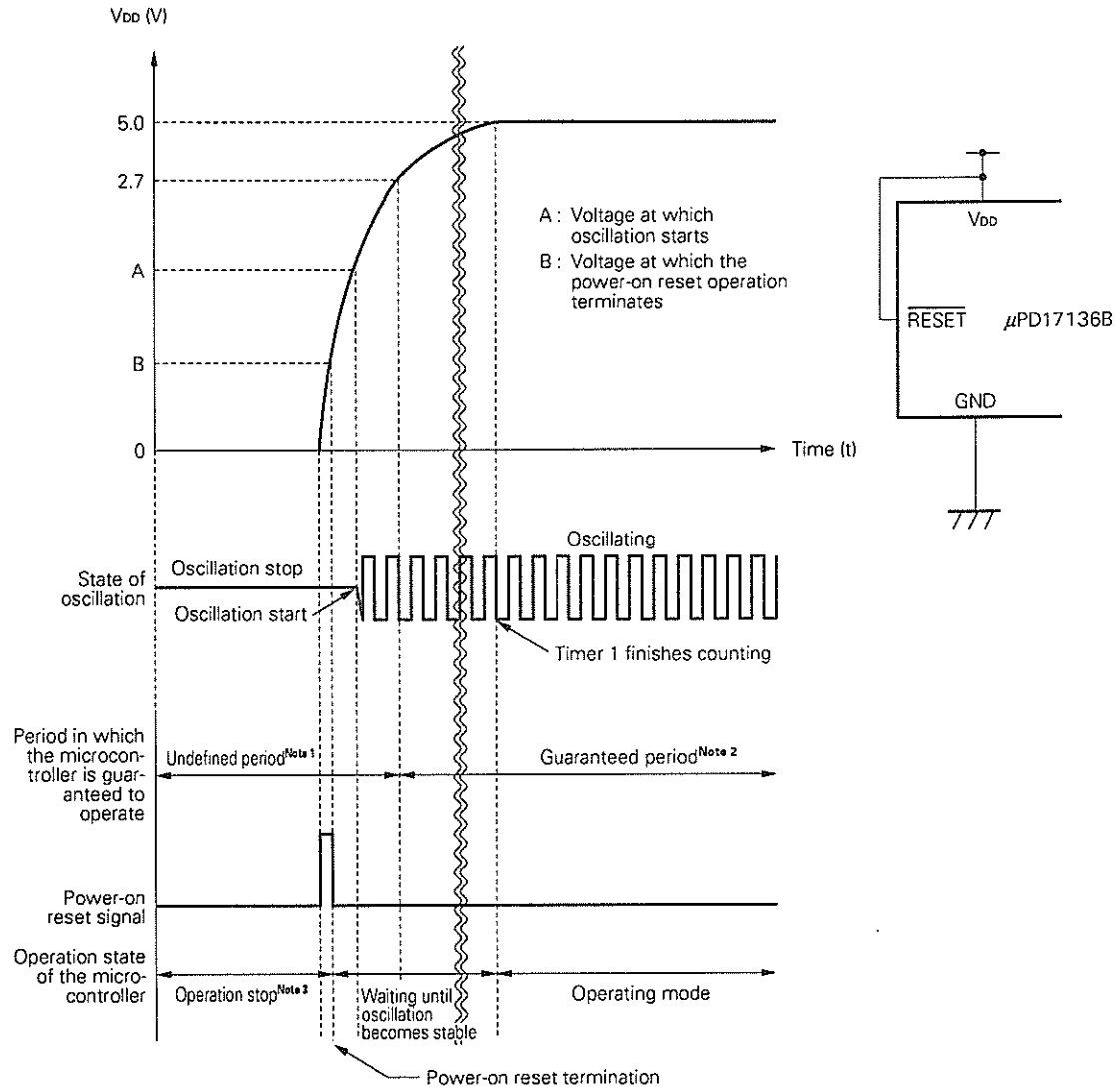
② This circuit resets[Note] the microcontroller until the power reaches the voltage specified for releasing the power-on reset operation (typically 1.5 V), regardless of whether the oscillation circuit is operating.

③ This circuit stops oscillation during the reset operation.

④ When reset is terminated, timer 1 counts oscillation pulses. The microcontroller waits until oscillation becomes stable and the power voltage becomes V_{DD} = 2.7 V or higher.

Note The power-on reset circuit resets the microcontroller when the power voltage reaches the voltage at which the internal circuit can operate, namely an internal reset signal can be accepted.

Fig. 19-3 Example of the Power-On Reset Operation



Notes 1. During the operation-undefined period, not all of the operations specified for the μPD17136B are not guaranteed. However, the power-on reset functions even in this period.

2. During the operation-guaranteed period, all the operations specified for the μPD17136B are guaranteed.

3. An operation stop state refers to the state in which all of the functions of the microcontroller are stopped.

19.3.3 Condition Required for Use of the Power-Down Reset Function

The power-down reset function can be enabled or disabled using software. The following condition is required to use this function:

- The power voltage must be 4.5 to 5.5 V during normal operation, including the standby state.

Caution When the microcontroller is used with a power voltage of 2.7 to 4.5 V, add an external reset circuit instead of using the internal power-down reset circuit. If the internal power-down reset circuit is used with a power voltage of 2.7 to 4.5 V, reset operation may not terminate.

19.3.4 Description and Operation of the Power-Down Reset Function

This function is enabled by setting the power-down reset enable flag (PDRESEN) using software.

When this function detects a power voltage drop, it issues the reset signal to the microcontroller. It then initializes the microcontroller. Stopping oscillation during reset prevents the power voltage in the microcontroller from fluctuating out of control. When the specified power voltage recovers and the power-down reset operation is terminated, the microcontroller waits the time required for stable oscillation using the timer. The microcontroller then enters normal operation (starts from the top of memory).

Fig. 19-4 shows an example of the power-down operation. Fig. 19-5 shows an example of reset operation during the period from power-down reset to power recovery.

Operation of the power-down reset circuit

① This circuit always monitors the voltage applied to the V_{DD} pin.

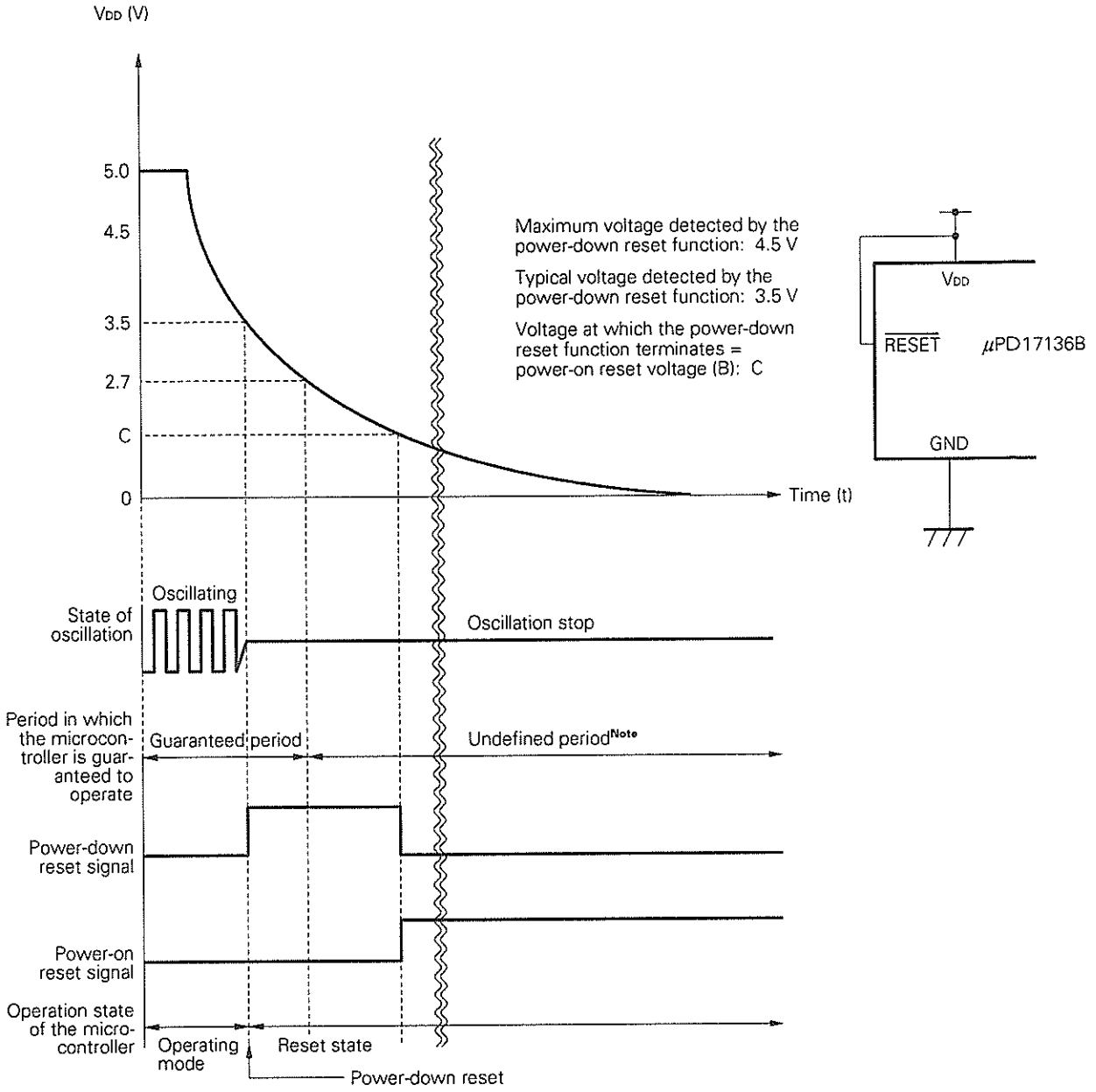
② When this circuit detects a power voltage drop, it issues a reset signal to the other parts of the microcontroller. It continues to send this reset signal until the power voltage recovers or all the functions in the microcontroller stop.

③ This circuit stops oscillation during the reset operation to prevent software crashes.
When the power voltage recovers to the low-voltage detection level (typically 3.5 V, 4.5 V maximum) before the power-down reset function stops, the microcontroller waits the time required for stable oscillation using timer 1, then enters normal operation mode.

④ When the power voltage recovers from 0 V, the power-on reset function has priority.

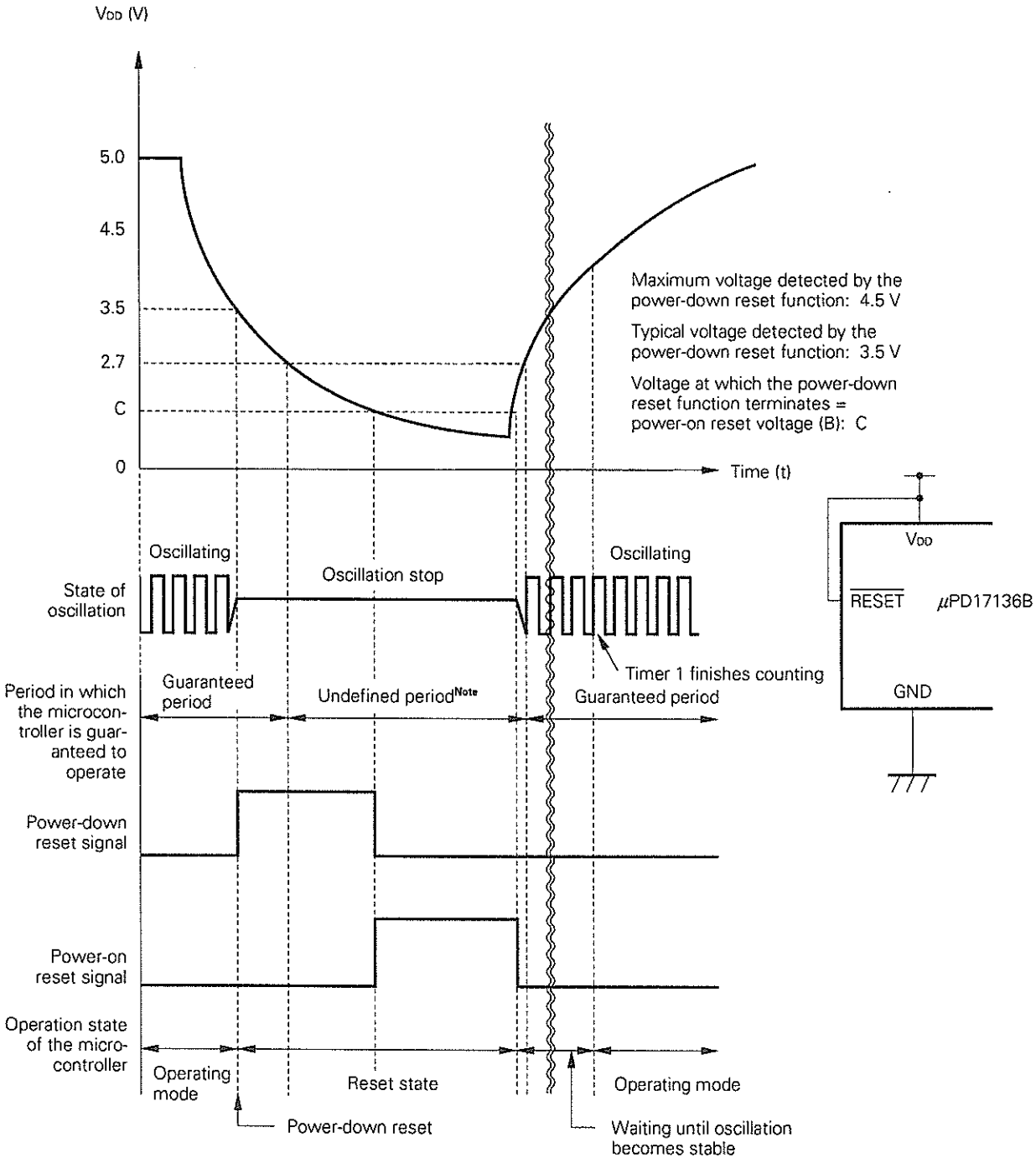
⑤ After the power-down reset function stops and the power voltage recovers before it reaches 0 V, the microcontroller waits using timer 1 until oscillation becomes stable and the power voltage (V_{DD}) reaches 2.7 V. The microcontroller then enters normal operation mode.

Fig. 19-4 Example of the Power-Down Reset Operation



Note During the operation-undefined period, not all the operations specified for the μPD17136B are not guaranteed. Even in this period, however, the power-down reset functions and continues to issue a reset signal until all the functions in the microcontroller stop.

Fig. 19-5 Example of Reset Operation during the Period from Power-Down Reset to Power Recovery



Note During the operation-undefined period, not all the operations specified for the μPD17136B are not guaranteed. Even in this period, however, the power-down reset functions and continues to issue the reset signal until all the functions in the microcontroller stop.

20. μPD17136B INSTRUCTION SET

20.1 LEGEND

AR	:	Address register
ASR	:	Address stack register pointed to by the stack pointer
addr	:	Program memory address (11 low-order bits)
BANK	:	Bank register
CMP	:	Compare flag
CY	:	Carry flag
DBF	:	Data buffer
h	:	Halt release condition
INTEF	:	Interrupt enable flag
INTR	:	Register automatically saved in the stack when an interrupt occurs
INTSK	:	Interrupt stack register
IX	:	Index register
MP	:	Data memory row address pointer
MPE	:	Memory pointer enable flag
m	:	Data memory address specified by m_R and mc
m_R	:	Data memory row address (high-order)
mc	:	Data memory column address (low-order)
n	:	Bit position (four bits)
n4	:	Immediate data (four bits)
PC	:	Program counter
p	:	Peripheral address
p_H	:	Peripheral address (three high-order bits)
p_L	:	Peripheral address (four low-order bits)
r	:	General register column address
rf	:	Register file address
rf_R	:	Register file row address (three high-order bits)
rfc	:	Register file column address (four low-order bits)
SP	:	Stack pointer
s	:	Stop release condition
WR	:	Window register
(×)	:	Contents of ×

20.2 LIST OF THE INSTRUCTION SET

Instruction set	Mnemonic	Operand	Operation	Machine code			
				Op code	Operand		
Add	ADD	r, m	(r) ← (r) + (m)	00000	m_R	mc	r
		m, #n4	(m) ← (m) + n4	10000	m_R	mc	n4
	ADDC	r, m	(r) ← (r) + (m) + CY	00010	m_R	mc	r
		m, #n4	(m) ← (m) + n4 + CY	10010	m_R	mc	n4
	INC	AR	AR ← AR + 1	00111	000	1001	0000
		IX	IX ← IX + 1	00111	000	1000	0000
Subtract	SUB	r, m	(r) ← (r) − (m)	00001	m_R	mc	r
		m, #n4	(m) ← (m) − n4	10001	m_R	mc	n4
	SUBC	r, m	(r) ← (r) − (m) − CY	00011	m_R	mc	r
		m, #n4	(m) ← (m) − n4 − CY	10011	m_R	mc	n4
Logical operation	OR	r, m	(r) ← (r) ∨ (m)	00110	m_R	mc	r
		m, #n4	(m) ← (m) ∨ n4	10110	m_R	mc	n4
	AND	r, m	(r) ← (r) ∧ (m)	00100	m_R	mc	r
		m, #n4	(m) ← (m) ∧ n4	10100	m_R	mc	n4
	XOR	r, m	(r) ← (r) ⊻ (m)	00101	m_R	mc	r
		m, #n4	(m) ← (m) ⊻ n4	10101	m_R	mc	n4
Test	SKT	m, #n	CMP ← 0, if (m) ∧ n = n, then skip	11110	m_R	mc	n
	SKF	m, #n	CMP ← 0, if (m) ∧ n = 0, then skip	11111	m_R	mc	n
Compare	SKE	m, #n4	(m) − n4, skip if zero	01001	m_R	mc	n4
	SKNE	m, #n4	(m) − n4, skip if not zero	01011	m_R	mc	n4
	SKGE	m, #n4	(m) − n4, skip if not borrow	11001	m_R	mc	n4
	SKLT	m, #n4	(m) − n4, skip if borrow	11011	m_R	mc	n4
Rotation	RORC	r	┌→ CY → $(r)_{b3}$ → $(r)_{b2}$ → $(r)_{b1}$ → $(r)_{b0}$ ┐	00111	000	0111	r
Transfer	LD	r, m	(r) ← (m)	01000	m_R	mc	r
	ST	m, r	(m) ← (r)	11000	m_R	mc	r
	MOV	@r, m	if MPE = 1: (MP, (r)) ← (m) if MPE = 0: (BANK, m_R, (r)) ← (m)	01010	m_R	mc	r
		m, @r	if MPE = 1: (m) ← (MP, (r)) if MPE = 0: (m) ← (BANK, m_R, (r))	11010	m_R	mc	r
		m, #n4	(m) ← n4	11101	m_R	mc	n4
	MOVT	DBF, @AR	SP ← SP − 1, ASR ← PC, PC ← AR, DBF ← (PC), PC ← ASR, SP ← SP + 1	00111	000	0001	0000

Instruction set	Mnemonic	Operand	Operation	Machine code			
				Op code	Operand		
Transfer	PUSH	AR	SP ← SP – 1, ASR ← AR	00111	000	1101	0000
	POP	AR	AR ← ASR, SP ← SP + 1	00111	000	1100	0000
	PEEK	WR, rf	WR ← (rf)	00111	rf_R	0011	rfc
	POKE	rf, WR	(rf) ← WR	00111	rf_R	0010	rfc
	GET	DBF, p	DBF ← (p)	00111	p_H	1011	p_L
	PUT	p, DBF	(p) ← DBF	00111	p_H	1010	p_L
Branch	BR	addr	PC ← addr	01100	addr		
		@AR	PC ← AR	00111	000	0100	0000
Sub-routine	CALL	addr	SP ← SP – 1, ASR ← PC PC ← addr	11100	addr		
		@AR	SP ← SP – 1, ASR ← PC PC ← AR	00111	000	0101	0000
	RET		PC ← ASR, SP ← SP + 1	00111	000	1110	0000
	RETSK		PC ← ASR, SP ← SP + 1 and skip	00111	001	1110	0000
	RETI		PC ← ASR, INTR ← INTSK, SP ← SP + 1	00111	100	1110	0000
Interrupt	EI		INTEF ← 1	00111	000	1111	0000
	DI		INTEF ← 0	00111	001	1111	0000
Others	STOP	s	STOP	00111	010	1111	s
	HALT	h	HALT	00111	011	1111	h
	NOP		No operation	00111	100	1111	0000

21. ASSEMBLER RESERVED WORDS

21.1 MASK OPTION PSEUDO INSTRUCTIONS

To create μPD17136B programs, it is necessary to specify whether pins that can have pull-up resistors have pull-up resistors. This is done in the assembler source program using mask option pseudo instructions. To set the mask option, note that D17136B.OPT file in the AS17136B (μPD17136B device file) must be in the current directory at assembly time.

Specify mask options for the following pins:

- $\overline{\text{RESET}}$ pin
- Port 0D ($P0D_3$, $P0D_2$, $P0D_1$, $P0D_0$)
- Port 1A ($P1A_3$, $P1A_2$, $P1A_1$, $P1A_0$)
- Port 1B ($P1B_0$)

21.1.1 OPTION and ENDOP Pseudo Instructions

The block from the OPTION pseudo instruction to the ENDOP pseudo instruction is defined as the option definition block.

The format for the mask option definition block is shown below. Only the four pseudo instructions listed in Table 21-1 can be described in this block.

Format:

Symbol	Mnemonic	Operand	Comment
[label:]	OPTION		[;comment]
	•		
	•		
	•		
	•		
	ENDOP		

21.1.2 Mask Option Definition Pseudo Instructions

Table 21-1 lists the pseudo instructions which define the mask options for each pin.

Table 21-1 Mask Option Definition Pseudo Instructions

Pin	Mask option pseudo instruction	Number of operands	Parameter name
$\overline{\text{RESET}}$	OPTRES	1	OPEN (without pull-up resistor) PULLUP (with pull-up resistor)
$P0D_3$-$P0D_0$	OPTP0D	4	OPEN (without pull-up resistor) PULLUP (with pull-up resistor)
$P1A_3$-$P1A_0$	OPTP1A	4	OPEN (without pull-up resistor) PULLUP (with pull-up resistor)
$P1B_0$	OPTP1B	1	OPEN (without pull-up resistor) PULLUP (with pull-up resistor)

The OPTRES format is shown below. Specify the $\overline{\text{RESET}}$ mask option in the operand field.

Symbol	Mnemonic	Operand	Comment
[label:]	OPTRES	($\overline{\text{RESET}}$)	[;comment]

The OPTP0D format is shown below. Specify mask options for all pins of port 0D. Specify the pins in the operand field starting at the first operand in the order $P0D_3$, $P0D_2$, $P0D_1$, then $P0D_0$.

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP0D	($P0D_3$),($P0D_2$),($P0D_1$),($P0D_0$)	[;comment]

The OPTP1A format is shown below. Specify mask options for all pins of port 1A. Specify the pins in the operand field starting at the first operand in the order $P1A_3$, $P1A_2$, $P1A_1$, then $P1A_0$.

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP1A	($P1A_3$),($P1A_2$),($P1A_1$),($P1A_0$)	[;comment]

The OPTP1B format is shown below. Specify the mask option of $P1B_0$ in the operand field.

Symbol	Mnemonic	Operand	Comment
[label:]	OPTP1B	($P1B_0$)	[;comment]

Example of describing mask options

$\overline{\text{RESET}}$ pin: Pull-up

$P0D_3$: Open, $P0D_2$: Open, $P0D_1$: Pull-up, $P0D_0$: Pull-up,

$P1A_3$: Pull-up, $P1A_2$: Open, $P1A_1$: Open, $P1A_0$: Open,

$P1B_0$: Open

Symbol	Mnemonic	Operand	Comment
; μPD17136B			
Setting mask options:	OPTION		
;			
	OPTRES	PULLUP	
	OPTP0D	OPEN,OPEN,PULLUP,PULLUP	
	OPTP1A	PULLUP,OPEN,OPEN,OPEN	
	OPTP1B	OPEN	
;			
	ENDOP		

21.2 RESERVED SYMBOLS

The reserved symbols defined in the μPD17136B device file (AS17136B) are listed below.

System register (SYSREG)

Symbolic name	Attribute	Value	Read/ write	Description
AR3	MEM	0.74H	R	Bits b15 to b12 of the address register
AR2	MEM	0.75H	R/W	Bits b11 to b8 of the address register
AR1	MEM	0.76H	R/W	Bits b7 to b4 of the address register
AR0	MEM	0.77H	R/W	Bits b3 to b0 of the address register
WR	MEM	0.78H	R/W	Window register
BANK	MEM	0.79H	R/W	Bank register
IXH	MEM	0.7AH	R/W	Index register high
MPH	MEM	0.7AH	R/W	Data memory row address pointer high
MPE	FLG	0.7AH.3	R/W	Memory pointer enable flag
IXM	MEM	0.7BH	R/W	Index register middle
MPL	MEM	0.7BH	R/W	Data memory row address pointer low
IXL	MEM	0.7CH	R/W	Index register low
RPH	MEM	0.7DH	R/W	General register pointer high
RPL	MEM	0.7EH	R/W	General register pointer low
PSW	MEM	0.7FH	R/W	Program status word
BCD	FLG	0.7EH.0	R/W	BCD flag
CMP	FLG	0.7FH.3	R/W	Compare flag
CY	FLG	0.7FH.2	R/W	Carry flag
Z	FLG	0.7FH.1	R/W	Zero flag
IXE	FLG	0.7FH.0	R/W	Index enable flag

Fig. 21-1 System Register Configuration

Address	74H	75H	76H	77H	78H	79H	7AH	7BH	7CH	7DH	7EH	7FH
Name	Address register (AR)				Window register (WR)	Bank register (BANK)	Index register (IX) / Data memory row address pointer (MP)			General register pointer (RP)		Program status word (PSWORD)
Symbol	AR3	AR2[Note 1]	AR1	AR0	WR	BANK	IXH / MPH	IXM / MPL	IXL	RPH	RPL	PSW
Bit	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0	b_3 b_2 b_1 b_0
Data[Note 2]	0 0 0 0 (AR)	0	(AR)	(AR)	(WR)	0 0 0 (BANK)	MPE 0 0 0 (MP)	(IX)	(IX)	0 0 0 (RP)	(RP)	BCD CMP CY Z IXE
Initial value when reset	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	Not defined	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0	0 0 0 0

Notes 1. For the μPD17134B, bit 2 of AR2 is fixed at 0.

2. A bit for which 0 is written is fixed at 0.

Data buffer (DBF)

Symbolic name	Attribute	Value	Read/ write	Description
DBF3	MEM	0.0CH	R/W	DBF bits b15 to b12
DBF2	MEM	0.0DH	R/W	DBF bits b11 to b8
DBF1	MEM	0.0EH	R/W	DBF bits b7 to b4
DBF0	MEM	0.0FH	R/W	DBF bits b3 to b0

Port register

Symbolic name	Attribute	Value	Read/ write	Description
P0A3	FLG	0.70H.3	R/W	Port 0A bit b3
P0A2	FLG	0.70H.2	R/W	Port 0A bit b2
P0A1	FLG	0.70H.1	R/W	Port 0A bit b1
P0A0	FLG	0.70H.0	R/W	Port 0A bit b0
P0B3	FLG	0.71H.3	R/W	Port 0B bit b3
P0B2	FLG	0.71H.2	R/W	Port 0B bit b2
P0B1	FLG	0.71H.1	R/W	Port 0B bit b1
P0B0	FLG	0.71H.0	R/W	Port 0B bit b0
P0C3	FLG	0.72H.3	R/W	Port 0C bit b3
P0C2	FLG	0.72H.2	R/W	Port 0C bit b2
P0C1	FLG	0.72H.1	R/W	Port 0C bit b1
P0C0	FLG	0.72H.0	R/W	Port 0C bit b0
P0D3	FLG	0.73H.3	R/W	Port 0D bit b3
P0D2	FLG	0.73H.2	R/W	Port 0D bit b2
P0D1	FLG	0.73H.1	R/W	Port 0D bit b1
P0D0	FLG	0.73H.0	R/W	Port 0D bit b0
P1A3	FLG	1.70H.3	R/W	Port 1A bit b3
P1A2	FLG	1.70H.2	R/W	Port 1A bit b2
P1A1	FLG	1.70H.1	R/W	Port 1A bit b1
P1A0	FLG	1.70H.0	R/W	Port 1A bit b0
P1B0	FLG	1.71H.0	R	Port 1B bit b0

Register file (control register)

(1/2)

Symbolic name	Attribute	Value	Read/ write	Description
SP	MEM	0.81H	R/W	Stack pointer
SIOTS	FLG	0.82H.3	R/W	Serial interface start flag
SIOHIZ	FLG	0.82H.2	R/W	$P0D_1$/SO pin function selection flag
SIOCK1	FLG	0.82H.1	R/W	Serial clock selection flag bit 1
SIOCK0	FLG	0.82H.0	R/W	Serial clock selection flag bit 0
WDTRES	FLG	0.83H.3	R/W	Watchdog timer reset flag
WDTEN	FLG	0.83H.0	R/W	Watchdog timer enable flag
TM0OSEL	FLG	0.8BH.3	R/W	$P0D_3$/$\overline{TM0OUT}$ pin function selection flag
SIOEN	FLG	0.8BH.0	R/W	Serial interface enable flag
P0BGPU	FLG	0.8CH.1	R/W	P0B group pull-up selection flag (pull-up = 1)
P0AGPU	FLG	0.8CH.0	R/W	P0A group pull-up selection flag (pull-up = 1)
INT	FLG	0.8FH.0	R	INT pin status flag
PDRESEN	FLG	0.90H.0	R/W	Power-down reset enable flag
TM0EN	FLG	0.91H.3	R/W	Timer 0 enable flag
TM0RES	FLG	0.91H.2	R/W	Timer 0 reset flag
TM0CK1	FLG	0.91H.1	R/W	Timer 0 count pulse selection flag bit 1
TM0CK0	FLG	0.91H.0	R/W	Timer 0 count pulse selection flag bit 0
TM1EN	FLG	0.92H.3	R/W	Timer 1 enable flag
TM1RES	FLG	0.92H.2	R/W	Timer 1 reset flag
TM1CK1	FLG	0.92H.1	R/W	Timer 1 count pulse selection flag bit 1
TM1CK0	FLG	0.92H.0	R/W	Timer 1 count pulse selection flag bit 0
BTMISEL	FLG	0.93H.3	R/W	BTM interrupt request clock selection flag
BTMRES	FLG	0.93H.2	R/W	BTM reset flag
BTMCK1	FLG	0.93H.1	R/W	BTM count pulse selection flag bit 1
BTMCK0	FLG	0.93H.0	R/W	BTM count pulse selection flag bit 0
P0C3IDI	FLG	0.9BH.3	R/W	$P0C_3$ input port disable flag (ADC_3/$P0C_3$ pin function selection)
P0C2IDI	FLG	0.9BH.2	R/W	$P0C_2$ input port disable flag (ADC_2/$P0C_2$ pin function selection)
P0C1IDI	FLG	0.9BH.1	R/W	$P0C_1$ input port disable flag (ADC_1/$P0C_1$ pin function selection)
P0C0IDI	FLG	0.9BH.0	R/W	$P0C_0$ input port disable flag (ADC_0/$P0C_0$ pin function selection)
P0CBIO3	FLG	0.9CH.3	R/W	$P0C_3$ input/output selection flag (1 = output port)
P0CBIO2	FLG	0.9CH.2	R/W	$P0C_2$ input/output selection flag (1 = output port)
P0CBIO1	FLG	0.9CH.1	R/W	$P0C_1$ input/output selection flag (1 = output port)
P0CBIO0	FLG	0.9CH.0	R/W	$P0C_0$ input/output selection flag (1 = output port)
ZCROSS	FLG	0.9DH.0	R/W	Zerocross detector enable flag
IEGMD1	FLG	0.9FH.1	R/W	INT pin edge detection selection flag bit 1
IEGMD0	FLG	0.9FH.0	R/W	INT pin edge detection selection flag bit 0
ADCSTRT	FLG	0.0A0H.0	R/W	A/D converter start flag (always 0 when read)
ADCSOFT	FLG	0.0A1H.3	R/W	Flag for selecting operating mode of A/D converter flag (1 = single mode)
ADCCMP	FLG	0.0A1H.1	R/W	A/D converter comparison result flag (valid only in single mode)
ADCEND	FLG	0.0A1H.0	R/W	A/D converter conversion end flag

Register file (control register)

(2/2)

Symbolic name	Attribute	Value	Read/ write	Description
ADCCH3	FLG	0.0A2H.3	R/W	Dummy flag
ADCCH2	FLG	0.0A2H.2	R/W	Dummy flag
ADCCH1	FLG	0.0A2H.1	R/W	A/D converter channel selection flag bit 1
ADCCH0	FLG	0.0A2H.0	R/W	A/D converter channel selection flag bit 0
P0DBIO3	FLG	0.0ABH.3	R/W	$P0D_3$ input/output selection flag (1 = output port)
P0DBIO2	FLG	0.0ABH.2	R/W	$P0D_2$ input/output selection flag (1 = output port)
P0DBIO1	FLG	0.0ABH.1	R/W	$P0D_1$ input/output selection flag (1 = output port)
P0DBIO0	FLG	0.0ABH.0	R/W	$P0D_0$ input/output selection flag (1 = output port)
P1AGIO	FLG	0.0ACH.2	R/W	P1A group input/output selection flag (1 = all P1As are output ports.)
P0BGIO	FLG	0.0ACH.1	R/W	P0B group input/output selection flag (1 = all P0Bs are output ports.)
P0AGIO	FLG	0.0ACH.0	R/W	P0A group input/output selection flag (1 = all P0As are output ports.)
IPSIO	FLG	0.0AEH.0	R/W	Serial interface interrupt enable flag
IPBTM	FLG	0.0AFH.3	R/W	BTM interrupt enable flag
IPTM1	FLG	0.0AFH.2	R/W	Timer 1 interrupt enable flag
IPTM0	FLG	0.0AFH.1	R/W	Timer 0 interrupt enable flag
IP	FLG	0.0AFH.0	R/W	INT pin interrupt enable flag
IRQSIO	FLG	0.0BBH.0	R/W	Serial interface interrupt request flag
IRQBTM	FLG	0.0BCH.0	R/W	BTM interrupt request flag
IRQTM1	FLG	0.0BDH.0	R/W	Timer 1 interrupt request flag
IRQTM0	FLG	0.0BEH.0	R/W	Timer 0 interrupt request flag
IRQ	FLG	0.0BFH.0	R/W	INT pin interrupt request flag

Peripheral hardware register

Symbolic name	Attribute	Value	Read/ write	Description
SIOSFR	DAT	01H	R/W	Peripheral address of the shift register
TM0M	DAT	02H	W	Peripheral address of the timer 0 modulo register
TM1M	DAT	03H	W	Peripheral address of the timer 1 modulo register
ADCR	DAT	04H	R/W	Peripheral address of A/D converter data register
TM0TM1C	DAT	45H	R	Peripheral address of timer 0 timer 1 count register
AR	DAT	40H	R/W	Peripheral address of the address register for GET, PUT, PUSH, CALL, BR, MOVT, and INC instructions

Others

Symbolic name	Attribute	Value	Description
DBF	DAT	0FH	Fixed operand value for a GET/PUT/MOVT instruction
IX	DAT	01H	Fixed operand value for an INC instruction

Fig. 21-2 Control Register Configuration (1/2)

Column address / Row address	Item	0	1	2	3	4	5	6	7
0 (8)	Symbol		0 SP	SIOTS SIOHIZ SIOCK1 SIOCK0	WDTRES 0 0 WDTEN				
	When reset		0 1 0 1	0 0 0 0	0 0 0 0				
	Read/ Write		R/W	R/W	R/W				
1 (9)	Symbol	0 0 0 PDRESEN	TM0EN TM0RES TM0CK1 TM0CK0	TM1EN TM1RES TM1CK1 TM1CK0	BTMISEL BTMRES BTMCK1 BTMCK0				
	When reset	0 0 0 0	0 0 0 0	1 0 0 0	0 0 0 0				
	Read/ Write	R/W	R/W	R/W	R/W				
2 (A)	Symbol	0 0 0 ADCSTRT	ADCSOFT 0 ADCCMP ADCEND	ADCCH3 ADCCH2 ADCCH1 ADCCH0					
	When reset	0 0 0 0	0 0 0 0	0 0 0 0					
	Read/ Write	R/W	R/W R	R/W					
3 (B)	Symbol								
	When reset								
	Read/ Write								

Remark The address enclosed in parentheses apply when the AS17K assembler is used.
The names of all the flags in the control registers are assembler reserved words saved in the device file. Using these reserved words is useful in programming.

Fig. 21-2 Control Register Configuration (2/2)

8	9	A	B	C	D	E	F
			TM0OSEL, 0, 0, SIOEN	0, 0, P0BGPU, P0AGPU			0, 0, 0, INT
			0, 0, 0, 0	0, 0, 0, 0			0, 0, 0, Note
			R/W	R/W			R
			P0C3IDI, P0C2IDI, P0C1IDI, P0C0IDI	P0CBIO3, P0CBIO2, P0CBIO1, P0CBIO0	0, 0, 0, ZCROSS		0, 0, IEGMD1, IEGMD0
			0, 0, 0, 0	0, 0, 0, 0	0, 0, 0, 0		0, 0, 0, 0
			R/W	R/W	R/W		R/W
			P0DBIO3, P0DBIO2, P0DBIO1, P0DBIO0	0, P1AGIO, P0BGIO, P0AGIO		0, 0, 0, IPSIO	IPBTM, IPTM1, IPTM0, IP
			0, 0, 0, 0	0, 0, 0, 0		0, 0, 0, 0	0, 0, 0, 0
			R/W	R/W		R/W	R/W
			0, 0, 0, IRQSIO	0, 0, 0, IRQBTM	0, 0, 0, IRQTM1	0, 0, 0, IRQTM0	0, 0, 0, IRQ
			0, 0, 0, 0	0, 0, 0, 0	0, 0, 0, 1	0, 0, 0, 0	0, 0, 0, 0
			R/W	R/W	R/W	R/W	R/W

Note The INT flag depends on the status of the INT pin.

22. ELECTRICAL CHARACTERISTICS

Absolute maximum ratings (T_A = 25 °C)

Parameter	Symbol	Conditions		Rated value	Unit
Supply voltage	V_{DD}			−0.3 to +7.0	V
Analog supply voltage	V_{ADC}	$V_{ADC} = V_{DD} \pm 0.3$ V		−0.3 to +7.0	V
Input voltage	V_I	P0A, P0B, P0C, P1B, INT, $\overline{RESET}$		−0.3 to V_{DD} + 0.3	V
		P0D, P1A	Note 1	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11.0	
Output voltage	V_O	P0A, P0B, P0C		−0.3 to V_{DD} + 0.3	V
		P0D, P1A	Note 1	−0.3 to V_{DD} + 0.3	V
			Note 2	−0.3 to +11.0	
High-level output current	I_{OH}	Each of P0A, P0B, and P0C		−15	mA
		Total of all pins		−30	mA
Low-level output current	I_{OL}	Each of P0A, P0B, and P0C		15	mA
		Each of P0D and P1A		30	mA
		Total of all pins		100	mA
Operating ambient temperature	T_A			−40 to +85	°C
Storage temperature	T_{stg}			−65 to +150	°C
Allowable dissipation	P_d	T_A = 85 °C	28-pin plastic shrink DIP	140	mW
			28-pin plastic SOP	85	

Notes 1. When a pull-up resistor is incorporated by mask option

2. When a pull-up resistor is not incorporated

Caution Absolute maximum ratings are rated values beyond which some physical damages may be caused to the product; if any of the parameters in the table above exceeds its rated value even for a moment, the quality of the product may deteriorate. Be sure to use the product within the rated values.

Recommended power voltage range (T_A = −40 to +85 °C)

Parameter	Conditions	Min.	Typ.	Max.	Unit
CPU[Note]		2.7		5.5	V
A/D converter	Absolute accuracy: ±1.5 LSB or less	4.5		5.5	V
Zerocross detection circuit	Zerocross accuracy: A_{ZX} = 120 mV or less	4.5		5.5	V
Power-on/power-down reset circuit	Rising time of the power voltage (from 0 to 2.7 V): 16t_{CY} or less	4.5		5.5	V

Note Excluding the A/D converter, zerocross detector, and power-on/power-down reset circuit

Remark t_{CY} = 16/f_{CC} (f_{CC}: frequency of system clock oscillator)

System clock oscillator characteristics (T_A = −40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
System clock oscillation frequency	f_{CC}	V_{DD} = 4.5 to 5.5 V, R_{OSC} = 9.1 kΩ	1.6	2	2.4	MHz
		V_{DD} = 4.5 to 5.5 V, R_{OSC} = 22 kΩ	0.8	1	1.2	MHz
		V_{DD} = 2.7 to 5.5 V, R_{OSC} = 22 kΩ	0.6	1	1.2	MHz
		V_{DD} = 2.7 to 3.3 V, R_{OSC} = 47 kΩ	400	500	600	kHz

DC characteristics (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

(1/2)

Parameter	Symbol	Conditions		Min.	Typ.	Max.	Unit
High-level input voltage	V_{IH1}	P0A, P0B, P0C, P1B		0.7V_{DD}		V_{DD}	V
	V_{IH2}	P0D, P1A	Note 1	0.7V_{DD}		V_{DD}	V
			Note 2			9	
	V_{IH3}	$\overline{RESET}$, $\overline{SCK}$, SI, INT		0.8V_{DD}		V_{DD}	V
Low-level input voltage	V_{IL1}	P0A, P0B, P0C, P1B		0		0.3V_{DD}	V
	V_{IL2}	P0D, P1A, $\overline{RESET}$, $\overline{SCK}$, SI, INT		0		0.2V_{DD}	V
High-level output voltage	V_{OH}	P0A, P0B, P0C	V_{DD} = 4.5 to 5.5 V, I_{OH} = -1.0 mA	V_{DD} - 0.3			V
		Note 2	V_{DD} = 2.7 to 4.5 V, I_{OH} = -0.5 mA	V_{DD} - 0.3			V
Low-level output voltage	V_{OL1}	P0A, P0B, P0C, P0D, P1A	V_{DD} = 4.5 to 5.5 V, I_{OL} = 1.0 mA			0.3	V
		Note 2	V_{DD} = 2.7 to 4.5 V, I_{OL} = 0.5 mA			0.3	V
	V_{OL2}	P0D, P1A	V_{DD} = 4.5 to 5.5 V			1.0	V
		I_{OL} = 15 mA	V_{DD} = 2.7 to 4.5 V			2.0	V
High-level input leakage current	I_{LIH1}	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = V_{DD}				3	μA
	I_{LIH2}	P0D, P1A, V_{IN} = 9 V Note 2				10	μA
Low-level input leakage current	I_{LIL}	P0A, P0B, P0C, P0D, P1A, P1B, V_{IN} = 0 V				-5	μA
High-level output leakage current	I_{LOH1}	P0A, P0B, P0C, P0D, P1A, V_{OUT} = V_{DD}				3	μA
	I_{LOH2}	P0D, P1A, V_{OUT} = 9 V Note 2				10	μA
Low-level output leakage current	I_{LOL}	P0A, P0B, P0C, P0D, P1A, V_{OUT} = 0 V				−5	μA
Built-in pull-up resistor	R_{PULL}	P0A, P0B, P0D, P1A, P1B, $\overline{RESET}$		50	100	200	kΩ

Notes 1. When a pull-up resistor is incorporated

2. When a pull-up resistor is not incorporated

DC characteristics (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

(2/2)

Parameter	Symbol	Conditions			Min.	Typ.	Max.	Unit
Power supply current[Note]	I_{DD1}	Operation mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %		0.8	2.0	mA
				V_{DD} = 3 V ±10 %		0.5	1.5	mA
			f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %		0.4	1.0	mA
				V_{DD} = 3 V ±10 %		0.25	0.75	mA
			f_{CC} = 500 kHz	V_{DD} = 5 V ±10 %		250	500	μA
				V_{DD} = 3 V ±10 %		125	375	μA
	I_{DD2}	HALT mode	f_{CC} = 2.0 MHz	V_{DD} = 5 V ±10 %		0.6	1.5	mA
				V_{DD} = 3 V ±10 %		0.3	1.0	mA
			f_{CC} = 1.0 MHz	V_{DD} = 5 V ±10 %		0.3	0.8	mA
				V_{DD} = 3 V ±10 %		0.15	0.5	mA
			f_{CC} = 500 kHz	V_{DD} = 5 V ±10 %		150	300	μA
				V_{DD} = 3 V ±10 %		100	200	μA
	I_{DD3}	STOP mode	V_{DD} = 5 V ±10 %			3.0	10	μA
			V_{DD} = 3 V ±10 %			2.0	10	μA

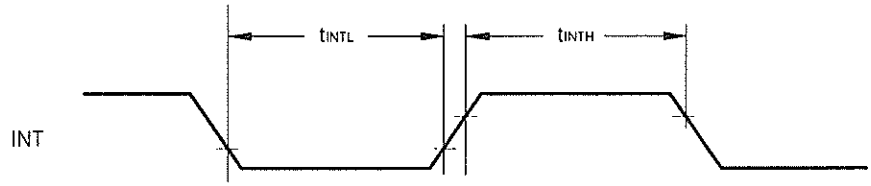
Note This current excludes the current which flows through the A/D converter, zerocross detector, and built-in pull-up resistors.

AC characteristics (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

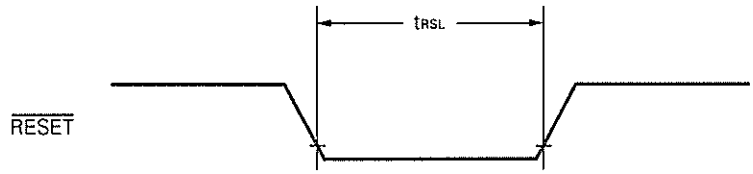
Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
CPU clock cycle time (instruction execution time)	t_{CY}		6.6		41	μs
INT high/low level width (external interrupt input)	t_{INTH}, t_{INTL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs
$\overline{RESET}$ low level width	t_{RSL}	V_{DD} = 4.5 to 5.5 V	10			μs
			50			μs

Remark t_{CY} = 16/fcc (fcc: frequency of system clock oscillator)

Interrupt input timing



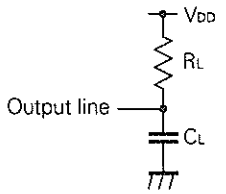
$\overline{RESET}$ input timing



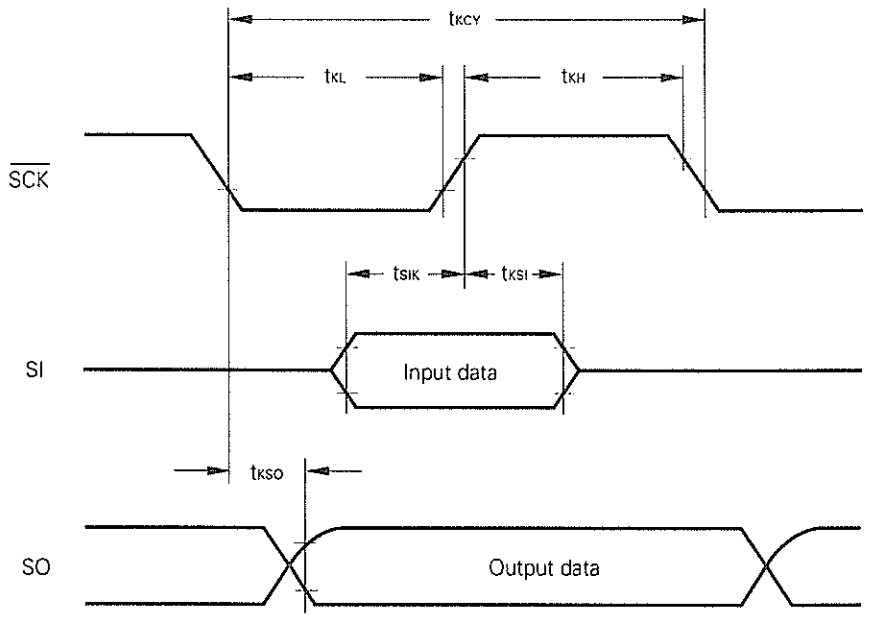
SERIAL TRANSFER OPERATION (V_{DD} = 2.7 to 5.5 V, T_A = −40 to +85 °C)

Parameter	Symbol		Conditions		Min.	Typ.	Max.	Unit
$\overline{SCK}$ cycle time	t_{KCY}	Input	V_{DD} = 4.5 to 5.5 V		2.0			μs
					10			μs
		Output	R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	8.0			μs
					16			μs
			Built-in pull-up resistor, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	150			μs
					300			μs
$\overline{SCK}$ high/low level width	t_{KH}, t_{KL}	Input	V_{DD} = 4.5 to 5.5 V		1.0			μs
					5.0			μs
		Output	R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2-0.6			μs
					t_{KCY}/2-1.2			μs
			Built-in pull-up resistor, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V	t_{KCY}/2-70			μs
					t_{KCY}/2-140			μs
SI setup time (with respect to $\overline{SCK}$↑)	t_{SIK}				100			ns
SI hold time (with respect to $\overline{SCK}$↑)	t_{KSI}				100			ns
Delay from $\overline{SCK}$↓ to SO	t_{KSO}		R_L = 1 kΩ, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V			0.8	μs
							1.4	μs
			Built-in pull-up resistor, C_L = 100 pF	V_{DD} = 4.5 to 5.5 V			70	μs
							140	μs

Remark R_L: a resistive load for the output line
C_L: a capacitive load for the output line

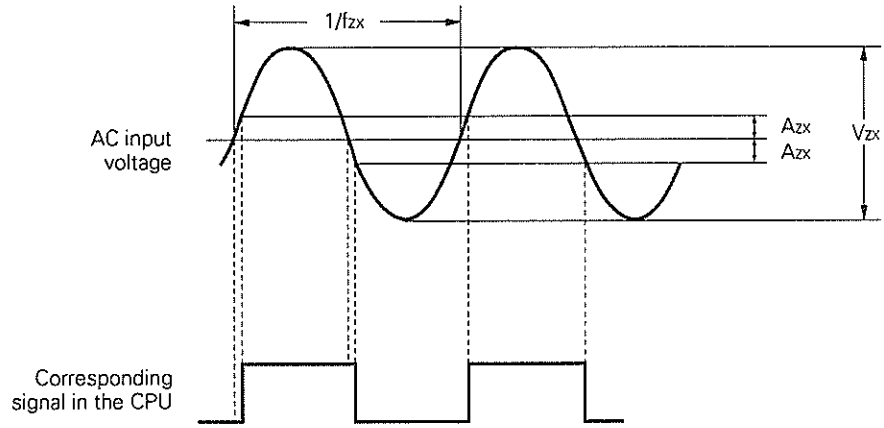


Serial transfer timing



Zerocross detector characteristics (V_{DD} = 4.5 to 5.5 V, T_A = −40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Zerocross detection input level	V_{ZX}	AC input, coupling capacity of 1 μF	1.0		3.0	V_{P-P}
Zerocross detection input frequency	f_{ZX}		40	50 or 60	1000	Hz
Zerocross accuracy	A_{ZX}	50 Hz or 60 Hz		40	120	mV
Zerocross detector current	I_{ZX}	There is no AC input.		15	90	μA



Caution The signal in the CPU delays from the original signal at the rising and falling edges indicated by A_{ZX} in the above figure. But it may advance. The timing fluctuation cannot be fixed.

A/D converter characteristics (V_{DD} = 4.5 to 5.5 V, T_A = −40 to +85 °C, V_{ADC} = V_{DD} ±0.5 %)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Resolution			8	8	8	bit
Absolute accuracy[Note 1]		V_{ADC} = V_{DD}			±1.5	LSB
ADC circuit current	I_{ADC}			1.5	2.0	mA
Conversion time[Note 2]	t_{CONV}				25t_{CY}	μs

Notes 1. Absolute accuracy excluding quantization error (±1/2 LSB)

2. Time from conversion start instruction execution (not including conversion start instruction execution time itself) to ADCEND = 1 (200 μs at fcc = 2 MHz)

Remark t_{CY} = 16/fcc (fcc: frequency of system clock oscillator)

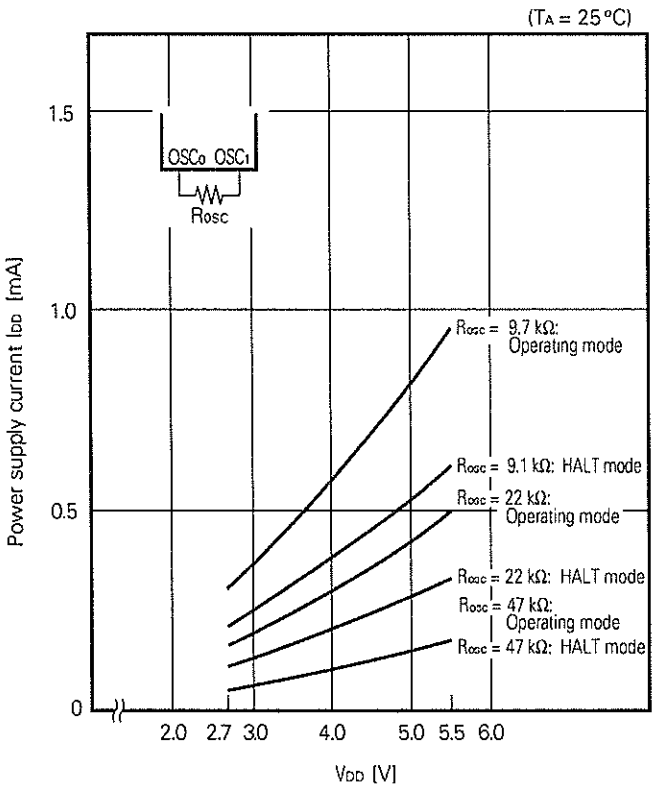
Characteristics of the power-on/power-down reset circuits (T_A = −40 to +85 °C)

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Unit
Power voltage rise time when power-on reset is valid	t_{POR}	V_{DD} = 0 → 2.7 V The power voltage (V_{DD}) must change from ground level to 2.7 V.			16t_{CY}	μs
Voltage for power-down reset circuit	V_{PDR}	When PDRESEN = 1		3.5	4.5	V

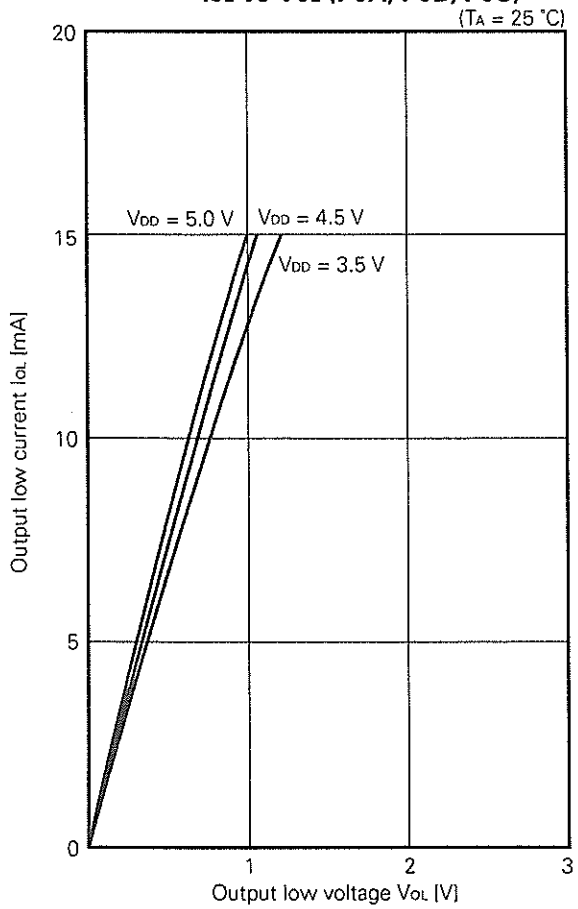
Remark t_{CY} = 16/fcc (fcc: frequency of system clock oscillator)

23. CHARACTERISTIC CURVES (FOR REFERENCE)

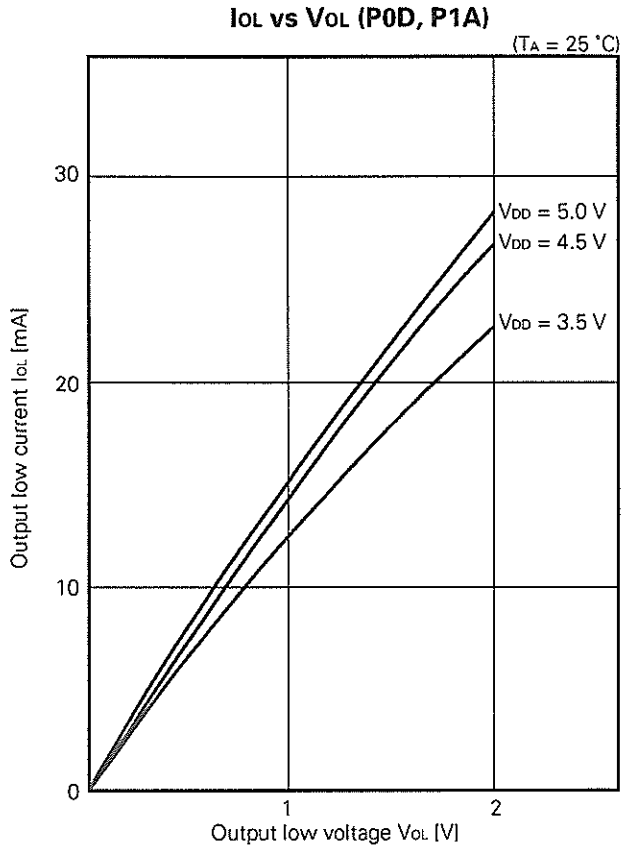
IDD vs VDD



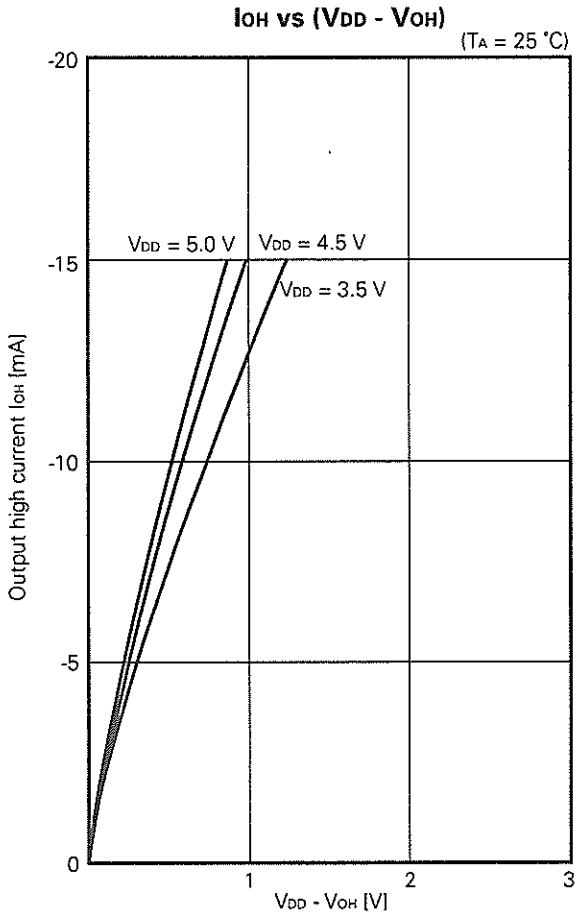
IOL vs VOL (P0A, P0B, P0C)



Caution Absolute maximum rating of output current is 15 mA per pin.

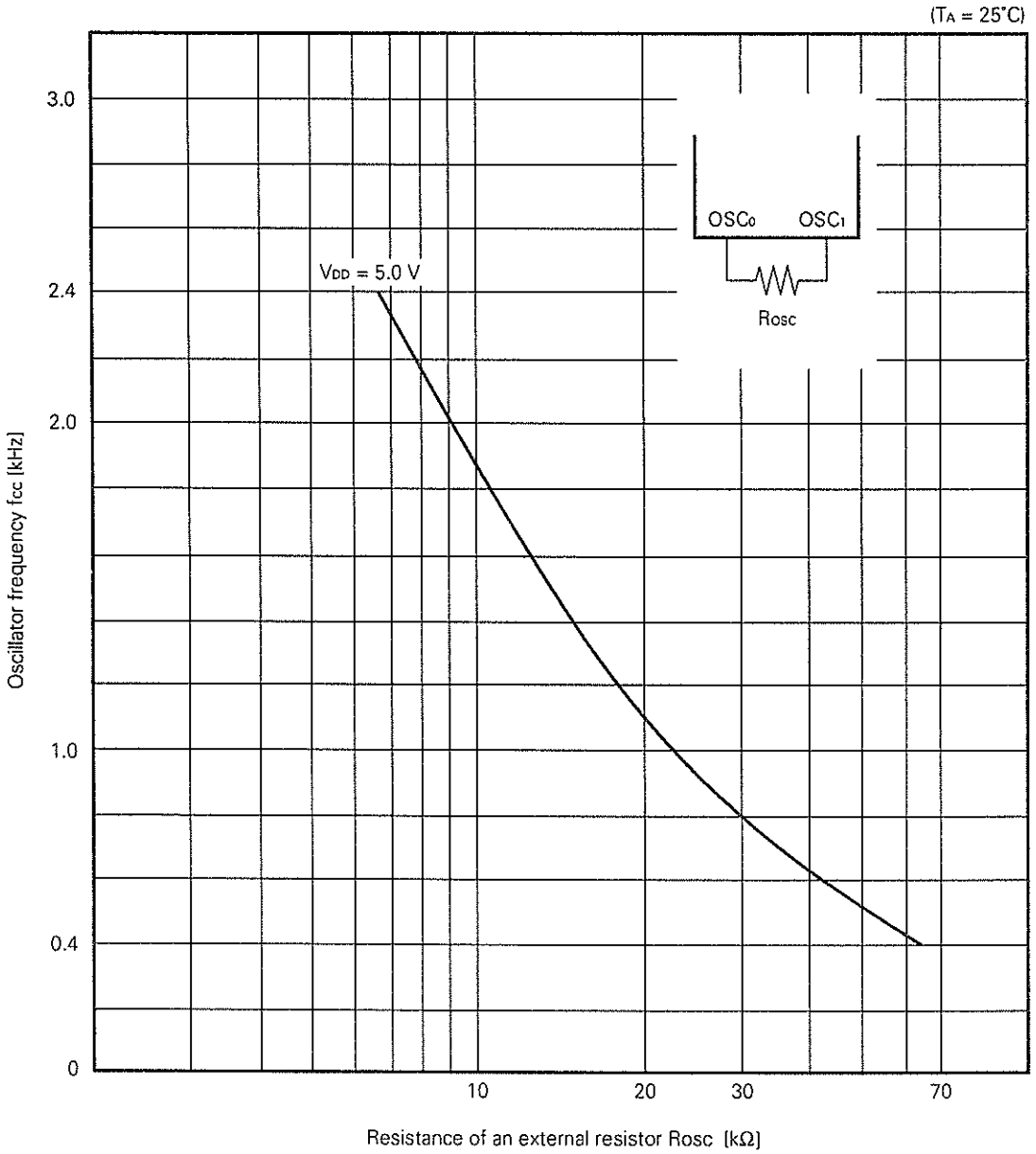


Caution Absolute maximum rating of output current is 30 mA per pin.



Caution Absolute maximum rating of output current is -15 mA per pin.

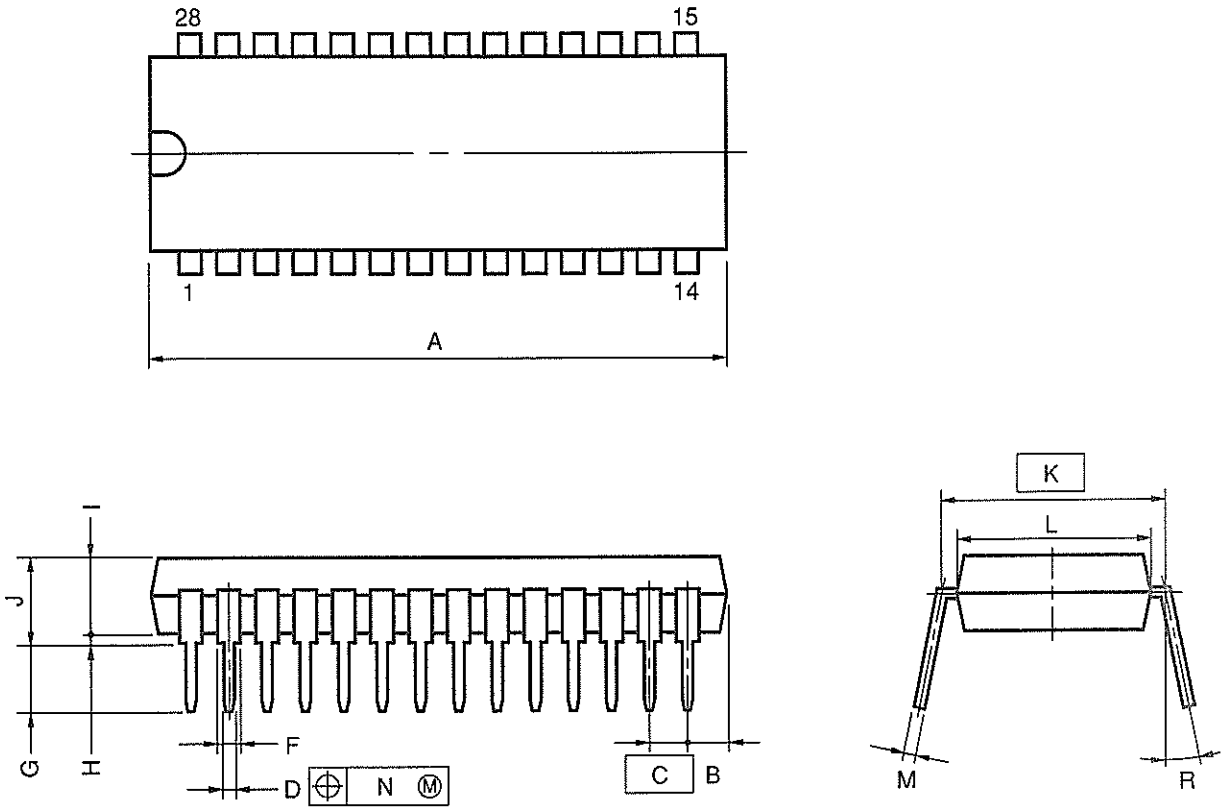
fcc vs Rosc


(TA = 25°C)
3.0
2.4
2.0
1.0
0.4
0
VDD = 5.0 V
OSC0
OSC1
Rosc
10
20
30
70
Oscillator frequency fcc [kHz]
Resistance of an external resistor Rosc [kΩ]

24. PACKAGE DRAWINGS

PACKAGE DRAWINGS OF MASS-PRODUCED PRODUCTS (1/2)

28 PIN PLASTIC SHRINK DIP (400 mil)



NOTES

1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

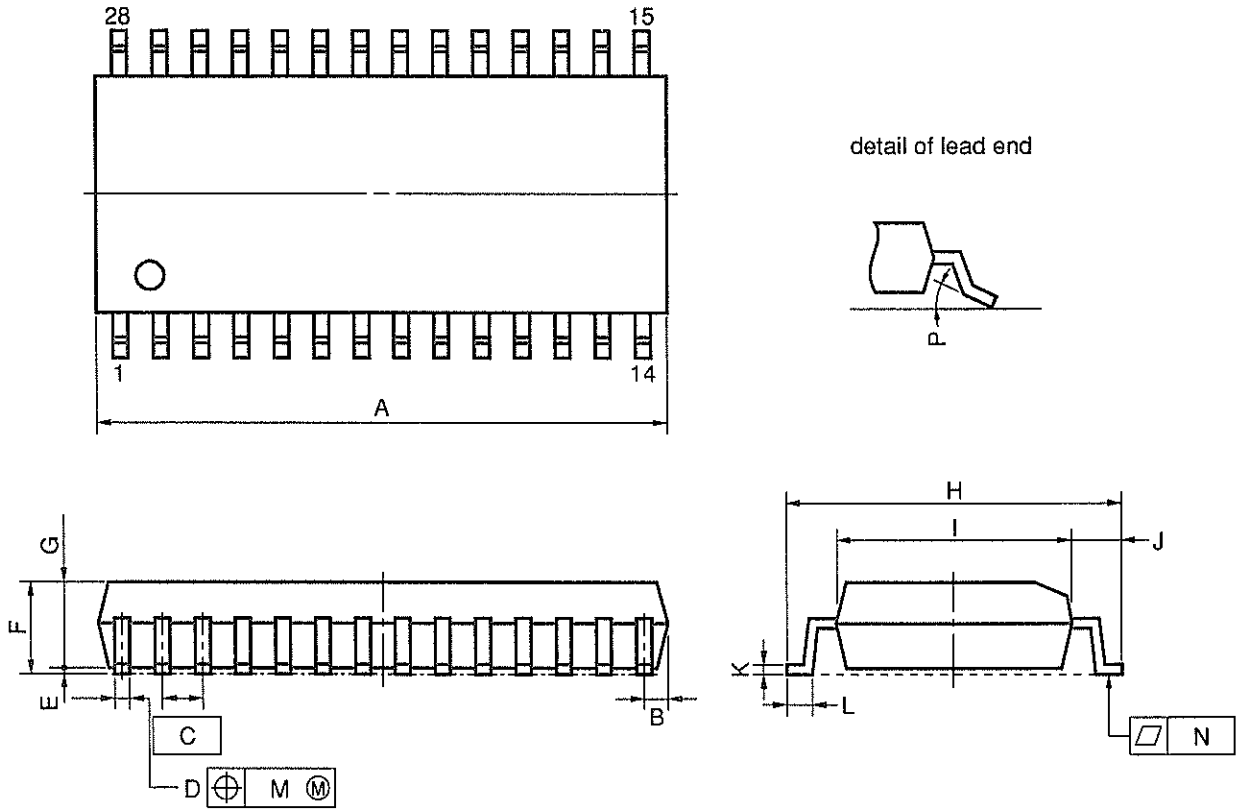
ITEM	MILLIMETERS	INCHES
A	28.46 MAX.	1.121 MAX.
B	2.67 MAX.	0.106 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.85 MIN.	0.033 MIN.
G	3.2 ± 0.3	0.126 ± 0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	8.6	0.339
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

S28C-70-400B-1

Caution The ES is different from the corresponding mass-produced products in shape and material. See "ES PACKAGE DRAWINGS (1/2)".

PACKAGE DRAWINGS OF MASS-PRODUCED PRODUCTS (2/2)

28 PIN PLASTIC SOP (375 mil)



NOTE

Each lead centerline is located within 0.12 mm (0.005 inch) of its true position (T.P.) at maximum material condition.

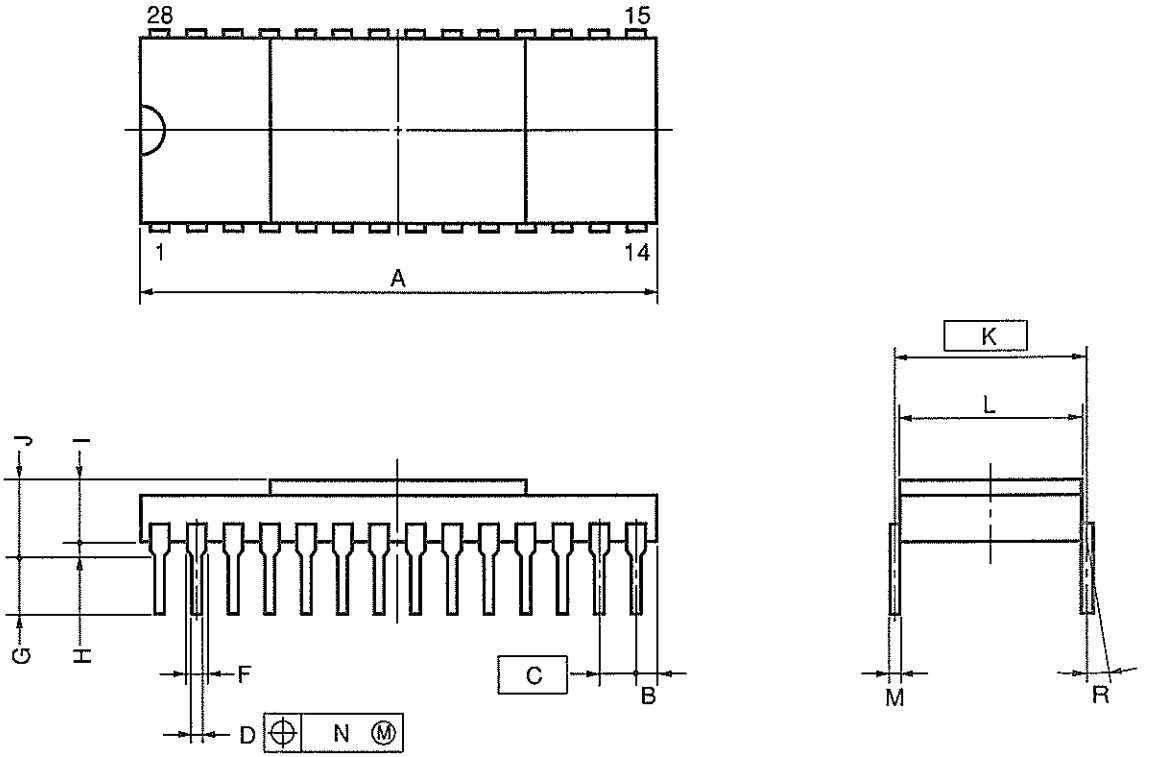
ITEM	MILLIMETERS	INCHES
A	18.07 MAX.	0.712 MAX.
B	0.78 MAX.	0.031 MAX.
C	1.27 (T.P.)	0.050 (T.P.)
D	$0.40^{+0.10}_{-0.05}$	$0.016^{+0.004}_{-0.003}$
E	0.1±0.1	0.004±0.004
F	2.9 MAX.	0.115 MAX.
G	2.50	0.098
H	10.3±0.3	$0.406^{+0.012}_{-0.013}$
I	7.2	0.283
J	1.6	0.063
K	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.002}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	0.12	0.005
N	0.15	0.006
P	$3°^{+7°}_{-3°}$	$3°^{+7°}_{-3°}$

P28GM-50-375B-3

Caution The ES is different from the corresponding mass-produced products in shape and material. See "ES PACKAGE DRAWINGS (2/2)".

ES PACKAGE DRAWINGS (1/2)

28 PIN CERAMIC SHRINK DIP (400mil) (FOR ES)



NOTES

1) Each lead centerline is located within 0.25 mm (0.01 inch) of its true position (T.P.) at maximum material condition.

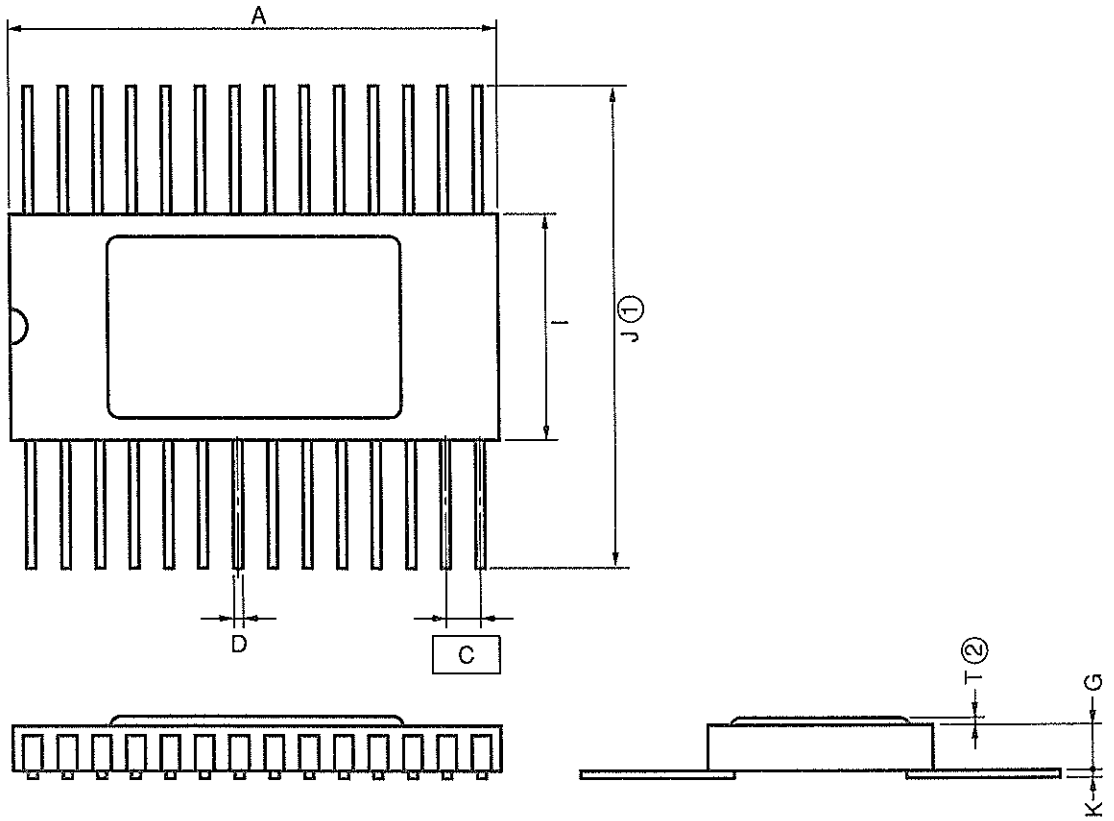
2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	28.0 MAX.	1.103 MAX.
B	5.1 MAX.	0.201 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.46±0.05	0.018±0.002
F	0.8 MIN.	0.031 MIN.
G	3.0±1.0	0.118±0.04
H	1.0 MIN.	0.039 MIN.
I	2.7	0.106
J	4.3 MAX.	0.170 MAX.
K	10.16 (T.P.)	0.400 (T.P.)
L	9.84	0.387
M	0.25±0.05	$0.010^{+0.002}_{-0.003}$
N	0.25	0.010
R	0~15°	0~15°

P28D-70-400B-1

ES PACKAGE DRAWINGS (2/2)

28 PIN CERAMIC SOP (FOR ES)



NOTE

The lengths of leads (①) and the height of potting (②) are not to be specified because the lead cutting process and the potting process are not controlled.

ITEM	MILLIMETERS	INCHES
A	18.0±0.2	$0.709^{+0.008}_{-0.009}$
C	1.27 (T.P.)	0.05 (T.P.)
D	0.4±0.05	$0.016^{+0.002}_{-0.003}$
G	1.52±0.15	0.06±0.006
I	8.4±0.15	$0.331^{+0.006}_{-0.007}$
J	16.4	0.646
K	0.15±0.025	0.006±0.001
T	1.0	0.039

X28B-50B1

Caution The lengths of leads are not to be specified because the process of cutting the lead ends is not yet controlled.

25. RECOMMENDED SOLDERING CONDITIONS

The following conditions (see table below) must be met when soldering the μPD17134B and μPD17136B.

For the details of the recommended soldering conditions refer to our document *SMD Surface Mount Technology Manual* (IEI-1207).

Please consult with our sales offices in case other soldering process is used, or in case soldering is done under different conditions.

Table 25-1 Soldering Conditions for Surface-Mount Devices

μPD17134BGT-xxx : 28-pin plastic SOP (375 mil)
μPD17136BGT-xxx : 28-pin plastic SOP (375 mil)

Soldering process	Soldering conditions	Symbol
Infrared ray reflow	Peak package's surface temperature: 230 °C Reflow time: 30 seconds or less (at 210 °C or more) Number of reflow processes: 1	IR30-00-1
VPS	Peak package's surface temperature: 215 °C Reflow time: 40 seconds or less (at 200 °C or more) Number of reflow processes: 1	VP15-00-1
Wave soldering	Temperature in the soldering vessel: 260 °C or less Soldering time: 10 seconds or less Number of reflow processes: 1 Preheating temperature: 120 °C max. (measured on the package surface)	WS60-00-1
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for each side of device)	Partial heating method

Caution Do not apply more than a single process at once, except for "Partial heating method."

Table 25-2 Soldering Conditions for Inserted Devices

μPD17134BCT-xxx : 28-pin plastic shrink DIP (400 mil)
μPD17136BCT-xxx : 28-pin plastic shrink DIP (400 mil)

Soldering process	Soldering conditions
Wave soldering (only for pins)	Temperature in the soldering vessel: 260 °C or less Soldering time: 10 seconds or less
Partial heating method	Terminal temperature: 300 °C or less Heat time: 3 seconds or less (for each side of device)

Caution In wave soldering, apply solder only to the pins. Care must be taken that jet solder does not contact the main body of the package.

APPENDIX DEVELOPMENT TOOLS

The following support tools are available for developing programs for the μPD17134B and μPD17136B.

Hardware

Name	Description
In-circuit emulator [IE-17K IE-17K-ET[Note 1] EMU-17K[Note 2]]	The IE-17K, IE-17K-ET, and EMU-17K are in-circuit emulators applicable to the 17K series. The IE-17K and IE-17K-ET are connected to the PC-9800 series (host machine) or IBM PC/AT™ through the RS-232-C interface. The EMU-17K is inserted into the extension slot of the PC-9800 series (host machine). Use the system evaluation board (SE board) corresponding to each product together with one of these in-circuit emulators. SIMPLEHOST™, a man machine interface, implements an advanced debug environment. The EMU-17K also enables user to check the contents of the data memory in real time.
SE board (SE-17134)	The SE-17134 is an SE board for the μPD17134A, μPD17135A, μPD17136A, and μPD17137A. It can be used as the SE board of the μPD17134B or μPD17136B together with the optional main chip μPD17134BCT-002 or μPD17136BCT-001. It is used solely for evaluating the system. It is also used for debugging in combination with the in-circuit emulator.
Main chip [μPD17134BCT-002 μPD17136BCT-001]	The μPD17134BCT-002 and μPD17136BCT-001 are the chips (main chips) for emulation. These chips are used on the SE-17134. Two identical chips are needed for one SE-17134.
Emulation probe (EP-17K28CT)	The EP-17K28CT is an emulation probe for the 17K series 28-pin shrink DIP (400 mil).
Emulation probe (EP-17K28GT)	The EP-17K28GT is an emulation probe for the 17K series 28-pin SOP (375 mil). Use this probe together with the conversion adapter EV-9500GT-28[Note 3], to check the target system with the corresponding SE board.
Conversion adapter (EV-9500GT-28[Note 3])	The EV-9500GT-28 is a conversion adapter for the 28-pin SOP (375 mil). Use this conversion adapter to connect the emulation probe, EP-17K28GT, to the target system.
PROM Programmer [AF-9703[Note 4] AF-9704[Note 4] AF-9705[Note 4] AF-9706[Note 4]]	The AF-9703, AF-9704, AF-9705, and AF-9706 are PROM writers for the μPD17P136B. Use one of these PROM writers with the program adapter, AF-9808F, to program the μPD17P136B.
Programmer adapter (AF-9808F[Note 4])	The AF-9808F is a socket unit for the μPD17P136B. It is used with the AF-9703, AF-9704, AF-9705, or AF-9706.

Notes 1. Low-end model, operating on an external power supply

2. The EMU-17K is a product of IC Co., Ltd. Contact IC Co., Ltd. (Tokyo, 03-3447-3793) for details.
3. An EP-17K28GT is supplied together with two EV-9500GT-28s. A set of five EV-9500GT-28s is also available.
4. The AF-9703, AF-9704, AF-9705, AF-9706, and AF-9808F are products of Ando Electric Co., Ltd. Contact Ando Electric Co., Ltd. (Tokyo, 03-3733-1151) for details.

Software

Name	Description	Host machine	OS		Distribution media	Part number
17K series assembler (AS17K)	AS17K is an assembler applicable to the 17K series. In developing μPD17134B, or μPD17136B program, AS17K is used in combination with a device file (AS17134B, or AS17136B).	PC-9800 series	MS-DOS™		5.25-inch, 2HD	μS5A10AS17K
					3.5-inch, 2HD	μS5A13AS17K
		IBM PC/AT	PC DOS™		5.25-inch, 2HC	μS7B10AS17K
					3.5-inch, 2HC	μS7B13AS17K
Device file (AS17134B, AS17136B)	AS17134B and AS17136B are device files for the μPD17134B, μPD17136B, and μPD17P136B. They are used together with the assembler (AS17K) which is applicable to the 17K series.	PC-9800 series	MS-DOS		5.25-inch, 2HD	μS5A10AS17134B[Note]
					3.5-inch, 2HD	μS5A13AS17134B[Note]
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10AS17134B[Note]
					3.5-inch, 2HC	μS7B13AS17134B[Note]
Support software (SIMPLEHOST)	SIMPLEHOST, running on the Windows™, provides man-machine-interface in developing programs by using a personal computer and the in-circuit emulator.	PC-9800 series	MS-DOS	Windows	5.25-inch, 2HD	μS5A10IE17K
					3.5-inch, 2HD	μS5A13IE17K
		IBM PC/AT	PC DOS		5.25-inch, 2HC	μS7B10IE17K
					3.5-inch, 2HC	μS7B13IE17K

Note μSxxxxAS17134B contains AS17134B and AS17136B.

Remark The following table lists the versions of the operating systems described in the above table.

OS	Versions
MS-DOS	Ver. 3.30 to Ver. 5.00A[Note]
PC DOS	Ver. 3.1 to Ver. 5.0[Note]
Windows	Ver. 3.0 to Ver. 3.1

Note MS-DOS versions 5.00 and 5.00A and PC DOS Ver. 5.0 are provided with a task swap function. This function, however, cannot be used in these software packages.

[MEMO]

Cautions on CMOS Devices

① **Countermeasures against static electricity for all MOSs**

Caution When handling MOS devices, take care so that they are not electrostatically charged.

Strong static electricity may cause dielectric breakdown in gates. When transporting or storing MOS devices, use conductive trays, magazine cases, shock absorbers, or metal cases that NEC uses for packaging and shipping. Be sure to ground MOS devices during assembling. Do not allow MOS devices to stand on plastic plates or do not touch pins. Also handle boards on which MOS devices are mounted in the same way.

② **CMOS-specific handling of unused input pins**

Caution Hold CMOS devices at a fixed input level.

Unlike bipolar or NMOS devices, if a CMOS device is operated with no input, an intermediate-level input may be caused by noise. This allows current to flow in the CMOS device, resulting in a malfunction. Use a pull-up or pull-down resistor to hold a fixed input level. Since unused pins may function as output pins at unexpected times, each unused pin should be separately connected to the V_{DD} or GND pin through a resistor.

If handling of unused pins is documented, follow the instructions in the document.

③ **Statuses of all MOS devices at initialization**

Caution The initial status of a MOS device is unpredictable when power is turned on.

Since characteristics of a MOS device are determined by the amount of ions implanted in molecules, the initial status cannot be determined in the manufacture process. NEC has no responsibility for the output statuses of pins, input and output settings, and the contents of registers at power on. However, NEC assures operation after reset and items for mode setting if they are defined.

When you turn on a device having a reset function, be sure to reset the device first.

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