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# MOS INTEGRATED CIRCUIT $\mu PD23C32000AL$

### 32M-BIT MASK-PROGRAMMABLE ROM 4M-WORD BY 8-BIT (BYTE MODE) / 2M-WORD BY 16-BIT (WORD MODE)

#### **Description**

The  $\mu$ PD23C32000AL is a 33,554,432 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 4,194,304 words by 8 bits, WORD mode : 2,097,152 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

The  $\mu$ PD23C32000AL is packed in 48-pin PLASTIC TSOP (I) and 44-pin PLASTIC SOP.

#### **Features**

Word organization

4,194,304 words by 8 bits (BYTE mode)

2,097,152 words by 16 bits (WORD mode)

• Operating supply voltage : Vcc = 2.7 V to 3.6 V

Operating supply voltage	Access time	Power supply current (Active mode)	Standby current (CMOS level input)
Vcc	ns (MAX.)	mA (MAX.)	μ <b>Α</b> (MAX.)
$3.0~\text{V}\pm0.3~\text{V}$	100	30	30
$3.3~\text{V}\pm0.3~\text{V}$	90		

#### **Ordering Information**

	Part Number		Package
	μPD23C32000ALGY-xxx-MJH	48-pin	PLASTIC TSOP (I) (12 x 18) (Normal bent)
	μPD23C32000ALGY-xxx-MKH	48-pin	PLASTIC TSOP (I) (12 x 18) (Reverse bent)
	μPD23C32000ALGX-xxx	44-pin	PLASTIC SOP (15.24 mm (600))
<r></r>	$\mu$ PD23C32000ALGY-xxx-MJH-A	48-pin	PLASTIC TSOP (I) (12 x 18) (Normal bent)
<r></r>	$\mu$ PD23C32000ALGY-xxx-MKH-A	48-pin	PLASTIC TSOP (I) (12 x 18) (Reverse bent)
<r></r>	μPD23C32000ALGX-xxx-A	44-pin	PLASTIC SOP (15.24 mm (600))

Remarks 1. xxx: ROM code suffix No.

<R> 2. Products with -A at the end of the part number are lead-free products.

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Document No. M15773EJ5V0DS00 (5th edition)
Date Published February 2006 NS CP(K)
Printed in Japan

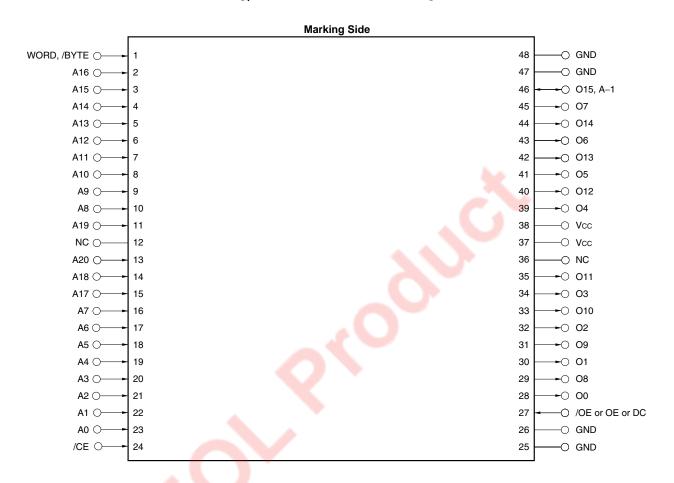
The mark <R> shows major revised points.

#### **Pin Configurations**

/xxx indicates active low signal.

### 48-pin PLASTIC TSOP (I) (12 x 18) (Normal bent) [ μPD23C32000ALGY-xxx-MJH ] [ μPD23C32000ALGY-xxx-MJH-A ]

<R>



A0 to A20 : Address inputs
O0 to O7, O8 to O14 : Data outputs

O15, A-1 : Data output 15 (WORD mode),

LSB Address input (BYTE mode)

WORD, /BYTE : Mode select
/CE : Chip Enable
/OE or OE : Output Enable
Vcc : Supply voltage

GND : Ground

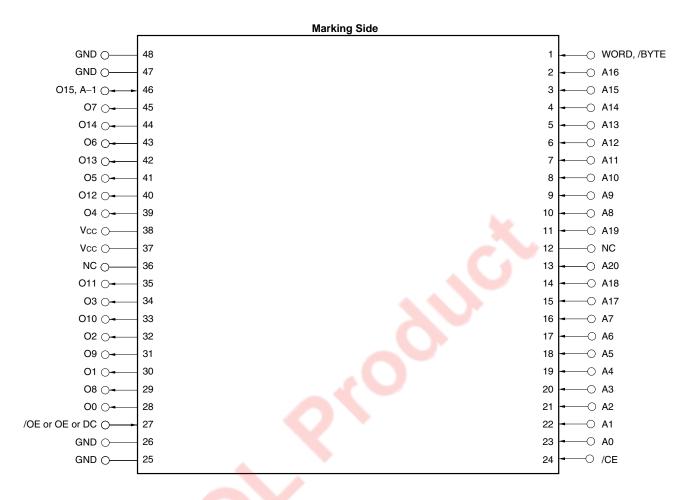
NC No Connection
DC : No Connection

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to Package Drawings for the 1-pin index mark.

## 48-pin PLASTIC TSOP (I) (12 x 18) (Reverse bent) [ μPD23C32000ALGY-xxx-MKH ] [ μPD23C32000ALGY-xxx-MKH-A ]

<R>



A0 to A20 : Address inputs
O0 to O7, O8 to O14 : Data outputs

O15, A-1 : Data output 15 (WORD mode),

LSB Address input (BYTE mode)

WORD, /BYTE : Mode select
/CE : Chip Enable
/OE or OE : Output Enable
Vcc : Supply voltage

GND : Ground

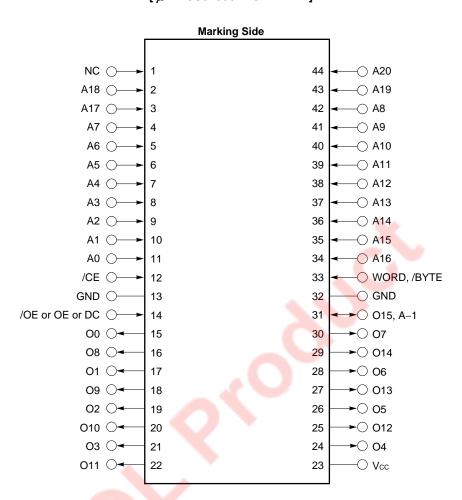
NC No Connection
DC : Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to Package Drawings for the 1-pin index mark.

### 44-pin PLASTIC SOP (15.24 mm (600)) [ μPD23C32000ALGX-xxx ] [ μPD23C32000ALGX-xxx-A ]

<R>



A0 to A20 : Address inputs
O0 to O7, O8 to O14 : Data outputs

O15, A-1 : Data output 15 (WORD mode),

: Ground

LSB Address input (BYTE mode)

WORD, /BYTE : Mode select
/CE : Chip Enable
/OE or OE : Output Enable
Vcc : Supply voltage

NC No Connection
DC : Don't Care

**GND** 

**Note** Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to Package Drawings for the 1-pin index mark.



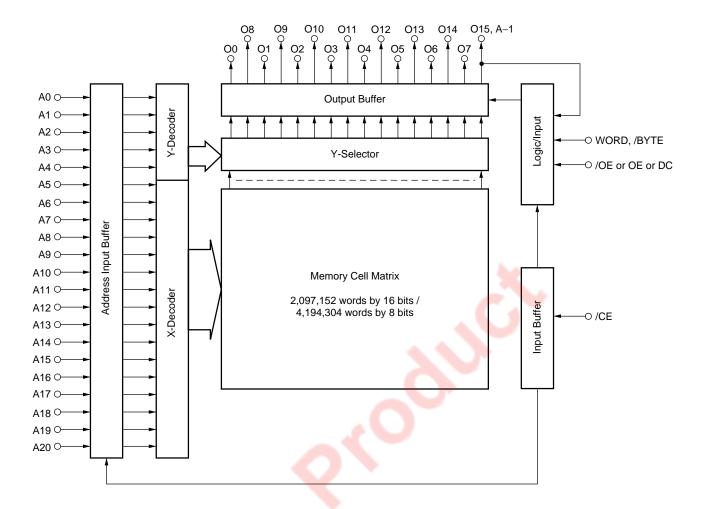
#### **Input / Output Pin Functions**

Pin name	Input / Output	Function	
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode.	
		High level: WORD mode (2M-word by 16-bit)	
		Low level : BYTE mode (4M-word by 8-bit)	
A0 to A20	Input	Address input pins.	
(Address inputs)		A0 to A20 are used differently in the WORD mode and the BYTE mode.	
		WORD mode (2M-word by 16-bit)	
		A0 to A20 are used as 21 bits address signals.	
		BYTE mode (4M-word by 8-bit)	
		A0 to A20 are used as the upper 21 bits of total 22 bits of address signal.	
		(The least significant bit (A–1) is combined to O15.)	
O0 to O7, O8 to O14	Output	Data output pins.	
(Data outputs)		O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode.	
		WORD mode (2M-word by 16-bit)	
		The lower 15 bits of 16 bits data outputs to O0 to O14.	
		(The most significant bit (O15) combined to A-1.)	
		BYTE mode (4M-word by 8-bit)	
		8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.	
O15, A-1	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode.	
(Data output 15,		WORD mode (2M-word by 16-bit)	
LSB Address input)		The most significant output data bus (O15).	
		BYTE mode (4M-word by 8-bit)	
		The least significant address bus (A-1).	
/CE	Input	Chip activating signal.	
(Chip Enable)		When the OE is active, output states are following.	
		High level : High-Z	
		Low level : Data out	
/OE or OE or DC	Input	Output enable signal. The active level of OE is mask option. The active level of OE	
(Output Enable, Don't care)		can be selected from high active, low active and Don't care at order.	
Vcc	-	Supply voltage	
GND	-	Ground	
NC	<b>/</b>	Not internally connected. (The signal can be connected.)	

Data Sheet M15773EJ5V0DS



#### **Block Diagram**





#### **Mask Option**

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	Н
х	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option: 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	Н		High-Z
Н	H or L	Standby	High-Z

Operation mode (Option: 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	Н		Data out
Н	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
Н	H or L	Standby	High-Z

Remark L: Low level input

H: High level input



#### **Electrical Specifications**

#### **Absolute Maximum Ratings**

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	Vcc		-0.3 to +4.6	V
Input voltage	Vı		-0.3 to Vcc+0.3	V
Output voltage	Vo		-0.3 to Vcc+0.3	V
Operating ambient temperature	TA		-10 to +70	°C
Storage temperature	T <sub>stg</sub>		-65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

#### Capacitance (TA = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	Сі	f = 1 MHz	<b>J</b>		10	pF
Output capacitance	Со				12	pF

#### DC Characteristics (TA = -10 to +70 °C, Vcc = 2.7 to 3.6 V)

Parameter	Symbol	Test cond	MIN.	TYP.	MAX.	Unit	
High level input voltage	VIH		•	2.0		Vcc + 0.3	V
Low level input voltage	VIL	$Vcc = 3.0 \text{ V} \pm 0.3 \text{ V}$		-0.3		+0.5	٧
		$Vcc = 3.3 \text{ V} \pm 0.3 \text{ V}$		-0.3		+0.8	
High level output voltage	Vон	$I_{OH} = -100 \ \mu A$	Ioн = -100 μA				V
Low level output voltage	Vol	IoL = 2.1 mA				0.4	V
Input leakage current	lu	V <sub>I</sub> = 0 V to Vcc		-10		+10	μА
Output leakage current	ILO	Vo = 0 V to Vcc, Chip des	selected	-10		+10	μА
Power supply current	Icc1	/CE = V <sub>IL</sub> (Active mode),	$Vcc = 3.0 \text{ V} \pm 0.3 \text{ V}$			30	mA
		Io = 0 mA	$Vcc = 3.3 \text{ V} \pm 0.3 \text{ V}$			30	
Standby current	Іссз	/CE = Vcc - 0.2 V (Stand	by mode)			30	μА



#### AC Characteristics (TA = -10 to +70 °C, Vcc = 2.7 to 3.6 V)

Parameter	Symbol	Test condition	Vcc :	$Vcc = 3.0 V \pm 0.3 V$		$Vcc = 3.3 V \pm 0.3 V$			Unit
			MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
Address access time	tacc				100			90	ns
Address skew time	tskew	Note			10			10	ns
Chip enable access time	tce				100			90	ns
Output enable access time	toe				25			25	ns
Output hold time	tон		0			0			ns
Output disable time	tof		0		25	0		25	ns
WORD, /BYTE access time	twв				100			90	ns

**Note** tskew indicates the following three types of time depending on the condition.

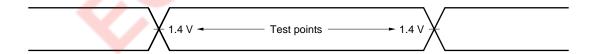
- 1) When switching /CE from high level to low level, tskew is the time from the /CE low level input point until the next address is determined.
- 2) When switching /CE from low level to high level, tskew is the time from the address change start point to the /CE high level input point.
- 3) When /CE is fixed to low level, tskew is the time from the address change start point until the next address is determined.

Since specs are defined for tskew only when /CE is active, tskew is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

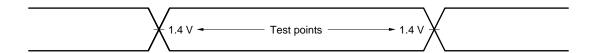
**Remark** to F is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

#### **AC Test Conditions**

Input waveform (Rise / Fall time ≤ 5 ns)



#### **Output waveform**



#### **Output load**

1TTL + 100 pF

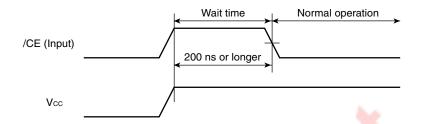


#### Cautions on power application

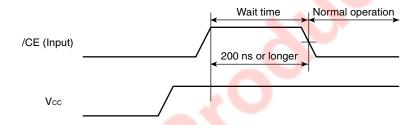
To ensure normal operation, always apply power using /CE following the procedure shown below.

- 1) Input a high level to /CE during and after power application.
- 2) Hold the high level input to /CE for 200 ns or longer (wait time).
- 3) Start normal operation after the wait time has elapsed.

#### Power Application Timing Chart 1 (When /CE is made high at power application)

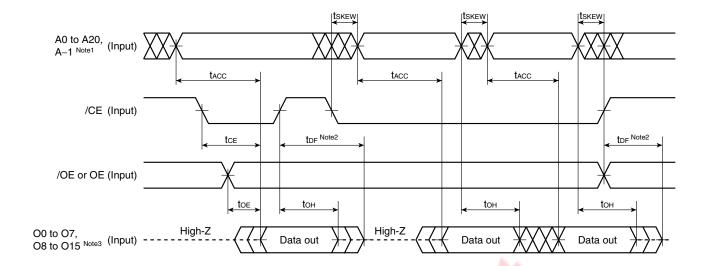


#### Power Application Timing Chart 2 (When /CE is made high after power application)



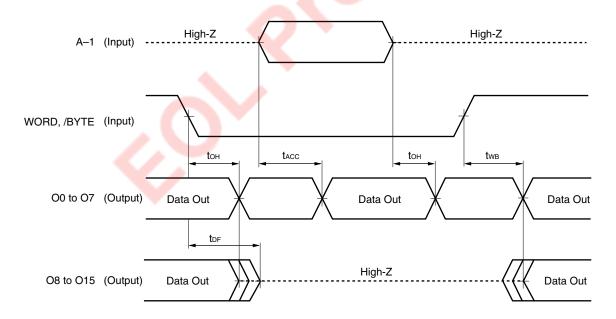
Caution Other signals can be either high or low during the wait time.

#### **Read Cycle Timing Chart**



- Notes 1. During WORD mode, A-1 is O15.
  - 2. top is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.
  - 3. During BYTE mode, O8 to O14 are high impedance and O15 is A-1.

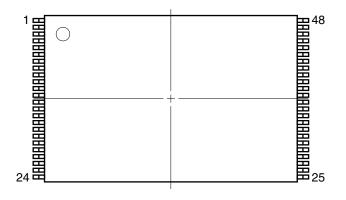
#### WORD, /BYTE Switch Timing Chart

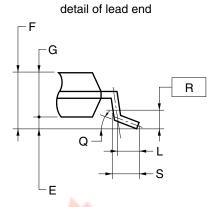


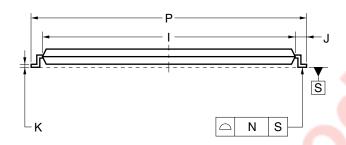
Remark Chip Enable (/CE) and Output Enable (/OE or OE): Active.

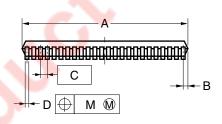
#### **Package Drawings**

#### 48-PIN PLASTIC TSOP(I) (12x18)









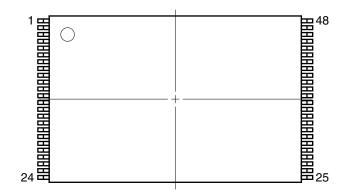
#### NOTES

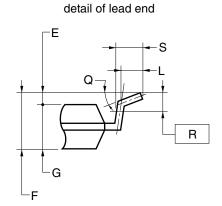
- 1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash: 12.4 mm MAX.)

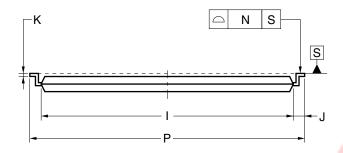
ITEM	MILLIMETERS
Α	12.0±0.1
В	0.45 MAX.
С	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
- 1	16.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
М	0.10
N	0.10
Р	18.0±0.2
Q	3°+5°
R	0.25
S	0.60±0.15

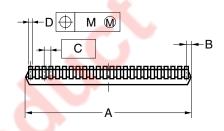
S48GY-50-MJH1-1

#### 48-PIN PLASTIC TSOP(I) (12x18)









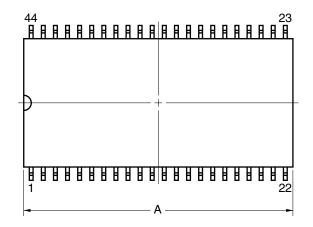
#### **NOTES**

- 1. Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.
- 2. "A" excludes mold flash. (Includes mold flash: 12.4 mm MAX.)

ITEM	MILLIMETERS		
Α	12.0±0.1		
В	0.45 MAX.		
С	0.5 (T.P.)		
D	0.22±0.05		
Е	0.1±0.05		
F	1.2 MAX.		
G	1.0±0.05		
I	16.4±0.1		
J	0.8±0.2		
K	0.145±0.05		
L	0.5		
М	0.10		
N	0.10		
Р	18.0±0.2		
Q	3°+5°		
R	0.25		
S	0.60±0.15		

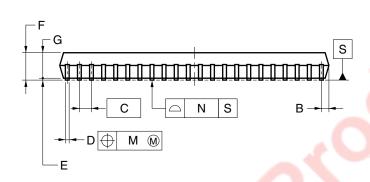
S48GY-50-MKH1-1

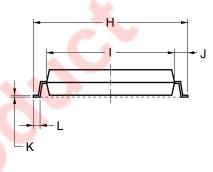
#### 44-PIN PLASTIC SOP (15.24 mm (600))



detail of lead end







#### NOTE

Each lead centerline is located within 0.12 mm of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS		
Α	27.83 <sup>+0.4</sup> <sub>-0.05</sub>		
В	0.78 MAX.		
С	1.27 (T.P.)		
D	$0.42^{+0.08}_{-0.07}$		
E	0.15±0.1		
F	3.0 MAX.		
G	2.7±0.05		
Н	16.04±0.3		
1	13.24±0.1		
J	1.4±0.2		
К	$0.22^{+0.08}_{-0.07}$		
L	0.8±0.2		
М	0.12		
N	0.10		
Р	3°+7°		

P44GX-50-600A-4



#### **Recommended Soldering Conditions**

Please consult with our sales offices for soldering conditions of the  $\mu$ PD23C32000AL.

#### **Types of Surface Mount Device**

 $\mu$ PD23C32000ALGY-MJH : 48-pin PLASTIC TSOP (I) (12 x 18) (Normal bent)  $\mu$ PD23C32000ALGY-MKH : 48-pin PLASTIC TSOP (I) (12 x 18) (Reverse bent)

μPD23C32000ALGX : 44-pin PLASTIC SOP (15.24 mm (600))

<R> μPD23C32000ALGY-MJH-A: 48-pin PLASTIC TSOP (I) (12 x 18) (Normal bent)
<R> μPD23C32000ALGY-MKH-A: 48-pin PLASTIC TSOP (I) (12 x 18) (Reverse bent)

<R>>  $\mu$ PD23C32000ALGX-A : 44-pin PLASTIC SOP (15.24 mm (600))





#### **Revision History**

Edition/	Pa	ige	Type of	Location	Description
Date	This	Previous	revision		(Previous edition This edition)
	edition	edition			
5th edition/	p.1	p.1	Addition	Ordering Information	Lead-free products have been added
Feb. 2006	pp.2-4	pp.2-4	Addition	Pin Configuration	Lead-free products have been added
	p.15	p.15	Addition	Recommended Soldering	Lead-free products have been added
				Conditions	



[MEMO]



[MEMO]



#### - NOTES FOR CMOS DEVICES

#### (1) VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{\rm IL}$  (MAX) and  $V_{\rm IH}$  (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{\rm IL}$  (MAX) and  $V_{\rm IH}$  (MIN).

#### (2) HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to VDD or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

#### ③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

#### **4** STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

#### **5** POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

#### 6 INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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