To our customers,

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April 1st, 2010
Renesas Electronics Corporation

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NEC

MOS INTEGRATED CIRCUIT

μPD23C64340, 23C64380

64M-BIT MASK-PROGRAMMABLE ROM
8M-WORD BY 8-BIT (BYTE MODE) / 4M-WORD BY 16-BIT (WORD MODE)
PAGE ACCESS MODE

Description

The μPD23C64340 and μPD23C64380 are 67,108,864 bits mask-programmable ROM. The word organization is selectable (BYTE mode : 8,388,608 words by 8 bits, WORD mode : 4,194,304 words by 16 bits).

The active levels of OE (Output Enable Input) can be selected with mask-option.

★ The μPD23C64340 and μPD23C64380 are packed in 48-pin PLASTIC TSOP (I) and 48-pin TAPE FBGA.

Features

- Pin compatible with NOR Flash Memory
- Word organization
  - 8,388,608 words by 8 bits (BYTE mode)
  - 4,194,304 words by 16 bits (WORD mode)
- Page access mode
  - BYTE mode : 8 byte random page access (μPD23C64340)
  - 16 byte random page access (μPD23C64380)
  - WORD mode : 4 word random page access (μPD23C64340)
  - 8 word random page access (μPD23C64380)
- Operating supply voltage : V_{CC} = 2.7 V to 3.6 V

	Operating supply voltage V_{CC}	Access time / Page access time ns (MAX.)	Power supply current (Active mode) mA (MAX.)		Standby current (CMOS level input) μA (MAX.)
			μPD23C64340	μPD23C64380	
★	3.0 V ± 0.3 V	120 / 30	40	60	30
★	3.3 V ± 0.3 V	100 / 25	55	75	

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Printed in Japan

The mark ★ shows major revised points.

Ordering Information

	Part Number	Package
★	μPD23C64340GZ-xxx-MJH	48-pin PLASTIC TSOP (I) (12 x 20) (Normal bent)
★	μPD23C64340GZ-xxx-MKH	48-pin PLASTIC TSOP (I) (12 x 20) (Reverse bent)
	μPD23C64340F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)
★	μPD23C64340GZ-xxx-MJH-A	48-pin PLASTIC TSOP (I) (12 x 20) (Normal bent)
★	μPD23C64340GZ-xxx-MKH-A	48-pin PLASTIC TSOP (I) (12 x 20) (Reverse bent)
★	μPD23C64340F9-xxx-BC3-A	48-pin TAPE FBGA (8 x 6)
★	μPD23C64380GZ-xxx-MJH	48-pin PLASTIC TSOP (I) (12 x 20) (Normal bent)
★	μPD23C64380GZ-xxx-MKH	48-pin PLASTIC TSOP (I) (12 x 20) (Reverse bent)
	μPD23C64380F9-xxx-BC3	48-pin TAPE FBGA (8 x 6)
★	μPD23C64380GZ-xxx-MJH-A	48-pin PLASTIC TSOP (I) (12 x 20) (Normal bent)
★	μPD23C64380GZ-xxx-MKH-A	48-pin PLASTIC TSOP (I) (12 x 20) (Reverse bent)
★	μPD23C64380F9-xxx-BC3-A	48-pin TAPE FBGA (8 x 6)

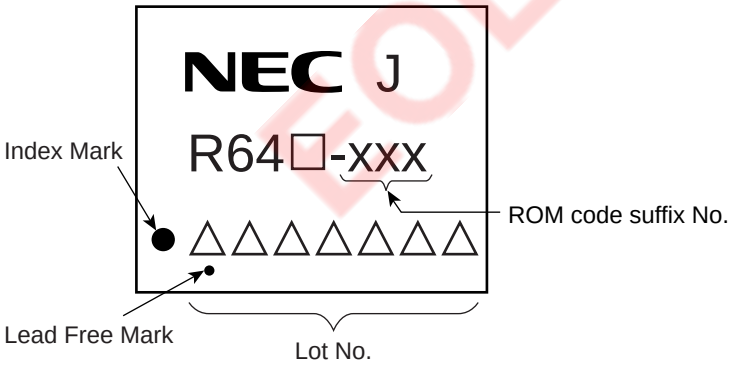
Remarks 1. xxx : ROM code suffix No.

★ **2.** Products with -A at the end of the part number are lead-free products.

Marking Image

	Part Number	Marking (□)
	μPD23C64340F9-xxx-BC3	B
★	μPD23C64340F9-xxx-BC3-A	B
	μPD23C64380F9-xxx-BC3	C
★	μPD23C64380F9-xxx-BC3-A	C

★



Pin Configuration

/xxx indicates active low signal.

★ **48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)**

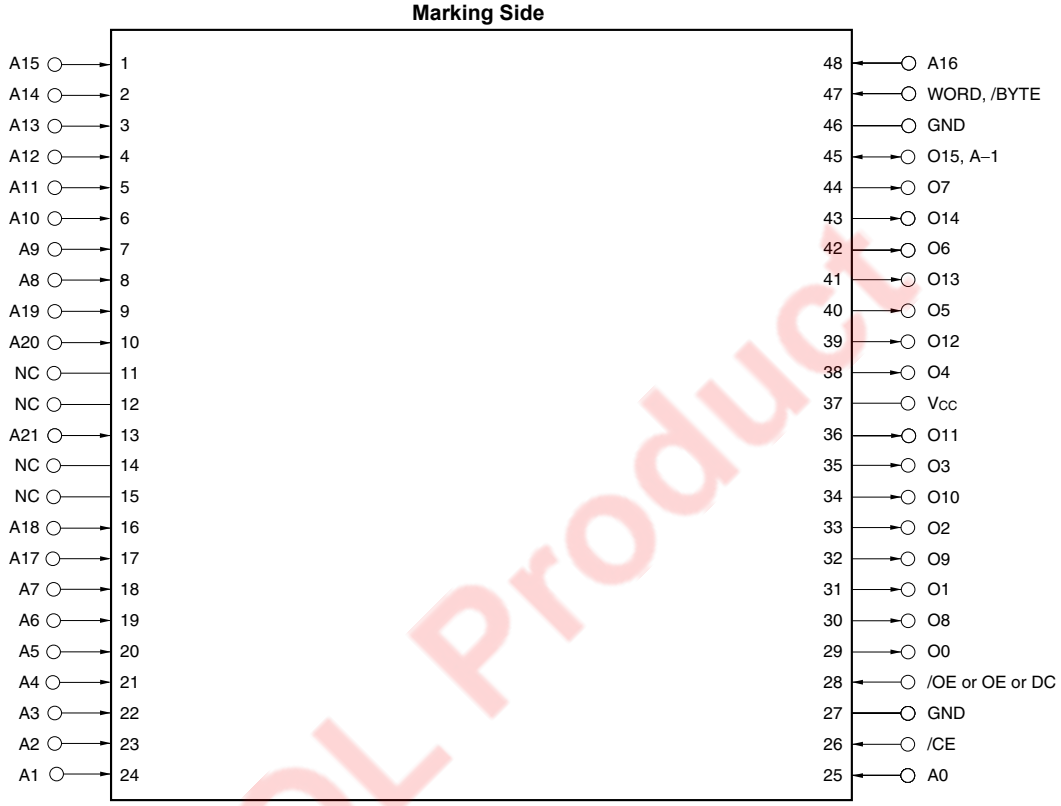
[μPD23C64340GZ-xxx-MJH]

[μPD23C64340GZ-xxx-MJH-A]

[μPD23C64380GZ-xxx-MJH]

[μPD23C64380GZ-xxx-MJH-A]

Marking Side



A0 to A21	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE or OE	:	Output Enable
V_{CC}	:	Supply voltage
GND	:	Ground
NC [Note]	:	No Connection
DC	:	Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the 1-pin index mark.

★ **48-pin PLASTIC TSOP(I) (12 x 20) (Reverse bent)**

[μPD23C64340GZ-xxx-MKH]

[μPD23C64340GZ-xxx-MKH-A]

[μPD23C64380GZ-xxx-MKH]

[μPD23C64380GZ-xxx-MKH-A]

Marking Side

A0 to A21	:	Address inputs
O0 to O7, O8 to O14	:	Data outputs
O15, A–1	:	Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE	:	Mode select
/CE	:	Chip Enable
/OE or OE	:	Output Enable
VCC	:	Supply voltage
GND	:	Ground
NC Note	:	No Connection
DC	:	Don't Care

Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawings** for the 1-pin index mark.

48-pin TAPE FBGA (8 x 6)

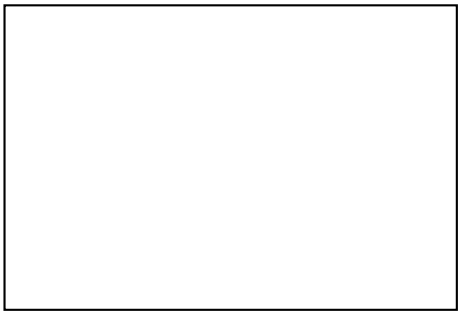
[μPD23C64340F9-xxx-BC3]

★ **[μPD23C64340F9-xxx-BC3-A]**

[μPD23C64380F9-xxx-BC3]

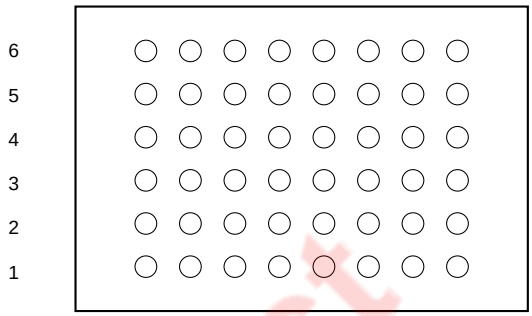
★ **[μPD23C64380F9-xxx-BC3-A]**

Top View



A B C D E F G H

Bottom View



H G F E D C B A

	A	B	C	D	E	F	G	H
6	A13	A12	A14	A15	A16	WORD, /BYTE	O15, A–1	GND
5	A9	A8	A10	A11	O7	O14	O13	O6
4	NC	NC	A21	A19	O5	O12	V_{CC}	O4
3	NC	NC	A18	A20	O2	O10	O11	O3
2	A7	A17	A6	A5	O0	O8	O9	O1
1	A3	A4	A2	A1	A0	/CE	/OE or OE	GND

	H	G	F	E	D	C	B	A
6	GND	O15, A–1	WORD, /BYTE	A16	A15	A14	A12	A13
5	O6	O13	O14	O7	A11	A10	A8	A9
4	O4	V_{CC}	O12	O5	A19	A21	NC	NC
3	O3	O11	O10	O2	A20	A18	NC	NC
2	O1	O9	O8	O0	A5	A6	A17	A7
1	GND	/OE or OE	/CE	A0	A1	A2	A4	A3

A0 to A21 : Address inputs
O0 to O7, O8 to O14 : Data outputs
O15, A–1 : Data output 15 (WORD mode), LSB Address input (BYTE mode)
WORD, /BYTE : Mode select
/CE : Chip Enable
/OE or OE : Output Enable
V_{CC} : Supply voltage
GND : Ground
NC [Note] : No Connection
DC : Don't Care

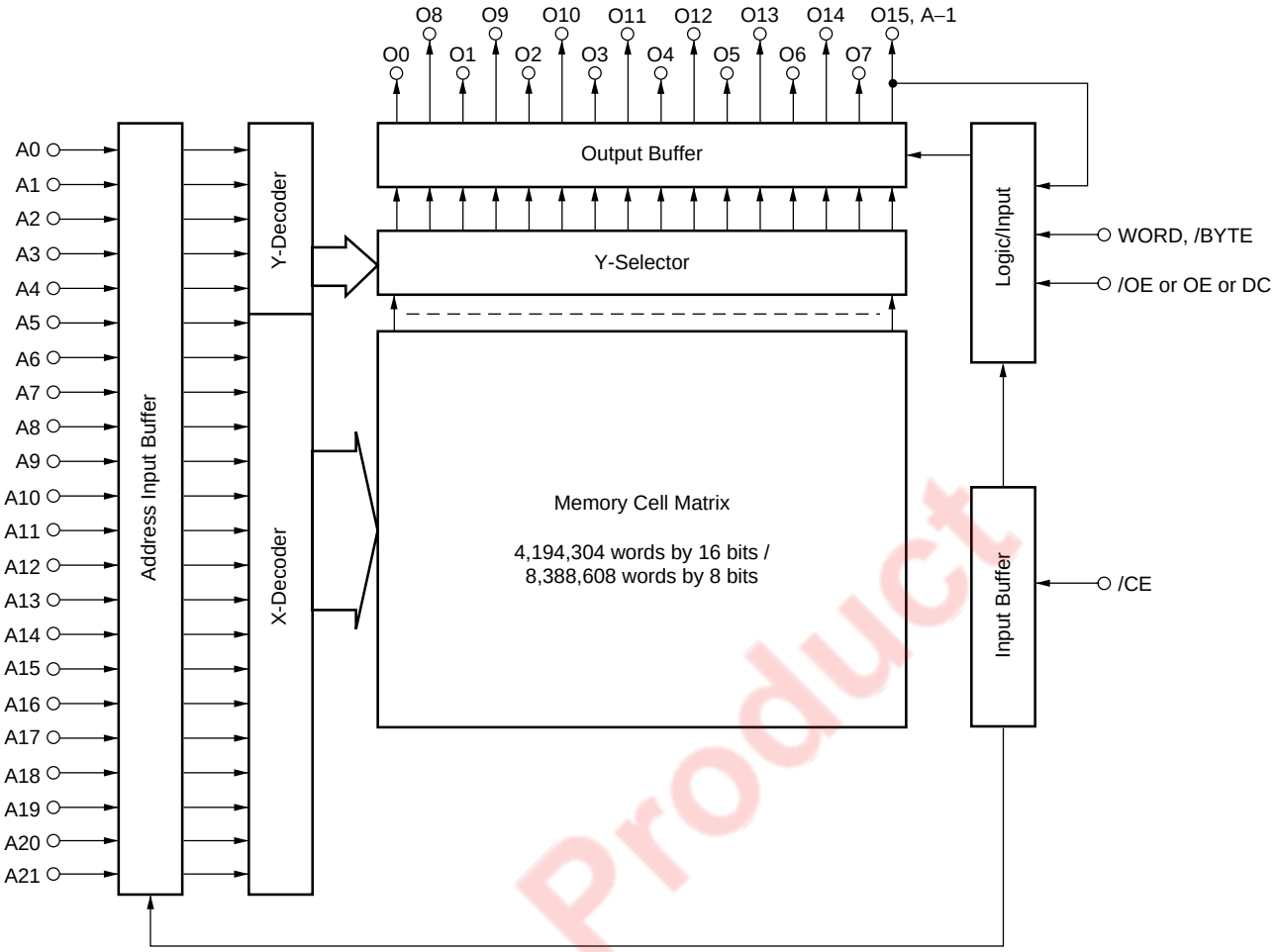
Note Some signals can be applied because this pin is not connected to the inside of the chip.

Remark Refer to **Package Drawing** for the index mark.

Input / Output Pin Functions

Pin name	Input / Output	Function
WORD, /BYTE	Input	The pin for switching WORD mode and BYTE mode. **High level** : WORD mode (4M-word by 16-bit) **Low level** : BYTE mode (8M-word by 8-bit)
A0 to A21 (Address inputs)	Input	Address input pins. A0 to A21 are used differently in the WORD mode and the BYTE mode. **WORD mode (4M-word by 16-bit)** A0 to A21 are used as 22 bits address signals. **BYTE mode (8M-word by 8-bit)** A0 to A21 are used as the upper 22 bits of total 23 bits of address signal. (The least significant bit (A–1) is combined to O15.)
O0 to O7, O8 to O14 (Data outputs)	Output	Data output pins. O0 to O7, O8 to O14 are used differently in the WORD mode and the BYTE mode. **WORD mode (4M-word by 16-bit)** The lower 15 bits of 16 bits data outputs to O0 to O14. (The most significant bit (O15) combined to A–1.) **BYTE mode (8M-word by 8-bit)** 8 bits data outputs to O0 to O7 and also O8 to O14 are high impedance.
O15, A–1 (Data output 15, LSB Address input)	Output, Input	O15, A–1 are used differently in the WORD mode and the BYTE mode. **WORD mode (4M-word by 16-bit)** The most significant output data bus (O15). **BYTE mode (8M-word by 8-bit)** The least significant address bus (A–1).
/CE (Chip Enable)	Input	Chip activating signal. When the OE is active, output states are following. **High level** : High-Z **Low level** : Data out
/OE or OE or DC (Output Enable, Don't care)	Input	Output enable signal. The active level of OE is mask option. The active level of OE can be selected from high active, low active and Don't care at order.
V_{CC}	–	Supply voltage
GND	–	Ground
NC	–	Not internally connected. (The signal can be connected.)

Block Diagram



Mask Option

The active levels of output enable pin (/OE or OE or DC) are mask programmable and optional, and can be selected from among " 0 " " 1 " " x " shown in the table below.

Option	/OE or OE or DC	OE active level
0	/OE	L
1	OE	H
x	DC	Don't care

Operation modes for each option are shown in the tables below.

Operation mode (Option : 0)

/CE	/OE	Mode	Output state
L	L	Active	Data out
	H		High-Z
H	H or L	Standby	High-Z

Operation mode (Option : 1)

/CE	OE	Mode	Output state
L	L	Active	High-Z
	H		Data out
H	H or L	Standby	High-Z

Operation mode (Option : x)

/CE	DC	Mode	Output state
L	H or L	Active	Data out
H	H or L	Standby	High-Z

Remark L : Low level input
H : High level input

Electrical Specifications

Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Supply voltage	V_{CC}		–0.3 to +4.6	V
Input voltage	V_I		–0.3 to V_{CC}+0.3	V
Output voltage	V_O		–0.3 to V_{CC}+0.3	V
Operating ambient temperature	T_A		–10 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Exposing the device to stress above those listed in Absolute Maximum Ratings could cause permanent damage. The device is not meant to be operated under conditions outside the limits described in the operational section of this specification. Exposure to Absolute Maximum Rating conditions for extended periods may affect device reliability.

Capacitance (T_A = 25 °C)

Parameter	Symbol	Test condition	MIN.	TYP.	MAX.	Unit
Input capacitance	C_I	f = 1 MHz			10	pF
Output capacitance	C_O				12	pF

DC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

Parameter	Symbol	Test conditions			MIN.	TYP.	MAX.	Unit
High level input voltage	V_{IH}				2.0		V_{CC} + 0.3	V
Low level input voltage	V_{IL}	V_{CC} = 3.0 V ± 0.3 V			–0.3		+0.5	V
		V_{CC} = 3.3 V ± 0.3 V			–0.3		+0.8	
High level output voltage	V_{OH}	I_{OH} = –100 μA			2.4			V
Low level output voltage	V_{OL}	I_{OL} = 2.1 mA					0.4	V
Input leakage current	I_{LI}	V_I = 0 V to V_{CC}			–10		+10	μA
Output leakage current	I_{LO}	V_O = 0 V to V_{CC}, Chip deselected			–10		+10	μA
Power supply current	I_{CC1}	/CE = V_{IL} (Active mode), I_O = 0 mA	μPD23C64340	V_{CC} = 3.0 V ± 0.3 V			40	mA
				V_{CC} = 3.3 V ± 0.3 V			55	
			μPD23C64380	V_{CC} = 3.0 V ± 0.3 V			60	
				V_{CC} = 3.3 V ± 0.3 V			75	
Standby current	I_{CC3}	/CE = V_{CC} – 0.2 V (Standby mode)					30	μA

AC Characteristics (T_A = –10 to +70 °C, V_{CC} = 2.7 to 3.6 V)

	Parameter	Symbol	Test condition	V_{CC} = 3.0 V ± 0.3 V			V_{CC} = 3.3 V ± 0.3 V			Unit
				MIN.	TYP.	MAX.	MIN.	TYP.	MAX.	
★	Address access time	t_{ACC}				120			100	ns
★	Page access time	t_{PAC}				30			25	ns
	Address skew time	t_{SKEW}	**Note**			10			10	ns
★	Chip enable access time	t_{CE}				120			100	ns
	Output enable access time	t_{OE}				25			25	ns
	Output hold time	t_{OH}		0			0			ns
	Output disable time	t_{DF}		0		25	0		25	ns
★	WORD, /BYTE access time	t_{WB}				120			100	ns

Note t_{SKEW} indicates the following three types of time depending on the condition.

1) When switching /CE from high level to low level, t_{SKEW} is the time from the /CE low level input point until the next address is determined.

2) When switching /CE from low level to high level, t_{SKEW} is the time from the address change start point to the /CE high level input point.

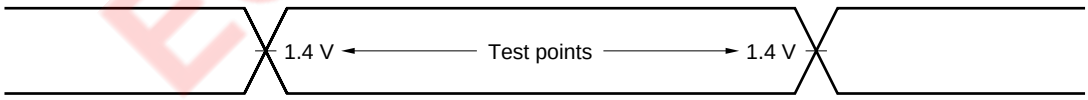
3) When /CE is fixed to low level, t_{SKEW} is the time from the address change start point until the next address is determined.

Since specs are defined for t_{SKEW} only when /CE is active, t_{SKEW} is not subject to limitations when /CE is switched from high level to low level following address determination, or when the address is changed after /CE is switched from low level to high level.

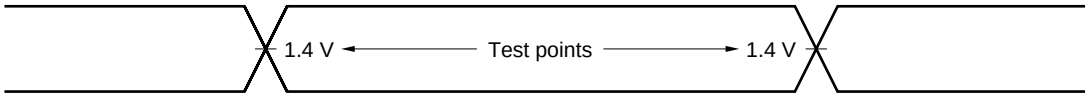
Remark t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

AC Test Conditions

Input waveform (Rise / Fall time ≤ 5 ns)



Output waveform



Output load

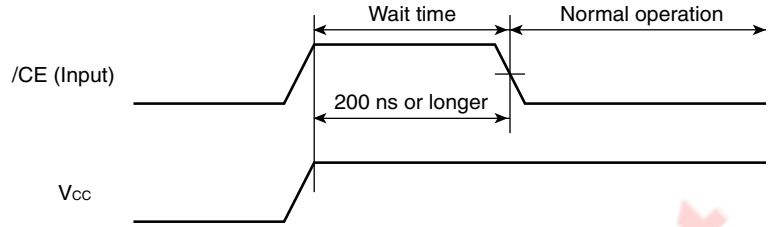
1TTL + 100 pF

Cautions on power application

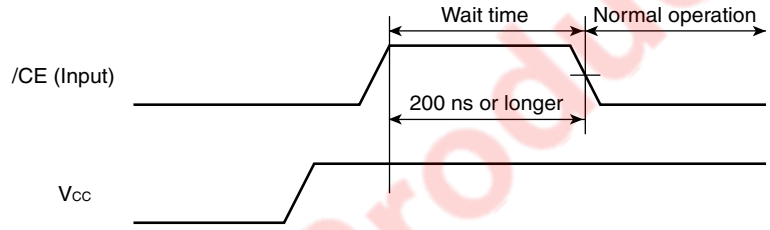
To ensure normal operation, always apply power using /CE following the procedure shown below.

1) Input a high level to /CE during and after power application.
2) Hold the high level input to /CE for 200 ns or longer (wait time).
3) Start normal operation after the wait time has elapsed.

Power Application Timing Chart 1 (When /CE is made high at power application)

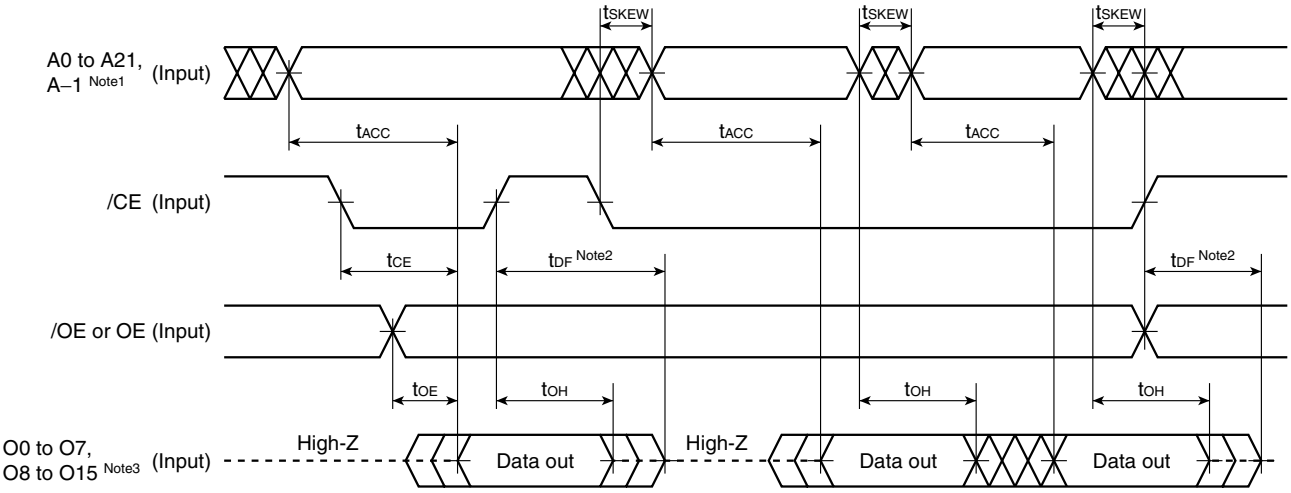


Power Application Timing Chart 2 (When /CE is made high after power application)



Caution Other signals can be either high or low during the wait time.

Read Cycle Timing Chart 1

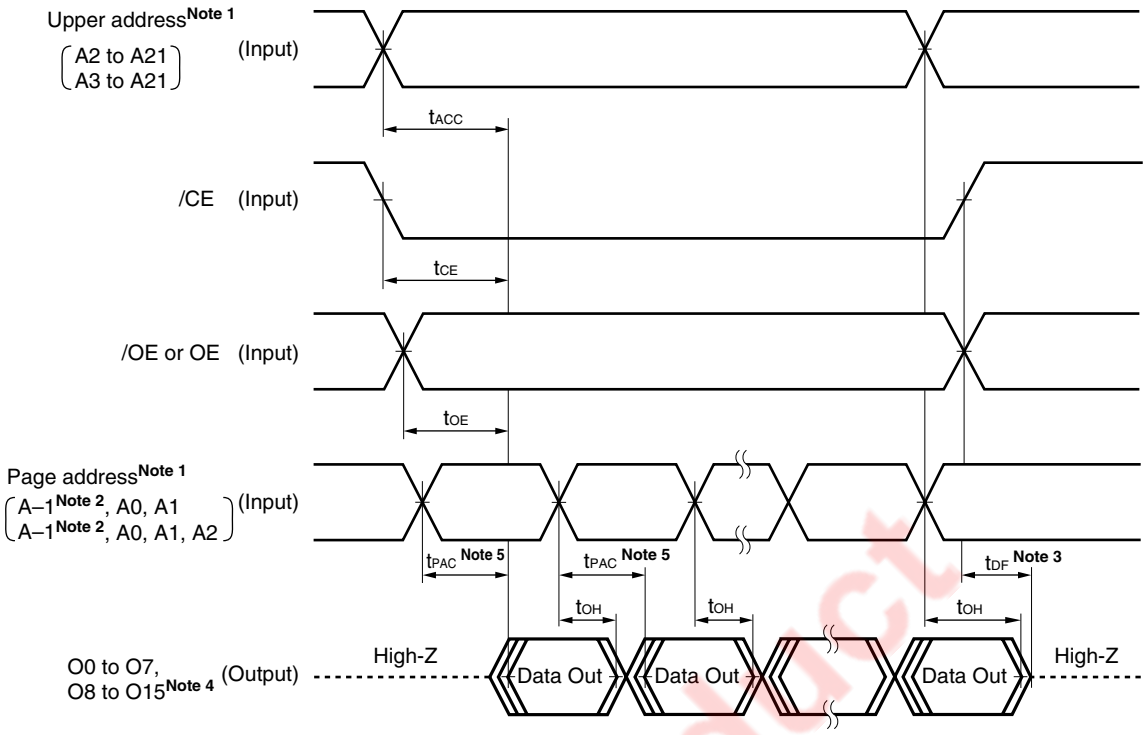


Notes 1. During WORD mode, A–1 is O15.

2. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

3. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

Read Cycle Timing Chart 2 (Page Access Mode)



Notes 1. The address differs depending on the product as follows.

Part Number	Upper address	Page address
μPD23C64340	A2 to A21	A–1, A0, A1
μPD23C64380	A3 to A21	A–1, A0, A1, A2

2. During WORD mode, A–1 is O15.

3. t_{DF} is the time from inactivation of Chip Enable input (/CE) or Output Enable input (/OE or OE) to high impedance state output.

4. During BYTE mode, O8 to O14 are high impedance and O15 is A–1.

5. The definition of page access time is as follows.

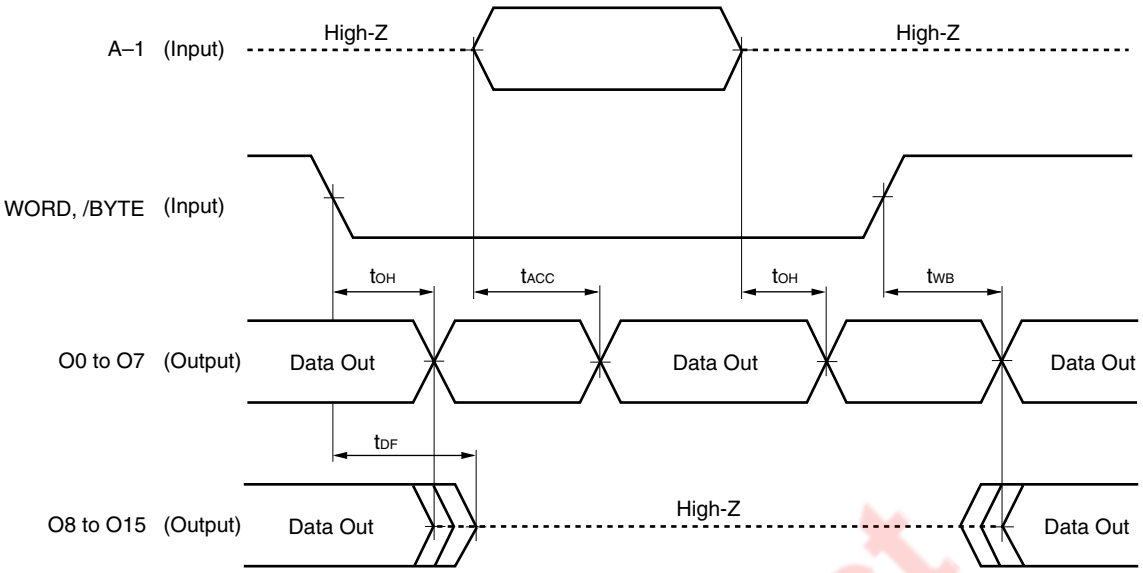
[μPD23C64340]

Page access time	Upper address (A2 to A21) inputs condition	/CE input condition	/OE or OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A–1, A0, A1)

[μPD23C64380]

Page access time	Upper address (A3 to A21) inputs condition	/CE input condition	/OE or OE input condition
t_{PAC}	Before $t_{ACC} - t_{PAC}$	Before $t_{CE} - t_{PAC}$	Before stabilizing of page address (A–1, A0, A1, A2)

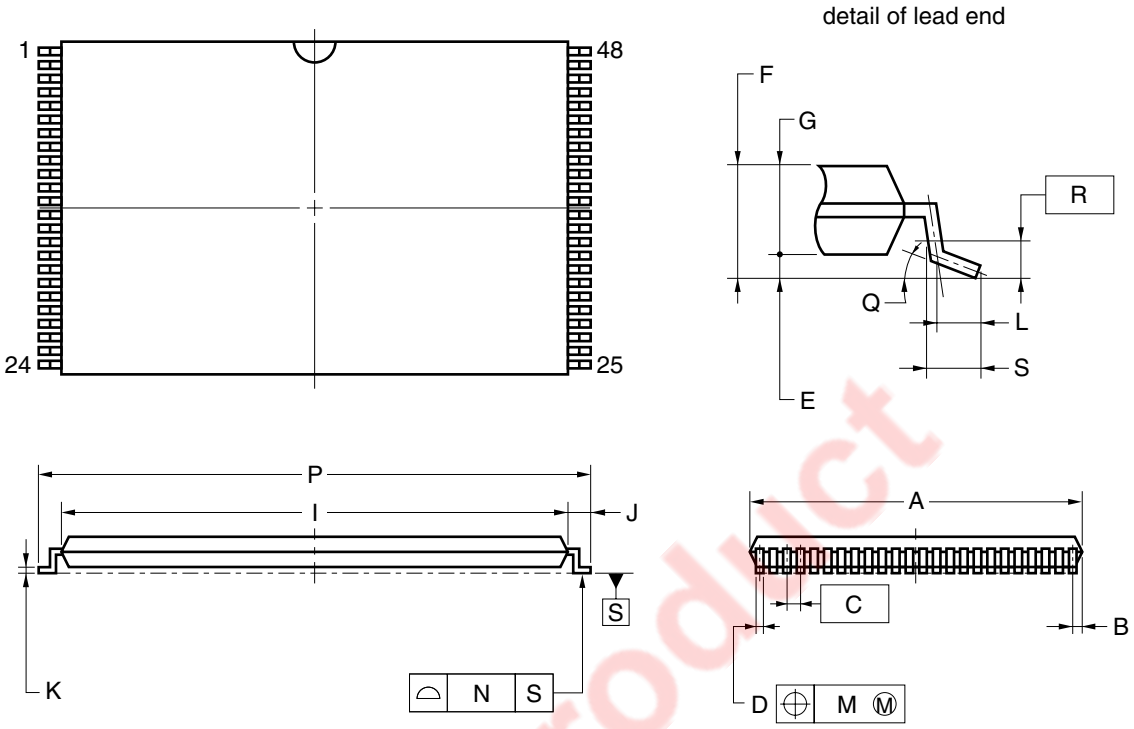
WORD, /BYTE Switch Timing Chart



Remark Chip Enable (/CE) and Output Enable (/OE or OE) : Active.

Package Drawing

★ 48-PIN PLASTIC TSOP (I) (12x20)



NOTES

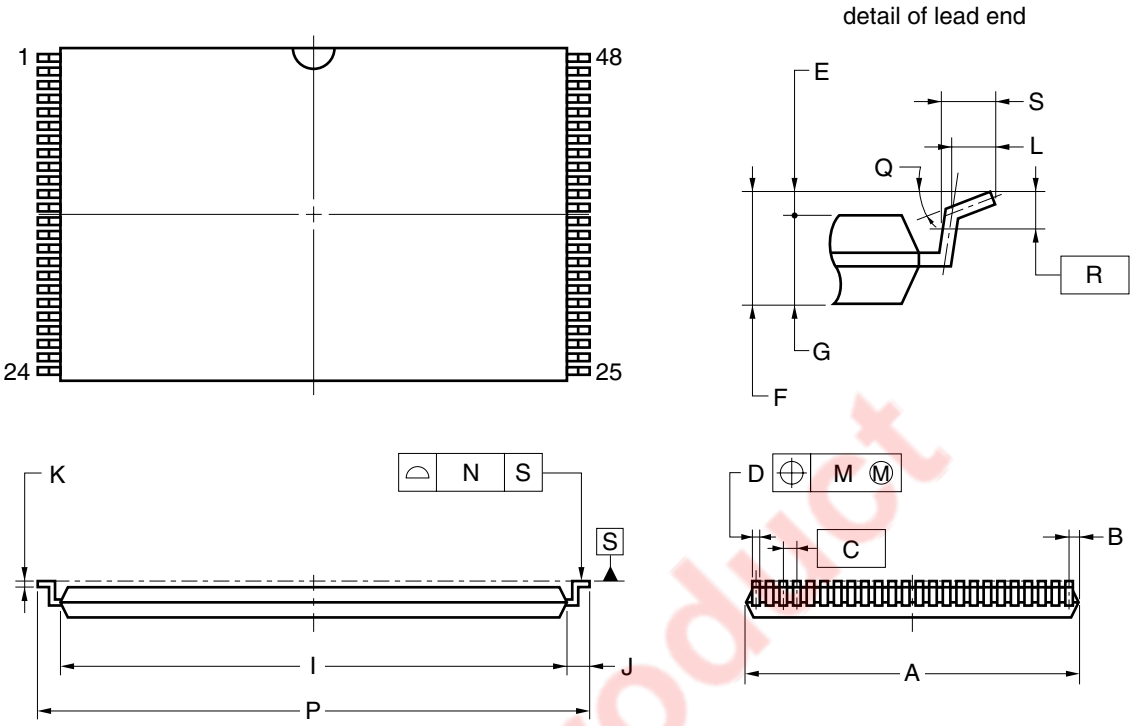
1) Each lead centerline is located within 0.10 mm of its true position (T.P.) at maximum material condition.

2) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
B	0.45 MAX.
C	0.5 (T.P.)
D	0.22±0.05
E	0.1±0.05
F	1.2 MAX.
G	1.0±0.05
I	18.4±0.1
J	0.8±0.2
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GZ-50-MJH-1

★ 48-PIN PLASTIC TSOP (I) (12x20)



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2) "A" excludes mold flash. (Includes mold flash : 12.4 mm MAX.)

ITEM	MILLIMETERS
A	12.0±0.1
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D	0.22±0.05
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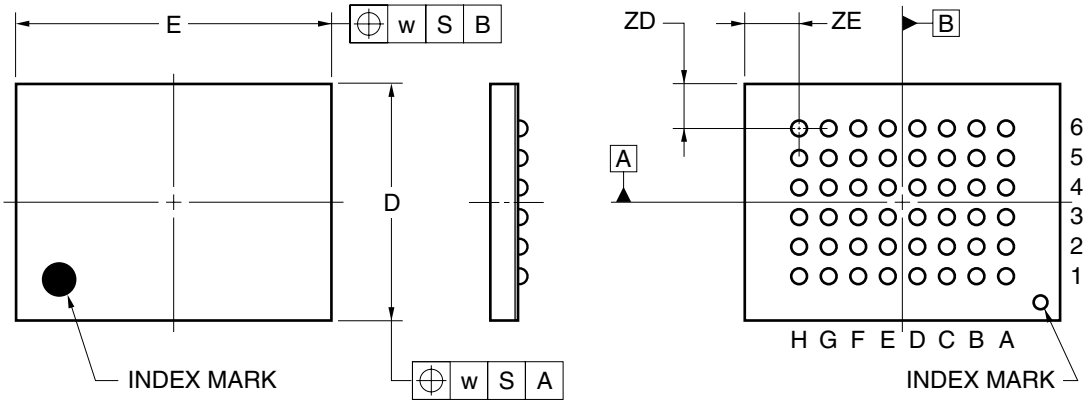
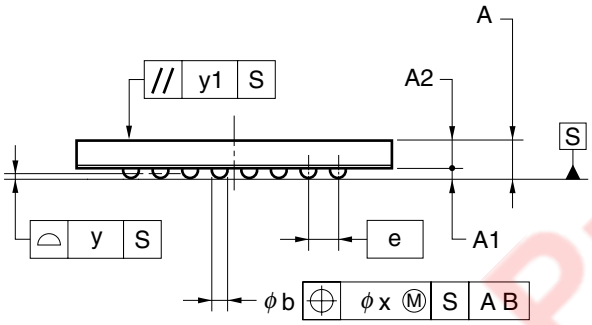
K	0.145±0.05
L	0.5
M	0.10
N	0.10
P	20.0±0.2
Q	$3^{\circ}{}^{+5^{\circ}}_{-3^{\circ}}$
R	0.25
S	0.60±0.15

S48GZ-50-MKH-1

48-PIN TAPE FBGA(8x6)





ITEM	MILLIMETERS
D	6.0±0.1
E	8.0±0.1
w	0.2
e	0.80
A	0.97±0.10
A1	0.27±0.05
A2	0.70
b	0.45±0.05
x	0.08
y	0.1
y1	0.2
ZD	1.00
ZE	1.20

P48F9-80-BC3

Recommended Soldering Conditions

Please consult with our sales offices for soldering conditions of the μPD23C64340 and μPD23C64380.

Types of Surface Mount Device

★ μPD23C64340GZ-MJH : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

★ μPD23C64340GZ-MKH : 48-pin PLASTIC TSOP(I) (12 x 20) (Reverse bent)

μPD23C64340F9-BC3 : 48-pin TAPE FBGA (8 x 6)

★ μPD23C64340GZ-MJH-A : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

★ μPD23C64340GZ-MKH-A : 48-pin PLASTIC TSOP(I) (12 x 20) (Reverse bent)

★ μPD23C64340F9-BC3-A : 48-pin TAPE FBGA (8 x 6)

★ μPD23C64380GZ-MJH : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

★ μPD23C64380GZ-MKH : 48-pin PLASTIC TSOP(I) (12 x 20) (Reverse bent)

μPD23C64380F9-BC3 : 48-pin TAPE FBGA (8 x 6)

★ μPD23C64380GZ-MJH-A : 48-pin PLASTIC TSOP(I) (12 x 20) (Normal bent)

★ μPD23C64380GZ-MKH-A : 48-pin PLASTIC TSOP(I) (12 x 20) (Reverse bent)

★ μPD23C64380F9-BC3-A : 48-pin TAPE FBGA (8 x 6)

Revision History

Edition/ Date	Page		Type of revision	Location	Description (Previous edition → This edition)
	This edition	Previous edition			
4th edition/ Nov. 2005	Throughout	Throughout	Addition	-	48-pin PLASTIC TSOP (I) (12 x 20)
	p.1	p.1	Modification	Access time/ Page access time	Vcc = 3.0 V ± 0.3 V: 100/25 → 120/30 ns (MAX.) Vcc = 3.3 V ± 0.3 V: 90/25 → 100/25 ns (MAX.)
	p.2	p.2	Addition	Ordering Information	Lead-free products have been added
	p.2	p.2	Modification	Marking Image	Marking Image has been modified
	pp.3-5	p.3	Addition	Pin Configuration	Lead-free products have been added
	p.18	p.14	Addition	Recommended Soldering Conditions	Lead-free products have been added

[MEMO]

[MEMO]

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NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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