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RENESAS

MOS INTEGRATED CIRCUIT

μPD78CP18

Phase-out/Discontinued

8-BIT SINGLE-CHIP MICROCOMPUTER

DESCRIPTION

The μPD78CP18 is a version of the μPD78C18 in which the internal mask ROM is replaced by one-time PROM or EPROM.

The one-time PROM version can be programmed once only by users, and is ideally suited for small-scale of many different products, and rapid development and time-to-market of a new product. The EPROM version can be programmed and reprogrammed, and is ideally suited for system evaluation.

The detailed functions are described in the following user's manual. Read this manual before starting design work.

87AD series μPD78C18 user's manual: IEU-1314

FEATURES

- Compatible with μPD78C11A, 78C12A, 78C14, 78C18
- Internal PROM: 32768 W × 8
  - Internal PROM capacity can be changed by software to conform to the μPD78C11A, 78C12A, 78C14, 78C18.
- PROM programming characteristics: μPD27C256A compatible
- Power supply voltage range: 5 V ± 10 %
- Supports QTOP™ microcomputer

Remark QTOP microcomputer is the generic name of NEC's single-chip microcomputers for which NEC provides total service including writing, marking, screening, and inspection.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78CP18CW	64-pin plastic shrink DIP (750 mil)	One-time PROM
μPD78CP18GF-3BE	64-pin plastic QFP (14 × 20 mm)	One-time PROM
μPD78CP18GQ-36	64-pin plastic QUIP	One-time PROM
μPD78CP18DW	64-pin ceramic shrink DIP with window (750 mil)	EPROM
μPD78CP18KB	64-pin ceramic WQFN	EPROM

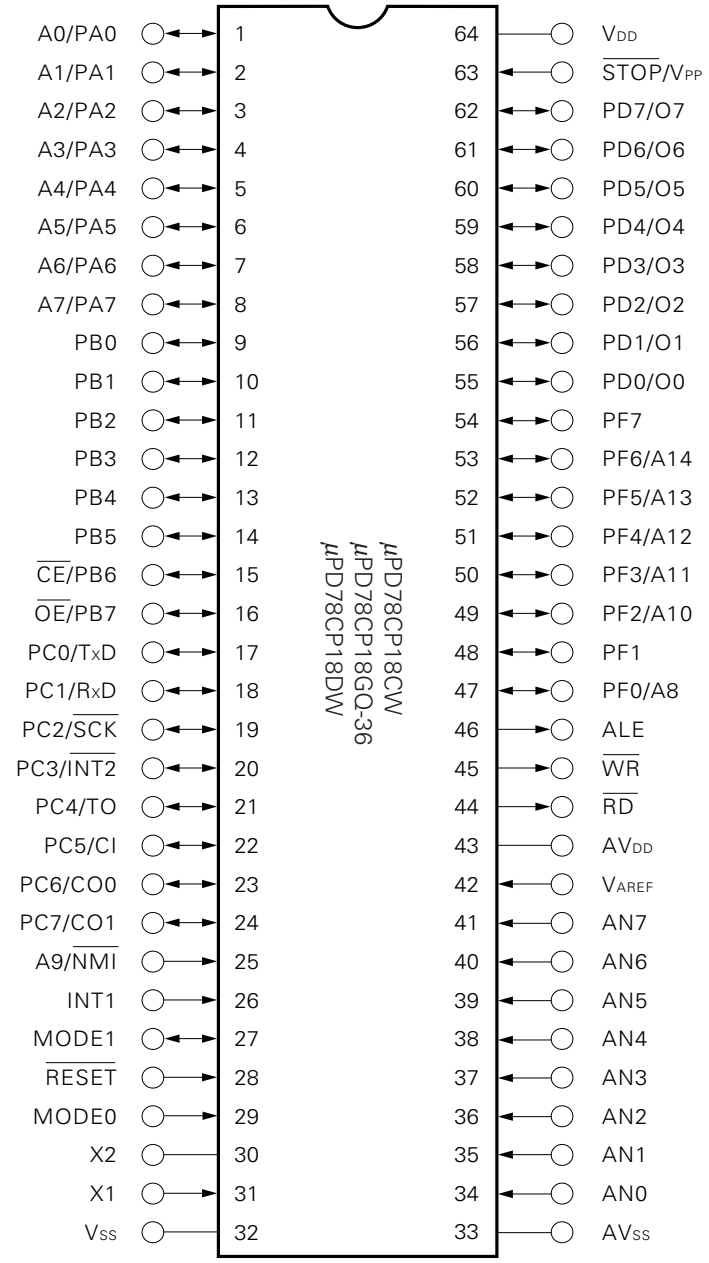
In this document, the functions common to the one-time PROM and EPROM versions are described as belonging to "PROM".

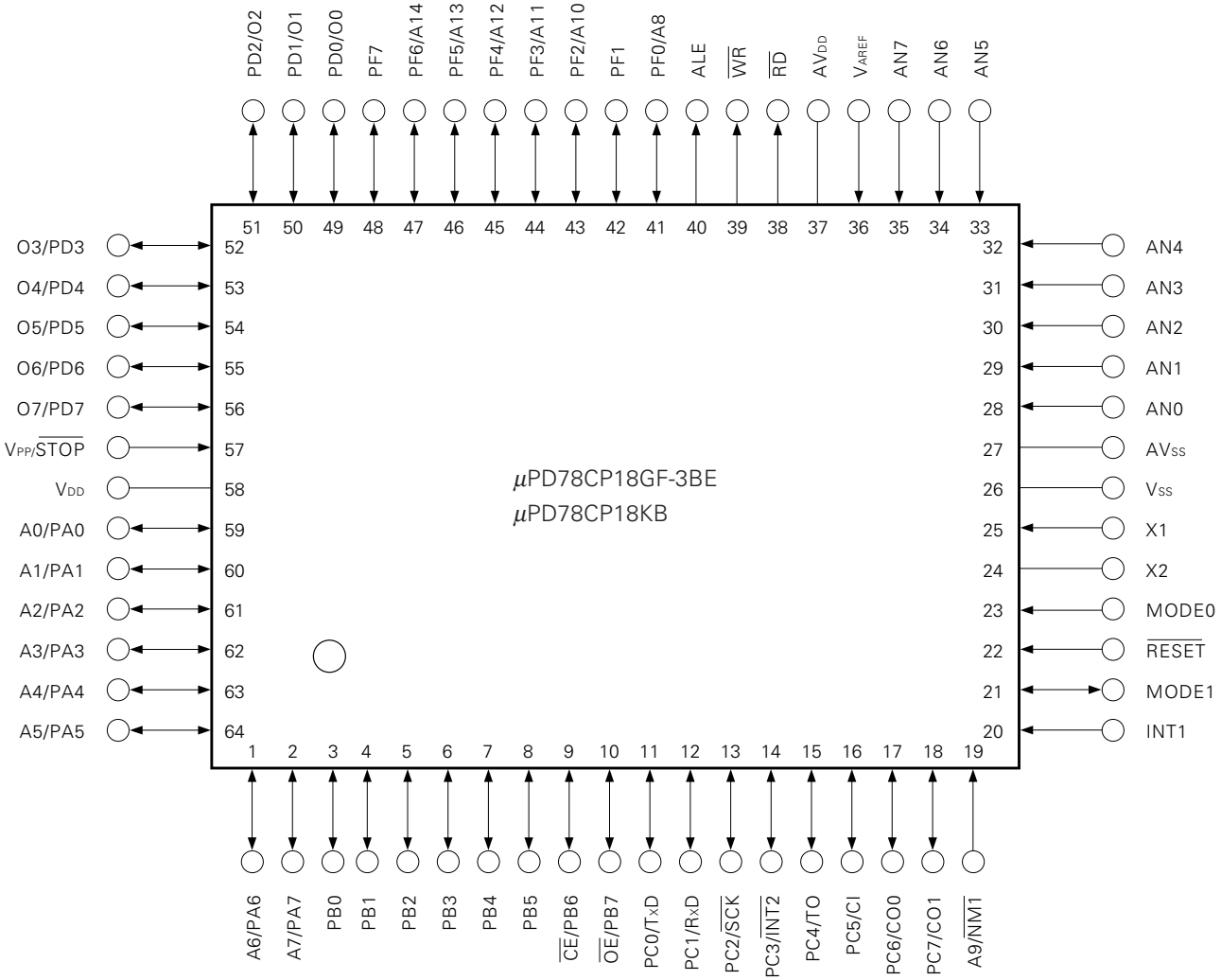
The information in this document is subject to change without notice.

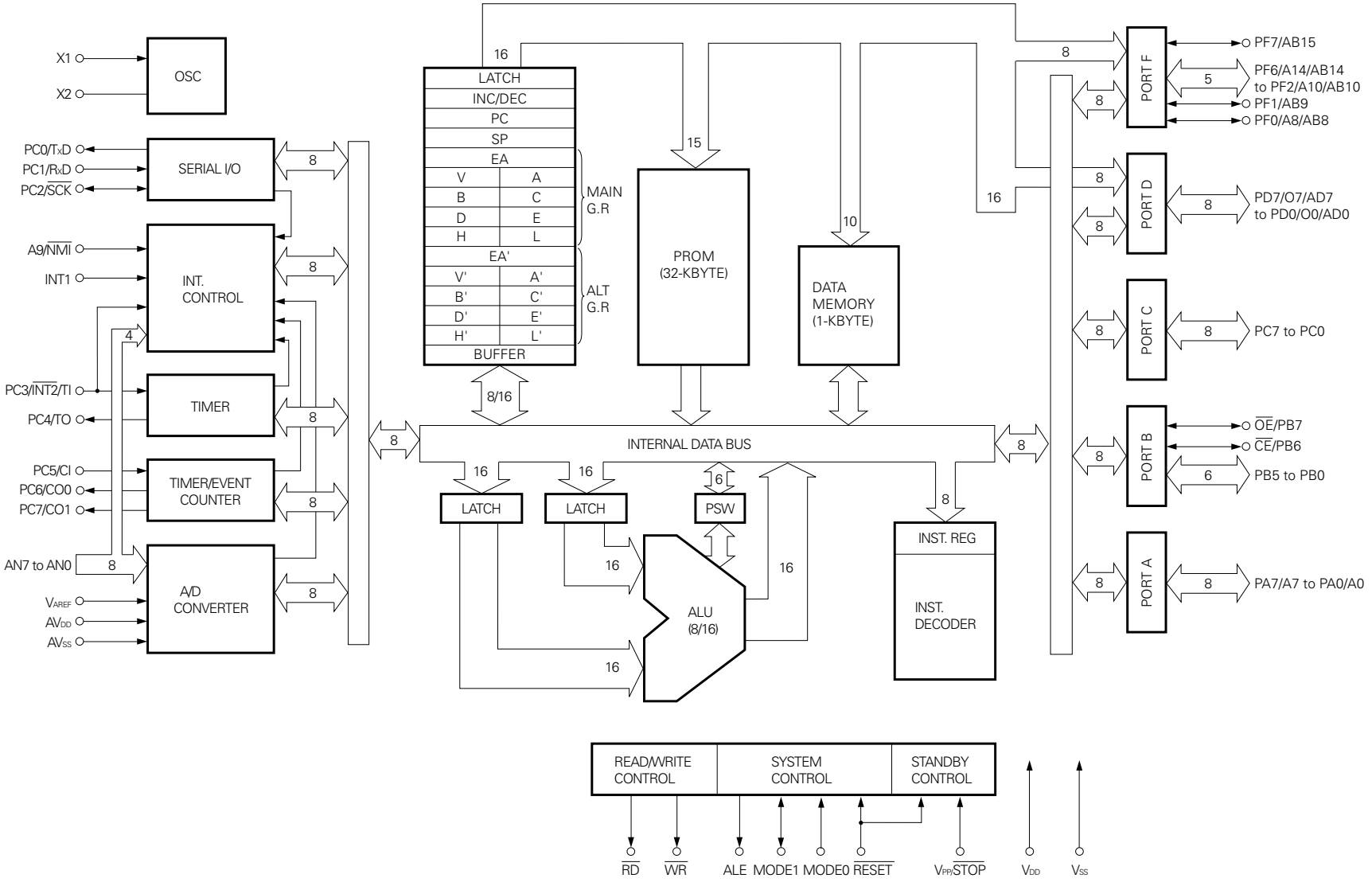
The mark ★ shows revised points.

Document No. IC-3033A
(O. D. No. IC-8054A)
Date Published March 1995 P
Printed in Japan

PIN CONFIGURATION (TOP VIEW)




PD2/O2
PD1/O1
PD0/O0
PF7
PF6/A14
PF5/A13
PF4/A12
PF3/A11
PF2/A10
PF1
PF0/A8
ALE
WR
RD
AVDD
VAREF
AN7
AN6
AN5
51 50 49 48 47 46 45 44 43 42 41 40 39 38 37 36 35 34 33
O3/PD3 52
O4/PD4 53
O5/PD5 54
O6/PD6 55
O7/PD7 56
VPP/STOP 57
VDD 58
A0/PA0 59
A1/PA1 60
A2/PA2 61
A3/PA3 62
A4/PA4 63
A5/PA5 64
32 AN4
31 AN3
30 AN2
29 AN1
28 AN0
27 AVSS
26 VSS
25 X1
24 X2
23 MODE0
22 RESET
21 MODE1
20 INT1
μPD78CP18GF-3BE
μPD78CP18KB
1 2 3 4 5 6 7 8 9 10 11 12 13 14 15 16 17 18 19
A6/PA6
A7/PA7
PB0
PB1
PB2
PB3
PB4
PB5
CE/PB6
OE/PB7
PC0/TxD
PC1/RxD
PC2/SCK
PC3/INT2
PC4/TO
PC5/CI
PC6/CO0
PC7/CO1
A9/NM1



Phase-out/Discontinued

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1. LIST OF PORT FUNCTIONS

1.1 PORT FUNCTIONS

Pin Name	I/O	Function
PA7 to PA0 (Port A)	Input/Output	8-bit input-output port, which can specify input/output bit-wise.
PB7 to PB0 (Port B)		
PC7 to PC0 (Port C)		
PD7 to PD0 (Port D)		8-bit input-output port, which can specify input/output in byte units.
PF7 to PF0 (Port F)		8-bit input-output port, which can specify input/output bit-wise.

Remark These port pins are dual-function pins as shown in **1.2 "NON-PORT FUNCTIONS (IN NORMAL OPERATION)"** and **1.3 "NON-PORT FUNCTIONS (DURING PROM WRITE/VERIFY/READ)"**.

1.2 NON-PORT FUNCTIONS (IN NORMAL OPERATION)

Pin Name	I/O	Alternate Function Pin	Function
TxD (Transmit Data)	Output	PC0	Serial data output pin
RxD (Receive Data)	Input	PC1	Serial data input pin
$\overline{SCK}$ (Serial Clock)	Input/output	PC2	Serial clock input/output pin. Output when internal clock is used, input when external clock is used.
$\overline{INT2}$ (Interrupt Request)	Input	PC3	Edge trigger (falling edge) maskable interrupt input pin
TI (Timer Input)	Input		Timer external clock input pin
Zero-cross	Input		AC input zero-cross detection pin
TO (Timer Output)	Output	PC4	During timer count time, square wave with one internal clock cycle as one half cycle is output.
CI (Counter Input)	Input	PC5	Timer/event counter external pulse input pin
CO0 and CO1 (Counter Output 0, 1)	Output	PC6 and PC7	Square wave output programmable by timer/event counter.
AD7 to AD0 (Address/Data Bus 7 to 0)	Input/output	PD7 to PD0	Multiplexed address/data bus when external memory is used
AB15 to AB8 (Address Bus 15 to 8)	Output	PF7 to PF0	Address bus when external memory is used
$\overline{WR}$ (Write Strobe)	Output		Strobe signal which is output for write operation of external memory. It becomes high in any cycle other than the data write machine cycle of external memory. When $\overline{RESET}$ signal is either low or in the hardware STOP mode, this signal becomes high-impedance.
$\overline{RD}$ (Read Strobe)	Output		Strobe signal which is output for read operation of external memory. It becomes high in any cycle other than the read machine cycle of external memory. When $\overline{RESET}$ signal is either low or in the hardware STOP mode, this signal becomes high-impedance.
ALE (Address Latch Enable)	Output		Strobe signal to latch externally the lower address information which is output to PD7 to PD0 pins to access external memory. When $\overline{RESET}$ signal is either low or in the hardware STOP mode, this signal becomes high-impedance.
MODE0 MODE1 (Mode)	Input Input/output		Set MODE0 pin to "0" (low level), and MODE1 pin to "1" (high level)[Note]
$\overline{NMI}$ (Non-Maskable Interrupt)	Input		Non-maskable interrupt input pin of the edge trigger (falling edge)

Note Pull-up. Pull-up resistor R is 4 [kΩ] ≤ R ≤ 0.4 t_{CYC} [kΩ] (t_{CYC} is ns unit).

Pin Name	I/O	Alternate Function Pin	Function
INT1 (Interrupt Request)	Input		A maskable interrupt input pin of the edge trigger (rising edge). Also, it can be used as a zero-cross detection pin for AC input.
AN7 to AN0 (Analog Input)	Input		8 pins of analog input to A/D converter. AN7 to AN4 can be used as edge detection (falling edge) input.
V_{AREF} (Reference Voltage)	Input		A common pin serving both as a reference voltage input pin for A/D converter and as a control pin for A/D converter operation.
AV_{DD} (Analog V_{DD})			Power supply pin for A/D converter.
AV_{SS} (Analog V_{SS})			GND pin for A/D converter.
X1, X2 (Crystal)			Crystal connection pins for system clock oscillation. X1 should be input when a clock is supplied from outside. Inverted clock of X1 should be input in X2.
$\overline{RESET}$ (Reset)	Input		Low-level active system reset input.
$\overline{STOP}$ (Stop)	Input		Hardware STOP mode control signal input pin. When the low-level is input to this pin, the oscillation stops.
V_{DD}			Positive power supply pin.
V_{SS}			GND pin.

1.3 NON-PORT FUNCTIONS (DURING PROM WRITE/VERIFY/READ)

Pin Name	I/O	Alternate Function Pin	Function
A7 to A0	Input	PA7 to PA0	Address lower 8 bit input pins
$\overline{CE}$	Input	PB6	Chip enable signal input pin
$\overline{OE}$	Input	PB7	Output enable signal input pin
O7 to O0	Input/output	PD7 to PD0	Data input/output pins
A14 to A10	Input	PF6 to PF2	Address higher 7 bit input pins
A8		PF0	
A9	Input	$\overline{NMI}$	
MODE0 MODE1	Input		Set MODE0 pin to “1” (high level), and MODE1 pin to “0” (low level).
$\overline{RESET}$	Input		Set to “0” (low level).
V_{PP}		$\overline{STOP}$	High-voltage application pin "1" (high level) is input when EPROM is read.

1.4 HANDLING OF UNUSED PINS

Pin	Recommended Connection
PA7 to PA0 PB7 to PB0 PC7 to PC0 PD7 to PD0 PF7 to PF0	Connect to V_{SS} or V_{DD} via resistor.
$\overline{RD}$ $\overline{WR}$ ALE	Leave open.
$\overline{STOP}$	Connect to V_{DD}.
INT1, $\overline{NMI}$	Connect to V_{SS} or V_{DD}.
AV_{DD}	Connect to V_{DD}.
V_{AREF} AV_{SS}	Connect to V_{SS}.
AN7 to AN0	Connect to AV_{SS} or AV_{DD}.

2. MEMORY CONFIGURATION

The μPD78CP18 memory can operate in the following 4 modes according to the mode specification.

- ○ μPD78C11A mode (see **Figure 2-1**)
- ○ μPD78C12A mode (see **Figure 2-2**)
- ○ μPD78C14 mode (see **Figure 2-3**)
- ○ μPD78C18 mode (see **Figure 2-4**)

In addition, the internal PROM and internal RAM address areas can be specified for efficient mapping of external memory (excluding PROM) (see **3.2 "MEMORY MAPPING REGISTER (MM)"**).

The vector area and call table area are common to all modes.

Setting the hardware/software STOP mode or HALT mode enables internal RAM data to be retained at a low consumption current.

Figure 2-1. Memory Map (μPD78C11A Mode)

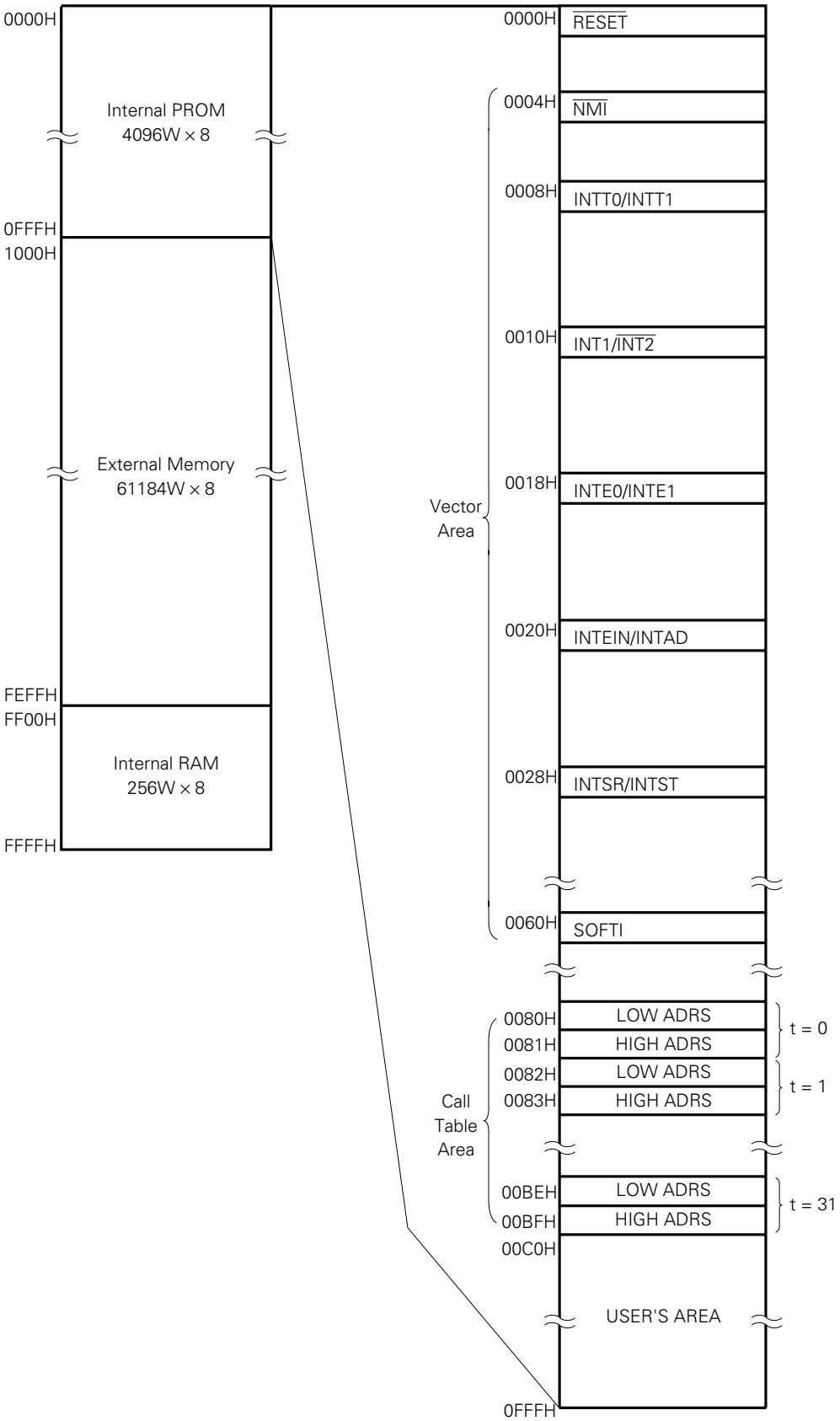


Figure 2-2. Memory Map (μPD78C12A Mode)

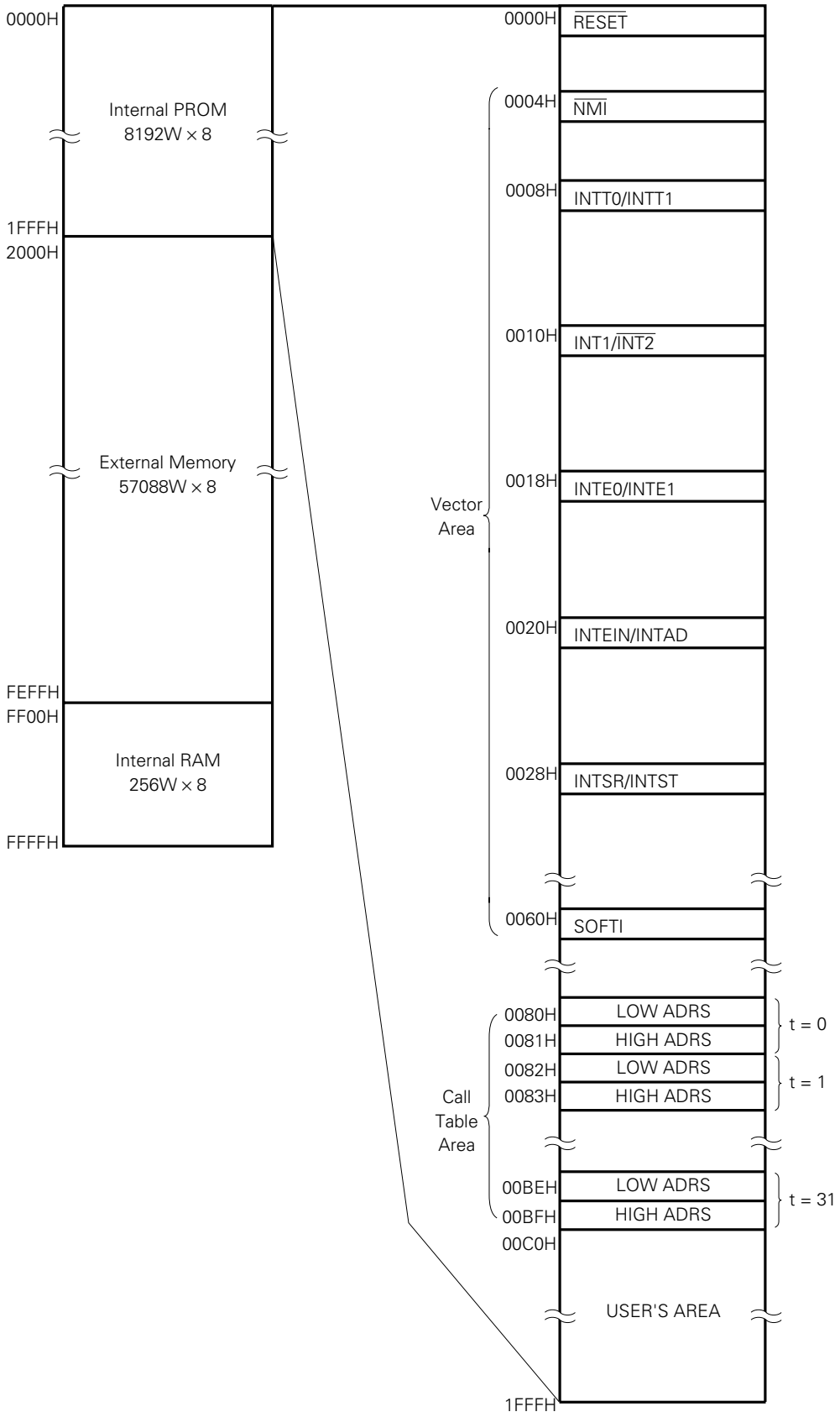


Figure 2-3. Memory Map (μPD78C14 Mode)

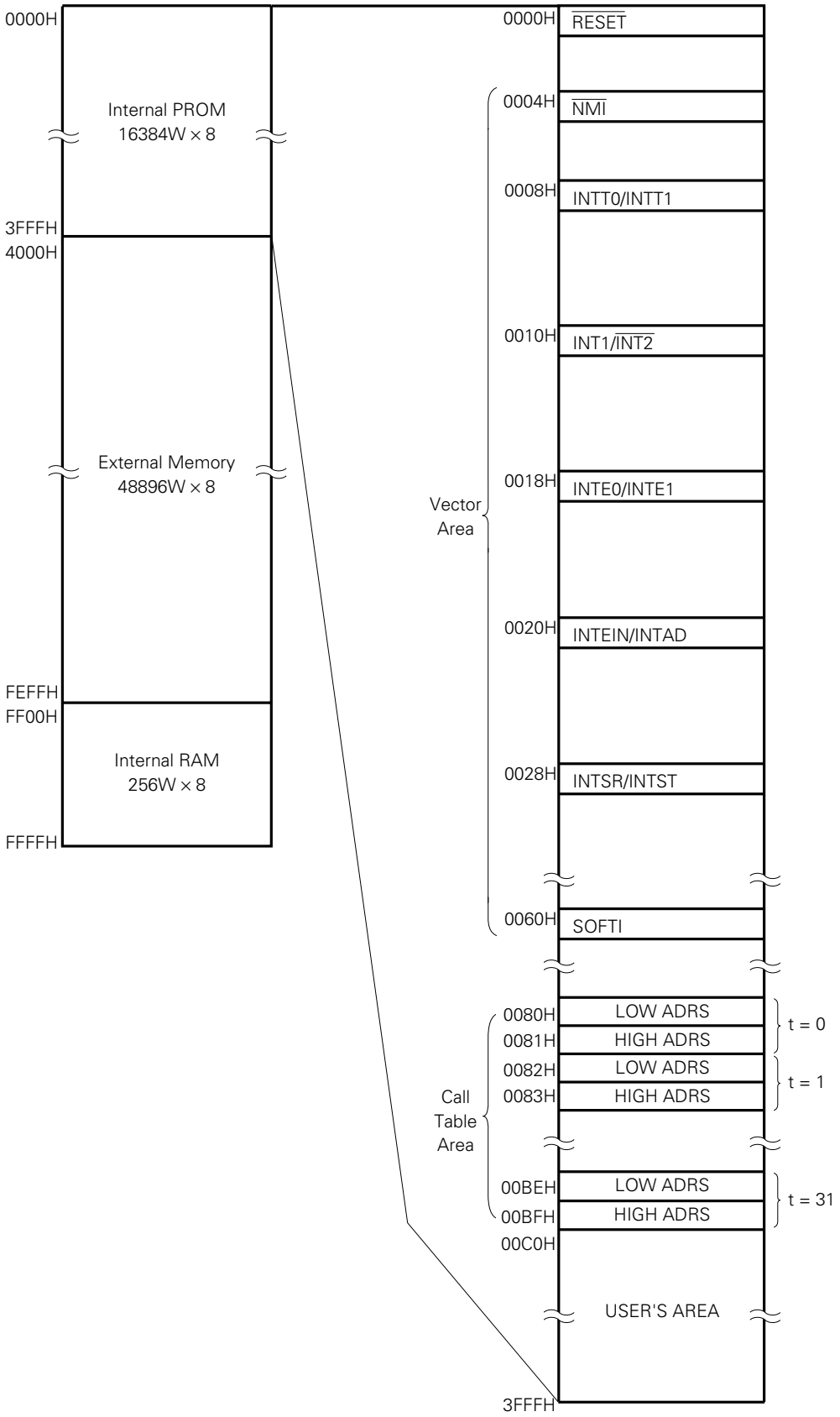
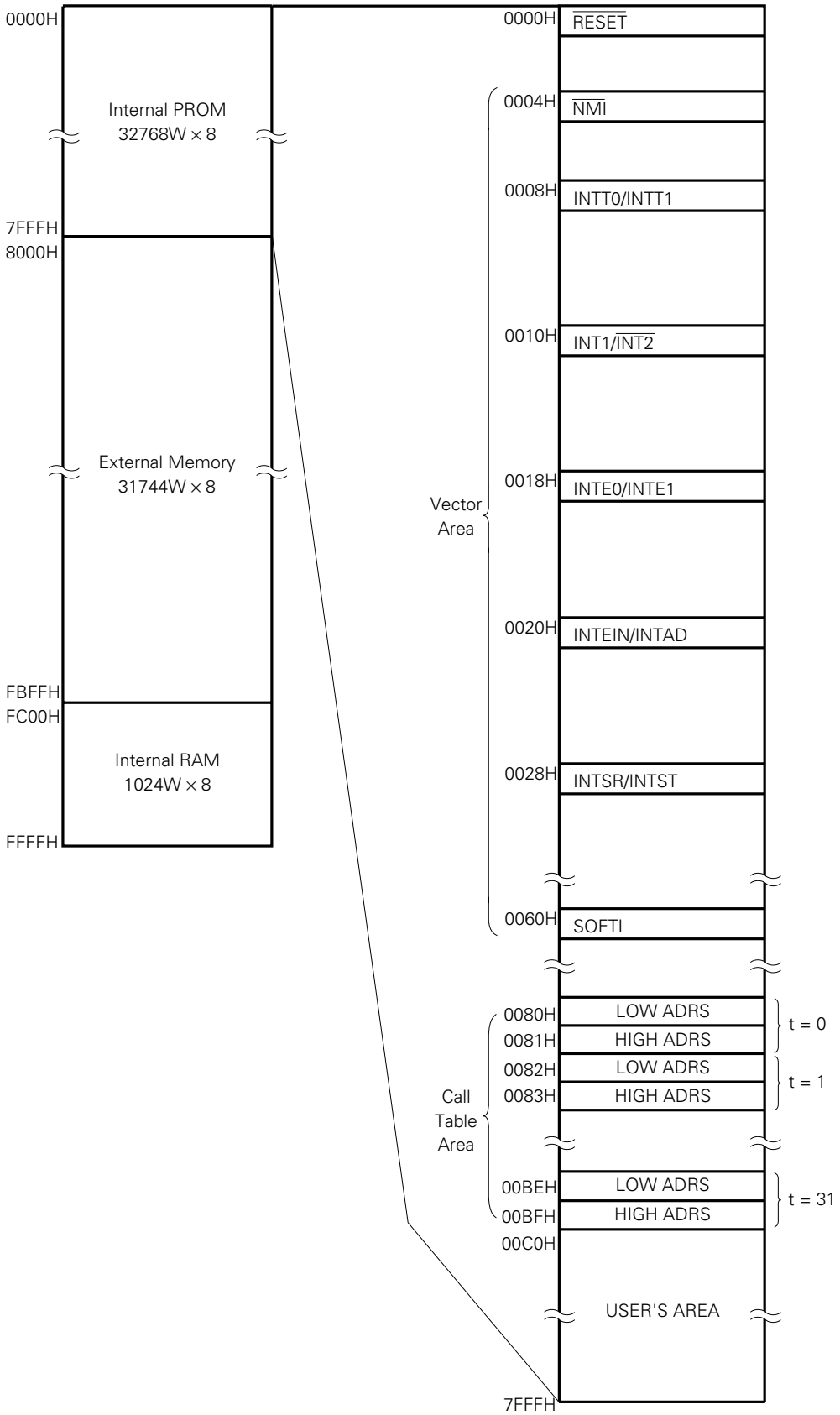


Figure 2-4. Memory Map (μPD78C18 Mode)



3. MEMORY EXTENSION

The μPD78CP18 allows external memory extension by means of the MEMORY MAPPING register (MM) or the MODE0 and MODE1 pins. Also, the internal PROM and internal RAM access areas can be specified by means of bits MM7, MM6 and MM5 of the MEMORY MAPPING register.

3.1 MODE PINS

The μPD78CP18 can be switched between programming mode and normal operation mode according to the specification of the MODE0 and MODE1 pins.

Table 3-1 shows the modes set by the MODE pins.

Table 3-1. Modes Set By MODE Pins

MODE1	MODE2	Operating Mode
L	L	Setting prohibited
L	H	Programming mode[Note]
H	L	Normal operation mode
H	H	Setting prohibited

Note See **4. "PROM PROGRAMMING"**.

When MODE0 and MODE1 are driven high, a 4 [kΩ] ≤ R ≤ 0.4 t_{CYC} [kΩ] pull-up resistor should be used (t_{CYC}: ns units).

3.2 MEMORY MAPPING REGISTER (MM)

The MEMORY MAPPING register is an 8-bit register which performs the following controls:

- Port/extension mode specification for PD7 to PD0 and PF7 to PF0
- Enabling/disabling of internal RAM accesses
- Specification of internal PROM and RAM access areas

The configuration of the MEMORY MAPPING register is shown in Figure 3-1.

(1) Bits MM2 to MM0

These bits control the PD7 to PD0 port/extension mode specification, input/output specification, and the PF7 to PF0 address output specification.

As shown in Figure 3-1, there is a choice of four capacities for the connectable external memory:

- 256 bytes
- 4 Kbytes
- 16 Kbytes
- 32 K/48 K/56 K/60 Kbytes (set by bits MM7 to MM5)

Ports of PF7 to PF0 not used as address outputs can be used as general-purpose ports.

When $\overline{\text{RESET}}$ signal is input or in the hardware STOP mode, these bits are reset to (0) and PD7 to PD0 are set to input port mode (high-impedance).

(2) MM3 bit (RAE)

This bit enables (RAE = 1) and disables (RAE = 0) of internal RAM access. This bit should be set to "0" during standby operation and when externally connected RAM, not internal RAM, is used.

In normal operation this bit retains its value when $\overline{\text{RESET}}$ signal is input. However, the RAE bit is undefined after a power-on reset, and must therefore be initialized by an instruction.

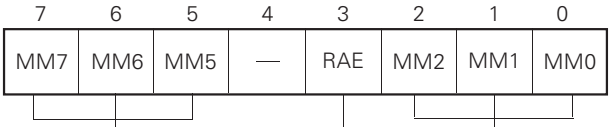
(3) Bits MM7 to MM5

These bits specify the access area of the internal PROM.

When $\overline{\text{STOP}}$ or $\overline{\text{RESET}}$ signal is input, these bits are reset, selecting the 32-Kbyte mode (μPD78C18 mode).

These bits are only valid in the μPD78CG14, 78CP14, and 78CP18; if data is written to these bits in the μPD78C11A, 78C12A, 78C14, or 78C18, it will be ignored. Therefore, a program developed on the μPD78CP18 can be directly ported to mask ROM.

Figure 3-1. MEMORY MAPPING Register Format



0 0 0	Port mode	Single-chip	PD7 to PD0 = Input port PF7 to PF0 = Port mode		
0 0 1			PD7 to PD0 = Output port PF7 to PF0 = Port mode		
0 1 0	Extension mode	256 bytes	PD7 to PD0 = Extension mode PF7 to PF0 = Port mode		
1 0 0		4 Kbytes	PD7 to PD0 = } Extension PF3 to PF0 = } mode PF7 to PF4 = Port mode		
1 1 0		16 Kbytes	PD7 to PD0 = } Extension PF5 to PF0 = } mode PF7 & PF6 = Port mode		
1 1 1		32 K/48 K/ 56 K/60K[Note] bytes	PD7 to PD0 = } Extension PF7 to PF0 = } mode		

Note Depends on MM7 to MM5 bit-setting

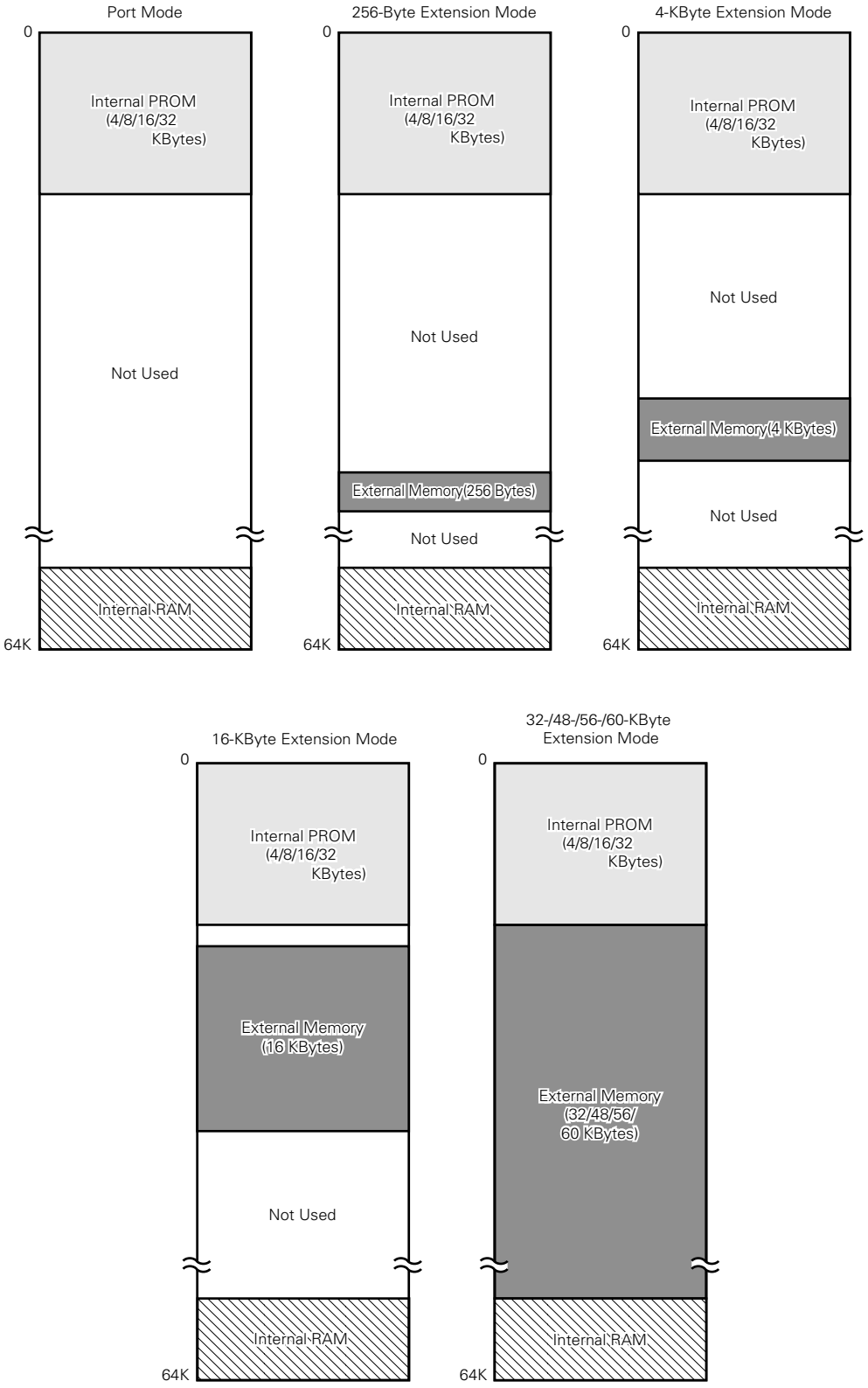
Internal RAM Access

0	Disable
1	Enable

Internal PROM/RAM Access Areas

MM7	MM6	MM5	Internal PROM Access Area	Internal RAM Access Area
0	0	0	0000H to 7FFFH (32 Kbytes: μPD78C18 mode)	FC00H to FFFFH (1 Kbyte)
0	0	1	0000H to 3FFFH (16 Kbytes: μPD78C14 mode)	FF00H to FFFFH (256 bytes)
0	1	1	0000H to 1FFFH (8 Kbytes: μPD78C12A mode)	FF00H to FFFFH (256 bytes)
1	0	1	0000H to 0FFFH (4 Kbytes: μPD78C11A mode)	FF00H to FFFFH (256 bytes)
Other than above			Setting Prohibited	

Figure 3-2. External Extension Modes Set by MEMORY MAPPING Register



Caution The internal PROM and internal RAM access areas are determined by MM7 to MM5.

4. PROM PROGRAMMING

The μPD78CP18 incorporates 32768 × 8-bit PROM as a program memory. The pins shown in Table 4-1 are used for write/verify operations on this PROM.

μPD78CP18 program timing is compatible with the μPD27C256A.

Please read the following in conjunction with documentation of the μPD27C256A.

Table 4-1. Pins Used in PROM Programming

Pin Name	Function
$\overline{RESET}$	Low-level input (at write/verify and read)
MODE0	High-level input (at write/verify and read)
MODE1	Low-level input (at write/verify and read)
V_{PP}Note	High-voltage input (at write/verify), high-level input (at read)
$\overline{CE}$Note	Chip enable input
$\overline{OE}$Note	Output enable input
A14 to A0Note	Address input
O7 to O0Note	Data input (at write), data output (at verify/read)
V_{DD}Note	Supply voltage input

Note These pins correspond to the μPD27C256A.

Cautions 1. Cover the erasure window of the μPD78CP18DW and 78CP18KB with an opaque film except while erasing the data in EPROM.

2. The μPD78CP18CW, 78CP18GF-3BE, and 78CP18GQ-36 one-time PROM version is not equipped with an erasure window, and therefore ultraviolet erasure can not be performed.

4.1 PROM PROGRAMMING OPERATING MODES

The PROM programming operating mode is set as shown in Table 4-2. Pins not used for programming should be handled as shown in Table 4-3.

Table 4-2. PROM Programming Modes

Operating Mode	$\overline{CE}$ Note	$\overline{OE}$ Note	V_{PP} Note	V_{DD} Note	$\overline{RESET}$	MODE0	MODE1
Program	L	H	+12.5 V	+6 V	L	H	L
Program verify	H	L					
Program inhibit	H	H					
Read	L	L	+5 V	+5 V			
Output disable	L	H					
Standby	H	L/H					

Note These pins correspond to the μPD27C256A.

Caution When +12.5 V is applied to V_{PP} and +6 V is applied to V_{DD}, setting both $\overline{CE}$ and $\overline{OE}$ to "L" is prohibited.

Table 4-3. Recommended Connection of Unused Pins (in PROM Programming Mode)

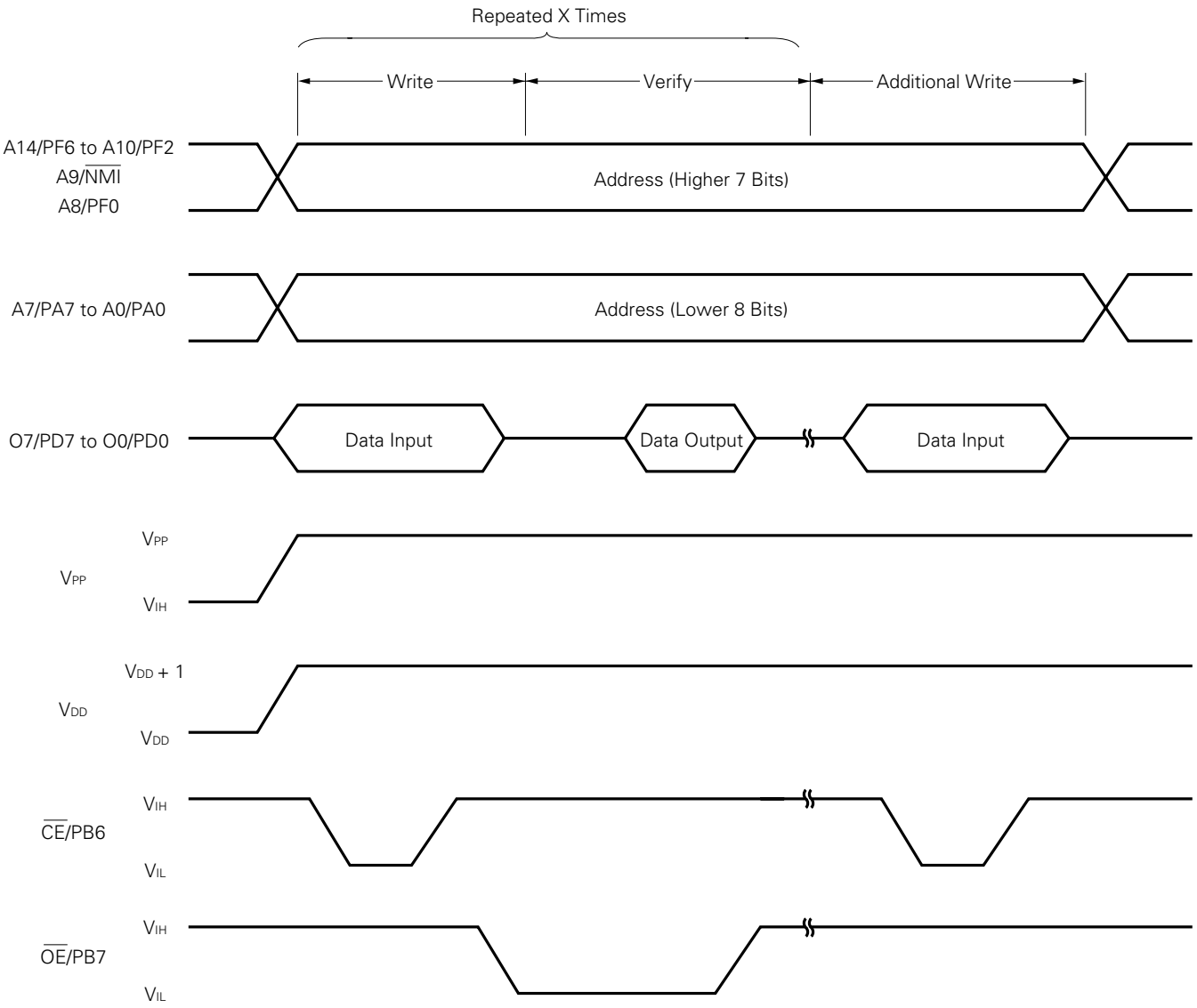
Pin	Recommended Connection
INT1	Connect to V_{SS}.
X1	
AN0 to AN7	
V_{AREF}	
AV_{DD}	
AV_{SS}	
Pins other than the above	Connect to V_{SS} via individual resistor.
X2	Leave open.

4.2 PROM WRITING PROCEDURE

The PROM writing procedure is as shown below, allowing high-speed writing.

(1) Connect unused pins to V_{SS} via a pull-down resistor, and supply +6 V to V_{DD} and +12.5 V to V_{PP}.
(2) Provide the initial address.
(3) Provide the write data.
(4) Provide a 1-ms program pulse (active low) to the $\overline{CE}$ pin.
(5) Verify mode. If written, go to (7); if not written, repeat (3) to (5). If the write operation has failed 25 times, go to (6).
(6) Halt write operation due to defective device.
(7) Provide write data and supply a program pulse that is X times 3 ms where X is the number of repetitions between numbers (3) and (5). above (additional write).
(8) Increment the address.
(9) Repeat (3) to (8) until the final address.

Figure 4-1. PROM Write/Verify Timing



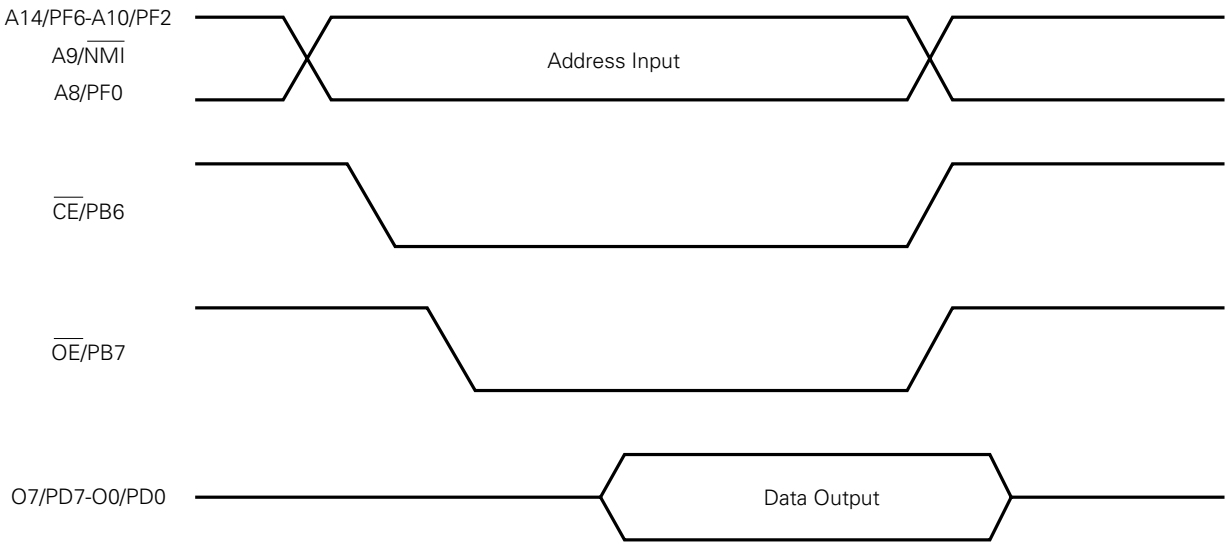
4.3 PROM READING PROCEDURE

PROM contents can be read onto the external data bus (O7 to O0) using the following procedure.

(1) Connect unused pins to V_{SS} via a pull-down resistor.
(2) Supply +5 V to the V_{DD} and V_{PP} pins.
(3) Input address of data to be read to pins A14 to A0.
(4) Read mode
(5) Output data to pins O7 to O0.

Timing for steps (2) to (5) above is shown in Figure 4-2.

Figure 4-2. PROM Read Timing



5. PROGRAM ERASURE (ONLY THE CERAMIC PACKAGE PRODUCT WITH WINDOW)

The data contents programmed in the ceramic package product (μPD78CP18DW, 78CP18KB) can be erased by exposing the window to an ultraviolet light source whose wavelength is about 250 nm. The minimum radiation exposure required to erase the written deta completely is 150 W•s/fcm^2 (ultraviolet ray strength times erase time). This corresponds to about 15 to 20 minutes with an UV lamp whose wavelength is 254 nm and ultraviolet ray strength is 12 mW/cm^2.

Cautions 1. The programmed data contents may also be erased if the uncovered window is exposed to direct sunlight or a fluorescent light for several hours. Thus, to protect the data contents, cover the window with an opaque film. NEC attaches quality-tested shading film to the UVE PROM products for shipping.

2. The distance between the light source and the products (μPD78CP18DW, 78CP18KB) should be 2.5 cm or less.

Remark The erasure time may be prolonged if the UV lamp is old or if the device window is dirty.

6. SCREENING OF ONE-TIME PROM VERSIONS

Because of their construction, one-time PROM products (μPD78CP18CW, 78CP18GF-3BE, and 78CP18GQ-36) cannot be fully tested by NEC before shipment. After the necessary data has been written, it is recommended that screening be implemented in which PROM verification is performed after high-temperature storage under the following conditions.

Storage Temperature	Storage Time
125 °C	24 hours

NEC provides writing, marking, screening, and inspection services for single-chip microcomputers labeled QTOP microcomputers. For details, consult NEC.

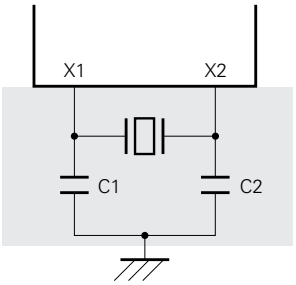
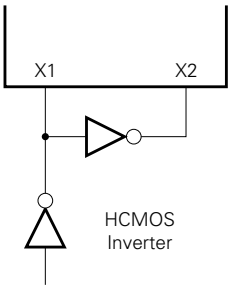
7. ELECTRICAL SPECIFICATIONS

ABSOLUTE MAXIMUM RATINGS (T_A = 25 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	RATINGS	UNIT
Power supply voltage	V_{DD}		–0.5 to +7.0	V
	AV_{DD}		AV_{SS} to V_{DD} + 0.5	V
	AV_{SS}		–0.5 to +0.5	V
	V_{PP}		–0.5 to +13.5	V
Input voltage	V_I	Other than $\overline{NMI}$/A9 pin	–0.5 to V_{DD} + 0.5	V
		$\overline{NMI}$/A9 pin	–0.5 to +13.5	V
Output voltage	V_O		–0.5 to V_{DD} + 0.5	V
Output current low	I_{OL}	All output pins	4.0	mA
		Total of all output pins	100	mA
Output current high	I_{OH}	All output pins	–2.0	mA
		Total of all output pins	–50	mA
A/D converter reference input voltage	V_{AREF}		–0.5 to AV_{DD} + 0.3	V
Ambient operating temperature	T_A		–40 to +85	°C ★
Storage temperature	T_{stg}		–65 to +150	°C

Caution If the absolute maximum rating of even one of the above parameters is exceeded even momentarily, the quality of the product may be degraded. The absolute maximum ratings, therefore, specify the values exceeding which the product may be physically damaged. Be sure to use the product with these rated values never exceeded. ★

OSCILLATOR CHARACTERISTICS **(T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.8 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})**

RESONATOR	RECOMMENDED CIRCUIT	PARAMETER	TEST CONDITIONS	MIN.	MAX.	UNIT
Ceramic or crystal resonator		Oscillator frequency (f_{XX})	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	
External clock		X1 input frequency (f_X)	A/D converter not used	4	15	MHz
			A/D converter used	5.8	15	
		X1 rise time, fall time (t_r, t_f)		0	20	ns
		X1 input high-, low-level width ($t_{\phi H}$, $t_{\phi L}$)		20	250	ns

Cautions 1. Place the oscillator as close as possible to the X1 and X2 pins.

2. Ensure that no other signal lines pass through the shaded area.

CAPACITANCE (T_A = 25 °C, V_{DD} = V_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input capacitance	C_I	f_C = 1 MHz Unmeasured pins returned to 0 V			10	pF
Output capacitance	C_O				20	pF
Input-output capacitance	C_{IO}				20	pF

DC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V)

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	TYP.	MAX.	UNIT
Input voltage low	V_{IL1}	All except $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7		0		0.8	V
	V_{IL2}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7		0		0.2V_{DD}	V
Input voltage high	V_{IH1}	All except $\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7, X1, X2		2.2		V_{DD}	V
	V_{IH2}	$\overline{\text{RESET}}$, $\overline{\text{STOP}}$, $\overline{\text{NMI}}$, $\overline{\text{SCK}}$, INT1, TI, AN4 to AN7, X1, X2		0.8 V_{DD}		V_{DD}	V
Output voltage low	V_{OL}	I_{OL} = 2.0 mA				0.45	V
Output voltage high	V_{OH}	I_{OH} = –1.0 mA		V_{DD} – 1.0			V
		I_{OH} = –100 μA		V_{DD} – 0.5			V
Input current	I_I	INT1[Note1], TI(PC3)[Note2] ; 0 V ≤ V_I ≤ V_{DD}				±200	μA
Input leakage current	I_{LI}	All except INT1, TI (PC3) ; 0 V ≤ V_I ≤ V_{DD}				±10	μA
Output leakage current	I_{LO}	0 V ≤ V_O ≤ V_{DD}				±10	μA
AV_{DD} power supply current	AI_{DD1}	Operating mode f_{XX} = 15 MHz			0.5	1.3	mA
	AI_{DD2}	STOP mode			10	20	μA
V_{DD} power supply current	I_{DD1}	Operating mode f_{XX} = 15 MHz			16	35	mA
	I_{DD2}	HALT mode f_{XX} = 15 MHz			7	13	mA
Data retention voltage	V_{DDDR}	Hardware/software STOP mode		2.5			V
Data retention current	I_{DDDR}	Hardware/software[Note3] STOP mode	V_{DDDR} = 2.5 V		1	15	μA
			V_{DDDR} = 5 V ± 10 %		10	50	μA ★

Notes 1. If self-bias should be generated by ZCM register.

2. If the control mode is set by MCC register, and self-bias should be generated by ZCM register.

3. If self-bias is not generated.

AC CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = AV_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V)
READ/WRITE OPERATION:

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
X1 input cycle time	t_{CYC}		66	167	ns
Address setup time (to ALE↓)	t_{AL}	f_{XX} = 15 MHz, CL = 150 pF	30		ns
Address hold time (from ALE↓)	t_{LA}		35		ns
$\overline{RD}$↓ delay time from address	t_{AR}		100		ns
Address float time from $\overline{RD}$↓	t_{AFR}	C_L = 150 pF		20	ns
Data input time from address	t_{AD}	f_{XX} = 15 MHz, C_L = 150 pF		250	ns
Data input time from ALE↓	t_{LDR}			135	ns
Data input time from $\overline{RD}$↓	t_{RD}			120	ns
$\overline{RD}$↓ delay time from ALE↓	t_{LR}		15		ns
Data hold time (from $\overline{RD}$↑)	t_{RDH}	C_L = 150 pF	0		ns
ALE↑ delay time from $\overline{RD}$↑	t_{RL}	f_{XX} = 15 MHz, C_L = 150 pF	80		ns
$\overline{RD}$ low-level width	t_{RR}	In data read f_{XX} = 15 MHz, C_L = 150 pF	215		ns
		In OP code fetch f_{XX} = 15 MHz, C_L = 150 pF	415		ns
ALE high-level width	t_{LL}	f_{XX} = 15 MHz, C_L = 150 pF	90		ns
$\overline{WR}$↓ delay time from address	t_{AW}	f_{XX} = 15 MHz, C_L = 150 pF	100		ns
Data output time from ALE↓	t_{LDW}			197	ns
Data output time from $\overline{WR}$↓	t_{WD}	C_L = 150 pF		140	ns
$\overline{WR}$↓ delay time from ALE↓	t_{LW}	f_{XX} = 15 MHz, C_L = 150 pF	15		ns
Data setup time (to $\overline{WR}$↑)	t_{DW}		127		ns
Data hold time (from $\overline{WR}$↑)	t_{WDH}		60		ns
ALE↑ delay time from $\overline{WR}$↑	t_{WL}		80		ns
$\overline{WR}$ low-level width	t_{WW}		215		ns

ZERO-CROSS CHARACTERISTICS :

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
Zero-cross detection input	V_{ZX}	AC coupling 60-Hz sine wave	1	1.8	VAC_{P-P}
Zero-cross accuracy	A_{ZX}			±135	mV
Zero-cross detection input frequency	f_{ZX}		0.05	1	kHz

SERIAL OPERATION :

PARAMETER	SYMBOL	TEST CONDITIONS		MIN.	MAX.	UNIT
$\overline{SCK}$ cycle time	t_{CYK}	$\overline{SCK}$ input	**Note1**	800		ns
			Note2	400		ns
		$\overline{SCK}$ output		1.6		μs
$\overline{SCK}$ low-level width	t_{KKL}	$\overline{SCK}$ input	**Note1**	335		ns
			Note2	160		ns
		$\overline{SCK}$ output		700		ns
$\overline{SCK}$ high-level width	t_{KKH}	$\overline{SCK}$ input	**Note1**	335		ns
			Note2	160		ns
		$\overline{SCK}$ output		700		ns
RxD setup time (to $\overline{SCK}\uparrow$)	t_{RXK}	**Note1**		80		ns
RxD hold time (from $\overline{SCK}\uparrow$)	t_{KRX}	**Note1**		80		ns
TxD delay time from $\overline{SCK}\downarrow$	t_{KTX}	**Note1**			210	ns

Notes 1. If clock rate is × 1 in asynchronous mode, synchronous mode, or I/O interface mode.

2. If clock rate is × 16 or × 64 in asynchronous mode.

Remark The numeric values in the table are those when f_{XX} = 15 MHz, C_L = 100 pF.

OTHER OPERATION :

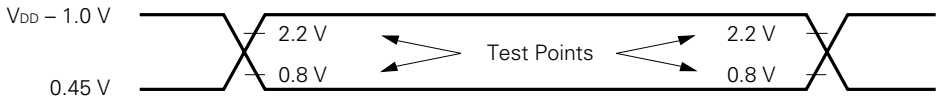
PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	MAX.	UNIT
TI high-, low-level width	t_{TIH}, t_{TIL}		6		t_{CYC}
CI high-, low-level width	t_{CI1H}, t_{CI1L}	• Event counter mode • Frequency test mode	6		t_{CYC}
	t_{CI2H}, t_{CI2L}	• Pulse width test mode • ECNT latch and clear input • INTEIN set input	48		t_{CYC}
$\overline{NMI}$ high-, low-level width	t_{NIH}, t_{NIL}		10		μs
INT1 high-, low-level width	t_{I1H}, t_{I1L}		36		t_{CYC}
$\overline{INT2}$ high-, low-level width	t_{I2H}, t_{I2L}		36		t_{CYC}
AN4 to AN7, low-level width	t_{ANH}, t_{ANL}		36		t_{CYC}
$\overline{RESET}$ high-, low-level width	t_{RSH}, t_{RSL}		10		μs

A/D CONVERTER CHARACTERISTICS (T_A = –40 to +85 °C, V_{DD} = +5.0 V ± 10 %, V_{SS} = AV_{SS} = 0 V, V_{DD} – 0.5 V ≤ AV_{DD} ≤ V_{DD}, 3.4 V ≤ V_{AREF} ≤ AV_{DD})

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Resolution			8			Bits
Absolute accuracy[Note]		3.4 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 167 ns			±0.8 %	FSR
		4.0 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 167 ns			±0.6 %	FSR
		T_A = –10 to +70 °C, 4.0 V ≤ V_{AREF} ≤ AV_{DD}, 66 ns ≤ t_{CYC} ≤ 167 ns			±0.4 %	FSR
Conversion time	t_{CONV}	66 ns ≤ t_{CYC} ≤ 110 ns	576			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 167 ns	432			t_{CYC}
Sampling time	t_{SAMP}	66 ns ≤ t_{CYC} ≤ 110 ns	96			t_{CYC}
		110 ns ≤ t_{CYC} ≤ 167 ns	72			t_{CYC}
Analog input voltage	V_{IAN}		–0.3		V_{AREF} + 0.3	V
★ Analog input impedance	R_{AN}			50		MΩ
Reference voltage	V_{AREF}		3.4		AV_{DD}	V
V_{AREF} current	I_{AREF1}	Operating mode		1.5	3.0	mA
	I_{AREF2}	STOP mode		0.7	1.5	mA
AV_{DD} power supply current	AI_{DD1}	Operating mode f_{XX} = 15 MHz		0.5	1.3	mA
	AI_{DD2}	STOP mode		10	20	μA

Note Quantization error (±1/2 LSB) is not included.

AC Timing Test Point



t_{CYC}-Dependent AC Characteristics Expression

PARAMETER	EXPRESSION	MIN./MAX.	UNIT
t_{AL}	2T – 100	MIN.	ns
t_{LA}	T – 30	MIN.	ns
t_{AR}	3T – 100	MIN.	ns
t_{AD}	7T – 220	MAX.	ns
t_{LDR}	5T – 200	MAX.	ns
t_{RD}	4T – 150	MAX.	ns
t_{LR}	T – 50	MIN.	ns
t_{RL}	2T – 50	MIN.	ns
t_{RR}	4T – 50 (In data read)	MIN.	ns
	7T – 50 (In OP code fetch)		
t_{LL}	2T – 40	MIN.	ns
t_{AW}	3T – 100	MIN.	ns
t_{LDW}	T + 130	MAX.	ns
t_{LW}	T – 50	MIN.	ns
t_{DW}	4T – 140	MIN.	ns
t_{WDH}	2T – 70	MIN.	ns
t_{WL}	2T – 50	MIN.	ns
t_{WW}	4T – 50	MIN.	ns
t_{CYK}	12T ($\overline{SCK}$ input)[Note1]	MIN.	ns
	6T ($\overline{SCK}$ input)[Note2]		
	24T ($\overline{SCK}$ output)		
t_{KKL}	5T + 5 ($\overline{SCK}$ input)[Note1]	MIN.	ns
	2.5T + 5 ($\overline{SCK}$ input)[Note2]		
	12T – 100 ($\overline{SCK}$ output)		
t_{KKH}	5T + 5 ($\overline{SCK}$ input)[Note1]	MIN.	ns
	2.5T + 5 ($\overline{SCK}$ input)[Note2]		
	12T – 100 ($\overline{SCK}$ output)		

Notes 1. If clock rate is ×1, in asynchronous mode, synchronous mode, or I/O interface mode.

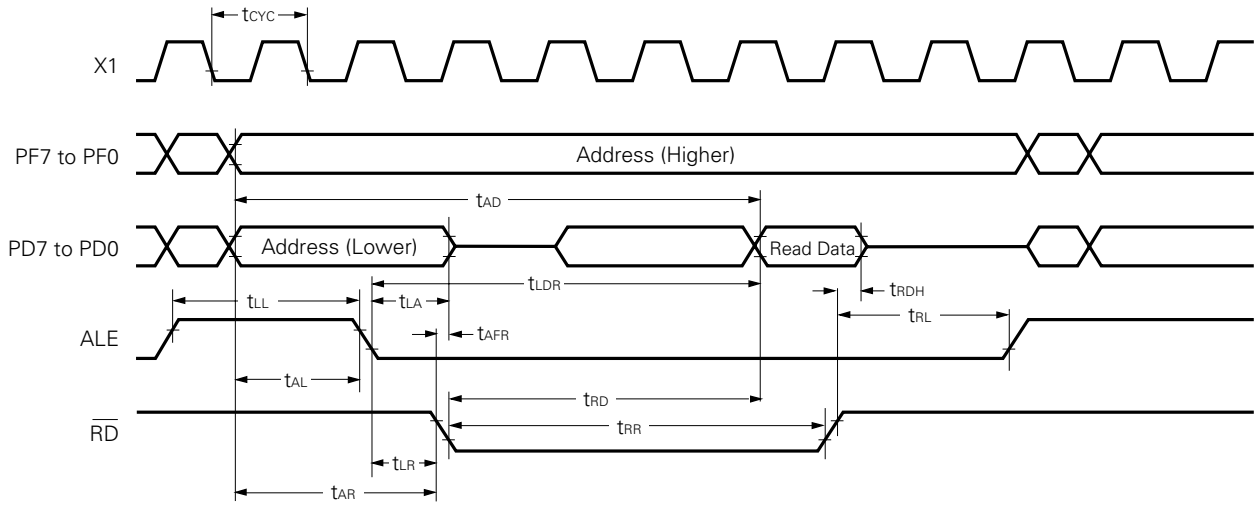
2. If clock rate is ×16, ×64 in asynchronous mode.

Remarks 1. $T = t_{CYC} = 1/f_{XX}$

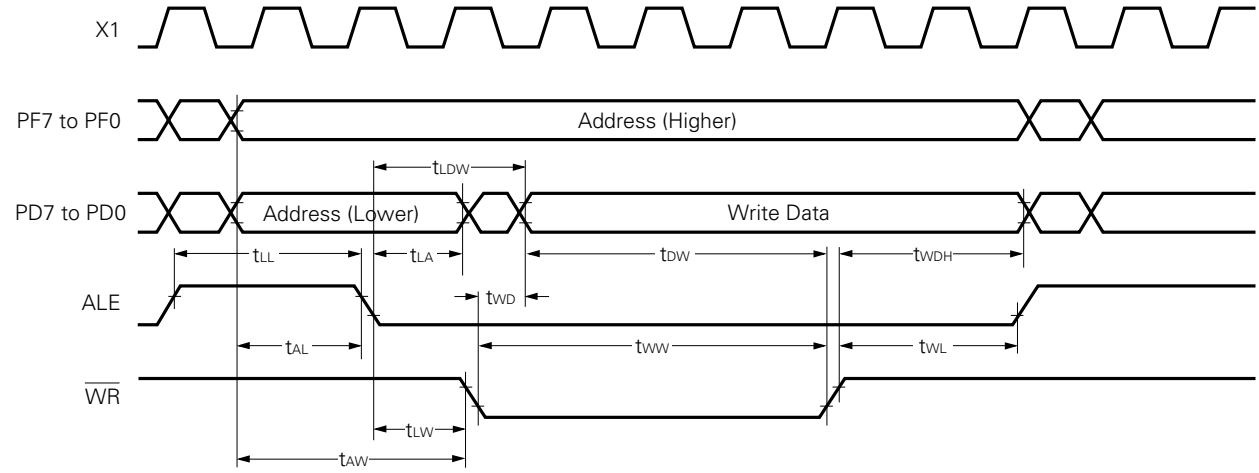
2. Other items which are not listed in this table are not dependent on oscillator frequency (f_{XX}).

Timing Waveforms

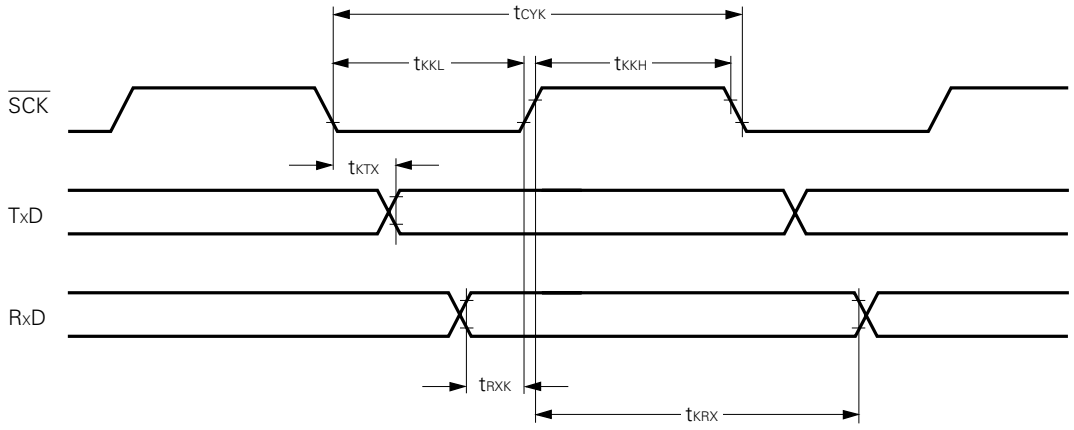
Read Operation



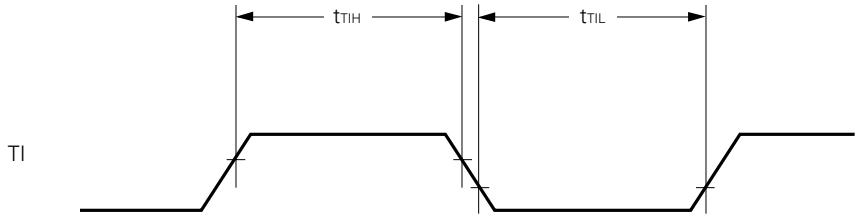
Write Operation



Serial Operation

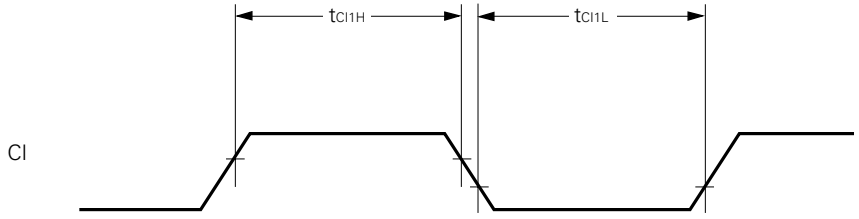


Timer Input Timing

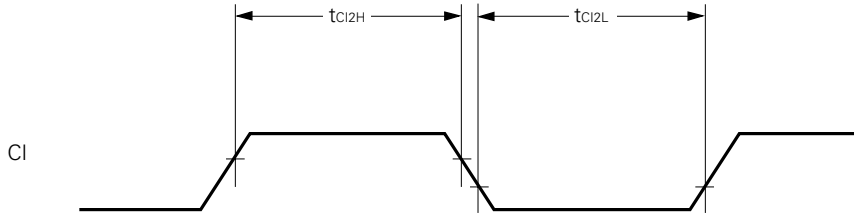


Timer/Event Counter Input Timing

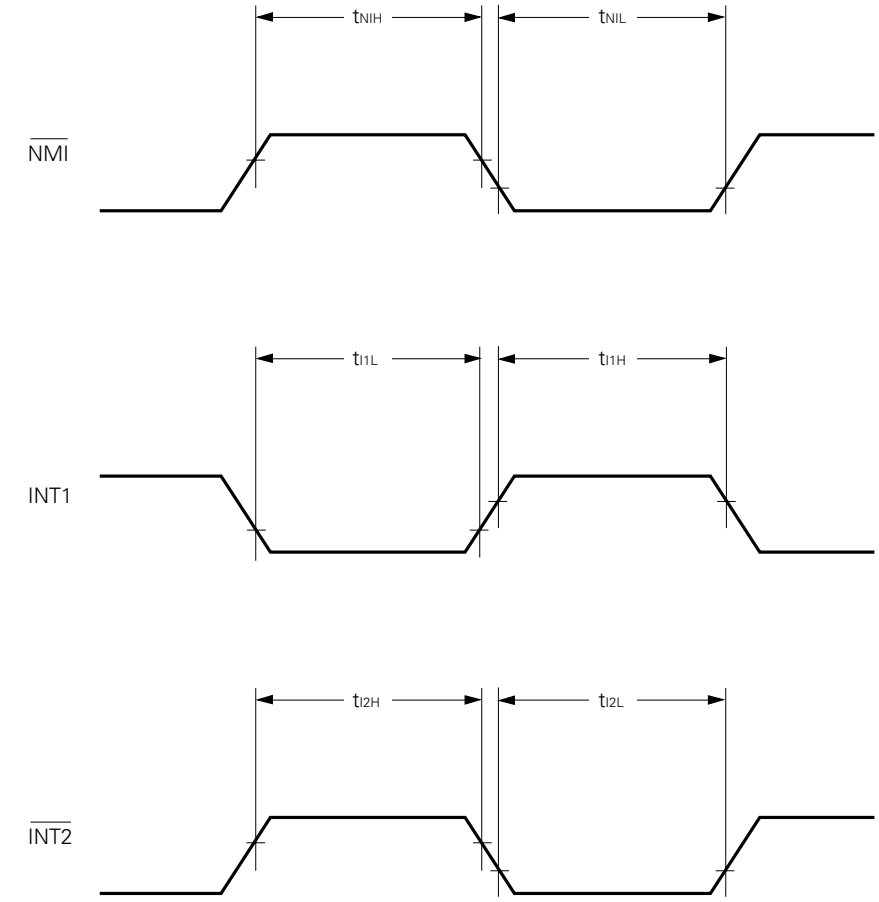
Event Count Mode



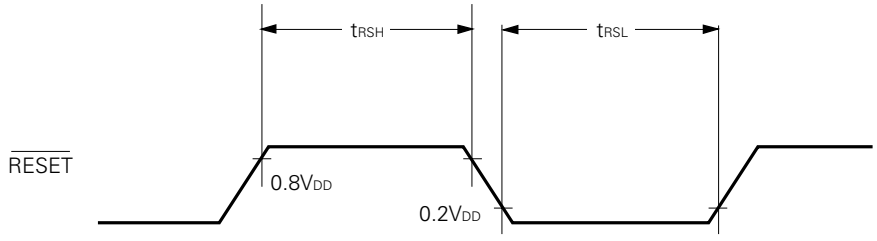
Pulse Width Test Mode



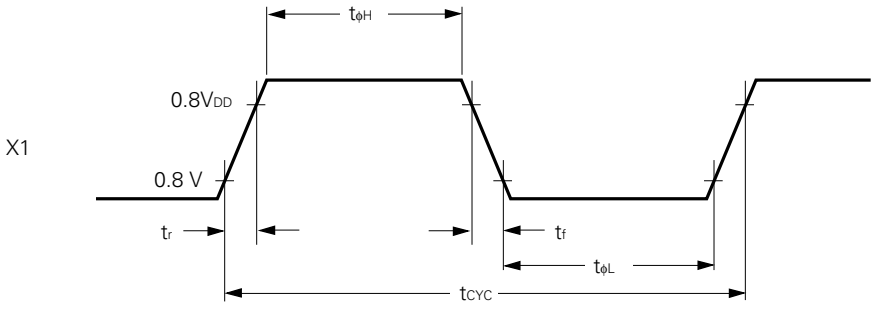
Interrupt Input Timing



Reset Input Timing



External Clock Timing

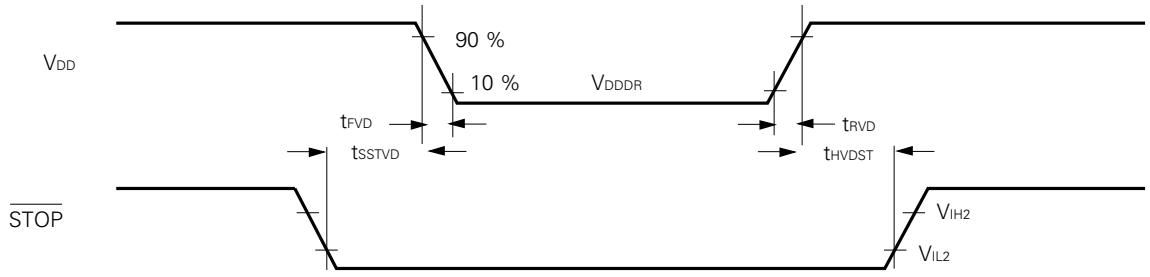


DATA MEMORY STOP MODE LOW POWER SUPPLY VOLTAGE DATA RETENTION CHARACTERISTICS (T_A = –40 to +85 °C)

PARAMETER	SYMBOL	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Data retention power supply voltage	V_{DDDR}		2.5		5.5	V
Data retention power supply current	I_{DDDR}	V_{DDDR} = 2.5 V		1	15	μA
		V_{DDDR} = 5 V ± 10 %		10	50	μA ★
V_{DD} rise/fall time	t_{RVD}, t_{FVD}		200			μs
$\overline{STOP}$ setup time (to V_{DD})	t_{SSTVD}		12T + 0.5 **Note**			μs
$\overline{STOP}$ hold time (from V_{DD})	t_{HVDST}		12T + 0.5 **Note**			μs

Note T= t_{CYC} = 1/fxx

Data Retention Timing



DC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5 °C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL[Note]	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Input voltage high	V_{IH}	V_{IH}		2.4		V_{DDP} + 0.3	V
Input voltage low	V_{IL}	V_{IL}		–0.3		0.8	V
Input leakage current	I_{LIP}	I_{LI}	0 ≤ V_I ≤ V_{DDP}; except INT1, TI (PC3)			±10	μA
Output voltage high	V_{OH}	V_{OH}	I_{OH} = –1.0 mA	V_{DD} – 1.0			V
Output voltage low	V_{OL}	V_{OL}	I_{OL} = 2.0 mA			0.45	V
Output leakage current	I_{LO}	—	0 ≤ V_O ≤ V_{DDP}, $\overline{OE}$ = V_{IH}			±10	μA
V_{DDP} supply voltage	V_{DDP}	V_{DD}	EPROM programming mode	5.75	6.0	6.25	V
			EPROM read mode	4.5	5.0	5.5	V
V_{PP} supply voltage	V_{PP}	V_{PP}	EPROM programming mode	12.2	12.5	12.8	V
			EPROM read mode	V_{PP} = V_{DDP}			V
V_{DDP} supply current	I_{DD}	I_{DD}	EPROM programming mode		5	50	mA
			EPROM read mode $\overline{CE}$ = V_{IL}, V_I = V_{IH}		5	50	mA
V_{PP} supply current	I_{PP}	I_{PP}	EPROM programming mode $\overline{CE}$ = V_{IL}, $\overline{OE}$ = V_{IH}		5	30	mA
			EPROM read mode		1	100	μA

Note Corresponding μPD27C256A symbol

Phase-out/Discontinued

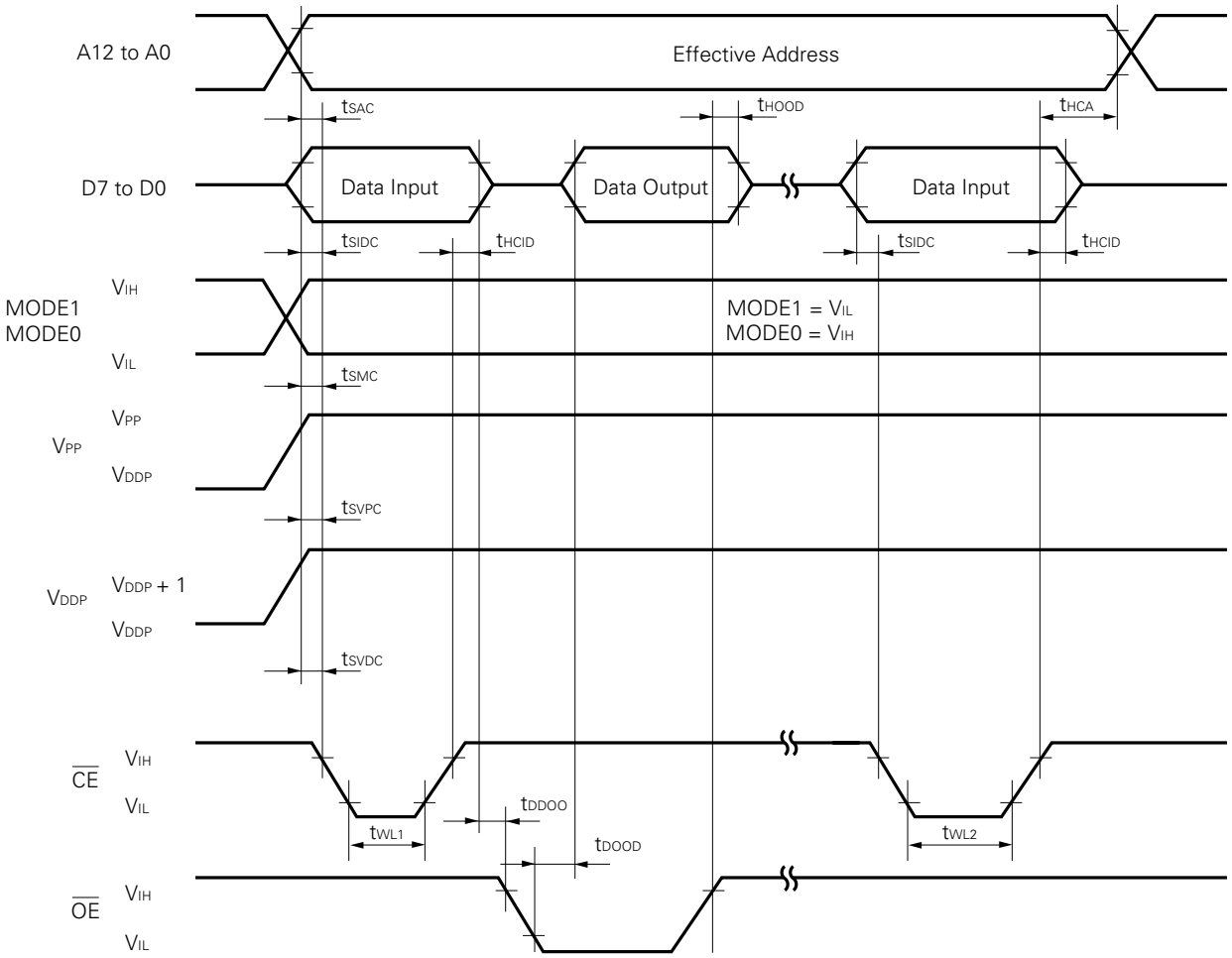
AC PROGRAMMING CHARACTERISTICS (T_A = 25 ± 5 °C, MODE1 = V_{IL}, MODE0 = V_{IH}, V_{SS} = 0 V)

PARAMETER	SYMBOL	SYMBOL[Note1]	TEST CONDITIONS	MIN.	TYP.	MAX.	UNIT
Address setup time (to $\overline{CE}\downarrow$)	t_{SAC}	t_{AS}		2			μs
$\overline{OE}\downarrow$ delay time from data	t_{DDOO}	t_{OES}		2			μs
Input data setup time (to $\overline{CE}\downarrow$)	t_{SIDC}	t_{DS}		2			μs
Address hold time (from $\overline{CE}\uparrow$)	t_{HCA}	t_{AH}		2			μs
Input data hold time (from $\overline{CE}\uparrow$)	t_{HCID}	t_{DH}		2			μs
Output data hold time (from $\overline{OE}\uparrow$)	t_{HOOD}	t_{DF}		0		130	ns
V_{PP} setup time (to $\overline{CE}\downarrow$)	t_{SVPC}	t_{VPS}		2			μs
V_{DDP} setup time (to $\overline{CE}\downarrow$)	t_{SVDC}	t_{VDS}		2			μs
Initial program pulse width	t_{WL1}	t_{PW}		0.95	1.0	1.05	ms
Additional program pulse width	t_{WL2}	t_{OPW}		2.85		78.75	ms
EPROM programming/read mode setup time (to $\overline{CE}\downarrow$)[Note2]	t_{SMC}	—		2			μs
Data output time from address	t_{DAOD}	t_{ACC}	$\overline{OE}$ = V_{IL}			1	μs
Data output time from $\overline{CE}\downarrow$	t_{DCOD}	t_{CE}				1	μs
Data output time from $\overline{OE}\downarrow$	t_{DOOD}	t_{OE}				1	μs
Data hold time (from $\overline{OE}\uparrow$)	t_{HCOD}	t_{DF}		0		130	ns
Data hold time (from address)	t_{HAOD}	t_{OH}	$\overline{OE}$ = V_{IL}	0			ns

Notes 1. Corresponding μPD27C256A symbol

2. Indicates state in which MODE1 = V_{IL} and MODE0 = V_{IH}.

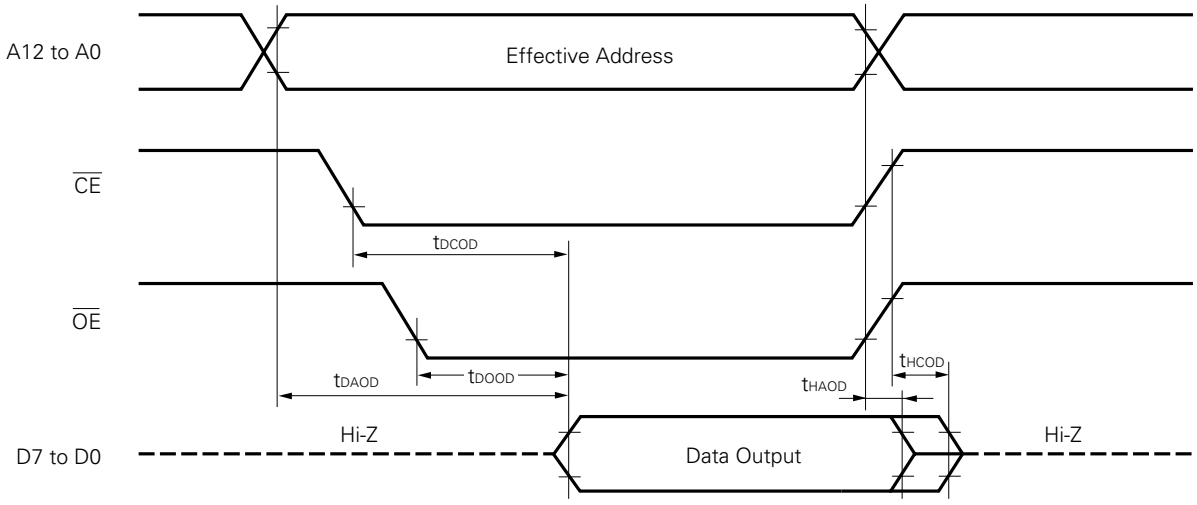
PROM Programming Mode Timing



Cautions 1. Ensure that V_{DDP} is applied before V_{PP}, and cut after V_{PP}.

2. Ensure that V_{PP} does not exceed +13 V including overshoot.

PROM Read Mode Timing

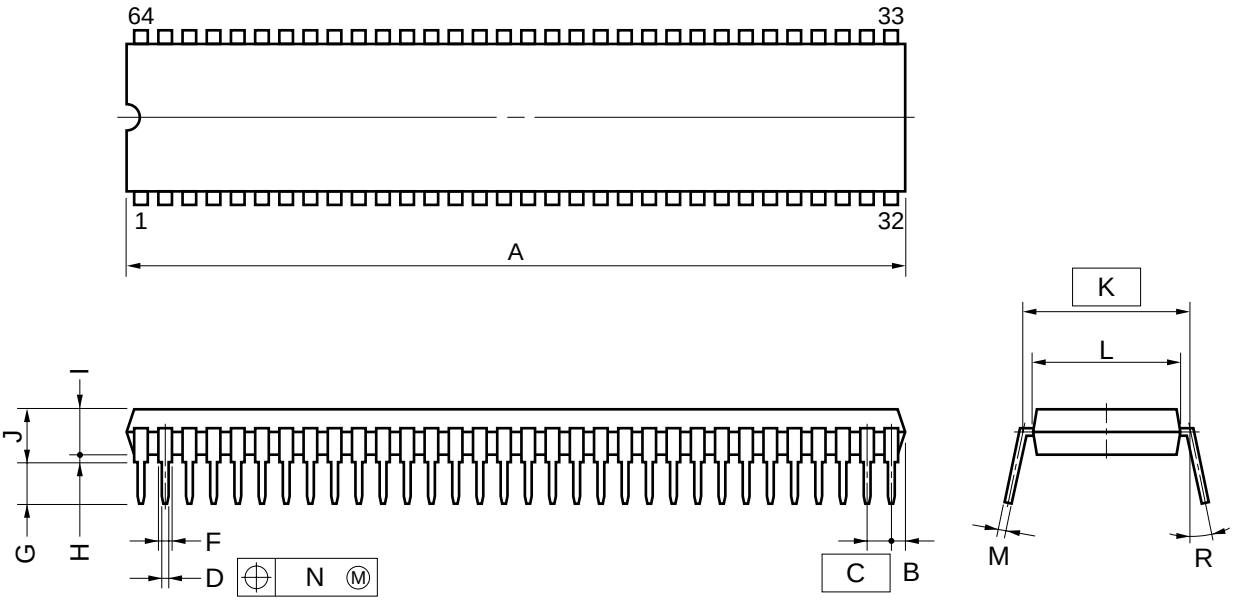


Cautions 1. If you wish to read within the t_{DAOD} range, the $\overline{OE}$ input delay time from the fall of $\overline{CE}$ should be a maximum of t_{DAOD} - t_{DOOD}.

2. t_{HCOD} is the time from the point at which $\overline{OE}$ or $\overline{CE}$ (whichever is first) reaches V_{IH}.

8. PACKAGE DRAWINGS

64 PIN PLASTIC SHRINK DIP (750 mil)



NOTE

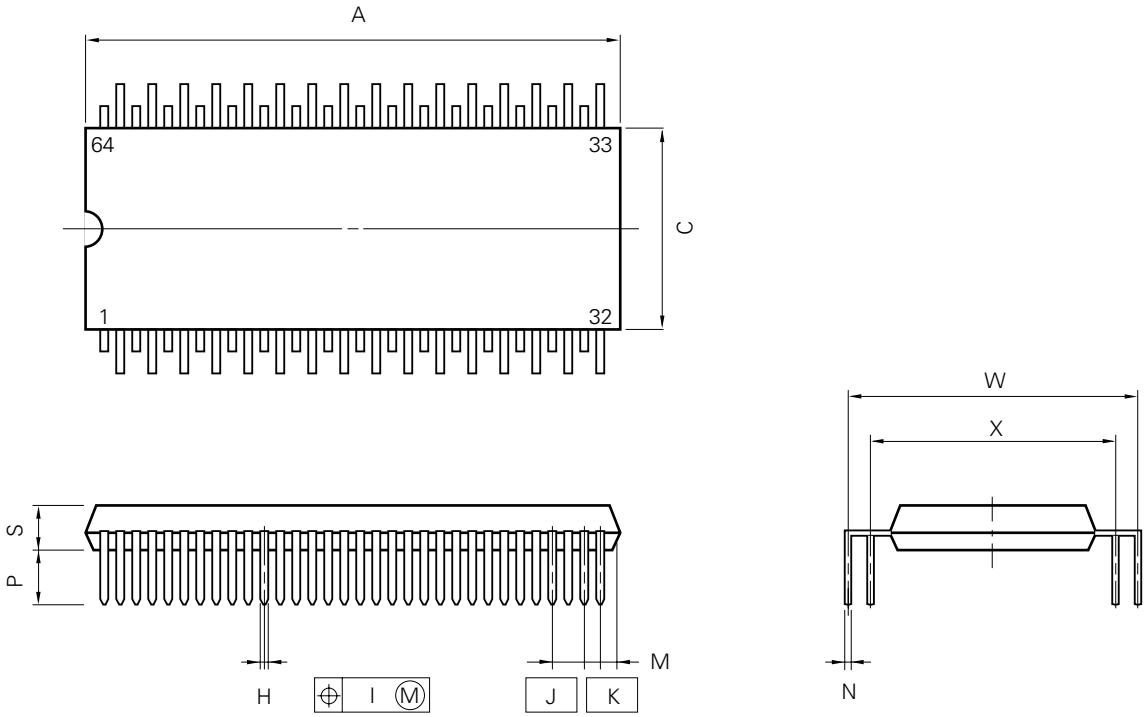
1) Each lead centerline is located within 0.17 mm (0.007 inch) of its true position (T.P.) at maximum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.311 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	0.50 ± 0.10	$0.020^{+0.004}_{-0.005}$
F	0.9 MIN.	0.035 MIN.
G	3.2±0.3	0.126±0.012
H	0.51 MIN.	0.020 MIN.
I	4.31 MAX.	0.170 MAX.
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	17.0	0.669
M	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
N	0.17	0.007
R	0~15°	0~15°

P64C-70-750A,C-1

64 PIN PLASTIC QUIP



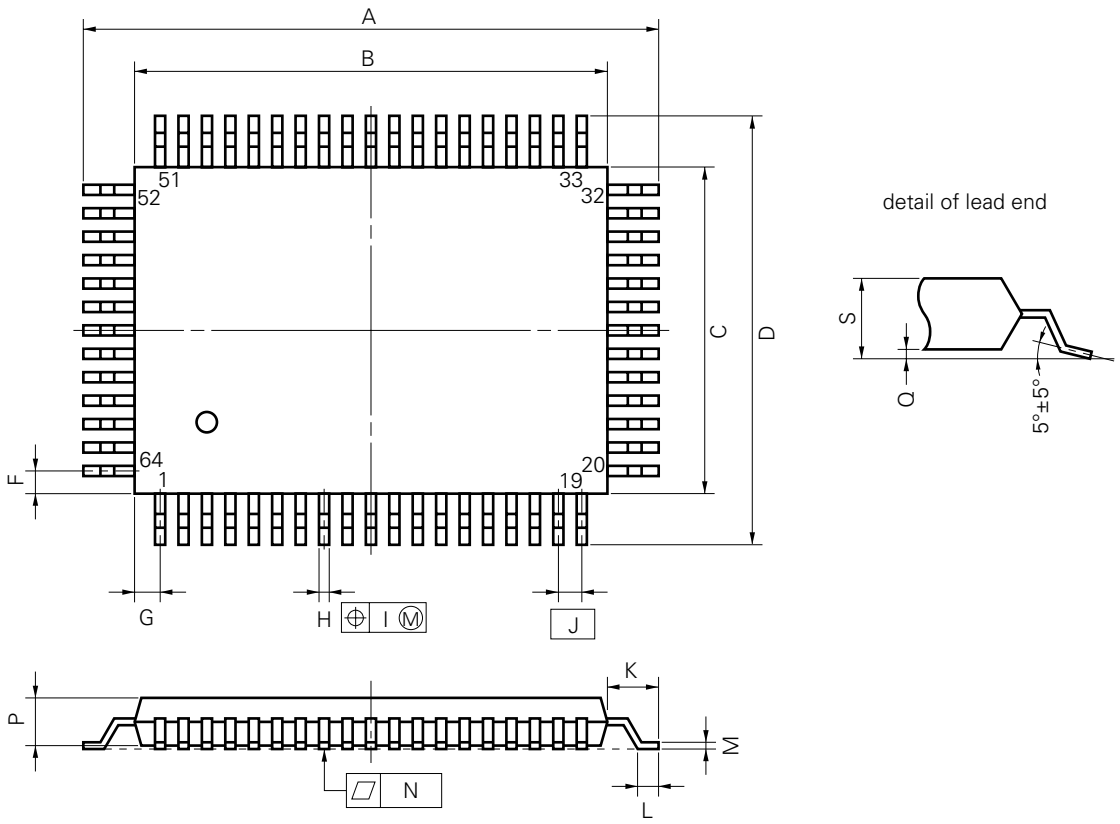
P64GQ-100-36

NOTE

Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	$41.5^{+0.3}_{-0.2}$	$1.634^{+0.012}_{-0.008}$
C	16.5	0.650
H	$0.50^{\pm0.10}$	$0.020^{+0.004}_{-0.005}$
I	0.25	0.010
J	2.54 (T.P.)	0.100 (T.P.)
K	1.27 (T.P.)	0.050 (T.P.)
M	$1.1^{+0.25}_{-0.15}$	$0.043^{+0.011}_{-0.006}$
N	$0.25^{+0.10}_{-0.05}$	$0.010^{+0.004}_{-0.003}$
P	$4.0^{\pm0.3}$	$0.157^{+0.013}_{-0.012}$
S	$3.6^{\pm0.1}$	$0.142^{+0.004}_{-0.005}$
W	$24.13^{\pm1.05}$	$0.950^{\pm0.042}$
X	$19.05^{\pm1.05}$	$0.750^{\pm0.042}$

64 PIN PLASTIC QFP (14×20)



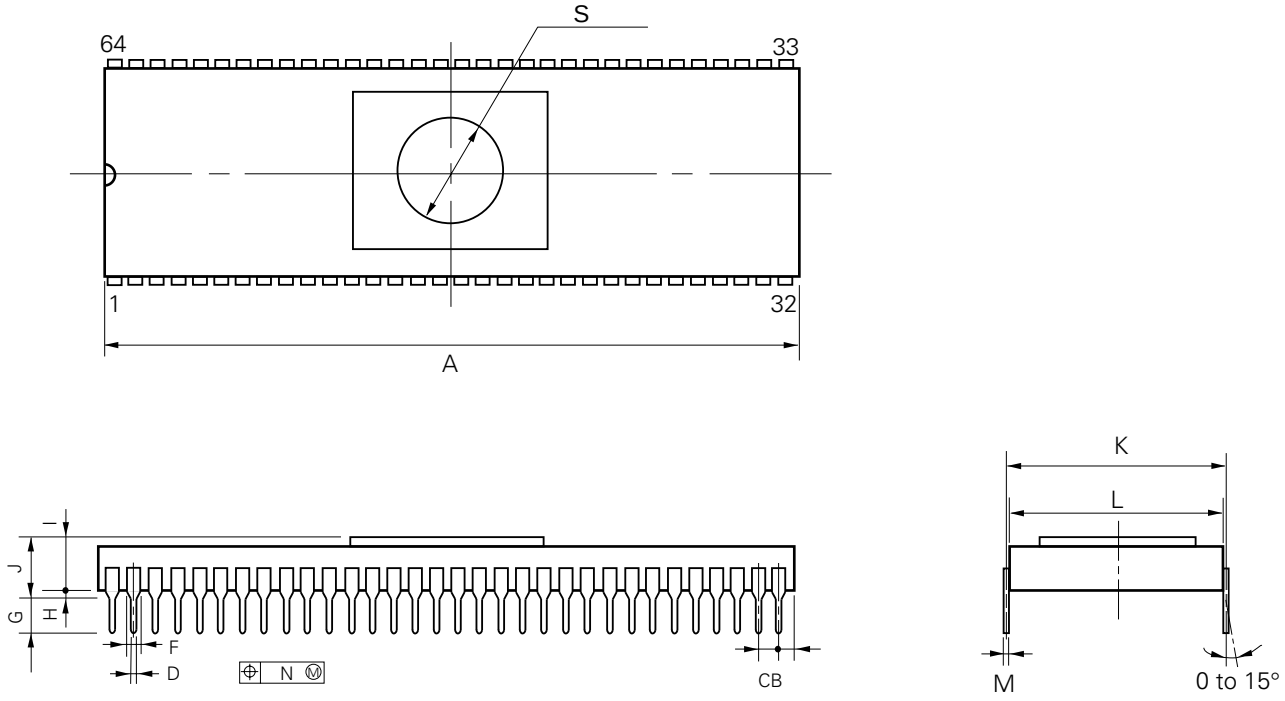
P64GF-100-3B8,3BE,3BR-1

NOTE

Each lead centerline is located within 0.20 mm (0.008 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	1.0	0.039
G	1.0	0.039
H	0.40±0.10	$0.016^{+0.004}_{-0.005}$
I	0.20	0.008
J	1.0 (T.P.)	0.039 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.12	0.005
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

64 PIN CERAMIC SHRINK DIP (750 mil)



P64DW-70-750A

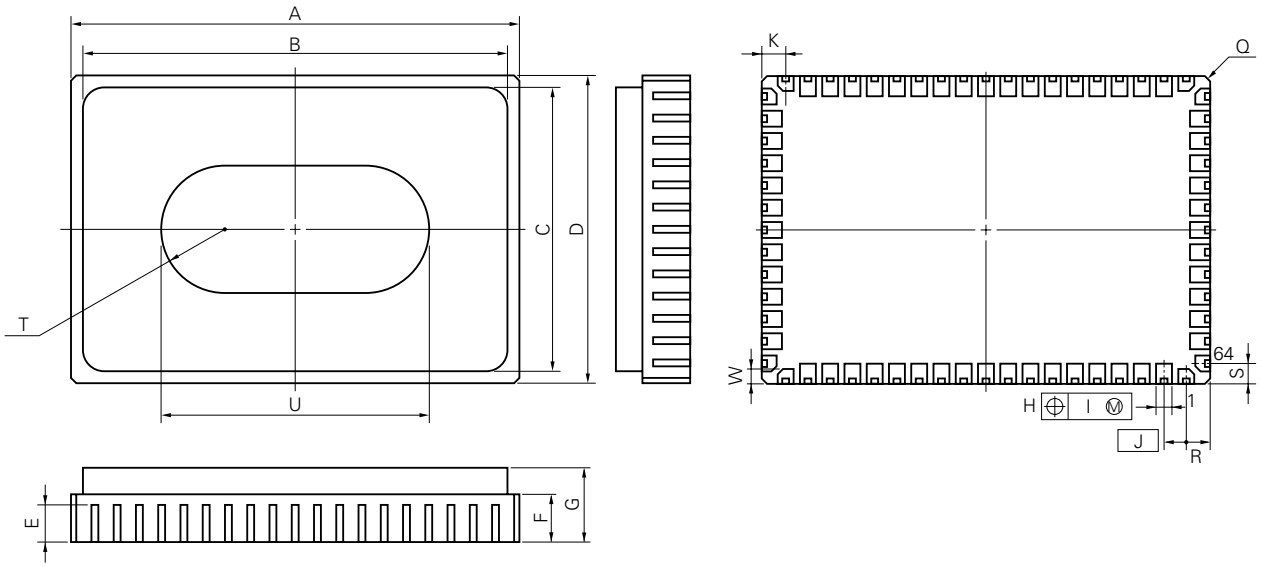
NOTES

1) Each lead centerline is located within 0.25 mm (0.010 inch) of its true position (T.P.) at maxi-mum material condition.

2) Item "K" to center of leads when formed parallel.

ITEM	MILLIMETERS	INCHES
A	58.68 MAX.	2.310 MAX.
B	1.78 MAX.	0.070 MAX.
C	1.778 (T.P.)	0.070 (T.P.)
D	$0.46^{\pm 0.05}$	$0.018^{\pm 0.002}$
F	0.8 MIN.	0.031 MIN.
G	$3.5^{\pm 0.3}$	$0.138^{\pm 0.012}$
H	1.0 MIN.	0.039 MIN.
I	3.0	0.118
J	5.08 MAX.	0.200 MAX.
K	19.05 (T.P.)	0.750 (T.P.)
L	18.8	0.740
M	$0.25^{\pm 0.05}$	$0.010^{+0.002}_{-0.003}$
N	0.25	0.01
S	⌀ 8.89	⌀ 0.350

64 PIN CERAMIC WQFN



X64KW-100A-2

NOTE

Each lead centerline is located within 0.10 mm (0.004 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	20.0±0.4	$0.787^{+0.017}_{-0.016}$
B	19.0	0.748
C	13.2	0.520
D	14.0±0.4	0.551±0.016
E	1.64	0.065
F	2.14	0.084
G	3.556 MAX.	0.140 MAX.
H	0.7±0.10	$0.028^{+0.004}_{-0.005}$
I	0.10	0.004
J	1.0 (T.P.)	0.039 (T.P.)
K	1.0±0.2	$0.039^{+0.009}_{-0.008}$
Q	C 0.25	C 0.010
R	1.0	0.039
S	1.0	0.039
T	R 3.0	R 0.118
U	12.0	0.472
W	0.8±0.2	$0.031^{+0.009}_{-0.008}$

★ 9. RECOMMENDED SOLDERING CONDITIONS

The μPD78CP18 should be soldered and mounted under the following recommended conditions.

For details of recommended soldering conditions, refer to the information document "Semiconductor Device Mounting Technology Manual (IEI-1207)".

For soldering methods and conditions other than those recommended below, contact an NEC representative.

Table 9-1. Surface Mount Type Soldering Conditions

μPD78CP18GF-3BE: 64-Pin Plastic QFP (14 × 20 mm)

Soldering Method	Soldering Conditions	Recommended Condition Symbol
Infrared reflow	Package peak temperature: 235 °C, Duration: 30 sec. max. (at 210 °C min.), Count: Twice or less **<Attention>** (1) Perform the second reflow at the time the device temperature is lowered to the room temperature from the heating by the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	IR35-00-2
VPS	Package peak temperature: 215 °C, Duration: 40 sec. max.(at 200 °C min.), Count: Twice or less **<Attention>** (1) Perform the second reflow at the time the device temperature is lowered to the room temperature from the heating by the first reflow. (2) Do not wash the soldered portion with the flux following the first reflow.	VP15-00-2
Wave soldering	Solder bath temperature: 260 °C max., Duration: 10 sec. max., Count: Once Preheating temperature: 120 °C max. (package surface temperature)	WS60-00-1
Partial heating	Pin temperature: 300 °C max., Time: 3 sec. max. (per device side row of pins)	——

Caution Use of more than one soldering method should be avoided (except in the case of pin part heating).

Table 9-2. Through-Hole Type Soldering Conditions

μPD78CP18CW: 64-Pin Plastic Shrink DIP (750 mil)
μPD78CP18DW: 64-Pin Ceramic Shrink DIP w/window (750 mil)
μPD78CP18GQ-36: 64-Pin Plastic QUIP

Soldering Method	Soldering Conditions
Wave soldering (pin part only)	Solder bath temperature: 260 °C max., Duration: 10 sec. max.
Partial heating	Pin temperature: 300 °C or less, Duration: 3 sec. max. (per pin)

Caution Wave soldering is used on the pin only, and care must be taken to prevent solder from coming into direct contact with the body.

Phase-out/Discontinued

10. DIFFERENCES BETWEEN THE μPD78CP18 AND μPD78C18

Item \ Product Name	μPD78CP18	μPD78C18
Internal ROM	32 K × 8 bits (PROM)	32 K × 8 bits (mask ROM)
Internal RAM	1 K × 8 bits	1 K × 8 bits
Pin connection	PB7/$\overline{OE}$	PB7
	PB6/$\overline{CE}$	PB6
	$\overline{STOP}$/V_{PP}	$\overline{STOP}$
	$\overline{NMI}$/A9	$\overline{NMI}$
	PA7/A7 to PA0/A0	PA7 to PA0
	PF6/A14 to PF2/A10	PF6 to PF2
	PF0/A8	PF0
	PD7/O7 to PD0/O0	PD7 to PD0
Mode set by MODE pins (when MODE0 is set to 1, and MODE1 to 0)	PROM programming mode	• Operates as the μPD78C17 (ROM-less mode) • External memory 16 K extension mode
MODE0 pin input/output function	Input only[Note]	Input/output
Internal memory access area setting by MM register	Yes	No
Port A to Port C	Pull-up resistors not incorporated	Pull-up resistor incorporation selectable bit-wise by mask option
Package	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm) • 64-pin plastic QUIP • 64-pin ceramic shrink DIP with window (750 mil) • 64-pin ceramic WQFN	• 64-pin plastic shrink DIP (750 mil) • 64-pin plastic QFP (14 × 20 mm) • 64-pin plastic QUIP
Electrical characteristics	Current dissipation differs. For details, refer to Data Sheet of each model.	★
Others	Noise immunity and noise radiation differ because of difference of circuit scale and mask layout.	★

Note An emulation control signal is not output even if the MODE0 pin is pulled high.

Caution The noise immunity and noise radiation differ between the PROM and mask ROM models. To replace the PROM model with the mask ROM model in the course of experimental development toward mass production of your application system, thoroughly evaluate the system by using the CS model (not ES model) of the mask ROM model. ★

★ APPENDIX A. DEVELOPMENT TOOLS

The following development tools are available to develop a system which uses the μPD78CP18.

Language Processor

<table>
<tr><td rowspan="5">87AD series
relocatable assembler
(RA87)</td><td colspan="4">This is a program which converts a program written in mnemonic to an object code for which microcomputer execution is possible.
Besides, it contains a function to automatically create a symbol/table, and optimize a branch instruction.</td></tr>
<tr><td>Host Machine</td><td>OS</td><td>Supply Medium</td><td>Ordering Code (Product Name)</td></tr>
<tr><td rowspan="2">PC-9800
series</td><td rowspan="2">MS-DOS™
Ver. 2.11
to
Ver. 5.00A Note</td><td>3.5-inch 2HD</td><td>μS5A13RA87</td></tr>
<tr><td>5-inch 2HD</td><td>μS5A10RA87</td></tr>
<tr><td rowspan="2">IBM PC/AT™</td><td rowspan="2">PC DOS™
(Ver. 3.1)</td><td>3.5-inch 2HC</td><td>μS7B13RA87</td></tr>
<tr><td>5-inch 2HC</td><td>μS7B10RA87</td></tr>
</table>

Note Versions 5.00 and 5.00A have a task swap function, but this function cannot be used with this software.

Remark The operations of the assembler are guaranteed only on the above host machines and operating systems.

PROM Write Tools

Hardware	PG-1500	With a provided board and an optional programmer adapter connected, this PROM programmer can manipulate from a stand-alone or host machine to perform programming on single-chip microcomputer which incorporates PROM. It is also capable of programming a typical PROM ranging from 256K to 4M bits.			
	PA-78CP14CW/GF/GQ/KB	PROM programmer adapter for the μPD78CP18. Used by connecting to the PG-1500.			
	PA-78CP14CW	For the μPD78CP18CW, 78CP18DW			
	PA-78CP14GF	For the μPD78CP18GF-3BE			
	PA-78CP14GQ	For the μPD78CP18GQ-36			
	PA-78CP14KB	For the μPD78CP18KB			
Software	PG-1500 controller	Connects the PG-1500 to a host machine by using serial and parallel interface, to control the PG-1500 on a host machine.			
		Host Machine	OS	Supply Medium	Ordering Code (Product Name)
		PC-9800 series	MS-DOS Ver. 2.11 to Ver. 5.00A[Note]	3.5-inch 2HD	μS5A13PG1500
				5-inch 2HD	μS5A10PG1500
		IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10PG1500

Note Versions 5.00 and 5.00A have a task swap function, but this function cannot be used with this software.

Remark The operations of the PG-1500 controller are guaranteed only on the above host machines and operating systems.

Debugging Tools

An in-circuit emulator (IE-78C11-M) is available as a program debugging tool for the μPD78CP18. The following table shows its system configuration.

Hardware	IE-78C11-M	The IE-78C11-M is an in-circuit emulator which works with the 87AD series. Only the IE-78C11-M is used if the plastic QUIP package is used. If the plastic shrink DIP is used, use the IE-78C11-M and a conversion socket in combination. It can be connected to a host machine to perform efficient debugging.			
	EV-9001-64	Conversion socket for plastic shrink DIP. Used in combination with IE-78C11-M.			
	EV-9200G-64	64-pin ceramic WQFN socket. Used in combination with the μPD78CP18KB as alternative of 64-pin plastic QFP package with window.			
Software	IE-78C11-M control program (IE controller)	Connects the IE-78C11-M to host machine by using the RS-232C, to control the IE-78C11-M on host machine.			
		Host Machine	OS	Supply Medium	Ordering Code (Product Name)
		PC-9800 series	MS-DOS [Ver. 2.11 to Ver. 3.30D]	3.5-inch 2HD	μS5A13IE78C11
				5-inch 2HD	μS5A10IE78C11
		IBM PC/AT	PC DOS (Ver. 3.1)	5-inch 2HC	μS7B10IE78C11

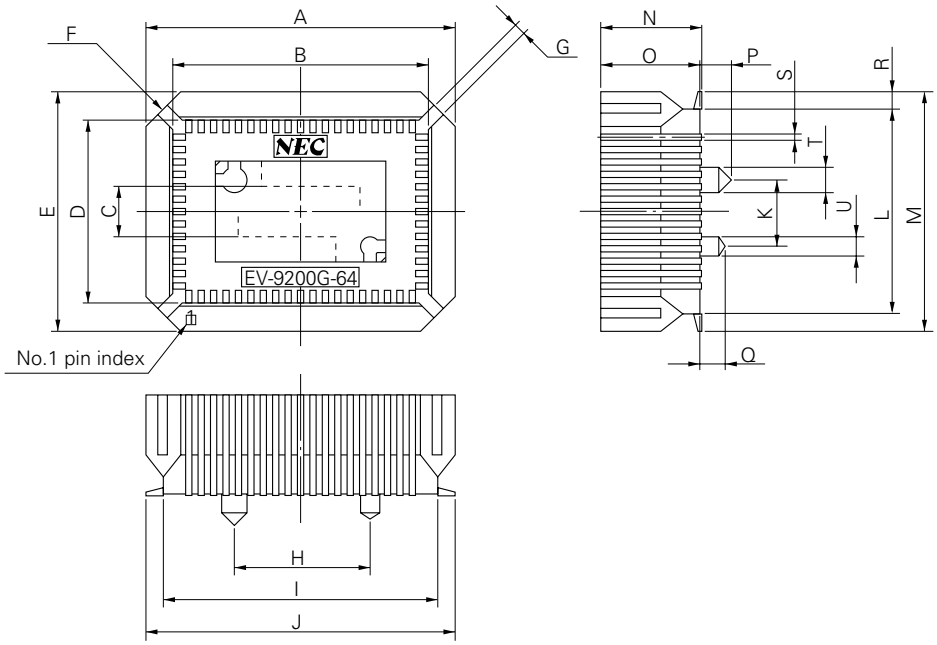
Remark The operations of the IE controller are guaranteed only on the above host machines and operating systems.

APPENDIX B. PACKAGE DRAWING AND FOOTPRINT OF CONVERSION SOCKET ★

The μPD78CP18KB (64-pin ceramic WQFN) is mounted with a conversion socket (EV-9200G-64) on a printed circuit board.

The figure below shows the package drawing and footprint of this conversion socket.

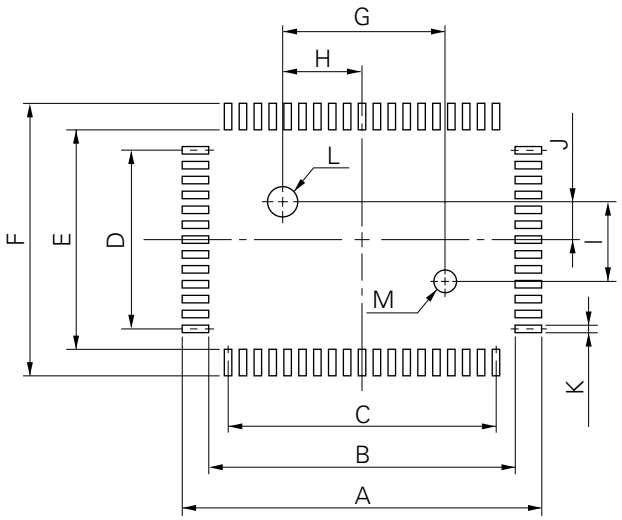
Figure B-1. Package Drawing of EV-9200G-64 (reference) (unit: mm)



EV-9200G-64-G0

ITEM	MILLIMETERS	INCHES
A	25.0	0.984
B	20.30	0.799
C	4.0	0.157
D	14.45	0.569
E	19.0	0.748
F	4-C 2.8	4-C 0.11
G	0.8	0.031
H	11.0	0.433
I	22.0	0.866
J	24.7	0.972
K	5.0	0.197
L	16.2	0.638
M	18.9	0.744
O	8.0	0.315
N	7.8	0.307
P	2.5	0.098
Q	2.0	0.079
R	1.35	0.053
S	0.35±0.1	$0.014^{+0.004}_{-0.005}$
T	φ2.3	φ0.091
U	φ1.5	φ0.059

Figure B-2. Footprint of EV-9200G-64 (reference) (unit: mm)



EV-9200G-64-P0

ITEM	MILLIMETERS	INCHES
A	25.7	1.012
B	21.0	0.827
C	1.0±0.02 × 18=18.0±0.05	$0.039^{+0.002}_{-0.001} \times 0.709 = 0.709^{+0.002}_{-0.003}$
D	1.0±0.02 × 12=12.0±0.05	$0.039^{+0.002}_{-0.001} \times 0.472 = 0.472^{+0.003}_{-0.002}$
E	15.2	0.598
F	19.9	0.783
G	11.00±0.08	$0.433^{+0.004}_{-0.003}$
H	5.50±0.03	$0.217^{+0.001}_{-0.002}$
I	5.00±0.08	$0.197^{+0.003}_{-0.004}$
J	2.50±0.03	$0.098^{+0.002}_{-0.001}$
K	0.6±0.02	$0.024^{+0.001}_{-0.002}$
L	ϕ2.36±0.03	$\phi 0.093^{+0.001}_{-0.002}$
M	ϕ1.57±0.03	$\phi 0.062^{+0.001}_{-0.002}$

Caution Dimensions of mount pad for EV-9200 and that for target device (QFP) may be different in some parts. For the recommended mount pad dimensions for QFP, refer to "SEMICONDUCTOR DEVICE MOUNTING TECHNOLOGY MANUAL" (IEI-1207).

Phase-out/Discontinued

NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards wiht semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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License not needed	**: μPD78CP18DW, 78CP18KB**
The customer must judge the need for license	**: μPD78CP18CW, 78CP18GF-3BE, 78CP18GQ-36**

M4 94.11