NEC

MOS INTEGRATED CIRCUIT

μPD78F0228

8-BIT SINGLE-CHIP MICROCONTROLLER

The μPD78F0228 is a member of the μPD780228 Subseries that belongs to the 78K/0 Series. It replaces the internal ROM of the μPD780228 with a flash memory.

Since the μPD78F0228 enables write/erase of a program while mounted on a board, it is suitable for applications involving system evaluation during system development, small-scale production of many different products, and rapid development and time-to-market of a new product.

The details of functions are described in the following user's manuals. Be sure to read them before designing.

μPD780228 Subseries User's Manual : Planned
78K/0 Series User's Manual Instructions : IEU-1372

FEATURES

- Pin-compatible with mask ROM versions (except V_{PP} pin)
- Flash memory: 60 Kbytes[Note]
- Internal high-speed RAM: 1024 bytes
- Internal expanded RAM: 512 bytes
- FIP® display RAM: 96 bytes
- Operable in the same supply voltage as mask ROM version (V_{DD} = 4.5 to 5.5 V)

Note The flash memory capacity can be changed with the memory size switching register (IMS).

Remark Refer to Section **1. DIFFERENCES BETWEEN μPD78F0228 AND MASK ROM VERSIONS** for the differences between flash memory version and mask ROM versions.

ORDERING INFORMATION

Part Number	Package	Internal ROM
μPD78F0228GF-3BA	100-pin plastic QFP (14 × 20 mm)	Flash memory

The information contained in this document is being issued in advance of the production cycle for the device. The parameters for the device may change before final production or NEC Corporation, at its own discretion, may withdraw the device prior to its production.

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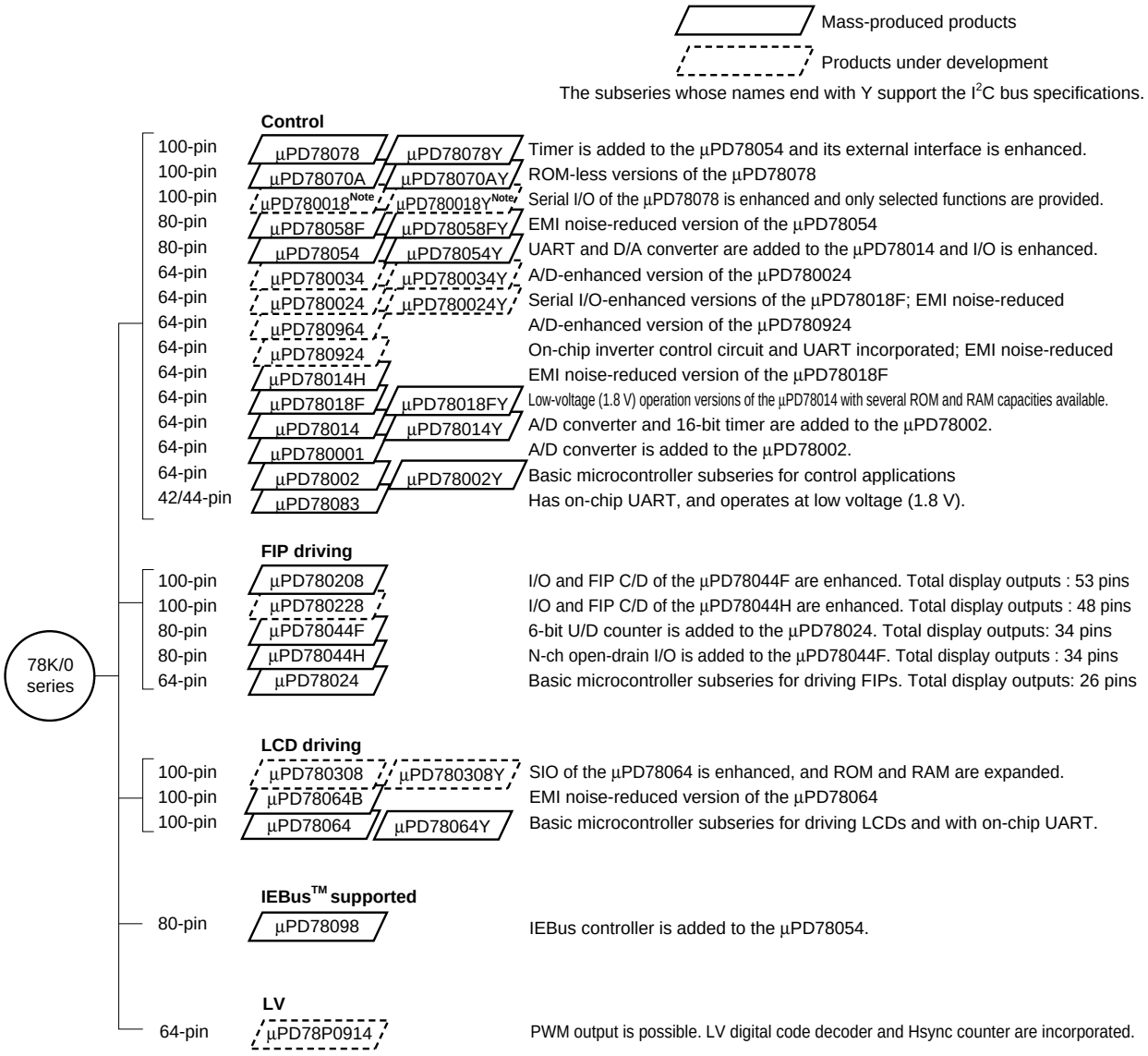
78K/0 Series Development

The following shows the 78K/0 Series products development. Subseries names are shown inside frames.



Note Under planning

The following table lists the main functional differences between subseries products.

Subseries name \ Function		ROM capacity	Timer				8-bit A/D	10-bit A/D	8-bit D/A	Serial interface	I/O	V_{DD} MIN. value	External expansion
			8-bit	16-bit	Watch	WDT							
Control	μPD78078	32K to 60K	4 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	88	1.8 V	Available
	μPD78070A	—									61	2.7 V	
	μPD780018	48K to 60K							—	2 ch (Time division 3-wire: 1 ch)	88		
	μPD78058F		2 ch						2 ch	3 ch (UART: 1 ch)	69		
	μPD78054	16K to 60K										2.0 V	
	μPD780034	8K to 32K					—	8 ch	—	3 ch (UART: 1 ch, Time division 3-wire: 1 ch)	51	1.8 V	
	μPD780024						8 ch	—					
	μPD780964		3 ch	**Note**	—		—	8 ch		2 ch (UART: 2 ch)	47	2.7 V	
	μPD780924						8 ch	—					
	μPD78014H		2 ch	1 ch	1 ch					2 ch	53	1.8 V	
	μPD78018F	8K to 60K											
	μPD78014	8K to 32K										2.7 V	
	μPD780001	8K		—	—					1 ch	39		—
	μPD78002	8K to 16K			1 ch		—				53		Available
	μPD78083	—			—		8 ch			1 ch (UART: 1 ch)	33	1.8 V	—
FIP driving	μPD780208	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	2 ch	74	2.7 V	—
	μPD780228	48K to 60K	3 ch	—	—					1 ch	72	4.5 V	
	μPD78044F	16K to 40K	2 ch	1 ch	1 ch					2 ch	68	2.7 V	
	μPD78044H	32K to 48K								1 ch			
	μPD78024	24K to 32K								2 ch	54		
LCD driving	μPD780308	48K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	—	3 ch (Time division UART: 1 ch)	57	1.8 V	—
	μPD78064B	32K								2 ch (UART: 1 ch)		2.0 V	
	μPD78064	16K to 32K											
IEBus supported	μPD78098	32K to 60K	2 ch	1 ch	1 ch	1 ch	8 ch	—	2 ch	3 ch (UART: 1 ch)	69	2.7 V	Available
LV	μPD78P0914	32K	6 ch	—	—	1 ch	8 ch	—	—	2 ch	54	4.5 V	Available

FUNCTION OVERVIEW

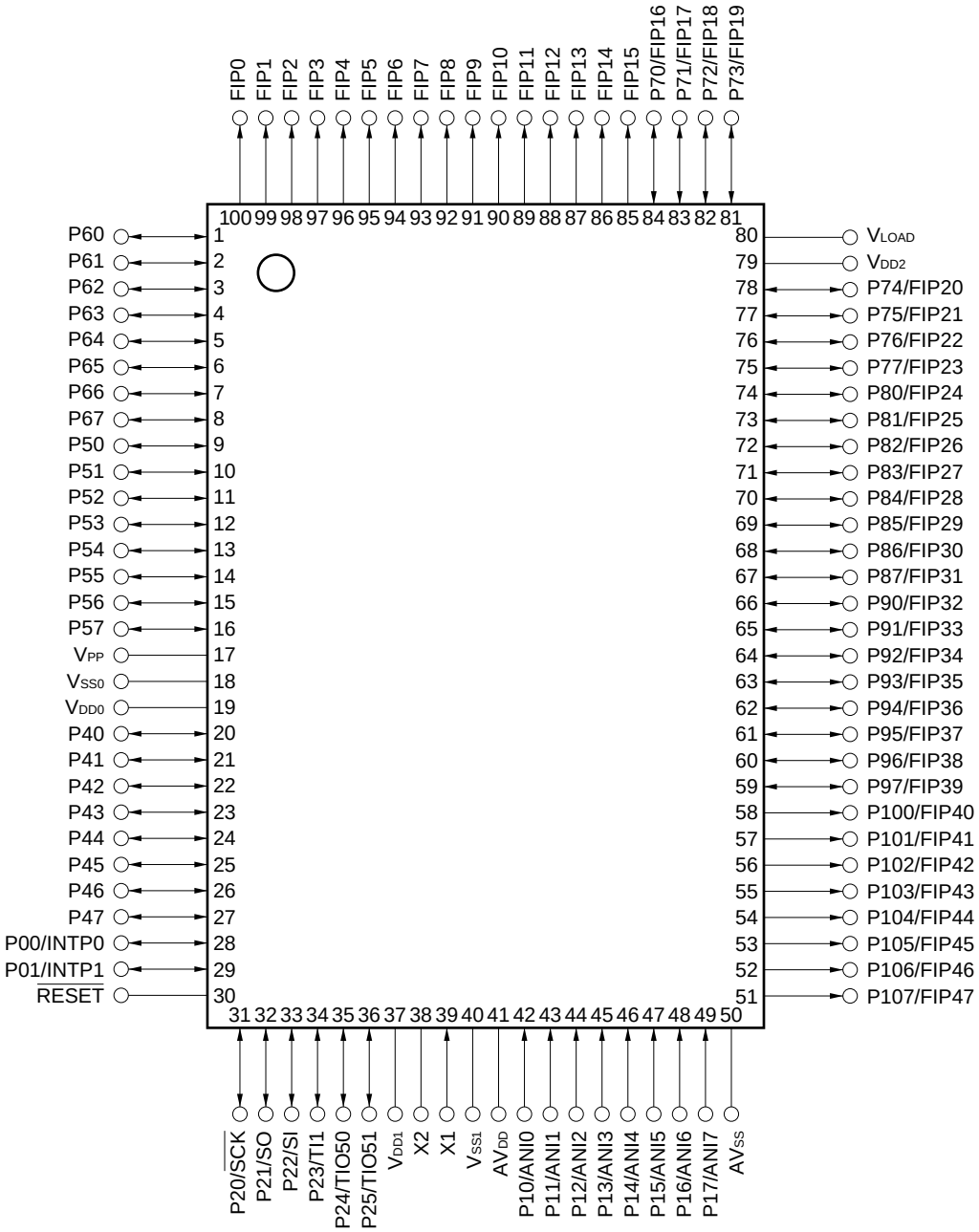
Item		Function
Internal memory	Flash memory	60 Kbytes[Note]
	High-speed RAM	1024 bytes
	Expansion RAM	512 bytes
	FIP display RAM	96 bytes
General-purpose register		8 bits x 32 registers (8 bits x 8 registers x 4 banks)
Instruction cycle		• On-chip instruction execution time variable function • 0.4 μs/0.8 μs/1.6 μs/3.2 μs/6.4 μs (@ 5.0-MHz operation with main system clock)
Instruction set		• Multiply/divide (8 bits x 8 bits, 16 bits ÷ 8 bits) • Bit manipulate (set, reset, test, Boolean operation)
I/O ports (including alternate function pins for FIP)		Total : 72 • CMOS inputs : 8 • CMOS I/Os : 16 • N-ch open-drain I/Os : 16 • P-ch open-drain I/Os : 24 • P-ch open-drain outputs : 8
FIP controller/driver		Total of display outputs : 48 • 10-mA display current : 16 • 3-mA display current : 32
A/D converter		• 8-bit resolution x 8 channels • Power supply voltage: AV_{DD} = 4.5 to 5.5 V
Serial interface		3-wired serial I/O mode: 1 channel
Timer		• 8-bit remote control timer : 1 channel • 8-bit PWM timer : 2 channels • Watchdog timer : 1 channel
Timer output		2 (8-bit PWM output is available)
Vectored-interrupt source	Maskable	Internal: 6, external: 4
	Non-maskable	Internal: 1
	Software	1
Power supply voltage		V_{DD} = 4.5 to 5.5 V
Package		100-pin plastic QFP (14 x 20 mm)

Note The flash memory capacity can be changed with the memory size switching register (IMS)

PIN CONFIGURATION (TOP VIEW)

• 100-pin plastic QFP (14 x 20 mm)

μPD78F0228GF-3BA



Cautions 1. Connect directly V_{PP} pin to V_{SS1} in nornmal operation mode.

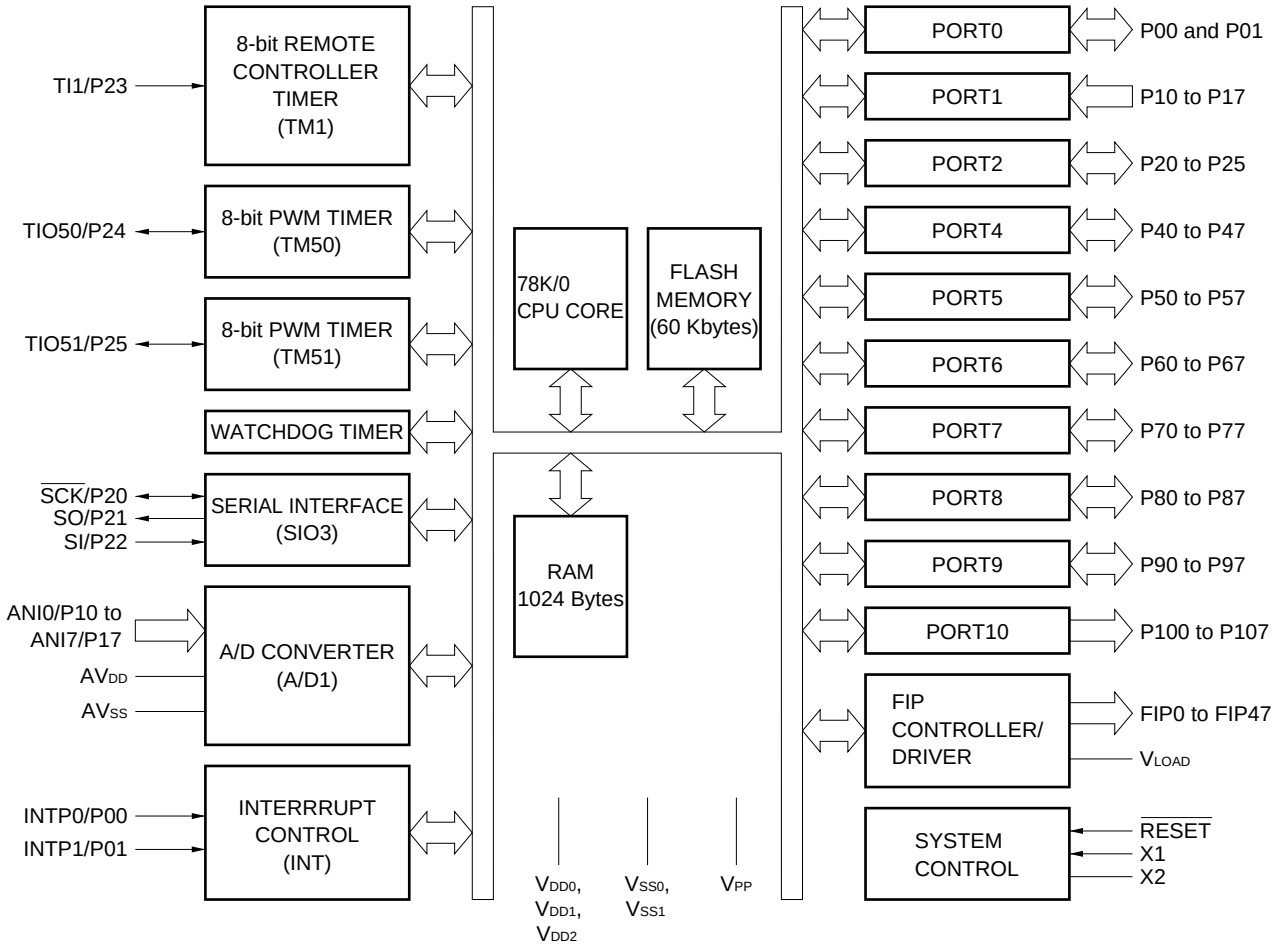
2. Connect AV_{DD} pin to V_{DD1}.

3. Connect AV_{SS} pin to V_{SS1}.

Remark When the μPD78F0228 is used in applications that require reduction of the noise from inside the microcontroller, the implementation of noise reduction measures, such as supplying voltage to V_{DD0} and V_{DD1} individually and connecting V_{SS0} and V_{SS1} to different ground lines, is recommended.

ANI0 to ANI7	:	Analog Input
AV_{DD}	:	Analog Power Supply
AV_{SS}	:	Analog Ground
FIP0 to FIP47	:	Fluorescent Indicator Panel
INTP0 and INTP1	:	Interrupt from Peripherals
P00 and P01	:	Port 0
P10 to P17	:	Port 1
P20 to P25	:	Port 2
P40 to P47	:	Port 4
P50 to P57	:	Port 5
P60 to P67	:	Port 6
P70 to P77	:	Port 7
P80 to P87	:	Port 8
P90 to P97	:	Port 9
P100 to P107	:	Port 10
$\overline{\text{RESET}}$	:	Reset
$\overline{\text{SCK}}$	:	Serial Clock
SI	:	Serial Input
SO	:	Serial Output
TI1	:	Timer Input
TIO50 and TIO51	:	Timer Input/Output
V_{DD0} to V_{DD2}	:	Power Supply
V_{LOAD}	:	Negative Power Supply
V_{PP}	:	Programming Power Supply
V_{SS0} and V_{SS1}	:	Ground
X1 and X2	:	Crystal

BLOCK DIAGRAM



CONTENTS

1. DIFFERENCES BETWEEN μPD78F0228 AND MASK ROM VERSION

The μPD78F0228 is a product provided with an internal flash memory which enables on-board program writing/erasing/rewriting.

The functions of the μPD78F0228, except those specified for flash memory, can be made the same as those of the mask ROM versions by setting the memory size switching rgister (IMS).

Table 1-1 shows the differences between the μPD78F0228 and the mask ROM versions.

Table 1-1. Differences between μPD78F0228 and Mask ROM Versions

Item	μPD78F0228	Mask ROM Version
Internal ROM structure	Flash memory	Mask ROM
Internal ROM capacity	60 Kbytes	μPD78F0226 : 48 Kbytes μPD78F0228 : 60 Kbytes
Internal ROM capacity changeability with memory size switching registers (IMS)	Changeable[Note]	Not changeable
IC pin	Not provided	Provided
V_{PP} pin	Provided	Not provided
Mask option with on-chip pull-up resistor in P50 to P57 and P60 to P67	Not provided	Provided
Mask option with on-chip pull-down resistor in P70 to P77, P80 to P87, and P100 to P107	Not provided	Provided

Note Flash memory is set to 60 Kbytes by $\overline{\text{RESET}}$ input.

2. PIN FUNCTION LIST

2.1 Port Pins (1/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P00	I/O	Port 0. 2-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	INTP0
P01				INTP1
P10 to P17	Input	Port 1. 8-bit input dedicated port.	Input	ANI0 to ANI7
P20	I/O	Port 2. 6-bit I/O port. Input/output can be specified bit-wise. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	$\overline{SCK}$
P21				SO
P22				SI
P23				TI1
P24				TIO50
P25				TIO51
P40 to P47	I/O	Port 4. 8-bit I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. When used as an input port, an on-chip pull-up resistor can be connected by software.	Input	—
P50 to P57	I/O	Port 5. N-ch open-drain 8-bit medium-voltage I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. A pull-up resistor can be incorporated bit-wise by mask option.	Input	—
P60 to P67	I/O	Port 6. N-ch open-drain 8-bit medium-voltage I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. A pull-up resistor can be incorporated bit-wise by mask option.	Input	—

2.1 Port Pins (2/2)

Pin Name	I/O	Function	After Reset	Alternate Function
P70 to P77	I/O	Port 7. P-ch open-drain 8-bit high-voltage I/O port. Input/output can be specified bit-wise. LEDs can be driven directly. A pull-down resistor can be incorporated bit-wise by mask option.	Input	FIP16 to FIP23
P80 to P87	I/O	Port 8. P-ch open-drain 8-bit high-voltage I/O port. Input/output can be specified bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.	Input	FIP24 to FIP31
P90 to P97	I/O	Port 9. P-ch open-drain 8-bit high-voltage I/O port. Input/output can be specified bit-wise. A pull-down resistor can be incorporated bit-wise by mask option.	Input	FIP32 to FIP39
P100 to P107	Output	Port 10. P-ch open-drain 8-bit high-voltage I/O port. A pull-down resistor can be incorporated bit-wise by mask option.	Output	FIP40 to FIP47

2.2 Non-port Pins

Pin Name	I/O	Function	After Reset	Alternate Function
INTP0	Input	Effective edge (rising edge, falling edge, or both rising and falling edges) can be specified. External interrupt request input.	Input	P00
INTP1				P01
$\overline{SCK}$	I/O	Serial interface serial clock I/O.	Input	P20
SO	Output	Serial interface serial data output.	Input	P21
SI	Input	Serial interface serial data input.	Input	P22
TI1	Input	8-bit remote control timer (TM1) timer input.	Input	P23
TIO50	I/O	8-bit PWM timer (TM50) capture trigger input/timer output.	Input	P24
TIO51	I/O	8-bit PWM timer (TM51) capture trigger input/timer output.	Input	P25
FIP0 to FIP15	Output	FIP controller/driver high-voltage withstand large current output.	Output	—
FIP16 to FIP23			Input	P70 to P77
FIP24 to FIP31				P80 to P87
FIP32 to FIP39				P90 to P97
FIP40 to FIP47				P100 to P107
V_{LOAD}	—	FIP controller/driver pull-down resistor connection.	—	—
$\overline{RESET}$	Input	System reset input.	—	—
X1	Input	Crystal connection for main system clock oscillation.	—	—
X2	—		—	—
ANI0 to ANI7	Input	A/D converter analog input.	Input	P10 to P17
AV_{DD}	—	A/D converter analog power supply (the same potential with V_{DD1}).	—	—
AV_{SS}	—	A/D converter ground potential (the same potential with V_{SS1}).	—	—
V_{DD0}	—	Positive power supply for ports.	—	—
V_{DD1}	—	Positive power supply except for ports, analog, and FIP controller/driver.	—	—
V_{DD2}	—	Positive power supply for FIP controller/driver.	—	—
V_{SS0}	—	Ground potential for ports.	—	—
V_{SS1}	—	Ground potential except for ports and analog.	—	—
V_{PP}	—	High-voltage applied during program writing/verifying. Connect directly to V_{SS1} pin in normal operation mode.	—	—

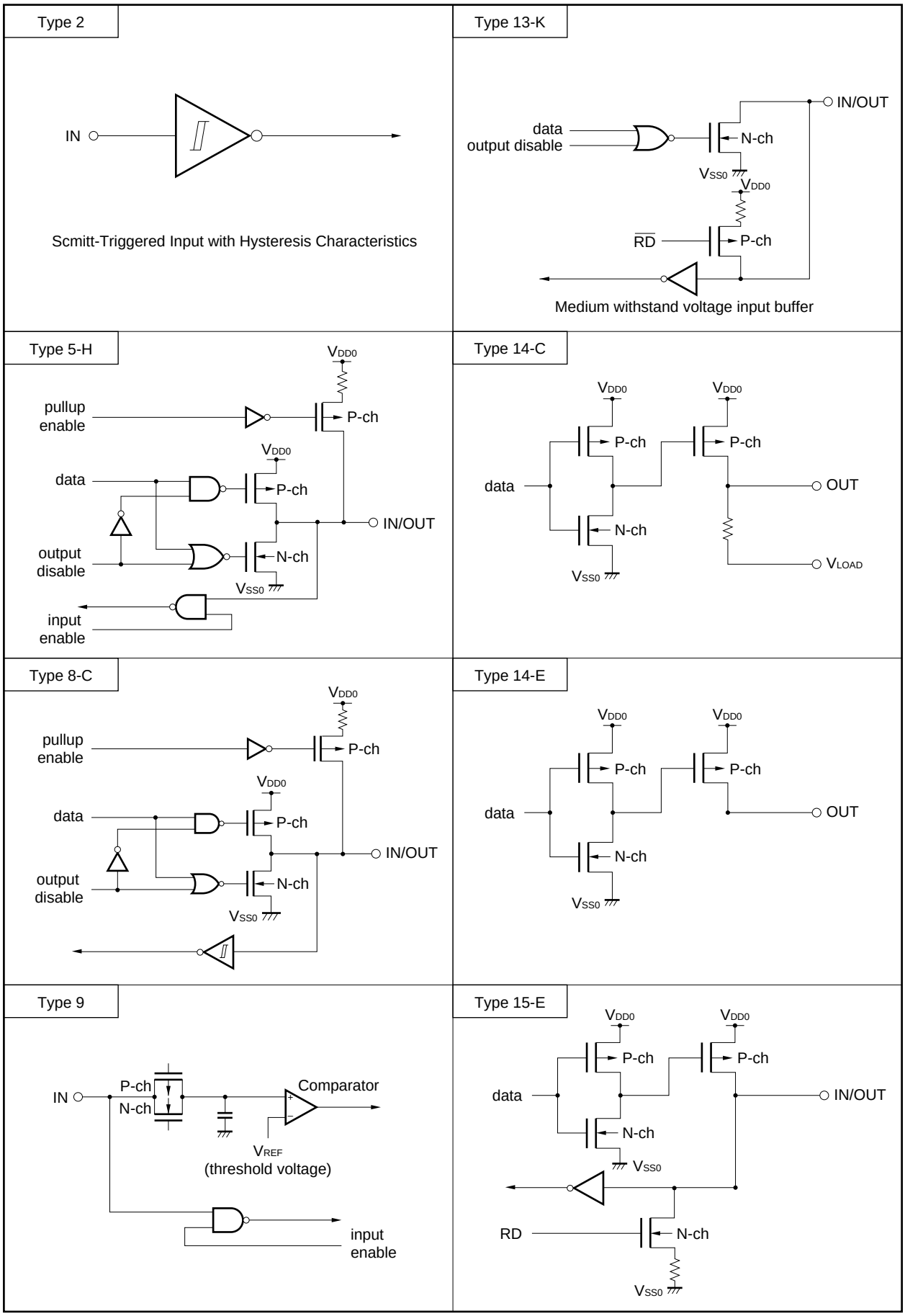
2.3 Pin I/O Circuits and Recommended Connection of Unused Pins

The I/O circuit type of each pin and the recommended connection of unused pins are shown in Table 2-1. For the I/O circuit configuration of each type, see Figure 2-1.

Table 2-1. Types of Pin I/O Circuits

Pin Name	I/O Circuit Type	I/O	Recommended Connection of Unused Pins
P00/INTP0	8-C	I/O	Individually connect to V_{SS0} via a resistor.
P01/INTP1			
P10/ANI0 to P17/ANI7	9	Input	
P20/$\overline{SCK}$	8-C	I/O	Individually connect to V_{DD0} or V_{SS0} via a resistor.
P21/SO	5-H		
P22/SI	8-C		
P23/TI1			
P24/TIO50			
P25/TIO51			
P40 to P47			
P50 to P57	13-K	I/O	Individually connect to V_{DD0} via a resistor.
P60 to P67			
P70/FIP16 to P77/FIP23	15-E	I/O	Individually connect to V_{DD0} or V_{SS0} via a resistor.
P80/FIP24 to P87/FIP31			
P90/FIP32 to P97/FIP39			
P100/FIP40 to P107/FIP47	14-E	Output	
FIP0 to FIP15	14-C	Output	
$\overline{RESET}$	2	Input	—
AV_{DD}	—	—	Connect to V_{DD1}.
AV_{SS}			Connect to V_{SS1}.
A_{LOAD}			
V_{PP}			Connect to V_{SS1} directly.

Figure 2-1. Pin I/O Circuits



3. MEMORY SIZE SWITCHING REGISTER (IMS)

The register prevents a part of internal memory from being used by software. The memory mapping can be made the same as that of mask ROM versions with different types of internal memory (ROM) by setting the memory size switching register (IMS).

The IMS is set with an 8-bit memory manipulation instruction.

$\overline{\text{RESET}}$ input sets the IMS to CCH.

Figure 3-1. Format of Memory Size Switching Register

Symbol	7	6	5	4	3	2	1	0	Address	At reset	R/W
IMS	RAM2	RAM1	RAM0	0	ROM3	ROM2	ROM1	ROM0	FFF0H	CCH	R/W

ROM3	ROM2	ROM1	ROM0	Selection of internal ROM capacity
1	1	0	0	48 Kbytes
1	1	1	1	60 Kbytes
Other than above				Setting prohibited

RAM2	RAM1	RAM0	Selection of internal high-speed RAM capacity
1	1	0	1024 bytes
Other than above			Setting prohibited

Table 3-1 shows the IMS set value to make the memory mapping the same as those of mask ROM versions.

Table 3-1. Set Value of Memory Size Switching Register

Target mask ROM versions	IMS set value
μPD780226	CCH
μPD780228	CFH

4. FLASH MEMORY PROGRAMMING

The μPD78F0228 can write to the flash memory while mounted on the target system board. To perform write operations, connect the dedicated flash programmer (Flashpro) to both the host machine and the target system.

In addition, to write to the flash memory it can be performed on the flash-writing adapter connected to Flashpro.

Remark Flashpro is a product of Naito Densei Machida Seisakusho Co., Ltd.

4.1 Selection of Transmission Method

Write operations to the flash memory are performed using Flashpro in the serial transmission mode. Choose a proper transmission method out of the ones listed in Table 4-1 to perform write operations. When selecting the transmission mode, use the format illustrated in Figure 4-1. Select the transmission mode according to the number of V_{PP} pulses shown in Table 4-1.

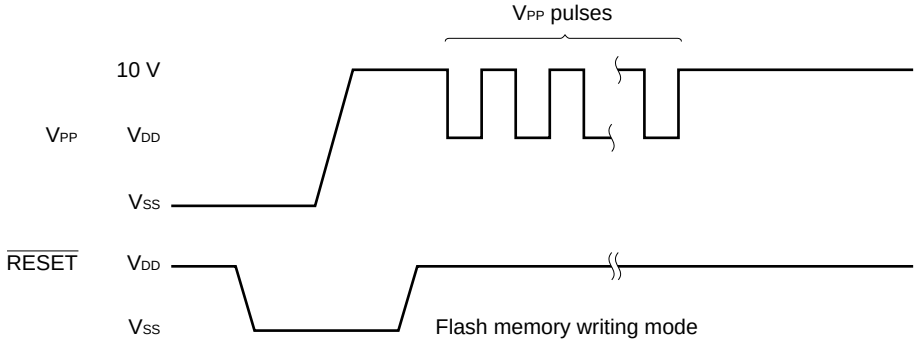
Table 4-1. List of Transmission Methods

Transmission method	No. of channels	Pins	V_{PP} pulses
3-wire serial I/O	1	$\overline{SCK}$/P20 SO/P21 SI/P22	0
Pseudo 3-wire serial I/O[Note]	1	P40 (serial clock I/O) P41 (serial data output) P42 (serial data input)	12

Note Performs serial transmission by controlling ports with software.

Caution Be sure to select the transmission mode according to the number of V_{PP} pulses shown in Table 4-1.

Figure 4-1. Format of Transmission Method Selection



4.2 Flash Memory Programming Functions

Operations such as writing to the flash memory are performed by various commands/data transmission and reception operations according to the selected transmission method. Table 4-2 describes the main flash memory programming functions.

Table 4-2. Main Flash Memory Programming Functions

Function	Description
Reset	Used in cancellation of writing and transmission synchronization detection.
One shot verify	Compares the contents of the entire memory and the input data.
One shot erase	Erases the contents of the entire memory.
One shot blank check	Checks that the entire memory has been deleted.
High-speed writing	Writes to the flash memory based on writing-starting address and the number of writing data (bytes)
Continuous writing	Writes continuously based on information input at high-speed writing.
Status	Used to check the current operation mode and the end of operation.
Oscillation frequency setting	Inputs information of frequency of resonator.
Erase time setting	Inputs the time-length to erase the contents of the memory.
Silicon signature reading	Outputs the device name, memory capacity, and information of device block.

4.3 Connection to Flashpro

The connection of the Flashpro and the μPD78F0228 differs according to the transmission method. The connection for each transmission method is shown in either Figure 4-2 and 4-3.

Figure 4-2. Connection to Flashpro in 3-wire serial I/O Mode

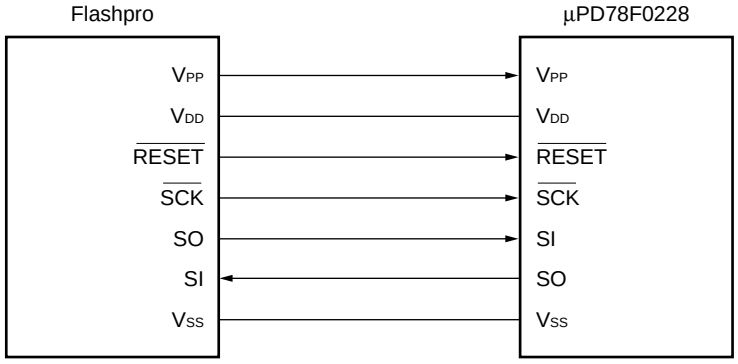
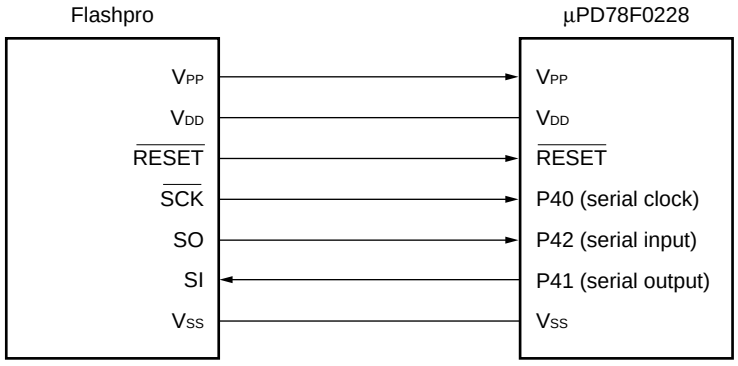
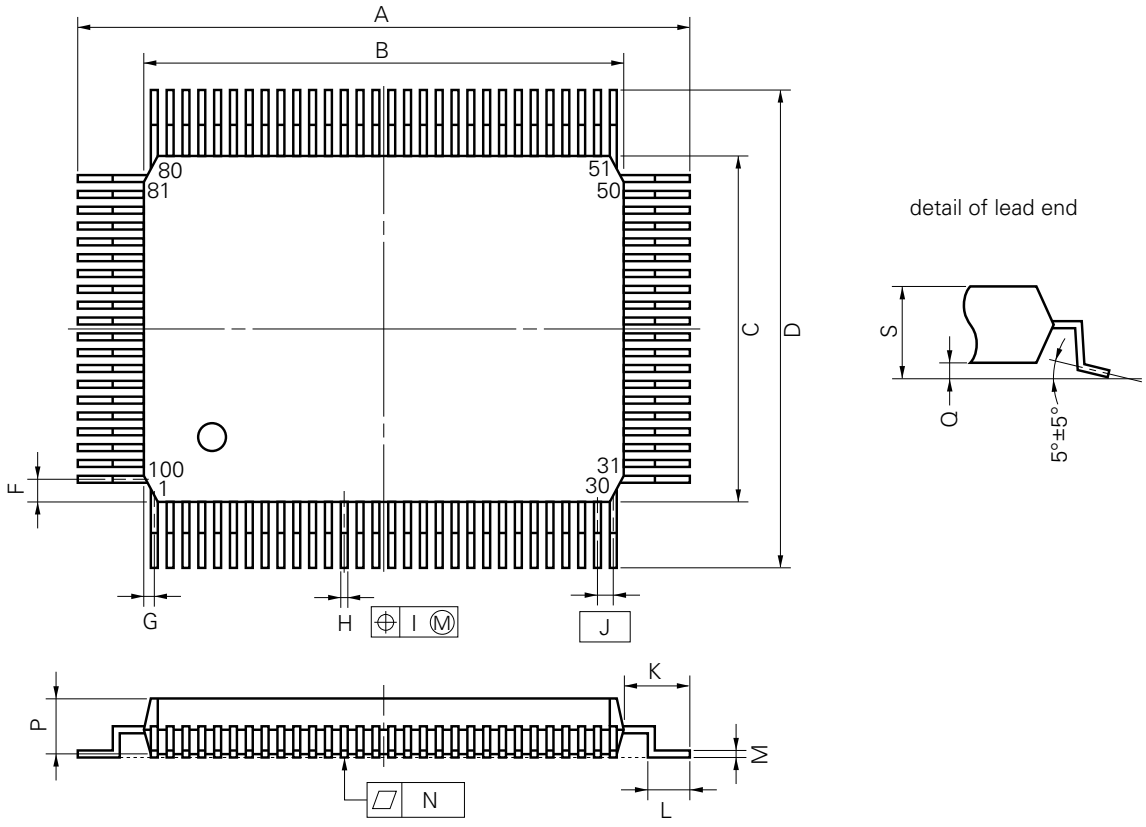


Figure 4-3. Connection to Flashpro in Pseudo 3-wire serial I/O Mode



5. PACKAGE DRAWING

100 PIN PLASTIC QFP (14 × 20)



P100GF-65-3BA1-2

NOTE

Each lead centerline is located within 0.15 mm (0.006 inch) of its true position (T.P.) at maximum material condition.

ITEM	MILLIMETERS	INCHES
A	23.6±0.4	0.929±0.016
B	20.0±0.2	$0.795^{+0.009}_{-0.008}$
C	14.0±0.2	$0.551^{+0.009}_{-0.008}$
D	17.6±0.4	0.693±0.016
F	0.8	0.031
G	0.6	0.024
H	0.30±0.10	$0.012^{+0.004}_{-0.005}$
I	0.15	0.006
J	0.65 (T.P.)	0.026 (T.P.)
K	1.8±0.2	$0.071^{+0.008}_{-0.009}$
L	0.8±0.2	$0.031^{+0.009}_{-0.008}$
M	$0.15^{+0.10}_{-0.05}$	$0.006^{+0.004}_{-0.003}$
N	0.10	0.004
P	2.7	0.106
Q	0.1±0.1	0.004±0.004
S	3.0 MAX.	0.119 MAX.

APPENDIX A DEVELOPMENT TOOLS

The following development tools are available for system development using the μPD78F0228.

Language Processing Software

RA78K/0 Notes 1, 2, 3, 4	78K/0 Series common assembler package
CC78K/0 Notes 1, 2, 3, 4	78K/0 Series common C compiler package
DF780228 Notes 1, 2, 3, 4, 8	μPD780228 Subseries common device file
CC78K/0-L Notes 1, 2, 3, 4	78K/0 Series common C compiler library source file

Flash Memory Writing Tools

Flashpro	Dedicated flash memory writer. The Flashpro is a product of Naito Densei Machida Seisakusho Co., Ltd.
PA-FLASH100GF (temporary name) Note 8	Adapter to write data to the flash memory; the product of Naito Densei Machida Seisakusho Co., Ltd.

Debugging Tools

IE-780000-SL Note 8	75XL, 78K/0S, 78K/0, and 78K/IV Series common in-circuit emulator
IE-78K0-SL-EM Note 8	78K/0 Series common CPU core board
IE-78K0-SL-P01 Note 8	I/O board to emulate the μPD780228 Subseries product
IE-780228-SL-EM4 Note 8	Probe board to emulate the μPD780228 Subseries product
EP-100GF-SL Note 8	Emulation probe for 100-pin plastic QFP (GF-3BA type)
EV-9200GF-100	Socket to be equipped on target system board produced for 100-pin plastic QFP (GF-3BA type)
SM78K0 Notes 5, 6, 7	78K/0 Series common system simulator
ID78K0 Notes 4, 5, 6, 7	IE-780000-SL integrated debugger
DF780228 Notes 4, 5, 6, 7, 8	μPD780228 Subseries device file

Real-Time OSs

RX78K/0 Notes 1, 2, 3, 4	78K/0 Series real-time OS
MX78K0 Notes 1, 2, 3, 4	78K/0 Series OS

Notes 1. PC-9800 series (MS-DOS™) based
2. IBM PC/AT™ and compatibles (PC DOS™/IBM DOS™/MS-DOS) based
3. HP9000 series 300™ (HP-UX™) based
4. HP9000 series 700™ (HP-UX) based, SPARCstation™ (SunOS™) based, EWS4800 series (EWS-UX/V) based
5. PC-9800 series (MS-DOS + Windows™) based
6. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based
7. NEWS™ (NEWS-OS™) based
8. Under development

Fuzzy Inference Development Support Systems

FE9000 Note 1, FE9200 Note 3	Fuzzy knowledge data creation tool
FT9080 Note 1, FT9085 Note 2	Translator
FI78K0 Notes 1, 2	Fuzzy inference module
FD78K0 Notes 1, 2	Fuzzy inference debugger

Notes 1. PC-9800 series (MS-DOS™) based

2. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS) based

3. IBM PC/AT and compatibles (PC DOS/IBM DOS/MS-DOS + Windows) based

Remark RA78K/0, CC78K/0, SM78K0, ID78K0, and RX78K/0 are used in combination with DF780228.

APPENDIX B RELATED DOCUMENTS

Device Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
μPD780228 Subseries User's Manual	Planned	Preparing
μPD780226, 780228 Preliminary Product Information	Planned	U11797J
μPD78F0228 Preliminary Product Information	This manual	U11971J
μPD780228 Subseries Special Function Register Table	—	Planned
78K/0 Series User's Manual Instructions	IEU-1372	IEU-849
78K/0 Series Instruction Table	—	U10903J
78K/0 Series Instruction Set	—	U10904J

Development Tool Related Documents (User's Manual)

Document Name		Document No. (English)	Document No. (Japanese)
RA78K Series Assembler Package	Operation	EEU-1399	EEU-809
	Language	EEU-1404	EEU-815
RA78K Series Structured Assembler Preprocessor		EEU-1402	EEU-817
CC78K Series C Compiler	Operation	EEU-1280	EEU-656
	Language	EEU-1284	EEU-655
CC78K0 C Compiler	Operation	U11517E	U11517J
	Language	U11518E	U11518J
CC78K/0 C Compiler Application Note	Programming know-how	EEA-1208	EEA-618
CC78K Series Library Source File		—	EEU-777
IE-780000-SL		Planned	Planned
IE-78K0-SL-EM		Planned	Planned
IE-78K0-SL-P01		Planned	Planned
IE-780228-SL-EM4		Planned	Planned
EP-100GF-SL		Planned	Planned
SM78K0 System Simulator Windows-based	Reference	U10181E	U10181J
SM78K Series System Simulator	External parts user open interface specifications	U10092E	U10092J
ID78K0 Integrated Debugger EWS-based	Reference	U11151E	U11151J
ID78K0 Integrated Debugger PC-based	Reference	U11539E	U11539J
ID78K0 Integrated Debugger Windows-based	Guide	U11649E	U11649J

Caution The above related documents are subject to change without notice. Be sure to use the latest documents when starting design.

Embedded Software Related Documents (User's Manuals)

Document Name		Document No. (English)	Document No. (Japanese)
78K/0 Series Real-time OS	Basics	—	U11537J
	Installation	—	U11536J
	Technical	—	U11538J
78K/0 Series OS MX78K0	Basics	EEU-1532	EEU-5010
Fuzzy Knowledge Data Creation Tool		EEU-1438	EEU-829
78K/0, 78K/II, 87AD Series Fuzzy Inference Development Support System Translator		EEU-1444	EEU-862
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Module		EEU-1441	EEU-858
78K/0 Series Fuzzy Inference Development Support System Fuzzy Inference Debugger		EEU-1458	EEU-921

Other Related Documents

Document Name	Document No. (English)	Document No. (Japanese)
IC Package Manual	C10943X	
Semiconductor Device Mounting Technology Manual	C10535E	C10535J
Quality Grades on NEC Semiconductor Devices	C11531E	C11531J
NEC Semiconductor Device Reliability/Quality Control System	C10983E	C10983J
Electrostatic Discharge (ESD) Test	IEI-1201	MEM-539
Guide to Quality Assurance for Semiconductor Devices	MEI-1202	MEI-603
Microcomputer Product Series Guide – Third Party	—	U11416J

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NOTES FOR CMOS DEVICES

① PRECAUTION AGAINST ESD FOR SEMICONDUCTORS

Note: Strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it once, when it has occurred. Environmental control must be adequate. When it is dry, humidifier should be used. It is recommended to avoid using insulators that easily build static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work bench and floor should be grounded. The operator should be grounded using wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with semiconductor devices on it.

② HANDLING OF UNUSED INPUT PINS FOR CMOS

Note: No connection for CMOS device inputs can be cause of malfunction. If no connection is provided to the input pins, it is possible that an internal input level may be generated due to noise, etc., hence causing malfunction. CMOS device behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using a pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND with a resistor, if it is considered to have a possibility of being an output pin. All handling related to the unused pins must be judged device by device and related specifications governing the devices.

③ STATUS BEFORE INITIALIZATION OF MOS DEVICES

Note: Power-on does not necessarily define initial status of MOS device. Production process of MOS does not define the initial operation status of the device. Immediately after the power source is turned ON, the devices with reset function have not yet been initialized. Hence, power-on does not guarantee out-pin levels, I/O settings or contents of registers. Device is not initialized until the reset signal is received. Reset operation must be executed immediately after power-on for devices having reset function.

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- Device availability
- Ordering information
- Product release schedule
- Availability of related technical literature
- Development environment specifications (for example, specifications for third-party tools and components, host computers, power plugs, AC supply voltages, and so forth)
- Network requirements

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