General Description

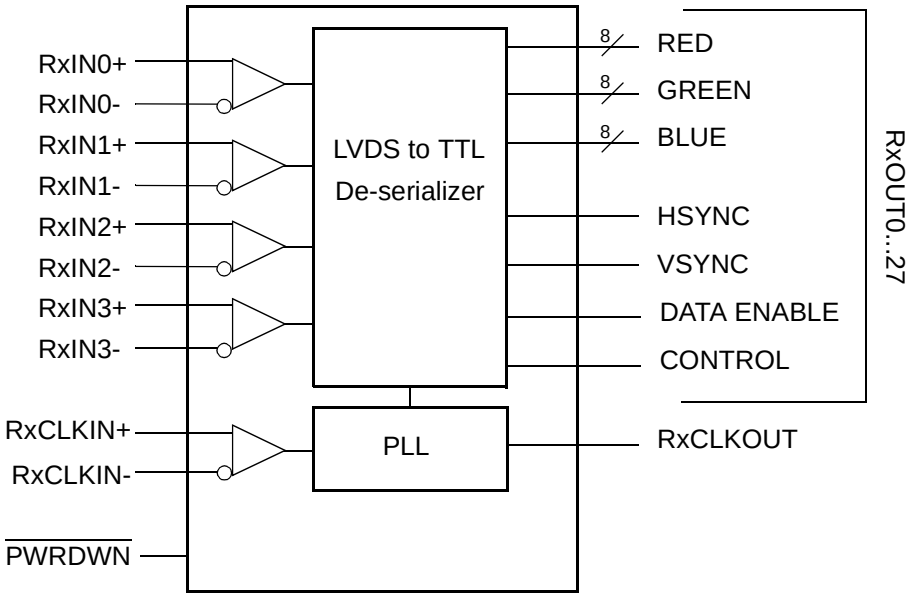
The VP386 is an ideal LVDS receiver that converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data with bandwidth up to 2.8 Gbps throughput or 350 Mbytes per second.

This chip is an ideal means to solve EMI and cable size problems associated with wide, high-speed TTL interfaces through very low-swing LVDS signals.

Features

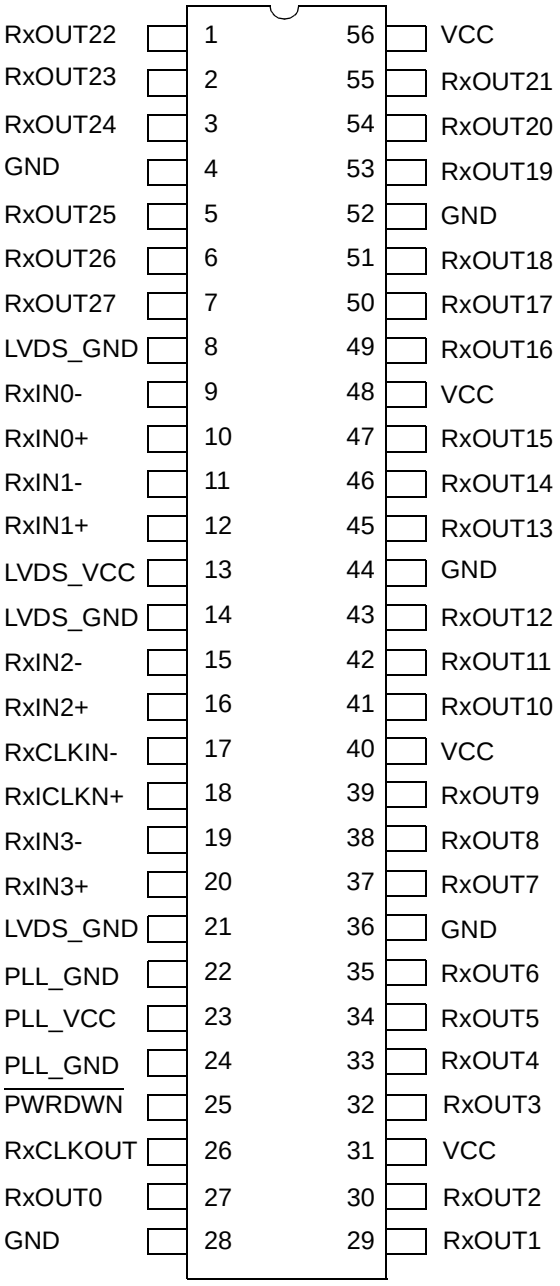
- Wide clock frequency range from 20 MHz to 100 MHz
- Pin compatible with the National DS90CF386, THine THC63LVDF84, TISN65LVDS94
- Converts 4-pair LVDS data streams into parallel 28 bits of CMOS/TTL data
- Fully spread spectrum compatible
- LVDS voltage swing of 350 mV for low EMI
- On-chip PLL requires no external components
- Low-power CMOS design
- Falling edge clock triggered outputs
- Power-down control function
- Compatible with TIA/EIA-644 LVDS standards
- Packaged in a 56-pin TSSOP (Pb free available)

Block Diagram



VP386

Pin Assignment



56-pin TSSOP
VP386

Pin Descriptions

Pin No.	Pin Name	Pin Type	Pin Description
1	RxOUT22	OUT	Data outputs on pins (RxOUT0..27)
2	RxOUT23		
3	RxOUT24		
4	GND	Ground	Digital ground
5	RxOUT25	OUT	Data outputs on pins (RxOUT0..27)
6	RxOUT26		
7	RxOUT27		
8	LVDS_GND	Ground	Analog ground
9	RxIN0-	LVDS IN	LVDS input (-)
10	RxIN0+		LVDS input (+)
11	RxIN1-		LVDS input (-)
12	RxIN1+		LVDS input (+)
13	LVDS_VCC	Power	Analog power
14	LVDS_GND	Ground	Analog ground
15	RxIN2-	LVDS IN	LVDS input (-)
16	RxIN2+		LVDS input (+)
17	RxCLKIN-		LVDS input (-)
18	RxCLKIN+		LVDS input (+)
19	RxIN3-		LVDS input (-)
20	RxIN3+		LVDS input (+)
21	LVDS_GND	Ground	Analog ground
22	PLL_GND		PLL ground
23	PLL_VCC	Power	PLL power
24	PLL_GND	Ground	PLL ground
25	$\overline{\text{PWRDWN}}$	IN	Power-down control input. H: Nomal L: Power down, all ouputs are pulled low.
26	RxCLKOUT	OUT	Clock output
27	RxOUT0		Data outputs on pins (RxOUT0..27)
28	GND	Ground	Digital ground
29	RxOUT1	OUT	Data outputs on pins (RxOUT0..27)
30	RxOUT2		
31	VCC	Power	Digital power
32	RxOUT3	OUT	Data outputs on pins (RxOUT0..27)
33	RxOUT4		
34	RxOUT5		

Pin No.	Pin Name	Pin Type	Pin Description
35	RxOUT6	OUT	Data outputs on pins (RxOUT0..27)
36	GND	Ground	Digital ground
37	RxOUT7	OUT	Data outputs on pins (RxOUT0..27)
38	RxOUT8		
39	RxOUT9		
40	VCC	Power	Digital power
41	RxOUT10	OUT	Data outputs on pins (RxOUT0..27)
42	RxOUT11		
43	RxOUT12		
44	GND	Ground	Digital ground
45	RxOUT13	OUT	Data outputs on pins (RxOUT0..27)
46	RxOUT14		
47	RxOUT15		
48	VCC	Power	Digital power
49	RxOUT16	OUT	Data outputs on pins (RxOUT0..27)
50	RxOUT17		
51	RxOUT18		
52	GND	Ground	Digital ground
53	RxOUT19	OUT	Data outputs on pins (RxOUT0..27)
54	RxOUT20		
55	RxOUT21		
56	VCC	Power	Digital power

Absolute Maximum Ratings

Item	Rating[1]
Supply Voltage, VCC	-0.3 V to +4 V
CMOS/TTL Output Voltage	-0.3 V to (VCC+0.3 V)
LVDS Receiver Input Voltage	-0.3 V to (VCC+0.3 V)
Ambient Operating Temperature	0 to +70°C
Storage Temperature	-65 to +150°C
Junction Temperature	150°C
Soldering Temperature (10 seconds max.)	260°C
Maximum Package Power	1.61 W (VP386)
Package Derating	12.4 mW/℃ above +25℃
	15 mW/℃ above +25℃

1. Stresses greater than those listed under Absolute Maximum Ratings may cause permanent damage to the device. This is a stress rating only and functional operation of the device at these or any other conditions above those indicated in the operational sections of this specification is not implied. Exposure to absolute maximum rating conditions for extended periods may affect reliability.

Recommended Operation Conditions

Parameter	Min.	Typ.	Max.	Units
Ambient Operating Temperature (Ta)	0	25	70	°C
3.3 V Supply Voltage (VCC)	3	3.3	3.6	V
Receiver Input Range (V_{IN})	0		2.4	V
Supply Noise Voltage (V_N)			100	mVpp

Electrical Characteristics

VDD=3.3 V ±10%, Ambient temperature 0 to 70°C

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
CMOS/TTL DC Specifications						
Input High Voltage	V_{IH}		2.0		VCC	V
Input Low Voltage	V_{IL}		GND		0.8	V
Output High Voltage	V_{OH}	I_{OH} = -0.4 mA	2.7	3.3	VCC	V
Output Low Voltage	V_{OL}	I_{OL} = 2 mA		0.06	0.3	V
Input Clamp Voltage	V_{CL}	I_{CL} = -18mA		-0.79	-1.5	V
Input Current	I_{IN}	VCC			±15	µA
		0V			±10	
Output Short Circuit Current	I_{OS}	V_{OUT} = 0V			-60	mA
LVDS Receiver DC Specifications						
Differential Input High Threshold	V_{TH}	V_{CM} = +1.2 V			+100	mV
Differential Input Low Threshold	V_{TL}		-100			mV
Input Current	I_{IN}	V_{IN} = +2.4 V, VCC = 3.6 V			±10	µA
		V_{IN} = 0V, VCC = 3.6 V			±15	µA
Receiver Supply Current						
Receiver Supply Current (worst case)	I_{CCRW}	C_L = 8 pF, f = 65 MHz, worst case pattern			220	mA
		C_L = 8 pF, f = 100 MHz, worst case pattern			240	mA
Receiver Supply Current (16 Grayscale)	I_{CCRG}	C_L= 8 pF, f = 65 MHz, 16 Grayscale pattern			125	mA
		C_L= 8 pF, f = 100 MHz, 16 Grayscale pattern			140	mA
Receiver Supply Current (Power Down)	I_{CCRZ}	Power_Down = Low, Receiver outputs stay low during Power-down mode		140	400	µA
Receiver Switching Characteristics						
CMOS/TTL Low-to-High Transition Time	CLHT	20% to 80% VCC, C_L= 8 pF		2	3.5	ns
CMOS/TTL High-to-Low Transition Time	CHLT	80% to 20% VCC, C_L= 8 pF		1.8	3.5	ns
CLKOUT period	RCOP		10	T	50	ns
CLKOUT High Time	RCOH			4T/7		ns
CLKOUT Low Time	RCOL			3T/7		ns
Data Setup to CLKOUT	RSRC		0.35T-0.3			ns
Data Hold to CLKOUT	RHRC		0.45T-1.6			ns

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
RCK+/- to CLKOUT Delay	RCCD	25°C / 3.3 V, 85MHz		14.6		ns
Receiver PLL Setup Time	RPLLS				10	ms
Receiver Power Down Delay	RPDD				1	µs
Receiver Input Strobe Position for Bit0	RSPos0	f = 100 MHz, T = 10 ns	-0.25	0	0.25	ns
Receiver Input Strobe Position for Bit1	RSPos1		T/7-0.25	T/7	T/7+0.25	ns
Receiver Input Strobe Position for Bit2	RSPos2		2T/7-0.25	2T/7	2T/7+0.25	ns
Receiver Input Strobe Position for Bit3	RSPos3		3T/7-0.25	3T/7	3T/7+0.25	ns
Receiver Input Strobe Position for Bit4	RSPos4		4T/7-0.25	4T/7	4T/7+0.4	ns
Receiver Input Strobe Position for Bit5	RSPos5		5T/7-0.25	5T/7	5T/7+0.25	ns
Receiver Input Strobe Position for Bit6	RSPos6		6T/7-0.25	6T/7	6T/7+0.25	ns
RxIn Skew Margin (see note and Figure 8)	Rskm	f = 100 MHz, T = 10 ns	250			ps
		f = 65 MHz, T = 15.38 ns	500			ps

Note: The skew margins mean the maximum timing tolerance between the clock and data channel when the receiver still works well. This margin takes into acount the receiver input setup and hold time, and internal clock jitter (i.e., internal data sampling window - RSPos). Thyis margin allows for LVDS transmitter pulse position, interconnect skew, inter-symbol interference and intrinsic channel mismatch which will cause the skew between clock (RC+ and RCK-) and data (RX[n]+ and RX[n]- ; n =0, 1, 2, 3) channels.

Thermal Characteristics

Parameter	Symbol	Conditions	Min.	Typ.	Max.	Units
Thermal Resistance Junction to Ambient	θ_{JA}	Still air		84		°C/W
	θ_{JA}	1 m/s air flow		76		°C/W
	θ_{JA}	2 m/s air flow		67		°C/W
Thermal Resistance Junction to Case	θ_{JA}			50		°C/W

Timing Diagrams

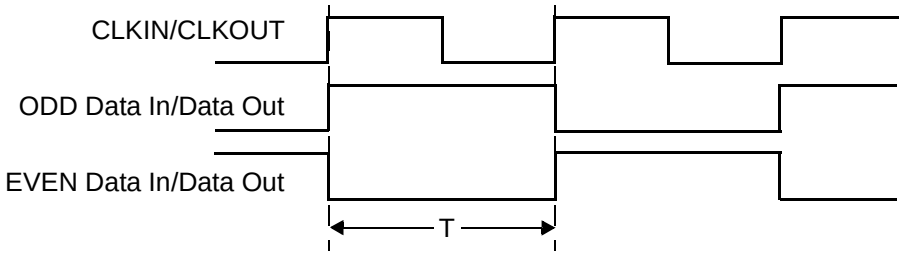


Figure 1. "Worst Case" Test Pattern

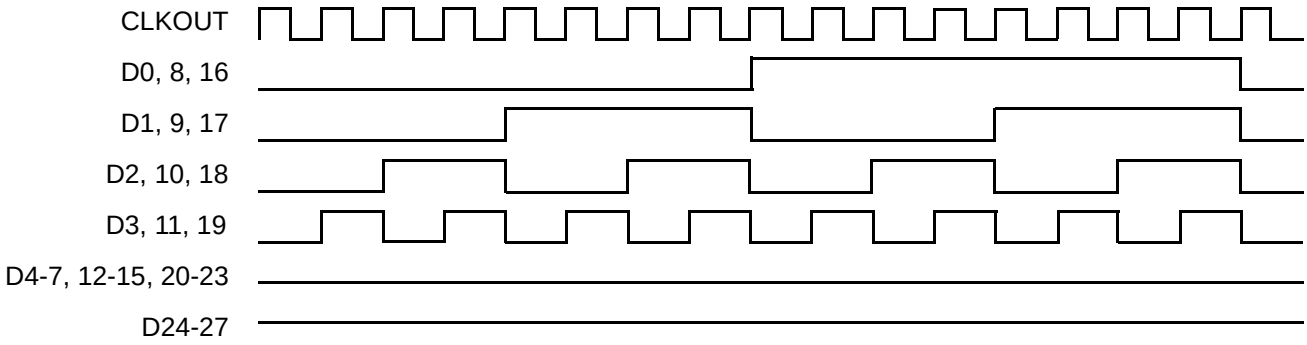


Figure 2. 16-Grayscale Test-Pattern Waveforms

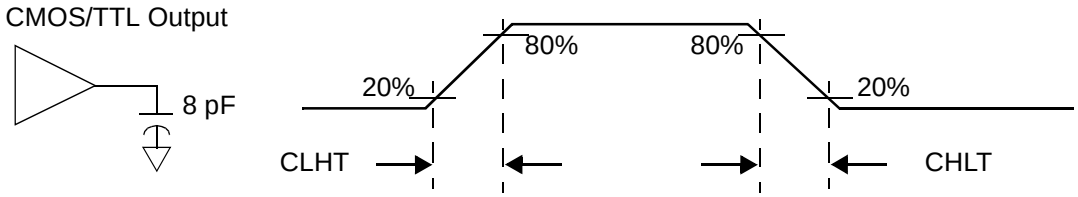


Figure 3. VP386 CMOS/TTL Output Load and Transition Time

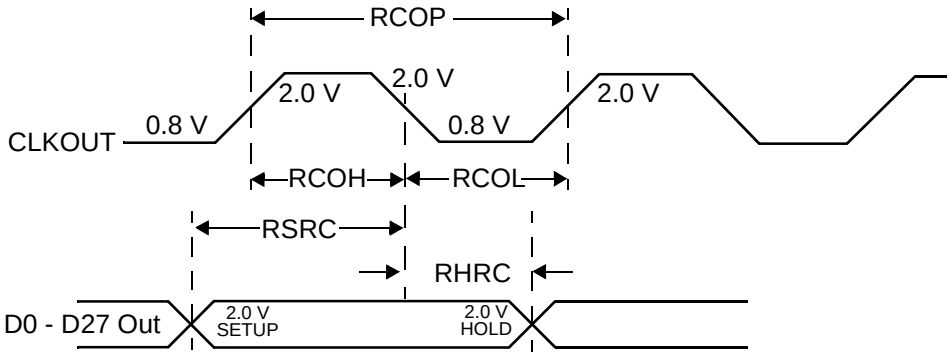


Figure 4. VP386 SETUP/HOLD and High/Low Times

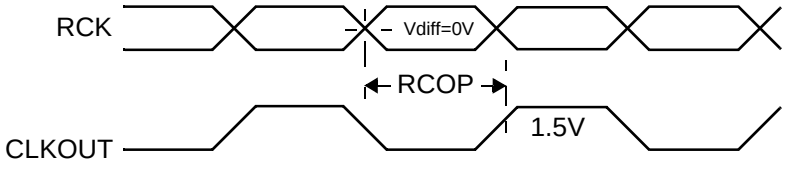


Figure 5. VP386 Clock In to Clock Out Delay

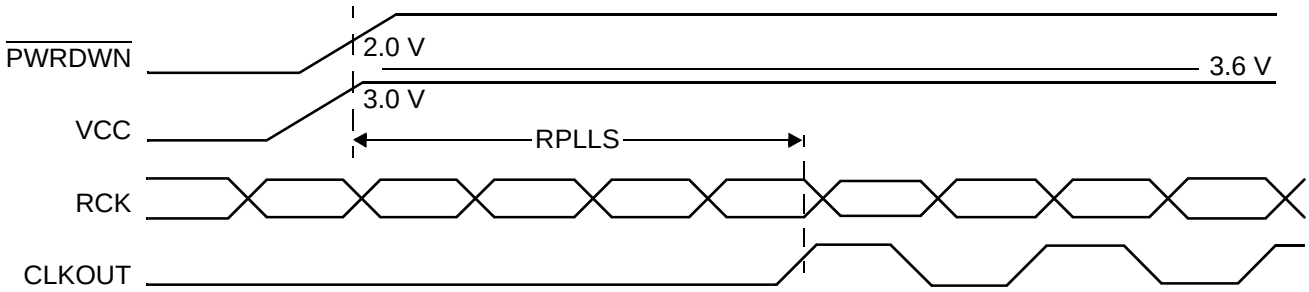


Figure 6. VP386 Phase Lock Loop Set Time

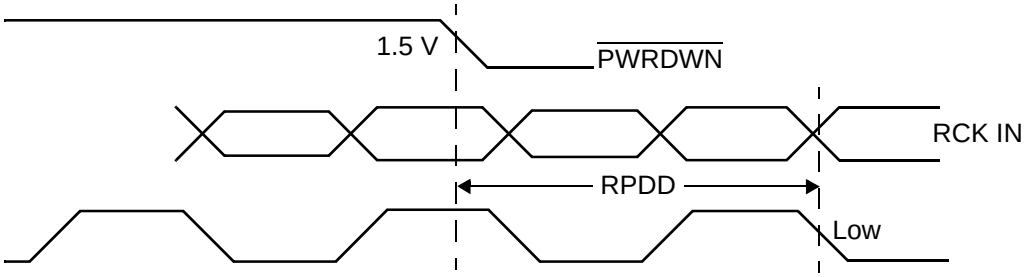


Figure 7. VP386 Power Down Delay

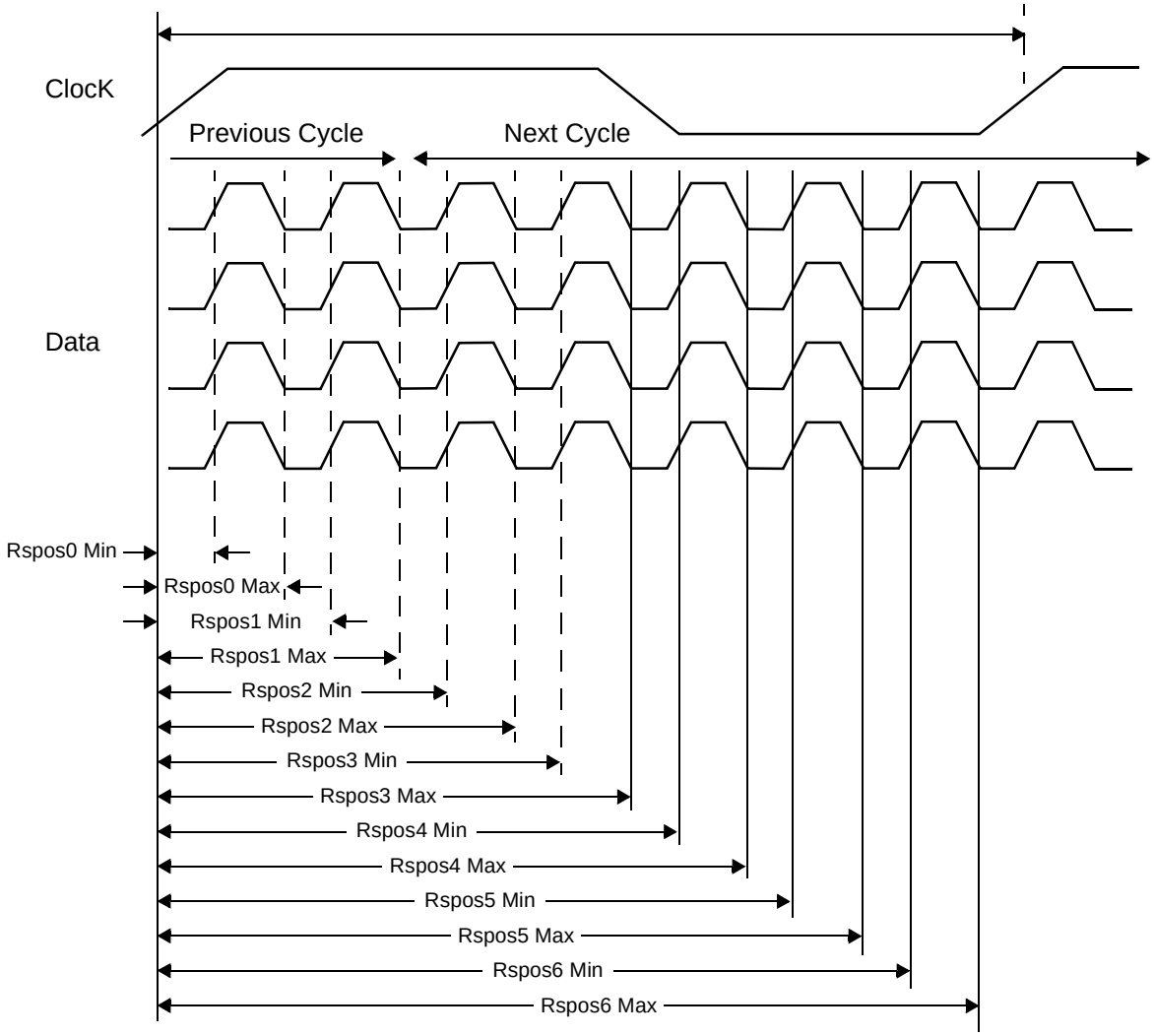


Figure 8. VP386 LVDS Input Strobe Position

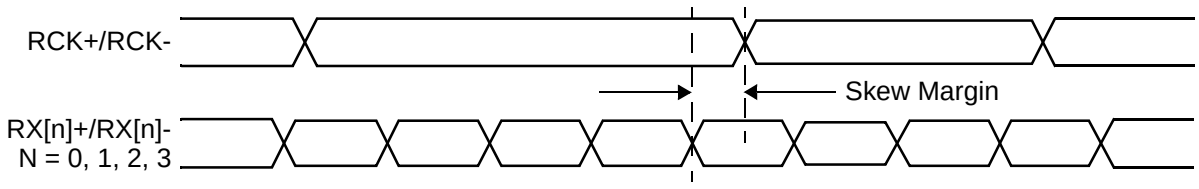
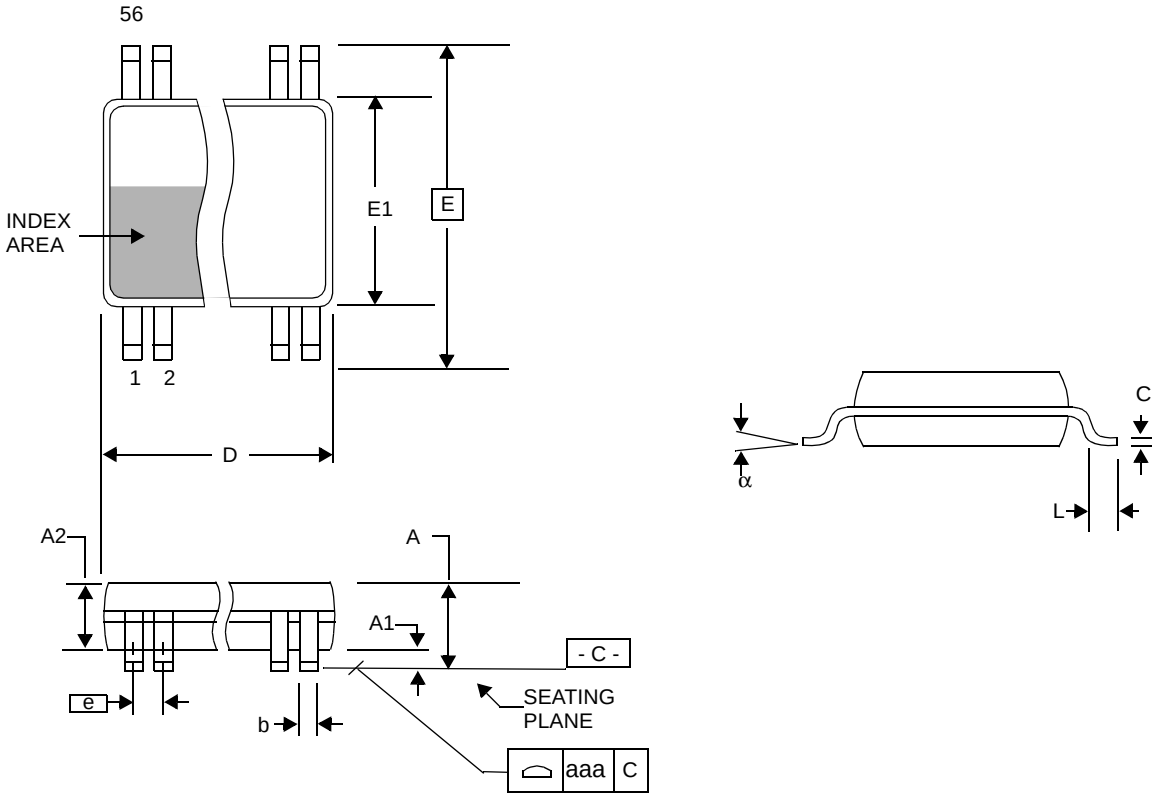


Figure 9. Receiver Input Skew Margin

Package Outline and Package Dimensions (56-pin TSSOP)

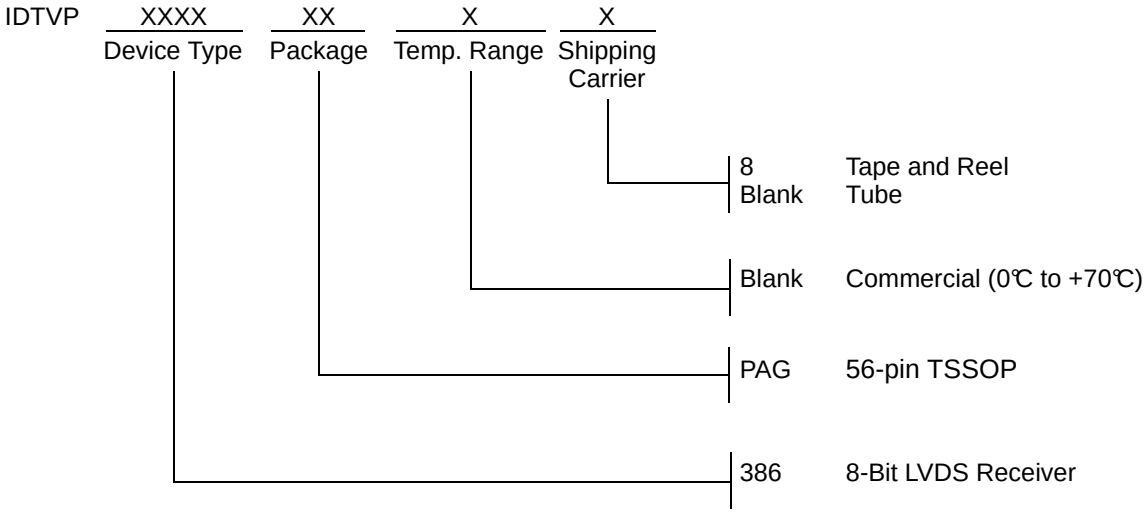
Package dimensions are kept current with JEDEC Publication No. 95



SYMBOL	In Millimeters COMMON DIMENSIONS		In Inches[1] COMMON DIMENSIONS	
	MIN	MAX	MIN	MAX
A	—	1.20	—	.047
A1	0.05	0.15	.002	.006
A2	0.80	1.05	.0032	.041
b	0.17	0.27	.007	.011
C	0.09	0.20	.0035	.008
D	13.90	14.10	.547	.555
E	8.10 BASIC		.319 BASIC	
E1	6.00	6.20	.236	.244
e	0.50 BASIC		.020 BASIC	
L	0.45	0.75	.018	.030
α	0°	8°	0°	8°
aaa	—	0.10	—	.004

1. For reference only. Controlling dimensions are in mm.

Ordering Information



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