October 25, 2005 FN8214.1

Sensor Conditioner with Dual Look Up Table Memory and DACs

FEATURES

- **Two Programmable Current Generators**
  - **—±3.2 mA max.**
  - **—8-bit (256 Step) Resolution**
  - **—External Resistor Pins to Set Full Scale Current Output**
- **External Sensor Input (Single Ended)**
- **Integrated 8-bit A/D Converter**
- **Internal Voltage Reference with Output/Input**
- **Temperature Compensation**
- **EEPROM Look-up Tables**
- **Hot Pluggable**
- **Write Protection Circuitry**
  - **—Intersil BlockLock™**
  - **—Logic Controlled Protection**
- **2-wire Bus with 3 Slave Address Bits**
- **3V to 5.5V, Single Supply Operation**
- **Package**
  - **—14 Ld TSSOP**
- **Pb-Free Plus Anneal Available (RoHS Compliant)**

APPLICATIONS

- **PIN Diode Bias Control**
- **RF PA Bias Control**
- **Temperature Compensated Process Control**
- **Laser Diode Bias Control**
- **Fan Control**
- **Motor Control**
- **Sensor Signal Conditioning**
- **Data Aquisition Applications**
- **Gain vs. Temperature Control**
- **High Power Audio**
- **Open Loop Temperature Compensation**
- **Close Loop Current, Voltage, Pressure, Temperature, Speed, Position Programmable Voltage sources, electronic loads, output amplifiers, or function generator**

DESCRIPTION

The X96010 is a highly integrated bias controller which incorporates two digitally controlled Programmable Current Generators and temperature compensation with dedicated look-up tables. All functions of the device are controlled via a 2-wire digital serial interface.

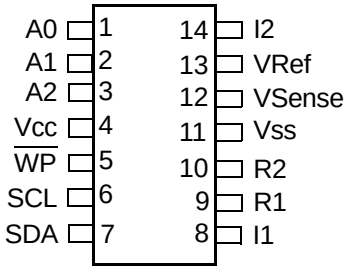
Two temperature compensated Programmable Current Generators, vary the output current with temperature according to the contents of the associated nonvolatile look-up table. The look-up table may be programmed with arbitrary data by the user via the 2-wire serial port, and an external temperature sensor may be used to control the output current response.

Ordering Information

PART NUMBER	PART MARKING	TEMP RANGE (°C)	PACKAGE
X96010V14I	X96010V I	-40 to 100	14 Ld TSSOP
X96010V14IZ (Note)	X96010VI Z	-40 to 100	14 Ld TSSOP (Pb-free)

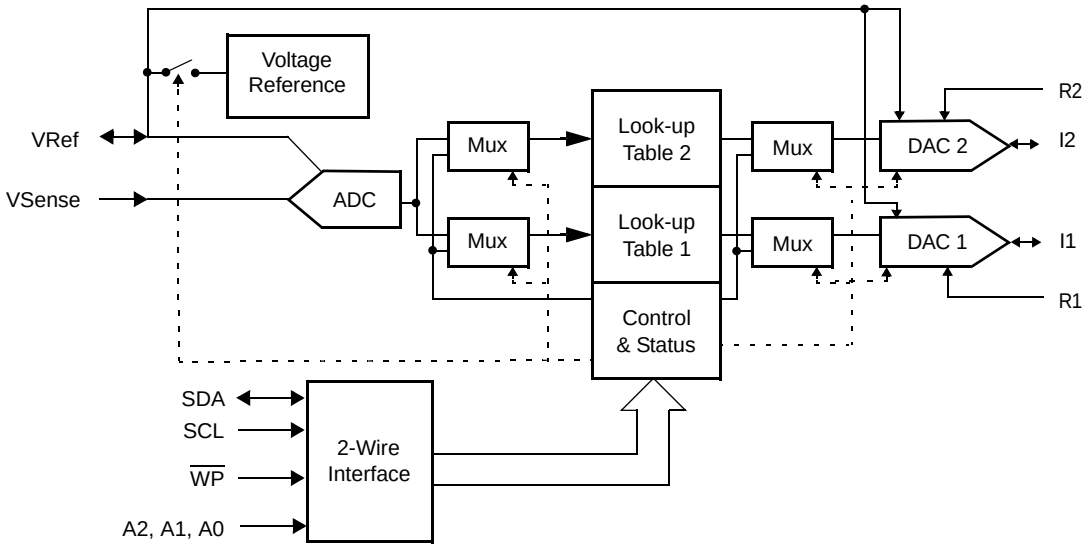
NOTE: Intersil Pb-free plus anneal products employ special Pb-free material sets; molding compounds/die attach materials and 100% matte tin plate termination finish, which are RoHS compliant and compatible with both SnPb and Pb-free soldering operations. Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.

PIN CONFIGURATION



TSSOP 14L

BLOCK DIAGRAM



PIN ASSIGNMENTS

TSSOP Pin	Pin Name	Pin Description
1	A0	**Device Address Select Pin 0.** This pin determines the LSB of the device address required to communicate using the 2-wire interface. The A0 pin has an on-chip pull-down resistor.
2	A1	**Device Address Select Pin 1.** This pin determines the intermediate bit of the device address required to communicate using the 2-wire interface. The A1 pin has an on-chip pull-down resistor.
3	A2	**Device Address Select Pin 2.** This pin determines the MSB of the device address required to communicate using the 2-wire interface. The A2 pin has an on-chip pull-down resistor.
4	Vcc	**Supply Voltage.**
5	$\overline{WP}$	**Write Protect Control Pin.** This pin is a CMOS compatible input. When LOW, Write Protection is enabled preventing any “Write” operation. When HIGH, various areas of the memory can be protected using the Block Lock bits BL1 and BL0. The $\overline{WP}$ pin has an on-chip pull-down resistor, which enables the Write Protection when this pin is left floating.
6	SCL	**Serial Clock.** This is a TTL compatible input pin. This input is the 2-wire interface clock controlling data input and output at the SDA pin.
7	SDA	**Serial Data.** This pin is the 2-wire interface data into or out of the device. It is TTL compatible when used as an input, and it is Open Drain when used as an output. This pin requires an external pull up resistor.
8	I1	**Current Generator 1 Output.** This pin sinks or sources current. The magnitude and direction of the current is fully programmable and adaptive. The resolution is 8 bits.
9	R1	**Current Programming Resistor 1.** A resistor between this pin and Vss can set the maximum output current available at pin I1. If no resistor is used, the maximum current must be selected using control register bits.
10	R2	**Current Programming Resistor 2.** A resistor between this pin and Vss can set the maximum output current available at pin I2. If no resistor is used, the maximum current must be selected using control register bits.
11	Vss	**Ground.**
12	VSense	**Sensor Voltage Input.** This voltage input may be used to drive the input of the on-chip A/D converter.
13	VRef	**Reference Voltage Input or Output.** This pin can be configured as either an Input or an Output. As an Input, the voltage at this pin is provided by an external source. As an Output, the voltage at this pin is a buffered output voltage of the on-chip bandgap reference circuit. In both cases, the voltage at this pin is the reference for the A/D converter and the two D/A converters.
14	I2	**Current Generator 2 Output.** This pin sinks or sources current. The magnitude and direction of the current is fully programmable and adaptive. The resolution is 8 bits.

ABSOLUTE MAXIMUM RATINGS

All voltages are referred to Vss.
Temperature under bias ..... -65°C to +100°C
Storage temperature ..... -65°C to +150°C
Voltage on every pin except Vcc ..... -1.0V to +7V
Voltage on Vcc Pin .....0 to 5.5V
D.C. Output Current at pin SDA ..... 0 to 5 mA
D.C. Output Current at pins R1, R2, and VRef ..... -0.50 to 1 mA
D.C. Output Current at pins I1 and I2 ..... -3.5 to +3.5mA
Lead temperature (soldering, 10s) ..... 300°C

COMMENT

Stresses above those listed under “Absolute Maximum Ratings” may cause permanent damage to the device. This is a stress rating only; functional operation of the device (at these or any other conditions above those listed in the operational sections of this specification) is not implied. Exposure to absolute maximum rating conditions for extended periods may affect device reliability.

RECOMMENDED OPERATING CONDITIONS

Parameter	Min.	Max.	Units
Temperature	-40	+100	°C
Temperature while writing to memory	0	+70	°C
Voltage on Vcc Pin	3	5.5	V
Voltage on any other Pin	-0.3	Vcc + 0.3	V

ELECTRICAL CHARACTERISTICS (Conditions are as follows, unless otherwise specified)

All typical values are for 25°C ambient temperature and 5V at pin Vcc. Maximum and minimum specifications are over the recommended operating conditions. All voltages are referred to the voltage at pin Vss. Bit 3 in Control register 0 is “1”, while all other bits in control registers are “0”. 255Ω, 0.1%, resistor connected between R1 and Vss, and another between R2 and Vss. 400kHz TTL input at SCL. SDA pulled to Vcc through an external 2kΩ resistor. 2-wire interface in “standby” (see notes 1 and 2 on page 5). WP, A0, A1, and A2 floating. VRef pin unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
Iccstby	Standby current into Vcc pin			2	mA	R1 and R2 floating, VRef unloaded.
Iccfull	Full operation current into Vcc pin			15	mA	2-wire interface reading from memory, I_1 and I_2 both connected to Vss, DAC input bytes: FFh, VRef unloaded.
Iccwrite	Nonvolatile Write current into Vcc pin		4		mA	Average from START condition until t_{WP} after the STOP condition WP: Vcc, R1 and R2 floating, VRef unloaded.
I_{PLDN}	On-chip pull down current at WP, A0, A1, and A2	0	1	20	µA	V(WP), V(A0), V(A1), and V(A2) from 0V to Vcc
V_{ILTTL}	SCL and SDA, input Low voltage			0.8	V	
V_{IHTTL}	SCL and SDA, input High voltage	2.0			V	
I_{INTTL}	SCL and SDA input current	-1		10	µA	Pin voltage between 0 and Vcc, and SDA as an input.
V_{OLSDA}	SDA output Low voltage	0		0.4	V	I(SDA) = 2 mA
I_{OHSDA}	SDA output High current	0		100	µA	V(SDA) = Vcc
V_{ILCMOS}	WP, A0, A1, and A2 input Low voltage	0		0.2 x Vcc	V	

ELECTRICAL CHARACTERISTICS (Continued) (Conditions are as follows, unless otherwise specified)

All typical values are for 25°C ambient temperature and 5V at pin Vcc. Maximum and minimum specifications are over the recommended operating conditions. All voltages are referred to the voltage at pin Vss. Bit 3 in Control register 0 is "1", while all other bits in control registers are "0". 255Ω, 0.1%, resistor connected between R1 and Vss, and another between R2 and Vss. 400kHz TTL input at SCL. SDA pulled to Vcc through an external 2kΩ resistor. 2-wire interface in "standby" (see notes 1 and 2 on page 5). $\overline{WP}$, A0, A1, and A2 floating. VRef pin unloaded.

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
V_{IHCMOS}	$\overline{WP}$, A0, A1, and A2 input High voltage	0.8 x Vcc		Vcc	V	
VRefout	Output Voltage at VRef at 25°C	1.205	1.21	1.215	V	-20 μA ≤ I(VRef) ≤ 20 μA
RVref	VRef pin input resistance	20		40	kΩ	VRM bit = "1", 25°C
TCOref	Temperature coefficient of VRef output voltage	-100		+100	ppm/°C	See note 4 and 5.
VRef Range	Voltage range when VRef is an input	1		1.3	V	See note 3.
I_R	Current from pin R1 or R2 to Vss	0		3200	μA	
V_{POR}	Power-on reset threshold voltage	1.5		2.8	V	
VccRamp	Vcc Ramp Rate	0.2		50	mV / μs	
V_{ADCOK}	ADC enable minimum voltage	2.6		2.8	V	See Figure 10.

Notes:
1. The device goes into Standby: 200 ns after any STOP, except those that initiate a nonvolatile write cycle. It goes into Standby t_{WC} after a STOP that initiates a nonvolatile write cycle. It also goes into Standby 9 clock cycles after any START that is not followed by the correct Slave Address Byte.
2. t_{WC} is the time from a valid STOP condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.
3. For this range of V(VRef) the full scale sink mode current at I1 and I2 follows V(VRef) with a linearity error smaller than 1%.
4. This parameter is periodically sampled and not 100% tested.
5. TCO_{ref} = [Max V(V_{REF}) - Min V(V_{REF})] x 10^6/(1.21V x 140°C)

D/A CONVERTER CHARACTERISTICS (See pg. 4 for Standard Conditions)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
IFS	I1 or I2 full scale current	1.56	1.58	1.6	mA	See note 1, 5, R = 510Ω
				3.2	mA	See note 1, 4, 6, R = 255Ω
$Offset_{DAC}$	I1 or I2 D/A converter offset error	1		1	LSB	See notes 2 and 3.
$FSError_{DAC}$	I1 or I2 D/A converter full scale error	-2		2	LSB	
DNL_{DAC}	I1 or I2 D/A converter Differential Nonlinearity	-0.5		0.5	LSB	
INL_{DAC}	I1 or I2 D/A converter Integral Nonlinearity with respect to a straight line through 0 and the full scale value	-1		1	LSB	
V_{ISink}	I1 or I2 Sink Voltage Compliance	1.2		Vcc	V	See note 5
		2.5		Vcc	V	See note 4, 6
$V_{ISource}$	I1 or I2 Source Voltage Compliance	0		Vcc-1.2	V	See note 5
		0		Vcc-2.5	V	See note 4, 6
I_{OVER}	I1 or I2 overshoot on D/A Converter data byte transition			0	µA	DAC input byte changing from 00h to FFh and vice versa, V(I1) and V(I2) are Vcc - 1.2V in source mode and 1.2V in sink mode. See note 4.
I_{UNDER}	I1 or I2 undershoot on D/A Converter data byte transition			0	µA	
t_{rDAC}	I1 or I2 rise time on D/A Converter data byte transition; 10% to 90%	5		30	µs	
TCO_{Iout}	Temperataure coefficient of output current due to internal parameters	-100		+100	ppm/°C	See Figure 7. VRMbit = “0”

Notes: 1. DAC input Byte = FFh, Source or sink mode.

2. LSB is defined as $\left[\frac{2}{3} \times \frac{V(VRef)}{255}\right]$ divided by the resistance between R1 or R2 to Vss.

3. $Offset_{DAC}$: The Offset of a DAC is defined as the deviation between the measured and ideal output, when the DAC input is 01h. It is expressed in LSB.
   $FSError_{DAC}$: The Full Scale Error of a DAC is defined as the deviation between the measured and ideal output, when the input is FFh. It is expressed in LSB. The $Offset_{DAC}$ is subtracted from the measured value before calculating $FSError_{DAC}$.
   DNL_{DAC}: The Differential Non-Linearity of a DAC is defined as the deviation between the measured and ideal incremental change in the output of the DAC, when the input changes by one code step. It is expressed in LSB. The measured values are adjusted for Offset and Full Scale Error before calculating DNL_{DAC}.
   INL_{DAC}: The Integral Non-Linearity of a DAC is defined as the deviation between the measured and ideal transfer curves, after adjusting the measured transfer curve for Offset and Full Scale Error. It is expressed in LSB.

4. These parameters are periodically sampled and not 100% tested.

5. V(I1) and V(I2) are V_{CC} - 1.2V in source mode and 1.2V in sink mode. In this range the current at I1 or I2 varies <1%.

6. The maximum current, sink or source, can be set with an external resistor to 3.2 mA with a minimum V_{CC} = 4.5V. The compliance voltage changes to 2.5V from the sourcing rail, and the current variation is <1%.

A/D CONVERTER CHARACTERISTICS (See pg. 4 for Standard Conditions)

Symbol	Parameter	Min	Typ	Max	Unit	Test Conditions / Notes
ADCTIME	A/D converter conversion time			9	ms	Proportional to A/D converter input voltage. This value is maximum at full scale input of A/D converter. ADCfiltOff = “1”
RIN_{ADC}	VSense pin input resistance	100			kΩ	VSense as an input, ADCIN bit = “1”
CIN_{ADC}	VSense pin input capacitance	1		7	pF	VSense as an input, ADCIN bit = “1”, Frequency = 1 MHz See note 3.
VIN_{ADC}	VSense input signal range	0		V(VRef)	V	This is the A/D Converter Dynamic Range. ADCIN bit = “1”
The ADC is monotonic						
$Offset_{ADC}$	A/D converter offset error		±1		LSB	See notes 1 and 2
$FSError_{ADC}$	A/D converter full scale error		±1		LSB	
DNL_{ADC}	A/D Converter Differential Nonlinearity		±0.5		LSB	
INL_{ADC}	A/D converter Integral Nonlinearity		±1		LSB	

Notes: 1. “LSB” is defined as V(VRef)/255, “Full Scale” is defined as V(VRef).

2. $Offset_{ADC}$: For an ideal converter, the first transition of its transfer curve occurs at $\left[\frac{0.5 \times V(VRef)}{255}\right]$ above zero. Offset error is the amount of deviation between the measured first transition point and the ideal point.
$FSError_{ADC}$: For an ideal converter, the last transition of its transfer curve occurs at $\left[\frac{254.5 \times V(VRef)}{255}\right]$. Full Scale Error is the amount of deviation between the measured last transition point and the ideal point, after subtracting the Offset from the measured curve.
DNL_{ADC}: DNL is defined as the difference between the ideal and the measured code transitions for successive A/D code outputs expressed in LSBs. The measured transfer curve is adjusted for Offset and Fullscale errors before calculating DNL.
INL_{ADC}: The deviation of the measured transfer function of an A/D converter from the ideal transfer function. The INL error is also defined as the sum of the DNL errors starting from code 00h to the code where the INL measurement is desired. The measured transfer curve is adjusted for Offset and Fullscale errors before calculating INL.

3. These parameters are periodically sampled and not 100% tested.

2-WIRE INTERFACE A.C. CHARACTERISTICS

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions / Notes
f_{SCL}	SCL Clock Frequency	1(3)		400	kHz	See "2-Wire Interface Test Conditions" (below), See Figure 1, Figure 2 and Figure 3.
t_{IN}(4)	Pulse width Suppression Time at inputs			50	ns	
t_{AA}(4)	SCL Low to SDA Data Out Valid			900	ns	
t_{BUF}(4)	Time the bus free before start of new transmission	1300			ns	
t_{LOW}	Clock Low Time	1.3		1200(3)	µs	
t_{HIGH}	Clock High Time	0.6		1200(3)	µs	
$t_{SU:STA}$	Start Condition Setup Time	600			ns	
$t_{HD:STA}$	Start Condition Hold Time	600			ns	
$t_{SU:DAT}$	Data In Setup Time	100			ns	
$t_{HD:DAT}$	Data In Hold Time	0			µs	
$t_{SU:STO}$	Stop Condition Setup Time	600			ns	
t_{DH}	Data Output Hold Time	50			ns	
t_R(4)	SDA and SCL Rise Time	20 +0.1Cb(1)		300	ns	
t_F(4)	SDA and SCL Fall Time	20 +0.1Cb(1)		300	ns	
$t_{SU:WP}$(4)	$\overline{WP}$ Setup Time	600			ns	
$t_{HD:WP}$(4)	$\overline{WP}$ Hold Time	600			ns	
Cb(4)	Capacitive load for each bus line			400	pF	

2-WIRE INTERFACE TEST CONDITIONS

Input Pulse Levels	10 % to 90 % of Vcc
Input Rise and Fall Times, between 10% and 90%	10 ns
Input and Output Timing Threshold Level	1.4V
External Load at pin SDA	2.3kΩ to Vcc and 100 pF to Vss

NONVOLATILE WRITE CYCLE TIMING

Symbol	Parameter	Min	Typ	Max	Units	Test Conditions / Notes
t_{WC}(2)	Nonvolatile Write Cycle Time		5	10	ms	See Figure 3

Notes: 1. Cb = total capacitance of one bus line (SDA or SCL) in pF.
2. t_{WC} is the time from a valid STOP condition at the end of a write sequence to the end of the self-timed internal nonvolatile write cycle. It is the minimum cycle time to be allowed for any nonvolatile write by the user, unless Acknowledge Polling is used.
3. The minimum frequency requirement applies between a START and a STOP condition.
4. These parameters are periodically sampled and not 100% tested.

TIMING DIAGRAMS

Figure 1. Bus Timing

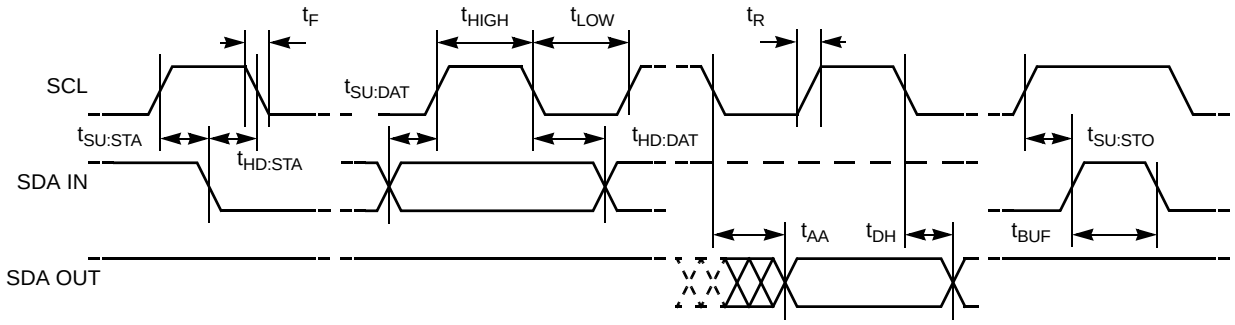


Figure 2. $\overline{WP}$ Pin Timing

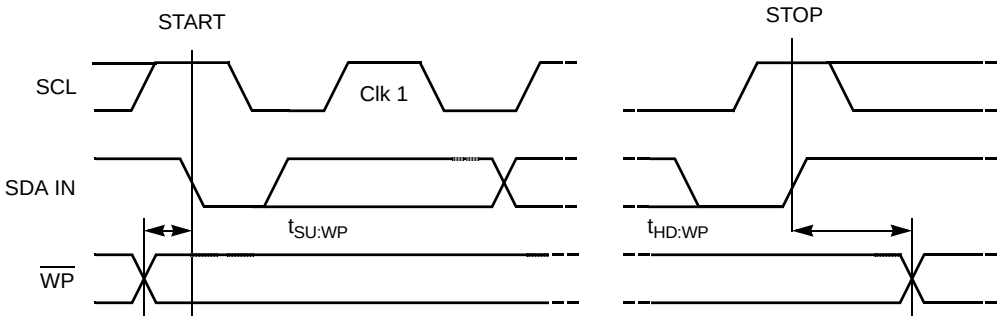
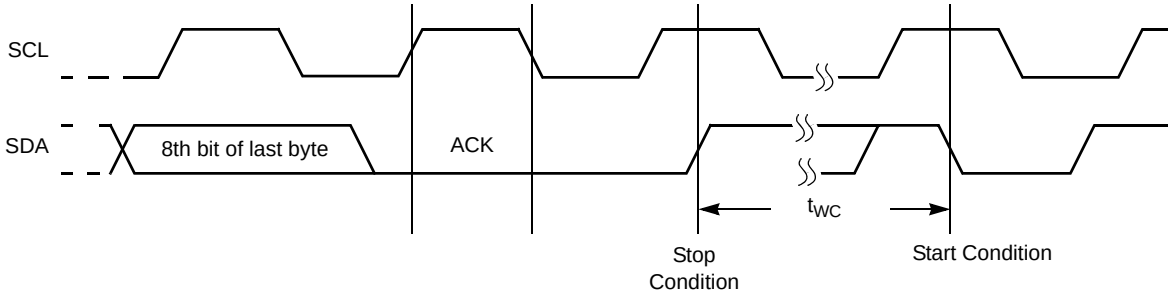


Figure 3. Non-Volatile Write Cycle Timing



INTERSIL SENSOR CONDITIONER PRODUCT FAMILY

Device	Title	Features / Functions							
		Internal Temperature Sensor	External Sensor Input	Internal Voltage Reference	VREF Input / Ouput	General Purpose EEPROM	Look Up Table Organi-zation	# of DACs	FSO Current DAC Setting Resistors
X96010	Sensor Conditioner with Dual Look-Up Table Memory and DACs	No	Yes	Yes	Yes	No	Dual Bank	Dual	Ext
X96011	Temperature Sensor with Look-Up Table Memory and DAC	Yes	No	Yes	No	No	Single Bank	Single	Int
X96012	Universal Sensor Conditioner with Dual Look-Up Table Memory and DACs	Yes	Yes	Yes	Yes	Yes	Dual Bank	Dual	Ext / Int

FSO = Full Scale Output, Ext = External, Int = Internal

DEVICE DESCRIPTION

The X96010 contains two independent Programmable Current Generators in one package. The combination of the X96010 functionality and Intersil's QFN package lowers system cost, increases reliability, and reduces board space requirements.

Two on-chip Programmable Current Generators may be independently programmed to either sink or source current. The maximum current generated is determined by using an externally connected programming resistor. Both current generators have a maximum output of ±3.2 mA, and may be controlled to an absolute resolution of 0.39% (256 steps / 8 bit).

Both current generators may be driven using an external sensor or Control Registers. The external sensor output drives a 8-bit A/D converter. The six MSBs of the ADC output select one of 64 bytes from each non-volatile look-up table (LUT).

The contents of the selected LUT row (8-bit wide) drives the input of an 8-bit D/A converter, which generates the output current.

All control and setup parameters of the X96010, including the look-up tables, are programmable via the 2-wire serial port.

PRINCIPLES OF OPERATION

CONTROL AND STATUS REGISTERS

The Control and Status Registers provide the user with a mechanism for changing and reading the value of various parameters of the X96010. The X96010 contains seven Control, one Status, and several Reserved registers, each being one Byte wide (See Figure 4). The Control registers 0 through 6 are located at memory addresses 80h through 86h respectively. The Status register is at memory address 87h, and the Reserved registers at memory address 88h through 8Fh.

All bits in Control register 6 always power-up to the logic state “0”. All bits in Control registers 0 through 5 power-up to the logic state value kept in their corresponding nonvolatile memory cells. The nonvolatile bits of a register retain their stored values even when the X96010 is powered down, then powered back up. The nonvolatile bits in Control 0 through Control 5 registers are all preprogrammed to the logic state “0” at the factory, except the cases that indicate “1” in Figure 4.

Bits indicated as “Reserved” are ignored when read, and must be written as “0”, if any Write operation is performed to their registers.

A detailed description of the function of each of the Control and Status register bits follows:

Control Register 0

This register is accessed by performing a Read or Write operation to address 80h of memory.

VRM: VOLTAGE REFERENCE PIN MODE (NON-VOLATILE)

The VRM bit configures the Voltage Reference pin (VRef) as either an input or an output. When the VRM bit is set to “0” (default), the voltage at pin VRef is an output from the X96010’s internal voltage reference. When the VRM bit is set to “1”, the voltage reference for the VRef pin is external. See Figure 5.

ADCFILTOFF: ADC FILTERING CONTROL (NON-VOLATILE)

When this bit is“1”, the status register at 87h is updated after every conversion of the ADC. When this bit is “0” (default), the status register is updated after four consecutive conversions with the same result, on the 6 MSBs.

NV1234: CONTROL REGISTERS 1, 2, 3, AND 4 VOLATILITY MODE SELECTION BIT (NON-VOLATILE)

When the NV1234 bit is set to “0” (default), bytes written to Control registers 1, 2, 3, and 4 are stored in volatile cells, and their content is lost when the X96010 is powered down. When the NV1234 bit is set to “1”, bytes written to Control registers 1, 2, 3, and 4 are stored in both volatile and nonvolatile cells, and their value doesn’t change when the X96010 is powered down and powered back up. See “Writing to Control Registers” on page 23.

I1DS: CURRENT GENERATOR 1 DIRECTION SELECT BIT (NON-VOLATILE)

The I1DS bit sets the polarity of Current Generator 1, DAC1. When this bit is set to “0” (default), the Current Generator 1 of the X96010 is configured as a Current Source. Current Generator 1 is configured as a Current Sink when the I1DS bit is set to “1”. See Figure 7.

Figure 4. Control and Status Register Format

Byte Address	MSB 7	6	5	4	3	2	1	LSB 0	Register Name
80h Non-Volatile	I2DS	I1DS	NV1234	ADCfiltOff	1	VRM	0	0	Control 0
	I1 and I2 Direction 0: Source 1: Sink		Control 1, 2, 3, 4 Volatility 0: Volatile 1: Non-volatile	ADC filtering 0: On 1: Off		Voltage Reference Mode 0: Internal 1: External			
	Direct Access to LUT1								
81h Volatile or Non-Volatile	Reserved	Reserved	L1DA5	L1DA4	L1DA3	L1DA2	L1DA1	L1DA0	Control 1
	Direct Access to LUT2								
82h Volatile or Non-Volatile	Reserved	Reserved	L2DA5	L2DA4	L2DA3	L2DA2	L2DA1	L2DA0	Control 2
	Direct Access to DAC1								
83h Volatile or Non-Volatile	D1DA7	D1DA6	D1DA5	D1DA4	D1DA3	D1DA2	D1DA1	D1DA0	Control 3
	Direct Access to DAC2								
84h Volatile or Non-Volatile	D2DA7	D2DA6	D2DA5	D2DA4	D2DA3	D2DA2	D2DA1	D2DA0	Control 4
85h Non-Volatile	D2DAS	L2DAS	D1DAS	L1DAS	0	0	0	0	Control 5
	Direct Access to DAC2 0: Disabled 1: Enabled	Direct Access to LUT2 0: Disabled 1: Enabled	Direct Access to DAC1 0: Disabled 1: Enabled	Direct Access to LUT1 0: Disabled 1: Enabled					
86h Volatile	WEL	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Reserved	Control 6
	Write Enable Latch 0: Write Disabled 1: Write Enabled								
	ADC Output								
87h Volatile	AD7	AD6	AD5	AD4	AD3	AD2	AD1	AD0	Status

Registers in byte addresses 88h through 8Fh are reserved.
Register bits shown as 0 or 1 should always use those values for proper operation.

I2DS: CURRENT GENERATOR 2 DIRECTION SELECT BIT (NON-VOLATILE)

The I2DS bit sets the polarity of Current Generator 2, DAC2. When this bit is set to “0” (default), the Current Generator 2 of the X96010 is configured as a Current Source. Current Generator 2 is configured as a Current Sink when the I2DS bit is set to “1”. See Figure 7.

Control Register 1

This register is accessed by performing a Read or Write operation to address 81h of memory. This byte’s volatility is determined by bit NV1234 in Control register 0.

L1DA5 - L1DA0: LUT1 DIRECT ACCESS BITS

When bit L1DAS (bit 4 in Control register 5) is set to “1”, LUT1 is addressed by these six bits, and it is not addressed by the output of the on-chip A/D converter. When bit L1DAS is set to “0”, these six bits are ignored by the X96010. See Figure 9.

A value between 00h (00_{10}) and 3Fh (63_{10}) may be written to these register bits, to select the corresponding row in LUT1. The written value is added to the base address of LUT1 (90h).

Control Register 2

This register is accessed by performing a read or write operation to address 82h of memory. This byte’s volatility is determined by bit NV1234 in Control register 0.

L2DA5 - L2DA0: LUT2 DIRECT ACCESS BITS

When bit L2DAS (bit 6 in Control register 5) is set to “1”, LUT2 is addressed by these six bits, and it is not addressed by the output of the on-chip A/D converter. When bit L2DAS is set to “0”, these six bits are ignored by the X96010. See Figure 9.

A value between 00h (00_{10}) and 3Fh (63_{10}) may be written to these register bits, to select the corresponding row in LUT2. The written value is added to the base address of LUT2 (D0h).

Control Register 3

This register is accessed by performing a Read or Write operation to address 83h of memory. This byte’s volatility is determined by bit NV1234 in Control register 0.

D1DA7 - D1DA0: D/A 1 DIRECT ACCESS BITS

When bit D1DAS (bit 5 in Control register 5) is set to “1”, the input to the D/A converter 1 is the content of bits D1DA7 - D1DA0, and it is not a row of LUT1. When bit D1DAS is set to “0” (default) these eight bits are ignored by the X96010. See Figure 8.

Control Register 4

This register is accessed by performing a Read or Write operation to address 84h of memory. This byte’s volatility is determined by bit NV1234 in Control register 0.

D2DA7 - D2DA0: D/A 2 DIRECT ACCESS BITS

When bit D2DAS (bit 7 in Control register 5) is set to “1”, the input to the D/A converter 1 is the content of bits D2DA7 - D2DA0, and it is not a row of LUT2. When bit D2DAS is set to “0” (default) these eight bits are ignored by the X96010. (See Figure 8).

Control Register 5

This register is accessed by performing a Read or Write operation to address 85h of memory.

L1DAS: LUT1 DIRECT ACCESS SELECT BIT (NON-VOLATILE)

When bit L1DAS is set to “0” (default), LUT1 is addressed by the output of the on-chip A/D converter. When bit L1DAS is set to “1”, LUT1 is addressed by bits L1DA5 - L1DA0.

D1DAS: D/A 1 DIRECT ACCESS SELECT BIT (NON-VOLATILE)

When bit D1DAS is set to “0” (default), the input to the D/A converter 1 is a row of LUT1. When bit D1DAS is set to “1”, that input is the content of the Control register 3.

L2DAS: LUT2 DIRECT ACCESS SELECT BIT (NON-VOLATILE)

When bit L2DAS is set to “0” (default), LUT2 is addressed by the output of the on-chip A/D converter. When bit L2DAS is set to “1”, LUT2 is addressed by bits L2DA5 - L2DA0.

D2DAS: D/A 2 DIRECT ACCESS SELECT BIT (NON-VOLATILE)

When bit D2DAS is set to “0” (default), the input to the D/A converter 2 is a row of LUT2. When bit D2DAS is set to “1”, that input is the content of the Control register 4.

Control Register 6

This register is accessed by performing a Read or Write operation to address 86h of memory.

WEL: WRITE ENABLE LATCH (VOLATILE)

The WEL bit controls the Write Enable status of the entire X96010 device. This bit must be set to “1” before any other Write operation (volatile or nonvolatile). Otherwise, any proceeding Write operation to memory is aborted and no ACK is issued after a Data Byte.

The WEL bit is a volatile latch that powers up in the “0” state (disabled). The WEL bit is enabled by writing 10000000_2 to Control register 6. Once enabled, the WEL bit remains set to “1” until the X96010 is powered down, and then up again, or until it is reset to “0” by writing 00000000_2 to Control register 6.

A Write operation that modifies the value of the WEL bit will not cause a change in other bits of Control register 6.

Status Register - ADC Output

This register is accessed by performing a Read operation to address 87h of memory.

AD7 - AD0: A/D CONVERTER OUTPUT BITS (READ ONLY)

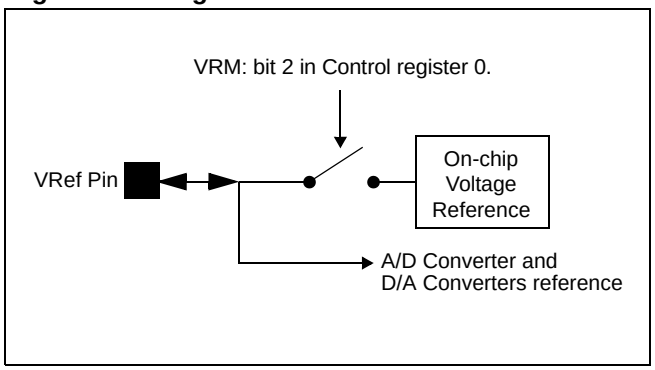
These eight bits are the binary output of the on-chip A/D converter. The output is 00000000_2 for minimum input and 11111111_2 for full scale input. The six MSBs select a row of the LUTs.

VOLTAGE REFERENCE

The voltage reference to the A/D and D/A converters on the X96010, may be driven from the on-chip voltage reference, or from an external source via the VRef pin. Bit VRM in Control Register 0 selects between the two options (See Figure 5).

The default value of VRM is “0”, which selects the internal reference. When the internal reference is selected, it’s output voltage is also an output at pin VRef with a nominal value of 1.21 V. If an external voltage reference is preferred, the VRM bit of the Control Register 0 must be set to “1”.

Figure 5. Voltage Reference Structure



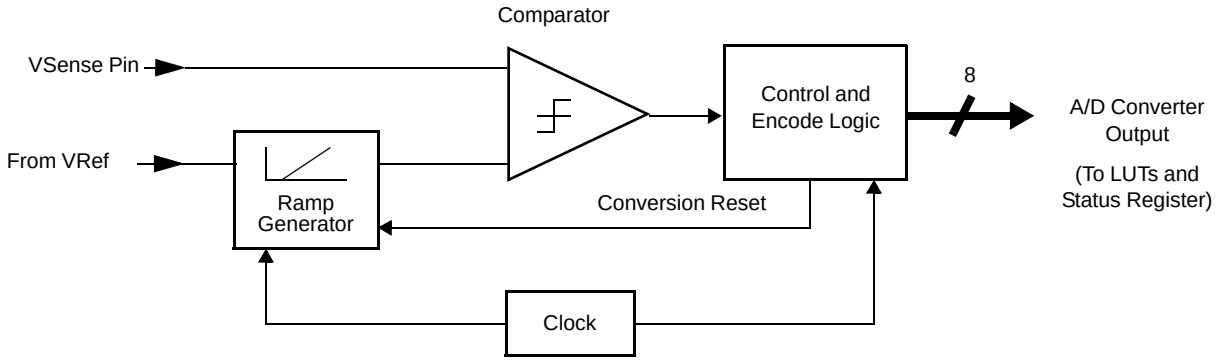
A/D CONVERTER

The X96010 contains a general purpose, on-chip, 8-bit Analog to Digital (A/D) converter whose output is available at the Status Register as bits AD[7:0]. By default these output bits are used to select a row in the look-up tables associated with the X96010’s Current Generators. When bit ADCfiltOff is “0” (default), bits AD[7:0] are updated each time the ADC performs four consecutive conversions with the same exact result at the 6 MSBs. When bit ADCfiltOff is “1”, these bits are updated after every ADC conversion.

A block diagram of the A/D converter is shown in Figure 6. The voltage reference input (see “VOLTAGE REFERENCE” for details), sets the maximum amplitude of the ramp generator output. The A/D converter input signal (see “A/D Converter Input Select” below for details) is compared to the ramp generator output. The control and encode logic produces a binary encoded output, with a minimum value of 00h (0_{10}), and a full scale output value of FFh (255_{10}).

The A/D converter input voltage range (VIN_{ADC}) is from 0 V to V(VRef).

Figure 6. A/D Converter Block Diagram



A/D Converter Range

From Figure 6 we can see that the operating range of the A/D converter input depends on the voltage reference.

The table below summarizes the voltage range restrictions on the VSense and VRef pins in different configurations :

VSense and VRef ranges

VRef	A/D Converter Input	Ranges
Internal	VSense Pin	$0 \le V(VSense) \le V(VRef)$
External	VSense Pin	$0 \le V(VRef) \le 1.3$ V $0 \le V(VSense) \le V(VRef)$
All voltages referred to Vss.		

LOOK-UP TABLES

The X96010 memory array contains two 64-byte look-up tables. One is associated to pin I1's output current generator and the other to pin I2's output current generator, through their corresponding D/A converters. The output of each look-up table is the byte contained in the selected row. By default these bytes are the inputs to the D/A converters driving pins I1 and I2.

The byte address of the selected row is obtained by adding the look-up table base address (90h for LUT1, and D0h for LUT2) and the appropriate row selection bits. See Figure 8.

By default the look-up table selection bits are the 6 MSBs of the A/D converter output. Alternatively, the A/D converter can be bypassed and the six row selection bits are the six LSBs of Control Registers 1 and 2, for the LUT1 and LUT2 respectively. The selection between these options is illustrated in Figure 9, and described in "I2DS: Current Generator 2 Direction Select Bit (Non-volatile)" on page 12, and "Control Register 2" on page 12.

CURRENT GENERATOR BLOCK

The Current Generator pins I1 and I2 are outputs of two independent current mode D/A converters.

D/A Converter Operation

The Block Diagram for each of the D/A converters is shown in Figure 7.

The input byte of the D/A converter selects a voltage on the non-inverting input of an operational amplifier. The output of the amplifier drives the gate of a FET, whose source is connected to ground via resistor R1 or R2. This node is also fed back to the inverting input of the amplifier. The drain of the FET is connected to the output current pin (I1 or I2) via a "polarity select" circuit block.

Figure 7. D/A Converter Block Diagram

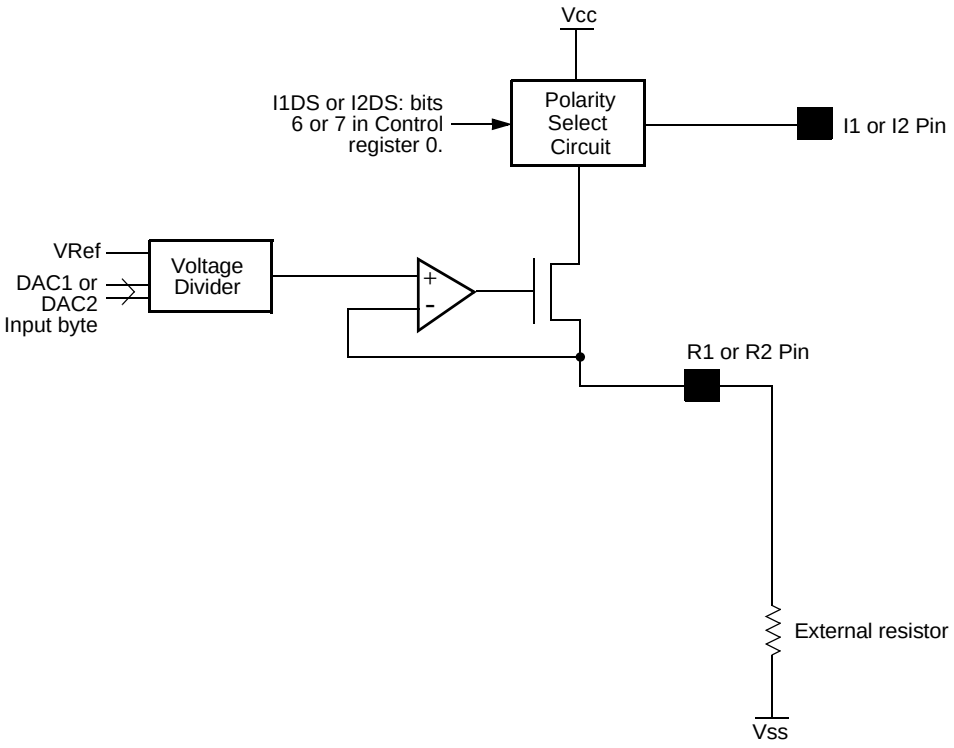
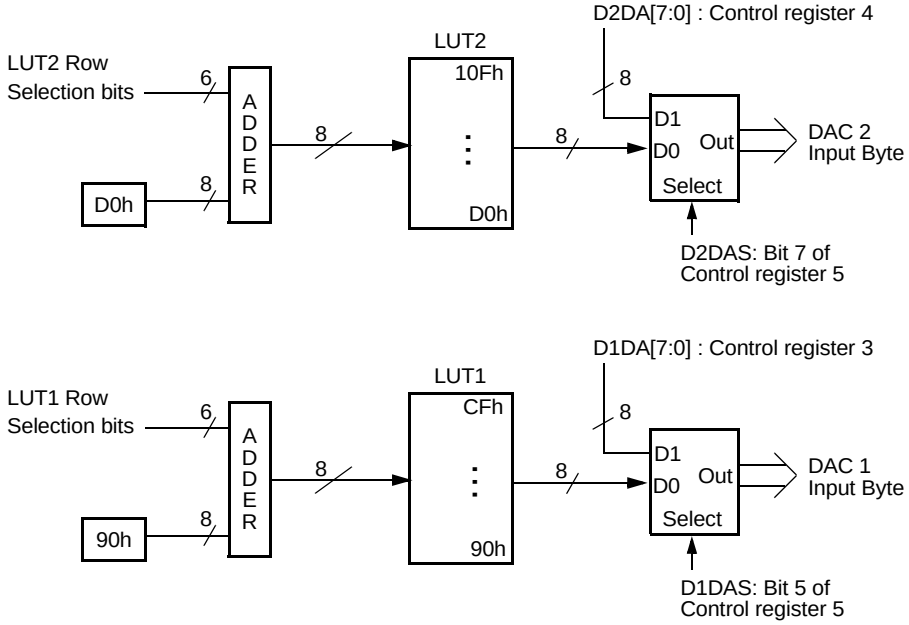


Figure 8. Look-up Table (LUT) Operation



By examining the block diagram in Figure 7, we see that the *maximum* current through pin I1 is set by fixing values for V(VRef) and R1. The output current can then be varied by changing the data byte at the D/A converter input.

In general, the magnitude of the current at the D/A converter output pins (I1, I2) may be calculated by:

$$Ix = (V(VRef) / (384 \cdot Rx)) \cdot N$$

where x = 1,2 and N is the decimal representation of the input byte to the corresponding D/A converter.

The value for the resistor Rx (x = 1,2) determines the *full scale output* current that the D/A converter may sink or source. The full scale output current has a maximum value of ±3.2 mA, which is obtained using a resistance of 255Ω for Rx. This resistance is connected externally to pin Rx of the X96010.

Bits I1DS and I2DS in Control Register 0 select the direction of the currents through pins I1 and I2 independently (See “I1DS: Current Generator 1 Direction Select Bit (Non-volatile)” on page 10 and “Control and Status Register Format” on page 11).

D/A Converter Output Current Response

When the D/A converter input data byte changes by an arbitrary number of bits, the output current changes from an intial current level (I_x) to some final level ($I_x + \Delta I_x$). The transition is monotonic and glitchless.

D/A Converter Control

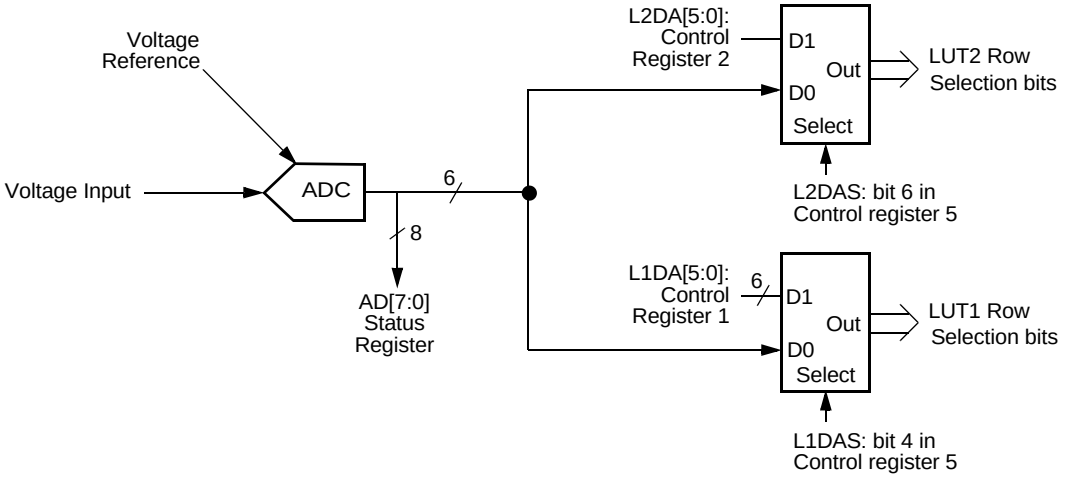
The data byte inputs of the D/A converters can be controlled in three ways:

– 1) With the A/D converter and through the look-up tables (default),

– 2) Bypassing the A/D converter and directly accessing the look-up tables,

– 3) Bypassing both the A/D converter and look-up tables, and directly setting the D/A converter input byte.

Figure 9. Look-Up Table Addressing



The options are summarized in the following tables:

D/A Converter 1 Access Summary

L1DAS	D1DAS	Control Source
0	0	A/D converter through LUT1 (Default)
1	0	Bits L1DA5 - L1DA0 through LUT1
X	1	Bits D1DA7 - D1DA0
“X” = Don’t Care Condition (May be either “1” or “0”)		

D/A Converter 2 Access Summary

L2DAS	D2DAS	Control Source
0	0	A/D converter through LUT2 (Default)
1	0	Bits L2DA5 - L2DA0 through LUT2
X	1	Bits D2DA7 - D2DA0
“X” = Don’t Care Condition (May be either “1” or “0”)		

The A/D converter is shared between the two current generators but the look-up tables, D/A converters, control bits, and selection bits can be set completely independently.

Bits D1DAS and D2DAS are used to bypass the A/D converter and look-up tables, allowing direct access to the inputs of the D/A converters with the bytes in control registers 3 and 4 respectively. See Figure 8, and the descriptions of the control bits.

Bits I1DS and I2DS in Control Register 0 select the direction of the currents through pins I1 and I2 independently See Figure 7, and the descriptions of the control bits.

POWER-ON RESET

When power is applied to the Vcc pin of the X96010, the device undergoes a strict sequence of events before the current outputs of the D/A converters are enabled.

When the voltage at Vcc becomes larger than the power-on reset threshold voltage (V_{POR}), the device recalls all control bits from non-volatile memory into volatile registers. Next, the analog circuits are powered up. When the voltage at Vcc becomes larger than a second voltage threshold (V_{ADCOK}), the ADC is enabled. In the default case, after the ADC performs four consecutive conversions with the same exact result, the ADC output is used to select a byte from each look-up table. Those bytes become the input of the DACs. During all the previous sequence the input of both DACs are 00h. If bit ADCfiltOff is “1”, only one ADC conversion is necessary. Bits D1DAS, D2DAS, L1DAS, and L2DAS, also modify the way the two DACs are accessed the first time after power-uppower-up, as described in “Control Register 5” on page 12.

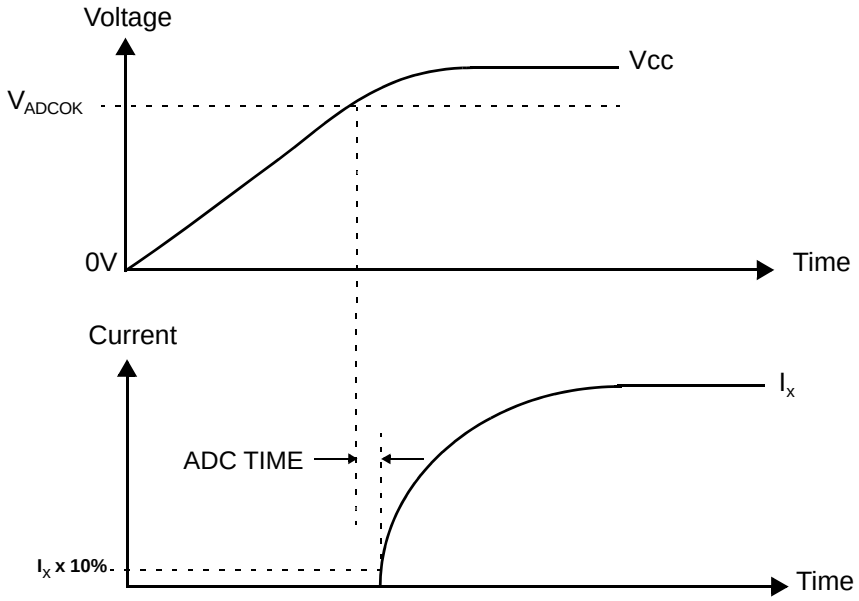
The X96010 is a hot pluggable device. Voltage distrubances on the Vcc pin are handled by the power-on reset circuit, allowing proper operation during hot plug-in applications.

SERIAL INTERFACE

Serial Interface Conventions

The device supports a bidirectional bus oriented protocol. The protocol defines any device that sends data onto the bus as a transmitter, and the receiving device as the receiver. The device controlling the transfer is called the master and the device being controlled is called the slave. The master always initiates data transfers, and provides the clock for both transmit and receive operations. The X96010 operates as a slave in all applications.

Figure 10. D/A Converter Power-on Reset Response



Serial Clock and Data

Data states on the SDA line can change only while SCL is LOW. SDA state changes while SCL is HIGH are reserved for indicating START and STOP conditions. See Figure 12. On power-up of the X96010, the SDA pin is in the input mode.

Serial Start Condition

All commands are preceded by the START condition, which is a HIGH to LOW transition of SDA while SCL is HIGH. The device continuously monitors the SDA and SCL lines for the START condition and does not respond to any command until this condition has been met. See Figure 11.

Serial Stop Condition

All communications must be terminated by a STOP condition, which is a LOW to HIGH transition of SDA while SCL is HIGH. The STOP condition is also used to place the device into the Standby power mode after a read sequence. A STOP condition can only be issued after the transmitting device has released the bus. See Figure 11.

Serial Acknowledge

An ACK (Acknowledge), is a software convention used to indicate a successful data transfer. The transmitting device, either master or slave, releases the bus after transmitting eight bits. During the ninth clock cycle, the receiver pulls the SDA line LOW to acknowledge the reception of the eight bits of data. See Figure 13.

The device responds with an ACK after recognition of a START condition followed by a valid Slave Address byte. A valid Slave Address byte must contain the Device Type Identifier 1010, and the Device Address bits matching the logic state of pins A2, A1, and A0. See Figure 15.

If a write operation is selected, the device responds with an ACK after the receipt of each subsequent eight-bit word.

In the read mode, the device transmits eight bits of data, releases the SDA line, and then monitors the line for an ACK. The device continues transmitting data if an ACK is detected. The device terminates further data transmissions if an ACK is not detected. The master must then issue a STOP condition to place the device into a known state.

The X96010 acknowledges all incoming data and address bytes except: 1) The “Slave Address Byte” when the “Device Identifier” or “Device Address” are wrong; 2) All “Data Bytes” when the “WEL” bit is “0”, with the exception of a “Data Byte” addresses to location 86h; 3) “Data Bytes” following a “Data Byte” addressed to locations 80h, 85h, or 86h.

Figure 11. Valid Start and Stop Conditions

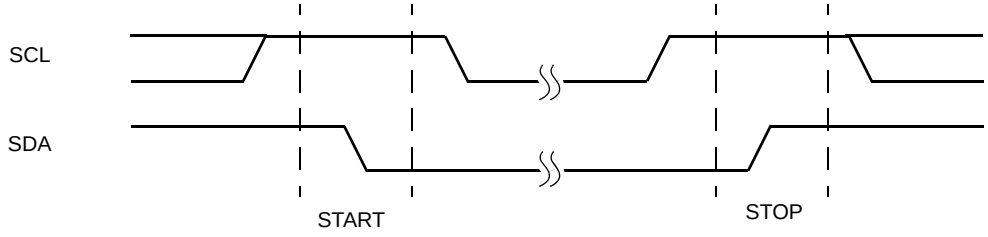


Figure 12. Valid Data Changes on the SDA Bus

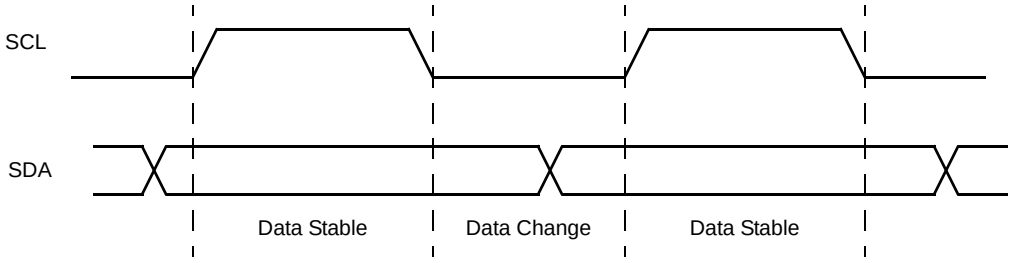
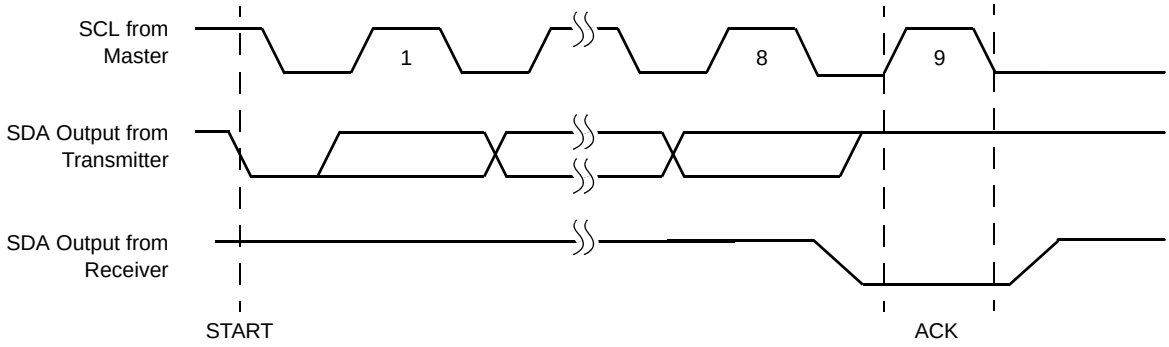


Figure 13. Acknowledge Response From Receiver



X96010 Memory Map

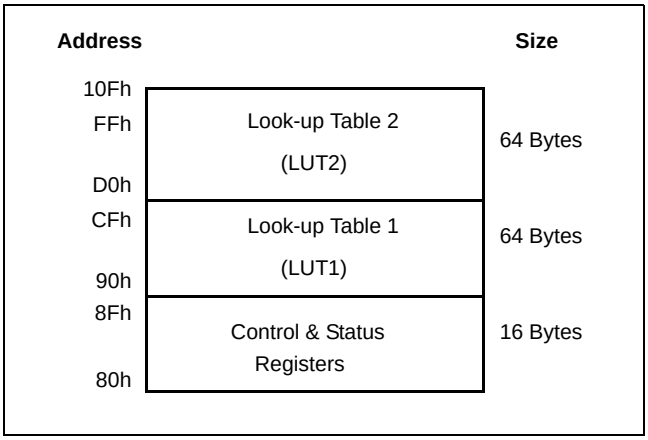
The X96010 contains a 144 byte array of mixed volatile and nonvolatile memory. This array is split up into three distinct parts, namely: (Refer to figure 14.)

– Look-up Table 1 (LUT1)

– Look-up Table 2 (LUT2)

– Control and Status Registers

Figure 14. X96010 Memory Map



The Control and Status registers of the X96010 are used in the test and setup of the device in a system. These registers are realized as a combination of both volatile and nonvolatile memory. These registers reside in the memory locations 80h through 8Fh. The reserved bits within registers 80h through 86h, must be written as “0” if writing to them, and should be ignored when reading. Register bits shown as 0 or 1, in Figure 4, must be written with the indicated value if writing to them. The reserved registers, from 88h through 8Fh, must not be written, and their content should be ignored.

Both look-up tables LUT1 and LUT2 are realized as nonvolatile EEPROM, and extend from memory locations 90h - CFh and D0h - 10Fh respectively. These look-up tables are dedicated to storing data solely for the purpose of setting the outputs of Current Generators I1 and I2 respectively.

All bits in both look-up tables are preprogrammed to “0” at the factory.

Addressing Protocol Overview

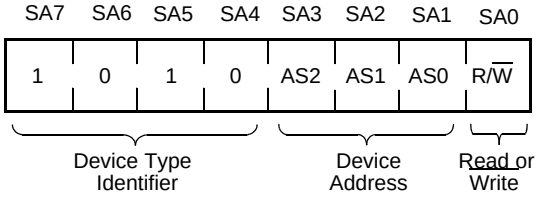
All Serial Interface operations must begin with a START, followed by a Slave Address Byte. The Slave address selects the X96010, and specifies if a Read or Write operation is to be performed.

It should be noted that the Write Enable Latch (WEL) bit must first be set in order to perform a Write operation to any other bit. (See “WEL: Write Enable Latch (Volatile)” on page 13.) Also, all communication to the X96010 over the 2-wire serial bus is conducted by sending the MSB of each byte of data first.

The memory is physically realized as one contiguous array, organized as 9 pages of 16 bytes each.

The X96010 2-wire protocol provides one address byte, therefore the next few sections explain how to access the different areas for reading and writing.

Figure 15. Slave Address (SA) Format



Slave Address Bit(s)	Description
SA7 - SA4	Device Type Identifier
SA3 - SA1	Device Address
SA0	Read or Write Operation Select

Slave Address Byte

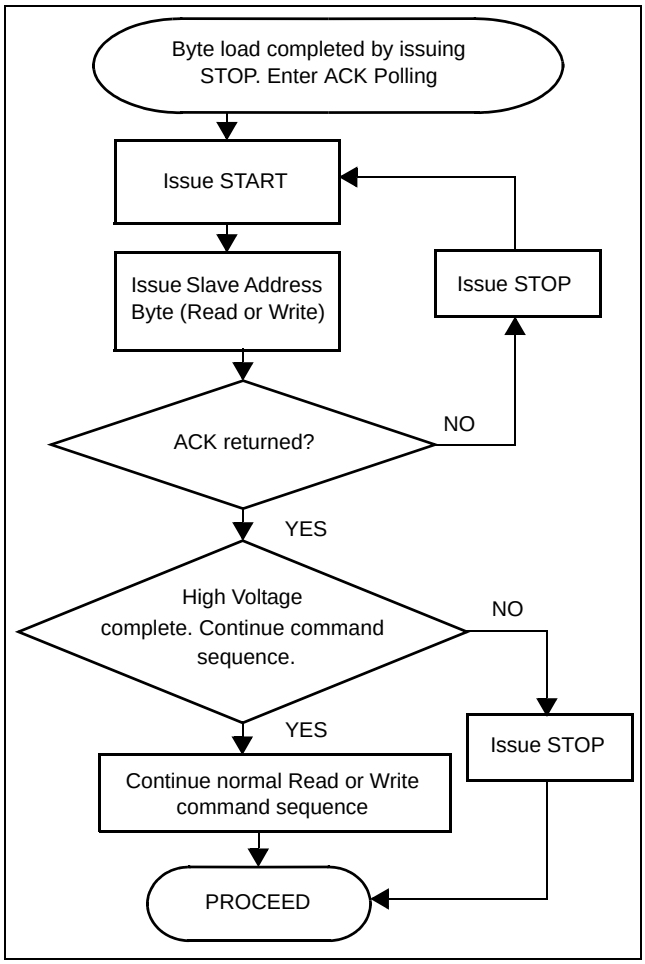
Following a START condition, the master must output a Slave Address Byte (Refer to figure 15.). This byte includes three parts:

– The four MSBs (SA7 - SA4) are the Device Type Identifier, which must always be set to 1010 in order to select the X96010.

– The next three bits (SA3 - SA1) are the Device Address bits (AS2 - AS0). To access any part of the X96010's memory, the value of bits AS2, AS1, and AS0 must correspond to the logic levels at pins A2, A1, and A0 respectively.

– The LSB (SA0) is the R/$\overline{W}$ bit. This bit defines the operation to be performed on the device being addressed. When the R/$\overline{W}$ bit is "1", then a Read operation is selected. A "0" selects a Write operation (Refer to figure 15.)

Figure 16. Acknowledge Polling Sequence



Nonvolatile Write Acknowledge Polling

After a nonvolatile write command sequence is correctly issued (including the final STOP condition), the X96010 initiates an internal high voltage write cycle. This cycle typically requires 5 ms. During this time, any Read or Write command is ignored by the X96010. Write Acknowledge Polling is used to determine whether a high voltage write cycle is completed.

During acknowledge polling, the master first issues a START condition followed by a Slave Address Byte. The Slave Address Byte contains the X96010's Device Type Identifier and Device Address. The LSB of the Slave Address (R/$\overline{W}$) can be set to either 1 or 0 in this case. If the device is busy within the high voltage cycle, then no ACK is returned. If the high voltage cycle is completed, an ACK is returned and the master can then proceed with a new Read or Write operation. (Refer to figure 16.).

Byte Write Operation

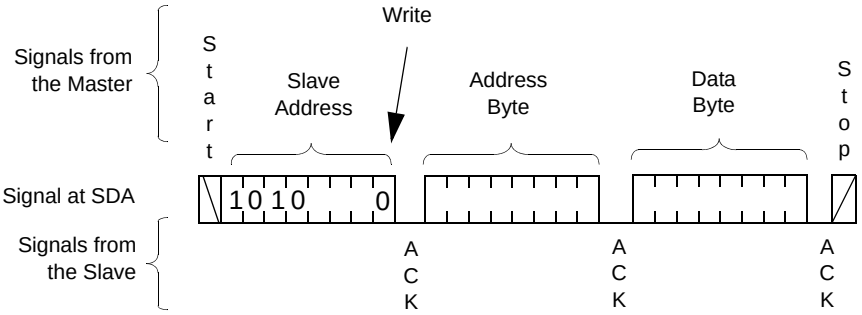
In order to perform a Byte Write operation to the memory array, the Write Enable Latch (WEL) bit of the Control 6 Register must first be set to "1". (See "WEL: Write Enable Latch (Volatile)" on page 13.)

For any Byte Write operation, the X96010 requires the Slave Address Byte, an Address Byte, and a Data Byte (See Figure 17). After each of them, the X96010 responds with an ACK. The master then terminates the transfer by generating a STOP condition. At this time, if all data bits are volatile, the X96010 is ready for the next read or write operation. If some bits are nonvolatile, the X96010 begins the internal write cycle to the nonvolatile memory. During the internal nonvolatile write cycle, the X96010 does not respond to any requests from the master. The SDA output is at high impedance.

A Byte Write operation can access bytes at locations 80h through FEh directly, when setting the Address Byte to 80h through FEh respectively. Setting the Address Byte to FFh accesses the byte at location 100h. The other sixteen bytes, at locations FFh and 101h through 10Fh can only be accessed using Page Write operations. The byte at location FFh can only be written using a "Page Write" operation.

Writing to Control bytes which are located at byte addresses 80h through 8Fh is a special case described in the section "Writing to Control Registers" .

Figure 17. Byte Write Sequence



Page Write Operation

The 144-byte memory array is physically realized as one contiguous array, organized as 9 pages of 16 bytes each. “Page Write” operations can be performed to any of the LUT pages. In order to perform a Page Write operation the Write Enable Latch (WEL) bit in Control register 6 must first be set (See “WEL: Write Enable Latch (Volatile)” on page 13.)

A Page Write operation is initiated in the same manner as the byte write operation; but instead of terminating the write cycle after the first data byte is transferred, the master can transmit up to 16 bytes (See Figure 18). After the receipt of each byte, the X96010 responds with an ACK, and the internal byte address counter is incremented by one. The page address remains constant. When the counter reaches the end of the page, it “rolls over” and goes back to the first byte of the same page.

For example, if the master writes 12 bytes to a 16-byte page starting at location 11 (decimal), the first 5 bytes are written to locations 11 through 15, while the last 7 bytes are written to locations 0 through 6 within that page. Afterwards, the address counter would point to location 7. If the master supplies more than 16 bytes of data, then new data overwrites the previous data, one byte at a time (See Figure 19).

The master terminates the loading of Data Bytes by issuing a STOP condition, which initiates the nonvolatile write cycle. As with the Byte Write operation, all inputs are disabled until completion of the internal write cycle.

A Page Write operation cannot be performed on the page at locations 80h through 8Fh. Next section describes the special cases within that page.

A Page Write operation starting with byte address FFh, accesses the page between locations 100h and 10Fh. The first data byte of such operation is written to location 100h.

Writing to Control Registers

The bytes at location 80h, 85h and 86h are written using Byte Write operations. They cannot be written using a Page Write operation.

Control bytes 1 through 4, at locations 81h through 84h respectively, are written during a single operation (See Figure 20). The sequence must be: a START, followed by a Slave Address byte, with the R/$\overline{W}$ bit equal to “0”, followed by 81h as the Address Byte, and then followed by exactly four Data Bytes, and a STOP condition. The first data byte is written to location 81h, the second to 82h, the third to 83h, and the last one to 84h.

Figure 18. Page Write Operation

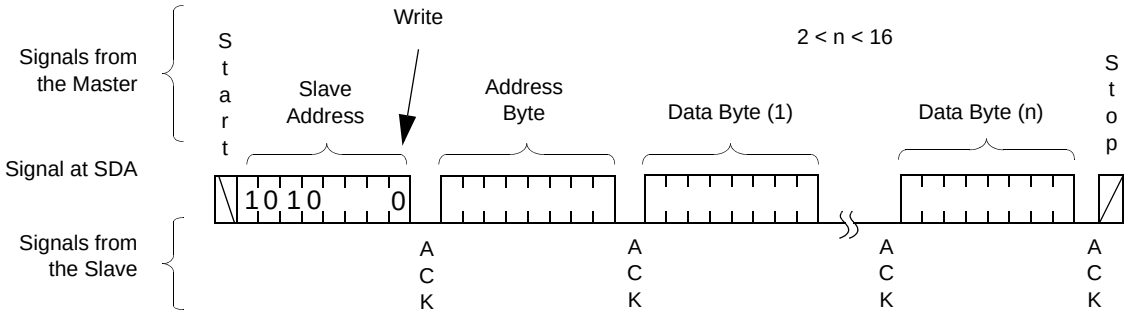
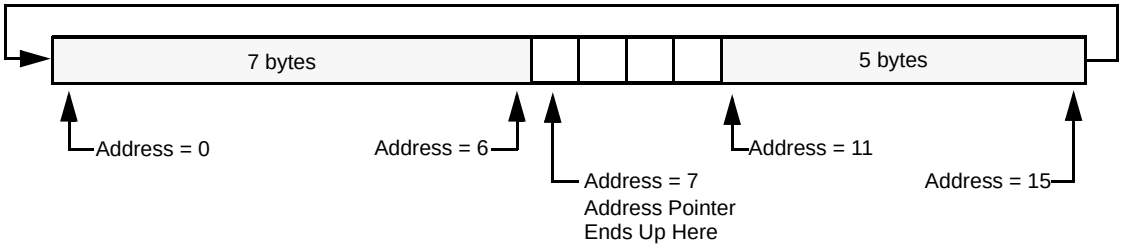


Figure 19. Example: Writing 12 bytes to a 16-byte page starting at location 11.



The four registers Control 1 through 4, have a nonvolatile and a volatile cell for each bit. At power-up, the content of the nonvolatile cells is automatically recalled and written to the volatile cells. The content of the volatile cells controls the X96010's functionality. If bit NV1234 in the Control 0 register is set to "1", a Write operation to these registers writes to both the volatile and nonvolatile cells. If bit NV1234 in the Control 0 register is set to "0", a Write operation to these registers only writes to the volatile cells. In both cases the newly written values effectively control the X96010, but in the second case, those values are lost when the part is powered down.

If bit NV1234 is set to "0", a Byte Write operation to Control registers 0 or 5 causes the value in the nonvolatile cells of Control registers 1 through 4 to be recalled into their corresponding volatile cells, as during power-up. This doesn't happen when the $\overline{WP}$ pin is LOW, because Write Protection is enabled. It is generally recommended to configure Control registers 0 and 5 before writing to Control registers 1 through 4.

When reading any of the control registers 1, 2, 3, or 4, the Data Bytes are always the content of the corresponding nonvolatile cells, even if bit NV1234 is "0" (See "Control and Status Register Format").

Read Operation

A Read operation consist of a three byte instruction followed by one or more Data Bytes (See Figure 21). The master initiates the operation issuing the following sequence: a START, the Slave Address byte with the $R/\overline{W}$ bit set to "0", an Address Byte, a second START, and a second Slave Address byte with the $R/\overline{W}$ bit set to "1". After each of the three bytes, the X96010 responds with an ACK. Then the X96010 transmits Data Bytes as long as the master responds with an ACK during the SCL cycle following the eigth bit of each byte. The master terminates the read operation (issuing a STOP condition) following the last bit of the last Data Byte (See Figure 21).

Figure 20. Writing to Control Registers 1, 2, 3, and 4

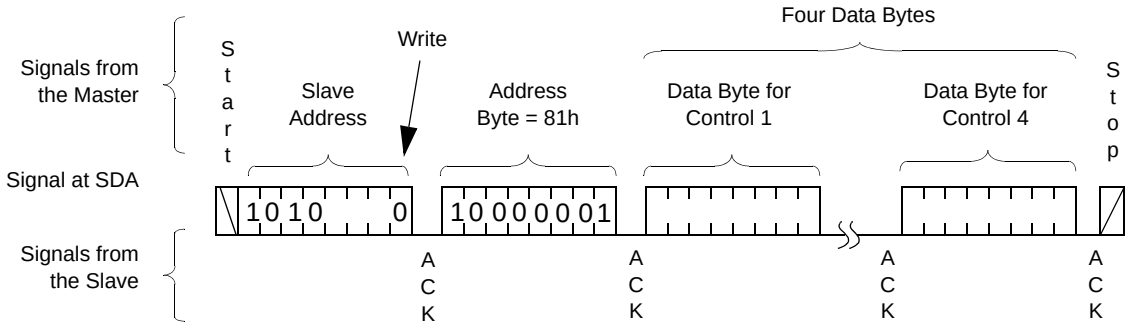
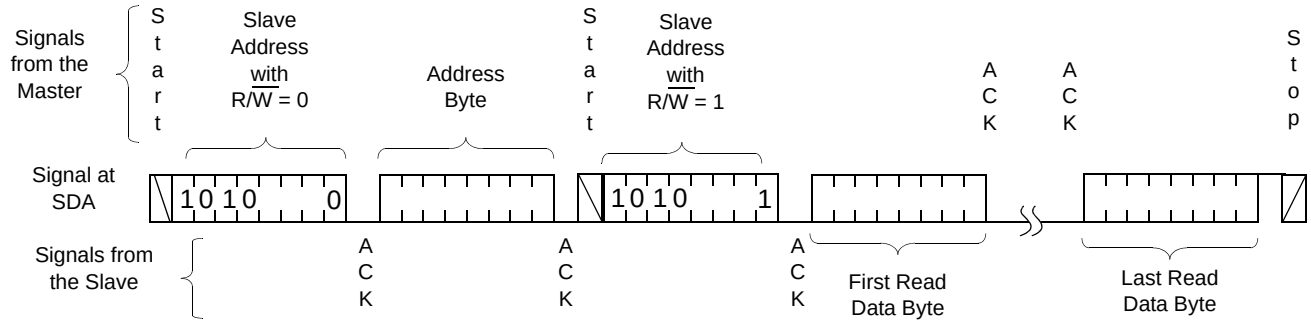


Figure 21. Read Sequence



The Data Bytes are from the memory location indicated by an internal pointer. This pointer initial value is determined by the Address Byte in the Read operation instruction, and increments by one during transmission of each Data Byte. After reaching the memory location 10Fh, a stop should be issued.

If the read operation continues, the output bytes are unpredictable. If the address is set between 00h and 7Fh, the output bytes are unpredictable.

A Read operation internal pointer can start at any memory location from 80h through FEh, when the Address Byte is 80h through FEh respectively. But it starts at location 100h if the Address Byte is FFh.

When reading any of the control registers 1, 2, 3, or 4, the Data Bytes are always the content of the corresponding nonvolatile cells, even if bit NV1234 is "0" (See “Control and Status Register Format”).

Data Protection

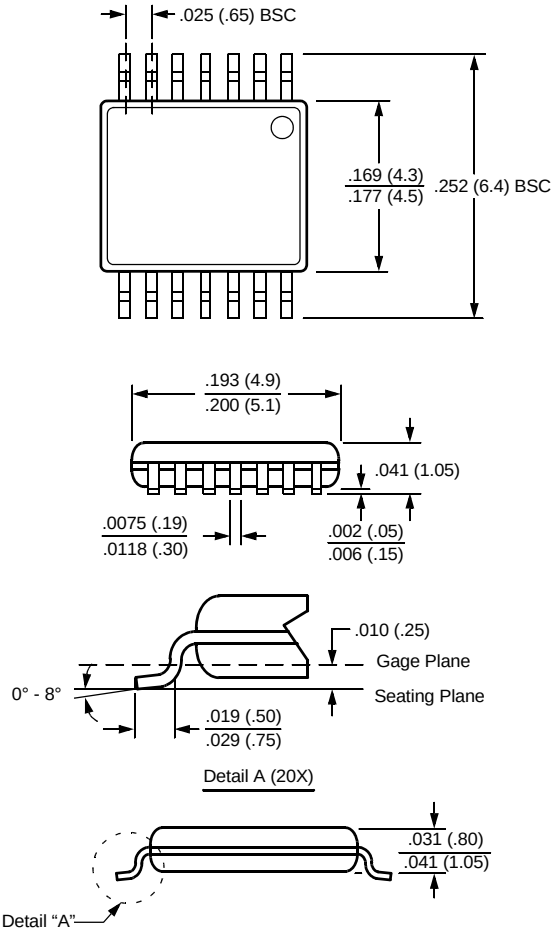
There are three levels of data protection designed into the X96010: 1- Any Write to the device first requires setting of the WEL bit in Control 6 register; 2- The Write Protection pin disables any writing to the X96010; 3- The proper clock count, data bit sequence, and STOP condition is required in order to start a nonvolatile write cycle, otherwise the X96010 ignores the Write operation.

$\overline{WP}$: Write Protection Pin

When the Write Protection ($\overline{WP}$) pin is active (LOW), any Write operations to the X96010 is disabled, except the writing of the WEL bit.

PACKAGING INFORMATION

14-Lead Plastic, TSSOP, Package Code V14



NOTE: ALL DIMENSIONS IN INCHES (IN PARENTHESES IN MILLIMETERS)