Brief Description

The ZSPM4551 is a DC/DC synchronous switching lithium-ion (Li-Ion) battery charger with fully integrated power switches, internal compensation, and full fault protection.

Its switching frequency of 1MHz enables the use of small filter components, resulting in smaller board space and reduced BOM costs.

In Full-Charge Constant-Current Mode, the regulation is for constant current (CC). Once termination voltage is reached, the regulator operates in voltage mode. When the regulator is disabled (the EN pin is low), the device draws 10µA (typical) quiescent current.

The ZSPM4551 includes supervisory reporting through the NFLT (inverted fault) open-drain output to interface other components in the system. Device programming is achieved by an I²C™* interface through the SCL and SDA pins.

Benefits

- Up to 1.5A of continuous output current in Full-Charge Constant-Current (CC) Mode
- High efficiency – up to 92% with typical loads

Available Support

- Evaluation Kit
- Support Documentation

Features

- VBAT reverse-current blocking
- Programmable temperature-compensated termination voltage: 3.94V to 4.18V ± 1%
- User programmable maximum charge current: 50mA to 1500mA
- Current mode PWM control in constant voltage
- Supervisor for VBAT reported at the NFLT pin
- Input supply under-voltage lockout
- Full protection for over-current, over-temperature, VBAT over-voltage, and charging timeout
- Charge status indication
- I^2C™ program interface with EEPROM registers

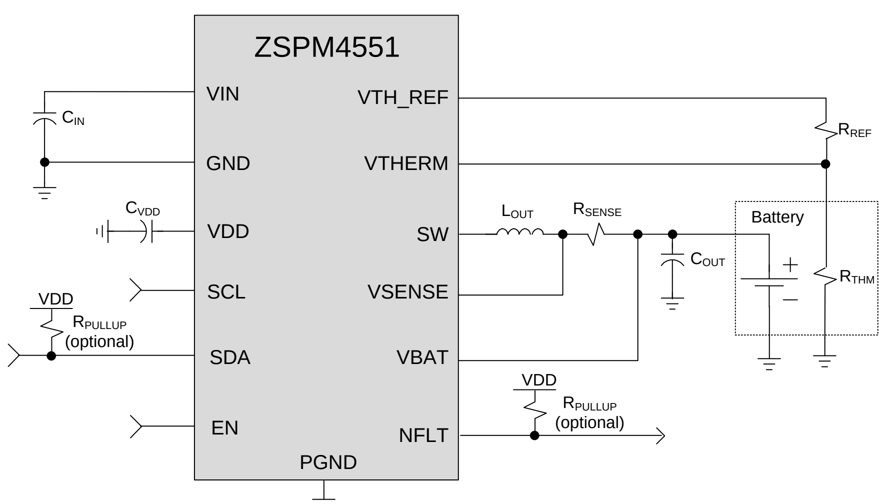
Related IDT Smart Power Products

- ZSPM4121 Ultra-low Power Under-Voltage Switch
- ZSPM4141 Ultra-Low-Power Linear Regulator

Physical Characteristics

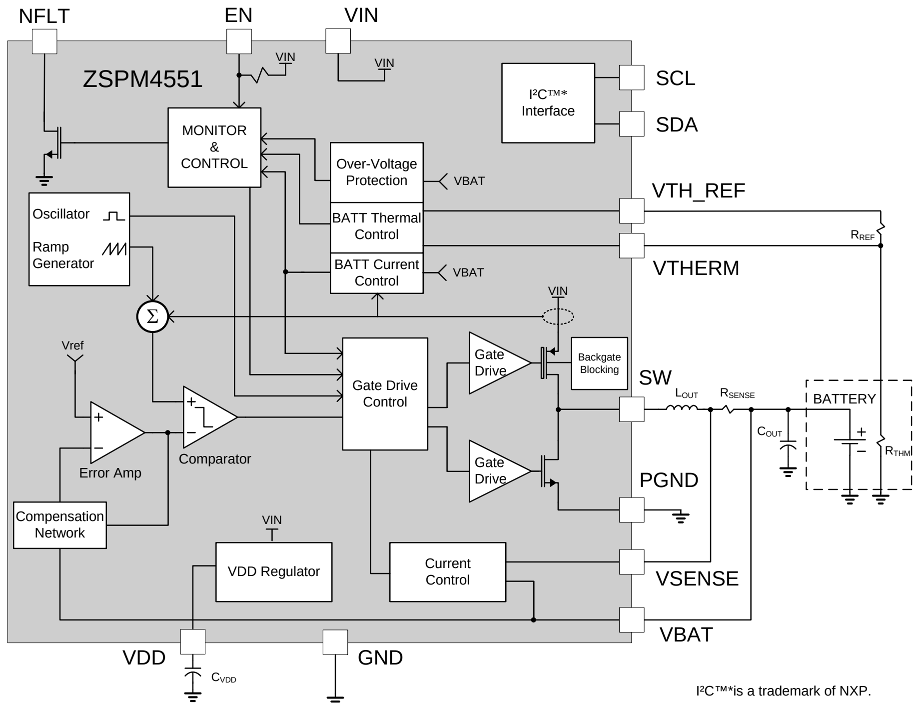
- Wide input voltage range: V_{BAT} + 0.3V (3.5V min.) to 7.2V
- Junction operating temperature: -40°C to 125°C
- Package: 16-pin PQFN (4mm x 4mm)

ZSPM4551 Application Circuit



* I^2C™ is a trademark of NXP.

ZSPM4551 Block Diagram



Typical Applications

- Portable battery chargers
- Smart phones
- Laptops
- Tablets/e-readers

Ordering Information

Ordering Code	Description	Package
ZSPM4551AA1W	ZSPM4551 High-Efficiency Li-Ion Battery Charger	16-pin PQFN / 7” Reel (1000 parts)
ZSPM4551AA1R	ZSPM4551 High-Efficiency Li-Ion Battery Charger	16-pin PQFN / 13” Reel (3300 parts)
ZSPM4551KIT	ZSPM4551 Evaluation Kit	

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1 ZSPM4551 Characteristics

Important: Stresses beyond those listed under “Absolute Maximum Ratings” (section 1.1) may cause permanent damage to the device. These are stress ratings only, and functional operation of the device at these or any other conditions beyond those indicated under “Recommended Operating Conditions” is not implied. Exposure to absolute–maximum–rated conditions for extended periods may affect device reliability.

1.1. **Absolute Maximum Ratings**

Over operating free–air temperature range unless otherwise noted.

Table 1.1 Absolute Maximum Ratings

Parameter	Value [1)]	Unit
VIN, EN, NFLT, SCL, SDA, VTHERM, VTH_REF, VBAT, VSENSE	-0.3 to 8	V
SW	-1 to 8.8	V
VDD	-0.3 to 3.6	V
Operating Junction Temperature Range, T_J	-40 to 125	°C
Storage Temperature Range, T_{STOR}	-65 to 150	°C
Electrostatic Discharge – Human Body Model [2)]	±2k	V
Electrostatic Discharge – Machine Model [2)]	+/-200	V
Lead Temperature (soldering, 10 seconds)	260	°C

1) All voltage values are with respect to network ground terminal.

2) ESD testing is performed according to the respective JESD22 JEDEC standard.

1.2. Thermal Characteristics

Table 1.2 Thermal Characteristics

Parameter	Symbol	Value [1)]	Unit
Thermal Resistance Junction to Air [1)]	θ_{JA}	50	°C/W

1) Assumes a 4x4mm QFN-16 in 1 in² area of 2 oz. copper and 25°C ambient temperature.

1.3. Recommended Operating Conditions

Table 1.3 Recommended Operating Conditions

Parameter	Symbol	Min	Typ	Max	Unit
Input Operating Voltage at VIN Pin	V_{IN}	V_{BAT} + 0.3V (3.5V min)	5.3	7.2	V
Sense Resistor	R_{SENSE}		50		mΩ
Output Filter Inductor Typical Value [1)]	L_{OUT}		4.7		µH
Output Filter Capacitor Typical Value [2)]	C_{OUT}		4.7		µF
Output Filter Capacitor ESR	$C_{OUT-ESR}$			100	mΩ
Input Supply Bypass Capacitor Value [3)]	C_{IN}	3.3	10		µF
VDD Supply Bypass Capacitor Value [2)]	C_{VDD}	70	100	130	nF
Operating Free Air Temperature	T_A	-40		85	°C
Operating Junction Temperature	T_J	-40		125	°C

1) For best performance, use an inductor with a saturation current rating higher than the maximum V_{BAT} load requirement plus the inductor current ripple.

2) For best performance, use a low ESR ceramic capacitor.

3) For best performance, use a low ESR ceramic capacitor. If C_{IN} is not a low ESR ceramic capacitor, add a 0.1µF ceramic capacitor in parallel to C_{IN}.

1.4. Electrical Characteristics

Electrical characteristics T_J = -40°C to 125°C, VIN = 5.3V, (unless otherwise noted)

Table 1.4 Electrical Characteristics

Parameter	Symbol	Condition	Min	Typ	Max	Unit
VIN Supply Voltage						
Voltage Input	V_{IN}		V_{BAT}+0.3V (3.5V min)	5.3	7.2	V
Quiescent Current Normal Mode	$I_{CC-NORM}$	I_{LOAD} = 0A, no switching EN ≥ 2.2V (HIGH)		3		mA
Quiescent Current Disabled Mode	$I_{CC--DISABLE}$	EN = 0V		10	50	µA
VBAT Leakage						
Leakage Current From Battery	$I_{BAT-LEAK}$	EN = 0V, V_{VBAT} = 4.1V			10	µA
Reverse Current	$I_{BAT-BACK}$	VBAT > VIN, VBAT = 4.1V, T_J < 85°C			10	µA
VIN Under-Voltage Lockout						
Input Supply Under-Voltage Threshold	V_{IN-UV}	V_{IN} increasing		3.15		V
Input Supply Under-Voltage Threshold Hysteresis	V_{IN-UV_HYST}		100	200		mV
OSC						
Oscillator Frequency	f_{OSC}		0.9	1	1.1	MHz
NFLT Open Drain Output						
High-Level Output Leakage	$I_{OH-NFLT}$	V_{NFLT} = 5.3V		0.1		µA
Low-Level Output Voltage	$V_{OL-NFLT}$	I_{NFLT} = -1mA			0.4	V
EN/SCL/SDA Input Voltage Thresholds						
High Level Input Voltage	V_{IH}		2.2			V
Low Level Input Voltage	V_{IL}				0.8	V
Input Hysteresis – EN, SCL, SDA Pins	V_{HYST}			200		mV

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Input Leakage – EN Pin	I_{IN-EN}	V_{EN}=VIN		0.1		µA
		V_{EN}=0V		-2.0		µA
Input Leakage – SCL Pin	I_{IN-SCL}	V_{SCL}=VIN		55		µA
		V_{SCL}=0V		-0.1		µA
Input Leakage – SDA Pin	I_{IN-SDA}	V_{SDA}=VIN		0.1		µA
		V_{SDA}=0V		-0.1		µA
Low-Level Output Voltage	V_{OL-SDA}	I_{SDA} = -1mA			0.4	V
Thermal Shutdown						
Thermal Shutdown Junction Temperature	T_{SD}		150	170		°C
TSD Hysteresis	$T_{SD-HYST}$			10		°C
Pre-Charge End						
Pre-charge Voltage Threshold	V_{PRECHG}		2.9	3.0	3.1	V
Pre-charge Voltage Hysteresis	$V_{PC-HYST}$			70		mV
Charge Restart						
Voltage Below Termination for Charging Restart	$V_{RESTART}$			100		mV
Charging Regulator with L_{OUT} =4.7µH and C_{OUT}=4.7µF						
Output Current Limit Tolerance in Full-Charge Mode	I_{BAT-FC}	I_{BAT} is user programmable; see Table 2.5.	I_{BAT} - 10%	I_{BAT}	I_{BAT} + 10%	A
Termination Voltage Tolerance in Top-Off Mode	V_{BAT-TO}	I_{BAT} = 0.1C, 0°C < T_J < 85°C V_{BAT} is user programmable; see section 2.4.	V_{BAT} - 1%	V_{BAT}	V_{BAT} + 1%	V
Top-Off Mode Time Out	t_{TO}		0		120	Minutes
Full-Charge Timer	t_{FC}		200		1400	Minutes
Timer Accuracy	t_{ACC}		-10%		+10%	
High Side Switch On Resistance	R_{DSON}	I_{SW} = -1A, T_J=25°C		200		mΩ
Low Side Switch On Resistance		I_{SW} = 1A, T_J=25°C		250		mΩ
Maximum Output Current	I_{BAT}			1.5		A
Over-Current Detect	I_{OCD}	HS switch current	2.5			A
V_{BAT} Over-Voltage Threshold	V_{BAT-OV}		101% V_{BAT}	102% V_{BAT}	103% V_{BAT}	
Maximum Duty Cycle	$DUTY_{MAX}$			98		%

Parameter	Symbol	Condition	Min	Typ	Max	Unit
Thermistor						
VTH_REF Output Voltage	V_{VTH_REF}	I_{VT_REF} = 2µA to 100µA		1.8		V
Thermistor: 10KΩ Temperature Thresholds – β=3434K						
0°C VTHERM Threshold (0°C)	0°C	Decreasing Temperature		75.6		%VTH_REF
0°C VTHERM Threshold with Hysteresis (10°C)	$0°C_{HYST}$	Increasing Temperature		66.5		%VTH_REF
10°C VTHERM Threshold (10°C)	10°C	Decreasing Temperature		66.2		%VTH_REF
10°C VTHERM Threshold with Hysteresis (11°C)	$10°C_{HYST}$	Increasing Temperature		65.4		%VTH_REF
45°C VTHERM Threshold (45°C)	45°C	Increasing Temperature		34.5		%VTH_REF
45°C VTHERM Threshold with Hysteresis (44°C)	$45°C_{HYST}$	Decreasing Temperature		35.3		%VTH_REF
50°C VTHERM Threshold (50°C)	50°C	Increasing Temperature		30.8		%VTH_REF
50°C VTHERM Threshold with Hysteresis (49°C)	$50°C_{HYST}$	Decreasing Temperature		31.5		%VTH_REF
60°C VTHERM Threshold (60°C)	60°C	Increasing Temperature		24.9		%VTH_REF
60°C VTHERM Threshold with Hysteresis (50°C)	$60°C_{HYST}$	Decreasing Temperature		30.8		%VTH_REF
Thermistor: 100KΩ Temperature Thresholds – β=4311K						
0°C VTHERM Threshold (0°C)	0°C	Decreasing Temperature		80.5		%VTH_REF
0°C VTHERM Threshold with Hysteresis (10°C)	$0°C_{HYST}$	Increasing Temperature		69.8		%VTH_REF
10°C VTHERM Threshold (10°C)	10°C	Decreasing Temperature		69.8		%VTH_REF
10°C VTHERM Threshold with Hysteresis (11°C)	$10°C_{HYST}$	Increasing Temperature		68.6		%VTH_REF
45°C VTHERM Threshold (45°C)	45°C	Increasing Temperature		31.3		%VTH_REF
45°C VTHERM Threshold with Hysteresis (44°C)	$45°C_{HYST}$	Decreasing Temperature		32.3		%VTH_REF

Parameter	Symbol	Condition	Min	Typ	Max	Unit
50°C VTHERM Threshold (50°C)	50°C	Increasing Temperature		27.0		%VTH_REF
50°C VTHERM Threshold with Hysteresis (49°C)	$50°C_{HYST}$	Decreasing Temperature		27.8		%VTH_REF
60°C VTHERM Threshold (60°C)	60°C	Increasing Temperature		19.4		%VTH_REF
60°C VTHERM Threshold with Hysteresis (50°C)	$60°C_{HYST}$	Decreasing Temperature		27.0		%VTH_REF

1.5. I^2C™ Interface Timing Requirements

Electrical characteristics T_J = -40°C to 125°C, VIN = 5.3V. See Figure 2.5 for an illustration of the timing specifications given in Table 1.5.

Table 1.5 I^2C™ Interface Timing Characteristics

Parameter	Symbol	Standard Mode		Fast Mode [1]		Unit
		Min	Max	Min	Max	
I^2C™ Clock Frequency	f_{scl}	0	100	0	400	kHz
I^2C™ Clock High Time	t_{sch}	4		0.6		µs
I^2C™ Clock Low Time	t_{scl}	4.7		1.3		µs
I^2C™ Tolerable Spike Time [2]	t_{sp}	0	50	0	50	ns
I^2C™ Serial Data Setup Time	t_{sds}	250		250		ns
I^2C™ Serial Data Hold Time	t_{sdh}	0		0		µs
I^2C™ Input Rise Time [2]	t_{icr}		1000		300	ns
I^2C™ Input Fall Time [2]	t_{icf}		300		300	ns
I^2C™ Output Fall Time; 10pF to 400pF Bus [2]	t_{ocf}		300		300	ns
I^2C™ Bus Free Time Between Stop and Start	t_{buf}	4.7		1.3		µs
I^2C™ Start or Repeated Start Condition Setup Time	t_{sts}	4.7		0.6		µs
I^2C™ Start or Repeated Start Condition Hold Time	t_{sth}	4		0.6		µs
I^2C™ Stop Condition Setup Time [2]	t_{sps}	4		0.6		µs

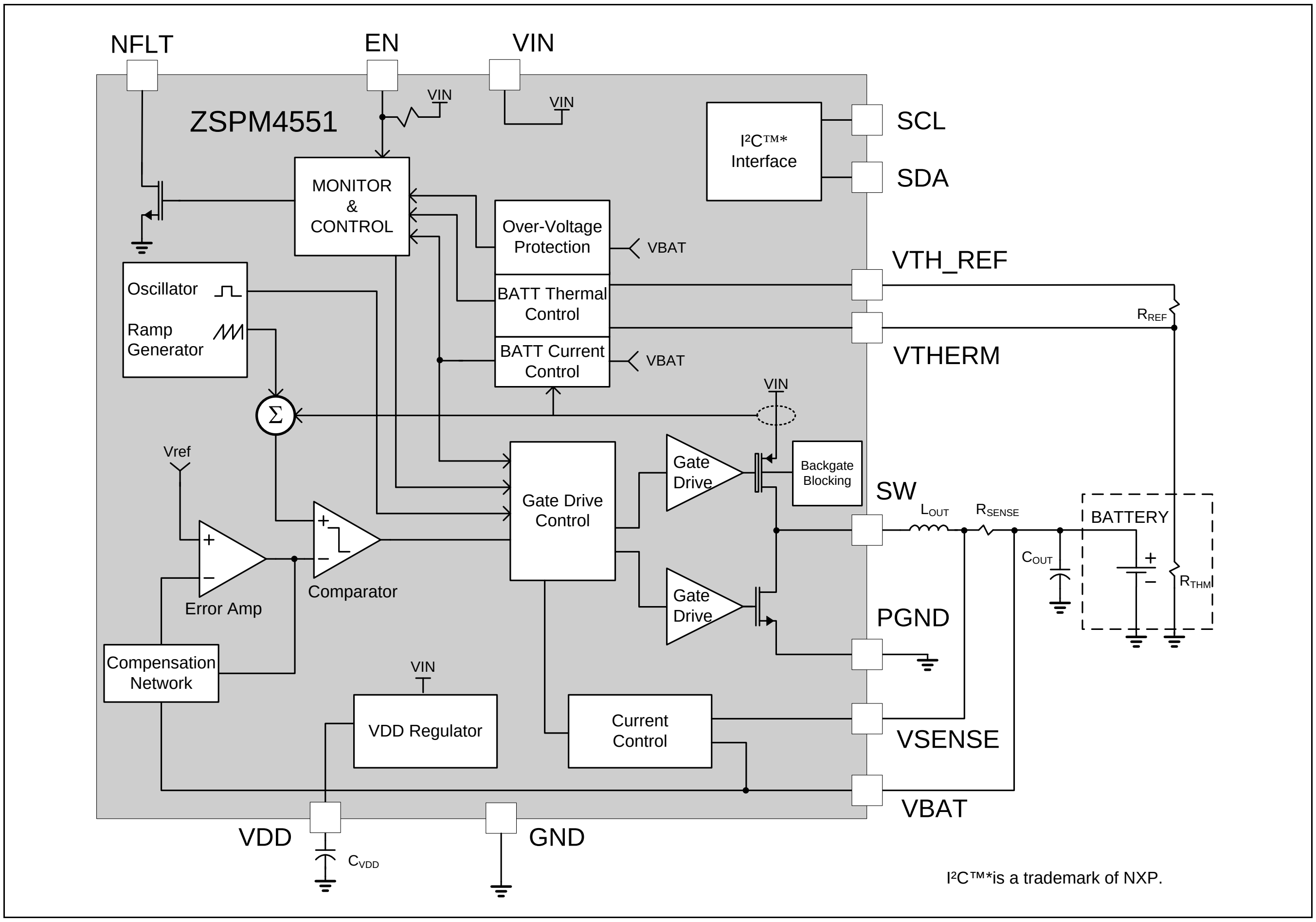
1) The I^2C™ interface will operate in either standard or fast mode.

2) Parameter not tested in production.

2 Functional Description

The ZSPM4551 is a fully-integrated Li-Ion battery charger IC based on a highly-efficient switching topology. It is configurable for termination voltage, charge current, and additional variables to allow optimum charging conditions for a wide range of Li-Ion batteries. A 1MHz internal switching frequency facilitates low-cost LC filter combinations. Figure 2.1 provides a block diagram for the ZSPM4551.

Figure 2.1 ZSPM4551 Block Diagram



When the battery voltage is below 3.0 volts, the ZSPM4551 enters a pre-charge state and applies a small, programmable charge current to safely charge the battery to a level for which full-charge current can be applied. Once the Full-Charge Mode has been initiated, the regulation will be for constant current (CC). When the battery voltage has increased enough to go into maintenance mode, the PWM control loop will force a constant voltage across the battery. Once in constant voltage mode, current is monitored to determine when the battery is fully charged. See Figure 2.2 for a diagram of the charging states.

This regulation voltage as well as the 1C charging current can be set to change based on the battery temperature. There are four temperature ranges for which the regulation voltage can be set independently: 0°C to 10°C, 10°C to 45°C, 45°C to 50°C, and 50°C to 60°C. The ZSPM4551 will stop charging if the temperature passes the descending temperature threshold at 0°C or the ascending threshold at 60°C. These thresholds have 10 degrees of hysteresis. The intermediate points have 1 degree of hysteresis.

2.1. Internal Protection

2.1.1. VIN Under-Voltage Lockout

The device is held in the off state until the EN pin voltage is HIGH (≥ 2.2V) and VIN rises to 3.15V (typical). There is a 200mV hysteresis on this input, which requires the input to fall below 2.95V (typical) before the device will disable.

2.1.2. Internal Current Limit

The current through the inductor L_{OUT} is sensed on a cycle-by-cycle basis and if the current limit (I_{OCD}; see section 1.4) is reached, the ZSPM4551 will abbreviate the cycle. The current limit is always active when the regulator is enabled.

2.1.3. Thermal Shutdown

If the junction temperature of the ZSPM4551 exceeds 170°C (typical), the SW output will tri-state to protect the device from damage. The NFLT and all other protection circuitry will stay active to inform the system of the failure mode. Once the device cools to 160°C (typical), the device will attempt to start up again. If the device reaches 170°C, the shutdown/restart sequence will repeat.

2.1.4. VBAT Over-Voltage Protection

The ZSPM4551 has a battery protection circuit designed to shut down the charging profile if the battery voltage is greater than the termination voltage. The termination voltage can change based on user programming, so the protection threshold is set to 2% above the termination voltage. Shutting down the charging profile puts the ZSPM4551 in a fault condition.

2.2. Fault Handling

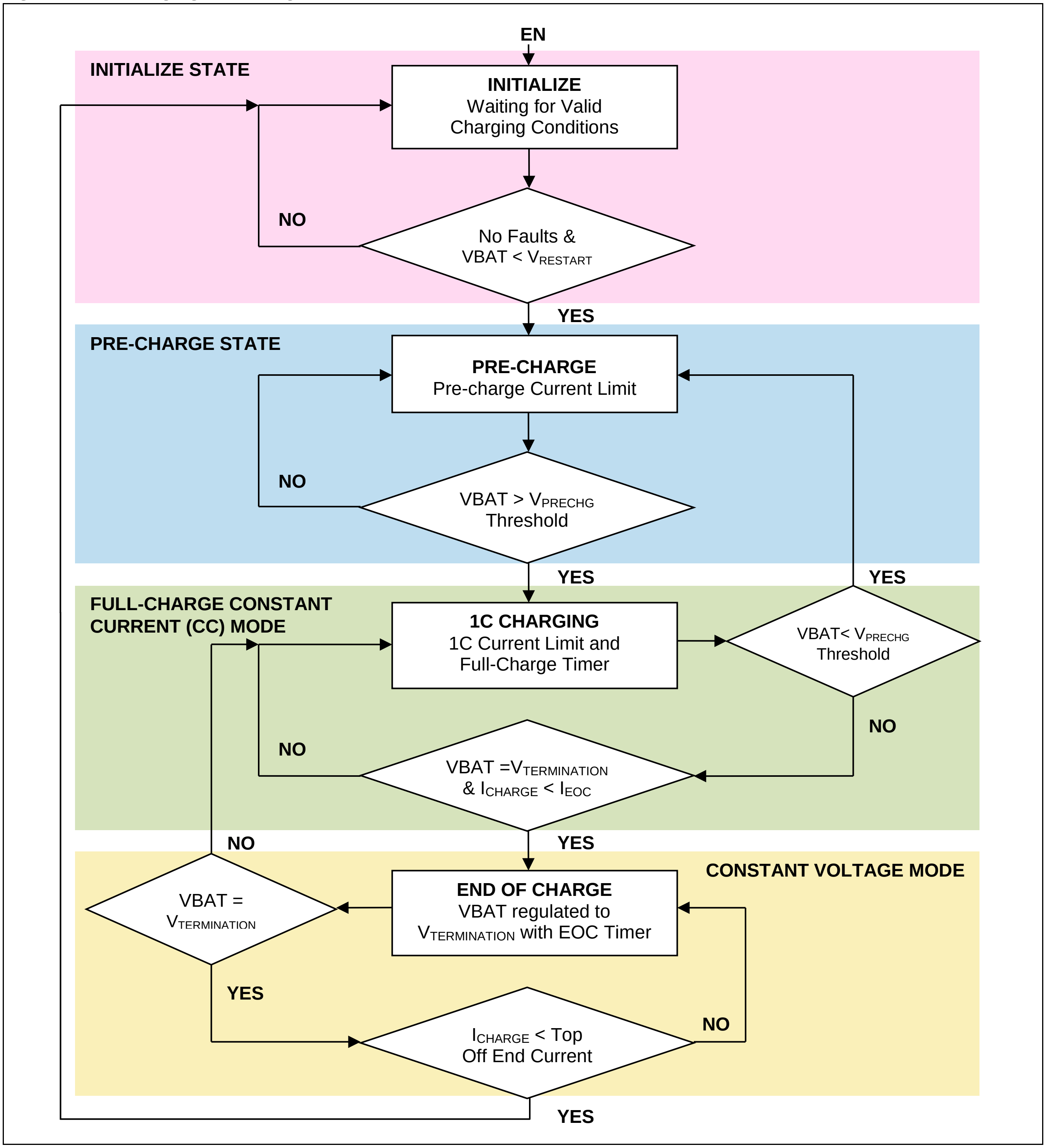
2.2.1. NFLT Pin Functionality

In the event of a battery over-voltage, the battery temperature being outside of the safe charging range, or the full charge timer expiring, charging stops, and the NFLT pin is pulled low. When the fault condition is no longer present, the device will enter the INITIALIZE state (see Figure 2.2), but the NFLT pin will remain low until the STATUS register (00_{HEX}) is read (see Table 2.2). When the STATUS register is read, the NFLT pin will go high until a new fault is detected.

2.2.2. Other Faults

When an open thermistor, thermal shut down, VIN under-voltage, or top-off time-out are detected, charging immediately stops and the corresponding bit in the STATUS register (00_{HEX}) is set. The device enters the INITIALIZE state until the fault is no longer detected.

Figure 2.2 Charging State Diagram



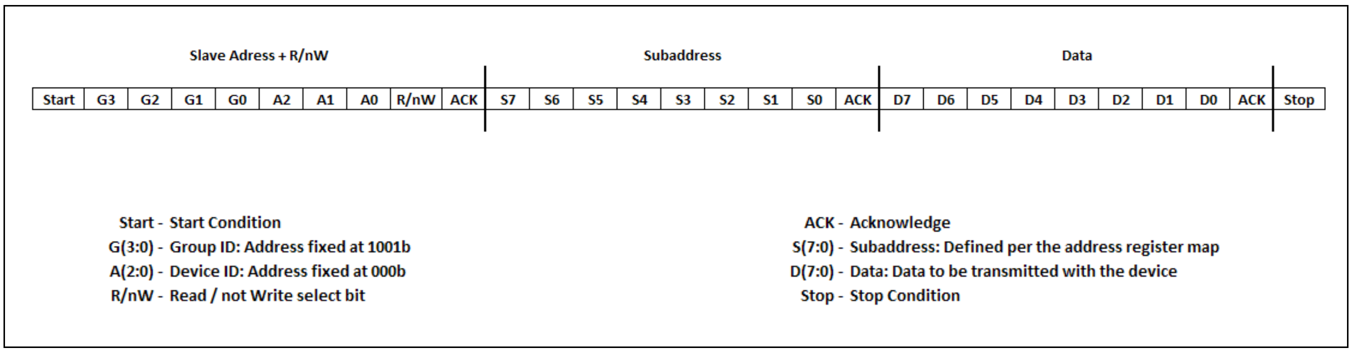
2.3. Serial Interface

The ZSPM4551 features an I^{2}C™ slave interface that offers advanced control and diagnostic features. It supports standard and fast mode data rates and auto-sequencing, and it is compliant to I^{2}C™ standard version 3.0.

I^{2}C™ operation offers configuration control for termination voltages, charge currents, and charge timeouts. This configurability allows optimum charging conditions in a wide range of Li-Ion batteries. I^{2}C™ operation also offers fault and warning indicators. Whenever a fault is detected, the associated status bit in the STATUS register is set and the NFLT pin is pulled low. Whenever a warning is detected, the associated status bit in the STATUS register is set, but the NFLT pin is not pulled low. Reading the STATUS register resets the fault and warning status bits, and the NFLT pin is released after all fault status bits have been reset.

2.3.1. I^{2}C™ Subaddress Definition

Figure 2.3 Subaddress in I^{2}C™ Transmission



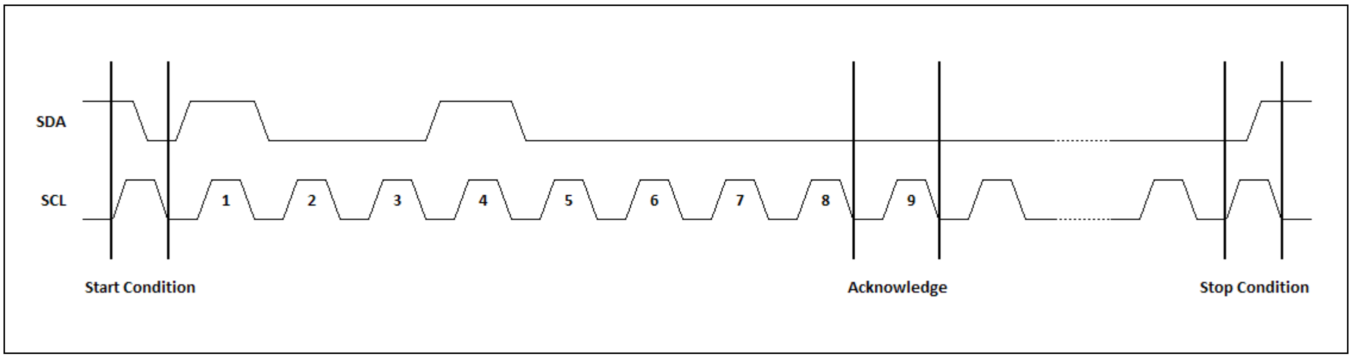
2.3.2. I^{2}C™ Bus Operation

The ZSPM4551's I^{2}C™ is a two-wire serial interface; the two lines are serial clock (SCL) and serial data (SDA) (see Figure 2.4). SDA must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor. The devices communicating on this bus can drive the SDA line low or release it to high impedance. To ensure proper operation, setup and hold times must be met (see Table 1.5). The device that initiates the I^{2}C™ transaction becomes the master of the bus.

Communication is initiated by the master sending a START condition, which is a high-to-low transition on SDA while the SCL line is high. After the START condition, the device address byte is sent, most significant bit (MSB) first, including the data direction bit (read = 1; write = 0). After receiving the valid address byte, the device responds with an acknowledge (ACK). An ACK is a low on SDA during the high of the ACK-related clock pulse. On the I^{2}C™ bus, during each clock pulse, only one data bit is transferred. The data on the SDA line must remain stable during the high pulse of the clock period, as changes in the data line at this time are interpreted as START or STOP control conditions. A low-to-high transition on SDA while the SCL input is high indicates a STOP condition and is sent by the master.

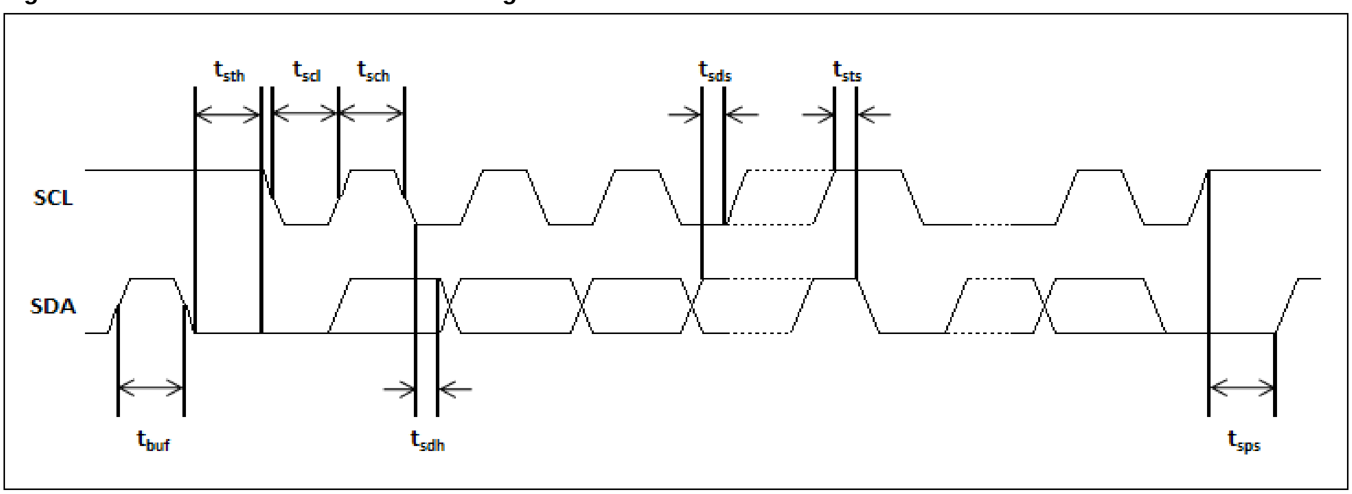
Any number of data bytes can be transferred from the transmitter to receiver between the START and the STOP conditions. Each byte of eight bits is followed by one ACK bit from the receiver. The SDA line must be released by the transmitter before the receiver can send an ACK bit. The receiver that acknowledges must pull down the SDA line during the ACK clock pulse, so that the SDA line is stable low during the high pulse of the ACK-related clock period. When a slave receiver is addressed, it must generate an ACK after each byte is received. Similarly, the master must generate an ACK after each byte that it receives from the slave transmitter. An end of data is signaled by the master receiver to the slave transmitter by not generating an acknowledge after the last byte has been clocked out of the slave. This is done by the master receiver by holding the SDA line high. The transmitter must then release the data line to enable the master to generate a STOP condition.

Figure 2.4 I²C™ Start / Stop Protocol



See Table 1.5 for the definitions and specifications for the timing parameters labeled in Figure 2.5.

Figure 2.5 I²C™ Data Transmission Timing



2.4. Status and Configuration Registers

Table 2.1 Register Descriptions (Device Address = 48_{HEX})

Register	Address	Name	Default	Description
0	00_{HEX}	STATUS	00_{HEX}	Status bit register
1	N/A	N/A	N/A	Register not implemented
2	02_{HEX}	CONFIG1 [1)]	EEPROM	Configuration register
3	03_{HEX}	CONFIG2 [1)]	EEPROM	Configuration register
4	04_{HEX}	CONFIG3 [1)]	EEPROM	Configuration register
5	05_{HEX}	CONFIG4 [1)]	EEPROM	Configuration register
6	06_{HEX}	CONFIG5 [1)]	EEPROM	Configuration register
7-16	N/A	N/A	N/A	Registers not implemented
17	11_{HEX}	CONFIG_ENABLE	00_{HEX}	Enable configuration register access
18	12_{HEX}	EEPROM_CTRL [1)]	00_{HEX}	EEPROM control register

1) CONFIGx and EEPROM_CTRL registers are only accessible when the CONFIG_ENABLE register is written with the EN_CFG bit set to 1 (see Table 2.8).

Table 2.2 STATUS Register—Address 00_{HEX}

Note: All of the STATUS register bits are READ-only.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	BATT_OV	1C_TO	TEMP_0C	TEMP_60C	TSD	TOP_TO	VIN_UV	TH_OPEN

FIELD NAME	BIT DEFINITION [1)]
BATT_OV	VBAT over-voltage.
1C_TO	Full charge timer has timed out.
TEMP_0C	Thermistor indicates battery temperature < 0°C.
TEMP_60C	Thermistor indicates battery temperature > 60°C.
TSD	Thermal shutdown.
TOP_TO	Top-off timer has timed out.
VIN_UV	VIN under-voltage.
TH_OPEN	Thermistor open (battery not present).

1) Faults are defined as BATT_OV, 1C_TO, TEMP_0C, and TEMP_60C. Warnings are defined as TSD, TOP_TO, VIN_UV, and TH_OPEN. Faults cause the NFLT pin to be pulled low. Warnings do not cause the NFLT pin to be pulled low. All status bits are cleared after STATUS register read access. The NFLT pin will go to high impedance (open-drain output) after the STATUS register has been read and all status bits have been reset.

Table 2.3 Configuration Register CONFIG1—Address 02_{HEX}

Note: All of the CONFIG1 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	PRE_CHRG[1:0]		V_TERM_0_10[2:0]			V_TERM_10_45[2:0]		

FIELD NAME	BIT DEFINITION	
PRE_CHRG[1:0] 1)	Pre-charging configuration	00_{BIN} – 50 mA 01_{BIN} – 100 mA 10_{BIN} – 185 mA 11_{BIN} – 370 mA
V_TERM_0_10[2:0] 2)	Voltage termination: 0-10°C configuration	000_{BIN} – 3.94 V 001_{BIN} – 4.00 V 010_{BIN} – 4.05 V 011_{BIN} – 4.10 V 100_{BIN} – 4.12 V 101_{BIN} – 4.15 V 110_{BIN} – 4.18 V 111_{BIN} – Invalid setting
V_TERM_10_45[2:0] 2)	Voltage termination: 10-45°C configuration	

1) *PRE_CHRG Note: Maximum output current when V_{out} < 3.0 V.*
2) *V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.4 for 45-50°C and 50-60°C). For <0°C and >60°C, charging is disabled and a fault is set.*

Table 2.4 Configuration Register CONFIG2—Address 03_{HEX}

Note: All of the CONFIG2 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	EOC[1:0]		V_TERM_45_50[2:0]			V_TERM_50_60[2:0]		

FIELD NAME	BIT DEFINITION	
EOC[1:0] 1)	End of charge configuration	00_{BIN} – 50 mA 01_{BIN} – 100 mA 10_{BIN} – 185 mA 11_{BIN} – 370 mA
V_TERM_45_50[2:0] 2)	Voltage termination: 45-50°C configuration	000_{BIN} – 3.94 V 001_{BIN} – 4.00 V 010_{BIN} – 4.05 V 011_{BIN} – 4.10 V 100_{BIN} – 4.12 V 101_{BIN} – 4.15 V 110_{BIN} – 4.18 V 111_{BIN} – Invalid setting
V_TERM_50_60[2:0] 2)	Voltage termination: 50-60°C configuration	

1) *EOC Note: Maximum output current when V_{OUT} < 3.0 V.*
2) *V_TERM Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C (see Table 2.3 for 0-10°C and 10-45°C). For <0°C and >60°C, charging is disabled and a fault is set.*

Table 2.5 Configuration Register CONFIG3—Address 04_{HEX}

Note: All of the CONFIG3 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	MAX_CHRG_CURR_0_10[3:0]				MAX_CHRG_CURR_10_45[3:0]			

FIELD NAME	BIT DEFINITION		
MAX_CHRG_CURR_0_10[3:0] [1)]	Maximum charge current: 0-10°C configuration	0000_{BIN} – 50 mA 0001_{BIN} – 100 mA 0010_{BIN} – 200 mA 0011_{BIN} – 300 mA 0100_{BIN} – 400 mA 0101_{BIN} – 500 mA 0110_{BIN} – 600 mA 0111_{BIN} – 700 mA	1000_{BIN} – 800 mA 1001_{BIN} – 900 mA 1010_{BIN} – 1000 mA 1011_{BIN} – 1100 mA 1100_{BIN} – 1200 mA 1101_{BIN} – 1300 mA 1110_{BIN} – 1400 mA 1111_{BIN} – 1500 mA
MAX_CHRG_CURR_10_45[3:0] [1)]	Maximum charge current; 10-45°C configuration		

1) *MAX_CHRG_CURR Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C, and 50-60°C (see Table 2.6 for 45-50°C and 50-60°C). For <0°C and >60°C, charging is disabled and a fault is set.*

Table 2.6 Configuration Register CONFIG4—Address 05_{HEX}

Note: All of the CONFIG4 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	MAX_CHRG_CURR_45_50[3:0]				MAX_CHRG_CURR_50_60[3:0]			

FIELD NAME	BIT DEFINITION		
MAX_CHRG_CURR_45_50[3:0] [1)]	Maximum charge current: 45-50°C configuration	0000_{BIN} – 50 mA 0001_{BIN} – 100 mA 0010_{BIN} – 200 mA 0011_{BIN} – 300 mA 0100_{BIN} – 400 mA 0101_{BIN} – 500 mA 0110_{BIN} – 600 mA 0111_{BIN} – 700 mA	1000_{BIN} – 800 mA 1001_{BIN} – 900 mA 1010_{BIN} – 1000 mA 1011_{BIN} – 1100 mA 1100_{BIN} – 1200 mA 1101_{BIN} – 1300 mA 1110_{BIN} – 1400 mA 1111_{BIN} – 1500 mA
MAX_CHRG_CURR_50_60[3:0] [1)]	Maximum charge current: 50-60°C configuration		

1) *MAX_CHRG_CURR Note: There are separate settings for battery temperatures 0-10°C, 10-45°C, 45-50°C , and 50-60°C (see Table 2.5 for 0-10°C and 10-45°C). For <0°C and >60°C, charging is disabled and a fault is set.*

Table 2.7 Configuration Register CONFIG5—Address 06_{HEX}

Note: All of the CONFIG5 register bits are READ/WRITE.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	TOP_END	TH	TOP_TO[2:0]			1C_TO[2:0]		

FIELD NAME	BIT DEFINITION
TOP_END [1]	Top-off end configuration 0_{BIN} – 25 mA 1_{BIN} – 92 mA
TH [2]	Thermistor configuration 0_{BIN} – 10kΩ 1_{BIN} – 100kΩ
TOP_TO[2:0] [3]	Top off timer time out configuration 000_{BIN} – 0 minutes 001_{BIN} – 20 minutes 010_{BIN} – 40 minutes 011_{BIN} – 60 minutes 100_{BIN} – 80 minutes 101_{BIN} – 100 minutes 110_{BIN} – 120 minutes 111_{BIN} – Disable time out timer
1C_TO[2:0] [4]	Full charge timer time out configuration 000_{BIN} – Disable full charge timer 001_{BIN} – 200 minutes 010_{BIN} – 400 minutes 011_{BIN} – 600 minutes 100_{BIN} – 800 minutes 101_{BIN} – 1000 minutes 110_{BIN} – 1200 minutes 111_{BIN} – 1400 minutes

1) *TOP_END Note: Charging stops when $V_{VBAT} = V_{TERMINATION}$ and I_{BAT} < TOP_END*
2) *TH Note: Setting for nominal thermistor and reference resistor value.*
3) *TOP_TO Note: Timer starts when VBAT = $V_{TERMINATION}$ and I_{BAT} < EOC.*
4) *1C_TO Note: Timer starts when VBAT > 3.0V.*

Table 2.8 Enable Configuration Register CONFIG_ENABLE—Address 11_{HEX}

Note: The reset value for all of the CONFIG_ENABLE register bits is 0.

DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	Not used	EN_CFG
READ/WRITE	R	R	R	R	R	R	R	R/W

FIELD NAME	BIT DEFINITION
EN_CFG	Enable-access control bit for configuration registers CONFIG1 through CONFIG5 (addresses 02_{HEX} to 06_{HEX}) 0_{BIN} – Disable access 1_{BIN} – Enable access

Table 2.9 EEPROM Control Register EEPROM_CTRL—Address 12_{HEX}

Note: The reset value for all of the EEPROM_CTRL register bits is 0.

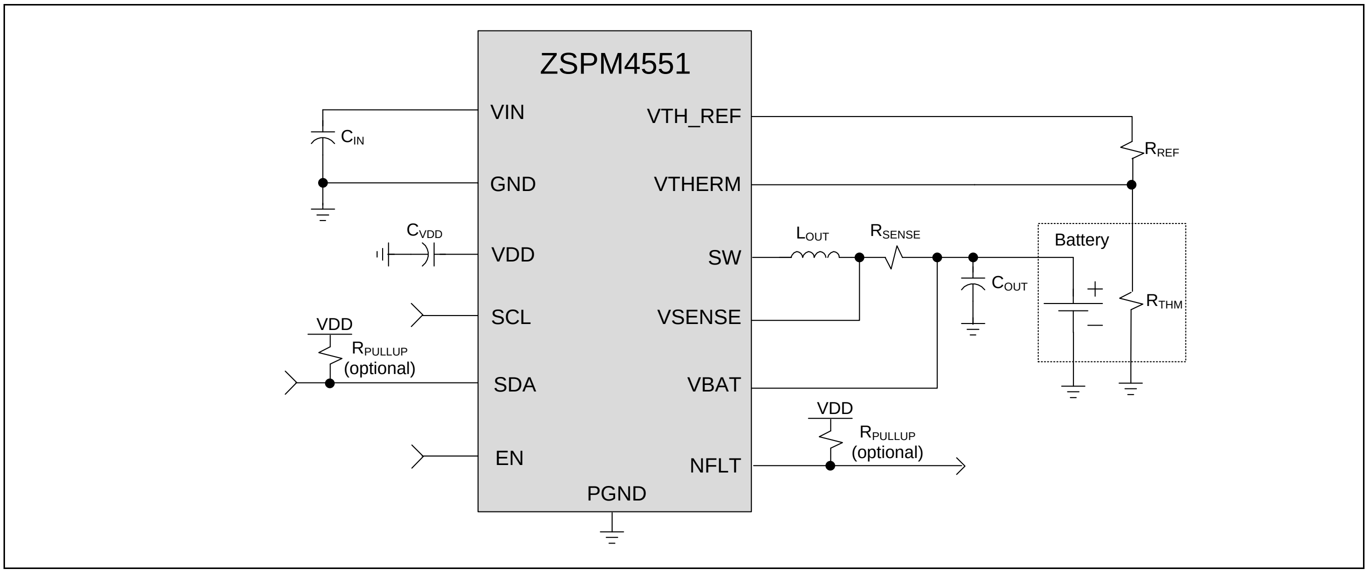
DATA BIT	D7	D6	D5	D4	D3	D2	D1	D0
FIELD NAME	Not used	Not used	Not used	Not used	Not used	Not used	Not used	EE_PROG
READ/WRITE	R	R	R	R	R	R	R	R/W

FIELD NAME	BIT DEFINITION
EE_PROG [1)]	EEPROM program control bit for configuration registers CONFIG1 through CONFIG5 (addresses 02_{HEX} to 06_{HEX}) 0_{BIN} – Disable EEPROM programming 1_{BIN} – Enable EEPROM programming with data from configuration registers CONFIG1 through CONFIG5 (addresses 02_{HEX} to 06_{HEX})
1) EE_PROG Note: Inputs VIN and EN must be present for 200ms.	

3 Application Circuits

3.1. Typical Application Circuit

Figure 3.1 Typical Application Circuit for Charging a Lithium-Ion Battery



3.2. Selection of External Components

Note that the internal compensation is optimized for a 4.7µF output capacitor (C_{OUT}) and a 4.7µH output inductor (L_{OUT}). Table 1.3 provides recommended ranges for most of the following components.

3.2.1. C_{OUT} Output Capacitor

To keep the output ripple low, a low ESR (less than 35mΩ) ceramic capacitor is recommended for the 4.7µF output filter capacitor. The ESR should not exceed 100mΩ.

3.2.2. L_{OUT} Output Inductor

For best performance, an inductor with a saturation current rating higher than the maximum V_{OUT} load requirement plus the inductor current ripple should be used for the 4.7µH output filter inductor.

3.2.3. C_{IN} Bypass Capacitor

For best performance, a low ESR ceramic capacitor should be used for the 10µF input supply bypass capacitor. If it is not a low ESR ceramic capacitor, a 0.1µF ceramic capacitor should be added in parallel to C_{IN}.

3.2.4. C_{VDD} Bypass Capacitor for VDD Internal Reference Voltage Output

For best performance, a low ESR ceramic capacitor should be used for the 100nF bypass capacitor from the VDD pin to ground.

3.2.5. R_{SENSE} Output Sensing Resistor

The typical value for the output sensing resistor is 50mΩ.

3.2.6. Pull-up Resistors

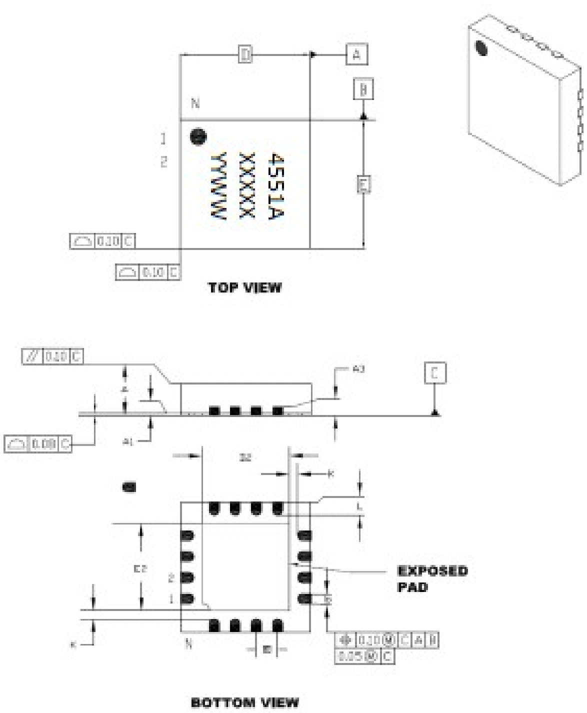
For proper function of the I²C™ interface, the SDA pin must be connected to a positive supply (e.g., the VDD pin) through an external pull-up resistor.

For proper function of the fault warning signal on the NFLT pin, it must be connected to a positive supply (VDD) through an external pull-up resistor.

4 Pin Configuration and Package

4.1. ZSPM4551 Package Dimensions

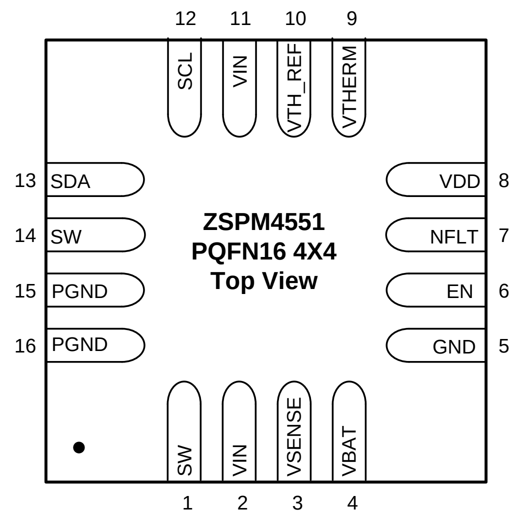
Figure 4.1 PQFN-16 Package Dimensions



Units		MILLIMETERS		
Dimensions Limits		MIN	NOM	MAX
Number of Pins	N		16	
Pitch	e		0.65 BSC	
Overall Height	A	0.80	0.90	1.00
Standoff	A1	0.00	0.02	0.05
Contact Thickness	A3		0.20 REF	
Overall Length	D		4.00 BSC	
Exposed Pad Width	E2	2.55	2.70	2.80
Overall Width	E		4.00 BSC	
Exposed Pad Length	D2	2.55	2.70	2.80
Contact Width	b	0.25	0.30	0.35
Contact Length	L	0.30	0.40	0.50
Contact-to-Exposed Pad	K	0.20	-	-

4.2. Pin-Out Assignments

Figure 4.2 ZSPM4551 Pin Assignments



4.3. Pin Description for 16-Pin PQFN (4 x 4 mm)

Table 4.1 Pin Description

Pin #	Name	Function	Description
1	SW	Switching Voltage Node	Connect to 4.7µH (typical) inductor L_{OUT}. Also connect to additional SW pin 14.
2	VIN	Input Voltage	Input voltage. Also connect to C_{IN}. Also connect to additional VIN pin 11.
3	VSENSE	Current Sense Positive Input	Positive input for the current loop.
4	VBAT	Output Voltage	Regulator feedback input.
5	GND	GND	Primary ground for the majority of the device except the low-side power FET.
6	EN	Enable Input	When EN is high (≥ 2.2V), the device is enabled. Ground the pin to disable the device. Includes internal pull-up.
7	NFLT	Inverted Fault	Open-drain output.
8	VDD	Internal 3.3V Supply Output	Connect to a 100nF capacitor to GND.
9	VTHERM	Battery Temperature Sensor Minus Node	Negative node for the thermistor, which must be located in close proximity to the battery.

Pin #	Name	Function	Description
10	VTH_REF	Battery Temperature Sensor Positive Node	Positive node for the thermistor, which must be located in close proximity to the battery.
11	VIN	Input Voltage	Additional VIN pin for input voltage; connect to VIN pin 2.
12	SCL	Clock Input	I^2C™ clock input.
13	SDA	Data Input/Output	I^2C™ data (open-drain output).
14	SW	Switching Voltage Node	Additional SW pin; connect to SW pin 1.
15	PGND	Power GND	GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 16.
16	PGND	Power GND	GND supply for internal low-side FET/integrated diode. Also connect to additional PGND pin 15.

4.4. Package Markings

Figure 4.3 Marking Diagram 16-Pin PQFN (4 x 4 mm)

4551A
XXXXX
oYYWW

XXXXX:	Lot Number (last five digits)
O:	Pin 1 mark
YY:	Year
WW:	Work Week

5 Layout Recommendations

To maximize the efficiency of this package for application on a single layer or multi-layer PCB, certain guidelines must be followed when laying out this part on the PCB.

5.1. Multi-Layer PCB Layout

The following are guidelines for mounting the exposed pad ZSPM4551 on a multi-layer PCB with ground a plane. In a multi-layer board application, the thermal vias are the primary method of heat transfer from the package thermal pad to the internal ground plane. The efficiency of this method depends on several factors, including die area, number of thermal vias, and thickness of copper, etc.

Figure 5.1 Package and PCB Land Configuration for Multi-Layer PCB

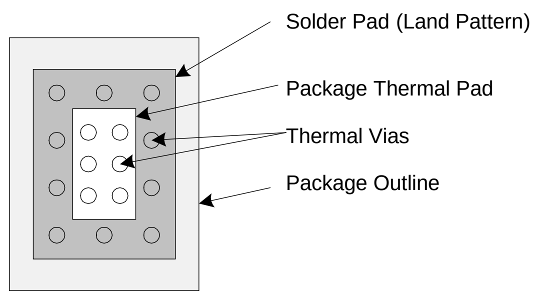


Figure 5.2 JEDEC Standard FR4 Multi-Layer Board – Cross-Sectional View

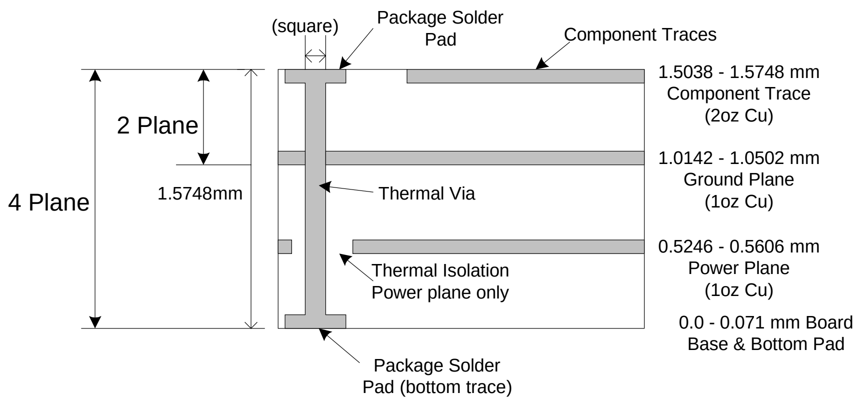
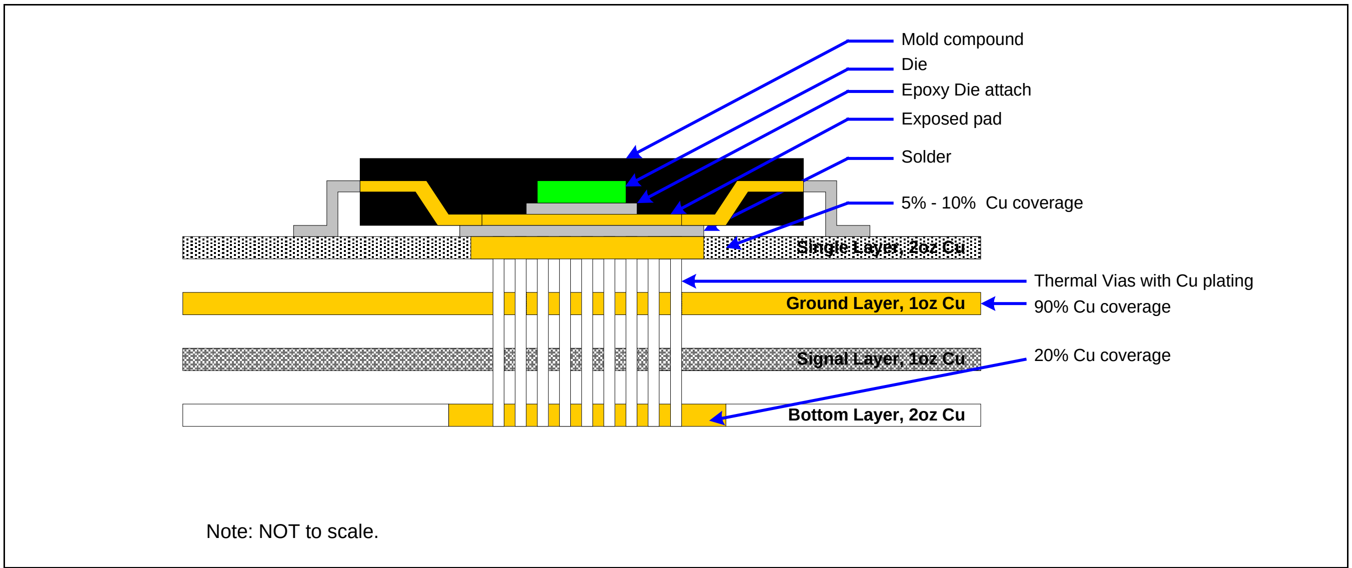


Figure 5.3 is a representation of how the heat can be conducted away from the die using an exposed pad package. Each application will have different requirements and limitations, and therefore the user should use sufficient copper to dissipate the power in the system. The output current rating for the linear regulators might need to be de-rated for ambient temperatures above 85°C. The de-rated value will depend on calculated worst case power dissipation and the thermal management implementation in the application.

Figure 5.3 Conducting Heat Away from the Die using an Exposed Pad Package

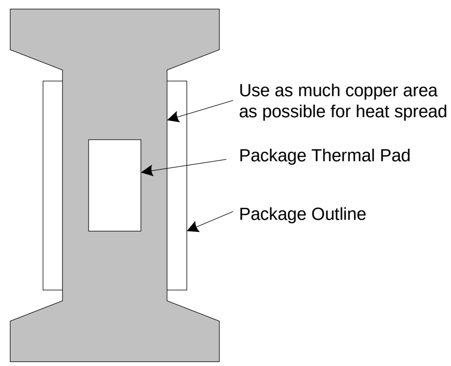


5.2. Single-Layer PCB Layout

Layout recommendations for a single-layer PCB: Utilize as much copper area for power management as possible. In a single-layer board application, the thermal pad is attached to a heat spreader (copper areas) by using a low thermal impedance attachment method (solder paste or thermal conductive epoxy).

In both of the methods mentioned above, it is advisable to use as much copper trace as possible to dissipate the heat.

Figure 5.4 Application Using a Single-Layer PCB



Important: If the attachment method is NOT implemented correctly, the functionality of the product is NOT guaranteed. Power dissipation capability will be adversely affected if the device is incorrectly mounted onto the circuit board.

6 Ordering Information

Ordering Code	Description	Package
ZSPM4551AA1W	ZSPM4551 High-Efficiency Charger for Li-Ion Batteries	16-pin PQFN / 7" Reel (1000 parts)
ZSPM4551AA1R	ZSPM4551 High-Efficiency Charger for Li-Ion Batteries	16-pin PQFN / 13" Reel (3300 parts)
ZSPM4551KIT	ZSPM4551 Evaluation Kit	

7 Related Documents

Document
ZSPM4551 Feature Sheet
ZSPM4551 Evaluation Kit Description
ZSPM4551 Application Note – Li-Ion Battery Charging Applications

Visit IDT's website www.IDT.com or contact your nearest sales office for the latest version of these documents.

8 Document Revision History

Revision	Date	Description
1.00	December 4, 2012	First release.
1.01	October 3, 2014	Revision of specification for VTH_REF output voltage in Table 1.4. Updates for contact information and imagery on cover and headers.
	January 29, 2016	Changed to IDT branding.

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