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ClockMatrix TDC

This document explains how to use the Input and Output Time-to-Digital Converters (TDCs) in <u>ClockMatrix</u> devices. It is intended to complement the <u>ClockMatrix TDC Application Note</u>.

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1. Input TDC

1.1 Main Screen

8A34001 / 8A34001P V8.0.0 Firmware: PR4.8.6 Display input and output labels 🔲 📑		50MHz	Configure GPIOs Configure Output Power Estimate Configure Input T Configure PWM Scratch Registe
Quick View		SYS APLL 13.5GHz System DPLL XO	To DCOs Disable Unused Channe Configure 800MHz
Enable Frequency	25MHz	Channel 0 DPLL Mode	Configure
С.K8 -	25MHz	Channel 1	Configure
Сске -		DPLL Mode	
		Channel 2 Phase Measurement	Configure
🖆 📃 🚰 сікз –			

- Any channel can be used for Phase Measurement mode (i.e., to measure the phase between two different inputs).
- Outputs are still useable for Synthesizer or DCO (FCW) mode when in Phase Measurement mode.

1.2 CH2 Phase Measurement Mode

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- Clk0 and CLK1 are used for Phase Measurement mode and must be the same frequency.
- Two types:
 - Phase Status has a resolution of 50ps.
 - Filter Status has a resolution of less than 1ps.
- Resolution is the step size.
- Filter Status is only activated when High Precision mode is enabled (see section 1.3).
- The "read" button gives the phase difference between CLK0 and CLK1.

	Channel 2	💼 🎦 Global Sync Enable
Mode of Operation: Phase Measurement		
Phase Measurement Low precision (configure Input TDC to switch to high precis REF: CLK0 PHASE_STATUS PHASE_STATUS Phase Measurement Phase Status Phase Status Pha		DCO.Omly DCO.Omly H35GHz PCO PCO PCO
	Combo Mode - Slave	Enable secondary combo source
	Clocks to Measure read Reference Clock: CLK0 Feedback Clock: CLK1 ♥ Phase Status: Ops	
		ToD Synchronization Enable:

1.3 Registers

- Input TDC Reference source can use the XTAL or the XO_DPLL (if available).
- The TDC source determines the accuracy.
- For small phase offsets using phase measurement such as 1ns or 1ps, XTAL or XO_DPLL does not make a difference.
- For large phase offsets such as 1us or 1ms, XTAL or XO_DPLL makes a difference

	XTAL	XO DPLL
Phase Offset	50 ppm	5 ppm
1.00E-03	5.00E-08	5.00E-09
1.00E-06	5.00E-11	5.00E-12
1.00E-09	5.00E-14	5.00E-15
1.00E-12	5.00E-17	5.00E-18



- Enabling High Precision mode activates Loop Filter Status for increased resolution (50ps to < 1ps).
- Resolution is the step size.
- If High Precision mode is OFF, TDC frequency is 625MHz by default.
- If High Precision mode is ON, TDC frequency is skewed such that it is not an integer multiple of the input frequency (for more information, see the *ClockMatrix TDC Application Note*).
- Enabling High Precision mode prevents DCO (FCW) access, but Synthesizer still available.



1.4 Reading a Measurement

- Enabling High Precision mode activates Loop Filter Status for increased resolution (50ps to < 1ps).
- Resolution is the step size.
- If High Precision mode is OFF, TDC frequency is 625MHz by default.
- If High Precision mode is ON, TDC frequency is skewed such that it is not an integer multiple of the input frequency (for more information, see the *ClockMatrix TDC Application Note*).
- Enabling High Precision mode prevents DCO (FCW) access, but Synthesizer still available.

		Channel 2	🔲 🚰 Global Sync Enable
ode of Operation:	Phase Measurement		ر <u>ا</u> ل
Phase Measurem figh precision (confi REF. CLK0	nent gure Input TDC to switch to low p PHASE_STATUS Decimator	PLITER_STATUS	DCO Only 13.5GP III 25GP III 25GP III 25GP III 25GP III 25GP III 25GP III 25GP
		Combo Mode - Slave	Enable secondary combo source
		Clocks to Measure Reference Clock: CLK0 Feedback Clock: CLK1 Phase Satus: 1.05ms Loop Filter Status: 1.06ms	
			ToD Synchronization Enable:

2. Output TDC

2.1 Main Screen

/8A34001P V8.0.0 : PR4.8.8 nput and output labels 💿 💼	TCXO/OCXO 49.152MHz	Power Estimate Configur	e Input TDC TOD2 I Registers TOD1 TOD3	EEPROMUMAY
ok View	SYS APLL 13.4676GHz System DPLL xo	To DCOs Disable Unuse	d Channels DCO frequencies and output dividers that outputs. To speed up entry of output freq finder until you have entered all outputs, i	can provide the desired encies, disable the solution and then enable it again.
Frequency	CLK0 Channel 0 500MHz	Configure	500MHz 00 10MHz •	enable: C G hood LVOS 1.8V
сия	DPLL Mode Combo: Syste	m DPLL	500MHz at 500MHz	enable: Desired:
CLK1	<u>Channel 1</u> 1000MHz Synthesizer	Configure	1000MHz 02 10MHz	enable: C G Desired:
	Channel 2 750MHz	m DPLL Channel 0 Configure 0	1000MHz 03 20MHz •	enable: Desired:
сиз		m DPLL Channel 0	750MHz • C1 25MHz •	enable: Desired:
CLK11	<u>Channel 3</u>	Configure		LVDS 1.8V

- Output TDCs enable output alignment of outputs from different channels.
- The example below aligns Q0, Q2, and Q4.
- Outputs from the same channel are obviously aligned and do not require a TDC: Q0 and Q1 or Q2 and Q3.

2.2 Masters and Slaves

- Master and slave satellites are assumed and are connected through the combo bus.
- Master normally has an input (Ch0):
 - DPLL mode
- Satellite slaves (Ch1 and CH2) follow the master (Ch0):
 - Synthesizer, DCO (FCW/PCW), or Phase Measurement mode
- Any stimulus on the master is propagated to the slaves through the combo mode.
- Combo mode passes only frequency (change in phase).
- Combo mode does not pass edge information.





2.3 Combo Bus



- All three Channel Combo configs are shown above.
- Ch0 has one master: sysDPLL.
- Ch1 and Ch2 have two masters each: Ch0 and sysDPLL.
- Slaves always inherit the master of its master (since Ch0 has sysDPLL as its master, Ch1 and Ch2 must also have sysDPLL as their master as well as Ch0).

2.4 Master Divider Frequency

Channel 0	Global Sync Enable	Channel 1	🔽 🎦 Global Sync Enable	Channel 2	Global Sync Enable
	<u>ل</u>	× 🖻	ų (L)		d u h
DCO Config for Channel 0	SYS APLL	DCO Config for Channel 1	SYS APLL	DCO Config for Channel 2	SYS APLL
Goal DCO Frequency: 500	13.4676GHz	Goal DCO Frequency:	13.4676GHz	Goal DCO Frequency: 750	13.4676GHz
Fractional Divider	500MHz	Fractional Divider	1000MHz	Fractional Divider	750MHz
Numerator (M): 32767500000000 5 Denominator (N): 65535 5		Numerator (M): 6553500000000 65535 Denominator (N): 65535 6		Numerator (M): 49151250000000	
Actual DCO Frequency: 500MHz		Actual DCO Frequency: 1000MHz		Denominator (N): 65535	
Master Divider: 100		Master Divider: 200		Master Divider: 150	

- For alignment to occur, the output of the master divider must all be the same frequency for every channel involved:
 - Ch0 MD frequency = 500MHz/100 = 5MHz
 - Ch1 MD frequency = 1000MHz/200 = 5MHz
 - Ch2 MD frequency = 750MHz/150 = 5MHz
- The higher the master divider frequency, the faster the alignment.
- The master divider frequency must be a common factor of each output frequency:
 - 5MHz is a factor of Q0 = 10MHz, Q2 = 10MHz, and Q4 = 25MHz

2.5 Global Sync Enable (GSE)

Channel 0 ✓	🖉 🙆 Global Sync Enable	Channel 1	🖉 🦳 Global Sync Enable	Channel 2	🖉 🦳 Global Sync Enable
×	d <u>D</u> b		d Dh		, Ch
DCO Config for Channel 0	SYS APLL	DCO Config for Channel 1	SYS APLL 13.4676GHz	DCO Config for Channel 2	SYS APLL 13.4676GHz
Goal DCO Frequency: 500 😭	13.4676GHz	Goal DCO Frequency: 1000	(13.40/rbuHz)	Goal DCO Frequency: 750	
Fractional Divider Numerator (M): 32767500000000	S00MHz	Fractional Divider Numerator (M): 6553500000000	1000MHz	Fractional Divider Numerator (M): 49151250000000	750MHz
Denominator (N): 65535		Denominator (N): 65535		Denominator (N): 65535	
Actual DCO Frequency: 500MHz Master Divider: 100		Actual DCO Frequency: 1000MHz Master Divider: 200		Actual DCO Frequency: 750MHz Master Divider: 150	

- GSE must be enabled for all channels involved.
- GSE performs the initial snap to align all outputs (coarse phase alignment).

2.6 Configuration

T	CXO/OCXO 12.8MHz	49.1521	1	Configure GP Power Estima Configure PV	ate Con	igure Outp figure Inpi ratch Reg		Configur TOD0 TOD1	TOD3		Configure Seria		vare Utility
					Output	TDC C	onfig						
Enable Output T Reference Clock		L 🗸 🖸	Fast Lock Enable	Delay:	0 🗂	500µs	Fast Lock [) isable Delay:		0 🚰 500µs		read	1
	Source	<u>Target</u>	Mode		Type		<u>Align Reset</u>			<u>Samples</u> (0 == 4096)	<u>Target Phase</u> Offset	Measurement Status	Go
Output TDC 0	DPLL0 ~	DPLL0 ~	alignment	contin	nuous Y	keep	accumulated	Align	ment Mask	0	• •		
Output TDC 1	DPLL0 ~	DPLL0 Y	measurement	_					x nt Mask			0] 🖬 🔂
Output TDC 2	DPLLO Y	DPLLO Y	measurement	✓ sinc		-	Alignmen	-	nt Mask	0	0	0] 🗆 🔁
Output TDC 3		DPLLO Y	measurement	Sinc	DPLL0		DPLL4 DPLL5		nt Mask	0		0	1 🗆 🗃
output for 5			measurement		DPLL2	2	DPLL6			2			
		Synthesize	r		DPLL3		DPLL7						
		Combo: Sj	ystem DPLL	Channel 0	Align Target	Mask	00000	110	251	H7 . N		enable: 🔽 📑 D	esired:

- Up to four different Output TDCs can be used individually.
- Output TDCs perform fine phase alignment.
- The Enable and Go buttons must be checked. Order is not important if saving to a TCS file. If connected to a device, the Go button must be last button clicked in entire box.

nable Output T	DC: 🛛 🖸				Output	TDC C	onfig						
eference Clock		LL 👻 🎦	Fast Lock Enable Dela	iy:	0 📑	500µs	Fast Lock	DisableDela	iy:	0 👩 500µs		read	
	Source	<u>Target</u>	Mode		Туре		Align Reset			<u>Samples</u> (0 == 4096)	<u>Target Phase</u> <u>Offset</u>	Measurement Status	Go
Output TDC 0	DPLLO ~	DPLLO Y	alignment 🛛 🖌	contir	nuous 👻		accumulate	d 🗡 🗛	gnment Mask	۰ ۲	0	0] 🛛 🕻
output TDC 1	DPLLO ~	DPLLO Y	measurement Y	sinc					x nt Mask	0	0	0] 🗆 (
utput TDC 2	DPLLO Y	DPLLO Y	measurement Y	sind			Alignmen DPLL4	nt Mask	nt Mask	۰ ۲	ہ 21	0] 0(
utput TDC 3	DPLLO Y	DPLLO Y	measurement ¥	sind					nt Mask	0	0	0	
		/bumHz Synthesizer		-(DPLL3 (> nQ3		

- Reference clock: XO_DPLL or XTAL. Select XO_DPLL for better accuracy, if possible.
- Source: DPLL0 is the Source (master) in this example.
- Mode: choose Alignment ode to align all slaves.
- When Alignment mode is chosen, Target is ignored and Alignment Mask selects the slaves.
- Measurement mode is for measuring the phase between the Source and Target.
- Type: Select continuous for continuous alignment instead of a single alignment.
- Samples: 0 selects 4096 samples.

Note: More samples means more averaging.

2.7 Visuals

System DPLL ○	Configure
Channel 0 500MHz DPLL Mode	Configure
Combo: System DPLL	
Channel 1 1000MHz Synthesizer	Configure
Combo: System DPLL	Channel 0
Channel 2 750MHz	Configure
Synthesizer	
Combo: System DPLL	Channel 0

- 0* indicates the Source for Output TDC 0.
- 0 indicates the Alignment Mask Slaves for Output TDC 0.

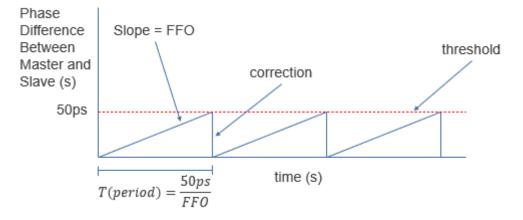
2.8 Initial Alignment Time (Single Shot)

 $Time_{Output \ TDCAlign} = \frac{N_{samples}N_{slaves}}{\min(10kHz, MDF)}$

The equation calculates the initial alignment time (single shot mode):

- Subsequent alignments (continuous mode) are not included
- Nsamples is the number of samples used for averaging
- MDF is the Master Divider Frequency
- N_{slaves} is the number of slaves or satellites being used
- Global Sync Enable (GSE) is assumed to be enabled
- GSE performs initial coarse phase adjustment (large output jumps)
- Output TDC performs fine phase adjustment (small output jumps)
- Output TDC Status Register will report when the alignment is done, but that time may be 2x the above time if samples have an average above the threshold of 50ps

2.9 Phase Correction



- TDC mechanism only adjusts the phase of the satellite channel when it drifts by more than 50ps.
- The 50ps threshold is fixed
- Truncation error when DCO frequencies are different can be up to 0.0032ppt, which would mean a correction every 4.3 hours. In reality the truncation error can be smaller depending on actual DCO frequencies.
- The correction happens at a maximum speed of 244ppm or 244 us/s.

3. Revision History

Revision	Date	Description
1.00	Nov 23, 2022	Initial release.

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