ISL6244EVAL1 Multi-phase Evaluation Board Setup Procedure

Application Note | September 2003 | AN1077

This document describes the setup procedure for the ISL6244EVAL1 Rev B board for AMD Mobile K8 Processors.

Description

The AMD Hammer family microprocessors feature higher clock speeds and greater device density than previous product families. The power management solution for this next generation family of microprocessors must contend with lower core voltages, tighter transient specifications, and higher peak current demands. Responding to the changing power management needs of its customers, Intersil introduces the ISL6244 controller to power the AMD Hammer family microprocessors.

Intersil ISL6244 and ISL6207

The ISL6244EVAL1 Rev B is a versatile voltage regulator-down (VRD) design. The evaluation board comes configured for 3-phase multi-phase buck operation, designed to meet AMD Hammer Family Desktop Processor specifications. The board layout supports removal or addition of the third and fourth phases to support multiple applications. The ISL6244 controller features are specifically designed to compliment and support the Hammer Family processors. Interfaced with ISL6207 drivers, the chipset forms a highly integrated solution for AMD Hammer processor applications.

The ISL6244 regulates output voltage and balances load currents for two to four synchronous buck converter channels. The controller features a 5-bit DAC which provides a digital interface for accurate step down conversion over the entire Hammer Family range of 0.800V to 1.550V. New multi-phase family features include differential remote output voltage sensing to improve regulation tolerance, pin-adjustable reference offset for ease of implementation, VID-on-the-Fly to respond to DAC changes during operation, and optional load line regulation. For a more detailed description of the ISL6244 functionality, refer to the data sheet [1].

The ISL6207 driver is chosen to drive two N-Channel power MOSFETs in a synchronous-rectified buck converter channel. Each channel has a single logic input which controls the upper and lower MOSFETs. Dead time is optimized on both switching edges to provide shoot-thru protection. Internal bootstrap circuitry only requires an external capacitor and provides better enhancement of the upper MOSFET. For a more detailed description of the ISL6207, refer to the data sheet [1].

The Intersil multi-phase family driver portfolio continues to expand with new selections to better fit our customer's needs.

1. Refer to our website for updated information, the ISL6207 data sheet, and the ISL6244 data sheet: **www.intersil.com**.

Features

- Multi-Phase Power Conversion
  - 2, 3 or 4 Phase Operation
- Precision $r_{DS(ON)}$ Current Sharing
  - Lossless
  - Low Cost
- Precision CORE Voltage Regulation
  - Differential Remote Output Voltage Sensing
  - Programmable Reference Offset
  - ±1% System Accuracy
- Programmable Droop Voltage
- Excellent Dynamic Response
  - Combined Input Voltage Feed-Forward and Pulse-by-Pulse Average Current Mode

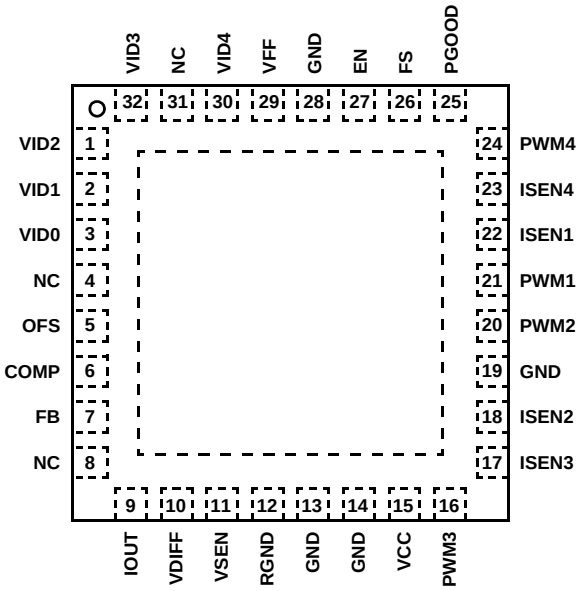
Ordering Information

PART NUMBER	TEMP. (^{O}C)	PACKAGE	PKG. DWG. #
ISL6244CR	0 to 70	32 Ld QFN	L32.5X5
ISL6244CRZ	0 to 70	32 Lead-Free QFN	L32.5X5
ISL6244HR	-10 to 100	32 Ld QFN	L32.5X5
ISL6244HRZ	-10 to 100	32 Lead-Free QFN	L32.5X5

NOTE: Add "-T" suffix for 32 QFN 5x5 Tape and Reel packages.

Pinout

ISL6244CR
(32 LEAD QFN 5X5)
TOP VIEW



NC = NO CONNECT

What's Inside

The Evaluation Board Kit contains the following materials:

- The ISL6244 EVAL Board
- The ISL6244 Evaluation Board document

What is Needed

The following materials will be needed to perform testing:

- 1 to 2 electronic loads [see note]
  - 0-25V @ 15A (+VDC)
  - 0-5V @ 5A (+5V)
  - 0-12V @ 1A (+12V)
- precision digital multi-meters

NOTE: amperage rating of power supplies are determined by maximum expected loading plus a percentage margin of error

Quick Setup Guide

Step 1: Set the 0-5V power supply to +5V and place in the "STANDBY" or "OFF" position. Connect the positive terminal (+) of the supply to the +5V terminal J5 and the negative terminal (-) of the supply to GND J7.

Step 2: Connect the positive terminal (+) of a DMM to the +5V terminal J5 and the negative terminal (-) to the GND terminal J7.

Step 3: Set the +VDC power supply to +19V and place in the "STANDBY" or "OFF" position. Connect the positive terminal (+) of the supply to the +VDC terminal J3 and the negative terminal (-) of the supply to GND J4.Connect the load

Step 4: Connect the positive terminal (+) of a DMM to the +VDC terminal J3 and the negative terminal (-) to the GND terminal J4.

Step 5: Set the 0-12V power supply to +12V and place in the "STANDBY" or "OFF" position. Connect the positive terminal (+) of the supply to the +12V terminal J6 and the negative terminal (-) of the supply to GND J8.

Step 6: Connect the positive terminal (+) of a DMM to the +5V terminal J5 and the negative terminal (-) to the GND terminal J7.

Step 7: Connect the positive terminal (+) of the electronic load to the VOUT terminal J1. Connect the negative terminal (-) of the electronic load to the GND terminal J2. Make sure the electronic load is set to the 0A condition.

Step 8: Connect the positive terminal (+) of a DMM to the VOUT test point TP13 and the negative terminal (-) to the GND test point TP14.

Step 9: Check to ensure all jumpers and switches are in their default positions prior to application of power (refer to"Detailed Description of Jumper Settings" and "Detailed Description of Switch Settings").

Step 10: Set all power supplies to the "ON" position. LED CR1 should show Red. Check all DMM displays for correct voltage levels. Adjust if necessary.

Step 11: Turn the ENABLE switch SW2 to the "ON" position. LED CR1 should show Green. The VOUT DMM should read 1.60V (±1%).

At this point the board has been properly powered up. Normal testing can begin.

NOTE: If you need technical assistance, or other assistance, with the ISL6244 Evaluation Board, call 1-888-INTERSIL (468-3774).

Detailed Description of Jumper Settings

JUMPER	POSITION	FUNCTION
JP1	Shunted	Berg Jumper for VCORE Set Point

Detailed Description of Switch Settings

JUMPER	POSITION	FUNCTION
SW1	On	ENABLE On-Board Load Transient
	Off (default)	DISABLE On-Board Load Transient
SW2	On	ENABLE ISL6244 and ISL6207
	Off(default)	DISABLE ISL6244 and ISL6207

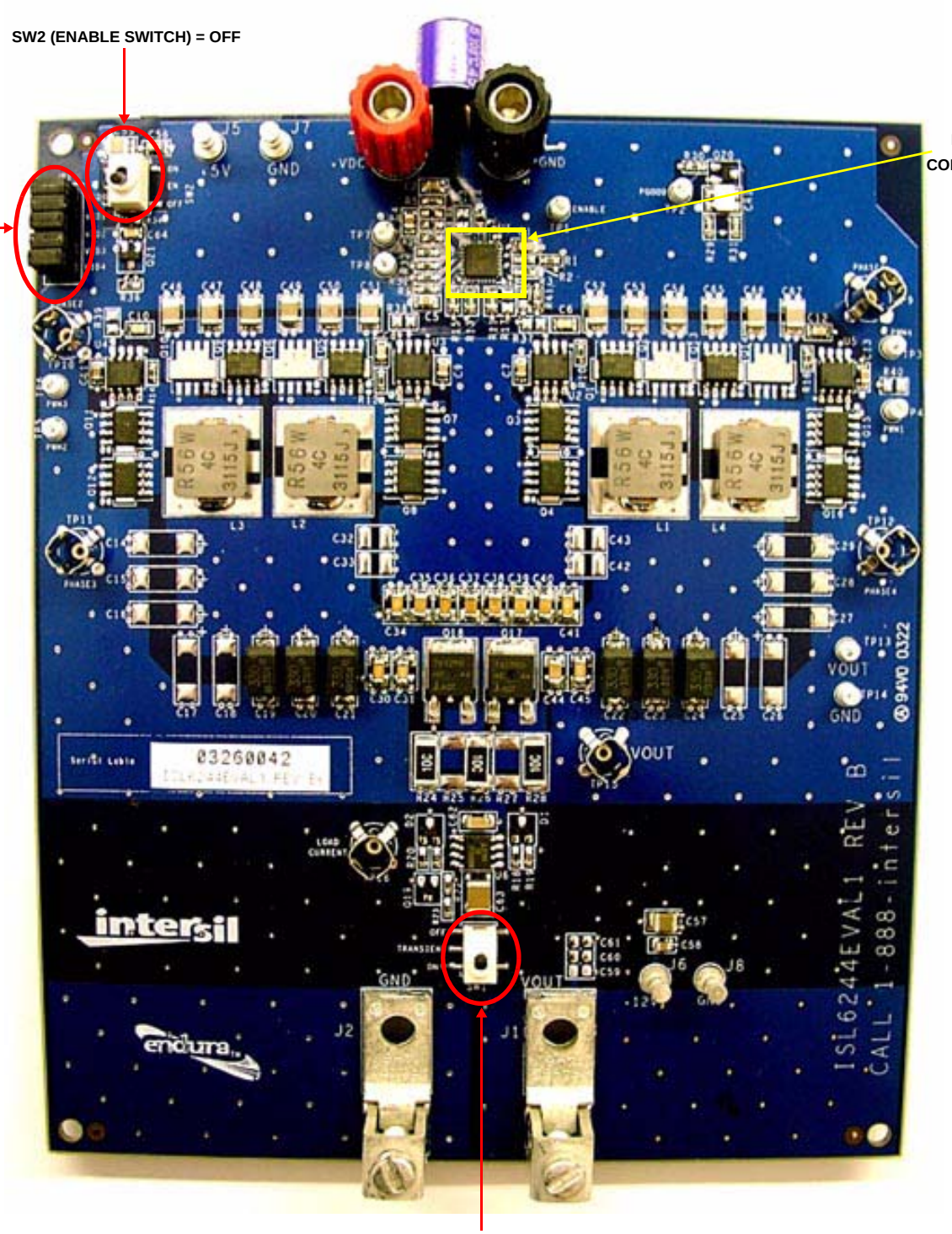


FIGURE 1. ISL6244 EVAL BOARD INITIAL JUMPER AND SWITCH SETTINGS

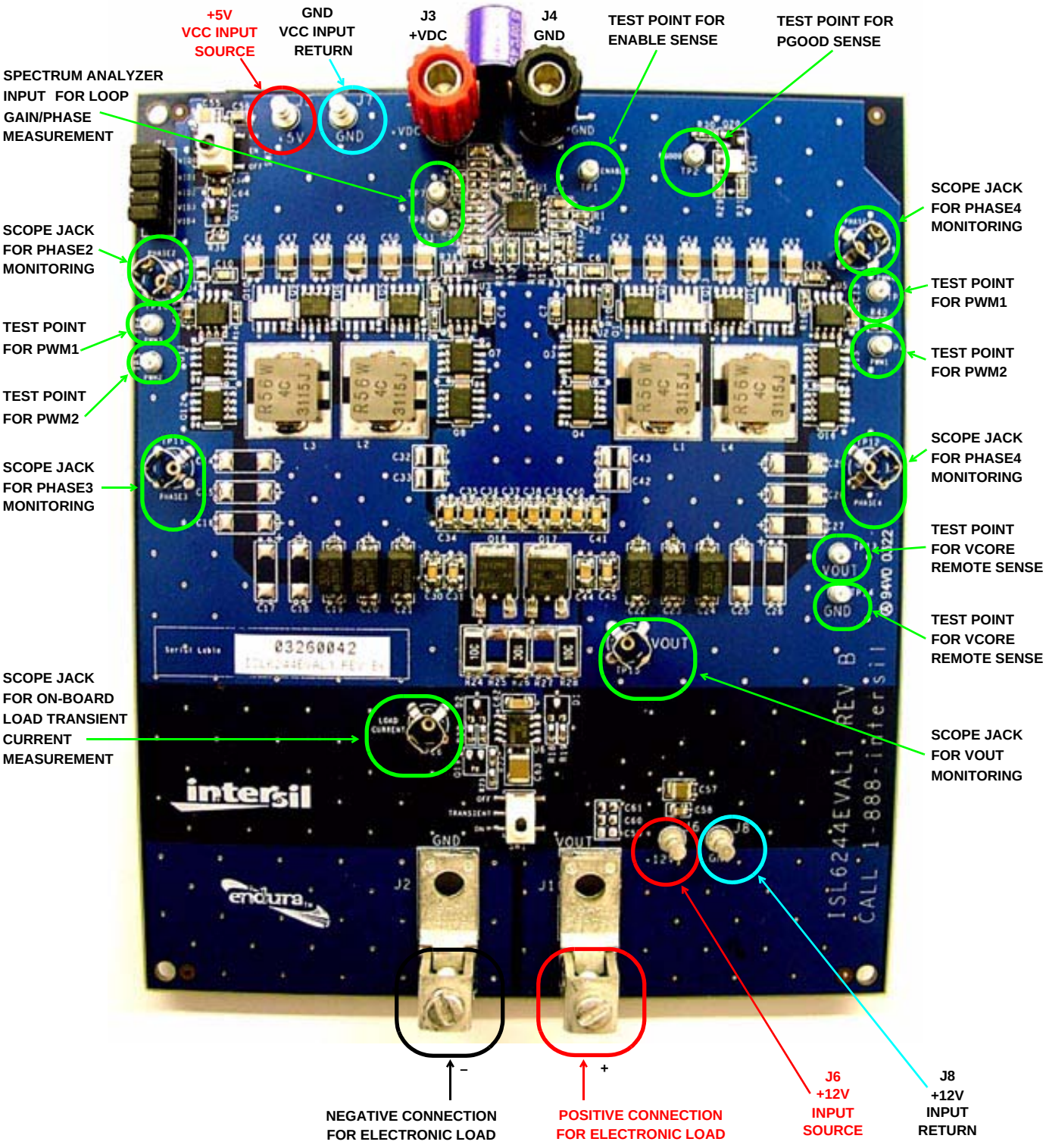


FIGURE 2. ISL6244 EVAL BOARD TEST POINTS

Board Layout Information

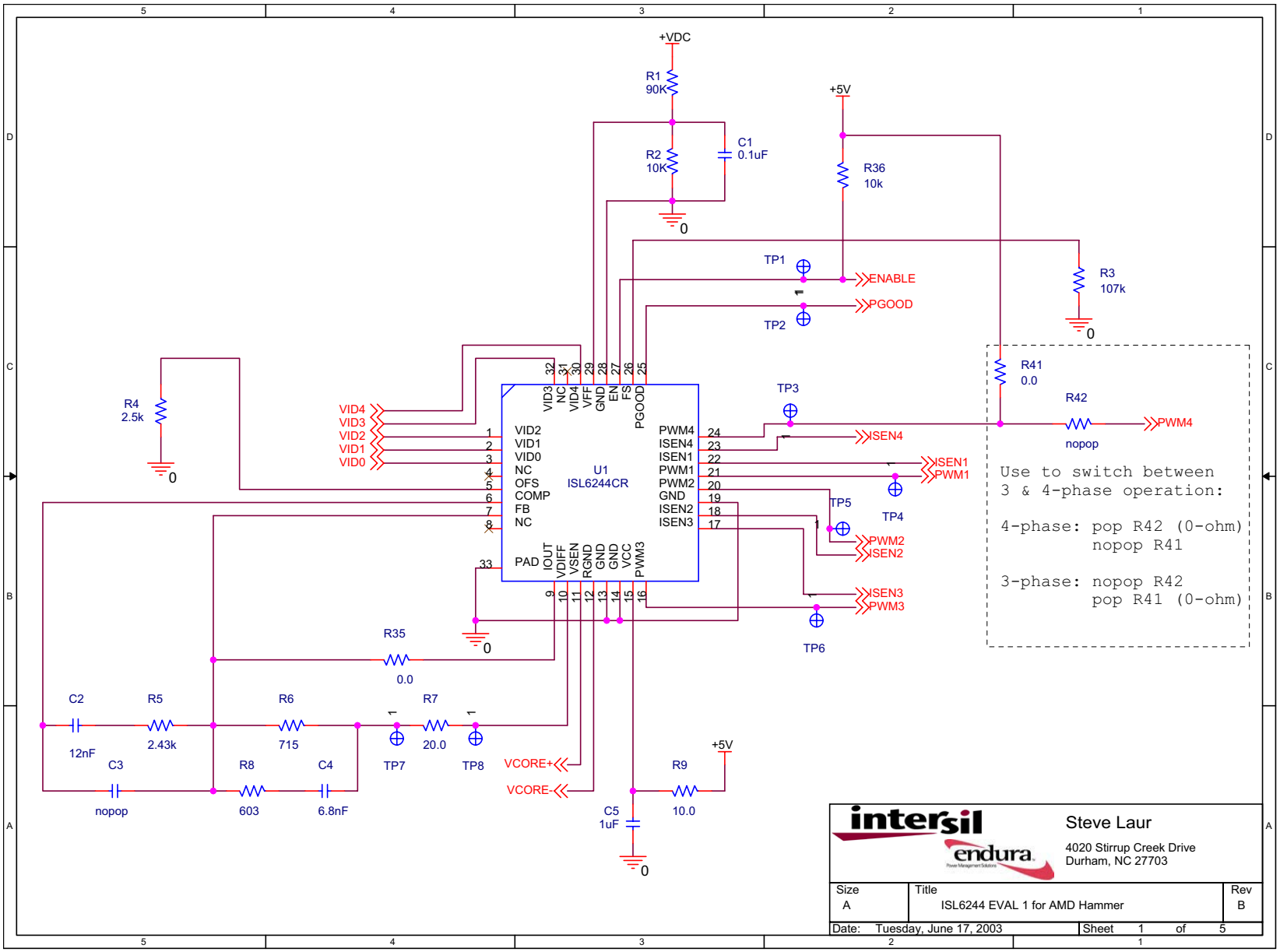


FIGURE 3. SCHEMATIC 1

Board Layout Information (Continued)

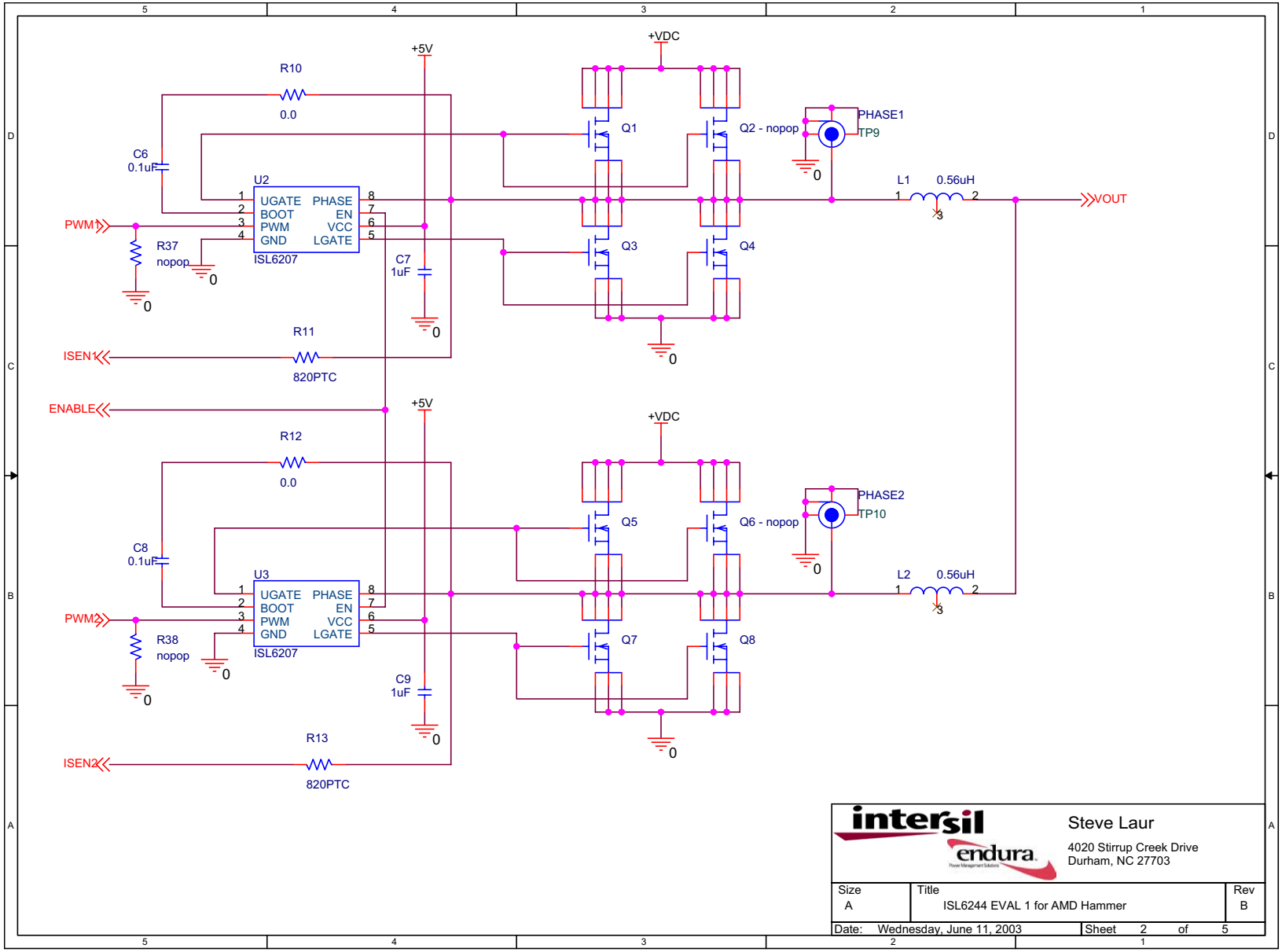


FIGURE 4. SCHEMATIC 2

Board Layout Information (Continued)

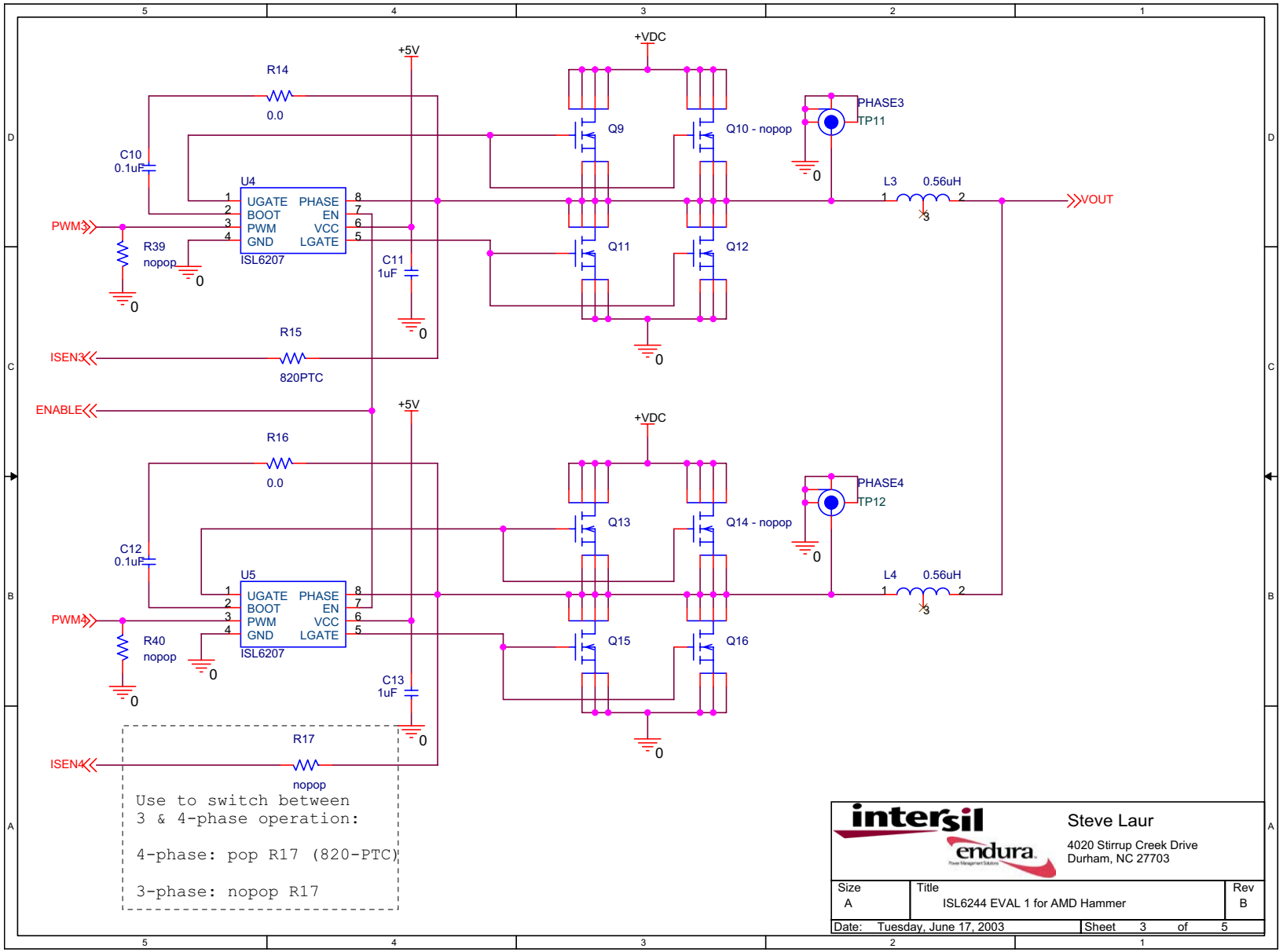


FIGURE 5. SCHEMATIC 3

Board Layout Information (Continued)

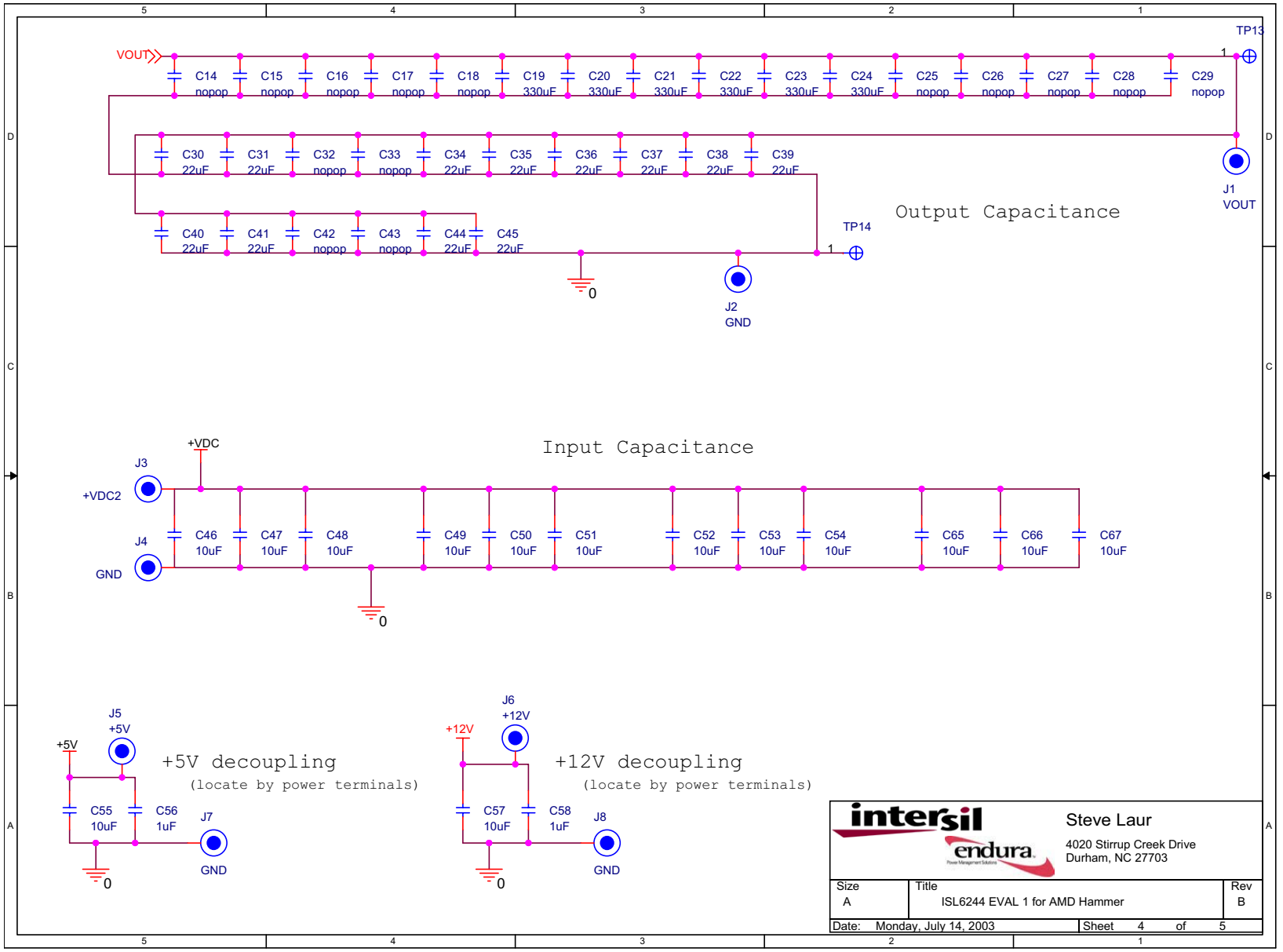


FIGURE 6. SCHEMATIC 4

Board Layout Information (Continued)

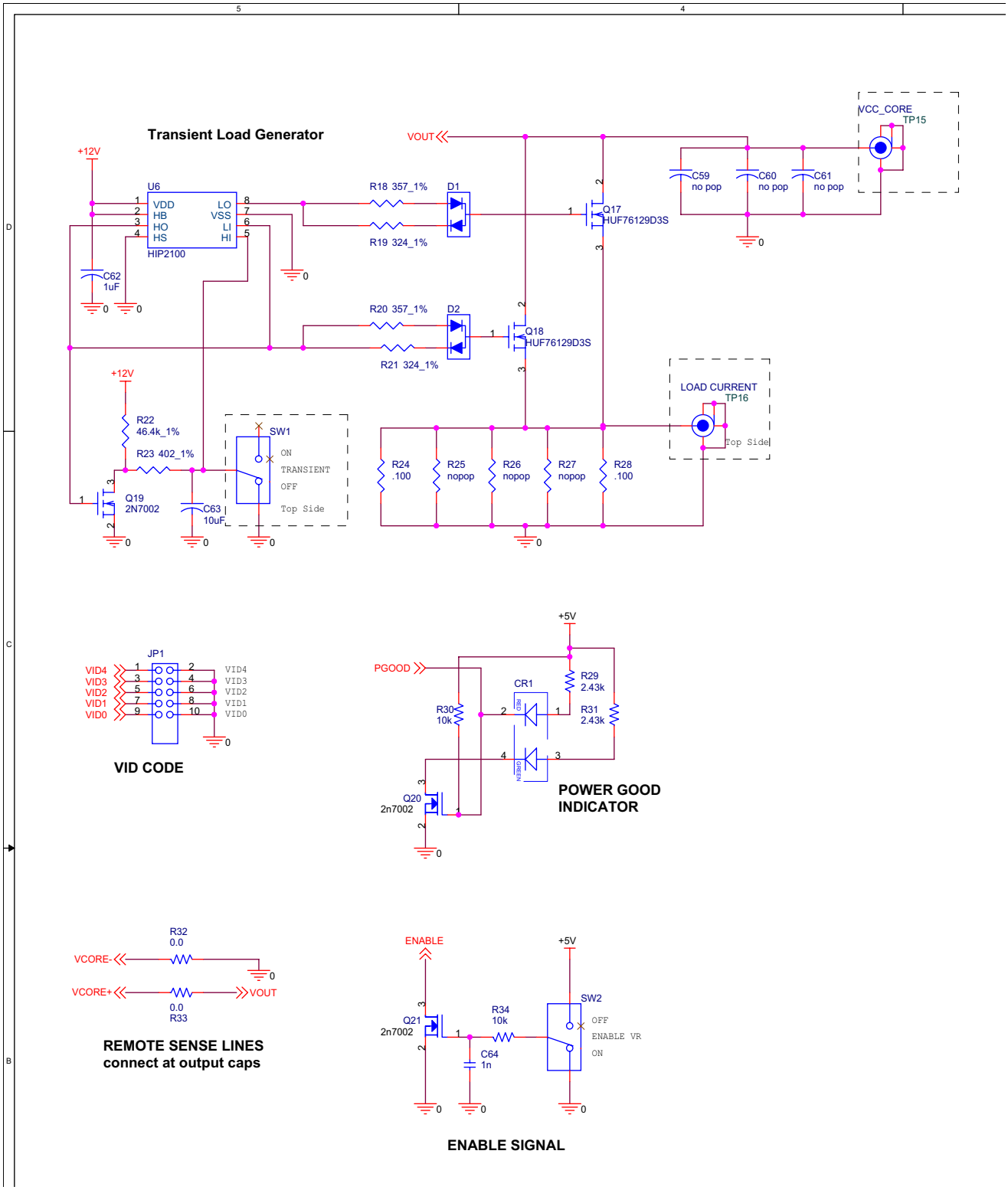


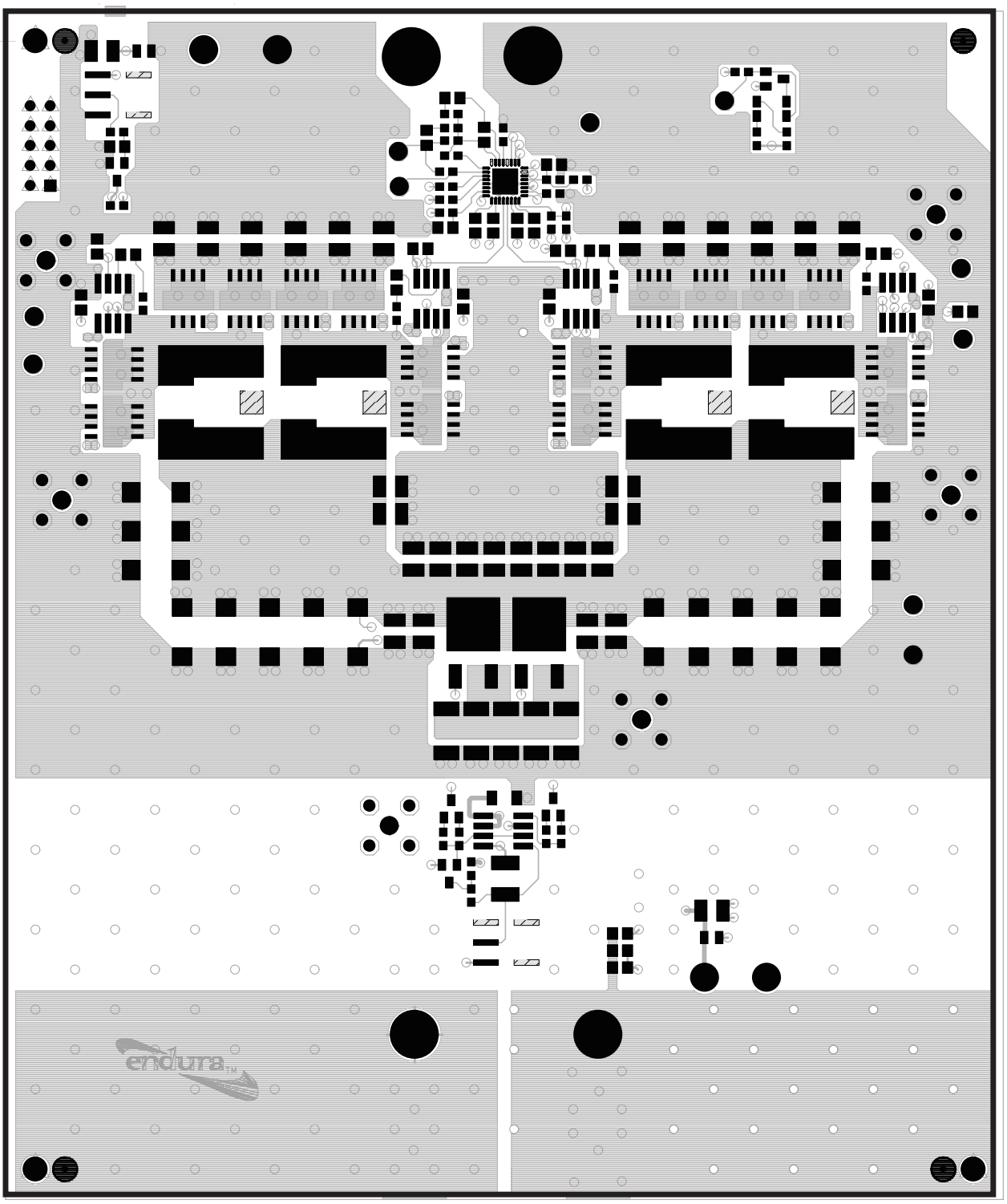
FIGURE 7. SCHEMATIC 5

TABLE 1. BILL OF MATERIALS

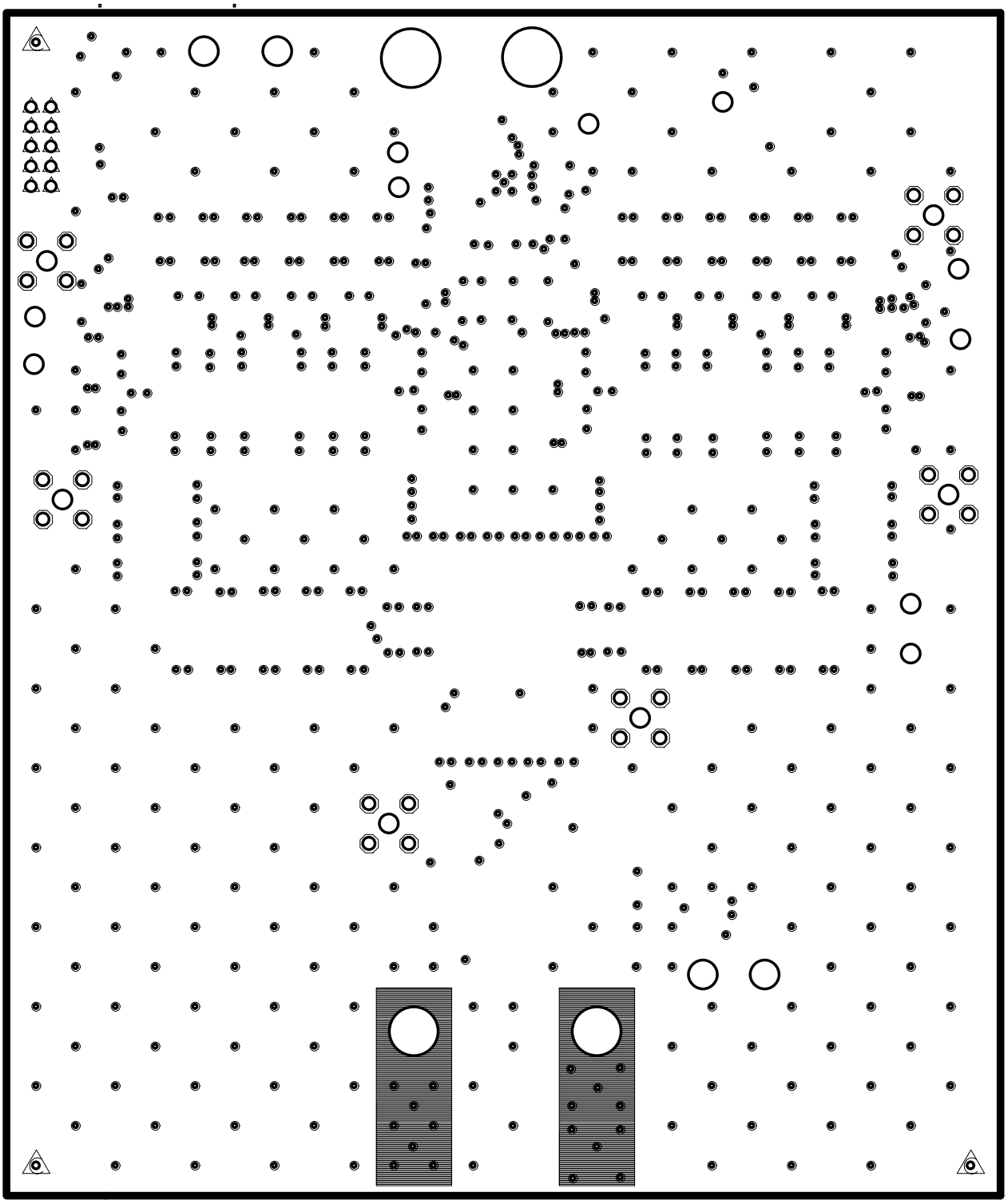
ITEM	QTY	REFERENCE	VALUE	TYPE	FOOTPRINT	VOLTAGE*
1	1	CR1	Dual LED2	DIGIKEY 67-1372-1-ND	smdp_led_gw	-
2	18	C3, C59, C60, C61, C14-C18, Q2, Q6, Q10, Q14, C25-C29, R25, R26, R27, R37, R38, R39, R40, R42, R17	nopop	-	-	-
3	1	C4	7.4nF	-	-	-
4	1	C2	12nF	-	0805	10V
5	7	C5, C7, C9, C11, C56, C58, C13	1µF	-	0805	16V
6	4	C32, C33, C42, C43	nopop	-	1210	10V
7	1	C62	1µF	-	1206	16V
8	4	C1, C6, C8, C10, C12	0.1µF	-	0805	10V
9	16	C19, C20, C21, C22, C23, C24	330µF	Panasonic EEFSE0E331R	7343	-
10	12	C30, C31, C34-C41, C44, C45	22µF	Panasonic: ECJ3YB0J226M	1206	6.3V
11	14	C46, C47, C48, C49, C50, C51, C52, C53, C54, C55, C57, C65, C66, C67	10µF	Taiyo Yuden TMK325F106ZH	1210	25V
12	1	C63	10µF	Taiyo Yuden TMK325F106ZH	1812	25V
13	1	C64	1n	-	0805	10V
14	2	D1, D2	BAV99LT1	BAV99LT1	SOT23	-
15	1	JP1	Jumper - 5Pos	BERG 2x5 100MIL Header	jumper10	-
16	1	J1	VOUT	BURNDY KPA8CTP	kpa8ctp	-
17	1	J2	GND	BURNDY KPA8CTP	kpa8ctp	-
18	1	J3	+VDC	NEWARK 111-0702-001 RED	pad-170	-
19	1	J4	GND	NEWARK 111-0703-001 BLK	pad-170	-
20	1	J5	+5V	DIGIKEY 1514-2K-ND	tp-150c100p	-
21	1	J6	+12V	DIGIKEY 1514-2K-ND	tp-150c100p	-
22	2	J7, J8	GND	DIGIKEY 1514-2K-ND	tp-150c100p	-
23	3	L1, L2, L3, L4	0.56µH	Panasonic PCC-M104L Series	pcc-nx1_nx2_j	-
24	4	Q1, Q5, Q9, Q13	IRF7811W	-	pwrpak_so8_single	-
25	8	Q3, Q4, Q7, Q8, Q11, Q12, Q15	SI4362	-	pwrpak_so8_single	-
		Q16	-	-	-	-
26	2	Q18, Q17	HUF76129D3S	-	TO-252AA	-
27	3	Q19, Q20, Q21	2N7002	-	SOT23	-
28	1	R1	90K	-	0603	-
29	4	R2, R30, R34, R36	10K	-	0603	-
30	1	R3	107K	-	0603	-
31	1	R4	2.5K	-	0603	-
32	1	R5	2.43K	-	0603	-
33	1	R6	710	-	0603	-
34	1	R7	20	-	0603	-
35	1	R8	603	-	-	-
36	1	R9	10	-	0603	-

TABLE 1. BILL OF MATERIALS (Continued)

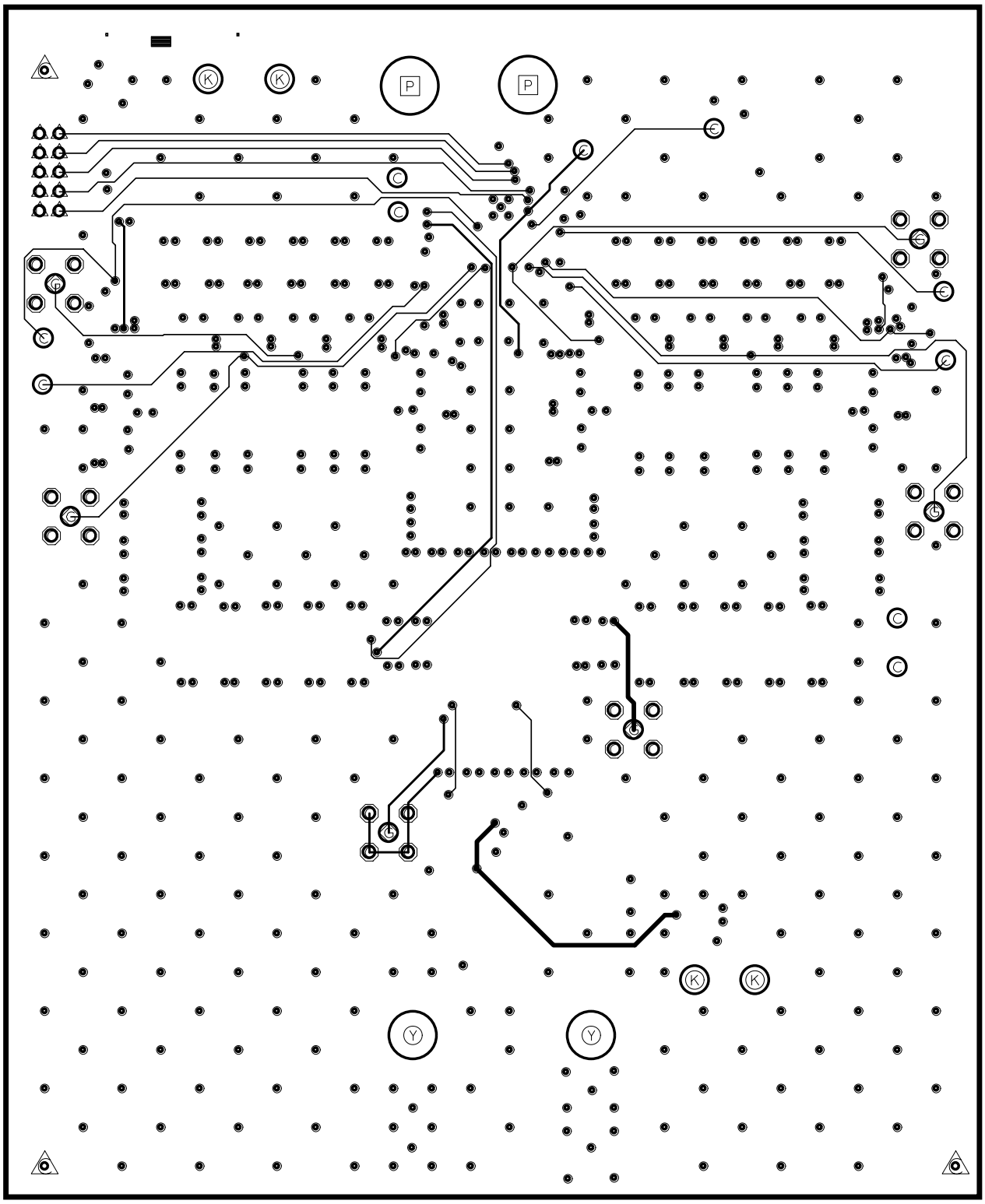
ITEM	QTY	REFERENCE	VALUE	TYPE	FOOTPRINT	VOLTAGE*
37	7	R10, R12, R14, R32, R33, R16, R35, R41	0.0	-	0603	-
38	3	R11, R13, R15	820PTC	Vishay TFPT0805L820F	0805	-
39	2	R18, R20	357_1%	-	0603	-
40	2	R19, R21	324_1%	-	0603	-
41	1	R22	46.4K_1%	-	0603	-
42	1	R23	402_1%	-	0603	-
43	2	R24, R28	0.1	Vishay WSL series	2512	-
44	2	R29, R31	2.43K		0603	-
45	1	SW1	SPDT	C&K SMT DIGIKEY PN CKN1101CT-ND	gt11sc	-
46	1	SW2	DPST	C&K SMT DIGIKEY PN CKN1099CT-ND	gt11sc	-
47	10	TP1, TP2, TP3, TP4, TP5, TP6,	Test Point	KEYSTONE 5002	PAD-100	-
		TP7, TP8, TP13, TP14	-	-	-	-
48	1	TP9	Phase1	TEK 131-4244-00	TEK 131-4244-00	-
49	1	TP10	Phase2	TEK 131-4244-00	TEK 131-4244-00	-
50	1	TP11	Phase3	TEK 131-4244-00	TEK 131-4244-00	-
51	1	TP12	Phase4	TEK 131-4244-00	TEK 131-4244-00	-
52	1	TP15	VCC_CORE	TEK 131-4244-00	TEK 131-4244-00	-
53	1	TP16	Load Current	TEK 131-4244-00	TEK 131-4244-00	-
54	1	U1	ISL6244CR	Intersil ISL6244	32mlfp_5x5	-
55	4	U2, U3, U4, U5	ISL6207	Intersil ISL6207	soic8	-
56	1	U6	HIP2100	Intersil HIP2100	soic8	-



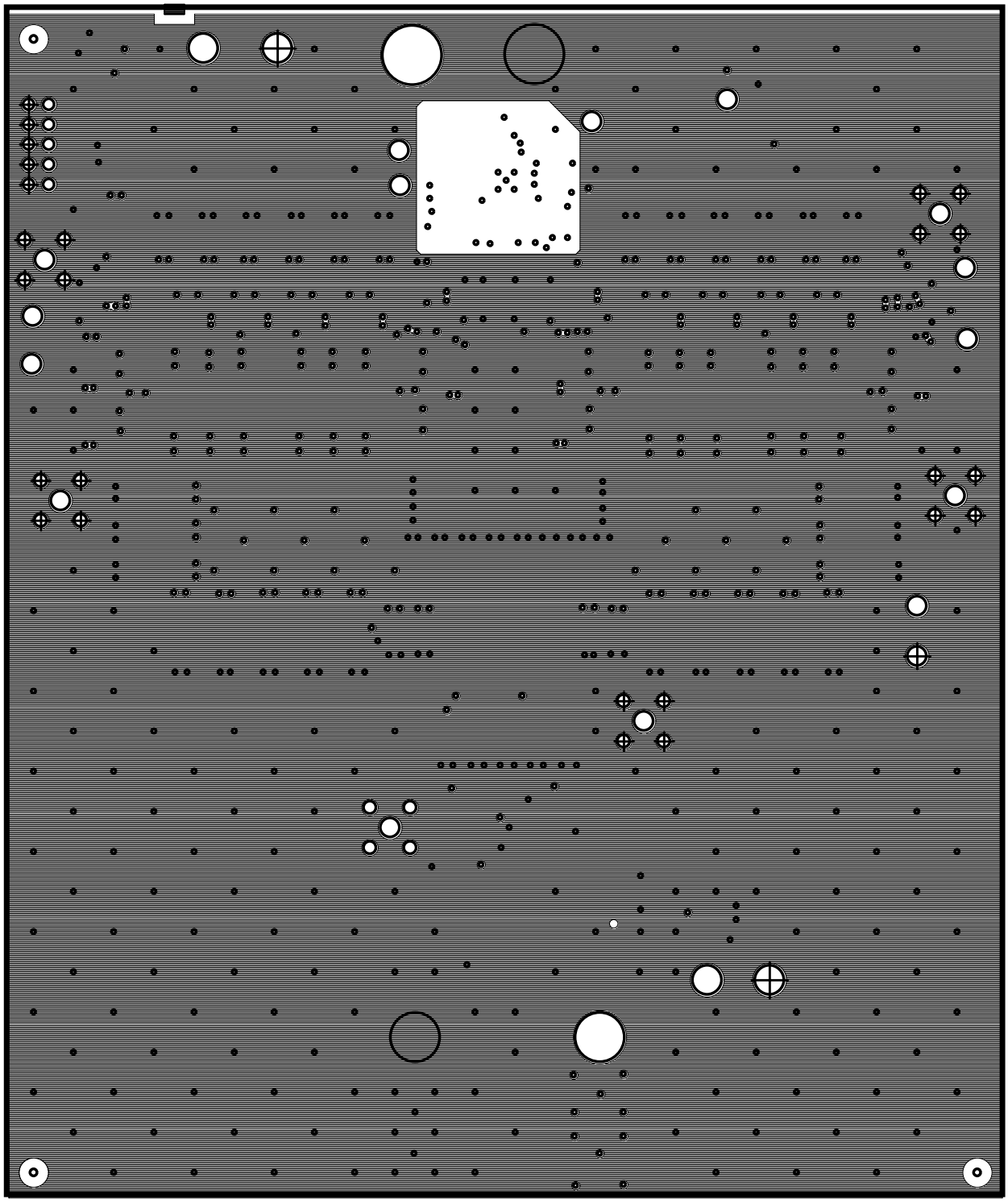
TOP LAYER SILKSCREEN



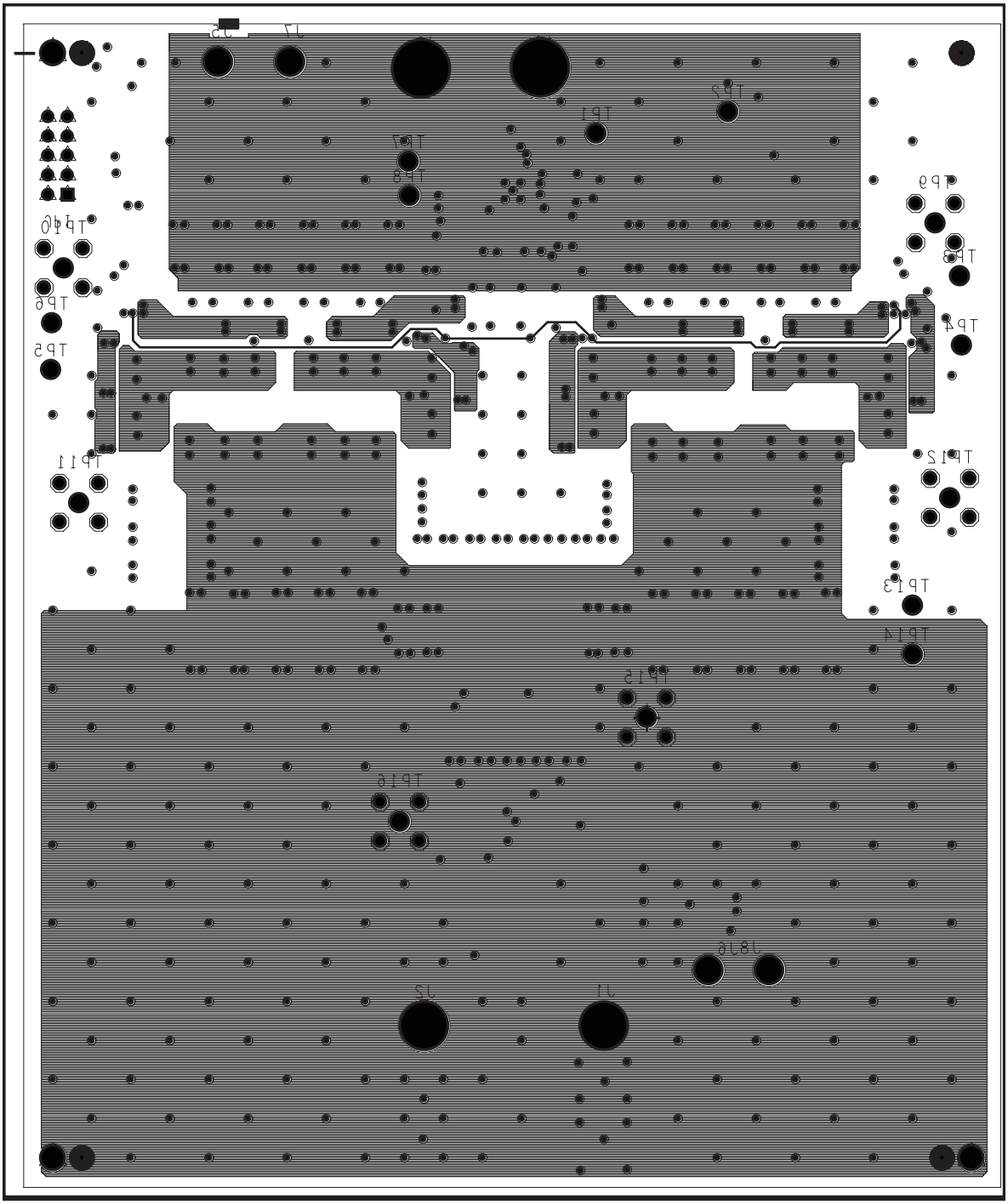
LAYER 2



LAYER 3



LAYER 4



BOTTOM SILKSCREEN

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