RENESAS

This document regroups all links necessary for the user to develop an application

Released: Jun. 2024
ECPA-IMB-24-0333-5
Mouseover "L" in "Link"

RZ/G3S Easy Download Guide

Step	Information for engineers	Contents Type	Contents Name	RZ/G3S Link	Note	Access levels
	RZ/G Series 32/64-bit MPU (Wiki)	Link summary	Introduction,Boards,Software and Documentation	Link	-	Non limitation
	Contact Support	QA Ticket	Technical Q&A	Link	-	Non limitation

Step	Introduction	Contents Type	Contents Name	RZ/G3S Link	Note	Access levels
1	RZ Family Broshure	Document	RZ Family Microprocessors	Link	-	Non limitation
2	Fleyer	Document	Renesas RZ/G3S Group	Link	-	Non limitation
3	User's Manual Overview	Document	User's Manual Overview	TBD	-	Non limitation
4	60's Video	Video	60's Video	Link	-	Non limitation

Step	Launch of board and evaluation environment	Contents Type	Contents Name	RZ/G3S Link	Note	Access levels
1	User's Manual	Document	User's Manual: Hardware	Link	-	Non limitation
		Document	Additional document for User's Manual(SDHI)(Requires LoA)	Please contact Disti/Sales	LoA*1	Please contact Disti/Sales
2	How to start up the board					
		Document	SMARC Module Board User's Manual	Link	-	Non limitation
		Document	SMARC Carrier Board User's Manual	Link	-	Non limitation
		Document	Evaluation Board Kit(EVK) Quick Start Guide	Link	-	Non limitation
3	Board information / how to get	Info/purchase	Evaluation Kit WEB Page	Link	-	Non limitation
4-1	Evaluation environment start-up method					
	Verified Linux Package (VLP)	Document	RZ/G Verified Linux Package V3.0.6 Release Note	Link	-	Non limitation
		Document	Linux Start-up Guide	Link	-	Non limitation
		Document	RZ/G3S Group BSP Manual Set	Link	EULA*2	MyRenesas
		Document	RZ/G Proprietary SW Package Handring	Please contact Disti/Sales	-	Please contact Disti/Sales
4-2	Evaluation environment start-up method					
	Multi-OS Package	Document	Release Note for Muti-OS Package v2.0.2	Link	-	Non limitation
		Document	Getting Started with Flexible Software Package	Link	-	Non limitation
		Document	Setting GPIO with Flexible Software Package	Link	-	Non limitation
		Document	FSP Documentation	Link	-	Non limitation
		Document	Release Note for Flexible Software Package	Link	-	Non limitation
5-1	How to get various software					
	Pre-built Images	Software	RZ/G3S Pre-built Images	Link	-	Non limitation
	Verified Linux Package (VLP)	Web Link	RZ/G Verified Linux Package [5.10-CIP]	Link	-	Non limitation
	Feature Package (Multi-OS Package)	Web Link	RZ/G3S Group Multi-OS Package	Link	EULA*2	MyRenesas
	Feature Package (Security Package)	Web Link	Security Package	Link	SLA*3	Secure Access
6	How to get various tools					
		Tool	Smart Configurator	Link	-	Non limitation
7	How to launch various tools					
		Document	Smart Configurator for RZ User's Guide	Link	-	Non limitation

Step	Custom board development	Contents Type	Contents Name	RZ/G3S Link	Note	Access levels
	PCB Desigh and Verification Flow (for DDR-IF)	Document	PCB Desigh and Verification Flow (for DDR-IF)	Please contact Disti/Sales		Please contact Disti/Sales
	PCB design checklist when designing a custom board	Document	Board circuit design checklist	Link	-	Non limitation
	PCB Design Guide for High Speed Serial Interfaces	Document	PCB Design Guidelines for MIPI-CSI, MIPI-DSI, USB2.0 and PCI Express Gen2	Link	-	Non limitation
	PCB Design Guide for DDR memory,DDR Config Generation Tool	Document,Tool	PCB Design Guideline for LDDR4, DDR Config Generation Tool	Link	TCU*5	Secure Access
	PCB Verification Guide for Core, PDN model	Document,Model	PCB verification guide for Core VDD, PDN model	Link	-	Non limitation
	PCB Verification Guide for DDR memory, PKG mode	Document,Model	PCB verification guide for LDDR4, PKG model	Link	TCU*5	Secure Access
	Reference Desing Data(Schamtics,Layout,BOM)	Design Data	SMARC Module Board Design Data(Schematics,Layout,BOM)	Link	Disclaimer*4	MyRenesas
	Reference Desing Data(Schamtics,Layout,BOM)	Design Data	Carrier Board Design Data(Schematics,Layout,BOM)	Link	Disclaimer*4	MyRenesas
	IBIS(For LSI)	Model	IBIS	Link	TCU*5	
	Boundary Scan Description Language file	File	BSDL	Link	Disclaimer*4	MyRenesas
	Guide to Using RGMII in Making an Ethernet-IF Connection	Document	Guide to Using RGMII in Making an Ethernet-IF Connection	Link	-	Non limitation
	Power Consumption Measurement	Document	Power Consumption Measurement	Link	-	Non limitation
	Thermal Management Guide	Document	Thermal Management Guideline	Link	-	Non limitation
	Mecanical Handling Guideline	Document	Mechanical Handling Guideline	Link	-	Non limitation
	Reflow Soldering conditions	Document	Mount Conditions Reflow Soldering Conditions	Link	-	Non limitation
	Baking conditions	Document	Mount Conditions Baking Conditions	TBD	-	Non limitation
	Semiconductor Package Mount Manual	Document	Semiconductor Package Mount Manual	Link	-	Non limitation
	Lifetime estimation guide	Document	Lifetime Guideline	Link	-	Non limitation
	Power Management IC installed in EVK	Device Info	Power Management IC	Link	-	Non limitation
	Clock Generator IC installed in EVK	Device Info	Clock Generator IC	Link	-	Non limitation
	Reliability Report	Document	R9A08G045XXGBG Reliability Report	TBD		Non limitation
	Power calculation sheet and guide	Document	Power calcuration sheet and guide	Please contact Disti/Sales	-	Please contact Disti/Sales

*1: Letter of Acknowledgement
*2: End User Lisence Agreement
*3: Software Lisence Agreement
*4: Disclaimer Letter
*5: Terms and Conditions of Use