IDT® 89EBPES32x8G2 Evaluation Board Manual

(Eval Board: 18-678-000)

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Introduction

The 89HPES32T8G2 and 89HPES32H8G2 switches (also referred to as PES32x8G2 in this manual) are members of IDT's PCI Express® standard based line of products. They are PCIe® Base Specification 2.0 compliant (Gen2) 8-port switches. There are eight x4 lanes ports. Two x4 ports can be merged to form one x8 port in PES32x8G2. One upstream port is provided for connecting to the root complex (RC), and up to seven downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the 89HPES32T8G2 and 89HPES328HG2 User Manuals.

The 89EBPES32x8G2 Evaluation Board (also referred to as EB32x8G2 in this manual) provides an evaluation platform for the PES32T8G2 and PES32H8G2 switches. It is also a cost effective way to add PCIe ports (slots) to an existing system with a limited number of PCIe ports/slots. The EB32x8G2 board is designed to function as an add-on card to be plugged into a x8 PCIe slot available on a motherboard hosting an appropriate root complex and microprocessor(s). The EB32x8G2 is a vehicle to test and evaluate the functionality of the PES32x8G2 switch. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB32x8G2 is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB32x8G2 board.

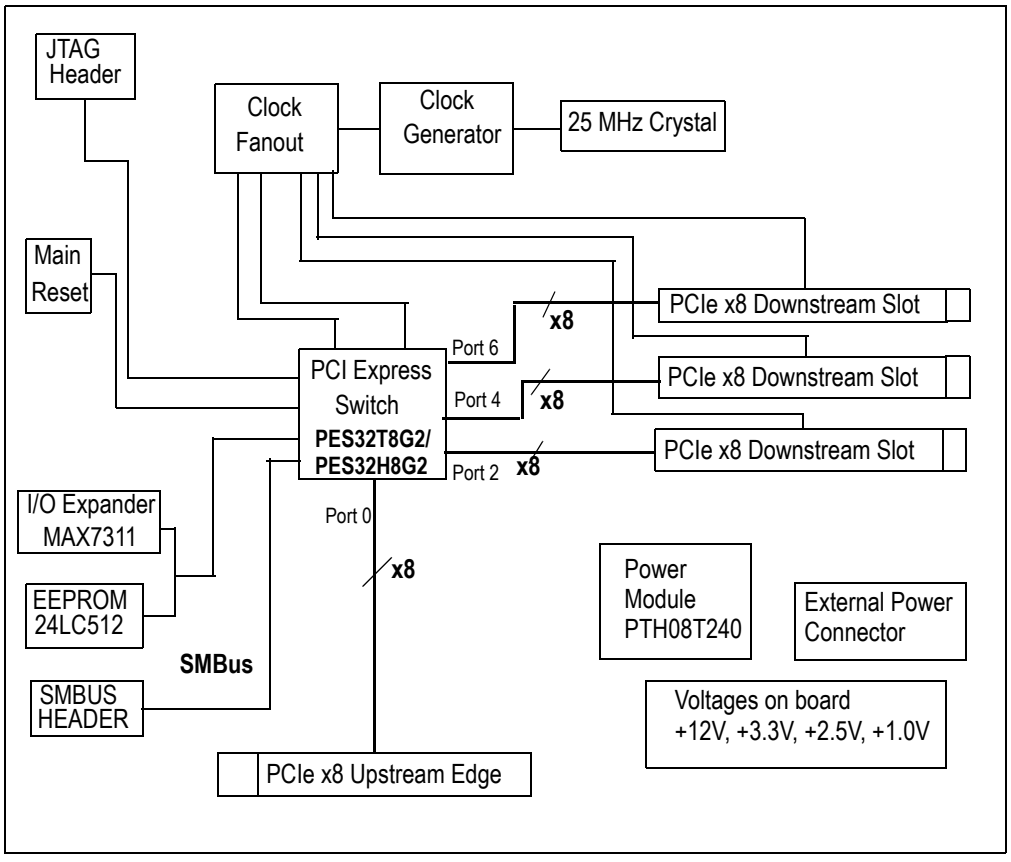


Figure 1.1 Function Block Diagram of the EB32x8G2 Eval Board

Notes

Board Features

Hardware

- **PES32x8G2 PCIe Gen2 switch**
  - *Up to eight x4 or four x8 ports - 32 PCIe lanes*
  - *PCIe Base Specification Revision 2.0 compliant (Gen2 SerDes speeds of 5 GT/S)*
  - *Up to 2048 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x8, x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- **Upstream, Downstream Port**
  - *One edge connector on the upstream port, to be plugged into a slot with at least x8 capable on a host motherboard*
  - *Three slot connectors on the downstream ports for PCIe endpoint add-on cards to be plugged in. These slot connectors are x8 mechanically and electrically connected as three x8, but open-ended for card widths greater than x8 (e.g. x16).*
- **Numerous user selectable configurations set using onboard jumpers and DIP-switches**
  - *Source of clock — host clock or onboard clock generator*
  - *Two clock rates (100/125 MHz) from an onboard clock generator*
  - *Boot mode selection*
- **SMBUS Slave Interface (4 pin header)**
- **SMBUS Master Interface connected to the Serial EEPROMs through I/O expander**
- **“Attention” button for each downstream port to initiate a hot swap event on each port**
- **Four pin connector for optional external power supply**
- **Push button for Warm Reset**
- **Several LEDs to display status, reset, power, “Attention”, etc.**
- **One 10-pin JTAG connector (pitch 2.54 mm x 2.54 mm)**

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES32x8G2 within host systems running popular operating systems.

- **Installation programs**
  - *Operating Systems Supported: Windows Server 2003, Windows Server 2008, WindowsXP, Vista, Linux*
- **GUI based application for Windows and Linux**
  - *Allows users to view and modify registers in the PES32x8G2*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is provided to firmly hold in place three endpoints plugged into the EB32x8G2 board.
- An external power supply may be required under some conditions.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB32x8G2 board for clock outputs.

Revision History

January 5, 2009: Initial publication of eval board manual.

Notes

May 7, 2009: In the Power Sources section of Chapter 2, revised the descriptions for PCI Express analog power, transmitter analog voltage, and I/O voltage. In the SMBus Slave Interface section of Chapter 2, the slave interface default address was changed to **0b1110111.** In Table 2.1, changed clock source to S2[3]. In Table 2.6, changed default setting for S3[1]. In Table 2.7, swapped pins 2 and 4. In Table 2.10, changed default and description for S9[4], S9[5], S9[6]. In Table 2.11, corrected location for Port 4: Power-is-good to DS24, and corrected location for GPIO1 to DS9. On page 15 of the Schematics in Chapter 4, changed W27 and W93 from position 2-3 to position 1-2 and added text “Slave SMBus Addr 0x77”.

Notes

Installation of the EB32x8G2 Eval Board

Notes

EB32x8G2 Installation

This chapter discusses the steps required to configure and install the EB32x8G2 evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Make sure that the host system (motherboard with root complex chipset) is powered off.
4. Insert the evaluation board into the host system.
5. Apply power to the host system.

The EB32x8G2 board is typically shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES32x8G2 is a 32-lane, 8-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides switching functions between a PCI Express upstream port and downstream ports or peer-to-peer switching between downstream ports.

The EB32x8G2 has three PCI Express downstream ports, accessible through three x8 connectors. Three ports are capable of negotiating a x1, x2, x4, and x8 link width. All endpoint cards connected to the PES32x8G2 must support one of these link widths.

Basic requirements for board operation are:

- Host system with a PCI Express root complex supporting at least x8 configuration through a PCI Express x8 or larger slot.
- x1, x2, x4, or x8 PCI Express Endpoint Cards.

Reference Clocks

The PES32x8G2 requires two differential reference clocks. The EB32x8G2 derives these clocks from a common source which is user-selectable. The common source can be either the host system's reference clock or it can be the onboard clock generator. Selection is made by stuffing resistors as in Table 2.1.

Clock Configuration Stuffing Option	
S2[3]	**Clock Source**
OFF	Onboard Reference Clock – Use onboard clock generator
ON	Upstream Reference Clock – Host system provides clock **(Default)**

Table 2.1 Clock Source Selection

The source for the onboard clock is the ICS841484 clock generator device (U10) connected to a 25MHz oscillator (X1). When using the onboard clock generator, the output frequency is fixed at 100MHz, therefore FSEL0 (S2, pin 2) should be in the ON position as the default setting.

Notes

The output of the onboard clock generator and clock buffer (ICS841484) is accessible through SMA connectors located on the Evaluation Board. See Table 2.2. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J9, J10	
J10	Positive Reference Clock
J9	Negative Reference Clock

Table 2.2 SMA Connectors - Onboard Reference Clock

Power Sources

The EB32x8G2 and all downstream ports are powered from the upstream port slot power. If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Header W1, W2, and W3 (see Table 2.10) are used to select the proper power source for the switch and all downstream ports.

External Power Source

If necessary, external power is supplied to the EB32x8G2 board through a 4-pin auxiliary power connector attached to J4. The external power supply provides +12V to the EB32x8G2 as described in Table 2.3. The +5V is unused.

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.3 External Power Connector - J4

PCI Express Analog High Power Voltage Converter

A DC-DC converter (U5) provides a 2.5V PCI Express analog high power voltage (shown as V_{DD}PEHA) to the PES32x8G2.

PCI Express Analog Power and Transmitter Analog Voltage Converter

A separate DC-DC converter (U4) provides a 1.0V PCI Express transmitter analog voltage (shown as V_{DD}PETA) and also provides, using the ferrite bead (FB2), a 1.0V PCI Express analog power voltage (shown as V_{DD}PEA) to the PES32x8G2.

Core Logic Voltage Converter

A separate DC-DC converter (U3) provides the 1.0V core voltage (V_{DD}CORE) to the PES32x8G2.

2.5V I/O Voltage Regulator

A 12V to 3.3V voltage regulator (VR1) and 12V to 2.5V voltage regulator (VR3) provide the I/O voltage (V_{DD}I/O) to the PES32x8G2. A 3-pin header enables the selection of either the 2.5V or 3.3V via a jumper (pin 1-2 is the default position for the 3.3V V_{DD}I/O).

Notes

Power-up Sequence for PES32x8G2

During power supply ramp-up, V_{DD}CORE must remain at least 1.0V below V_{DD}I/O at all times. There are no other power-up sequence requirements for the various operating supply voltages.

Reset

The PES32x8G2 supports two types of reset mechanisms as described in the PCI Express specification:

- Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES32x8G2, and the endpoints.
- Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES32x8G2 User Manuals. The EB32x8G2 evaluation board provides seamless support for Hot Reset.

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB32x8G2 evaluation board:

- Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES32x8G2.
- Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:
  - Pressing a push-button switch (S1) located on EB32x8G2 board
  - The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB32x8G2. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W4.

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES32x8G2 while power is on.

Downstream Reset

The PES32x8G2 provides a a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.4.

Port #	Jumper	Selection
2	W9	[1-2] Software controlled reset through I/O Expander 0 [2-3] Fundamental reset PERST# (default)
4	W5	[1-2] Software controlled reset through I/O Expander 2 [2-3] Fundamental reset PERST# (default)
6	W7	[1-2] Software controlled reset through I/O Expander 2 [2-3] Fundamental reset PERST# (default)

Table 2.4 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.5 is sampled by the PES32x8G2 during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S3 and S13 as defined in Table 2.6.

Notes

Signal	Description
CLKMODE[1:0]	**Initial Port Clocking mode (for PES32x8G2). Default: 0x0** 0x0 - Global Clock mode on all ports. Port0/2/4 SCLK = 0 0x1 - Global Clock mode on all ports. Port0 SCLK =1, Port2 SCLK =0, Port4 SCLK =0 0x2 - Global Clock mode on all ports. Port0 SCLK =0, Port2 SCLK =1, Port4 SCLK =1 0x3 - Global Clock mode on all ports. Port0 SCLK =1, Port2 SCLK =1, Port4 SCLK =1
SWMODE[3:0]	**Switch Mode.** These configuration pins determine the PES32x8G2 switch operating mode. **Default: 0x0** 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0xF - Reserved

Table 2.5 Boot Configuration Vector Signals

Signal	Description	Default
S13[1]	CLKMODE0	ON
S13[2]	CLKMODE1	ON
S3[1]	SWMODE[0]	OFF
S3[2]	SWMODE[1]	ON
S3[3]	SWMODE[2]	ON
S3[4]	SWMODE[3]	ON

Table 2.6 Boot Configuration Vector Switches S3 & S13 (ON=0, OFF=1)

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consists of an SMBus clock pin and an SMBus data pin.

The PES32x8G2 contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROM used for initialization and the I/O expanders used for hot-plug signals.

SMBus Slave Interface

On the PES32x8G2 board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.7.

> **Note:** The SMBus signals to the PCI Express edge connector is disabled by default. To enable them, place 0-ohm resistors at locations R160 and R161.

Notes

Slave SMBus Interface Connector J8	
Pin	**Signal**
1	N/C
2	SDA
3	GND
4	SCL

Table 2.7 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[2:1] pins is used. For a fixed address, the SMBus address of the PES32x8G2 slave interface is **0b1110111** by default.

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- Byte and Word Write/Read
- Block Write/Read

SMBus Master Interface

Connected to the master SMBus interface are six 16-bit I/O Expanders (MAX7311) and a serial EEPROM (24LC512). These I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B). The SMbus address for the I/O Expander0/2/8/11/12/13 are fixed as 0x40, 0x44, 0x50, 0x56, 0x58, and 0x5A, respectively.

Note: The seven bits address for the selected EEPROM device is fixed at **`0b1010_000`** by default.

Notes

JTAG Header

The PES32x8G2 provides a JTAG connector J5 for access to the PES32x8G2 JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.8 for the JTAG Connector J5 pin out.

JTAG Connector J5					
Pin	**Signal**	**Direction**	**Pin**	**Signal**	**Direction**
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.8 JTAG Connector Pin Out

Attention Buttons

The PES32x8G2 features three attention buttons, shown in Table 2.9. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
S7	Port 2 Attention Button
S12	Port 4 Attention Button
S6	Port 6 Attention Button

Table 2.9 Attention Buttons

Notes

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	**Type**	**Default**	**Description**
W1-W3	Header	1-2 Shunted	1-2: 12.0V source from Upstream Port **(Default)** 2-3: 12.0V source from external power connector
W38	Header	Shunted	Disable EEPROM Write protect feature **(Default)**
S9[1]	Switch	ON	ON: Port2, Force hot-plug controller on **(Default)** OFF: Port2, Power Enable bit controls hot-plug controller
S9[2]	Switch	ON	ON: Port4, Force hot-plug controller on **(Default)** OFF: Port4, Power Enable bit controls hot-plug controller
S9[3]	Switch	ON	ON: Port6, Force hot-plug controller on **(Default)** OFF: Port6, Power Enable bit controls hot-plug controller
S9[4]	Switch	ON	OFF: Hot-plug disabled, enables direct power to downstream port 2 via S9[1] ON: Downstream port 2 power will be controlled by P2_PWRGDN pin **(Default)**
S9[5]	Switch	ON	OFF: Hot-plug disabled, enables direct power to downstream port 4 via S9[2] ON: Downstream port 4 power will be controlled by P4_PWRGDN pin **(Default)**
S9[6]	Switch	ON	OFF: Hot-plug disabled, enables direct power to downstream port 6 via S9[3] ON: Downstream port 6 power will be controlled by P6_PWRGDN pin **(Default)**
W45	Header	2-3 Shunted	2-3: Port 2, +12V source from Upstream port **(Default)** 1-2: Port 2, +12V source from hot-plug controller
W46	Header	2-3 Shunted	2-3: Port 4, +12V source from Upstream port **(Default)** 1-2: Port 4, +12V source from hot-plug controller
W51	Header	2-3 Shunted	2-3: Port 6, +12 source from Upstream port **(Default)** 1-2: Port 6, +12 source from hot-plug controller
W47	Header	2-3 Shunted	2-3: Port 2, +3.3V source from Upstream port **(Default)** 1-2: Port 2, +3.3V source from hot-plug controller
W48	Header	2-3 Shunted	2-3: Port 4, +3.3V source from Upstream port **(Default)** 1-2: Port 4, +3.3V source from hot-plug controller
W53	Header	2-3 Shunted	2-3: Port 6, +3.3V source from Upstream port **(Default)** 1-2: Port 6, +3.3V source from hot-plug controller
W49	Header	2-3 Shunted	2-3: Port 2, +3.3AUX source from upstream port **(Default)** 1-2: Port 2, +3.3V source from hot-plug controller
W50	Header	2-3 Shunted	2-3: Port 4, +3.3AUX source from upstream port **(Default)** 1-2: Port 4, +3.3V source from hot-plug controller
W55	Header	2-3 Shunted	2-3: Port 6, +3.3AUX source from upstream port **(Default)** 1-2: Port 6, +3.3V source from hot-plug controller

Table 2.10 Miscellaneous Jumpers, Headers

Notes

LEDs

There are several LED indicators on the EB32x8G2 which convey status feedback. A description of each is provided in Table 2.11.

Location	Color	Definition
DS14	Green	Port 2: Power-is-good Indicator
DS24	Green	Port 4: Power-is-good Indicator
DS20	Green	Port 6: Power-is-good Indicator
DS16	Green	Port 2: Power Indicator
DS26	Green	Port 4: Power Indicator
DS23	Green	Port 6: Power Indicator
DS15	Yellow	Port 2: Attention Indicator
DS25	Yellow	Port 4: Attention Indicator
DS21	Yellow	Port 6: Attention Indicator
DS27	Green	Port 0: Activity Indicator
DS28	Green	Port 2: Activity Indicator
DS29	Green	Port 4: Activity Indicator
DS30	Green	Port 6: Activity Indicator
DS8	Green	Port 0: Linkup Indicator
DS9	Green	Port 2: Linkup Indicator
DS10	Green	Port 4: Linkup Indicator
DS11	Green	Port 6: Linkup Indicator
DS38	Green	GPIO7
DS37	Green	GPIO6
DS36	Green	GPIO5
DS35	Green	GPIO4
DS34	Green	GPIO3
DS33	Green	GPIO2
DS9	Green	GPIO1
DS3	Green	GPIO0

Table 2.11 LED Indicators

Notes

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved
33	PETp4	Transmitter differential	RSVD	Reserved

Table 2.12 PCI Express x8 Connector Pinout (Part 1 of 2)

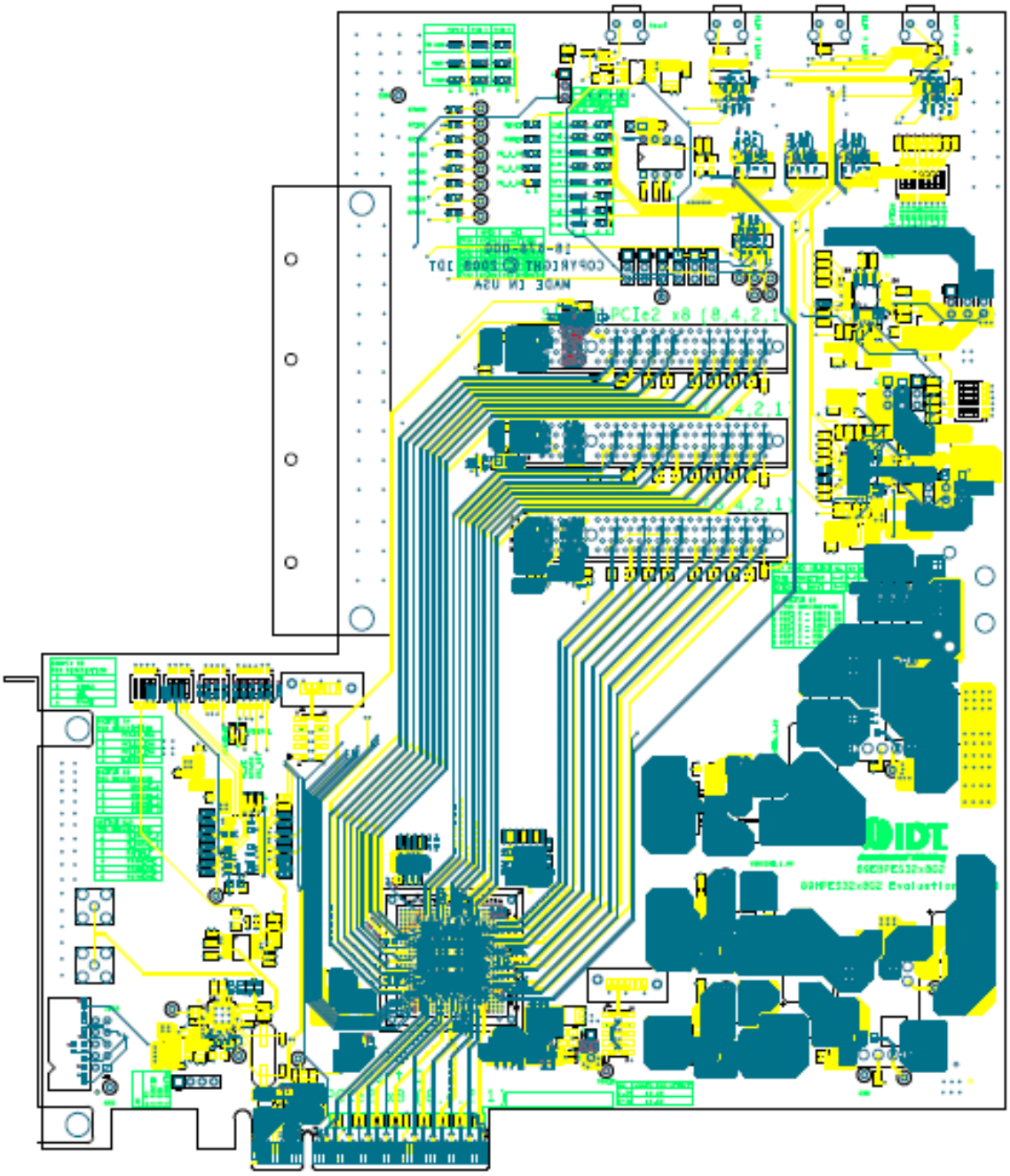
Notes

Pin	Side A		Side B	
34	PETn4	pair, Lane 4	GND	Ground
35	GND	Ground	PERp4	Receiver differential
36	GND	Ground	PERn4	pair, Lane 4
37	PETp5	Transmitter differential	GND	Ground
38	PETn5	pair, Lane 5	GND	Ground
39	GND	Ground	PERp5	Receiver differential
40	GND	Ground	PERn5	pair, Lane 5
41	PETp6	Transmitter differential	GND	Ground
42	PETn6	pair, Lane 6	GND	Ground
43	GND	Ground	PERp6	Receiver differential
44	GND	Ground	PERn6	pair, Lane 6
45	PETp7	Transmitter differential	GND	Ground
46	PETn7	pair, Lane 7	GND	Ground
47	GND	Ground	PERp7	Receiver differential
48	PRSNT2#	Hot-Plug presence detect	PERn7	pair, Lane 7
49	GND	Ground	GND	Ground

Table 2.12 PCI Express x8 Connector Pinout (Part 2 of 2)

Note: These x8 PCI Express connectors comply with the PCIe specification. According to the PCI Express specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB32x8G2, all PRSNT2# pins are tied together. This allows a board with a x1 or x4 width to be installed.

EB32x8G2 Board Figure



Software for the EB32x8G2 Eval Board

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Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB32x8G2 evaluation board using the device management software.

Device Management Software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES32x8G2 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES32x8G2.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES32x8G2, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES32x8G2 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

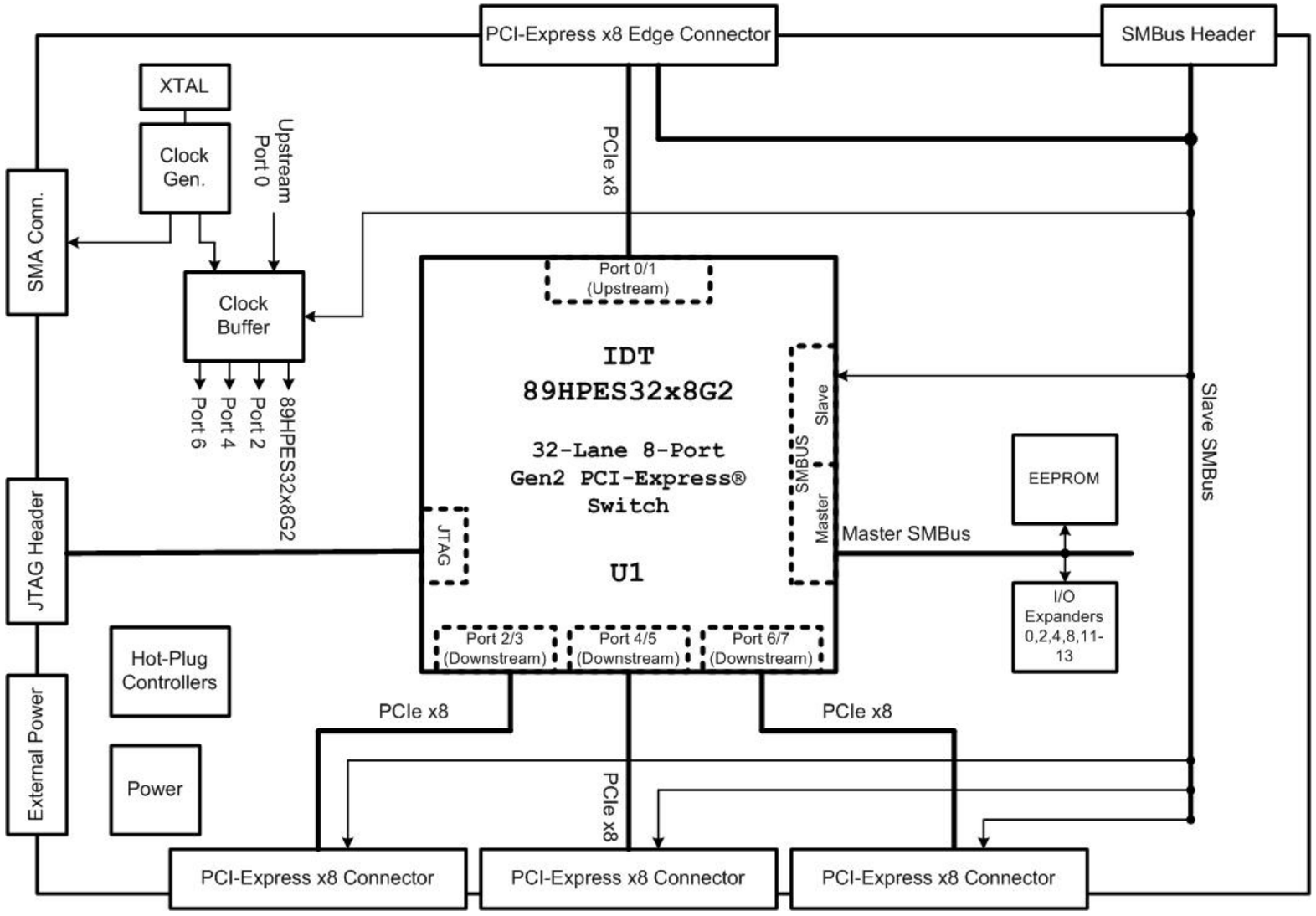
Notes

Schematics

Notes

Schematics

89EBPES32x8G2 – 89HPES32x8G2 Evaluation Board

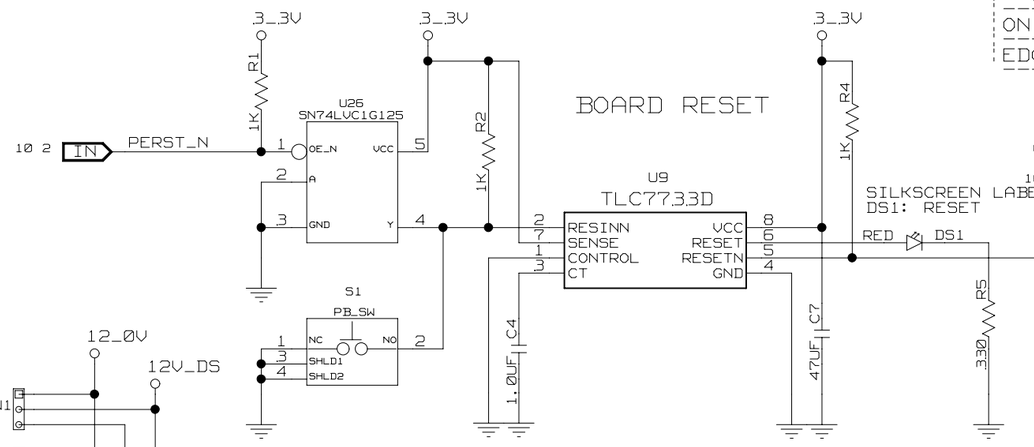


REVISIONS				
DCN	REV	DESCRIPTION	DATE	CHANGE BY
PCB-0172R01	1.0	INITIAL RELEASE	2008-09-23	T. TRAN

SHEET DESCRIPTION

TITLE: 89EBPES32x8G2			
SIZE: B	DRAWING NO.: SCH-00173	FAB P/N: 18-678-000	REV.: 1.0
AUTHOR: T. Tran		CHECKED BY: D. Huang	
Tue Sep 23 17:22:33 2008		SHEET 1 OF 16	

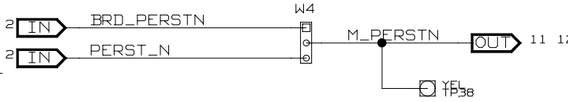
BOARD RESET



SILKSCREEN TABLE

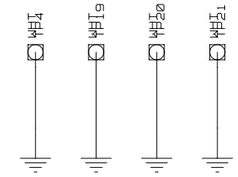
RESET SELECT	W4
ON BOARD CIRCUIT	1-2
EDGE CONNECTOR	2-3

SILKSCREEN LABEL
DS1: RESET

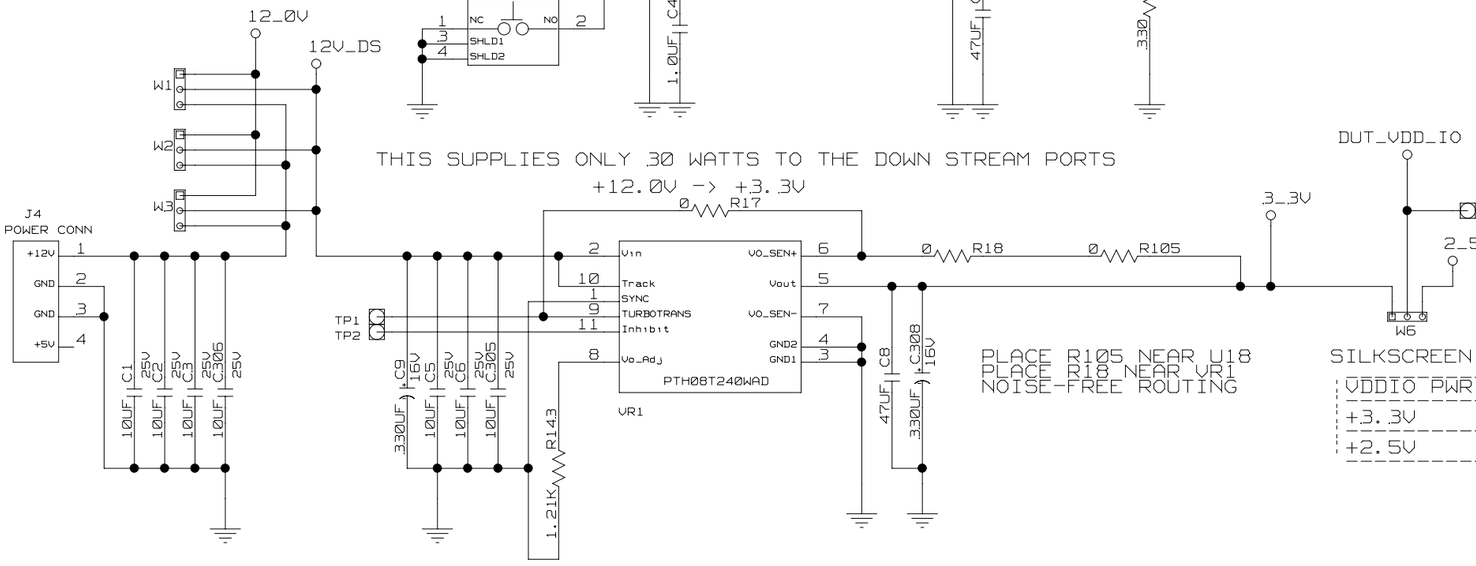


POWER INDICATOR
PLACE NEAR TOP EDGE
LABEL 'POWER'

LABEL 'GND'



THIS SUPPLIES ONLY 30 WATTS TO THE DOWN STREAM PORTS
+12.0V -> +3.3V



PLACE R105 NEAR U18
PLACE TRIM NEAR VR1
NOISE-FREE ROUTING

SILKSCREEN TABLE

VDDIO PWR SELECT	W6
+3.3V	1-2
+2.5V	2-3

SILKSCREEN TABLE

12V POWER SELECT	W1	W2	W3
EDGE CONNECTOR	1-2	1-2	1-2
EXTERNAL INPUT	2-3	2-3	2-3

TITLE 89EBPES32x8G2
POWER, RESET

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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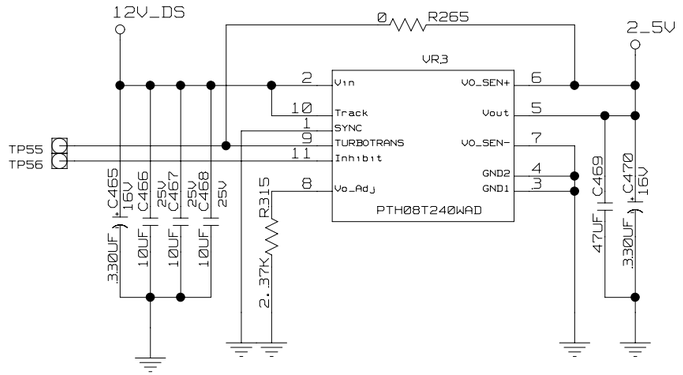
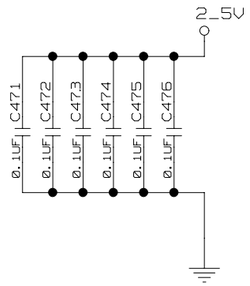
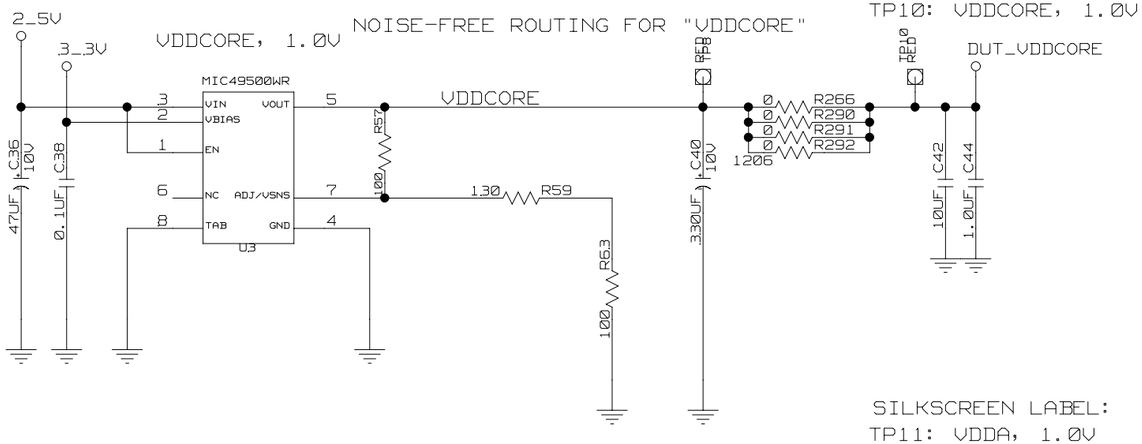
+12.0V -> +2.5V





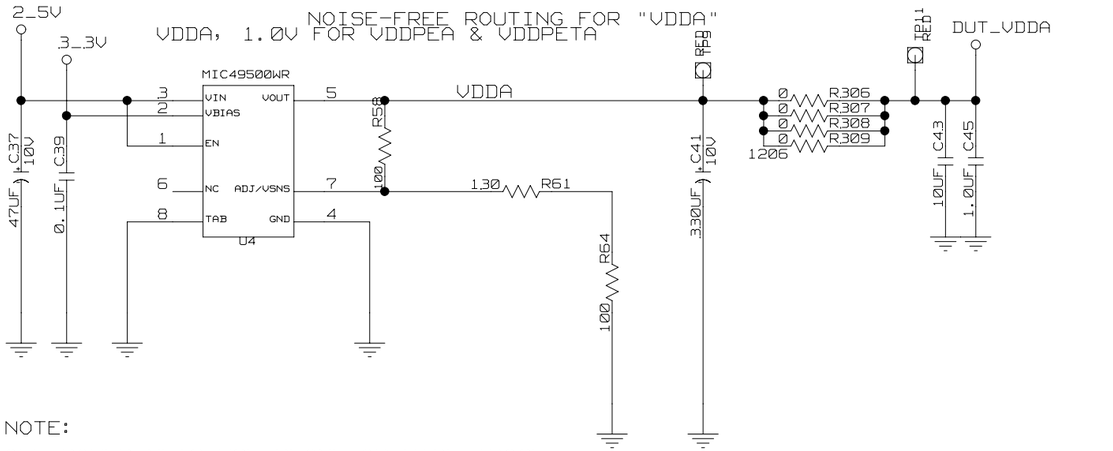
SILKSCREEN LABEL:
TP10: VDDCORE, 1.0V

NOISE-FREE ROUTING FOR "VDDCORE"



SILKSCREEN LABEL:
TP11: VDDA, 1.0V

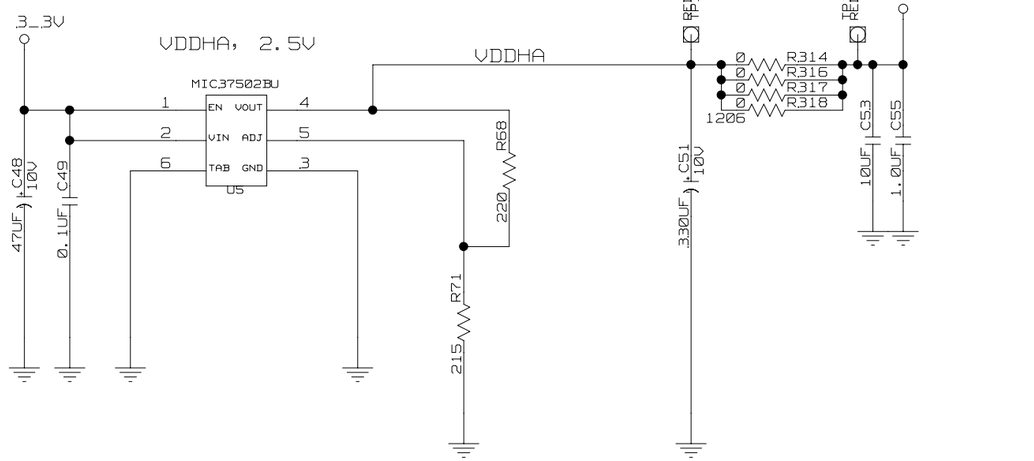
NOISE-FREE ROUTING FOR "VDDA"
VDDA, 1.0V FOR VDDPEA & VDDPETA



NOTE:
ALL POWER NETS USE PLANE OR WIDE TRACE

SILKSCREEN LABEL:
TP15: VDDPEHA, 2.5V

NOISE-FREE ROUTING FOR "VDDHA"



COPPER AREA AS LARGE AS POSSIBLE

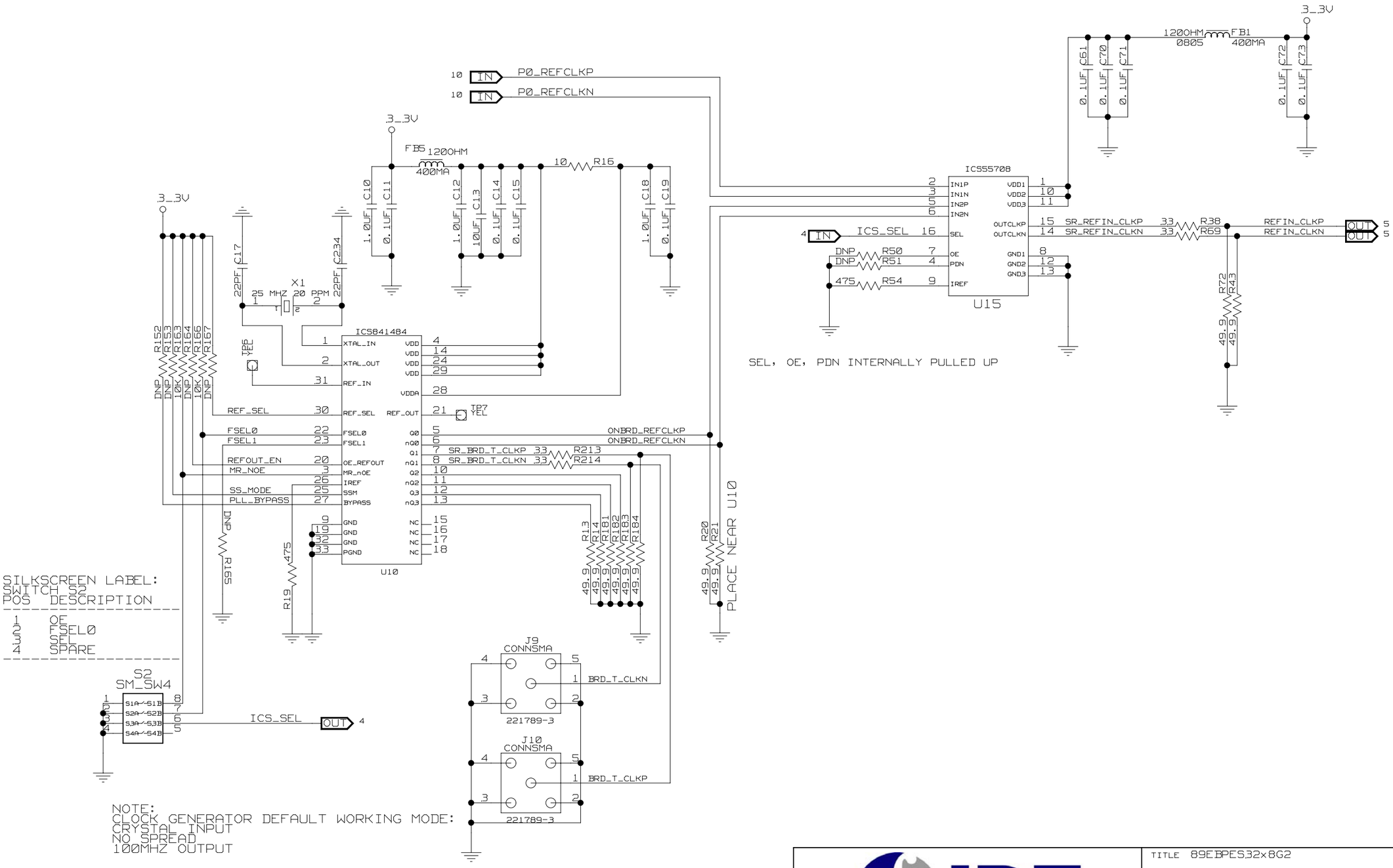
NOTE:
ALL POWER NETS USE PLANE OR WIDE TRACE

TITLE 89EBPES32x8G2
POWER REGULATORS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Tue May 12 17:25:10 2009 SHEET 3 OF 16



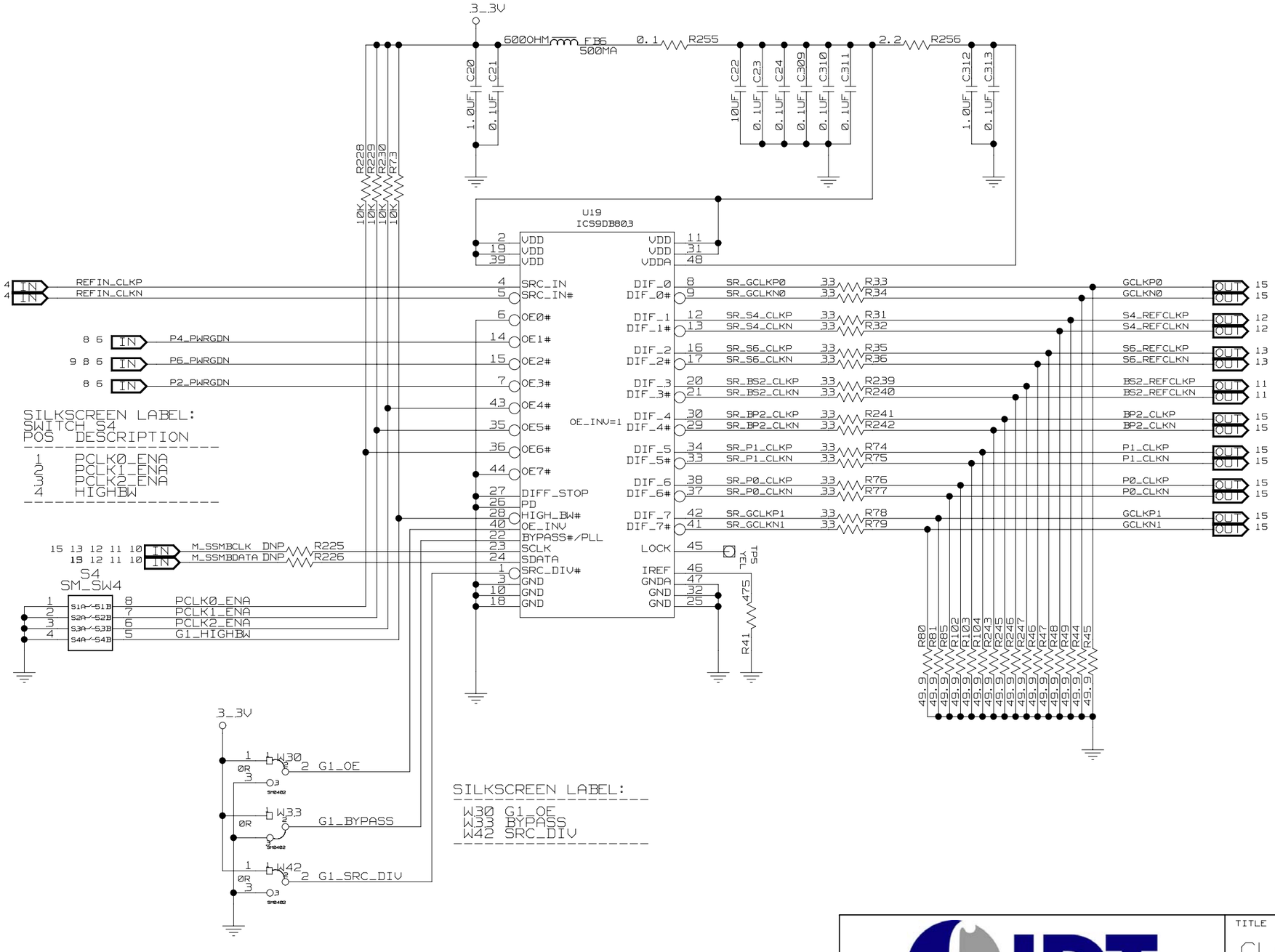
TITLE 89EBPES32x8G2

CLOCK GENERATOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Tue May 12 17:25:06 2009 SHEET 4 OF 16



TITLE 89EBPES32x8G2

CLOCK BUFFER

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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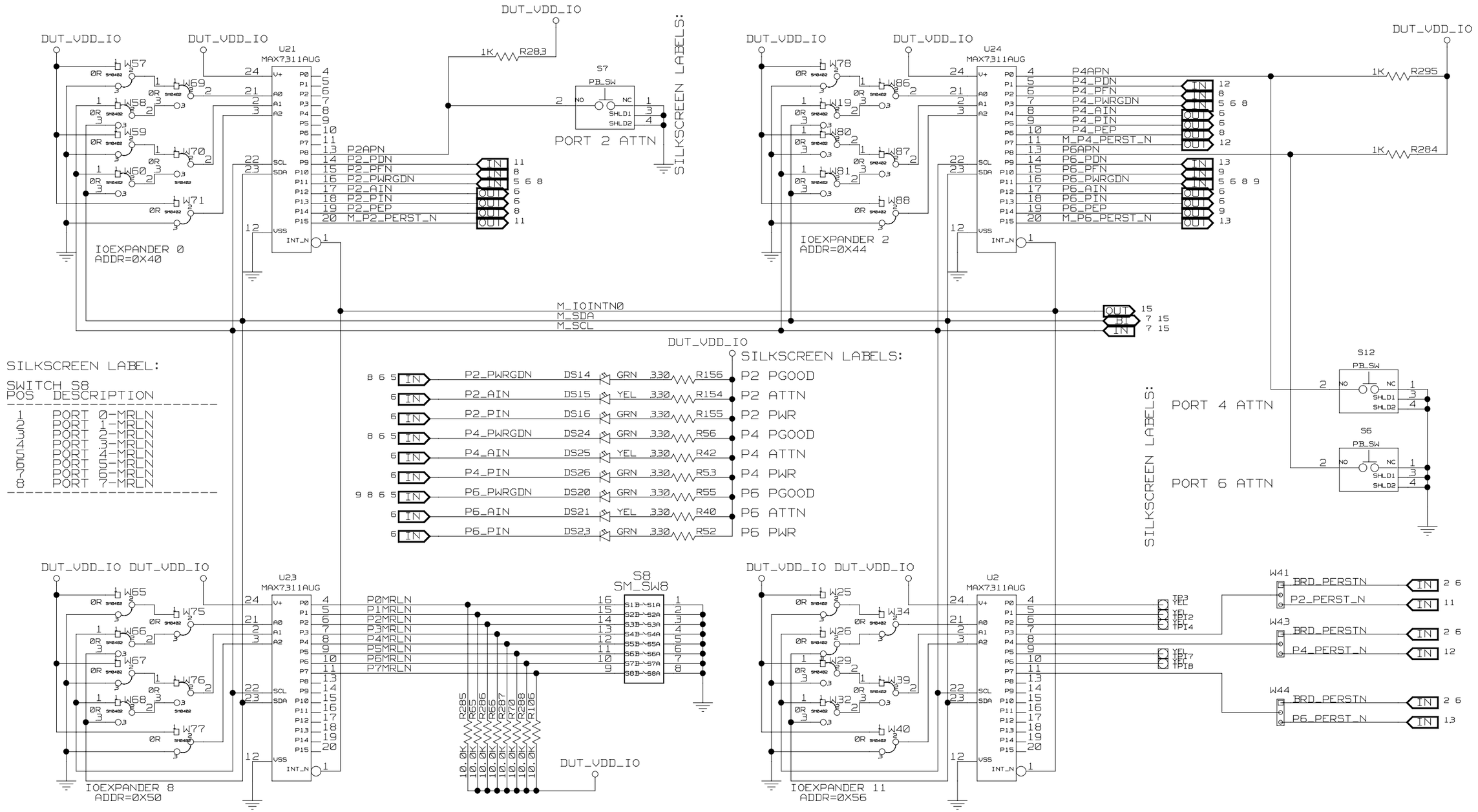

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TITLE 89EBPES32x8G2

I/O EXPANDER, ATTN BUTTONS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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DUT_VDD_IO DUT_VDD_IO

W10 W14 W11 W12 W15 W13 W16 (0R, SMB402)

IOEXPANDER 12
ADDR=0X58

U11
MAX7311AUG

V+ A0 A1 A2 SCL SDA VSS INT_N
P0 P1 P2 P3 P4 P5 P6 P7 P8 P9 P10 P11 P12 P13 P14 P15

PLACE LED NEAR ASSIGNED PORT

DUT_VDD_IO

P0LINKUPN	DS8	GRN	R170	330
P1LINKUPN	DS12	GRN	R107	330
P2LINKUPN	DS9	GRN	R171	330
P3LINKUPN	DS13	GRN	R108	330
P4LINKUPN	DS10	GRN	R172	330
P5LINKUPN	DS17	GRN	R112	330
P6LINKUPN	DS11	GRN	R173	330
P7LINKUPN	DS18	GRN	R115	330

SILKSCREEN LABELS:

P0 LINKUP
P1 LINKUP
P2 LINKUP
P3 LINKUP
P4 LINKUP
P5 LINKUP
P6 LINKUP
P7 LINKUP

M_SDA BI 6 15
M_SCL IN 6 15

3_3VAUX

R128 R129 R130 10.0K

12 IN P4_WAKE_N
13 IN P6_WAKE_N
11 IN P2_WAKE_N

U6 SN74LVC1G125
U7 SN74LVC1G125
U8 SN74LVC1G125

OE_N A GND VCC Y

DNP R132
DNP R131
TP16
P0_WAKE_N OUT 10

C304 C95 C97 C98 C99 0.1UF

DUT_VDD_IO DUT_VDD_IO

W17 W22 W18 W20 W23 W21 W24 (0R, SMB402)

IOEXPANDER 13
ADDR=0X5A

U13
MAX7311AUG

PLACE LED NEAR ASSIGNED PORT

DUT_VDD_IO

P0ACTIVEN	DS27	GRN	R177	330
P1ACTIVEN	DS19	GRN	R116	330
P2ACTIVEN	DS28	GRN	R178	330
P3ACTIVEN	DS22	GRN	R119	330
P4ACTIVEN	DS29	GRN	R179	330
P5ACTIVEN	DS31	GRN	R123	330
P6ACTIVEN	DS30	GRN	R180	330
P7ACTIVEN	DS32	GRN	R125	330

SILKSCREEN LABELS:

P0 ACT
P1 ACT
P2 ACT
P3 ACT
P4 ACT
P5 ACT
P6 ACT
P7 ACT

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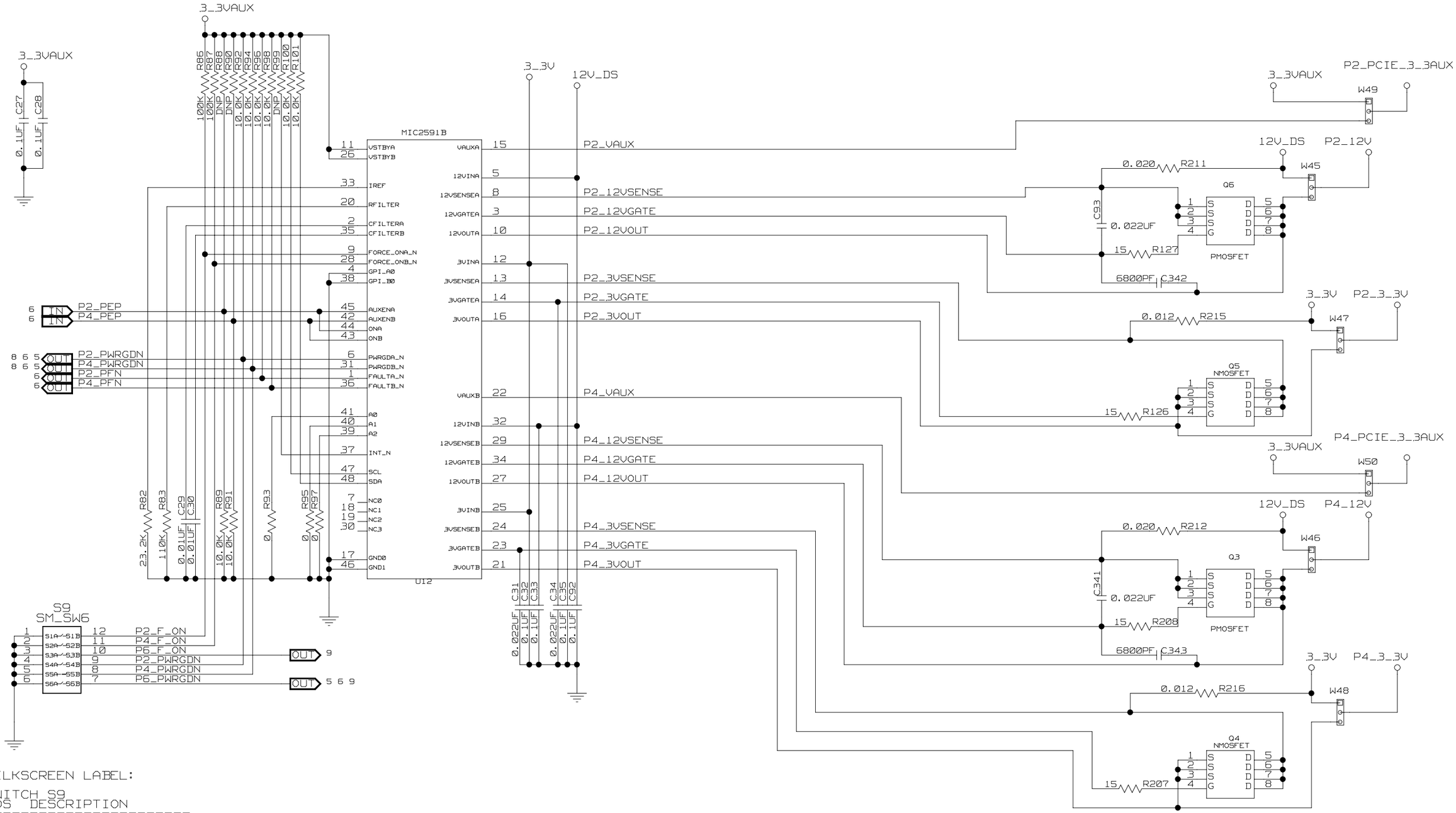
TITLE 89EBPES32x8G2			
IO EXP, WAKE			
SIZE B	DRAWING NO. SCH-00173	FAB P/N 18-678-000	REV. 1.0
AUTHOR T. Tran		CHECKED BY D. Huang	
Tue May 12 17:25:08 2009		SHEET 7 OF 16	



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TITLE 89EBPES32x8G2

HOT SWAP PORT 2, 4

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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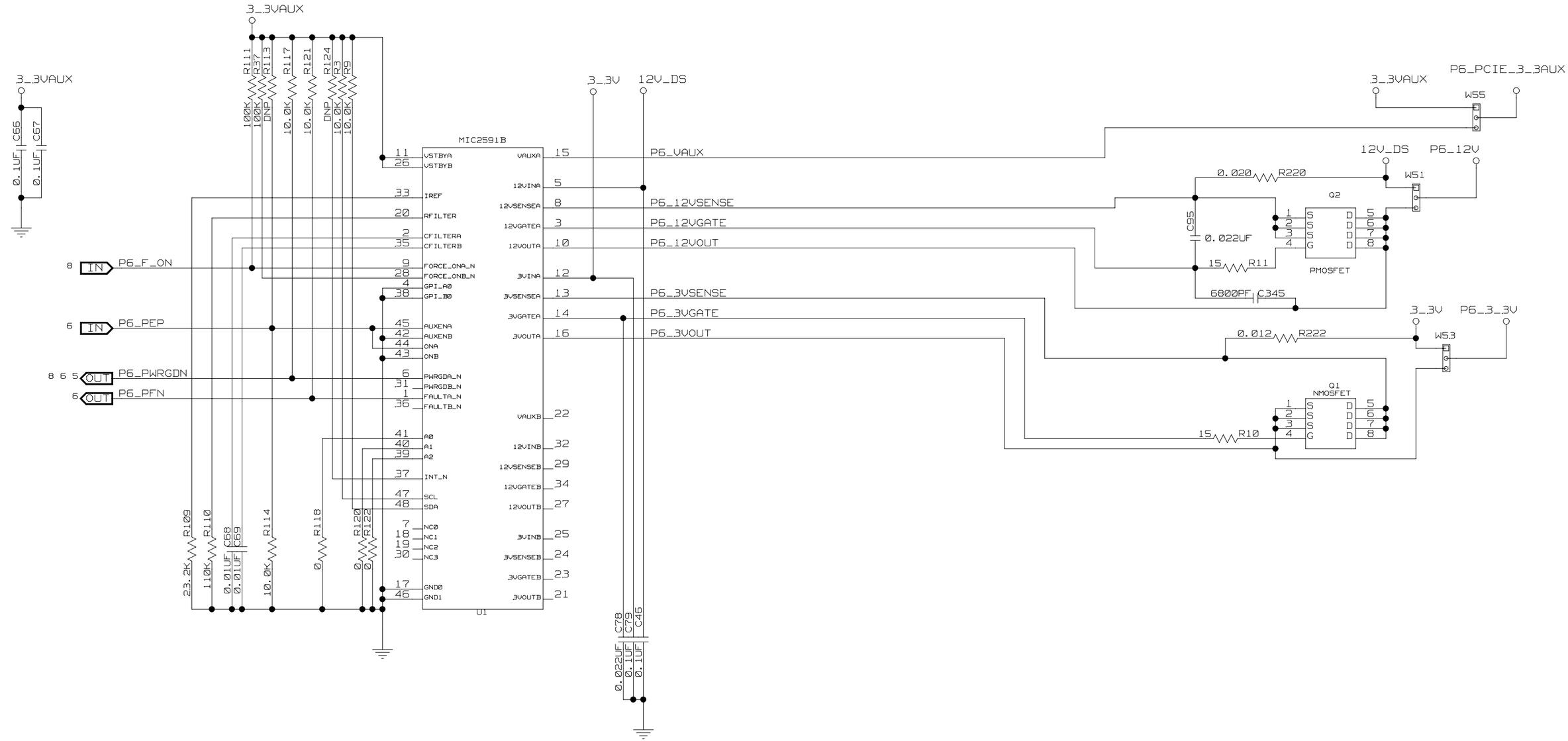

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TITLE 89EBPES32x8G2

HOT SWAP PORT 6

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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SILKSCREEN LABEL:

SWITCH_J8

POS	DESCRIPTION
4	SMBDATA
3	GND
2	SMBCLK
1	NC

DUT_VDD_IO

1K R158
1K R159

J8 4 3 2 1

15 13 12 11 5 OUT B1 — M_SSMBCLK
15 12 11 5 — M_SSMBDATA

DNP R160
DNP R161

3_3VAUX P0_3_3V 12_0V

C62 10UF
C63 10UF 25V

PCIE_ADD_ON_PRESENT_N

12_0V P0_3_3V

C64 10UF 25V
C65 10UF

PCIe x8 EDGE

B1	+12V	PRSTN1#	A1
B2	+12V	+12V	A2
B3	RSVD	+12V	A3
B4	GND	GND	A4
B5	SMCLK	JTAG_TCK	A5
B6	SMDAT	JTAG_TDI	A6
B7	GND	JTAG_TDO	A7
B8	+3.3V	JTAG_TMS	A8
B9	JTAG_TRSTN	+3.3V	A9
B10	3.3VAUX	+3.3V	A10
B11	WAKE#	PERST#	A11
B12	RSVD	GND	A12
B13	GND	REFCLK+	A13
B14	PETP0	REFCLK-	A14
B15	PETN0	GND	A15
B16	GND	PERP0	A16
B17	PRSTN2#	PERN0	A17
B18	GND	GND	A18
B19	PETP1	RSVD	A19
B20	PETN1	GND	A20
B21	GND	PERP1	A21
B22	GND	PERN1	A22
B23	PETP2	GND	A23
B24	PETN2	GND	A24
B25	GND	PERP2	A25
B26	GND	PERN2	A26
B27	PETP3	GND	A27
B28	PETN3	GND	A28
B29	GND	PERP3	A29
B30	RSVD	PERN3	A30
B31	PRSTN2#	GND	A31
B32	GND	RSVD	A32
B33	PETP4	RSVD	A33
B34	PETN4	GND	A34
B35	GND	PERP4	A35
B36	GND	PERN4	A36
B37	PETP5	GND	A37
B38	PETN5	GND	A38
B39	GND	PERP5	A39
B40	GND	PERN5	A40
B41	PETP6	GND	A41
B42	PETN6	GND	A42
B43	GND	PERP6	A43
B44	GND	PERN6	A44
B45	PETP7	GND	A45
B46	PETN7	GND	A46
B47	GND	PERP7	A47
B48	PRSTN2#	PERN7	A48
B49	GND	GND	A49

P1

7 IN P0_WAKE_N

PERST_N OUT 2

P0_REFCLKP OUT 4
P0_REFCLKN OUT 4

LANE REVERSED TO OPTIMIZE ROUTING

LANE REVERSED TO OPTIMIZE ROUTING

14 OUT	P1_PERP<3>	P1_PERN<3>	OUT 14
14 OUT	P1_PERP<2>	P1_PERN<2>	OUT 14
14 OUT	P1_PERP<1>	P1_PERN<1>	OUT 14
14 OUT	P1_PERP<0>	P1_PERN<0>	OUT 14
14 OUT	P0_PERP<3>	P0_PERN<3>	OUT 14
14 OUT	P0_PERP<2>	P0_PERN<2>	OUT 14
14 OUT	P0_PERP<1>	P0_PERN<1>	OUT 14
14 OUT	P0_PERP<0>	P0_PERN<0>	OUT 14

DNP R162
DNP R244

P1_PETP<3>	P1_PETN<3>	IN 14	IN 14
P1_PETP<2>	P1_PETN<2>	IN 14	IN 14
P1_PETP<1>	P1_PETN<1>	IN 14	IN 14
P1_PETP<0>	P1_PETN<0>	IN 14	IN 14
P0_PETP<3>	P0_PETN<3>	IN 14	IN 14
P0_PETP<2>	P0_PETN<2>	IN 14	IN 14
P0_PETP<1>	P0_PETN<1>	IN 14	IN 14
P0_PETP<0>	P0_PETN<0>	IN 14	IN 14

SILKSCREEN LABEL:

CONECTOR P1

PORT 0 PCIE2 X8(8,4,2,1)

TITLE 89EBPES32x8G2

PORT 0 UPSTREAM EDGE CONN.

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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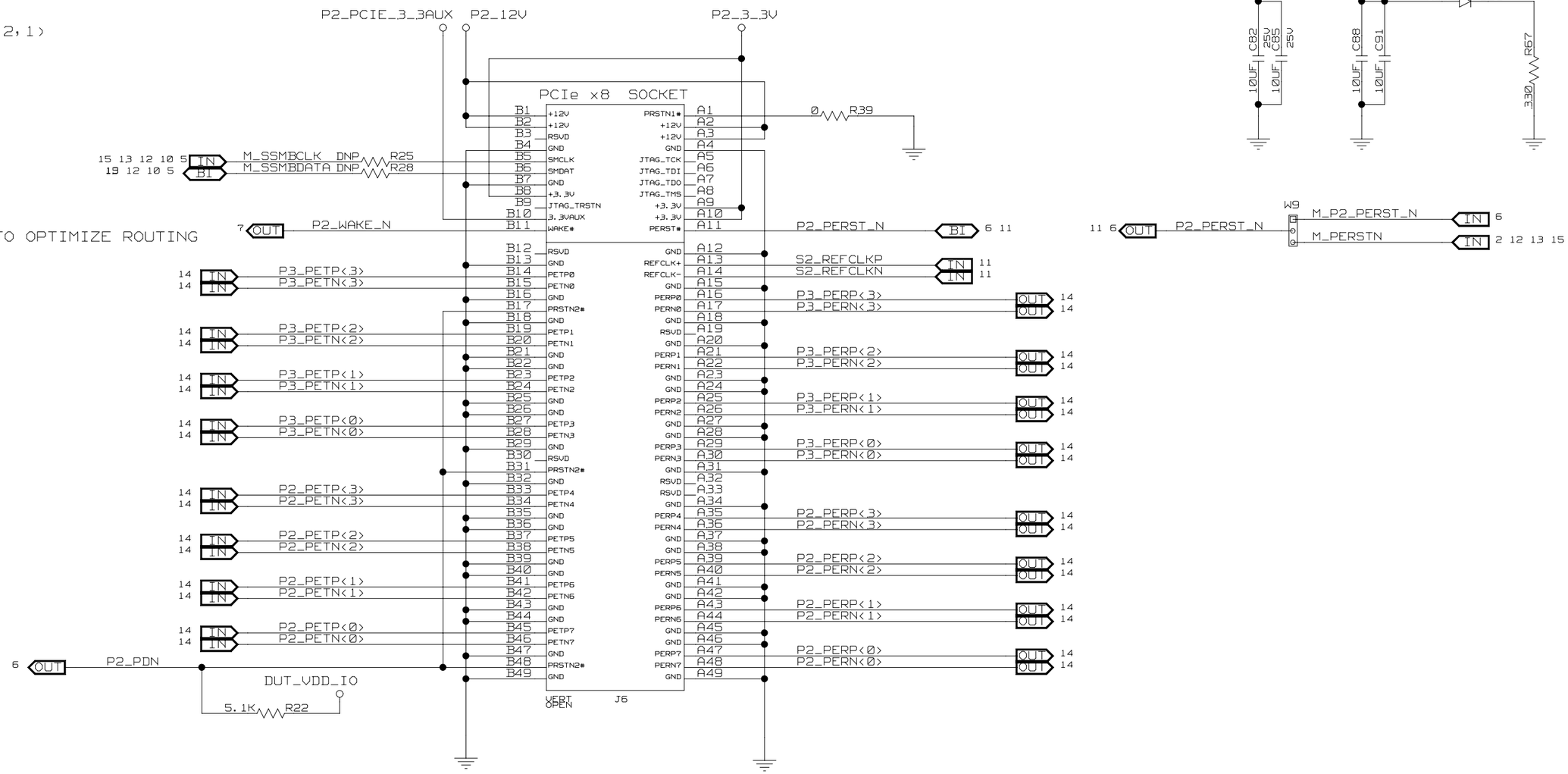
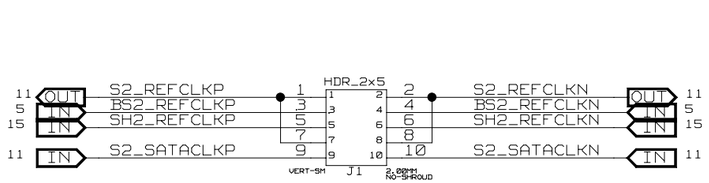
SILKSCREEN LABEL:

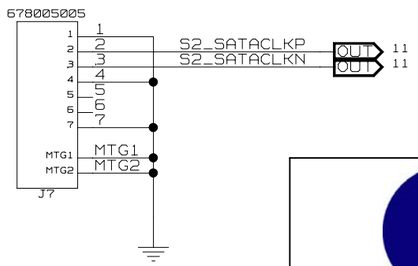
CONECTOR J6

SLOT 2 PCIE2 X8(8,4,2,1)

LANE REVERSED TO OPTIMIZE ROUTING







TITLE 89EBPES32x8G2

PORT 2 - SLOT CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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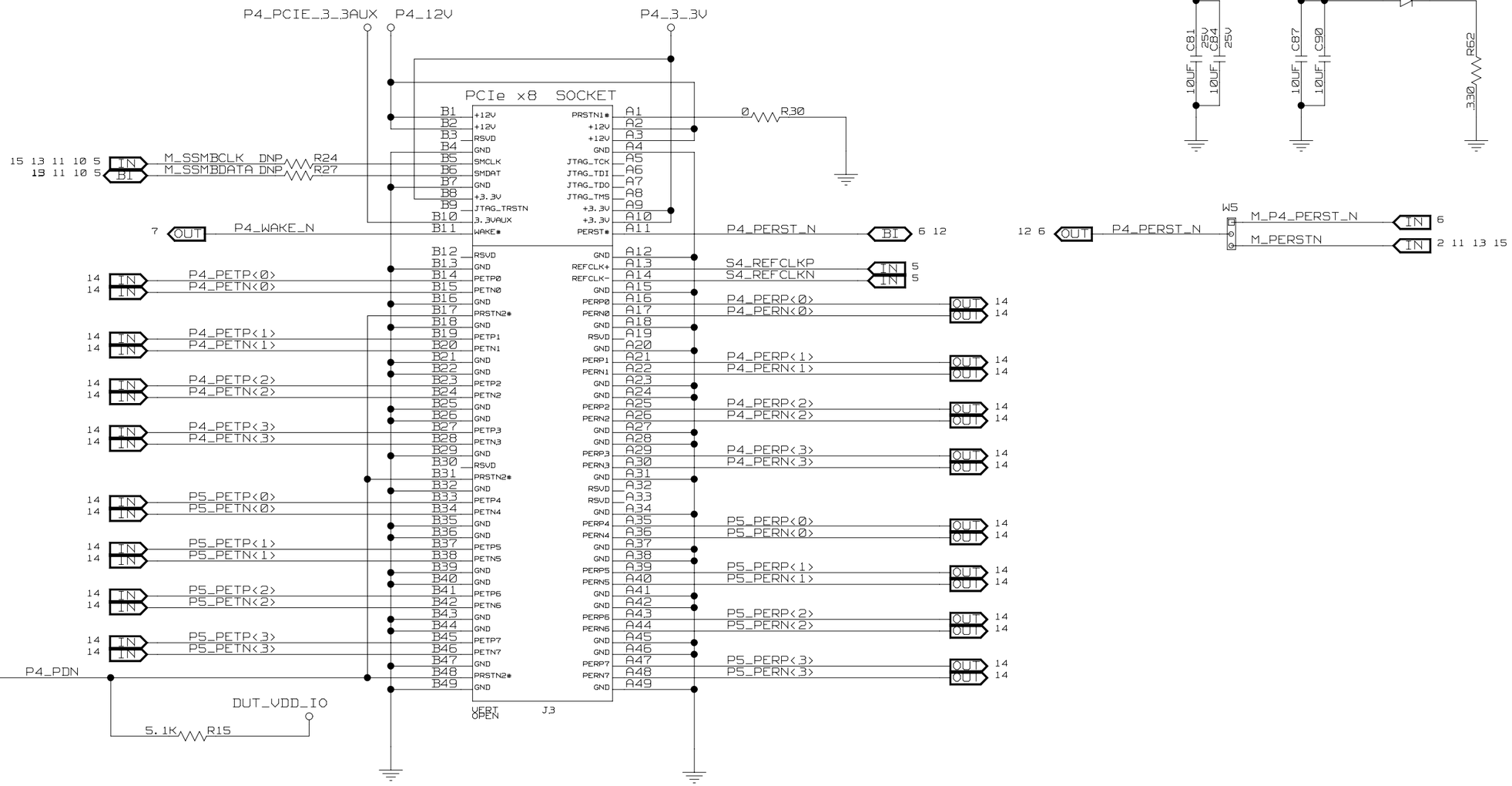

SILKSCREEN LABEL:

CONECTOR J3

SLOT 4 PCIE2 X8(8,4,2,1)

TITLE 89EBPES32x8G2

PORT 4 - SLOT CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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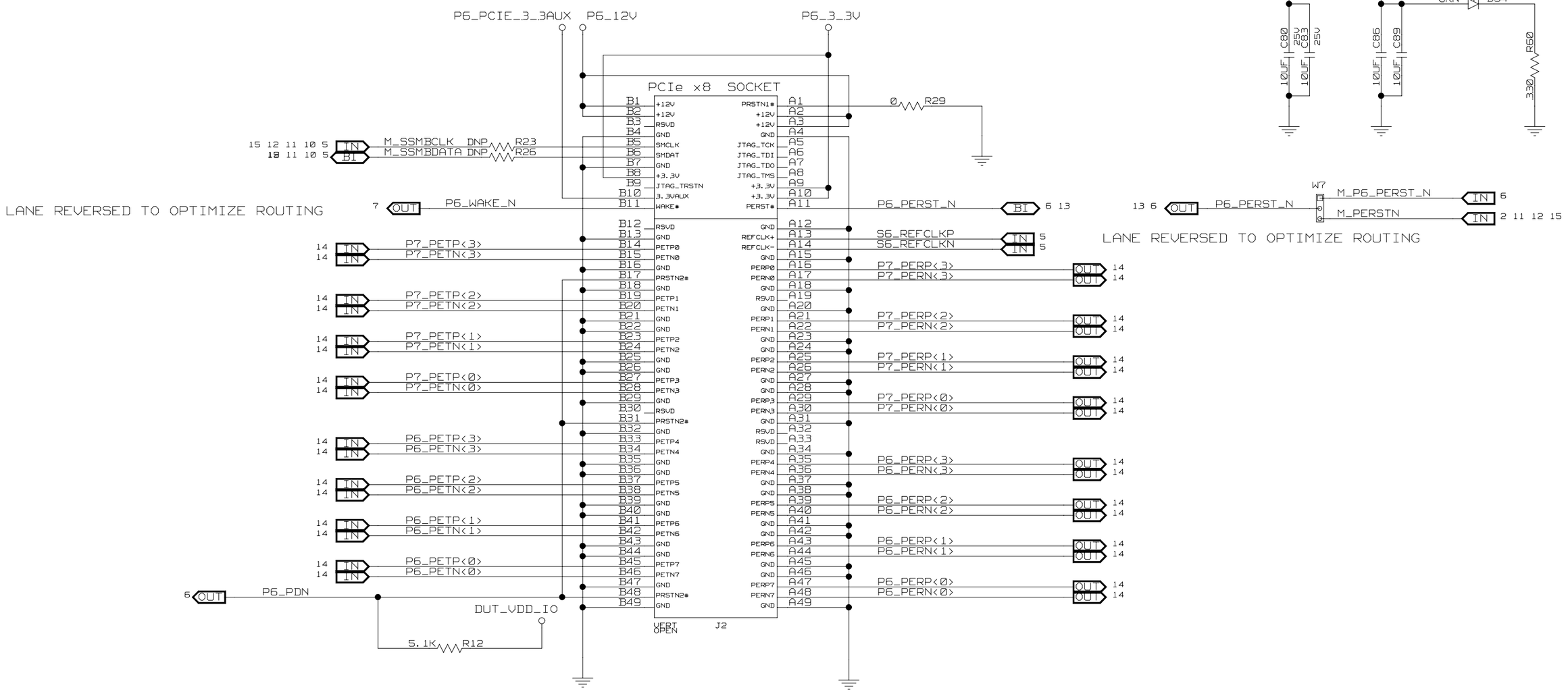

SILKSCREEN LABEL:

CONECTOR J2

SLOT 6 PCIE2 X8(8,4,2,1)

TITLE 89EBPES32x8G2

PORT 6 - SLOT CONNECTOR

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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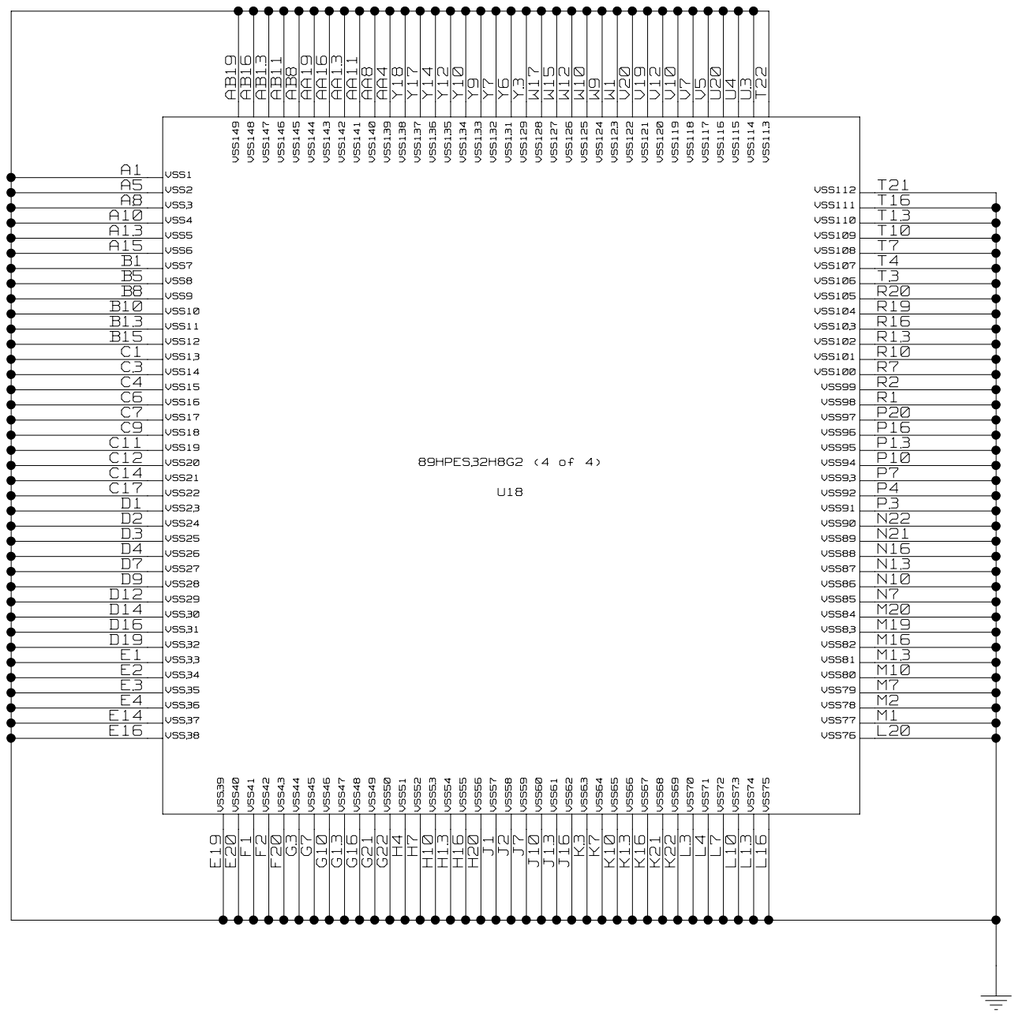
PLACE CAPS CLOSE TO CONNECTORS

89HPES32H8G2 (2 of 4)

10	IN	P0_PERP<0>	G20	PE00RP0	PE00TP0	E22	AC_P0_PETP0	0.1UF	C135	P0_PETP<0>	OUT	10
10	IN	P0_PERN<0>	G19	PE00RN0	PE00TN0	E21	AC_P0_PETN0	0.1UF	C120	P0_PETN<0>	OUT	10
10	IN	P0_PERP<1>	H19	PE00RP1	PE00TP1	F22	AC_P0_PETP1	0.1UF	C137	P0_PETP<1>	OUT	10
10	IN	P0_PERN<1>	H18	PE00RN1	PE00TN1	F21	AC_P0_PETN1	0.1UF	C121	P0_PETN<1>	OUT	10
10	IN	P0_PERP<2>	K20	PE00RP2	PE00TP2	L22	AC_P0_PETP2	0.1UF	C138	P0_PETP<2>	OUT	10
10	IN	P0_PERN<2>	K19	PE00RN2	PE00TN2	L21	AC_P0_PETN2	0.1UF	C122	P0_PETN<2>	OUT	10
10	IN	P0_PERP<3>	L18	PE00RP3	PE00TP3	M22	AC_P0_PETP3	0.1UF	C139	P0_PETP<3>	OUT	10
10	IN	P0_PERN<3>	L19	PE00RN3	PE00TN3	M21	AC_P0_PETN3	0.1UF	C123	P0_PETN<3>	OUT	10
10	IN	P1_PERP<0>	N19	PE01RP0	PE01TP0	P22	AC_P1_PETP0	0.1UF	C140	P1_PETP<0>	OUT	10
10	IN	P1_PERN<0>	N20	PE01RN0	PE01TN0	P21	AC_P1_PETN0	0.1UF	C124	P1_PETN<0>	OUT	10
10	IN	P1_PERP<1>	P18	PE01RP1	PE01TP1	R22	AC_P1_PETP1	0.1UF	C141	P1_PETP<1>	OUT	10
10	IN	P1_PERN<1>	P19	PE01RN1	PE01TN1	R21	AC_P1_PETN1	0.1UF	C125	P1_PETN<1>	OUT	10
10	IN	P1_PERP<2>	T19	PE01RP2	PE01TP2	U22	AC_P1_PETP2	0.1UF	C142	P1_PETP<2>	OUT	10
10	IN	P1_PERN<2>	T20	PE01RN2	PE01TN2	U21	AC_P1_PETN2	0.1UF	C126	P1_PETN<2>	OUT	10
10	IN	P1_PERP<3>	U18	PE01RP3	PE01TP3	V22	AC_P1_PETP3	0.1UF	C143	P1_PETP<3>	OUT	10
10	IN	P1_PERN<3>	U19	PE01RN3	PE01TN3	V21	AC_P1_PETN3	0.1UF	C127	P1_PETN<3>	OUT	10
11	IN	P2_PERP<0>	D18	PE02RP0	PE02TP0	A17	AC_P2_PETP0	0.1UF	C381	P2_PETP<0>	OUT	11
11	IN	P2_PERN<0>	C18	PE02RN0	PE02TN0	B17	AC_P2_PETN0	0.1UF	C357	P2_PETN<0>	OUT	11
11	IN	P2_PERP<1>	E17	PE02RP1	PE02TP1	A16	AC_P2_PETP1	0.1UF	C378	P2_PETP<1>	OUT	11
11	IN	P2_PERN<1>	D17	PE02RN1	PE02TN1	B16	AC_P2_PETN1	0.1UF	C107	P2_PETN<1>	OUT	11
11	IN	P2_PERP<2>	D15	PE02RP2	PE02TP2	A12	AC_P2_PETP2	0.1UF	C375	P2_PETP<2>	OUT	11
11	IN	P2_PERN<2>	C15	PE02RN2	PE02TN2	B12	AC_P2_PETN2	0.1UF	C104	P2_PETN<2>	OUT	11
11	IN	P2_PERP<3>	D13	PE02RP3	PE02TP3	A11	AC_P2_PETP3	0.1UF	C372	P2_PETP<3>	OUT	11
11	IN	P2_PERN<3>	C13	PE02RN3	PE02TN3	B11	AC_P2_PETN3	0.1UF	C101	P2_PETN<3>	OUT	11
11	IN	P3_PERP<0>	D10	PE03RP0	PE03TP0	A7	AC_P3_PETP0	0.1UF	C393	P3_PETP<0>	OUT	11
11	IN	P3_PERN<0>	C10	PE03RN0	PE03TN0	B7	AC_P3_PETN0	0.1UF	C369	P3_PETN<0>	OUT	11
11	IN	P3_PERP<1>	D8	PE03RP1	PE03TP1	A6	AC_P3_PETP1	0.1UF	C390	P3_PETP<1>	OUT	11
11	IN	P3_PERN<1>	C8	PE03RN1	PE03TN1	B6	AC_P3_PETN1	0.1UF	C366	P3_PETN<1>	OUT	11
11	IN	P3_PERP<2>	E6	PE03RP2	PE03TP2	A4	AC_P3_PETP2	0.1UF	C387	P3_PETP<2>	OUT	11
11	IN	P3_PERN<2>	D6	PE03RN2	PE03TN2	B4	AC_P3_PETN2	0.1UF	C363	P3_PETN<2>	OUT	11
11	IN	P3_PERP<3>	D5	PE03RP3	PE03TP3	A3	AC_P3_PETP3	0.1UF	C384	P3_PETP<3>	OUT	11
11	IN	P3_PERN<3>	C5	PE03RN3	PE03TN3	B3	AC_P3_PETN3	0.1UF	C360	P3_PETN<3>	OUT	11
12	IN	P4_PERP<0>	V4	PE04RP0	PE04TP0	U1	AC_P4_PETP0	0.1UF	C380	P4_PETP<0>	OUT	12
12	IN	P4_PERN<0>	V3	PE04RN0	PE04TN0	U2	AC_P4_PETN0	0.1UF	C356	P4_PETN<0>	OUT	12
12	IN	P4_PERP<1>	R4	PE04RP1	PE04TP1	T1	AC_P4_PETP1	0.1UF	C377	P4_PETP<1>	OUT	12
12	IN	P4_PERN<1>	R3	PE04RN1	PE04TN1	T2	AC_P4_PETN1	0.1UF	C106	P4_PETN<1>	OUT	12
12	IN	P4_PERP<2>	N5	PE04RP2	PE04TP2	P1	AC_P4_PETP2	0.1UF	C374	P4_PETP<2>	OUT	12
12	IN	P4_PERN<2>	N4	PE04RN2	PE04TN2	P2	AC_P4_PETN2	0.1UF	C103	P4_PETN<2>	OUT	12
12	IN	P4_PERP<3>	M4	PE04RP3	PE04TP3	N1	AC_P4_PETP3	0.1UF	C371	P4_PETP<3>	OUT	12
12	IN	P4_PERN<3>	M3	PE04RN3	PE04TN3	N2	AC_P4_PETN3	0.1UF	C100	P4_PETN<3>	OUT	12
12	IN	P5_PERP<0>	K5	PE05RP0	PE05TP0	L1	AC_P5_PETP0	0.1UF	C57	P5_PETP<0>	OUT	12
12	IN	P5_PERN<0>	K4	PE05RN0	PE05TN0	L2	AC_P5_PETN0	0.1UF	C16	P5_PETN<0>	OUT	12
12	IN	P5_PERP<1>	J4	PE05RP1	PE05TP1	K1	AC_P5_PETP1	0.1UF	C58	P5_PETP<1>	OUT	12
12	IN	P5_PERN<1>	J3	PE05RN1	PE05TN1	K2	AC_P5_PETN1	0.1UF	C25	P5_PETN<1>	OUT	12
12	IN	P5_PERP<2>	G5	PE05RP2	PE05TP2	H1	AC_P5_PETP2	0.1UF	C59	P5_PETP<2>	OUT	12
12	IN	P5_PERN<2>	G4	PE05RN2	PE05TN2	H2	AC_P5_PETN2	0.1UF	C26	P5_PETN<2>	OUT	12
12	IN	P5_PERP<3>	F4	PE05RP3	PE05TP3	G1	AC_P5_PETP3	0.1UF	C60	P5_PETP<3>	OUT	12
12	IN	P5_PERN<3>	F3	PE05RN3	PE05TN3	G2	AC_P5_PETN3	0.1UF	C56	P5_PETN<3>	OUT	12
13	IN	P6_PERP<0>	W5	PE06RP0	PE06TP0	AB6	AC_P6_PETP0	0.1UF	C382	P6_PETP<0>	OUT	13
13	IN	P6_PERN<0>	Y5	PE06RN0	PE06TN0	AA6	AC_P6_PETN0	0.1UF	C358	P6_PETN<0>	OUT	13
13	IN	P6_PERP<1>	V6	PE06RP1	PE06TP1	AB7	AC_P6_PETP1	0.1UF	C379	P6_PETP<1>	OUT	13
13	IN	P6_PERN<1>	W6	PE06RN1	PE06TN1	AA7	AC_P6_PETN1	0.1UF	C355	P6_PETN<1>	OUT	13
13	IN	P6_PERP<2>	W8	PE06RP2	PE06TP2	AB9	AC_P6_PETP2	0.1UF	C376	P6_PETP<2>	OUT	13
13	IN	P6_PERN<2>	Y8	PE06RN2	PE06TN2	AA9	AC_P6_PETN2	0.1UF	C105	P6_PETN<2>	OUT	13
13	IN	P6_PERP<3>	W11	PE06RP3	PE06TP3	AB10	AC_P6_PETP3	0.1UF	C373	P6_PETP<3>	OUT	13
13	IN	P6_PERN<3>	Y11	PE06RN3	PE06TN3	AA10	AC_P6_PETN3	0.1UF	C102	P6_PETN<3>	OUT	13
13	IN	P7_PERP<0>	W13	PE07RP0	PE07TP0	AB14	AC_P7_PETP0	0.1UF	C394	P7_PETP<0>	OUT	13
13	IN	P7_PERN<0>	Y13	PE07RN0	PE07TN0	AA14	AC_P7_PETN0	0.1UF	C370	P7_PETN<0>	OUT	13
13	IN	P7_PERP<1>	V14	PE07RP1	PE07TP1	AB15	AC_P7_PETP1	0.1UF	C391	P7_PETP<1>	OUT	13
13	IN	P7_PERN<1>	W14	PE07RN1	PE07TN1	AA15	AC_P7_PETN1	0.1UF	C367	P7_PETN<1>	OUT	13
13	IN	P7_PERP<2>	W16	PE07RP2	PE07TP2	AB17	AC_P7_PETP2	0.1UF	C388	P7_PETP<2>	OUT	13
13	IN	P7_PERN<2>	Y16	PE07RN2	PE07TN2	AA17	AC_P7_PETN2	0.1UF	C364	P7_PETN<2>	OUT	13
13	IN	P7_PERP<3>	W19	PE07RP3	PE07TP3	AB18	AC_P7_PETP3	0.1UF	C385	P7_PETP<3>	OUT	13
13	IN	P7_PERN<3>	Y19	PE07RN3	PE07TN3	AA18	AC_P7_PETN3	0.1UF	C361	P7_PETN<3>	OUT	13

U18

PLACE CAPS CLOSE TO CONNECTORS



TITLE 89EBPES32x8G2

DUT SERDES, GROUND

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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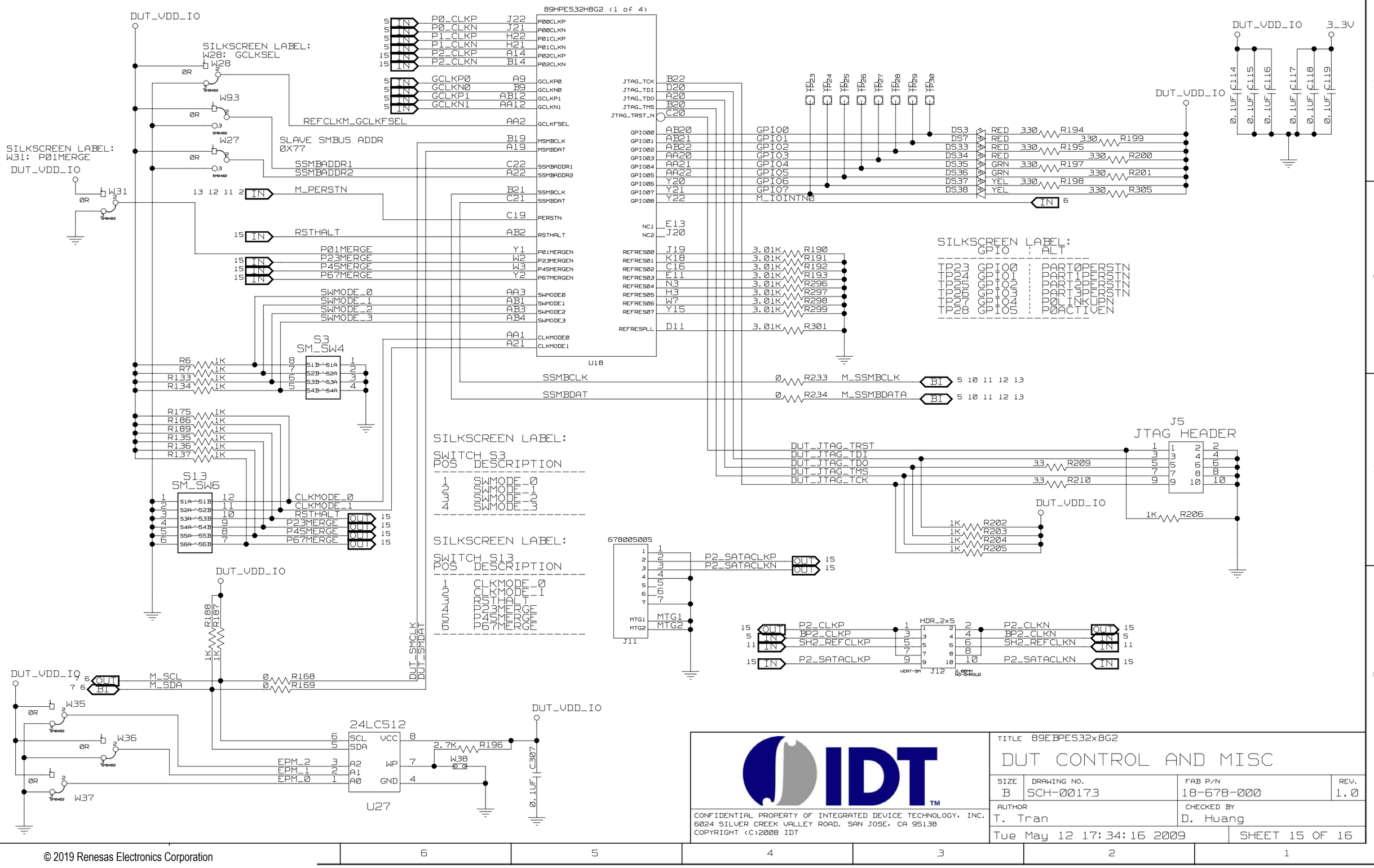

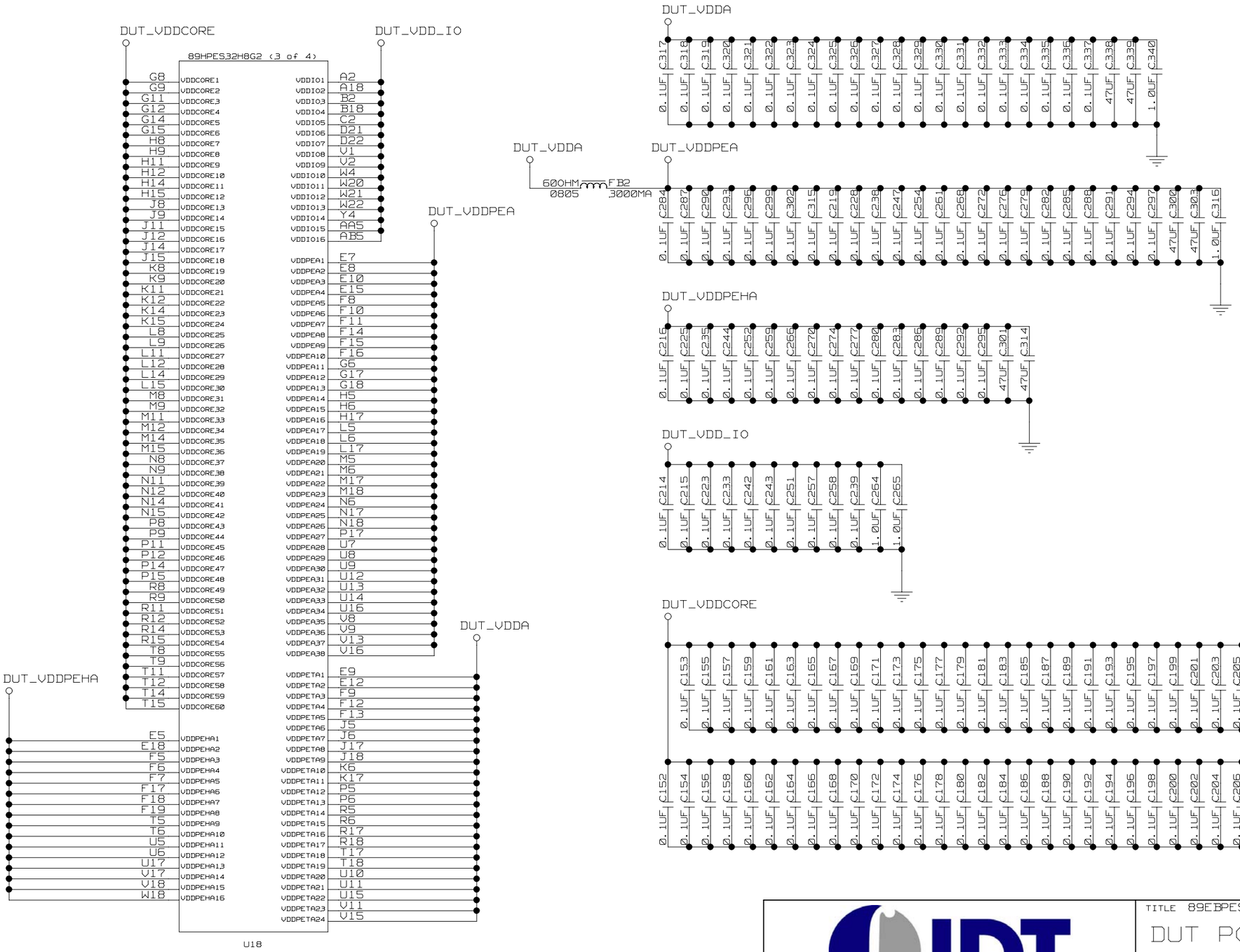

TITLE 89EBPES32x8G2

DUT POWER SUPPLY

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00173	18-678-000	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Tue May 12 17:25:14 2009 SHEET 16 OF 16

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