

Board Features

- Single x1 lane, 2.5 Gbps PCIe extended height riser card
- Fully compliant with PCI Express Specification (Revision 1.1)
- Four 32-bit, 25–66 MHz, PCI slots
- Serial EEPROM that can be programmed with optimized settings for the Tsi382
- PCI power supported through system or external ATX supply
- 3.3V/Universal PCI card support
- Optional 5V PCI card support
- Optional on-board PCIe reference clock
- Optional on-board PCI bus clock
- Manual and auto-detect PCI bus clock frequency
- Over current protection

Board Benefits

- Evaluate features and functionalities of the Tsi382
- Test and tune performance of the Tsi382 in desired application
- Prototype hardware development before finalizing application design

Board Overview

The IDT Tsi382 evaluation board is ideal for evaluating and prototyping the Tsi382 PCIe-to-PCI bridge. The Tsi382 evaluation board is an extended height x1 PCIe card that is designed to fit into a standard PCIe slot on a PC motherboard, or interconnect with other cards equipped with a standard PCIe connector.

The evaluation board uses the Tsi382 to bridge between x1 PCIe on the card edge to four 32-bit PCI slots on the board.

Developers can plug 32-bit 3.3V or Universal PCI adapter cards into any or all of the four slots. The evaluation board can adapt the cards to PCIe allowing developers to test the design's behavior on the PCI card when bridging to PCIe. For example, a PC card developer can take an existing PCI adapter card and use the evaluation board to quickly prototype a new design with a PCIe interface.

To evaluate the feature set of the Tsi382, IDT also offers an easy-to-use Microsoft Windows based tool called "TsiView." This tool provides read and write access to an IDT "Tsi" PCIe device's register settings. In addition, it can be used to program an on-board, serial EEPROM device with register settings that have been optimized by TsiView.

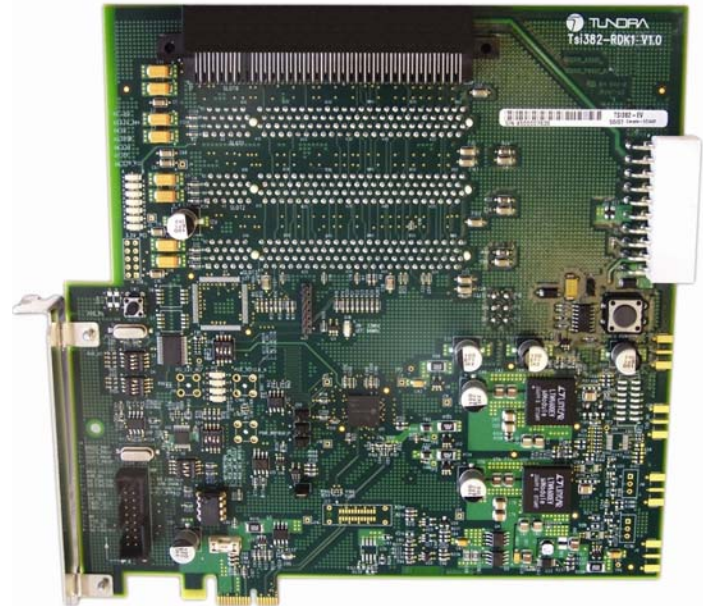


Figure 1 Tsi382 Evaluation Board

Tsi382 Overview

The Tsi382 is a high performance bridge that connects a single lane PCIe interface to the PCI bus 3.0 standard.

The device's PCIe Interface is compliant with the *PCI Express Specification (Revision 1.1)*. Its 32-bit PCI Interface can operate up to 66 MHz in PCI mode, and offer designers extensive flexibility by supporting three types of addressing modes: transparent, opaque, and non-transparent.

Tsi382 Key Features

General

- PCI Express to PCI bridge
- Fully compliant with *PCI Express Specification (Revision 1.1)*
- Transparent, Non-transparent and Opaque modes
- Efficient queuing and buffering for low latency and high throughput

PCIe

- x1 lane PCIe Interface
- Advanced error reporting capability
- End-to-end CRC check and generation
- Up to four outstanding memory reads

PCI

- 32/64-bit addressing and 32-bit data
- Operates at 25, 33, 50, and 66 MHz
- Up to eight outstanding memory reads
- Four external PCI masters supported through internal arbiter
- PCI clock outputs for up to four devices
- 3.3V PCI I/Os, 5V tolerant

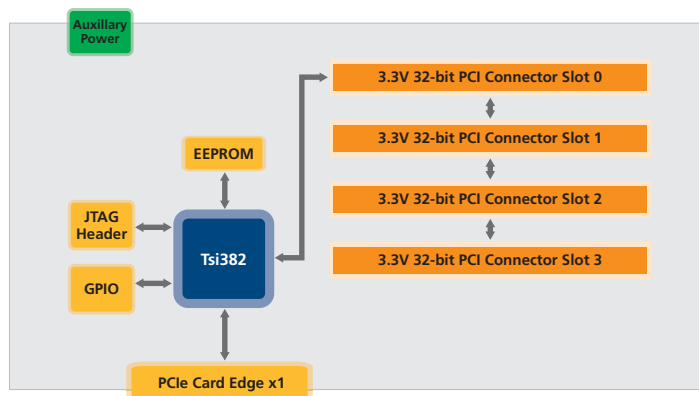


Figure 2 Tsi382 Evaluation Board – Block Diagram

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.