IDT™ 89EBPES8T5A Evaluation Board Manual

(Eval Board: 18-636-002)

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Introduction

In this manual, references to the PES8T5A also apply to the PES6T5 and PES5T5 unless otherwise indicated.

The 89HPES8T5A switch (also referred to as PES8T5A in this manual) is a member of IDT's PCI Express® standard (PCIe®) based line of products. It is an 8-lane, 5-port switch. One upstream port is provided for connecting to the root complex (RC), and up to four downstream ports are available for connecting to PCIe endpoints or to another switch. More information on this device can be found in the appropriate User Manual (89HPES8T5A, 89HPES6T5, or 89HPES5T5).

The 89EBPES8T5A Evaluation Board (also referred to as EB8T5A in this manual) provides an evaluation platform for the PES8T5A switch. It is also a cost effective way to add a PCIe downstream port (x1) to an existing system with a limited number of PCIe downstream ports. The EB8T5A eval board is designed to function as an add-on card to be plugged into a x4 PCIe slot available on a motherboard hosting an appropriate root complex, microprocessor(s), and four downstream ports. The EB8T5A is a vehicle to test and evaluate the functionality of the PES8T5A chip. Customers can use this board to get a headstart on software development prior to the arrival of their own hardware. The EB8T5A is also used by IDT to reproduce system-level hardware or software issues reported by customers. Figure 1.1 illustrates the functional block diagram representing the main parts of the EB8T5A board.

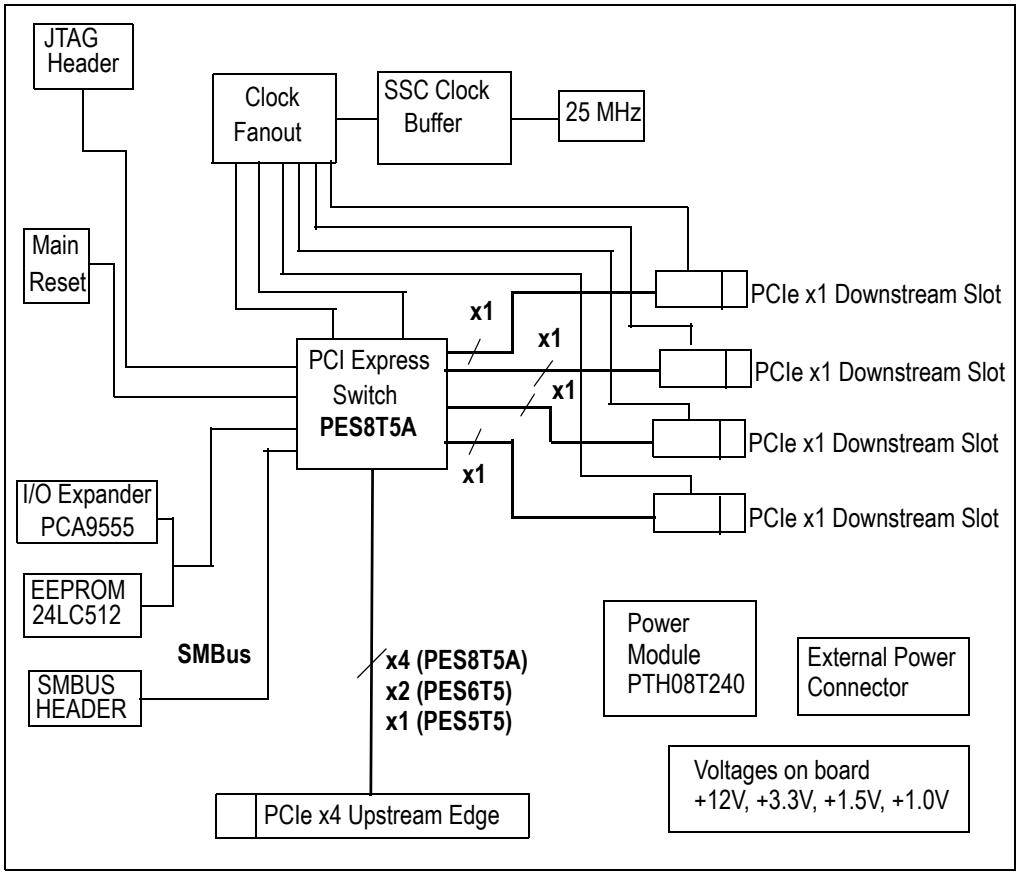


Figure 1.1 Function Block Diagram of the EB8T5A Eval Board

Notes

Board Features

Hardware

- **PCIe 5 port switch**
  - *PES8T5A — Five ports (one x4 port and four x1 ports), 8 PCIe lanes*
  - *PES6T5 — Five ports (one x2 port and four x1 ports), 6 PCIe lanes*
  - *PES5T5 — Five ports (five x1 ports), 5 PCIe lanes*
  - *PCIe Base Specification Revision 1.1 compliant*
  - *Integrates eight 2.5 Gbps embedded SerDes*
  - *Up to 256 byte maximum Payload Size*
  - *Automatic lane reversal and polarity inversion supported on all lanes*
  - *Automatic per port link width negotiation to x4, x2, x1*
  - *Load configuration from an optional serial EEPROM via SMBUS*
- **Upstream, Downstream Port**
  - *One edge connector on the upstream port, to be plugged into a slot with at least x4 capable mechanical slot connector on a host motherboard*
  - *Four slot connectors on the downstream ports, for PCIe endpoint add-on cards to be plugged in.*
- **Numerous user selectable configurations set using onboard jumpers and DIP-switches**
  - *Source of clock - host clock or onboard clock generator*
  - *Two clock rates and spread spectrum settings*
  - *Boot mode selection*
- **Vaux Support**
- **SMBUS Slave Interface (4 pin header)**
- **SMBUS Master Interface connected to the Serial EEPROMs through I/O expander**
- **“Attention” button for each downstream port to initiate a hot swap event on each port**
- **Four pin connector for optional external power supply**
- **Push button for Warm Reset**
- **Several LEDs to display status, reset, power, “Attention”, etc.**
- **One 14-pin JTAG header**

Software

There is no software or firmware executed on the board. However, useful software is provided along with the Evaluation Board to facilitate configuration and evaluation of the PES8T5A within host systems running popular operating systems.

- **Installation programs**
  - *Operating Systems Supported: Windows2000, WindowsXP, Linux*
- **GUI based application for Windows and Linux**
  - *Allows users to view and modify registers in the PES8T5A*
  - *Binary file generator for programming the serial EEPROMs attached to the SMBUS.*

Other

- A metal bracket is required to firmly hold in place the four endpoints plugged into the EB8T5A board.
- An external power supply may be required under some conditions.
- SMBUS cable may be required for certain evaluation exercises.
- SMA connectors are provided on the EB8T5A board for specific test points.

Notes

Revision History

September 10, 2007: Initial publication of board manual.

July 23, 2009: Added PES6T5 and PES5T5 devices to eval board manual. Updated Power Sources section, Table 2.15, and Schematics. Added Note after Table 2.17.

Notes

Installation of the EB8T5A Eval Board

Notes

EB8T5A Installation

This chapter discusses the steps required to configure and install the EB8T5A evaluation board. All available DIP switches and jumper configurations are explained in detail.

The primary installation steps are:

1. Configure jumper/switch options suitable for the evaluation or application requirements.
2. Connect PCI Express endpoint cards to the downstream port PCIe slots on the evaluation board.
3. Insert the evaluation board into the host system (motherboard with root complex chipset).
4. Apply power to the host system.

The EB8T5A board is shipped with all jumpers and switches configured to their default settings. In most cases, the board does not require further modification or setup.

Hardware Description

The PES8T5 is an 8-lane, 5-port PCI Express® switch. It is a peripheral chip that performs PCI Express based switching with a feature set optimized for high performance applications such as servers and storage. It provides fan-out and switching functions between a PCI Express upstream port and 4 downstream ports or peer-to-peer switching between downstream ports.

The EB8T5A has four PCI Express downstream ports, accessible through four x4 open-ended connectors.

Basic requirements for the board to run are:

- *Host system with a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot.*
- *PCI Express Endpoint Cards capable of training x1 link.*

Host System

The evaluation board cannot be operated as a standalone unit. A host system implementing a PCI Express root complex supporting x4 configuration through a PCI Express x4 slot is required to take full advantage of the PES8T5's capabilities.

Reference Clocks

The PES8T5A requires a differential reference clock. The EB8T5A derives this clock from a common source which is user-selectable. The common source can be either the host system's reference clock or the onboard clock generator. Selection is made by resistor switch described in Table 2.1.

Clock Configuration Switch - S3[3]	
S3[3]	**Clock Source**
ON	Onboard Reference Clock – Use onboard clock generator
OFF	Upstream Reference Clock – Host system provides clock **(Default)**

Table 2.1 Clock Source Selection

Notes

The source for the onboard clock is the ICS9FG104 clock generator device (U8) connected to a 25MHz oscillator (Y1). When using the onboard clock generator, the EB8T5A allows selection between multiple clock rates and spread spectrum settings via DIP switches as described in Tables 2.2 and 2.3 respectively. Spread Spectrum technology reduces peak EMI emissions by modulating the frequency to spread the peak energy over a wider bandwidth.

Clock Frequency Switch - S3[1]	
S3[1]	**Clock Frequency**
OFF	125MHz
ON	100MHz (Default)

Table 2.2 Clock Frequency Selection

Clock Spread Spectrum Switch - S3[2]	
S3[2]	**Spread Spectrum**
OFF	Enable Spread Spectrum
ON	Disable Spread Spectrum (Default)

Table 2.3 Spread Spectrum Clock Selection

If the Clock Spread Spectrum is used to modulate data rate, then both ports must use same modulated clock source. Therefore, if your system uses SSC, the on-board clock generator must be disabled and the upstream reference clock should be used instead.

The output of the onboard clock generator is accessible through two SMA connectors located on the Evaluation Board. See Table 2.4. This can be used to connect a scope for probing or capturing purposes and cannot be used to drive the clock from an external source.

Onboard Reference Clock Output (Differential) – J18, J19	
J19	Positive Reference Clock
J18	Negative Reference Clock

Table 2.4 SMA Connectors - Onboard Reference Clock

Figure 2.1 illustrates the clock distribution block diagram for the EB8T5A evaluation board.

Notes

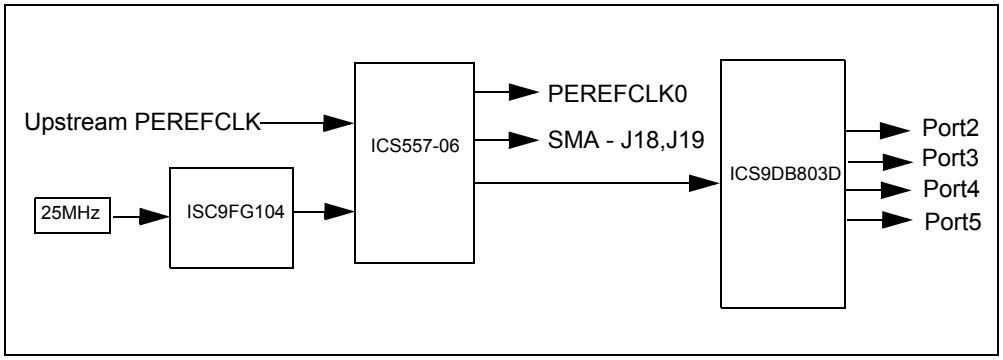


Figure 2.1 Clock Distribution Block Diagram

Power Sources

Power for the EB8T5A is generated from the 12.0V PCI Express upstream slot power or optionally from 3.3Vaux. A 12.0V to 3.3V DC-DC converter will be used to provide power to four DC-DC converters to generate VDDcore, VDDpe, VDDpea, and VTT voltages. The 3.3V from the 12.0V converter is used to power VDDio. When in power down mode the DC-DC converters is powered directly from 3.3Vaux through a MOSFET switch.

If add-in cards require more power than the upstream slot can support, an external source is required to supply this extra power via an auxiliary 4-pin power connector on the board. Header W1, W5, and W11 (see Table 2.15) are used to select the proper power source for the switch and all downstream ports.

External Power Source

If necessary, external power is supplied to the EB8T5A board through a 4-pin auxiliary power connector attached to J4. The external power supply provides +12V to the EB8T5A as described in Table 2.5. The +5V is unused.

Pin	Signal
1	+12V
2	GND
3	GND
4	+5V

Table 2.5 External Power Connector - J4

Notes

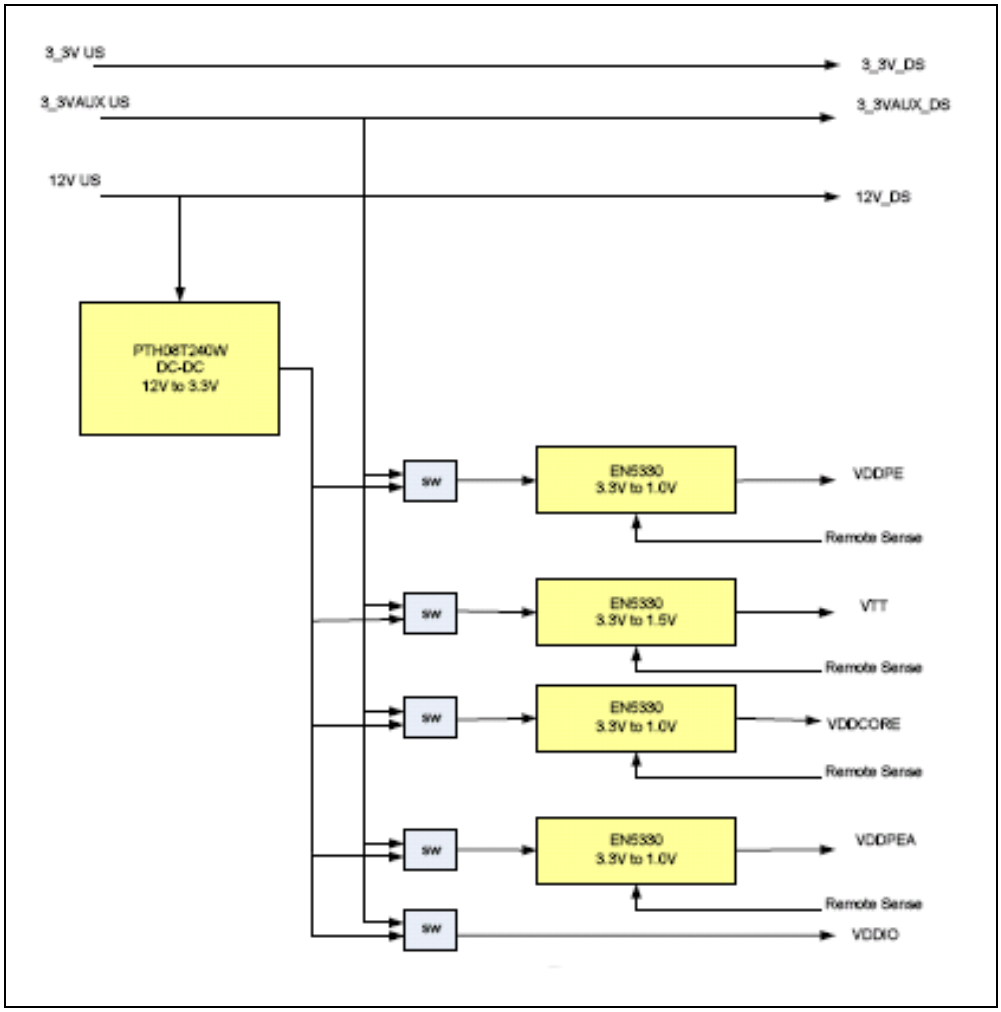


Figure 2.2 Power Distribution Block Diagram

Vaux Support

Power supply support will be provided to EB8T5A from 12.0V upstream power to 3.3Vaux upstream power when in sleep mode. The WAKE# signal direction, both an input and output will be supported by jumper selection. The APWRDIS# signal for auxiliary power disable requires the following timing on power-up.

Notes

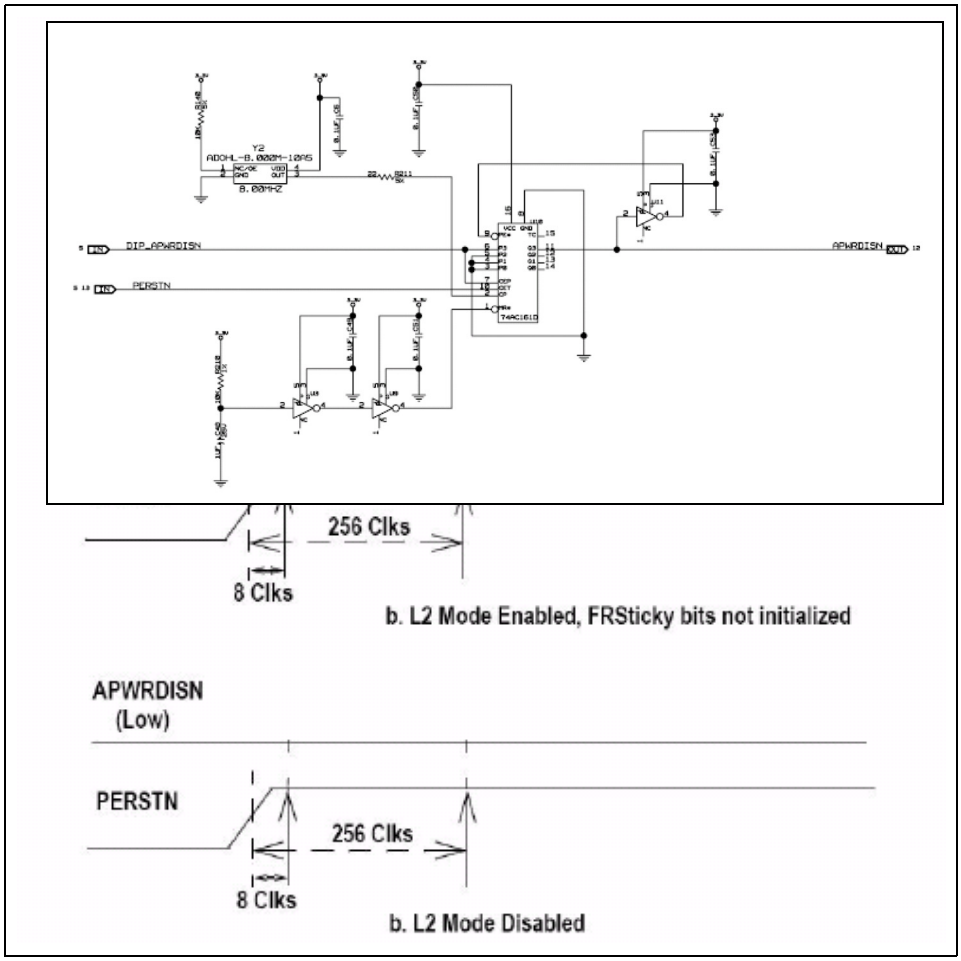


Figure 2.3 APWRDIS# Timing

On initial power up APWRDIS# must be held low initially for 8 clocks after PERST# is removed. Then it must be sampled high 256 clocks after PERSTN# is removed to enable L2 mode. Subsequent PERST# will not affect the APWRDIS# state. This timing will be provided by the following circuit.

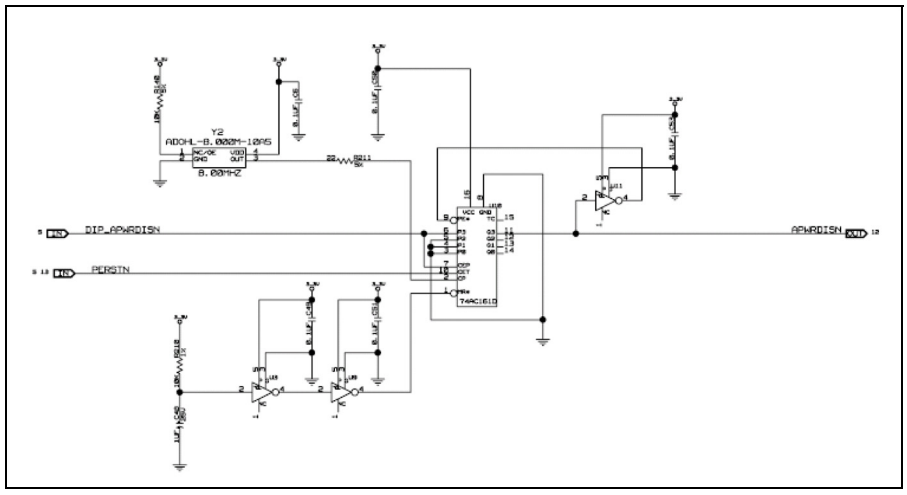


Figure 2.4 APWRDIS# Timing Circuit

Notes

PCI Express Serial Data Transmit Termination Voltage Converter

A DC-DC converter (U6) provides a 1.5V PCI Express serial data transmit termination voltage (shown as VTTPE or VPETVTT) to the PES8T5A.

PCI Express Digital Power Voltage Converter

A separate DC-DC converter (U16) provides a 1.0V PCI Express digital power voltage (VDDPE) to the PES8T5A.

PCI Express Analog Power Voltage Converter

A separate DC-DC converter (U7) provides a 1.0V PCI Express analog power voltage (shown as VDDAPE or VDDPEA) to the PES8T5A.

Core Logic Voltage Converter

A separate DC-DC converter (U1) provides the 1.0V core voltage (VDDCORE) to the PES8T5A.

3.3V I/O Power Module

A 12V to 3.3V power module (U5) provides the 3.3V I/O voltage (VDDIO) to the PES8T5A.

Power-up Sequence

The power-up sequence must be as following:

1. VDDIO - 3.3V
2. VDDCORE, VDDAPE, VDDPE - 1.0V
3. VTTPE - 1.5V

When powering up, each voltage level must ramp up and stabilize prior to applying the next voltage in the sequence to ensure internal latch-up issues are avoided. There are no maximum time limitations between sequential valid power level requirements. To insure that the sequencing requirements are met, a 0.047µF is used at the SOFTSTART cap on the VTTPE's voltage converter (U6 pin 36) in the EB8T5A.

Required Jumpers

To deliver power to the PES8T5A switch, the following jumpers must be shunted: W4, W10, W23, W24, and W25. These jumpers were implemented so that the power consumption of the PES8T5A can be measured.

Reset

The PES8T5A supports two types of reset mechanisms as described in the PCI Express specification:

- *Fundamental Reset: This is a system-generated reset that propagates along the PCI Express tree through a single side-band signal PERST# which is connected to the Root Complex, the PES8T5A, and the endpoints.*
- *Hot Reset: This is an In-band Reset, communicated downstream via a link from one device to another. Hot Reset may be initiated by software. This is further discussed in the 89HPES8T5A User Manual. The EB8T5A evaluation board provides seamless support for Hot Reset.*

Fundamental Reset

There are two types of Fundamental Resets which may occur on the EB8T5A evaluation board:

- *Cold Reset: During initial power-on, the onboard voltage monitor (TLC7733D) will assert the PCI Express Reset (PERSTN) input pin of the PES8T5A.*
- *Warm Reset: This is triggered by hardware while the device is powered on. Warm Reset can be initiated by two methods:*
  - *Pressing a push-button switch (S1) located on EB8T5A board*

Notes

- *The host system board IO Controller Hub asserting PERST# signal, which propagates through the PCIe upstream edge connector of the EB8T5A. Note that one can bypass the onboard voltage monitor (TLC7733D) by moving the shunt from pin 1-2 to pin 2-3 (default) on W2.*

Both events cause the onboard voltage monitor (TLC7733D) to assert the PCI Express Reset (PERSTN) input of the PES8T5A while power is on.

Downstream Reset

The PES8T5A provides a a choice of either a software-controlled reset for each downstream port through GPIO pins or a fundamental reset through PERST#. Selection is made by jumpers described in Table 2.6.

Port #	Jumper	Selection
5	W8	[1-2] Software controlled reset through GPIO10 [2-3] Fundamental reset PERST# (default)
4	W9	[1-2] Software controlled reset through GPIO1 [2-3] Fundamental reset PERST# (default)
3	W6	[1-2] Software controlled reset through GPIO9 [2-3] Fundamental reset PERST# (default)
2	W7	[1-2] Software controlled reset through GPIO0 [2-3] Fundamental reset PERST# (default)

Table 2.6 Downstream Reset Selection

Boot Configuration Vector

A boot configuration vector consisting of the signals listed in Table 2.7 is sampled by the PES8T5A during a fundamental reset (while PERSTN is active). The boot configuration vector defines the essential parameters for switch operation and is set using DIP switches S3, S4, and S5 as defined in Table 2.8.

Signal	Description
CCLKDS	**Common Clock Downstream.** When the CCLKDS pin is asserted, it indicates that a common clock is being used between the downstream device and the downstream port. **Default: 0x1**
CCLKUS	**Common Clock Upstream.** When the CCLKUS pin is asserted, it indicates that a common clock is being used between the upstream device and the upstream port. **Default: 0x1**
MSMBSMODE	**Master SMBus Slow Mode.** The assertion of this pin indicates that the master SMBus should operate at 100 KHz instead of 400 kHz. **Default: 0x0**
RSTHALT	**Reset Halt.** When this signal is asserted during a PCI Express fundamental reset, the PES8T5A executes the reset procedure and remains in a reset state with the Master and Slave SMBuses active. This allows software to read and write registers internal to the device before normal device operation begins. The device exits the reset state when the RSTHALT bit is cleared in the P0_SWCTL register through the SMBus. The value may be overridden by modifying the RSTHALT bit in the P0_SWCTL register. **Default: 0x0**

Table 2.7 Boot Configuration Vector Signals (Part 1 of 2)

Notes

Signal	Description
SWMODE[2:0]	**Switch Mode.** These configuration pins determine the PES8T5A switch operating mode. **Default: 0x0** 0x0 - Normal switch mode 0x1 - Normal switch mode with Serial EEPROM-based initialization 0x2 through 0x8 - Reserved
REFCLKM	**PCI Express Reference Clock Mode Select**. This signal selects the frequency of the reference clock input. **Default: 0x0** 0x0 - 100 MHz 0x1 - 125 MHz
MSMBADDR[2:0]	**Master SMBus Address.** These pins determine the SMBus address of the serial EEPROM from which configuration information is loaded. **Default: 0x0**
APWRDIS#	**Auxiliary Power Disable.** When this pin is active, it disables the device from using auxiliary power supply. **Default: 0x0**

Table 2.7 Boot Configuration Vector Signals (Part 2 of 2)

Signal	Description	Default
S3[4]	CCLKDS	OFF
S3[5]	CCLKUS	OFF
S3[6]	MSMBSMODE	ON
S5[6]	RSTHALT	ON
S5[1]	SWMODE[0]	ON
S5[2]	SWMODE[1]	ON
S5[3]	SWMODE[2]	ON
S5[5]	APWRDIS#	ON
S4[5]	MSMBADDR[1]	ON
S4[6]	MSMBADDR[2]	ON
S4[7]	MSMBADDR[3]	ON
S4[8]	MSMBADDR[4]	ON

Table 2.8 Boot Configuration Vector Switches S3, S4, and S5 (ON=0, OFF=1)

SMBus Interfaces

The System Management Bus (SMBus) is a two-wire interface through which various system component chips can communicate. It is based on the principles of operation of I^2C. Implementation of the SMBus signals in the PCI Express connector is optional and may not be present on the host system. The SMBus interface consist of an SMBus clock pin, an SMBus data pin, and 4 SMBus address pins.

The PES8T5A contains two SMBus interfaces: a slave SMBus interface and a master SMBus interface. The slave SMBus interface allows a SMBus Master device (such as the Intel E7520) full access to all software-visible registers. The Master SMBus interface provides connection to the external serial EEPROMs used for initialization and the I/O expander used for hot-plug signals.

SMBus Slave Interface

On the PES8T5A board, the slave SMBus interface is accessible through the PCI Express edge connector as well as a 4-pin header as described in Table 2.9.

Notes

Slave SMBus Interface Connector J21	
Pin	**Signal**
1	N/C
2	SCL
3	GND
4	SDA

Table 2.9 Slave SMBus Interface Connector

A fixed slave SMBus address specified by the SSMBADDR[5,3:1] pins is used.

For a fixed address, the SMBus address of the PES8T5A slave interface is **0b1110111** by default and is configurable using DIP switch S4 as described in Tables 2.10 and 2.11.

Slave Interface Address Configuration	
Address Bit	**Signal**
1	SSMBUSADDR[1]
2	SSMBUSADDR[2]
3	SSMBUSADDR[3]
4	0
5	SSMBUSADDR[5]
6	1
7	1

Table 2.10 SMBus Slave Interface Address Configuration

SMBUS Slave Interface Address Setting				
S4[4] SSMBADDR[5]	**S4[3] SSMBADDR[3]**	**S4[2] SSMBADDR[2]**	**S4[1] SSMBADDR[1]**	**Slave Interface Bus Address**
OFF	OFF	OFF	OFF	0b1110111 **(Default)**
OFF	OFF	OFF	ON	0b1110110
OFF	OFF	ON	OFF	0b1110101
OFF	OFF	ON	ON	0b1110100
OFF	ON	OFF	OFF	0b1110011
OFF	ON	OFF	ON	0b1110010
OFF	ON	ON	OFF	0b1110001
OFF	ON	ON	ON	0b1110000
ON	OFF	OFF	OFF	0b1100111
ON	OFF	OFF	ON	0b1100110

Table 2.11 PES8T5A SMBus Slave Interface Address Setting (Part 1 of 2)

Notes

SMBUS Slave Interface Address Setting				
S4[4] SSMBADDR[5]	S4[3] SSMBADDR[3]	S4[2] SSMBADDR[2]	S4[1] SSMBADDR[1]	Slave Interface Bus Address
ON	OFF	ON	OFF	0b1100101
ON	OFF	ON	ON	0b1100100
ON	ON	OFF	OFF	0b1100011
ON	ON	OFF	ON	0b1100010
ON	ON	ON	OFF	0b1100001
ON	ON	ON	ON	0b1100000

Table 2.11 PES8T5A SMBus Slave Interface Address Setting (Part 2 of 2)

The slave SMBus interface responds to the following SMBus transactions initiated by an SMBus master. Initiation of any SMBus transaction other than those listed above produces undefined results. See the SMBus 2.0 specification for a detailed description of the following transactions:

- *Byte and Word Write/Read*
- *Block Write/Read*

SMBus Master Interface

Connected to the master SMBus interface are four 16-bit I/O Expanders (PCA9555) and a serial EEPROM (24LC512). Four I/O Expanders are used as the interface for the onboard hot-plug controllers (MIC2591B).

The bus address for the selected EEPROM device is **0b1010000** by default and the lower four bits is configurable using switch S4 as described in Table 2.12.

S4[8]	S4[7]	S4[6]	S4[5]	Bus Address
OFF	OFF	OFF	OFF	0b1111
OFF	OFF	OFF	ON	0b1110
OFF	OFF	ON	OFF	0b1101
OFF	OFF	ON	ON	01100
OFF	ON	OFF	OFF	0b1011
OFF	ON	OFF	ON	0b1010
OFF	ON	ON	OFF	0b1001
OFF	ON	ON	ON	0b1000
ON	ON	ON	ON	0b0000 **(Default)**

Table 2.12 EEPROM SMBus Address Setting

JTAG Header

The PES8T5A provides a JTAG connector J4 for access to the PES8T5A JTAG interface. The connector is a 2.54 x 2.54 mm pitch male 10-pin connector. Refer to Table 2.12 for the JTAG Connector J2 pin out.

Notes

JTAG Connector J2					
Pin	**Signal**	**Direction**	**Pin**	**Signal**	**Direction**
1	/TRST - Test reset	Input	2	GND	—
3	TDI - Test data	Input	4	GND	—
5	TDO - Test data	Output	6	GND	—
7	TMS - Test mode select	Input	8	GND	—
9	TCK - Test clock	Input	10	GND	—

Table 2.13 JTAG Connector Pin Out

Attention Buttons

The PES8T5A features four attention buttons, shown in Table 2.13. Each button corresponds to a particular port and is used to initiate hot-swapping events.

Button	Description
SW4	Port 5 Attention Button
SW3	Port 4 Attention Button
SW2	Port 3 Attention Button
SW1	Port 2 Attention Button

Table 2.14 Attention Buttons

Miscellaneous Jumpers, Headers

Miscellaneous Jumpers, Headers			
Ref. Designator	**Type**	**Default**	**Description**
S2[1]	Switch	OFF	Port2: Manually-operated Retention Latch
S2[2]	Switch	OFF	Port3: Manually-operated Retention Latch
S2[3]	Switch	OFF	Port4: Manually-operated Retention Latch
S2[4]	Switch	OFF	Port5: Manually-operated Retention Latch
S6[4]	Switch	OFF	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Port 5 **(Default)**
S6[3]	Switch	OFF	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 4 **(Default)**
S6[2]	Switch	OFF	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 3 **(Default)**
S6[1]	Switch	OFF	Bypass hot-plug controller - Enables direct power (+12V and +3.3V) to Ports 2 **(Default)**

Table 2.15 Miscellaneous Jumpers, Headers (Part 1 of 2)

Notes

Miscellaneous Jumpers, Headers			
Ref. Designator	**Type**	**Default**	**Description**
W32	Header	2-3 Shunted	1-2: Port 2, +3.3V source base on hot-plug controller 2-3: Port 2, +3.3V source from upstream port power
W31	Header	2-3 Shunted	1-2: Port 2, +12V source base on hot-plug controller 2-3: Port 2, +12V source from upstream port power
W30	Header	2-3 Shunted	1-2: Port 2, +3.3Vaux source base on hot-plug controller 2-3: Port 2, +3.3Vaux source from upstream port power
W35	Header	2-3 Shunted	1-2: Port 3, +3.3V source base on hot-plug controller 2-3: Port 3, +3.3V source from upstream port power
W34	Header	2-3 Shunted	1-2: Port 3, +12V source base on hot-plug controller 2-3: Port 3, +12V source from upstream port power
W33	Header	2-3 Shunted	1-2: Port 3, +3.3Vaux source base on hot-plug controller 2-3: Port 3, +3.3Vaux source from upstream port power
W38	Header	2-3 Shunted	1-2: Port4, +3.3V source base on hot-plug controller 2-3: Port 4, +3.3V source from upstream port power
W37	Header	2-3 Shunted	1-2: Port 4, +12V source base on hot-plug controller 2-3: Port 4, +12V source from upstream port power
W36	Header	2-3 Shunted	1-2: Port 4, +3.3Vaux source base on hot-plug controller 2-3: Port 4, +3.3Vaux source from upstream port power
W50	Header	2-3 Shunted	1-2: Port 5, +3.3V source base on hot-plug controller 2-3: Port 5, +3.3V source from upstream port power
W40	Header	2-3 Shunted	1-2: Port 5, +12V source base on hot-plug controller 2-3: Port 5, +12V source from upstream port power
W39	Header	2-3 Shunted	1-2: Port 5, +3.3Vaux source base on hot-plug controller 2-3: Port 5, +3.3Vaux source from upstream port power
W15	Header	Open	1-2: Select WAKEN# as an input 2-3: Select WAKE# as in output
S2[6]	Switch	On	Power Good Enable Force On switch for ICS90DB803 clock output enable (OE2#)
S2[1]	Switch	On	Power Good Enable Force On switch for ICS90DB803 clock output enable (OE3#)
S6[6]	Switch	On	Power Good Enable Force On switch for ICS90DB803 clock output enable (OE4#)
S6[5]	Switch	On	Power Good Enable Force On switch for ICS90DB803 clock output enable (OE5#)
W1, W5, W11	Header	1-2 Shunted	1-2: +12V source from upstream port (Default) 2-3: +12V source from external power connect
W3	Header	Shunted	Disable EEPROM Write protect feature (Default)

Table 2.15 Miscellaneous Jumpers, Headers (Part 2 of 2)

LEDs

There are several LED indicators on the EB8T5A which convey status feedback. A description of each is provided in Table 2.15.

Notes

Location	Color	Definition
DS87	Green	Port 2: Power-is-good indicator
DS86	Green	Port 3: Power-is-good indicator
DS85	Green	Port 4: Power-is-good indicator
DS84	Green	Port 5: Power-is-good indicator
DS83	Amber	Port2: Attention Input indicator
DS82	Amber	Port3: Attention Input indicator
DS81	Amber	Port4: Attention Input indicator
DS80	Amber	Port5: Attention Input indicator
DS79	Green	Port2: Presence Detect indicator
DS78	Green	Port3: Presence Detect indicator
DS77	Green	Port4: Presence Detect indicator
DS76	Green	Port5: Presence Detect indicator
DS64	Amber	Port2: Attention Output indicator
DS63	Amber	Port3: Attention Output indicator
DS62	Amber	Port4: Attention Output indicator
DS61	Amber	Port5: Attention Output indicator
DS57	Green	Port 2: Power indicator
DS56	Green	Port 3: Power indicator
DS55	Green	Port 4: Power indicator
DS54	Green	Port 5: Power indicator
DS91	Red	Port 2: MRL indicator
DS90	Red	Port 3: MRL indicator
DS89	Red	Port 4: MRL indicator
DS88	Red	Port 5: MRL indicator
DS95	Red	Port 2: Power Fault indicator
DS94	Red	Port 3: Power Fault indicator
DS93	Red	Port 4: Power Fault indicator
DS92	Red	Port 5: Power Fault indicator
DS99	Green	Port 2: Link Up indicator
DS98	Green	Port 3: Link Up indicator
DS97	Green	Port 4: Link Up indicator
DS96	Green	Port 5: Link Up indicator
DS100	Green	Port 0: Link Up indicator
DS105	Amber	Port0: Link Activity indicator
DS104	Amber	Port2: Link Activity indicator

Table 2.16 LED Indicators (Part 1 of 2)

Notes

Location	Color	Definition
DS103	Amber	Port3: Link Activity indicator
DS102	Amber	Port4: Link Activity indicator
DS101	Amber	Port5: Link Activity indicator

Table 2.16 LED Indicators (Part 2 of 2)

PCI Express Connectors

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground
19	PETp1	Transmitter differential	RSVD	Reserved
20	PETn1	pair, Lane 1	GND	Ground
21	GND	Ground	PERp1	Receiver differential
22	GND	Ground	PERn1	pair, Lane 1
23	PETp2	Transmitter differential	GND	Ground
24	PETn2	pair, Lane 2	GND	Ground
25	GND	Ground	PERp2	Receiver differential
26	GND	Ground	PERn2	pair, Lane 2

Table 2.17 PCI Express x4 Connector Pinout (Part 1 of 2)

Notes

Pin	Side A		Side B	
27	PETp3	Transmitter differential	GND	Ground
28	PETn3	pair, Lane 3	GND	Ground
29	GND	Ground	PERp3	Receiver differential
30	RSVD	Reserved	PERn3	pair, Lane 3
31	PRSNT2#	Hot-Plug presence detect	GND	Ground
32	GND	Ground	RSVD	Reserved

Table 2.17 PCI Express x4 Connector Pinout (Part 2 of 2)

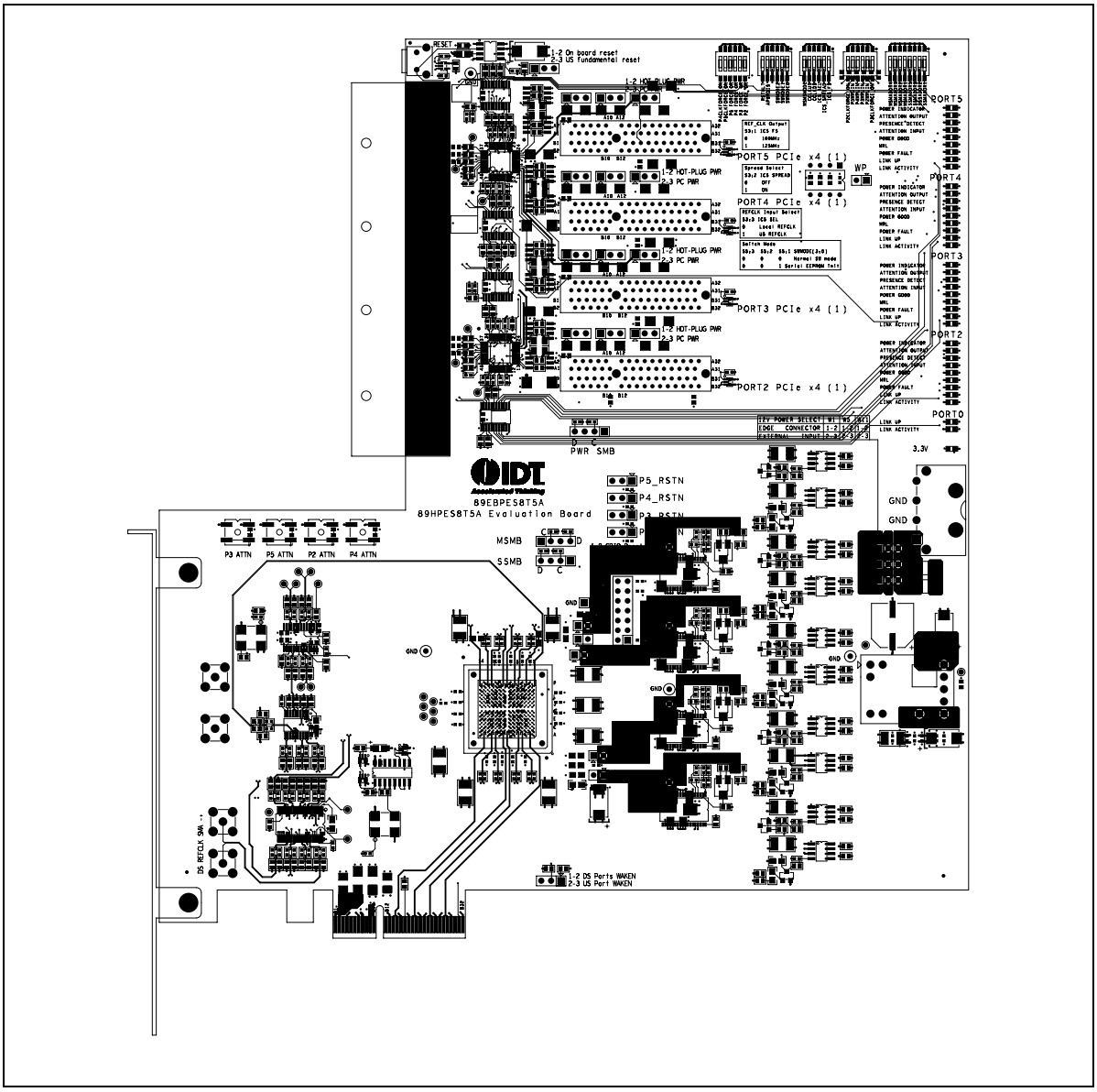
Note: R347 should be populated with a 0 ohm resistor (0402) for systems that require PRSNT2# for the x1 width to be connected.

Pin	Side A		Side B	
1	+12V	12V power	PRSNT1#	Hot-Plug presence detect
2	+12V	12V power	+12V	12V power
3	RSVD	Reserved	+12V	12V power
4	GND	Ground	GND	Ground
5	SMCLK	SMBus clock	JTAG2	TCK (Test Clock) JTAG i/f clk i/p
6	SMDAT	SMBus Data	JTAG	TDI (Test Data Input)
7	GND	Ground	JTAG	TDO (Test Data Output)
8	+3.3V	3.3V power	JTAG	TMS (Test Mode Select)
9	JTAG1	TRST# (Test/Reset) resets JTAG i/f	+3.3V	3.3V power
10	3.3Vaux	3.3V auxiliary power	+3.3V	3.3V power
11	WAKE#	Signal for Link reactivation	PERST#	Fundamental Reset
Mechanical Key				
12	RSVD	Reserved	GND	Ground
13	GND	Ground	REFCLK+	REFCLK Reference clock
14	PETp0	Transmitter differential	REFCLK-	(differential pair)
15	PETn0	pair, Lane 0	GND	Ground
16	GND	Ground	PERp0	Receiver differential
17	PRSNT2#	Hot-Plug presence detect	PERn0	pair, Lane 0
18	GND	Ground	GND	Ground

Table 2.18 PCI Express x1 Connector Pinout

Note: These x4 and x1 PCI Express connectors comply with the PCIe specification. The EB8T5A uses x1 (mechanically x4) connector on all downstream ports. According to the PCI Express specification, the PRSNT1# pin should be wired to the farthest available PRSNT2# pin on the connector. In the EB8T5A, all PRSNT2# pins are tied together. This allows the board to be installed in a x1 or a x4 slot. The open-ended x4 slot allows the insertion of physical lane width greater than x4 to be installed without the need of slot reducer.

EB8T5A Board Figure



Software for the EB8T5A Eval Board

Notes

Introduction

This chapter discusses some of the main features of the available software to give users a better understanding of what can be achieved with the EB8T5A evaluation board using the device management software.

Device management software and related user documentation are available on a CD which is included in the Evaluation Board Kit. This information is also available on IDT's FTP site. For more information, contact IDT at ssdhelp@idt.com.

Device Management Software

The primary use of the Device Management Software package is to enable users of the evaluation board to access all the registers in the PES8T5 device. This access can be achieved using the PCI Express in-band configuration cycles through the upstream port on the PES8T5.

This software also enables users to save a snapshot of the current register set into a dump file which can be used for debugging purposes. An export/import facility is also available to create and use "Configuration" files which can be used to initialize the switch device with specific values in specific registers.

A conversion utility is also provided to translate a configuration file into an EEPROM programmable data structure. This enables the user to program an appropriate serial EEPROM with desirable register settings for the PES8T5, and then to populate that EEPROM onto the Evaluation Board. It is also possible to program the EEPROM directly on the Evaluation Board using a feature provided by the software package.

The front end of the Device Management Software is a user-friendly Graphical User Interface which allows the user to quickly read or write the registers of interest. The GUI also permits the user to run the software in "simulation" mode with no real hardware attached, allowing the creation of configuration files for the PES8T5 in the absence of the actual device.

Much of the Device Management Software is written with device-independent and OS-independent code. The software will be guaranteed to work on Linux (/sys interface) and MS Windows XP. It may function flawlessly on various flavors of MS Windows, but may not be validated on all. The fact that the software is device-independent assures its scalability to future PCIe parts from IDT. Once users are familiar with the GUI, they will be able to use the same GUI on all PCIe parts from IDT. This software is customized for each device through an XML device description file which includes information on the number of ports, registers, types of registers, information on bit-fields within each register, etc.

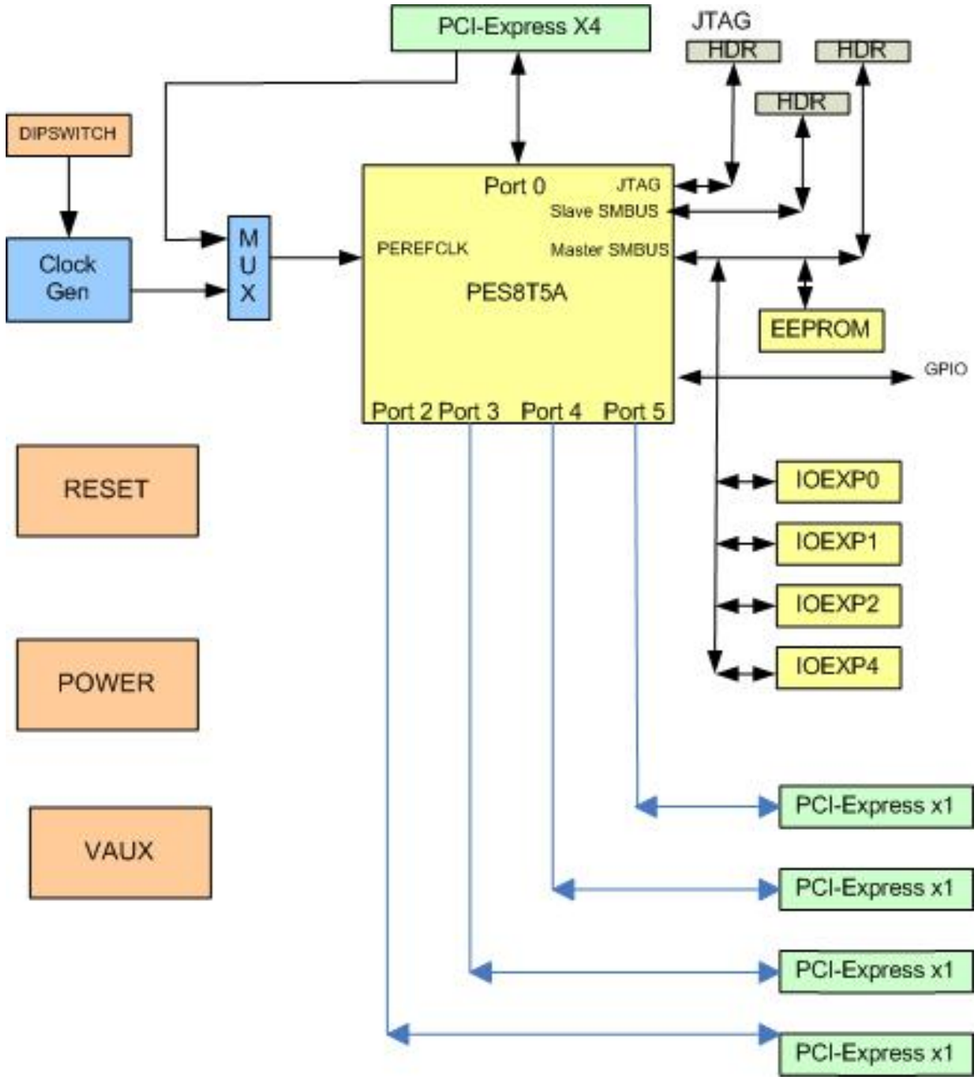
Notes

Schematics

Notes

Schematics

BLOCK DIAGRAM



REVISIONS

DCN	REV	DESCRIPTION	DATE	CHANGE BY
PCB-0161R01	1.0	INTIAL RELEASE	2008-04-14	T. TRAN

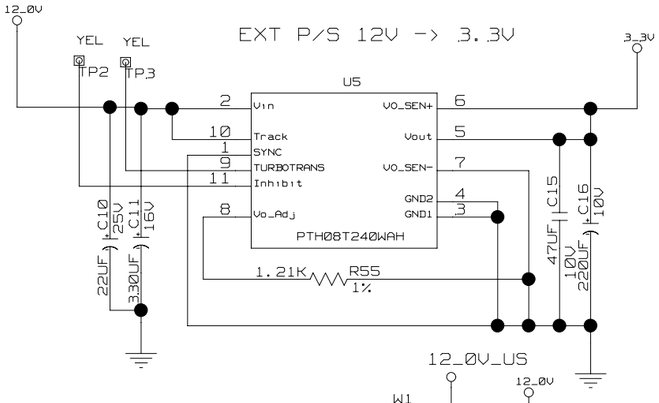
SHEET	DESCRIPTION
1	TABLE OF CONTENTS
2	POWER REGULATORS PES8T5A
3	POWER MOSFETS FOR 3.3VAUX
4	CLOCKS
5	RESET, SMBUS, JTAG, DIPSW
6	APWRDISN TIMING CIRCUIT
7	EPROM ATTN_SW WAKE
8	IO EXPANDERS
9	IO EXPANDER LEDS
10	HOT SWAP CONTROL PORT 2/4
11	HOT SWAP CONTROL PORT 3/5
12	PES8T5A - CLOCK, SMBUS, GPIO
13	PES8T5A - PORT 0
14	PES8T5A - DOWNSTREAM PORTS
15	DOWNSTREAM PORT 2/3 CONNECTORS
16	DOWNSTREAM PORT 4/5 CONNECTORS
17	PES8T5A - POWER

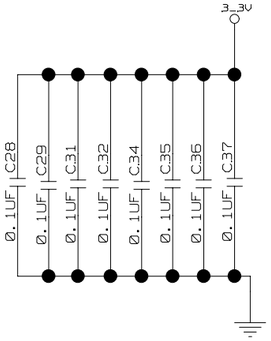
TITLE 89HPES8T5A EVALUATION BOARD
89EBPES8T5A

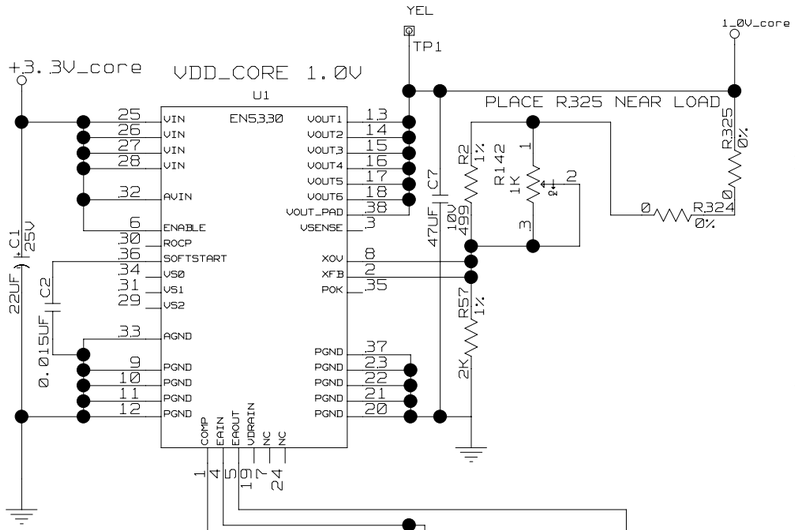
SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-6.36-002	1.0

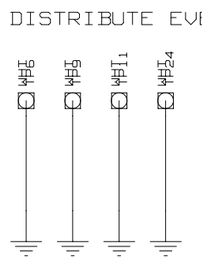
AUTHOR	CHECKED BY
T. Tran	D. Huang

Tue Apr 15 14:25:57 2008 | SHEET 1 OF 17



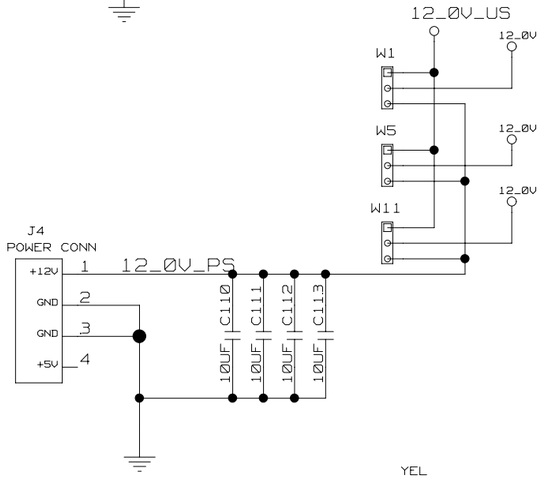


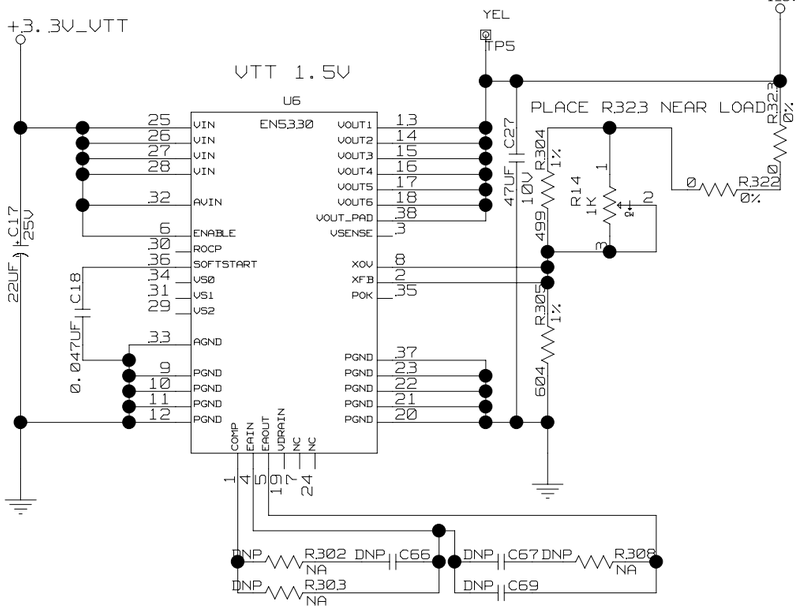


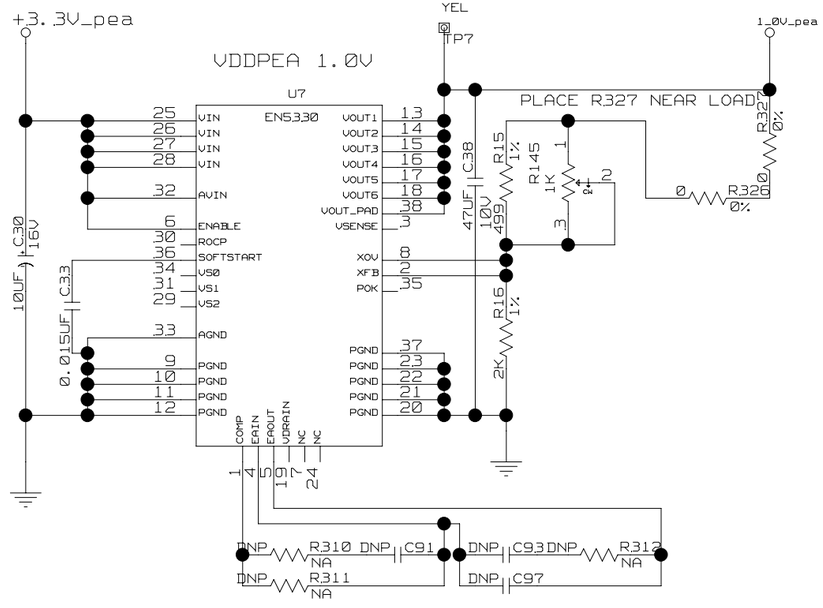


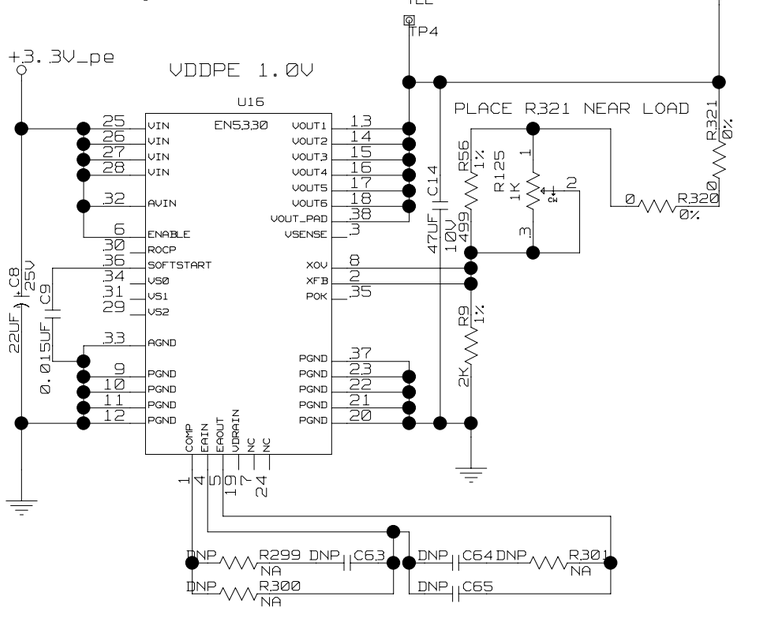
SILKSCREEN

12V POWER SELECT	W1	W5	W11
EDGE CONNECTOR	1-2	1-2	1-2
EXTERNAL INPUT	2-3	2-3	2-3









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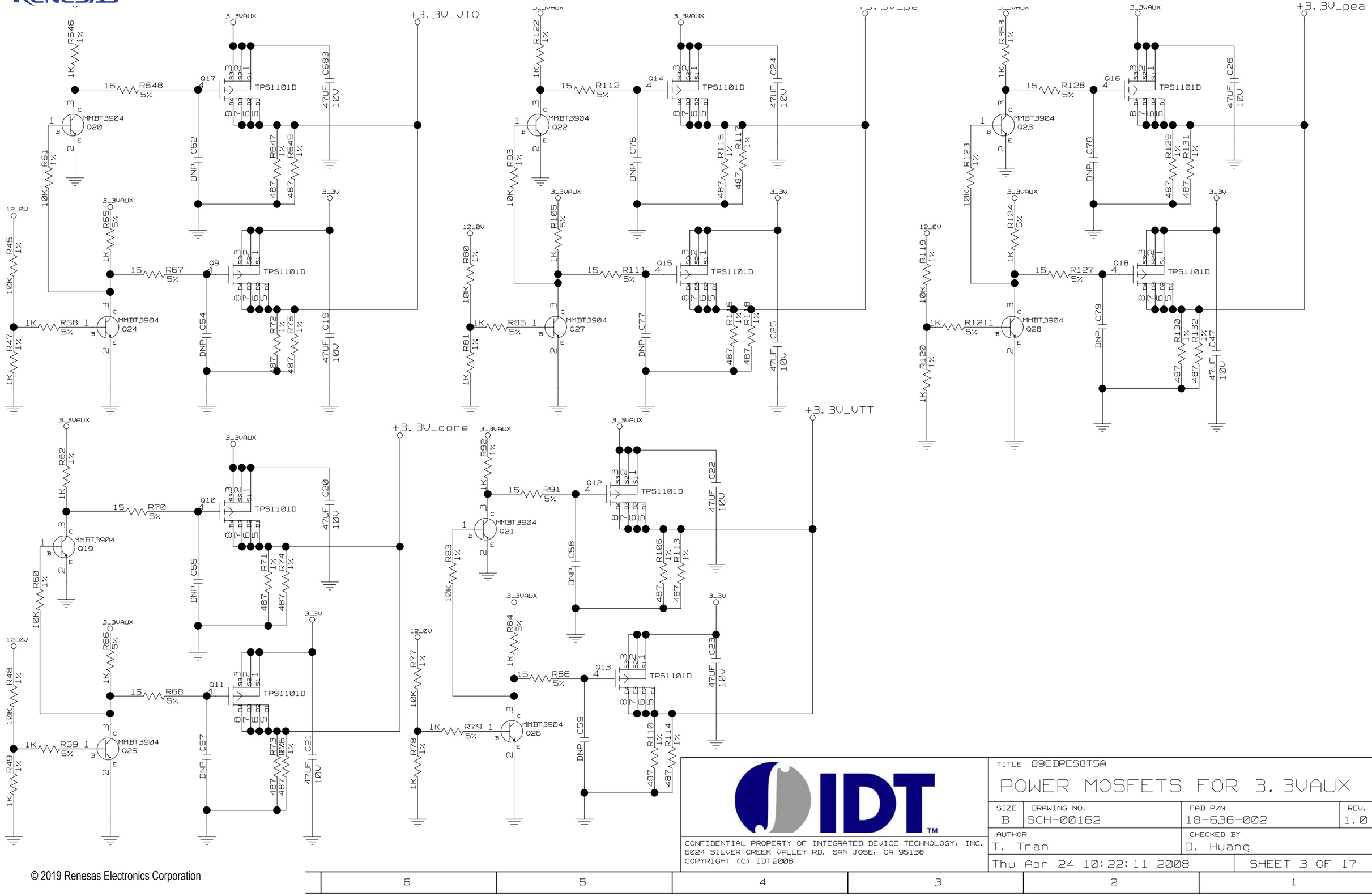
TITLE 89EBPES8T5A

POWER REGULATORS 8T5A

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Thu Apr 24 10:22:10 2008 — SHEET 2 OF 17



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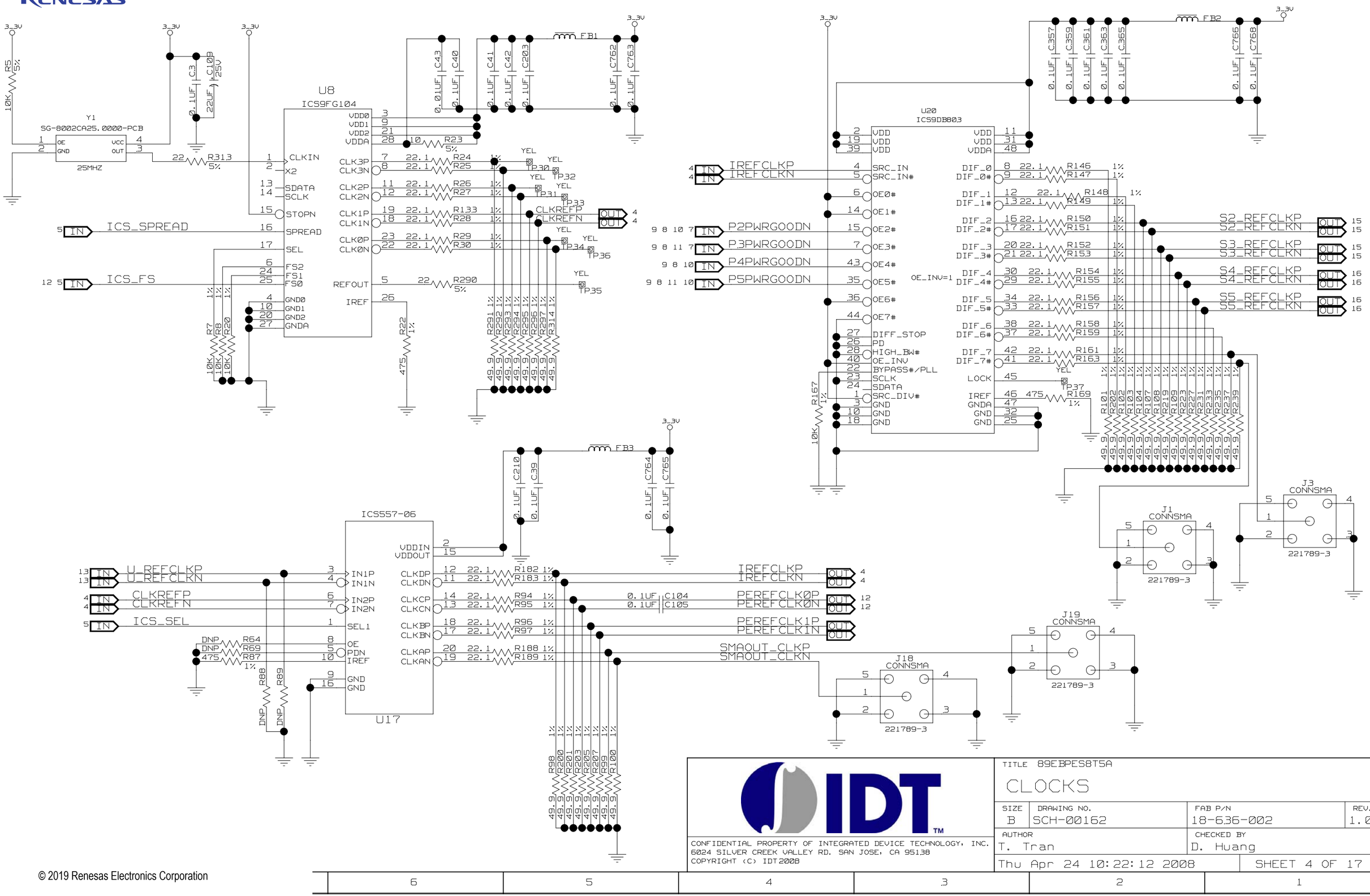
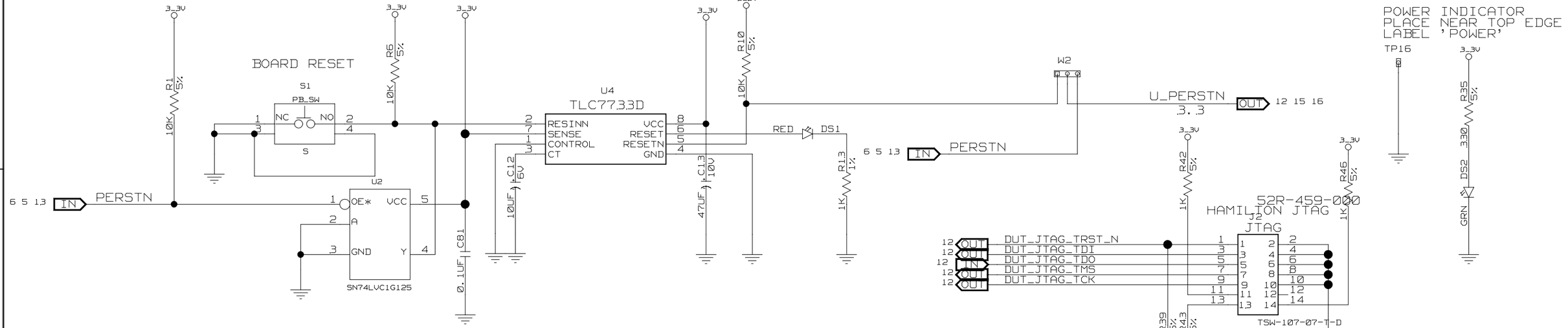
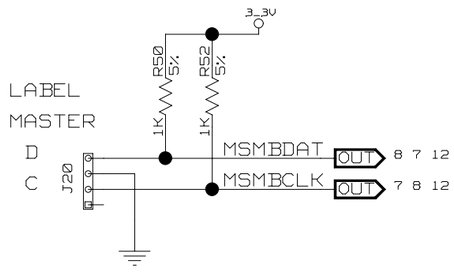
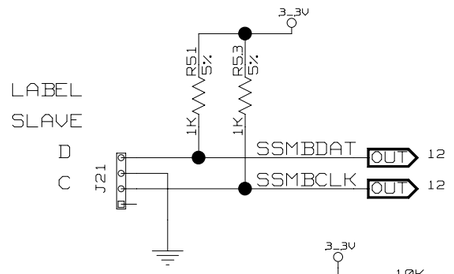
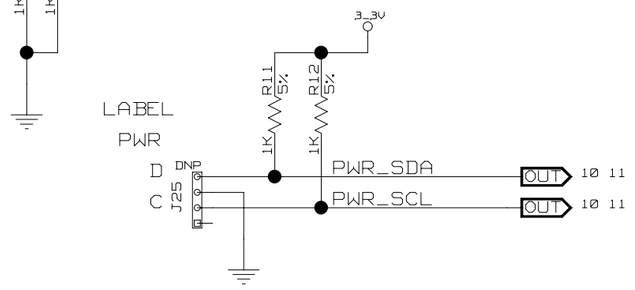
TITLE: 89EBPES8T5A POWER MOSFETS FOR 3.3VAUX			
SIZE: B	DRAWING NO.: SCH-00162	FAB P/N: 18-636-002	REV.: 1.0
AUTHOR: T. Tran		CHECKED BY: D. Huang	
Thu Apr 24 10:22:11 2008		SHEET 3 OF 17	

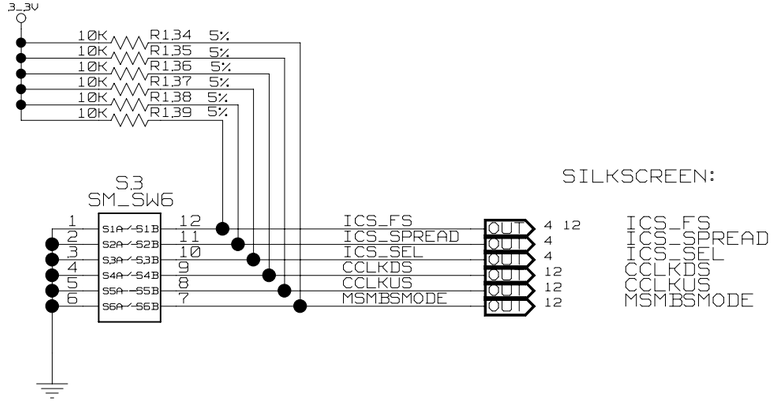


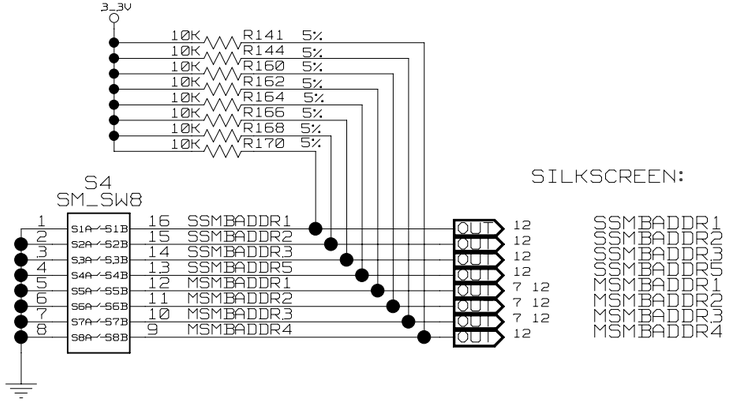


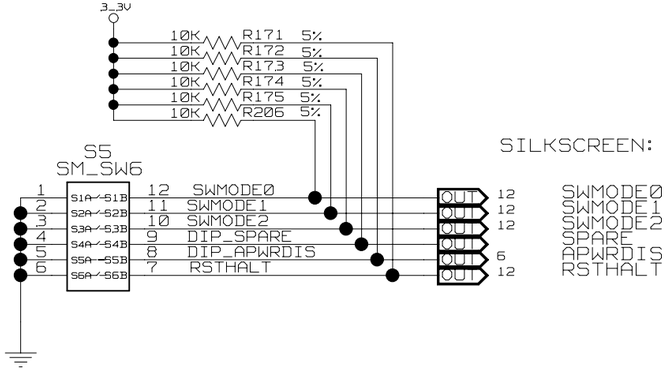












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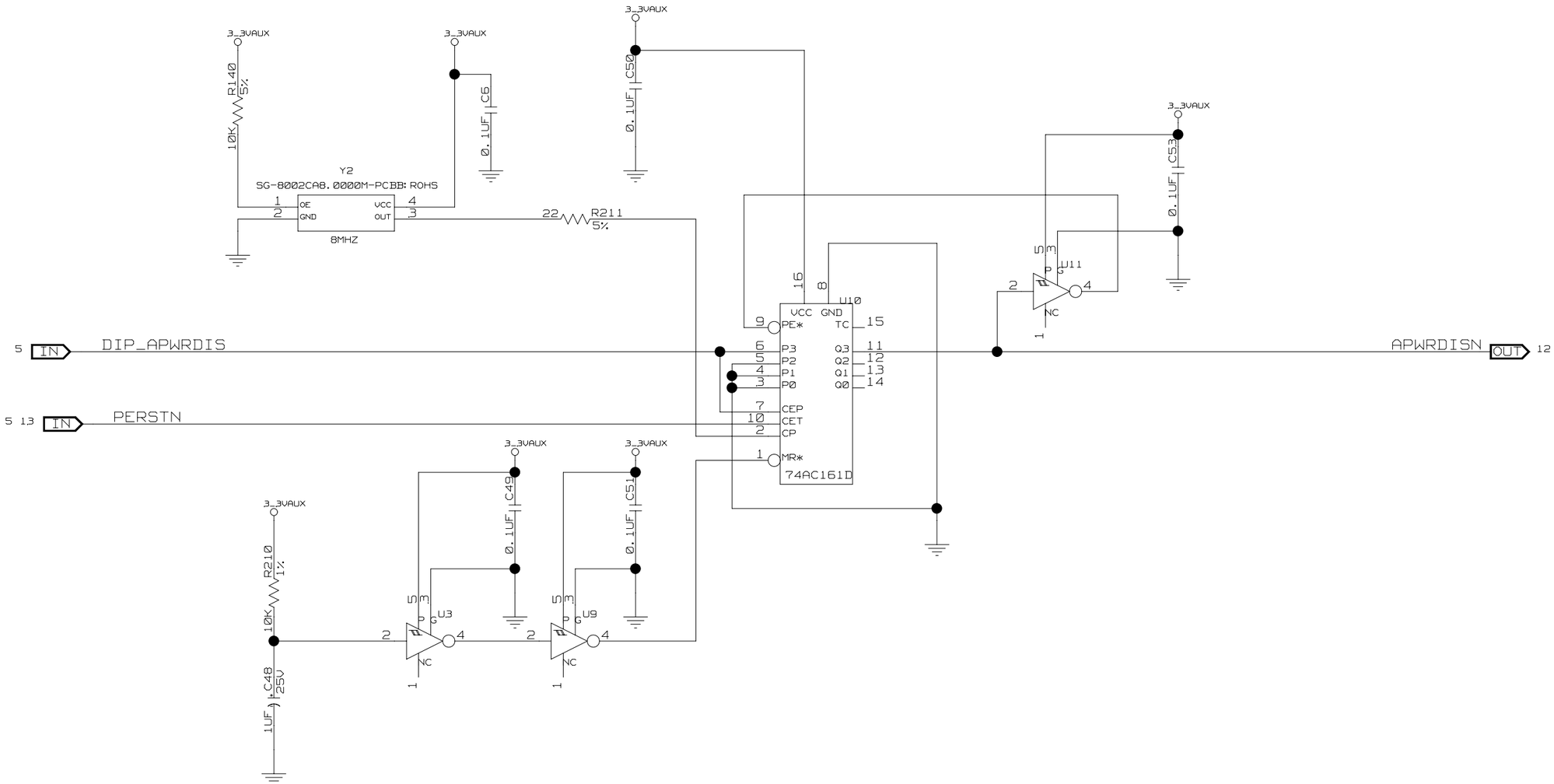
TITLE 89EBPES8T5A			
RESET, JTAG, SMBUS, DIPSW			
SIZE B	DRAWING NO. SCH-00162	FAB P/N 18-636-002	REV. 1.0
AUTHOR T. Tran		CHECKED BY D. Huang	
Thu Apr 24 10:22:13 2008		SHEET 5 OF 17	



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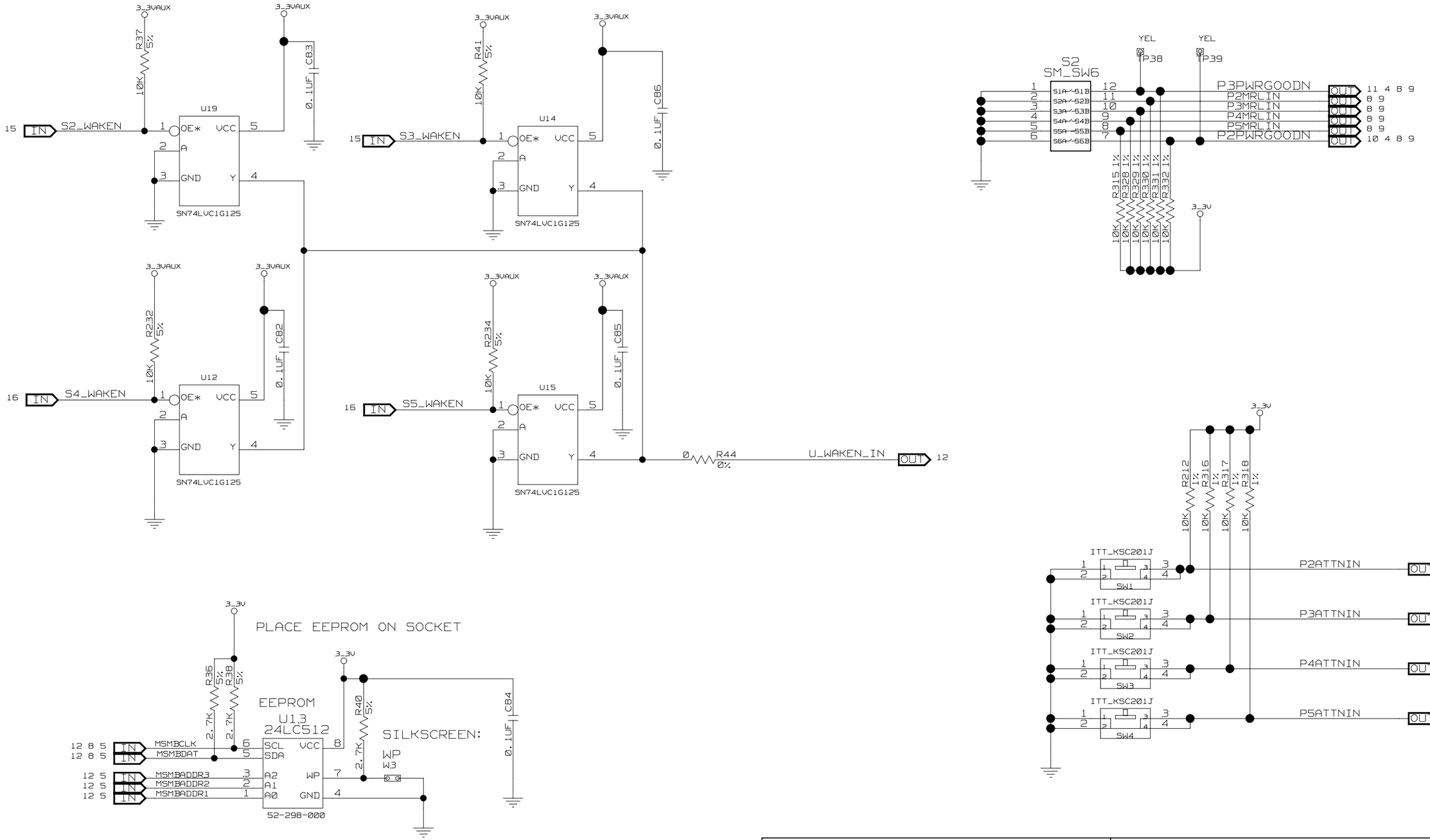
TITLE 89EBPES8T5A

APWRDISN TIMING CIRCUIT

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Thu Apr 24 10:22:13 2008 SHEET 6 OF 17



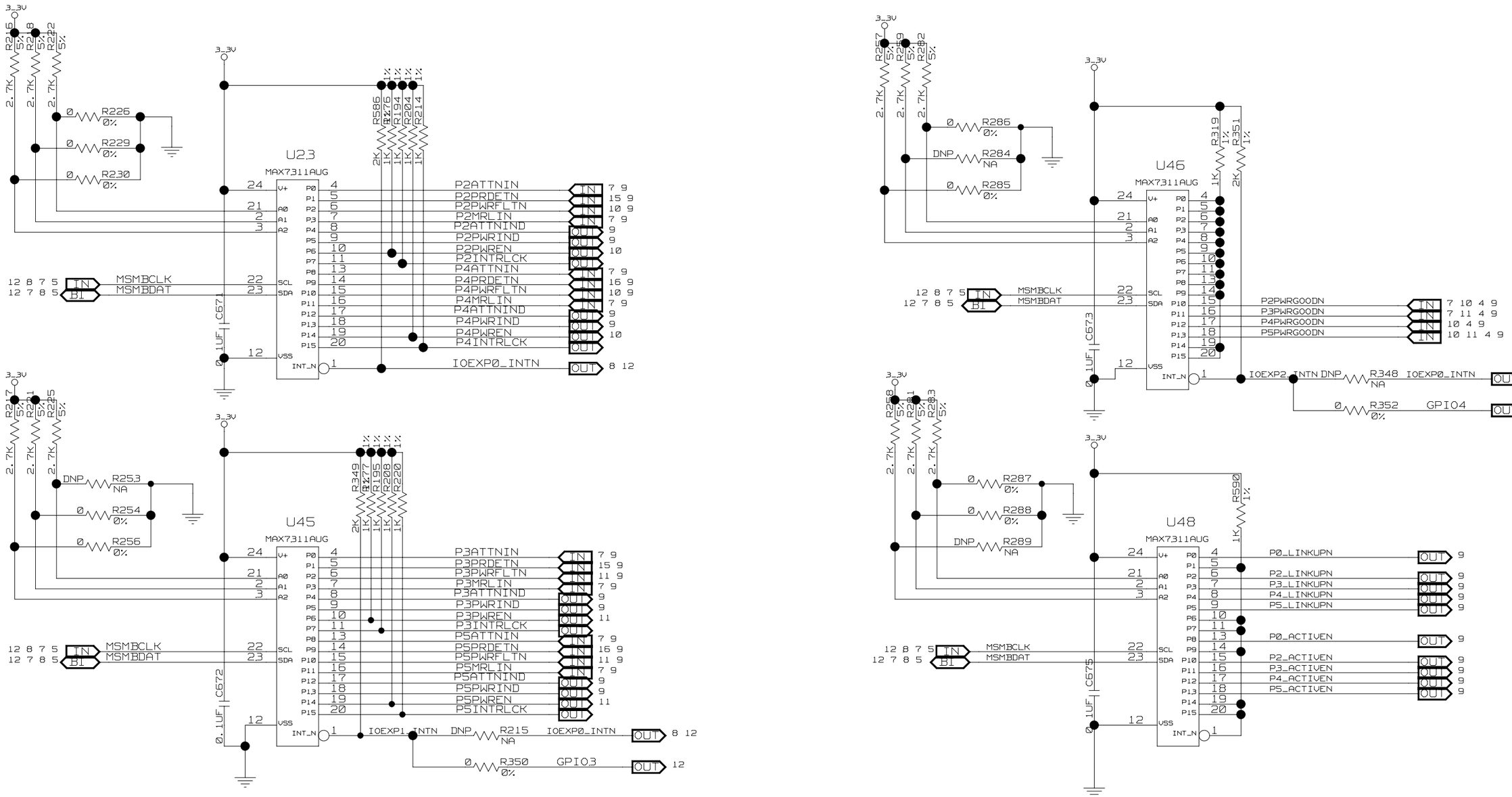
TITLE 89EBPES8T5A

EEPROM ATTN_SW WAKE MRL

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

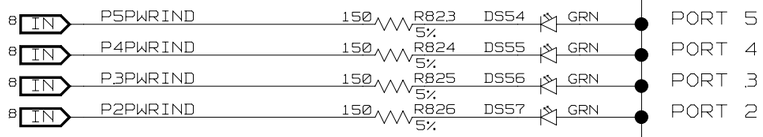
AUTHOR	CHECKED BY
T. Tran	D. Huang

Thu Apr 24 10:22:14 2008 — SHEET 7 OF 17

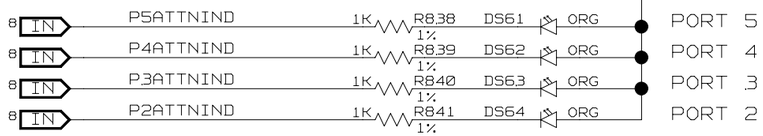


TITLE 89EBPES8T5A IO EXPANDERS			
SIZE B	DRAWING NO. SCH-00162	FAB P/N 18-636-002	REV. 1.0
AUTHOR T. Tran		CHECKED BY D. Huang	
Thu Apr 24 10:22:14 2008		SHEET 8 OF 17	

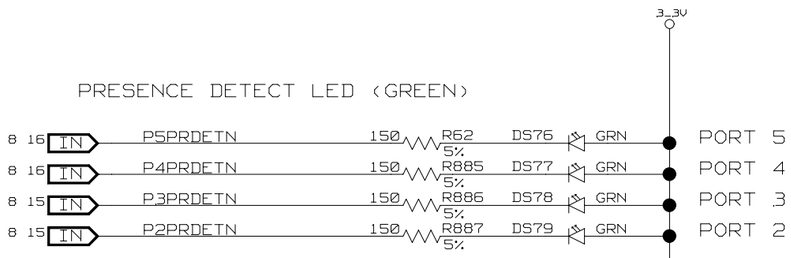
POWER INDICATOR LED (GREEN)



ATTENTION OUTPUT LED (AMBER)

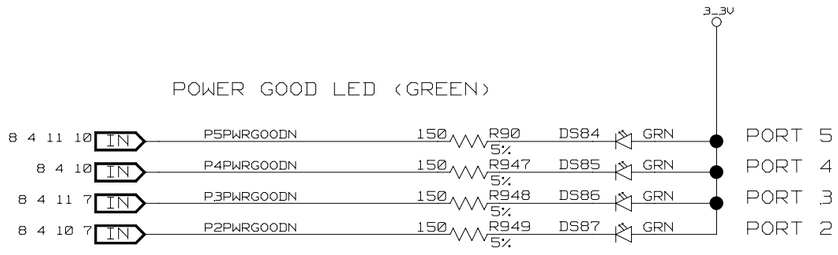


PRESENCE DETECT LED (GREEN)

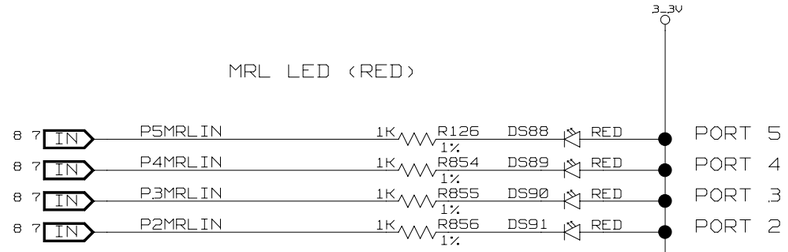


ATTENTION INPUT LED (AMBER)

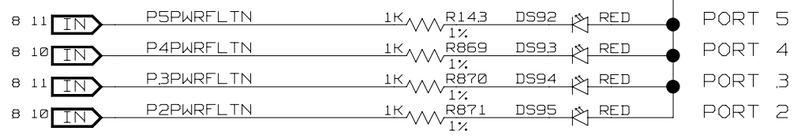
POWER GOOD LED (GREEN)



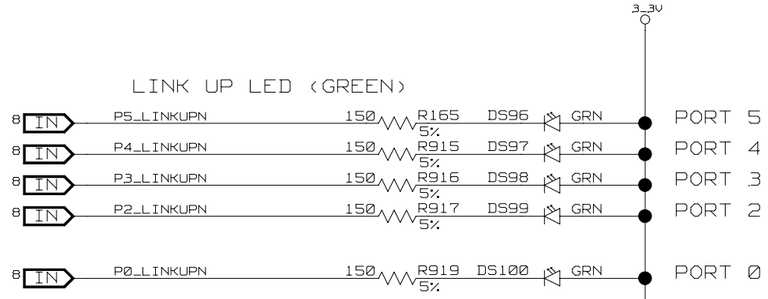
MRL LED (RED)



POWER FAULT LED (RED)



LINK UP LED (GREEN)



LINK ACTIVITY LED (AMBER)

TITLE 89EBPES8T5A

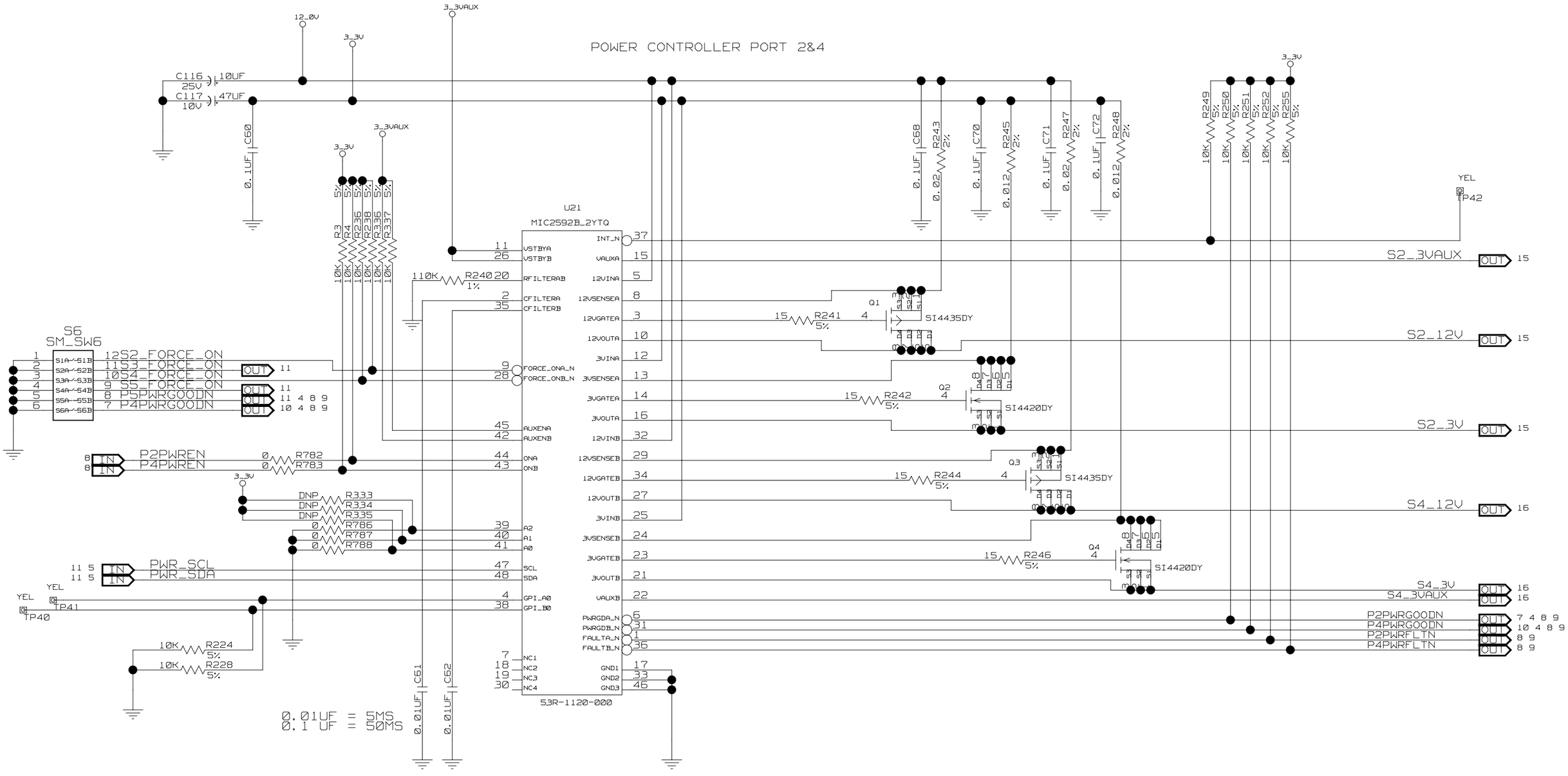
IO EXPANDER LEDS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Thu Apr 24 10:22:15 2008 SHEET 9 OF 17

POWER CONTROLLER PORT 2&4



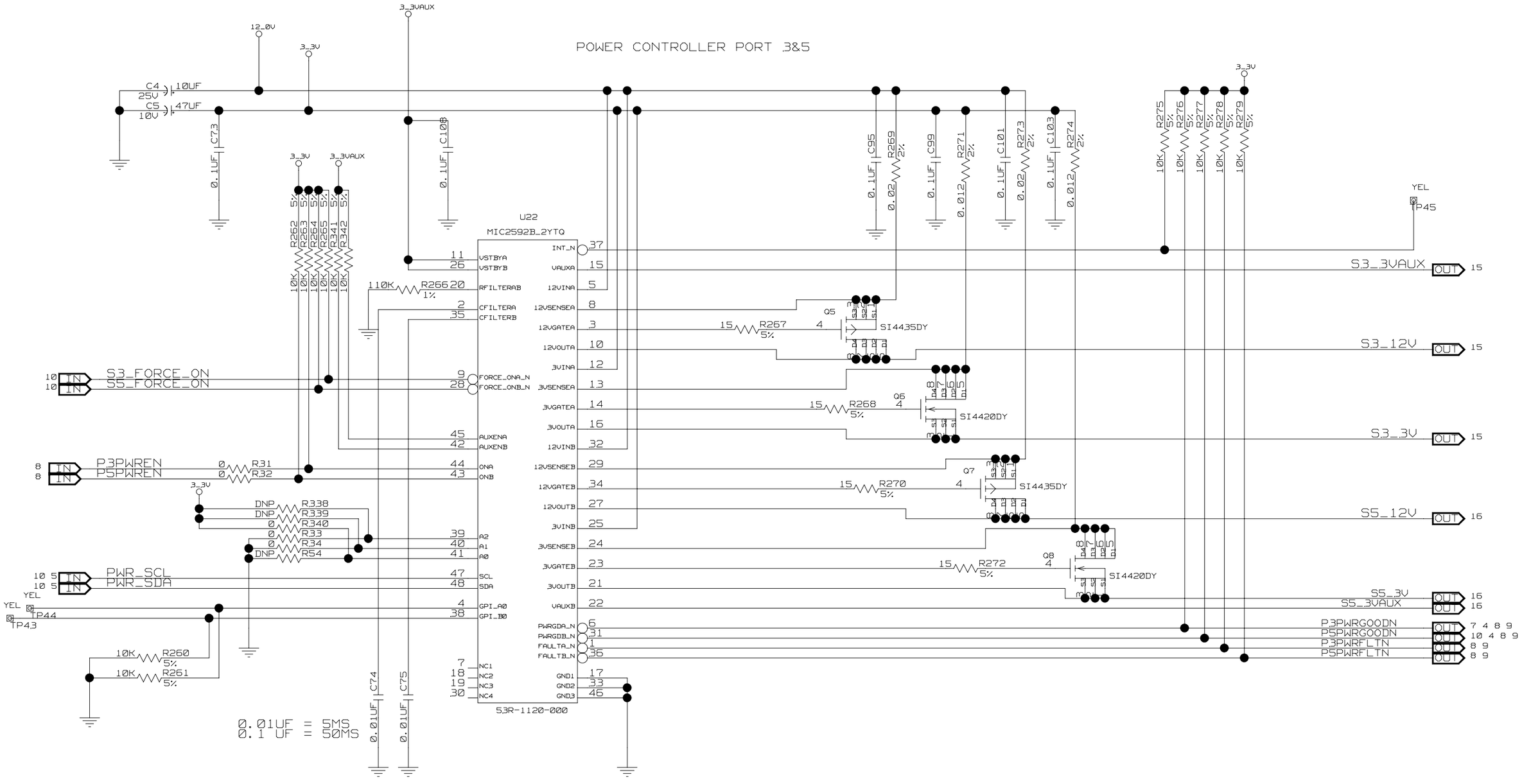
TITLE 89EBPES8T5A

HOT SWAP CONTROL PORT 2/3

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

Thu Apr 24 10:22:16 2008 SHEET 10 OF 17



TITLE 89EBPES8T5A

HOT SWAP CONTROL PORT 3/5

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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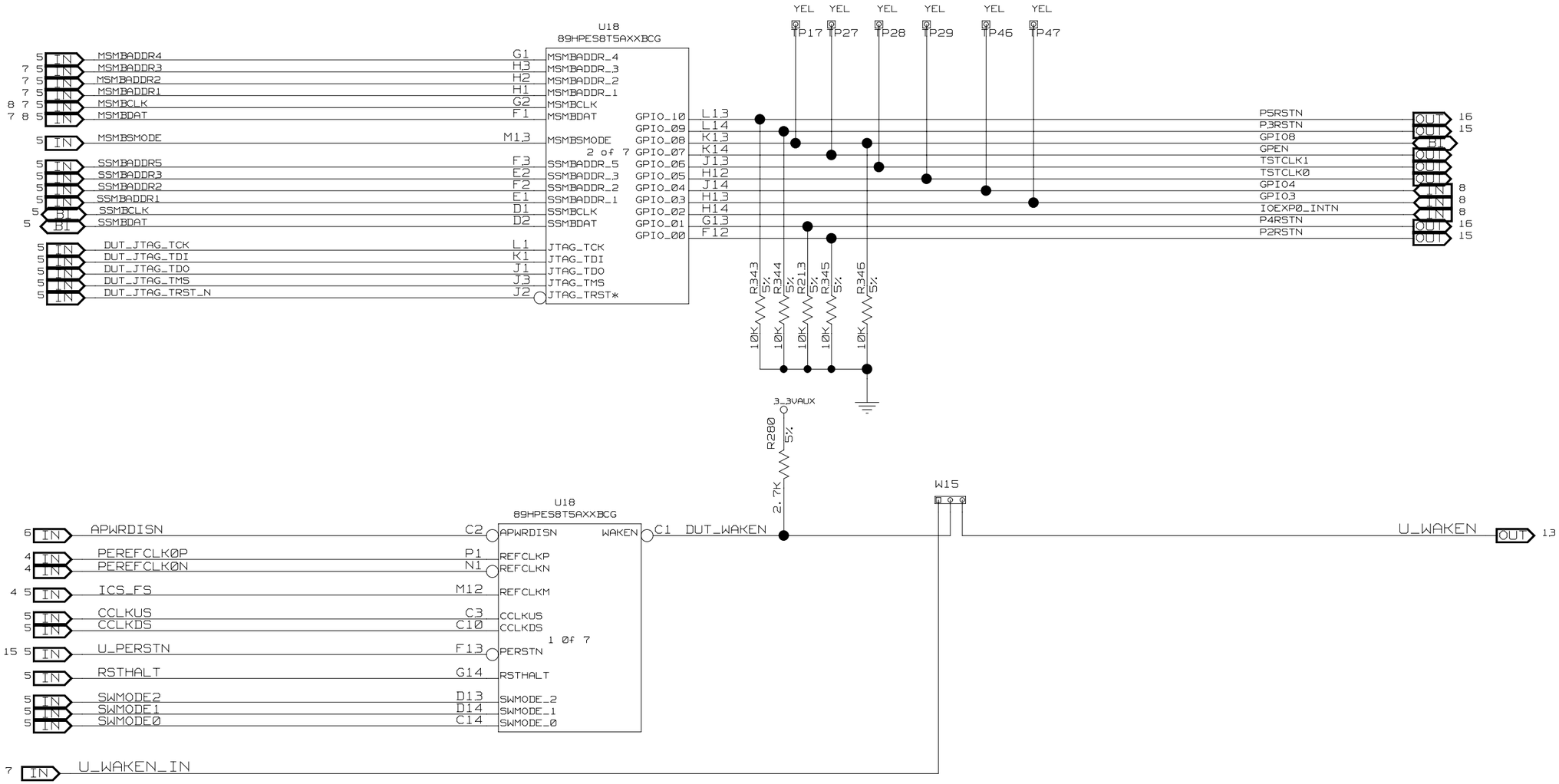

TITLE 89EBPES8T5A PES8T5A CLOCK, SMBUS, GPIO			
SIZE B	DRAWING NO. SCH-00162	FAB P/N 18-6.36-002	REV. 1.0
AUTHOR T. Tran		CHECKED BY D. Huang	
Thu Apr 24 10:22:17 2008		SHEET 12 OF 17	

RENESAS

12_0V_US

3_3V_US

3_3VAUX

C44 10UF 25V

C45 6.8UF 25V

C46 10UF 25V

C56 6.8UF 25V

P1

PCIE_X4_EDGE

B1	+12V	PRSTN1#	A1
B2	+12V	+12V	A2
B3	RSVD	+12V	A3
B4	GND	GND	A4
B5	SMCLK	JTAG_TCK	A5
B6	SMDAT	JTAG_TDI	A6
B7	GND	JTAG_TDO	A7
B8	+3.3V	JTAG_TMS	A8
B9	JTAG_TRSTN	+3.3V	A9
B10	3.3VAUX	+3.3V	A10
B11	WAKE#	PERST#	A11
B12	RSVD	GND	A12
B13	GND	REFCLK+	A13
B14	PETP0	REFCLK-	A14
B15	PETN0	GND	A15
B16	GND	PERP0	A16
B17	PRSTN2#	PERN0	A17
B18	GND	GND	A18
B19	PETP1	RSVD	A19
B20	PETN1	GND	A20
B21	GND	PERP1	A21
B22	GND	PERN1	A22
B23	PETP2	GND	A23
B24	PETN2	GND	A24
B25	GND	PERP2	A25
B26	GND	PERN2	A26
B27	PETP3	GND	A27
B28	PETN3	GND	A28
B29	GND	PERP3	A29
B30	RSVD	PERN3	A30
B31	PRSTN2#	GND	A31
B32	GND	RSVD	A32

12 IN U_WAKEN

13 IN U_PERN0

13 IN U_PERP0

13 IN U_PERP1

13 IN U_PERN1

13 IN U_PERP2

13 IN U_PERN2

13 IN U_PERP3

13 IN U_PERN3

DNP R347 NA

PERSTN OUT 5 6

U_REFCLKP OUT 4

U_REFCLKN OUT 4

U_PETP0 OUT 13

U_PETN0 OUT 13

U_PETP1 OUT 13

U_PETN1 OUT 13

U_PETP2 OUT 13

U_PETN2 OUT 13

U_PETP3 OUT 13

U_PETN3 OUT 13

PORT 0 UPSTREAM EDGE CONNECTOR PROVIDES ALL POWER FOR BOARD

U18

89HPES8T5AXXBCG

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13 IN	U_PERP0	A13	PE0RP00	PE0TP00	B11	0.1UF C160	U_PETP0 OUT 13
13 IN	U_PERN0	B13	PE0RN00	PE0TN00	A11	0.1UF C152	U_PETN0 OUT 13
13 IN	U_PERP1	B8	PE0RP01	PE0TP01	A10	0.1UF C161	U_PETP1 OUT 13
13 IN	U_PERN1	A8	PE0RN01	PE0TN01	B10	0.1UF C153	U_PETN1 OUT 13
13 IN	U_PERP2	B7	PE0RP02	PE0TP02	A5	0.1UF C162	U_PETP2 OUT 13
13 IN	U_PERN2	A7	PE0RN02	PE0TN02	B5	0.1UF C154	U_PETN2 OUT 13
13 IN	U_PERP3	A2	PE0RP03	PE0TP03	B4	0.1UF C163	U_PETP3 OUT 13
13 IN	U_PERN3	B2	PE0RN03	PE0TN03	A4	0.1UF C155	U_PETN3 OUT 13

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TITLE 89EBPES8T5A

PES8T5A PORT 0 EDGE CONN

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-6.36-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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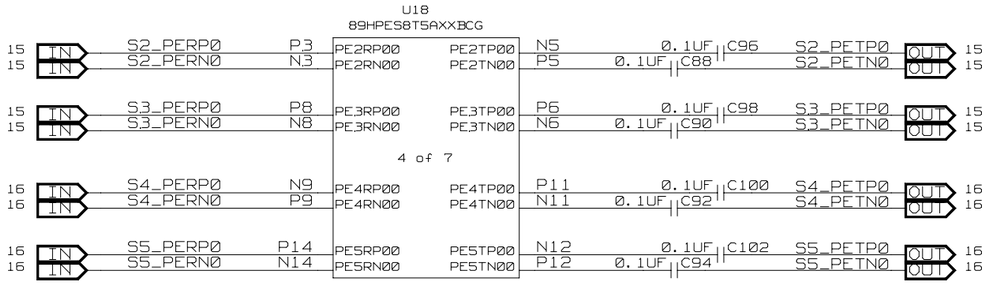

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TITLE 89EBPES8T5A

PES8T5A DOWNSTREAM PORTS

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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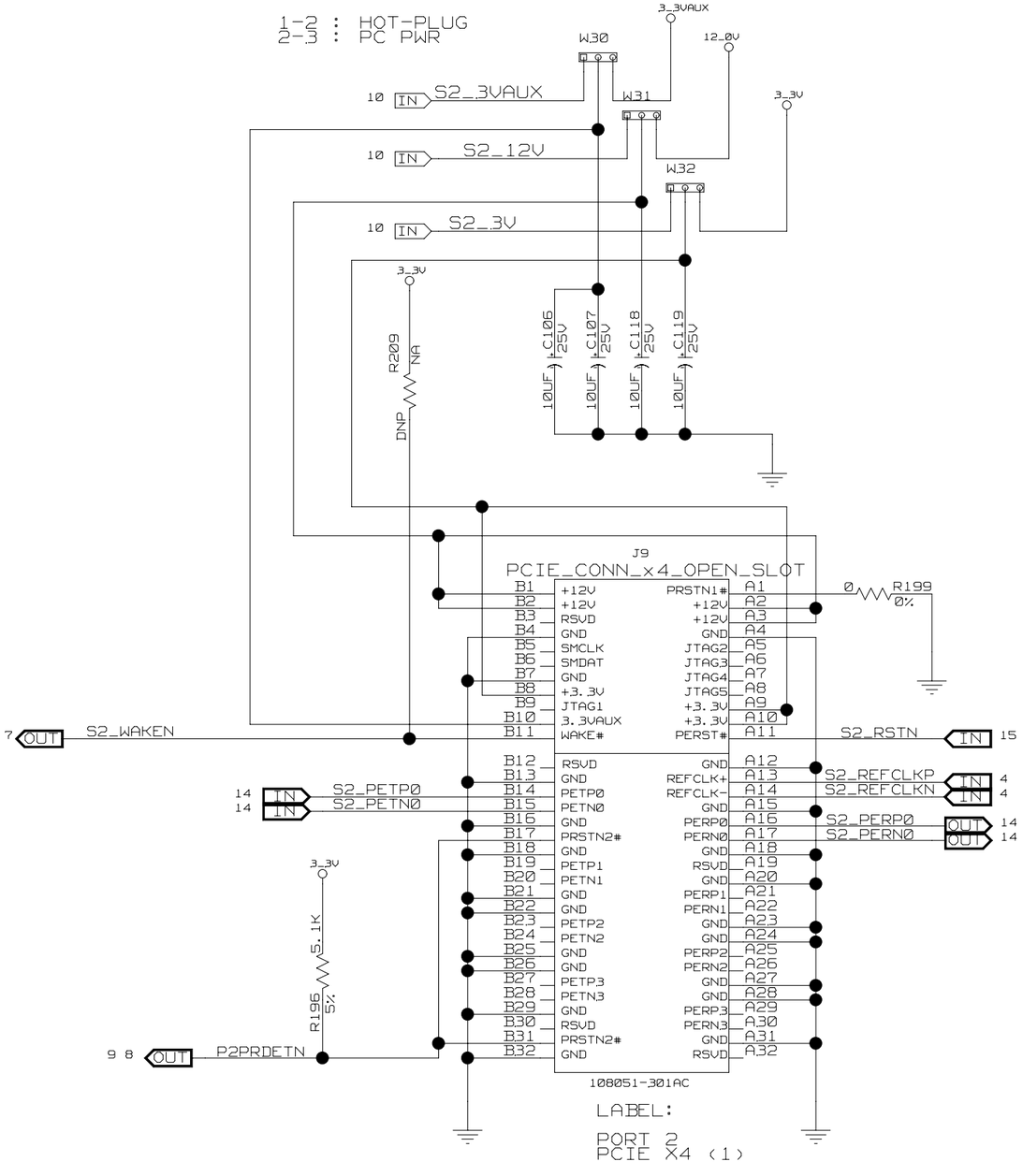
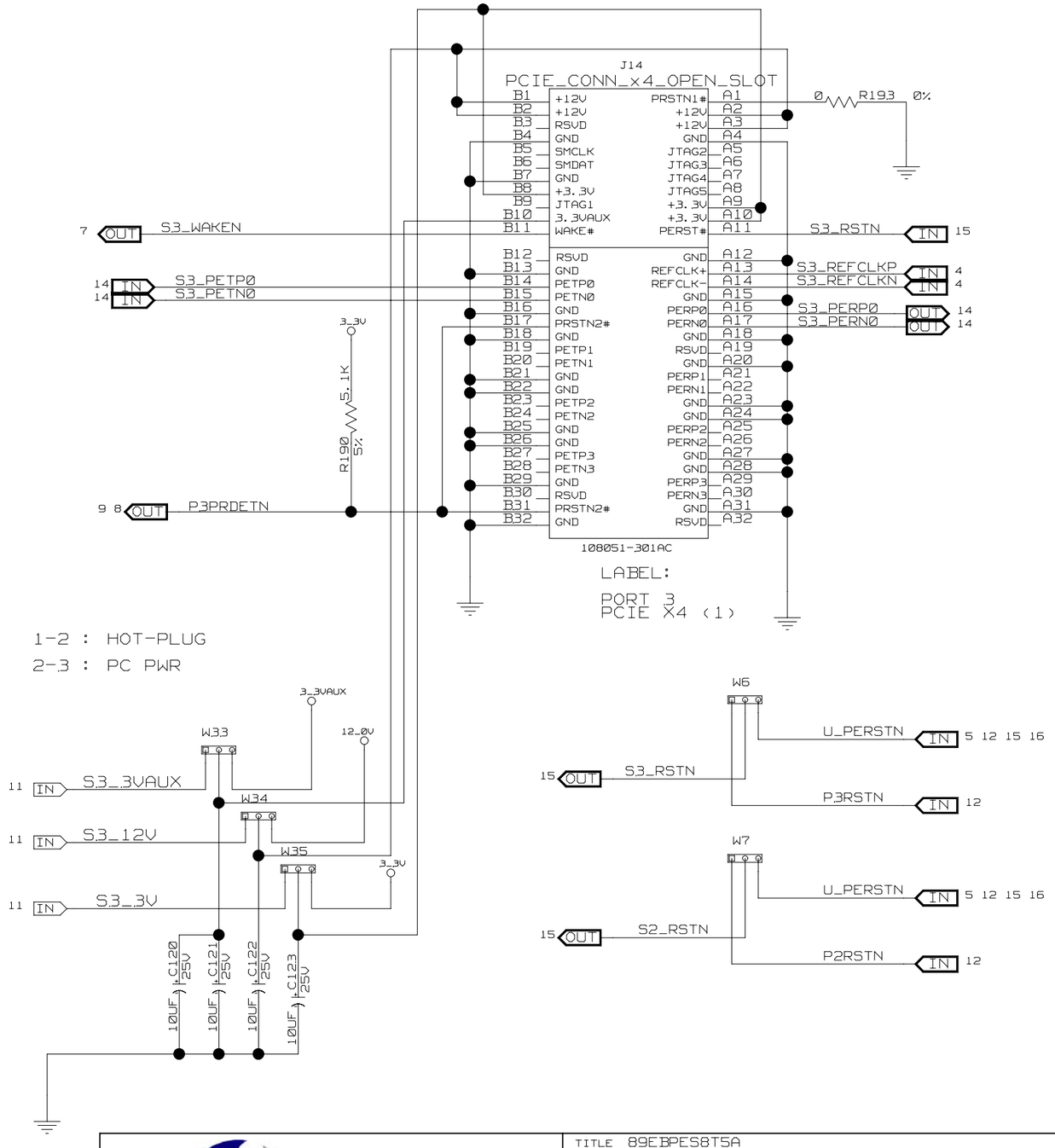
1-2 : HOT-PLUG
2-3 : PC PWR



1-2 : HOT-PLUG
2-3 : PC PWR



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PORT 2 AND PORT 3

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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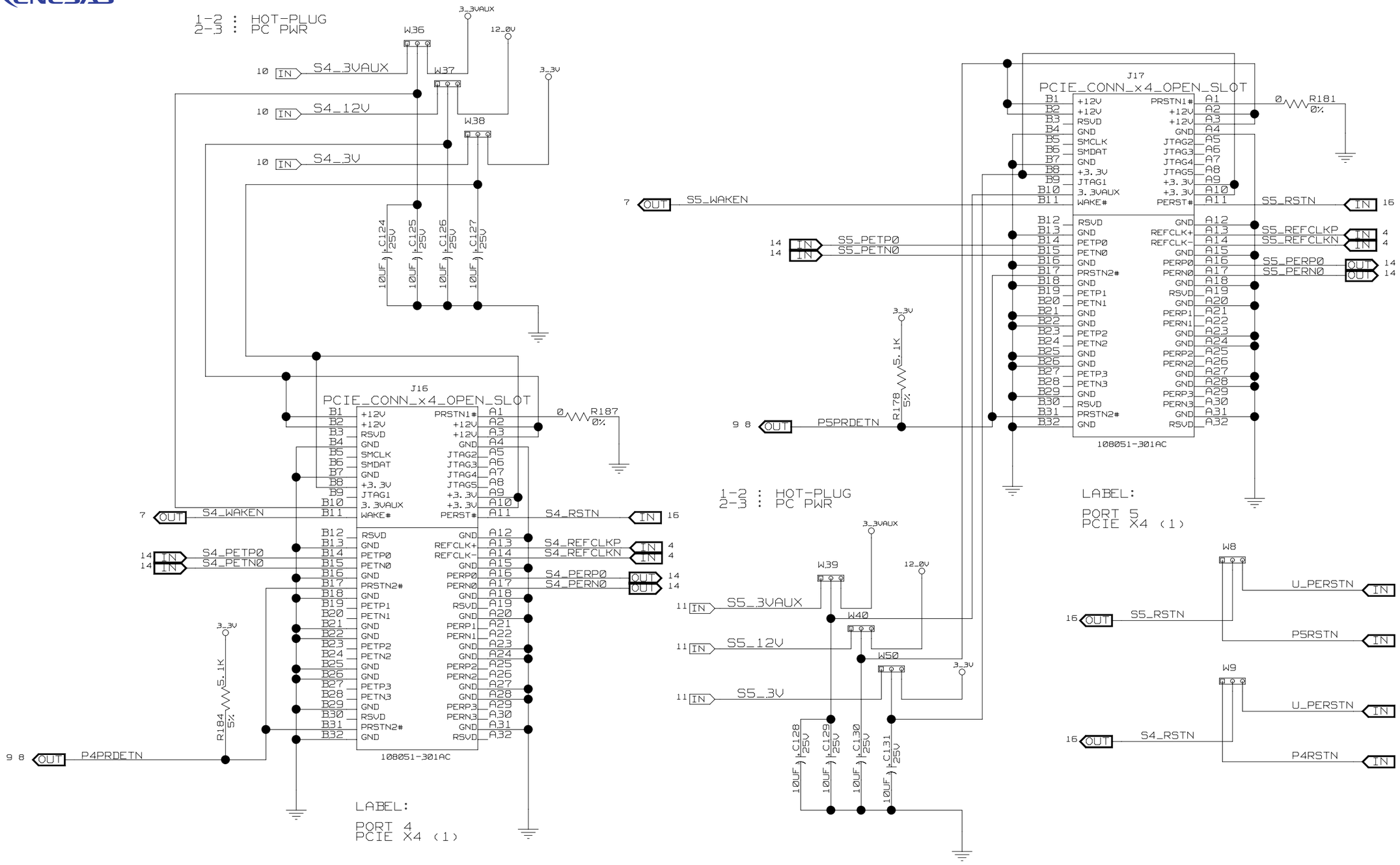

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TITLE 89EBPES8T5A

PORT 4 AND PORT 5

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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JUMPERS MUST BE POPULATED FOR NORMAL OPERATION

DUT_VTT

DUT_VDDPE

DUT_3_3V

DUT_VDDCORE

1_0V_pea

DUT_VDDPEA

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U18
89HPES8T5AXXBCG
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89HPES8T5AXXBCG
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TITLE 89EBPES8T5A

PES8T5A POWER

SIZE	DRAWING NO.	FAB P/N	REV.
B	SCH-00162	18-636-002	1.0

AUTHOR	CHECKED BY
T. Tran	D. Huang

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