User's Manual

RZ/G1C

User's Manual: Hardware

for Rich Graphics Applications

ARM®

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the hardware functions and electrical characteristics of the LSI. It is intended for users designing application systems incorporating the LSI. A basic knowledge of electric circuits, logical circuits, and LSIs is necessary in order to use this manual.

The manual comprises an overview of the product; descriptions of the CPU, system control functions, peripheral functions, and electrical characteristics; and usage notes.

> Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The following documents apply to the RZ/G1C. Make sure to refer to the latest versions of these documents.

Document Type	Description	Document Title	Document No.
User's manual for Hardware	Overview of hardware, area map, pin assignment, pin multiplexing, pin function controller, general purpose I/O port pins, clock, reset, core functions, graphics, video processing, sound processing, and network modules, serial interfaces, storage, timers, other on-chip peripheral functions, debugging, and electrical characteristics of the RZ/G1C.	RZ/G1C User's Manual: Hardware	R01UH0695EJ0100

2. Notation of Numbers and Symbols

Bit notation: Bits are shown in high-to-low order from left to right.

Number notation: Binary numbers are given as B'XXXX, hexadecimal numbers are given as H'XXXX, and decimal numbers are given as XXXX.

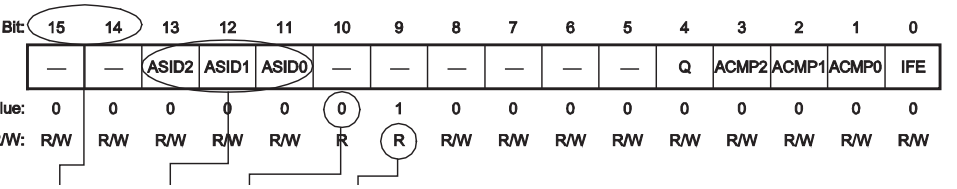
Signal notation: A number sign (#) after the name indicates that a signal or pin is active-low, unless otherwise specified.

Example: PRESET#

3. Register Notation

Each register description includes a bit chart, illustrating the arrangement of bits, and a table of bits, describing the meanings of the bit settings, unless otherwise specified.

[Bit Chart]



[Table of Bits]

(1) (2) (3) (4) (5)

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved
14	—	0	R	These bits are always read as 0.
13 to 11	ASID2 to ASID0	All 0	R/W	Address Identifier These bits enable or disable the pin function.
10	—	0	R	Reserved This bit is always read as 0.
9	—	1	R	Reserved This bit is always read as 1.
	—	0		

Note: The bit names and sentences in the above figure are examples, and have nothing to do with the contents of this manual.

(1) Bit
Indicates the bit number or numbers.
In the case of a 32-bit register, the bits are arranged in order from 31 to 0. In the case of a 16-bit register, the bits are arranged in order from 15 to 0.

(2) Bit name
Indicates the name of the bit or bit field.
When the number of bits has to be clearly indicated in the field, appropriate notation is included (e.g., ASID[3:0]).
A reserved bit is indicated by "–".
Certain kinds of bits, such as those of timer counters, are not assigned bit names. In such cases, the entry under Bit Name is blank.

(3) Initial value
Indicates the value of each bit immediately after a power-on reset, i.e., the initial value.
0: The initial value is 0.
1: The initial value is 1.
–: The initial value is undefined

(4) R/W
For each bit and bit field, this entry indicates whether the bit or field is readable or writable, or both writing to and reading from the bit or field are impossible.
The notation is as follows:

R/W: The bit or field is readable and writable.
R/(W): The bit or field is readable and writable.
However, writing is only performed to flag clearing.
R/WC0: The bit or field is readable and writable. Writing 0 to the bit initializes the bit.
Writing 1 to the bit is ignored.
R/WC1: The bit or field is readable and writable. Writing 1 to the bit initializes the bit.
Writing 0 to the bit is ignored.
R: The bit or field is readable.
"R" is indicated for all reserved bits. When writing to the register, write the value under Initial Value in the bit chart to reserved bits or fields.
W: The bit or field is writable.
Note that values read from write-only bits are not guaranteed, unless they are specified in the chart of bits.

(5) Description
Describes the function of the bit or field and specifies the values for writing.

Contents

1. Overview

1.1 Introduction

The RZ/G1C is MCU that features the basic functions for Rich Graphics Applications.

The RZ/G1C includes:

- Two 1.0 GHz ARM® Cortex®-A7 MPCore™ cores,
- Memory controller for DDR3-SDRAM (DDR3-1000) with 32 bits × 1 channel,
- Three-dimensional graphics engines,
- Video processing unit,
- 2 channels Display Output,
- 2 channels Video Input,
- Sound processing unit,
- SD card host interface,
- USB2.0 host/function interfaces,
- CAN interface,
- Digital video encoder / decoder, and
- LVDS display output interface.

Also, a full implementation of the extremely expandable and Internal AXI bus has been adopted for the RZ/G1C.

This bus structure is optimized for maximum system performance, leading to the realization of high-performance and cost-effective rich graphics applications.

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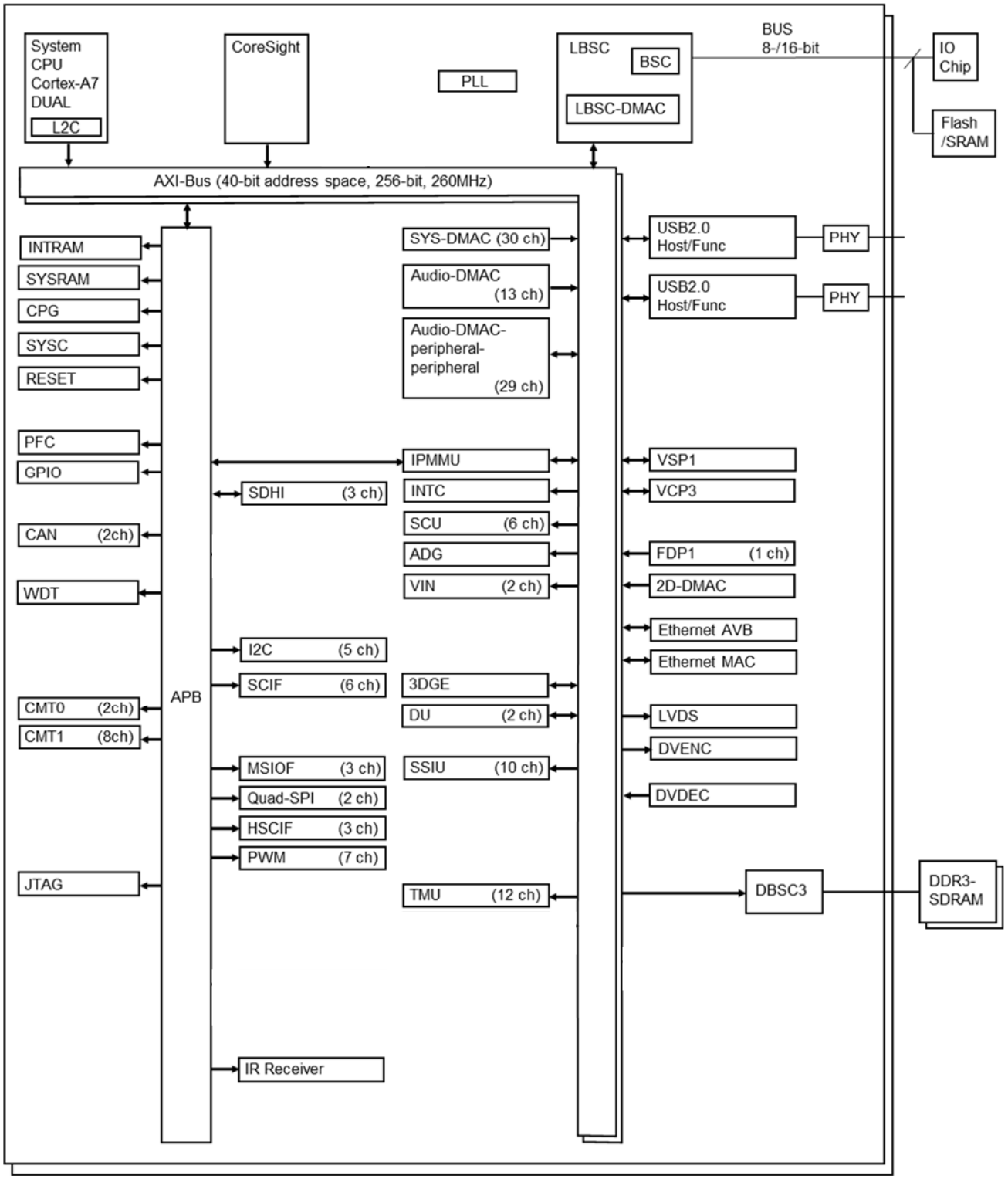
1.2 System Configuration Diagram



Note: For the description of each abbreviation, refer to following "item" column in table.

Figure 1.1 RZ/G1C System Configuration

1.3 List of Specifications

1.3.1 ARM Core

Item	Description
System CPU Cortex-A7 (Dual core)	• Cortex-A7 Dual MPCore 1.0 GHz • L1 I/D cache 32/32 KBytes, L2 cache 512 KBytes • NEON™/VFPv4 supported • Security extension supported
ARM debugger (ARM® CoreSight™)	• CoreSight system compliant • JTAG/SWD I/F supported • CoreSight ETR 16 KBytes for program flow trace • CoreSight ETR 4 KBytes for system trace

1.3.2 CPU Core Peripherals

Item	Description
Operating clock pulse generation circuit (CPG)	• Generates the clocks from external clock (EXTAL). — Maximum Cortex-A7 clock: 1.0 GHz — Maximum AXI-bus clock: 260 MHz — Maximum SDRAM bus clock: DDR3-1000 — Maximum media clock: 260 MHz — Maximum peripheral clock (HPϕ): 130 MHz • Module-standby mode supported • Includes module reset registers to control reset operation of individual on-chip peripheral modules
Reset (RESET)	• Includes one reset-signal external output port for external modules • Includes Boot Address Register etc.
Pin function controller (PFC)	• Setting multiplexed pin functions for LSI pins Function of the RZ/G1C pin selectable by setting the registers in the PFC module • Module selection Enable and disable the functions of RZ/G1C LSI pins to which pin functions from multiple pin groups are assigned by setting the registers in the PFC module. • Pull-up control for each LSI pin On/off of the pull-up resistor on each LSI pin can be controlled by setting the registers in the PFC module. • Control of SDIO functions SDIO functions, including the driving ability of pins for the SDIF, can be controlled by setting registers of the PFC
General-purpose I/O (GPIO)	• General-purpose I/O ports: 156 ports • Supports GPIO interrupts.

1.3.3 External Bus Module

Item	Description
Local bus state controller (LBSC)	• EX-BUS interface: max. 16-bit bus • Frequency: 65 MHz • External area divided into several areas and managed — Allocation to space of area 0 and area 1 or allocation to space of area 0 only is selected at startup time. — Area 0 supports 128-MByte memory space (startup mode). — I/F settings, bus width settings, and wait state insertion are possible for each area • SRAM interface — Wait states can be inserted through register settings Period of waiting is set in cycle unit, and the maximum value is 15. — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Burst ROM interface — Wait states can be inserted through register settings — Number of bursts can be set through register settings — Connectable bus widths: 16 bits or 8 bits • Byte-control SRAM interface (available with area 1 only) — Byte-control SRAM interface — Wait states can be inserted through register settings — EX_WAIT pin can be used for wait state insertion — Connectable bus widths: 16 bits or 8 bits • Supports external buffer enable/direction control
LBSC-DMAC	• Number of channels: LBSC-DMAC three channels • Address space: Physical address space • Transfer direction: Peripheral to memory (AXI-bus), memory (AXI-bus) to peripheral • Data packing for peripheral read data: Memory write data length is selectable as transfer data length to memory side. • Transfer data length: Peripheral (APB-bus) side: 1, 2, 4 bytes Memory (AXI-bus) side: 4 or 16 (channel 2), 32 (channel 0 and 1) bytes • Transfer burst length: 1, 8 (transfer with a burst length of 8 supported only for LBSCDMAC00, 01) • Number of transfers — Maximum number of transfers: 16 M (16,777,216 transfers), 64M (67,108,864 transfers), (64 M transfers supported only for LBSC-DMAC00) — Minimum number of transfers: One • Address mode: Dual address mode • Transfer modes: Single transfer mode, continuous transfer mode • Transfer end interrupt: Occurs at the end of the number of transfers specified in the register

Item	Description	
DDR3-SDRAM bus state controller (DBSC)	• 1 channel (32-bit bus) • DDR3-SDRAM can be connected directly. • Memory Size: Up to 2 GB (8-Gbit memory × 2) • Data bus width: 32 bits × 1 • Auto Refresh/Self Refresh/Partial Array Self Refresh supported • Auto Pre-charge Mode/Bank Active Mode	
Memory connections	DDR3-SDRAM compliant to JEDEC JESD79-3E	Supports from 512-Mbit to 8-Gbit memory unit configurations 32-bit DDR3-1000 (two units with 16-bit width)

1.3.4 Internal Bus Module

Item	Description
AXI-bus	• On-chip main bus — Bus protocol: AXI3 with QoS control — Frequency: 260 MHz — Bus width: 256 bits/128 bits
Direct memory access controller (SYS-DMAC)	• 30 channels for ARM domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller (Audio-DMAC)	• 13 channels for Audio domain • Address space: 4 GBytes on architecture • Data transfer length: Byte, word (2 Bytes), longword (4 Bytes), 8 Bytes, 16 Bytes, 32 Bytes and 64 Bytes • Maximum number of transfer times: 16,777,216 times • Transfer request: Selectable from on-chip peripheral module request and auto request • Bus mode: Selectable from normal mode and slow mode • Priority: Selectable from fixed channel priority mode and round-robin mode • Interrupt request: Supports interrupt request to CPU at the end of data transfer • Repeat function: Automatically resets the transfer source, destination, and count at the end of DMA transfer (by descriptor function) • Descriptor function (each channel) supported • MMU (each channel) supported • Channel bandwidth arbiter (each channel)
Direct memory access controller (Audio-DMAC-Peripheral-Peripheral)	Audio-DMAC (for transfer from Peripheral to Peripheral) • 29 channels for audio domain • Data transfer length: longword (4 Bytes) • Transfer count: Transfer count is not specified (DMA transfer is made from the transfer-start to transfer-stop settings.) • Transfer request: Selectable from on-chip audio peripheral module request • Priority: round-robin mode • Interrupt request: not supports interrupt request to CPU at the end of data transfer

Item	Description	
IPMMU	An IPMMU is a memory management unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.	
Interrupt controller (INTC)	INTC-SYS	• 10 interrupt pins which can detect external interrupts • Fall/rise/high level/low level detection is selectable • On-chip peripheral interrupts: Priority can be specified for each module • Max. 384 shared peripheral interrupts supported • 16 software interrupts that have been generated and 6 private peripheral interrupts supported • 32-level priority selectable • Trust Zone supported

1.3.5 Local Memory

Item	Description
Inter connect RAM (INTRAM)	• RAM0 of 72 KBytes • RAM1 of 4 Kbytes • RAM2 of 128 KBytes

1.3.6 Graphics Units

Item		Description
3D graphics engine (3DGE)		• Imagination Technologies PowerVR Series5 SGX531 (260 MHz) • Tile based architecture • Universal Scalable Shader Engine (USSE) • Advanced Shader Feature Set - in excess of Microsoft VS3.0, PS3.0 & OGL2.0 • Industry standard API support - OGL-ES 2.0 • Fine grained task switching, load balancing and power management • Advanced geometry DMA driven operation for minimum CPU interaction • Programmable high quality image anti-aliasing • Fully virtualized memory addressing for OS operation in an unified memory architecture
Display unit (DU)	Display channel	Two independently controllable channels
	Interface	• Digital RGB: Two channel (RGB888 × 2) • LVDS output: Four lanes × One channel • NTSC (CVBS) analog output × 1 channel • digital video encoder, D/A converter integrated
	Screen size and number of composite planes	• Maximum screen size: 4095 × 2047 • Number of planes specifiable: 1 (ARGB8888)
	CRT scanning method	Non-interlaced, interlaced sync, interlaced sync & video
	Synchronization method	Master, TV sync
	Internal color palette	Includes four color palette planes which can display 256 of 260 thousands colors at the same time.
	Digital RGB	• Two output channel • Output on rising and falling edges of the synchronizing signal (resolution for the same display) • 8-bit precision for each RGB color • Frequency: Dotclk 100 MHz (Single edge) Dotclk 50 MHz (Double edge)
	LVDS interface (1ch)	• Output: compliant with TIA/EIA-644; five pairs of differential output (Four pairs of data and one pair of clock) • Frequency: Dotclk 87 MHz • Selectable 8 output formats
	Blending ratio settings	Number of color palette planes with blending ratio: 4
	Dot clock	Switchable between external input and internal clock
	Digital Video encoder	See Digital Video encoder below

Item	Description	
Video input (VIN)	Input data format	• 8-, 10-, or 12-bit YCbCr422 (CbYCrY format) • 16-bit YCbCr422 (8 bits (Y) + 8 bits (CbCr) format) • 20-bit YCbCr422 (10 bits (Y) + 10 bits (CbCr) format) • 24-bit YCbCr422 (12 bits (Y) + 12 bits (CbCr) format) • 18-bit RGB666 • 24-bit RGB888
	Clipping function	Up to 2048 × 2048
	Horizontal scaling	Uses a 9-tap multi-phase filter. Up to two times, but only scaling down is possible for HD1080i or HD720P data.
	Vertical scaling	Scaling by linear interpolation Up to three times, but only scaling down is possible for HD1080i or HD720P data.
	Output format	RGB-565, ARGB-1555, YCbCr422, RGB888(channel 0,1), YC separation, and extraction of the Y component
	Video clock	100 MHz
Digital video decoder (DVDEC)	• Video input Composite video input (CVBS) • A/D converter for video signal input VIN0 and VIN1 pin input selection Low-pass filter (LPF) Sync tip clamp Programmable gain amplifier (PGA) (0 to 6.021 dB) 10-bit precision pipelined A/D converter • Sync separation Noise reduction LPF, auto level control sync slicer, horizontal auto frequency control (AFC), vertical count-down, interlace detection, auto gain control (AGC)/peak limiter control • Y/C separation NTSC 2D, PAL 2D, and SECAM 1D supported. • Chroma-key decoding NTSC, PAL, and SECAM supported. Color killer, auto color control (ACC), TINT correction, R-Y axis correction • Digital clamp Pedestal clamp (Y), center clamp (Cb/Cr), noise detection • Adjustment of output gain Contrast: 0 to approximately 2 times Color (Cb/Cr independently): 0 to approximately 2 times	

Item	Description	
Digital video encoder (DVENC)	NTSC encoder	• Input 480i data (8 bits for each of Y and CB/CR) • Output composite Y/C • NTSC, PAL, PAL-M, PAL-N, and PAL-60 encode processing • Y1+C composite (CVBS) signal generation • Image quality adjustment function (12 bits) Color TINT Skin tone correction Brightness Contrast Black stretch Sharpness/unsharpness • Correction • Superimposition of CGMS (525i) or WSS (625i) • Superimposition of closed caption • BPF processing for chroma (C) signal • Rovi's Rev. 7.1.L1 ACP encoding technology • Total gain control in response to changes in the full-scale voltage from the DAC
	Video DAC	• Supports the NTSC/PAL composite output. • Analog macro output voltage: 1.30 Vp-p (typ.) • Caution: AV33 = 3.3 V; Rload ≥ 10 kΩ; Cload ≤ 20 pF • Low-power-consumption function (power-down mode). • 10-bit digital signal output (8bit available) • Conversion on rising edges of the 27-MHz clock signal

1.3.7 Video Processing

Item	Description
Video signal processor 1 (VSP1)	The VSP1 is the successor IP of Renesas' VIO6-IP series, and has the following features. (1) Supports Various Data Formats and Conversion — Supports YCbCr444/422/420, RGB, αRGB, αplane — Color space conversion and changes to the number of colors by dithering — Color keying (2) Full HD Video Processing — Up and down scaling with arbitrary scaling ratio — Super resolution processing — Blending of four picture layers and raster operations (ROPs) (3) Full HD Picture Quality/Color Correction with 1D/3D Look Up Table(LUT) — Dynamic γ correction and gain correction — Correction of color (to adjust skin tones or colors in memory) — Hue, brightness, and saturation adjustment — 1D histogram (4) Direct Connection to Display Module — Display unit (DU) supported

Item	Description
Video processing unit (VCP3)	The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This IP (Intellectual Property) is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU. The VCP3 has the following features: • Support for multiple codecs H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding H.262/MPEG-2 MP (Main Profile) decoding MPEG-4 ASP (Advanced Simple Profile) decoding VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding H.263 Baseline decoding AVS Jizhun Profile decoding VP8 decoding • Support for HDTV resolutions 1920 pixels × 1080 lines × 60 frames/second × 1channels Maximum performance will change with securable bus bandwidth. • Data handling on a picture-by-picture basis Encodes/decodes data one picture (frame or field) at a time. • High picture quality Supports the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix). High-efficiency motion vector detection by a combination of discrete search and trace search Highly efficient real-time intra-prediction by Prediction from Original Image (POI) Optimal-mode selection by Rate-Distortion (RD) cost evaluation Picture quality control based on activity analysis results which match visual models • Low power dissipation Dynamically disables the clocks for the entire VCP3. Dynamically disables the clocks for individual submodules. • Includes its own dedicated 64-KByte cache
Fine display processor 1 (FDP1)	The FDP1 is the de-interlacing module which converts the interlaced video to progressive video, and has the following features. (1) Supports various data formats — Input: YCbCr444/422/420 — Output: YCbCr444/422/420 and RGB/αRGB (2) Full HD video processing performance (3) High image quality de-interlacing algorithm — Motion adaptive de-interlacing — Accurate still detection — Diagonal line interpolation (DLI)
2-dimensional DMAC (2D-DMAC)	• Supports conversion between various RGB formats. • Image extraction function: Capable of extracting an image and storing it as a separate image in the RAM. • Image rotation/reversal function: Reverses an image vertically/horizontally or rotates it by 90°/270°. • Simple scaling function: Capable of scaling an image two times in the X or Y direction. • Format conversion • Supports conversion from RGB to RGB and from YCbCr to YCbCr.

1.3.8 Sound Interface

Item	Description	
Sampling rate converter unit (SCU)	Overall specification	• Includes six SRC modules — Supports the quality suitable for audio sound (THD+N -132dB) : four modules — Supports the quality suitable for voice sound (THD+N -96dB) : two modules • The SRC module is capable of correcting phase change and delay (timing jitter) generated during data transfer over external memories or external devices. • The channel transfer unit (CTU), mixer (MIX), and digital mute and volume function (DVC) can be used on two fixed output channels.
	Sampling rate conversion (SRC)	• Capable of asynchronous sampling rate conversion • Supports resolutions up to 24 bits • Two kinds of filter type for SRC. — Supports the quality suitable for audio sound (THD+N -132dB) : Realized the filter by passband -1dB@0.4575FS, cutoff -18dB@0.5FS. — Supports the quality suitable for voice sound (THD+N -96dB) : Realized the filter by passband -1dB@0.4561FS, cutoff -72dB@0.5FS. (Characteristics of each filter is written in the equivalent/up-sampling cases.) • Automatically generates antialiasing filter coefficients • For monaural to eight-channel sound sources
	Channel transfer unit (CTU)	• Downmixing and splitter functions — Conversion of eight input channels into four output channels — Conversion of six input channels into two output channels — Conversion of two input channels into four sets of two output channels — Conversion of one input channel into eight sets of one output channel — No conversion
	Mixer (MIX)	• Mixing (adds) two to four sources into one • Ratio for adding sources is selectable • Ratio is dynamically changeable • Mixing with volume ramp is available (ramp period is selectable)
	Digital volume and mute function (DVC)	• Volume control function including digital volume, volume ramp, and zero-crossing mute • The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute, or -120 to 18 dB) • The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment • The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2 • The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Item	Description	
Serial sound interface unit (SSIU)	Overall specification	• Includes ten SSI modules functioning as interfaces with external devices. — Supports short and long formats — Supports TDM format (six modules of ten modules can be used for this function) • Max. 4 independent stereo sound sources in a TDM format can be distributed to each course within RZ/G1C. Moreover Max. 4 independent stereo sound source in RZ/G1C can be combined output in TDM format.
	Serial sound interface (SSI)	• Operating mode: non-compressed mode (Not support compressed mode) • Supports versatile serial audio formats (I2S/left justified/right justified) • Supports master/slave functions • Programmable word clock, bit clock generation functions • Multichannel format functions (up to four channels) • Supports 8-/16-/18-/20-/22-/24-/32-bit data formats • Supports TDM mode • Supports WS continue mode • The DMA controller or interrupts control the transfer of data to and from the SSI module. • Supports short and long frames for monaural data (valid data lengths are 8 and 16 bits) • Up to nine independent clock signals can be input.
Audio clock generator (ADG)	• Selection or division of audio clock signals	

1.3.9 Storage

Item	Description
USB2.0 host & function module (USB2.0)	• 2 channels (Host-Function 2 channel) • PHY integrated • USB Host (EHCI/OHCI) 2LINK • Compliant with USB2.0 • USB Function 2LINK • Compliant with USB2.0 (High-Speed) • Interrupt request • Internal dedicated DMA
SD host interface (SDHI)	• 3 channels — Interfaces 0 and 1: Support SDR104 class transfer rate at Max. 78 MBytes/sec. @ 156 MHz, and SDXC. Does not support CPRM. — Interfaces 1: Also support eMMC mode. eMMC 4.41 base — Data bus 1/4/8-bit MMC mode (not support SPI mode) — Interfaces 2: SDR50 class transfer rate at Max. 48 MBytes/sec. @ 97.5 MHz, and SDXC. Does not support CPRM. • Supports SD memory/SDIO interface (1-/4-bit SD buses). • Error check function: CRC7 (command/response), CRC16 (data) • Card detection function • Supports write protection

1.3.10 Network

Item	Description
CAN interface (CAN)	• 2 channels • Supports CAN specification 2.0B • ISO-11898-1 compliant • Maximum bit rate: 1 Mbps • Message box — Normal mode: 32 receive-only mailboxes and 32 mailboxes for transmission/reception — FIFO mode: 32 receive-only mailboxes and 24 mailboxes for transmission/reception, 4-stage FIFO for transmission, and 4-stage FIFO for reception • Reception — Data frame and remote frame can be received. — Selectable receiving ID format — Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • Acceptance filter — Mask can be enabled or disabled for each mailbox. • Transmission — Data frame and remote frame can be transmitted. — Selectable transmitting ID format (only standard ID, only extended ID, or both IDs) — Selectable ID priority mode or mailbox number priority mode • Sleep mode for reducing power consumption
Ethernet AVB	• Supports IEEE802.1BA, IEEE802.1AS, IEEE802.1Qav and IEEE1722 functions • Supports transfer at 1000 Mbps and 100 Mbps • Magic packet detection • Supports Reception Filtering to separate streaming frames from different sources • Supports interface conforming to IEEE802.3 PHY GMII (Gigabit Media Independent Interface) and MII (Media Independent Interface)
Ethernet MAC	• IEEE802.3u MAC (Ether) function • Supports transfer at 10 and 100 Mbps • Flow control conforming to IEEE802.3x or back pressure system • Supports interface conforming to IEEE802.3u • Magic packet detection • Includes DMAC • Supports RMII (Reduced Media Independent Interface)

1.3.11 Timer

Item	Description
Watchdog timer (WDT)	• Single channel • Internal 16-bit watchdog timer operated by RCLK • Programmable overflow time-period: more than 1 hour count capable
Compare match timer 0 (CMT0)	• Two channels • 32-bit timer (16 bits/32 bits can be selected) • Source clock: RCLK clock • Compare match function provided • Interrupt requests
Compare match timer 1 (CMT1)	• Eight channels • 48-bit timer (16 bits/32 bits/48 bits can be selected) • Source clock: RCLK/system clock • Compare match function provided • Interrupt requests
Timer unit (TMU)	• 4 sets of 3-channel 32-bit timer • Auto-reload type 32-bit down counter • Internal prescaler • Interrupt request • 2 channels for input capture

1.3.12 Peripheral Module

Item	Description
Multi-master I2C bus interface (I2C)	• 5 channels for general purpose • Philips I2C bus interface method supported • Master/slave functions • Multi-master functions • Transfer rate up to 400 kbps supported • Programmable clock generation from the system clock

Item	Description	
Serial communication interface with FIFO (SCIF)	Overall specification	• 6 channels • Asynchronous, clock-synchronized modes • Asynchronous serial communication mode The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats. — Data length: 7 bits or 8 bits — Stop bits: 1 bit or 2 bits — Parity: Even/odd/none — Receive error detection: Parity, framing, and overrun errors — Break detection: A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level). When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR). • Clock synchronous serial communication mode The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication. — Data length: 8 bits — Receive error detection: Overrun errors • Full-duplex communication capability The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception. • On-chip baud rate generator, enabling any bit rate to be selected The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock. • Eight interrupt sources The SCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently. • DMA data transfer When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

Item	Description
Clock-synchronized serial interface with FIFO (MSIOF)	• 3 channels • Max. speed: 26 Mbps • Internal 64 stages transmit FIFOs/internal 128 stages receive FIFOs • Supports master and slave modes • Internal prescaler • Supports serial formats: IIS, SPI (master and slave modes) • Interrupt request, DMAC request
Quad-SPI (QSPI)	• 2 channels • Single/Dual/Quad-SPI: serial slave transfer enabled • Supports master mode • SPCLK clock rate: 1…4080 in master mode; Max. 97.5 MHz
High-speed serial communication interface with FIFO (HSCIF)	• 3 channels • Asynchronous serial communication mode • Capable of full-duplex communication • On-chip baud rate generator, enabling any bit rate to be selected • Eight interrupt sources • DMA data transfer • Modem control functions (HRTS and HCTS) are stored. • The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available. • A receive data ready (DR) or a timeout error (TO) can be detected during reception.
PWM timer (PWM)	• 7 channels • Cycle width (10 bits) of PWM output can be set. • High-level periods (10 bits) of PWM output can be set. • Periods in the range from two to 2^{24} × 1024 cycles of the Pϕ clock can be set. • Continuous pulse or single pulse output selectable
IR Receiver (IR)	• Auto detection of a leader • Built-in circuit for synchronization protection (noise malfunction prevention) during the detection of a leader • Up to 64 bits of a code are receivable per frame. • Capable of receiving a maximum of two frames of code
Boot Function (BOOT)	• System startup with selectable boot mode at power-on reset • Program downloaded to internal memory (LRAM) • Autorun function for the downloaded program • LBSC area 0 boot support • QSPI boot (ch0 only) support • eMMC boot support

1.3.13 Others

Item	Description
JTAG	JTAG interface for CoreSight
Package	FC-BGA 501pin 21mm × 21mm 0.8mm ball pitch

1.4 Power Supply Voltages and Temperature Range

- Power supply voltage (typ.)
  1.8 V: (SD and JTAG)
  1.2 V: (Core)
  1.5 V: (DDR3-I/O SSTL)
  3.3 V: (Others)
- Temperature range
  Tc = –40°C to 115°C
  Ta = –40°C to 85°C

2. Area Map

Table 2.1 Address Space (Over 4-Gbyte Space)

Address			Space	Description
H'00_00000000	to	H'00_FFFFFFFF	Legacy 4-Gbyte space	LBSC, DBSC3, etc.
H'01_00000000	to	H'01_FFFFFFFF	DDR0/DBSC3 (DDR0)	DBSC3
H'02_00000000	to	H'02_FFFFFFFF	Reserved	—
H'03_00000000 (H'03_40000000	to to	H'03_FFFFFFFF H'03_BFFFFFFF)	DBSC3 (DDR0) shadow	DBSC3 (up to 2 Gbytes)
H'04_00000000	to	H'04_FFFFFFFF	DDR0 shadow	DBSC3
H'05_00000000	to	H'05_FFFFFFFF	Reserved	—
H'06_00000000	to	H'06_FFFFFFFF	DDR0 shadow	DBSC3
H'07_00000000	to	H'07_FFFFFFFF	Reserved	—
H'08_00000000	to	H'08_FFFFFFFF	CCI-AXI	CCI-AXI
H'09_00000000	to	H'09_FFFFFFFF	Reserved	—
H'0A_00000000	to	H'0A_FFFFFFFF	Reserved	—
H'0B_00000000	to	H'0B_FFFFFFFF	Reserved	—
H'0C_00000000	to	H'0C_FFFFFFFF	Reserved	—
H'0D_00000000	to	H'0D_FFFFFFFF	Reserved	—
H'0E_00000000	to	H'0E_FFFFFFFF	Reserved	—
H'0F_00000000	to	H'0F_0FFFFFFF	uTLB (IPMMUS0 slave)	IPMMUv7 slave for uTLB (SYS0)
H'0F_10000000	to	H'0F_1FFFFFFF	uTLB (IPMMUS1 slave)	IPMMUv7 slave for uTLB (SYS1)
H'0F_20000000	to	H'0F_2FFFFFFF	uTLB (IPMMUMP slave)	IPMMUv7 slave for uTLB (MP)
H'0F_30000000	to	H'0F_3FFFFFFF	Reserved	—
H'0F_40000000	to	H'0F_4FFFFFFF	uTLB (IPMMUDS slave)	IPMMUv7 slave for uTLB (SYS-DMA)
H'0F_50000000	to	H'0F_5FFFFFFF	uTLB (IPMMUM slave)	IPMMUv7 slave for uTLB (Media)
H'FF_00000000	to	H'FF_FFFFFFFF	Reserved	—

Note: Access to the reserved spaces is prohibited.

Table 2.2 Address Space (Legacy 4-Gbyte Space)

Address			Space	Description
H'00_00000000	to	H'00_03FFFFFF	LBSC	Area 0 asynchronous memory
H'00_04000000	to	H'00_07FFFFFF		Area 1 asynchronous memory
H'00_08000000	to	H'00_0BFFFFFF		Reserved
H'00_0C000000	to	H'00_0FFFFFFF		Reserved
H'00_10000000	to	H'00_13FFFFFF		Reserved
H'00_14000000	to	H'00_15FFFFFF		Reserved
H'00_16000000	to	H'00_17FFFFFF		Reserved
H'00_18000000	to	H'00_19FFFFFF		Area 6A asynchronous memory
H'00_1A000000	to	H'00_1BFFFFFF		Area 6B asynchronous memory
H'00_1C000000	to	H'00_1FFFFFFF		Reserved
H'00_20000000	to	H'00_2FFFFFFF		Reserved
H'00_30000000	to	H'00_37FFFFFF	Reserved	—
H'00_40000000	to	H'00_5FFFFFFF	DBSC3 (DDR0)	SDRAM Area (over 4-Gbyte mirror space)
H'00_60000000	to	H'00_7FFFFFFF		
H'00_80000000	to	H'00_BFFFFFFF		
H'00_C0000000	to	H'00_DFFFFFFF	Extended DRAM0	
H'00_E0000000	to	H'00_E5FFFFFF	Reserved	—
H'00_E6000000	to	H'00_E61FFFFF	SYS-APB1	System-domain peripheral bus (CP)
H'00_E6200000	to	H'00_E6BFFFFF	SYS-APB2	System-domain peripheral bus (HP)
H'00_E6C00000	to	H'00_E6FFFFFF	SYS-APB3	System-domain peripheral bus (MP)
H'00_E7000000	to	H'00_E77FFFFF	SYS-APB4	System-domain peripheral bus (DMAC)(CP)
H'00_E7800000	to	H'00_E7BFFFFF	SYS-APB5	System-domain peripheral bus (DMAC)(HP)
H'00_E7C00000	to	H'00_E7FFFFFF	SYS-APB6	System-domain peripheral bus (DMAC)(MP)
H'00_E8000000	to	H'00_E807FFFF	S3 cache	IPMMU, ICB control register
H'00_E8080000	to	H'00_E8FFFFFF	Reserved	—
H'00_E9000000	to	H'00_E9FFFFFF	CDBGTOP STM	CoreSight STM
H'00_EA000000	to	H'00_EBFFFFFF	Reserved	—
H'00_EC000000	to	H'00_EC0FFFFF	MP-APB1	SRC/CMD
H'00_EC100000	to	H'00_EC1FFFFF	MP-APB2	SSI
H'00_EC200000	to	H'00_EC2FFFFF	MP-APB3	SSI0-9
H'00_EC300000	to	H'00_EC3FFFFF	MP-APB4	SRC/CMD
H'00_EC400000	to	H'00_EC4FFFFF	MP-APB5	SSI
H'00_EC500000	to	H'00_EC5FFFFF	MP-APB6	SRC/CMD/SSI/ADG
H'00_EC600000	to	H'00_EC9FFFFF	MP-APB7	SYS-DMAC/PP-DMAC
H'00_ECA00000	to	H'00_ECBFFFFF	SPUV	SPUV
H'00_ECC00000	to	H'00_ECFFFFFF	Reserved	—
H'00_ED000000	to	H'00_EDFFFFFF	S3 cache	On-chip RAM mirror address for MP-domain
H'00_EE000000	to	H'00_EE07FFFF	Reserved	—
H'00_EE080000	to	H'00_EE09FFFF	USB0	USB (EHCI)
H'00_EE0A0000	to	H'00_EE0BFFFF	Reserved	—

Address			Space	Description
H'00_EE0C0000	to	H'00_EE0DFFFF	USB2	—
H'00_EE0E0000	to	H'00_EE0E7FFF	Reserved	—
H'00_EE0E8000	to	H'00_EE0EBFFF	STBE	SRAM area (16 KB) for the EtherAVB descriptor
H'00_EE0EC000	to	H'00_EE0FFFFF	Reserved	—
H'00_EE100000	to	H'00_EE2FFFFF	Reserved	—
H'00_EE300000	to	H'00_EE4FFFFF	SDHI1	—
H'00_EE500000	to	H'00_EE6FFFFF	Reserved	—
H'00_EE700000	to	H'00_EE8FFFFF	EtherMAC	—
H'00_EE900000	to	H'00_EFFFFFFF	Reserved	—
(H'00_F0000000	to	H'00_F0FFFFFF)	Reserved	—
H'00_F1000000	to	H'00_F10FFFFF	GIC	GIC
(H'00_F1000000	to	H'00_FBFFFFFF)	Reserved	—
H'00_F1100000	to	H'00_FBFFFFFF	Reserved	—
H'00_FC000000	to	H'00_FCFFFFFF	DBG	Debug module (JTAG)
H'00_FD000000	to	H'00_FD7FFFFF	Reserved	—
H'00_FD800000	to	H'00_FDFFFFFF	3DG	3D accelerator control register (128 bit) SGX531
H'00_FE000000	to	H'00_FE5FFFFF	Reserved	—
H'00_FE600000	to	H'00_FE67FFFF	MXT	Image accelerator control registers
H'00_FE680000	to	H'00_FE6FFFFF		
H'00_FE700000	to	H'00_FE77FFFF		
H'00_FE780000	to	H'00_FE8FFFFF	Reserved	—
H'00_FE900000	to	H'00_FE93FFFF	SYS-APB7	Image accelerator control register
H'00_FE940000	to	H'00_FE95FFFF		
H'00_FE960000	to	H'00_FEAAFFFF		
H'00_FEAB0000	to	H'00_FEBFFFFF	Reserved	—
H'00_FEC00000	to	H'00_FEFFFFFF	LBSC	Asynchronous memory controller control register
(H'00_FF000000	to	H'00_FF5FFFFF)	Reserved	—
H'00_FF000000	to	H'00_FF1FFFFF	SYS-APB8	AXI router
H'00_FF600000	to	H'00_FF6FFFFF	Reserved	—
H'00_FF700000	to	H'00_FF7FFFFF	Reserved	—
H'00_FF800000	to	H'00_FF8FFFFF	SYS-APB8	AXI-bus register
H'00_FF900000	to	H'00_FFBFFFFF	Reserved	—
H'00_FFC00000	to	H'00_FFCFFFFF	Reserved	—
H'00_FFD00000	to	H'00_FFEFFFFF	Reserved	—
H'00_FFF00000	to	H'00_FFFFFFFF	Reserved	—

Note: Access to reserved spaces and reserved addresses is prohibited.

Table 2.3 List of Module Base Address in each Domain (CP, HP, MP and other Clock Domains)

Domain	Address[31:24]	Address[23:0]	Module
SYS-APB1 (cpck)	H'E6	H'02 0000	RWDT
		H'05 0000	GPIO0
		H'05 1000	GPIO1
		H'05 2000	GPIO2
		H'05 3000	GPIO3
		H'05 4000	GPIO4
		H'05 5000	GPIO5
		H'06 0000	PFC
		H'10 0000	DBG
		H'13 0000	CMT1
		H'15 0000	CPGA
		H'16 0000	RESET
		H'18 0000	SYSC
		H'1C 0000	IRQC

Domain	Address[31:24]	Address[23:0]	Module
SYS-APB2 (hpck)	H'E6	H'28 0000	IPMMUS0
		H'29 0000	IPMMUS1
		H'2A 0000	IPMMUGP
		H'2C 0000	HSCIF0 (CIS)
		H'2C 8000	HSCIF1 (CIS)
		H'2D 0000	HSCIF2 (CIS)
		H’30 0000	Inter-connect RAM 2
		H’31 0000	Inter-connect RAM 2
		H'3A 0000	Inter-connect RAM 0
		H'3B 0000	Inter-connect RAM 0
		H'3C 0000	Inter-connect RAM 1
		H'50 8000	I2C0 (CIS)
		H'51 8000	I2C1 (CIS)
		H'52 0000	I2C4 (CIS)
		H'53 0000	I2C2 (CIS)
		H'54 0000	I2C3 (CIS)
		H'59 0000	USBHS0
		H'59 8000	USBHS1
		H'5A 0000	USBHS-DMAC00
		H’5A 8000	USBHS-DMAC01
		H'5B 0000	USBHS-DMAC10
		H’5B 8000	USBHS-DMAC11
		H'5C 0000	USB-DDM0
		H’60 0000	CC5.2P
		H'68 0000	USB-DDM1
		H'70 0000	SYS-DMAC (0 to 14)
		H'72 0000	SYS-DMAC (15 to 29)
		H'74 0000	IPMMUDS
		H'78 0000	S3CTRL
		H'79 0000	DBSC1
		H'7A 0000	DBSC2
SYS-Ether	H'E6	H'80 0000	EtherAVB
SYS-QSPI	H'E6	H'B1 0000	QSPI0
SYS-APB3 (mpck)	H'E6	H'E0 0000	MSIOF2
		H'E1 0000	MSIOF1
		H'E2 0000	MSIOF0

Domain	Address[31:24]	Address[23:0]	Module
65 MHz clock module	H'E6	H'E3 0000	PWM0
		H'E3 1000	PWM1
		H'E3 2000	PWM2
		H'E3 3000	PWM3
		H'E3 4000	PWM4
		H'E3 5000	PWM5
		H'E3 6000	PWM6
		H'E5 8000	SCIF2(CIS)
		H'E6 0000	SCIF0(CIS)
		H'E6 8000	SCIF1(CIS)
		H'E8 0000	CAN0
		H'E8 8000	CAN1
		H'EA 8000	SCIF3(CIS)
		H'EE 0000	SCIF4(CIS)
		H'EE 8000	SCIF5(CIS)
		H'EF 0000	VIN0
		H'EF 1000	VIN1
SYS-APB2	H'E6	H'F0 0000	CoreSight APB bridge
		H'F1 0000	CoreSight APB bridge
		H'F2 0000	CoreSight APB bridge
		:	CoreSight APB bridge
		H'FD 0000	CoreSight APB bridge
		H'FE 0000	CoreSight APB bridge
		H'FF 0000	CoreSight APB bridge
MP-APB1	H'EC	H'00 0000	SRC_CMD_BUSIF (window)
MP-APB2	H'EC	H'10 0000	SSIU (window)
MP-APB3	H'EC	H'24 1000	SSI0 to SSI9 (window)
MP-APB4	H'EC	H'30 0000	SRC_CMD_BUSIF (window)
MP-APB5	H'EC	H'40 0000	SSIU (window)
MP-APB6	H'EC	H'50 0000	SRC1 to SRC6, CMD0 and CMD1 (apb)
		H'54 0000	SSI0 to SSI9 (apb)
		H'5A 0000	ADG (apb)
MP-APB7	H'EC	H'68 0000	IPMMUMP
		H'70 0000	SYS-DMAC1 (apb)

Domain	Address[31:24]	Address[23:0]	Module
SDHI	H'EE	H'10 0000	SDHI0-APB (optional)
		H'16 0000	SDHI2-APB
SYS-QSPI	H'EE	H'20 0000	QSPI1
MXT	H'FE	H'90 0000	VLC (VCP)
		H'90 0200	CE (VCP)
		H'90 8000	VPC0
		H'92 8000	VSP1
		H'93 0000	VSPD0
		H'94 0000	FDP0
		H'95 1000	IPMMUMX
		H'96 0000	MXI
MXT	H'FE	H'A0 0000	2D-DMAC
		H'B0 0000	DU0-0
		H'B8 0000	DVENC-APB
		H'B8 1000	DVDEC-APB
		H'B8 9000	DISCOM0
		H'B8 A000	DISCOM1
		H'B9 0000	LVD-APB
SYS-APB8	H'FF	H'00 0044	PRR
		H'80 0000	SYS-AXIRouter
		H'82 0000	MP-AXIRouter
		H'84 0000	Audio-AXIRouter
		H'85 0000	DM-AXIRouter
		H'86 0000	SYS-AXIRouter256
		H'87 0000	MXT-AXIRouter
		H'88 0000	armpu

Domain	Address[31:24]	Address[23:0]	Module
RT-APB1 (bck)	H'FF	H'CA 0000	CMT0
RT-APB3 (pclk)	H'FF	H'F6 0000	TMU1 (channels 3 to 5)
		H'F7 0000	TMU2 (channels 6 to 8)
		H'F8 0000	TMU3 (channels 9 to 11)

Notes: 1. "—": Undefined address
2. Addresses other than the above are reserved and access to reserved or undefined addresses is prohibited.
3. Some modules are internal and unused.

Contact your local sales representative regarding these modules and modules listed as "optional" in the table.

3. Pin Assignment

3.1 Pin Assignment

PKG TOP VIEW 21 mm PKG (ball 25 × 25, 0.8 mm pitch)

Total 501

	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	
A	VSS	SSI_WS5_A	SSI_SCK5_A	TX3_A	MSIOF0_SCK_A	MSIOF0_RXD_A	HRX1_A	SD0_CD	SD2_CLK	MMC0_CLK	MMC0_D2	MMC0_D6	SD0_CLK	VSS	M0DQ31	M0DQ28	M0DQ27	VDDQ_M0	VSS	M0DQ21	M0DQ18	VDDQ_M0	M0CS1#	M0CK1#	VSS	A
B	SSI_SCK6_A	SSI_SDATA5_A	RX3_A	SCL2_A	MSIOF0_SYNC_A	MSIOF0_TXD_A	HTX1_A	SD0_WP	SD2_DAT1	MMC0_CMD	MMC0_D1	MMC0_D5	SD0_DAT0	SD0_DAT3	M0DQ29	M0DQ30	VSS	M0DQ22	M0DQ16	M0DM2	VSS	M0DQ23	M0CK1	VSS	M0CK0#	B
C	SSI_SDATA6_A	SSI_WS6_A	VSS	SDA2_A	SCL1_A	MSIOF0_SS1_A	VSS	SD2_CD	SD2_DAT0	SD2_DAT3	VSS	MMC0_D4	MMC0_D7	SD0_DAT2	M0DM3	M0DQS3#	M0DQ25	M0DQ17	M0VREFDQ1	M0DQS2#	M0DQ20	M0ODT1	VSS	M0CK0	M0CS0#	C
D	VSS	SSI_WS78_A	SSI_SCK78_A	VSS	SDA1_A	MSIOF0_SS2_A	HRTS1#_A	SD2_WP	SD2_CMD	SD2_DAT2	MMC0_D0	MMC0_D3	SD0_CMD	SD0_DAT1	M0DQ26	M0DQS3	M0DQ24	M0DQ19	VSS	M0DQS2	M0CKE1	VSS	M0ODT0	M0DQ7	VDDQ_M0	D
E	AUDIO_CLKOUT_A	AUDIO_CLKA_A	AUDIO_CLKB_A	AUDIO_CLKC_A	VSS	VSS	VCCQ	HCTS1#_A	VSS	VCCQ_SD2	VCCQ_MMC	VSS	VCCQ_SD0	VSS	VDDQ_M0	VSS	VDDQ_M0	VSS_DDRPLL1	VSS	VSS	VSS	M0CKE0	M0DQ5	VSS	M0DQ4	E
F	SSI_SDATA3	SSI_WS34	SSI_SCK34	SSI_SDATA8_A	SSI_SDATA7_A	VSS	VCCQ	VSS	VSS	VSS	VSS	VSS	VSS	VSS	VDDQ_M0	VSS	VDDQ_M0	VDD_DDRPLL1	VSS	VSS	VSS	M0DQS0	M0DQS0#	M0DM0	M0DQ6	F
G	SSI_WS0129_A	SSI_SCK0129_A	SSI_SDATA4_A	SSI_SCK4_A	SSI_WS4_A	VSS														VDD_DDRPLL2	VSS_DDRPLL2	VSS	VSS	M0DQ1	VSS	G
H	SSI_WS1_A	SSI_SCK1_A	VSS	SSI_SDATA0_A	VCCQ	VCCQ														VSS	VSS	M0DQ3	M0DQ2	M0DQ0	VDDQ_M0	H
J	SSI_SDATA2_A	SSI_WS2_A	SSI_SCK2_A	SSI_SDATA1_A	VSS	VSS														VDDQ_M0	VDDQ_M0	M0DQ8	M0DM1	VSS	M0DQ10	J
K	SSI_SDATA9_A	SSI_WS9_A	SSI_SCK9_A	SCL0_A	VCCQ	VCCQ					VSS	VDD	VSS	VDD	VSS_CPGPLL1	VDD_CPGPLL1				VSS	VSS	VSS	M0VREFDQ0	M0DQ9	M0DQ15	K
L	VI1_DATA11	AVB_TXD3	AVB_TXD4	AVB_TXD5	SDA0_A	VSS				VSS	VSS	VDD	VSS	VDD	VSS_CPGPLL1	VDD_CPGPLL1				VDDQ_M0	VDDQ_M0	M0DQS1#	M0DQS1	M0DQ12	VSS	L
M	VI1_DATA8	VI1_DATA9	VI1_DATA10	VI1_VSYNC#	VCCQ	VCCQ				VDD	VDD	VDD	VSS	VDD	VSS	VSS				VSS	VSS	M0DQ14	M0DQ13	VDDQ_M0	M0DQ11	M
N	VI1_DATA7	VI1_CLKENB	VI1_FIELD	VI1_HSYNC#	VSS	VSS				VDD	VDD				VDD	VDD				VDD_CPGPLL3	VSS_CPGPLL3	M0CAS#	VSS	M0WE#	M0RAS#	N
P	VI1_DATA3	VI1_DATA4	VI1_DATA5	VI1_DATA6	VCCQ	VCCQ				VDD	VDD	VDD	VSS	VDD	VSS	VSS				VDDQ_M0	VDDQ_M0	M0A11	M0A10	M0BA2	M0A15	P
R	VI1_CLK	VSS	VI1_DATA0	VI1_DATA1	VI1_DATA2	VSS				VSS	VSS	VDD	VSS	VDD	VDD_CPGPLL0	VDD_CPGPLL0				VSS	VSS	M0BKPRST#	M0A6	M0BA0	VSS	R
T	VDD	VDD	VDD	VDD	VDD	VDD				VSS	VSS	VDD	VSS	VDD	VSS_CPGPLL0	VSS_CPGPLL0				VSS	M0VREFCA	M0ZQ	M0A9	M0SDBUP	M0A3	T
U	VO	VSSQA_DAC	VSS	CBP	VSSQA_ADC	VCCQA_ADC														VSS	VDDQ_M0	M0A8	M0A4	M0A7	VDDQ_M0	U
V	VCCQA_DAC	VSSQA_DAC	VSSQA_DAC	VIN2A	VRP	VRM														VDDA_USBPLL	VSSA_USB	M0BA1	VSS	M0RESET#	M0A0	V
W	VIDEO_X1	VIDEO_X2	VSS	VIN1A	VSS	REXT														USB_REF	VSSA_USB	M0A12	M0A2	M0A13	M0A14	W
Y	D15	D14	D13	D12	D11	VSS	VSS	VCCQ	VSS	VCCQ	VSS	VSS	LVDSREFRIN	VCCQA_LVDS	VDDA_LVDSPLL	VCCQ18	VCCQ	VCCQ	VSS	VSS	VSS	USB0_PWEN	VSSA_USB	M0A5	M0A1	Y
AA	D10	D9	D8	D7	VSS	VSS	DU0_DG1	VCCQ	DU0_DB2	VCCQ	DU0_CDE	VSS	VSS	VSSQA_LVDS	VSS	VSS	VCCQ18	VSS	VSS	VSS	VSS	USB0_OVC	USB0_VBUS	VCCQA_USB	VSS	AA
AB	D6	D5	D4	VSS	DU0_DR0	DU0_DR4	DU0_DG0	DU0_DG5	DU0_DB1	DU0_DB6	DU0_DOTCLKOUT1	DU0_EXVSYNC/DU0_VSYNC	VSS	TXOUT1P	VSS	TXCLKOUTP	VSS	BSMODE	VSS	NMI	USB1_PWEN	VSS	USB1_VBUS	USB0_DM	USB0_DP	AB
AC	D3	D2	VSS	QSPI0_MISO/QSPI0_IO1	QSPI0_IO3	DU0_DR3	DU0_DR7	DU0_DG4	DU0_DB0	DU0_DB5	DU0_DOTCLKOUT0	DU0_EXHSYNC/DU0_HSYNC	VSS	TXOUT1M	VSS	TXCLKOUTM	VSS	VSS	TCK	PRESETOUT#	PRESET#	USB1_OVC	VSS	USB1_DM	USB1_DP	AC
AD	D1	D0	QSPI0_SSL	QSPI0_MOSI/QSPI0_IO0	QSPI0_IO2	DU0_DR2	DU0_DR6	DU0_DG3	DU0_DG7	DU0_DB4	DU0_DB7	DU0_EXODDF/DU0_ODDF_DISP_CDE	TXOUT0P	VSS	TXOUT2P	VSS	TXOUT3P	TDI	TRST#	TMS	VSS	VSS	VSS	VSS	VSS	AD
AE	VSS	CLKOUT	EX_WAIT0	QSPI0_SPCLK	VSS	DU0_DR1	DU0_DR5	DU0_DG2	DU0_DG6	DU0_DB3	DU0_DOTCLKIN	DU0_DISP	TXOUT0M	VSS	TXOUT2M	VSS	TXOUT3M	ACK	TDO	VSS	XTAL	EXTAL	USB_XTAL	USB_EXTAL	VSS	AE
	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15	16	17	18	19	20	21	22	23	24	25	

3.2 Mode Pin Settings

Input fixed values for BSMODE and MD0 pins. These values cannot be changed after power is supplied. The values of pins MD1 to MD11, MD13, MD14, MD21, MDT0 and MDT1 are input upon power-on reset using the PRESET pin. Power-on reset results in switching to a different function.

Legend: "0" means logic low level input, "1" means logic high level input.
"—" means either "0" or "1", but its level must be fixed.

BSMODE	Reserved Fix to 0

MD0	Reserved Fix to 0

MD3	MD2	MD1	Boot Device Selection
0	0	0	External ROM boot (area 0)
0	0	1	eMMC boot via SDHI1
0	1	0	Serial flash ROM boot via QSPI; 16 KB transfer at 48.75 MHz
0	1	1	Reserved
1	0	0	Serial flash ROM boot via QSPI; 16 KB transfer at 39.0 MHz
1	0	1	Reserved
1	1	0	Serial flash ROM boot via QSPI; 4 KB transfer at 39.0 MHz
1	1	1	Reserved

MD4	Area Division
0	Area 0: 64 Mbytes
1	Area 0: 128 Mbytes

MD5	Reserved, fixed to 1

MD7	MD6	Master Boot Processor Selection
0	0	Setting prohibited
0	1	Booted through CPU0 in Cortex-A7
1	0	Setting prohibited
1	1	Setting prohibited

MD8	EXBUS Area 0 Data Bus Width
0	8-bit
1	16-bit

MD9	EXTAL/XTAL Pin Setting
0	Inputs an external clock to the EXTAL pin
1	Connects a crystal resonator to the EXTAL/XTAL pin

MD10	MD21, MD20	MD11	MDT [1:0]	JTAG	MMC	SDHI2
0	00	—	—	Boundary SCAN	Normal mode	Normal mode
	01	—	—	Reserved	Reserved	Reserved
	10	0	—	CoreSight debug port	Normal mode	Normal mode
		1	00		Reserved	Reserved
			01		Reserved	Normal mode
			10		Reserved	Reserved
			11		Normal mode	Reserved
	11	0	—	Reserved	Normal mode	Normal mode
		1	00		CoreSight debug port	Normal mode
1	—	—	—	Reserved	Reserved	Reserved

MD14	MD13	Resonator/ Input Clock	Internal Divider	PLL1	PLL0	PLL3
0	0	20 MHz	× 1/1	× 78*	× 80	× 50
0	1	26 MHz	× 1/1	× 60*	× 60	× 56
1	0	Reserved	—	—	—	—
1	1	30 MHz	× 1/1	× 52*	× 52	× 50

Note: * VCO = 1560 MHz

4. Pin Multiplexing

Legend for the Pin Multiplexing

pullup*	Pullup on/off is controllable in PFC register. Initial state is pullup on. When these pins are used as I2C interface, external pull-up resistors are mandatory.
pulldown*	Pulldown on/off is controllable in PFC register. Initial state is pulldown on.
*	Pull on/off is controllable in PFC register. Initial state is pull off.
—	Pullup Control Column: No pullup/pulldown Function Column: Setting prohibited

Following notes are related with section 4.1.

Notes 1 After negate PRESET#, pin state is Low output and then change to High output.
Regarding transition timing, refer to Hardware manual section.

2 MD4 = 0 (64MB mode) : High output.
MD4 = 1 (128MB mode) : Low output.

3 Depends on MD21, MD20, MD11, MD10, MDT[1:0] setting.

4 Depends on MD21, MD20, MD11, MD10, MDT[1:0] setting.
In case JTAG interface is selected, "—" (no pullup/pulldown) is selected.
In case of other settings, "*" (pullup on/off is controllable in PFC register. Initial state is pullup off) is selected.

4.1 Pin Multiplexing

Table 4.1 Pin Multiplexing

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
1	E22	—	—	DDR3	M0CKE0	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
2	D21	—	—	DDR3	M0CKE1	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
3	T21	—	—	DDR3	M0VREFCA	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
4	R22	—	—	DDR3	M0BKPRST#	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
5	V24	—	—	DDR3	M0RESET#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
6	C24	—	—	DDR3	M0CK0	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
7	B25	—	—	DDR3	M0CK0#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
8	B23	—	—	DDR3	M0CK1	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
9	A24	—	—	DDR3	M0CK1#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
10	C25	—	—	DDR3	M0CS0#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
11	A23	—	—	DDR3	M0CS1#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
12	D23	—	—	DDR3	M0ODT0	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
13	C22	—	—	DDR3	M0ODT1	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
14	T22	—	—	DDR3	M0ZQ	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
15	N24	—	—	DDR3	M0WE#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
16	N25	—	—	DDR3	M0RAS#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
17	N22	—	—	DDR3	M0CAS#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
18	V25	—	—	DDR3	M0A0	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
19	Y25	—	—	DDR3	M0A1	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
20	W23	—	—	DDR3	M0A2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
1	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
2	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
3	—	—	—	—	—	—	—	—	VSS	—	—	—	—	—	—	—	—	—	—
4	—	—	—	—	—	—	VDDQ_M0	1.5V	pullup	—	—	—	—	—	—	—	—	—	—
5	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
6	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
7	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
8	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
9	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
10	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
11	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
12	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
13	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
14	—	—	—	—	—	—	VDDQ_M0	1.5V	pulldown	—	—	—	—	—	—	—	—	—	—
15	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
16	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
17	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
18	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
19	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
20	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
21	T25	—	—	DDR3	M0A3	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
22	U23	—	—	DDR3	M0A4	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
23	Y24	—	—	DDR3	M0A5	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
24	R23	—	—	DDR3	M0A6	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
25	U24	—	—	DDR3	M0A7	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
26	U22	—	—	DDR3	M0A8	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
27	T23	—	—	DDR3	M0A9	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
28	P23	—	—	DDR3	M0A10	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
29	P22	—	—	DDR3	M0A11	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
30	W22	—	—	DDR3	M0A12	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
31	W24	—	—	DDR3	M0A13	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
32	W25	—	—	DDR3	M0A14	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
33	P25	—	—	DDR3	M0A15	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
34	R24	—	—	DDR3	M0BA0	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
35	V22	—	—	DDR3	M0BA1	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
36	P24	—	—	DDR3	M0BA2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
37	F18	—	—	DDR3	VDD_DDRPLL1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
38	E18	—	—	DDR3	VSS_DDRPLL1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
39	H24	—	—	DDR3	M0DQ0	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
40	G24	—	—	DDR3	M0DQ1	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
21	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
22	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
23	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
24	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
25	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
26	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
27	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
28	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
29	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
30	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
31	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
32	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
33	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
34	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
35	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
36	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
37	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
38	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
39	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
40	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
41	H23	—	—	DDR3	M0DQ2	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
42	H22	—	—	DDR3	M0DQ3	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
43	E25	—	—	DDR3	M0DQ4	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
44	E23	—	—	DDR3	M0DQ5	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
45	F25	—	—	DDR3	M0DQ6	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
46	D24	—	—	DDR3	M0DQ7	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
47	F22	—	—	DDR3	M0DQS0	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
48	F23	—	—	DDR3	M0DQS0#	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
49	F24	—	—	DDR3	M0DM0	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
50	G20	—	—	DDR3	VDD_DDRPLL2	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
51	G21	—	—	DDR3	VSS_DDRPLL2	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
52	K23	—	—	DDR3	M0VREFDQ0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
53	J22	—	—	DDR3	M0DQ8	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
54	K24	—	—	DDR3	M0DQ9	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
55	J25	—	—	DDR3	M0DQ10	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
56	M25	—	—	DDR3	M0DQ11	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
57	L24	—	—	DDR3	M0DQ12	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
58	M23	—	—	DDR3	M0DQ13	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
59	M22	—	—	DDR3	M0DQ14	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
60	K25	—	—	DDR3	M0DQ15	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
41	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
42	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
43	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
44	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
45	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
46	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
47	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
48	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
49	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
50	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
51	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
52	—	—	—	—	—	—	—	1.5V/2	VDDQ_M0/2	—	—	—	—	—	—	—	—	—	—
53	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
54	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
55	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
56	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
57	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
58	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
59	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
60	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
61	L23	—	—	DDR3	M0DQS1	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
62	L22	—	—	DDR3	M0DQS1#	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
63	J23	—	—	DDR3	M0DM1	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
64	B19	—	—	DDR3	M0DQ16	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
65	C18	—	—	DDR3	M0DQ17	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
66	A21	—	—	DDR3	M0DQ18	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
67	D18	—	—	DDR3	M0DQ19	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
68	C21	—	—	DDR3	M0DQ20	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
69	A20	—	—	DDR3	M0DQ21	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
70	B18	—	—	DDR3	M0DQ22	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
71	B22	—	—	DDR3	M0DQ23	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
72	D20	—	—	DDR3	M0DQS2	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
73	C20	—	—	DDR3	M0DQS2#	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
74	B20	—	—	DDR3	M0DM2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
75	C19	—	—	DDR3	M0VREFDQ1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
76	D17	—	—	DDR3	M0DQ24	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
77	C17	—	—	DDR3	M0DQ25	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
78	D15	—	—	DDR3	M0DQ26	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
79	A17	—	—	DDR3	M0DQ27	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
80	A16	—	—	DDR3	M0DQ28	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
61	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
62	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
63	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
64	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
65	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
66	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
67	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
68	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
69	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
70	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
71	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
72	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
73	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
74	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
75	—	—	—	—	—	—	—	1.5V/2	VDDQ_M0/2	—	—	—	—	—	—	—	—	—	—
76	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
77	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
78	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
79	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
80	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
81	B15	—	—	DDR3	M0DQ29	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
82	B16	—	—	DDR3	M0DQ30	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
83	A15	—	—	DDR3	M0DQ31	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
84	D16	—	—	DDR3	M0DQS3	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
85	C16	—	—	DDR3	M0DQS3#	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
86	C15	—	—	DDR3	M0DM3	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
87	T24	—	—	DDR3	M0SDBUP	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
88	R15	—	—	PLL	VDD_CPGPLL0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
89	R16	—	—	PLL	VDD_CPGPLL0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
90	T15	—	—	PLL	VSS_CPGPLL0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
91	T16	—	—	PLL	VSS_CPGPLL0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
92	K16	—	—	PLL	VDD_CPGPLL1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
93	L16	—	—	PLL	VDD_CPGPLL1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
94	K15	—	—	PLL	VSS_CPGPLL1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
95	L15	—	—	PLL	VSS_CPGPLL1	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
96	N20	—	—	PLL	VDD_CPGPLL3	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
81	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
82	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
83	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
84	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
85	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
86	—	—	—	—	—	—	VDDQ_M0	1.5V	open	—	—	—	—	—	—	—	—	—	—
87	—	—	—	—	—	—	VDDQ_M0	1.5V	pullup	—	—	—	—	—	—	—	—	—	—
88	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
89	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
90	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
91	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
92	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
93	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
94	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
95	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
96	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
97	N21	—	—	PLL	VSS_CPGPLL3	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
98	AE22	—	—	CPG	EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
99	AE21	—	—	CPG	XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
100	AC21	—	—	RESET	PRESET#	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
101	AC20	—	—	RESET	PRESETOUT#	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
102	AB18	—	—	Power	BSMODE	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
103	AD19	—	—	Debug	TRST#	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
104	AC19	—	—	Debug	TCK	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
105	AD20	—	—	Debug	TMS	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
106	AD18	—	—	Debug	TDI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
107	AE19	—	—	Debug	TDO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
108	AE18	—	—	Debug	ACK	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
109	AE24	—	—	USB	USB_EXTAL	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
110	AE23	—	—	USB	USB_XTAL	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
111	AA24	—	—	USB	VCCQA_USB	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
112	V21	—	—	USB	VSSA_USB	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
113	V20	—	—	USB	VDDA_USBPLL	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
114	W21	—	—	USB	VSSA_USB	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
115	Y23	—	—	USB	VSSA_USB	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L		Pin condition after							
	Module	Pin Name	IO	Module	Pin Name	IO					Pin state	Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state	IO direction	Drivability	Pull-up control	Schmitt
97	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
98	—	—	—	—	—	—	VCCQ	3.3V	EXTAL	EXTAL	I	EXTAL	I	EXTAL	I	—	—	—	—
99	—	—	—	—	—	—	VCCQ	3.3V	open	XTAL	O	XTAL	O	XTAL	O	—	—	—	—
100	—	—	—	—	—	—	VCCQ	3.3V	PRESET#	PRESET#	I	PRESET#	I	PRESET#	I	I	—	—	schmitt
101	—	—	—	—	—	—	VCCQ	3.3V	open	PRESETOUT#	L	PRESETOUT# (*1)	H	PRESETOUT# (*1)	H	O	—	*	—
102	—	—	—	—	—	—	VCCQ	3.3V	VSS	BSMODE	I	BSMODE	I	BSMODE	I	I	—	—	schmitt
103	—	—	—	—	—	—	VCCQ18	1.8V	pulldown (1kΩ) or PRESET#	TRST#	I	TRST#	I	TRST#	I	I	—	pullup*	—
104	—	—	—	—	—	—	VCCQ18	1.8V	open	TCK	I	TCK	I	TCK	I	I	—	pullup*	—
105	—	—	—	—	—	—	VCCQ18	1.8V	open	TMS	I	TMS	I	TMS	I	IO	variable (initail 10)	pullup*	—
106	—	—	—	—	—	—	VCCQ18	1.8V	open	TDI	I	TDI	I	TDI	I	I	—	pullup*	—
107	—	—	—	—	—	—	VCCQ18	1.8V	open	TDO	O	TDO	O	TDO	O	IO	variable (initail 10)	*	—
108	—	—	—	—	—	—	VCCQ18	1.8V	open	ACK	I	ACK	I	ACK	I	IO	variable (initail 10)	pulldown *	—
109	—	—	—	—	—	—	VCCQ	3.3V	pulldown	USB_EXTAL	I	USB_EXTAL	I	USB_EXTAL	I	—	—	—	—
110	—	—	—	—	—	—	VCCQ	3.3V	open	USB_XTAL	O	USB_XTAL	O	USB_XTAL	O	—	—	—	—
111	—	—	—	—	—	—	VCCQA_USB	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
112	—	—	—	—	—	—	VSSA_USB	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
113	—	—	—	—	—	—	VDDA_USBPLL	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
114	—	—	—	—	—	—	VSSA_USB	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
115	—	—	—	—	—	—	VSSA_USB	0.0V	VSS	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
116	W20	—	—	USB	USB_REF	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
117	AB25	—	—	USB 2.0 ch0	USB0_DP	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
118	AB24	—	—	USB 2.0 ch0	USB0_DM	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
119	AA23	—	—	USB 2.0 ch0	USB0_VBUS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
120	AC25	—	—	USB 2.0 ch1	USB1_DP	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
121	AC24	—	—	USB 2.0 ch1	USB1_DM	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
122	AB23	—	—	USB 2.0 ch1	USB1_VBUS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
123	Y22	—	GP0_0	USB 2.0 ch0	USB0_PWEN	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
124	AA22	—	GP0_1	USB 2.0 ch0	USB0_OVC	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
125	AB21	—	GP0_2	USB 2.0 ch1	USB1_PWEN	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
126	AC22	—	GP0_3	USB 2.0 ch1	USB1_OVC	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
127	AB20	—	—	INTC	NMI	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
128	AE2	—	GP0_4	LBSC	CLKOUT	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
129	AA19	—	—	Power	VSS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
130	AA18	—	—	Power	VSS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L		Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO					Pin state	Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
116	—	—	—	—	—	—	—	—	pulldown	—	—	—	—	—	—	—	—	—	—
117	—	—	—	—	—	—	VCCQ	3.3V	VSS	—	—	—	—	—	—	—	—	—	—
118	—	—	—	—	—	—	VCCQ	3.3V	VSS	—	—	—	—	—	—	—	—	—	—
119	—	—	—	—	—	—	—	5.0V	VSS	—	—	—	—	—	—	—	—	—	—
120	—	—	—	—	—	—	VCCQ	3.3V	VSS	—	—	—	—	—	—	—	—	—	—
121	—	—	—	—	—	—	VCCQ	3.3V	VSS	—	—	—	—	—	—	—	—	—	—
122	—	—	—	—	—	—	—	5.0V	VSS	—	—	—	—	—	—	—	—	—	—
123	—	—	—	—	—	—	VCCQ	3.3V	open	USB0_PWEN	L	USB0_PWEN	L	USB0_PWEN	L	IO	—	*	—
124	—	—	—	—	—	—	VCCQ	3.3V	open	USB0_OVC	ZU	USB0_OVC	ZU	USB0_OVC	ZU	IO	—	pullup*	—
125	—	—	—	—	—	—	VCCQ	3.3V	open	USB1_PWEN	L	USB1_PWEN	L	USB1_PWEN	L	IO	—	*	—
126	—	—	—	—	—	—	VCCQ	3.3V	open	USB1_OVC	ZU	USB1_OVC	ZU	USB1_OVC	ZU	IO	—	pullup*	—
127	—	—	—	—	—	—	VCCQ	3.3V	NMI	NMI	I	NMI	I	NMI	I	I	—	*	—
128	—	—	—	—	—	—	VCCQ	3.3V	open	CLKOUT	O	CLKOUT	O	CLKOUT	O	IO	—	*	—
129	—	—	—	—	—	—	VSS	0.0V	VSS	TEST1	I	TEST1	I	TEST1	I	I	—	—	schmitt
130	—	—	—	—	—	—	VSS	0.0V	VSS	TEST2	I	TEST2	I	TEST2	I	I	—	—	schmitt

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
131	AA20	—	—	Power	VSS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
132	AC18	—	—	Power	VSS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
133	AB19	—	—	Power	VSS	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
134	E13	—	—	SDHI0 Power	VCCQ_SD0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
135	A13	—	GP0_5	SDHI0	SD0_CLK	O	—	—	—	—	—	—	SSI1	SSI_SCK1_C	IO	SCIF3	RX3_C	I	—	—	—
136	D13	—	GP0_6	SDHI0	SD0_CMD	IO	—	—	—	—	—	—	SSI1	SSI_WS1_C	IO	SCIF3	TX3_C	O	—	—	—
137	B13	—	GP0_7	SDHI0	SD0_DAT0	IO	—	—	—	—	—	—	SSI1	SSI_SDATA1_C	IO	SCIF4	RX4_E	I	—	—	—
138	D14	—	GP0_8	SDHI0	SD0_DAT1	IO	—	—	—	—	—	—	SSI0	SSI_SCK0129_B	IO	SCIF4	TX4_E	O	—	—	—
139	C14	—	GP0_9	SDHI0	SD0_DAT2	IO	—	—	—	—	—	—	SSI0	SSI_WS0129_B	IO	SCIF5	RX5_E	I	—	—	—
140	B14	—	GP0_10	SDHI0	SD0_DAT3	IO	—	—	—	—	—	—	SSI0	SSI_SDATA0_B	IO	SCIF5	TX5_E	O	—	—	—
141	A8	—	GP0_11	SDHI0	SD0_CD	I	—	—	—	RCAN0	CAN0_RX_A	I	—	—	—	—	—	—	—	—	—
142	B8	—	GP0_12	SDHI0	SD0_WP	I	INTC	IRQ7	I	RCAN0	CAN0_TX_A	O	—	—	—	—	—	—	—	—	—
143	E11	—	—	MMC Power	VCCQ_MMC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
144	A10	—	GP0_13	MMC	MMC0_CLK	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L		Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO					Pin state	Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
131	—	—	—	—	—	—	VSS	0.0V	VSS	TESTCLK	I	TESTCLK	I	TESTCLK	I	I	—	—	schmitt
132	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
133	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
134	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	VCCQ_SD0	—	—	—	—	—	—	—	—	—	—
135	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
136	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
137	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
138	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
139	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
140	—	—	—	—	—	—	VCCQ_SD0	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
141	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
142	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
143	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	VCCQ_MMC	—	—	—	—	—	—	—	—	—	—
144	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO/TDO2(*3)	Z	GPIO/TDO2(*3)	Z	GPIO/TDO2(*3)	Z	IO	variable (initail 10)	*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
145	B10	—	GP0_14	MMC	MMC0_CMD	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
146	D11	—	GP0_15	MMC	MMC0_D0	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
147	B11	—	GP0_16	MMC	MMC0_D1	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
148	A11	—	GP0_17	MMC	MMC0_D2	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
149	D12	—	GP0_18	MMC	MMC0_D3	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
150	C12	—	GP0_19	MMC	MMC0_D4	IO	SDHI1	SD1_CD	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
151	B12	—	GP0_20	MMC	MMC0_D5	IO	SDHI1	SD1_WP	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
152	A12	—	GP0_21	MMC	MMC0_D6	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
153	C13	—	GP0_22	MMC	MMC0_D7	IO	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
154	AD2	—	GP1_0	LBSC	D0	IO	—	Reserved	—	I2C3	SCL3_B	IO	SCIF5	RX5_B	I	INTC	IRQ4	I	MSIOF2	MSIOF2_RXD_C	I			

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
145	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO/TRST2# (*3)	Z	GPIO/TRST2# (*3)	Z	GPIO/TRST2# (*3)	Z	IO	variable (initail 10)	*/—(*4)	—
146	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO/TCK2(*3)	Z	GPIO/TCK2(*3)	Z	GPIO/TCK2(*3)	Z	IO	variable (initail 10)	*/—(*4)	—
147	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO/TMS2(*3)	Z	GPIO/TMS2(*3)	Z	GPIO/TMS2(*3)	Z	IO	variable (initail 10)	*/—(*4)	—
148	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO/TDI2(*3)	Z	GPIO/TDI2(*3)	Z	GPIO/TDI2(*3)	Z	IO	variable (initail 10)	*/—(*4)	—
149	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO (*3)	Z	GPIO (*3)	Z	GPIO (*3)	Z	IO	variable (initail 10)	*/—(*4)	—
150	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
151	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
152	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
153	—	—	—	—	—	—	VCCQ_MMC	1.8V/3.3V	pullup or pulldown	GPIO	Z	GPIO	Z	GPIO	Z	IO	variable (initail 10)	*	—
154	SSI5	SSI_SDATA5_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D0	ZU	GPIO	ZU	IO	—	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
155	AD1	—	GP1_1	LBSC	D1	IO	—	Reserved	—	I2C3	SDA3_B	IO	SCIF5	TX5_B	O	—	—	—	MSIOF2	MSIOF2_TXD_C	O
156	AC2	—	GP1_2	LBSC	D2	IO	—	Reserved	—	SCIF4	RX4_B	I	I2C0	SCL0_D	IO	PWM1	PWM1_C	O	MSIOF2	MSIOF2_SCK_C	IO
157	AC1	—	GP1_3	LBSC	D3	IO	—	Reserved	—	SCIF4	TX4_B	O	I2C0	SDA0_D	IO	PWM0	PWM0_A	O	MSIOF2	MSIOF2_SYNC_C	IO
158	AB3	—	GP1_4	LBSC	D4	IO	—	—	—	INTC	IRQ3	I	TMU	TCLK1_A	I	PWM6	PWM6_C	O	—	Reserved	—
159	AB2	—	GP1_5	LBSC	D5	IO	HSCIF2	HRX2	I	I2C1	SCL1_B	IO	PWM2	PWM2_C	O	TMU	TCLK2_B	I	—	Reserved	—
160	AB1	—	GP1_6	LBSC	D6	IO	HSCIF2	HTX2	O	I2C1	SDA1_B	IO	PWM4	PWM4_C	O	—	—	—	—	Reserved	—
161	AA4	—	GP1_7	LBSC	D7	IO	HSCIF2	HSCK2	IO	SCIF1	SCIF1_SCK_C	IO	INTC	IRQ6	I	PWM5	PWM5_C	O	—	Reserved	—
162	AA3	—	GP1_8	LBSC	D8	IO	HSCIF2	HCTS2#	IO	SCIF1	RX1_C	I	I2C1	SCL1_D	IO	PWM3	PWM3_C	O	—	—	—
163	AA2	—	GP1_9	LBSC	D9	IO	HSCIF2	HRTS2#	IO	SCIF1	TX1_C	O	I2C1	SDA1_D	IO	—	—	—	—	—	—
164	AA1	—	GP1_10	LBSC	D10	IO	MSIOF2	MSIOF2_RXD_A	I	HSCIF0	HRX0_B	I	—	—	—	—	—	—	—	—	—
165	Y5	—	GP1_11	LBSC	D11	IO	MSIOF2	MSIOF2_TXD_A	O	HSCIF0	HTX0_B	O	—	—	—	—	—	—	—	—	—
166	Y4	—	GP1_12	LBSC	D12	IO	MSIOF2	MSIOF2_SCK_A	IO	HSCIF0	HSCK0	IO	—	—	—	RCAN	CAN_CLK_C	I	—	—	—
167	Y3	—	GP1_13	LBSC	D13	IO	MSIOF2	MSIOF2_SYNC_A	IO	—	—	—	SCIF4	RX4_C	I	—	—	—	—	—	—
168	Y2	—	GP1_14	LBSC	D14	IO	MSIOF2	MSIOF2_SS1	O	—	—	—	SCIF4	TX4_C	O	RCAN1	CAN1_RX_B	I	—	—	—
169	Y1	—	GP1_15	LBSC	D15	IO	MSIOF2	MSIOF2_SS2	O	PWM4	PWM4_A	O	—	—	—	RCAN1	CAN1_TX_B	O	INTC	IRQ2	I
170	AE4	—	GP1_16	QSPI0	QSPI0_SPCLK	IO	LBSC	WE0#	O	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
155	SSI5	SSI_WS5_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D1	ZU	GPIO	ZU	IO	—	pullup*	—
156	SSI5	SSI_SCK5_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D2	ZU	GPIO	ZU	IO	—	pullup*	—
157	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D3	ZU	GPIO	ZU	IO	—	pullup*	—
158	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D4	ZU	GPIO	ZU	IO	—	pullup*	—
159	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D5	ZU	GPIO	ZU	IO	—	pullup*	—
160	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D6	ZU	GPIO	ZU	IO	—	pullup*	—
161	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D7	ZU	GPIO	ZU	IO	—	pullup*	—
162	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D8	ZU	GPIO	ZU	IO	—	pullup*	—
163	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D9	ZU	GPIO	ZU	IO	—	pullup*	—
164	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D10	ZU	GPIO	ZU	IO	—	pullup*	—
165	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D11	ZU	GPIO	ZU	IO	—	pullup*	—
166	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D12	ZU	GPIO	ZU	IO	—	pullup*	—
167	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D13	ZU	GPIO	ZU	IO	—	pullup*	—
168	EtherAVB	AVB_AVTP_CAPTURE_A	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D14	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
169	EtherAVB	AVB_AVTP_MATCH_A	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	D15	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
170	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	WE0#	H	GPIO	ZU	IO	—	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
171	AD4	—	GP1_17	QSPI0	QSPI0_MOSI/QSPI0_IO0	IO	LBSC	BS#	O	—	—	—	—	—	—	—	—	—	—	—	—
172	AC4	—	GP1_18	QSPI0	QSPI0_MISO/QSPI0_IO1	IO	LBSC	RD/WR#	O	—	—	—	—	—	—	—	—	—	—	—	—
173	AD5	—	GP1_19	QSPI0	QSPI0_IO2	IO	LBSC	CS0#	O	—	—	—	—	—	—	—	—	—	—	—	—
174	AC5	—	GP1_20	QSPI0	QSPI0_IO3	IO	LBSC	RD#	O	—	—	—	—	—	—	—	—	—	—	—	—
175	AD3	—	GP1_21	QSPI0	QSPI0_SSL	IO	LBSC	WE1#	O	—	—	—	—	—	—	—	—	—	—	—	—
176	AE3	—	GP1_22	LBSC	EX_WAIT0	I	RCAN	CAN_CLK_B	I	SCIF	SCIF_CLK_A	I	—	—	—	—	—	—	—	—	—
177	AB5	—	GP2_0	DU0	DU0_DR0	O	—	Reserved	—	SCIF5	RX5_C	I	I2C2	SCL2_D	IO	—	—	—	—	—	—
178	AE6	—	GP2_1	DU0	DU0_DR1	O	—	Reserved	—	SCIF5	TX5_C	O	I2C2	SDA2_D	IO	—	—	—	—	—	—
179	AD6	—	GP2_2	DU0	DU0_DR2	O	—	Reserved	—	SCIF0	RX0_D	I	I2C0	SCL0_E	IO	—	—	—	—	—	—
180	AC6	—	GP2_3	DU0	DU0_DR3	O	—	Reserved	—	SCIF0	TX0_D	O	I2C0	SDA0_E	IO	PWM0	PWM0_B	O	—	—	—
181	AB6	MD0	GP2_4	DU0	DU0_DR4	O	—	Reserved	—	SCIF1	RX1_D	I	—	—	—	—	—	—	—	—	—
182	AE7	MD1	GP2_5	DU0	DU0_DR5	O	—	Reserved	—	SCIF1	TX1_D	O	—	—	—	PWM1	PWM1_B	O	—	—	—
183	AD7	MD2	GP2_6	DU0	DU0_DR6	O	—	Reserved	—	SCIF2	RX2_C	I	—	—	—	—	—	—	—	—	—
184	AC7	MD3	GP2_7	DU0	DU0_DR7	O	—	Reserved	—	SCIF2	TX2_C	O	—	—	—	PWM2	PWM2_B	O	—	—	—
185	AB7	—	GP2_8	DU0	DU0_DG0	O	—	Reserved	—	SCIF3	RX3_B	I	I2C3	SCL3_D	IO	—	—	—	—	—	—
186	AA7	—	GP2_9	DU0	DU0_DG1	O	—	Reserved	—	SCIF3	TX3_B	O	I2C3	SDA3_D	IO	PWM3	PWM3_B	O	—	—	—
187	AE8	MD4	GP2_10	DU0	DU0_DG2	O	—	Reserved	—	SCIF4	RX4_D	I	—	—	—	—	—	—	—	—	—
188	AD8	MD5	GP2_11	DU0	DU0_DG3	O	—	Reserved	—	SCIF4	TX4_D	O	—	—	—	PWM4	PWM4_B	O	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
171	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	BS#	H	GPIO	ZU	IO	—	pullup*	—
172	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	RD/WR#	H	GPIO	ZU	IO	—	pullup*	—
173	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	CS0#	ZU	GPIO	ZU	IO	—	pullup*	—
174	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	RD#	H	GPIO	ZU	IO	—	pullup*	—
175	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	WE1#	H	GPIO	ZU	IO	—	pullup*	—
176	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	EX_WAIT0	I	GPIO	ZU	IO	—	pullup*	—
177	LBSC	A0	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A0	L	GPIO	ZU	IO	—	pullup*	—
178	LBSC	A1	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A1	L	GPIO	ZU	IO	—	pullup*	—
179	LBSC	A2	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A2	L	GPIO	ZU	IO	—	pullup*	—
180	LBSC	A3	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A3	L	GPIO	ZU	IO	—	pullup*	—
181	LBSC	A4	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD0	I	A4	L	GPIO	Z	IO	—	*	—
182	LBSC	A5	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD1	I	A5	L	GPIO	Z	IO	—	*	—
183	LBSC	A6	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD2	I	A6	L	GPIO	Z	IO	—	*	—
184	LBSC	A7	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD3	I	A7	L	GPIO	Z	IO	—	*	—
185	LBSC	A8	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A8	L	GPIO	ZU	IO	—	pullup*	—
186	LBSC	A9	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A9	L	GPIO	ZU	IO	—	pullup*	—
187	LBSC	A10	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD4	I	A10	L	GPIO	Z	IO	—	*	—
188	LBSC	A11	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD5	I	A11	L	GPIO	Z	IO	—	*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
189	AC8	MD6	GP2_12	DU0	DU0_DG4	O	—	Reserved	—	HSCIF0	HRX0_A	I	—	—	—	—	—	—	—	—	—
190	AB8	MD7	GP2_13	DU0	DU0_DG5	O	—	Reserved	—	HSCIF0	HTX0_A	O	—	—	—	PWM5	PWM5_B	O	—	—	—
191	AE9	MD8	GP2_14	DU0	DU0_DG6	O	—	Reserved	—	HSCIF1	HRX1_C	I	—	—	—	—	—	—	—	—	—
192	AD9	MD9	GP2_15	DU0	DU0_DG7	O	—	Reserved	—	HSCIF1	HTX1_C	O	—	—	—	PWM6	PWM6_B	O	—	—	—
193	AC9	—	GP2_16	DU0	DU0_DB0	O	—	Reserved	—	—	—	—	I2C4	SCL4_D	IO	RCAN0	CAN0_RX_C	I	—	—	—
194	AB9	—	GP2_17	DU0	DU0_DB1	O	—	Reserved	—	—	—	—	I2C4	SDA4_D	IO	RCAN0	CAN0_TX_C	O	—	—	—
195	AA9	MD10	GP2_18	DU0	DU0_DB2	O	—	Reserved	—	HSCIF0	HCTS0#	IO	—	—	—	—	—	—	—	—	—
196	AE10	MD11	GP2_19	DU0	DU0_DB3	O	—	Reserved	—	HSCIF0	HRTS0#	IO	—	—	—	—	—	—	—	—	—
197	AD10	—	GP2_20	DU0	DU0_DB4	O	—	Reserved	—	HSCIF1	HCTS1#_C	IO	—	Reserved	—	—	—	—	—	—	—
198	AC10	—	GP2_21	DU0	DU0_DB5	O	—	Reserved	—	HSCIF1	HRTS1#_C	IO	—	Reserved	—	—	—	—	—	—	—
199	AB10	MD13	GP2_22	DU0	DU0_DB6	O	—	Reserved	—	—	—	—	—	Reserved	—	—	—	—	—	—	—
200	AD11	MD14	GP2_23	DU0	DU0_DB7	O	—	Reserved	—	—	—	—	—	Reserved	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
189	LBSC	A12	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD6	I	A12	L	GPIO	Z	IO	—	*	—
190	LBSC	A13	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD7	I	A13	L	GPIO	Z	IO	—	*	—
191	LBSC	A14	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD8	I	A14	L	GPIO	Z	IO	—	*	—
192	LBSC	A15	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD9	I	A15	L	GPIO	Z	IO	—	*	—
193	LBSC	A16	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A16	L	GPIO	ZU	IO	—	pullup*	—
194	LBSC	A17	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A17	L	GPIO	ZU	IO	—	pullup*	—
195	LBSC	A18	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD10	I	A18	L	GPIO	Z	IO	—	*	—
196	LBSC	A19	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD11	I	A19	L	GPIO	Z	IO	—	*	—
197	LBSC	A20	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A20	L	GPIO	ZU	IO	—	pullup*	—
198	LBSC	A21	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A21	L	GPIO	ZU	IO	—	pullup*	—
199	LBSC	A22	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD13	I	A22	L	GPIO	Z	IO	—	*	—
200	LBSC	A23	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD14	I	A23	L	GPIO	Z	IO	—	*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
201	AE11	—	GP2_24	DU0	DU0_DOTCLKIN	I	—	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—
202	AC11	—	GP2_25	DU0	DU0_DOTCLKOUT0	O	—	Reserved	—	—	—	—	—	—	—	—	—	—	—	—	—
203	AB11	—	GP2_26	DU0	DU0_DOTCLKOUT1	O	—	Reserved	—	MSIOF2	MSIOF2_RXD_B	I	—	—	—	—	—	—	—	—	—
204	AC12	MD20	GP2_27	DU0	DU0_EXHSYNC/DU0_HSYNC	IO	—	Reserved	—	MSIOF2	MSIOF2_TXD_B	O	—	—	—	—	—	—	—	—	—
205	AB12	MD21	GP2_28	DU0	DU0_EXVSYNC/DU0_VSYNC	IO	—	Reserved	—	MSIOF2	MSIOF2_SYNC_B	IO	—	—	—	—	—	—	—	—	—
206	AD12	—	GP2_29	DU0	DU0_EXODDF/DU0_ODDF_DISP_CDE	IO	—	Reserved	—	MSIOF2	MSIOF2_SCK_B	IO	—	—	—	—	—	—	—	—	—
207	AE12	MDT0	GP2_30	DU0	DU0_DISP	O	—	Reserved	—	—	—	—	—	—	—	RCAN1	CAN1_RX_C	I	—	—	—
208	AA11	MDT1	GP2_31	DU0	DU0_CDE	O	—	Reserved	—	—	—	—	—	—	—	RCAN1	CAN1_TX_C	O	—	—	—
209	R1	—	GP3_0	VIN1	VI1_CLK	I	—	—	—	—	—	—	—	—	—	EtherAVB	AVB_RX_CLK	I	EtherMAC	ETH_REF_CLK	IO
210	R3	—	GP3_1	VIN1	VI1_DATA0	I	—	—	—	—	—	—	—	—	—	EtherAVB	AVB_RX_DV	I	EtherMAC	ETH_CRS_DV	I
211	R4	—	GP3_2	VIN1	VI1_DATA1	I	—	—	—	—	—	—	—	—	—	EtherAVB	AVB_RXD0	I	EtherMAC	ETH_RXD0	I
212	R5	—	GP3_3	VIN1	VI1_DATA2	I	—	—	—	—	—	—	—	—	—	EtherAVB	AVB_RXD1	I	EtherMAC	ETH_RXD1	I

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
201	LBSC	A24	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A24	L	GPIO	ZU	IO	—	pullup*	—
202	LBSC	A25	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	A25	L	GPIO	ZU	IO	variable (initail 10)	pullup*	—
203	LBSC	CS1#/A26	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	CS1#/A26(*2)	H/L	GPIO	ZU	IO	variable (initail 10)	pullup*	—
204	LBSC	DREQ0#	I	—	—	—	VCCQ	3.3V	pullup or pulldown	MD20	I	GPIO	Z	GPIO	Z	IO	—	*	—
205	LBSC	DACK0	O	—	—	—	VCCQ	3.3V	pullup or pulldown	MD21	I	GPIO	Z	GPIO	Z	IO	—	*	—
206	LBSC	DRACK0	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
207	—	—	—	—	—	—	VCCQ	3.3V	pullup or pulldown	MDT0	I	GPIO	Z	GPIO	Z	IO	—	*	—
208	—	—	—	—	—	—	VCCQ	3.3V	pullup or pulldown	MDT1	I	GPIO	Z	GPIO	Z	IO	—	*	—
209	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
210	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
211	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
212	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
213	P1	—	GP3_4	VIN1	VI1_DATA3	I	—	—	—	—	—	—	—	—	—	Ether AVB	AVB_RXD2	I	Ether MAC	ETH_MDIO	I
214	P2	—	GP3_5	VIN1	VI1_DATA4	I	—	—	—	—	—	—	—	—	—	Ether AVB	AVB_RXD3	I	Ether MAC	ETH_RX_ER	I
215	P3	—	GP3_6	VIN1	VI1_DATA5	I	—	—	—	—	—	—	—	—	—	Ether AVB	AVB_RXD4	I	Ether MAC	ETH_LINK	I
216	P4	—	GP3_7	VIN1	VI1_DATA6	I	—	—	—	—	—	—	—	—	—	Ether AVB	AVB_RXD5	I	Ether MAC	ETH_TXD1	O
217	N1	—	GP3_8	VIN1	VI1_DATA7	I	—	—	—	—	—	—	—	—	—	Ether AVB	AVB_RXD6	I	Ether MAC	ETH_TX_EN	O
218	N2	—	GP3_9	VIN1	VI1_CLKENB	I	I2C3	SCL3_A	IO	—	—	—	—	—	—	Ether AVB	AVB_RXD7	I	Ether MAC	ETH_MAGIC	O
219	N3	—	GP3_10	VIN1	VI1_FIELD	I	I2C3	SDA3_A	IO	—	—	—	—	—	—	Ether AVB	AVB_RX_ER	I	Ether MAC	ETH_TXD0	O
220	N4	—	GP3_11	VIN1	VI1_HSYNC#	I	SCIF0	RX0_B	I	I2C0	SCL0_C	IO	—	—	—	Ether AVB	AVB_GTXREFCLK	I	Ether MAC	ETH_MDC	O
221	M4	—	GP3_12	VIN1	VI1_VSYNC#	I	SCIF0	TX0_B	O	I2C0	SDA0_C	IO	ADG	AUDIO_CLKOUT_B	O	Ether AVB	AVB_TX_CLK	O	—	—	—
222	M1	—	GP3_13	VIN1	VI1_DATA8	I	—	—	—	—	—	—	I2C2	SCL2_B	IO	Ether AVB	AVB_TX_EN	I	—	—	—
223	M2	—	GP3_14	VIN1	VI1_DATA9	I	—	—	—	—	—	—	I2C2	SDA2_B	IO	Ether AVB	AVB_TXD0	O	—	—	—
224	M3	—	GP3_15	VIN1	VI1_DATA10	I	—	—	—	—	—	—	RCAN0	CAN0_RX_B	I	Ether AVB	AVB_TXD1	O	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
213	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
214	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
215	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
216	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
217	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
218	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
219	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
220	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
221	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
222	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
223	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
224	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
225	L1	—	GP3_16	VIN1	VI1_DATA11	I	—	—	—	—	—	—	RCAN0	CAN0_TX_B	O	EtherAVB	AVB_TXD2	O	—	—	—
226	L2	—	GP3_27	EtherAVB	AVB_TXD3	O	—	—	—	ADGA	AUDIO_CLKA_B	I	—	—	—	SSI1	SSI_SCK1_D	IO	SCIF5	RX5_F	I
227	L3	—	GP3_28	EtherAVB	AVB_TXD4	O	—	—	—	ADGB	AUDIO_CLKB_B	I	—	—	—	SSI1	SSI_WS1_D	IO	SCIF5	TX5_F	O
228	L4	—	GP3_29	EtherAVB	AVB_TXD5	O	SCIF	SCIF_CLK_B	I	ADGC	AUDIO_CLKC_B	I	—	—	—	SSI1	SSI_SDATA1_D	IO	—	—	—
229	K4	—	GP4_0	I2C0	SCL0_A	IO	SCIF0	RX0_C	I	PWM5	PWM5_A	O	TMU	TCLK1_B	I	EtherAVB	AVB_TXD6	O	RCAN1	CAN1_RX_D	I
230	L5	—	GP4_1	I2C0	SDA0_A	IO	SCIF0	TX0_C	O	INTC	IRQ5	I	RCAN	CAN_CLK_A	I	EtherAVB	AVB_GTX_CLK	O	RCAN1	CAN1_TX_D	O
231	C5	—	GP4_2	I2C1	SCL1_A	IO	SCIF4	RX4_A	I	PWM5	PWM5_D	O	DU1	DU1_DR0	O	—	—	—	—	—	—
232	D5	—	GP4_3	I2C1	SDA1_A	IO	SCIF4	TX4_A	O	—	—	—	DU1	DU1_DR1	O	—	—	—	—	—	—
233	A6	—	GP4_4	MSIOF0	MSIOF0_RXD_A	I	SCIF5	RX5_A	I	I2C2	SCL2_C	IO	DU1	DU1_DR2	O	—	—	—	QSPI1	QSPI1_MOSI/QSPI1_IO0	IO
234	B6	—	GP4_5	MSIOF0	MSIOF0_TXD_A	O	SCIF5	TX5_A	O	I2C2	SDA2_C	IO	DU1	DU1_DR3	O	—	—	—	QSPI1	QSPI1_MISO/QSPI1_IO1	IO
235	A5	—	GP4_6	MSIOF0	MSIOF0_SCK_A	IO	INTC	IRQ0	I	—	Reserved	—	DU1	DU1_DR4	O	—	Reserved	—	QSPI1	QSPI1_SPCLK	IO
236	B5	—	GP4_7	MSIOF0	MSIOF0_SYNC_A	IO	PWM1	PWM1_A	O	—	Reserved	—	DU1	DU1_DR5	O	—	Reserved	—	QSPI1	QSPI1_IO2	IO
237	C6	—	GP4_8	MSIOF0	MSIOF0_SS1_A	O	—	—	—	—	Reserved	—	DU1	DU1_DR6	O	—	Reserved	—	QSPI1	QSPI1_IO3	IO
238	D6	—	GP4_9	MSIOF0	MSIOF0_SS2_A	O	—	—	—	—	Reserved	—	DU1	DU1_DR7	O	—	Reserved	—	QSPI1	QSPI1_SSL	IO

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
225	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
226	MSIOF0	MSIOF0_RXD_B	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
227	MSIOF0	MSIOF0_TXD_B	O	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
228	MSIOF0	MSIOF0_SCK_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
229	MSIOF0	MSIOF0_SYNC_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
230	SCU	DVC_MUTE	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
231	SSI6	SSI_SCK6_B	IO	VIN0	VI0_G0	I	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
232	SSI6	SSI_WS6_B	IO	VIN0	VI0_G1	I	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
233	SSI6	SSI_SDATA6_B	IO	VIN0	VI0_G2	I	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
234	SSI7	SSI_WS78_B	IO	VIN0	VI0_G3	I	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
235	SSI7	SSI_SCK78_B	IO	VIN0	VI0_G4	I	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
236	SSI7	SSI_SDATA7_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
237	SSI8	SSI_SDATA8_B	IO	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
238	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
239	A7	—	GP4_10	HSCIF1	HRX1_A	I	I2C4	SCL4_A	IO	PWM6	PWM6_A	O	DU1	DU1_DG0	O	SCIF0	RX0_A	I	—	—	—
240	B7	—	GP4_11	HSCIF1	HTX1_A	O	I2C4	SDA4_A	IO	—	—	—	DU1	DU1_DG1	O	SCIF0	TX0_A	O	—	—	—
241	E8	—	GP4_12	HSCIF1	HCTS1#_A	IO	PWM2	PWM2_A	O	—	—	—	DU1	DU1_DG2	O	REMOCON	REMOCON_B	I	—	—	—
242	D7	—	GP4_13	HSCIF1	HRTS1#_A	IO	—	—	—	—	—	—	DU1	DU1_DG3	O	SSI1	SSI_WS1_B	IO	INTC	IRQ1	I
243	E10	—	—	SDHI2 Power	VCCQ_SD2	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
244	A9	—	GP4_14	SDHI2	SD2_CLK	O	HSCIF1	HSCK1	IO	—	—	—	DU1	DU1_DG4	O	SSI1	SSI_SCK1_B	IO	—	—	—
245	D9	—	GP4_15	SDHI2	SD2_CMD	IO	SCIF1	SCIF1_SCK_A	IO	TMU	TCLK2_A	I	DU1	DU1_DG5	O	SSI2	SSI_SCK2_B	IO	PWM3	PWM3_A	O
246	C9	—	GP4_16	SDHI2	SD2_DAT0	IO	SCIF1	RX1_A	I	I2C1	SCL1_E	IO	DU1	DU1_DG6	O	SSI1	SSI_SDATA1_B	IO	—	—	—
247	B9	—	GP4_17	SDHI2	SD2_DAT1	IO	SCIF1	TX1_A	O	I2C1	SDA1_E	IO	DU1	DU1_DG7	O	SSI2	SSI_WS2_B	IO	—	—	—
248	D10	—	GP4_18	SDHI2	SD2_DAT2	IO	SCIF2	RX2_A	I	—	—	—	DU1	DU1_DB0	O	SSI2	SSI_SDATA2_B	IO	—	—	—
249	C10	—	GP4_19	SDHI2	SD2_DAT3	IO	SCIF2	TX2_A	O	—	—	—	DU1	DU1_DB1	O	SSI9	SSI_WS9_B	IO	—	—	—
250	C8	—	GP4_20	SDHI2	SD2_CD	I	SCIF2	SCIF2_SCK_A	IO	—	—	—	DU1	DU1_DB2	O	SSI9	SSI_SCK9_B	IO	—	—	—
251	D8	—	GP4_21	SDHI2	SD2_WP	I	SCIF3	SCIF3_SCK	IO	—	—	—	DU1	DU1_DB3	O	SSI9	SSI_SDATA9_B	IO	—	—	—
252	B3	—	GP4_22	SCIF3	RX3_A	I	I2C1	SCL1_C	IO	MSIOF1	MSIOF1_RXD_B	I	DU1	DU1_DB4	O	ADGA	AUDIO_CLKA_C	I	SSI4	SSI_SDATA4_B	IO
253	A4	—	GP4_23	SCIF3	TX3_A	O	I2C1	SDA1_C	IO	MSIOF1	MSIOF1_TXD_B	O	DU1	DU1_DB5	O	ADGB	AUDIO_CLKB_C	I	SSI4	SSI_WS4_B	IO
254	B4	—	GP4_24	I2C2	SCL2_A	IO	—	—	—	MSIOF1	MSIOF1_SCK_B	IO	DU1	DU1_DB6	O	ADGC	AUDIO_CLKC_C	I	SSI4	SSI_SCK4_B	IO

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
239	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
240	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
241	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
242	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
243	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	VCCQ_SD2	—	—	—	—	—	—	—	—	—	—
244	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	pullup or pulldown	GPIO/TDO3(*3)	Z	GPIO/TDO3(*3)	Z	GPIO/TDO3(*3)	Z	IO	variable (initail 10)	*	—
245	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	pullup or pulldown	GPIO/TRST3# (*3)	Z	GPIO/TRST3# (*3)	Z	GPIO/TRST3# (*3)	Z	IO	variable (initail 10)	*/—(*4)	—
246	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	pullup or pulldown	GPIO/TCK3(*3)	Z	GPIO/TCK3(*3)	Z	GPIO/TCK3(*3)	Z	IO	variable (initail 10)	*/—(*4)	—
247	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	pullup or pulldown	GPIO/TMS3(*3)	Z	GPIO/TMS3(*3)	Z	GPIO/TMS3(*3)	Z	IO	variable (initail 10)	*/—(*4)	—
248	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	pullup or pulldown	GPIO/TDI3(*3)	Z	GPIO/TDI3(*3)	Z	GPIO/TDI3(*3)	Z	IO	variable (initail 10)	*/—(*4)	—
249	—	—	—	—	—	—	VCCQ_SD2	1.8V/3.3V	pullup or pulldown	GPIO (*3)	Z	GPIO (*3)	Z	GPIO (*3)	Z	IO	variable (initail 10)	*/—(*4)	—
250	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
251	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
252	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
253	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
254	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
255	C4	—	GP4_25	I2C2	SDA2_A	IO	—	—	—	MSIOF1	MSIOF1_SYNC_B	IO	DU1	DU1_DB7	O	ADG	AUDIO_CLKOUT_C	O	—	—	—
256	A3	—	GP5_0	SSI5	SSI_SCK5_A	IO	—	—	—	—	—	—	DU1	DU1_DOTCLKOUT1	O	—	—	—	—	—	—
257	A2	—	GP5_1	SSI5	SSI_WS5_A	IO	—	—	—	I2C3	SCL3_C	IO	DU1	DU1_DOTCLKIN	I	—	—	—	—	—	—
258	B2	—	GP5_2	SSI5	SSI_SDATA5_A	IO	—	—	—	I2C3	SDA3_C	IO	DU1	DU1_DOTCLKOUT0	O	—	—	—	—	—	—
259	B1	—	GP5_3	SSI6	SSI_SCK6_A	IO	—	—	—	—	—	—	DU1	DU1_EXODDF/DU1_ODDF_DISP_CDE	IO	—	—	—	—	—	—
260	C2	—	GP5_4	SSI6	SSI_WS6_A	IO	—	—	—	I2C4	SCL4_C	IO	DU1	DU1_EXHSYNC/DU1_HSYNC	IO	—	—	—	—	—	—
261	C1	—	GP5_5	SSI6	SSI_SDATA6_A	IO	—	—	—	I2C4	SDA4_C	IO	DU1	DU1_EXVSYNC/DU1_VSYNC	IO	—	—	—	—	—	—
262	D3	—	GP5_6	SSI7	SSI_SCK78_A	IO	—	—	—	I2C4	SDA4_E	IO	DU1	DU1_DISP	O	—	—	—	—	—	—
263	D2	—	GP5_7	SSI7	SSI_WS78_A	IO	—	—	—	I2C4	SCL4_E	IO	DU1	DU1_CDE	O	—	—	—	—	—	—
264	F5	—	GP5_8	SSI7	SSI_SDATA7_A	IO	—	—	—	—	—	—	INTC	IRQ8	I	ADGA	AUDIO_CLKA_D	I	RCAN	CAN_CLK_D	I
265	G2	—	GP5_9	SSI0	SSI_SCK0129_A	IO	MSIOF1	MSIOF1_RXD_A	I	SCIF5	RX5_D	I	—	—	—	—	—	—	—	—	—
266	G1	—	GP5_10	SSI0	SSI_WS0129_A	IO	MSIOF1	MSIOF1_TXD_A	O	SCIF5	TX5_D	O	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
255	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
256	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
257	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
258	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
259	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
260	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
261	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
262	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
263	—	—	—	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
264	VIN0	VI0_G5	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
265	VIN0	VI0_G6	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
266	VIN0	VI0_G7	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI		
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
267	H4	—	GP5_11	SSI0	SSI_SDATA0_A	IO	MSIOF1	MSIOF1_SYNC_A	IO	PWM0	PWM0_C	O	—	—	—	—	—	—	—	—	—
268	F3	—	GP5_12	SSI3	SSI_SCK34	IO	MSIOF1	MSIOF1_SCK_A	IO	EtherAVB	AVB_MDC	O	—	—	—	—	—	—	LBSC	DACK1	O
269	F2	—	GP5_13	SSI3	SSI_WS34	IO	MSIOF1	MSIOF1_SS1_A	O	EtherAVB	AVB_MDIO	IO	—	—	—	RCAN1	CAN1_RX_A	I	LBSC	DREQ1#	I
270	F1	—	GP5_14	SSI3	SSI_SDATA3	IO	MSIOF1	MSIOF1_SS2_A	O	EtherAVB	AVB_LINK	I	—	—	—	RCAN1	CAN1_TX_A	O	LBSC	DREQ2#	I
271	G4	—	GP5_15	SSI4	SSI_SCK4_A	IO	—	—	—	EtherAVB	AVB_MAGIC	O	—	—	—	—	—	—	—	—	—
272	G5	—	GP5_16	SSI4	SSI_WS4_A	IO	—	—	—	EtherAVB	AVB_PHY_INT	I	—	—	—	—	—	—	—	—	—
273	G3	—	GP5_17	SSI4	SSI_SDATA4_A	IO	—	—	—	EtherAVB	AVB_CRS	I	—	—	—	—	—	—	—	—	—
274	H2	—	GP5_18	SSI1	SSI_SCK1_A	IO	SCIF1	SCIF1_SCK_B	IO	PWM1	PWM1_D	O	INTC	IRQ9	I	REMOCON	REMOCON_A	I	LBSC	DACK2	O
275	F4	—	GP5_19	SSI8	SSI_SDATA8_A	IO	SCIF1	RX1_B	I	—	—	—	—	—	—	RCAN0	CAN0_RX_D	I	EtherAVB	AVB_AVTP_CAPTURE_B	I
276	H1	—	GP5_20	SSI1	SSI_WS1_A	IO	SCIF1	TX1_B	O	—	—	—	—	—	—	RCAN0	CAN0_TX_D	O	EtherAVB	AVB_AVTP_MATCH_B	O
277	J4	—	GP5_21	SSI1	SSI_SDATA1_A	IO	HSCIF1	HRX1_B	I	—	—	—	—	—	—	—	—	—	—	—	—
278	J3	—	GP5_22	SSI2	SSI_SCK2_A	IO	HSCIF1	HTX1_B	O	—	—	—	—	—	—	—	—	—	EtherAVB	AVB_TXD7	O
279	J2	—	GP5_23	SSI2	SSI_WS2_A	IO	HSCIF1	HCTS1#_B	IO	—	—	—	—	—	—	—	—	—	EtherAVB	AVB_TX_ER	O
280	J1	—	GP5_24	SSI2	SSI_SDATA2_A	IO	HSCIF1	HRTS1#_B	IO	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
267	VIN0	VI0_R0	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
268	VIN0	VI0_R1	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
269	VIN0	VI0_R2	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
270	VIN0	VI0_R3	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
271	VIN0	VI0_R4	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
272	VIN0	VI0_R5	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
273	VIN0	VI0_R6	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
274	VIN0	VI0_CLK	I	EtherAVB	AVB_COL	I	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
275	VIN0	VI0_R7	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
276	VIN0	VI0_DATA0_VI0_B0	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
277	VIN0	VI0_DATA1_VI0_B1	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
278	VIN0	VI0_DATA2_VI0_B2	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
279	VIN0	VI0_DATA3_VI0_B3	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	variable (initail 10)	pullup*	—
280	VIN0	VI0_DATA4_VI0_B4	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
281	K3	—	GP5_25	SSI9	SSI_SCK9_A	IO	SCIF2	RX2_B	I	I2C3	SCL3_E	IO	—	—	—	—	—	—	LBSC	EX_WAIT1	I
282	K2	—	GP5_26	SSI9	SSI_WS9_A	IO	SCIF2	TX2_B	O	I2C3	SDA3_E	IO	—	—	—	—	—	—	—	—	—
283	K1	—	GP5_27	SSI9	SSI_SDATA9_A	IO	SCIF2	SCIF2_SCK_B	IO	PWM2	PWM2_D	O	—	—	—	—	—	—	—	—	—
284	E2	—	GP5_28	ADGA	AUDIO_CLKA_A	I	I2C0	SCL0_B	IO	—	Reserved	—	—	—	—	—	—	—	—	—	—
285	E3	—	GP5_29	ADGB	AUDIO_CLKB_A	I	I2C0	SDA0_B	IO	—	Reserved	—	—	—	—	—	—	—	—	—	—
286	E4	—	GP5_30	ADGC	AUDIO_CLKC_A	I	I2C4	SCL4_B	IO	—	Reserved	—	—	—	—	—	—	—	—	—	—
287	E1	—	GP5_31	ADG	AUDIO_CLKOUT_A	O	I2C4	SDA4_B	IO	—	Reserved	—	—	—	—	—	—	—	—	—	—
288	U6	—	—	CVBS in	VCCQA_ADC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
289	U5	—	—	CVBS in	VSSQA_ADC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
290	W4	—	—	CVBS in	VIN1A	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
291	V4	—	—	CVBS in	VIN2A	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
292	V5	—	—	CVBS in	VRP	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
293	V6	—	—	CVBS in	VRM	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
294	W6	—	—	CVBS in	REXT	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
295	W1	—	—	CVBS in	VIDEO_X1	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
296	W2	—	—	CVBS in	VIDEO_X2	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
297	Y14	—	—	LVDS	VCCQA_LVDS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
298	AA14	—	—	LVDS	VSSQA_LVDS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
281	VIN0	VI0_DATA5_VI0_B5	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
282	VIN0	VI0_DATA6_VI0_B6	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
283	VIN0	VI0_DATA7_VI0_B7	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
284	VIN0	VI0_CLKENB	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
285	VIN0	VI0_FIELD	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
286	VIN0	VI0_HSYNC#	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
287	VIN0	VI0_VSYNC#	I	—	—	—	VCCQ	3.3V	open	GPIO	ZU	GPIO	ZU	GPIO	ZU	IO	—	pullup*	—
288	—	—	—	—	—	—	VCCQA_ADC	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
289	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
290	—	—	—	—	—	—	VCCQA_ADC	3.3V	open	—	—	—	—	—	—	—	—	—	—
291	—	—	—	—	—	—	VCCQA_ADC	3.3V	open	—	—	—	—	—	—	—	—	—	—
292	—	—	—	—	—	—	VCCQA_ADC	3.3V	open	—	—	—	—	—	—	—	—	—	—
293	—	—	—	—	—	—	VCCQA_ADC	3.3V	open	—	—	—	—	—	—	—	—	—	—
294	—	—	—	—	—	—	VCCQA_ADC	3.3V	open	—	—	—	—	—	—	—	—	—	—
295	—	—	—	—	—	—	VCCQ	3.3V	pulldown	—	—	—	—	—	—	—	—	—	—
296	—	—	—	—	—	—	VCCQ	3.3V	open	—	—	—	—	—	—	—	—	—	—
297	—	—	—	—	—	—	VCCQA_LVDS	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
298	—	—	—	—	—	—	VSSQA_LVDS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
299	Y15	—	—	LVDS	VDDA_LVDSPLL	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
300	Y13	—	—	LVDS	LVDSREFRIN	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
301	AD13	—	—	LVDS	TXOUT0P	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
302	AE13	—	—	LVDS	TXOUT0M	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
303	AB14	—	—	LVDS	TXOUT1P	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
304	AC14	—	—	LVDS	TXOUT1M	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
305	AD15	—	—	LVDS	TXOUT2P	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
306	AE15	—	—	LVDS	TXOUT2M	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
307	AD17	—	—	LVDS	TXOUT3P	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
308	AE17	—	—	LVDS	TXOUT3M	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
309	AB16	—	—	LVDS	TXCLKOUTP	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
310	AC16	—	—	LVDS	TXCLKOUTM	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
311	U2	—	—	CVBS out	VSSQA_DAC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
312	V2	—	—	CVBS out	VSSQA_DAC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
313	V3	—	—	CVBS out	VSSQA_DAC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
314	U1	—	—	CVBS out	VO	O	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
315	V1	—	—	CVBS out	VCCQA_DAC	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
316	U4	—	—	CVBS out	CBP	I	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
317	H5	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
318	K5	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
299	—	—	—	—	—	—	VDDA_LVDSPLL	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
300	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
301	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
302	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
303	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
304	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
305	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
306	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
307	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
308	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
309	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
310	—	—	—	—	—	—	VCCQA_LVDS	3.3V	open	—	—	—	—	—	—	—	—	—	—
311	—	—	—	—	—	—	VSSQA_DAC	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
312	—	—	—	—	—	—	VSSQA_DAC	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
313	—	—	—	—	—	—	VSSQA_DAC	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
314	—	—	—	—	—	—	VCCQA_DAC	3.3V	open	—	—	—	—	—	—	—	—	—	—
315	—	—	—	—	—	—	VCCQA_DAC	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
316	—	—	—	—	—	—	VCCQA_DAC	3.3V	open	—	—	—	—	—	—	—	—	—	—
317	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
318	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
319	M5	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
320	P5	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
321	H6	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
322	K6	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
323	M6	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
324	P6	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
325	E7	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
326	F7	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
327	Y8	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
328	AA8	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
329	Y10	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
330	AA10	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
331	Y17	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
332	Y18	—	—	Power	VCCQ	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
333	Y16	—	—	Power	VCCQ18	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
334	AA17	—	—	Power	VCCQ18	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
335	T1	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
336	T2	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
337	T3	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
338	T4	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
339	T5	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
340	T6	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
341	M10	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
342	N10	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
343	P10	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
344	M11	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
345	N11	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
346	P11	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
347	K12	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
348	L12	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
349	M12	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
350	P12	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
319	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
320	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
321	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
322	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
323	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
324	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
325	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
326	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
327	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
328	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
329	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
330	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
331	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
332	—	—	—	—	—	—	VCCQ	3.3V	VCCQ	—	—	—	—	—	—	—	—	—	—
333	—	—	—	—	—	—	VCCQ18	1.8V	VCCQ18	—	—	—	—	—	—	—	—	—	—
334	—	—	—	—	—	—	VCCQ18	1.8V	VCCQ18	—	—	—	—	—	—	—	—	—	—
335	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
336	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
337	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
338	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
339	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
340	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
341	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
342	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
343	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
344	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
345	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
346	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
347	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
348	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
349	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
350	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—

No.	PKG Pin	MD	GPIO	Function I			Function II			Function III			Function IV			Function V			Function VI			
				Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
351	R12	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
352	T12	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
353	K14	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
354	L14	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
355	M14	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
356	P14	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
357	R14	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
358	T14	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
359	N15	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
360	N16	—	—	Power	VDD	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
361	E15	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
362	F15	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
363	E17	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
364	F17	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
365	A18	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
366	J20	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
367	L20	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
368	P20	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
369	J21	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
370	L21	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
371	P21	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
372	U21	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
373	A22	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
374	M24	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
351	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
352	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
353	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
354	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
355	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
356	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
357	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
358	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
359	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
360	—	—	—	—	—	—	VDD	1.2V	VDD	—	—	—	—	—	—	—	—	—	—
361	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
362	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
363	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
364	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
365	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
366	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
367	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
368	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
369	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
370	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
371	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
372	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
373	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
374	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
375	D25	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
376	H25	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
377	U25	—	—	Power	VDDQ_M0	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
378	A1	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
379	D1	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
380	AE1	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
381	R2	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
382	C3	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
383	H3	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
384	U3	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
385	W3	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
386	AC3	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
387	D4	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
388	AB4	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
389	E5	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
390	J5	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
391	N5	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
392	W5	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
393	AA5	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
394	AE5	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
395	E6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
396	F6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
397	G6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
398	J6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
399	L6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
400	N6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
401	R6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
402	Y6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
403	AA6	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
404	C7	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
405	Y7	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
406	F8	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
407	E9	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
408	F9	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
409	Y9	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
410	F10	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
375	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
376	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
377	—	—	—	—	—	—	VDDQ_M0	1.5V	VDDQ_M0	—	—	—	—	—	—	—	—	—	—
378	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
379	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
380	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
381	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
382	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
383	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
384	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
385	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
386	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
387	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
388	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
389	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
390	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
391	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
392	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
393	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
394	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
395	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
396	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
397	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
398	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
399	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
400	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
401	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
402	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
403	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
404	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
405	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
406	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
407	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
408	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
409	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
410	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
411	L10	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
412	R10	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
413	T10	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
414	C11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
415	F11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
416	K11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
417	L11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
418	R11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
419	T11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
420	Y11	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
421	E12	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
422	F12	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
423	Y12	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
424	AA12	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
425	F13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
426	K13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
427	L13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
428	M13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
429	P13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
430	R13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
431	T13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
432	AA13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
433	AB13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
434	AC13	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
435	A14	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
436	E14	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
437	F14	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
438	AD14	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
439	AE14	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
440	M15	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
441	P15	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
442	AA15	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
443	AB15	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
444	AC15	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
445	E16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
446	F16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
447	M16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
448	P16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
449	AA16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
450	AD16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
411	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
412	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
413	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
414	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
415	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
416	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
417	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
418	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
419	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
420	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
421	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
422	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
423	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
424	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
425	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
426	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
427	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
428	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
429	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
430	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
431	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
432	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
433	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
434	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
435	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
436	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
437	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
438	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
439	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
440	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
441	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
442	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
443	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
444	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
445	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
446	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
447	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
448	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
449	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
450	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
451	AE16	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
452	B17	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
453	AB17	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
454	AC17	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
455	A19	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
456	D19	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
457	E19	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
458	F19	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
459	Y19	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
460	E20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
461	F20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
462	H20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
463	K20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
464	M20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
465	R20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
466	T20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
467	U20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
468	Y20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
469	AE20	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
470	B21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
471	E21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
472	F21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
473	H21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
474	K21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
475	M21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
476	R21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
477	Y21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
478	AA21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
479	AD21	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
480	D22	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
481	G22	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
482	K22	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
483	AB22	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
484	AD22	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
485	C23	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
486	G23	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
487	N23	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
488	V23	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
489	AC23	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
490	AD23	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
451	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
452	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
453	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
454	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
455	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
456	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
457	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
458	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
459	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
460	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
461	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
462	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
463	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
464	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
465	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
466	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
467	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
468	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
469	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
470	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
471	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
472	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
473	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
474	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
475	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
476	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
477	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
478	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
479	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
480	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
481	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
482	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
483	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
484	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
485	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
486	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
487	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
488	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
489	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
490	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—

				Function I			Function II			Function III			Function IV			Function V			Function VI			
No.	PKG Pin	MD	GPIO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO	Module	Pin Name	IO
491	B24	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
492	E24	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
493	J24	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
494	AD24	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
495	A25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
496	G25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
497	L25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
498	R25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
499	AA25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
500	AD25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
501	AE25	—	—	Power	VSS	P	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

No.	Function VII			Function VIII			Power Domain	Voltage	Pin setting for unuse	Pin condition at PRESET# = L	Pin state	Pin condition after				IO direction	Drivability	Pull-up control	Schmitt
	Module	Pin Name	IO	Module	Pin Name	IO						Power-on reset deassert(LBSC) MD[3:1] = 000	Pin state	Power-on reset deassert MD[3:1] = others	Pin state				
491	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
492	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
493	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
494	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
495	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
496	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
497	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
498	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
499	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
500	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—
501	—	—	—	—	—	—	VSS	0.0V	VSS	—	—	—	—	—	—	—	—	—	—

5. Pin Function Controller (PFC)

5.1 Overview

The pin function controller (PFC) is a module that consists of registers for selecting the function of the multiplexed pins and controlling the pull resistor (up/down) on each LSI pin.

Notes: 1. Some functions are optional or internal.
2. Pin function name that has two or more functions is indicated by using "_" instead of "/".

5.1.1 Features

- Register access through APB bus interface.
- LSI pin multiplex function selecting:
  Functions of LSI pins are selected by setting the IPSR/GPSR registers in the PFC module. For details, refer to section from 5.3.1 to 5.3.41.
- Function groups selecting:
  Function has multiple group pins are selected by setting the module select registers (from MOD_SEL0 to MOD_SEL2). For details, refer to section from 5.3.26 to 5.3.28.
- Pull control
  Pull-up or pull-down resistors on LSI pins are controlled by setting PUPR registers (from PUPR0 to PUPR5).
- Driving ability control, power on control, RSEL, TDSEL
  Driving ability (DRV), power on control (POC) of some specific modules, RSEL, and TDSEL can be control by setting IOCTRL registers (from IOCRTL0 to IOCTRL6).

5.2 Register Configuration

All the registers in the PFC are mapped into the APB bus space. Table 5.1 shows the configuration of the registers provided in the PFC. Details on each register in the PFC are given in sections 5.3.1 to 5.3.41.

Table 5.1 Configuration of Registers in PFC

Name	Abbr.	R/W	Initial Value	Address	Access Size
LSI Multiplexed Pin Setting Mask Register	PMMR	R/W	H'0000 0000	H'E606 0000	32
GPIO/peripheral function select register 0	GPSR0	R/W	H'0000 001F	H'E606 0004	32
GPIO/peripheral function select register 1	GPSR1	R/W	H'007F FFFF (when md[3:1] = 000) H'0000 0000 (others case)	H'E606 0008	32
GPIO/peripheral function select register 2	GPSR2	R/W	H'07FF FFFF (when md[3:1] = 000) H'0000 0000 (others case)	H'E606 000C	32
GPIO/peripheral function select register 3	GPSR3	R/W	H'0000 0000	H'E606 0010	32
GPIO/peripheral function select register 4	GPSR4	R/W	H'0000 0000	H'E606 0014	32
GPIO/peripheral function select register 5	GPSR5	R/W	H'0000 0000	H'E606 0018	32
Peripheral function select register 0	IPSR0	R/W	H'0000 0000	H'E606 0040	32
Peripheral function select register 1	IPSR1	R/W	H'0000 0000	H'E606 0044	32
Peripheral function select register 2	IPSR2	R/W	H'0000 0000	H'E606 0048	32
Peripheral function select register 3	IPSR3	R/W	H'1111 1100	H'E606 004C	32
Peripheral function select register 4	IPSR4	R/W	H'6666 6660	H'E606 0050	32
Peripheral function select register 5	IPSR5	R/W	H'6666 6666	H'E606 0054	32
Peripheral function select register 6	IPSR6	R/W	H'6666 6666	H'E606 0058	32
Peripheral function select register 7	IPSR7	R/W	H'0000 6666	H'E606 005C	32
Peripheral function select register 8	IPSR8	R/W	H'0000 0000	H'E606 0060	32
Peripheral function select register 9	IPSR9	R/W	H'0000 0000	H'E606 0064	32
Peripheral function select register 10	IPSR10	R/W	H'0000 0000	H'E606 0068	32
Peripheral function select register 11	IPSR11	R/W	H'0000 0000	H'E606 006C	32
Peripheral function select register 12	IPSR12	R/W	H'0000 0000	H'E606 0070	32
Peripheral function select register 13	IPSR13	R/W	H'0000 0000	H'E606 0074	32
Peripheral function select register 14	IPSR14	R/W	H'0000 0000	H'E606 0078	32
Peripheral function select register 15	IPSR15	R/W	H'0000 0000	H'E606 007C	32
Peripheral function select register 16	IPSR16	R/W	H'0000 0000	H'E606 0080	32
Peripheral function select register 17	IPSR17	R/W	H'0000 0000	H'E606 0084	32
Module select register 0	MOD_SEL0	R/W	H'0000 0000	H'E606 00C0	32
Module select register 1	MOD_SEL1	R/W	H'0000 0000	H'E606 00C4	32
Module select register 2	MOD_SEL2	R/W	H'0000 0000	H'E606 00C8	32
LSI pin pull-up control register 0	PUPR0	R/W	H'7AA0 1801	H'E606 0100	32

Name	Abbr.	R/W	Initial Value	Address	Access Size
LSI pin pull-up control register 1	PUPR1	R/W	H'FFFF FFC3	H'E606 0104	32
LSI pin pull-up control register 2	PUPR2	R/W	H'0333 93FF	H'E606 0108	32
LSI pin pull-up control register 3	PUPR3	R/W	H'FFFF FF03	H'E606 010C	32
LSI pin pull-up control register 4	PUPR4	R/W	H'FFFF FFFF	H'E606 0110	32
LSI pin pull-up control register 5	PUPR5	R/W	H'F000 0000	H'E606 0114	32
Drivability control register 0	IOCTRL0	R/W	H'AAAA AAAA	H'E606 0094	32
Drivability control register 1	IOCTRL1	R/W	H'AAAA AAAA	H'E606 0098	32
Drivability control register 2	IOCTRL2	R/W	H'AAAA AAAA	H'E606 009C	32
Drivability control register 3	IOCTRL3	R/W	H'AAAA AAAA	H'E606 00A0	32
RSEL control register	IOCTRL4	R/W	H'003F FFFF	H'E606 00A8	32
TDSEL control register	IOCTRL5	R/W	H'0000 0AAA	H'E606 00AC	32
POC control register	IOCTRL6	R/W	H'0000 0007	H'E606 00B0	32

5.3 Register Description

[Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

-/W: Write-only. The read value is undefined.

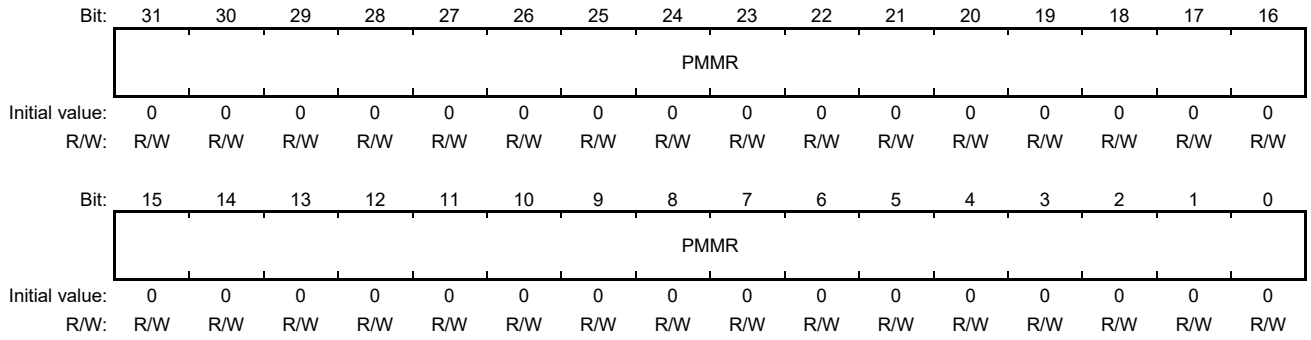
All the bits are active high unless otherwise specified, and deactivated on reset.

All access to registers is made in long word units.

The write value to a reserved bit should always be 0.

5.3.1 LSI Multiplexed Pin Setting Mask Register (PMMR)

Function: PMMR enables/disables writing to the multiplexed pin setting registers.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PMMR[31:0]	H'0000 0000	R/W	Multiplexed Pin Setting Mask Writing a value to any register from among the GPIO/peripheral function select registers GPSR0 to GPSR5, peripheral function select registers IPSR0 to IPSR17, drivability control registers DRVCTRL0-3, RSEL control register IOCTRL4, TDSEL control registers IOCRTL5, POC register IOCRL6, Pull control registers PUPR0-5 and Module select register MOD_SEL0-2 is enabled by writing the inverse of the value to this register.

Note: This register must be set before setting each of the GPIO/peripheral function select registers GPSR0 to GPSR5, peripheral function select registers IPSR0 to IPSR17, module select registers MOD_SEL0, MOD_SEL1, MOD_SEL2, IO cell control registers IOCTRL0 to IOCTRL6 and pull control registers PUPR0 to PUPR5.

5.3.2 GPIO/Peripheral Function Select Register 0 (GPSR0)

Function: GPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	GP0[22]	GP0[21]	GP0[20]	GP0[19]	GP0[18]	GP0[17]	GP0[16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP0[15]	GP0[14]	GP0[13]	GP0[12]	GP0[11]	GP0[10]	GP0[9]	GP0[8]	GP0[7]	GP0[6]	GP0[5]	GP0[4]	GP0[3]	GP0[2]	GP0[1]	GP0[0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP0[31:0]	H'0000 001F	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[0]	GP-0-0	USB0_PWEN
GP0[1]	GP-0-1	USB0_OVC
GP0[2]	GP-0-2	USB1_PWEN
GP0[3]	GP-0-3	USB1_OVC
GP0[4]	GP-0-4	CLKOUT
GP0[5]	GP-0-5	Peripheral function selected by IP0[3:0]
GP0[6]	GP-0-6	Peripheral function selected by IP0[7:4]
GP0[7]	GP-0-7	Peripheral function selected by IP0[11:8]
GP0[8]	GP-0-8	Peripheral function selected by IP0[15:12]
GP0[9]	GP-0-9	Peripheral function selected by IP0[19:16]
GP0[10]	GP-0-10	Peripheral function selected by IP0[23:20]
GP0[11]	GP-0-11	Peripheral function selected by IP0[27:24]
GP0[12]	GP-0-12	Peripheral function selected by IP0[31:28]
GP0[13]	GP-0-13	MMC0_CLK / SDHI1_CLK
GP0[14]	GP-0-14	MMC0_CMD / SDHI1_CMD
GP0[15]	GP-0-15	MMC0_D0 / SDHI1_D0
GP0[16]	GP-0-16	MMC0_D1 / SDHI1_D1
GP0[17]	GP-0-17	MMC0_D2 / SDHI1_D2
GP0[18]	GP-0-18	MMC0_D3 / SDHI1_D3
GP0[19]	GP-0-19	Peripheral function selected by IP1[3:0]
GP0[20]	GP-0-20	Peripheral function selected by IP1[7:4]
GP0[21]	GP-0-21	MMC0_D6
GP0[22]	GP-0-22	MMC0_D7
GP0[23]	—	—
GP0[24]	—	—
GP0[25]	—	—

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP0[26]	—	—
GP0[27]	—	—
GP0[28]	—	—
GP0[29]	—	—
GP0[30]	—	—
GP0[31]	—	—

5.3.3 GPIO/Peripheral Function Select Register 1 (GPSR1)

Function: GPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	GP1 [22]	GP1 [21]	GP1 [20]	GP1 [19]	GP1 [18]	GP1 [17]	GP1 [16]
Initial value:	0	0	0	0	0	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP1 [15]	GP1 [14]	GP1 [13]	GP1 [12]	GP1 [11]	GP1 [10]	GP1 [9]	GP1 [8]	GP1 [7]	GP1 [6]	GP1 [5]	GP1 [4]	GP1 [3]	GP1 [2]	GP1 [1]	GP1 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP1[31:0]	H'007F FFFF (when md[3:1] = 000) H'0000 0000 (others case)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[0]	GP-1-0	Peripheral function selected by IP1[11:8]
GP1[1]	GP-1-1	Peripheral function selected by IP1[15:12]
GP1[2]	GP-1-2	Peripheral function selected by IP1[19:16]
GP1[3]	GP-1-3	Peripheral function selected by IP1[23:20]
GP1[4]	GP-1-4	Peripheral function selected by IP1[27:24]
GP1[5]	GP-1-5	Peripheral function selected by IP1[31:28]
GP1[6]	GP-1-6	Peripheral function selected by IP2[3:0]
GP1[7]	GP-1-7	Peripheral function selected by IP2[7:4]
GP1[8]	GP-1-8	Peripheral function selected by IP2[11:8]
GP1[9]	GP-1-9	Peripheral function selected by IP2[15:12]
GP1[10]	GP-1-10	Peripheral function selected by IP2[19:16]
GP1[11]	GP-1-11	Peripheral function selected by IP2[23:20]
GP1[12]	GP-1-12	Peripheral function selected by IP2[27:24]
GP1[13]	GP-1-13	Peripheral function selected by IP2[31:28]
GP1[14]	GP-1-14	Peripheral function selected by IP3[3:0]
GP1[15]	GP-1-15	Peripheral function selected by IP3[7:4]
GP1[16]	GP-1-16	Peripheral function selected by IP3[11:8]
GP1[17]	GP-1-17	Peripheral function selected by IP3[15:12]
GP1[18]	GP-1-18	Peripheral function selected by IP3[19:16]
GP1[19]	GP-1-19	Peripheral function selected by IP3[23:20]
GP1[20]	GP-1-20	Peripheral function selected by IP3[27:24]
GP1[21]	GP-1-21	Peripheral function selected by IP3[31:28]
GP1[22]	GP-1-22	Peripheral function selected by IP4[3:0]

Bit Name	GPIO (Set Value = 0)	Peripheral Function (Set Value = 1)
GP1[23]	—	—
GP1[24]	—	—
GP1[25]	—	—
GP1[26]	—	—
GP1[27]	—	—
GP1[28]	—	—
GP1[29]	—	—
GP1[30]	—	—
GP1[31]	—	—

5.3.4 GPIO/Peripheral Function Select Register 2 (GPSR2)

Function: GPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP2 [31]	GP2 [30]	GP2 [29]	GP2 [28]	GP2 [27]	GP2 [26]	GP2 [25]	GP2 [24]	GP2 [23]	GP2 [22]	GP2 [21]	GP2 [20]	GP2 [19]	GP2 [18]	GP2 [17]	GP2 [16]
Initial value:	0	0	0	0	0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP2 [15]	GP2 [14]	GP2 [13]	GP2 [12]	GP2 [11]	GP2 [10]	GP2 [9]	GP2 [8]	GP2 [7]	GP2 [6]	GP2 [5]	GP2 [4]	GP2 [3]	GP2 [2]	GP2 [1]	GP2 [0]
Initial value:	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0	1/0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP2[31:0]	H'07FF FFFF (when md[3:1] = 000) H'0000 0000 (others case)	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP2[0]	GP-2-0	Peripheral function selected by IP4[7:4]
GP2[1]	GP-2-1	Peripheral function selected by IP4[11:8]
GP2[2]	GP-2-2	Peripheral function selected by IP4[15:12]
GP2[3]	GP-2-3	Peripheral function selected by IP4[19:16]
GP2[4]	GP-2-4	Peripheral function selected by IP4[23:20]
GP2[5]	GP-2-5	Peripheral function selected by IP4[27:24]
GP2[6]	GP-2-6	Peripheral function selected by IP4[31:28]
GP2[7]	GP-2-7	Peripheral function selected by IP5[3:0]
GP2[8]	GP-2-8	Peripheral function selected by IP5[7:4]
GP2[9]	GP-2-9	Peripheral function selected by IP5[11:8]
GP2[10]	GP-2-10	Peripheral function selected by IP5[15:12]
GP2[11]	GP-2-11	Peripheral function selected by IP5[19:16]
GP2[12]	GP-2-12	Peripheral function selected by IP5[23:20]
GP2[13]	GP-2-13	Peripheral function selected by IP5[27:24]
GP2[14]	GP-2-14	Peripheral function selected by IP5[31:28]
GP2[15]	GP-2-15	Peripheral function selected by IP6[3:0]
GP2[16]	GP-2-16	Peripheral function selected by IP6[7:4]
GP2[17]	GP-2-17	Peripheral function selected by IP6[11:8]
GP2[18]	GP-2-18	Peripheral function selected by IP6[15:12]
GP2[19]	GP-2-19	Peripheral function selected by IP6[19:16]
GP2[20]	GP-2-20	Peripheral function selected by IP6[23:20]
GP2[21]	GP-2-21	Peripheral function selected by IP6[27:24]
GP2[22]	GP-2-22	Peripheral function selected by IP6[31:28]

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP2[23]	GP-2-23	Peripheral function selected by IP7[3:0]
GP2[24]	GP-2-24	Peripheral function selected by IP7[7:4]
GP2[25]	GP-2-25	Peripheral function selected by IP7[11:8]
GP2[26]	GP-2-26	Peripheral function selected by IP7[15:12]
GP2[27]	GP-2-27	Peripheral function selected by IP7[19:16]
GP2[28]	GP-2-28	Peripheral function selected by IP7[23:20]
GP2[29]	GP-2-29	Peripheral function selected by IP7[27:24]
GP2[30]	GP-2-30	Peripheral function selected by IP7[31:28]
GP2[31]	GP-2-31	Peripheral function selected by IP8[3:0]

5.3.5 GPIO/Peripheral Function Select Register 3 (GPSR3)

Function: GPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	GP3 [29]	GP3 [28]	GP3 [27]	—	—	—	—	—	—	—	—	—	—	GP3 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP3 [15]	GP3 [14]	GP3 [13]	GP3 [12]	GP3 [11]	GP3 [10]	GP3 [9]	GP3 [8]	GP3 [7]	GP3 [6]	GP3 [5]	GP3 [4]	GP3 [3]	GP3 [2]	GP3 [1]	GP3 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP3[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP3[0]	GP-3-0	Peripheral function selected by IP8[7:4]
GP3[1]	GP-3-1	Peripheral function selected by IP8[11:8]
GP3[2]	GP-3-2	Peripheral function selected by IP8[15:12]
GP3[3]	GP-3-3	Peripheral function selected by IP8[19:16]
GP3[4]	GP-3-4	Peripheral function selected by IP8[23:20]
GP3[5]	GP-3-5	Peripheral function selected by IP8[27:24]
GP3[6]	GP-3-6	Peripheral function selected by IP8[31:28]
GP3[7]	GP-3-7	Peripheral function selected by IP9[3:0]
GP3[8]	GP-3-8	Peripheral function selected by IP9[7:4]
GP3[9]	GP-3-9	Peripheral function selected by IP9[11:8]
GP3[10]	GP-3-10	Peripheral function selected by IP9[15:12]
GP3[11]	GP-3-11	Peripheral function selected by IP9[19:16]
GP3[12]	GP-3-12	Peripheral function selected by IP9[23:20]
GP3[13]	GP-3-13	Peripheral function selected by IP9[27:24]
GP3[14]	GP-3-14	Peripheral function selected by IP9[31:28]
GP3[15]	GP-3-15	Peripheral function selected by IP10[3:0]
GP3[16]	GP-3-16	Peripheral function selected by IP10[7:4]
GP3[17]	—	—
GP3[18]	—	—
GP3[19]	—	—
GP3[20]	—	—
GP3[21]	—	—
GP3[22]	—	—
GP3[23]	—	—
GP3[24]	—	—
GP3[25]	—	—

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP3[26]	—	—
GP3[27]	GP-3-27	Peripheral function selected by IP10[11:8]
GP3[28]	GP-3-28	Peripheral function selected by IP10[15:12]
GP3[29]	GP-3-29	Peripheral function selected by IP10[19:16]
GP3[30]	—	—
GP3[31]	—	—

5.3.6 GPIO/Peripheral Function Select Register 4 (GPSR4)

Function: GPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	GP4 [25]	GP4 [24]	GP4 [23]	GP4 [22]	GP4 [21]	GP4 [20]	GP4 [19]	GP4 [18]	GP4 [17]	GP4 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP4 [15]	GP4 [14]	GP4 [13]	GP4 [12]	GP4 [11]	GP4 [10]	GP4 [9]	GP4 [8]	GP4 [7]	GP4 [6]	GP4 [5]	GP4 [4]	GP4 [3]	GP4 [2]	GP4 [1]	GP4 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP4[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP4[0]	GP-4-0	Peripheral function selected by IP10[23:20]
GP4[1]	GP-4-1	Peripheral function selected by IP10[27:24]
GP4[2]	GP-4-2	Peripheral function selected by IP10[31:28]
GP4[3]	GP-4-3	Peripheral function selected by IP11[3:0]
GP4[4]	GP-4-4	Peripheral function selected by IP11[7:4]
GP4[5]	GP-4-5	Peripheral function selected by IP11[11:8]
GP4[6]	GP-4-6	Peripheral function selected by IP11[15:12]
GP4[7]	GP-4-7	Peripheral function selected by IP11[19:16]
GP4[8]	GP-4-8	Peripheral function selected by IP11[23:20]
GP4[9]	GP-4-9	Peripheral function selected by IP11[27:24]
GP4[10]	GP-4-10	Peripheral function selected by IP11[31:28]
GP4[11]	GP-4-11	Peripheral function selected by IP12[3:0]
GP4[12]	GP-4-12	Peripheral function selected by IP12[7:4]
GP4[13]	GP-4-13	Peripheral function selected by IP12[11:8]
GP4[14]	GP-4-14	Peripheral function selected by IP12[15:12]
GP4[15]	GP-4-15	Peripheral function selected by IP12[19:16]
GP4[16]	GP-4-16	Peripheral function selected by IP12[23:20]
GP4[17]	GP-4-17	Peripheral function selected by IP12[27:24]
GP4[18]	GP-4-18	Peripheral function selected by IP12[31:28]
GP4[19]	GP-4-19	Peripheral function selected by IP13[3:0]
GP4[20]	GP-4-20	Peripheral function selected by IP13[7:4]
GP4[21]	GP-4-21	Peripheral function selected by IP13[11:8]
GP4[22]	GP-4-22	Peripheral function selected by IP13[15:12]
GP4[23]	GP-4-23	Peripheral function selected by IP13[19:16]
GP4[24]	GP-4-24	Peripheral function selected by IP13[23:20]
GP4[25]	GP-4-25	Peripheral function selected by IP13[27:24]

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP4[26]	—	—
GP4[27]	—	—
GP4[28]	—	—
GP4[29]	—	—
GP4[30]	—	—
GP4[31]	—	—

5.3.7 GPIO/Peripheral Function Select Register 5 (GPSR5)

Function: GPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	GP5 [31]	GP5 [30]	GP5 [29]	GP5 [28]	GP5 [27]	GP5 [26]	GP5 [25]	GP5 [24]	GP5 [23]	GP5 [22]	GP5 [21]	GP5 [20]	GP5 [19]	GP5 [18]	GP5 [17]	GP5 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	GP5 [15]	GP5 [14]	GP5 [13]	GP5 [12]	GP5 [11]	GP5 [10]	GP5 [9]	GP5 [8]	GP5 [7]	GP5 [6]	GP5 [5]	GP5 [4]	GP5 [3]	GP5 [2]	GP5 [1]	GP5 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	GP5[31:0]	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP5[0]	GP-5-0	Peripheral function selected by IP13[31:28]
GP5[1]	GP-5-1	Peripheral function selected by IP14[3:0]
GP5[2]	GP-5-2	Peripheral function selected by IP14[7:4]
GP5[3]	GP-5-3	Peripheral function selected by IP14[11:8]
GP5[4]	GP-5-4	Peripheral function selected by IP14[15:12]
GP5[5]	GP-5-5	Peripheral function selected by IP14[19:16]
GP5[6]	GP-5-6	Peripheral function selected by IP14[23:20]
GP5[7]	GP-5-7	Peripheral function selected by IP14[27:24]
GP5[8]	GP-5-8	Peripheral function selected by IP14[31:28]
GP5[9]	GP-5-9	Peripheral function selected by IP15[3:0]
GP5[10]	GP-5-10	Peripheral function selected by IP15[7:4]
GP5[11]	GP-5-11	Peripheral function selected by IP15[11:8]
GP5[12]	GP-5-12	Peripheral function selected by IP15[15:12]
GP5[13]	GP-5-13	Peripheral function selected by IP15[19:16]
GP5[14]	GP-5-14	Peripheral function selected by IP15[23:20]
GP5[15]	GP-5-15	Peripheral function selected by IP15[27:24]
GP5[16]	GP-5-16	Peripheral function selected by IP15[31:28]
GP5[17]	GP-5-17	Peripheral function selected by IP16[3:0]
GP5[18]	GP-5-18	Peripheral function selected by IP16[7:4]
GP5[19]	GP-5-19	Peripheral function selected by IP16[11:8]
GP5[20]	GP-5-20	Peripheral function selected by IP16[15:12]
GP5[21]	GP-5-21	Peripheral function selected by IP16[19:16]
GP5[22]	GP-5-22	Peripheral function selected by IP16[23:20]
GP5[23]	GP-5-23	Peripheral function selected by IP16[27:24]
GP5[24]	GP-5-24	Peripheral function selected by IP16[31:28]
GP5[25]	GP-5-25	Peripheral function selected by IP17[3:0]

Bit Name	Function 1 (Set Value = 0)	Function 2 (Set Value = 1)
GP5[26]	GP-5-26	Peripheral function selected by IP17[7:4]
GP5[27]	GP-5-27	Peripheral function selected by IP17[11:8]
GP5[28]	GP-5-28	Peripheral function selected by IP17[15:12]
GP5[29]	GP-5-29	Peripheral function selected by IP17[19:16]
GP5[30]	GP-5-30	Peripheral function selected by IP17[23:20]
GP5[31]	GP-5-31	Peripheral function selected by IP17[27:24]

5.3.8 Peripheral Function Select Register 0 (IPSR0)

Function: IPSR0 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP0 [31]	IP0 [30]	IP0 [29]	IP0 [28]	IP0 [27]	IP0 [26]	IP0 [25]	IP0 [24]	IP0 [23]	IP0 [22]	IP0 [21]	IP0 [20]	IP0 [19]	IP0 [18]	IP0 [17]	IP0 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP0 [15]	IP0 [14]	IP0 [13]	IP0 [12]	IP0 [11]	IP0 [10]	IP0 [9]	IP0 [8]	IP0 [7]	IP0 [6]	IP0 [5]	IP0 [4]	IP0 [3]	IP0 [2]	IP0 [1]	IP0 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP0[3:0]	SD0_CLK	—	—	SSI_SCK1_C	RX3_C	—	—
IP0[7:4]	SD0_CMD	—	—	SSI_WS1_C	TX3_C	—	—
IP0[11:8]	SD0_DAT0	—	—	SSI_SDATA1_C	RX4_E	—	—
IP0[15:12]	SD0_DAT1	—	—	SSI_SCK0129_B	TX4_E	—	—
IP0[19:16]	SD0_DAT2	—	—	SSI_WS0129_B	RX5_E	—	—
IP0[23:20]	SD0_DAT3	—	—	SSI_SDATA0_B	TX5_E	—	—
IP0[27:24]	SD0_CD	—	CAN0_RX_A	—	—	—	—
IP0[31:28]	SD0_WP	IRQ7	CAN0_TX_A	—	—	—	—

Legend: — Setting disabled

5.3.9 Peripheral Function Select Register 1 (IPSR1)

Function: IPSR1 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP1 [31]	IP1 [30]	IP1 [29]	IP1 [28]	IP1 [27]	IP1 [26]	IP1 [25]	IP1 [24]	IP1 [23]	IP1 [22]	IP1 [21]	IP1 [20]	IP1 [19]	IP1 [18]	IP1 [17]	IP1 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP1 [15]	IP1 [14]	IP1 [13]	IP1 [12]	IP1 [11]	IP1 [10]	IP1 [9]	IP1 [8]	IP1 [7]	IP1 [6]	IP1 [5]	IP1 [4]	IP1 [3]	IP1 [2]	IP1 [1]	IP1 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP1[3:0]	MMC0_D4	SD1_CD	—	—	—	—	—
IP1[7:4]	MMC0_D5	SD1_WP	—	—	—	—	—
IP1[11:8]	D0	Reserved	SCL3_B	RX5_B	IRQ4	MSIOF2_RXD_C	SSI_SDATA5_B
IP1[15:12]	D1	Reserved	SDA3_B	TX5_B	—	MSIOF2_TXD_C	SSI_WS5_B
IP1[19:16]	D2	Reserved	RX4_B	SCL0_D	PWM1_C	MSIOF2_SCK_C	SSI_SCK5_B
IP1[23:20]	D3	Reserved	TX4_B	SDA0_D	PWM0_A	MSIOF2_SYNC_C	—
IP1[27:24]	D4	—	IRQ3	TCLK1_A	PWM6_C	Reserved	—
IP1[31:28]	D5	HRX2	SCL1_B	PWM2_C	TCLK2_B	Reserved	—

Legend: — Setting disabled

5.3.10 Peripheral Function Select Register 2 (IPSR2)

Function: IPSR2 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP2 [31]	IP2 [30]	IP2 [29]	IP2 [28]	IP2 [27]	IP2 [26]	IP2 [25]	IP2 [24]	IP2 [23]	IP2 [22]	IP2 [21]	IP2 [20]	IP2 [19]	IP2 [18]	IP2 [17]	IP2 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP2 [15]	IP2 [14]	IP2 [13]	IP2 [12]	IP2 [11]	IP2 [10]	IP2 [9]	IP2 [8]	IP2 [7]	IP2 [6]	IP2 [5]	IP2 [4]	IP2 [3]	IP2 [2]	IP2 [1]	IP2 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP2[3:0]	D6	HTX2	SDA1_B	PWM4_C	—	Reserved	—
IP2[7:4]	D7	HSCK2	SCIF1_SCK_C	IRQ6	PWM5_C	Reserved	—
IP2[11:8]	D8	HCTS2#	RX1_C	SCL1_D	PWM3_C	—	—
IP2[15:12]	D9	HRTS2#	TX1_C	SDA1_D	—	—	—
IP2[19:16]	D10	MSIOF2_RXD_A	HRX0_B	—	—	—	—
IP2[23:20]	D11	MSIOF2_TXD_A	HTX0_B	—	—	—	—
IP2[27:24]	D12	MSIOF2_SCK_A	HSCK0	—	CAN_CLK_C	—	—
IP2[31:28]	D13	MSIOF2_SYNC_A	—	RX4_C	—	—	—

Legend: — Setting disabled

5.3.11 Peripheral Function Select Register 3 (IPSR3)

Function: IPSR3 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP3 [31]	IP3 [30]	IP3 [29]	IP3 [28]	IP3 [27]	IP3 [26]	IP3 [25]	IP3 [24]	IP3 [23]	IP3 [22]	IP3 [21]	IP3 [20]	IP3 [19]	IP3 [18]	IP3 [17]	IP3 [16]
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP3 [15]	IP3 [14]	IP3 [13]	IP3 [12]	IP3 [11]	IP3 [10]	IP3 [9]	IP3 [8]	IP3 [7]	IP3 [6]	IP3 [5]	IP3 [4]	IP3 [3]	IP3 [2]	IP3 [1]	IP3 [0]
Initial value:	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'1111 1100	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP3[3:0]	D14	MSIOF2_SS1	—	TX4_C	CAN1_RX_B	—	AVB_AVTP_CAPTURE_A
IP3[7:4]	D15	MSIOF2_SS2	PWM4_A	—	CAN1_TX_B	IRQ2	AVB_AVTP_MATCH_A
IP3[11:8]	QSPI0_SPCLK	WE0#	—	—	—	—	—
IP3[15:12]	QSPI0_MOSI/ QSPI0_IO0	BS#	—	—	—	—	—
IP3[19:16]	QSPI0_MISO/ QSPI0_IO1	RD/WR#	—	—	—	—	—
IP3[23:20]	QSPI0_IO2	CS0#	—	—	—	—	—
IP3[27:24]	QSPI0_IO3	RD#	—	—	—	—	—
IP3[31:28]	QSPI0_SSL	WE1#	—	—	—	—	—

Legend: — Setting disabled

5.3.12 Peripheral Function Select Register 4 (IPSR4)

Function: IPSR4 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP4 [31]	IP4 [30]	IP4 [29]	IP4 [28]	IP4 [27]	IP4 [26]	IP4 [25]	IP4 [24]	IP4 [23]	IP4 [22]	IP4 [21]	IP4 [20]	IP4 [19]	IP4 [18]	IP4 [17]	IP4 [16]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP4 [15]	IP4 [14]	IP4 [13]	IP4 [12]	IP4 [11]	IP4 [10]	IP4 [9]	IP4 [8]	IP4 [7]	IP4 [6]	IP4 [5]	IP4 [4]	IP4 [3]	IP4 [2]	IP4 [1]	IP4 [0]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'6666 6660	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP4[3:0]	EX_WAIT0	CAN_CLK_B	SCIF_CLK_A	—	—	—	—
IP4[7:4]	DU0_DR0	Reserved	RX5_C	SCL2_D	—	—	A0
IP4[11:8]	DU0_DR1	Reserved	TX5_C	SDA2_D	—	—	A1
IP4[15:12]	DU0_DR2	Reserved	RX0_D	SCL0_E	—	—	A2
IP4[19:16]	DU0_DR3	Reserved	TX0_D	SDA0_E	PWM0_B	—	A3
IP4[23:20]	DU0_DR4	Reserved	RX1_D	—	—	—	A4
IP4[27:24]	DU0_DR5	Reserved	TX1_D	—	PWM1_B	—	A5
IP4[31:28]	DU0_DR6	Reserved	RX2_C	—	—	—	A6

Legend: — Setting disabled

5.3.13 Peripheral Function Select Register 5 (IPSR5)

Function: IPSR5 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP5 [31]	IP5 [30]	IP5 [29]	IP5 [28]	IP5 [27]	IP5 [26]	IP5 [25]	IP5 [24]	IP5 [23]	IP5 [22]	IP5 [21]	IP5 [20]	IP5 [19]	IP5 [18]	IP5 [17]	IP5 [16]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP5 [15]	IP5 [14]	IP5 [13]	IP5 [12]	IP5 [11]	IP5 [10]	IP5 [9]	IP5 [8]	IP5 [7]	IP5 [6]	IP5 [5]	IP5 [4]	IP5 [3]	IP5 [2]	IP5 [1]	IP5 [0]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'6666 6666	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP5[3:0]	DU0_DR7	Reserved	TX2_C	—	PWM2_B	—	A7
IP5[7:4]	DU0_DG0	Reserved	RX3_B	SCL3_D	—	—	A8
IP5[11:8]	DU0_DG1	Reserved	TX3_B	SDA3_D	PWM3_B	—	A9
IP5[15:12]	DU0_DG2	Reserved	RX4_D	—	—	—	A10
IP5[19:16]	DU0_DG3	Reserved	TX4_D	—	PWM4_B	—	A11
IP5[23:20]	DU0_DG4	Reserved	HRX0_A	—	—	—	A12
IP5[27:24]	DU0_DG5	Reserved	HTX0_A	—	PWM5_B	—	A13
IP5[31:28]	DU0_DG6	Reserved	HRX1_C	—	—	—	A14

Legend: — Setting disabled

5.3.14 Peripheral Function Select Register 6 (IPSR6)

Function: IPSR6 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP6 [31]	IP6 [30]	IP6 [29]	IP6 [28]	IP6 [27]	IP6 [26]	IP6 [25]	IP6 [24]	IP6 [23]	IP6 [22]	IP6 [21]	IP6 [20]	IP6 [19]	IP6 [18]	IP6 [17]	IP6 [16]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP6 [15]	IP6 [14]	IP6 [13]	IP6 [12]	IP6 [11]	IP6 [10]	IP6 [9]	IP6 [8]	IP6 [7]	IP6 [6]	IP6 [5]	IP6 [4]	IP6 [3]	IP6 [2]	IP6 [1]	IP6 [0]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'6666 6666	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP6[3:0]	DU0_DG7	Reserved	HTX1_C	—	PWM6_B	—	A15
IP6[7:4]	DU0_DB0	Reserved	—	SCL4_D	CAN0_RX_C	—	A16
IP6[11:8]	DU0_DB1	Reserved	—	SDA4_D	CAN0_TX_C	—	A17
IP6[15:12]	DU0_DB2	Reserved	HCTS0#	—	—	—	A18
IP6[19:16]	DU0_DB3	Reserved	HRTS0#	—	—	—	A19
IP6[23:20]	DU0_DB4	Reserved	HCTS1#_C	Reserved	—	—	A20
IP6[27:24]	DU0_DB5	Reserved	HRTS1#_C	Reserved	—	—	A21
IP6[31:28]	DU0_DB6	Reserved	—	Reserved	—	—	A22

Legend: — Setting disabled

5.3.15 Peripheral Function Select Register 7 (IPSR7)

Function: IPSR7 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP7 [31]	IP7 [30]	IP7 [29]	IP7 [28]	IP7 [27]	IP7 [26]	IP7 [25]	IP7 [24]	IP7 [23]	IP7 [22]	IP7 [21]	IP7 [20]	IP7 [19]	IP7 [18]	IP7 [17]	IP7 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP7 [15]	IP7 [14]	IP7 [13]	IP7 [12]	IP7 [11]	IP7 [10]	IP7 [9]	IP7 [8]	IP7 [7]	IP7 [6]	IP7 [5]	IP7 [4]	IP7 [3]	IP7 [2]	IP7 [1]	IP7 [0]
Initial value:	0	1	1	0	0	1	1	0	0	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 6666	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP7[3:0]	DU0_DB7	Reserved	—	Reserved	—	—	A23
IP7[7:4]	DU0_DOTCLKIN	Reserved	—	—	—	—	A24
IP7[11:8]	DU0_DOTCLKOUT0	Reserved	—	—	—	—	A25
IP7[15:12]	DU0_DOTCLKOUT1	Reserved	MSIOF2_RXD_B	—	—	—	CS1#/A26
IP7[19:16]	DU0_EXHSYNC/ DU0_HSYNC	Reserved	MSIOF2_TXD_B	—	—	—	DREQ0#
IP7[23:20]	DU0_EXVSYNC/ DU0_VSYNC	Reserved	MSIOF2_SYNC_B	—	—	—	DACK0
IP7[27:24]	DU0_EXODDF/DU0 _ODDF_DISP_CDE	Reserved	MSIOF2_SCK_B	—	—	—	DRACK0
IP7[31:28]	DU0_DISP	Reserved	—	—	CAN1_RX_C	—	—

Legend: — Setting disabled

5.3.16 Peripheral Function Select Register 8 (IPSR8)

Function: IPSR8 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP8 [31]	IP8 [30]	IP8 [29]	IP8 [28]	IP8 [27]	IP8 [26]	IP8 [25]	IP8 [24]	IP8 [23]	IP8 [22]	IP8 [21]	IP8 [20]	IP8 [19]	IP8 [18]	IP8 [17]	IP8 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP8 [15]	IP8 [14]	IP8 [13]	IP8 [12]	IP8 [11]	IP8 [10]	IP8 [9]	IP8 [8]	IP8 [7]	IP8 [6]	IP8 [5]	IP8 [4]	IP8 [3]	IP8 [2]	IP8 [1]	IP8 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP8[3:0]	DU0_CDE	Reserved	—	—	CAN1_TX_C	—	—
IP8[7:4]	VI1_CLK	—	—	—	AVB_RX_CLK	ETH_REF_CLK	—
IP8[11:8]	VI1_DATA0	—	—	—	AVB_RX_DV	ETH_CRS_DV	—
IP8[15:12]	VI1_DATA1	—	—	—	AVB_RXD0	ETH_RXD0	—
IP8[19:16]	VI1_DATA2	—	—	—	AVB_RXD1	ETH_RXD1	—
IP8[23:20]	VI1_DATA3	—	—	—	AVB_RXD2	ETH_MDIO	—
IP8[27:24]	VI1_DATA4	—	—	—	AVB_RXD3	ETH_RX_ER	—
IP8[31:28]	VI1_DATA5	—	—	—	AVB_RXD4	ETH_LINK	—

Legend: — Setting disabled

5.3.17 Peripheral Function Select Register 9 (IPSR9)

Function: IPSR9 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP9 [31]	IP9 [30]	IP9 [29]	IP9 [28]	IP9 [27]	IP9 [26]	IP9 [25]	IP9 [24]	IP9 [23]	IP9 [22]	IP9 [21]	IP9 [20]	IP9 [19]	IP9 [18]	IP9 [17]	IP9 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP9 [15]	IP9 [14]	IP9 [13]	IP9 [12]	IP9 [11]	IP9 [10]	IP9 [9]	IP9 [8]	IP9 [7]	IP9 [6]	IP9 [5]	IP9 [4]	IP9 [3]	IP9 [2]	IP9 [1]	IP9 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP9[3:0]	VI1_DATA6	—	—	—	AVB_RXD5	ETH_TXD1	—
IP9[7:4]	VI1_DATA7	—	—	—	AVB_RXD6	ETH_TX_EN	—
IP9[11:8]	VI1_CLKENB	SCL3_A	—	—	AVB_RXD7	ETH_MAGIC	—
IP9[15:12]	VI1_FIELD	SDA3_A	—	—	AVB_RX_ER	ETH_TXD0	—
IP9[19:16]	VI1_HSYNC#	RX0_B	SCL0_C	—	AVB_GTXREFCLK	ETH_MDC	—
IP9[23:20]	VI1_VSYNC#	TX0_B	SDA0_C	AUDIO_CLKOUT_B	AVB_TX_CLK	—	—
IP9[27:24]	VI1_DATA8	—	—	SCL2_B	AVB_TX_EN	—	—
IP9[31:28]	VI1_DATA9	—	—	SDA2_B	AVB_TXD0	—	—

Legend: — Setting disabled

5.3.18 Peripheral Function Select Register 10 (IPSR10)

Function: IPSR10 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP10 [31]	IP10 [30]	IP10 [29]	IP10 [28]	IP10 [27]	IP10 [26]	IP10 [25]	IP10 [24]	IP10 [23]	IP10 [22]	IP10 [21]	IP10 [20]	IP10 [19]	IP10 [18]	IP10 [17]	IP10 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP10 [15]	IP10 [14]	IP10 [13]	IP10 [12]	IP10 [11]	IP10 [10]	IP10 [9]	IP10 [8]	IP10 [7]	IP10 [6]	IP10 [5]	IP10 [4]	IP10 [3]	IP10 [2]	IP10 [1]	IP10 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP10[3:0]	VI1_DATA10	—	—	CAN0_RX_B	AVB_TXD1	—	—	—
IP10[7:4]	VI1_DATA11	—	—	CAN0_TX_B	AVB_TXD2	—	—	—
IP10[11:8]	AVB_TXD3	—	AUDIO_CLKA_B	—	SSI_SCK1_D	RX5_F	MSIOF0_RXD_B	—
IP10[15:12]	AVB_TXD4	—	AUDIO_CLKB_B	—	SSI_WS1_D	TX5_F	MSIOF0_TXD_B	—
IP10[19:16]	AVB_TXD5	SCIF_CLK_B	AUDIO_CLKC_B	—	SSI_SDATA1_D	—	MSIOF0_SCK_B	—
IP10[23:20]	SCL0_A	RX0_C	PWM5_A	TCLK1_B	AVB_TXD6	CAN1_RX_D	MSIOF0_SYNC_B	—
IP10[27:24]	SDA0_A	TX0_C	IRQ5	CAN_CLK_A	AVB_GTX_CLK	CAN1_TX_D	DVC_MUTE	—
IP10[31:28]	SCL1_A	RX4_A	PWM5_D	DU1_DR0	—	—	SSI_SCK6_B	VI0_G0

Legend: — Setting disabled

5.3.19 Peripheral Function Select Register 11 (IPSR11)

Function: IPSR11 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP11 [31]	IP11 [30]	IP11 [29]	IP11 [28]	IP11 [27]	IP11 [26]	IP11 [25]	IP11 [24]	IP11 [23]	IP11 [22]	IP11 [21]	IP11 [20]	IP11 [19]	IP11 [18]	IP11 [17]	IP11 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP11 [15]	IP11 [14]	IP11 [13]	IP11 [12]	IP11 [11]	IP11 [10]	IP11 [9]	IP11 [8]	IP11 [7]	IP11 [6]	IP11 [5]	IP11 [4]	IP11 [3]	IP11 [2]	IP11 [1]	IP11 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP11[3:0]	SDA1_A	TX4_A	—	DU1_DR1	—	—	SSI_WS6_B	VI0_G1
IP11[7:4]	MSIOF0_RXD_A	RX5_A	SCL2_C	DU1_DR2	—	QSPI1_MOSI/ QSPI1_IO0	SSI_SDATA6_B	VI0_G2
IP11[11:8]	MSIOF0_TXD_A	TX5_A	SDA2_C	DU1_DR3	—	QSPI1_MISO/ QSPI1_IO1	SSI_WS78_B	VI0_G3
IP11[15:12]	MSIOF0_SCK_A	IRQ0	Reserved	DU1_DR4	Reserved	QSPI1_SPCLK	SSI_SCK78_B	VI0_G4
IP11[19:16]	MSIOF0_SYNC_A	PWM1_A	Reserved	DU1_DR5	Reserved	QSPI1_IO2	SSI_SDATA7_B	—
IP11[23:20]	MSIOF0_SS1_A	—	Reserved	DU1_DR6	Reserved	QSPI1_IO3	SSI_SDATA8_B	—
IP11[27:24]	MSIOF0_SS2_A	—	Reserved	DU1_DR7	Reserved	QSPI1_SSL	—	—
IP11[31:28]	HRX1_A	SCL4_A	PWM6_A	DU1_DG0	RX0_A	—	—	—

Legend: — Setting disabled

5.3.20 Peripheral Function Select Register 12 (IPSR12)

Function: IPSR12 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP12 [31]	IP12 [30]	IP12 [29]	IP12 [28]	IP12 [27]	IP12 [26]	IP12 [25]	IP12 [24]	IP12 [23]	IP12 [22]	IP12 [21]	IP12 [20]	IP12 [19]	IP12 [18]	IP12 [17]	IP12 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP12 [15]	IP12 [14]	IP12 [13]	IP12 [12]	IP12 [11]	IP12 [10]	IP12 [9]	IP12 [8]	IP12 [7]	IP12 [6]	IP12 [5]	IP12 [4]	IP12 [3]	IP12 [2]	IP12 [1]	IP12 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP12 [3:0]	HTX1_A	SDA4_A	—	DU1_DG1	TX0_A	—	—
IP12 [7:4]	HCTS1#_A	PWM2_A	—	DU1_DG2	REMOCON_B	—	—
IP12 [11:8]	HRTS1#_A	—	—	DU1_DG3	SSI_WS1_B	IRQ1	—
IP12 [15:12]	SD2_CLK	HSCK1	—	DU1_DG4	SSI_SCK1_B	—	—
IP12 [19:16]	SD2_CMD	SCIF1_SCK_A	TCLK2_A	DU1_DG5	SSI_SCK2_B	PWM3_A	—
IP12 [23:20]	SD2_DAT0	RX1_A	SCL1_E	DU1_DG6	SSI_SDATA1_B	—	—
IP12 [27:24]	SD2_DAT1	TX1_A	SDA1_E	DU1_DG7	SSI_WS2_B	—	—
IP12 [31:28]	SD2_DAT2	RX2_A	—	DU1_DB0	SSI_SDATA2_B	—	—

Legend: — Setting disabled

5.3.21 Peripheral Function Select Register 13 (IPSR13)

Function: IPSR13 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP13 [31]	IP13 [30]	IP13 [29]	IP13 [28]	IP13 [27]	IP13 [26]	IP13 [25]	IP13 [24]	IP13 [23]	IP13 [22]	IP13 [21]	IP13 [20]	IP13 [19]	IP13 [18]	IP13 [17]	IP13 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP13 [15]	IP13 [14]	IP13 [13]	IP13 [12]	IP13 [11]	IP13 [10]	IP13 [9]	IP13 [8]	IP13 [7]	IP13 [6]	IP13 [5]	IP13 [4]	IP13 [3]	IP13 [2]	IP13 [1]	IP13 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP13 [3:0]	SD2_DAT3	TX2_A	—	DU1_DB1	SSI_WS9_B	—	—
IP13 [7:4]	SD2_CD	SCIF2_SCK_A	—	DU1_DB2	SSI_SCK9_B	—	—
IP13 [11:8]	SD2_WP	SCIF3_SCK	—	DU1_DB3	SSI_SDATA9_B	—	—
IP13 [15:12]	RX3_A	SCL1_C	MSIOF1_RXD_B	DU1_DB4	AUDIO_CLKA_C	SSI_SDATA4_B	—
IP13 [19:16]	TX3_A	SDA1_C	MSIOF1_TXD_B	DU1_DB5	AUDIO_CLKB_C	SSI_WS4_B	—
IP13 [23:20]	SCL2_A	—	MSIOF1_SCK_B	DU1_DB6	AUDIO_CLKC_C	SSI_SCK4_B	—
IP13 [27:24]	SDA2_A	—	MSIOF1_SYNC_B	DU1_DB7	AUDIO_CLKOUT_C	—	—
IP13 [31:28]	SSI_SCK5_A	—	—	DU1_DOTCLKOUT1	—	—	—

Legend: — Setting disabled

5.3.22 Peripheral Function Select Register 14 (IPSR14)

Function: IPSR14 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP14 [31]	IP14 [30]	IP14 [29]	IP14 [28]	IP14 [27]	IP14 [26]	IP14 [25]	IP14 [24]	IP14 [23]	IP14 [22]	IP14 [21]	IP14 [20]	IP14 [19]	IP14 [18]	IP14 [17]	IP14 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP14 [15]	IP14 [14]	IP14 [13]	IP14 [12]	IP14 [11]	IP14 [10]	IP14 [9]	IP14 [8]	IP14 [7]	IP14 [6]	IP14 [5]	IP14 [4]	IP14 [3]	IP14 [2]	IP14 [1]	IP14 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP14 [3:0]	SSI_WS5_A	—	SCL3_C	DU1_DOTCLKIN	—	—	—
IP14 [7:4]	SSI_SDATA5_A	—	SDA3_C	DU1_DOTCLKOUT0	—	—	—
IP14 [11:8]	SSI_SCK6_A	—	—	DU1_EXODDF/ DU1_ODDF_DISP_CDE	—	—	—
IP14 [15:12]	SSI_WS6_A	—	SCL4_C	DU1_EXHSYNC/ DU1_HSYNC	—	—	—
IP14 [19:16]	SSI_SDATA6_A	—	SDA4_C	DU1_EXVSYNC/ DU1_VSYNC	—	—	—
IP14 [23:20]	SSI_SCK78_A	—	SDA4_E	DU1_DISP	—	—	—
IP14 [27:24]	SSI_WS78_A	—	SCL4_E	DU1_CDE	—	—	—
IP14 [31:28]	SSI_SDATA7_A	—	—	IRQ8	AUDIO_CLKA_D	CAN_CLK_D	VI0_G5

Legend: — Setting disabled

5.3.23 Peripheral Function Select Register 15 (IPSR15)

Function: IPSR15 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP15 [31]	IP15 [30]	IP15 [29]	IP15 [28]	IP15 [27]	IP15 [26]	IP15 [25]	IP15 [24]	IP15 [23]	IP15 [22]	IP15 [21]	IP15 [20]	IP15 [19]	IP15 [18]	IP15 [17]	IP15 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP15 [15]	IP15 [14]	IP15 [13]	IP15 [12]	IP15 [11]	IP15 [10]	IP15 [9]	IP15 [8]	IP15 [7]	IP15 [6]	IP15 [5]	IP15 [4]	IP15 [3]	IP15 [2]	IP15 [1]	IP15 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP15 [3:0]	SSI_SCK0129_A	MSIOF1_RXD_A	RX5_D	—	—	—	VI0_G6
IP15 [7:4]	SSI_WS0129_A	MSIOF1_TXD_A	TX5_D	—	—	—	VI0_G7
IP15 [11:8]	SSI_SDATA0_A	MSIOF1_SYNC_A	PWM0_C	—	—	—	VI0_R0
IP15 [15:12]	SSI_SCK34	MSIOF1_SCK_A	AVB_MDC	—	—	DACK1	VI0_R1
IP15 [19:16]	SSI_WS34	MSIOF1_SS1_A	AVB_MDIO	—	CAN1_RX_A	DREQ1#	VI0_R2
IP15 [23:20]	SSI_SDATA3	MSIOF1_SS2_A	AVB_LINK	—	CAN1_TX_A	DREQ2#	VI0_R3
IP15 [27:24]	SSI_SCK4_A	—	AVB_MAGIC	—	—	—	VI0_R4
IP15 [31:28]	SSI_WS4_A	—	AVB_PHY_INT	—	—	—	VI0_R5

Legend: — Setting disabled

5.3.24 Peripheral Function Select Register 16 (IPSR16)

Function: IPSR16 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IP16 [31]	IP16 [30]	IP16 [29]	IP16 [28]	IP16 [27]	IP16 [26]	IP16 [25]	IP16 [24]	IP16 [23]	IP16 [22]	IP16 [21]	IP16 [20]	IP16 [19]	IP16 [18]	IP16 [17]	IP16 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP16 [15]	IP16 [14]	IP16 [13]	IP16 [12]	IP16 [11]	IP16 [10]	IP16 [9]	IP16 [8]	IP16 [7]	IP16 [6]	IP16 [5]	IP16 [4]	IP16 [3]	IP16 [2]	IP16 [1]	IP16 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)	Function 8 (Set Value = H'7)
IP16[3:0]	SSI_SDATA4_A	—	AVB_CRS	—	—	—	VI0_R6	—
IP16[7:4]	SSI_SCK1_A	SCIF1_SCK_B	PWM1_D	IRQ9	REMOCON_A	DACK2	VI0_CLK	AVB_COL
IP16[11:8]	SSI_SDATA8_A	RX1_B	—	—	CAN0_RX_D	AVB_AVTP_CAPTURE_B	VI0_R7	—
IP16[15:12]	SSI_WS1_A	TX1_B	—	—	CAN0_TX_D	AVB_AVTP_MATCH_B	VI0_DATA0_VI0_B0	—
IP16[19:16]	SSI_SDATA1_A	HRX1_B	—	—	—	—	VI0_DATA1_VI0_B1	—
IP16[23:20]	SSI_SCK2_A	HTX1_B	—	—	—	AVB_TXD7	VI0_DATA2_VI0_B2	—
IP16[27:24]	SSI_WS2_A	HCTS1#_B	—	—	—	AVB_TX_ER	VI0_DATA3_VI0_B3	—
IP16[31:28]	SSI_SDATA2_A	HRTS1#_B	—	—	—	—	VI0_DATA4_VI0_B4	—

Legend: — Setting disabled

5.3.25 Peripheral Function Select Register 17 (IPSR17)

Function: IPSR17 selects the functions of the multiplexed LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	IP17 [27]	IP17 [26]	IP17 [25]	IP17 [24]	IP17 [23]	IP17 [22]	IP17 [21]	IP17 [20]	IP17 [19]	IP17 [18]	IP17 [17]	IP17 [16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IP17 [15]	IP17 [14]	IP17 [13]	IP17 [12]	IP17 [11]	IP17 [10]	IP17 [9]	IP17 [8]	IP17 [7]	IP17 [6]	IP17 [5]	IP17 [4]	IP17 [3]	IP17 [2]	IP17 [1]	IP17 [0]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	The functions of the LSI pins are selected according to the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function 1 (Set Value = H'0)	Function 2 (Set Value = H'1)	Function 3 (Set Value = H'2)	Function 4 (Set Value = H'3)	Function 5 (Set Value = H'4)	Function 6 (Set Value = H'5)	Function 7 (Set Value = H'6)
IP17 [3:0]	SSI_SCK9_A	RX2_B	SCL3_E	—	—	EX_WAIT1	VI0_DATA5_VI0_B5
IP17 [7:4]	SSI_WS9_A	TX2_B	SDA3_E	—	—	—	VI0_DATA6_VI0_B6
IP17 [11:8]	SSI_SDATA9_A	SCIF2_SCK_B	PWM2_D	—	—	—	VI0_DATA7_VI0_B7
IP17 [15:12]	AUDIO_CLKA_A	SCL0_B	Reserved	—	—	—	VI0_CLKENB
IP17 [19:16]	AUDIO_CLKB_A	SDA0_B	Reserved	—	—	—	VI0_FIELD
IP17 [23:20]	AUDIO_CLKC_A	SCL4_B	Reserved	—	—	—	VI0_HSYNC#
IP17 [27:24]	AUDIO_CLKOUT_A	SDA4_B	Reserved	—	—	—	VI0_VSYNC#
IP17 [31:28]	—	—	—	—	—	—	—

Legend: — Setting disabled

5.3.26 Module Select Register 0 (MOD_SEL0)

Function: MOD_SEL selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the ADG, CAN, I2C, and AVB is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group. Correct operation is not guaranteed when a pin is used in combination with pins from other groups.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	sel_adga_1	sel_adga_0	—	—	sel_canclk_1	sel_canclk_0	sel_can1_1	sel_can1_0	sel_can0_1	sel_can0_0	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_i2c04_2	sel_i2c04_1	sel_i2c04_0	sel_i2c03_2	sel_i2c03_1	sel_i2c03_0	—	sel_i2c02_1	sel_i2c02_0	sel_i2c01_2	sel_i2c01_1	sel_i2c01_0	sel_i2c00_2	sel_i2c00_1	sel_i2c00_0	sel_avb
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function Name	LSI pin name (Group A) Set value: 0	LSI pin name (Group B) Set value: 1	LSI pin name (Group C) Set value 2	LSI pin name (Group D) Set value 3	LSI pin name (Group E) Set value 4
sel_adga[1:0]	AUDIO_CLKA	AUDIO_CLKA_A	AVB_TXD3	RX3_A	SSI_SDATA7_A	—
sel_canclk[1:0]	CAN_CLK	SDA0_A	EX_WAIT0	D12	SSI_SDATA7_A	—
sel_can1[1:0]	CAN1_RX	SSI_WS34	D14	DU0_DISP	SCL0_A	—
	CAN1_TX	SSI_SDATA3	D15	DU0_CDE	SDA0_A	—
sel_can0[1:0]	CAN0_RX	SD0_CD	VI1_DATA10	DU0_DB0	SSI_SDATA8_A	—
	CAN0_TX	SD0_WP	VI1_DATA11	DU0_DB1	SSI_WS1_A	—
sel_i2c04 [2:0]	SCL4	HRX1_A	AUDIO_CLKC_A	SSI_WS6_A	DU0_DB0	SSI_SCK78_A
	SDA4	HTX1_A	AUDIO_CLKOUT_A	SSI_SDATA6_A	DU0_DB1	SSI_WS78_A
sel_i2c03 [2:0]	SCL3 SDA3	VI1_CLKENB	D0	SSI_WS5_A	DU0_DG0	SSI_SCK9_A
		VI1_FIELD	D1	SSI_SDATA5_A	DU0_DG1	SSI_WS9_A
sel_i2c02 [1:0]	SCL2	SCL2_A	VI1_DATA8	MSIOF0_RXD_A	DU0_DR0	—
	SDA2	SDA2_A	VI1_DATA9	MSIOF0_TXD_A	DU0_DR1	—
sel_i2c01 [2:0]	SCL1	SCL1_A	D5	RX3_A	D8	SD2_DAT0
	SDA1	SDA1_A	D6	TX3_A	D9	SD2_DAT1
sel_i2c00 [2:0]	SCL0	SCL0_A	AUDIO_CLKA_A	VI1_HSYNC#	D2	DU0_DR2
	SDA0	SDA0_A	AUDIO_CLKB_A	VI1_VSYNC#	D3	DU0_DR3
sel_avb	AVB_AVTP_CAPTURE	D14	SSI_SDATA8_A	—	—	—
	AVB_AVTP_MATCH	D15	SSI_WS1_A	—	—	—

Legend: — Setting disabled

5.3.27 Module Select Register 1 (MOD_SEL1)

Function: MOD_SEL1 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the SCIF, MSIOF, RCN, TMU and HSCIF is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	sel_scif clk	sel_scif 5_2	sel_scif 5_1	sel_scif 5_0	sel_scif 4_2	sel_scif 4_1	sel_scif 4_0	sel_scif 3_1	sel_scif 3_0	sel_scif 2_1	sel_scif 2_0	sel_scif 2_clk	sel_scif 1_1	sel_scif 1_0	sel_scif 0_1	sel_scif 0_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_msiof2_1	sel_msiof2_0	—	sel_msiof1_0	—	sel_msiof0_0	sel_rcn	—	—	sel_tmu2	sel_tmu1	—	—	sel_hscif1_1	sel_hscif1_0	sel_hscif0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function Name	LSI pin name (Group A) (Set Value = 0)	LSI pin name (Group B) (Set Value = 1)	LSI pin name (Group C) (Set Value = 2)	LSI pin name (Group D) (Set Value = 3)	LSI pin name (Group E) (Set Value = 4)	LSI pin name (Group F) (Set Value = 5)
sel_scifclk	SCIF_CLK	EX_WAIT0	AVB_TXD5	—	—	—	—
sel_scif5 [2:0]	RX5	MSIOF0_RXD_A	D0	DU0_DR0	SSI_SCK0129_A	SD0_DAT2	AVB_TXD3
	TX5	MSIOF0_TXD_A	D1	DU0_DR1	SSI_WS0129_A	SD0_DAT3	AVB_TXD4
sel_scif4 [2:0]	RX4	SCL1_A	D2	D13	DU0_DG2	SD0_DAT0	—
	TX4	SDA1_A	D3	D14	DU0_DG3	SD0_DAT1	—
sel_scif3 [1:0]	RX3	RX3_A	DU0_DG0	SD0_CLK	—	—	—
	TX3	TX3_A	DU0_DG1	SD0_CMD	—	—	—
sel_scif2 [1:0]	RX2	SD2_DAT2	SSI_SCK9_A	DU0_DR6	—	—	—
	TX2	SD2_DAT3	SSI_WS9_A	DU0_DR7	—	—	—
sel_scif2_clk	SCIF2_SCK	SD2_CD	SSI_SDATA9_A	—	—	—	—
sel_scif1 [1:0]	RX1	SD2_DAT0	SSI_SDATA8_A	D8	DU0_DR4	—	—
	TX1	SD2_DAT1	SSI_WS1_A	D9	DU0_DR5	—	—
	SCIF1_SCK	SD2_CMD	SSI_SCK1_A	D7	—	—	—
sel_scif0 [1:0]	RX0	HRX1_A	VI1_HSYNC#	SCL0_A	DU0_DR2	—	—
	TX0	HTX1_A	VI1_VSYNC#	SDA0_A	DU0_DR3	—	—
sel_msiof2 [1:0]	MSIOF2_RXD	D10	DU0_DOTCLKOUT1	D0	—	—	—
	MSIOF2_TXD	D11	DU0_EXHSYNC/DU0_HSYNC	D1	—	—	—
	MSIOF2_SYNC	D13	DU0_EXVSYNC/DU0_VSYNC	D3	—	—	—
	MSIOF2_SCK	D12	DU0_EXODDF/DU0_ODDF_DISP_CDE	D2	—	—	—
	MSIOF2_SS1	D14	—	—	—	—	—
	MSIOF2_SS2	D15	—	—	—	—	—

Bit Name	Function Name	LSI pin name (Group A) (Set Value = 0)	LSI pin name (Group B) (Set Value = 1)	LSI pin name (Group C) (Set Value = 2)	LSI pin name (Group D) (Set Value = 3)	LSI pin name (Group E) (Set Value = 4)	LSI pin name (Group F) (Set Value = 5)
sel_msiof1	MSIOF1_RXD	SSI_SCK0129_A	RX3_A	—	—	—	—
	MSIOF1_TXD	SSI_WS0129_A	TX3_A	—	—	—	—
	MSIOF1_SCK	SSI_SCK34	SCL2_A	—	—	—	—
	MSIOF1_SYNC	SSI_SDATA0_A	SDA2_A	—	—	—	—
	MSIOF1_SS1	SSI_WS34	—	—	—	—	—
	MSIOF1_SS2	SSI_SDATA3	—	—	—	—	—
sel_msiof0	MSIOF0_RXD	MSIOF0_RXD_A	AVB_TXD3	—	—	—	—
	MSIOF0_TXD	MSIOF0_TXD_A	AVB_TXD4	—	—	—	—
	MSIOF0_SCK	MSIOF0_SCK_A	AVB_TXD5	—	—	—	—
	MSIOF0_SYNC	MSIOF0_SYNC_A	SCL0_A	—	—	—	—
	MSIOF0_SS1	MSIOF0_SS1	—	—	—	—	—
	MSIOF0_SS2	MSIOF0_SS2	—	—	—	—	—
sel_rcn	REMOCON	SSI_SCK1_A	HCTS1#_A	—	—	—	—
sel_tmu2	TCLK2	SD2_CMD	D5	—	—	—	—
sel_tmu1	TCLK1	D4	SCL0_A	—	—	—	—
sel_hscif1 [1:0]	HRX1	HRX1_A	SSI_SDATA1_A	DU0_DG6	—	—	—
	HTX1	HTX1_A	SSI_SCK2_A	DU0_DG7	—	—	—
	HCTS1#	HCTS1#_A	SSI_WS2_A	DU0_DB4	—	—	—
	HRTS1#	HRTS1#_A	SSI_SDATA2_A	DU0_DB5	—	—	—
sel_hscif0	HRX0	DU0_DG4	D10	—	—	—	—
	HTX0	DU0_DG5	D11	—	—	—	—
	HCTS0#	DU0_DB2	—	—	—	—	—
	HRTS0#	DU0_DB3	—	—	—	—	—

Legend: — Setting disabled

5.3.28 Module Select Register 2 (MOD_SEL2)

Function: MOD_SEL2 selects the group for multiple LSI pins with multiplexed pin functions.

Each input or input/output signal of the ADG and SSI is assigned to two or more groups of pins. Select one of these groups when using these signals. Do not use the module pins in the unselected group; if a module pin in the unselected group is used, correct operation is not guaranteed.

For some modules, however, although the output signals are assigned to two or more groups of pins, there is no bit for selecting the group. Select one of these pins for each output signal through the corresponding peripheral function select register. Also note that each pin can only be used in combination with the other input or input/output pins of the same group.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	sel_adgb_1	sel_adgb_0	sel_adgc_1	sel_adgc_0	sel_ssi9_1	sel_ssi9_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	sel_ssi8_1	sel_ssi8_0	sel_ssi7_1	sel_ssi7_0	sel_ssi6_1	sel_ssi6_0	sel_ssi5_1	sel_ssi5_0	sel_ssi4_1	sel_ssi4_0	sel_ssi2_1	sel_ssi2_0	sel_ssi1_1	sel_ssi1_0	sel_ssi_0_1	sel_ssi_0_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Initial Value	R/W	Description
31 to 0	H'0000 0000	R/W	These bits select multiplexed pin functions as indicated in the table below.

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Bit Name	Function Name	LSI pin name (Group A) (Set Value = 0)	LSI pin name (Group B) (Set Value = 1)	LSI pin name (Group C) (Set Value = 2)	LSI pin name (Group D) (Set Value = 3)	LSI pin name (Group E) (Set Value = 4)	LSI pin name (Group F) (Set Value = 5)
sel_adgb [1:0]	AUDIO_CLKB	AUDIO_CLKB_A	AVB_TXD4	TX3_A	—	—	—
sel_adgc [1:0]	AUDIO_CLKC	AUDIO_CLKC_A	AVB_TXD5	SCL2_A	—	—	—
sel_ssi9 [1:0]	SSI_SCK9	SSI_SCK9_A	SD2_CD	—	—	—	—
	SSI_WS9	SSI_WS9_A	SD2_DAT3	—	—	—	—
	SSI_SDATA9	SSI_SDATA9_A	SD2_WP	—	—	—	—
sel_ssi8 [1:0]	SSI_WS78	SSI_WS78_A	MSIOF0_TXD_A	—	—	—	—
	SSI_SCK78	SSI_SCK78_A	MSIOF0_SCK_A	—	—	—	—
	SSI_SDATA8	SSI_SDATA8_A	MSIOF0_SS1_A	—	—	—	—
sel_ssi7 [1:0]	SSI_WS78	SSI_WS78_A	MSIOF0_TXD_A	—	—	—	—
	SSI_SCK78	SSI_SCK78_A	MSIOF0_SCK_A	—	—	—	—
	SSI_SDATA7	SSI_SDATA7_A	MSIOF0_SYNC_A	—	—	—	—
sel_ssi6 [1:0]	SSI_SCK6	SSI_SCK6_A	SCL1_A	—	—	—	—
	SSI_WS6	SSI_WS6_A	SDA1_A	—	—	—	—
	SSI_SDATA6	SSI_SDATA6_A	MSIOF0_RXD_A	—	—	—	—
sel_ssi5 [1:0]	SSI_SCK5	SSI_SCK5_A	D2	—	—	—	—
	SSI_WS5	SSI_WS5_A	D1	—	—	—	—
	SSI_SDATA5	SSI_SDATA5_A	D0	—	—	—	—
sel_ssi4 [1:0]	SSI_SCK4	SSI_SCK4_A	SCL2_A	—	—	—	—
	SSI_WS4	SSI_WS4_A	TX3_A	—	—	—	—
	SSI_SDATA4	SSI_SDATA4_A	RX3_A	—	—	—	—
sel_ssi2 [1:0]	SSI_SCK2	SSI_SCK2_A	SD2_CMD	—	—	—	—
	SSI_WS2	SSI_WS2_A	SD2_DAT1	—	—	—	—
	SSI_SDATA2	SSI_SDATA2_A	SD2_DAT2	—	—	—	—

Bit Name	Function Name	LSI pin name (Group A) (Set Value = 0)	LSI pin name (Group B) (Set Value = 1)	LSI pin name (Group C) (Set Value = 2)	LSI pin name (Group D) (Set Value = 3)	LSI pin name (Group E) (Set Value = 4)	LSI pin name (Group F) (Set Value = 5)
sel_ssi1 [1:0]	SSI_SCK1	SSI_SCK1_A	SD2_CLK	SD0_CLK	AVB_TXD3	—	—
	SSI_WS1	SSI_WS1_A	HRTS1#_A	SD0_CMD	AVB_TXD4	—	—
	SSI_SDATA1	SSI_SDATA1_A	SD2_DAT0	SD0_DAT0	AVB_TXD5	—	—
sel_ssi0 [1:0]	SSI_SCK0129	SSI_SCK0129_A	SD0_DAT1	—	—	—	—
	SSI_WS0129	SSI_WS0129_A	SD0_DAT2	—	—	—	—
	SSI_SDATA0	SSI_SDATA0_A	SD0_DAT3	—	—	—	—

Legend: — Setting disabled

5.3.29 LSI Pin Pull-Up Control Register 0 (PUPR0)

Function: PUPR0 performs on/off control of the pull-up resistors.

Note: When these pins are used as I2C interface, external pull-up resistors are mandatory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR0 [31]	PUPR0 [30]	PUPR0 [29]	PUPR0 [28]	PUPR0 [27]	PUPR0 [26]	PUPR0 [25]	PUPR0 [24]	PUPR0 [23]	PUPR0 [22]	PUPR0 [21]	PUPR0 [20]	PUPR0 [19]	PUPR0 [18]	PUPR0 [17]	PUPR0 [16]
Initial value:	0	1	1	1	1	0	1	0	1	0	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR0 [15]	PUPR0 [14]	PUPR0 [13]	PUPR0 [12]	PUPR0 [11]	PUPR0 [10]	PUPR0 [9]	PUPR0 [8]	PUPR0 [7]	PUPR0 [6]	PUPR0 [5]	PUPR0 [4]	PUPR0 [3]	PUPR0 [2]	PUPR0 [1]	PUPR0 [0]
Initial value:	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR0[31:0]	H'7AA0 1801	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR0[31]	PRESETOUT# pin is pulled up
PUPR0[30]	TRST# pin is pulled up
PUPR0[29]	TCK pin is pulled up
PUPR0[28]	TMS pin is pulled up
PUPR0[27]	TDI pin is pulled up
PUPR0[26]	TDO pin is pulled up
PUPR0[25]	ACK pin is pulled down
PUPR0[24]	USB0_PWEN pin is pulled up
PUPR0[23]	USB0_OVC pin is pulled up
PUPR0[22]	USB1_PWEN pin is pulled up
PUPR0[21]	USB1_OVC pin is pulled up
PUPR0[20]	NMI pin is pulled up
PUPR0[19]	CLKOUT pin is pulled up
PUPR0[18]	SD0_CLK pin is pulled up
PUPR0[17]	SD0_CMD pin is pulled up
PUPR0[16]	SD0_DAT0 pin is pulled up
PUPR0[15]	SD0_DAT1 pin is pulled up
PUPR0[14]	SD0_DAT2 pin is pulled up
PUPR0[13]	SD0_DAT3 pin is pulled up
PUPR0[12]	SD0_CD pin is pulled up
PUPR0[11]	SD0_WP pin is pulled up
PUPR0[10]	MMC0_CLK pin is pulled up
PUPR0[9]	MMC0_CMD pin is pulled up
PUPR0[8]	MMC0_D0 pin is pulled up

Bit Name	Set Value = 1
PUPR0[7]	MMC0_D1 pin is pulled up
PUPR0[6]	MMC0_D2 pin is pulled up
PUPR0[5]	MMC0_D3 pin is pulled up
PUPR0[4]	MMC0_D4 pin is pulled up
PUPR0[3]	MMC0_D5 pin is pulled up
PUPR0[2]	MMC0_D6 pin is pulled up
PUPR0[1]	MMC0_D7 pin is pulled up
PUPR0[0]	D0 pin is pulled up

5.3.30 LSI Pin Pull-Up Control Register 1 (PUPR1)

Function: PUPR1 performs on/off control of the pull-up resistors.

Note: When these pins are used as I2C interface, external pull-up resistors are mandatory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR1 [31]	PUPR1 [30]	PUPR1 [29]	PUPR1 [28]	PUPR1 [27]	PUPR1 [26]	PUPR1 [25]	PUPR1 [24]	PUPR1 [23]	PUPR1 [22]	PUPR1 [21]	PUPR1 [20]	PUPR1 [19]	PUPR1 [18]	PUPR1 [17]	PUPR1 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR1 [15]	PUPR1 [14]	PUPR1 [13]	PUPR1 [12]	PUPR1 [11]	PUPR1 [10]	PUPR1 [9]	PUPR1 [8]	PUPR1 [7]	PUPR1 [6]	PUPR1 [5]	PUPR1 [4]	PUPR1 [3]	PUPR1 [2]	PUPR1 [1]	PUPR1 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR1[31:0]	H'FFFF FFC3	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR1[31]	D1 pin is pulled up
PUPR1[30]	D2 pin is pulled up
PUPR1[29]	D3 pin is pulled up
PUPR1[28]	D4 pin is pulled up
PUPR1[27]	D5 pin is pulled up
PUPR1[26]	D6 pin is pulled up
PUPR1[25]	D7 pin is pulled up
PUPR1[24]	D8 pin is pulled up
PUPR1[23]	D9 pin is pulled up
PUPR1[22]	D10 pin is pulled up
PUPR1[21]	D11 pin is pulled up
PUPR1[20]	D12 pin is pulled up
PUPR1[19]	D13 pin is pulled up
PUPR1[18]	D14 pin is pulled up
PUPR1[17]	D15 pin is pulled up
PUPR1[16]	QSPI0_SPCLK pin is pulled up
PUPR1[15]	QSPI0_MOSI/QSPI0_IO0 pin is pulled up
PUPR1[14]	QSPI0_MISO/QSPI0_IO1 pin is pulled up
PUPR1[13]	QSPI0_IO2 pin is pulled up
PUPR1[12]	QSPI0_IO3 pin is pulled up
PUPR1[11]	QSPI0_SSL pin is pulled up
PUPR1[10]	EX_WAIT0 pin is pulled up
PUPR1[9]	DU0_DR0 pin is pulled up
PUPR1[8]	DU0_DR1 pin is pulled up

Bit Name	Set Value = 1
PUPR1[7]	DU0_DR2 pin is pulled up
PUPR1[6]	DU0_DR3 pin is pulled up
PUPR1[5]	DU0_DR4 pin is pulled up
PUPR1[4]	DU0_DR5 pin is pulled up
PUPR1[3]	DU0_DR6 pin is pulled up
PUPR1[2]	DU0_DR7 pin is pulled up
PUPR1[1]	DU0_DG0 pin is pulled up
PUPR1[0]	DU0_DG1 pin is pulled up

5.3.31 LSI Pin Pull-Up Control Register 2 (PUPR2)

Function: PUPR2 performs on/off control of the pull-up resistors.

Note: When these pins are used as I2C interface, external pull-up resistors are mandatory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR2 [31]	PUPR2 [30]	PUPR2 [29]	PUPR2 [28]	PUPR2 [27]	PUPR2 [26]	PUPR2 [25]	PUPR2 [24]	PUPR2 [23]	PUPR2 [22]	PUPR2 [21]	PUPR2 [20]	PUPR2 [19]	PUPR2 [18]	PUPR2 [17]	PUPR2 [16]
Initial value:	0	0	0	0	0	0	1	1	0	0	1	1	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR2 [15]	PUPR2 [14]	PUPR2 [13]	PUPR2 [12]	PUPR2 [11]	PUPR2 [10]	PUPR2 [9]	PUPR2 [8]	PUPR2 [7]	PUPR2 [6]	PUPR2 [5]	PUPR2 [4]	PUPR2 [3]	PUPR2 [2]	PUPR2 [1]	PUPR2 [0]
Initial value:	1	0	0	1	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR2[31:0]	H'0333 93FF	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up/down function is disabled. 1: Pull-up/down function is enabled.

Bit Name	Set Value = 1
PUPR2[31]	DU0_DG2 pin is pulled up
PUPR2[30]	DU0_DG3 pin is pulled up
PUPR2[29]	DU0_DG4 pin is pulled up
PUPR2[28]	DU0_DG5 pin is pulled up
PUPR2[27]	DU0_DG6 pin is pulled up
PUPR2[26]	DU0_DG7 pin is pulled up
PUPR2[25]	DU0_DB0 pin is pulled up
PUPR2[24]	DU0_DB1 pin is pulled up
PUPR2[23]	DU0_DB2 pin is pulled up
PUPR2[22]	DU0_DB3 pin is pulled up
PUPR2[21]	DU0_DB4 pin is pulled up
PUPR2[20]	DU0_DB5 pin is pulled up
PUPR2[19]	DU0_DB6 pin is pulled up
PUPR2[18]	DU0_DB7 pin is pulled up
PUPR2[17]	DU0_DOTCLKIN pin is pulled up
PUPR2[16]	DU0_DOTCLKOUT0 pin is pulled up
PUPR2[15]	DU0_DOTCLKOUT1 pin is pulled up
PUPR2[14]	DU0_EXHSYNC/DU0_HSYNC pin is pulled up
PUPR2[13]	DU0_EXVSYNC/DU0_VSYNC pin is pulled up
PUPR2[12]	DU0_EXODDF/DU0_ODDF_DISP_CDE pin is pulled up
PUPR2[11]	DU0_DISP pin is pulled up
PUPR2[10]	DU0_CDE pin is pulled up
PUPR2[9]	VI1_CLK pin is pulled up
PUPR2[8]	VI1_DATA0 pin is pulled up

Bit Name	Set Value = 1
PUPR2[7]	VI1_DATA1 pin is pulled up
PUPR2[6]	VI1_DATA2 pin is pulled up
PUPR2[5]	VI1_DATA3 pin is pulled up
PUPR2[4]	VI1_DATA4 pin is pulled up
PUPR2[3]	VI1_DATA5 pin is pulled up
PUPR2[2]	VI1_DATA6 pin is pulled up
PUPR2[1]	VI1_DATA7 pin is pulled up
PUPR2[0]	VI1_CLKENB pin is pulled up

5.3.32 LSI Pin Pull-Up Control Register 3 (PUPR3)

Function: PUPR3 performs on/off control of the pull-up resistors.

Note: When these pins are used as I2C interface, external pull-up resistors are mandatory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR3 [31]	PUPR3 [30]	PUPR3 [29]	PUPR3 [28]	PUPR3 [27]	PUPR3 [26]	PUPR3 [25]	PUPR3 [24]	PUPR3 [23]	PUPR3 [22]	PUPR3 [21]	PUPR3 [20]	PUPR3 [19]	PUPR3 [18]	PUPR3 [17]	PUPR3 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR3 [15]	PUPR3 [14]	PUPR3 [13]	PUPR3 [12]	PUPR3 [11]	PUPR3 [10]	PUPR3 [9]	PUPR3 [8]	PUPR3 [7]	PUPR3 [6]	PUPR3 [5]	PUPR3 [4]	PUPR3 [3]	PUPR3 [2]	PUPR3 [1]	PUPR3 [0]
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR3[31:0]	H'FFFF FF03	R/W	Performs individual on/off control of the pull-up/down resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR3[31]	VI1_FIELD pin is pulled up
PUPR3[30]	VI1_HSYNC# pin is pulled up
PUPR3[29]	VI1_VSYNC# pin is pulled up
PUPR3[28]	VI1_DATA8 pin is pulled up
PUPR3[27]	VI1_DATA9 pin is pulled up
PUPR3[26]	VI1_DATA10 pin is pulled up
PUPR3[25]	VI1_DATA11 pin is pulled up
PUPR3[24]	AVB_TXD3 pin is pulled up
PUPR3[23]	AVB_TXD4 pin is pulled up
PUPR3[22]	AVB_TXD5 pin is pulled up
PUPR3[21]	SCL0_A pin is pulled up
PUPR3[20]	SDA0_A pin is pulled up
PUPR3[19]	SCL1_A pin is pulled up
PUPR3[18]	SDA1_A pin is pulled up
PUPR3[17]	MSIOF0_RXD_A pin is pulled up
PUPR3[16]	MSIOF0_TXD_A pin is pulled up
PUPR3[15]	MSIOF0_SCK_A pin is pulled up
PUPR3[14]	MSIOF0_SYNC_A pin is pulled up
PUPR3[13]	MSIOF0_SS1_A pin is pulled up
PUPR3[12]	MSIOF0_SS2_A pin is pulled up
PUPR3[11]	HRX1_A pin is pulled up
PUPR3[10]	HTX1_A pin is pulled up
PUPR3[9]	HCTS1#_A pin is pulled up
PUPR3[8]	HRTS1#_A pin is pulled up

Bit Name	Set Value = 1
PUPR3[7]	SD2_CLK pin is pulled up
PUPR3[6]	SD2_CMD pin is pulled up
PUPR3[5]	SD2_DAT0 pin is pulled up
PUPR3[4]	SD2_DAT1 pin is pulled up
PUPR3[3]	SD2_DAT2 pin is pulled up
PUPR3[2]	SD2_DAT3 pin is pulled up
PUPR3[1]	SD2_CD pin is pulled up
PUPR3[0]	SD2_WP pin is pulled up

5.3.33 LSI Pin Pull-Up Control Register 4 (PUPR4)

Function: PUPR4 performs on/off control of the pull-up resistors.

Note: When these pins are used as I2C interface, external pull-up resistors are mandatory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR4 [31]	PUPR4 [30]	PUPR4 [29]	PUPR4 [28]	PUPR4 [27]	PUPR4 [26]	PUPR4 [25]	PUPR4 [24]	PUPR4 [23]	PUPR4 [22]	PUPR4 [21]	PUPR4 [20]	PUPR4 [19]	PUPR4 [18]	PUPR4 [17]	PUPR4 [16]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PUPR4 [15]	PUPR4 [14]	PUPR4 [13]	PUPR4 [12]	PUPR4 [11]	PUPR4 [10]	PUPR4 [9]	PUPR4 [8]	PUPR4 [7]	PUPR4 [6]	PUPR4 [5]	PUPR4 [4]	PUPR4 [3]	PUPR4 [2]	PUPR4 [1]	PUPR4 [0]
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR4[31:0]	H'FFFF FFFF	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR4[31]	RX3_A pin is pulled up
PUPR4[30]	TX3_A pin is pulled up
PUPR4[29]	SCL2_A pin is pulled up
PUPR4[28]	SDA2_A pin is pulled up
PUPR4[27]	SSI_SCK5_A pin is pulled up
PUPR4[26]	SSI_WS5_A pin is pulled up
PUPR4[25]	SSI_SDATA5_A pin is pulled up
PUPR4[24]	SSI_SCK6_A pin is pulled up
PUPR4[23]	SSI_WS6_A pin is pulled up
PUPR4[22]	SSI_SDATA6_A pin is pulled up
PUPR4[21]	SSI_SCK78_A pin is pulled up
PUPR4[20]	SSI_WS78_A pin is pulled up
PUPR4[19]	SSI_SDATA7_A pin is pulled up
PUPR4[18]	SSI_SCK0129_A pin is pulled up
PUPR4[17]	SSI_WS0129_A pin is pulled up
PUPR4[16]	SSI_SDATA0_A pin is pulled up
PUPR4[15]	SSI_SCK34 pin is pulled up
PUPR4[14]	SSI_WS34 pin is pulled up
PUPR4[13]	SSI_SDATA3 pin is pulled up
PUPR4[12]	SSI_SCK4_A pin is pulled up
PUPR4[11]	SSI_WS4_A pin is pulled up
PUPR4[10]	SSI_SDATA4_A pin is pulled up
PUPR4[9]	SSI_SCK1_A pin is pulled up
PUPR4[8]	SSI_SDATA8_A pin is pulled up

Bit Name	Set Value = 1
PUPR4[7]	SSI_WS1_A pin is pulled up
PUPR4[6]	SSI_SDATA1_A pin is pulled up
PUPR4[5]	SSI_SCK2_A pin is pulled up
PUPR4[4]	SSI_WS2_A pin is pulled up
PUPR4[3]	SSI_SDATA2_A pin is pulled up
PUPR4[2]	SSI_SCK9_A pin is pulled up
PUPR4[1]	SSI_WS9_A pin is pulled up
PUPR4[0]	SSI_SDATA9_A pin is pulled up

5.3.34 LSI Pin Pull-Up Control Register 5 (PUPR5)

Function: PUPR5 performs on/off control of the pull-up resistors.

Note: When these pins are used as I2C interface, external pull-up resistors are mandatory.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PUPR5 [31]	PUPR5 [30]	PUPR5 [29]	PUPR5 [28]	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PUPR5[31:0]	H'F000 0000	R/W	Performs individual on/off control of the pull-up resistor provided in each signal pin of the LSI. 0: Pull-up function is disabled. 1: Pull-up function is enabled.

Bit Name	Set Value = 1
PUPR5[31]	AUDIO_CLKA_A pin is pulled up
PUPR5[30]	AUDIO_CLKB_A pin is pulled up
PUPR5[29]	AUDIO_CLKC_A pin is pulled up
PUPR5[28]	AUDIO_CLKOUT_A pin is pulled up
PUPR5[27]	—
PUPR5[26]	—
PUPR5[25]	—
PUPR5[24]	—
PUPR5[23]	—
PUPR5[22]	—
PUPR5[21]	—
PUPR5[20]	—
PUPR5[19]	—
PUPR5[18]	—
PUPR5[17]	—
PUPR5[16]	—
PUPR5[15]	—
PUPR5[14]	—
PUPR5[13]	—
PUPR5[12]	—
PUPR5[11]	—
PUPR5[10]	—
PUPR5[9]	—
PUPR5[8]	—

Bit Name	Set Value = 1
PUPR5[7]	—
PUPR5[6]	—
PUPR5[5]	—
PUPR5[4]	—
PUPR5[3]	—
PUPR5[2]	—
PUPR5[1]	—
PUPR5[0]	—

5.3.35 Drivability Control Register 0 (IOCTRL0)

Function: IOCTRL0 controls the driving abilities of LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	pfc_drv2_sd0_clk	pfc_drv1_sd0_clk	pfc_drv2_sd0_cmd	pfc_drv1_sd0_cmd	pfc_drv2_sd0_dat0	pfc_drv1_sd0_dat0	pfc_drv2_sd0_dat1	pfc_drv1_sd0_dat1	pfc_drv2_sd0_dat2	pfc_drv1_sd0_dat2	pfc_drv2_sd0_dat3	pfc_drv1_sd0_dat3	pfc_drv2_mmc0_clk	pfc_drv1_mmc0_clk	pfc_drv2_mmc0_cmd	pfc_drv1_mmc0_cmd
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	pfc_drv2_mmc0_d0	pfc_drv1_mmc0_d0	pfc_drv2_mmc0_d1	pfc_drv1_mmc0_d1	pfc_drv2_mmc0_d2	pfc_drv1_mmc0_d2	pfc_drv2_mmc0_d3	pfc_drv1_mmc0_d3	pfc_drv2_mmc0_d4	pfc_drv1_mmc0_d4	pfc_drv2_mmc0_d5	pfc_drv1_mmc0_d5	pfc_drv2_mmc0_d6	pfc_drv1_mmc0_d6	pfc_drv2_mmc0_d7	pfc_drv1_mmc0_d7
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	pfc_drv2_sd0_clk	1	R/W	SD0_CLK drive ability control
30	pfc_drv1_sd0_clk	0	R/W	
29	pfc_drv2_sd0_cmd	1	R/W	SD0_CMD drive ability control
28	pfc_drv1_sd0_cmd	0	R/W	
27	pfc_drv2_sd0_dat0	1	R/W	SD0_DAT0 drive ability control
26	pfc_drv1_sd0_dat0	0	R/W	
25	pfc_drv2_sd0_dat1	1	R/W	SD0_DAT1 drive ability control
24	pfc_drv1_sd0_dat1	0	R/W	
23	pfc_drv2_sd0_dat2	1	R/W	SD0_DAT2 drive ability control
22	pfc_drv1_sd0_dat2	0	R/W	
21	pfc_drv2_sd0_dat3	1	R/W	SD0_DAT3 drive ability control
20	pfc_drv1_sd0_dat3	0	R/W	
19	pfc_drv2_mmc0_clk	1	R/W	MMC0_CLK drive ability control
18	pfc_drv1_mmc0_clk	0	R/W	
17	pfc_drv2_mmc0_cmd	1	R/W	MMC0_CMD drive ability control
16	pfc_drv1_mmc0_cmd	0	R/W	
15	pfc_drv2_mmc0_d0	1	R/W	MMC0_D0 drive ability control
14	pfc_drv1_mmc0_d0	0	R/W	
13	pfc_drv2_mmc0_d1	1	R/W	MMC0_D1 drive ability control
12	pfc_drv1_mmc0_d1	0	R/W	
11	pfc_drv2_mmc0_d2	1	R/W	MMC0_D2 drive ability control
10	pfc_drv1_mmc0_d2	0	R/W	
9	pfc_drv2_mmc0_d3	1	R/W	MMC0_D3 drive ability control
8	pfc_drv1_mmc0_d3	0	R/W	
7	pfc_drv2_mmc0_d4	1	R/W	MMC0_D4 drive ability control
6	pfc_drv1_mmc0_d4	0	R/W	
5	pfc_drv2_mmc0_d5	1	R/W	MMC0_D5 drive ability control
4	pfc_drv1_mmc0_d5	0	R/W	
3	pfc_drv2_mmc0_d6	1	R/W	MMC0_D6 drive ability control
2	pfc_drv1_mmc0_d6	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
1	pfc_drv2_mmc0_d7	1	R/W	MMC0_D7 drive ability control
0	pfc_drv1_mmc0_d7	0	R/W	

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Values	Drivability	
drv[1:0]	1.8V Mode	3.3V Mode
B'00	1/4	1/4
B'01	1/2	1/2
B'10	3/4	3/4
B'11	Full	Full

5.3.36 Drivability Control Register 1 (IOCTRL1)

Function: IOCTRL1 controls the driving abilities of LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	pfc_drv2_d14	pfc_drv1_d14	pfc_drv2_d15	pfc_drv1_d15	pfc_drv2_du0_dotclkout0	pfc_drv1_du0_dotclkout0	pfc_drv2_du0_dotclkout1	pfc_drv1_du0_dotclkout1	pfc_drv2_vi1_clk	pfc_drv1_vi1_clk	pfc_drv2_vi1_data0	pfc_drv1_vi1_data0	pfc_drv2_vi1_data1	pfc_drv1_vi1_data1	pfc_drv2_vi1_data2	pfc_drv1_vi1_data2
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	pfc_drv2_vi1_data3	pfc_drv1_vi1_data3	pfc_drv2_vi1_data4	pfc_drv1_vi1_data4	pfc_drv2_vi1_data5	pfc_drv1_vi1_data5	pfc_drv2_vi1_data6	pfc_drv1_vi1_data6	pfc_drv2_vi1_data7	pfc_drv1_vi1_data7	pfc_drv2_vi1_clkenb	pfc_drv1_vi1_clkenb	pfc_drv2_vi1_field	pfc_drv1_vi1_field	pfc_drv2_vi1_hsync_n	pfc_drv1_vi1_hsync_n
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	pfc_drv2_d14	1	R/W	D14 drive ability control
30	pfc_drv1_d14	0	R/W	
29	pfc_drv2_d15	1	R/W	D15 drive ability control
28	pfc_drv1_d15	0	R/W	
27	pfc_drv2_du0_dotclkout0	1	R/W	DU0_DOTCLKOUT0 drive ability control
26	pfc_drv1_du0_dotclkout0	0	R/W	
25	pfc_drv2_du0_dotclkout1	1	R/W	DU0_DOTCLKOUT1 drive ability control
24	pfc_drv1_du0_dotclkout1	0	R/W	
23	pfc_drv2_vi1_clk	1	R/W	VI1_CLK drive ability control
22	pfc_drv1_vi1_clk	0	R/W	
21	pfc_drv2_vi1_data0	1	R/W	VI1_DATA0 drive ability control
20	pfc_drv1_vi1_data0	0	R/W	
19	pfc_drv2_vi1_data1	1	R/W	VI1_DATA1 drive ability control
18	pfc_drv1_vi1_data1	0	R/W	
17	pfc_drv2_vi1_data2	1	R/W	VI1_DATA2 drive ability control
16	pfc_drv1_vi1_data2	0	R/W	
15	pfc_drv2_vi1_data3	1	R/W	VI1_DATA3 drive ability control
14	pfc_drv1_vi1_data3	0	R/W	
13	pfc_drv2_vi1_data4	1	R/W	VI1_DATA4 drive ability control
12	pfc_drv1_vi1_data4	0	R/W	
11	pfc_drv2_vi1_data5	1	R/W	VI1_DATA5 drive ability control
10	pfc_drv1_vi1_data5	0	R/W	
9	pfc_drv2_vi1_data6	1	R/W	VI1_DATA6 drive ability control
8	pfc_drv1_vi1_data6	0	R/W	
7	pfc_drv2_vi1_data7	1	R/W	VI1_DATA7 drive ability control
6	pfc_drv1_vi1_data7	0	R/W	
5	pfc_drv2_vi1_clkenb	1	R/W	VI1_CLKENB drive ability control
4	pfc_drv1_vi1_clkenb	0	R/W	
3	pfc_drv2_vi1_field	1	R/W	VI1_FIELD drive ability control
2	pfc_drv1_vi1_field	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
1	pfc_drv2_vi1_hsync_n	1	R/W	VI1_HSYNC# drive ability control
0	pfc_drv1_vi1_hsync_n	0	R/W	

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Values	Drivability	
drv[1:0]	1.8V Mode	3.3V Mode
B'00	1/4	1/4
B'01	1/2	1/2
B'10	3/4	3/4
B'11	Full	Full

5.3.37 Drivability Control Register 2 (IOCTRL2)

Function: IOCTRL2 controls the driving abilities of LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	pfc_drv2_vi1_vsync_n	pfc_drv1_vi1_vsync_n	pfc_drv2_vi1_data8	pfc_drv1_vi1_data8	pfc_drv2_vi1_data9	pfc_drv1_vi1_data9	pfc_drv2_vi1_data10	pfc_drv1_vi1_data10	pfc_drv2_vi1_data11	pfc_drv1_vi1_data11	pfc_drv2_avb_txd3	pfc_drv1_avb_txd3	pfc_drv2_avb_txd4	pfc_drv1_avb_txd4	pfc_drv2_avb_txd5	pfc_drv1_avb_txd5
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	pfc_drv2_scl0_a	pfc_drv1_scl0_a	pfc_drv2_sd2_clk	pfc_drv1_sd2_clk	pfc_drv2_sd2_cmd	pfc_drv1_sd2_cmd	pfc_drv2_sd2_dat0	pfc_drv1_sd2_dat0	pfc_drv2_sd2_dat1	pfc_drv1_sd2_dat1	pfc_drv2_sd2_dat2	pfc_drv1_sd2_dat2	pfc_drv2_sd2_dat3	pfc_drv1_sd2_dat3	pfc_drv2_ssi_sck5_a	pfc_drv1_ssi_sck5_a
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	pfc_drv2_vi1_vsync_n	1	R/W	VI1_VSYNC# drive ability control
30	pfc_drv1_vi1_vsync_n	0	R/W	
29	pfc_drv2_vi1_data8	1	R/W	VI1_DATA8 drive ability control
28	pfc_drv1_vi1_data8	0	R/W	
27	pfc_drv2_vi1_data9	1	R/W	VI1_DATA9 drive ability control
26	pfc_drv1_vi1_data9	0	R/W	
25	pfc_drv2_vi1_data10	1	R/W	VI1_DATA10 drive ability control
24	pfc_drv1_vi1_data10	0	R/W	
23	pfc_drv2_vi1_data11	1	R/W	VI1_DATA11 drive ability control
22	pfc_drv1_vi1_data11	0	R/W	
21	pfc_drv2_avb_txd3	1	R/W	AVB_TXD3 drive ability control
20	pfc_drv1_avb_txd3	0	R/W	
19	pfc_drv2_avb_txd4	1	R/W	AVB_TXD4 drive ability control
18	pfc_drv1_avb_txd4	0	R/W	
17	pfc_drv2_avb_txd5	1	R/W	AVB_TXD5 drive ability control
16	pfc_drv1_avb_txd5	0	R/W	
15	pfc_drv2_scl0_a	1	R/W	SCL0_A drive ability control
14	pfc_drv1_scl0_a	0	R/W	
13	pfc_drv2_sd2_clk	1	R/W	SD2_CLK drive ability control
12	pfc_drv1_sd2_clk	0	R/W	
11	pfc_drv2_sd2_cmd	1	R/W	SD2_CMD drive ability control
10	pfc_drv1_sd2_cmd	0	R/W	
9	pfc_drv2_sd2_dat0	1	R/W	SD2_DAT0 drive ability control
8	pfc_drv1_sd2_dat0	0	R/W	
7	pfc_drv2_sd2_dat1	1	R/W	SD2_DAT1 drive ability control
6	pfc_drv1_sd2_dat1	0	R/W	
5	pfc_drv2_sd2_dat2	1	R/W	SD2_DAT2 drive ability control
4	pfc_drv1_sd2_dat2	0	R/W	
3	pfc_drv2_sd2_dat3	1	R/W	SD2_DAT3 drive ability control
2	pfc_drv1_sd2_dat3	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
1	pfc_drv2_ssi_sck5_a	1	R/W	SSI_SCK5_A drive ability control
0	pfc_drv1_ssi_sck5_a	0	R/W	

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Values	Drivability	
drv[1:0]	1.8V Mode	3.3V Mode
B'00	1/4	1/4
B'01	1/2	1/2
B'10	3/4	3/4
B'11	Full	Full

5.3.38 Drivability Control Register 3 (IOCTRL3)

Function: IOCTRL3 controls the driving abilities of LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	pfc_drv2_tms	pfc_drv1_tms	pfc_drv2_ssi_ws2_a	pfc_drv1_ssi_ws2_a	pfc_drv2_ssi_sck2_a	pfc_drv1_ssi_sck2_a	pfc_drv2_sda0_a	pfc_drv1_sda0_a	pfc_drv2_ssi_sdata5_a	pfc_drv1_ssi_sdata5_a	pfc_drv2_tdo	pfc_drv1_tdo	—	—	pfc_drv2_ssi_sck34_a	pfc_drv1_ssi_sck34_a
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	pfc_drv2_ssi_ws34_a	pfc_drv1_ssi_ws34_a	pfc_drv2_ssi_sdata3_a	pfc_drv1_ssi_sdata3_a	pfc_drv2_ssi_sck4_a	pfc_drv1_ssi_sck4_a	pfc_drv2_ssi_ws4_a	pfc_drv1_ssi_ws4_a	pfc_drv2_ssi_sdata4_a	pfc_drv1_ssi_sdata4_a	pfc_drv2_ssi_sck1_a	pfc_drv1_ssi_sck1_a	pfc_drv2_ssi_sdata8_a	pfc_drv1_ssi_sdata8_a	pfc_drv2_ssi_ws1_a	pfc_drv1_ssi_ws1_a
Initial value:	1	0	1	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	pfc_drv2_tms	1	R/W	TMS drive ability control
30	pfc_drv1_tms	0	R/W	
29	pfc_drv2_ssi_ws2_a	1	R/W	SSI_WS2_A drive ability control
28	pfc_drv1_ssi_ws2_a	0	R/W	
27	pfc_drv2_ssi_sck2_a	1	R/W	SSI_SCK2_A drive ability control
26	pfc_drv1_ssi_sck2_a	0	R/W	
25	pfc_drv2_sda0_a	1	R/W	SDA0_A drive ability control
24	pfc_drv1_sda0_a	0	R/W	
23	pfc_drv2_ssi_sdata5_a	1	R/W	SSI_SDATA5_A drive ability control
22	pfc_drv1_ssi_sdata5_a	0	R/W	
21	pfc_drv2_tdo	1	R/W	TDO drive ability control
20	pfc_drv1_tdo	0	R/W	
19	—	1	R/W	Reserved
18	—	0	R/W	
17	pfc_drv2_ssi_sck34_a	1	R/W	SSI_SCK34 drive ability control
16	pfc_drv1_ssi_sck34_a	0	R/W	
15	pfc_drv2_ssi_ws34_a	1	R/W	SSI_WS34 drive ability control
14	pfc_drv1_ssi_ws34_a	0	R/W	
13	pfc_drv2_ssi_sdata3_a	1	R/W	SSI_SDATA3 drive ability control
12	pfc_drv1_ssi_sdata3_a	0	R/W	
11	pfc_drv2_ssi_sck4_a	1	R/W	SSI_SCK4_A drive ability control
10	pfc_drv1_ssi_sck4_a	0	R/W	
9	pfc_drv2_ssi_ws4_a	1	R/W	SSI_WS4_A drive ability control
8	pfc_drv1_ssi_ws4_a	0	R/W	
7	pfc_drv2_ssi_sdata4_a	1	R/W	SSI_SDATA4_A drive ability control
6	pfc_drv1_ssi_sdata4_a	0	R/W	
5	pfc_drv2_ssi_sck1_a	1	R/W	SSI_SCK1_A drive ability control
4	pfc_drv1_ssi_sck1_a	0	R/W	
3	pfc_drv2_ssi_sdata8_a	1	R/W	SSI_SDATA8_A drive ability control
2	pfc_drv1_ssi_sdata8_a	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
1	pfc_drv2_ssi_ws1_a	1	R/W	SSI_WS1_A drive ability control
0	pfc_drv1_ssi_ws1_a	0	R/W	

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Values	Drivability	
drv[1:0]	1.8V Mode	3.3V Mode
B'00	1/4	1/4
B'01	1/2	1/2
B'10	3/4	3/4
B'11	Full	Full

5.3.39 RSEL Control Register (IOCTRL4)

Function: IOCTRL4 controls the pull resistor selecting of LSI pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	pfc_rsel_mmc0_clk	pfc_rsel_mmc0_cmd	pfc_rsel_mmc0_d0	pfc_rsel_mmc0_d1	pfc_rsel_mmc0_d2	pfc_rsel_mmc0_d3
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	pfc_rsel_mmc0_d4	pfc_rsel_mmc0_d5	pfc_rsel_mmc0_d6	pfc_rsel_mmc0_d7	pfc_rsel_sd0_clk	pfc_rsel_sd0_cmd	pfc_rsel_sd0_dat0	pfc_rsel_sd0_dat1	pfc_rsel_sd0_dat2	pfc_rsel_sd0_dat3	pfc_rsel_sd2_clk	pfc_rsel_sd2_cmd	pfc_rsel_sd2_dat0	pfc_rsel_sd2_dat1	pfc_rsel_sd2_dat2	pfc_rsel_sd2_dat3
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The purpose of RSEL: adjust to pull resistance value by power supply.

RSEL control register must be set according to IO voltage level that is supplied to the pin.

If 1.8v is supplied, RSEL bit of these LSI pins must set to Low.

If 3.3v is supplied, RSEL bit of these LSI pins must set to High.

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R/W	—
30	—	0	R/W	—
29	—	0	R/W	—
28	—	0	R/W	—
27	—	0	R/W	—
26	—	0	R/W	—
25	—	0	R/W	—
24	—	0	R/W	—
23	—	0	R/W	—
22	—	0	R/W	—
21	pfc_rsel_mmc0_clk	1	R/W	MMC0_CLK Pull resistor control
20	pfc_rsel_mmc0_cmd	1	R/W	MMC0_CMD Pull resistor control
19	pfc_rsel_mmc0_d0	1	R/W	MMC0_D0 Pull resistor control
18	pfc_rsel_mmc0_d1	1	R/W	MMC0_D1 Pull resistor control
17	pfc_rsel_mmc0_d2	1	R/W	MMC0_D2 Pull resistor control
16	pfc_rsel_mmc0_d3	1	R/W	MMC0_D3 Pull resistor control
15	pfc_rsel_mmc0_d4	1	R/W	MMC0_D4 Pull resistor control
14	pfc_rsel_mmc0_d5	1	R/W	MMC0_D5 Pull resistor control
13	pfc_rsel_mmc0_d6	1	R/W	MMC0_D6 Pull resistor control
12	pfc_rsel_mmc0_d7	1	R/W	MMC0_D7 Pull resistor control
11	pfc_rsel_sd0_clk	1	R/W	SD0_CLK Pull resistor control
10	pfc_rsel_sd0_cmd	1	R/W	SD0_CMD Pull resistor control
9	pfc_rsel_sd0_dat0	1	R/W	SD0_DAT0 Pull resistor control
8	pfc_rsel_sd0_dat1	1	R/W	SD0_DAT1 Pull resistor control

Bit	Bit Name	Initial Value	R/W	Description
7	pfc_rsel_sd0_dat2	1	R/W	SD0_DAT2 Pull resistor control
6	pfc_rsel_sd0_dat3	1	R/W	SD0_DAT3 Pull resistor control
5	pfc_rsel_sd2_clk	1	R/W	SD2_CLK Pull resistor control
4	pfc_rsel_sd2_cmd	1	R/W	SD2_CMD Pull resistor control
3	pfc_rsel_sd2_dat0	1	R/W	SD2_DAT0 Pull resistor control
2	pfc_rsel_sd2_dat1	1	R/W	SD2_DAT1 Pull resistor control
1	pfc_rsel_sd2_dat2	1	R/W	SD2_DAT2 Pull resistor control
0	pfc_rsel_sd2_dat3	1	R/W	SD2_DAT3 Pull resistor control

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

5.3.40 TDSEL Control Register (IOCTRL5)

Function: IOCTRL5 controls the delay of clock pins when using for the SD, MMC interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	sd0td sel1	sd0td sel0	sd2td sel1	sd2td sel0	sd1td sel1	sd1td sel0
Initial value:	0	0	0	0	1	0	1	0	1	0	1	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R/W	—
30	—	0	R/W	
29	—	0	R/W	—
28	—	0	R/W	
27	—	0	R/W	—
26	—	0	R/W	
25	—	0	R/W	—
24	—	0	R/W	
23	—	0	R/W	—
22	—	0	R/W	
21	—	0	R/W	—
20	—	0	R/W	
19	—	0	R/W	—
18	—	0	R/W	
17	—	0	R/W	—
16	—	0	R/W	
15	—	0	R/W	—
14	—	0	R/W	
13	—	0	R/W	—
12	—	0	R/W	
11	—	1	R/W	—
10	—	0	R/W	
9	—	1	R/W	—
8	—	0	R/W	
7	—	1	R/W	—
6	—	0	R/W	
5	sd0tdsel1	1	R/W	SD0_CLK pin delay control
4	sd0tdsel0	0	R/W	
3	sd2tdsel1	1	R/W	SD2_CLK pin delay control
2	sd2tdsel0	0	R/W	

Bit	Bit Name	Initial Value	R/W	Description
1	sd1tdsel1	1	R/W	MMC0_CLK pin delay control
0	sd1tdsel0	0	R/W	

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Values	Target Delay	
tdsel[1:0]	1.8V Mode	3.3V Mode
B'00	5 pF	10 pF
B'01	10 pF	20 pF
B'10	15 pF	30 pF
B'11	20 pF	40 pF

5.3.41 POC Control Register (IOCTRL6)

Function: IOCTRL6 controls the IO voltage of SD interfaces.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	pfc_poc_mmc0_clk	pfc_poc_sd2_clk	pfc_poc_sd0_clk
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R/W	—
30	—	0	R/W	—
29	—	0	R/W	—
28	—	0	R/W	—
27	—	0	R/W	—
26	—	0	R/W	—
25	—	0	R/W	—
24	—	0	R/W	—
23	—	0	R/W	—
22	—	0	R/W	—
21	—	0	R/W	—
20	—	0	R/W	—
19	—	0	R/W	—
18	—	0	R/W	—
17	—	0	R/W	—
16	—	0	R/W	—
15	—	0	R/W	—
14	—	0	R/W	—
13	—	0	R/W	—
12	—	0	R/W	—
11	—	0	R/W	—
10	—	0	R/W	—
9	—	0	R/W	—
8	—	0	R/W	—
7	—	0	R/W	—
6	—	0	R/W	—
5	—	0	R/W	—
4	—	0	R/W	—
3	—	0	R/W	—
2	pfc_poc_mmc0_clk	1	R/W	MMC0_CLK power on control
1	pfc_poc_sd2_clk	1	R/W	SD2_CLK power on control

Bit	Bit Name	Initial Value	R/W	Description
0	pfc_poc_sd0_clk	1	R/W	SD0_CLK power on control

Note: To enable this register to be set, appropriately set the multiplexed pin setting mask register (PMMR) immediately before setting this register.

Supply Voltage	Setting value	Usage
1.8V	0	Possible
1.8V	1	Do not use
3.3V	0	Do not use (broken)
3.3V	1	Possible

5.4 Operation

5.4.1 Function Setting for Multiplexed Pins

Setting the LSI multiplexed pin setting mask register (PMMR) is necessary before setting each of the GPIO/peripheral function select registers 0 to 5 (GPSR0 to GPSR5) and peripheral function select registers 0 to 17 (IPSR0 to IPSR17). Specifically, the inverse of the value to be set in the select register must be written to the LSI multiplexed pin setting mask register. Otherwise, the GPIO/peripheral function select registers 0 to 5 (GPSR0 to GPSR5) and peripheral function select registers 0 to 17 (IPSR0 to IPSR17) cannot be set.

IPSR0 to IPSR17, MOD_SEL0, MOD_SEL1, and MOD_SEL2 registers shall be set before setting GPSR0 to GPSR5 registers in case that they need to be configured. MOD_SEL0, MOD_SEL1, and MOD_SEL2 registers can be set either earlier or later than setting IPSR0 to IPSR17 registers.

(1) Procedure for changing pin function from GPIO to peripheral function

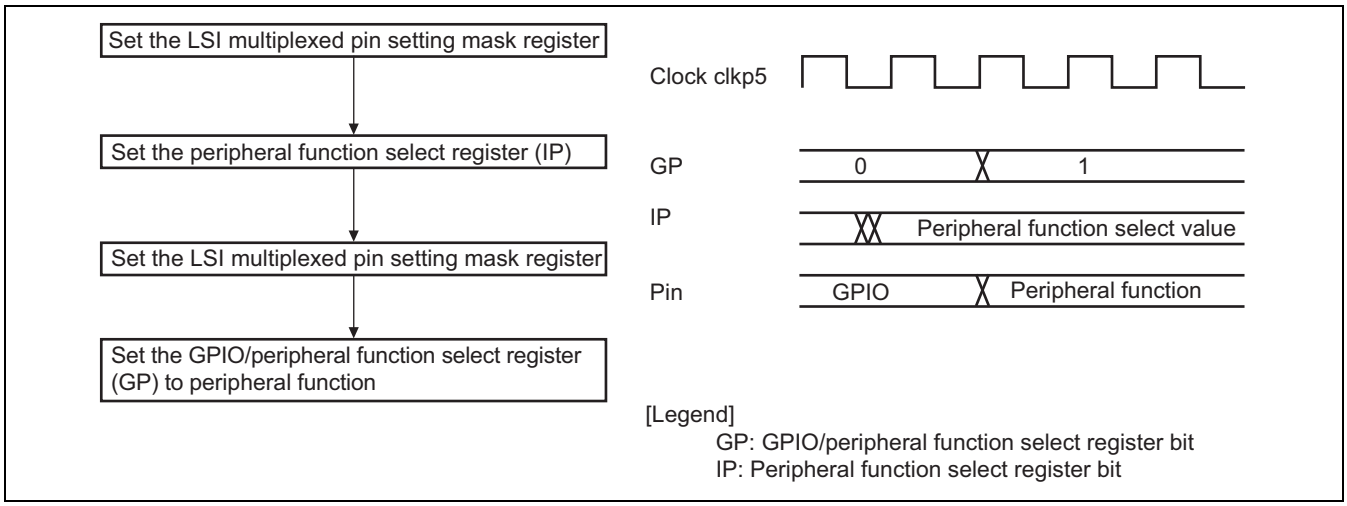


Figure 5.1 Procedure for Changing Pin Function from GPIO to Peripheral Function

(2) Procedure for changing pin function from peripheral function to GPIO

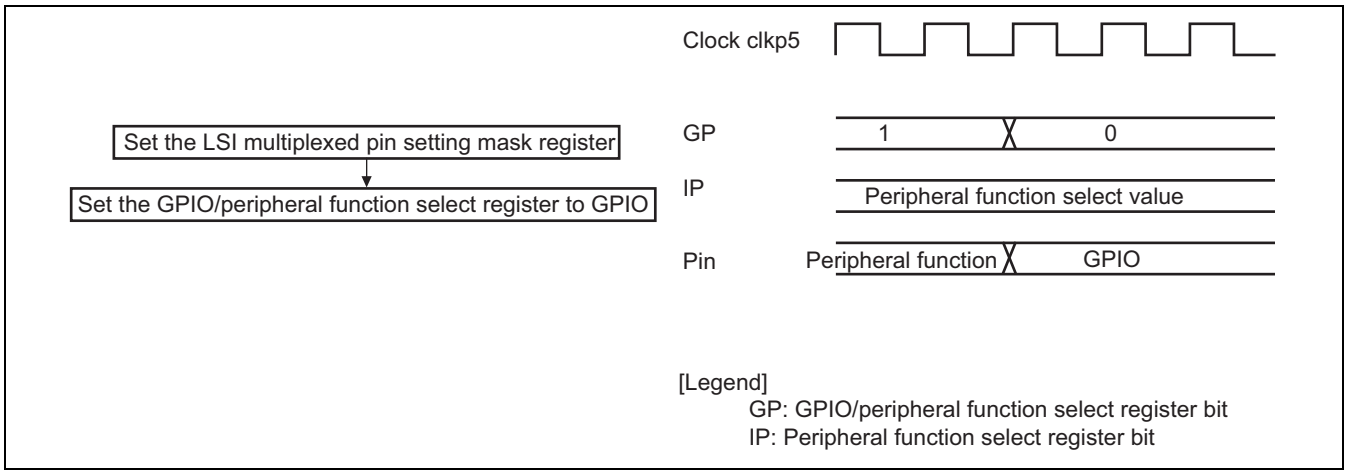


Figure 5.2 Procedure for Changing Pin Function from Peripheral function to GPIO

(3) Procedure 1 for changing pin function from one peripheral function to another peripheral function

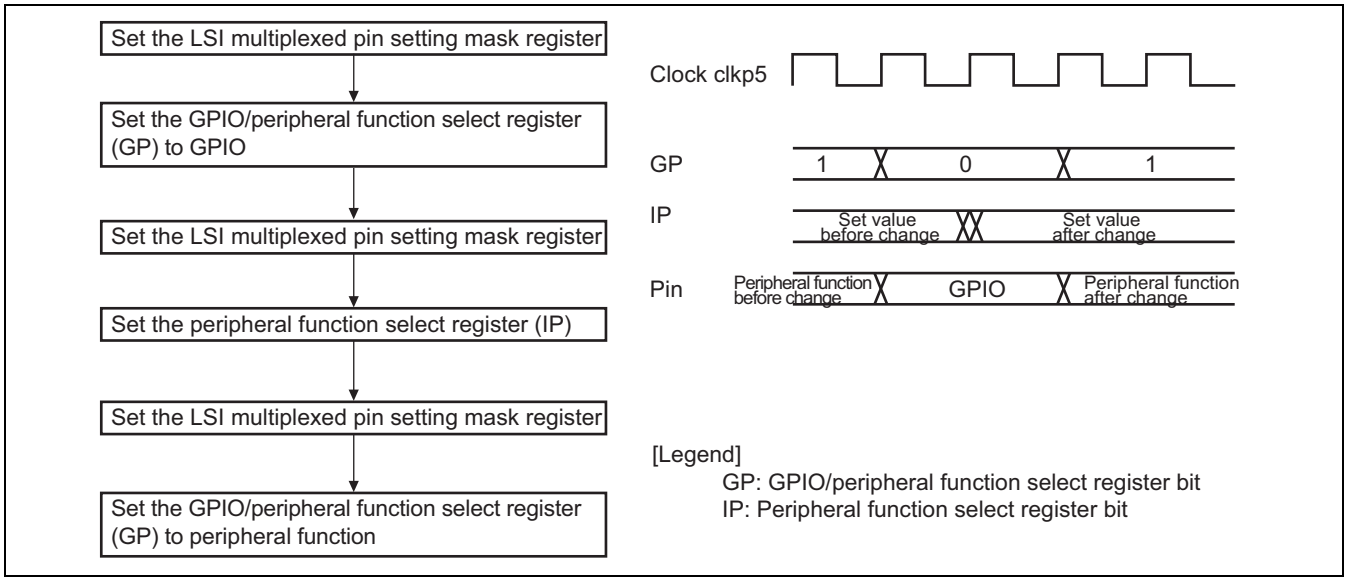


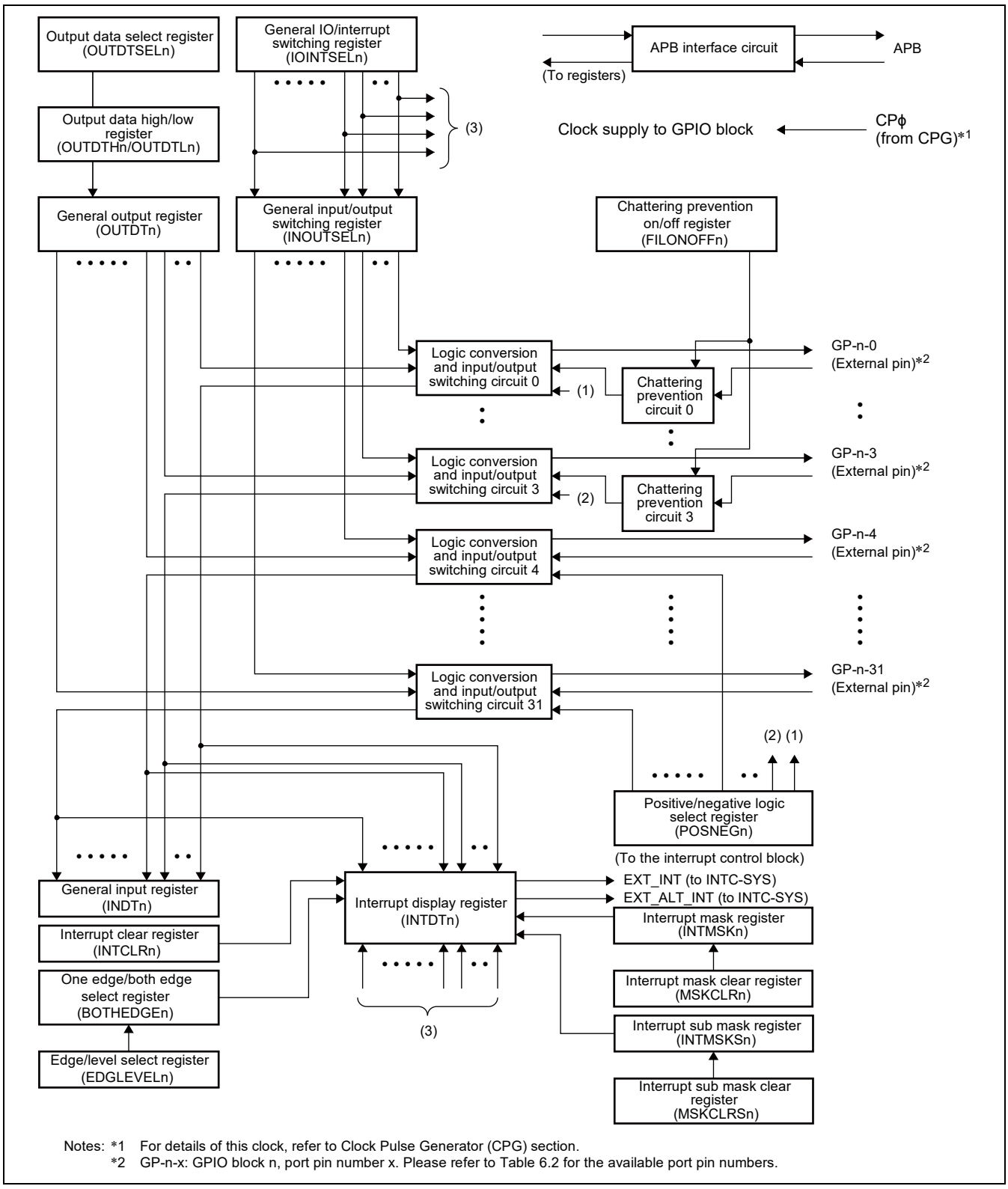
Figure 5.3 Procedure for Changing Pin Function from One Peripheral Function to Another Peripheral Function (with GPIO Setting)

6. General-Purpose Input/Output Ports (GPIO)

6.1 Overview

The General-Purpose Input/Output Ports (GPIO) have six blocks, each of which is a functional block that supports up to 32 port pins for general input/output and interrupt input. When the relevant register is written to, a signal is output via the corresponding general output port pin. When a signal is input via the general input port pin, the corresponding register indicates the value of the input signal; specifically, when an interrupt is input via a general port pin, the relevant register indicates that it is currently receiving an interrupt input, and an interrupt is also requested to the CPU core via the interrupt control block. The functions (modes) can be assigned to each port pin as desired by some setting the corresponding registers. It is also possible to select the signal polarity (positive or negative logic) and the interrupt detection condition (one edge/both edge or level) for each port. In this LSI, general output data mode of GPIO can be set in normal mode (outputting data as normal) or high/low level data output mode. Particularly, a filtering function to prevent external chattering is also available for port pins 0 to 3 in input modes for each GPIO block.

6.1.1 GPIO Block Diagram (block n)



Notes: *1 For details of this clock, refer to Clock Pulse Generator (CPG) section.
*2 GP-n-x: GPIO block n, port pin number x. Please refer to Table 6.2 for the available port pin numbers.

Figure 6.1 GPIO Block Configuration

6.1.2 Input/Output Pins

Table 6.1 shows the pin configuration of the GPIO.

Table 6.1 Pin Configuration

Function	Pin Name	I/O	Descriptions
IO/interrupt input ports	GP-0-0 to GP-5-31	I/O	General input/output and interrupt input

Note: Numbers of available pin for each GPIO is defined as below
- GPIO0: 23 pins (GP-0-0 to GP-0-22)
- GPIO1: 23 pins (GP-1-0 to GP-1-22)
- GPIO2: 32 pins (GP-2-0 to GP-2-31)
- GPIO3: 20 pins (GP-3-0 to GP 3-16 and GP-3-27 to GP-3-29)
- GPIO4: 26 pins (GP-4-0 to GP-4-25)
- GPIO5: 32 pins (GP-5-0 to GP-5-31)

6.2 Port Pin Specifications

Each GPIO block is provided with up to 32 port pins for general input/output and external interrupt input ports. Table 6.2 specifies these pins.

Table 6.2 Port Pin Specifications (1)

Block	Number	Abbreviation	Name	Descriptions
GPIO-0 Applicable registers: IOINTSEL0 INOUTSEL0 OUTDT0 INDT0 INTDT0 INTCLR0 INTMSK0 MSKCLR0 POSNEG0 EDGLEVEL0 FILONOFF0 INTMSKS0 MSKCLRS0 OUTDTSEL0 OUTDTH0 OUTDTL0 BOTHEDGE0	1	GP-0-0	IO/Interrupt input port A0	• Either general input/output mode or interrupt input mode can be set for each port. • In general input mode, the polarity of input signals can be set for each port. • In general output mode, the polarity of output signals can be set for each port. • In interrupt input mode, the polarity of interrupt signal can be set for each port. • In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	2	GP-0-1	IO/Interrupt input port A1	
	3	GP-0-2	IO/Interrupt input port A2	
	4	GP-0-3	IO/Interrupt input port A3	
	5	GP-0-4	IO/Interrupt input port A4	
	6	GP-0-5	IO/Interrupt input port A5	
	7	GP-0-6	IO/Interrupt input port A6	
	8	GP-0-7	IO/Interrupt input port A7	
	9	GP-0-8	IO/Interrupt input port A8	
	10	GP-0-9	IO/Interrupt input port A9	
	11	GP-0-10	IO/Interrupt input port A10	
	12	GP-0-11	IO/Interrupt input port A11	
	13	GP-0-12	IO/Interrupt input port A12	
	14	GP-0-13	IO/Interrupt input port A13	
	15	GP-0-14	IO/Interrupt input port A14	
	16	GP-0-15	IO/Interrupt input port A15	
	17	GP-0-16	IO/Interrupt input port A16	
	18	GP-0-17	IO/Interrupt input port A17	
	19	GP-0-18	IO/Interrupt input port A18	
	20	GP-0-19	IO/Interrupt input port A19	
	21	GP-0-20	IO/Interrupt input port A20	
	22	GP-0-21	IO/Interrupt input port A21	
	23	GP-0-22	IO/Interrupt input port A22	

Block	Number	Abbreviation	Name	Descriptions
GPIO-1 Applicable registers: IOINTSEL1 INOUTSEL1 OUTDT1 INDT1 INTDT1 INTCLR1 INTMSK1 MSKCLR1 POSNEG1 EDGLEVEL1 FILONOFF1 INTMSKS1 MSKCLRS1 OUTDTSEL1 OUTDTH1 OUTDTL1 BOTHEDGE1	24	GP-1-0	IO/Interrupt input port B0	• Either general input/output mode or interrupt input mode can be set for each port. • In general input mode, the polarity of input signals can be set for each port. • In general output mode, the polarity of output signals can be set for each port. • In interrupt input mode, the polarity of interrupt signal can be set for each port. • In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	25	GP-1-1	IO/Interrupt input port B1	
	26	GP-1-2	IO/Interrupt input port B2	
	27	GP-1-3	IO/Interrupt input port B3	
	28	GP-1-4	IO/Interrupt input port B4	
	29	GP-1-5	IO/Interrupt input port B5	
	30	GP-1-6	IO/Interrupt input port B6	
	31	GP-1-7	IO/Interrupt input port B7	
	32	GP-1-8	IO/Interrupt input port B8	
	33	GP-1-9	IO/Interrupt input port B9	
	34	GP-1-10	IO/Interrupt input port B10	
	35	GP-1-11	IO/Interrupt input port B11	
	36	GP-1-12	IO/Interrupt input port B12	
	37	GP-1-13	IO/Interrupt input port B13	
	38	GP-1-14	IO/Interrupt input port B14	
	39	GP-1-15	IO/Interrupt input port B15	
	40	GP-1-16	IO/Interrupt input port B16	
	41	GP-1-17	IO/Interrupt input port B17	
	42	GP-1-18	IO/Interrupt input port B18	
	43	GP-1-19	IO/Interrupt input port B19	
	44	GP-1-20	IO/Interrupt input port B20	
	45	GP-1-21	IO/Interrupt input port B21	
	46	GP-1-22	IO/Interrupt input port B22	

Block	Number	Abbreviation	Name	Descriptions
GPIO-2 Applicable registers: IOINTSEL2 INOUTSEL2 OUTDT2 INDT2 INTDT2 INTCLR2 INTMSK2 MSKCLR2 POSNEG2 EDGLEVEL2 FILONOFF2 INTMSKS2 MSKCLRS2 OUTDTSEL2 OUTDTH2 OUTDTL2 BOTHEDGE2	47	GP-2-0	IO/Interrupt input port C0	• Either general input/output mode or interrupt input mode can be set for each port. • In general input mode, the polarity of input signals can be set for each port. • In general output mode, the polarity of output signals can be set for each port. • In interrupt input mode, the polarity of interrupt signal can be set for each port. • In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	48	GP-2-1	IO/Interrupt input port C1	
	49	GP-2-2	IO/Interrupt input port C2	
	50	GP-2-3	IO/Interrupt input port C3	
	51	GP-2-4	IO/Interrupt input port C4	
	52	GP-2-5	IO/Interrupt input port C5	
	53	GP-2-6	IO/Interrupt input port C6	
	54	GP-2-7	IO/Interrupt input port C7	
	55	GP-2-8	IO/Interrupt input port C8	
	56	GP-2-9	IO/Interrupt input port C9	
	57	GP-2-10	IO/Interrupt input port C10	
	58	GP-2-11	IO/Interrupt input port C11	
	59	GP-2-12	IO/Interrupt input port C12	
	60	GP-2-13	IO/Interrupt input port C13	
	61	GP-2-14	IO/Interrupt input port C14	
	62	GP-2-15	IO/interrupt input port C15	
	63	GP-2-16	IO/interrupt input port C16	
	64	GP-2-17	IO/interrupt input port C17	
	65	GP-2-18	IO/interrupt input port C18	
	66	GP-2-19	IO/interrupt input port C19	
	67	GP-2-20	IO/interrupt input port C20	
	68	GP-2-21	IO/interrupt input port C21	
	69	GP-2-22	IO/interrupt input port C22	
	70	GP-2-23	IO/interrupt input port C23	
	71	GP-2-24	IO/interrupt input port C24	
	72	GP-2-25	IO/interrupt input port C25	
	73	GP-2-26	IO/interrupt input port C26	
	74	GP-2-27	IO/interrupt input port C27	
	75	GP-2-28	IO/interrupt input port C28	
	76	GP-2-29	IO/interrupt input port C29	
	77	GP-2-30	IO/interrupt input port C30	
	78	GP-2-31	IO/interrupt input port C31	

Block	Number	Abbreviation	Name	Descriptions
GPIO-3 Applicable registers: IOINTSEL3 INOUTSEL3 OUTDT3 INDT3 INTDT3 INTCLR3 INTMSK3 MSKCLR3 POSNEG3 EDGLEVEL3 FILONOFF3 INTMSKS3 MSKCLRS3 OUTDTSEL3 OUTDTH3 OUTDTL3 BOTHEDGE3	79	GP-3-0	IO/interrupt input port D0	• Either general input/output mode or interrupt input mode can be set for each port. • In general input mode, the polarity of input signals can be set for each port. • In general output mode, the polarity of output signals can be set for each port. • In interrupt input mode, the polarity of interrupt signal can be set for each port. • In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	80	GP-3-1	IO/interrupt input port D1	
	81	GP-3-2	IO/interrupt input port D2	
	82	GP-3-3	IO/interrupt input port D3	
	83	GP-3-4	IO/interrupt input port D4	
	84	GP-3-5	IO/interrupt input port D5	
	85	GP-3-6	IO/interrupt input port D6	
	86	GP-3-7	IO/interrupt input port D7	
	87	GP-3-8	IO/interrupt input port D8	
	88	GP-3-9	IO/interrupt input port D9	
	89	GP-3-10	IO/interrupt input port D10	
	90	GP-3-11	IO/interrupt input port D11	
	91	GP-3-12	IO/interrupt input port D12	
	92	GP-3-13	IO/interrupt input port D13	
	93	GP-3-14	IO/interrupt input port D14	
	94	GP-3-15	IO/interrupt input port D15	
	95	GP-3-16	IO/interrupt input port D16	
	96	GP-3-27	IO/interrupt input port D27	
	97	GP-3-28	IO/interrupt input port D28	
	98	GP-3-29	IO/interrupt input port D29	

Block	Number	Abbreviation	Name	Descriptions
GPIO-4 Applicable registers: IOINTSEL4 INOUTSEL4 OUTDT4 INDT4 INTDT4 INTCLR4 INTMSK4 MSKCLR4 POSNEG4 EDGLEVEL4 FILONOFF4 INTMSKS4 MSKCLRS4 OUTDTSEL4 OUTDTH4 OUTDTL4 BOTHEDGE4	99	GP-4-0	IO/interrupt input port E0	• Either general input/output mode or interrupt input mode can be set for each port. • In general input mode, the polarity of input signals can be set for each port. • In general output mode, the polarity of output signals can be set for each port. • In interrupt input mode, the polarity of interrupt signal can be set for each port. • In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	100	GP-4-1	IO/interrupt input port E1	
	101	GP-4-2	IO/interrupt input port E2	
	102	GP-4-3	IO/interrupt input port E3	
	103	GP-4-4	IO/interrupt input port E4	
	104	GP-4-5	IO/interrupt input port E5	
	105	GP-4-6	IO/interrupt input port E6	
	106	GP-4-7	IO/interrupt input port E7	
	107	GP-4-8	IO/interrupt input port E8	
	108	GP-4-9	IO/interrupt input port E9	
	109	GP-4-10	IO/interrupt input port E10	
	110	GP-4-11	IO/interrupt input port E11	
	111	GP-4-12	IO/interrupt input port E12	
	112	GP-4-13	IO/interrupt input port E13	
	113	GP-4-14	IO/interrupt input port E14	
	114	GP-4-15	IO/interrupt input port E15	
	115	GP-4-16	IO/interrupt input port E16	
	116	GP-4-17	IO/interrupt input port E17	
	117	GP-4-18	IO/interrupt input port E18	
	118	GP-4-19	IO/interrupt input port E19	
	119	GP-4-20	IO/interrupt input port E20	
	120	GP-4-21	IO/interrupt input port E21	
	121	GP-4-22	IO/interrupt input port E22	
	122	GP-4-23	IO/interrupt input port E23	
	123	GP-4-24	IO/interrupt input port E24	
	124	GP-4-25	IO/interrupt input port E25	

Block	Number	Abbreviation	Name	Descriptions
GPIO-5 Applicable registers: IOINTSEL5 INOUTSEL5 OUTDT5 INDT5 INTDT5 INTCLR5 INTMSK5 MSKCLR5 POSNEG5 EDGLEVEL5 FILONOFF5 INTMSKS5 MSKCLRS5 OUTDTSEL5 OUTDTH5 OUTDTL5 BOTHEDGE5	125	GP-5-0	IO/interrupt input port F0	• Either general input/output mode or interrupt input mode can be set for each port. • In general input mode, the polarity of input signals can be set for each port. • In general output mode, the polarity of output signals can be set for each port. • In interrupt input mode, the polarity of interrupt signal can be set for each port. • In interrupt input mode, the detection conditions of interrupt signals can be set for each port.
	126	GP-5-1	IO/interrupt input port F1	
	127	GP-5-2	IO/interrupt input port F2	
	128	GP-5-3	IO/interrupt input port F3	
	129	GP-5-4	IO/interrupt input port F4	
	130	GP-5-5	IO/interrupt input port F5	
	131	GP-5-6	IO/interrupt input port F6	
	132	GP-5-7	IO/interrupt input port F7	
	133	GP-5-8	IO/interrupt input port F8	
	134	GP-5-9	IO/interrupt input port F9	
	135	GP-5-10	IO/interrupt input port F10	
	136	GP-5-11	IO/interrupt input port F11	
	137	GP-5-12	IO/interrupt input port F12	
	138	GP-5-13	IO/interrupt input port F13	
	139	GP-5-14	IO/interrupt input port F14	
	140	GP-5-15	IO/interrupt input port F15	
	141	GP-5-16	IO/interrupt input port F16	
	142	GP-5-17	IO/interrupt input port F17	
	143	GP-5-18	IO/interrupt input port F18	
	144	GP-5-19	IO/interrupt input port F19	
	145	GP-5-20	IO/interrupt input port F20	
	146	GP-5-21	IO/interrupt input port F21	
	147	GP-5-22	IO/interrupt input port F22	
	148	GP-5-23	IO/interrupt input port F23	
	149	GP-5-24	IO/interrupt input port F24	
	150	GP-5-25	IO/interrupt input port F25	
	151	GP-5-26	IO/interrupt input port F26	
	152	GP-5-27	IO/interrupt input port F27	
	153	GP-5-28	IO/interrupt input port F28	
	154	GP-5-29	IO/interrupt input port F29	
	155	GP-5-30	IO/interrupt input port F30	
	156	GP-5-31	IO/interrupt input port F31	

6.3 Operations in Each Mode

6.3.1 Mode Switching

Two registers are used to switch modes of the general IO/interrupt input pins of the GPIO blocks. Each register is provided with up to 32 bits each controlling one of the GPIOn* port pins. The general IO/interrupt switching register is first used to select either general input/output mode or interrupt input mode for each port pin. When general input/output mode is selected, the setting of the relevant bit in the second register, i.e., the general input/output switching register, is used. Specifically, when a bit in the general input/output switching register is set for general output mode, the corresponding port pin is turned to the output direction and the route is formed so that the set value in the corresponding bit in the general output register should be output via the pin. Likewise, when set for the general input mode, the corresponding port pin is turned to the input direction and the route is formed so that the value received via the pin should be indicated by the corresponding bit in the general input register. When interrupt input mode is selected, the corresponding port pin is turned to the input direction and the route is formed so that the reception of the signal input via the pin should be indicated by the interrupt display register. Here, the setting of the second register, i.e., the general input/output switching register, is invalid.

Note: * n = 0 to 5

6.3.2 General Input/Output Mode

When a port is set for general input/output mode using the corresponding bit in the general IO/interrupt switching register, the corresponding port serves as a general input/output pin. In general input/output mode, either mode can be selected using the corresponding bit in the general input/output switching register. When a port is set for general output mode, the port outputs the value set in the corresponding bit in the general output register or output data high/output data low register with appropriate configuring in output data select register. Here, the polarity of the actual output signal is determined by the setting of the corresponding bit in the positive/negative logic select register. When a port is set for general input mode, the polarity of the input signal is also determined by the setting of the corresponding bit in the positive/negative logic select register. The general input register indicates the value accordingly. Note that the general input register does not hold the input signal using the FF.

6.3.3 Interrupt Input Mode

When a port is set for interrupt input mode using the corresponding bit in the general IO/interrupt switching register, the corresponding port serves as an interrupt input pin. In interrupt input mode, when the port receives an external interrupt, the corresponding bit in the interrupt display register indicates the input of an interrupt signal on the corresponding port pin, and an interrupt signal is output to the interrupt control block. In this mode, the polarity and detection conditions (edge or level) of the external input signal can be set for each port. The corresponding bits in the positive/negative logic select register and edge/level select register, one edge/both edge select register should be used to set the polarity and detection conditions, respectively.

If a port is set for edge detection using the corresponding bit in the edge/level select register, even when an external pulse interrupt signal is input, the corresponding bit in the interrupt display register holds the input using the FF and allows the level interrupt signal to be output to the interrupt control block. To stop all the interrupt signal outputs, all the bits in the interrupt clear register corresponding to the bits in the interrupt display register currently indicating the reception of the corresponding interrupt signals should be cleared to 0. Note that if a port is set for level detection using the corresponding bit in the edge/level select register and an external level interrupt signal is input, the corresponding bit in the interrupt display register does not use the FF to hold the input.

Interrupts indicated by the interrupt display register can be separately masked using the corresponding bits in the interrupt mask register and the interrupt sub mask register. When all the bits currently indicating the reception of the interrupt signals are masked, no interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt mask clear register or the interrupt sub mask clear register depending on the interrupt mask register or the interrupt sub mask register is used.

6.4 Registers in GPIO Blocks

Each GPIO block incorporates seventeen 32-bit registers. These registers can be accessed via the APB interface. Table 6.3 describes all the GPIO block registers.

Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

Table 6.3 Register Configuration

Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size
General IO/interrupt switching register 0	IOINTSEL0	R/W	H'0000 0000	H'E6050000	32
General input/output switching register 0	INOUTSEL0	R/W	H'0000 0000	H'E6050004	32
General output register 0	OUTDT0	R/W	H'0000 0000	H'E6050008	32
General input register 0	INDT0	R	State of the port pins	H'E605000C	32
Interrupt display register 0	INTDT0	R	H'0000 0000	H'E6050010	32
Interrupt clear register 0	INTCLR0	R/W	H'0000 0000	H'E6050014	32
Interrupt mask register 0	INTMSK0	R/W	H'0000 0000	H'E6050018	32
Interrupt mask clear register 0	MSKCLR0	R/W	H'0000 0000	H'E605001C	32
Positive/negative logic select register 0	POSNEG0	R/W	H'0000 0000	H'E6050020	32
Edge/level select register 0	EDGLEVEL0	R/W	H'0000 0000	H'E6050024	32
Chattering prevention on/off register 0	FILONOFF0	R/W (for available bits)	H'0000 0000	H'E6050028	32
Interrupt sub mask register 0	INTMSKS0	R/W	H'0000 0000	H'E6050038	32
Interrupt sub mask clear register 0	MSKCLRS0	R/W	H'0000 0000	H'E605003C	32
Output data select register 0	OUTDTSEL0	R/W	H'0000 0000	H'E6050040	32
Output data high register 0	OUTDTH0	R/W	H'0000 0000	H'E6050044	32
Output data low register 0	OUTDTL0	R/W	H'0000 0000	H'E6050048	32
One edge/both edge select register 0	BOTHEDGE0	R/W	H'0000 0000	H'E605004C	32
General IO/interrupt switching register 1	IOINTSEL1	R/W	H'0000 0000	H'E6051000	32
General input/output switching register 1	INOUTSEL1	R/W	H'0000 0000	H'E6051004	32
General output register 1	OUTDT1	R/W	H'0000 0000	H'E6051008	32
General input register 1	INDT1	R	State of the port pins	H'E605100C	32
Interrupt display register 1	INTDT1	R	H'0000 0000	H'E6051010	32
Interrupt clear register 1	INTCLR1	R/W	H'0000 0000	H'E6051014	32
Interrupt mask register 1	INTMSK1	R/W	H'0000 0000	H'E6051018	32
Interrupt mask clear register 1	MSKCLR1	R/W	H'0000 0000	H'E605101C	32
Positive/negative logic select register 1	POSNEG1	R/W	H'0000 0000	H'E6051020	32
Edge/level select register 1	EDGLEVEL1	R/W	H'0000 0000	H'E6051024	32
Chattering prevention on/off register 1	FILONOFF1	R/W (for available bits)	H'0000 0000	H'E6051028	32
Interrupt sub mask register 1	INTMSKS1	R/W	H'0000 0000	H'E6051038	32
Interrupt sub mask clear register 1	MSKCLRS1	R/W	H'0000 0000	H'E605103C	32
Output data select register 1	OUTDTSEL1	R/W	H'0000 0000	H'E6051040	32
Output data high register 1	OUTDTH1	R/W	H'0000 0000	H'E6051044	32
Output data low register 1	OUTDTL1	R/W	H'0000 0000	H'E6051048	32
One edge/both edge select register 1	BOTHEDGE1	R/W	H'0000 0000	H'E605104C	32
General IO/interrupt switching register 2	IOINTSEL2	R/W	H'0000 0000	H'E6052000	32
General input/output switching register 2	INOUTSEL2	R/W	H'0000 0000	H'E6052004	32
General output register 2	OUTDT2	R/W	H'0000 0000	H'E6052008	32

Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size
General input register 2	INDT2	R	State of the port pins	H'E605200C	32
Interrupt display register 2	INTDT2	R	H'0000 0000	H'E6052010	32
Interrupt clear register 2	INTCLR2	R/W	H'0000 0000	H'E6052014	32
Interrupt mask register 2	INTMSK2	R/W	H'0000 0000	H'E6052018	32
Interrupt mask clear register 2	MSKCLR2	R/W	H'0000 0000	H'E605201C	32
Positive/negative logic select register 2	POSNEG2	R/W	H'0000 0000	H'E6052020	32
Edge/level select register 2	EDGLEVEL2	R/W	H'0000 0000	H'E6052024	32
Chattering prevention on/off register 2	FILONOFF2	R/W	H'0000 0000	H'E6052028	32
Interrupt sub mask register 2	INTMSKS2	R/W	H'0000 0000	H'E6052038	32
Interrupt sub mask clear register 2	MSKCLRS2	R/W	H'0000 0000	H'E605203C	32
Output data select register 2	OUTDTSEL2	R/W	H'0000 0000	H'E6052040	32
Output data high register 2	OUTDTH2	R/W	H'0000 0000	H'E6052044	32
Output data low register 2	OUTDTL2	R/W	H'0000 0000	H'E6052048	32
One edge/both edge select register 2	BOTHEDGE2	R/W	H'0000 0000	H'E605204C	32
General IO/interrupt switching register 3	IOINTSEL3	R/W	H'0000 0000	H'E6053000	32
General input/output switching register 3	INOUTSEL3	R/W	H'0000 0000	H'E6053004	32
General output register 3	OUTDT3	R/W	H'0000 0000	H'E6053008	32
General input register 3	INDT3	R	State of the port pins	H'E605300C	32
Interrupt display register 3	INTDT3	R	H'0000 0000	H'E6053010	32
Interrupt clear register 3	INTCLR3	R/W	H'0000 0000	H'E6053014	32
Interrupt mask register 3	INTMSK3	R/W	H'0000 0000	H'E6053018	32
Interrupt mask clear register 3	MSKCLR3	R/W	H'0000 0000	H'E605301C	32
Positive/negative logic select register 3	POSNEG3	R/W	H'0000 0000	H'E6053020	32
Edge/level select register 3	EDGLEVEL3	R/W	H'0000 0000	H'E6053024	32
Chattering prevention on/off register 3	FILONOFF3	R/W (for available bits)	H'0000 0000	H'E6053028	32
Interrupt sub mask register 3	INTMSKS3	R/W	H'0000 0000	H'E6053038	32
Interrupt sub mask clear register 3	MSKCLRS3	R/W	H'0000 0000	H'E605303C	32
Output data select register 3	OUTDTSEL3	R/W	H'0000 0000	H'E6053040	32
Output data high register 3	OUTDTH3	R/W	H'0000 0000	H'E6053044	32
Output data low register 3	OUTDTL3	R/W	H'0000 0000	H'E6053048	32
One edge/both edge select register 3	BOTHEDGE3	R/W	H'0000 0000	H'E605304C	32
General IO/interrupt switching register 4	IOINTSEL4	R/W	H'0000 0000	H'E6054000	32
General input/output switching register 4	INOUTSEL4	R/W	H'0000 0000	H'E6054004	32
General output register 4	OUTDT4	R/W	H'0000 0000	H'E6054008	32
General input register 4	INDT4	R	State of the port pins	H'E605400C	32
Interrupt display register 4	INTDT4	R	H'0000 0000	H'E6054010	32
Interrupt clear register 4	INTCLR4	R/W	H'0000 0000	H'E6054014	32
Interrupt mask register 4	INTMSK4	R/W	H'0000 0000	H'E6054018	32
Interrupt mask clear register 4	MSKCLR4	R/W	H'0000 0000	H'E605401C	32
Positive/negative logic select register 4	POSNEG4	R/W	H'0000 0000	H'E6054020	32
Edge/level select register 4	EDGLEVEL4	R/W	H'0000 0000	H'E6054024	32
Chattering prevention on/off register 4	FILONOFF4	R/W	H'0000 0000	H'E6054028	32
Interrupt sub mask register 4	INTMSKS4	R/W	H'0000 0000	H'E6054038	32
Interrupt sub mask clear register 4	MSKCLRS4	R/W	H'0000 0000	H'E605403C	32
Output data select register 4	OUTDTSEL4	R/W	H'0000 0000	H'E6054040	32

Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size
Output data high register 4	OUTDTH4	R/W	H'0000 0000	H'E6054044	32
Output data low register 4	OUTDTL4	R/W	H'0000 0000	H'E6054048	32
One edge/both edge select register 4	BOTHEDGE4	R/W	H'0000 0000	H'E605404C	32
General IO/interrupt switching register 5	IOINTSEL5	R/W	H'0000 0000	H'E6055000	32
General input/output switching register 5	INOUTSEL5	R/W	H'0000 0000	H'E6055004	32
General output register 5	OUTDT5	R/W	H'0000 0000	H'E6055008	32
General input register 5	INDT5	R	State of the port pins	H'E605500C	32
Interrupt display register 5	INTDT5	R	H'0000 0000	H'E6055010	32
Interrupt clear register 5	INTCLR5	R/W	H'0000 0000	H'E6055014	32
Interrupt mask register 5	INTMSK5	R/W	H'0000 0000	H'E6055018	32
Interrupt mask clear register 5	MSKCLR5	R/W	H'0000 0000	H'E605501C	32
Positive/negative logic select register 5	POSNEG5	R/W	H'0000 0000	H'E6055020	32
Edge/level select register 5	EDGLEVEL5	R/W	H'0000 0000	H'E6055024	32
Chattering prevention on/off register 5	FILONOFF5	R/W (for available bits)	H'0000 0000	H'E6055028	32
Interrupt sub mask register 5	INTMSKS5	R/W	H'0000 0000	H'E6055038	32
Interrupt sub mask clear register 5	MSKCLRS5	R/W	H'0000 0000	H'E605503C	32
Output data select register 5	OUTDTSEL5	R/W	H'0000 0000	H'E6055040	32
Output data high register 5	OUTDTH5	R/W	H'0000 0000	H'E6055044	32
Output data low register 5	OUTDTL5	R/W	H'0000 0000	H'E6055048	32
One edge/both edge select register 5	BOTHEDGE5	R/W	H'0000 0000	H'E605504C	32

6.4.1 General IO/Interrupt Switching Register n (IOINTSELn)

Note: n = 0 to 5

IOINTSEL selects either general input/output mode or interrupt input mode for each of the port pins 0 to 31 of the GPIO block. When general input/output mode is selected for a port, it is also necessary to select either input or output mode for the port using the corresponding bit in the general input/output switching register. When interrupt input mode is selected for a port, the setting of the general input/output switching register for the port is ignored.

[Hardware default value: H'00000000 = general input/output mode is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	IOINTSEL[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IOINTSEL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IOINTSEL[31:0]	All 0	R/W	Selects either general input/output mode or interrupt input mode for each port using the bits corresponding to the port numbers. 0: General input/output mode. 1: Interrupt input mode.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.2 General Input/Output Switching Register n (INOUTSELn)

Note: n = 0 to 5

INOUTSEL is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register. Specifically, INOUTSEL selects either general input or general output mode for a port using the bit corresponding to the port number. The INOUTSEL bits can be written to only when the corresponding bits in the general IO/interrupt switching register are 0. Note that after general input/output mode is changed to interrupt input mode, INOUTSEL retains the setting but is read as 0.

[Hardware default value: H'00000000 = general input mode is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INOUTSEL[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INOUTSEL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INOUTSEL[31:0]	All 0	R/W	Selects either general input mode or general output mode for each port using the bits corresponding to the port numbers. 0: General input mode 1: General output mode

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.3 General Output Register n (OUTDTn)

Note: n = 0 to 5

OUTDT is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register. Specifically, the value of the bit in OUTDT corresponding to the port number is inverted or not inverted depending on the setting of the positive/negative logic select register before being output from the corresponding port pin. Note that the polarity of the output signal should previously be set using the corresponding bit in the positive/negative logic select register. This register must be set after the output data select register is appropriately set to choose level of output data.

[Hardware default value: H'00000000 = 0 is output from all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDT[31:0]	All 0	R/W	Allows the port to output the value set in the bit corresponding to the port number when the port is appropriately set by IOINTSEL0 to IOINTSELn, INOUTSEL0 to INOUTSELn and OUTDTSEL0 to OUTDTSELn. (n = 5) 0: 0 is output. 1: 1 is output.

Note: The values set in OUTDT are not directly output from the GPIO pins; the above set values are processed according to the settings of the positive/negative logic select register before being output.
Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available

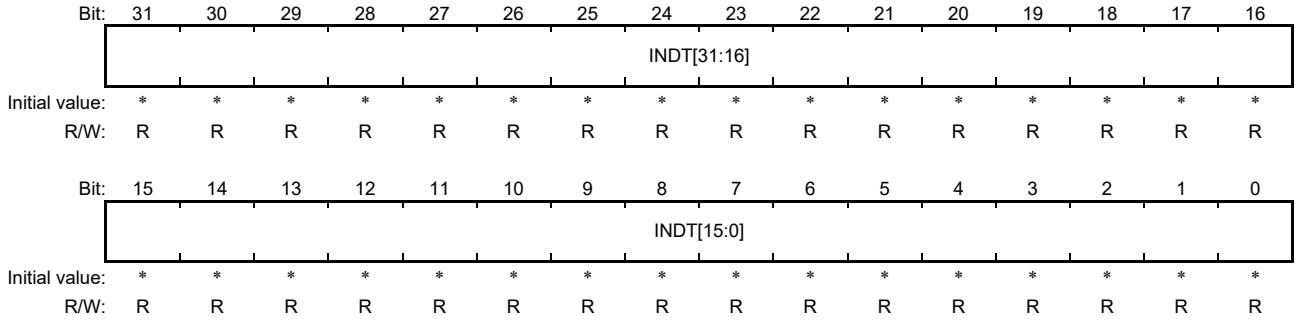
6.4.4 General Input Register n (INDTn)

Note: n = 0 to 5

INDT is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general input mode is selected by the general input/output switching register. Each bit reflects the value received through the corresponding port pin.

Note that when a bit in the positive/negative logic select register is 1, the corresponding bit in INDT indicates the inverted value of the input signal.

[Hardware default value: state of the signals input to the port pins.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INDT[31:0]	*	R	Each bit reflects the value received through the corresponding port pin. 0: Input is 0. (assuming positive logic) 1: Input is 1. (assuming positive logic)

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

* State of the signals input to the port pins.
* The GPIO input function is still enabled even if after the pin function has been set for any modules other than the GPIO; if the module pin setting is input, the input signal is also propagated to the GPIO block and the GPIO input related registers are updated by the latest input of the corresponding pin. It may occur an unexpected GPIO interrupt unless the GPIO interrupt is masked.
* The GPIO interrupt should be masked when the multiplexed pin is used for input of other than the GPIO function. Refer to section 6.4.7, INTMSKn for the GPIO interrupt mask.

6.4.5 Interrupt Display Register n (INTDTn)

Note: n = 0 to 5

INTDT is valid only when interrupt input mode is selected by the general IO/interrupt switching register. Specifically, when an interrupt is input via a port pin when INTDT is valid, the bit in INTDT corresponding to the port indicates whether the port has received an interrupt input or not. In interrupt input mode, the polarity and detection conditions (one edge/both edge or level) of the external input signal can be set for each port pin. Before using a port pin for interrupt input, the corresponding bits in the positive/negative logic select register and edge/level select register (one edge/both edge register should be appropriately configured if edge detection mode is selected) should be set, respectively.

If a port is set for edge detection using the corresponding bit in the edge/level select register, even when an external pulse interrupt signal is input, the corresponding bit in INTDT holds the input using the FF and allows the level interrupt signal to be output to the interrupt control block.

To stop all the interrupt signal outputs, all the bits in the interrupt clear register corresponding to the bits in INTDT currently indicating the reception of the corresponding interrupt signals should be cleared to 0. Note that if a port is set for level detection using the corresponding bit in the edge/level select register and an external level interrupt signal is input, the corresponding bit in INTDT does not use the FF to hold the input. Therefore, when an external input signal is stopped, the corresponding bit in INTDT is cleared automatically. When all the bits in INTDT are turned off (= 0), the GPIO stops outputting all the interrupt signals.

[Hardware default value: H'00000000 = no interrupt signals are input from ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTDT[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTDT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTDT[31:0]	All 0	R	Each bit indicates the input of an interrupt signal on the corresponding port pin. 0: No interrupt signal has been input. 1: Interrupt signal has been input.

Conditions of Indicating Interrupt Input:

1. For level-sensitive interrupt input (EDGLEVEL = 0)
   - External input signals are constantly monitored and indicated. (When the negative logic is selected, the inverted value of the external input signal is indicated.)
2. For edge-sensitive interrupt input (EDGLEVEL = 1)
   - Clearing condition: When the interrupt clear register is cleared, indication is cleared regardless of the positive/negative logic select register.
   - Setting condition: With the positive logic (POSNEG = 0), when the rising edge of an external interrupt signal is detected, the interrupt input is indicated. With the negative logic (POSNEG = 1), when the falling edge is detected, the interrupt input is indicated. With both edge mode (BOTHEDGE = 1), when either the rising or falling edge, the interrupt input is indicated.

Notes: * The GPIO input function is still enabled even if after the pin function has been set for any modules other than the GPIO; if the module pin setting is input, the input signal is also propagated to the GPIO block and the GPIO input related registers are updated by the latest input of the corresponding pin. It may occur an unexpected GPIO interrupt unless the GPIO interrupt is masked.

* The GPIO interrupt should be masked when the multiplexed pin is used for input of other than the GPIO function. Refer to section 6.4.7, INTMSKn for the GPIO interrupt mask.

6.4.6 Interrupt Clear Register n (INTCLRn)

Note: n = 0 to 5

When the interrupt display register currently indicates the reception of the interrupt input on the port for which the edge detection is selected by the edge/level select register (with configuring for one edge/both edge select register) in interrupt input mode, INTCLR clears the indication. Specifically, writing 1 to the bits in INTCLR corresponding to port numbers can clear the corresponding bits in the interrupt display register. However, when the interrupt display register currently indicates the reception of the interrupt input on the port for which the level detection is selected by the edge/level select register, writing 1 to the corresponding bits in INTCLR cannot clear the corresponding bits in the interrupt display register. Only writing 1 to INTCLR is effective; INTCLR is always read as 0.

[Hardware default value: H'00000000 = interrupt indication is cleared for no ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTCLR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTCLR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTCLR[31:0]	All 0	R/W	Writing 1 to bits corresponding to port numbers clears the corresponding bits in the interrupt display register. 0: No effect 1: Interrupt display register bit is cleared.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.7 Interrupt Mask Register n (INTMSKn)

Note: n = 0 to 5

INTMSK masks the interrupt requests indicated by the interrupt display register. Interrupts can be separately masked using the corresponding bits in INTMSK. When all the bits currently indicating the reception of the interrupt signals are masked, no interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt mask clear register. Only writing 0 to this register is effective.

[Hardware default value: H'00000000 = all the ports are masked.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTMSK[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTMSK[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTMSK[31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding interrupt signal to be output to the interrupt control block. 0: Interrupt is masked. 1: Interrupt is not masked.

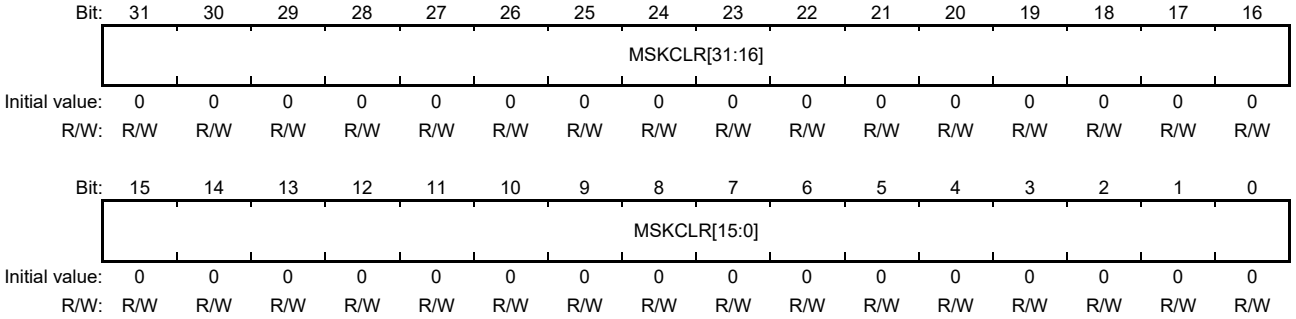
Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.8 Interrupt Mask Clear Register n (MSKCLRn)

Note: n = 0 to 5

MSKCLR cancels masks that are set by the interrupt mask register. Each mask can be canceled (cleared) by writing 1 to the corresponding bit in MSKCLR. Only writing 1 to MSKCLR is effective; MSKCLR is always read as 0.

[Hardware default value: H'00000000 = interrupt masks are cleared for no ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKCLR[31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding interrupt signal to be output to the interrupt control block. 0: No effect 1: Interrupt is not masked.

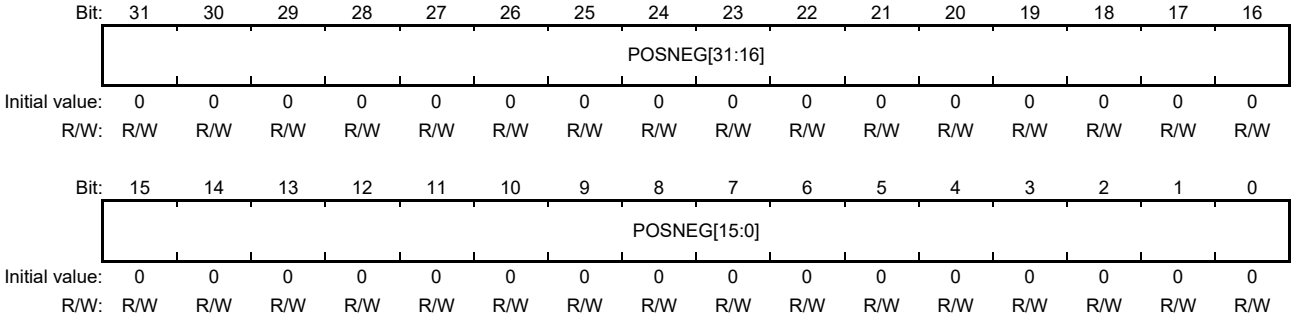
Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.9 Positive/Negative Logic Select Register n (POSNEGn)

Note: n = 0 to 5

POSNEG selects the polarity (positive or negative logic) of each port pin in general input mode, general output mode, or interrupt input mode. POSNEG should be set before mode selection.

[Hardware default value: H'00000000 = positive logic is selected for all the ports.]



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	POSNEG[31:0]	All 0	R/W	Selects the polarity (positive or negative logic) of each port pin. 0: Positive logic 1: Negative logic

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.10 Edge/level Select Register n (EDGLEVELn)

Note: n = 0 to 5

EDGLEVEL is valid only for the ports for which interrupt input mode is selected by the general IO/interrupt switching register. Specifically, EDGLEVEL selects the detection conditions (edge or level) of the interrupt input signal on each port pin for which interrupt input mode is selected. EDGLEVEL should be set before selection of interrupt input mode.

[Hardware default value: H'00000000 = level detection is selected for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDGLEVEL[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDGLEVEL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDGLEVEL [31:0]	All 0	R/W	Selects the level or edge as detection conditions of the interrupt input signal on each port pin for which interrupt input mode is selected. 0: Level 1: Edge

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.11 Chattering Prevention On/Off Register n (FILONOFFn)

Note: n = 0 to 5

FILONOFF prevents chattering input to the port pins 0 to 3 of each GPIO block and controls frequency of filter clock (generated from peripheral clock CPϕ) for chattering prevention function. For details, refer to section 6.5, Handling of Input Signals on Port Pins.

[Hardware default value: H'00000000 = chattering prevention function is turned off for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CLKSEL[1:0]		—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FILONOFF[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	CLKSEL[1:0]	00	R/W	Filter clock frequency setting. 00: CPϕ/25000. 01: CPϕ/12500. 10: CPϕ/6250. 11: CPϕ/3125.
29 to 4	—	0	R	Reserved. (These bits are always read as 0. The write value should always be 0)
3 to 0	FILONOFF[3:0]	All 0	R/W	Enables or disables the chattering prevention function. 0: Chattering prevention function is disabled. 1: Chattering prevention function is enabled. The bits FILONOFF[n] (n = 0 to 3) are used to control the port pin n.

Note: Unused bits should be set to the initial values.

6.4.12 Interrupt Sub Mask Register n (INTMSKSn)

Note: n = 0 to 5

INTMSKS masks the alternative interrupt requests indicated by the interrupt display register. Interrupts can be separately masked using the corresponding bits in INTMSKS. When all the bits currently indicating the reception of the interrupt signals are masked, no alternative interrupt signals are output to the interrupt control block. Masks can be canceled by writing 1 to the corresponding bits in the interrupt sub mask clear register. Only writing 0 to this register is effective.

[Hardware default value: H'00000000 = all the ports are masked.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	INTMSKS[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTMSKS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	INTMSKS[31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding alternative interrupt signal to be output to the interrupt control block. 0: Interrupt is masked. 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.13 Interrupt Sub Mask Clear Register n (MSKCLRSn)

Note: n = 0 to 5

MSKCLRS cancels masks that are set by the interrupt sub mask register. Each mask can be canceled (cleared) by writing 1 to the corresponding bit in MSKCLRS. Only writing 1 to MSKCLRS is effective; MSKCLRS is always read as 0.

[Hardware default value: H'00000000 = alternative interrupt masks are cleared for no ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSKCLRS[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSKCLRS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKCLRS[31:0]	All 0	R/W	Setting a mask to the bit disables the corresponding alternative interrupt signal to be output to the interrupt control block. 0: No effect 1: Interrupt is not masked.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.
(When GPIO is not selected by the pin multiplex settings, do not cancel the alternative interrupt mask.)

6.4.14 Output Data Select Register n (OUTDTSELn)

Note: n = 0 to 5

OUTDTSEL is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register. OUTDTSEL selects if OUTDT or OUTDTH/OUTDTL will be the output data of GPIO. When choosing OUTDT, configuration is performed as described in section 6.4.3, General Output Register n (OUTDT0 to OUTDTn). When choosing OUTDTH/OUTDTL, output data will be output by writing the appropriate data to the corresponding bits in OUTDTH or OUTDTL. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be set before writing data to OUTDTH/OUTDTL registers.

[Hardware default value: H'00000000 = Out data register is used to output data.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDTSEL[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDTSEL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTSEL [31:0]	All 0	R/W	Choosing whether output data is output by general output register OUTDT or output data high register OUTDTH/output data low register OUTDTL. 0: General output register is used to output the data. 1: Output data high register and output data low register is used to output the data.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.15 Output Data High Register n (OUTDTHn)

Note: n = 0 to 5

OUTDTH is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register, and the output data select register OUTDTSEL is configured to choose OUTDTH/OUTDTL register to output the data of GPIO. Only writing 1 to OUTDTH is effective. Otherwise, setting makes no changes. Reading OUTDTH returns the values of the latest data set to OUTDTH or OUTDTL right before that. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be written and read after output data select register OUTDTSEL is set. Reading OUTDTH without appropriately configuring OUTDTSEL can return value of OUTDT register.

[Hardware default value: H'00000000 = 0 is output from all the ports with setting OUTDTSEL.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDTH[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDTH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTH[31:0]	All 0	R/W	Outputting high value data. 0: Invalid data. 1: Valid data.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.16 Output Data Low Register n (OUTDTLn)

Note: n = 0 to 5

OUTDTL is valid only for the ports for which general input/output mode is selected by the general IO/interrupt switching register and then general output mode is selected by the general input/output switching register, and the output data select register OUTDTSEL is configured to choose OUTDTH/OUTDTL register to output the data of GPIO. Only writing 0 to OUTDTL is effective. Otherwise, setting makes no changes. Reading OUTDTL returns the values of the latest data set to OUTDTL or OUTDTH right before that. Note that the polarity of the output signal should be previously set using the corresponding bit in the positive/negative logic select register. Furthermore, this register should be written or read after output data select registers OUTDTSEL is set. Reading OUTDTH without appropriately configuring OUTDTSEL can return value of OUTDT register.

[Hardware default value: H'00000000 = 0 is output from all the ports with setting OUTDTSEL.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	OUTDTL[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OUTDTL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	OUTDTL[31:0]	All 0	R/W	Outputting low value data. 0: Valid data. 1: Invalid data.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.4.17 One Edge/Both Edge Select Register n (BOTHEDGEn)

Note: n = 0 to 5

BOTHEDGE is valid only when the edge detection mode is selected by the edge/level select registers. Specially, BOTHEDGE selects the detection condition (one edge or both edges) of the interrupt input signal on each port pin for which interrupt input mode (selected by the general IO/interrupt switching registers) and edge detection mode are selected. BOTHEDGE should be set before selection of interrupt input mode.

[Hardware default value: H'00000000 = both edge detection mode is disabled for all the ports.]

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BOTHEDGE[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BOTHEDGE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	BOTHEDGE [31:0]	All 0	R/W	Selecting one edge or both edge detection condition of the interrupt input signal on each port pin for which interrupt input mode and edge detection mode are selected. 0: One edge. 1: Both edges.

Note: Unused bits should be set to the initial values. Please refer to GPIO pin number from Table 6.2 to know what bit is unused. For example: GPIO 0 has 23 pins that mean only bit 0 to bit 23 is available.

6.5 Handling of Input Signals on Port Pins

6.5.1 Chattering

In general input mode and interrupt input modes, a filtering function can be used for the port pins 0 to 3 of each GPIO block to prevent external chattering input. Specifically, when a bit in the chattering prevention on/off register is set to use the function, the external input to the corresponding port pin is sampled four consecutive times based on the filter clock signal, which is internally generated by the GPIO. The external input is canceled except when the active input is detected four consecutive times. Therefore, when a filtering function is used, input to the port pins 0 to 3 of each GPIO block need to be at least four sampling clock cycles long (with the peripheral clock (CPϕ)).

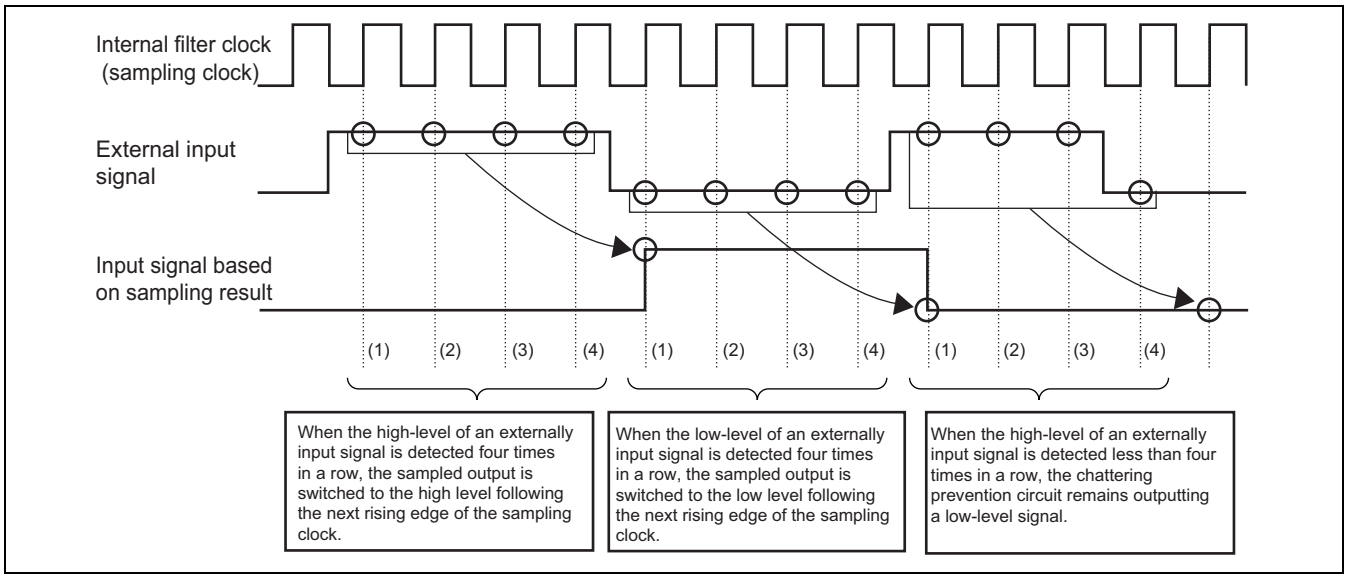


Figure 6.2 Sampling Timing Chart

6.5.2 Input Signal Synchronization

In general input mode and interrupt input mode, external input signals on all port pins are synchronized with the GPIO clock (CPϕ).

6.6 Interrupt Display Timing Charts

Figure 6.3 shows the interrupt display timing and Figure 6.4 shows the note on the timing. In both figures, the positive logic and edge-sensitive input are assumed.

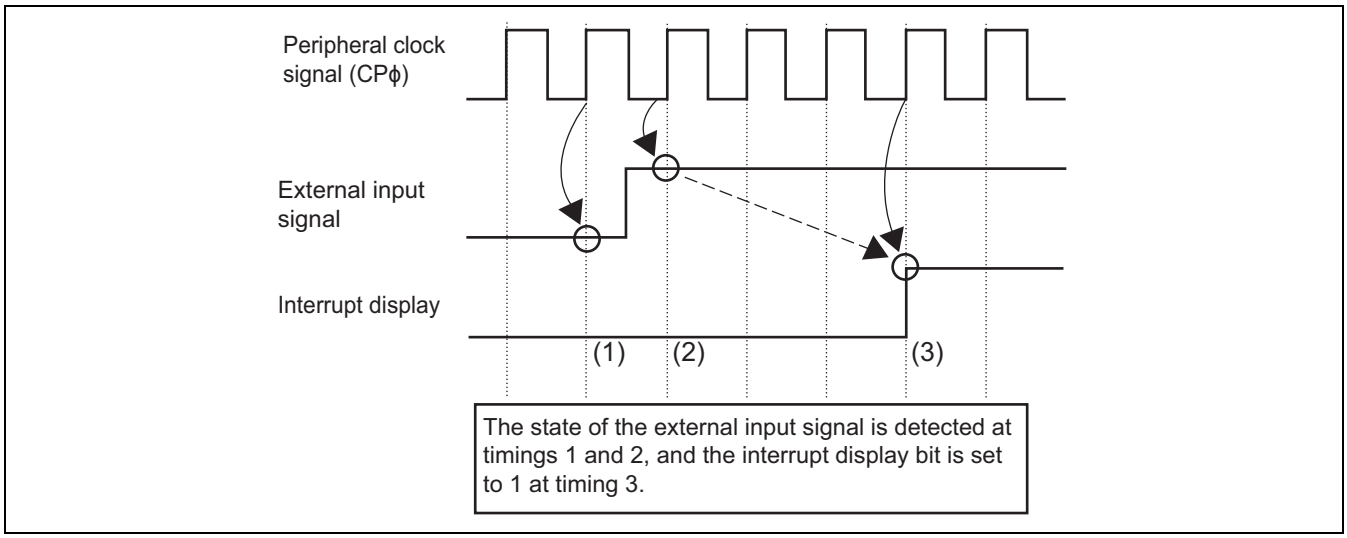


Figure 6.3 Interrupt Display Timing

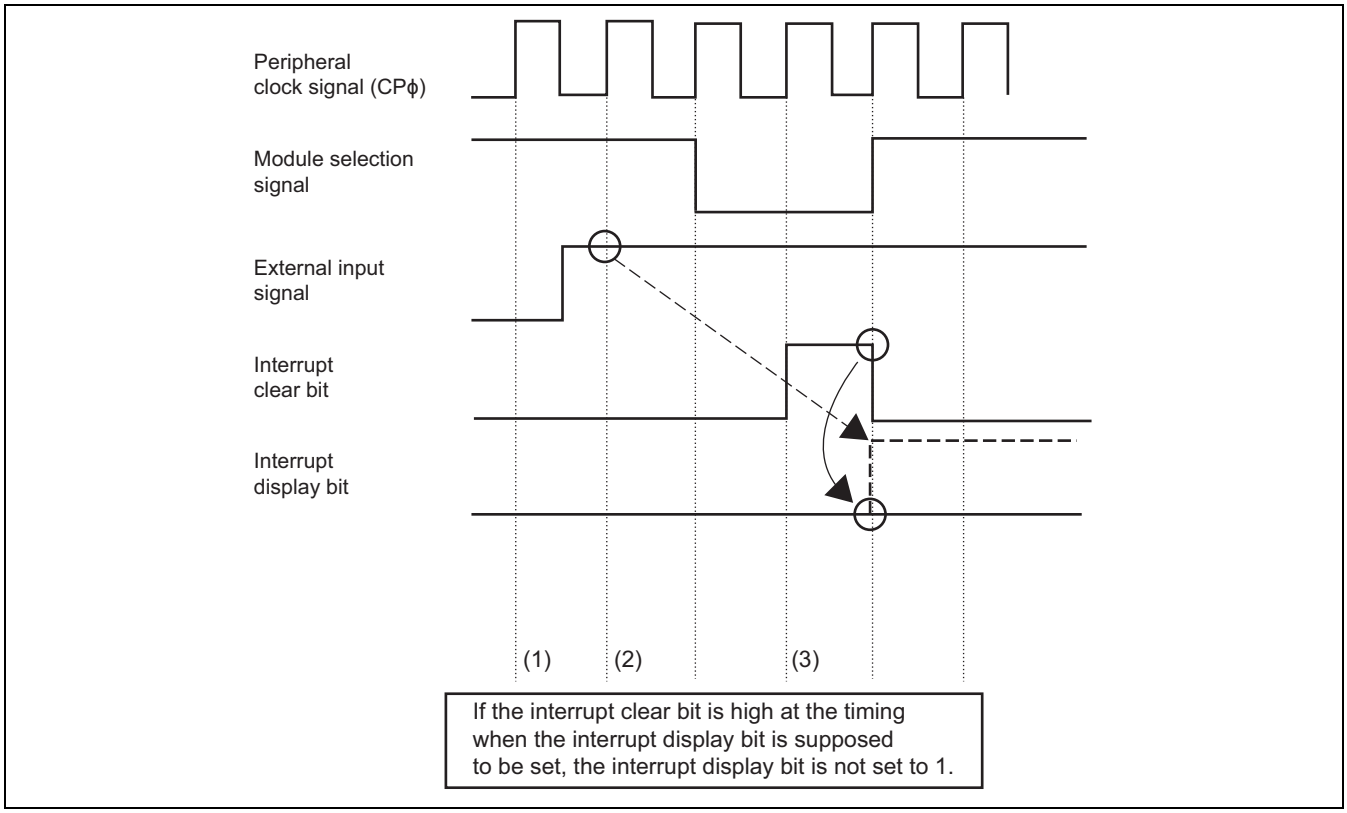


Figure 6.4 Notes on Interrupt Display Timing

6.7 Using GPIO

The following sections describe how to use the GPIO. If the GPIO is not used according to the procedures shown here, operations are not guaranteed.

6.7.1 Setting Edge-Sensitive Interrupt Input Mode

For setting edge-sensitive interrupt input mode, refer to the procedure shown in Figure 6.5.

Note that an unexpected interrupt might be generated in the module if setting (1), (2), (3) or (4) in the flowchart is changed. When changing the setting, (5) and (6) should be done.

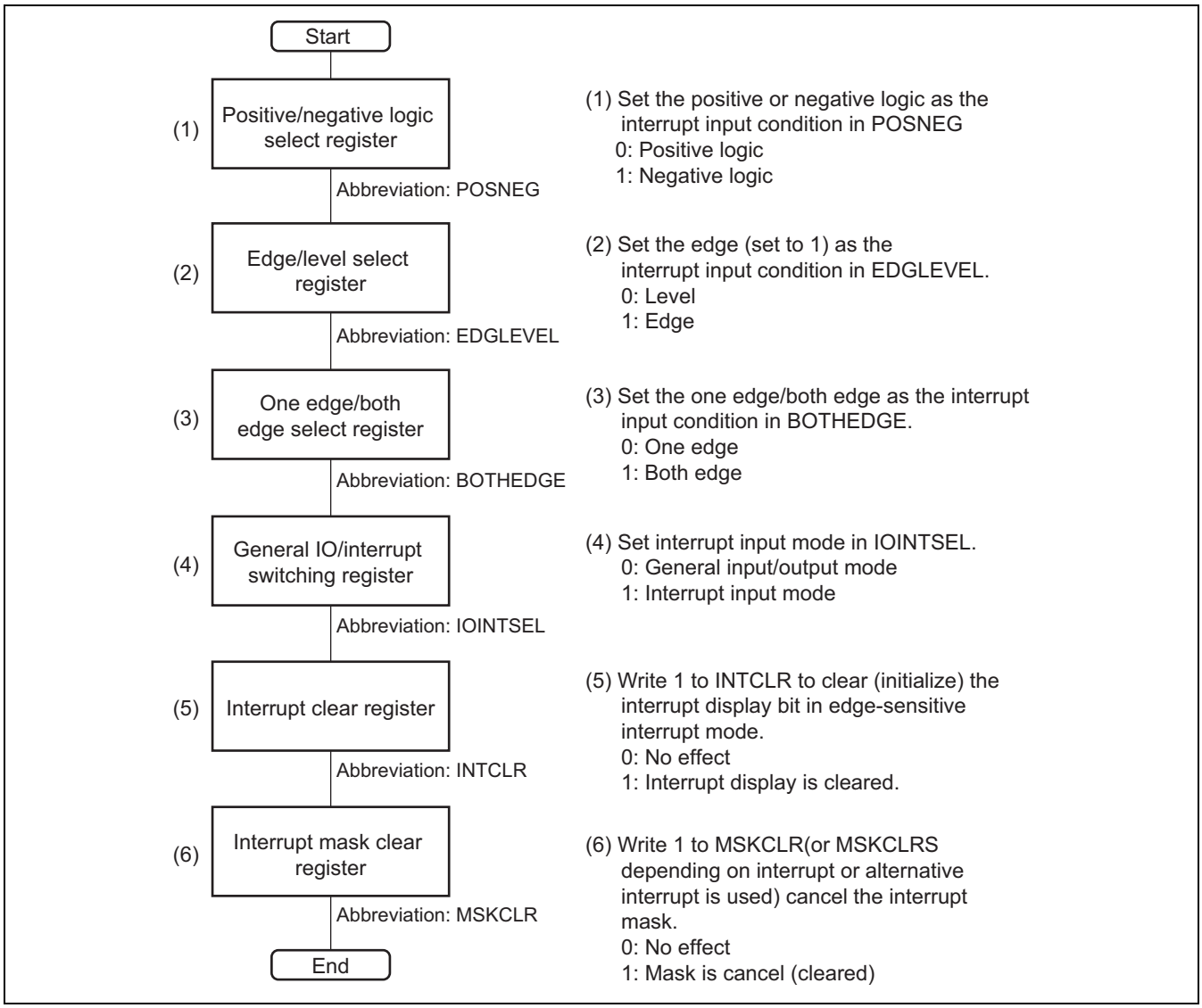


Figure 6.5 Flowchart of Setting the GPIO to Edge-Sensitive Interrupt Input Mode

6.7.2 Setting Level-Sensitive Interrupt Input Mode

For setting level-sensitive interrupt input mode, refer to the procedure shown in Figure 6.6.

Note that when an external level-sensitive interrupt input signal is stopped, the corresponding interrupt is canceled automatically. In level-sensitive interrupt input mode, the interrupt clear register is invalid.

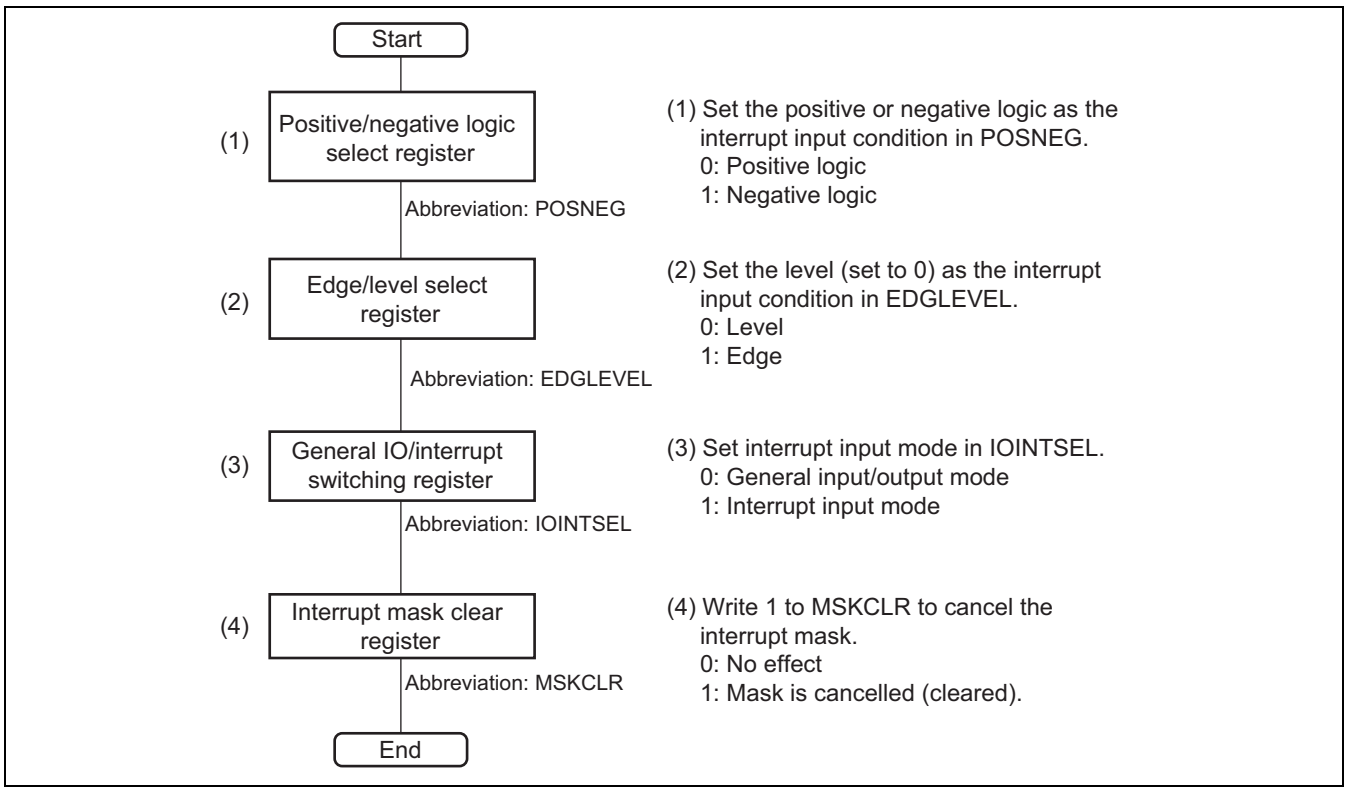


Figure 6.6 Flowchart of Setting the GPIO to Level-Sensitive Interrupt Input Mode

6.7.3 Setting General Output Mode

For setting general output mode, refer to the procedure shown in Figure 6.7.

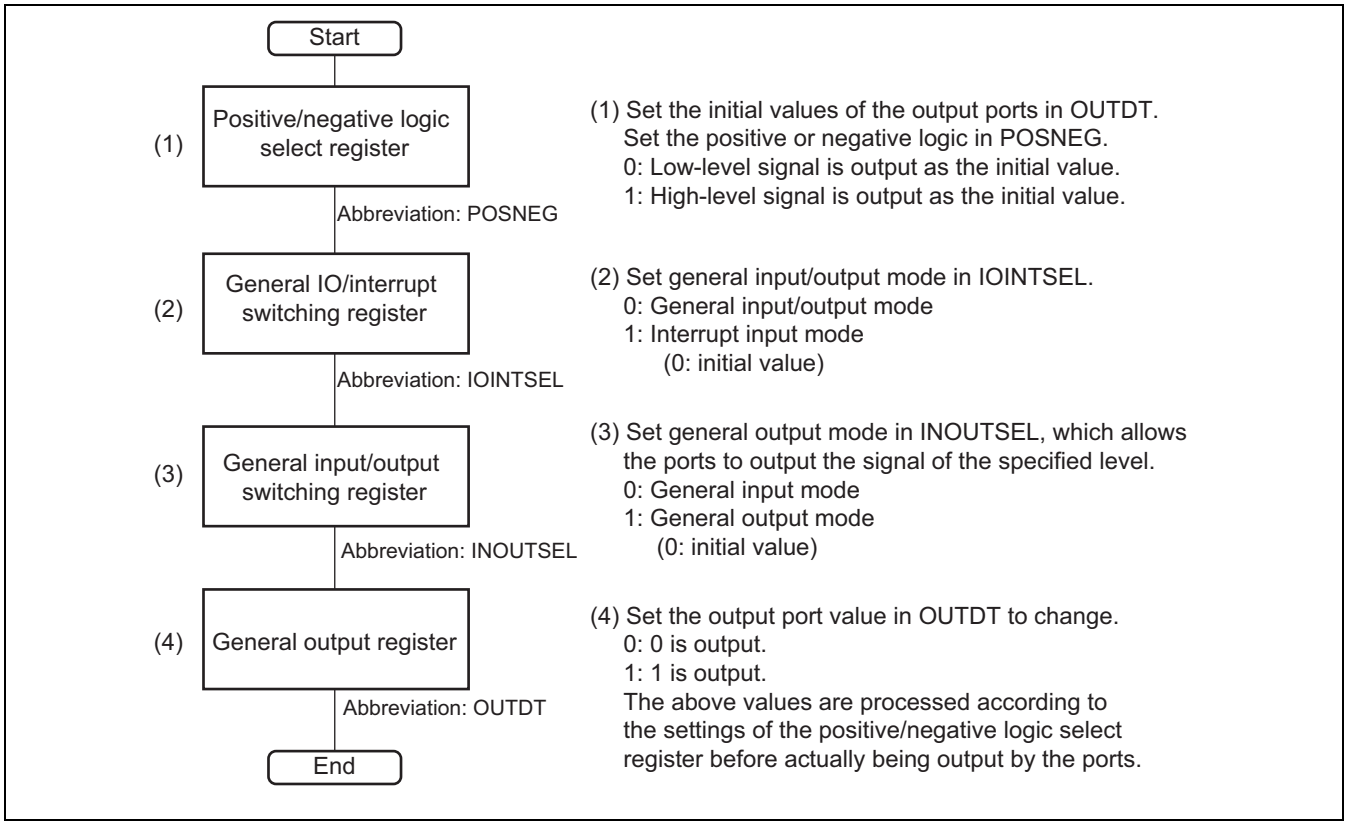


Figure 6.7 Flowchart of Setting the GPIO to General Output Mode

6.7.4 Setting Output data high/Output data low Mode

For setting output data high/output data low mode, refer to the procedure shown in Figure 6.8.

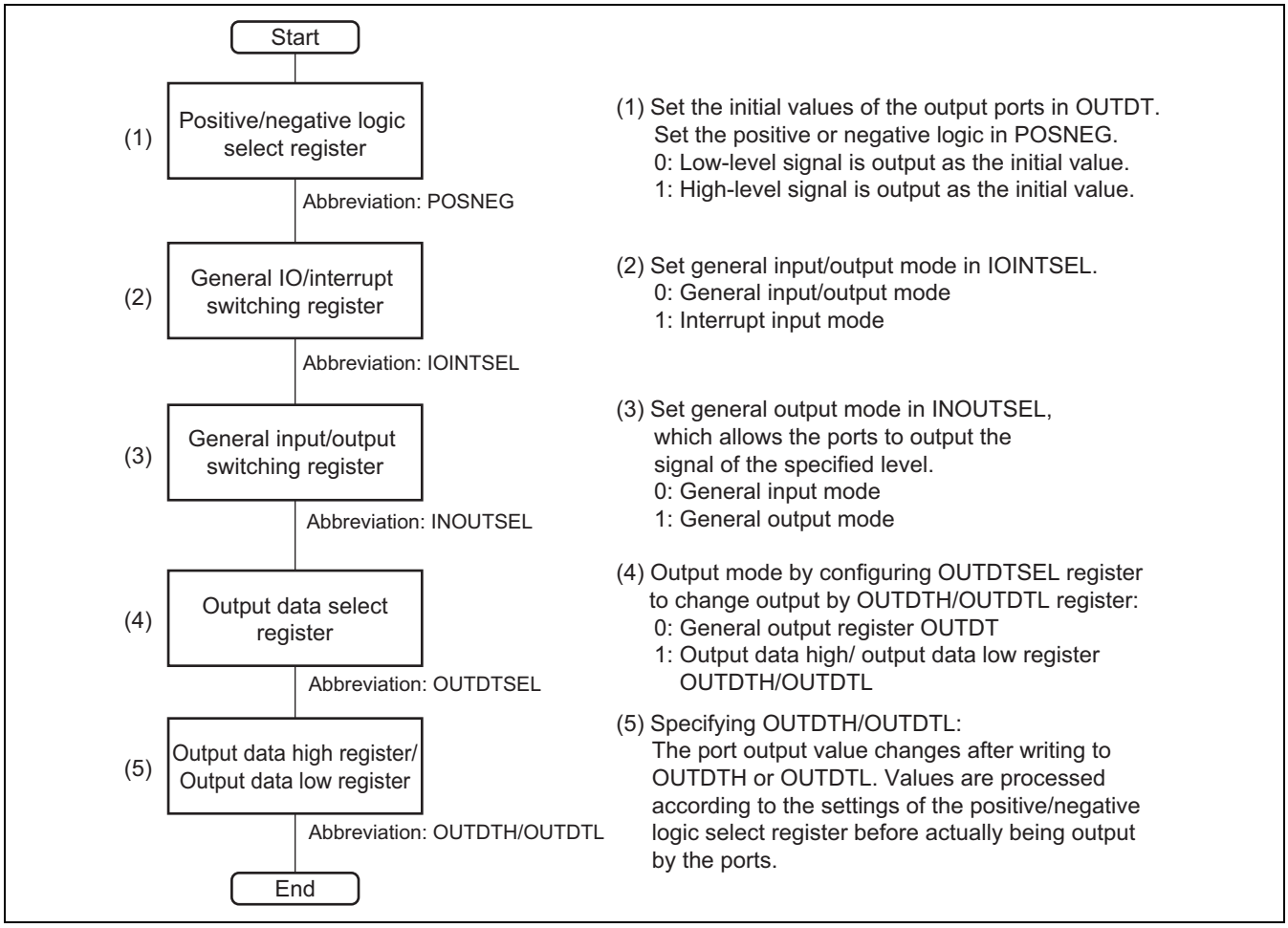


Figure 6.8 Flowchart of Setting the GPIO to Output data high/ Output data low Mode

6.7.5 Setting General Input Mode

For setting general input mode, refer to the procedure shown in Figure 6.9.

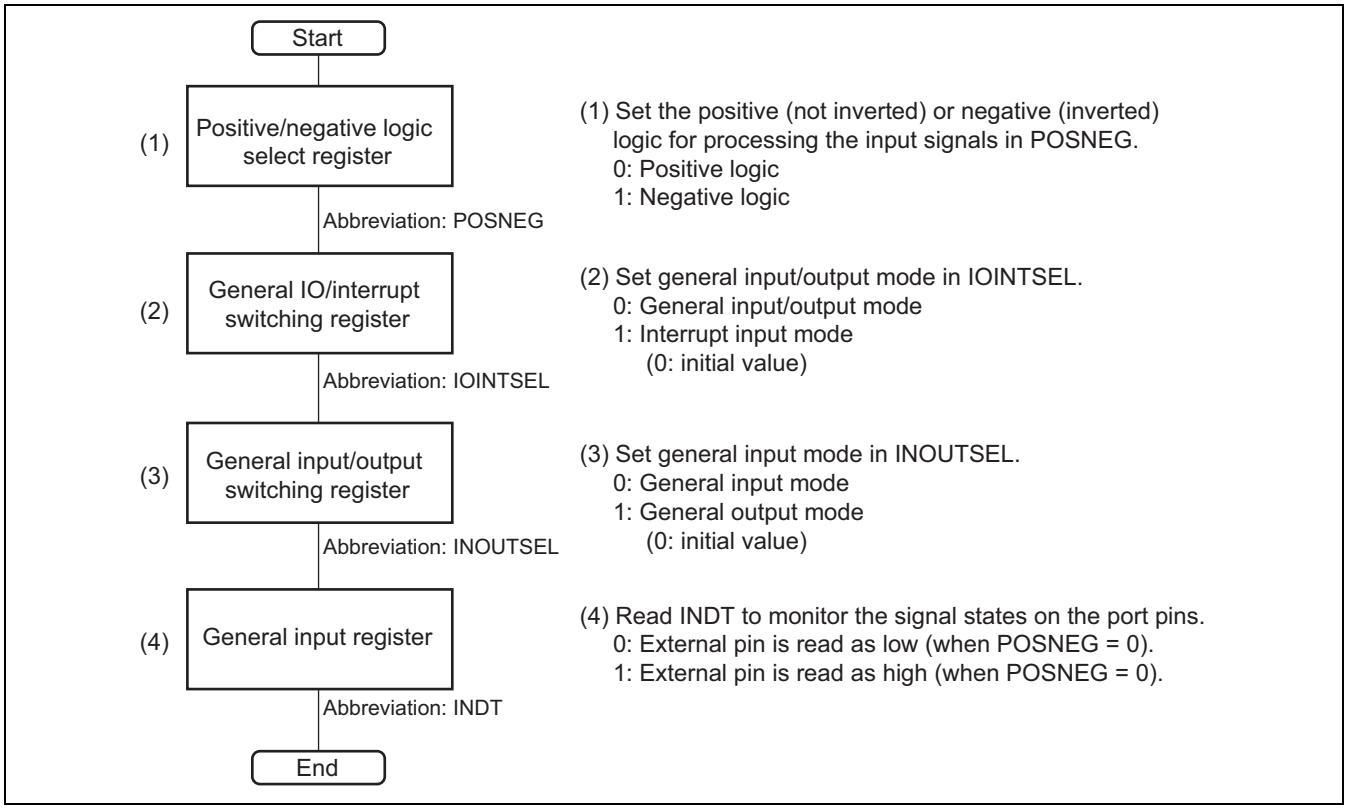


Figure 6.9 Flowchart of Setting the GPIO to General Input Mode

7. Clock Pulse Generator (CPG)

7.1 Overview

This LSI has a clock pulse generator (CPG). The CPG consists of oscillators, PLL circuit 0, PLL circuit 1, PLL circuit 3, clock dividers, and the control circuit. The CPG generates various clocks used by this LSI.

7.1.1 Features

- Generates various clocks for LSI internal operation.
  - 3 PLLs for common/application part modules
  - SYS-CPU divider, common divider and DDR divider for system basic operation.
  - Dedicated dividers for special clock
- Controls clock supply to modules according to the module status (power supply status, etc.)

A block diagram of the CPG is shown in Figure 7.1.

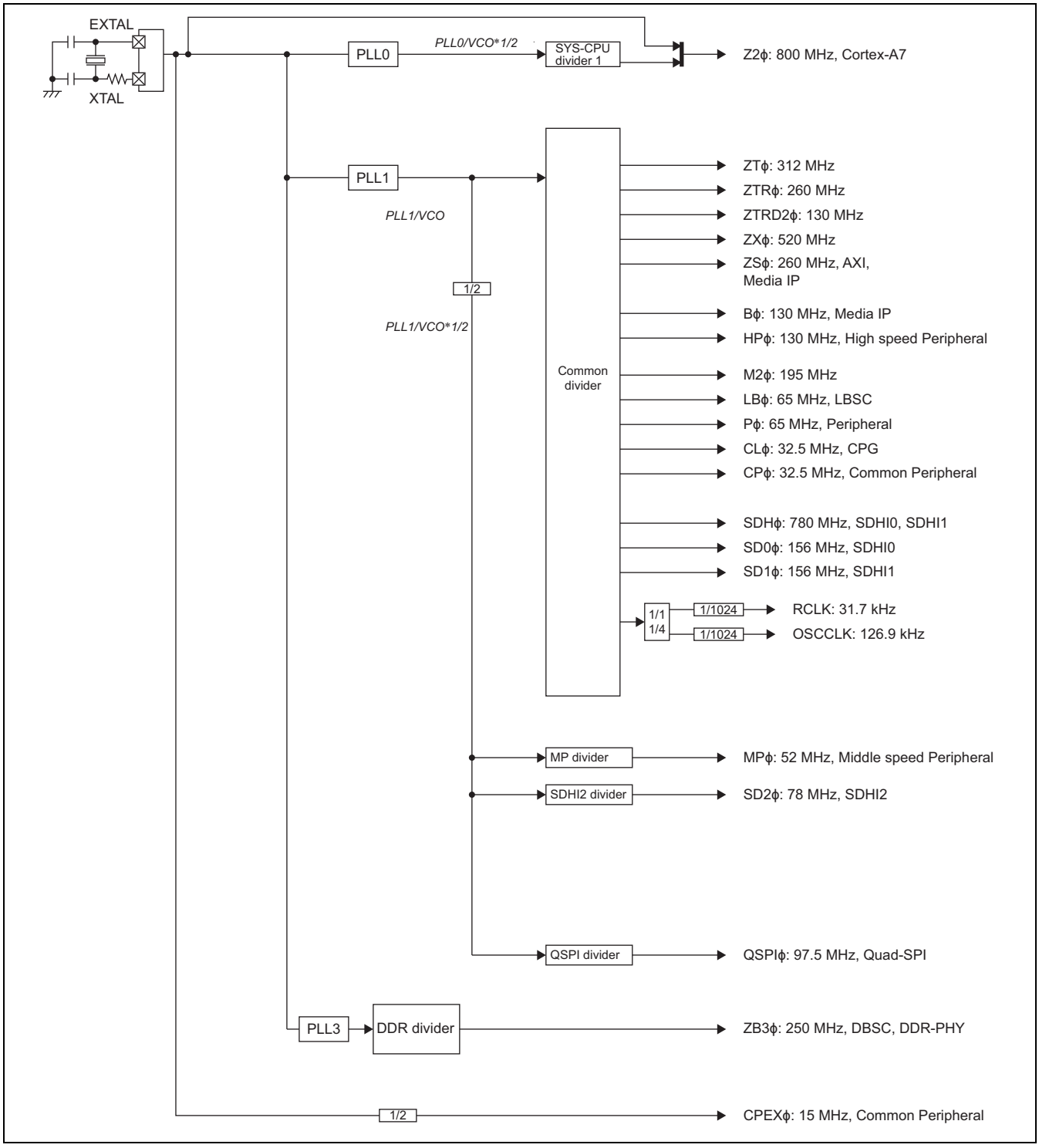


Figure 7.1 Block Diagram of CPG

Followings are the functions of each block of CPG.

(1) PLL circuit 0 (PLL0)

PLL circuit 0 multiplies EXTAL clock. The multiplication ratio is set by the PLL0CR.

(2) PLL circuit 1 (PLL1)

PLL circuit 1 multiplies the input clock from EXTAL by the multiplication ratio shown in Table 7.4.

(3) PLL Circuit 3 (PLL3)

PLL circuit 3 multiplies the input clock from EXTAL by the multiplication ratio shown in Table 7.4.

(4) SYS-CPU clock divider 1

The SYS-CPU clock divider 1 divides PLL0 output clock. This divider generates the AP-System core clocks (Z2ϕ).

(5) Common clock divider

The common clock divider divides PLL1 output clock. This divider generates various system clocks. The division ratio is set by the frequency control register B (FRQCRB).

(6) DDR clock divider

The DDR clock divider divides PLL3 output clock, and generates DDR-PHY clock and DBSC clock.

(7) Dedicated dividers

The each dedicated divider generates special clock for the related modules.

7.1.2 Input/Output Pins

Table 7.1 lists the CPG pin configuration.

Table 7.1 Pin Configuration and Functions of CPG

Pin Name	Function	I/O	Description
XTAL	Clock input pins	Output	Outputs amplified negative feedback of EXTAL
EXTAL		Input	Used as an external clock input pin
CLKOUT	External Bus Clock output pin	Output	Used as an external clock output pin
MD0	Mode 0	Input	Be sure to set MD0 to 0.
MD9	Mode 9	Input	EXTAL/XTAL pin setting
MD13	Mode 13	Input	PLL multiplication ratio setting
MD14	Mode 14	Input	PLL multiplication ratio setting

7.1.3 List of Clock Outputs

Table 7.2 lists the clock output of CPG.

Table 7.2 List of Clocks

Name	Clock Source	Frequency			Clock Domain, Function
		Dividing ratio	Maximum	Initial	
Z2ϕ	SYS-CPU divider 1	Variable	1 GHz	~800 MHz	System CPU (Cortex-A7) clock
ZTRϕ	Common divider	Variable	260 MHz	260 MHz	Trace interface clock
ZTRD2ϕ	Common divider	Variable	130 MHz	130 MHz	System trace interface clock
ZTϕ	Common divider	Variable	312 MHz	312 MHz	Internal trace clock
ZXϕ	Common divider	Fixed	520 MHz	520 MHz	
ZSϕ	Common divider	Fixed	260 MHz	260 MHz	AXI clock / media IP clock
HPϕ	Common divider	Fixed	130 MHz	130 MHz	High-speed peripheral clock
Bϕ	Common divider	Fixed	130 MHz	130 MHz	Media clock
LBϕ	Common divider	Fixed	65 MHz	65 MHz	LBSC clock
Pϕ	Common divider	Fixed	65 MHz	65 MHz	Peripheral clock
CLϕ	Common divider	Fixed	32.5 MHz	32.5 MHz	CPG
CPϕ	Common divider	Fixed	32.5 MHz	32.5 MHz	Common peripheral
M2ϕ	Common divider	Fixed	195 MHz	195 MHz	Media clock 2
ZB3ϕ	DDR divider	Fixed	400 MHz	400 MHz	DBSC/DDR-PHY clock
SDHϕ	Common divider	Variable	780 MHz	780 MHz	SDHI clock H
SD0ϕ	Common divider	Variable	156 MHz	97.5 MHz	SDHI clock 0
SD1ϕ	Common divider	Variable	156 MHz	97.5 MHz	SDHI clock 1
SD2ϕ	SDHI2 divider	Variable	78 MHz	48.75 MHz	SDHI clock 2
MPϕ	MP divider	Fixed	52 MHz	52 MHz	MP clock
QSPIϕ	QSPI divider	Variable	97.5 MHz	*1	QSPI clock
CPEXϕ	EXTAL	Fixed	15 MHz	*2	Common peripheral clock, EXTAL × 1/2
RCANϕ	USB_EXTAL	Fixed	8 MHz *4	*3	RCAN clock USB_EXTAL × 1/6
RCLK	Common divider	Fixed	31.7 kHz	31.7 kHz	
OSCCLK	Common divider	Fixed	126.9 kHz	126.9 kHz	

Notes: 1. The frequency of QSPIϕ depends on the value of MD3, MD2 and MD1.
When MD3 = L, MD2 = H, MD1 = L, QSPIϕ = 97.5 MHz.
In the other cases of MD3, MD2 and MD1 setting, QSPIϕ = 78 MHz.
2. The frequency of CPEXϕ is equal to EXTAL × 1/2. For example, when the frequency of EXTAL is equal to 20 MHz, the frequency of CPEXϕ is equal to 10 MHz.
3. The frequency of RCANϕ is equal to USB_EXTAL × 1/6.
4. The maximum value of the RCAN clock frequency is defined by calculating from the frequency of divided-by-6 of the USB clock. Note that external clock input from USB_EXTAL pin is not supported; use the crystal resonator for the USB clock.

7.1.4 Clock Operating Modes

Table 7.3 MD9 Settings

MD9	EXTAL/XTAL Pin Settings
0	Inputs an external clock to the EXTAL pin.
1	Connects the crystal resonator to the EXTAL and XTAL pins.

Table 7.4 PLL Multiplication Ratio

MD14	MD13	EXTAL Input Frequency (MHz)	Divider Setting of EXTAL Input	PLL0*1 Multiplication Ratio	PLL1*3 Multiplication Ratio	PLL3*2 Multiplication Ratio
0	0	20	× 1	× 80	× 78	× 50
0	1	26	× 1	× 60	× 60	× 56
1	0	Prohibited setting				
1	1	30	× 1	× 52	× 52	× 50

Notes: 1. PLL to create Z2ϕ for Cortex-A7

Example of frequency calculation (in the case MD14 = H, MD13 = H)
VCO output frequency of PLL0 = 30 MHz × 52 = 1560 MHz
Frequency of Z2ϕ = 1560 MHz × 1/2 (fixed divider) = 780 MHz

2. PLL to create clocks related to DBSC & DDR-PHY
3. PLL to create the other clocks

7.1.5 Register Configuration

Table 7.5 shows the CPG register configuration block. Table 7.6 shows the register states in each operating mode.

32bit-width access is only available when access to this register.

Table 7.5 Register Configurations

Register Name	Abbreviation	R/W	Address	Access Size
Frequency control register B	FRQCRB	R/W	H'E615 0004	32
PLL Enable Control Register	PLLECR	R	H'E615 00D0	32
PLL0 control register	PLL0CR	R/W	H'E615 00D8	32
RGX control register	RGXCR	R/W	H'E615 00B4	32
SDHI clock frequency control register	SDCKCR	R/W	H'E615 0074	32
SDHI2 clock frequency control register	SD2CKCR	R/W	H'E615 0078	32
RCAN clock frequency control register	RCANCKCR	R/W	H'E615 0270	32

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

Table 7.6 Register States in Each Operating Mode

Register	Power-On Reset
All Registers	Initialized

7.2 Register Description

Legend for Register Description

Initial value : Register value after a reset

— : Undefined value

R/W : Readable/writable. The written value can be read.

R : Read-only.

W : Write-only. The read value is undefined.

7.2.1 Frequency Control Register B (FRQCRB)

FRQCRB is a 32-bit readable/writable register. This register specifies the frequency division ratios of debug trace port clock (ZTRϕ), debug trace bus clock (ZTϕ), and debug clock (ZTRD2ϕ).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	KICK	—	—	—	—	—	—	—	ZTRFC[3:0]				ZTFC[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	ZTRD2FC[3:0]			
Initial value:	0	0	0	1	0	0	1	1	0	1	0	1	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	KICK	0	R/W	KICK bit Setting 1 to this register activates the FRQCRB setting. 0: Does not activate the FRQCRB settings. 1: Activates the FRQCRB settings. This bit is automatically cleared to 0 when the frequency division setting is completed after 1 is written to this bit.
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 20	ZTRFC[3:0]	0011	R/W	Debug Trace port Clock (ZTRϕ) Frequency Division Ratio 0011: × 1/6 0100: × 1/8 0101: × 1/12 0110: × 1/16 0111: × 1/18 1000: × 1/24 Other values: Setting prohibited Note: ZTRϕ is supplied only in debugging mode.

Bit	Bit Name	Initial Value	R/W	Description
19 to 16	ZTFC[3:0]	1100	R/W	Debug Trace bus Clock (ZTϕ) Frequency Division Ratio 1100: × 1/5 0011: × 1/6 0100: × 1/8 0101: × 1/12 0110: × 1/16 0111: × 1/18 1000: × 1/24 Other values: Setting prohibited Note: ZTϕ is supplied only in debugging mode.
15 to 12	—	0001	R	These bits are always read as 0001. The write value should always be 0001.
11 to 8	—	0011	R	These bits are always read as 0011. The write value should always be 0011.
7 to 4	—	0101	R	These bits are always read as 0101. The write value should always be 0101.
3 to 0	ZTRD2FC[3:0]	0101	R/W	Debug Clock (ZTRD2ϕ) Frequency Division Ratio 0101: × 1/12 0110: × 1/16 0111: × 1/18 1000: × 1/24 Other values: Setting prohibited Note: ZTRϕ is supplied only in debugging mode.

7.2.2 PLL Enable Control Register (PLLECR)

PLLECR is a 32-bit readable register that indicates the state of PLL0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	PLL0ST	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	1	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
10	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
8	PLL0ST	1	R	PLL circuit 0 status Displays PLL circuit 0 status (on or off). 0: PLL circuit 0 is turned off. The main clock is supplied as a clock output. 1: PLL circuit 0 is turned on. The output from PLL circuit 0 is supplied as a clock output.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

7.2.3 PLL0 Control Register (PLL0CR)

PLL0CR is a 32-bit readable/writable register. This register specifies the multiplication ratio of PLL circuit 0. When writing to this register, change only bits STC[6:0] (Read-modify-write).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	STC[6:0]							—	—	—	—	—	—	—	—
Initial value:	0	*1	*1	*1	*1	*1	*1	*1	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 24	STC[6:0]	*1	R/W	PLL Circuit 0 Multiplication Ratio*2 PLL circuit 0 performs multiplication with a ratio of (setting + 1) The realized frequency has the following relationship. (PLL0/VCO) = (PLL0 reference clock) × (setting + 1) × 2 (PLL0 output) = (SYS-CPU divider1 input) = PLL0/VCO × 1/2 = (PLL0 reference clock) × (setting + 1) 0010011: × 40 0010100: × 42 ... 0100111: × 80 (Ex: 20 MHz × 80 = 1600 MHz) ... 0110001: × 100 (Ex: 20 MHz × 100 = 2000 MHz) Set the PLL circuit 0 frequency (PLL0 output frequency) between 475 MHz to 1 GHz.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. Initial value of STC[6:0] is determined by MD14 and MD13 as shown in Table 7.4.
2. Actual multiplication ratio of PLL0 VCO to the reference clock of PLL0 is (setting + 1) × 2. The factor “2” is derived from the fixed divider in the PLL feedback loop. The input clock to the SYS-CPU divider 1 is generated by dividing PLL0 VCO by 2. That is why the input clock frequency to the SYS-CPU divider 1 is expressed as (STC[6:0] + 1) × (reference clock of PLL0).

7.2.4 RGX Control Register (RGXCR)

RGXCR is a 32-bit readable/writable register. This register enables/disables the external logic for SGX Series5.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGXEX
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	SGXEX	0	R/W	Disable external logic for SGX Series5 0: Enable external logic for SGX Series5 1: Disable external logic for SGX Series5
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

7.2.5 SDHI Clock Frequency Control Register (SDCKCR)

SDCKCR is a 32-bit readable/writable register. This register controls SDH clock (SDHϕ), SDHI0 clock (SD0ϕ) and SDHI1 clock (SD1ϕ) frequency. This register should be set before SDHI modules are operated. Do not access SDHI0 and SDHI1 modules during changing the clock frequency of SDHϕ, SD0ϕ, and SD1ϕ or stopping these clocks.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SDHFC[3:0]				SD0FC[3:0]				SD1FC[3:0]			
Initial value:	1	1	1	1	0	0	0	0	0	1	1	0	0	1	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
11 to 8	SDHFC [3:0]	0000	R/W	SDH clock (SDHϕ) Frequency Division Ratio 0000: × 1/2 0001: × 1/3 0010: × 1/4 0011: × 1/6 0100: × 1/8 0101: × 1/12 0110: × 1/16 0111: × 1/18 1000: × 1/24 1010: × 1/36 1011: × 1/48 Other values: Setting prohibited
7 to 4	SD0FC [3:0]	0110	R/W	SDHI0 clock (SD0ϕ) Frequency Division Ratio 1100: × 1/10 0101: × 1/12 0110: × 1/16 0111: × 1/18 1000: × 1/24 1010: × 1/36 1011: × 1/48 Other values: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	SD1FC [3:0]	0110	R/W	SDHI1 clock (SD1ϕ) Frequency Division Ratio 1100: × 1/10 0101: × 1/12 0110: × 1/16 0111: × 1/18 1000: × 1/24 1010: × 1/36 1011: × 1/48 Other values: Setting prohibited

7.2.6 SDHI2 Clock Frequency Control Register (SD2CKCR)

SD2CKCR is a 32-bit readable/writable register. This register controls SDHI2 clock (SD2ϕ) frequency. Do not access SDHI2 module during changing the clock frequency of SD2ϕ or stopping this clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CKSTP	—	—	DIV[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	0	R/W	Clock Stop 0: Supplies SDHI2 clock 1: Stops SDHI2 clock
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	DIV[5:0]	001111	R/W	Division Ratio These bits set the frequency division ratio of SDHI2 clock divider. The clock source is divided by the division ratio of 1/(setting + 1).

7.2.7 RCAN Clock Frequency Control Register (RCANCKCR)

RCANCKCR is a 32-bit readable/writable register. This register controls the RCAN clock.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CKSTP	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CKSTP	1	R/W	Clock Stop 0: Supplies clock to RCAN 1: Stops clock to RCAN
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.

7.3 Operation

7.3.1 Changing Frequency

The clock frequencies controlled by the frequency control registers can be changed either by changing the multiplication ratio of PLL circuits 0 or by changing the division ratio of the dividers. They are controlled by software through the frequency control registers. The methods are described below.

(1) Changing Multiplication Ratio of PLL circuit 0

Changing the multiplication ratio of PLL circuit 0 can be done by modifying the STC[6:0] bits in PLL0CR. The PLL oscillation settling time is internally detected automatically. If the oscillation of PLL circuits is settled, 1 can be read through PLL0ST bit of PLLECR.

(2) Changing Division Ratio

Changing the frequency of ZTϕ, ZTRϕ, and ZTRD2ϕ can be done by modifying each set of bits for setting the division ratio in FRQCRB. After setting new ratio, write 1 to the KICK bit in FRQCRB to start the division ratio change. Before changing the division ratio, the KICK bit must be checked for 0. After 1 is written to the KICK bit in FRQCRB, 0 can be read when the change of new division ratio is completed. While the setting is being changed with the KICK bit being 1, do not modify FRQCRB. When the KICK bit is read as 1, do not write 0 into the KICK bit.

7.4 Usage Notes

7.4.1 Notes on Board Designing

(1) Bypass Capacitor

Insert laminated ceramic capacitors as bypass capacitors for each V_{SS}/V_{CC} pair. Mount the bypass capacitor near the power supply pins of the LSI. Use components with a frequency characteristic suitable for the operating frequency of the LSI, as well as a suitable capacitance value.

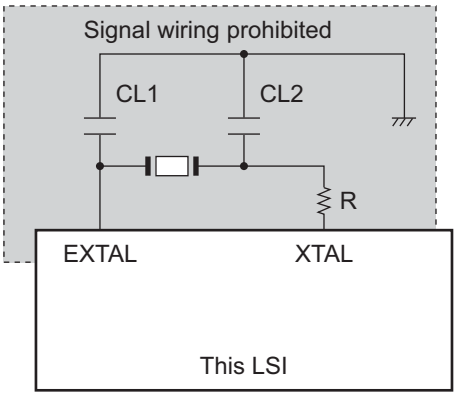
(2) Notes on Using a PLL Oscillation Circuit

Keep the wiring from the PLL V_{DD} and V_{SS} connection pattern to the power supply pins short, and make the pattern width large, to minimize the inductance component.

The analog power supply system of the PLL circuits is sensitive to noise. Therefore system malfunction may occur by the intervention with another power supply. Do not supply the analog power supply with the same resource as the digital power supply of V_{DD} and $V_{CC}Q$.

(3) When Using an External Crystal Resonator

Place the crystal resonator, capacitors CL1 and CL2, and damping resistor R as close to the XTAL, and EXTAL pins as possible. To minimize induction and thus obtain oscillation at the correct frequency, the capacitors to be attached to the resonator must be grounded to the same ground. Do not bring wiring patterns close to these components.



Note: The values for CL1, CL2, and damping resistor R should be determined after consultation with the crystal resonator manufacturer.

Figure 7.2 Note on Using a Crystal Resonator

(4) When Supplying External Clock from EXTAL Pin

Leave the XTAL pin open.

7A. Module Standby and Software Reset

The CPG functions related to module control are explained in this section. Under software control, the CPG is capable of turning the supply of clock signals to individual modules on or off and of resetting individual modules.

7A.1 Overview

7A.1.1 Features

- Module standby
  Clock supply to specified modules is stopped by setting the module stop control register bits.
  Two registers (MSTPSR and SMSTPCR) for one module, and supply of the clock signal to a module is stopped when all two register bits are set to 'stop'.
- Software Reset
  Initialize the specified module by setting the software reset register bit.

7A.1.2 Input/Output Pins

There is no input/output pin related with this function.

7A.1.3 Register Configuration

Table 7A.1 lists of the CPG registers for module standby and software reset. Table 7A.2 lists the register states in response to a reset.

Table 7A.1 Register Configurations

Register Name	Abbreviation	R/W	Address	Access Size
Module stop status register 0	MSTPSR0	R	H'E615 0030	32
Module stop status register 1	MSTPSR1	R	H'E615 0038	32
Module stop status register 2	MSTPSR2	R	H'E615 0040	32
Module stop status register 3	MSTPSR3	R	H'E615 0048	32
Module stop status register 4	MSTPSR4	R	H'E615 004C	32
Module stop status register 5	MSTPSR5	R	H'E615 003C	32
Module stop status register 7	MSTPSR7	R	H'E615 01C4	32
Module stop status register 8	MSTPSR8	R	H'E615 09A0	32
Module stop status register 9	MSTPSR9	R	H'E615 09A4	32
Module stop status register 10	MSTPSR10	R	H'E615 09A8	32
System module stop control register 0	SMSTPCR0*	R/W	H'E615 0130	32
System module stop control register 1	SMSTPCR1*	R/W	H'E615 0134	32
System module stop control register 2	SMSTPCR2*	R/W	H'E615 0138	32
System module stop control register 3	SMSTPCR3*	R/W	H'E615 013C	32
System module stop control register 4	SMSTPCR4*	R/W	H'E615 0140	32
System module stop control register 5	SMSTPCR5*	R/W	H'E615 0144	32
System module stop control register 7	SMSTPCR7*	R/W	H'E615 014C	32
System module stop control register 8	SMSTPCR8*	R/W	H'E615 0990	32
System module stop control register 9	SMSTPCR9*	R/W	H'E615 0994	32

Register Name	Abbreviation	R/W	Address	Access Size
System module stop control register 10	SMSTPCR10*	R/W	H'E615 0998	32
Software reset register 0	SRCR0	R/W	H'E615 00A0	32
Software reset register 1	SRCR1	R/W	H'E615 00A8	32
Software reset register 2	SRCR2	R/W	H'E615 00B0	32
Software reset register 3	SRCR3	R/W	H'E615 00B8	32
Software reset register 4	SRCR4	R/W	H'E615 00BC	32
Software reset register 5	SRCR5	R/W	H'E615 00C4	32
Software reset register 7	SRCR7	R/W	H'E615 01CC	32
Software reset register 8	SRCR8	R/W	H'E615 0920	32
Software reset register 9	SRCR9	R/W	H'E615 0924	32
Software reset register 10	SRCR10	R/W	H'E615 0928	32
Software reset clearing register 0	SRSTCLR0	W	H'E615 0940	32
Software reset clearing register 1	SRSTCLR1	W	H'E615 0944	32
Software reset clearing register 2	SRSTCLR2	W	H'E615 0948	32
Software reset clearing register 3	SRSTCLR3	W	H'E615 094C	32
Software reset clearing register 4	SRSTCLR4	W	H'E615 0950	32
Software reset clearing register 5	SRSTCLR5	W	H'E615 0954	32
Software reset clearing register 7	SRSTCLR7	W	H'E615 095C	32
Software reset clearing register 8	SRSTCLR8	W	H'E615 0960	32
Software reset clearing register 9	SRSTCLR9	W	H'E615 0964	32
Software reset clearing register 10	SRSTCLR10	W	H'E615 0968	32

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

* SMSTPCRn is collectively indicated as MSTPCRn.

Table 7A.2 Register States in Response to a Reset

Register	Power-On Reset
All Registers	Initialized

7A.2 Register Description

Legend for Register Description

Initial value : Register value after a reset

— : Undefined value

R/W : Readable/writable. The written value can be read.

R : Read-only.

W : Write-only. The read value is undefined.

7A.2.1 Module Stop Status Register (MSTPSRn (n = 0 to 5, 7 to 10))

MSTPSRn is a 32-bit readable register that indicates whether the on-chip modules are in the module standby state.

Setting a bit in this register to 1 stops supply of the clock signal to the corresponding module and the setting a bit to 0 enables clock supply to the corresponding module.

Positions, names and initial values of each bit are shown below. The Tables from 7A.3 to 7A.12 show the assignment of modules to bits.

7A.2.1.1 Module Stop Status Register 0 (MSTPSR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP ST000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.3 Assignment of Modules to Bits in MSTPSR0

Bit	Assignment of modules to bits in MSTPSR0
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR0
2	—
1	—
0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.2 Module Stop Status Register 1 (MSTPSR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST131	—	—	MSTP ST128	—	—	—	MSTP ST124	—	MSTP ST122	MSTP ST121	—	MSTP ST119	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST115	—	—	MSTP ST112	MSTP ST111	—	—	—	—	—	—	MSTP ST104	MSTP ST103	—	MSTP ST101	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.4 Assignment of Modules to Bits in MSTPSR1

Bit	Assignment of modules to bits in MSTPSR1
31	VSP1 (SY)
30	—
29	—
28	VSP1DU0
27	—
26	—
25	—
24	CMT0
23	—
22	TMU2
21	TMU3
20	—
19	FDP1-0
18	—
17	—
16	—
15	2D-DMAC
14	—
13	—
12	3DG
11	TMU1
10	—
9	—
8	—
7	—
6	—
5	—
4	STB
3	VPC0

Bit	Assignment of modules to bits in MSTPSR1
2	—
1	VCP0
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.3 Module Stop Status Register 2 (MSTPSR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	MSTPST219	MSTPST218	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MSTPST208	—	—	MSTPST205	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.5 Assignment of Modules to Bits in MSTPSR2

Bit	Assignment of modules to bits in MSTPSR2
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	SYS-DMAC0
18	SYS-DMAC1
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	MSIOF1
7	—
6	—
5	MSIOF2
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR2
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.4 Module Stop Status Register 3 (MSTPSR3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTPST331	MSTPST330	MSTPST329	—	MSTPST327	MSTPST326	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	MSTPST314	MSTPST313	MSTPST312	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.6 Assignment of Modules to Bits in MSTPSR3

Bit	Assignment of modules to bits in MSTPSR3
31	USBHS-DMAC1 ch0
30	USBHS-DMAC0 ch0
29	CMT1
28	—
27	USBHS-DMAC1 ch1
26	USBHS-DMAC0 ch1
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	SDHI0
13	SDHI1
12	SDHI2
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR3
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.5 Module Stop Status Register 4 (MSTPSR4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MSTP ST409	MSTP ST408	MSTP ST407	MSTP ST406	—	—	—	MSTP ST402	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.7 Assignment of Modules to Bits in MSTPSR4

Bit	Assignment of modules to bits in MSTPSR4
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	USB_DDM1
8	INTC-SYS
7	IRQC
6	USB DDM0
5	—
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR4
2	RWDT
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.6 Module Stop Status Register 5 (MSTPSR5)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTP ST530	—	—	—	—	—	—	MSTP ST523	—	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP ST502	—	—
Initial value:	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.8 Assignment of Modules to Bits in MSTPSR5

Bit	Assignment of modules to bits in MSTPSR5
31	—
30	Boot ROM
29	—
28	—
27	—
26	—
25	—
24	—
23	PWM
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR5
2	Audio-DMAC0
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.7 Module Stop Status Register 7 (MSTPSR7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	MSTPST727	MSTPST726	—	MSTPST724	MSTPST723	—	MSTPST721	MSTPST720	MSTPST719	MSTPST718	MSTPST717	MSTPST716
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTPST715	MSTPST714	MSTPST713	—	—	—	—	—	—	MSTPST606	MSTPST605	MSTPST704	MSTPST703	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.9 Assignment of Modules to Bits in MSTPSR7

Bit	Assignment of modules to bits in MSTPSR7
31	—
30	—
29	—
28	—
27	Digital Video Encoder
26	LVDS
25	—
24	DU0
23	DU1
22	—
21	SCIF0
20	SCIF1
19	SCIF2
18	SCIF3
17	HSCIF0
16	HSCIF1
15	SCIF4
14	SCIF5
13	HSCIF2
12	—
11	—
10	—
9	—
8	—
7	—
6	USBHS1
5	USB (EHCI)1
4	USBHS0
3	USB (EHCI)0

Bit	Assignment of modules to bits in MSTPSR7
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.8 Module Stop Status Register 8 (MSTPSR8)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MSTP ST813	MSTP ST812	MSTP ST811	MSTP ST810	—	—	—	—	—	—	—	—	MSTP ST801	MSTP ST800
Initial value:	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.10 Assignment of Modules to Bits in MSTPSR8

Bit	Assignment of modules to bits in MSTPSR8
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	Ether
12	EtherAVB
11	VIN0
10	VIN1
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR8
2	—
1	Digital Video Decoder
0	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.9 Module Stop Status Register 9 (MSTPSR9)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP ST931	MSTP ST930	MSTP ST929	MSTP ST928	MSTP ST927	—	—	—	—	MSTP ST922	—	—	—	MSTP ST918	MSTP ST917	MSTP ST916
Initial value:	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP ST915	—	—	MSTP ST912	MSTP ST911	MSTP ST910	MSTP ST909	MSTP ST908	MSTP ST907	—	—	—	MSTP ST903	—	—	—
Initial value:	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.11 Assignment of Modules to Bits in MSTPSR9

Bit	Assignment of modules to bits in MSTPSR9
31	I2C0
30	I2C1
29	I2C2
28	I2C3
27	I2C4
26	—
25	—
24	—
23	—
22	ADG
21	—
20	—
19	—
18	Quad-SPI0
17	Quad-SPI1
16	CAN0
15	CAN1
14	—
13	—
12	GPIO0
11	GPIO1
10	GPIO2
9	GPIO3
8	GPIO4
7	GPIO5
6	—
5	—
4	—
3	IR Receiver

Bit	Assignment of modules to bits in MSTPSR9
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.1.10 Module Stop Status Register 10 (MSTPSR10)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTPST1030	MSTPST1029	MSTPST1028	MSTPST1027	MSTPST1026	MSTPST1025	—	—	—	MSTPST1021	MSTPST1020	MSTPST1019	MSTPST1018	MSTPST1017	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTPST1015	MSTPST1014	MSTPST1013	MSTPST1012	MSTPST1011	MSTPST1010	MSTPST1009	MSTPST1008	MSTPST1007	MSTPST1006	MSTPST1005	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

0: Supply of the clock signal to the corresponding module is enabled.

1: Supply of the clock signal to the corresponding module is stopped.

Table 7A.12 Assignment of Modules to Bits in MSTPSR10

Bit	Assignment of modules to bits in MSTPSR10
31	—
30	SCU (SRC1)
29	SCU (SRC2)
28	SCU (SRC3)
27	SCU (SRC4)
26	SCU (SRC5)
25	SCU (SRC6)
24	—
23	—
22	—
21	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)
20	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)
19	SCU (DVC0)
18	SCU (DVC1)
17	SCU (all)*1
16	—
15	SSI0
14	SSI1
13	SSI2
12	SSI3
11	SSI4
10	SSI5
9	SSI6
8	SSI7
7	SSI8
6	SSI9
5	SSI (all)*2
4	—
3	—

Bit	Assignment of modules to bits in MSTPSR10
2	—
1	—
0	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. When the MSTP1017 bit is set to 1, supply of the clock signal to the circuits assigned to bits MSTP1030 to MSTP1025, MSTP1021 to MSTP1018 is stopped simultaneously without writing 1 to these bits. When supply of the clock signal to any of the circuits assigned to bits MSTP1030 to MSTP1025, MSTP1021 to MSTP1018 is to be enabled, clear the MSTP1017 bit.
2. When the MSTP1005 bit is set to 1, supply of the clock signal to the SSI0 to SSI9 modules is stopped simultaneously without setting bits MSTP1015 to MSTP1006 to 1. When supply of the clock signal to any of the SSI0 to SSI9 modules is to be enabled, clear the MSTP1005 bit.

7A.2.2 Module Stop Control Register (SMSTPCRn (n = 0 to 5, 7 to 10))

SMSTPCRn is 32-bit readable/writable register which control supply of the clock signal to the modules assigned to the corresponding bits. SMSTPCRn register is for the AP system CPU core. When the control bit in SMSTPCRn is set to 1 (halt), input of the clock signal to the module is halted (the module is on standby). When a corresponding control bit in SMSTPCRn is 0, the clock signal is supplied. Whether the module is stopped or not can be checked through a corresponding bit in MSTPSRn register.

Setting a bit in this register to 1 requests that the module be placed on standby and setting a bit to 0 requests that the module operate.

The reserved bits should be set to the values read from the bits. Positions, names and initial values of each bit are shown below. The Tables from 7A.13 to 7A.22 show the assignment of modules to bits.

7A.2.2.1 System Module Stop Control Register 0 (SMSTPCR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.13 Assignment of Modules to Bits in SMSTPCR0

Bit	Assignment of modules to bits in SMSTPCR0
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR0
2	—
1	—
0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.2 System Module Stop Control Register 1 (SMSTPCR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP131	—	—	MSTP128	—	—	—	MSTP124	—	MSTP122	MSTP121	—	MSTP119	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP115	—	—	MSTP112	MSTP111	—	—	—	—	MSTP106	—	MSTP104	MSTP103	—	MSTP101	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R	R	R/W	R/W	R	R	R/W	R	R/W	R	R/W	R/W	R	R/W	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.14 Assignment of Modules to Bits in SMSTPCR1

Bit	Assignment of modules to bits in SMSTPCR1
31	VSP1 (SY)
30	—
29	—
28	VSP1DU0
27	—
26	—
25	—
24	CMT0
23	—
22	TMU2
21	TMU3
20	—
19	FDP1-0
18	—
17	—
16	—
15	2D-DMAC
14	—
13	—
12	3DG
11	TMU1
10	—
9	—
8	—
7	—
6	ADG (M2ϕ)*
5	—
4	STB
3	VPC0

Bit	Assignment of modules to bits in SMSTPCR1
2	—
1	VCP0
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.
* This bit indicates the state of the clock signal (M2ϕ) for the ADG.

7A.2.2.3 System Module Stop Control Register 2 (SMSTPCR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	MSTP 219	MSTP 218	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MSTP 208	—	—	MSTP 205	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R/W	R	R	R/W	R	R	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.15 Assignment of Modules to Bits in SMSTPCR2

Bit	Assignment of modules to bits in SMSTPCR2
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	SYS-DMAC0
18	SYS-DMAC1
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	MSIOF1
7	—
6	—
5	MSIOF2
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR2
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.4 System Module Stop Control Register 3 (SMSTPCR3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP331	MSTP330	MSTP329	—	MSTP327	MSTP326	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	MSTP314	MSTP313	MSTP312	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.16 Assignment of Modules to Bits in SMSTPCR3

Bit	Assignment of modules to bits in SMSTPCR3
31	USBHS-DMAC1 ch0
30	USBHS-DMAC0 ch0
29	CMT1
28	—
27	USBHS-DMAC1 ch1
26	USBHS-DMAC0 ch1
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	SDHI0
13	SDHI1
12	SDHI2
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR3
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.5 System Module Stop Control Register 4 (SMSTPCR4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MSTP 409	MSTP 408	MSTP 407	MSTP 406	—	—	—	MSTP 402	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.17 Assignment of Modules to Bits in SMSTPCR4

Bit	Assignment of modules to bits in SMSTPCR4
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	USB_DDM1
8	INTC-SYS
7	IRQC
6	USB DDM0
5	—
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR4
2	RWDT
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.6 System Module Stop Control Register 5 (SMSTPCR5)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTP530	—	—	—	—	—	—	MSTP523	—	—	—	—	—	—	—
Initial value:	1	0	0	0	0	0	1	1	1	1	1	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	MSTP502	—	—
Initial value:	1	0	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.18 Assignment of Modules to Bits in SMSTPCR5

Bit	Assignment of modules to bits in SMSTPCR5
31	—
30	Boot ROM
29	—
28	—
27	—
26	—
25	—
24	—
23	PWM
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR5
2	Audio-DMAC0
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.7 System Module Stop Control Register 7 (SMSTPCR7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	MSTP 727	MSTP 726	—	MSTP 724	MSTP 723	—	MSTP 721	MSTP 720	MSTP 719	MSTP 718	MSTP 717	MSTP 716
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R/W	R	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 715	MSTP 714	MSTP 713	—	—	—	—	—	—	MSTP 706	MSTP 705	MSTP 704	MSTP 703	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	0	1	1	1	1	1
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.19 Assignment of Modules to Bits in SMSTPCR7

Bit	Assignment of modules to bits in SMSTPCR7
31	—
30	—
29	—
28	—
27	Digital Video Encoder
26	LVDS
25	—
24	DU0
23	DU1
22	—
21	SCIF0
20	SCIF1
19	SCIF2
18	SCIF3
17	HSCIF0
16	HSCIF1
15	SCIF4
14	SCIF5
13	HSCIF2
12	—
11	—
10	—
9	—
8	—
7	—
6	USBHS1
5	USB (EHCI)1
4	USBHS0
3	USB (EHCI)0

Bit	Assignment of modules to bits in SMSTPCR7
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.8 System Module Stop Control Register 8 (SMSTPCR8)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MSTP813	MSTP812	MSTP811	MSTP810	—	—	—	—	—	—	—	—	MSTP801	MSTP800
Initial value:	1	1	1	1	1	1	1	1	1	0	0	0	0	1	1	0
R/W:	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.20 Assignment of Modules to Bits in SMSTPCR8

Bit	Assignment of modules to bits in SMSTPCR8
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	Ether
12	EtherAVB
11	VIN0
10	VIN1
9	—
8	—
7	—
6	—
5	—
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR8
2	—
1	Digital Video Decoder
0	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.9 System Module Stop Control Register 9 (SMSTPCR9)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MSTP931	MSTP930	MSTP929	MSTP928	MSTP927	—	—	—	—	MSTP922	—	—	—	MSTP918	MSTP917	MSTP916
Initial value:	0	0	0	0	0	0	0	1	1	1	0	1	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP915	—	—	MSTP912	MSTP911	MSTP910	MSTP909	MSTP908	MSTP907	—	—	—	MSTP903	—	—	—
Initial value:	1	1	1	0	0	0	0	0	0	1	0	0	0	1	1	1
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.21 Assignment of Modules to Bits in SMSTPCR9

Bit	Assignment of modules to bits in SMSTPCR9
31	I2C0
30	I2C1
29	I2C2
28	I2C3
27	I2C4
26	—
25	—
24	—
23	—
22	ADG
21	—
20	—
19	—
18	Quad-SPI0
17	Quad-SPI1
16	CAN0
15	CAN1
14	—
13	—
12	GPIO0
11	GPIO1
10	GPIO2
9	GPIO3
8	GPIO4
7	GPIO5
6	—
5	—
4	—
3	IR Receiver

Bit	Assignment of modules to bits in SMSTPCR9
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.2.10 System Module Stop Control Register 10 (SMSTPCR10)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MSTP 1030	MSTP 1029	MSTP 1028	MSTP 1027	MSTP 1026	MSTP 1025	—	—	—	MSTP 1021	MSTP 1020	MSTP 1019	MSTP 1018	MSTP 1017	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSTP 1015	MSTP 1014	MSTP 1013	MSTP 1012	MSTP 1011	MSTP 1010	MSTP 1009	MSTP 1008	MSTP 1007	MSTP 1006	MSTP 1005	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

0: Enables supply of the clock signal to the corresponding module.

1: Stops supply of the clock signal to the corresponding module.

Table 7A.22 Assignment of Modules to Bits in SMSTPCR10

Bit	Assignment of modules to bits in SMSTPCR10
31	—
30	SCU (SRC1)
29	SCU (SRC2)
28	SCU (SRC3)
27	SCU (SRC4)
26	SCU (SRC5)
25	SCU (SRC6)
24	—
23	—
22	—
21	SCU (CTU00, CTU01, CTU02, CTU03, MIX0)
20	SCU (CTU10, CTU11, CTU12, CTU13, MIX1)
19	SCU (DVC0)
18	SCU (DVC1)
17	SCU (all)*1
16	—
15	SSI0
14	SSI1
13	SSI2
12	SSI3
11	SSI4
10	SSI5
9	SSI6
8	SSI7
7	SSI8
6	SSI9
5	SSI (all)*2
4	—
3	—

Bit	Assignment of modules to bits in SMSTPCR10
2	—
1	—
0	—

Notes: "—" indicates the bit is reserved. Set the value read from the bit.

1. When the MSTP1017 bit is set to 1, supply of the clock signal to the circuits assigned to bits MSTP1030 to MSTP1025, MSTP1021 to MSTP1018 is stopped simultaneously without writing 1 to these bits. When supply of the clock signal to any of the circuits assigned to bits MSTP1030 to MSTP1025, MSTP1021 to MSTP1018 is to be enabled, clear the MSTP1017 bit.
2. When the MSTP1005 bit is set to 1, supply of the clock signal to the SSI0 to SSI9 modules is stopped simultaneously without setting bits MSTP1015 to MSTP1006 to 1. When supply of the clock signal to any of the SSI0 to SSI9 modules is to be enabled, clear the MSTP1005 bit.

7A.2.3 Software Reset Register (SRCRn (n = 0 to 5, 7 to 10))

Each SRCRn is a 32-bit readable/writable register. Each effective bit is assigned to a module in the chip. Writing 1 to a given bit resets the corresponding module. Writing 1 to a given bit of the software reset clearing register (SRSTCLRn (n = 0 to 11)) clears the corresponding bit of SRCRn and releases the module from the reset state. SRCRn is written in a read-modify-write sequence but writing to SRSTCLRn can proceed by simply setting the target bits to 1. After writing 1 to a software reset bit in SRCRn, ensure that the module has actually been initialized by waiting for at least one cycle of the RCLK clock before writing 1 to the corresponding bit of SRSTCLRn to release the module from the reset state. Before applying a software reset to a module connected to the AXI, make sure that any data transfer to the module is complete.

Positions, names and initial values of each bit are shown below. The Tables from 7A.23 to 7A.32 show the assignment of modules to bits.

7A.2.3.1 Software Reset Register 0 (SRCR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRT 000
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Table 7A.23 Assignment of Modules to Bits in SRCR0

Bit	Assignment of modules to bits in SRCR0
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—
2	—
1	—

Bit	Assignment of modules to bits in SRCR0
0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.2 Software Reset Register 1 (SRCR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 131	—	—	SRT 128	—	—	—	SRT 124	—	SRT 122	SRT 121	—	SRT 119	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 115	—	—	SRT 112	SRT 111	—	—	—	—	—	—	SRT 104	SRT 103	—	SRT 101	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R	R/W	R

Table 7A.24 Assignment of Modules to Bits in SRCR1

Bit	Assignment of modules to bits in SRCR1
31	VSP1 (SY)
30	—
29	—
28	VSP1DU0
27	—
26	—
25	—
24	CMT0
23	—
22	TMU2
21	TMU3
20	—
19	FDP1-0
18	—
17	—
16	—
15	2D-DMAC
14	—
13	—
12	3DG
11	TMU1
10	—
9	—
8	—
7	—
6	—
5	—
4	STB
3	VPC0
2	—
1	VCP0

Bit	Assignment of modules to bits in SRCR1
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.3 Software Reset Register 2 (SRCR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	SRT 219	SRT 218	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SRT 208	—	—	SRT 205	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R	R	R	R	R

Table 7A.25 Assignment of Modules to Bits in SRCR2

Bit	Assignment of modules to bits in SRCR2
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	SYS-DMAC0
18	SYS-DMAC1
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	MSIOF1
7	—
6	—
5	MSIOF2
4	—
3	—
2	—
1	—

Bit	Assignment of modules to bits in SRCR2
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.4 Software Reset Register 3 (SRCR3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT 331	SRT 330	SRT 329	—	SRT 327	SRT 326	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SRT 314	SRT 313	SRT 312	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Table 7A.26 Assignment of Modules to Bits in SRCR3

Bit	Assignment of modules to bits in SRCR3
31	USBHS-DMAC1 ch0
30	USBHS-DMAC0 ch0
29	CMT1
28	—
27	USBHS-DMAC1 ch1
26	USBHS-DMAC0 ch1
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	SDHI0
13	SDHI1
12	SDHI2
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—
2	—
1	—

Bit	Assignment of modules to bits in SRCR3
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.5 Software Reset Register 4 (SRCR4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SRT 409	SRT 408	SRT 407	SRT 406	—	—	—	SRT 402	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R

Table 7A.27 Assignment of Modules to Bits in SRCR4

Bit	Assignment of modules to bits in SRCR4
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	USB_DDM1
8	INTC-SYS
7	IRQC
6	USB DDM0
5	—
4	—
3	—
2	RWDT
1	—

Bit	Assignment of modules to bits in SRCR4
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.6 Software Reset Register 5 (SRCR5)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SRT 523	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SRT 508	—	—	—	—	—	SRT 502	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R	R

Table 7A.28 Assignment of Modules to Bits in SRCR5

Bit	Assignment of modules to bits in SRCR5
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	PWM
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	SCU
7	—
6	—
5	—
4	—
3	—
2	Audio-DMAC0
1	—

Bit	Assignment of modules to bits in SRCR5
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.7 Software Reset Register 7 (SRCR7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SRT 727	SRT 726	—	SRT 724	—	—	SRT 721	SRT 720	SRT 719	SRT 718	SRT 717	SRT 716
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R/W	R/W	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 715	SRT 714	SRT 713	—	—	—	—	—	—	SRT 706	SRT 705	SRT 704	SRT 703	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R

Table 7A.29 Assignment of Modules to Bits in SRCR7

Bit	Assignment of modules to bits in SRCR7
31	—
30	—
29	—
28	—
27	Digital Video Encoder
26	LVDS
25	—
24	DU0, DU1
23	—
22	—
21	SCIF0
20	SCIF1
19	SCIF2
18	SCIF3
17	HSCIF0
16	HSCIF1
15	SCIF4
14	SCIF5
13	HSCIF2
12	—
11	—
10	—
9	—
8	—
7	—
6	USBHS1
5	USB (EHCI)1
4	USBHS0
3	USB (EHCI)0
2	—
1	—

Bit	Assignment of modules to bits in SRCR7
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.8 Software Reset Register 8 (SRCR8)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SRT 813	SRT 812	SRT 811	SRT 810	—	—	—	—	—	—	—	—	SRT 801	SRT 800
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W

Table 7A.30 Assignment of Modules to Bits in SRCR8

Bit	Assignment of modules to bits in SRCR8
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	Ether
12	EtherAVB
11	VIN0
10	VIN1
9	—
8	—
7	—
6	—
5	—
4	—
3	—
2	—
1	Digital Video Decoder

Bit	Assignment of modules to bits in SRCR8
0	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.9 Software Reset Register 9 (SRCR9)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRT931	SRT930	SRT929	SRT928	SRT927	—	—	—	—	SRT922	—	—	—	SRT918	SRT917	SRT916
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT915	—	—	SRT912	SRT911	SRT910	SRT909	SRT908	SRT907	—	—	—	SRT903	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R

Table 7A.31 Assignment of Modules to Bits in SRCR9

Bit	Assignment of modules to bits in SRCR9
31	I2C0
30	I2C1
29	I2C2
28	I2C3
27	I2C4
26	—
25	—
24	—
23	—
22	ADG
21	—
20	—
19	—
18	Quad-SPI0
17	Quad-SPI1
16	CAN0
15	CAN1
14	—
13	—
12	GPIO0
11	GPIO1
10	GPIO2
9	GPIO3
8	GPIO4
7	GPIO5
6	—
5	—
4	—
3	IR Receiver
2	—
1	—

Bit	Assignment of modules to bits in SRCR9
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.3.10 Software Reset Register 10 (SRCR10)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRT 1015	SRT 1014	SRT 1013	SRT 1012	SRT 1011	SRT 1010	SRT 1009	SRT 1008	SRT 1007	SRT 1006	SRT 1005	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

Table 7A.32 Assignment of Modules to Bits in SRCR10

Bit	Assignment of modules to bits in SRCR10
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	SSI0
14	SSI1
13	SSI2
12	SSI3
11	SSI4
10	SSI5
9	SSI6
8	SSI7
7	SSI8
6	SSI9
5	SSI (all)
4	—
3	—
2	—
1	—

Bit	Assignment of modules to bits in SRCR10
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7A.2.4 Software Reset Clearing Register n (SRSTCLRn (n = 0 to 5, 7 to 10))

Each SRSTCLRn is a 32-bit write only register. Each effective bit is assigned to a module in this chip. Writing 1 to a given bit clears the corresponding bit of SRCRn and releases the corresponding module from the reset state in which it was placed by writing 1 to the bit of SRCRn. Write 0 to the reserved bits of these registers.

Positions, names and initial values of each bit are shown below. The Tables from 7A.33 to 7A.42 show the assignment of modules to bits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRTCL Rn31	SRTCL Rn30	SRTCL Rn29	SRTCL Rn28	SRTCL Rn27	SRTCL Rn26	SRTCL Rn25	SRTCL Rn24	SRTCL Rn23	SRTCL Rn22	SRTCL Rn21	SRTCL Rn20	SRTCL Rn19	SRTCL Rn18	SRTCL Rn17	SRTCL Rn16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRTCL Rn15	SRTCL Rn14	SRTCL Rn13	SRTCL Rn12	SRTCL Rn11	SRTCL Rn10	SRTCL Rn09	SRTCL Rn08	SRTCL Rn07	SRTCL Rn06	SRTCL Rn05	SRTCL Rn04	SRTCL Rn03	SRTCL Rn02	SRTCL Rn01	SRTCL Rn00
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Table 7A.33 Assignment of Modules to Bits in SRSTCLR0

Bit	Assignment of modules to bits in SRSTCLR0
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	—
7	—
6	—

Bit	Assignment of modules to bits in SRSTCLR0
5	—
4	—
3	—
2	—
1	—
0	MSIOF0

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.34 Assignment of Modules to Bits in SRSTCLR1

Bit	Assignment of modules to bits in SRSTCLR1
31	VSP1 (SY)
30	—
29	—
28	VSP1DU0
27	—
26	—
25	—
24	CMT0
23	—
22	TMU2
21	TMU3
20	—
19	FDP1-0
18	—
17	—
16	—
15	2D-DMAC
14	—
13	—
12	3DG
11	TMU1
10	—
9	—
8	—
7	—
6	—
5	—
4	STB
3	VPC0
2	—
1	VCP0
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.35 Assignment of Modules to Bits in SRSTCLR2

Bit	Assignment of modules to bits in SRSTCLR2
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	SYS-DMAC0
18	SYS-DMAC1
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	MSIOF1
7	—
6	—
5	MSIOF2
4	—
3	—
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.36 Assignment of Modules to Bits in SRSTCLR3

Bit	Assignment of modules to bits in SRSTCLR3
31	USBHS-DMAC1 ch0
30	USBHS-DMAC0 ch0
29	CMT1
28	—
27	USBHS-DMAC1 ch1
26	USBHS-DMAC0 ch1
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	SDHI0
13	SDHI1
12	SDHI2
11	—
10	—
9	—
8	—
7	—
6	—
5	—
4	—
3	—
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.37 Assignment of Modules to Bits in SRSTCLR4

Bit	Assignment of modules to bits in SRSTCLR4
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	USB_DDM1
8	INTC-SYS
7	IRQC
6	USB DDM0
5	—
4	—
3	—
2	RWDT
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.38 Assignment of Modules to Bits in SRSTCLR5

Bit	Assignment of modules to bits in SRSTCLR5
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	PWM
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	—
12	—
11	—
10	—
9	—
8	SCU
7	—
6	—
5	—
4	—
3	—
2	Audio-DMAC0
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.39 Assignment of Modules to Bits in SRSTCLR7

Bit	Assignment of modules to bits in SRSTCLR7
31	—
30	—
29	—
28	—
27	Digital Video Encoder
26	LVDS
25	—
24	DU0, DU1
23	—
22	—
21	SCIF0
20	SCIF1
19	SCIF2
18	SCIF3
17	HSCIF0
16	HSCIF1
15	SCIF4
14	SCIF5
13	HSCIF2
12	—
11	—
10	—
9	—
8	—
7	—
6	USBHS1
5	USB (EHCI)1
4	USBHS0
3	USB (EHCI)0
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.40 Assignment of Modules to Bits in SRSTCLR8

Bit	Assignment of modules to bits in SRSTCLR8
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	—
14	—
13	Ether
12	EtherAVB
11	VIN0
10	VIN1
9	—
8	—
7	—
6	—
5	—
4	—
3	—
2	—
1	Digital Video Decoder
0	IPMMU-SGX

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.41 Assignment of Modules to Bits in SRSTCLR9

Bit	Assignment of modules to bits in SRSTCLR9
31	I2C0
30	I2C1
29	I2C2
28	I2C3
27	I2C4
26	—
25	—
24	—
23	—
22	ADG
21	—
20	—
19	—
18	Quad-SPI0
17	Quad-SPI1
16	CAN0
15	CAN1
14	—
13	—
12	GPIO0
11	GPIO1
10	GPIO2
9	GPIO3
8	GPIO4
7	GPIO5
6	—
5	—
4	—
3	IR Receiver
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

Table 7A.42 Assignment of Modules to Bits in SRSTCLR10

Bit	Assignment of modules to bits in SRSTCLR10
31	—
30	—
29	—
28	—
27	—
26	—
25	—
24	—
23	—
22	—
21	—
20	—
19	—
18	—
17	—
16	—
15	SSI0
14	SSI1
13	SSI2
12	SSI3
11	SSI4
10	SSI5
9	SSI6
8	SSI7
7	SSI8
6	SSI9
5	SSI (all)
4	—
3	—
2	—
1	—
0	—

Note: "—" indicates the bit is reserved. Set the value read from the bit.

7B. Advanced Power Management Unit for AP-System Core (APMU)

7B.1 Overview

7B.1.1 Features

The AP-system core power management unit (APMU) is a module to control power supply and clock supply to the AP-system core.

This module includes the following function:

- Controls power supply to each CPU core and L2 cache area.

The APMU includes the following submodule:

- Power supply control unit (PCCU) which controls the power supply to each CPU core and L2 cache area.

7B.1.2 Input/Output Pins

There is no input/output pin related with this function.

7B.1.3 Register Configuration

Table 7B.1 lists the registers of the APMU. All registers listed in this table are cleared by the reset.

Table 7B.1 Register Configurations

Register Name	Abbreviation	R/W	Address	Access Size
Cortex-A7 CPU wake up control register	CA7WUPCR	R/W	H'E615 1010/H'E615 4010*1	32
Cortex-A7 power status register	CA7PSTR	R	H'E615 1040/H'E615 4040*1	32
Cortex-A7 CPU0 power status control register	CA7CPU0CR	R/W	H'E615 1100/H'E615 4100*1	32
Cortex-A7 CPU1 power status control register	CA7CPU1CR	R/W	H'E615 1110/H'E615 4110*1	32
Cortex-A7 debug resource reset control register	CA7DBGRCR	R/W	H'E615 1180	32
Cortex-A7 common power control register	CA7CPUCMCR	R/W	H'E615 1184/H'E615 4184*1	32

Notes: The register address maps both “H'E615 1xxx” and “H'E615 4xxx” are accessible by Cortex-A7.
1. Cortex-A7 access to this address is access to this register.

7B.2 Register Description

Legend for Register Description

Initial value : Register value after a reset

— : Undefined value

R/W : Readable/writable. The written value can be read.

R : Read-only.

W : Write-only. The read value is undefined.

7B.2.1 Cortex-A7 CPU*n* Power Status Control Register (CA7CPU*n*CR (*n* = 0 to 1))

Cortex-A7 CPU*n* power status control registers are 32-bit readable/writable registers of PCCU. These registers define the operation of related CPU when the CPU*n* core issues WFI instruction. Please write to these registers while the power of related CPU is ON.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPUPWR	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CPUPWR	00	R/W	CPU*n* PWR Bit Defines the power supply of corresponding CPU*n* when the CPU*n* issues WFI instruction. 00: Sleep mode 11: CoreStandby mode (power-cut of CPU core, L1$) Other than above: Setting prohibited These bits are automatically cleared to 00 when the PCCU completes CoreStandby instruction after 11 is written to these bits.

7B.2.2 Cortex-A7 Common Power Control Register (CA7CPUCMCR)

Cortex-A7 common power control registers are 32-bit readable/writable registers. These registers define power supply control of CPU peripheral (SCU and L2 cache controller) of AP-system core (Cortex-A7). The CMPWR bits of this register define the operation when all CPU cores are in the CoreStandby state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	L2RST	—	—	CMPWR	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	L2RST	0	R/W	CPU L2 Reset Control Bit Defines the power supply when all of the CPUs in the cluster are in CoreStandby mode (power-off). 0: Normal mode 1: L2 dormant mode
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CMPWR	00	R/W	CPU Common Power Control Bit Defines the power supply when all of the CPUs in the cluster are in CoreStandby mode (power-off). 00: Normal mode, CPU peripheral (SCU and L2 cache controller) ON 01: Setting prohibited 10: L2 dormant mode, CPU peripheral (SCU and L2 cache controller) OFF 11: Setting prohibited

7B.2.3 Cortex-A7 CPU Wake Up Control Register (CA7WUPCR)

Cortex-A7 CPU wake up control registers are 32-bit readable/writable registers of PCCU. These registers request power on of each CPU core. Writing 1 to the CPU*n*WUP bit wakes up the corresponding CPU*n*, and the CPU*n* starts operation from the reset vector. Each bit is automatically cleared to 0 after the wake up procedure is finished.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU1 WUP	CPU0 WUP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CPU1WUP	0	R/W	CPU1 Wake Up Bit Write access: 0: Ignores. 1: Requests wake up of CPU1 (CPU1 power on). Read access: 0: CPU1 wakeup sequence is completed. 1: CPU1 wakeup sequence is in progress.
0	CPU0WUP	0	R/W	CPU0 Wake Up Bit Write access: 0: Ignores. 1: Requests wake up of CPU0 (CPU0 power on). Read access: 0: CPU0 wakeup sequence is completed. 1: CPU0 wakeup sequence is in progress.

7B.2.4 Cortex-A7 Power Status Register (CA7PSTR)

Cortex-A7 power status registers are 32-bit readable registers of PCCU. These registers show power status of AP-system CPU cores.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	—	0	0	0	—	0	0	0	—	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CPU1ST[1:0]		—	—	CPU0ST[1:0]	
Initial value:	0	0	1	1	0	0	1	1	0	0	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: — stands for unknown value.

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0.
28	—	Undefined	R	Reserved This bit is always read as unknown value.
27 to 25	—	All 0	R	Reserved These bits are always read as 0.
24	—	Undefined	R	Reserved This bit is always read as unknown value.
23 to 21	—	All 0	R	Reserved These bits are always read as 0.
20	—	Undefined	R	Reserved This bit is always read as unknown value.
19 to 17	—	All 0	R	Reserved These bits are always read as 0.
16	—	Undefined	R	Reserved This bit is always read as unknown value.
15, 14	—	All 0	R	Reserved These bits are always read as 0.
13, 12	—	11	R	Reserved These bits are always read as 11.
11, 10	—	All 0	R	Reserved These bits are always read as 0.
9, 8	—	11	R	Reserved These bits are always read as 11.
7, 6	—	All 0	R	Reserved These bits are always read as 0.
5, 4	CPU1ST [1:0]	11	R	CPU1 Status Bit Displays CPU1 status. 00: Run mode 11: CoreStandby mode Other than above: Invalid

Bit	Bit Name	Initial Value	R/W	Description
3, 2	—	All 0	R	Reserved These bits are always read as 0.
1, 0	CPU0ST [1:0]	00	R	CPU0 Status Bit Displays CPU0 status. 00: Run mode 11: CoreStandby mode Other than above: Invalid

7B.2.5 Cortex-A7 Debug Resource Reset Control Register (CA7DBGRCR)

Cortex-A7 debug resource reset control registers are 32-bit readable/writable registers of PCCU. These registers enable the reset requests derived from power-shutoff to the AP-system CPU cores in the debug mode. When you write to these registers, please modify only the target bits you want to change (read-modify-write). In the debug mode, bits 24 to 19 must be set to all 1 before the AP-system cores first resume from power-shutoff. In the normal mode (i.e. not debug mode), writing all 1 to bits 24 to 19 doesn't disturb normal operation. Therefore the same code to write these registers can be applied for both debug mode and normal mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	DBGCPUREN	—	—	DBGCPU1REN	DBGCPU0REN	DBGCPUPREN	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	0	—	—	0	0	—	—	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	DBGCPUREN	0	R/W	Enable the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode. 0: Disables the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode. 1: Enables the reset request derived from power-shutoff to the circuits other than CPU cores in the debug mode.
23	—	0	R/W	Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1C. Therefore the write value can be either 0 or 1.
22	—	0	R/W	Reserved The initial value of this bit is 0. The value of this bit doesn't affect the operation of RZ/G1C. Therefore the write value can be either 0 or 1.
21	DBGCPU1REN	0	R/W	Enable the reset request derived from power-shutoff to CPU1 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU1 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU1 in the debug mode.
20	DBGCPU0REN	0	R/W	Enable the reset request derived from power-shutoff to CPU0 in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU0 in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU0 in the debug mode.

Bit	Bit Name	Initial Value	R/W	Description
19	DBGCPUPREN	0	R/W	Enable the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode. 0: Disables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode. 1: Enables the reset request derived from power-shutoff to CPU Peripheral (SCU and L2 cache controller) in the debug mode.
18	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
17, 16	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	—	Undefined	R	Reserved These bits are always read as unknown values. The write value should always be the same as read values (read-modify-write).

7B.3 Operation

7B.3.1 PCCU Function

(1) Power Control

The PCCU manages the CPU power supply when the CPU issues WFI instruction, and recovers from the low power state. Table 7B.2 shows power status of CPU.

Table 7B.2 CPU Power Mode

Power Mode	CPU#*n* Clock	CPU#*n* Power	CPU Peripheral (SCU and L2 Cache Controller) Power
Run mode	ON	ON	ON
Sleep mode	OFF	ON	ON
CoreStandby mode	OFF	ON	ON
L2 shutdown mode	OFF	ON	ON

The following is method to enter each mode.

Sleep mode

Issue WFI instruction when the CPUPWR bits of CA7CPUnCR are B'00.

CoreStandby mode

Issue WFI instruction with the CPUPWR bits of CA7CPUnCR are B'11.

The CPUPWR bits of CA7CPUnCR are automatically cleared to B'00 when the PCCU completes CoreStandby operation. So the interrupt to CPUn is masked while CPUPWR bits of CA7CPUnCR are B'11. In the case of cancel, it is cancelled by setting B'00 to the CPUPWR bits of CA7CPUnCR.

L2 shutdown mode

Issue WFI instruction when all of the conditions below are met:

Other CPU cores in the same CPU cluster are in the CoreStandby mode.

The CMPWR bits of CA7CPUCMCR are B'10.

The L2RST bit of CA7CPUCMCR is B'0.

The CPUPWR bits of CA7CPUnCR are B'11

Run mode

Interrupt and reset of CPU recovers each CPU to the RUN mode.

8. Reset (RST)

8.1 Overview

The reset (RST) consists of the bus interface block and registers related to reset control. Timing of the bus interface block is based on CPϕ.

8.1.1 Features

The following functions are implemented by RST.

- Register-based reset control for the Cortex-A7
- Latching of the levels on mode pins when PRESET# is negated
- Mode monitoring register
- Boot address registers for the Cortex-A7

8.1.2 Features of WDT reset

- WDT resets can be issued by the RWDT module.
- WDTRSTCR controls the permission or prohibition of WDT resets.
- The reset (RST) module is not initialized by a WDT reset.

8.1.3 Block Diagram

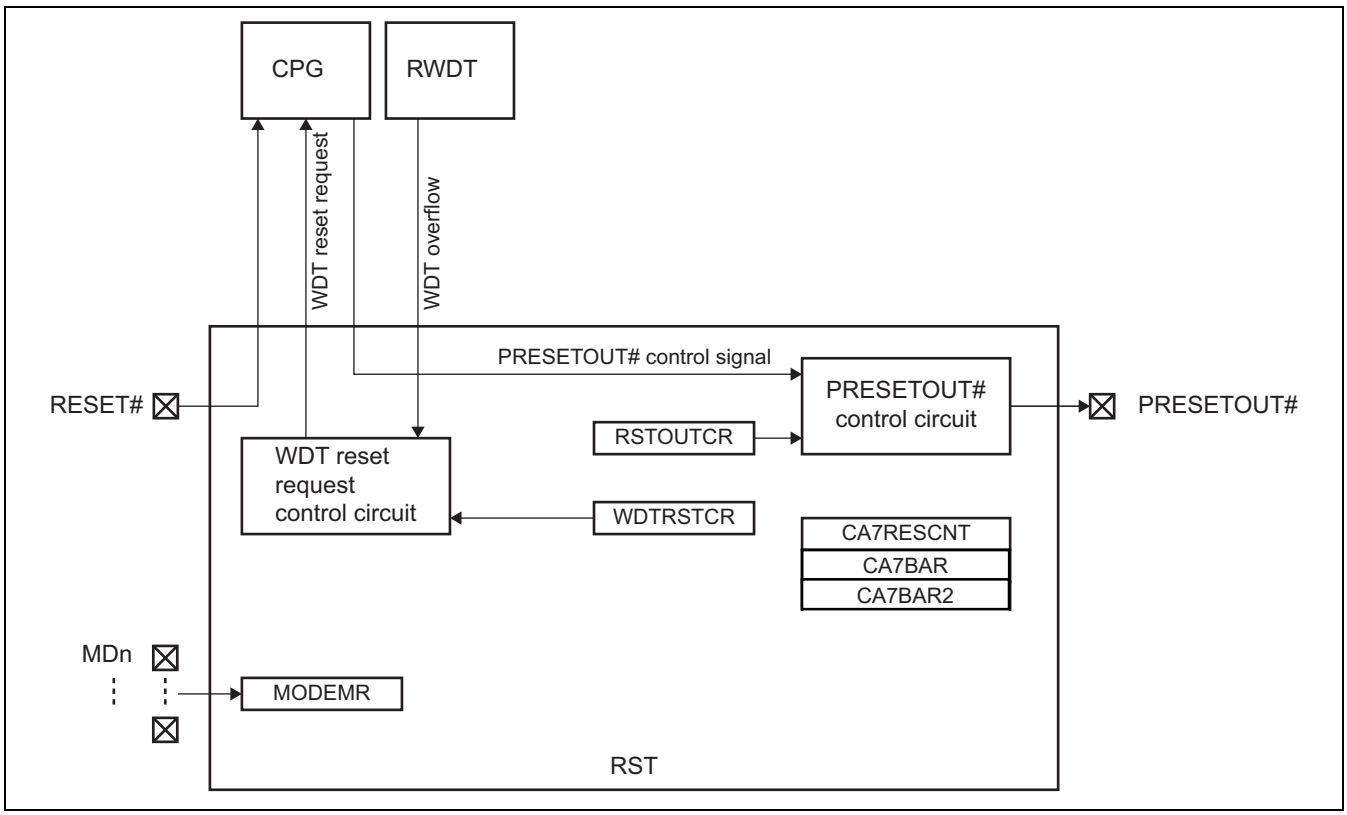


Figure 8.1 Block Diagram of RST

8.1.4 Input/Output Pins

The following table lists the pins connected to the RST.

Table 8.1 External Pins for RST

Pin Name	Function	Direction	Remarks
MD0 to MD11	Mode pins	IN	Mode pins
MD13 to MD14	Mode pins	IN	Mode pins
MD20 to MD21	Mode pins	IN	Mode pins
MDT0 to MDT1	Mode pins	IN	Mode pins
PRESET#	Power-on-reset	IN	Power-on-reset The low-level input on this pin places the LSI in the power-on-reset state.
PRESETOUT#	Indicates internal reset	OUT	Reset output

8.1.5 Register Configuration

Table 8.2 RST Register Details

Register Name	Mnemonic	R/W	Address	Access Size	Access Permission
Mode monitoring register	MODEMR	R	H'E616 0060	32	All
Cortex-A7 reset control register	CA7RESCNT	R/W	H'E616 0044	32	All
Watchdog timer reset control register	WDTRSTCR	R/W	H'E616 0054	32	All
PRESETOUT control register	RSTOUTCR	R/W	H'E616 0058	32	All
SYS boot address register	SBAR	R/W	H'E616 0010	32	Cortex-A7
SYS boot address register 2	SBAR2	R/W	H'E616 0014	32	Cortex-A7
Cortex-A7 boot address register	CA7BAR	R/W	H'E616 0030	32	All
Cortex-A7 boot address register 2	CA7BAR2	R/W	H'E616 0034	32	All

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

Table 8.3 State of the Registers on Reset

Mnemonic	Power-On Reset
MODEMR	Initialized*
CA7RESCNT	Initialized*
WDTRSTCR	Initialized*
RSTOUTCR	Initialized*
SBAR	Initialized*
SBAR2	Initialized*
CA7BAR	Initialized*
CA7BAR2	Initialized*

Note: * Initialized only on power-on reset caused by PRESET#.

8.2 Register Description

Legend for Register Description

Initial value : Register value after a reset

— : Undefined value

R/W : Readable/writable. The written value can be read.

R : Read-only.

W : Write-only. The read value is undefined.

8.2.1 Mode Monitoring Register (MODEMR)

MODEMR is a 32-bit read-only register, which can be accessed only in longwords.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	MDT1	MDT0	—	—	—	—	—	—	—	MD21	MD20	—	—	—	—
Initial value:	0	—	—	0	0	0	0	0	0	0	—	—	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	MD14	MD13	—	MD11	MD10	MD09	MD08	MD07	MD06	MD05	MD04	MD03	MD02	MD01	MD00
Initial value:	0	—	—	0	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved When read, returns 0.
30, 29	MDT[1:0]	Depend on mode setting	R	The value of MDT0 and MDT1
28 to 22	—	All 0	R	Reserved. These bits are always read as 0. Writing is inhibited.
21, 20	MD[21:20]	Depend on mode setting	R	The value of MD21 and MD20
19, 18	—	All 0	R	Reserved. These bits are always read as 0. Writing is inhibited.
17, 16	—	All 1	R	Reserved. These bits are always read as 1. Writing is inhibited.
15	—	0	R	Reserved When read, returns 0.
14, 13	MD[14:13]	Depend on mode setting	R	The value of MD14 and MD13
12	—	0	R	Reserved When read, returns 0.
11 to 0	MD[11:00]	Depend on mode setting	R	The value of MD11 to MD0

8.2.2 Cortex-A7 Reset Control Register (CA7RESCNT)

CA7RESCNT is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies whether the reset is issued to Cortex-A7 CPUn (n = 0 to 1) or not. The upper word of the write value should always be the code value H'5A5A. If the code value is read, it is always read as 0.

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'5A5A)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CA7 CPU0R	CA7 CPU1R	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	MD7 | ~ MD6	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'5A5A) When read, returns 0.
15 to 4	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
3	CA7CPU0R	MD7| ~ MD6	R/W	Issue reset to Cortex-A7 CPU0 0: Not assert the reset to Cortex-A7 CPU0 1: Assert the reset to Cortex-A7 CPU0
2	CA7CPU1R	1	R/W	Issue reset to Cortex-A7 CPU1 0: Not assert the reset to Cortex-A7 CPU1 1: Assert the reset to Cortex-A7 CPU1
1, 0	—	All 1	R	Reserved When read, returns 1. The write value should always be 1.

8.2.3 Watchdog Timer Reset Control Register (WDTRSTCR)

WDTRSTCR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies whether the watchdog timer overflow should be masked or not as a reset trigger. The upper word of the write value should always be the code value H'A55A. If the code value is read, it is always read as 0.

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Code value (H'A55A)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RWDT_ RSTMSK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	Code value	H'0000	R/W	Code value (H'A55A) When read, returns 0.
15 to 2	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
1	—	1	R	Reserved When read, returns 1. The write value should always be 1.
0	RWDT_ RSTMSK	1	R/W	RWDT Reset Mask This bit is used to mask the detection of RWDT overflow. 0: Reset request 1: Not reset request

8.2.4 PRESETOUT Control Register (RSTOUTCR)

RSTOUTCR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register controls the output level of external LSI pin RESETOUT# by software.

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RESOUT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
0	RESOUT	1	R/W	PRESETOUT# control by software This bit is used to specify the output level of PRESETOUT#. 0: PRESETOUT# is asserted 1: PRESETOUT# is negated

8.2.5 SYS Boot Address Register (SBAR)

SBAR is a link to CA7BAR. SBAR is write-only register. Therefore read access to SBAR is prohibited.

If System CPU (Cortex-A7) accesses to SBAR, System CPU (Cortex-A7) can write to CA7BAR.

8.2.6 SYS Boot Address Register2 (SBAR2)

SBAR2 is a link to CA7BAR2. SBAR2 is write-only register. Therefore read access to SBAR2 is prohibited.

If System CPU (Cortex-A7) accesses to SBAR2, System CPU (Cortex-A7) can write to CA7BAR2.

8.2.7 Cortex-A7 Boot Address Register (CA7BAR)

CA7BAR is a 32-bit readable/writable register, which can be accessed only in longwords.

This register specifies the boot space of the System CPU (Cortex-A7).

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SBAR[39:24]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SBAR[23:18]						—	—	—	—	—	BAREN	—	—	BTMD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0	00/10	
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	SBAR[39:18]	{H'00000, B'00}	R/W	System CPU (Cortex-A7) Boot Address When System CPU (Cortex-A7) accesses to the range of physical address from H'00 0000 0000 to H'00 0003 FFFF, the address bit in [39:18] is replaced by SBAR[39:18].
9 to 5	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
4	BAREN*2	0/1*1	R/W	BAREN bit 0: SBAR is not valid. 1: SBAR is valid.
3, 2	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
1, 0	BTMD[1:0]	00/10*1	R/W	Specifies the Boot area of System CPU (Cortex-A7) During Hardware Power On Reset the initial value of these bits depends upon MD3, MD2 and MD1 pin setting. 00: SBAR[39:18] is assigned to Boot address, set SBAR[17:0] to 0. 01: Prohibited. 10: Boots from Built-in memory. 11: Prohibited.

Notes: 1. Initial value depends upon MD3, MD2 and MD1 pin setting.

2. Do not rewrite BAREN = 1 simultaneously with SBAR and BTMD. After completing the setting of SBAR and BTMD with BAREN = 0, set only BAREN = 1.
   For example: Change SBAR[39:18] from A to B, and BTMD[1:0] = 00
   Step 1: Write SBAR[39:18] = B, BAREN = 0, BTMD[1:0] = 00
   Step 2: Write SBAR[39:18] = B, BAREN = 1, BTMD[1:0] = 00

8.2.8 Cortex-A7 Boot Address Register2 (CA7BAR2)

CA7BAR2 is a 32-bit readable/writable register, which can be accessed only in longwords. This register can be changed only in the secure mode.

This register specifies the boot space of the System CPU (Cortex-A7).

This register is initialized on power on reset caused by PRESET#.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SBAR2[39:24]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SBAR2[23:18]						—	—	—	—	—	BAREN	—	—	—	VLD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	SBAR2[39:18]	{H'00000, B'00}	R/W	System CPU (Cortex-A7) Boot Address2 When System CPU (Cortex-A7) accesses to the range of physical address from H'00 0000 0000 to H'00 0003 FFFF, the address bit in [39:18] is replaced by SBAR2[39:18].
9 to 5	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
4	BAREN*	0	R/W	BAREN bit 0: SBAR2 is not valid. 1: SBAR2 is valid.
3 to 1	—	All 0	R	Reserved When read, returns 0. The write value should always be 0.
0	VLD	0	R/W	VALID bit When 1 is set to this bit, System CPU (Cortex-A7) starts only from the address set to SBAR2. 0: System CPU (Cortex-A7) starts from the address set to SBAR. 1: System CPU (Cortex-A7) starts from the address set to SBAR2.

Note: * Do not rewrite BAREN = 1 simultaneously with SBAR2 and VLD. After completing the setting of SBAR2 and VLD with BAREN = 0, set only BAREN = 1.
For example: Change SBAR2[39:18] from A to B, and VLD = 1
Step 1: Write SBAR2[39:18] = B, BAREN = 0, VLD = 1
Step 2: Write SBAR2[39:18] = B, BAREN = 1, VLD = 1

8.3 Operation

8.3.1 Power-On Reset by PRESET# Pin

Since the PLL circuit is initialized when the LSI enters the power-on reset state, the PLL oscillation settling time needs to be secured. This means that a high level must not be input to the PRESET# pin during the PLL oscillation settling time. For the power-on oscillation settling time (tOSC), see section 51, Electrical Characteristics.

After the state on the PRESET# pin input is changed from a low level to high level, the internal reset state continues until the flash ROM reset time (longer than 50 µs), the flash ROM holding time (longer than 5 µs) and the reset holding time elapse.

(1) Sequence for Turning on the Power

When the power is turned on, ensure that a low level is input to the PRESET# pin. A low level input is also needed on the TRST# pin.

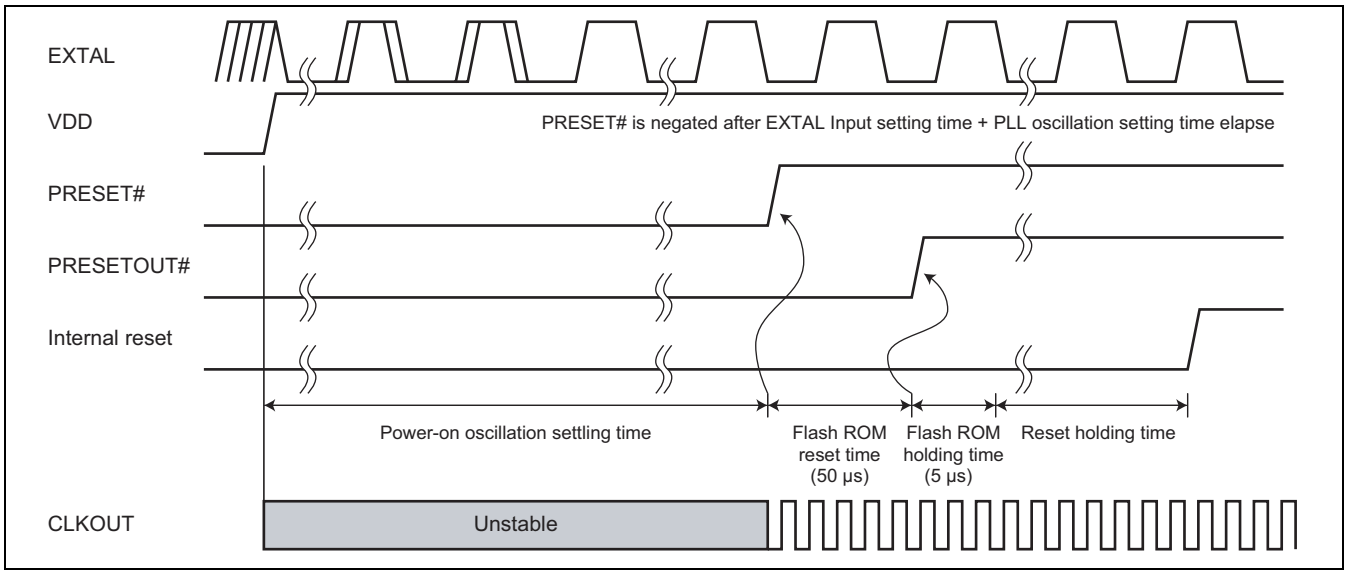


Figure 8.2 Free-Running Mode

8.4 Usage Notes

8.4.1 Usage of SYS Boot Address Register (SBAR) and SYS Boot Address Register 2 (SBAR2)

The SYS boot address register (SBAR) and SYS boot address register 2 (SBAR2) are write-only registers. Therefore read access to these registers is prohibited. Read CA7BAR and CA7BAR2, if read access is required.

8.4.2 Usage of Boot Address Register and Boot Address Register 2 (SBAR, SBAR2, CA7BAR, and CA7BAR2)

The boot address register and boot address register 2 (SBAR, SBAR2, CA7BAR and CA7BAR2) are not initialized by WDT reset. In the case of changing these boot address registers, the boot address must point to the address of internal RAMs. Because the internal RAMs are not initialized by WDT reset, the master boot processor can boot from them regardless of the selected boot device.

Read WOVF bit in the register RWTCSRA of RWDT by the program allocated on the internal RAMs pointed by the boot address registers and judge whether the cause of reset is WDT overflow or not. When the cause of reset is judged as WDT reset, apply appropriate processing, for example jump to the top address of mask ROM.

9. AP-System Core

9.1 Overview

The AP-System core is a core block equipped with Cortex-A7. For details on the functions of Cortex-A7, see the relevant Technical Reference Manual.

Table 9.1 Features of the AP-System Core Block (Cortex-A7)

Version	r0p5
Cluster number	Cluster 0
Number of CPUs	Dual CPU
L1 cache (per CPU)	I/ 32 KB (16 KB × 2 way) D/32 KB (8 KB × 4 way)
L2 cache	512 KB (64 KB × 8 way)
ECC	Not supported
MMU	Supported
NEON/VFP	NEON supported (SIMDv2) VFP supported (VFPv4)
Operating clock	CPU core: 1 GHz (Z2ϕ) L2-Tag RAMs: Z2ϕ L2-Data RAMs: 2-divided clock of Z2ϕ AXI bus: 520 MHz (ZXϕ)
Low power mode	Sleep mode (each CPU) Core standby mode (each CPU) AP-system core power down mode (CPUs and L2 cache shutdown)
Private peripherals	ARM Generic Timer supported

9.2 Generic Counter

For the general explanation about Generic Counter, and the details of the relation between Generic Counter and Generic Timer, refer to the ARM manual. In this section, it is explained that the frequency for count-up of the Generic Counter.

9.2.1 Frequency for Counting Up

The generic timer counts up by one every clock edge of the following frequency continuously.

Count-up clock frequency: ZSϕ × 1/8

The operating frequency of EXTAL is decided by mode pin setting. For details, see Table 7.4, PLL Multiplication Ratio in section 7, Clock Pulse Generator (CPG).

9.2.2 Counter Module Control and Status Registers

The base address of counter module control and status registers is H'E6080000.

For the details of these registers, refer to the ARM manual shown below.

DDI0406C2c_arm_architecture_reference_manual Appendix D.3 Counter module control and status registers.

9.2.3 How to Start a Generic Counter

Set bit 0 in CNTCR to 1 to start the Generic Counter when the CPU is placed in the secure mode.

9.2.4 Relation with a CoreSight Timestamp

The Generic Counter serves as the CoreSight Timestamp function.

For details, refer to the ARM manual shown below.

DDI0406C2c_arm_architecture_reference_manual Appendix D.1.2 Generic Timer relationship with CoreSight Timestamp counter.

9.3 Power-Down Mechanism

9.3.1 Overview

The AP-System core supports the following power-down modes.

- AP-System core power down mode
  (CPUs and L2 Cache shutdown)
- Core standby mode (each CPU)*[1]
- Sleep mode (clock stop, each CPU)
- L2 shutdown mode*[2]

However, this product doesn't support the power-gating in the AP-System core.

In AP-System core power down mode, the power of the AP-System core area is still supplied. The system boots up from the reset vector at its return from AP-System core power down mode. For detail of the AP-system core power down control, see section 49, System Controller (SYSC).

In Core standby mode, all memories including L1 cache of the relevant CPU do not keep its contents, but the contents of the SRAM of level 2 cache is retained.

In L2 shutdown mode, the contents of both L1s and L2 are not to be retained.

For details of Core standby mode and L2 shutdown mode, see section 7B, Advanced Power Management Unit for AP-System Core (APMU).

Notes: 1. If each CPU enters into the core standby mode, the clock supply for each CPU is stopped even if CPU core is always supplied power. After the power-on reset, the CPU other than the master CPU is in the core standby mode. When using the CPU in the core standby mode, follow the power-on sequence in order to start supply of the clock.

2. In L2 shutdown mode, all CPUs & L2 Cache (including both logic & memory) are still supplied power. However, after resuming from this mode, all CPUs & L2 Cache are reset. The contents of both L1 RAMs & L2 RAMs are not to be retained. Therefore, when using L2 shutdown mode, please follow the sequence that is described in Technical Reference Manual – section 2.4.2 - Multiprocessor device shutdown mode

10. Inter Connect RAM

10.1 Overview

The module provides a set of the Inter Connect RAM.

10.1.1 Features

- Memory size:
  Inter connect RAM0 : 72 Kbytes
  Inter connect RAM1 : 4 Kbytes
  Inter connect RAM2 : 128 Kbytes
- Undefined on power-on reset. Retained on other resets.
- Inter connect RAM takes charge of buffer between CPUs.

Table 10.1 Address Maps

Register Name	R/W	Address	Access Size
Inter connect RAM2 direct access space	R/W	H'E630 0000 to H'E631 FFFF	8, 16, 32
Inter connect RAM0 direct access space	R/W	H'E63A 0000 to H'E63B 1FFF	8, 16, 32
Inter connect RAM1 direct access space	R/W	H'E63C 0000 to H'E63C 0FFF	8, 16, 32

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

11. Interrupt Controller for AP-System Core (INTC-SYS)

This module handles system domain interrupt events.

11.1 Features

(1) INTC-SYS

- Interrupt controller for AP-system core
- 32 programmable priority levels
- ARM-IRQ interrupt generation
- INTC-SYS peripheral interrupt

(2) IRQC

- Common module to handle the external NMI/IRQ inputs
- Edge-triggered on rising, falling or both
- Level-sensitive on high or low values
- IRQ signal debouncing

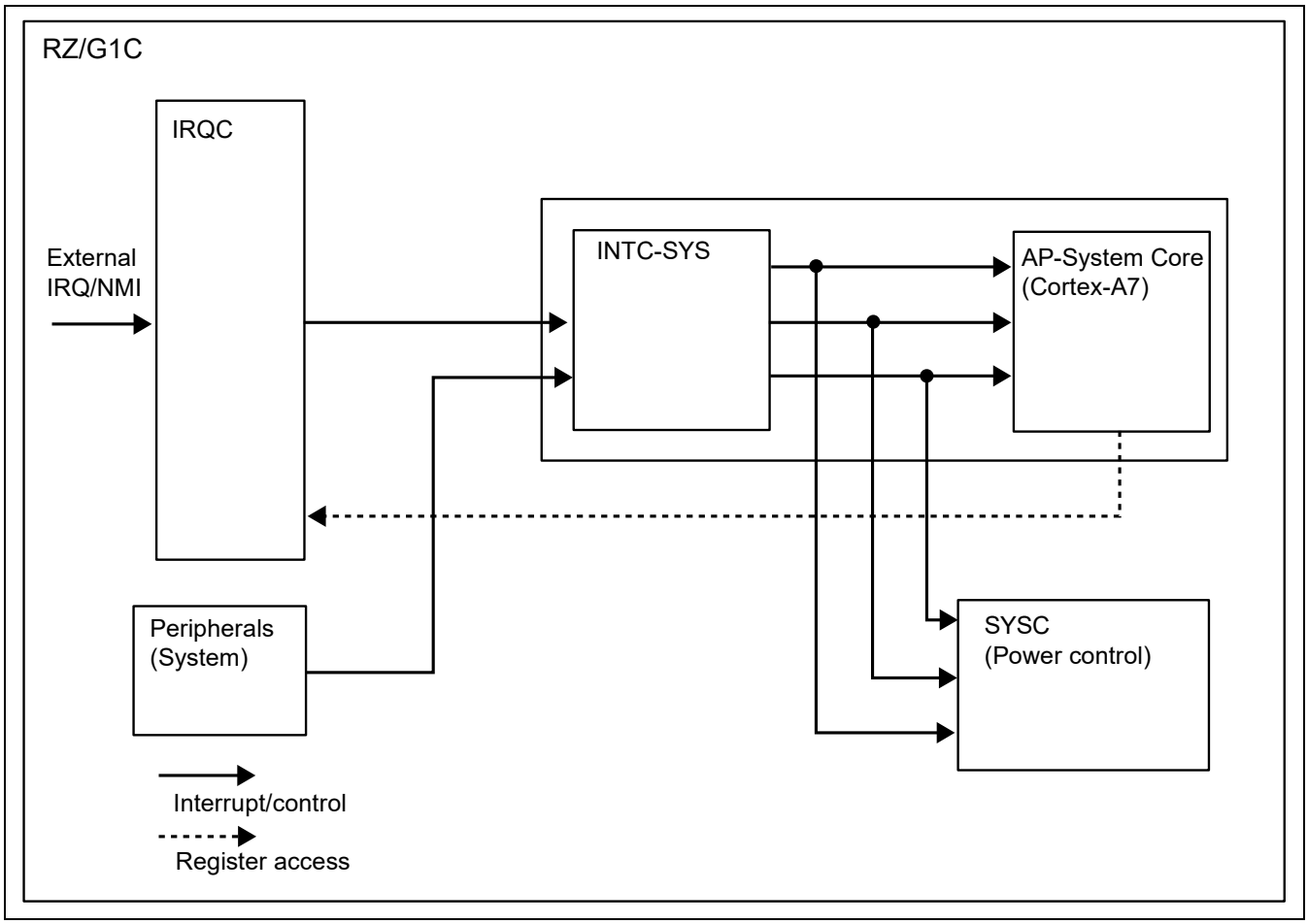


Figure 11.1 Block diagram of INTC

11.2 Interrupt Requests to AP-SYSTEM core

INTC-SYS is based on ARM Generic Interrupt Controller. For more information, see ARM Generic Interrupt Controller Architecture Specification and section 9, AP-System Core.

11.2.1 Interrupts Mapping

Table 11.1 shows the AP-system core interrupt controller (INTC-SYS) interrupt mapping.

Note: All interrupts should be level-sensitive configuration.

Table 11.1 AP-System core (INTC-SYS) Interrupt Mapping

SPI#	Source	SPI#	Source
0	IRQ0	34	DRI ch.2
1	IRQ1	35	DRI ch.3
2	IRQ2	36	Reserved
3	IRQ3	37	Reserved
4	GPIO0	38	Reserved
5	GPIO1	39	Reserved
6	GPIO2	40	Reserved
7	GPIO3	41	Reserved
8	GPIO4	42	Reserved
9	GPIO5	43	Reserved
10	Reserved	44	Reserved
11	Reserved	45	Reserved
12	IRQ4	46	Reserved
13	IRQ5	47	Reserved
14	IRQ6	48	Reserved
15	IRQ7	49	Reserved
16	IRQ8	50	Reserved
17	IRQ9	51	Reserved
18	Reserved	52	Reserved
19	I2C4	53	Reserved
20	Reserved	54	Reserved
21	HSCIF2	55	Reserved
22	SCIF2	56	Reserved
23	SCIF3	57	Reserved
24	SCIF4	58	Reserved
25	SCIF5	59	Reserved
26	Reserved	60	Reserved
27	Reserved	61	Reserved
28	Reserved	62	Reserved
29	Reserved	63	Reserved
30	Reserved	64	Reserved
31	Reserved	65	Reserved
32	DRI ch.0	66	Reserved
33	DRI ch.1	67	Reserved

SPI#	Source
68	Reserved
69	Reserved
70	Reserved
71	Reserved
72	Reserved
73	Reserved
74	Reserved
75	Reserved
76	Reserved
77	Reserved
78	Reserved
79	Reserved
80	Reserved
81	Reserved
82	CA7_IRQPMU-Core0
83	CA7_IRQPMU-Core1
84	Reserved
85	Reserved
86	CA7_CTIIRQ-Core0
87	CA7_CTIIRQ-Core1
88	Reserved
89	Reserved
90	Reserved
91	CA7_nAXIERRIRQ
92	Reserved
93	Reserved
94	Reserved
95	Reserved
96	LBSC-WT0
97	Reserved
98	LBSC-DMAC0
99	LBSC-DMAC1
100	LBSC-DMAC2
101	Reserved
102	Reserved
103	Reserved
104	Reserved
105	Reserved
106	Reserved
107	HS-USB Ch0 interrupt
108	USB2.0 HOST 0
109	USB-DMAC00
110	USB-DMAC10
111	USB-DMAC (DDM0)

SPI#	Source
112	Reserved
113	USB2.0 HOST 1
114	Reserved
115	Reserved
116	Reserved
117	Reserved
118	Reserved
119	SGX531
120	CMT1_0
121	CMT1_1
122	CMT1_2
123	CMT1_3
124	CMT1_4
125	CMT1_5
126	CMT1_6
127	CMT1_7
128	TMU_TUNI3
129	TMU_TUNI4
130	TMU_TUNI5
131	TMU_TUNI9
132	TMU_TUNI10
133	TMU_TUNI11
134	Reserved
135	Reserved
136	TMU_TUNI0
137	TMU_TUNI1
138	TMU_TUNI2
139	Reserved
140	RWDT
141	Reserved
142	CMT0_0
143	CMT0_1
144	Reserved
145	Reserved
146	Reserved
147	TMU_TICPI5
148	Reserved
149	Reserved
150	Reserved
151	Reserved
152	SCIF0
153	SCIF1
154	HSCIF0
155	HSCIF1

SPI#	Source
156	MSIOF0
157	MSIOF1
158	MSIOF2
159	Reserved
160	Reserved
161	Reserved
162	Ethernet MAC (Fast Ether)
163	Ethernet AVB
164	Reserved
165	SDHI0
166	SDHI1
167	SDHI2
168	Reserved
169	Reserved
170	Reserved
171	Reserved
172	Reserved
173	Reserved
174	Reserved
175	Reserved
176	Reserved
177	Reserved
178	Reserved
179	Reserved
180	Reserved
181	Reserved
182	Reserved
183	Reserved
184	QSPI0
185	STB
186	CAN interface 0
187	CAN interface 1
188	VIN0
189	VIN1
190	Reserved
191	Reserved
192	Reserved
193	Reserved
194	Reserved
195	Reserved
196	Reserved
197	SYS-DMAC0_ERR
198	IPMMUDS
199	IPMMUDS (SEC)

SPI#	Source
200	SYS-DMAC_DEI0
201	SYS-DMAC_DEI1
202	SYS-DMAC_DEI2
203	SYS-DMAC_DEI3
204	SYS-DMAC_DEI4
205	SYS-DMAC_DEI5
206	SYS-DMAC_DEI6
207	SYS-DMAC_DEI7
208	SYS-DMAC_DEI8
209	SYS-DMAC_DEI9
210	SYS-DMAC_DEI10
211	SYS-DMAC_DEI11
212	SYS-DMAC_DEI12
213	SYS-DMAC_DEI13
214	SYS-DMAC_DEI14
215	Reserved
216	SYS-DMAC_DEI15
217	SYS-DMAC_DEI16
218	SYS-DMAC_DEI17
219	SYS-DMAC_DEI18
220	SYS-DMAC_ERR
221	IPMMU_M (SEC)
222	IPMMU_M
223	IPMMU_SY0
224	IPMMU_SY0 (SEC)
225	IPMMU_SY1
226	IPMMU_MP
227	Reserved
228	Reserved
229	Reserved
230	Reserved
231	Reserved
232	Reserved
233	CoreSight (RT)
234	APMU1
235	Reserved
236	Reserved
237	SDHI1 other
238	Reserved
239	QSPI1
240	Reserved
241	Reserved
242	Reserved
243	Reserved

SPI#	Source
244	CPG
245	APMU0
246	VSPD0
247	Reserved
248	GPIO0 (ALT)
249	GPIO1 (ALT)
250	GPIO2 (ALT)
251	GPIO3 (ALT)
252	GPIO4 (ALT)
253	GPIO5 (ALT)
254	Reserved
255	Reserved
256	DU0
257	Reserved
258	VCP3_VLC ch.0
259	VCP3_CE ch.0
260	IPMMU-GP
261	IPMMU-GP (SEC)
262	FDP1 ch.0
263	Reserved
264	Reserved
265	Reserved
266	Reserved
267	VSPS
268	DU1
269	Reserved
270	Reserved
271	Reserved
272	Reserved
273	Reserved
274	Reserved
275	Reserved
276	Reserved
277	Reserved
278	Reserved
279	Reserved
280	Reserved
281	Reserved
282	Reserved
283	Reserved
284	Reserved
285	2D-DMAC
286	I2C2
287	I2C0

SPI#	Source
288	I2C1
289	Reserved
290	I2C3
291	HS-USB Ch1 interrupt
292	USB-DMAC11
293	USB-DMAC01
294	USB-DMAC (DDM1)
295	Reserved
296	Reserved
297	SYSC
298	Reserved
299	Reserved
300	Reserved
301	Reserved
302	IR Receiver
303	TMU_TUNI6
304	TMU_TUNI7
305	TMU_TUNI8
306	TMU_TICPI8
307	Reserved
308	SYS-DMAC_DEI19
309	SYS-DMAC_DEI20
310	SYS-DMAC_DEI21
311	SYS-DMAC_DEI22
312	SYS-DMAC_DEI23
313	SYS-DMAC_DEI24
314	SYS-DMAC_DEI25
315	SYS-DMAC_DEI26
316	SYS-DMAC_DEI27
317	SYS-DMAC_DEI28
318	SYS-DMAC_DEI29
319	Reserved
320	AUDIO-DMAC_DEI0
321	AUDIO-DMAC_DEI1
322	AUDIO-DMAC_DEI2
323	AUDIO-DMAC_DEI3
324	AUDIO-DMAC_DEI4
325	AUDIO-DMAC_DEI5
326	AUDIO-DMAC_DEI6
327	AUDIO-DMAC_DEI7
328	AUDIO-DMAC_DEI8
329	AUDIO-DMAC_DEI9
330	AUDIO-DMAC_DEI10
331	AUDIO-DMAC_DEI11

SPI#	Source
332	AUDIO-DMAC_DEI12
333	Reserved
334	Reserved
335	Reserved
336	Reserved
337	Reserved
338	Reserved
339	Reserved
340	Reserved
341	Reserved
342	Reserved
343	Reserved
344	Reserved
345	Reserved
346	AUDIO-DMAC0_ERR
347	Reserved
348	Reserved
349	Reserved
350	Reserved
351	Reserved
352	Reserved
353	SCU1
354	SCU2
355	SCU3
356	SCU4
357	SCU5
358	SCU6

SPI#	Source
359	Reserved
360	Reserved
361	Reserved
362	Reserved
363	Reserved
364	Reserved
365	Reserved
366	Reserved
367	Reserved
368	Reserved
369	Reserved
370	SSI0
371	SSI1
372	SSI2
373	SSI3
374	SSI4
375	SSI5
376	SSI6
377	SSI7
378	SSI8
379	SSI9
380	Reserved
381	Reserved
382	Reserved
383	Reserved

11.3 Register Descriptions

This section describes the registers of INTC-SYS.

Module Name	Base Address
INTC-SYS CPU-IF	H'F100_2000
INTC-SYS Distributer-IF	H'F100_1000

11.3.1 INTC-SYS Register Configuration and Function Description

384 SPI interrupts are integrated into ID[415:32].

The INTC-SYS supports two CPU cores which are mapped as shown below.

Interface	CPU core
CPU0 interface	AP-System core (Cortex-A7) CPU0
CPU1 interface	AP-System core (Cortex-A7) CPU1
CPU2 interface	Reserved
CPU3 interface	Reserved
CPU4 interface	Reserved
CPU5 interface	Reserved
CPU6 interface	Reserved
CPU7 interface	Reserved

For more information of these registers, see Cortex-A7 Technical Reference Manual and ARM GIC-400 Generic Interrupt Controller Technical Reference Manual.

11.4 External Interrupt Controller (IRQC)

The IRQC is a common sub-module of interrupt controllers. This sub-module provides interrupt from external device and inter-domain communication.

11.4.1 Input/Output Pins

Table 11.2 shows the INTC pin configuration.

Table 11.2 Pin Configuration

Pin Name	Function	I/O	Description
MSIOF0_SCK_A	IRQ0 - External interrupt input pins	Input	Input of IRQ0 interrupt request signals from external device.
HRTS1#_A	IRQ1 - External non maskable Interrupt input pins	Input	Input of IRQ1 interrupt request signal from external device.
D15	IRQ2 - External non maskable Interrupt input pins	Input	Input of IRQ2 interrupt request signals from external device.
D4	IRQ3 - External non maskable Interrupt input pins	Input	Input of IRQ3 interrupt request signals from external device.
D0	IRQ4 - External non maskable Interrupt input pins	Input	Input of IRQ4 interrupt request signals from external device.
SDA0_A	IRQ5 - External non maskable Interrupt input pins	Input	Input of IRQ5 interrupt request signals from external device.
D7	IRQ6 - External non maskable Interrupt input pins	Input	Input of IRQ6 interrupt request signals from external device.
SD0_WP	IRQ7 - External non maskable Interrupt input pins	Input	Input of IRQ7 interrupt request signals from external device.
SSI_SDATA7_A	IRQ8 - External non maskable Interrupt input pins	Input	Input of IRQ8 interrupt request signals from external device.
SSI_SCK1_A	IRQ9 - External non maskable Interrupt input pins	Input	Input of IRQ9 interrupt request signals from external device.
NMI	NMI - External non maskable Interrupt input pins	Input	Input of NMI interrupt request signal from external device.

Note: All IRQ signals are always active.

11.4.2 Clocking and Pulse Width

This module uses 2 clocks:

Module clock: CPϕ.
Debounce clock: RCLK.

Because of sampling operation, the minimum pulse width on IRQ request signal is five module clock cycles.

11.4.3 Block Diagram

Figures 11.2 and 11.3 are block diagrams of IRQC.

The event detector block detects external IRQn, and supports noise reduction and edge detection.

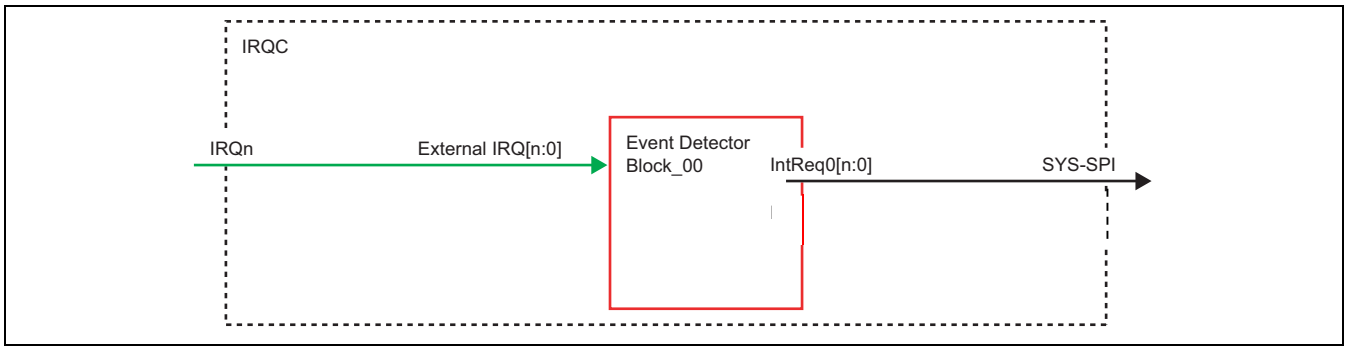


Figure 11.2 IRQC Block Diagram1

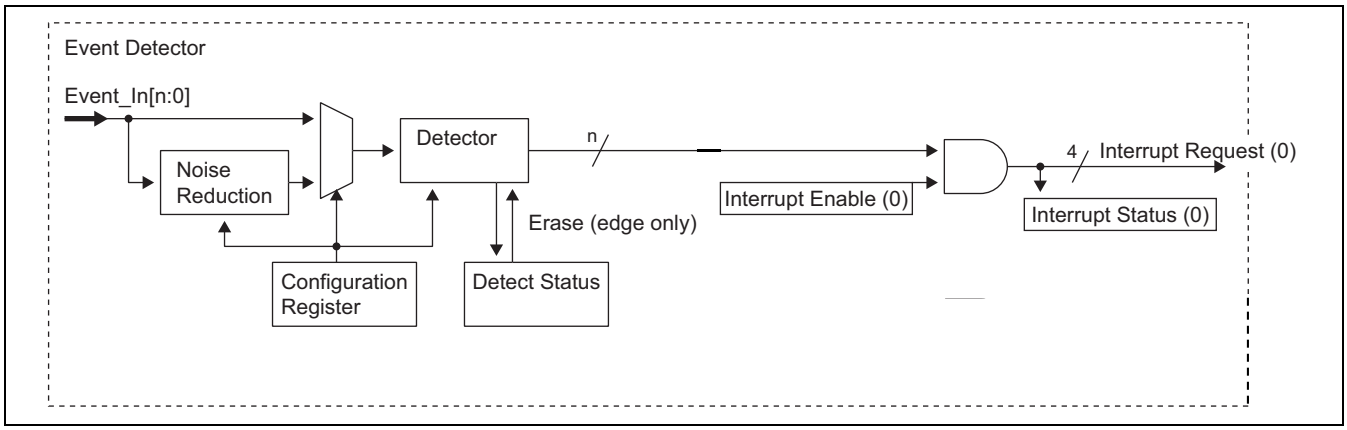


Figure 11.3 IRQC Event Detector

11.4.4 Register Descriptions

Table 11.3 shows the base address of each block and Tables 11.4 to 11.6 show register configuration.

Table 11.3 IRQC Base Address

Module Name	Base Address
IRQC	H'E61C 0000
IRQC event detector block	H'E61C 0000
NMI event detector block	H'E61C 0400
NMI mask lock block	H'E61C 0A00

Table 11.4 IRQC Event Detector Register Configuration

Register Name	Abbreviation	R/W	Address Offset	Access Size
Interrupt request status register 0	INTREQ_STS0	R	H'000	32
Interrupt enable status register 0	INTEN_STS0	R/WC1	H'004	32
Interrupt enable set register 0	INTEN_SET0	W	H'008	32
IRQn detect status register	DETECT_STATUS	R/WC1	H'100	32
IRQn signal level monitor register	MONITOR	R	H'104	32
IRQn high level detect status register	HLVL_STS	R	H'108	32
IRQn low level detect status register	LLVL_STS	R	H'10C	32
IRQn sync rising edge detect status register	S_R_EDGE_STS	R	H'110	32
IRQn sync falling edge detect status register	S_F_EDGE_STS	R	H'114	32
IRQn async rising edge detect status register	A_R_EDGE_STS	R	H'118	32
IRQn async falling edge detect status register	A_F_EDGE_STS	R	H'11C	32
IRQn chattering reduction status register	CHTEN_STS	R	H'120	32
IRQ0 configuration register	CONFIG_00	R/W	H'180	32
IRQ1 configuration register	CONFIG_01	R/W	H'184	32
IRQ2 configuration register	CONFIG_02	R/W	H'188	32
IRQ3 configuration register	CONFIG_03	R/W	H'18C	32
IRQ4 configuration register	CONFIG_04	R/W	H'190	32
IRQ5 configuration register	CONFIG_05	R/W	H'194	32
IRQ6 configuration register	CONFIG_06	R/W	H'198	32
IRQ7 configuration register	CONFIG_07	R/W	H'19C	32
IRQ8 configuration register	CONFIG_08	R/W	H'1A0	32
IRQ9 configuration register	CONFIG_09	R/W	H'1A4	32

Table 11.5 NMI Event Detector Register Configuration

Register Name	Abbreviation	R/W	Address Offset	Access Size
NMI request status register 0	NMIREQ_STS0	R	H'000	32
NMI enable status register 0	NMIEN_STS0	R/WC1	H'004	32
NMI enable set register 0	NMIEN_SET0	W	H'008	32
NMI detect status register	DETECT_STATUS_NMI	R/WC1	H'100	32
NMI signal level monitor register	MONITOR_NMI	R	H'104	32
NMI high level detect status register	HLVL_STS_NMI	R	H'108	32
NMI low level detect status register	LLVL_STS_NMI	R	H'10C	32
NMI sync rising edge detect status register	S_R_EDGE_STS_NMI	R	H'110	32
NMI sync falling edge detect status register	S_F_EDGE_STS_NMI	R	H'114	32
NMI async rising edge detect status register	A_R_EDGE_STS_NMI	R	H'118	32
NMI async falling edge detect status register	A_F_EDGE_STS_NMI	R	H'11C	32
NMI chattering reduction status register	CHTEN_STS_NMI	R	H'120	32
NMI debounce setting register	DEB_SET_NMI	R/W	H'140	32
NMI configuration 0 register	CONFIG0_NMI	R/W	H'180	32
NMI configuration 1 register	CONFIG1_NMI	R/W	H'184	32

Table 11.6 NMI Lock Register Configuration

Register Name	Abbreviation	R/W	Address Offset	Access Size
NMI mask lock set register	NMI_LCK	R/W*	H'000	32
NMI lock code register	NMI_LCKCODE	R/W*	H'004	32
NMI debug control enable register	NMI_DBG	R/W	H'008	32
NMI debug code register	NMI_DBGCODE	R/W	H'00C	32

Note: * It cannot update register value during lock.

11.4.4.1 Interrupt Request Status Register x (INTREQ_STSx [x = 0])

Note: x = 0: for INTC-SYS.

This register shows interrupt request status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	INTREQ									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	INTREQ[9:0]	All 0	R	Interrupt Status 0: Interrupt not generation 1: Interrupt generation

11.4.4.2 Interrupt Enable Status Register x (INTEN_STSx [x = 0])

Note: x = 0: for INTC-SYS.

This register shows interrupt enable status and clear interrupt enable.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	INTEN									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	INTEN[9:0]	All 0	R/WC1	Interrupt Enable Read 0: Interrupt generation is disabled Read 1: Interrupt generation is enabled Write 0: No functional effect Write 1: Interrupt enable clear

11.4.4.3 Interrupt Enable Set Register x (INTEN_SETx [x = 0])

Note: x = 0: for INTC-SYS.

This register set interrupt enable.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	INTENS									
Initial value:	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	INTENS[9:0]	—	W	Interrupt Enable Set Write 0: No functional effect Write 1: Interrupt enable set

11.4.4.4 IRQn Chattering Reduction Status Register (CHTEN_STS)

This register shows chattering reduction enable status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CHTEN									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	CHTEN[9:0]	All 0	R	Chattering Reduction Enable Status 0: Chattering reduction disabled 1: Chattering reduction enabled

Note: These bits need to reflect 3 rclk clock cycle.

11.4.4.5 IRQn Detect Status Register (DETECT_STATUS)

This register shows IRQn event detection status and provides the function to clear edge-triggered event. The status bit is cleared by writing 1 to the corresponding bit in edge-triggered mode. Writing 0 to this register bits does not affect to the register value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnDET									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnDET[9:0]	All 0	R/WC1	IRQn Event Detection Status Edge-triggered mode: Read 0: No interrupt request occurred Read 1: Interrupt request occurred Write 0: No functional effect Write 1: Cleared detection. Level-sensitive mode: Read 0: No interrupt request occurred. Read 1: Interrupt request occurred Write 0: No functional effect. Write 1: No functional effect.

11.4.4.6 IRQn Signal Level Monitor Register (MONITOR)

This register provides external signal monitor.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnMON									
Initial value:	0	0	0	0	0	0	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnMON[9:0]	—	R	IRQn External Signal Level Monitor This function show input value of external PINS. 0: IRQn is low level 1: IRQn is high level

11.4.4.7 IRQn High Level Detect Status Register (HLVL_STS)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnHSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnHSTS[9:0]	All 0	R	IRQn High Level Interrupt Status 0: IRQn high level interrupt request not occurred 1: IRQn high level interrupt request occurred

11.4.4.8 IRQn Low Level Detect Status Register (LLVL_STS)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnLSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnLSTS[9:0]	All 0	R	IRQn Low Level Interrupt Status 0: IRQn low level interrupt request not occurred 1: IRQn low level interrupt request occurred

11.4.4.9 IRQn Sync Rising Edge Detect Status Register (S_R_EDGE_STS)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnSRSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnSRSTS [9:0]	All 0	R	IRQn Synchronous Rise Edge Interrupt Status 0: IRQn rise edge interrupt request not occurred 1: IRQn rise edge interrupt request occurred

11.4.4.10 IRQn Sync Falling Edge Detect Status Register (S_F_EDGE_STS)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnSFSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnSFSTS [9:0]	All 0	R	IRQn Synchronous Fall Edge Interrupt Status 0: IRQn fall edge interrupt request not occurred 1: IRQn fall edge interrupt request occurred

11.4.4.11 IRQn Async Rising Edge Detect Status Register (A_R_EDGE_STS)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnARSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnARSTS [9:0]	All 0	R	IRQn Asynchronous Rise Edge Interrupt Status 0: IRQn rise edge interrupt request not occurred 1: IRQn rise edge interrupt request occurred

11.4.4.12 IRQn Async Falling Edge Detect Status Register (A_F_EDGE_STS)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	IRQnAFSTS									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	IRQnAFSTS [9:0]	All 0	R	IRQn Asynchronous Fall Edge Interrupt Status 0: IRQn fall edge interrupt request not occurred 1: IRQn fall edge interrupt request occurred

11.4.4.13 IRQn Configuration Register (CONFIG_n)

Note: n = 0 to 9

This register provides detection mode and noise reduction setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CHTEN	—	—	—	—	—	—	—	STS1		STS2					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SS					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CHTEN	0	R/W	Chattering Reduction Enable 0: Chattering reduction disabled 1: Chattering reduction enabled
30 to 24	—	All0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	STS1	00	R/W	IRQn Scan Timing These bits provide chattering reduction timing. 00: 1 ms 01: 2 ms 10: 4 ms 11: 8 ms
21 to 16	STS2	H'00	R/W	IRQn Chattering Reduction Period The chattering reduction period is defined by STS1 × STS2. H'00: No reduction H'01 to H'3F: STS1 × STS2 Notes: 1. These bits should not be set to H'00 when chattering reduction enable. 2. Check chattering reduction is disabled completely with corresponding bit of chattering reduction status register (CHTEN_STS) when this bit change.
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	SS	000000	R/W	Sense Selection 000000: Disable event detection 000001: Enable low level sensitive 000010: Enable high level sensitive 000100: Enable synchronous falling edge triggered 001000: Enable synchronous rising edge triggered 001100: Enable synchronous both edge triggered 010000: Enable asynchronous falling edge triggered 100000: Enable asynchronous rising edge triggered 110000: Enable asynchronous both edge triggered Others: setting prohibit Note: The Asynchronous edge triggered can use only as follow conditions. + EXTAL1 off + Chattering reduction not use. The synchronous edge triggered can use always.

11.4.4.14 NMI Request Status Register x (NMIREQ_STSx [x = 0])

Note: x = 0: for INTC-SYS.

This register shows external NMI request status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CnSTS							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	CnSTS	All 0	R	NMI Status (n = 0 to 7)* 0: not during NMI service 1: during NMI service

Note: * x = 0, n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 7 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.15 NMI Enable Status Register x (NMIEN_STSx [x = 0])

Note: x = 0: for INTC-SYS.

This register shows NMI interrupt enable status and clears NMI interrupt enable.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CnIEN							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	CnIEN	All 0	R/WC1	Interrupt Enable (n = 0 to 7)* Read 0: NMI interrupt generation is disabled Read 1: NMI interrupt generation is enabled Write 0: No functional effect Write 1: NMI interrupt enable clear

Note: * x = 0, n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 7 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.16 NMI Enable Set Register x (NMIEN_SETx [x = 0])

Note: x = 0: for INTC-SYS.

This register enables the NMI interrupt to each CPU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CnSET							
Initial value:	0	0	0	0	0	0	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	CnSET	—	W	Interrupt Enable Set (n = 0 to 7)* Write 0: No functional effect Write 1: Interrupt enable set

Note: * x = 0, n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 7 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.17 NMI Chattering Reduction Status Register (CHTEN_STS_NMI)

This register shows chattering reduction enable status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CHTEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	CHTEN	0	R	Chattering Reduction Enable Status 0: Chattering reduction disabled 1: Chattering reduction enabled

Note: These bits need to reflect 3 rclk clock cycle.

11.4.4.18 NMI Detect Status Register (DETECT_STATUS_NMI)

This register shows NMI event detection status and provides the function to clear edge-triggered event. The status bit is cleared by writing 1 to the corresponding bit in edge-triggered mode. Writing 0 to this register bits does not affect to the register value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInDET								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	NMInDET	All 0	R/WC1	NMIn Event Detect Status (n = 0 to 8)* Edge-triggered mode: Read 0: No interrupt request occurred Read 1: Interrupt request occurred Write 0: No functional effect Write 1: Cleared detection Level-sensitive mode: Read 0: No interrupt request occurred Read 1: Interrupt request occurred Write 0: No functional effect Write 1: No functional effect

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.19 NMI Signal Level Monitor Register (MONITOR_NMI)

This register provides external signal monitor.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NMIMON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	NMIMON	—	R	NMI External Signal Level Monitor This function show input value of external PINS. So, initial value depends on input value. 0: NMI is low level 1: NMI is high level

11.4.4.20 NMI Debounce Setting Register (DEB_SET_NMI)

This register provides noise reduction setting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CHTEN	—	—	—	—	—	—	—	STS1		STS2					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	CHTEN	0	R/W	Chattering Reduction Enable 0: Chattering reduction disabled 1: Chattering reduction enabled
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23, 22	STS1	00	R/W	NMI Scan Timing These bits provide chattering reduction timing. 00: 1 ms 01: 2 ms 10: 4 ms 11: 8 ms
21 to 16	STS2	H'00	R/W	NMI Chattering Reduction Period The chattering reduction period is defined by STS1 × STS2. H'00: No reduction H'01 to H'3F: STS1 × STS2 Note 1. These bits should not be set H'00 when chattering reduction enable. 2. Check chattering reduction is disabled completely with bit of chattering reduction status register (CHTEN_STS) when this bit change.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.

11.4.4.21 NMI High Level Detect Status Register (HLVL_STS_NMI)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInHSTS								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInHSTS	All 0	R	NMIn High Level Interrupt Status (n = 0 to 8)* 0: NMIn high level interrupt request not occurred 1: NMIn high level interrupt request occurred

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.22 NMI Low Level Detect Status Register (LLVL_STS_NMI)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInLSTS								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInLSTS	All 0	R	NMIn Low Level Interrupt Status (n = 0 to 8)* 0: NMIn low level interrupt request not occurred 1: NMIn low level interrupt request occurred

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.23 NMI Sync Rising Edge Detect Status Register (S_R_EDGE_STS_NMI)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInSRSTS								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInSRSTS	All 0	R	NMIn Synchronous Rise Edge Interrupt Status (n = 0 to 8)* 0: NMIn rise edge interrupt request not occurred 1: NMIn rise edge interrupt request occurred

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.24 NMI Sync Falling Edge Detect Status Register (S_F_EDGE_STS_NMI)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInSFSTS								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInSFSTS	All 0	R	NMIn Synchronous Fall Edge Interrupt Status (n = 0 to 8)* 0: NMIn fall edge interrupt request not occurred 1: NMIn fall edge interrupt request occurred

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.25 NMI Async Rising Edge Detect Status Register (A_R_EDGE_STS_NMI)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInARSTS								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInARSTS	All 0	R	NMIn Asynchronous Rise Edge Interrupt Status (n = 0 to 8)* 0: NMIn rise edge interrupt request not occurred 1: NMIn rise edge interrupt request occurred

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.26 NMI Async Falling Edge Detect Status Register (A_F_EDGE_STS_NMI)

This register provides interrupt detail detect status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	NMInAFSTS								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The writing value should always be 0.
8 to 0	NMInAFSTS	All 0	R	NMIn Asynchronous Fall Edge Interrupt Status (n = 0 to 8)* 0: NMIn fall edge interrupt request not occurred 1: NMIn fall edge interrupt request occurred

Note: * n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
n = 2 to 8 Reserved
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

11.4.4.27 NMI Configuration n Register (CONFIGn_NMI)

Note: n = 0 CPU0 interface (INTC-SYS)
n = 1 CPU1 interface (INTC-SYS)
For the CPUn interface, see section 11.3.1, INTC-SYS Register Configuration and Function Description.

This register provides detection mode and noise reduction setting.

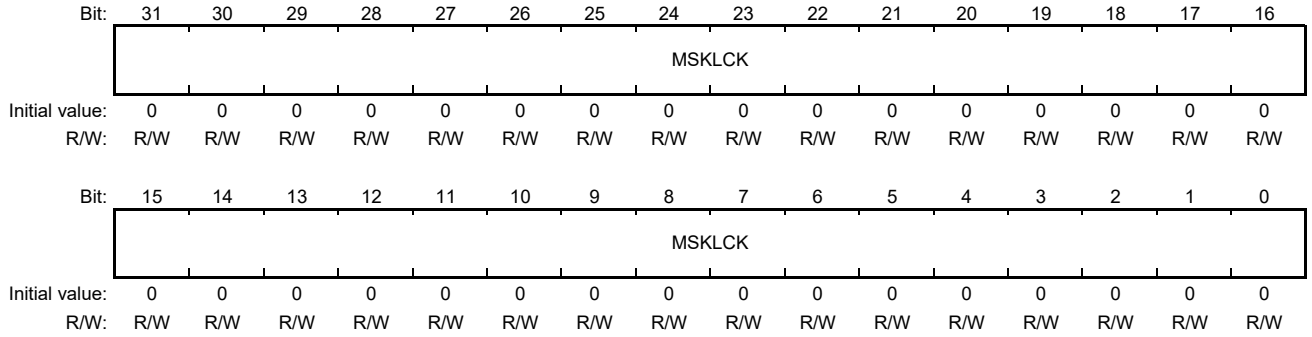
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	SS					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	SS	000000	R/W	Sense Selection 000000: Disable event detection 000001: Enable low level sensitive 000010: Enable high level sensitive 000100: Enable synchronous falling edge triggered 001000: Enable synchronous rising edge triggered 001100: Enable synchronous both edge triggered 010000: Enable asynchronous falling edge triggered 100000: Enable asynchronous rising edge triggered 110000: Enable asynchronous both edge triggered Others: setting prohibit Note: The Asynchronous edge triggered can be used only following conditions. - EXTAL1 off - Chattering reduction not be used. - Only low level sensitive can be used for ARM.

11.4.4.28 NMI Mask Lock Set Register (NMI_LCK)

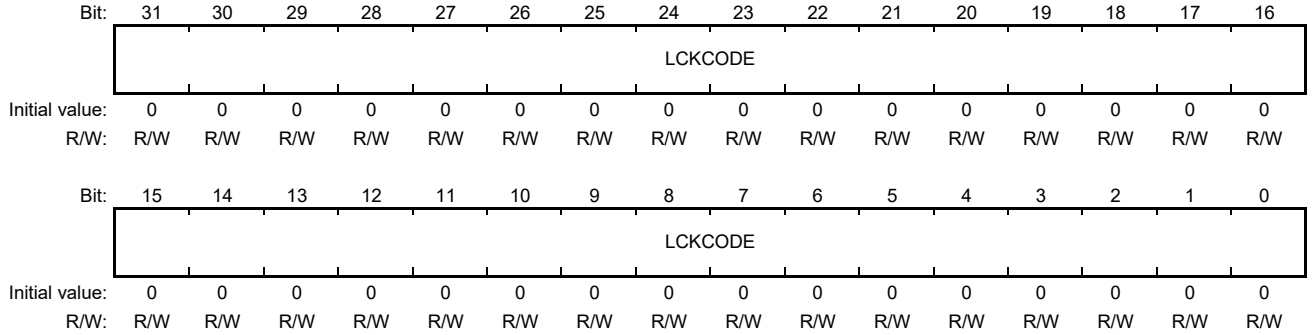
This register provides NMI mask locking feature. When set the same value as NMI_LCKCODE, then NMI cannot be masked by software (always accept NMI interrupt).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MSKLCK	All 0	R/W	Lock code setting

11.4.4.29 NMI Lock Code Register (NMI_LCKCODE)

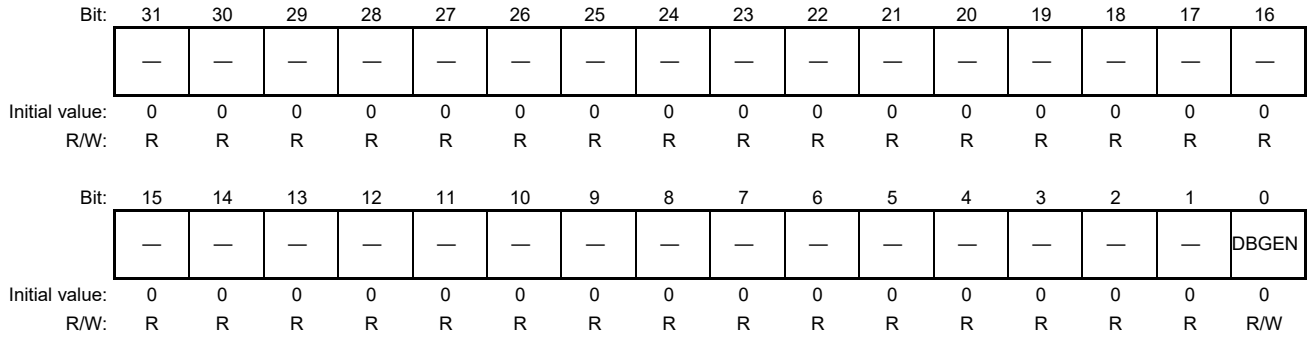
This register sets the value for lock code of NMI mask.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LCKCODE	All 0	R/W	NMI mask lock code setting

11.4.4.30 NMI Debug Control Enable Register (NMI_DBG)

This register enables the debug feature for NMI mask lock.

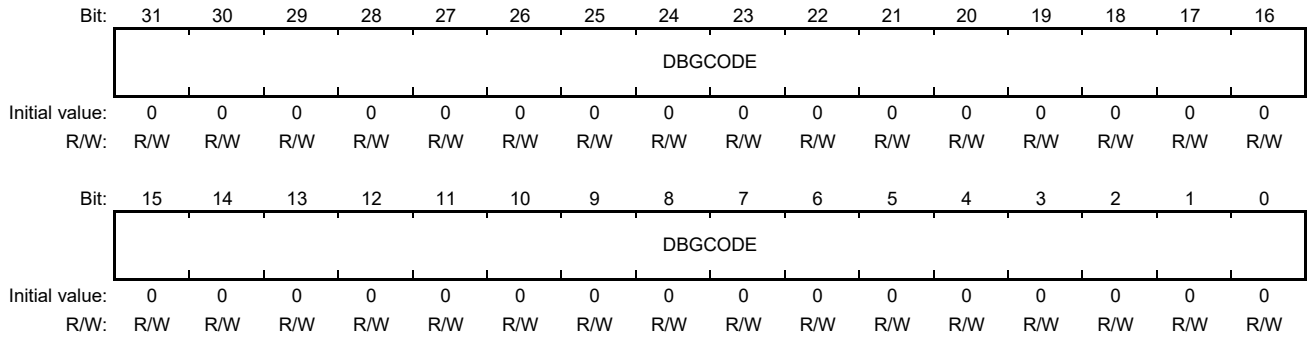


Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved
0	DBGEN	0	R/W	Enable debug for NMI mask lock feature

11.4.4.31 NMI Debug Code Register (NMI_DBGCODE)

This register sets value for debug code of NMI mask lock. When set the following value, then unlock this mask feature.

Debug code[31:0] = ~(lock code [0:31] (bit reversed))



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DBGCODE	All 0	R/W	NMI mask lock debug code setting

11.4.5 NMI Mask Lock Feature

NMI can be masked by setting NMI mask register. If you set the lock code to NMI lock code register and set the same lock code to NMI lock set register, then NMI cannot be masked by software (locked NMI mask). If you want to unlock NMI mask, you need to set DBGEN bit of NMI debug control register and set the unlock code to the NMI debug code register.

11.4.6 Procedure of NMI Mask Lock

- Lock feature

1. Write the lock code to NMI lock code register
   ex) Write32 (IRQC_BASE + H'0A04), H'00ACCE55
2. Write the lock code to NMI mask lock set register
   ex) Write32 (IRQC_BASE + H'0A00), H'00ACCE55
3. Write access to NMI lock code register and NMI mask lock set register
   — Check whether these registers cannot be updated

- Unlock feature

1. Set enable bit to NMI debug control register
   ex) Write32 (IRQC_BASE + H'0A08), H'00000001
2. Write unlock code to NMI debug code register
   ex) Write32 (IRQC_BASE + H'0A0C), H'558CCAFF
3. Write access to NMI lock code register and NMI mask lock register
   — Check whether these registers can be updated

12. AXI-bus

12.1 Overview

The AXI-bus is an on-chip interconnect bus based on the ARM® AMBA® Advanced eXtensible Interface (AXI) protocol specification. The AXI-bus has the following domains arranged in a hierarchical structure.

- Media domain AXI (MXI)
- Audio domain AXI
- System domain AXI
- ARM CPU domain AXI
- 3DGE AXI
- DMA domain AXI

12.1.1 Features

The AXI-bus has the following features.

- Frequency: 260 or 520 MHz
- Bus width: 256 bits or 128 bits
- High bandwidth and low latency
- Split transaction
- Separate data channels for reading and writing
- Quality-of-Service (QoS)
- Low-power function
- Secure access function

QoS is an extension to the standard AXI4 functionality, and allows control over the latency and bandwidth for the main memory.

12.1.2 Block Diagram

Figure 12.1 is a block diagram of the AXI-bus.

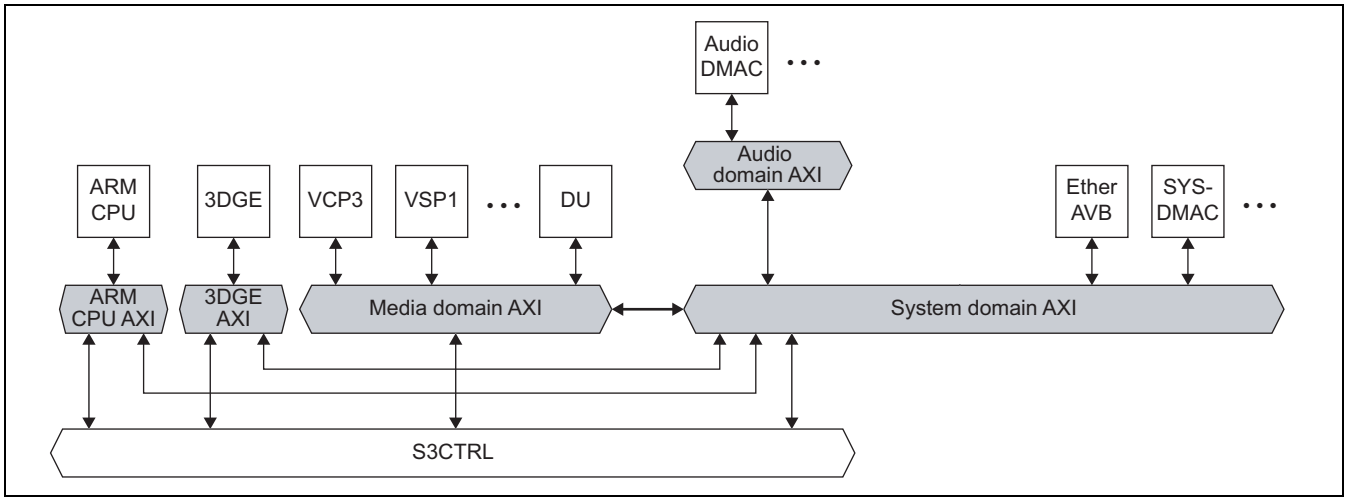


Figure 12.1 Block Diagram of AXI-bus

12.1.3 Input/Output Pins

No external pins are supported.

12.1.4 Register Base Address of AXI-bus

Base address of registers is allocated to following address. The method of setting is provided separately.

- H'FF80_0300 to H'FF80_21FF (system domain)
- H'FF82_0100 to H'FF82_21FF (audio domain)
- H'FF84_0100 to H'FF84_21FF (DMA domain)
- H'FF85_0100 to H'FF84_21FF (DMA domain)
- H'FF86_0100 to H'FF86_21FF (system domain)
- H'FF87_2000 to H'FF87_21FF (media domain)
- H'FF88_0100 to H'FF88_0FFF (ARM CPU domain)
- H'FF88_1100 to H'FF88_21FF (3DGE domain)
- H'FE96_4100 to H'FE96_7FFF (media domain)

12.1.5 Register Configuration

Table 12.1 shows a part of register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register in longword (32-bit) units. Operation cannot be guaranteed if access to a register is not in longword units.

Table 12.1 Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
MXI SDRAM address allocation register 0	MXSAAR0	R/W	H'FE96 0000	H'004000C0	32
MXI SDRAM address allocation register 1	MXSAAR1	R/W	H'FE96 0004	H'01000800	32
MXI read transaction control register	MXRTCR	R/W	H'FE96 0040	H'00000000	32
MXI write transaction control register	MXWTCR	R/W	H'FE96 0044	H'00000000	32

12.2 Register Description

Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers must be in longword units.

12.2.1 MXI SDRAM Address Allocation Register 0 (MXSAAR0)

Function: The media domain AXI (MXI) can control the target port of transaction for DRAM access. The transaction of the address between SADD0 and EADD0 is issued to S3CTRL. Others are issued to the system domain AXI.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SADD0[39:24]															
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EADD0[39:24]															
Initial value:	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SADD0[39:24]	H'0040	R/W	Start Address 0 [39:24].
15 to 0	EADD0[39:24]	H'00C0	R/W	End Address 0 [39:24].

12.2.2 MXI SDRAM Address Allocation Register 1 (MXSAAR1)

Function: The media domain AXI (MXI) can control the target port of transaction for DRAM access. The transaction of the address between SADD1 and EADD1 is issued to S3CTRL. Others are issued to the system domain AXI.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SADD1[39:24]															
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EADD1[39:24]															
Initial value:	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SADD1[39:24]	H'0100	R/W	Start Address 1 [39:24].
15 to 0	EADD1[39:24]	H'0800	R/W	End Address 1 [39:24].

12.2.3 MXI Read Transaction Control Register (MXRTCR)

Function: This register controls the read transaction of the media domain AXI (MXI).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	KPAR	RQPUSHEN	—	RTHRES		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	KPAR	0	R/W	0: Switch arbitration based on each transaction's QoS while ARVALID = 1 in ROB 1: Keep arbitration while ARVALID = 1 in ROB
4	RQPUSHEN	0	R/W	This bit should be set to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	RTHRES	000	R/W	These bits specify the unit of transaction threshold at which QoS arbitration is performed. The appropriate configuration depends on the system. 000: No limit 001: 1 010: 2 011: 4 100: 8 101: 16 110: 32 111: Reserved

12.2.4 MXI Write Transaction Control Register (MXWTCR)

Function: This register controls the write transaction of the media domain AXI (MXI).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	KPAW	WQPUSHEN	—	WTHRES		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	KPAW	0	R/W	0: Switch arbitration based on each transaction's QoS while AWVALID = 1 in ROB 1: Keep arbitration while AWVALID = 1 in ROB
4	WQPUSHEN	0	R/W	This bit should be set to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	WTHRES	000	R/W	These bits specify the unit of transaction threshold at which QoS arbitration is performed. The appropriate configuration depends on the system. 000: No limit 001: 1 010: 2 011: 4 100: 8 101: 16 110: 32 111: Reserved

12.3 Operation

12.3.1 Media Domain AXI Access Control

The media domain AXI (MXI) can control the target port of transaction for DRAM access. One of the target ports of S3CTRL or system domain AXI can be chosen for DRAM access through MXSAAR0 and MXSAAR1 registers. The transaction of the address through MXSAAR0 or MXSAAR1 register is issued to S3CTRL port.

13. IPMMU

13.1 Overview

The IPMMU is a Memory Management Unit (MMU) which provides address translation and access protection functionalities to processing units and interconnect networks.

13.1.1 Features

IPMMU includes the following main features.

- MMU architecture compatible with ARMv7 VMSA including the Large Physical Address Extension (LPAE), the Security Extensions and the Multiprocessing Extensions
- PMB address translation
- Caching recently used page table entries in translation look-aside buffer (TLB)
- Performance monitoring for ARMv7 LPAE, VMSA
- Distributed Virtual Memory (DVM) messages through Cache Coherent Interconnect doesn’t support

Note: IPMMU for 3D graphics module (IPMMU-GP) supports the 40-bit translation system with the ARMv7 long-descriptor translation table format and the PMB address translation. The IPMMU-GP doesn't support address translation of short-descriptor formats.

For more information about ARMv7 VMSA, see ARM Architecture Reference Manual ARMv7-A and ARMv7-R edition.

13.1.2 Block Diagram

Figure 13.1 shows the IPMMU system integration. When a master (a processing unit or an interconnect) issues a transaction, a micro-TLB connected to the master sends a virtual address to the IPMMU. If the virtual address is not cached in a main TLB of the IPMMU, the IPMMU performs a page table walk through an interconnect and returns a physical address to the micro-TLB.

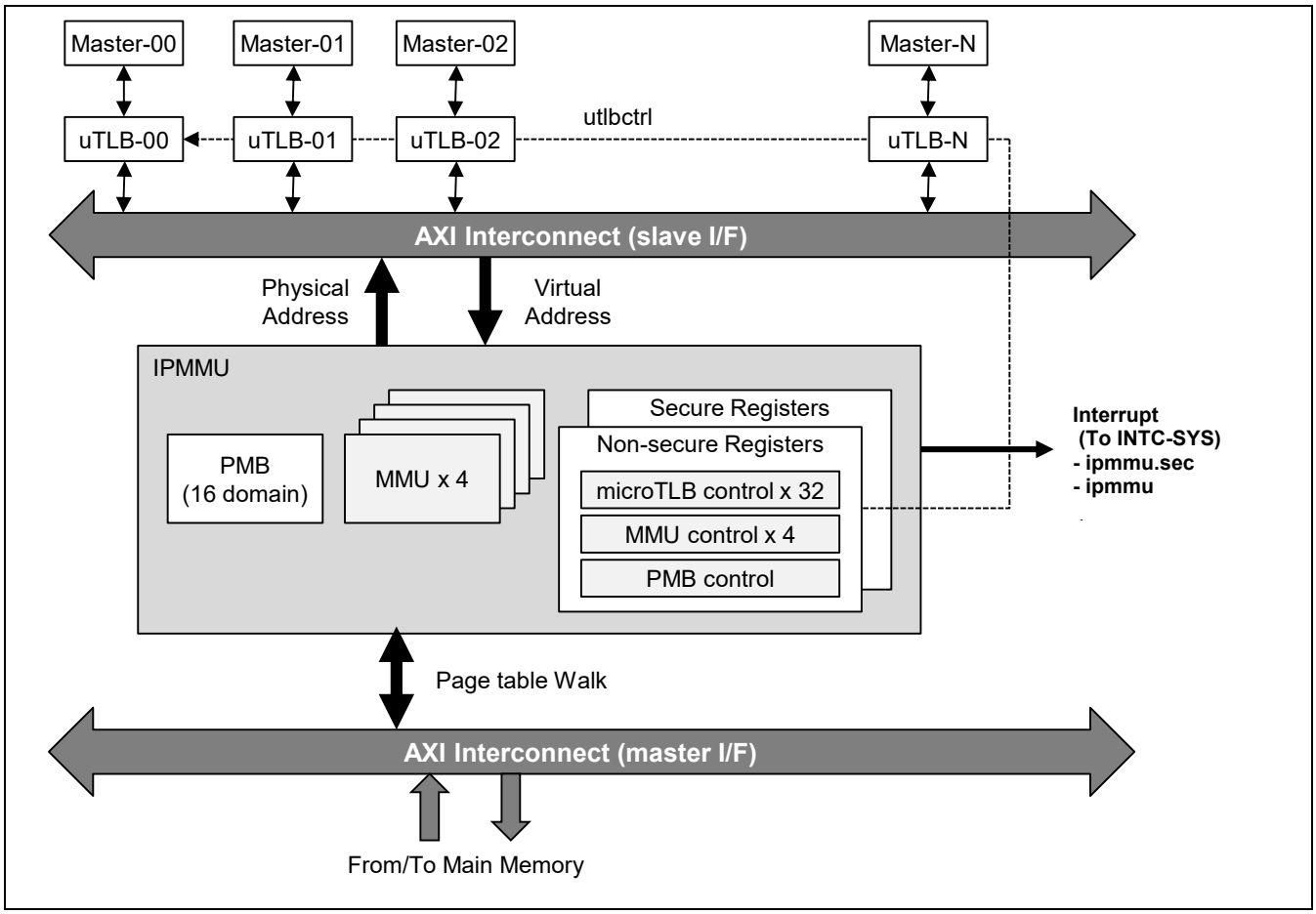


Figure 13.1 IPMMU Block Diagram

13.1.3 Input/Output Pins

There are no external pins in this module.

13.1.4 Register Configuration

Table 13.1 shows the IPMMU registers.

These registers are 32-bit access registers. When modifying reserved bits or read-only bits, write 0 to the bits.

Table 13.1 Register Configuration

Name	Abbreviation	R/W	Address	Size
MMU Control Register n (n = 0 to 3: * For IPMMU-GP, only n = 0)	IMCTRn IMSCTRn	R/W	H'0000 + H'40 × n	32
MMU Translation Table Base Control Register n	IMTTBCRn IMSTTBCRn	R/W	H'0008 + H'40 × n	32
MMU Translation Table Lower Base Register 0n	IMTTLBR0n IMSTTLBR0n	R/W	H'0010 + H'40 × n	32
MMU Translation Table Upper Base Register 0n	IMTTUBR0n IMSTTUBR0n	R/W	H'0014 + H'40 × n	32
MMU Translation Table Lower Base Register 1n	IMTTLBR1n IMSTTLBR1n	R/W	H'0018 + H'40 × n	32
MMU Translation Table Upper Base Register 1n	IMTTUBR1n IMSTTUBR1n	R/W	H'001C + H'40 × n	32
MMU Status Register n	IMSTRn IMSSTRn	R/W	H'0020 + H'40 × n	32
MMU Memory Attribute Indirection Register 0n	IMMAIR0n IMSMAIR0n	R/W	H'0028 + H'40 × n	32
MMU Memory Attribute Indirection Register 1n	IMMAIR1n IMSMAIR1n	R/W	H'002C + H'40 × n	32
MMU Error Address Register n	IMEARn IMSEARn	R	H'0030 + H'40 × n	32
PMB Control Register	IMPCTR IMPSCTR	R/W	H'0200	32
PMB Status Register	IMPSTR IMPSSTR	R/W	H'0208	32
PMB Error Address Register	IMPEAR IMPSEAR	R	H'020C	32
PMB Address Array n (n = 0 to 15)	IMPMBAn IMPMBSAn	R/W	H'0280 to H'02BC	32
PMB Data Array n	IMPMBDn IMPMBSDn	R/W	H'02C0 to H'02FC	32
uTLB Control Register n (n = 0 to 31: * For IPMMU-GP, only n = 0)	IMUCTRn IMUSCTRn	R/W	H'0300 + H'10 × n	32
uTLB ASID Register n	IMUASIDn IMUSASIDn	R/W	H'0308 + H'10 × n	32
MMU Performance Monitor Control Register	IMPFMCTR	R/W	H'0580	32
MMU Performance Monitor Total Transaction Counter	IMPFMMTOTAL	R	H'0590	32
MMU Performance Monitor Hit Counter	IMPFMMHIT	R	H'0594	32
MMU Performance Monitor L3 Miss Counter	IMPFMML3MISS	R	H'0598	32
MMU Performance Monitor L2 Miss Counter	IMPFMML2MISS	R	H'059C	32

Name	Abbreviation	R/W	Address	Size
Address alias of Non-secure registers *	—	R/W	H'0800 to H'0FFF	32

Note: * Non-secure registers (H'0000 to H'07FF) can be accessed through this address space in Secure state. In Non-secure state, this address space is always read as 0.

Table 13.2 shows the each IPMMU base address. Each IPMMU is connected to the each BUS modules.

Table 13.2 IPMMU Base Address

MMU	Base Address
IPMMU-SY0 (System domain AXI #0)	H'E6280000
IPMMU-SY1 (System domain AXI #1)	H'E6290000
IPMMU-DS (DMA domain AXI)	H'E6740000
IPMMU-MP (Audio domain AXI)	H'EC680000
IPMMU-MX (Media domain AXI)	H'FE951000
IPMMU-GP (3DGE AXI)	H'E62A0000

Table 13.3 shows the register state in each processing mode.

Table 13.3 Register State in Each Processing Mode

Register Abbreviation	Reset*	Initial value	Module Standby
IMCTRn IMSCTRn	Initialized	H'00000000	Retained
IMTTBCRn IMSTTBCRn	Initialized	H'00000000	Retained
IMTTLBR0n IMSTTLBR0n	Initialized	H'00000000	Retained
IMTTUBR0n IMSTTUBR0n	Initialized	H'00000000	Retained
IMTTLBR1n IMSTTLBR1n	Initialized	H'00000000	Retained
IMTTUBR1n IMSTTUBR1n	Initialized	H'00000000	Retained
IMSTRn IMSSTRn	Initialized	H'00000000	Retained
IMMAIR0n IMSMAIR0n	Initialized	H'00000000	Retained
IMMAIR1n IMSMAIR1n	Initialized	H'00000000	Retained
IMELARn IMSELARn	Initialized	H'00000000	Retained
IMEUARn IMSEUARn	Initialized	H'00000000	Retained
IMEWIDn IMSEWIDn	Initialized	H'00000000	Retained
IMERIDn IMSERIDn	Initialized	H'00000000	Retained

Register Abbreviation	Reset*	Initial value	Module Standby
IMPCTR IMPSCTR	Initialized	H'00000000	Retained
IMPSTR IMPSSTR	Initialized	H'00000000	Retained
IMPEAR IMPSEAR	Initialized	H'00000000	Retained
IMPMBA00 to 15 IMPMBSA00 to 15	Initialized	H'00000000	Retained
IMPMBD00 to 15 IMPMBSD00 to 15	Initialized	H'00000000	Retained
IMUCTRn IMUSCTRn	Initialized	H'00000000	Retained
IMUASIDn IMUSASIDn	Initialized	H'00000000	Retained
IMPFMMCTR	Initialized	H'00000000	Retained
IMPFMMTOTAL	Initialized	H'00000000	Retained
IMPFMHIT	Initialized	H'00000000	Retained
IMPFML3MISS	Initialized	H'00000000	Retained
IMPFML2MISS	Initialized	H'00000000	Retained

Note: * Refer to section 8, Reset (RST).

13.2 Register Description

13.2.1 MMU Control Register n (IMCTRn)

Note: n = 0 to 3

This register controls the behavior of the MMU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRE	AFE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	RTSEL[1:0]		TREN	INTEN	FLUSH	MMUEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	TRE	0	R/W	TEX Remap Enable This field is used when EAE is 0. 0: TEX remap disabled. 1: TEX remap enabled. Note: For IPMMUGP, set 0 to this bit
16	AFE	0	R/W	Access Flag Enable 0: Behave as if AF bit is always set to 1. 1: Enable software management of the Access Flag.
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	RTSEL[1:0]	00	R/W	Retranslation Table Select When TREN is 1, RTSEL indicates the table number to retranslate. Note: For IPMMUGP, set 0 to this bit
3	TREN	0	R/W	MMU Retranslation Enable 0: Output PA as a physical address. 1: Output PA as an intermediate physical address to retranslate through 40-bit TLB. Note: For IPMMUGP, set 0 to this bit
2	INTEN	0	R/W	Interrupt Enable 0: Don’t assert an interrupt when an error occurs. 1: Assert an interrupt when an error occurs.
1	FLUSH	0	R/W	TLB Invalidate This bit is automatically cleared to 0. 1: Invalidate all TLB entries.
0	MMUEN	0	R/W	MMU Enable 0: MMU disabled 1: MMU enabled

13.2.2 MMU Translation Table Base Control Register n (IMTTBCRn)

Note: n = 0 to 3

This register controls the attribute of TLB managed by each MMU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EAE	PMB	SH1[1:0]		ORGN1[1:0]		IRGN1[1:0]		—	—	—	—	—	TSZ1[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SH0[1:0]		ORGN0[1:0]		IRGN0[1:0]		—	—	—	SL0	—	TSZ0[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	EAE	0	R/W	Extended Address Enable 0: Enable the 32-bit translation system with the ARMv7 Short-descriptor translation table format or PMB address translation. 1: Enable the 40-bit translation System with the ARMv7 Long-descriptor translation table format. Note: IPMMU-GP, set this bit to 1 (default).
30	PMB	0	R/W	PMB Enable 0: Disable PMB address translation. 1: Enable PMB address translation in the virtual address range from H'80000000 to H'BFFFFFFF. This field is used when EAE is 0.
29, 28	SH1[1:0]	00	R/W	Share ability attributes for the memory associated with the translation table walks using TTBR1n. 00: Non-shareable 01: Reserved 10: Outer shareable 11: Inner shareable
27, 26	ORGN1[1:0]	00	R/W	Outer Cache ability attributes for the memory associated with the translation table walks using TTBR1n. 00: Normal memory, Outer Non-cacheable 01: Normal memory, Outer Write-Back Write-Allocate Cacheable 10: Normal memory, Outer Write-Through Cacheable 11: Normal memory, Outer Write-Back no Write-Allocate Cacheable
25, 24	IRGN1[1:0]	00	R/W	Inner Cache ability attributes for the memory associated with the translation table walks using TTBR1n. 00: Normal memory, Inner Non-cacheable 01: Normal memory, Inner Write-Back Write-Allocate Cacheable 10: Normal memory, Inner Write-Through Cacheable 11: Normal memory, Inner Write-Back no Write-Allocate Cacheable
23 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	TSZ1[2:0]	000	R/W	The size offset of the TTBR1n addressed region, encoded as a 3-bit unsigned number, giving the size of the region as 2^(32-TSZ1).

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	SH0[1:0]	00	R/W	Share ability attributes for the memory associated with the translation table walks using TTBR0n. 00: Non-shareable 01: Reserved 10: Outer shareable 11: Inner shareable
11, 10	ORGN0[1:0]	00	R/W	Outer Cache ability attributes for the memory associated with the translation table walks using TTBR0n. 00: Normal memory, Outer Non-cacheable 01: Normal memory, Outer Write-Back Write-Allocate Cacheable 10: Normal memory, Outer Write-Through Cacheable 11: Normal memory, Outer Write-Back no Write-Allocate Cacheable
9, 8	IRGN0[1:0]	00	R/W	Inner Cache ability attributes for the memory associated with the translation table walks using TTBR0n. 00: Normal memory, Inner Non-cacheable 01: Normal memory, Inner Write-Back Write-Allocate Cacheable 10: Normal memory, Inner Write-Through Cacheable 11: Normal memory, Inner Write-Back no Write-Allocate Cacheable
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SL0	0	R/W	Starting level for translation table walks. 0: Start at second level 1: Start at first level
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	TSZ0[2:0]	000	R/W	The size offset of the TTBR0n addressed region, encoded as a 3-bit unsigned number, giving the size of the region as 2^(32-TSZ0).

13.2.3 MMU Translation Table Upper Base Register 0/1n (IMTTUBR0/1n)

Note: n = 0 to 3

This register indicates the base address of the TLB managed by each MMU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TTBR[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	TTBR[39:32]	H'00	R/W	Bits [39:32] of translation table base address This field is used when EAE is 1.

13.2.4 MMU Translation Table Lower Base Register 0/1n (IMTTLBR0/1n)

Note: n = 0 to 3

This register indicates the base address of the TLB managed by each MMU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TTBR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TTBR[15:4]												—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	TTBR[31:4]	All 0	R/W	Bits [31:4] of translation table base address
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

13.2.5 MMU Memory Attribute Indirection Register 0n (IMMAIR0n)

Note: n = 0 to 3

When using the Long-descriptor translation format, this register works as MAIR0, Memory Attribute Indirection Register in ARMv7 VMSA. When using the Short-descriptor translation format, this register works as PRRR, Primary Region Remap Register in ARMv7 VMSA.

(Long-descriptor translation format)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ATTR3[7:0]								ATTR2[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ATTR1[7:0]								ATTR0[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ATTR3[7:0]	H'00	R/W	The memory attribute encoding for an AttrIndx[2:0] entry.
23 to 16	ATTR2[7:0]	H'00	R/W	
15 to 8	ATTR1[7:0]	H'00	R/W	
7 to 0	ATTR0[7:0]	H'00	R/W	

(Short-descriptor translation format)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NOS7-0								—	—	—	—	NS1	NS0	DS1	DS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TRn[1:0] (n = 0 to 7)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	NOS7-0	All 0	R/W	Outer Shareable property mapping for memory attributes n. 0: Memory region is outer shareable. 1: Memory region is inner shareable.
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	NS1	0	R/W	Mapping of S = 1 attribute for Normal memory. 0: Region is not shareable. 1: Region is shareable.

Bit	Bit Name	Initial Value	R/W	Description
18	NS0	0	R/W	Mapping of S = 0 attribute for Normal memory. 0: Region is not shareable. 1: Region is shareable.
17	DS1	0	R/W	Mapping of S = 1 attribute for Device memory. 0: Region is not shareable. 1: Region is shareable.
16	DS0	0	R/W	Mapping of S = 0 attribute for Device memory. 0: Region is not shareable. 1: Region is shareable.
15 to 0	TRn[1:0] (n = 0 to 7)	All 0	R/W	Primary TEX mapping for memory attributes n. n is the value of TEX[0], C and B bits. 00: Strongly-ordered 01: Device 10: Normal memory 11: Reserved

13.2.6 MMU Memory Attribute Indirection Register 1n (IMMAIR1n)

Note: n = 0 to 3

When using the Long-descriptor translation format, this register works as MAIR1, Memory Attribute Indirection Register in ARMv7 VMSA. When using the Short-descriptor translation format, this register works as NMRR, Normal Memory Remap Register in ARMv7 VMSA.

(Long-descriptor translation format)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ATTR7[7:0]								ATTR6[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ATTR5[7:0]								ATTR4[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	ATTR7[7:0]	H'00	R/W	The memory attribute encoding for an AttrIndx[2:0] entry.
23 to 16	ATTR6[7:0]	H'00	R/W	
15 to 8	ATTR5[7:0]	H'00	R/W	
7 to 0	ATTR4[7:0]	H'00	R/W	

(Short-descriptor translation format)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	ORn[1:0] (n = 0 to 7)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IRn[1:0] (n = 0 to 7)															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	ORn[1:0] (n = 0 to 7)	All 0	R/W	Outer Cacheable property mapping for memory attributes n. 00: Region is non-cacheable. 01: Region is write-back, write-allocate. 10: Region is write-through, no write-allocate. 11: Region is write-back, no write-allocate.

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	IRn[1:0] (n = 0 to 7)	All 0	R/W	Inner Cacheable property mapping for memory attributes n. 00: Region is non-cacheable. 01: Region is write-back, write-allocate. 10: Region is write-through, no write-allocate. 11: Region is write-back, no write-allocate.

13.2.7 MMU Error Status Register n (IMSTRn)

Note: n = 0 to 3

This register indicates the error status of during address translation.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ERRLVL[1:0]		—	ERRCODE[2:0]			—	—	—	MHIT	—	ABORT	PF	TF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	ERRLVL [1:0]	00	R	indicate which level of page table walk caused the error
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	ERRCODE [2:0]	000	R	Indicate error type 001: TLB format error (except “block” or “table”) 100: access permission error 101: secure access error Others: reserved
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MHIT	0	R/W	Indicate that multiple TLB hits occurred.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ABORT	0	R/W	This bit is set to 1 when the IPMMU received an error response during a page table walk.
1	PF	0	R/W	Page Fault This bit is set to 1 when an access right violation occurred.
0	TF	0	R/W	Translation Fault This bit is set to 1 when a translation fault occurred during a page table walk.

13.2.8 MMU Error Address Register n (IMEARn)

Note: n = 0 to 3

This register indicates the address which an address translation error occurred.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EAR[31:0]	All 0	R/W	The faulting virtual address is set when an address translation error occurred.

13.2.9 PMB Control Register (IMPCTR)

This register controls the behavior of the PMB function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TTSEL[1:0]		TTEN	INTEN	—	PMBEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	TTSEL[1:0]	00	R/W	Translation Table Select Note: For IPMMU-GP, set 00 to this bit.
3	TTEN	0	R/W	TLB Translation Enable 0: Output PPN as a physical address. 1: Output PPN as an intermediate physical address to retranslate through 40-bit TLB. PPN[39:32] is not used in retranslation. Note: For IPMMU-GP, set 0 to this bit.
2	INTEN	0	R/W	Interrupt Enable 0: Don’t assert an interrupt when an error occurred. 1: Assert an interrupt when an error occurred.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	PMBEN	0	R/W	PMB Enable 0: PMB disabled 1: PMB enabled

13.2.10 PMB Address Array n (IMPMBAn)

Note: n = 0 to 15

This register is used for setting the virtual page number.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VPN[31:24]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	V	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VPN[31:24]	All 0	R/W	Virtual Page Number For 16-Mbyte page, VPN[31:24] is used. For 64-Mbyte page, VPN[31:26] is used. For 128-Mbyte page, VPN[31:27] is used. For 512-Mbyte page, VPN[31:29] is used.
23 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	V	0	R/W	Enable this page translation.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

13.2.11 PMB Data Array n (IMPMBDn)

Note: n = 0 to 15

This register is used for setting the physical page number and the memory size which PMB managed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PPN[31:24]								PPN[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	V	SZ[1]	—	—	SZ[0]	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PPN[31:24]	All 0	R/W	Physical Page Number For 16-Mbyte page, PPN[31:24] is used. For 64-Mbyte page, PPN[31:26] is used. For 128-Mbyte page, PPN[31:27] is used. For 512-Mbyte page, PPN[31:29] is used.
23 to 16	PPN[39:32]	All 0	R/W	Upper Physical Page Number
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	V	0	R/W	Enable this page translation.
7	SZ[1]	0	R/W	This bit and SZ[0] (bit 4) specify the page size. SZ[1:0] = 00: 16-Mbyte page 01: 64-Mbyte page 10: 128-Mbyte page 11: 512-Mbyte page
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SZ[0]	0	R/W	Page Size See the description of SZ[1] (bit 7).
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

13.2.12 PMB Status Register (IMPSTR)

This register indicates the error status of the address translation by PMB.

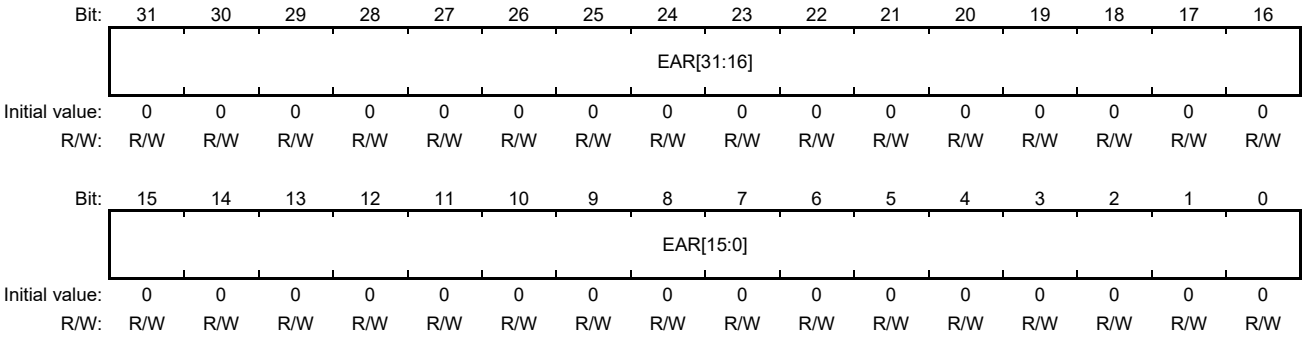
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	MHIT	—	—	—	TF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	MHIT	0	R/W	Multiple hit Indicate that multiple PMB hits occurred.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TF	0	R/W	Translation Fault This bit is set to 1 when a translation fault occurred during a PMB translation.

13.2.13 PMB Error Address Register (IMPEAR)

This register indicates the address which an address translation error occurred.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EAR[31:0]	All 0	R/W	The faulting virtual address is set when an address translation error occurred.

13.2.14 uTLB Control Register n (IMUCTRn)

Note: n = 0 to 31

This register controls the behavior of each uTLB.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIXADDEN	—	—	—	—	—	—	—	FIXADD[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

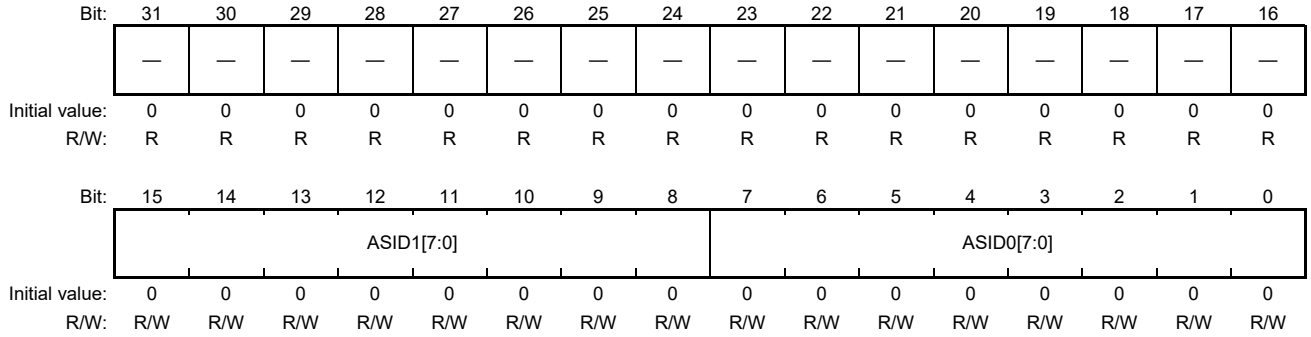
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TTSEL[3:0]				—	—	FLUSH	MMUEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FIXADDEN	0	R/W	Fix the upper 8 bits of physical address Always output the upper 8 bits of physical address as FIXADD[39:32]. This bit must be used only in 32-bit translation mode. 0: Disable FIXADD[39:32]
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	FIXADD [39:32]	All 0	R/W	When FIXADDEN is 1, the upper 8bit of physical address is FIXADD[39:32]. This bit must be used only in 32-bit translation mode.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	TTSEL[3:0]	0000	R/W	Translation Table 0000 to 0011: MMUn 0100 to 0111: Reserved 1000: PMB 1001 to 1111: Reserved Note: For IPMMU-GP, set 0000 or 1000 to these bits.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	FLUSH	0	R/W	micro-TLB Invalidate Invalidate all entries in the micro-TLB. This bit is automatically cleared to 0. 1: Invalidate all entries.
0	MMUEN	0	R/W	Address Translation Enable 0: Disable address translation 1: Enable address translation

13.2.15 uTLB ASID Register n (IMUASIDn)

Note: n = 0 to 31

This register is used for setting ASID of each uTLB.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	ASID1[7:0]	H'00	R/W	ASID1 This field indicates the ASID which the micro-TLB uses in the 2nd translation stage.
7 to 0	ASID0[7:0]	H'00	R/W	ASID0 This field indicates the ASID which the micro-TLB uses in the 1st translation stage.

13.2.16 MMU Performance Monitor Control Register (IMPFMMCTR)

This register is used to enable performance monitor function.

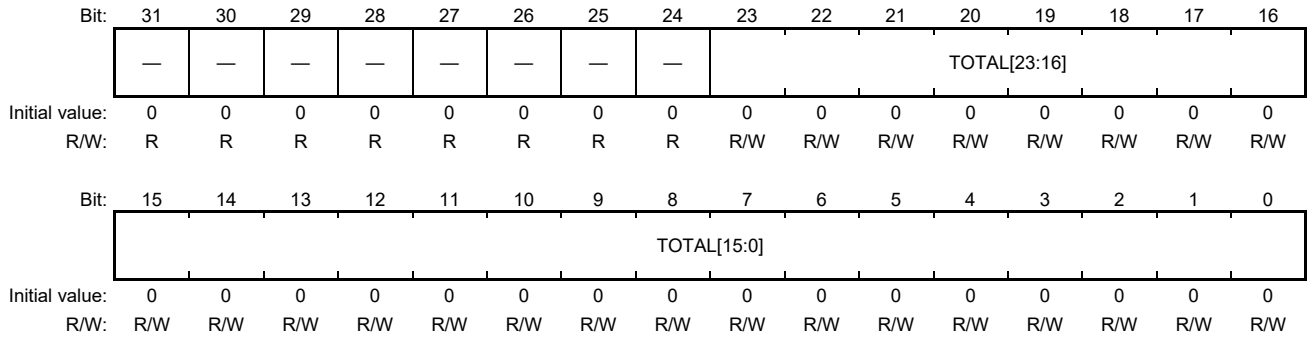
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MD[1:0]		—	—	SEL[1:0]		—	—	—	—	—	—	RST	EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	MD[1:0]	00	R/W	Monitor Mode 00: Monitor all 40-bit MMUs 01: Monitor all 32-bit MMUs 10: Reserved 11: Monitor only MMUn (specified by the SEL bits)
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	SEL[1:0]	00	R/W	When MD is B'11, SEL indicates the MMU table number to be monitored.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	RST	0	R/W	Reset all status and counter values. This bit is valid when EN = 1.
0	EN	0	R/W	Performance Monitor Enable 0: Stop to count 1: Start to count All counters stop and END is set to 1 when TOTAL bits get full.

13.2.17 MMU Performance Monitor Total Translation Counter (IMPFMMTOTAL)

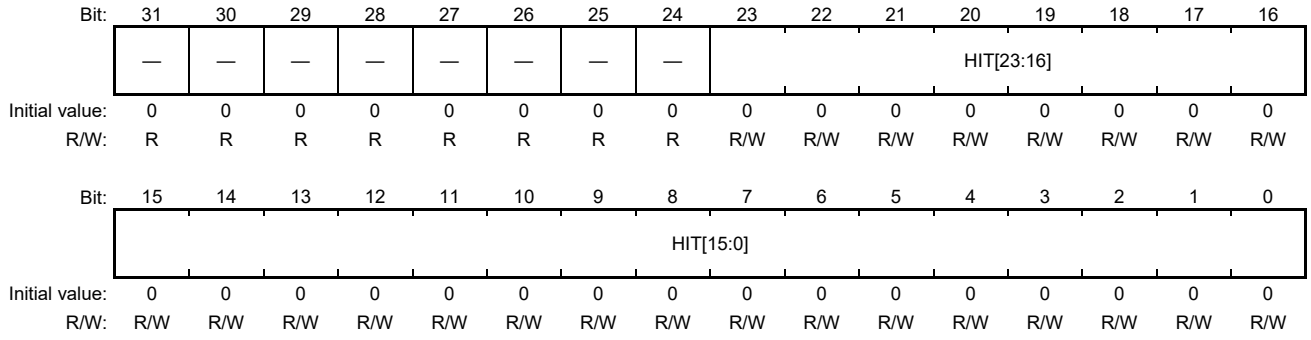
This register shows the total number of page table walk request when performance counter enabled.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	TOTAL[23:0]	H'00 0000	R/W	The total number of translation requests

13.2.18 MMU Performance Monitor Hit Counter (IMPFMHIT)

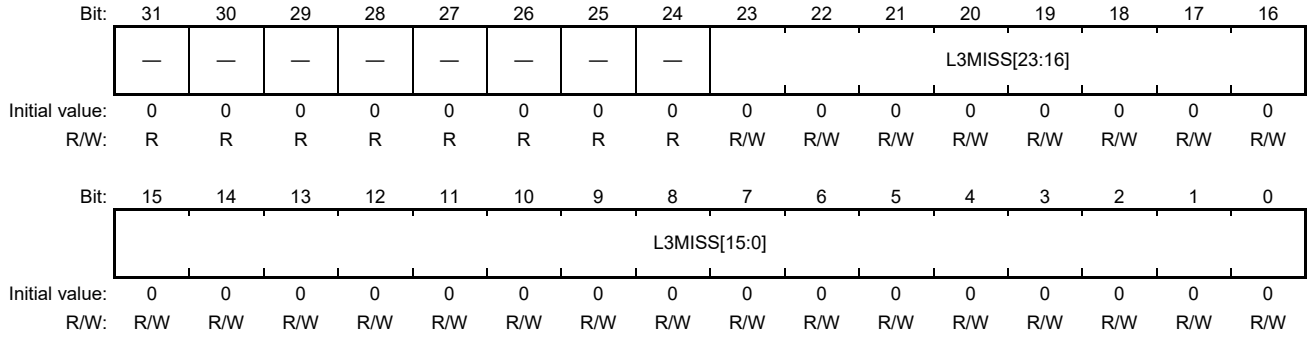
This register shows the total number of TLB hit when page table walk request received and performance monitor enabled.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	HIT[23:0]	H'00 0000	R/W	The total number of TLB hit requests = L3 TLB hit

13.2.19 MMU Performance Monitor L3 Miss Counter (IMPFML3MISS)

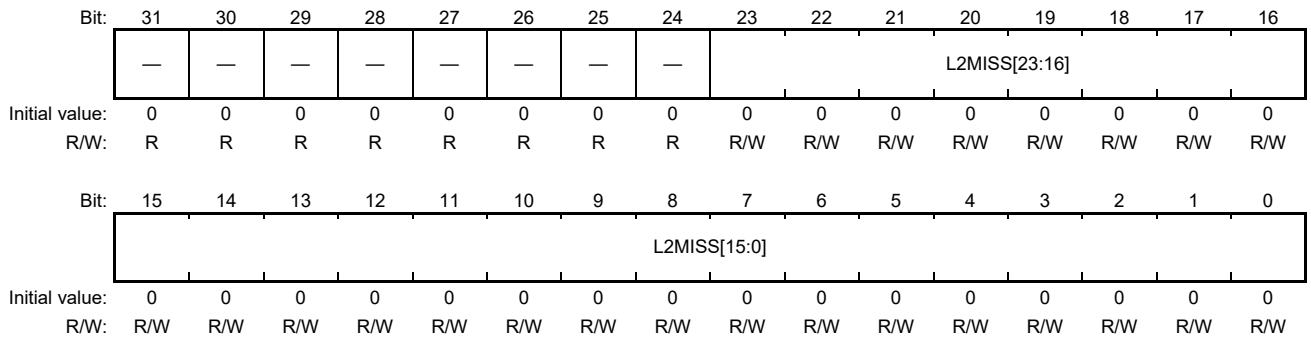
This register shows the total number of L3-TLB miss when page table walk request received and performance monitor enabled.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	L3MISS [23:0]	H'00 0000	R/W	The total number of L3 miss requests (not including L2 miss and L1 miss) = L2 TLB hit

13.2.20 MMU Performance Monitor L2 Miss Counter (IMPFML2MISS)

This register shows the total number of L2-TLB miss when page table walk request received and performance monitor enabled.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	L2MISS [23:0]	H'00 0000	R/W	The total number of L2 miss requests (not including L1 miss) = Page Table Walk

13.3 Operation

13.3.1 Address Translation Sequence in micro-TLBs

Each micro-TLB has independent entries and can translate from a virtual address to a physical address without sending translation requests to the IPMMU if the virtual address is cached in the micro-TLB.

When a translation error occurred in address translation, the micro-TLB blocks subsequent transactions until a valid page entry is registered. Set IMUCTRn.FLUSH = 1 after the entry registration.

Figure 13.2 shows the micro-TLB address translation sequence.

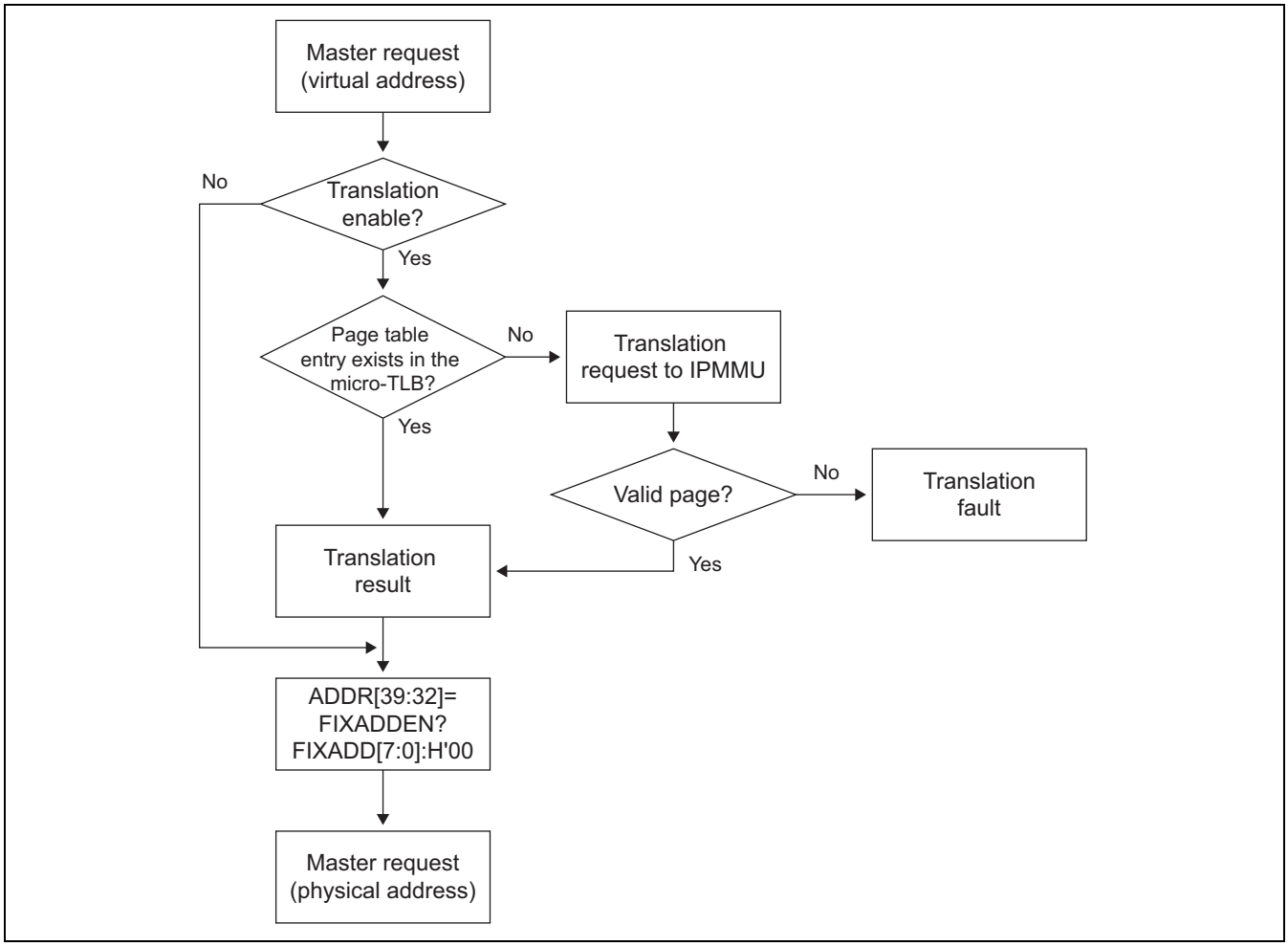


Figure 13.2 micro-TLB Address Translation Sequence

13.3.2 Address Translation Sequence in the IPMMU

(1) MMU Address Translation

The IPMMU has independent four non-secure page tables and four secure page tables which support two page table formats, the Short-descriptor format and the Long-descriptor format. When the IPMMU receives an address translation request from a micro-TLB, the IPMMU starts address translation sequence based on the page table specified by IMUCTRn.TTSEL.

Figure 13.3 shows the MMU address translation sequence.

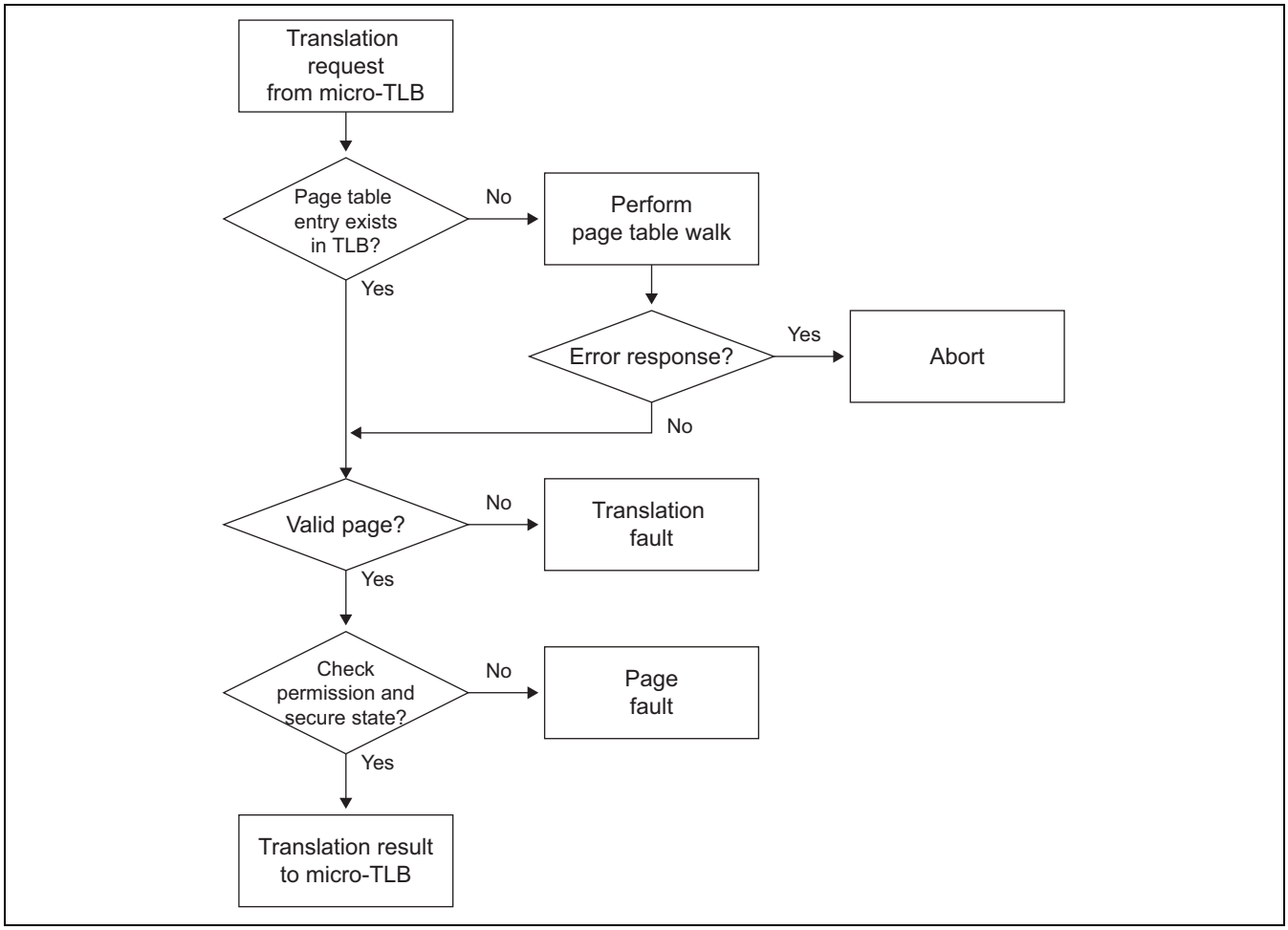


Figure 13.3 MMU Address Translation Sequence

(2) PMB Address Translation

PMB address translation is performed in two ways. When PMB address translation is chosen in IMUCTRn.TTSEL, all virtual addresses are translated by PMB. When PMB address translation is performed in a part of MMU translation (IMTTBCRn.PMB = 1), virtual addresses within H'80000000 to H'BFFFFFFF are translated to physical addresses by PMB.

Figure 13.4 shows the PMB translation flow.

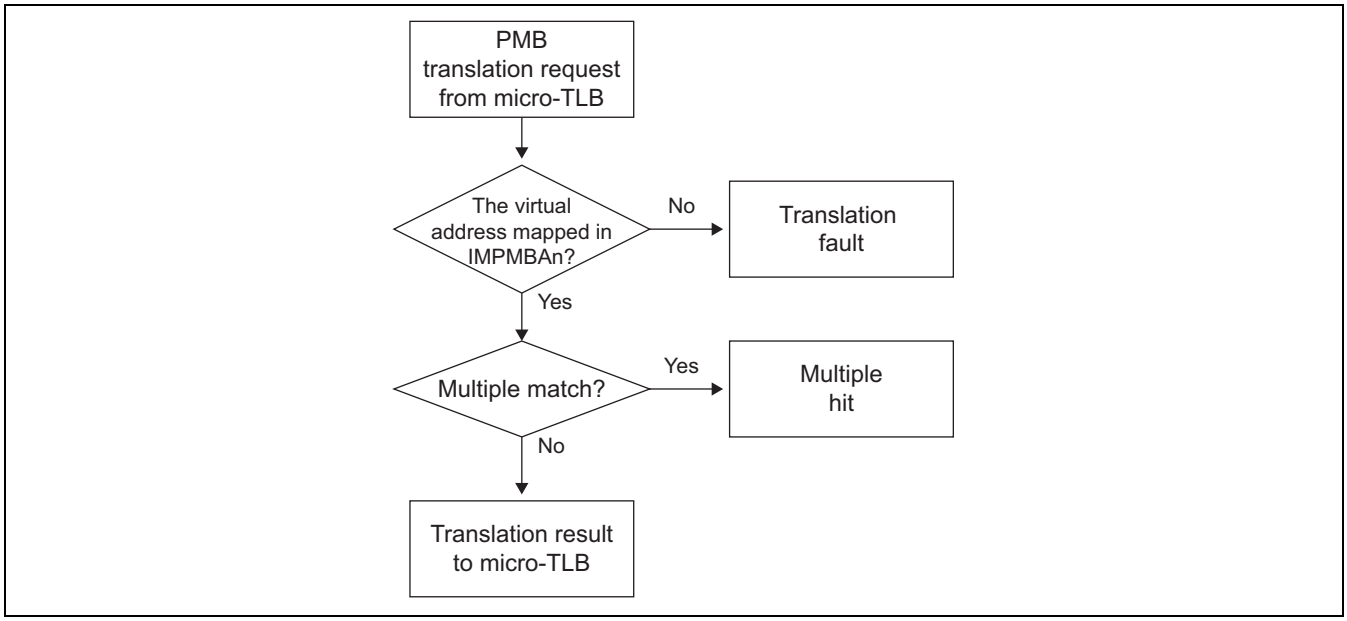


Figure 13.4 PMB Translation Flow

13.3.3 Address Space

(1) Short-descriptor

In the short-descriptor format, 32-bit virtual address space is translated to 32-bit physical address space managed by TTBR0/1. When IMTTBCRn.PMB = 1, translation address space is compatible with our previous products. In this mode, a virtual address within H'80000000 to H'BFFFFFFF is translated by PMB and a virtual address within H'C0000000 to H'FFFFFFFF is mapped to a physical address of the same value.

Note: IPMMU-GP doesn't support the Short-descriptor translation format.

Figure 13.5 shows the Short-descriptor address space.

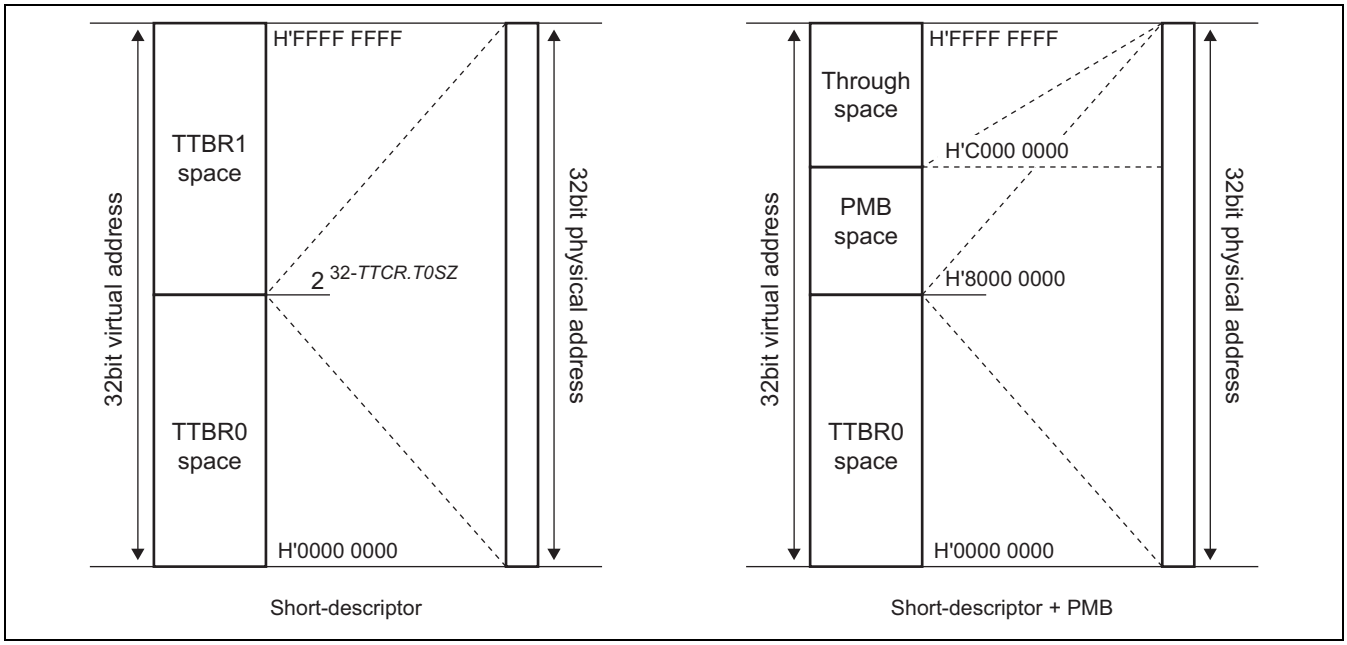


Figure 13.5 Short-descriptor Address Space

(2) Long-descriptor

In the long-descriptor format, 32-bit virtual address space is translated to 40-bit physical address space managed by TTBR0/1. The IPMMU supports the Secure PL1 and PL0 stage 1 translation and the Non-secure PL1 and PL0 stage 1 translation. The IPMMU doesn't support the Virtualization Extensions.

Figure 13.6 shows the Long-descriptor address space.

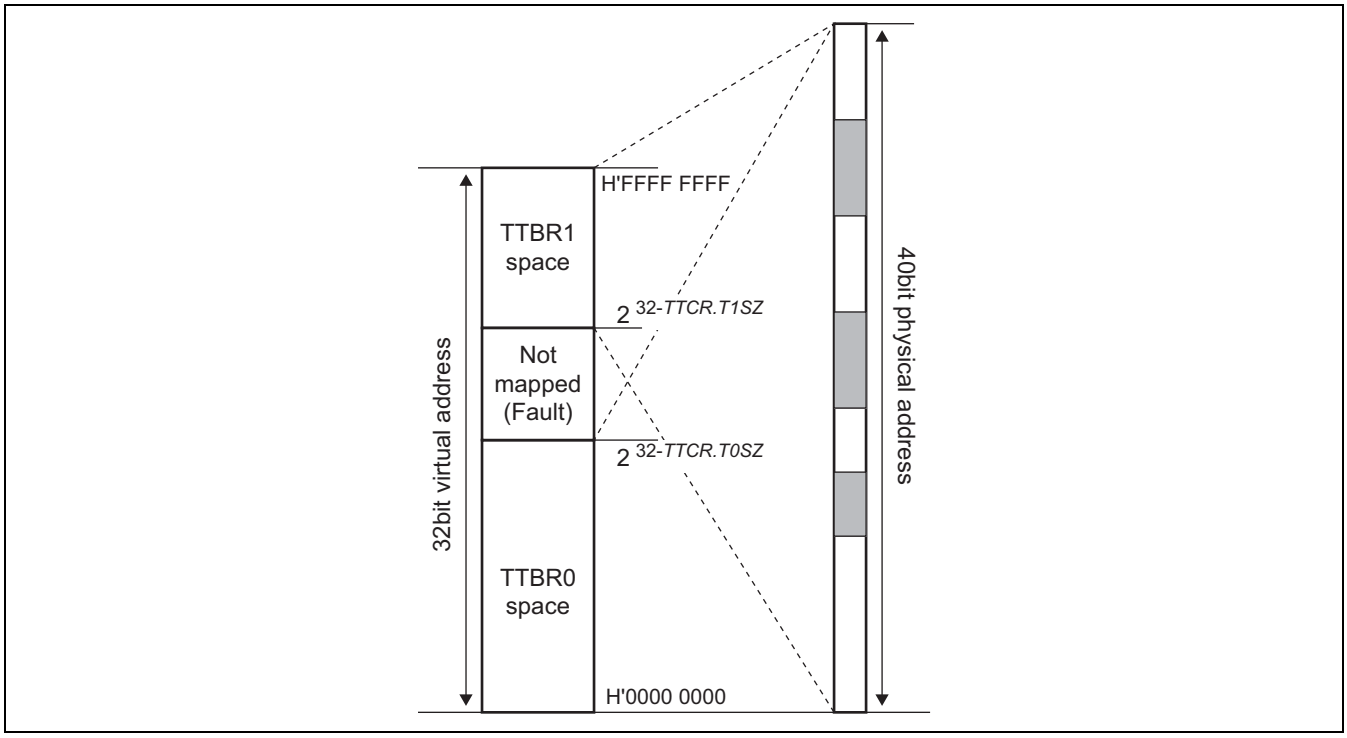


Figure 13.6 Long-descriptor Address Space

(3) PMB

The IPMMU supports the PMB address translation system. Figure 13.7 shows the PMB address space.

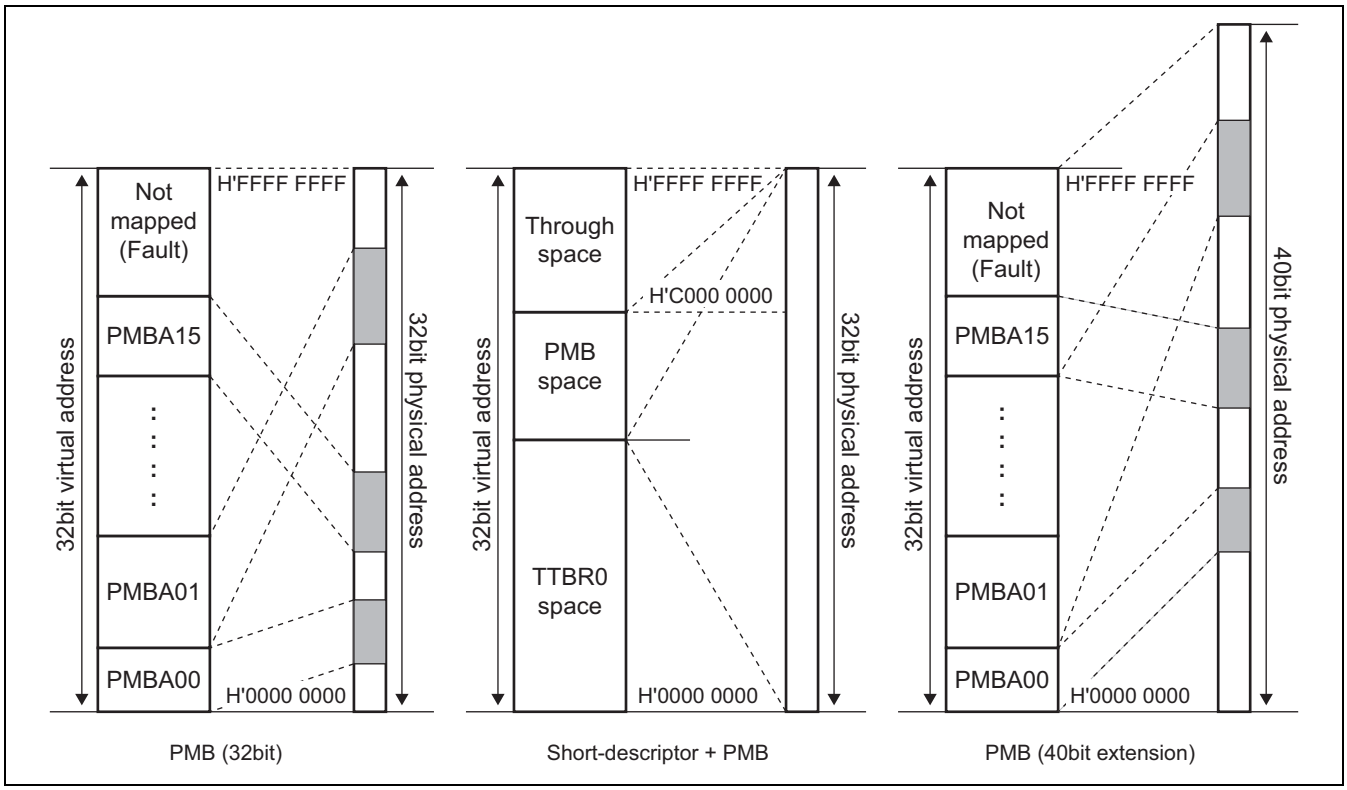


Figure 13.7 PMB Address Space

(4) 2-Stage Translation

The IPMMU supports 2-stage translation. At the 1st-stage, 32-bit address space is translated to 32-bit intermediate physical address (IPA) space. At the 2nd-stage, 32-bit IPA space is translated to 40-bit physical address space. In order to enable the 2-stage translation, set 1 to IMCTRn.TREN and set its 2nd-stage page table to IMCTRn.RTSEL.

Note: IPMMU-GP doesn't support the 2-stage translation.

Figure 13.8 shows the 2-stage translation address space.

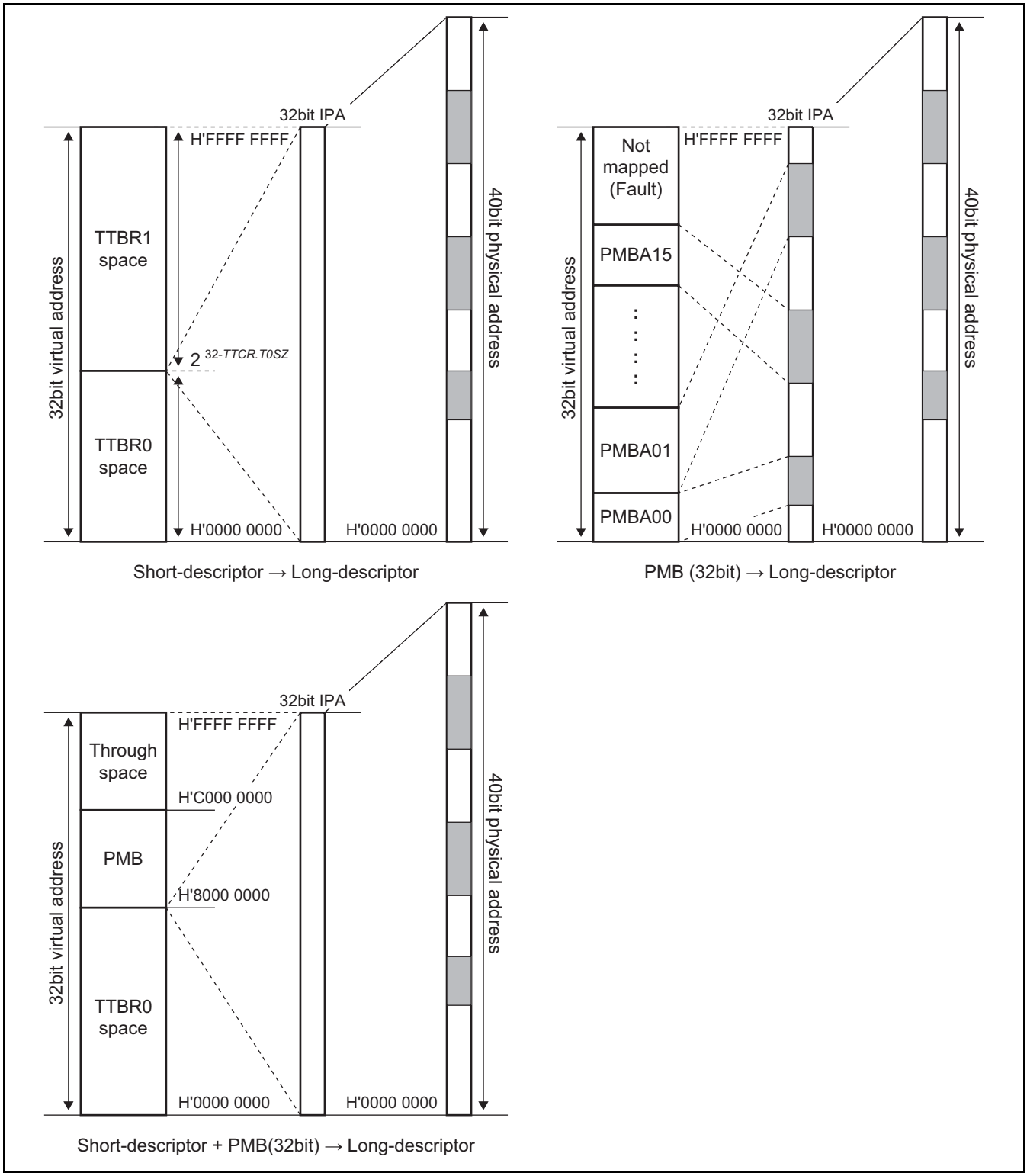


Figure 13.8 2-Stage Translation Address Space

13.3.4 Initialization Sequence

This section describes the initialization sequence of the IPMMU.

(1) Module Stop

The IPMMU doesn't support module stop control. The IPMMU can be used whenever a master requires address translation through the IPMMU. When a master doesn't require address translation, the corresponding IMUCTRn MMUEN must be disabled.

(2) micro-TLB

Before a master access, the corresponding micro-TLB registers which includes the translation mode and ASIDs must be configured.

13.3.5 TLB Maintenance

Some TLB maintenances between an IPMMU and the connected micro-TLBs are performed automatically by hardware.

Table 13.4 TLB Maintenance

Category	Software operation	TLB maintenance in IPMMU	TLB maintenance in micro-TLB
MMU Page Table	First entry registration	Not required	Not required
	Entry update	Invalidate the target TLB (IMCTRn.FLUSH = 1)	Automatically invalidated
	Entry release	Invalidate the target TLB (IMCTRn.FLUSH = 1)	Automatically invalidated
ASID	ASID update	Automatically invalidated	Automatically invalidated
MMU registers	MMU register values update	Invalidate the target TLB (IMCTRn.FLUSH = 1)	Automatically invalidated
PMB	PMB entry registration	Not required	Not required
	PMB entry update	Not required	Invalidate the target micro-TLB
	PMB entry release	Not required	Invalidate the target micro-TLB

13.3.6 Security Extensions

The IPMMU supports the ARMv7 Security Extensions and additional extensions.

(1) Banked Registers

The IPMMU has two copies of a register at the same address. They are banked with secure and non-secure. A Non-secure access can read and write only non-secure registers and a secure access can read and write secure registers. A secure access can also read and write non-secure registers through the alias address space to non-secure registers (from H'0800 to H'0FFF). Table 13.5 shows whether each IPMMU support the secure operation mode.

Table 13.5 Supported Secure Mode

IPMMU	Secure
IPMMUSY0	√
IPMMUSY1	√
IPMMUDS	√
IPMMUMP	√
IPMMUMX	√
IPMMUGP	√

(2) Address Translation

When a Secure master sends a translation request to an IPMMU through a micro-TLB, Secure MMU registers are referred to perform its page table walk. The Secure page table walk can read secure page table entries (NS = 0). In the case of a Non-secure translation request, Non-secure MMU registers are referred and the access to secure page table entries is ignored.

13.3.7 Error Handling

(1) IPMMU Interrupt Requests

Table 13.6 shows the error events which can cause interrupts. The errors in secure access are set in IMSSTRn registers and the errors in non-secure access are set in IMSTRn registers.

Table 13.6 IPMMU Error Events

Category	Error	Description
Long-descriptor Short-descriptor	Translation Fault	A virtual address was not mapped in the region defined by TTBR0 and TTBR1.*
		A descriptor was neither Table nor Block format
	Page Fault	AP (access permissions) / AF (access flag) bit mismatch occurred.
		NS bit mismatch occurred. Non-secure master read a Secure page table entry.
	Abort	The IPMMU got an error response from an Interconnect during a page table walk.
	Multiple Hit (MHIT)	Multiple TLB hits occurred.
PMB	Translation Fault	A virtual address was not mapped in IMPMBAn.
	Multiple Hit (MHIT)	Multiple PMB hits occurred.

Note: * This factor is only for long-descriptor.

(2) Error Handling Flow

When the micro-TLB cannot translate its virtual address because of some IPMMU errors, the micro-TLB stops to issue the following transactions. When the IPMMU detects an error, IMCTRn.FLUSH must be set after the IMSTRn/IMSSTRn register is cleared and page table entries are updated. After the TLB invalidation, the micro-TLB resumes to issue transactions.

Figure 13.9 shows the error handling flow.

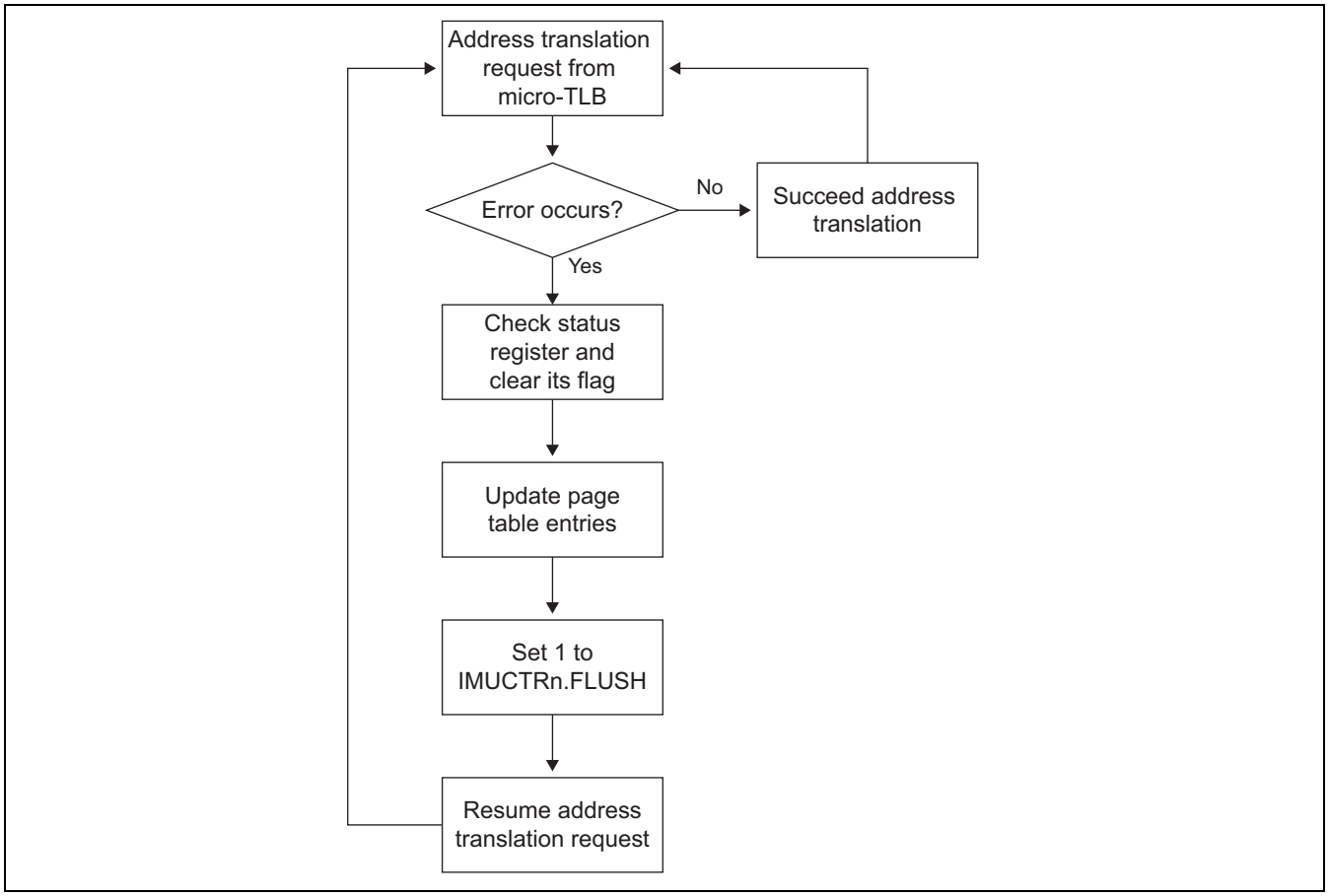


Figure 13.9 Error Handling Flow

13.4 micro-TLB Assignment

The assignment of micro-TLB.

13.4.1 micro-TLB Assignment

Table 13.7 micro-TLB Assignment in IPMMUSY0

micro-TLB	Master Module
00	Reserved
01	Reserved
02	Reserved
03	USB-DMAC (DDM ch.1)
04	Reserved
05	Reserved
06	Reserved
07	Reserved
08	SDHI
09	USB-DMAC (function1 ch.1)
10	Reserved
11	Reserved
12	LBSC

Table 13.8 micro-TLB Assignment in IPMMUSY1

micro-TLB	Master Module
00	USB-DMAC (function0 ch.0)
01	USB-DMAC (function0 ch.1)
02	Reserved
03	Reserved
04	USB-DMAC (function1 ch.0)
05	Reserved
06	USB2.0 HOST(EHCI/OHCI) ch.0
07	Reserved
08	Reserved
09	USB2.0 HOST(EHCI/OHCI) ch.1
10	Ethernet AVB
11	Ethernet MAC Controller
12	USB-DMAC (DDM ch.0)
13	Reserved

Table 13.9 micro-TLB Assignment in IPMMUDS

micro-TLB	Master Module
00	SYS-DMAC ch.0
01	SYS-DMAC ch.1
02	SYS-DMAC ch.2
03	SYS-DMAC ch.3
04	SYS-DMAC ch.4
05	SYS-DMAC ch.5
06	SYS-DMAC ch.6
07	SYS-DMAC ch.7
08	SYS-DMAC ch.8
09	SYS-DMAC ch.9
10	SYS-DMAC ch.10
11	SYS-DMAC ch.11
12	SYS-DMAC ch.12
13	SYS-DMAC ch.13
14	SYS-DMAC ch.14
15	SYS-DMAC ch.15
16	SYS-DMAC ch.16
17	SYS-DMAC ch.17
18	SYS-DMAC ch.18
19	SYS-DMAC ch.19
20	SYS-DMAC ch.20
21	SYS-DMAC ch.21
22	SYS-DMAC ch.22
23	SYS-DMAC ch.23
24	SYS-DMAC ch.24
25	SYS-DMAC ch.25
26	SYS-DMAC ch.26
27	SYS-DMAC ch.27
28	SYS-DMAC ch.28
29	SYS-DMAC ch.29
30	Reserved
31	Reserved

Table 13.10 micro-TLB Assignment in IPMMUMP

micro-TLB	Master Module
00	Reserved
01	Reserved
02	Reserved
03	Reserved
04	Audio-DMAC ch.0
05	Audio-DMAC ch.1
06	Audio-DMAC ch.2
07	Audio-DMAC ch.3
08	Audio-DMAC ch.4
09	Audio-DMAC ch.5
10	Audio-DMAC ch.6
11	Audio-DMAC ch.7
12	Audio-DMAC ch.8
13	Audio-DMAC ch.9
14	Audio-DMAC ch.10
15	Audio-DMAC ch.11
16	Audio-DMAC ch.12
17	Reserved
18	Reserved
19	Reserved
20	Reserved
21	Reserved
22	Reserved
23	Reserved
24	Reserved
25	Reserved
26	Reserved
27	Reserved
28	Reserved
29	Reserved

Table 13.11 micro-TLB Assignment in IPMMUMX

micro-TLB	Master Module
00	Reserved
01	Reserved
02	Reserved
03	2D-DMAC
04	VSP1-CTU (VSPS)
05	VSP1-CTU (VSPD) ch.0
06	Reserved
07	FDP1 ch.0
08	Reserved
09	Reserved
10	VSP1 (VSPS)
11	Reserved
12	Reserved
13	VSP1 (VSPD) ch.0
14	Reserved
15	DU0
16	Reserved
17	VCP3-CE ch.0
18	VCP3-VLC ch.0
19	VPC ch.0
20	Reserved
21	Reserved
22	Reserved
23	VIN ch.0/1

Table 13.12 micro-TLB Assignment in IPMMUGP

micro-TLB	Master Module
00	SGX531 master I/F
01	Reserved

14. LBSC within Bus Bridge

14.1 Overview

The LBSC performs bus arbitration and necessary interface conversion for the accesses from the CPU (AXI bus) and DMA accesses from LBSC-DMAC channels 0 to 2 and outputs them to the external buses. Further, for external bus access, various settings can be specified in the LBSC control registers for the selection of a connection interface type for each area on the external bus or for the adjustment of number of setup/hold cycles on addresses and chip select signals with respect to read/write enable signals. Thus, the LBSC configuration allows diversity in methodology for accessing various external devices that are assigned to their corresponding areas.

The frequency of the external bus clock CLKOUT signal is up to 65.0 MHz. The LBSC outputs bus signals in synchronization with the external bus clock.

14.2 Features

The key features of the LBSC include:

- Support for areas 0, 1
  - Each area is allocated to EX-BUS, and SRAM, or byte-control SRAM bus protocol can be selected.
  - Interface, bus size, and wait-cycle insertion can be controlled in each area.
  - Provides bus signals in synchronization with the CLKOUT signal (65.0 MHz).
- External DMA transfer (for details on DMAC, refer to section 17, LBSC-DMAC).
  - Three channels
  - Support of devices with the DACK signal
  - Support of edge-detection and level-detection external request signals
  - Synchronous/asynchronous DREQ and the polarity of DREQ, DACK, and DRACK can be inverted through register settings.
- SRAM interface
  - Wait-cycle insertion can be controlled through register settings.
  - Wait cycles can be inserted with the EX_WAIT pins.
  - Connectable bus size: 16 or 8 bits.
- Burst ROM interface (area 0 and CPU access only)
  - Wait-cycle insertion can be controlled through register settings.
  - Burst count can be specified through register settings (cases where this reaches an address branching point are automatically detected, after which the access is broken off).
  - Connectable bus size: 16 or 8 bits
- Byte-control SRAM interface (areas 1 only)
  - SRAM interface with byte control.
  - Wait-cycle insertion can be controlled through register settings.
  - Wait cycles can be inserted with the EX_WAIT pins.
  - Connectable bus size: 16 or 8 bits.
- Wait timeout
  - Wait timeout detection

    Detection time in ns = period in ns at EX-BUS operating frequency × (the time specified in the EX-BUS wait timeout base counter register (EXBCT) and EX-BUS wait timeout detection counter register (EXTCT))

14.3 Block Diagram

Figure 14.1 is a block diagram of the LBSC. Placed on the AXI bus, the LBSC outputs accesses from the CPU in sequence to an external bus according to the settings that are provided in internal registers of the LBSC. For the external bus EX-BUS, the SRAM bus protocol can be selected. In addition, the LBSC incorporates three LBSC-DMAC channels that control DMA transfers between an external bus and the DDR3-SDRAM. For details on the LBSC-DMAC, see the relevant section. Since the CPU and the LBSC-DMAC generate access contention for an external bus, the BSC uses an arbiter unit to arbitrate such access requests. The access request that was selected by means of arbitration is converted into an external bus waveform by the bus interface unit before being output. The LBSC has an external wait control input that controls the pulse width. When a request for access is received by an external device, the external device uses this to control the wait for a response to suit the situation at the time of access-request reception.

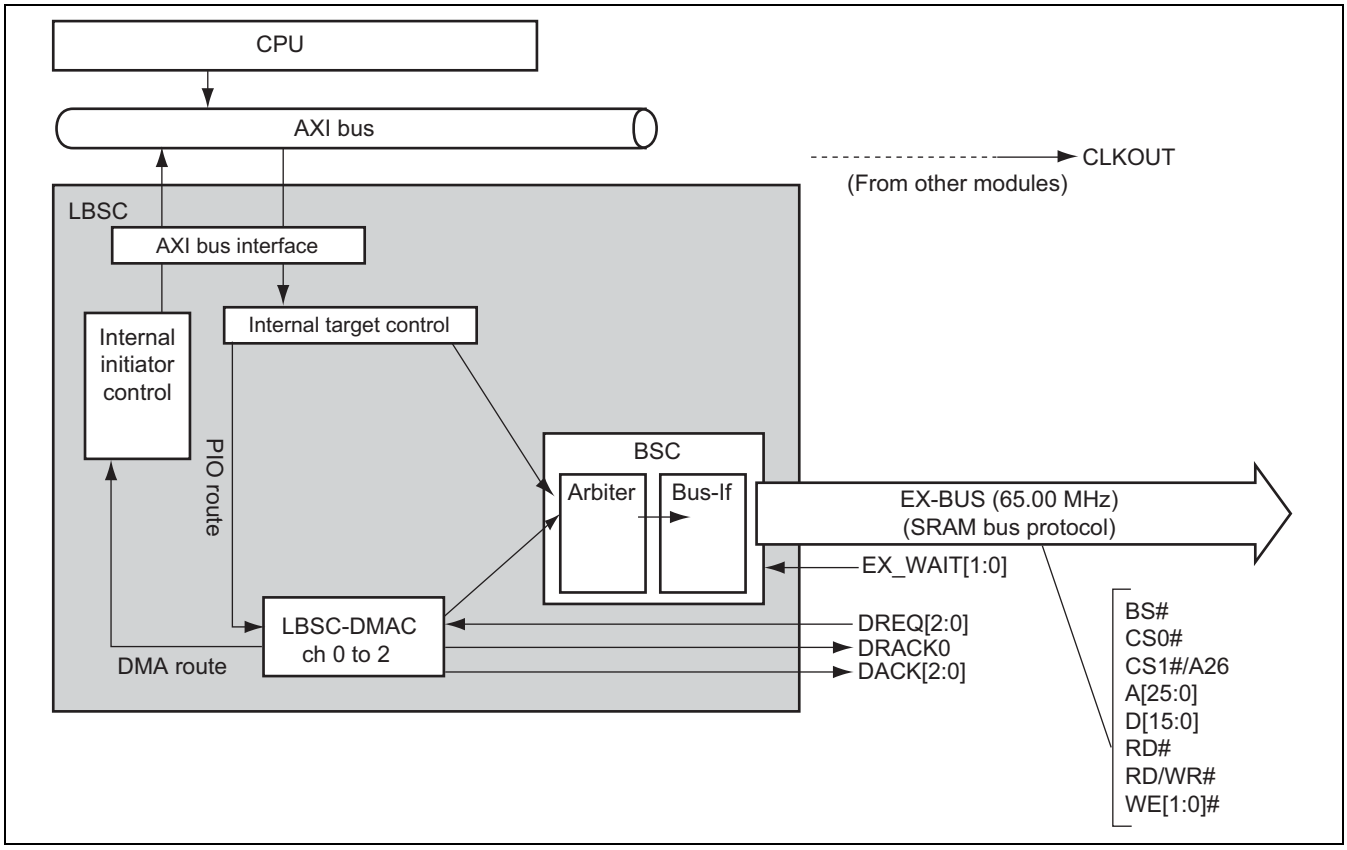


Figure 14.1 Block Diagram of LBSC

14.4 Input/Output Pins

The pin configuration of LBSC is shown in table 14.1. For detail, see section 5, Pin Function Controller (PFC).

Table 14.1 Pin Configuration

Name	Pin Name	I/O	Function
Address pin	DU0_DR0	O	Address bus A0
Address pin	DU0_DR1	O	Address bus A1
Address pin	DU0_DR2	O	Address bus A2
Address pin	DU0_DR3	O	Address bus A3
Address pin	DU0_DR4	O	Address bus A4
Address pin	DU0_DR5	O	Address bus A5
Address pin	DU0_DR6	O	Address bus A6
Address pin	DU0_DR7	O	Address bus A7
Address pin	DU0_DG0	O	Address bus A8
Address pin	DU0_DG1	O	Address bus A9
Address pin	DU0_DG2	O	Address bus A10
Address pin	DU0_DG3	O	Address bus A11
Address pin	DU0_DG4	O	Address bus A12
Address pin	DU0_DG5	O	Address bus A13
Address pin	DU0_DG6	O	Address bus A14
Address pin	DU0_DG7	O	Address bus A15
Address pin	DU0_DB0	O	Address bus A16
Address pin	DU0_DB1	O	Address bus A17
Address pin	DU0_DB2	O	Address bus A18
Address pin	DU0_DB3	O	Address bus A19
Address pin	DU0_DB4	O	Address bus A20
Address pin	DU0_DB5	O	Address bus A21
Address pin	DU0_DB6	O	Address bus A22
Address pin	DU0_DB7	O	Address bus A23
Address pin	DU0_DOTCLKIN	O	Address bus A24
Address pin	DU0_DOTCLKOUT0	O	Address bus A25
Data pins	D[15:0]	IO	Data bus pins D[15:0]
Chip select pin	QSPI0_IO2	O	Chip select CS0# signal for external memory or device.
Chip select pin	DU0_DOTCLKOUT1	O	Chip select CS1#/A26 signal for external memory or device.
Bus cycle start pin	QSPI0_MOSI/QSPI0_IO0	O	Bus cycle start (BS#) signal
DMA request pin	DU0_EXHSYNC/DU0_HSYNC	I	DMA request (DREQ0#)
DMA request pin	SSI_WS34	I	DMA request (DREQ1#)
DMA request pin	SSI_SDATA3	I	DMA request (DREQ2#)
DMA acknowledge pin	DU0_EXODDF/ DU0_ODDF_DISP_CDE	O	DMA request acknowledge (DRACK0)
DMA acknowledge pin	DU0_EXVSYNC/DU0_VSYNC	O	DMAC0 Acknowledge Signal (DACK0).
DMA acknowledge pin	SSI_SCK34	O	DMAC0 Acknowledge Signal (DACK1).
DMA acknowledge pin	SSI_SCK1_A	O	DMAC0 Acknowledge Signal (DACK2).

Name	Pin Name	I/O	Function
External wait pin	EX_WAIT0	I	External wait Signal 0 (EX_WAIT0).
External wait pin	SSI_SCK9_A	I	External wait Signal 1 (EX_WAIT1).
Data Enable pin	QSPI0_SPCLK	O	Data Enable 0 (WE0#)
Data Enable pin	QSPI0_SSL	O	Data Enable 1 (WE1#)
Read pin	QSPI0_IO3	O	Read data (RD#)
Read/Write pin	QSPI0_MISO/QSPI0_IO1	O	Read/Write direction (RD/RW#)
Clock output pin	CLKOUT	O	CLKOUT clock

14.5 LBSC Areas

14.5.1 LBSC Support Areas

Figure 14.2 shows LBSC response support areas from the CPU.

The basic configuration of the LBSC supports area 0 and area 1 as external spaces. For area 0 can be made into a 128-Mbyte space depending on the specific LSI startup mode (MD4 mode pin) in use (the MD4 mode pin = 1). In this case, however, area 1 is completely allocated as a space in area 0, and the CS1# signal is changed to the signal equivalent to A[26] in a bus address (addition of one bit to the address signal changes the capacity from 64 Mbytes to 128 Mbytes).

Registers of the BSC and LBSC-DMAC are provided in the internal register space of the LBSC.

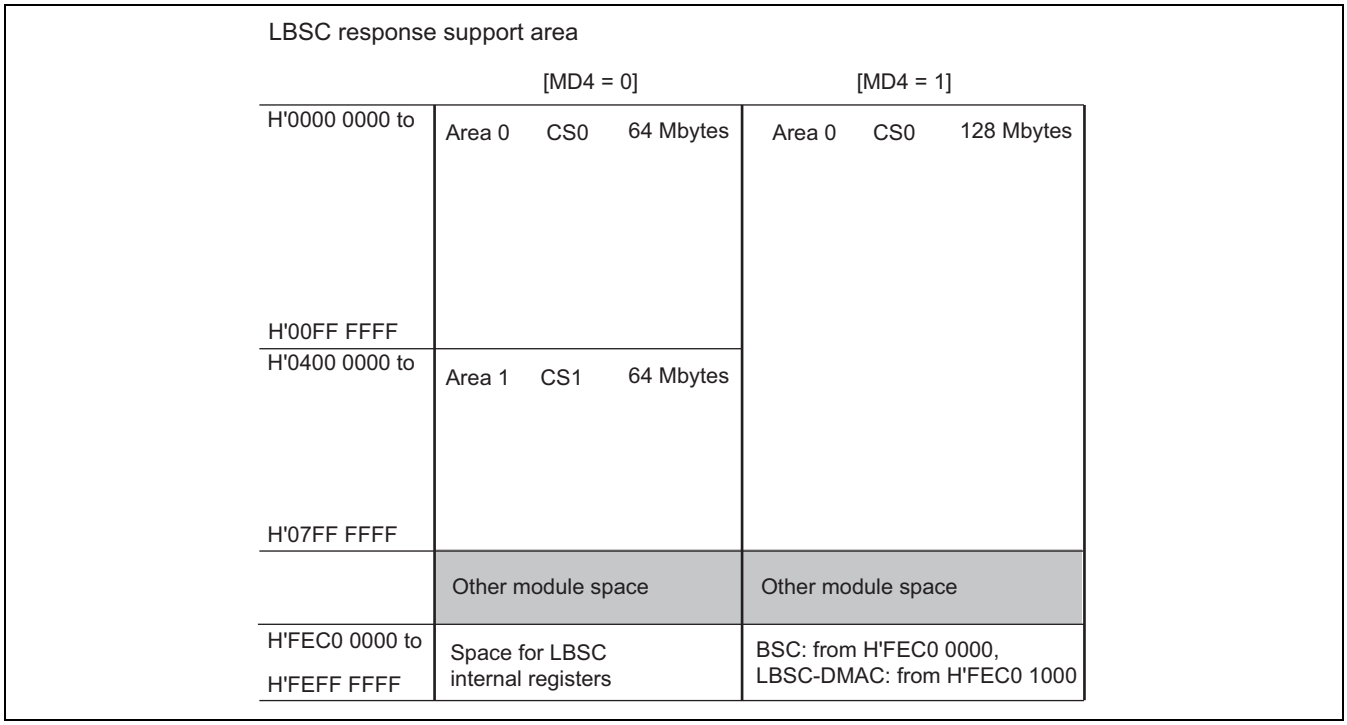


Figure 14.2 LBSC Response Support Areas from the CPU

14.5.2 Functionality Supported in Each Area

Table 14.2 lists the functions supported by the LBSC in each area on the EX-BUS.

Table 14.2 Functions Supported in Each Area on EX-BUS

Area	Bus	Capacity	Operating Mode	Guard interval	WAIT Function
0	8/16 bits	64/128 Mbytes selectable Area 0 divided MD4 pin specified	SRAM DMA Burst ROM	Disabled	Enabled
1	8/16 bits	Fixed to 64 Mbytes When area 0 = 128 Mbytes, no space exists.	SRAM DMA Byte-control SRAM	Enabled	Enabled

Notes: 1. The bus size for area 0 is specified with the LSI mode pins (MD8 = 0: 8 bits, MD8 = 1: 16 bits).
2. When using area 0 in 128-Mbyte mode (MD4 = 1), no space exists for area 1.
3. When accessing through EX-BUS, A[0] is output as byte address even if 16-bit bus is selected.
4. One DMAC channel cannot be allocated to two areas simultaneously.

14.6 Register Descriptions

The LBSC set registers to control the interface, bus size, RD/WE# signal pulse cycles, and setup and hold cycles for the CS# signal with respect to the RD/WE# signal, for each of externally connected devices. Table 14.3 lists registers of the LBSC. Note that correct operation is not guaranteed in principle if each register is modified during external bus access (for register modification in other cases, refer to the note under specific register description).

Table 14.3 LBSC Register Configuration

Register Name	Abbreviation	Access Type	Value after Power-On Reset	Address	Access Size	Remarks
Area 0 control register	CS0CTRL	R/W	Undefined	H'FEC0 0200	32	
Area 1 control register	CS1CTRL	R/W	H'0000 0020	H'FEC0 0204	32	
Area 0 RD/WE pulse control register	CSWCR0	R/W	H'FF70 FF70	H'FEC0 0230	32	
Area 1 RD/WE pulse control register	CSWCR1	R/W	H'FF70 FF70	H'FEC0 0234	32	
LBSC-DMAC channel y RD/WE pulse control register	EXDMAWCRy	R/W	H'FF70 FF70	H'FEC0 0250 to H'FEC0 0258	32	y = 0 to 2
Area 0 external wait control register	CSPWCR0	R/W	H'0000 0000	H'FEC0 0280	32	
Area 1 external wait control register	CSPWCR1	R/W	H'0000 0000	H'FEC0 0284	32	
External wait input control register	EXWTSYNC	R/W	H'0000 0000	H'FEC0 02A0	32	
Area 0 burst control register	CS0BSTCTL	R/W	H'0000 0000	H'FEC0 02B0	32	
Area 0 burst pitch set register	CS0BTPH	R/W	H'0000 00F7	H'FEC0 02B4	32	
Area 1 guard setting register	CS1GDST	R/W	H'0000 0000	H'FEC0 02C0	32	
LBSC-DMAC channel y area allocation register	EXDMASETy	R/W	H'0000 0000	H'FEC0 02F0 to H'FEC0 02F8	32	y = 0 to 2
LBSC-DMAC channel y control register	EXDMCRy	R/W	H'0000 0000	H'FEC0 0310 to H'FEC0 0318	32	y = 0 to 2
BSC interrupt source status register	BCINTSR	R	H'0000 0000	H'FEC0 0330	32	
BSC interrupt source clear register	BCINTCR	—/WC1	H'0000 0000	H'FEC0 0334	32	
BSC interrupt enable register	BCINTMR	R/W	H'0000 0000	H'FEC0 0338	32	
EX-BUS priority level set register	EXBATLV	R/W	H'0000 0000	H'FEC0 0340	32	
External wait status register	EXWTSTS	R	Undefined	H'FEC0 0344	32	
EX-BUS wait timeout detection base counter register	EXBCT	R/W	H'0000 0000	H'FEC0 03C0	32	
EX-BUS wait timeout detection counter register	EXTCT	R/W	H'0000 0000	H'FEC0 03C4	32	

Register Name	Abbreviation	Access Type	Value after Power-On Reset	Address	Access Size	Remarks
EX-BUS wait timeout detection access source indication register	EXTSR	R/WC1	H'0000 0000	H'FEC0 0010	32	
EX-BUS wait timeout detection address indication register	EXTADR	R/W	H'0000 0000	H'FEC0 0014	32	

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

[Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

R: Read-only. The write value should always be 0.

—/W: Write-only. The read value is undefined.

—/WC1: Write-only. Writing 1 initializes the bit. Writing 0 is ignored.

14.6.1 Area 0 Control Register (CS0CTRL)

Function: CS0CTRL specifies the interface in area 0 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	128B	—	—	CS0SZ		—	—	CS0IF	
Initial value:	1	0	0	0	0	0	0	—	0	0	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	128B	—	R	Area 0 Capacity Indication (These bits indicate the value specified by the LSI mode pin MD4.) 0: 64 Mbytes 1: 128 Mbytes
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	CS0SZ	—	R	Area 0 Bus Size Indication (These bits indicate the value specified by the LSI mode pin MD8.) 00: Setting prohibited 01: 8 bits 10: 16 bits 11: Setting prohibited
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CS0IF	00	R/W	Area 0 Interface Selection 00: Standard (SRAM) 01: Burst ROM 10: Setting prohibited 11: Setting prohibited

Notes: 1. Even when the burst ROM interface is selected by setting CS0IF = B'01, burst ROM operation is not available unless appropriate setting is made in CS0BSTCTL. Be sure to specify both CS0BSTCTL and CS0BTPH before using the burst ROM interface.

2. Setting of burst ROM is valid for CPU access only. For DMA transfer access to area 0, SRAM interface (enabled when EXDMAWCR/CSPWCR0 is valid) is usually selected.

14.6.2 Area 1 Control Register (CS1CTRL)

Function: CS1CTRL specifies the interface in area 1 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CS1SZ		—	CS1BRM	CS1IF	
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R/W	Reserved This bit is always read as 0. The write value should always be 0.
15 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	CS1SZ	10	R/W	Area 1 Bus Size Selection 00: Setting prohibited 01: 8 bits 10: 16 bits 11: Setting prohibited
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CS1BRM	0	R/W	Area 1 Byte-Control SRAM Mode Selection (valid only when CS1IF = 01) 0: Same cycle as CS# 1: Same cycle as RD#
1, 0	CS1IF	00	R/W	Area 1 Interface Selection 00: Standard (SRAM) 01: Byte-control SRAM 10: Setting prohibited 11: Setting prohibited

14.6.3 Area 0 RD/WE Pulse Control Register (CSWCR0)

Function: CSWCR0 specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to area 0 (EX-BUS). (The settings for read access are ignored when the burst ROM interface is selected.)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE# pulse cycles during writing to area 0. 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during writing to area 0. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during writing to area 0. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	—	0000	R	These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during reading from area 0. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during reading from area 0. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	—	0	R	These bits are always read as 0. The write value should always be 0.

Notes: 1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.

Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.

Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.

2. When controlling wait insertion through LSI external pins (EX_WAIT1 to EX_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
3. When the burst ROM interface is specified for area 0, the read access-related settings for area 0 in this register is ignored and settings in CS0BTPH are enabled.
4. DMA transfer access is performed according to the settings in the RD/WE pulse control register (EXDMAWCRy (y = 0 to 2)) for the respective LBSC-DMAC channel.
5. For details, refer to section 14.7.1, SRAM Interface (Basic Functionality).

14.6.4 Area 1 RD/WE Pulse Control Register (CSWCR1)

Function: CSWCR1 specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to area 1 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE pulse cycles during writing to area 0. 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during writing to area 1. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during writing to area 1. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	—	0000	R	These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during reading from area 1. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during reading from area 1. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	—	0000	R	These bits are always read as 0. The write value should always be 0.

Notes: 1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.
Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.
Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.
2. When controlling wait insertion through LSI external pins (EX_WAIT1 to EX_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
3. DMA transfer access to area 1 is performed according to the settings in the RD/WE pulse control register (EXDMAWCRy (y = 0 to 2)) for the respective LBSC-DMAC channel.
4. For details, refer to section 14.7.1, SRAM Interface (Basic Functionality).

14.6.5 LBSC-DMAC Channel y RD/WE Pulse Control Register (EXDMAWCRy (y = 0 to 2))

Function: EXDMAWCRy specifies the RD/WE# pulse cycles and setup and hold cycles for the CS# signal and address during access to EX-BUS in LBSC-DMAC channel y (y = 0 to 2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	WRITE PULSE CYCLE					WRITE CS SETUP CYCLE			—	WRITE CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	READ PULSE CYCLE					READ CS SETUP CYCLE			—	READ CS HOLD CYCLE			—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	1	1	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	WRITE PULSE CYCLE	11111	R/W	These bits specify the WE# pulse cycles during writing to area 0. 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
26 to 24	WRITE CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the WE# signal during write in channel y. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 20	WRITE CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the WE# signal during write in channel y. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
19 to 16	—	0000	R	These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	READ PULSE CYCLE	11111	R/W	These bits specify the RD# pulse cycles during reading from area 0. 00000: Setting prohibited 00001: 1-cycle pulse 00010: 2-cycle pulse 00011: 3-cycle pulse 00100: 4-cycle pulse : 11101: 29-cycle pulse 11110: 30-cycle pulse 11111: 31-cycle pulse
10 to 8	READ CS SETUP CYCLE	111	R/W	These bits specify the CS# and address setup cycles with respect to the RD# signal during read in channel y. 000: 0 cycle for setup period 001: 1 cycle for setup period 010: 2 cycles for setup period : 110: 6 cycles for setup period 111: 7 cycles for setup period
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	READ CS HOLD CYCLE	111	R/W	These bits specify the CS# and address hold cycles with respect to the RD# signal during read in channel y. 000: 0 cycle for hold period 001: 1 cycle for hold period 010: 2 cycles for hold period : 110: 6 cycles for hold period 111: 7 cycles for hold period
3 to 0	—	0000	R	These bits are always read as 0. The write value should always be 0.

Notes: 1. A minimum of two clock cycles are required for one EX-BUS access cycle and therefore, the setting must satisfy this lower limit.
Setting less than two clock cycles for one access cycle is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.
Example: When CSSetupCycle = B'000, CSHoldCycle = B'000, and PulseCycle = B'00001, correct operation is not guaranteed.
2. When controlling wait insertion through LSI external pins (EX_WAIT1 to EX_WAIT0), set PulseCycle to B'00010 or a larger value. If B'00001 or a smaller value is specified, wait insertion through an external pin is disabled.
3. External wait insertion is controlled according to the external wait control register for the area where the DMAC channel (0 to 2) is assigned.
4. For details, refer to section 14.7.3, LBSC-DMAC → DMA Interface.

14.6.6 Area 0 External Wait Control Register (CSPWCR0)

Function: CSPWCR0 makes settings for external wait signal during access to area 0 (EX-BUS) (the settings are ignored when the burst ROM interface is selected).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	V	RB	WINV	—	EXWT1	EXWT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	V	0	R/W	Area 0 External Wait Signal Enable/Disable 0: Disabled 1: Enabled
4	RB	0	R/W	Area 0 READY/BUSY Logic Selection 0: BUSY logic 1: READY logic
3	WINV	0	R/W	Area 0 External Wait Signal Polarity 0: Does not invert the polarity of the area 0 external wait signal. 1: Inverts the polarity of the area 0 external wait signal.
2	—	0	R	The write value must always be 0. Operation is not guaranteed if setting 1.
1	EXWT1	0	R/W	Area 0 EX_WAIT1 Enable 0: Disables EX_WAIT1 for area 0. 1: Enables EX_WAIT1 for area 0.
0	EXWT0	0	R/W	Area 0 EX_WAIT0 Enable 0: Disables EX_WAIT0 for area 0. 1: Enables EX_WAIT0 for area 0.

Notes: 1. When this register setting is made valid (bit V = 1), any one of bits EXWT0 to EXWT1 must be set to 1. Simultaneously setting more than one of EXWT0 to EXWT1 to 1 is not expected in the design of this LSI, and attempted correct operation is not guaranteed.

2. When bit V = 0, the settings in EXWT0 to EXWT1 are ignored. In area 0, this register setting is ignored in read access when the burst ROM interface is selected. For details on wait control, refer to section 14.7.1, SRAM Interface (Basic Functionality).

14.6.7 Area 1 External Wait Control Register (CSPWCR1)

Function: CSPWCR1 makes settings for external wait input pins during access to area 1 (EX-BUS).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	V	RB	WINV	—	EXWT1	EXWT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	V	0	R/W	Area 1 External Wait Signal Enable/Disable 0: Disabled 1: Enabled
4	RB	0	R/W	Area 1 READY/BUSY Logic Selection 0: BUSY logic 1: READY logic
3	WINV	0	R/W	Area 1 External Wait Signal Polarity 0: Does not invert the polarity of the area 1 external wait signal. 1: Inverts the polarity of the area 1 external wait signal.
2	—	0	R	The write value must always be 0. Operation is not guaranteed if setting 1.
1	EXWT1	0	R/W	Area 1 EX_WAIT1 Enable 0: Disables EX_WAIT1 for area 1. 1: Enables EX_WAIT1 for area 1.
0	EXWT0	0	R/W	Area 1 EX_WAIT0 Enable 0: Disables EX_WAIT0 for area 1. 1: Enables EX_WAIT0 for area 1.

Notes: 1. When this register setting is made valid (bit V = 1), any one of bits EXWT0 to EXWT1 must be set to 1. Simultaneously setting more than one of EXWT0 to EXWT1 to 1 is not expected in the design of this LSI, and attempted correct operation is not guaranteed.

2. When bit V = 0, the settings in EXWT0 to EXWT1 are ignored. For details on wait control, refer to section 14.7.1, SRAM Interface (Basic Functionality).

14.6.8 External Wait Input Control Register (EXWTSYNC)

Function: EXWTSYNC controls whether or not to synchronize the external wait pins (EX_WAIT1 to EXWAIT0).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWT SYNC1	EXWT SYNC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	—	0	R/W	Reserved The write value should always be 0.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	—	0	R	The write value must always be 0. Operation is not guaranteed if setting 1.
1	EXWTSYNC1	0	R/W	0: Does not synchronize EX_WAIT1 (the original EX_WAIT1 is synchronous with CLKOUT). 1: Synchronizes EX_WAIT1 (the original EX_WAIT1 is asynchronous with CLKOUT).
0	EXWTSYNC0	0	R/W	0: Does not synchronize EX_WAIT0 (the original EX_WAIT0 is synchronous with CLKOUT). 1: Synchronizes EX_WAIT0 (the original EX_WAIT0 is asynchronous with CLKOUT).

Note: For details on wait control, refer to section 14.7.1, SRAM Interface (Basic Functionality).

14.6.9 Area 0 Burst Control Register (CS0BSTCTL)

Function: CS0BSTCTL specifies the burst length for area 0 when the burst ROM interface is selected.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	A0BST[2:0]			—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 11	A0BST[2:0]	000	R/W	Area 0 Burst Length for Burst ROM Interface 001: 4 access cycles 010: 8 access cycles 011: 16 access cycles 100: 32 access cycles Others: No burst transfer
10 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Notes: 1. This register is valid only when the burst ROM interface is selected (CS0IF = B'01 in CS0CTRL).
2. Set bits A0BST2 to A0BST0 to an appropriate value so that (area 0 bus size) × (burst length set in this register) becomes 32 bytes or less.
3. For details, refer to section 14.7.2, CPU (AXI Bus) → Burst ROM Interface.

14.6.10 Area 0 Burst Pitch Set Register (CS0BTPH)

Function: CS0BTPH specifies the burst pitches for the first access cycle and the second and later cycles for area 0 when the burst ROM interface is selected.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	A0H	A0W[3:0]				—	A0B[2:0]		
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	A0H	0	R/W	Specifies the CS# and address hold cycles with respect to the RD# signal for area 0 in the burst ROM interface. 0: 0 cycle for hold period 1: 1 cycle for hold period
7 to 4	A0W[3:0]	1111	R/W	These bits specify the burst pitch (wait cycles to be inserted) after the first burst cycle for area 0 in the burst ROM interface. 0000: Setting prohibited 0001: Setting prohibited 0010: 2 cycles 0011: 3 cycles 0100: 4 cycles : 1101: 13 cycles 1110: 14 cycles 1111: 15 cycles
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	A0B[2:0]	111	R/W	These bits specify the burst pitch (wait cycles to be inserted) after the second burst cycle for area 0 in the burst ROM interface. 000: Setting prohibited 001: 1 cycle 010: 2 cycles : 110: 6 cycles 111: 7 cycles

Notes: 1. Be sure to specify this register before specifying CS0BSTCTL.
2. For details, refer to section 14.7.2, CPU (AXI Bus) → Burst ROM Interface.

14.6.11 Area 1 Guard Setting Register (CS1GDST)

Function: CS1GDST specifies the guard interval (period of access prohibition) between sequential access cycles in area 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CS1GD	TIMER_SET			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CS1GD	0	R/W	0: Makes the TIMER_SET setting invalid. 1: Makes the TIMER_SET setting valid.
3 to 0	TIMER_SET	0000	R/W	Guard Interval (Period of Access Prohibition) between Sequential Access Cycles for Area 1 0000: 0 clock cycle 0001: 1 clock cycle 0010: 2 clock cycles 0011: 3 clock cycles 0100: 4 clock cycles : 1101: 13 clock cycles 1110: 14 clock cycles 1111: 15 clock cycles

Notes: 1. The TIMER_SET setting is ignored when CS1GD = 0.
2. This register must not be dynamically modified regardless of whether area 1 is being accessed.
3. The actual guard interval between sequential access cycles on the EX-BUS is (register setting) + (idle cycles due to hardware processing and EX-BUS arbitration).
4. For details, refer to section 14.7.1 (4), Controlling Guard Intervals.

14.6.12 LBSC-DMAC Channel y Area Assignment Register (EXDMASETy (y = 0 to 2))

Function: EXDMASETy specifies the area where LBSC-DMAC channel y is assigned (y = 0 to 2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMyCS1	DMyCS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	DMyCS1	0	R/W	0: Does not assign LBSC-DMAC channel y to area 1. 1: Assigns LBSC-DMAC channel y to area 1.
0	DMyCS0	0	R/W	0: Does not assign LBSC-DMAC channel y to area 0. 1: Assigns LBSC-DMAC channel y to area 0.

Notes: 1. Setting more than one bit to 1 in this register is prohibited. Such a setting is not expected in the design of this LSI, and if attempted correct operation is not guaranteed.
2. Be sure to specify this register before starting LBSC-DMAC access. If an LBSC-DMAC channel starts access before specifying this register, correct operation is not guaranteed (such access is not expected in the design of this LSI).
3. When CS0 area is used as a 128-Mbyte space, DMAC channel must not be assigned to CS1 area.
4. For details, refer to section 14.7.3, LBSC-DMAC → DMA Interface.

14.6.13 LBSC-DMAC Channel y Control Register (EXDMCRy (y = 0 to 2))

Function: EXDMCRy specifies conversion of DREQ[y], DACK[y], and DRACK[0] in the area where LBSC-DMAC channel y is assigned.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRST	—	DSTS	DBST	—	EXQL	EXDY	EXDS	—	—	EXRS	EXRL	—	EXAL	DAKCTL	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	DRST	0	W	DACK Signal Forcible Negation (Enabled when DBST = 1) 0: Writing 0 is ignored. 1: Forcibly negates the DACK signal being continuously asserted for 1 CLKOUT cycle
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	DSTS	0	R	DACK Signal Assert State Indication 0: The DACK signal is not currently asserted. 1: The DACK signal is currently asserted.
12	DBST	0	R/W	Specifies whether or not to continuously assert the DACK signal if DREQ is continuously asserted during the intervals between DMA bus transfers 0: Negates DACK after each bus transfer. 1: Continuously asserts DACK even during the intervals between bus transfers if DREQ is continuously asserted. (When negation of DREQ is detected, DACK is also negated.)
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	EXQL	0	R/W	0: Receives DREQ[y] signal at a low level. 1: Receives DREQ[y] signal at a high level.
9	EXDY	0	R/W	0: Does not synchronize the DREQ[y] signal. 1: Synchronizes the DREQ[y] signal.
8	EXDS	0	R/W	0: Detects DREQ[y] signal at a level. 1: Detects DREQ[y] signal at an edge.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	EXRS	0	R/W	0: Asserts DRACK[0] one clock cycle before CS#/DACK[0] is asserted. 1: Asserts DRACK[0] two clock cycles before CS#/DACK[0] is asserted.

Bit	Bit Name	Initial Value	R/W	Description
4	EXRL	0	R/W	0: Outputs DRACK[0] as a high-active signal. 1: Outputs DRACK[0] as a low-active signal.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	EXAL	0	R/W	0: Outputs DACK[y] as a high-active signal. 1: Outputs DACK[y] as a low-active signal.
1, 0	DAKCTL	00	R/W	Signals asserted for area where LBSC-DMAC channel y is assigned 00 and 11: Asserts the CS# signal and DACK[y] signal together for the area. 01: Asserts only the CS# signal for the area. 10: Asserts only the DACK[y] signal for the area.

Notes: 1. This register except for DRST bit must not be dynamically modified regardless of whether the respective area is being accessed.
2. The EXRL and EXRS settings are valid only for LBSC-DMAC channel 0 (DRACK[0]). LBSC-DMAC channels 1 and 2 do not have the DRACK signal.
3. For details on the DMA interface, refer to section 14.7.3, LBSC-DMAC → DMA Interface.

14.6.14 BSC Interrupt Source Status Register (BCINTSR)

Function: BCINTSR indicates the status of the BSC interrupt source.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWTE	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EXWTE	0	R	EX-BUS Wait Timeout Error Status 0: The EX-BUS is working correctly. 1: An EX-BUS timeout error has occurred. (A timeout error occurs when an EX-BUS clock (CLKOUT) cycle of EXBCT and EXTCT setting values have elapsed.)
0	—	0	R	This bit is always read as 0. The write value should always be 0.

14.6.15 BSC Interrupt Source Clear Register (BCINTCR)

Function: BCINTCR clears the state of the BSC interrupt indicator.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWTEC	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	–/WC1	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EXWTEC	0	–/WC1	EX-BUS Wait Timeout Error Status Clear 0: Writing 0 is ignored. 1: Clears the EX-BUS wait timeout error state.
0	—	0	R	The write value should always be 0.

Note: This register is always read as 0.

14.6.16 BSC Interrupt Enable Register (BCINTMR)

Function: BCINTMR enables or disables the BSC interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWTEM	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	EXWTEM	0	R/W	EX-BUS Wait Timeout Error Interrupt Enable 0: Disables output of an interrupt signal for this interrupt source. 1: Enables output of an interrupt signal for this interrupt source.
0	—	0	R	The write value must always be 0. Operation is not guaranteed if setting 1.

14.6.17 EX-BUS Priority Level Set Register (EXBATLV)

Function: Specifies the priority levels for EX-BUS arbitration.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EX-BLV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	EX-BLV	0	R/W	Priority Level Setting for EX-BUS Arbitration (Access Selection) 0: Higher priority: PIO (AXI access) Lower priority: LBSC-DMAC 1: Higher priority: LBSC-DMAC Lower priority: PIO (AXI access)

Notes: 1. EX-BLV sets a fixed priority between PIO and LBSC-DMAC.
2. This register must not be dynamically modified except for initial setting.
3. For details on external bus arbitration, refer to section 14.7.6, EX-BUS Arbitration.

14.6.18 External Wait Status Register (EXWTSTS)

Function: EXWTSTS indicates the state of the external wait pins EX_WAITn (n = 0, 1).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXWT1 STS	EXWT0 STS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	—	—	R	This bit is always read as 0. The write value should always be 0.
1	EXWT1STS	—	R	Indicates the EX_WAIT1 pin state.
0	EXWT0STS	—	R	Indicates the EX_WAIT0 pin state.

14.6.19 EX-BUS Wait Timeout Detection Base Counter Register (EXBCT)

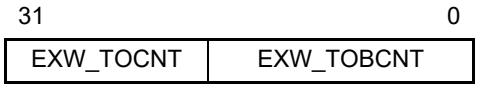
Function: EXBCT specifies the lower-order part of the value for counting to detect a timeout in waiting for access to the EX-BUS, which is monitored through pins EX_WAIT0, EX_WAIT1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EXWB_KEY								—	—	—	—	EXW_TOBCNT			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EXW_TOBCNT															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	EXWB_KEY	H'00	W	EX-BUS Wait Timeout Detection Base Counter Register Write Key For writing to this register to be effective, the value H’5A must be written to these bits. Values read from these bits are meaningless.
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 0	EXW_TOBCNT	H'0 0000	R/W	EX-BUS Wait Timeout Counter Setting Maximum value: H’0 0000 Minimum value: H’0 0001

Note: Counting to detect a timeout in waiting for access to the EX-BUS is handled by a 32-bit counter, which is formed by the EXW_TOBCNT bits in the EXBCT register and the EXW_TOCNT bits in the EXTCT register as shown below.



14.6.20 EX-BUS Wait Timeout Detection Counter Register (EXTCT)

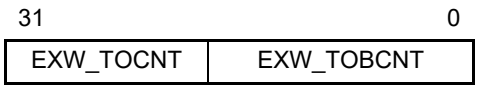
Function: EXTCT specifies the higher-order part of the value for counting to detect a timeout in waiting for access to the EX-BUS, which is monitored through pins EX_WAIT0, EX_WAIT1 and enables or disables the detection.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EXWB_KEY								—	—	—	—	—	—	—	EXW_TOEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	EXW_TOCNT											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	EXWB_KEY	H'00	W	EX-BUS Wait Timeout Detection Counter Register Write Key For writing to this register to be effective, the value H’5A must be written to these bits. Values read from these bits are meaningless.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	EXW_TOEN	0	R/W	EX-BUS Wait Timeout Enable 0: Timeout in waiting for access to the EX-BUS has not been detected. 1: Timeout in waiting for access to the EX-BUS has been detected.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	EXW_TOCNT	H'000	R/W	EX-BUS Wait Timeout Counter Setting Maximum value: H’000 Minimum value: H’001

Note: Counting to detect a timeout in waiting for access to the EX-BUS is handled by a 32-bit counter, which is formed by the EXW_TOBCNT bits in the EXBCT register and the EXW_TOCNT bits in the EXTCT register as shown below.



14.6.21 EX-BUS Wait Timeout Detection Access Source Indication Register (EXTSR)

Function: EXTSR indicates the source of attempted access to the EX-BUS that reached timeout as detected through the EX_WAIT0, EX_WAIT1 pins.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	EXW_TOSHW
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	EXW_TODC2	EXW_TODC1	EXW_TODC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	EXW_TOSHW	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS from the AXI bus. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	EXW_TODC2	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS by channel 2 of the LBSC-DMAC. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.
1	EXW_TODC1	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS by channel 1 of the LBSC-DMAC. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.
0	EXW_TODC0	0	R/WC1	Indication of timeout in waiting for access to the EX-BUS by channel 0 of the LBSC-DMAC. 0: Timeout has not been reached. 1: Timeout has been reached. To clear this bit, write 1 to it.

14.6.22 EX-BUS Wait Timeout Detection Address Indication Register (EXTADR)

Function: EXTADR indicates the address at which access to the EX-BUS was attempted but timeout was detected through pins EX_WAIT0, EX_WAIT1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EXW_TOADR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EXW_TOADR															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EXW_TOADR	H'0000 0000	R/W	Indication of the address for which attempted access to the EX-BUS by the AXI bus reached timeout

Notes: 1. This register is readable and writable. To clear this register, write 0s to all bits.
2. This register only indicates the address to which access was attempted if this was from the AXI bus (i.e. addresses are not indicated if access was attempted from the LBSC-DMAC).

14.7 Operation

14.7.1 SRAM Interface (Basic Functionality)

The BSC reads access requests from the CPU stored in the FIFO mounted in the LBSC module and writes them to the EX-BUS. By default, all spaces, areas 0 and 1 are all set for SRAM interface. The pulse width for access signals in this SRAM access interface can be varied according to register settings. Thus, the SRAM interface has functionality for easily accommodating devices with various access specifications, connected on the EX-BUS. In addition, to support low-speed external devices, the guard-interval control functionality is provided for insertion of the appropriate interval for each bus access; and the SRAM interface receives wait-for-response requests (or access complete signals) from external devices on a synchronous/asynchronous-selectable and polarity-selectable basis, thus ensuring flexibility in bus design. Figures 14.3 and 14.4 show SRAM interface timing charts for AXI → EX-BUS conversions.

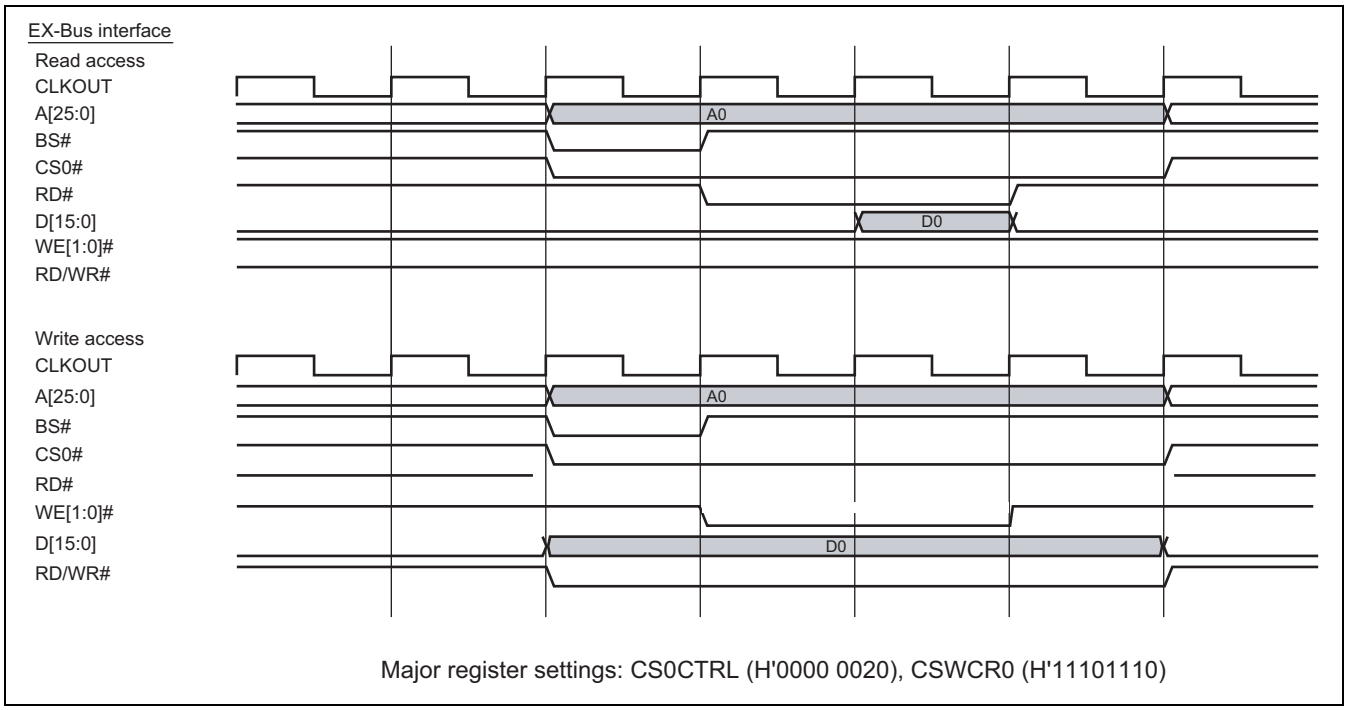


Figure 14.3 Basic Timing Chart for Access from AXI to SRAM (Area 0)

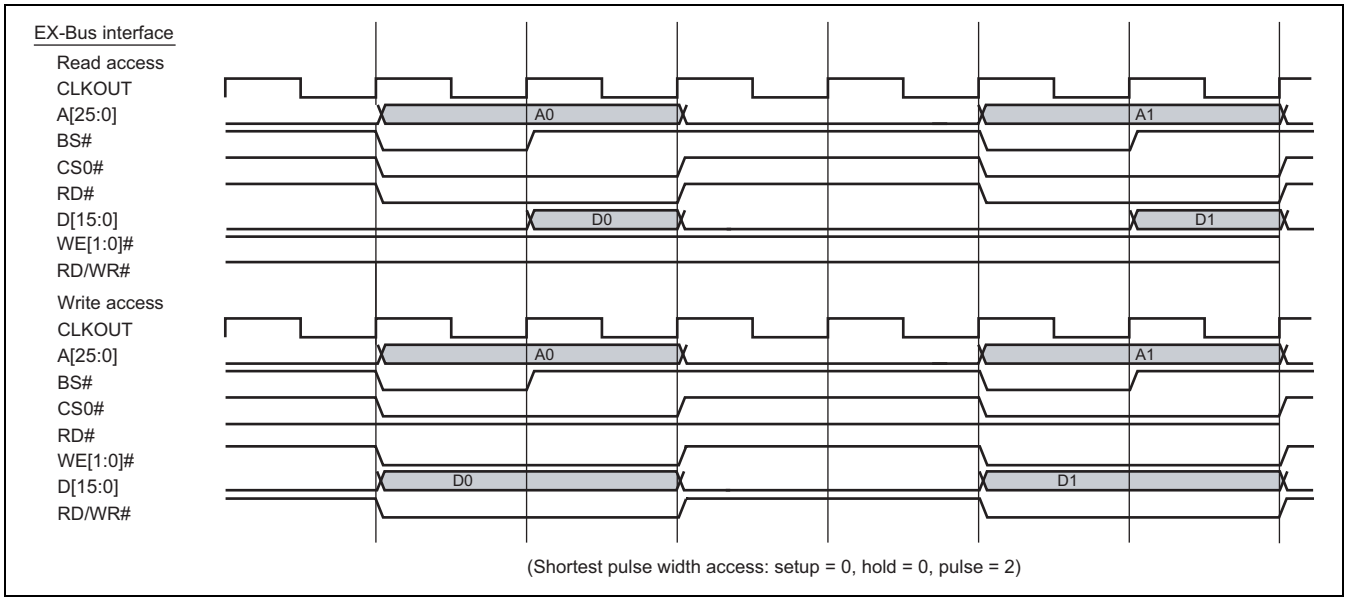


Figure 14.4 Basic Timing Chart for Access from AXI to SRAM (Shortest Pulse Width × Shortest PIO Consecutive Accesses)

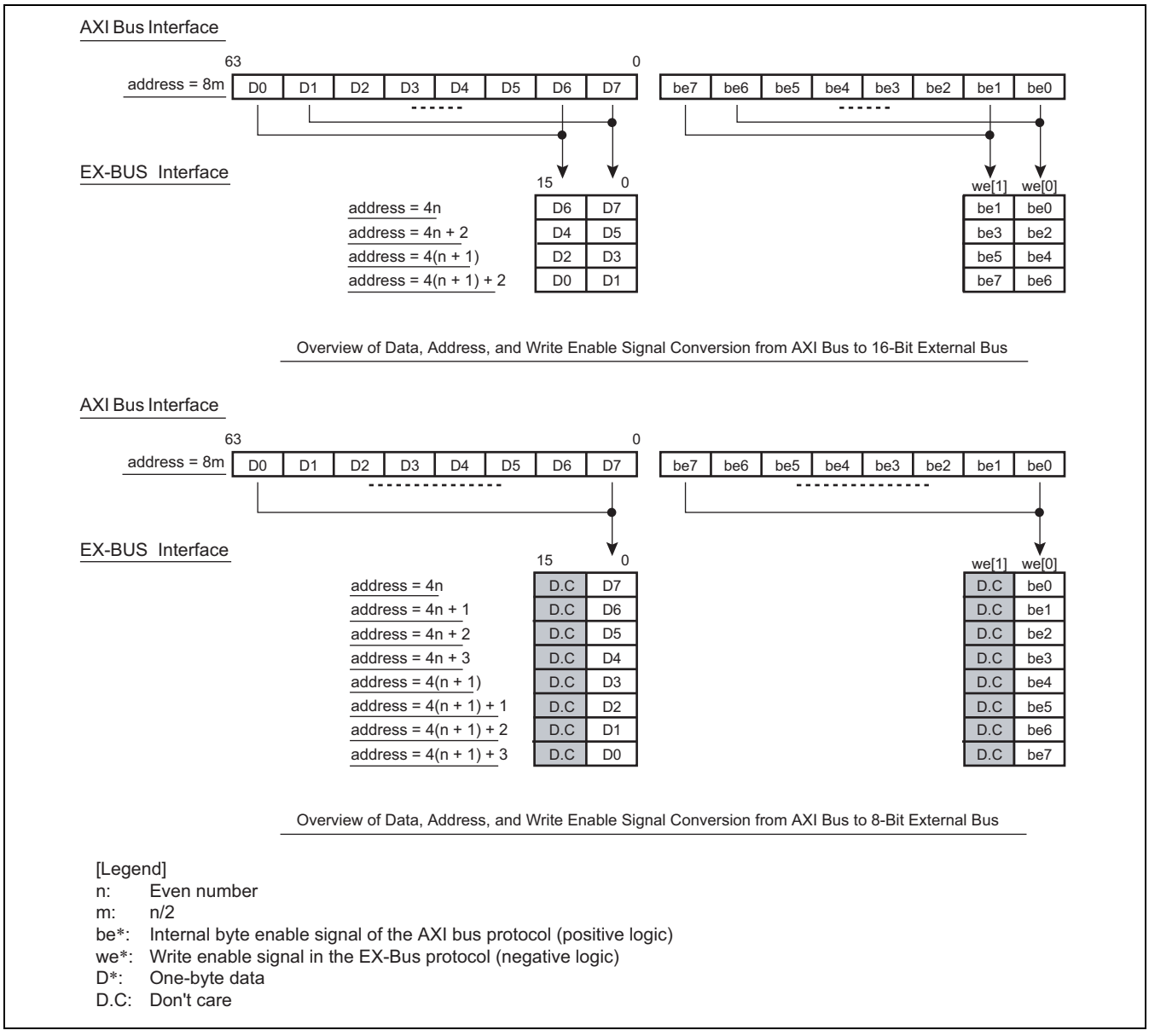
Figure 14.4 is an example of the basic SRAM interface waveform with the shortest pulse width, wherein the same waveform occurs twice in succession.

If consecutive PIO access requests are made from the CPU (AXI bus), the access interval will be 2 clock cycles, as indicated in the above waveforms, regardless of whether the preceding or succeeding access request is for the same area or for different areas. If a switching occurs, such as PIO → DMA or DMA → PIO, however, the access interval will be 1 clock cycle.

The access interval can be extended by means of the guard setting registers.

(1) Address Generation/Alignment

When making access to the EX-BUS as an SRAM interface, the LBSC generates addresses and performs data alignment conversions. Figure 14.5 provides an overview of address generation and data alignment/write enable conversions.



[Legend]
n: Even number
m: n/2
be*: Internal byte enable signal of the AXI bus protocol (positive logic)
we*: Write enable signal in the EX-Bus protocol (negative logic)
D*: One-byte data
D.C: Don't care

Figure 14.5 Overview of Data, Address, and Write Enable Signal Conversion from CPU (64-Bit AXI Bus) to External Bus

(2) Setting the Pulse Width for an Access Signal

When making access to the EX-BUS, the LBSC can set the setup or hold time for addresses, RD/WR#, and CS# signals based on WE# signals and RD# signals, and the pulse width for WE# and RD# signals in units of clock cycles, according to the values that are set for each area by means of the CSWCR0, CSWCR1 registers. (During a burst ROM read operation, however, the LBSC conforms to CS0BTPH settings rather than CSWCR0 settings. Similarly, during a DMA operation, it conforms to EXDMAWCR0 to EXDMAWCR2 settings rather than CSWCR0, CSWCR1 settings.) The pulse width for WE# or RD# signal that is stored in a register can be extended by an externally supplied EX_WAIT signal. The minimum total value that is set should be two clock cycles.

(3) External Wait Control

The LBSC controls the external wait signal (EX_WAIT) from a device connected to the EX-BUS based on settings that are provided on external wait control registers (CSPWCR0, CSPWCR1) and the external wait input control register (EXWTSYNC). The external wait control registers permit the selection of the four types of interfaces to accommodate various types of specifications, whether the wait signal input from an external device is based on the READY logic (posting a READY status) or BUSY logic (posting a BUSY status), or which signal polarity is in effect.

Figure 14.6 shows waveforms for the four wait signal patterns that can be input and the waveforms for the wait signals internal to the LBSC after conversion according to the register settings.

The external wait input control register allows the switching between the synchronous/asynchronous handling of external wait input signals. The default is to treat such signals on a synchronous basis. Figure 14.7 shows external wait input timings for synchronization/asynchronization. In the figure, the position indicated by the symbol * represents the point at which the LBSC determines whether or not external wait is in effect. Specifically, for synchronization, the position is one clock cycle before the point at which the WE# and RD# signals would normally be negated by pulse width settings. If external wait is in effect at this position, the pulse width for the WE# or RD# signal continues to extend until the wait status becomes the ready status. If the pulse width for the WE# or RD# signal is extended by the EX_WAIT signal, the address and the RD/WR# and CS# signals are negated when the hold time is satisfied. If the synchronization setting is switched to the asynchronization setting, any external wait is nullified unless there is an external wait two clock cycles before the * position, or three clock cycles before the point in which the WE# and RD# signals would normally be negated.

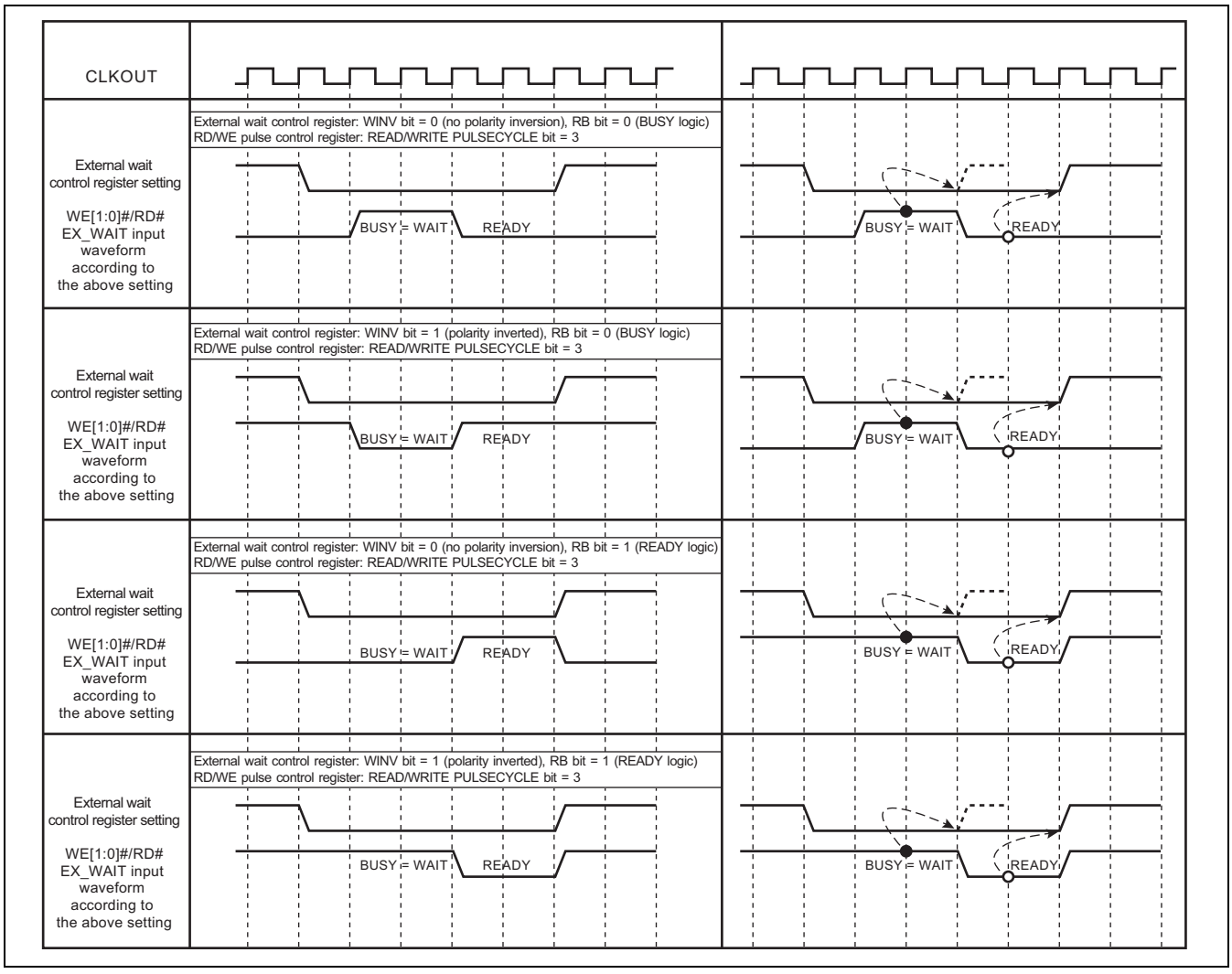


Figure 14.6 Waveforms of Converted External Wait Interface

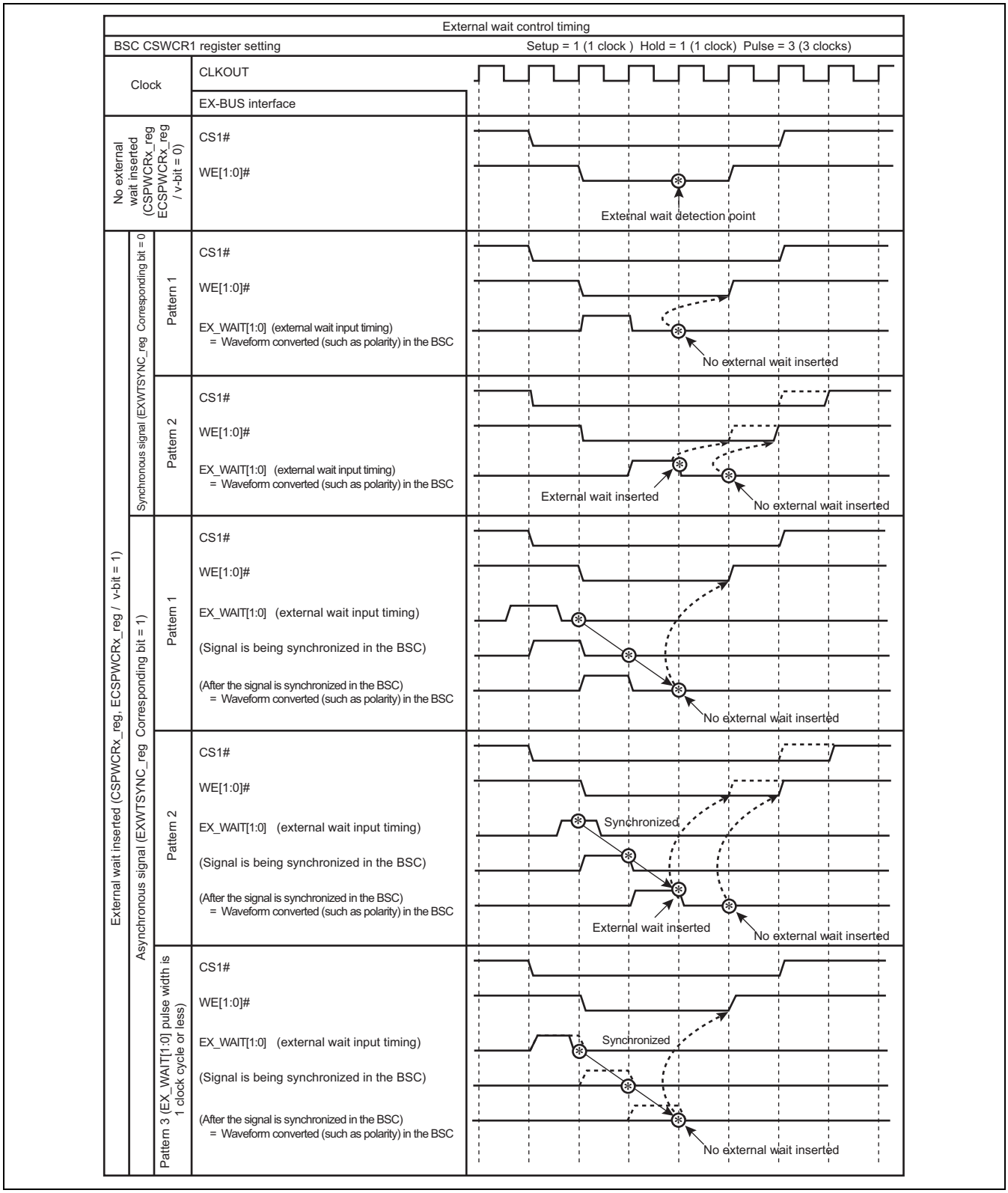


Figure 14.7 Waveforms of External Wait Input Signals

(4) Controlling Guard Intervals

For some external devices, the transition of the data lines to the high-Z state after completion of read access takes a relatively long time. To prevent any contention for the data bus when further access over the EX-BUS proceeds immediately after a read operation for such a device, the LBSC supports a function to guard against further access over a given interval following each bus access. The function is also effective for external devices that have difficulty coping with consecutive reception of access requests. Specifically, set the number of clock cycles over which guarding against access applies in the guard setting register (CS1GDST) for the given area. (Even if the value assigned to the guard setting register is 0, hardware processing before a further bus access request is issued requires at least 2 clock cycles between PIO and PIO, and at least 1 clock cycle between PIO and DMA. Therefore, in PIO accesses, the actual interval on the EX-BUS is 2 clock cycles when value in the guard setting register is 0 or 1. And it is 1 clock cycles plus the setting for number of clock cycles in the guard setting register when the setting value is 2 or more.)

After access to a given area, the guard interval is assigned corresponding to the register for that area, regardless of the kind of access or target space of the next access request. Note, however, that there is no guard setting register for area 0. Therefore, guard intervals are not set up for access that immediately follows access to this area. Since area 0 is supposed to be for the connection of general-purpose memory such as ROM, SRAM, or flash-ROM, guard intervals should not be necessary for this area. Figure 14.8 is a basic timing chart to illustrate the concept of guard-interval control.

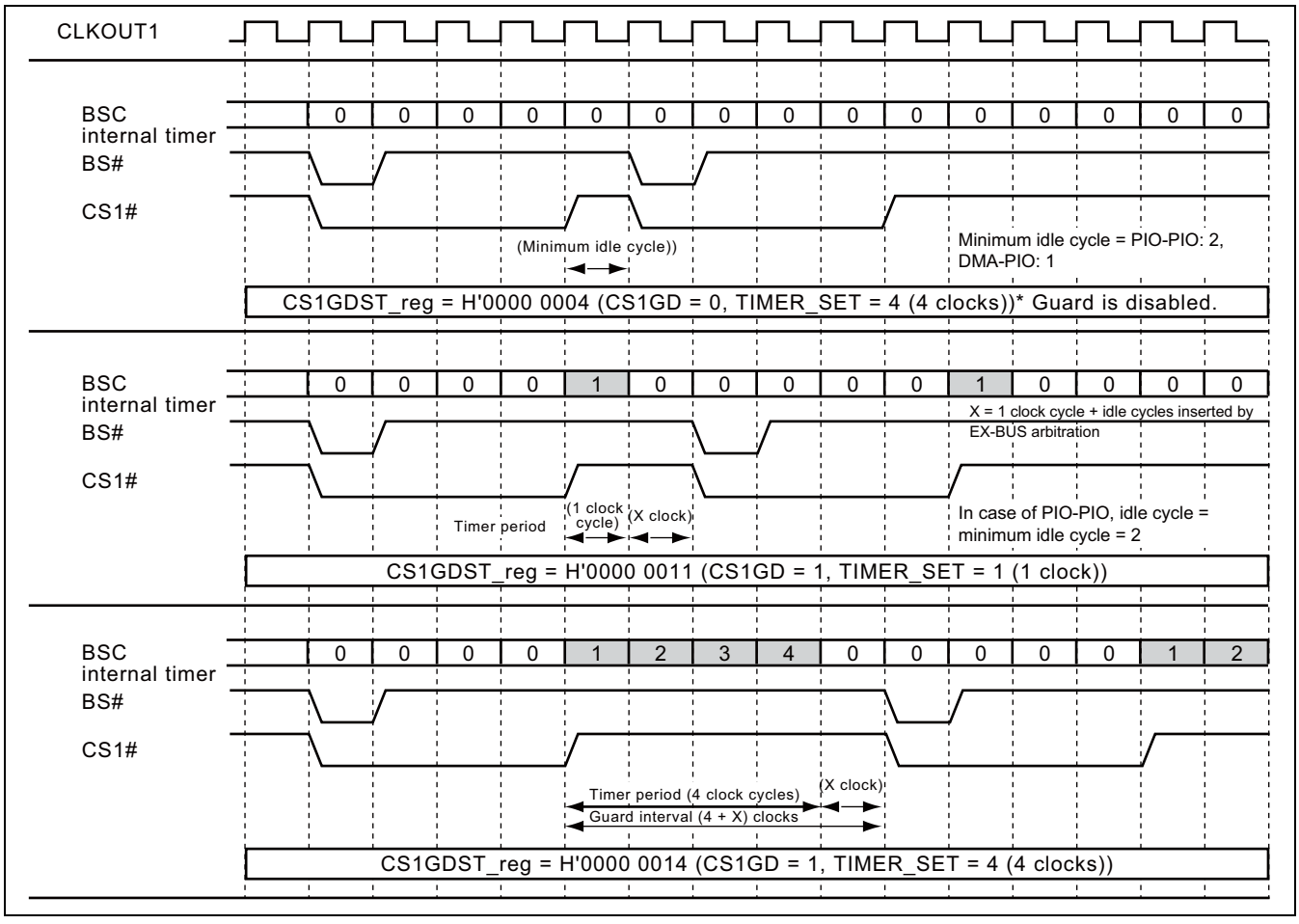


Figure 14.8 Concept of Guard-Interval Control

14.7.2 CPU (AXI Bus) → Burst ROM Interface

For area 0 on the EX-BUS, the BSC supports a page-mode read burst ROM interface. Switching to the burst ROM interface is performed by CS0CTRL settings. Because burst ROM access operations begin immediately after setting CS0CTRL, values must be pre-assigned to the CS0BTPH and CS0BSTCTL. In CS0BTPH, burst ROM access waveforms can be assigned, such as a first-cycle burst pitch, second and subsequent cycle burst pitches, and CS# signal hold cycles on the RD# signal. A burst access count (burst length) can be assigned to CS0BSTCTL. A burst access count should be assigned according to the component specifications for the actual external ROM that is connected.

In two kinds of exceptional cases, however, the BSC handles access with a burst count less than the specified burst count. The first are those cases where the CPU requests access to fewer data than the specified burst count. In such cases, access is terminated on completion of processing for the number of bytes requested by the CPU, even though the specified burst count has not been reached. The second are those cases where a variable burst address boundary is crossed in the midst of a specified burst count. In such cases, access is terminated immediately before the boundary is crossed, and the burst access is divided up, with the remainder of the access executed in a second round. The reason for this behavior is that the variable address boundaries for burst ROM devices, by which the LBSC must abide, are defined. Table 14.4 shows the LBSC's methodology for breaking off burst access.

Table 14.4 Methodology for Breaking off Bust Access

Burst Count Assigned in CS0BSTCTL	Bus Width	
	8-Bit Bus Width	16-Bit Bus Width
4	Break at a change of A2	Break at a change of A3 (A0 not connected)
8	Break at a change of A3	Break at a change of A4 (A0 not connected)
16	Break at a change of A4	Break at a change of A5* (A0 not connected)
32	Break at a change of A5*	(Setting prohibited)

Note: * Since A5 never changes in the midst of a 32-byte burst operation (a 32-byte boundary), access is not broken off in the case indicated by *, and the specified number of access operations proceed.

As described above, in burst ROM access, the LBSC performs a maximum of 32-byte access to accommodate CPU cache fill while performing access breakup. However, because this operation involves access on 32-byte boundaries, for setting a burst ROM device, the user should specify wrap-around settings instead of continuous burst operations.

Depending on the mode of burst ROM connection, burst operations can also be accommodated in the synchronous burst mode. When using the LBSC in synchronous burst mode, the user should not receive the Wait signals that are output by the burst ROM. Instead, a first-word data output latency should be assigned to the configuration register of the burst ROM, and CS0BTPH should be set as the pitch for the first word and this latency. For the second and subsequent words, a pitch count of 2 should be assigned to both the configuration register of the burst ROM and CS0BTPH. Subject to the AC characteristics of the burst ROM and given frequency for the EX-BUS, if a pitch count of 1 is assigned to, data reception timing can lag behind due to the fact that the burst ROM has a data output delay of approximately 13 ns. Figure 14.9 shows a basic timing chart for the burst ROM interface.

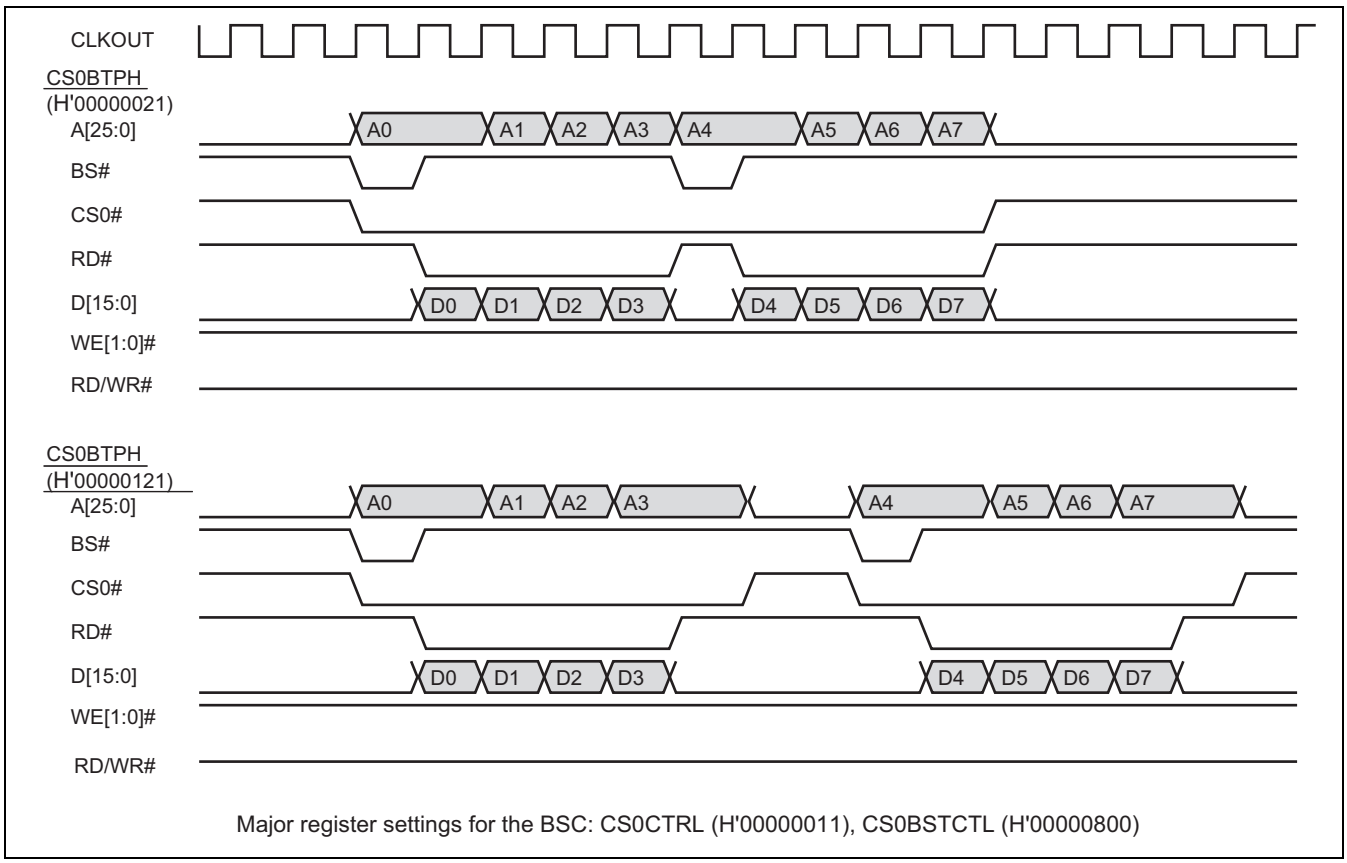


Figure 14.9 Timing Chart for Burst ROM Interface

14.7.3 LBSC-DMAC → DMA Interface

On the EX-BUS, three LBSC-DMAC channels (0 to 2) are assigned as DMACs that have external pins DREQ, DRACK, and DACK to support DMA transfer operations. Among these, channels 0 and 1 also support DMA with a burst length of 8.

All DMA channels operate in dual address mode. Table 14.5 provides a list of DMA pins by channel.

When operating a DMAC channel, first each DMAC should be assigned to the applicable area by using area assignment registers (EXDMASET0 to EXDMASET2) for the LBSC-DMAC channels. Also, in RD/WE pulse control registers (EXDMAWCR0 to EXDMAWCR2) for LBSC-DMAC channels, waveform pulse widths to be used during DMA bus access should be assigned (LBSC-DMAC channels 0 to 2 operate by the settings provided in EXDMAWCR0 to EXDMAWCR2, not by pulse width settings that are provided in CSWCR0, CSWCR1. In addition, methods by which DREQ, DACK, and DRACK signals are to be sent and received should be specified with the LBSC-DMAC channel control registers (EXDMCR0 to EXDMCR2).

Table 14.5 List of DMA Pins by Channel

DMAC Channel Number	Operating Mode	Pins			Remarks
		DREQ	DRACK	DACK	
Channel 0	Dual address mode (with 8-burst function)	DREQ0 (polarity and edge/level detection selectable)	DRACK0 (output timing adjustable and polarity selectable)	DACK0 (polarity selectable)	The burst count (8) does not depend on the access size; 8 consecutive bus accesses are executed for 8-bit and 16-bit bus widths equally.
Channel 1	Dual address mode (with 8-burst function)	DREQ1 (polarity and edge/level detection selectable)	—	DACK1 (polarity selectable)	DRACK1 does not exist as an LSI pin. The burst count (8) does not depend on the access size; 8 consecutive bus accesses are executed for 8-bit and 16-bit bus widths equally.
Channel 2	Dual address mode	DREQ2 (polarity and edge/level detection selectable)	—	DACK2 (polarity selectable)	DRACK2 does not exist as an LSI pin.

(1) Data Alignment during LBSC-DMAC Access

When receiving an access request from the LBSC-DMAC, the BSC translates the LBSC-DMAC interface into the EX-BUS protocol. During this operation, the BSC determines the area to be accessed based on the settings provided in the LBSC-DMAC area assignment registers (EXDMASET0 to EXDMASET2), and generates a chip select signal. For the data alignment of DMAC channels, one of two modes can be selected based on DMAC register settings.

- Fixed Alignment Mode

  In this operating mode, when performing a DMA transfer with a device on the EX-BUS, the LBSC determines that the access size from the LBSC-DMAC is equal to the data width used by the external device (not bound by the bus width specified in the CS0CTRL, CS1CTRL). In the fixed alignment mode, no alignment translation is performed in the BSC. Instead, data is output using the alignment received from the LBSC-DMAC. The LBSC, however, generates the WE1# to WE0# signals, depending on the access size received from the LBSC-DMAC. In the initial state, the LBSC operates in this mode. Table 14.6 shows the relationship between data widths and access sizes.

Table 14.6 Relationship between Data Widths and Access Sizes in Fixed Alignment Mode

Access Size Set in DMAC (Assumed to be Bus Width)	Data Bus Read/Write Position		Write Enable Signal Output Position	
	D15 to D8	D7 to D0	WE1#	WE0#
16 bits	Data 15 to 8	Data 7 to 0	Assert	Assert
8 bits	—	Data 7 to 0	—	Assert

- Variable Alignment Mode

  If the access size set in the DMAC is smaller than the bus width set in the BSC, variable alignment mode can be set up by DMAC register settings. In this case, the BSC changes byte lanes according to the specific access address to be serviced. Table 14.7 shows the relationship between data widths and access sizes in variable alignment mode. If the bus width set in the LBSC is equal to the DMAC access size, variable alignment mode operates in the same way as fixed mode.

Table 14.7 Relationship between Data Widths and Access Sizes in Variable Alignment Mode (Little Endian)

Bus Width Set in BSC	Access Size Set in DMAC	Data Bus Read/Write Position		Write Enable Signal Output Position	
		D15 to D8	D7 to D0	WE1#	WE0#
16 bits	16 bits	2n address		2n address	
	8 bits	2n+1 address	2n address	2n+1 address	2n address
8 bits	8 bits	—	n address	—	n address

(2) External Device DMA Transfer Request Detection Function

To provide generality, the LBSC supports a polarity and level/edge selection function as a method for the reception of external device DMA transfer request signals (DREQ). The selections are made by setting the relevant values in registers EXDMCR0 to EXDMCR2. In compliance with the settings, the BSC internally receives a DREQ signal and outputs the DMA transfer request signal from the BSC to the LBSC-DMAC. If level detection is selected, the BSC continues to output the DMA transfer request signal to the LBSC-DMAC as long as the DREQ signal from the external device is asserted. Conversely, if edge detection of the DREQ signal is selected, the BSC will not output a DMA transfer request signal to the LBSC-DMAC until an edge is detected, even if the DREQ signal from the external device continues to be asserted. In addition, even if more than one edge is detected during the period from the first edge detection to the start of DMA transfer, only one transfer request is issued.

(3) Role of the BSC between the LBSC-DMAC and an External Device

Figure 14.10 shows a basic timing chart for LBSC-DMAC-to-EX-BUS output translation. Upon receipt of an access request from the DMAC, the BSC first performs bus contention arbitration. When the LBSC-DMAC acquires the bus mastership, the BSC controls the pulse width of RD#, WE1# and WE0# that are output on the EX-BUS according to the settings provided in the LBSC-DMAC channel RD/WE pulse control registers (EXDMAWCR0 to EXDMAWCR2) that the BSC possesses, for the LBSC-DMAC access period.

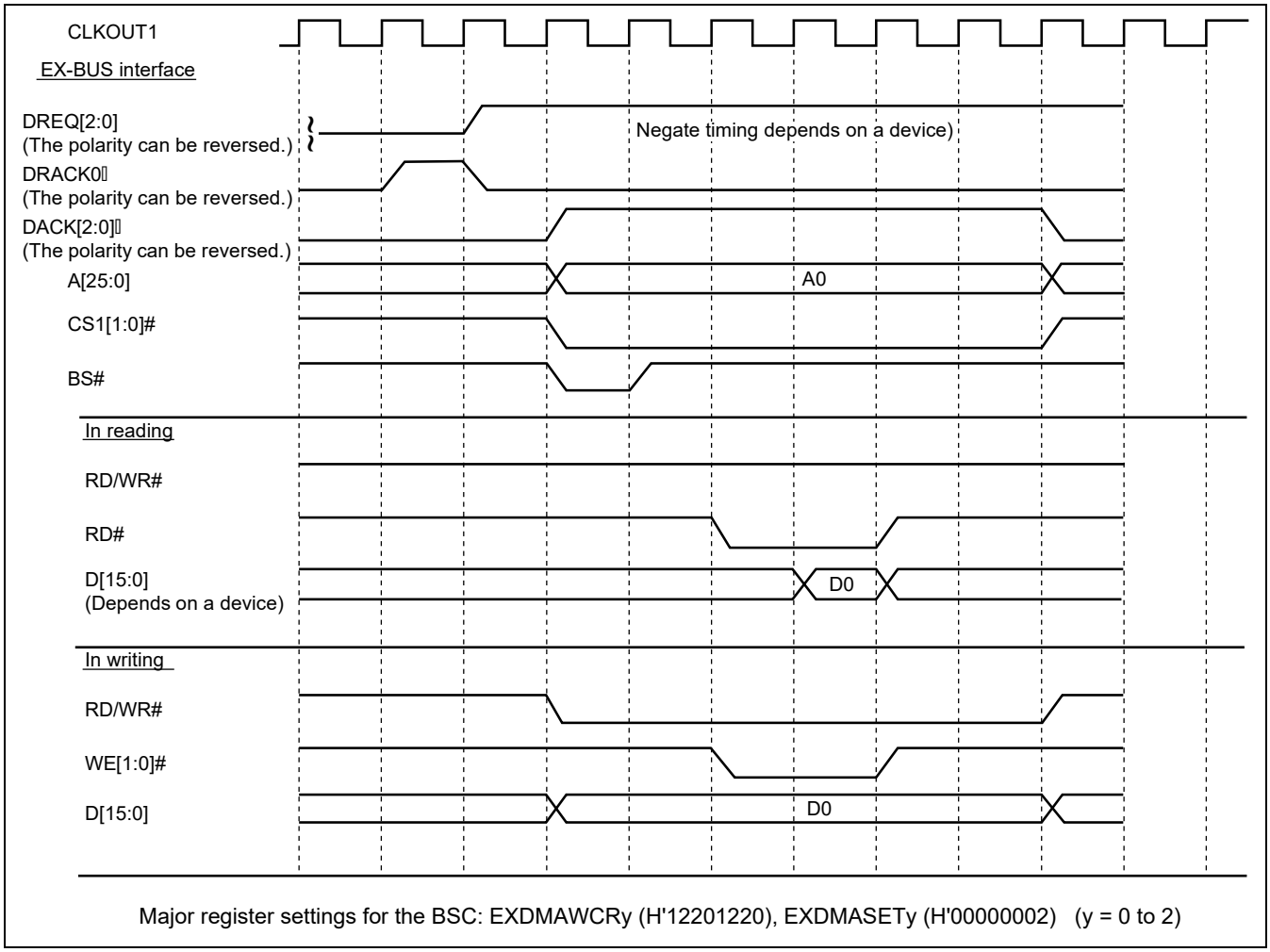


Figure 14.10 Basic Timing Chart for Access from LBSC-DMAC to EX-BUS

(4) LBSC-DMAC → EX-BUS Burst Access

The BSC supports the EX-BUS output function for burst access operations from the LBSC-DMAC (eight consecutive transfers irrespective of the access size). Figure 14.11 shows a timing chart on LBSC-DMAC burst access. The waveform for LBSC-DMAC burst access basically takes the form of repeated single-access waveforms. However, because external DMAC bus access does not release the bus mastership until the burst access is finished, PIO access from the CPU (AXI) does not result in a cycle stealing. In addition, transfer performance is enhanced because the DMAC treats data involving 8 transfer operations as a single packet and performs transfer operations with the destination.

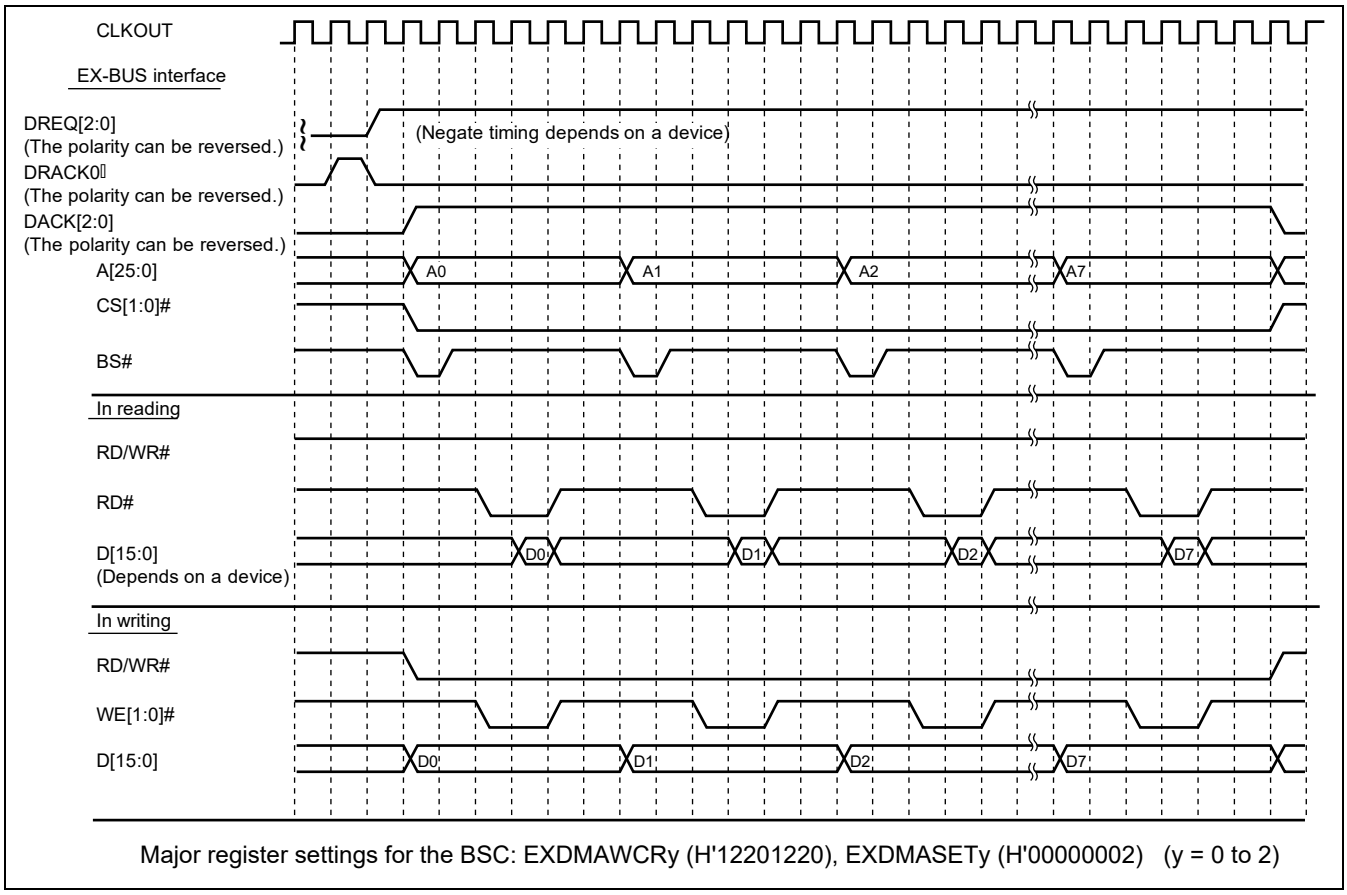
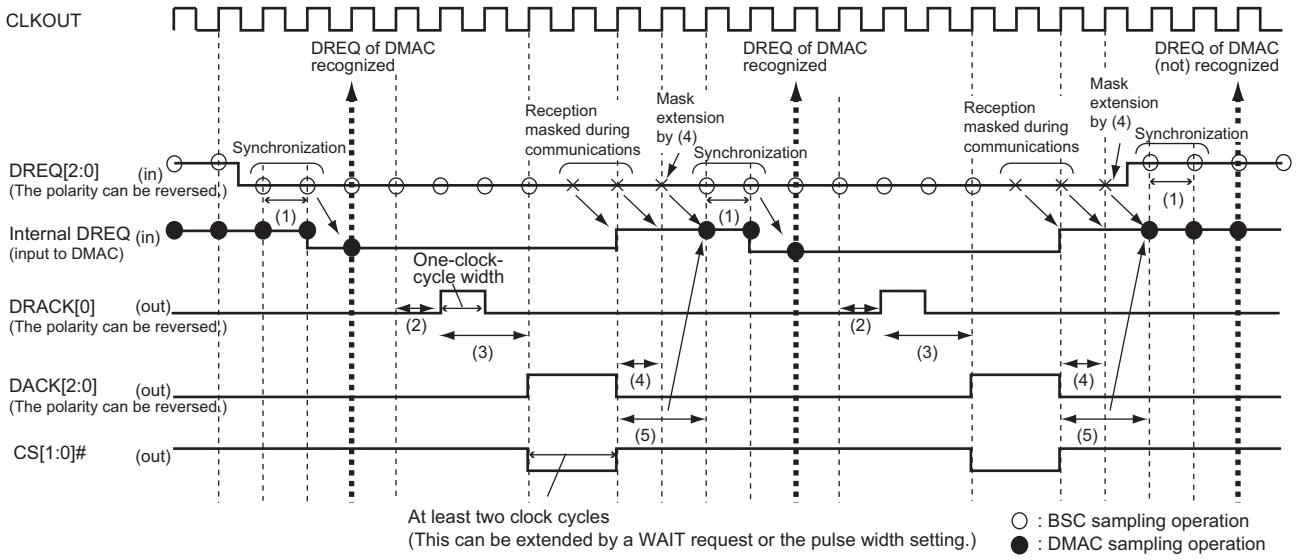


Figure 14.11 Basic Timing Chart for Burst Access from LBSC- DMAC to EX-BUS

(5) DREQ Reception Timing

Figure 14.12 shows the timing at which a DMA request (DREQ) signal is set in the level reception mode and any continuation of an asserted state is regarded as another DMA request. The figure also shows DREQ negate timing that prevents the above condition from being mistaken as another DREQ request.



(1) Synchronization time for asynchronous DREQ
By setting an appropriate value in EXDMCR0 of the BSC within bus bridge, DREQ can also be treated as a synchronous signal.
The default is to treat it as a synchronous signal, in which case the above 1 clock cycle becomes 0 clock.

(2) EX-BUS arbitration time
The above 1 clock cycle represents the shortest time. In the case of contention, the time is extended until the access right is acquired.

(3) DRACK → DACK time
Either one or two clock cycles can be selected by means of EXDMCR0 of the BSC within bus bridge.
The above diagram is a case where the DRACK-to-DACK time is specified as two clock cycles.
Because IO-DMAC channels other than channel 0 do not have a DRACK, the interval in (3) will be 1clock cycle for the channels.

(4) Next DREQ recognition masking time (not available in the edge mode)
In the clock points following the CS# negate, the reception of the next DREQ can be masked.
The above diagram represents the case where a 1 clock cycle interval is masked.
This varies in a 0 to 15 clock-cycle range in DRMSKR of the DMAC within bus bridge.

Note: Setting (4) is not allowed in the edge mode, in which exists no such period of reception masking during communications as shown in the diagram above. Therefore, DREQ is detected on an edge basis even during the interval indicated as "Reception masked during communications" in the diagram above.

(5) Next DREQ for DMAC sampling resumption timing
This is the timing at which the DMAC resumes the sampling of another DREQ (a synchronized signal) from the CS# negate points.
The timing at which DREQ sampling is resumed, shown in the table below, varies with access mode.

Access Mode	Clock Cycle Count
Write access	Sampling resumed after two clock cycles
Read access	Sampling resumed after three clock cycles

According to the above diagram, in the case where setting (4) is 0, DREQ is detected as another DMA request unless DREQ is negated between the CS# negate points and the next clock cycle.

Figure 14.12 Next DREQ Signal Recognition Timing on EX-BUS

14.7.4 CPU (AXI Bus) → Byte-Control SRAM Interface

With respect to EX-BUS area 1, the LBSC supports byte-control SRAM interface from the CPU (AXI bus) or LBSC-DMAC (area 0 is excluded). Byte-control SRAM interface is a memory interface in which byte select strobe signal WE# is output in both read and write cycles. Write timing for byte-control SRAM interface is the same as that for SRAM interface. In read access, however, WE# is output at a different timing. In read access, WE# is output for a read byte only. The assertion timing of WE# can be selected with the CS1BRM bit in the CS1CTRL register to be the same as that of CS# or RD#. In default setting, SRAM operating mode is set for each area. Accordingly, along with the setting of assertion timing, byte-control SRAM mode should be set in the registers corresponding to a given area (CS1CTRL).

(1) Byte-control SRAM Interface

- The WE# assertion period can be selected by the CS1BRM bit to be the same as that of CS# or RD#.
- In read access, WE# is asserted only for a valid access byte. (For example, when a byte is read from a device with the byte-control SRAM interface and a bus width of 16 bits, any one of the WE# bits is asserted.)
- The waveform in write access is the same as that for SRAM interface.

(2) Basic Timing Charts

Figure 14.13 shows the basic timing chart for byte-control SRAM interface.

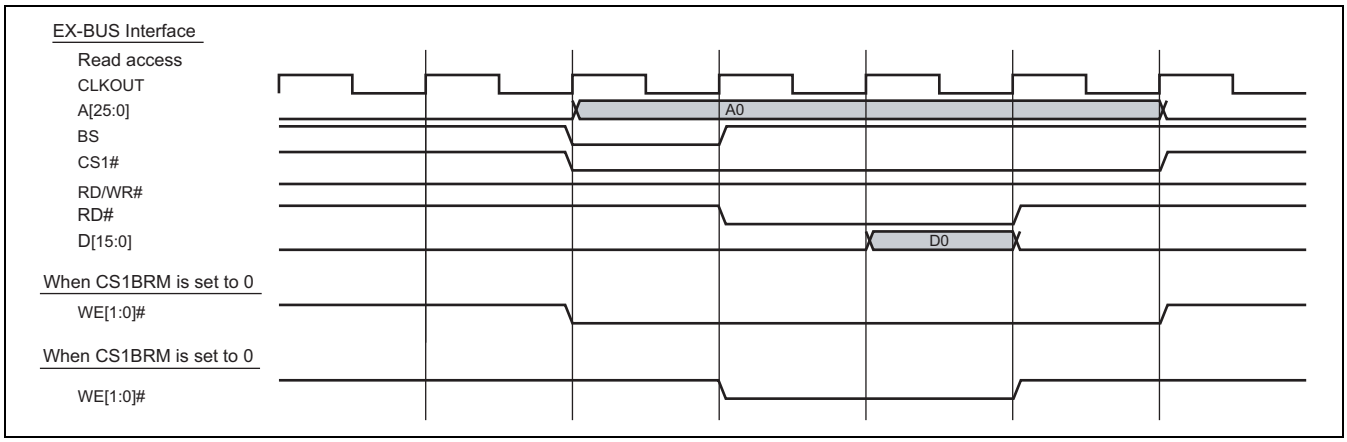


Figure 14.13 Waveforms for Byte-Control SRAM Interface

14.7.5 Wait Timeout

For the detection of timeout in waiting for access to the EX-BUS, the BSC monitors the states of the EX_WAIT1, and EX_WAIT0 signals from external devices. When an external device is waiting for more than a certain length of time, this is detected as an EX-BUS wait timeout error. The error is reflected in a register within the BSC, and forces the termination of access to the EX-BUS interface.

The value of the timeout counter is specified in a total of 32 bits, consisting of the EXW_TOBCNT bits in the EX-TIME wait timeout detection base counter register (EXBCT) and the EXW_TOCNT bits in the EX-BUS wait timeout detection counter register (EXTCT). EXW_TOBCNT is a 20-bit counter that operates at the EX-BUS operating frequency (CLKOUT). EXW_TOCNT is a 12-bit counter that counts up by one every time the EXW_TOBCNT bits overflow.

Writing 0s to all of the bits specifies the maximum time until overflow. The required detection time depends on the EX-BUS operating frequency as defined in the following formula.

Detection time in ns = period in ns at EX-BUS operating frequency × {EXW_TOCNT, EXW_TOBCNT}

14.7.6 EX-BUS Arbitration

To deal with the conflicts between the access requests from the CPU (AXI bus) and LBSC-DMAC channels 0 to 2, the EXBATLV register in the LBSC can set the priority levels for these accesses. Furthermore, to deal with the conflicts among the LBSC-DMAC channels 0 to 2, the three channels are grouped into two groups by the DMA memory access priority level control register (DMLVLR) in the LBSC-DMAC, and the priority levels are determined according to the round-robin scheme in each group.

Figure 14.14 shows a concept diagram for EX-BUS arbitration.

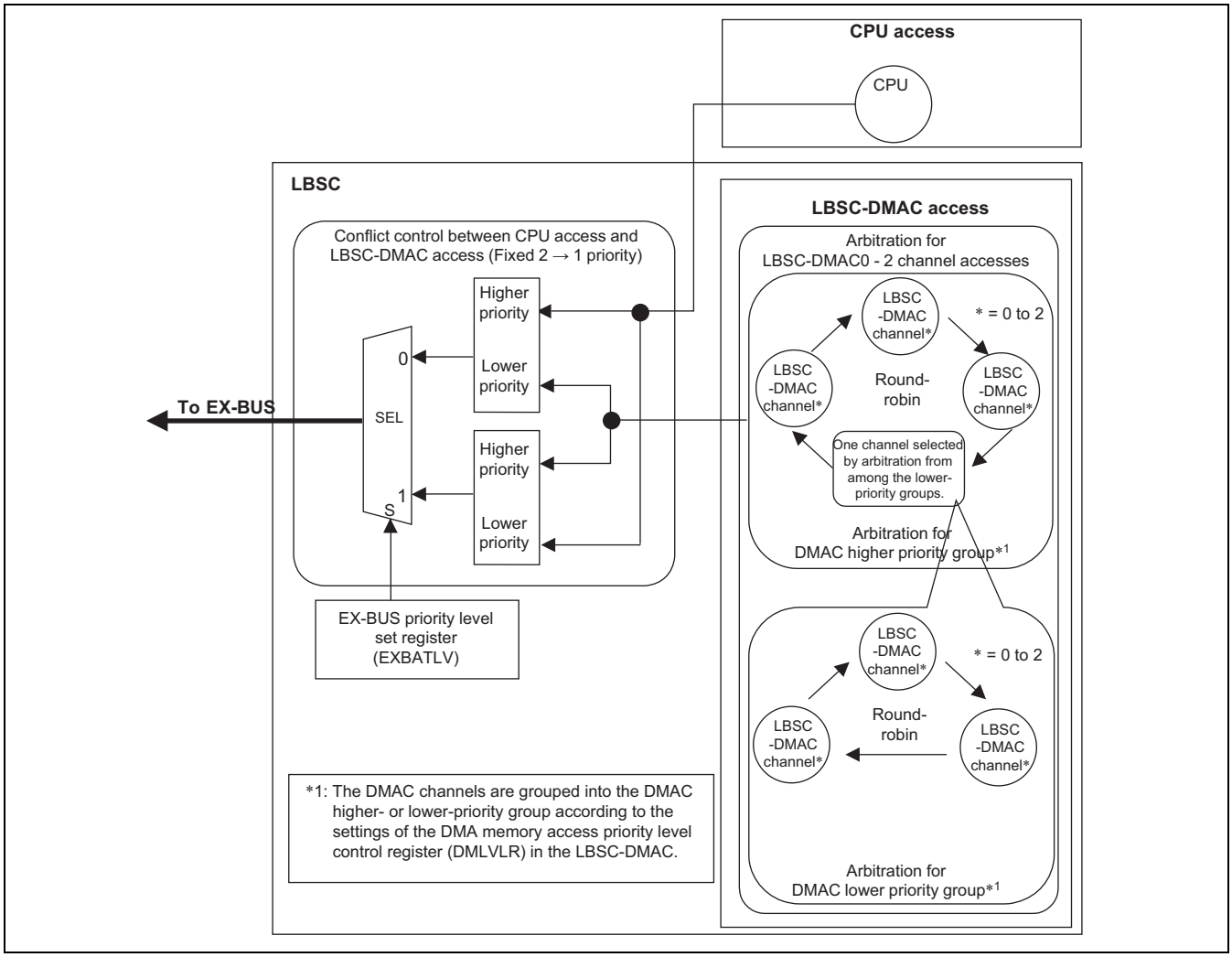


Figure 14.14 Concept Diagram for EX-BUS Arbitration

14.8 Usage Notes

Keep the following notes in mind when using this LBSC.

14.8.1 Pin Multiplexing

When starting this LSI, be sure to set multiplexed pins appropriately using the LSI pin multiplexing set register.

Also, make pull-up resistor settings using the LSI pin pull-up control registers.

For details on the specific set values, refer to section 5, Pin Function Controller (PFC).

14.8.2 Short period low driving at the end of SRAM write access

The external bus is instantaneously driven low at the end of SRAM write access with high write data as shown in Figure 14.15. If the external bus has high load due to system board composition, this short period low driving might cause overshoot on the external bus signals. In designing system board, note that this overshoot might cause voltage level that exceeds the input high voltage.

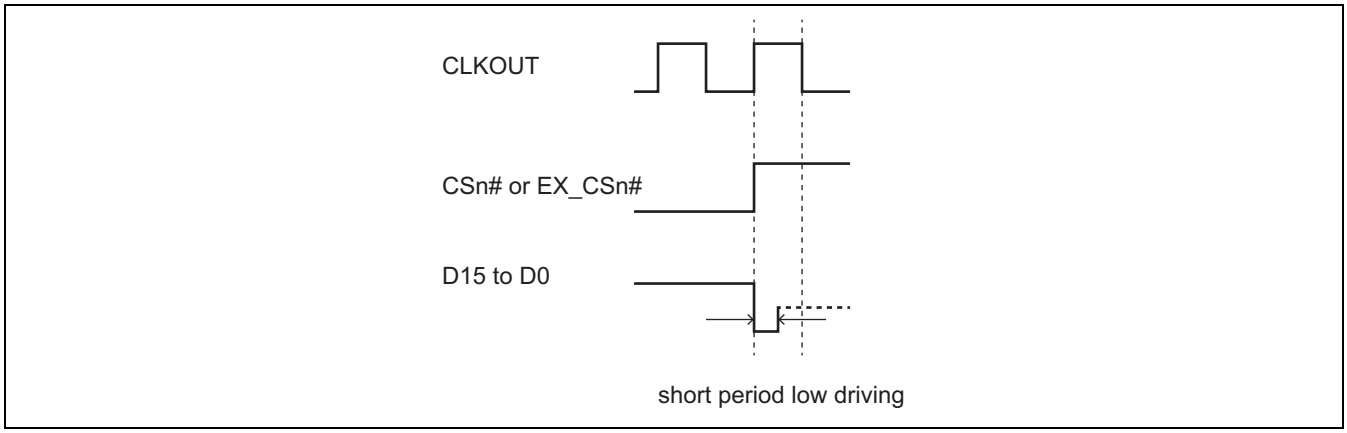


Figure 14.15 Short period low driving at the end of SRAM write access

14.8.3 Usage Note

When using QSPI or HSCIF booting by mode pins setting (MD[3:1]), the area 0 beginning 256-KByte space (H'00 0000 0000 to H'00 0003 FFFF) cannot be accessed from LBSC even after booting.

15. External Bus Controller for DDR3-SDRAM (DBSC3)

15.1 Overview

The external bus controller for DDR3-SDRAM (DBSC3) supports DDR3-SDRAM only. The DBSC3 contains bus control, device control, and register control units. The bus control unit receives requests from the bus and issues commands to the device control and register control units. The device control unit reads from and writes to the SDRAM according to the issued commands. Also, the device control unit refreshes the SDRAM. The register control unit reads from and writes to the control registers according to the issued commands.

15.1.1 Features

The DBSC3 enables the maximum use of SDRAM bus bandwidth using the following functions:

1. Multibank operation that improves the page hit rate.
2. DDR3-SDRAM operation with burst length 8 that reduces the number of SDRAM command issues.
3. Preceding execution of the bank precharge and activate commands for subsequent requests.

Table 15.1 shows the main functions of the DBSC3.

Table 15.1 DBSC3 Functions

Item	Function
Multibank supported	Supports 8-bank multibank operation
Number of banks	Supports eight banks
External bus width	32 bits
Preceding precharge/ activate functions	Determines the content of subsequent requests in a request queue and performs preceding precharge/activate processing for the bank to be accessed during an empty command cycle upon page-miss.
Operating modes	Burst length: 8 (fixed) Burst type: Sequential (fixed) DLL-off mode for the DDR3-SDRAM is not supported.
Power-down mode	Supports self-refresh mode, precharged power-down mode, and active power-down mode.
Address order (address translation function)	The addresses arranged in descending order are: rank address, row address, bank address, and column address. (The 3-bit bank address can be divided into two parts. One can be placed in the upper half of the row address and the other in the lower half. Register settings can be used to determine how to divide the bank address.)
Timing setting	The following timing settings can be specified: CAS latency, CAS write latency, ACT to READ or ACT to WRITE minimum period, PRE period, ACT to ACT or ACT to REF minimum period, ACT to PRE minimum period, ACT(A) to ACT(B) minimum period, four active window minimum period, READ to PRE minimum period, write recovery period, READ to WRITE minimum period, WRITE to READ minimum period, REF to ACT or REF to REF (all banks) minimum period, REF to ACT or REF to REF (per bank) minimum period, minimum period over which CKE is held high, and minimum period over which CKE is held low Only 0 is supported for additive latency (AL).
Refreshes	Average interval and the maximum post count are set by the register. If an empty cycle for request is found, preceding refresh can be performed.
Auto power-down operation	When there is no access for a specified period, power-down mode is automatically entered. The period before power-down mode is entered can be specified through register settings.

Item	Function
ZQ calibration operation	Supports the automatic ZQCS issuing function. After auto-refresh, the ZQCS command is issued to DDR3-SDRAM. The frequency of issuing ZQCS can be specified through register settings in units of the auto-refresh count. The intervals between auto-refresh and ZQCS and between ZQCS and auto-refresh can also be specified through register settings.
PHY interface	1-ch mode: 32-bit bus width
Memory to be connected	DDR3-SDRAM compliant with JEDEC JESD79-3E. (Supports memory with sizes from 512 Mbits to 8 Gbits. SDRAM with a data bus width of 4 bits and 8 bit is not supported.)
ECC	Not supported.
Parity	Not supported.

15.1.2 Definition of Terms and Symbols

The following terms and symbols are used throughout the DBSC3 specifications:

- DDR3-SDRAM is abbreviated as SDRAM in some cases.
- "ceil(x)" is the smallest integer which is greater than or equal to real number x.
- "floor(x)" is the greatest integer which is less than or equal to real number x.

15.1.3 Block Diagram

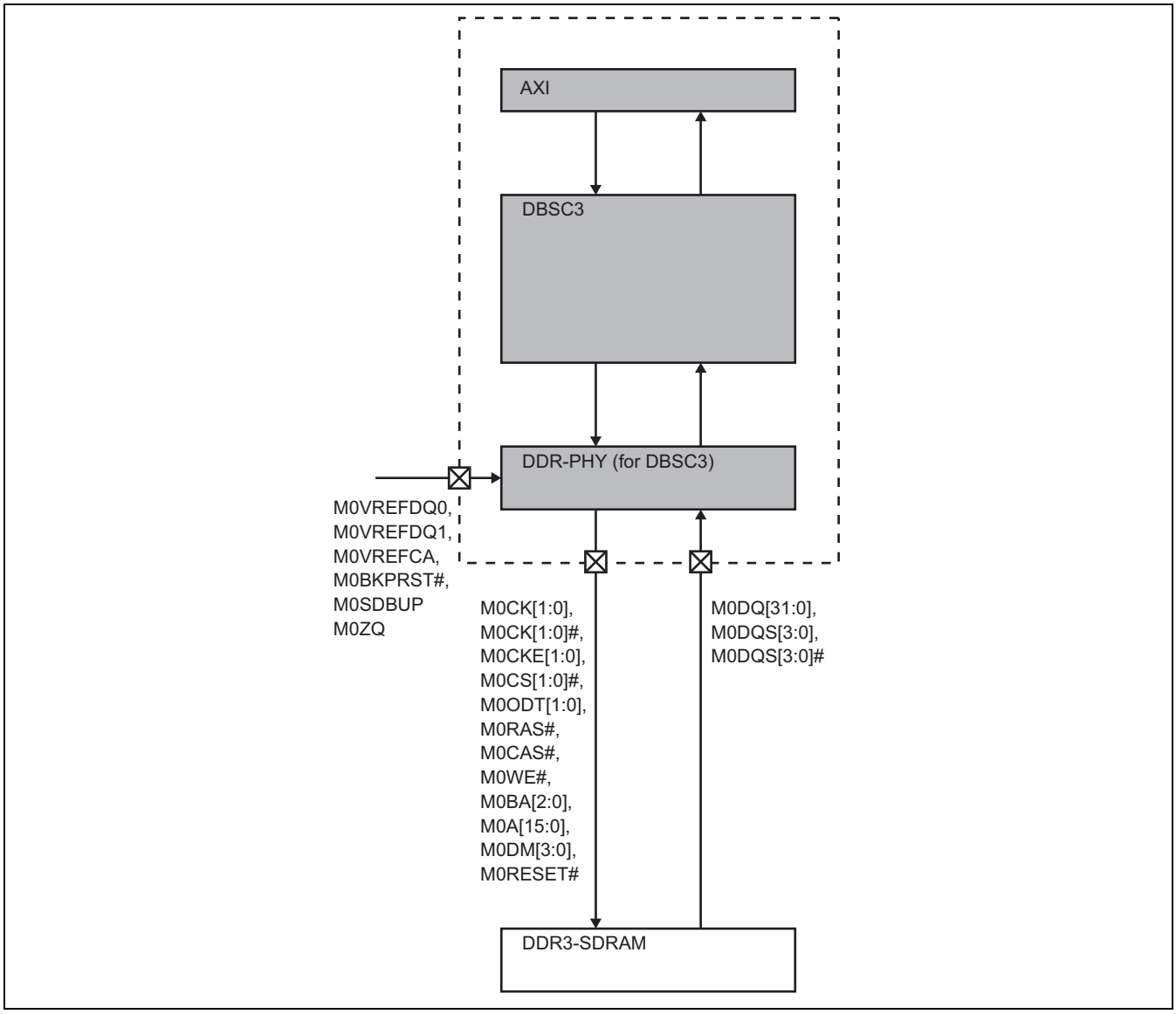


Figure 15.1 Block Diagram of the DBSC3

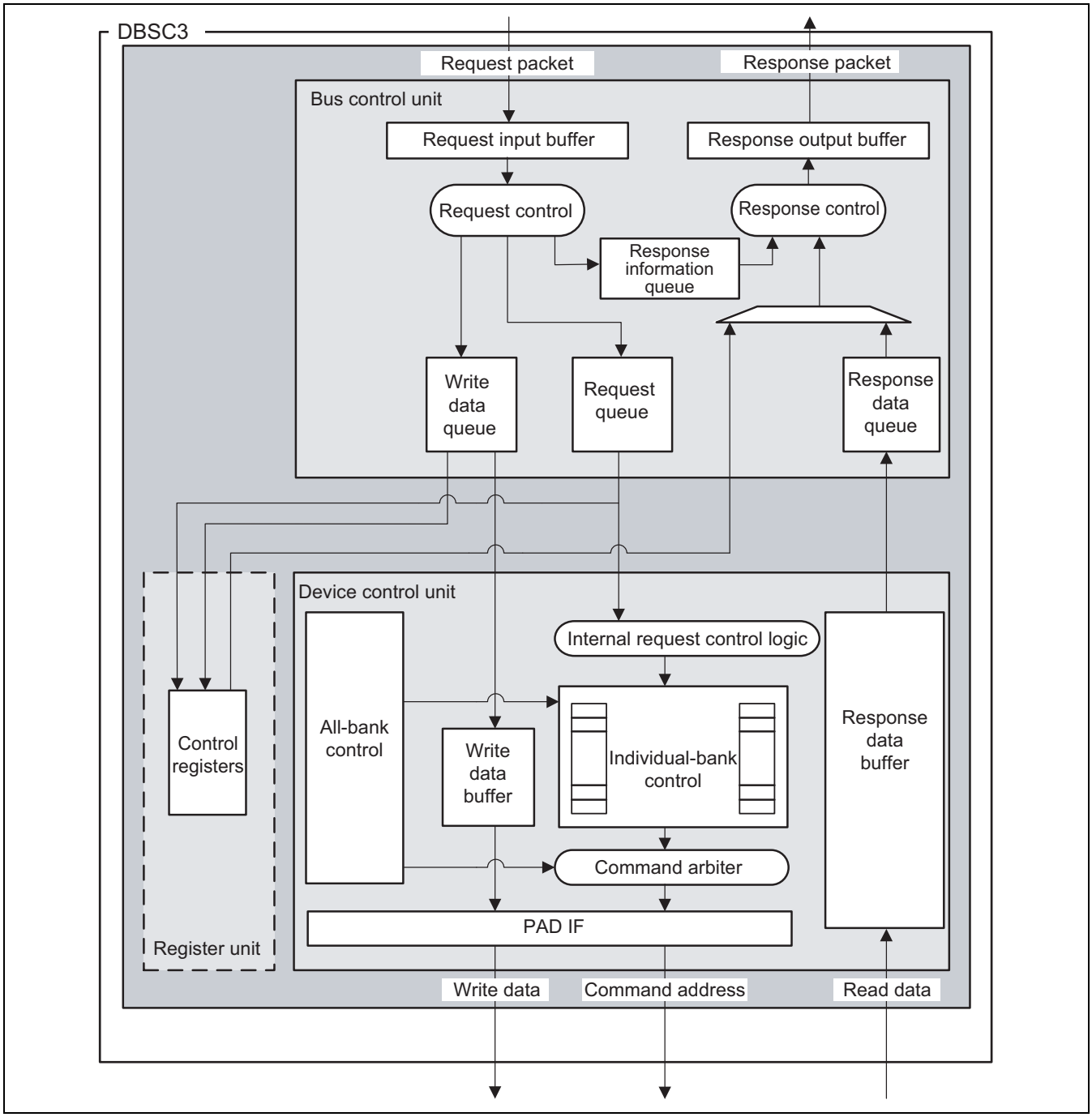


Figure 15.2 Internal Block Diagram of DBSC3

15.1.4 Input/Output Pins

Table 15.2 show the pin configuration of the DBSC3.

Table 15.2 Pin Configuration of the DBSC3

Name	Pin Name	I/O	Function
DDR3-SDRAM clock	M0CK[1:0]	Output	Clock output signals for the DDR3-SDRAM
DDR3-SDRAM clock	M0CK[1:0]#	Output	Clock output signals for the DDR3-SDRAM or M0CK[1:0] inverted clock output signals
Addresses	M0A[15:0]	Output	Address output signals for the DDR3-SDRAM
Bank address	M0BA[2:0]	Output	Bank address output signals
Chip select	M0CS[1:0]#	Output	Chip select output signals
Row address strobe	M0RAS#	Output	Row address strobe output signal
Column address strobe	M0CAS#	Output	Column address strobe output signal
Write enable	M0WE#	Output	Write enable output signal
Clock enable	M0CKE[1:0]	Output	CKE output signals
ODT enable	M0ODT[1:0]	Output	ODT enable output signals in the SDRAM
Power backup reset	M0BKPRST#	Input	When this pin is brought to the low level, M0CKE[1:0] pins are fixed to the low level and M0RESET# pin to the high level.
Power backup mode	M0SDBUP	Input	This pin must be held at the high level.
Reset	M0RESET#	Output	Reset output for the DDR3-SDRAM
Impedance matching	M0ZQ	I/O	Impedance matching Refer to section 15.4.1, Connection of M0ZQ Pin.
Data mask	M0DM[3:0]	Output	Data mask output signals
I/O data strobe	M0DQS[3:0]	I/O	Data strobe I/O signals
I/O data strobe	M0DQS[3:0]#	I/O	Data strobe I/O signals or M0DQS[3:0] inverted signals
Data	M0DQ[31:0]	I/O	Data I/O signals
Reference voltage input	M0VREFCA	Input	Should be fixed at GND.
Reference voltage input	M0VREFDQ0	Input	Input reference voltage
Reference voltage input	M0VREFDQ1	Input	Input reference voltage

15.1.5 Register Configuration

Table 15.3 shows the DBSC3 register mapping, followed by a description of each register. Register addresses are shown in the form of the sum of the DBSC3 register start address (DB_ADDR for DBSC3) and an offset (hexadecimal) from that start address.

Registers other than particular ones are initialized by power-on reset.

Access the DBSC3 registers 32 bits at a time. Otherwise, correct operation cannot be guaranteed.

DB_ADDR (DBSC3) = H'E679 0000

Table 15.3 DBSC3 Register Configuration

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size (Bits)
DBSC3 status register 1	DBSTATE1	R	DB_ADDR + H'00C	H'000X 000X	32
SDRAM access enable register	DBACEN	R/W	DB_ADDR + H'010	H'0000 0000	32
Auto-refresh enable register	DBRFEN	R/W	DB_ADDR + H'014	H'0000 0000	32
Manual command-issuing register	DBCMD	R/W	DB_ADDR + H'018	H'0000 0000	32
Operation completion waiting register	DBWAIT	R	DB_ADDR + H'01C	H'0000 0000	32
SDRAM type setting register	DBKIND	R/W	DB_ADDR + H'020	H'0000 0000	32
SDRAM configuration setting register 0	DBCONF0	R/W	DB_ADDR + H'024	H'0000 0000	32
PHY type setting register	DBPHYTYPE	R/W	DB_ADDR + H'030	H'0000 0000	32
SDRAM timing register 0	DBTR0	R/W	DB_ADDR + H'040	H'0000 0000	32
SDRAM timing register 1	DBTR1	R/W	DB_ADDR + H'044	H'0000 0000	32
SDRAM timing register 2	DBTR2	R/W	DB_ADDR + H'048	H'0000 0000	32
SDRAM timing register 3	DBTR3	R/W	DB_ADDR + H'050	H'0000 0000	32
SDRAM timing register 4	DBTR4	R/W	DB_ADDR + H'054	H'0000 0000	32
SDRAM timing register 5	DBTR5	R/W	DB_ADDR + H'058	H'0000 0000	32
SDRAM timing register 6	DBTR6	R/W	DB_ADDR + H'05C	H'0000 0000	32
SDRAM timing register 7	DBTR7	R/W	DB_ADDR + H'060	H'0000 0000	32
SDRAM timing register 8	DBTR8	R/W	DB_ADDR + H'064	H'0000 0000	32
SDRAM timing register 9	DBTR9	R/W	DB_ADDR + H'068	H'0000 0000	32
SDRAM timing register 10	DBTR10	R/W	DB_ADDR + H'06C	H'0000 0000	32
SDRAM timing register 11	DBTR11	R/W	DB_ADDR + H'070	H'0000 0000	32
SDRAM timing register 12	DBTR12	R/W	DB_ADDR + H'074	H'0000 0000	32
SDRAM timing register 13	DBTR13	R/W	DB_ADDR + H'078	H'0000 0000	32
SDRAM timing register 14	DBTR14	R/W	DB_ADDR + H'07C	H'0000 0000	32
SDRAM timing register 15	DBTR15	R/W	DB_ADDR + H'080	H'0000 0000	32
SDRAM timing register 16	DBTR16	R/W	DB_ADDR + H'084	H'0000 0000	32
SDRAM timing register 17	DBTR17	R/W	DB_ADDR + H'088	H'0000 0000	32
SDRAM timing register 18	DBTR18	R/W	DB_ADDR + H'08C	H'0000 0000	32
SDRAM timing register 19	DBTR19	R/W	DB_ADDR + H'090	H'0000 0000	32
SDRAM operation setting register	DBBL	R/W	DB_ADDR + H'0B0	H'0000 0000	32
DBSC3 operation adjustment register 0	DBADJ0	R/W	DB_ADDR + H'0C0	H'0000 0000	32
DBSC3 operation adjustment register 2	DBADJ2	R/W	DB_ADDR + H'0C8	H'0000 0000	32
Refresh configuration register 0	DBRFCNF0	R/W	DB_ADDR + H'0E0	H'0000 0000	32

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size (Bits)
Refresh configuration register 1	DBRFCNF1	R/W	DB_ADDR + H'0E4	H'0000 0000	32
Refresh configuration register 2	DBRFCNF2	R/W	DB_ADDR + H'0E8	H'0000 0000	32
DDR3-SDRAM calibration configuration register	DBCALCNF	R/W	DB_ADDR + H'0F4	H'0000 0000	32
DDR3-SDRAM calibration timing register	DBCALTR	R/W	DB_ADDR + H'0F8	H'0000 0000	32
ODT operation setting register	DBRNK0	R/W	DB_ADDR + H'100	H'0000 0000	32
Power-down configuration register	DBPDNCNF	R/W	DB_ADDR + H'180	H'0000 0000	32
PHY Unit Control Register 0	DBPDCNT0	R/W	DB_ADDR + H'200	H'0000 0000	32
PHY Unit Control Register 1	DBPDCNT1	R/W	DB_ADDR + H'204	H'0000 0000	32
PHY Unit Control Register 2	DBPDCNT2	R/W	DB_ADDR + H'208	H'0000 0000	32
PHY Unit Control Register 3	DBPDCNT3	R/W	DB_ADDR + H'20C	H'0000 0000	32
Bus control unit 0 control register 1	DBBS0CNT1	R/W	DB_ADDR + H'304	H'0000 0000	32
AXI port setting register 0	DBWT0CNF0	R/W	DB_ADDR + H'380	H'0000 0000	32
AXI port setting register 4	DBWT0CNF4	R/W	DB_ADDR + H'390	H'0000 0000	32

Note: Do not write to addresses other than the listed above. Otherwise, correct operation is not guaranteed.

15.2 Register Description

The legends used in register descriptions have the following meanings.

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in longword units.

Write 0 to the reserved bits.

15.2.1 DBSC3 Status Register 1 (DBSTATE1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFU	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BKUP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	X
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	RFU	Undefined	R	Reserved
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	BKUP	X	R	This bit reflects the signal level being input on the M0 SDBUP pin, corresponding to the following states.

15.2.2 SDRAM Access Enable Register (DBACEN)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ACCEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	ACCEN	0	R/W	SDRAM Access Enable Bit This bit enables data access to the SDRAM. Make data access to the SDRAM after setting this bit to 1. When this bit is 0, do not access the SDRAM area. 0: Disables access to the SDRAM. 1: Enables access to the SDRAM.

Note: When making the setting to disable access (writing 0 to this register), a precharge all or precharge command for the SDRAM may be issued automatically.

15.2.3 Auto-Refresh Enable Register (DBRFEN)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ARFEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	ARFEN	0	R/W	Auto-Refresh Enable Bit This bit starts or stops the auto-refresh function. Writing 1 to this bit resets the refresh counter (refresh history) in the DBSC3 and starts the auto-refresh function. While this bit is 1, the DBSC3 issues a refresh command at regular intervals. The refresh cycle time and other settings depend on the values held in the refresh configuration registers 0 to 2 (DBRFCNF0 to DBRFCNF2) when 1 is written to this bit. 0: Stops the auto-refresh function. 1: Starts the auto-refresh function.

15.2.4 Manual Command-Issuing Register (DBCMD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	OPC						—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ARG															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
29 to 24	OPC	000000	R/W	Operation Code Bits Specify the type of command to be issued. Refer to Table 15.4. If Wait is specified through these bits, valid SDRAM commands are not output and no processing is performed except reserving the time until the next operation. These bits are read as undefined values.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 0	ARG	H'0000	R/W	Parameter Bits The meaning can differ according to the operation code indicated by the OPC bits. When OPC indicates Mode Register Set (MRS0 to MRS3), the ARG bits specify the value to be issued on the address pins (MA) of SDRAM. When OPC is any other value, the ARG bits specify the minimum interval to issuing of the next command in SDRAM cycles. When ARG = 0, however, the values default to those given in "Interval" column of Table 15.4. These bits are read as undefined values.

The manual command-issuing register (DBCMD) is used to issue the required commands for the sequence of initializing the SDRAM and of transitions to and from the self-refresh mode. The command corresponding to the OPC bits is issued once as a result of writing to this register. For instance, issuing the refresh command twice requires that "001100" be written to the OPC bits twice. Do not write to this register while access to the SDRAM is enabled (ACCEN = 1 in the DBACEN register). The timing with which an operation is complete (i.e. the timing with which the specified SDRAM command is output to the PHY unit from DBSC3) may be later than the response of DBSC3 to writing to this register. If you wish to wait until actual output of the specified SDRAM command to SDRAM; do this by reading the DBWAIT register (described later).

When this register is used to issue a command, the issuing of a subsequent SDRAM command is delayed by a certain period of time from the moment at which each operation is completed (i.e. from the time when the specified SDRAM command is output to SDRAM). This facilitates securing of the required amounts of time between commands in the issuing of multiple consecutive commands.

These periods are given in the "Interval" column of Table 15.4. They can also be customized by using the ARG bits (except in cases where the OPC bits indicate MRS0 to MRS3).

Table 15.4 Manual Command Issue Functions

OPC	Code	Operation	Interval (Number of SDRAM Cycles)	ARG Function
00 0000	Wait	Issue "Device Deselected" (and insert wait cycles)	4	Customizing the interval (for ARG = 0, the value is that given at left)
00 0010	ZQCS	Issue "ZQ Calibration Short"	4	
00 0011	ZQCL	Issue "ZQ Calibration Long"	4	
00 1011	PREA	Issue "Precharge All"	TRPA	
00 1100	Ref	Issue "Refresh"	TRFC	
01 0000	PDEn	Power Down Entry	4	
01 0001	PDXt	Power Down Exit	4	
01 1000	SREn	Self-Refresh Entry	4	
01 1001	SRXt	Self-Refresh Exit	TRFC	
10 0000	RstL	Set Reset Pins to Low	4	
10 0001	RstH	Set Reset Pins to High	4	
10 1000	MRS0	Issue "ModeRegisterSet" (for MRS/MR0)"	TMOD	Specifying the setting for SDRAM mode register
10 1001	MRS1	Issue "ModeRegisterSet" (for EMRS1/MR1)	TMOD	
10 1010	MRS2	Issue "ModeRegisterSet" (for EMRS2/MR2)	TMOD	
10 1011	MRS3	Issue "ModeRegisterSet" (for EMRS3/MR3)	TMOD	

Notes: 1. TRPA, TRFC, and TMOD in the "Interval" column of the above table indicate timing registers. The intervals in these cases are determined by the corresponding register settings.

2. Only write to this register after having disabled SDRAM access (i.e. the ACCEN bit in the DBACEN register = 0).

3. Only write to this register after having stopped the auto-refresh function (i.e. the ARFEN bit in the DBRFEN register = 0). However, sequences described in section 15.3, Operation, are not limited to these. If Wait is specified in the OPC bits in this register during auto-refresh operations, the auto-refresh function may issue a refresh command during the time secured for the Wait command.

15.2.5 Operation Completion Waiting Register (DBWAIT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WAIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	WAIT	0	R	Operation Completion Waiting Bit This value is meaningless. This bit is always read as 0.

When this register is read, a response is returned after all command issuing that has been specified by using the DBCMD register by that time is completed (i.e., after command output from the DBSC3 to the PHY unit).

This register can be used to guarantee correctness for the relationship between the timing with which SDRAM commands are issued by DBSC3 and timing that is not managed by DBSC3 (e.g. clock control).

15.2.6 SDRAM Type Setting Register (DBKIND)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DDCG		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
2 to 0	DDCG	000	R/W	SDRAM Type Bits These bits can set the type of SDRAM. 111: DDR3-SDRAM Other settings are prohibited.

Notes: 1. This register must only be written from within the initialization sequence (see section 15.3.4, Initialization Sequence).
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
3. Set the defined value in each group.
4. Specify the same SDRAM type as the SDRAM specified at power-on.

15.2.7 SDRAM Configuration Setting Register 0 (DBCONF0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AWRW0					—	—	—	AWRK0	—	—	AWBK0	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	AWCL0				—	—	—	—	—	—	DW0	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
28 to 24	AWRW0	00000	R/W	Row Address Bit Width Setting Bits These bits specify the width, in bits, of row addresses. 01100: 12 bits : 10000: 16 bits Other settings are prohibited.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
20	AWRK0	0	R/W	Number of Ranks Setting Bits These bits specify the number of ranks. 0: One rank 1: Setting prohibited
19, 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	AWBK0	00	R/W	Number of Banks Setting Bits These bits specify the number of banks. 11: Eight banks Other settings are prohibited.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 8	AWCL0	0000	R/W	Column Address Bit Width Setting Bits These bits specify the width, in bits, of column addresses. 1010: 10 bits 1011: 11 bits Other settings are prohibited.

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	DW0	00	R/W	External Data Bus Width Setting Bits These bits specify the width of the external bus. 10: 32 bits Other settings are prohibited.

This register sets the memory configuration to be used.

Refer to section 15.3.9, Setting the SDRAM Configuration Setting Register, for details on the memory configurations supported by DBSC3. For details on the relationship between the chip select and address pins of the SDRAM and the logical addresses of this LSI, refer to section 15.3.10, Address Multiplexing.

Notes: 1. Memory Configuration Supported
• 32-bit bus configuration connected with two 16-bit wide SDRAM modules
2. Although DBSC3 supports the connection of multiple SDRAM modules, the electrical characteristics of some chips may impose a limitation on the number of connectable SDRAM modules.
3. This register must only be written from within the initialization sequence (see section 15.3.4, Initialization Sequence).
4. Writing to this register should only be performed when the following conditions are met:
• Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
• Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
5. Specify predetermined bit values based on the product type.

15.2.8 PHY Type Setting Register (DBPHYTYPE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PHYTYPE	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	PHYTYPE	00	R/W	PHY Type Setting Bits 00: initial setting Other settings are prohibited.

Notes: 1. This register must only be written from within the initialization sequence (see section 15.3.4, Initialization Sequence).

2. Writing to this register should only be performed when the following conditions are met.
   - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.9 SDRAM Timing Register 0 (DBTR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	CL	0000	R/W	CAS Latency Setting Bits These bits are for setting the CAS latency of the SDRAM. 0011: 3 cycles : 1110: 14 cycles Other settings are prohibited.

DBTR0 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.10 SDRAM Timing Register 1 (DBTR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CWL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	CWL	0000	R/W	CAS Write Latency Setting Bits These bits are for setting the CAS-write latency of the SDRAM. 0010: 2 cycles : 1010: 10 cycles Other settings are prohibited.

DBTR1 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.11 SDRAM Timing Register 2 (DBTR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	AL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	AL	0000	R/W	Additive Latency Setting Bits These bits are for setting the additive latency of the SDRAM. 0000: 0 cycles Other settings are prohibited.

DBTR2 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.12 SDRAM Timing Register 3 (DBTR3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TRCD				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4 to 0	TRCD	00000	R/W	ACT to READ/ACT to WRITE Interval Setting Bits These bits set the minimum interval from an ACT command to a READ/WRITE command. 00011: 3 cycles : 11111: 31 cycles Other settings are prohibited.

DBTR3 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.13 SDRAM Timing Register 4 (DBTR4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	TRPA				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TRP				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
20 to 16	TRPA	00000	R/W	PREA Time Setting Bits These bits set the minimum interval from a PREA (precharge all banks) command to an ACT/REF command. The value set in these bits must be greater than or equal to that in the TRP bits. 00011: 3 cycles : 11111: 31 cycles Other settings are prohibited.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4 to 0	TRP	00000	R/W	PRE Time Setting Bits These bits set the minimum interval from a PRE (precharge) command to an ACT/REF command. 00011: 3 cycles : 11111: 31 cycles Other settings are prohibited.

DBTR4 is used to set timing parameters for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The following conditions must be satisfied:
TRPA ≥ TRP
TRC – TRP < 32
3. Writing to this register should only be performed when the following conditions are met.
• Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
• Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.14 SDRAM Timing Register 5 (DBTR5)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TRC					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TRC	000000	R/W	ACT to ACT/ACT to REF Interval Setting Bits These bits set the minimum interval from one ACT command to another ACT command (for the same bank) or to a REF command. 000110: 6 cycles : 111111: 63 cycles Other settings are prohibited.

DBTR5 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The following condition must be satisfied: TRC – TRP < 32
3. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.15 SDRAM Timing Register 6 (DBTR6)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TRAS					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TRAS	000000	R/W	ACT to PRE Interval Setting Bits These bits set the minimum interval from an ACT command to a PRE command. 000011: 3 cycles : 100010: 34 cycles Other settings are prohibited.

DBTR6 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.

2. Writing to this register should only be performed when the following conditions are met.
   - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.16 SDRAM Timing Register 7 (DBTR7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TRRD			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TRRD	0000	R/W	ACT(A) to ACT(B) Interval Setting Bits These bits set the minimum interval between ACT commands issued for different banks. 0010: 2 cycles : 1111: 15 cycles Other settings are prohibited.

DBTR7 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.

2. Writing to this register should only be performed when the following conditions are met.
   - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.17 SDRAM Timing Register 8 (DBTR8)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TFAW							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
7 to 0	TFAW	00000000	R/W	Four Activate Window Length Setting Bits These bits set the length of the four activate window. The value of these bits must be at least four times as large as that of the TRRD bits in DBTR7. 00001000: 8 cycles : 00111111: 63 cycles Other settings are prohibited.

DBTR8 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The following condition must be satisfied: TFAW $\geq 4 \times$ TRRD.
3. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.18 SDRAM Timing Register 9 (DBTR9)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TRDPR			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TRDPR	0000	R/W	READ-PRE Interval Setting Bits These bits set the minimum interval from a READ command to a PRE command. 0100: 4 cycles : 1111: 15 cycles Other settings are prohibited.

DBTR9 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The following condition must be satisfied: TRDPR ≥ BL/2.
3. If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.
   TRDPR = max {4, ceil(tRTP / tCK)}
4. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.19 SDRAM Timing Register 10 (DBTR10)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TWR			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TWR	0000	R/W	Write-Recovery Period Setting Bits These bits set the write-recovery period. 0011: 3 cycles 0100: 4 cycles : 1110: 14 cycles Other settings are prohibited.

DBTR10 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.20 SDRAM Timing Register 11 (DBTR11)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TRDWR					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TRDWR	000000	R/W	READ to WRITE Interval Setting Bits These bits set the minimum interval from a READ command to a WRITE command. 000110: 6 cycles 000111: 7 cycles : 001111: 15 cycles Other settings are prohibited.

DBTR11 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.

2. If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.

   When the number of (CL + (BL/2) + 2 - CWL) is even:

   $$TRDWR > CL + (BL/2) + 2 - CWL$$

   Otherwise:

   $$TRDWR \geq CL + (BL/2) + 2 - CWL$$

3. Writing to this register should only be performed when the following conditions are met.
   - Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   - Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.21 SDRAM Timing Register 12 (DBTR12)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	TWRRD					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
5 to 0	TWRRD	000000	R/W	WRITE to READ Interval Setting Bits These bits set the minimum interval from a WRITE command to a READ command. 000110: 6 cycles : 011111: 31 cycles Other settings are prohibited.

DBTR12 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The following condition must be satisfied: TWRRD ≥ CWL + BL/2.
3. If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.
   TWRRD = CWL + 4 + ceil(tWTR / tCK)
4. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.22 SDRAM Timing Register 13 (DBTR13)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TRFC/TRFCAB											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 0	TRFC/TRFCAB	H'000	R/W	REF to ACT/REF or All Bank REF to ACT/REF Interval Setting Bits These bits set the minimum interval from a REF (refresh) command for all the banks to an ACT/REF command. H'008: 8 cycles : H'1FF: 511 cycles Other settings are prohibited.

DBTR13 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.23 SDRAM Timing Register 14 (DBTR14)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCKEHDLL							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TCKEH							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
23 to 16	TCKEHDLL	H'00	R/W	CKEH (DLL-LOCK) Period Setting Bits These bits set the minimum interval from the time the CKE signal goes high until the issuing of a further valid command that requires the DLL to be locked. H'02: 2 cycles : H'17: 23 cycles Other settings are prohibited.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
7 to 0	TCKEH	H'00	R/W	CKEH Period Setting Bits These bits set the minimum interval from the time the CKE signal goes high until the issuing of a further valid command. H'02: 2 cycles : H'0F: 15 cycles Other settings are prohibited.

DBTR14 is used to set timing parameters for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.

2. The following condition must be satisfied: TCKEH ≤ TCKEHDLL.
3. When the power-down mode is to be used, this register must be set accordingly.
   If the SDRAM in use conforms to the JEDEC standard, the value of the bits can be calculated from the following formula.
   TCKEHDLL = ceil(tXPDLL / tCK)
   TCKEH = ceil(tXP / tCK)
4. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.24 SDRAM Timing Register 15 (DBTR15)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TCKESR			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	TCKEL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
19 to 16	TCKESR	0000	R/W	CKESR Period Setting Bits These bits set the minimum time for self-refresh from the time the CKE signal goes low until it goes high. 0010: 2 cycles 0011: 3 cycles : 1111: 15 cycles Other settings are prohibited.
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	TCKEL	0000	R/W	CKEL Period Setting Bits These bits set the minimum time for power down from the time the CKE signal goes low until it goes high. 0010: 2 cycles 0011: 3 cycles : 0111: 7 cycles Other settings are prohibited.

DBTR15 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.25 SDRAM Timing Register 16 (DBTR16)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DQIENLTNCY				—	—	—	—	—	—	DQL					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DQENLTNCY				—	—	—	—	—	—	—	—	WDQL			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	DQIENLTNCY	0000	R/W	dqienltncy Setting Bits 0001: One cycles Other settings are prohibited.
27 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
21 to 16	DQL	000000	R/W	dqltncy Setting Bits These bits set the latency from issuing of a read command to the PHY unit 000111: 7 cycles : 111111: 63 cycles Other settings are prohibited.
15 to 12	DQENLTNCY	0000	R/W	dqenltncy Setting Bits 0001: One cycle Other settings are prohibited.
11 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	WDQL	0000	R/W	wdqltncy Setting Bits These bits set the latency from issuing of a write command until the write data is output. 0001: One cycle Other settings are prohibited.

DBTR16 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The DQL setting should satisfy the following conditions:
Minimum value for DDR3-800 (MCK[*] is 400 MHz or lower): CL + 15
Minimum value for DDR3-800 (MCK[*] is higher than 400 MHz): CL + 16
3. Writing to this register should only be performed when the following conditions are met.
• Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
• Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.26 SDRAM Timing Register 17 (DBTR17)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TMOD					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
21 to 16	TMOD	000000	R/W	MRS Time Setting Bits These bits indicate the minimum interval from an MRS (mode register set) command to a subsequent command. 000010: 2 cycles : 001111: 15 cycles Other settings are prohibited.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

DBTR17 is used to set timing parameters for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.27 SDRAM Timing Register 18 (DBTR18)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	RODTL			—	—	—	—	—	RODTA		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	WODTL			—	—	—	—	—	WODTA		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
26 to 24	RODTL	000	R/W	Bits for ODT Assert Period Setting at Read These bits set the assert period of the ODT signal that is output when a read command is output. 000: BL/2 cycles 001: BL/2 + 1 cycle : 111: BL/2 + 7 cycles Other settings are prohibited.
23 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
18 to 16	RODTA	000	R/W	Bits for ODT Assert Start Timing Setting Bits Read These bits set the assert start timing for the ODT signal that is output when a read command is output. 000: Simultaneous with the read command 001: One cycle after the read command 010: Two cycles after the read command 011: Three cycles after the read command Other settings are prohibited.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	WODTL	000	R/W	Bits for ODT Assert Period Setting at Write These bits set the assert period of the ODT signal that is output when a write command is output. 000: BL/2 cycles 001: BL/2 cycles + 1 cycle : 111: BL/2 cycles + 7 cycles Other settings are prohibited.
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
2 to 0	WODTA	000	R/W	Bits for ODT Assert Start Timing Setting at Write These bits set the assert start timing for the ODT signal that is output when a write command is output. 000: Simultaneous with the write command 001: One cycle after the write command 010: Two cycles after the write command 011: Three cycles after the write command Other settings are prohibited.

DBTR18 is used to set timing parameters for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
3. The following conditions must be satisfied when setting this register:
   RODTL + RODTA ≤ 7
   WODTL + WODTA ≤ 7

15.2.28 SDRAM Timing Register 19 (DBTR19)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TZQCS							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
7 to 0	TZQCS	00000000	R/W	Calibration Period Setting Bits These bits specify the minimum interval from a ZQCS (short calibration) command to the next command. 00000110: 6 cycles 00000111: 7 cycles : 01000000: 64 cycles : 11111111: 255 cycles Other settings are prohibited.

DBTR19 is used to set a timing parameter for the SDRAM.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. The following condition must be satisfied:
TZQCS ≥ TMOD
3. Writing to this register should only be performed when the following conditions are met.
• Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
• Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.29 SDRAM Operation Setting Register (DBBL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BL	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	BL	00	R/W	Burst Length Setting Bits These bits specify the burst length of SDRAM. 00: Fixed to 8 Other settings are prohibited.

DBBL is used to set a burst operation mode of the memory.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.30 DBSC3 Operation Adjustment Register 0 (DBADJ0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FREQRATIO	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CAMODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	FREQRATIO	00	R/W	PHY Frequency Ratio Setting Bits These bits should be set to 01 (1:2 operating mode). 01: DBSC3: PHY frequency ratio is 1:2. Other settings are prohibited.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	CAMODE	0	R/W	Command/Address Output Mode Setting Bit When the CAMODE bit is 1, the DBSC3 outputs a single command per two clock cycles. In this case, command signals and address signals, except for the M0CS[1:0]# signals of SDRAM, are kept constant for two clock cycles. During this period, the CS# signal becomes low only in the latter one clock cycle. 0: Setting prohibited 1: One command output in two clock cycles

DBADJ0 adjusts the DBSC3 operation.

Note: Writing to this register should only be performed when access to the SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0).

15.2.31 DBSC3 Operation Adjustment Register 2 (DBADJ2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ACAPC0								—	—	—	—	ACAPX0			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 8	ACAPC0	H'00	R/W	H'20 (fixed value) Other settings are prohibited.
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
3 to 0	ACAPX0	H'0	R/W	Bits for Setting Transaction Count Acceptable by Device Control Unit (for the low priority port) These bits set the number of requests acceptable by the device control unit (for the low priority port) in the DBSC3 in transaction units. H'4: fewer value H'8: default value Other settings are prohibited. If you want to reduce average access latency, please set this bit to H'8. If you want to reduce worst access latency, please set this bit to H'4.

DBADJ2 adjusts the DBSC3 operation.

Notes: 1. Writing to this register should only be performed when access to the SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0).

2. The display unit module requires to set ACAPX0 and ACAPX1 to H'4.

15.2.32 Refresh Configuration Register 0 (DBRFCNF0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	REFTHF											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 0	REFTHF	H'000	R/W	Forcible Auto-Refresh Threshold Setting Bits These bits set the timing for forcible refreshing regardless of bus requests. The value represented by these bits affects the amount of jitter in the refresh interval and performance in access to memory. A smaller value means less jitter in the refresh interval but may reduce performance in access. For details on the amount of jitter in the refresh interval, see section 15.2.33, Refresh Configuration Register 1 (DBRFCNF1). H'080: 128 cycles : H'1FF: 511 cycles Other settings are prohibited.

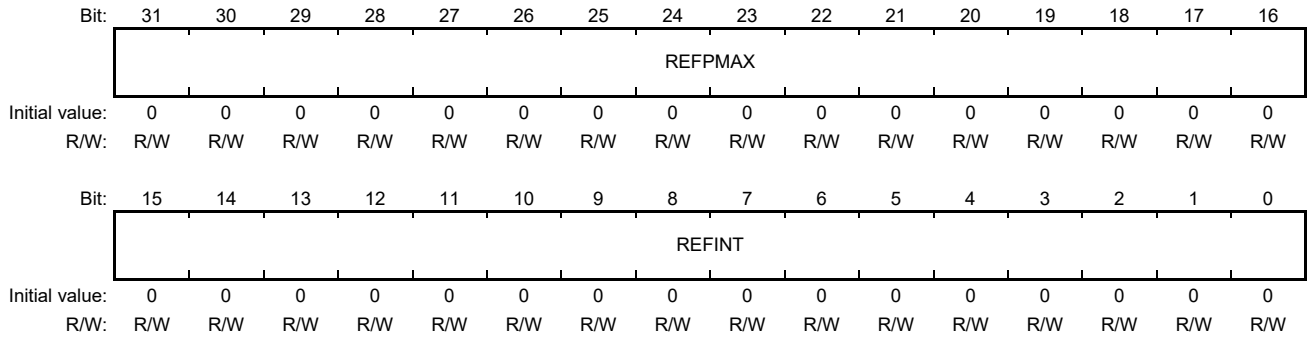
DBRFCNF0 is used to set the timing for refreshing of the SDRAM.

If you change the value of this register while auto-refresh is active (i.e. the ARFEN bit in the DBRFEN register is 1), the auto-refresh facility must be re-activated to reflect the new value in refreshing. To re-activate the auto-refresh facility, write 1 to the ARFEN bit in the DBRFEN register.

Notes: 1. If auto-refresh is activated (i.e. the ARFEN bit in the DBRFEN register is set to 1) after a value smaller than the minimum value defined in the above table has been set in this register, correct operation cannot be guaranteed.

2. The following conditions must be satisfied:
   REFTHF ≥ (TCKEL + TCKEH) + REFTH0
   (REFTH0 = max (TRDPR, CWL + (BL/2) + TWR, TRAS, TRC – TRP) + TRPA + 24)

15.2.33 Refresh Configuration Register 1 (DBRFCNF1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	REFPMAX	H'0000	R/W	Maximum Post Number of Refresh Commands Setting Bits These bits set the maximum number of refresh commands (post number) accumulated by auto-refresh. As long as the number of refresh commands that has been accumulated is smaller than REFPMAX, refresh commands are issued while there are no bus requests. H'0002: Two (minimum amount of jitter in the refresh interval) : H'0008: Eight cycles (maximum amount of jitter in the refresh interval) Other settings are prohibited.
15 to 0	REFINT	H'0000	R/W	Average Refresh Interval Setting Bits These bits set the average interval for issuing of refresh commands. When the REFINTS bit of the DBRFCNF2 register is 0, the average interval (in cycles) is REFINT. When the REFINTS bit of the DBRFCNF2 register is 1, on the other hand, the average interval (in cycles) is floor (REFINT/2). This average interval is hereafter referred to as REFINT_E. Thus, REFINT_E = REFINT >> REFINTS (>>: logical right-shift operator). H'0080: 128 cycles H'0081: 129 cycles : H'3FFF: 16383 cycles Other settings are prohibited.

DBRFCNF1 is used to set the timing for refreshing of the SDRAM.

If you change the value of this register while auto-refresh is active (i.e. the ARFEN bit in the DBRFEN register is 1), the auto-refresh facility must be re-activated to reflect the new value in refreshing. To re-activate the auto-refresh facility, write 1 to the ARFEN bit in the DBRFEN register.

In the descriptions below, the "number of cycles" unless otherwise specified means the value measured with the SDRAM clock.

(1) Register Settings and Refresh Generation Timing

The following is an example of the settings in refresh configuration registers 1 and 2 and the timing of refresh generation.

In the explanations, "a ± b" indicates the range of values from a - b to a + b.

(a) To make the refresh interval flexible

Set REFPMAX to a value greater than or equal to 2.

REFINT holds the setting for the average refresh interval (tREFI in the normal range of operating temperatures), which is given in memory-vendor datasheets as an integer number of cycles. Set a value that has been rounded down from this integer. Set REFINTS to 0 or 1 according to the temperature at the time.

In this case, taking n as a positive integer, the time from one round of refresh generation to refresh generation n rounds later is (n × REFINT_E + REFPMAX × REFINT_E cycles) or shorter. However, this is on the assumption of no writing to the DBRFEN register during this period.

The following condition must be satisfied:

REFINT ≥ (TCALRZ + TCALZR + REFTHF × 2) << REFINTS

Notes: 1. If auto-refresh is activated (i.e. the ARFEN bit in the DBRFEN register is set to 1) after a value smaller than the minimum value defined in the above table has been set in this register, correct operation cannot be guaranteed.
2. Other restrictions not mentioned in the above may apply to some types of SDRAM according to the PHY unit specifications.

15.2.34 Refresh Configuration Register 2 (DBRFCNF2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	REFPMIN			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REF INTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

In the descriptions below, the number of cycles means the value measured with the SDRAM clock unless otherwise specified.

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
19 to 16	REFPMIN	H'0	R/W	Minimum Post Number of Refresh Commands Setting Bits These bits set the minimum number of refresh commands (post number) accumulated by auto-refresh. As long as the number of refresh commands that has been accumulated is smaller than REFPMIN, refresh commands are issued irrespective of the bus request state. H'1: 1 Other settings are prohibited.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	REFINTS	0	R/W	Average Refresh Interval Adjustment Bit When this bit is 0, the average interval (in cycles) is the value set in the REFINT bits. When this bit is 1, on the other hand, the average interval (in cycles) is floor (REFINT/2). 0: Average interval is REFINT 1: Average interval is 1/2 REFINT

DBRFCNF2 is used to set the timing for refreshing of the SDRAM.

If you change the value of this register while auto-refresh is active (i.e. the ARFEN bit in the DBRFEN register is 1), the auto-refresh facility must be re-activated to reflect the new value in refreshing. To re-activate the auto-refresh facility, write 1 to the ARFEN bit in the DBRFEN register.

The following condition must be satisfied:
REFPMAX ≥ REFPMIN

15.2.35 DDR3-SDRAM Calibration Configuration Register (DBCALCNF)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	CALEN	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CALINT															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
24	CALEN	0	R/W	DDR3-SDRAM Calibration Enable Bit While this bit is set to 1, calibration of DDR3-SDRAM is executed (ZQCS command is issued) at regular intervals. 0: DDR3-SDRAM calibration is disabled. 1: DDR3-SDRAM calibration is enabled.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 0	CALINT	H'0000	R/W	DDR3-SDRAM Calibration Frequency Setting Bits These bits adjust the frequency of DDR3-SDRAM calibration. When the CALINT bits are set to n, the ZQCS command is issued once every time the refresh command has been issued for n times by the auto-refresh function. H'0000: Executed only once after auto-refresh executed immediately after the CALEN bit is set to 1. H'0001: Executed at every auto-refresh. H'0002: Executed at every two times of auto-refresh. : H'FFFF: Executed at every 65535 times of auto-refresh.

DBCALCNF controls the function for calibrating DDR3-SDRAM at regular intervals.

Notes: 1. When CALINT = 0, calibration is executed (ZQCS command is issued) only once after auto-refresh executed immediately after 1 is written to the CALEN bit; no calibration is executed after that. To execute calibration again, write 1 to the CALEN bit.

2. Even when the CALEN bit is set to 1, the ZQCS command is not issued when the auto-refresh function is stopped (i.e. the ARFEN bit in the DBRFEN register is 0).
3. Writing a value other than H'0100 0000 to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)
4. Writing H'0100 0000 to this register should only be performed when the following condition is met.
   • Auto-refresh is enabled (i.e. the ARFEN bit in the DBRFEN register is 1)

15.2.36 DDR3-SDRAM Calibration Timing Register (DBCALTR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	TCALRZ											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TCALZR											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
27 to 16	TCALRZ	H'000	R/W	DDR3-SDRAM Calibration Timing Setting (REF to ZQCS Interval Setting) Bits These bits specify the minimum interval between a REF and ZQCS commands for calibration execution. H'080: 128 cycles : H'FFF: 4095 cycles Other settings are prohibited.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11 to 0	TCALZR	H'000	R/W	DDR3-SDRAM Calibration Timing Setting (ZQCS to REF Interval Setting) Bits These bits specify the minimum interval between a ZQCS command for calibration and a REF command for the next auto-refresh execution. H'080: 128 cycles : H'FFF: 4095 cycles Other settings are prohibited.

DBCALTR specifies the command interval limitations for DDR3-SDRAM calibration executed at regular intervals.

Notes: 1. This register value has no effect when CALEN = 0.
2. The setting is in cycles of the SDRAM operating clock.
3. The following conditions must be satisfied:
   TCALRZ ≥ max (128, TRFC + (7 × TFAW ÷ 4) + tACTANY + 32)
   TCALZR ≥ max (128, TZQCS + (7 × TFAW ÷ 4) + tACTANY + 32)
   REFINT ≥ (TCALRZ + TCALZR + (REFTHF × 2)) << REFINTS
   (tACTANY = max (TRCD, TRAS, TRC – TRPA, TFAW))
4. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
   • Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.37 ODT Operation Setting Register (DBRNK0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RODT OUT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WODT OUT0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
16	RODTOUT0	0	R/W	Bit for ODT Output Level Setting at Read This bit set the ODT output level at read. 0: ODT output level at read is set to 0. 1: ODT output level at read is set to 1.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
0	WODTOUT0	0	R/W	Bit for ODT Output Level Setting at Write This bit set the ODT output level at write. 0: ODT output level at write is set to 0. 1: ODT output level at write is set to 1.

DBRNK0 specifies the ODT output level of SDRAM.

Note: Writing to this register should only be performed when the following conditions are met.

- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.38 Power-Down Configuration Register (DBPDNCNF)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PDWAIT								—	—	—	PDDLL	—	—	PDMODE	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
15 to 8	PDWAIT	H'00	R/W	Power-Down Wait Bits These bits set the number of cycles it takes to enter power-down mode after memory accesses no longer occur. H'10: 16 cycles : H'FF: 255 cycles Other settings are prohibited.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4	PDDLL	0	R/W	Power-Down DLL Control Bit This bit turns on or off the DLL of SDRAM when entering power-down mode. 0: DLL is turned off at a precharged power-down. DLL is turned on at an active power-down 1: DLL is turned on at a power-down.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	PDMODE	00	R/W	Power-Down Mode Bits When these bits are set to "01" and there has been no memory access for a certain period, the power-down entry command is issued to place the SDRAM in power-down mode. 00: Auto power-down mode is off. 01: Auto power-down mode is on. Other settings are prohibited.

DBPDNCNF controls the auto power-down function.

Notes: 1. The setting is in cycles of the SDRAM operating clock.
2. Return from a power-down mode incurs a time penalty of max(3, TCKEH) - 3 cycles.
3. Writing to this register should only be performed when the following conditions are met.
• Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
• Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.39 PHY Unit Control Register 0 (DBPDCNT0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BW32	—	—	—	—	—	—	—	—	—	—	ODT_DIS	—	—	ODT_TSEL	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	BW32	0	R/W	PHY Unit 32-Bit Mode Setting Bit Set either the BW32 bit. Set this bit and the DW0 bit in DBCONF0 to the same value. 1: PHY unit 32-bit mode
30 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
20	ODT_DIS	0	R/W	Internal ODT Enable Bit This bit enables or disables the ODT in the PHY unit. Set this bit to 0 in most cases. 0: ODT is enabled. 1: ODT is disabled.
19, 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
17, 16	ODT_TSEL	00	R/W	Internal ODT Impedance Setting Bits These bits set the ODT impedance in the PHY unit. 01: 60 Ω for DDR3 (normal setting) Other settings are prohibited.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

DBPDCNT0 is used to set parameters for the PHY unit.

Note: Writing to this register should only be performed when the following conditions are met.
- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.40 PHY Unit Control Register 1 (DBPDCNT1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

DBPDCNT1 is used to set parameters for the PHY unit.

Note: Writing to this register should only be performed when the following conditions are met.

- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.41 PHY Unit Control Register 2 (DBPDCNT2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	NC_SIG									NC_FIX	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
26 to 18	NC_SIG	H'000	R/W	Fixed Control Signal Setting Bits These bits select the signals that output the fixed value specified in the NC_FIX bits. When a bit is set to 1, the corresponding signal outputs the fixed value. NC_SIG[8]: M0(/1)RESET# NC_SIG[7]: M0(/1)A[15] NC_SIG[6]: M0(/1)A[14] NC_SIG[5]: M0(/1)A[13] NC_SIG[4]: M0(/1)BA[2] NC_SIG[3]: M0(/1)CS[1]#, M0(/1)CKE[1], and M0(/1)ODT[1] NC_SIG[2]: M0(/1)CS[0]#, M0(/1)CKE[0], and M0(/1)ODT[0] NC_SIG[1]: M0(/1)CK[1] and M0(/1)CK[1]# NC_SIG[0]: M0(/1)CK[0] and M0(/1)CK[0]#
17, 16	NC_FIX	00	R/W	Control Signal Fixed Value Setting Bits These bits specify the state of the signals selected by the NC_SIG bits. 00: Not fixed 01: Initial value (reset state) 10: Hi-Z state 11: Setting prohibited
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

DBPDCNT2 is used to set parameters for the PHY unit.

Note: Writing to this register should only be performed when the following conditions are met.

- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.42 PHY Unit Control Register 3 (DBPDCNT3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PLL2_RESET	—	STBY		COM_HIZ	—	—	DLL_RESET	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R	R	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	IO_ENABLE	—	CAL MODE	CAL EN	—	PTRRST	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R/W	R/W	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	PLL2_RESET	0	R/W	Reset Signal Bit for PLL2 in PHY Unit This bit resets PLL2 in the PHY unit. For details, refer to section 15.3.4, Initialization Sequence. 0: PLL2 is reset. 1: PLL2 reset is released.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
29, 28	STBY	00	R/W	Clock Signal Standby Setting Bits These bits specify the standby state for the clock signals. When this bit is set to 0, the clock signals enter standby state. This setting takes priority over the NC_SIG and NC_FIX bit settings. For details, refer to section 15.3.4, Initialization Sequence. STBY[1]: M0(/1)CK[1] and M0(/1)CK[1]# STBY[0]: M0(/1)CK[0] and M0(/1)CK[0]#
27	COM_HIZ	0	R/W	Control Signal Hi-Z Setting Bit When this bit is set to 1, the I/O pins, except for M0(/1)CK[1:0], M0(/1)CK[1:0]#, M0(/1)CKE[1:0], and M0(/1)RESET#, enter Hi-Z state. This setting is not applied to the pins specified by the NC_SIG and NC_FIX bits.
26, 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
24	DLL_RESET	0	R/W	DLL Reset Bit When this bit is set to 0, the DLL is reset. When this bit is set to 1, the DLL reset state is released. For details, refer to section 15.3.4, Initialization Sequence. 0: DLL is reset. 1: DLL reset is released.
23 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

Bit	Bit Name	Initial Value	R/W	Description
13	IO_ENABLE	0	R/W	I/O Enable Setting Bit This bit enables I/O operation. For details, refer to section 15.3.4, Initialization Sequence. 0: I/O operation is disabled. 1: I/O operation is enabled.
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
11	CALMODE	0	R/W	Calibration Mode Setting Bit This bit specifies the calibration mode. For details, refer to section 15.3.4, Initialization Sequence. 0: External control mode 1: Automatic calibration mode
10	CALEN	0	R/W	Automatic Calibration Setting Bit This bit enables automatic calibration. This bit setting is valid only when CALMODE = 1. For details, refer to section 15.3.4, Initialization Sequence. 0: Automatic calibration is disabled. 1: Automatic calibration is enabled.
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
8	PTRRST	0	R/W	Pointer Reset Bit When this bit is set to 1, the point is reset. When this bit is cleared to 0, the pointer reset state is released. For details, refer to section 15.3.4, Initialization Sequence. 1: Pointer is reset. 0: Pointer reset is released.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.

DBPDCNT3 is used to set parameters for the PHY unit.

Note: Writing to this register should only be performed when the following conditions are met.

- Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)
- Auto-refresh is disabled (i.e. the ARFEN bit in the DBRFEN register is 0)

15.2.43 Bus Control Unit 0 Control Register 1 (DBBS0CNT1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	BKADM	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
1, 0	BKADM	00	R/W	Bank Assignment Setting Bits These bits are used to set the method for assigning the SDRAM banks to the logical address space, i.e. whether and how logical addresses are divided into multiple blocks to which different SDRAM banks are assigned. For details on the relation between the logical addresses and SDRAM addresses, refer to section 15.3.10, Address Multiplexing. 00: The whole logical address space is regarded as one block. Other settings are prohibited.

Notes: 1. This register must only be written from within the initialization sequence (see section 15.3.4, Initialization Sequence).

2. Writing to this register should only be performed when the following conditions are met.
   • Access to SDRAM is disabled (i.e. the ACCEN bit in the DBACEN register is 0)

15.2.44 AXI Port Setting Register 0 (DBWT0CNF0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	WASYN		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	WCN		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
18 to 16	WASYN	000	R/W	"010" Other settings are prohibited.
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
2 to 0	WCN	000	R/W	AXI Clock to Memory Clock Ratio Setting Bits These bits specify the ratio of the memory clock/4 (MCLK) to the AXI clock (AXICLK). When WASYN = 010, 000: 0.5 MCLK < AXICLK < MCLK (default) 001: MCLK < AXICLK < 1.2 MCLK 010: 1.2 MCLK < AXICLK < 1.4 MCLK 011: 1.4 MCLK < AXICLK < 1.6 MCLK 100: 1.6 MCLK < AXICLK < 1.8 MCLK 101: 1.8 MCLK < AXICLK < 2 MCLK Other settings are prohibited.

Note: This register should only be written to only during the initialization sequence (refer to section 15.3.4, Initialization Sequence) or while AXI bus access and external memory access are idle.

15.2.45 AXI Port Setting Register 4 (DBWT0CNF4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	RDFIIFONUM				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0. If a value other than 0 is written, correct operation cannot be guaranteed.
4 to 0	RDFIIFONUM	00000	R/W	This bit specifies the capacity of the read data FIFO. 11111: 32 Other settings are prohibited.

Note: This register should only be written to only during the initialization sequence (refer to section 15.3.4, Initialization Sequence).

15.3 Operation

15.3.1 Supported SDRAM Commands

Table 15.5 lists the SDRAM commands issued by the DBSC3. These commands are issued to the SDRAM in synchronously with the M0CK[1:0] and M0CK[1:0]# signals. In the table, "n-1" indicates the state of the signal applied to the SDRAM one cycle before SDRAM command issue; n indicates the state of the signal at the time of command issue.

Table 15.5 SDRAM Commands Issued by the DBSC3

Function	Symbol	MCKE[1:0]		MCS [1:0]#	MRAS#	MCAS#	MWE#	MBA [2:0]	MA [15:3]	MA12 /BC	MA10 /AP	MA11, MA[9:0]
		n-1	n									
Device deselected	DES	H	H	H	X	X	X	X	X	X	X	X
Read	READ	H	H	L	H	L	H	V	V	V	L	V
Write	WRITE	H	H	L	H	L	L	V	V	V	L	V
Bank activate	ACT	H	H	L	L	H	H	V	V	V	V	V
Precharge select bank	PRE	H	H	L	L	H	L	V	V	V	L	V
Precharge all banks	PREA	H	H	L	L	H	L	V	V	V	H	V
Auto-refresh	REF	H	H	L	L	L	H	V	V	V	V	V
Self-refresh entry	SRE	H	L	L	L	L	H	V	V	V	V	V
Self-refresh exit	SRX	L	H	H	V	V	V	V	V	V	V	V
				L	H	H	H					
Power down entry	PDE	H	L	L	H	H	H	V	V	V	V	V
				H	V	V	V					
Power down exit	PDX	L	H	L	H	H	H	V	V	V	V	V
				H	V	V	V					
Mode register set	MRS	H	H	L	L	L	L	V	V	V	V	V
ZQ calibration short issue	ZQCS	H	H	L	H	H	L	X	X	X	H	X
ZQ calibration long issue	ZQCL	H	H	L	H	H	L	X	X	X	L	X

[Legend]

H: High level

L: Low level

X: High or low level (don't care)

V: Valid data

In the table, corrective names are used for signals. For example, MCKE and MA indicate M0CKE and M0A signals, respectively.

The above DES command is issued when the SDRAM is not accessed, and so cannot be explicitly issued by the user.

15.3.2 Data Alignment in DDR3-SDRAM

The DBSC3 accesses DDR3-SDRAM with a fixed burst length of 8 (Figure 15.3). As shown in table 15.6, invalid read data is discarded during reading, and data mask signals are used to mask invalid data during writing, according to the access size. The access times in table 15.6, correspond to the burst times during reading/writing shown in Figure 15.3. For example, in the case of little endian, the second access (falling edge of MDQS) includes valid data if a byte access of address (8n + 0, 1, 2, 3) occurs.

Tables 15.7 and 15.8 show the correspondence with data on the external data bus for each access size.

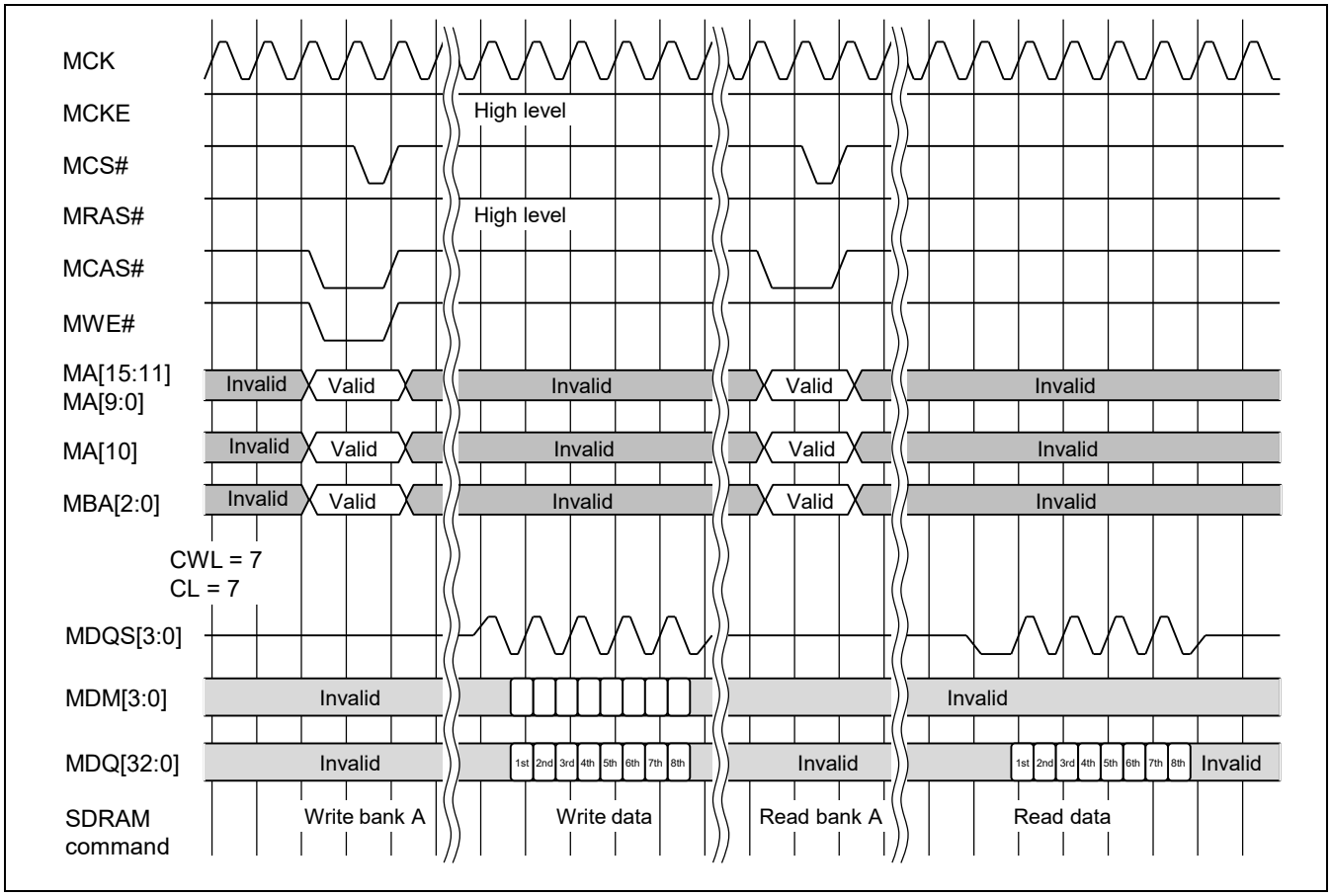


Figure 15.3 Burst Access Operation

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Table 15.6 Positions of Valid Data for Access with Burst Length of 8 (32-Bit Mode)

Address	First Access	Second Access	Third Access	Fourth Access	Fifth Access	Sixth Access	Seventh Access	Eighth Access
Byte access (address 8n + 0, 1, 2, 3)	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Byte access (address 8n + 4, 5, 6, 7)	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Byte access (address 8n + 8, 9, 10, 11)	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid
Byte access (address 8n + 12, 13, 14, 15)	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid
Byte access (address 8n + 16, 17, 18, 19)	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid
Byte access (address 8n + 20, 21, 22, 23)	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid
Byte access (address 8n + 24, 25, 26, 27)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid
Byte access (address 8n + 28, 29, 30, 31)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid
Word access (address 8n + 0, 2)	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Word access (address 8n + 4, 6)	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Word access (address 8n + 8, 10)	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid
Word access (address 8n + 12, 14)	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid
Word access (address 8n + 16, 18)	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid
Word access (address 8n + 20, 22)	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid
Word access (address 8n + 24, 26)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid
Word access (address 8n + 28, 30)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid
Longword access (address 8n + 0)	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Longword access (address 8n + 4)	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Longword access (address 8n + 8)	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid
Longword access (address 8n + 12)	Invalid	Invalid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid
Longword access (address 8n + 16)	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid
Longword access (address 8n + 20)	Invalid	Invalid	Invalid	Invalid	Valid	Invalid	Invalid	Invalid
Longword access (address 8n + 24)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid
Longword access (address 8n + 28)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Invalid
Quadword access (address 8n + 0)	Valid	Valid	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid
Quadword access (address 8n + 8)	Invalid	Invalid	Valid	Valid	Invalid	Invalid	Invalid	Invalid
Quadword access (address 8n + 16)	Invalid	Invalid	Invalid	Invalid	Valid	Valid	Invalid	Invalid
Quadword access (address 8n + 24)	Invalid	Invalid	Invalid	Invalid	Invalid	Invalid	Valid	Valid

Table 15.7 Data Alignment for Access (32-Bit Mode)

Access Size	Address	MDQ31 to MDQ24	MDQ23 to MDQ16	MDQ15 to MDQ8	MDQ7 to MDQ0
Byte	Address 00				Data 7 to 0
	Address 01			Data 7 to 0	
	Address 02		Data 7 to 0		
	Address 03	Data 7 to 0			
	Address 04				Data 7 to 0
	Address 05			Data 7 to 0	
	Address 06		Data 7 to 0		
	Address 07	Data 7 to 0			
	Address 08				Data 7 to 0
	Address 09			Data 7 to 0	
	Address 0A		Data 7 to 0		
	Address 0B	Data 7 to 0			
	Address 0C				Data 7 to 0
	Address 0D			Data 7 to 0	
	Address 0E		Data 7 to 0		
	Address 0F	Data 7 to 0			
	Address 10				Data 7 to 0
	Address 11			Data 7 to 0	
	Address 12		Data 7 to 0		
	Address 13	Data 7 to 0			
	Address 14				Data 7 to 0
	Address 15			Data 7 to 0	
	Address 16		Data 7 to 0		
	Address 17	Data 7 to 0			
	Address 18				Data 7 to 0
	Address 19			Data 7 to 0	
	Address 1A		Data 7 to 0		
	Address 1B	Data 7 to 0			
	Address 1C				Data 7 to 0
	Address 1D			Data 7 to 0	
	Address 1E		Data 7 to 0		
	Address 1F	Data 7 to 0			
Word	Address 00			Data 15 to 8	Data 7 to 0
	Address 02	Data 15 to 8	Data 7 to 0		
	Address 04			Data 15 to 8	Data 7 to 0
	Address 06	Data 15 to 8	Data 7 to 0		
	Address 08			Data 15 to 8	Data 7 to 0
	Address 0A	Data 15 to 8	Data 7 to 0		
	Address 0C			Data 15 to 8	Data 7 to 0
	Address 0E	Data 15 to 8	Data 7 to 0		
	Address 10			Data 15 to 8	Data 7 to 0
	Address 12	Data 15 to 8	Data 7 to 0		
	Address 14			Data 15 to 8	Data 7 to 0
	Address 16	Data 15 to 8	Data 7 to 0		
	Address 18			Data 15 to 8	Data 7 to 0
	Address 1A	Data 15 to 8	Data 7 to 0		
	Address 1C			Data 15 to 8	Data 7 to 0
	Address 1E	Data 15 to 8	Data 7 to 0		
Longword	Address 00	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 04	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 08	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 0C	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 10	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 14	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 18	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 1C	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0

Access Size	Address	MDQ31 to MDQ24	MDQ23 to MDQ16	MDQ15 to MDQ8	MDQ7 to MDQ0
Quadword	Address 00 (First access: address 04)	Data 63 to 56	Data 55 to 48	Data 47 to 40	Data 39 to 32
	Address 00 (Second access: address 00)	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 00 (Third access: address 0C)	Data 63 to 56	Data 55 to 48	Data 47 to 40	Data 39 to 32
	Address 00 (Fourth access: address 08)	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 10 (Fifth access: address 14)	Data 63 to 56	Data 55 to 48	Data 47 to 40	Data 39 to 32
	Address 10 (Sixth access: address 10)	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0
	Address 10 (Seventh access: address 1C)	Data 63 to 56	Data 55 to 48	Data 47 to 40	Data 39 to 32
	Address 10 (Eighth access: address 18)	Data 31 to 24	Data 23 to 16	Data 15 to 8	Data 7 to 0

Table 15.8 Relationships between Data and Addresses (32-Bit Mode)

	First Access	Second Access	Third Access	Fourth Access	Fifth Access	Sixth Access	Seventh Access	Eighth Access
MDQ[7:0]	Address 04	Address 00	Address 0C	Address 08	Address 14	Address 10	Address 1C	Address 18
MDQ[15:8]	Address 05	Address 01	Address 0D	Address 09	Address 15	Address 11	Address 1D	Address 19
MDQ[23:16]	Address 06	Address 02	Address 0E	Address 0A	Address 16	Address 12	Address 1E	Address 1A
MDQ[31:24]	Address 07	Address 03	Address 0F	Address 0B	Address 17	Address 13	Address 1F	Address 1B

15.3.3 SDRAM Command Issue

(1) Basic Access

The DBSC3 stores in a queue the requests received via the AXI. The order for the start of request processing changes according to whether or not this is preceded by processing for precharging or activation, but processing is executed in the order allowed in AXI protocol to improve the memory efficiency.

When SDRAM initialization is completed, upon receiving a read/write request, a page miss occurs with all banks in the closed state. Hence the DBSC3 first issues an activate (ACT) command, to open the corresponding bank. After opening the bank, the read/write command of the SDRAM corresponding to the read/write request is issued. At this time, the number of issued read/write commands differs depending on the bus width and the request size (1/2/4/8/16/32 bytes), as indicated in Figure 15.4. For example, when performing 32-byte reading from the AXI bus with an external data bus width of 16 bits, two read commands are issued. When issuing the read command in the first cycle, data is read with a burst length of 8 (four DDR clock cycles), so that it is necessary to wait until the fifth cycle to issue the second read command.

When access ends, the DBSC3 leaves the bank open, without using a precharge (PRE) command. The bank is closed when (1) the following request is for the same bank with a different row address; (2) there is an auto-refresh request; or (3) the user issues a precharge-all (PREA) command using the SDRAM command control register, for self-refresh processing.

Thus in normal access other than self-refresh, the DBSC3 uses hardware for bank management, so that except for the register settings upon initialization, the user need not execute control.

Furthermore, the DBSC3 performs multibank operation of eight banks. Hence the maximum number of banks that can be opened simultaneously is eight. Refer to section 15.3.10, Address Multiplexing, for the correspondence between access addresses from the AXI and SDRAM bank/row addresses.

Usage Note:

In a command processing, the DBSC3 may change the order of the command execution after acceptance of the command request to improve the memory efficiency. This change is done by the DBSC3 automatically within the allowance of the AXI-bus protocol, so they cannot be explicitly issued by software.

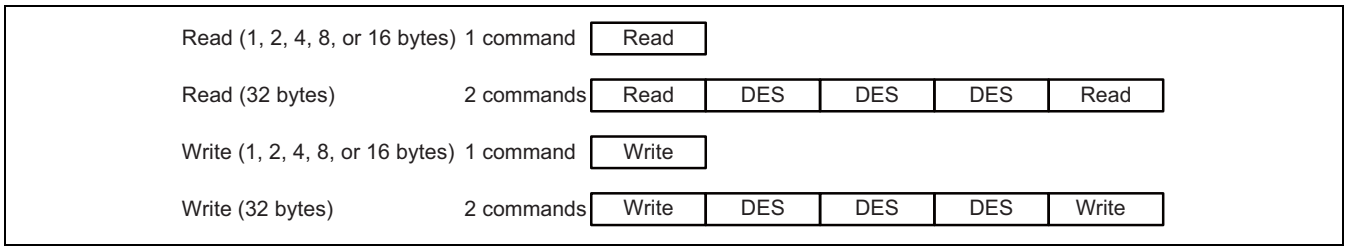


Figure 15.4 Read/Write Command Issued to the SDRAM in Response to the Request from the AXI

(2) Preceding Precharge/Activate Processing

In order to utilize SDRAM multibank functions to reduce SDRAM command vacant cycles insofar as possible and improve the efficiency of bus use, the DBSC3 issues in advance a PRE/ACT command corresponding to the following request queue page miss processing. Only the PRE/ACT command is issued in advance, so there is no change in the read/write order. A PRE/ACT command is issued in advance only when the following request (1) results in a page miss, and moreover (2) entails access of a bank different from that of the request currently being processed. Figure 15.5 shows an example of execution of preceding precharge/activate processing (as an example for operational description). This is an example of a command issued to the SDRAM when the external data bus width is 16 bits, the PRE-ACT minimum time constraint is 4 cycles, the ACT-READ/WRITE minimum time constraint is 4 cycles, and the ACT-ACT minimum time constraint is 2 cycles. In this example, the first through fourth requests are accumulated, and the first request is the request initially provided to the queue.

The DBSC3 issues one command each time it has received two memory clock pulses. Thus, there are always an even number of clock pulses between commands. At time 1, the DBSC3 issues to the SDRAM a PRE command for processing the first read (16-byte) request. Then, when determining the command to be issued at time 3, due to timing constraints it is not possible to issue at time 3 the ACT command necessary as request processing for the first read (16-byte) request, which has higher priority. Hence the DBSC3 searches for a command to be issued at time 3 from the following request queue. From the search results it is seen that preceding precharge processing can be executed for the third read (8-byte) request. Because the DBSC3 gives priority to preceding requests, it decides to perform preceding precharge processing for the third read (8-byte) request, and issues a PRE command to the SDRAM.

At time 5, the DBSC3 can process the first read (16-byte) request and it issues an ACT command to the SDRAM. At time 7, it issues an ACT command to the SDRAM for the first read (8-byte) request processing. After issuing the read command for the first read (16-byte) request processing, it issues a PRE command to the SDRAM for the fourth read (16-byte) request processing at time 11.

Thereafter, the processing described above is repeated.

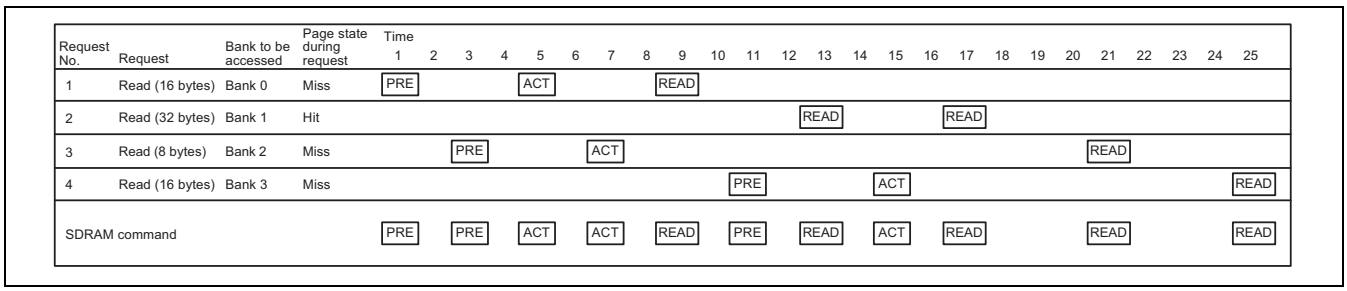


Figure 15.5 Example of Preceding Precharge/Activate Processing

15.3.4 Initialization Sequence

The following shows examples of initialization sequence for each memory type. The initialization sequence should be executed to enable SDRAM access after power to the DBSC3 is turned on.

Note that the sequence differs depending on the specifications of the target memory.

For detailed information such as the power supply and timing parameters, refer to the datasheet for the SDRAM being used.

15.3.4.1 Starting the System

(1) 32 Bits × 1-ch Mode

(a) After power is turned on, apply a power-on reset and wait until the DBSC3 is released from the reset state.

1. Wait until the supplied power, reference voltage, and clock settle (it takes at least 200 µs until the clock settles). Apply a power-on reset to the DBSC3 through the reset pin of the LSI.
2. Set the M0BKPRST# pin to the high level.
3. Write H'0000A55A to DB_ADDR + H'4000.
4. Write H'00000001 to DB_ADDR + H'4008.
5. Use the manual command-issuing register (DBCMD) to set the M0RESET pin of the SDRAM to the low level. The value written to this register should be OPC = RstL, ARG = 0.
6. Use the manual command-issuing register (DBCMD) to set the M0CKE[1:0] pins of SDRAM to the low level. The value written to this register should be OPC = PDEn, ARG = 100 µs.
7. Set the M0SDBUP pin to the high level.

(b) DBSC3 Setting 1

1. SDRAM type setting register (DBKIND)
2. SDRAM configuration setting register 0 (DBCONF0)
3. PHY type setting register (DBPHYTYPE)
4. SDRAM operation setting register (DBBL)
5. SDRAM timing registers 0 to 19 (DBTR0 to DBTR19)
6. ODT operation setting register 0 (DBRNK0)
7. Set the CAMODE bit to 1 in DBSC3 operation adjustment register 0 (DBADJ0).
8. Set the FREQRATIO bit to H'01 in DBSC3 operation adjustment register 0 (DBADJ0).
9. Set the ACAPX0 bits to H'8 in DBSC3 operation adjustment register 2 (DBADJ2).
10. Set the ACAPC0 bits to H'20 in DBSC3 operation adjustment register 2 (DBADJ2).
11. AXI port setting registers 0 and 4 (DBWT0CNF0, DBWT0CNF4)

(c) PHY Setting 1

1. Write to the PHY unit access register3 (DBPDCNT3) as follows.
   - Set the PTRRST bit to 1 in PHY unit control register 3 (DBPDCNT3).
   - Clear the PTRRST bit to 0 in PHY unit control register 3 (DBPDCNT3).
   - Set the CALMODE bit to 1 in PHY unit control register 3 (DBPDCNT3).
   - Set the CALEN bit to 1 in PHY unit control register 3 (DBPDCNT3).
   - Set the DLL_RESET bit to 1 in PHY unit control register 3 (DBPDCNT3).
2. Ensure that the software allows the required waiting time (at least 50 µs).
3. Write to the PHY unit access register3 (DBPDCNT3) as follows. Set the IO_ENABLE bit to 1 in PHY unit control register 3 (DBPDCNT3).
4. Set the PLL2_RESET bit to 1 in PHY unit control register 3 (DBPDCNT3).
5. Ensure that the software allows the required waiting time (at least 100 µs).
6. Set the STBY bit to 1 in PHY unit control register 3 (DBPDCNT3) and the clock is output through the MCK pins.
7. Set the BW32 bit to 1 in PHY unit control register 0 (DBPDCNT0).
8. Make other necessary settings in PHY unit control registers 0 to 3 (DBPDCNT0 to DBPDCNT3).

Usage Note:

However there is no number of order for these sequences, they must be executed in above order from top-bullet to bottom-bullet.

(d) DDR3-SDRAM setting

1. Use the manual command-issuing register (DBCMD) to insert a waiting time. The value written to this register should be OPC = Wait, ARG = 100 µs.
2. Use the manual command-issuing register (DBCMD) to set the M0RESET pin of SDRAM to the high level. The value written to this register should be OPC = RstH, ARG = 100 µs.
3. Use the manual command-issuing register (DBCMD) to insert a waiting time. Write OPC = Wait, ARG = 100 µs to this register four times.
4. Use the manual command-issuing register (DBCMD) to set the M0CKE[1:0] pins of SDRAM to the high level.
5. The value written to this register should be OPC = PDXt, ARG = tXPR (normally tRFC + 10 ns).
6. Use the manual command-issuing register (DBCMD) to issue the MRS (MR2) command. Adjust the setting for CWL to the setting of the CWL bits in SDRAM timing register 1 (DBTR1).
7. Use the manual command-issuing register (DBCMD) to issue the MRS (MR3) command. Set the MPR for normal operation.
8. Use the manual command-issuing register (DBCMD) to issue the MRS (MR1) command. Set the additive latency to 0, and the DLL Enable to enabled.
9. Use the manual command-issuing register (DBCMD) to issue the MRS (MR0) command. At this time, set the mode of operation to normal, the DLL to reset, the burst length to eight, and the burst type to sequential.

   Also adjust the setting of the CAS latency to match the setting of the CL bits in SDRAM timing register 0 (DBTR0). Adjust the setting of WR to match the settings of the TWR bits in the
10. Use the manual command-issuing register (DBCMD) to issue the ZQ Calibration Long command. The value written to this register should be OPC = ZQCL, ARG = max {tZQinit, tDLLK – tMOD}

(e) DBSC3 Setting 2

1. Make other necessary settings in DBSC3.
   - DBSC3 operation adjustment registers 0 to 3 (DBADJ0 to DBADJ3)
   - Bus control unit 0 control registers 0 and 1 (DBBS0CNT0 and DBBS0CNT1)
   - DDR3-SDRAM calibration configuration register (DBCALCNF)

- DDR3-SDRAM calibration timing register (DBCALTR)
- Power-down configuration register (DBPDNCNF)

2. Make settings in refresh configuration registers 0 to 2 (DBRFCNF0 to DBRFCNF2).
3. Set the ARFEN bit to 1 in the auto-refresh enable register (DBRFEN).
4. Write H'00000000 to DB_ADDR + H'4008.
5. Write H'00000000 to DB_ADDR + H'4000.
6. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).
7. Read the operation completion waiting register (DBWAIT) and wait for the response.

End of initialization sequence

Usage Note:

However there is no number of order for these sequences, they must be executed in above order from top-bullet to bottom-bullet.

15.3.5 Self-Refresh Operation

If it is not necessary to access the SDRAM, the SDRAM can be put in self-refresh mode to reduce power consumption while still retaining data contents.

Since access to the SDRAM is disabled in self-refresh mode, requesting an SDRAM data access to the DBSC3 will cause an error.

The following procedure should be used to enter or release self-refresh mode.

(1) Self-Refreshing (When the Clock is Not Stopped)

Use the following procedure to enter self-refresh mode.

1. Set the ACCEN bit to 0 (access disabled) in the SDRAM access enable register (DBACEN).
2. Use the manual command-issuing register (DBCMD) to issue the PREA (precharge all) command. The value written to this register should be OPC = PreA, ARG = 0.
3. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Entry command. The value written to this register should be OPC = SREn, ARG = 0.
4. Set the ARFEN bit to 0 in the auto-refresh enable register (DBRFEN).

Use the following procedure to release self-refresh mode.

1. Set the ARFEN bit to 1 in the auto-refresh enable register (DBRFEN).
2. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Exit command. The value written to this register should be OPC = SRXt, ARG = 0.
3. Use the manual command-issuing register (DBCMD) to insert wait cycles until access to the SDRAM is enabled. The value written to this register should be OPC = Wait, ARG = tXSDLL (normally, 512).
4. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).

(2) Self-Refreshing (When the Clock is Stopped or Clock Frequency is Changed)

Use the following procedure to enter self-refresh mode.

1. Set the ACCEN bit to 0 (access disabled) in the SDRAM access enable register (DBACEN).
2. Use the manual command-issuing register (DBCMD) to issue the PREA (precharge all) command. The value written to this register should be OPC = PreA, ARG = 0.
3. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Entry command. The value written to this register should be OPC = SREn, ARG = 0.

4. Set the ARFEN bit to 0 in the auto-refresh enable register (DBRFEN).
5. Use the manual command-issuing register (DBCMD) to insert wait cycles for the clock to stop. The value written to this register should be OPC = Wait, ARG = tCKSRE (normally, max {5, 10 ns}).
6. Read the operation completion waiting register (DBWAIT) and wait for the response.
7. The clock supplied to the DBSC3 can be stopped at this point

Use the following procedure to release self-refresh mode.

1. Restart the clock supply and wait until the clock settles.
2. Reconfigure the PHY unit.
    - Set the PTRRST bit to 1 in PHY unit control register 3 (DBPDCNT3).
    - Clear the PTRRST bit to 0 in PHY unit control register 3 (DBPDCNT3).
    - Set the CALMODE bit to 1 in PHY unit control register 3 (DBPDCNT3).
    - Set the CALEN bit to 1 in PHY unit control register 3 (DBPDCNT3).
    - Set the DLL_RESET bit to 1 in PHY unit control register 3 (DBPDCNT3).
    - Ensure that the software allows the required waiting time (at least 50 µs).
    - Set the IO_ENABLE bit to 1 in PHY unit control register 3 (DBPDCNT3).
    - Set the PLL2_RESET bit to 1 in PHY unit control register 3 (DBPDCNT3).
    - Ensure that the software allows the required waiting time (at least 100 µs).
    - Set the STBY bit to 1 in PHY unit control register 3 (DBPDCNT3) and the clock is output through the MCK pins.
    - Set either the BW32 or BW16 bit to 1 in PHY unit control register 0 (DBPDCNT0).
    - Make other necessary settings in PHY unit control registers 0 to 3 (DBPDCNT0 to DBPDCNT3).
3. Use the manual command-issuing register (DBCMD) to insert wait cycles until self-refresh mode is released. The value written to this register should be OPC = Wait, ARG = tCKSRX (normally, max {5, 10 ns}).
4. Set the ARFEN bit to 1 in the auto-refresh enable register (DBRFEN).
5. Use the manual command-issuing register (DBCMD) to issue the Self-Refresh Exit command. The value written to this register should be OPC = SRXt, ARG = 0.
6. Use the manual command-issuing register (DBCMD) to insert wait cycles until access to the SDRAM is enabled. The value written to this register should be OPC = Wait, ARG = tXSDLL (normally, 512).
7. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).

Usage Note:

However there is no number of order for these sequences, they must be executed in above order from top-bullet to bottom-bullet.

15.3.6 Power-Down Operation

If there is no need to access SDRAM, entering the power-down mode can place the SDRAM internal clock in inactive state, which can effectively lower the power consumption in the device. Even in a power-down mode, the clock and power need to be supplied.

Use the following procedure to enter the power-down mode.

1. Set the ACCEN bit to 0 (access disabled) in the SDRAM access enable register (DBACEN).
2. Use the manual command-issuing register (DBCMD) to issue the Power Down Entry command. The value written to this register should be OPC = PDEn, ARG = 0.

Use the following procedure to release the power-down mode.

1. Use the manual command-issuing register (DBCMD) to issue the Power Down Exit command. The value written to this register should be OPC = PDXt, ARG = 0.
2. Set the ACCEN bit to 1 (access enabled) in the SDRAM access enable register (DBACEN).

To keep holding the SDRAM data in power-down mode, a refresh command needs to be issued at regular intervals in the same way as in normal operation. In the DBSC3, by entering the power-down mode with the auto-refresh function operating (ARFEN = 1 in the DBRFEN register), refresh is performed regularly and the SDRAM data is held even in the power-down mode.

Since access to the SDRAM is disabled in self-refresh mode, requesting an SDRAM data access to the DBSC3 will cause an error.

15.3.7 Modifying Refresh Settings during Operation

In the DBSC3, refresh settings (such as refresh frequency) can be modified during operation. The following gives the procedure for it. Note that it is assumed that the ACCEN bit in the DBACEN register has been set to 1 (access is enabled) and the ARFEN bit in the DBRFEN register has been set to 1 (auto-refresh is active) in advance.

1. Write to refresh configuration registers 0 to 2 (DBRFCNF0 to DBRFCNF2) to modify settings.
2. Write 1 to the ARFEN bit in the auto-refresh enable register (DBRFEN).

After step 2, the new settings made in step 1 are applied to the refresh operation.

15.3.8 Restrictions on AXI Bus Interface

This section describes the restrictions on the AXI bus interface.

(1) Fixed Burst Transfer

Only a burst length of 1 is supported for the fixed burst length transfer. The DBSC3 returns an error response to the transactions with the other burst length.

15.3.9 Setting the SDRAM Configuration Setting Register

(1) DDR3-SDRAM (32-Bit External Bus)

Capacity	Memory Configuration	Rank	Bank [No. of Banks]	Row [No. of Bits]	Column [No. of Bits]	DBCONF0 Setting				
						AWRW0	AWRK0	AWBK0	AWCL0	DW0
128 Mbytes	32 M × 16 bits "512 Mbits" (2 modules)	1	8	12	10	01100	0	11	1010	10
256 Mbytes	64 M × 16 bits "1 Gbit" (2 modules)	1	8	13	10	01101	0	11	1010	10
512 Mbytes	128 M × 16 bits "2 Gbits" (2 modules)	1	8	14	10	01110	0	11	1010	10
1 Gbyte	256 M × 16 bits "4 Gbits" (2 modules)	1	8	15	10	01111	0	11	1010	10
2 Gbytes	512 M × 16 bits "8 Gbits" (2 modules)	1	8	16	10	10000	0	11	1010	10

15.3.10 Address Multiplexing

Memory of various sizes can be connected through the settings of the SDRAM configuration setting register 0 (DBCONF0). The DW0 bits are used to set the external data bus width, and the AWRW0 and AWCL0 bits are used to set the size of the memory connected. The AWBK0 bits are used to specify the number of banks; depending on the application the possibility of page hits may be increased.

(1) DDR3-SDRAM (32-Bit External Bus)

Table 15.9 Relation between Address Pins and Logical Addresses (BKADM = B'00) (When Two 16-Bit-Width SDRAM Modules are Connected)

Memory Type		BA2	BA1	BA0	MA15	MA14	MA13	MA12	MA11	MA10	MA9	MA8	MA7	MA6	MA5	MA4	MA3	MA2	MA1	MA0
32 M × 32 bits	ROW	A14	A13	A12	0	0	0	0	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
64 M × 32 bits	ROW	A14	A13	A12	0	0	0	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
128 M × 32 bits	ROW	A14	A13	A12	0	0	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
256 M × 32 bits	ROW	A14	A13	A12	0	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0
512 M × 32 bits	ROW	A14	A13	A12	A30	A29	A28	A27	A26	A25	A24	A23	A22	A21	A20	A19	A18	A17	A16	A15
	COL	A14	A13	A12	0	0	0	BC#	0	AP	A11	A10	A9	A8	A7	A6	A5	A4	0	0

Notes: 1. A31 to A0 are the logical address bits in byte units. A31 represents the MSB, and A0 the LSB.
2. AP is an abbreviation of auto precharge option.
3. BC# is an abbreviation of burst chop option.

15.3.11 SDRAM Access and Timing Constraints

In this section, waveforms at the various pins during basic SDRAM access are explained first and then the relation between SDRAM access and the CAS latency (CL, CWL), tRAS, tRFC, tRCD, tRP, tRRD, tWR, tRTP, tRC, READ to WRITE minimum interval, and WRITE to READ minimum interval set using SDRAM timing registers 0 to 19 (DBTR0 to DBTR19) is explained.

(1) Basic SDRAM Access

In this section, waveforms at the various pins during basic SDRAM access, including reading, writing, auto-refresh, and self-refresh operations, are explained.

Figure 15.6 shows waveforms for 1-/2-/4-/8-/16-byte reading. In this case, single reading is performed in which the READ command is issued once. In this example, read access processing is executed for bank A after the ACT command is issued, but when there is a page hit, access begins with the issue of the READ command.

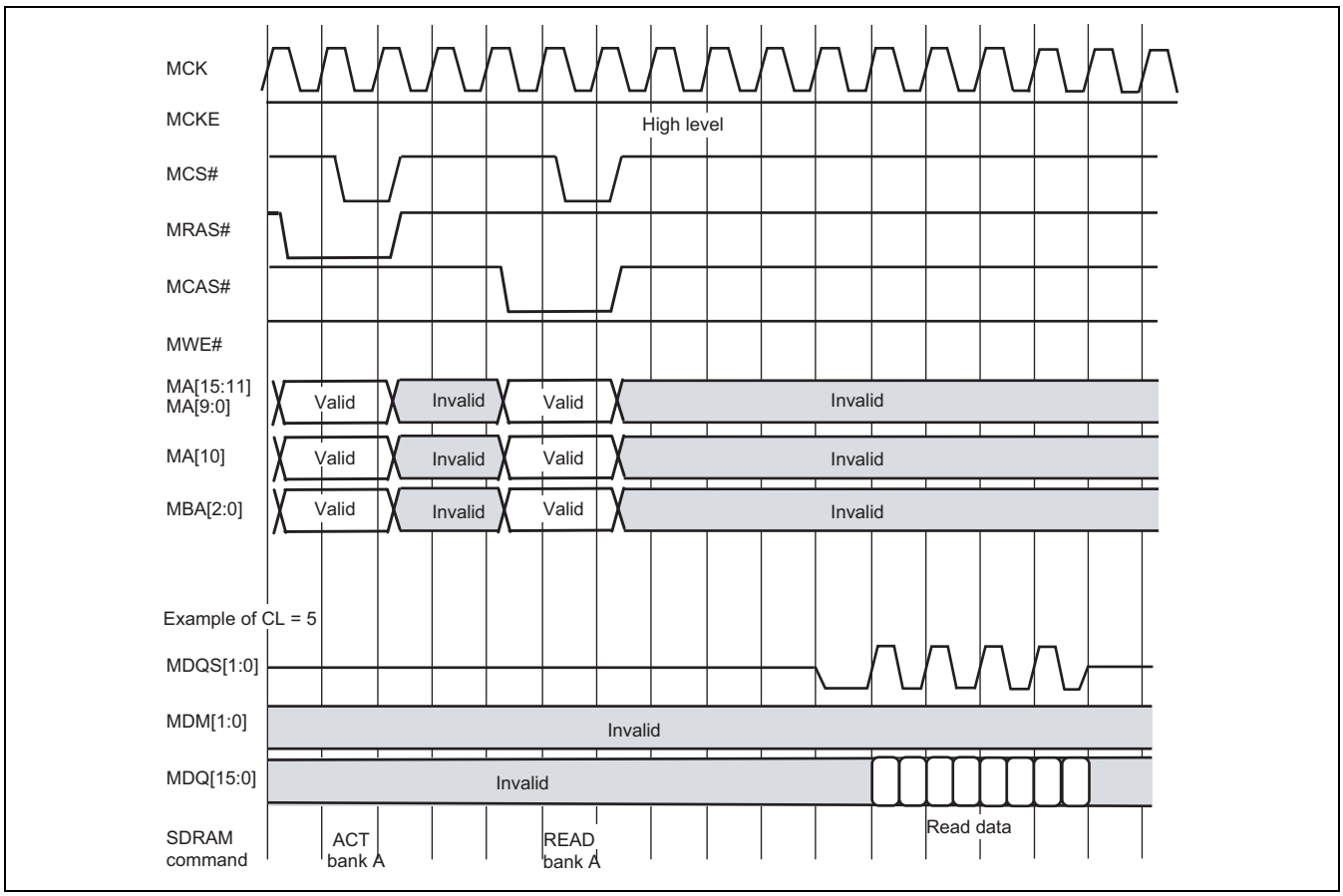


Figure 15.6 Waveforms for 1/2/4/8/16-Byte Reading

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.7 shows waveforms for 1-/2-/4-/8-/16-byte writing. In this case, single writing is performed in which the WRITE command is issued once. In this example, write access processing is executed for bank A after the ACT command is issued, but when there is a page hit, access begins with the issue of the WRITE command.

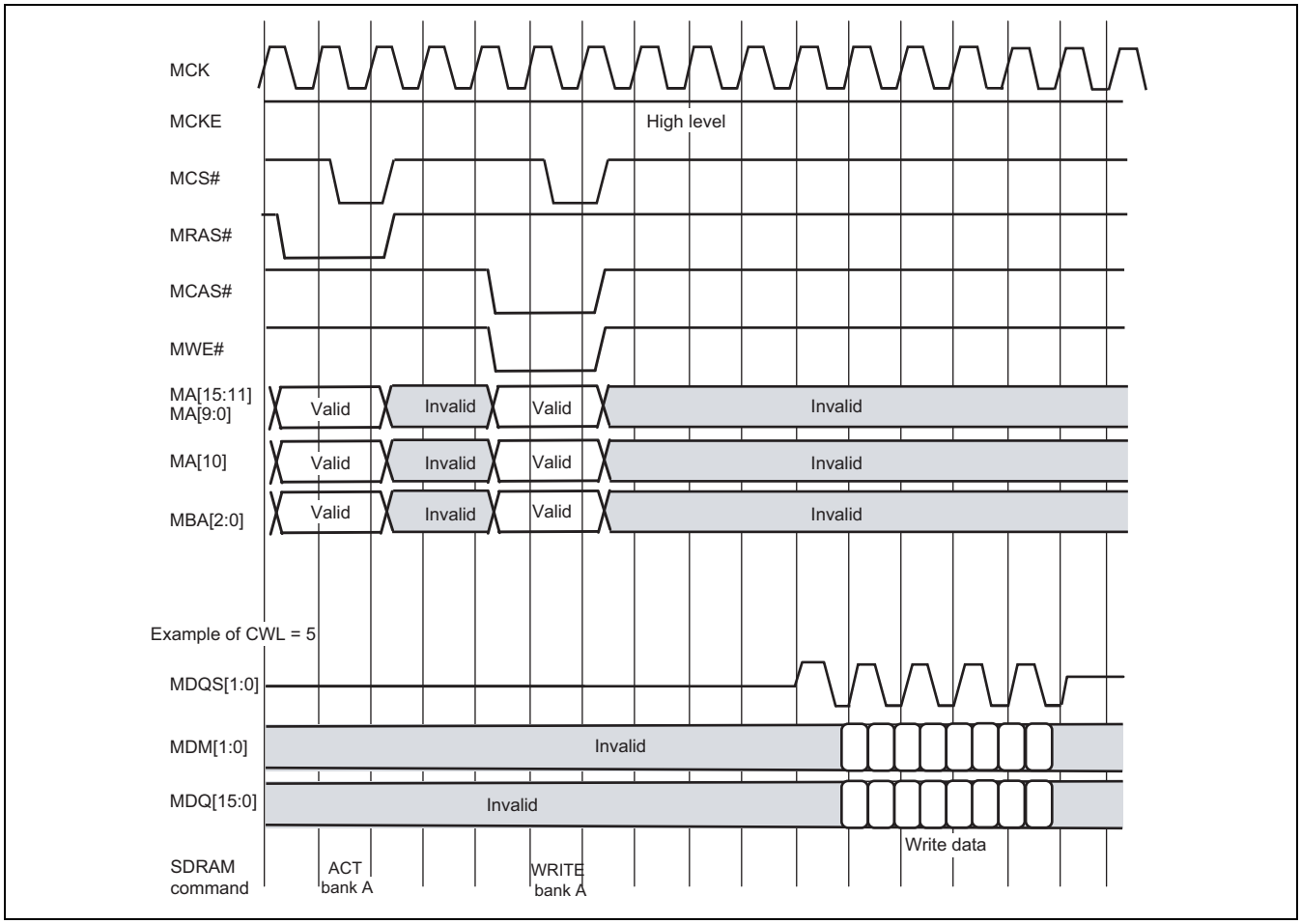


Figure 15.7 Waveforms for 1/2/4/8/16-Byte Writing

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.8 shows waveforms during auto-refresh operation resulting from settings of the refresh configuration registers 0 to 2. The DBSC3 issues a REF command automatically after the PALL command is issued when at least one SDRAM bank is activated before the REF command. Consequently, there is no need to use software to manage precharging of all the banks for the auto-refresh operation.

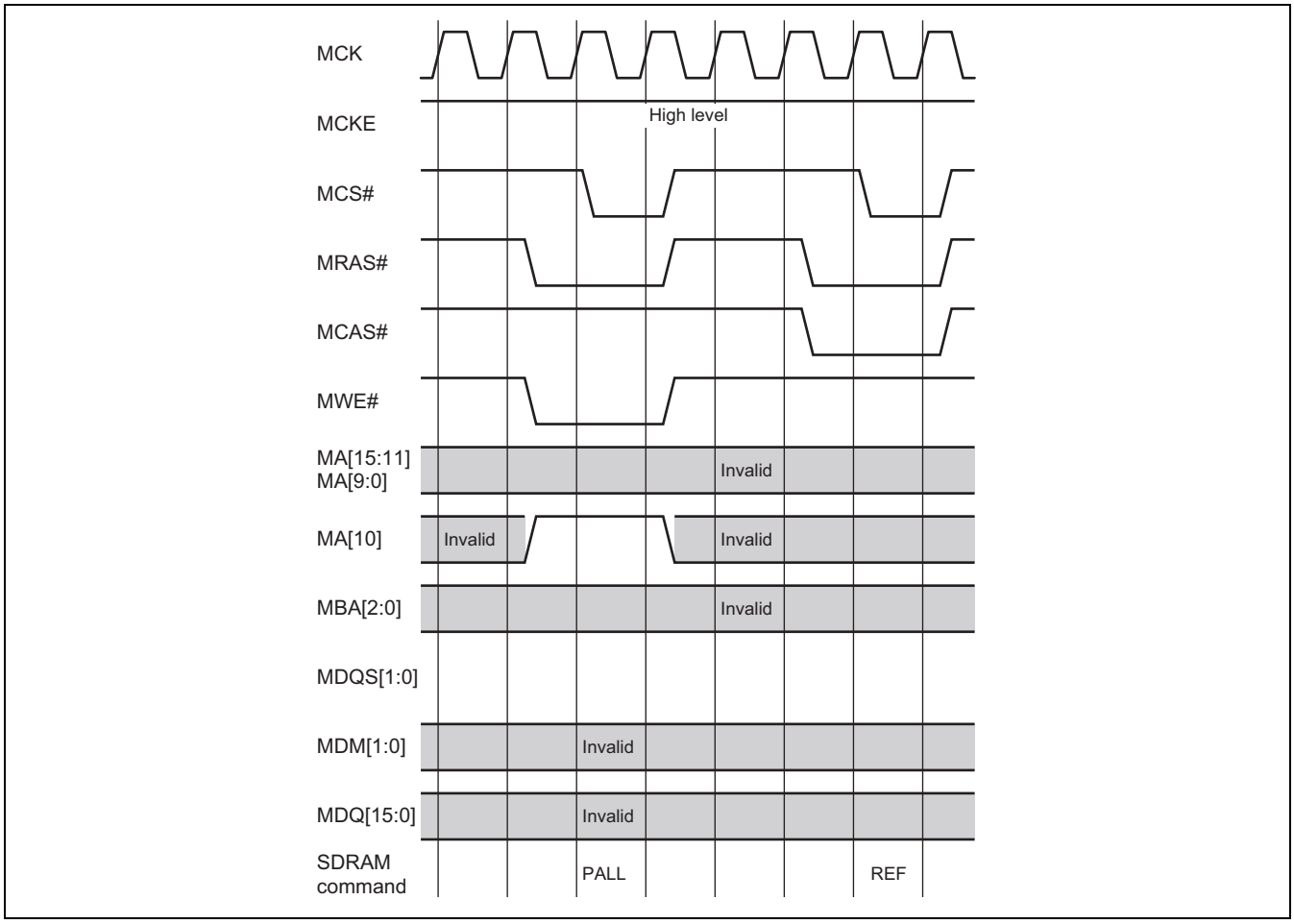


Figure 15.8 Auto-Refresh Operation

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A/ signals, respectively.

Figure 15.9 shows the self-refresh operation. In order to perform self-refresh operation, the specified sequence must be observed. For details, refer to section 15.3.5, Self-Refresh Operation.

When performing processing according to the sequence in section 15.3.5, Self-Refresh Operation, commands to be issued to the SDRAM are those shown in Figure 15.9. Before the transition to self-refresh, the PALL command is issued by software. Then, software is used to issue the REF command and the SRX (self-refresh entry from IDLE) command. The SDRAM is in self-refresh mode until self-refresh is released by software. After issuing the SRX (self-refresh exit) command by software, it is necessary to wait for the time (tXSNR) specified in the datasheet for the SDRAM being used until issuing a REF command. A wait example is shown in section 15.3.4.12, Method for Securing Time Required for Initialization, Self-Refresh Release, etc.

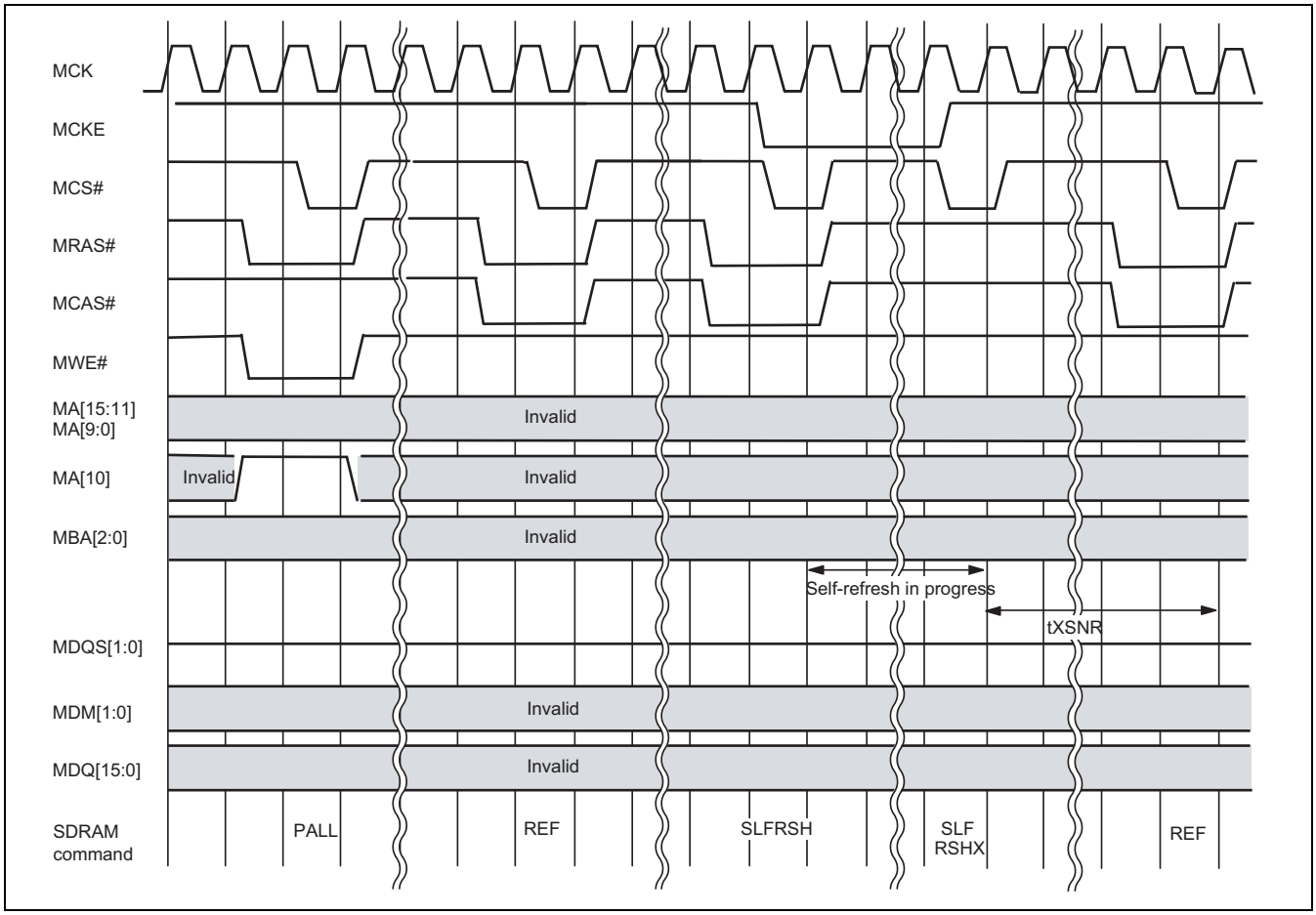


Figure 15.9 Self-Refresh Operation

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

(2) Timing Constraints

Figure 15.10 shows the relation between the settings of CL, tRAS, tRCD, and tRP, and the issuing of commands. Figure 15.11 shows the relation to tRRD and tRTP, Figure 15.12 shows the relation to tWR, Figure 15.13 shows the relation to tRC, Figure 15.14 shows the relation to READ-WRITE, Figure 15.15 shows the relation to WRITE-READ, and Figure 15.16 shows the relation to tRFC.

Figure 15.10 corresponds to operation in a case in which bank A is open, there is read access of bank A, and a page miss occurs. The constraint tRP between the PRE command and ACT command, the constraint tRCD between the ACT command and READ command, and the constraint tRCD between the ACT command and the PRE command are involved. The DBSC3 waits to issue commands until each of the constraints is satisfied.

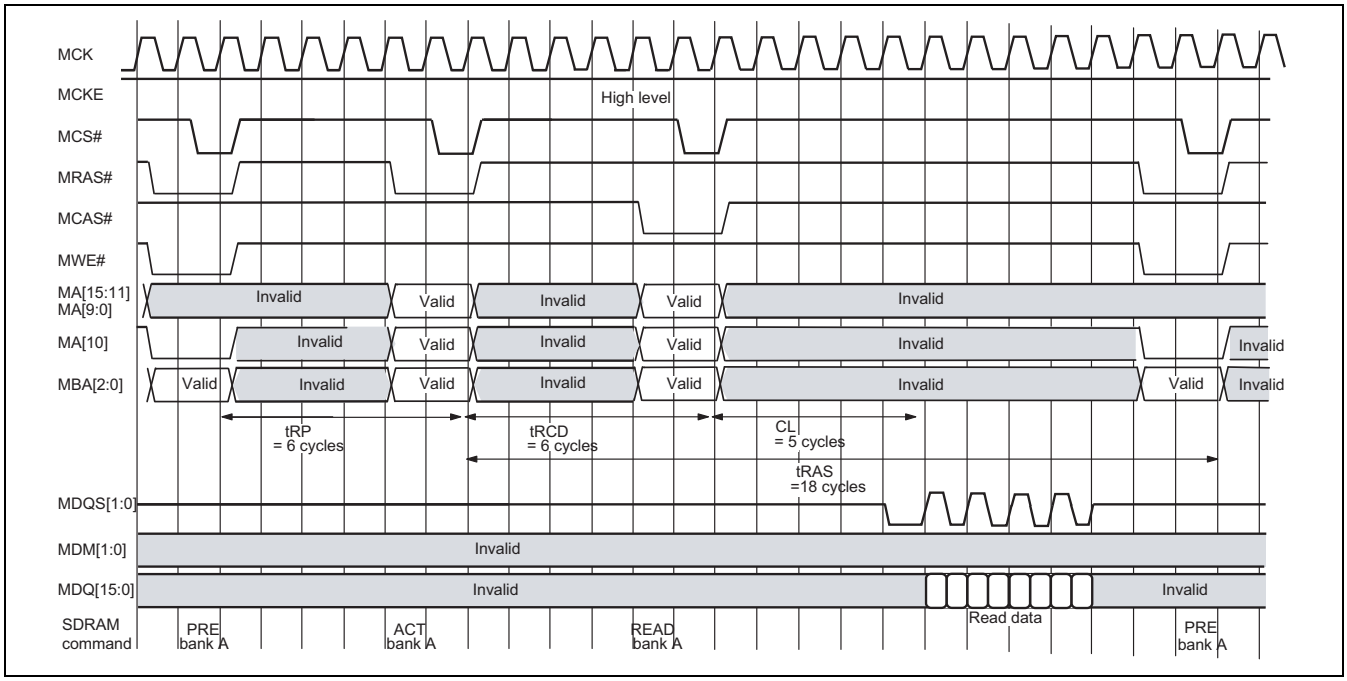


Figure 15.10 tRP, tRCD, CL, and tRAS

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.11 shows a case in which the pages for both of banks A and B are closed, the page for bank C is open, and a page hit has occurred. When the tRRD time constraint has been satisfied starting from issue of the ACT command for bank A, the ACT command for bank B is issued. Because time tRCD has elapsed from the issue of the ACT command for bank A, a READ command can be used. The READ command has a burst length of 8, so after four cycles a READ command for bank B can be issued. A further four cycles later, a READ command for bank C can be issued. However, the next request is access for which bank C must be closed, and so after the elapse of time tRTP, a PRE command is issued.

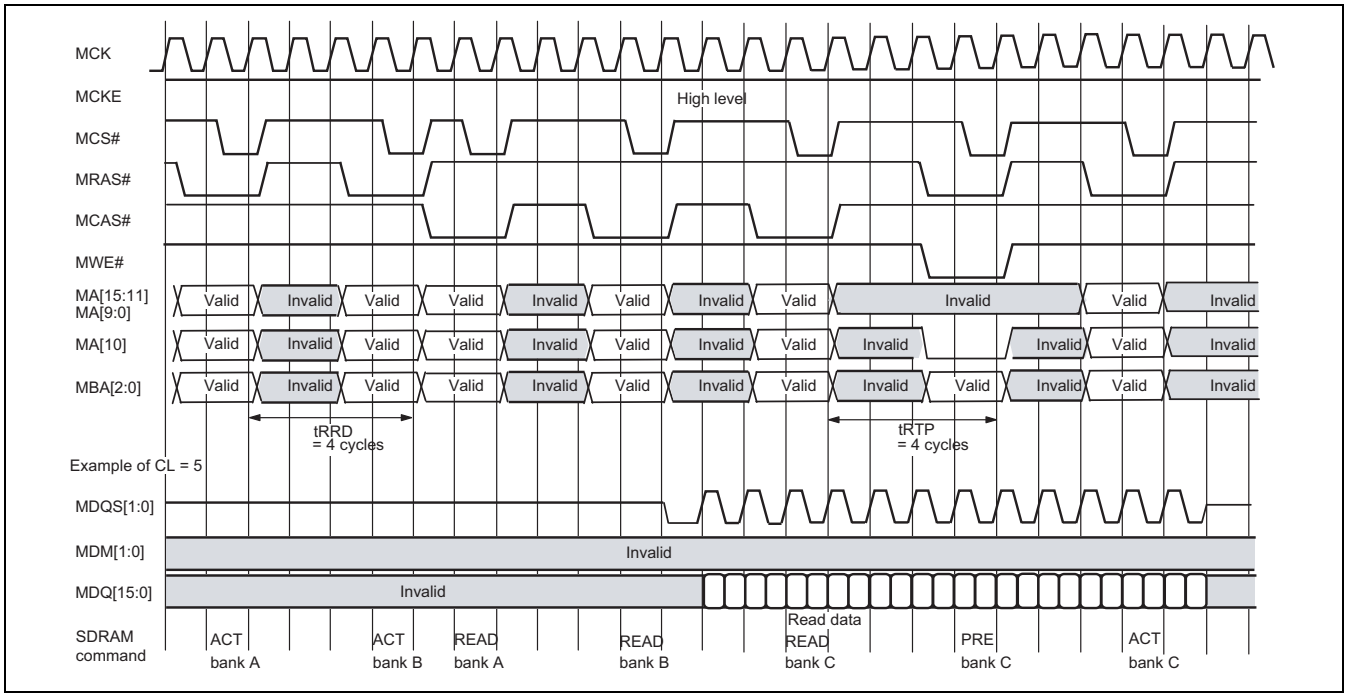


Figure 15.11 tRRD and tRTP

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.12 shows a case in which, after a write request, access occurs requiring that bank B be closed. After the issue of a WRITE command, it is necessary to wait for time tWR or longer after output of the write data before issuing a PRE command.

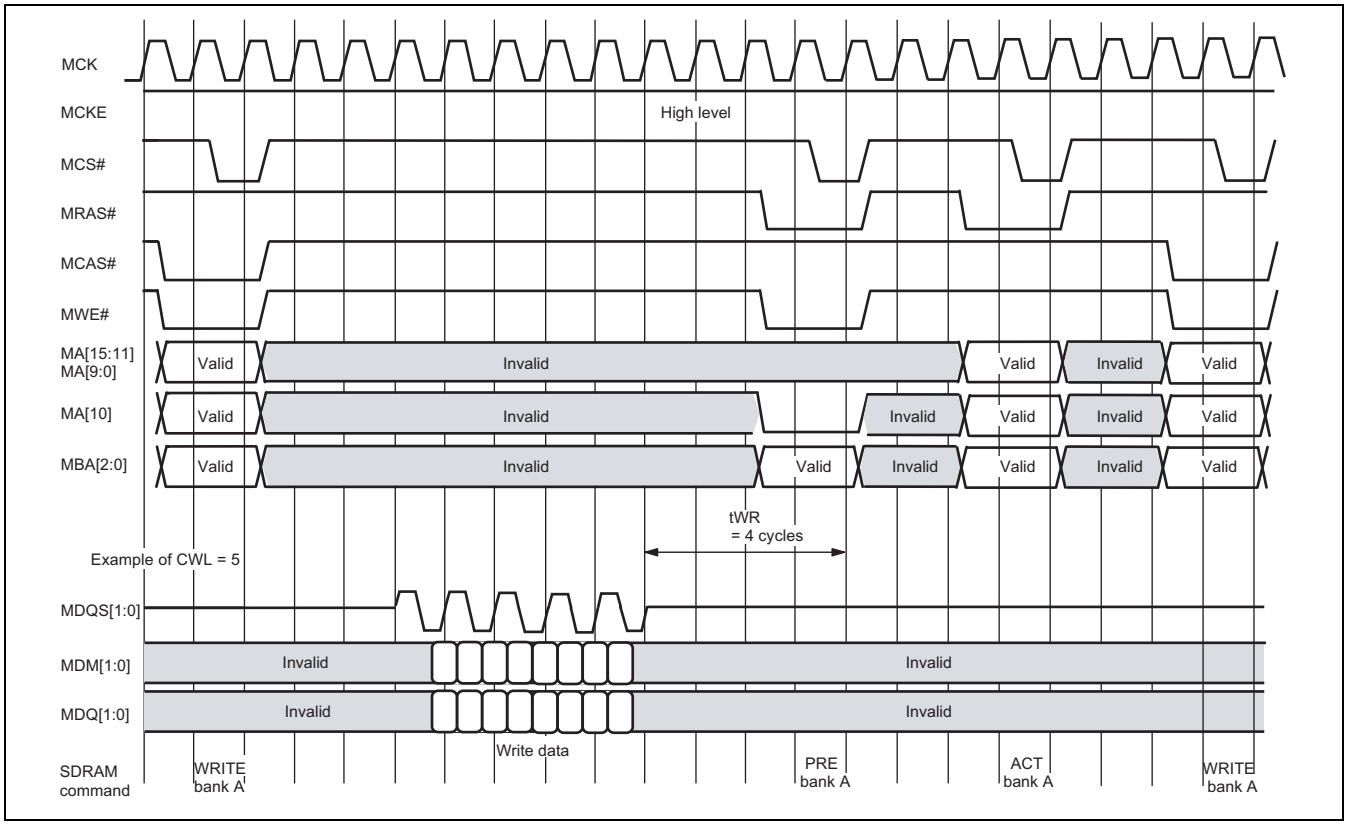


Figure 15.12 tWR

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.13 shows an example of performing auto-refresh after read access of bank A, the page for which had been closed. After issuing an ACT command and READ command for bank A and performing data reading, a PALL command must be used to close all banks in order to perform auto-refresh. In order to issue the PREA command, the tRAS time constraint must be satisfied and issuing of the PREA command is delayed until this time. Then, when issuing the REF command, both of time constraints tRPA and tRC must be satisfied simultaneously. When these constraints are both satisfied, the REF command is issued and auto-refresh is performed.

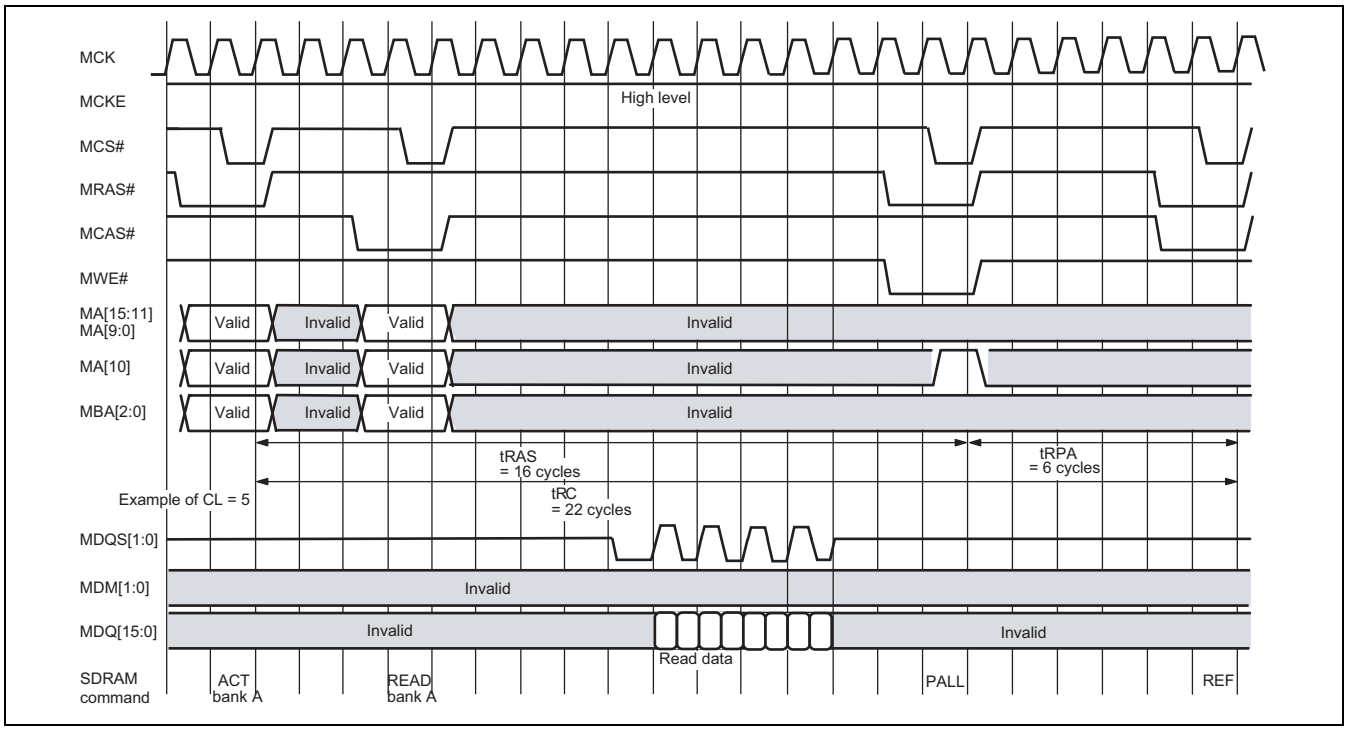


Figure 15.13 tRC

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.14 shows an example of a case in which, after issuing a READ command, a WRITE command is issued. In order to issue the WRITE command after issuing the READ command, the DBSC3 waits for a minimum time stipulated by the RDWR bits.

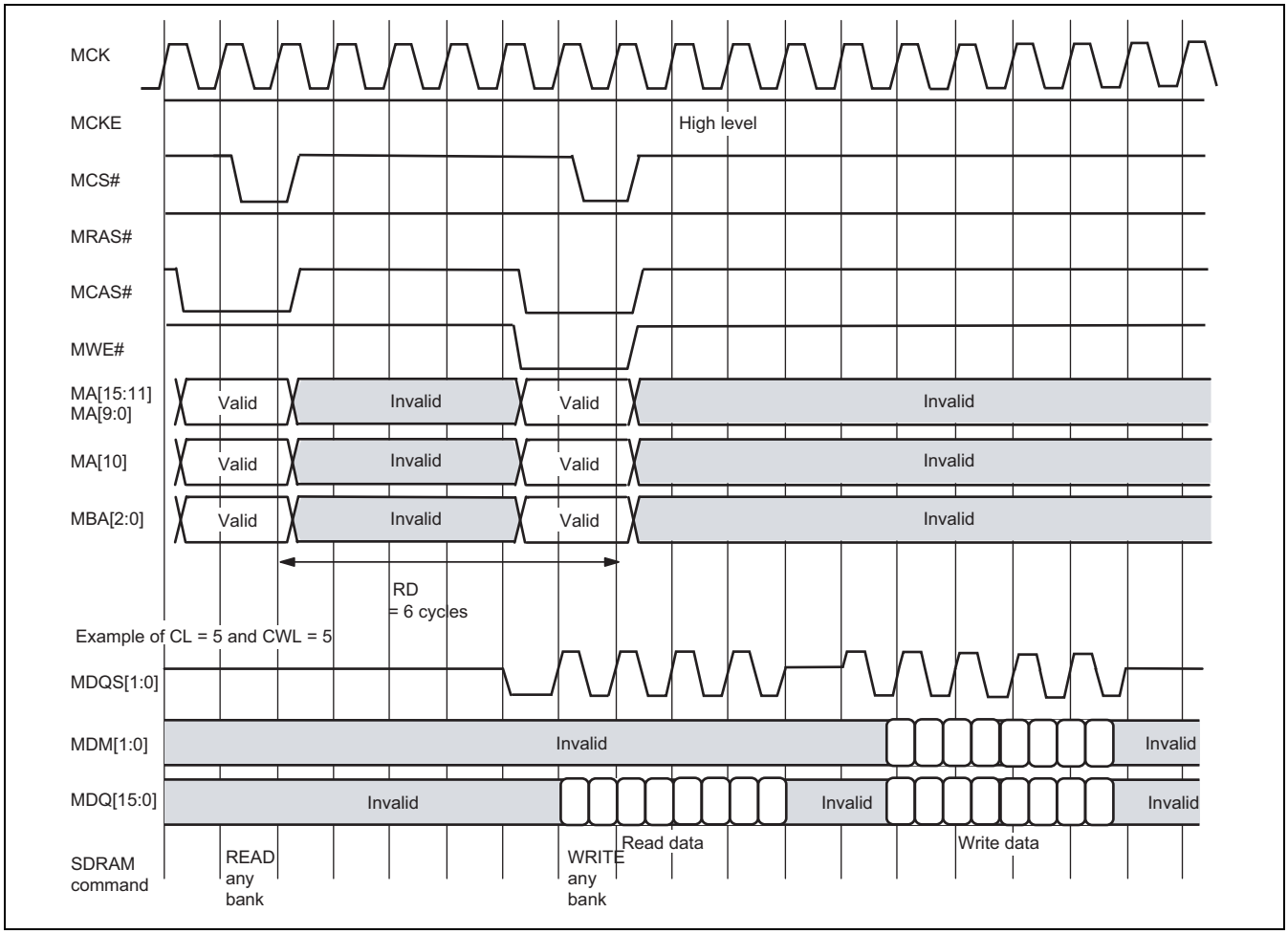


Figure 15.14 READ-WRITE Minimum Time

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.15 shows an example of a case in which, after issuing a WRITE command, a READ command is issued. In order to issue the READ command after issuing the WRITE command, the DBSC3 waits for a minimum time stipulated by the WRRD bits.

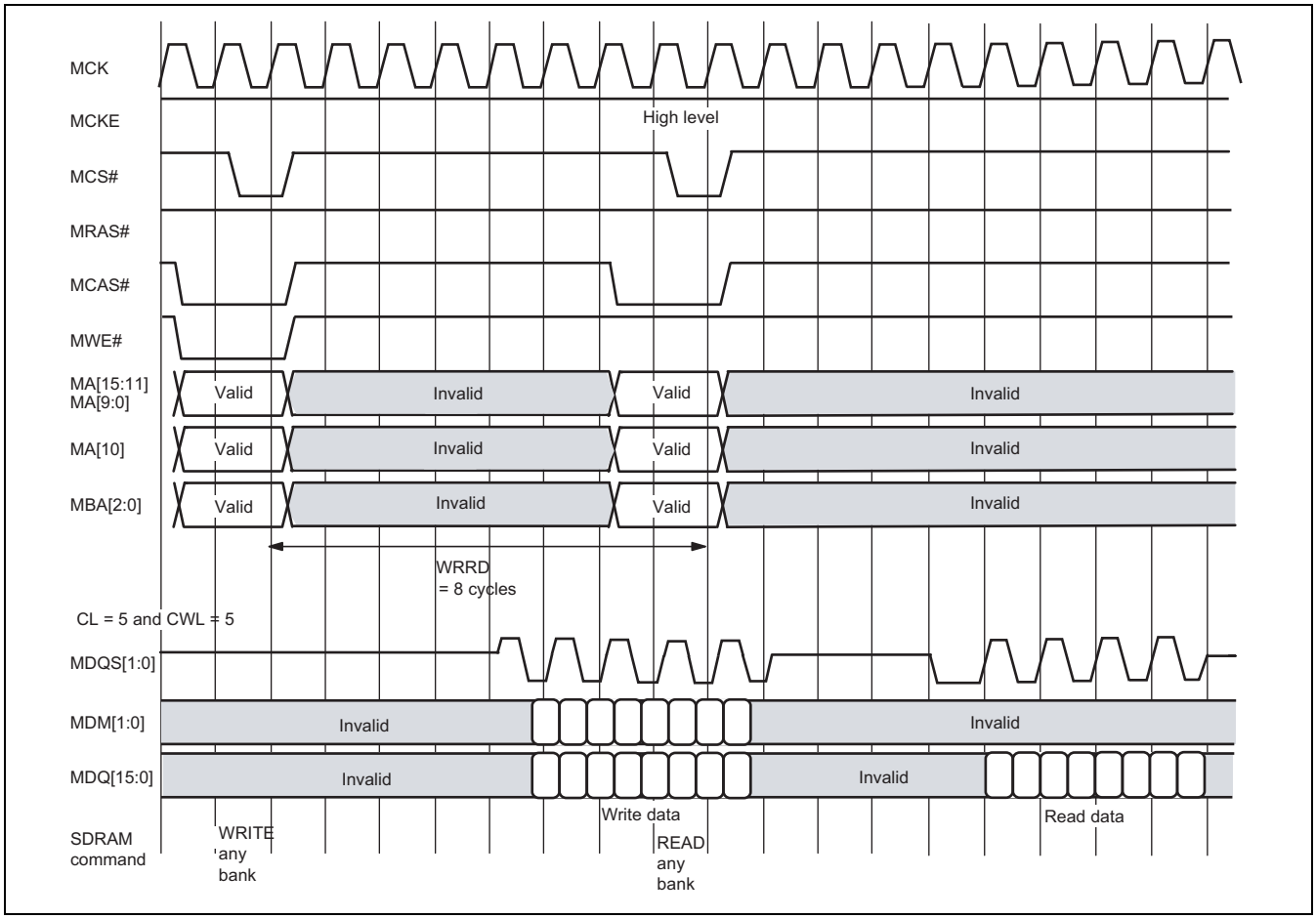


Figure 15.15 WRITE-READ Minimum Time

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

Figure 15.16 shows an example of a case in which, after issuing a REF command, a READ request is issued. In order to issue the ACT command after issuing the REF command, the DBSC3 waits for a time stipulated by tRFC.

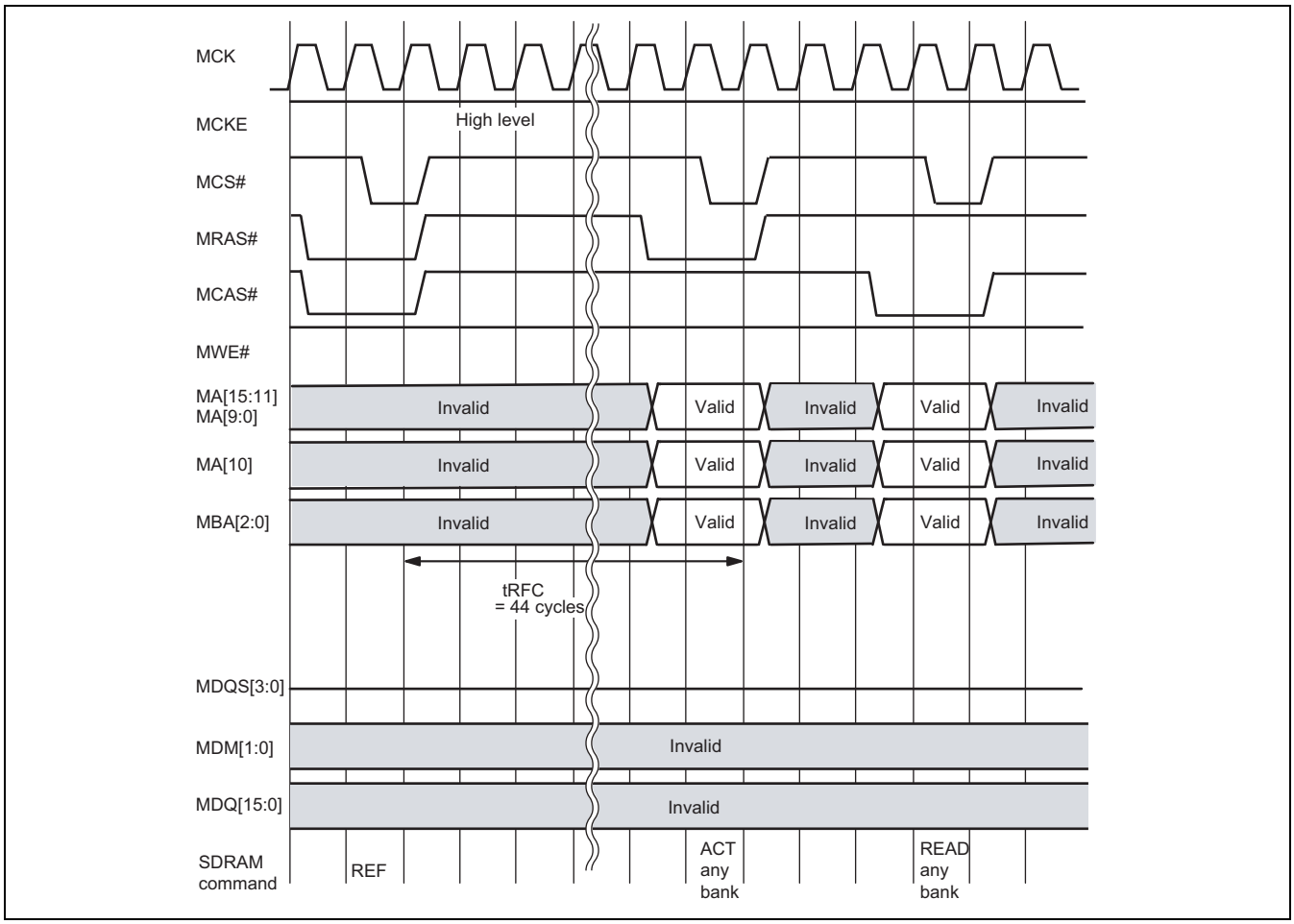


Figure 15.16 tRFC

Note: In the figure, collective names are used for signals. For example, MCK and MA indicate M0CK and M0A signals, respectively.

15.3.12 Method for Securing Time Required for Initialization, Self-Refresh Release, etc.

When using DBSC3 register settings to set initialization or release the self-refresh state, there is a need to wait for the time defined in the SDRAM specifications. To reserve this waiting time, read from the DBSC3 status register 1 (DBSTATE1). When this is done, at least seven memory clock cycles elapse. For 250-MHz operation, about 28 ns elapse upon one DBSTATE1 read. This can be utilized to secure the required time, by repeating read access the necessary number of times.

15.4 Notes on Board Design

15.4.1 Connection of M0ZQ Pin

A resistor having the following value should be connected to the M0ZQ pin outside this LSI.

DDR3-SDRAM: 120 Ω (± 1%)

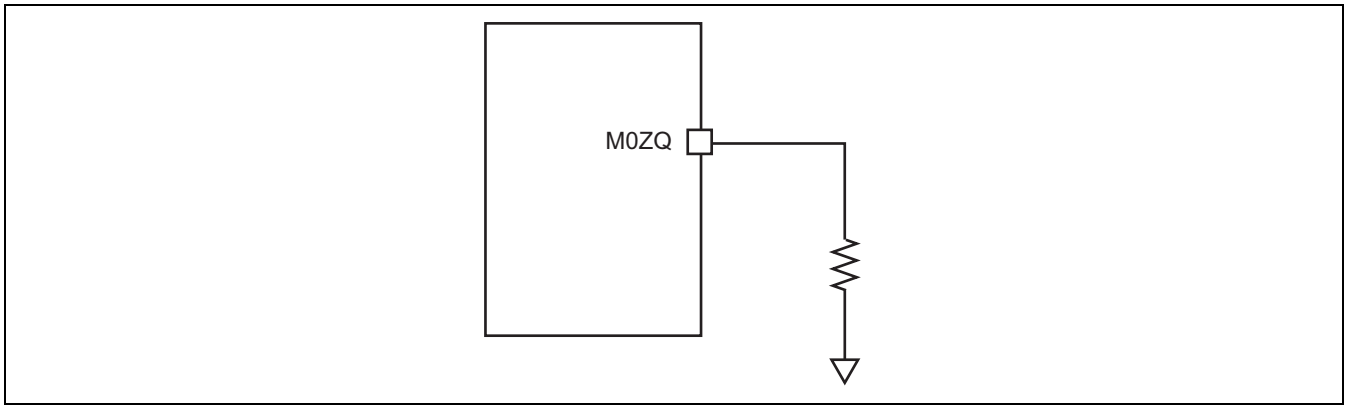


Figure 15.17 Connection of M0ZQ Pin

15A. S3 Controller (S3CTRL)

15A.1 Overview

The S3 controller (S3CTRL) includes a local interconnect placed between AXI-bus interconnects and DBSC memory controller.

15A.1.1 Features

The S3CTRL include the following features.

- XY command decoder (media domain only)
- Support 8 entries of system CPU's exclusive access command.

15A.1.2 Block Diagram

Figure 15A.1 is a block diagram of the S3CTRL.

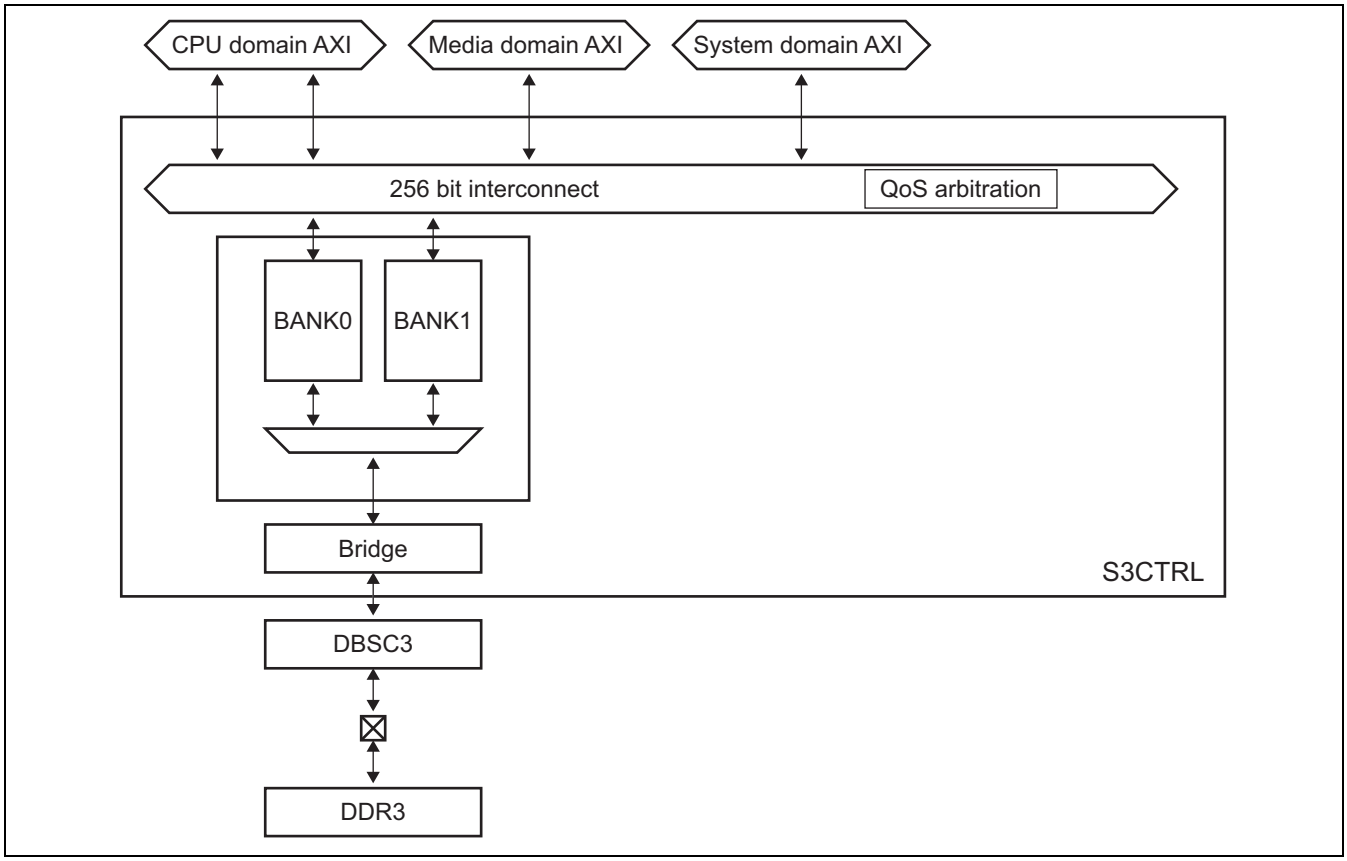


Figure 15A.1 Block Diagram of S3CTRL

15A.1.3 Input / Output Pins

No external pins are supported.

15A.1.4 Register Configuration

Table 15A.1 shows the register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register as a long-word (32 bits). Operation cannot be guaranteed if the register is not accessed as a long-word.

Table 15A.1 Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
Exclusive Address Mask Register	S3CEXCLADDMSK	R/W	H'E678 4000	H'FFFFFFFF	32
Exclusive ID Mask Register	S3CEXCLIDMSK	R/W	H'E678 4004	H'FFFFFFFF	32
S3C Read Outstanding Regulation Register	S3CRORR	R/W	H'E678 4014	H'0F0D0B07	32
S3C Write Outstanding Regulation Register	S3CWORR	R/W	H'E678 4018	H'0F0D0B07	32
XY TL Area Control Register A0	XYTLAREAA0	R/W	H'E678 4B00	H'00000000	32
XY TL Area Control Register A1	XYTLAREAA1	R/W	H'E678 4B04	H'00000000	32
XY TL Area Control Register A2	XYTLAREAA2	R/W	H'E678 4B08	H'00000000	32
XY TL Area Control Register A3	XYTLAREAA3	R/W	H'E678 4B0C	H'00000000	32
XY TL Area Control Register A4	XYTLAREAA4	R/W	H'E678 4B10	H'00000000	32
XY TL Area Control Register A5	XYTLAREAA5	R/W	H'E678 4B14	H'00000000	32
XY TL Area Control Register A6	XYTLAREAA6	R/W	H'E678 4B18	H'00000000	32
XY TL Area Control Register A7	XYTLAREAA7	R/W	H'E678 4B1C	H'00000000	32
XY TL Area Control Register B0	XYTLAREAB0	R/W	H'E678 4B20	H'00000000	32
XY TL Area Control Register B1	XYTLAREAB1	R/W	H'E678 4B24	H'00000000	32
XY TL Area Control Register B2	XYTLAREAB2	R/W	H'E678 4B28	H'00000000	32
XY TL Area Control Register B3	XYTLAREAB3	R/W	H'E678 4B2C	H'00000000	32
XY TL Area Control Register B4	XYTLAREAB4	R/W	H'E678 4B30	H'00000000	32
XY TL Area Control Register B5	XYTLAREAB5	R/W	H'E678 4B34	H'00000000	32
XY TL Area Control Register B6	XYTLAREAB6	R/W	H'E678 4B38	H'00000000	32
XY TL Area Control Register B7	XYTLAREAB7	R/W	H'E678 4B3C	H'00000000	32
XY Mode Configuration Register	XYMODECONF	R/W	H'E678 4B40	H'00000000	32

15A.2 Register Description

Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

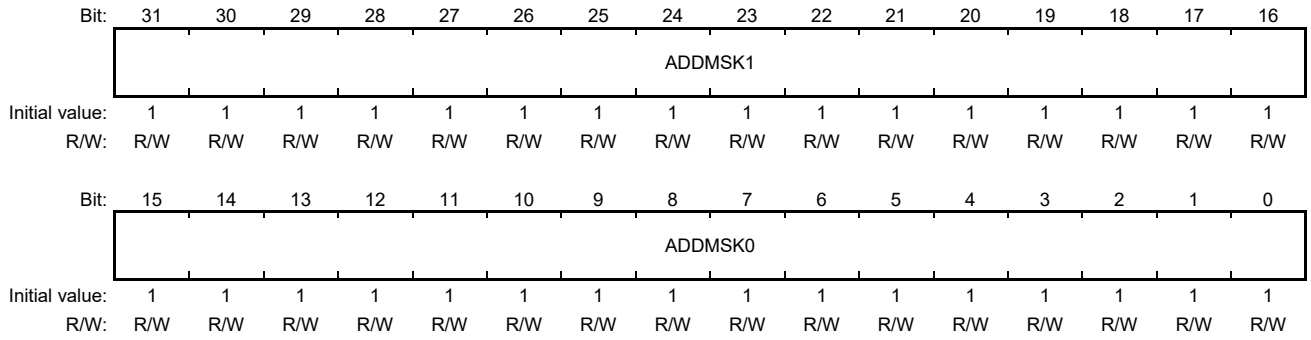
W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in long-word units.

15A.2.1 Exclusive Address Mask Register (S3CEXCLADDMSK)

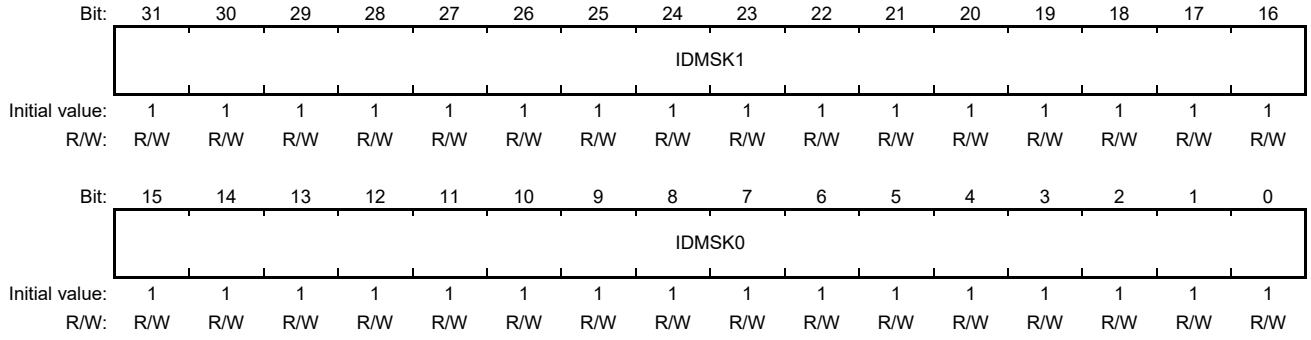
Function: Address bit mask of exclusive access. Lower 16-bit address can be masked.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	ADDMSK1	H'FFFF	R/W	Reserved These bits are always read as H'FFFF. The write value should always be H'FFFF.
15 to 0	ADDMSK0	H'FFFF	R/W	Exclusive address mask (Lower 16 bits) enable bit for DBSC channel 0 0: Disable bit 1: Enable bit

15A.2.2 Exclusive ID Mask Register (S3CEXCLIDMSK)

Function: ID bit mask of exclusive access



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	IDMSK1	H'FFFF	R/W	Reserved These bits are always read as H'FFFF. The write value should always be H'FFFF.
15 to 0	IDMSK0	H'FFFF	R/W	Exclusive ID mask (Lower 16 bits) enable bit for DBSC channel 0 0: Disable bit 1: Enable bit

15A.2.3 S3C Read Outstanding Regulation Register (S3CRORR)

Function: S3CTRL can control the number of read transaction at every QoS level to prevent DBSC's queue with low priority transactions. Transaction number is set by QOSTHn + 1. When QOSTHn = H'1F, its transaction number is not limited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RST	—	—	QOSTH3					—	—	—	QOSTH2				
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	1
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	QOSTH1					—	—	—	QOSTH0				
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RST	0	R/W	Reset the read transaction counter.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	QOSTH3	H'0F	R/W	The threshold queue length which the read transactions of QOS-Level3 can fill.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	QOSTH2	H'0D	R/W	The threshold queue length which the read transactions of QOS-Level2 can fill.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	QOSTH1	H'0B	R/W	The threshold queue length which the read transactions of QOS-Level1 can fill.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	QOSTH0	H'07	R/W	The threshold queue length which the read transactions of QOS-Level0 can fill.

15A.2.4 S3C Write Outstanding Regulation Register (S3CWORR)

Function: S3CTRL can control the number of write transaction at every QoS level to prevent DBSC's queue with low priority transactions. Transaction number is set by QOSTHn + 1. When QOSTHn = H'1F, its transaction number is not limited.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RST	—	—	QOSTH3					—	—	—	QOSTH2				
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	1	1	0	1
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	QOSTH1					—	—	—	QOSTH0				
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	0	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RST	0	R/W	Reset the write transaction counter.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	QOSTH3	H'0F	R/W	The threshold queue length which the write transactions of QOS-Level3 can fill.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	QOSTH2	H'0D	R/W	The threshold queue length which the write transactions of QOS-Level2 can fill.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	QOSTH1	H'0B	R/W	The threshold queue length which the write transactions of QOS-Level1 can fill.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	QOSTH0	H'07	R/W	The threshold queue length which the write transactions of QOS-Level0 can fill.

15A.2.5 XY TL Area Control Register A0 to A7 (XYTLAREAAn (n = 0 to 7))

Function: This register sets XY TL area. To change the value, set EN bit to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EN	—	—	—	—	—	—	—	—	BA[34:28]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BA[27:12]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	EN	0	R/W	Enable bit for this Area. 0: Disable 1: Enable
30 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 0	BA[34:12]	H'00 0000	R/W	Base address [34:12] The start address of Tile area is specified. Set values by STRIDE × 32 align.

15A.2.6 XY TL Area Control Register B0 to B7 (XYTLAREABn (n = 0 to 7))

Function: This register sets XY TL area. To change the value, set XYTLAREAAn.EN bit to 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	TT	—	—	—	—	SIZE			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	STRIDE[11:4]								—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	TT	0	R/W	Tile Type 0: 128 pix × 32 line 1: 256 pix × 32 line
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	SIZE	0000	R/W	Size of area 0000: 256 Kbytes 0001: 512 Kbytes 0010: 1 Mbyte 0011: 2 Mbytes 0100: 4 Mbytes 0101: 8 Mbytes 0110: 16 Mbytes 0111: 32 Mbytes 1000: 64 Mbytes 1001: 128 Mbytes 1010: 256 Mbytes others: Never Set
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 4	STRIDE[11:4]	H'00	R/W	Breadth of Tile Area. The value which can be set has restriction by TT (Tile Type) bit. 128 × 2^n (n = 0 to 5) (TT bit is 0) 256 × 2^n (n = 0 to 4) (TT bit is 1)
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

15A.2.7 XY Mode Configuration Register (XYMODECONF)

Function: This register sets XY mode configuration.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	XRCM	XWCM	YRCM	YWCM	—	—	—	LM	—	—	—	TT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	XRCM	0	R/W	X Read Convert Mode. Convert 16 × 1 to 16 × 2. 0: Disable 1: Enable
10	XWCM	0	R/W	X Write Convert Mode. Convert 16 × 1 to 16 × 2. 0: Disable 1: Enable
9	YRCM	0	R/W	Y Read Convert Mode. Convert 16 × 1 to 16 × 2. 0: Disable 1: Enable
8	YWCM	0	R/W	Y Write Convert Mode. Convert 16 × 1 to 16 × 2. 0: Disable 1: Enable
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	LM	0	R/W	Line Mode 0: 16 × 1 mode 1: 16 × 2 mode
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	TT	0	R/W	Tile Type 0: 128 pix × 32 line 1: 256 pix × 32 line

15A.3 Operation

15A.3.1 SDRAM Address Space

The S3CTRL supports one independent SDRAM memory controllers (DBSC) and 2 Gbytes address space on this controller. The SDRAM address mapping is managed on 40-bit physical address. Legacy address space is mapped to H'01 0000 0000 to H'01 7FFF FFFF.

Figure 15A.2 is shown SDRAM address map related to S3CTRL.

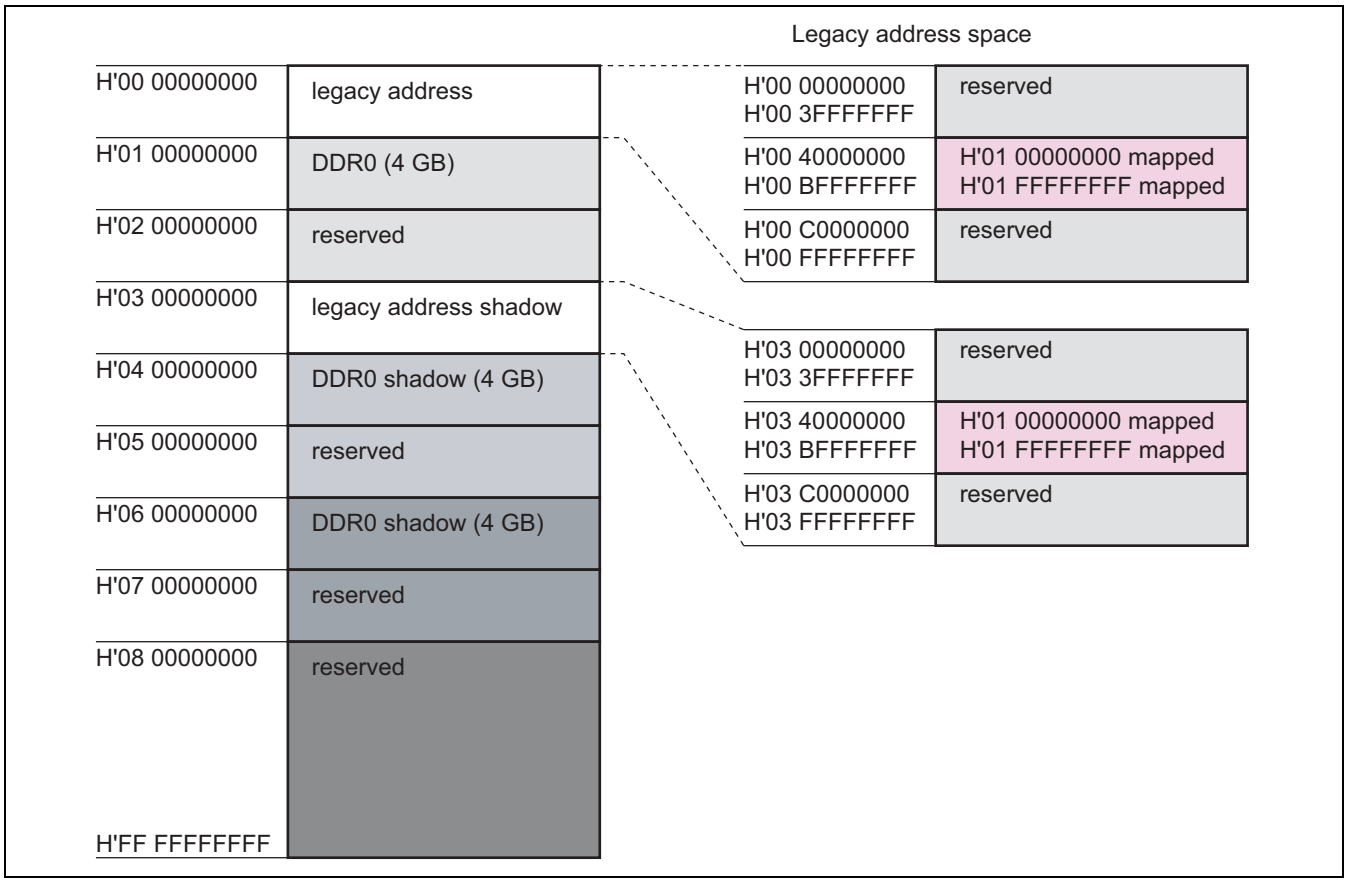


Figure 15A.2 SDRAM Address Map (Concerned with S3CTRL)

15A.3.2 XY Command Address Area

S3CTRL supports XY operation from Media domain. The address area accessed by XY operation is defined as Tile-Linear translated area. This area can be defined up to 8 areas. This Tile-Linear translated area also can be accessed by normal (linear) transaction from Media domain.

15A.3.3 QoS Arbitration

Every AXI domain has their own QoS level generator which can change a priority value of transactions dynamically based on its mode. The value is used when choosing the highest priority transaction at arbitration points. Read/Write transaction queues before a memory controller can limit the maximum number of transaction that can be enquired at every QoS level through S3CRORR/S3CWORR register. That allows low QoS transactions not to fill the queues and reserves space for higher QoS transactions.

15A.3.4 About Exclusive Instruction Monitor

The S3CTRL provides 8 exclusive access monitors for the memory controller. In the AXI specification, the AXI IDs and the addresses of the exclusive read and the exclusive write must be identical. However, the S3CTRL can specify the valid range of the IDs and the address through S3CEXCLADMSK and S3CEXCLIDMSK registers.

16. Direct Memory Access Controller for System (SYS-DMAC)

This LSI includes a direct memory access controller for system (SYS-DMAC). The SYS-DMAC can be used in place of the CPU to handle high-speed data transfer to and from an external memory, the on-chip memory, memory-mapped external devices, or on-chip peripheral modules.

16.1 Features

- Up to 30 channels are available.
- 4-Gbyte physical address space
- Transfer data length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes
- Maximum number of transfer times: 16,777,215
- Address mode: Dual address mode
- Transfer requests:

  Requests from on-chip peripheral modules or auto requests can be selected. The following modules can issue on-chip peripheral module requests.

  MSIOF0/1/2, HSCIF0/1/2, SCIF0/1/2/3/4/5, SDHI0/2, QSPI0/1
- Selectable bus modes:

  Normal speed mode or slow mode can be selected for each channel.
- Either fixed priority or round-robin arbitration can be selected for use in arbitration among the transfer channels.
- Interrupt request:

  The SYS-DMAC can be set up to generate an interrupt request for the CPU upon completion of transfer under the control of one stage of the descriptor memory, at the end of the data transfer, in response to an MMU error, and in response to an address error.
- Descriptor memory function:

  Up to 128 sets of the settings for the source address register, destination address register, and transfer count register are available (if use of the descriptor memory is only enabled for one channel) for use in setting up consecutive DMA transfers (the memory can hold register values for up to 256 stages of transfer when the external memory is selected). An infinite repeat mode is also available.

Figure 16.1 shows the block diagram of the SYS-DMAC.

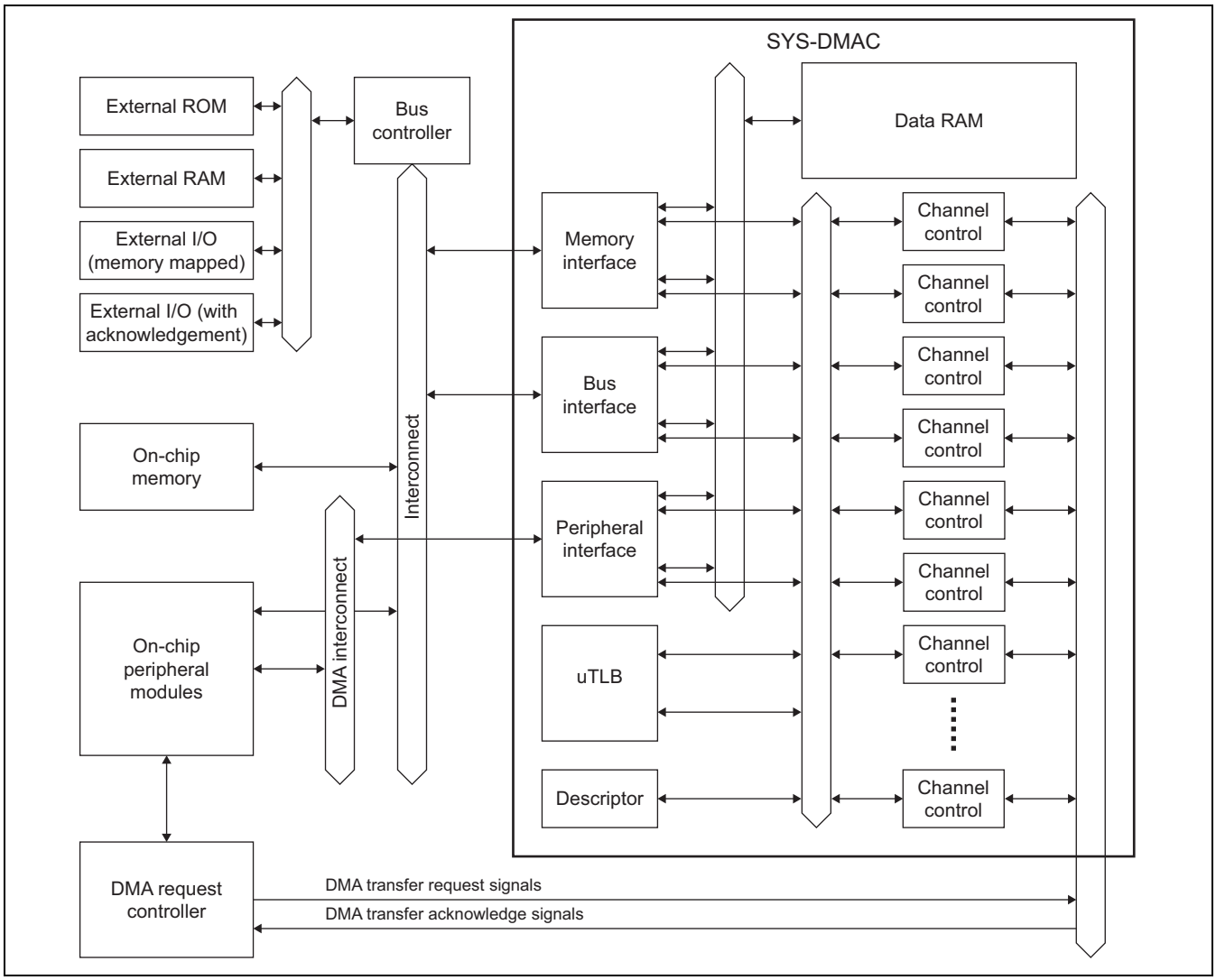


Figure 16.1 Block Diagram of the SYS-DMAC

16.2 Input/Output Pins

There are no external pins relevant to the SYS-DMAC.

16.3 Register Descriptions

Table 16.1 lists the registers of the SYS-DMAC. Table 16.2 shows the register states of the SYS-DMAC in each operating mode.

Table 16.1 Register Configuration of the SYS-DMAC

Name	Abbreviation	R/W	Address	Access Size
DMA interrupt status register (for lower-numbered channels)	DMAISTA_L	R	H'E670 0020	32
DMA secure control register (for lower-numbered channels)	DMASEC_L	R/W	H'E670 0030	32
DMA operation register (for lower-numbered channels)	DMAOR_L	R/W	H'E670 0060	16
DMA channel clear register (for lower-numbered channels)	DMACHCLR_L	W	H'E670 0080	32
DPRAM secure control register (for lower-numbered channels)	DMADPSEC_L	R/W	H'E670 00A0	32
DMA source address register_0	DMASAR_0	R/W	H'E670 8000 H'E670 8020*	32
DMA destination address register_0	DMADAR_0	R/W	H'E670 8004 H'E670 8024*	32
DMA transfer count register_0	DMATCR_0	R/W	H'E670 8008	32
DMA transfer size register_0	DMATSR_0	R/W	H'E670 8028*	32
DMA channel control register_0	DMACHCR_0	R/W	H'E670 800C H'E670 802C*	32
DMA transfer count register B_0	DMATCRB_0	R/W	H'E670 8018	32
DMA transfer size register B_0	DMATSRB_0	R/W	H'E670 8038	32
DMA channel control register B_0	DMACHCRB_0	R/W	H'E670 801C	32
DMA extended resource selector_0	DMARS_0	R/W	H'E670 8040	16
DMA buffer control register_0	DMABUFCR_0	R/W	H'E670 8048	32
DMA descriptor base address register_0	DMADPBASE_0	R/W	H'E670 8050	32
DMA descriptor control register_0	DMADPCR_0	R/W	H'E670 8054	32
DMA fixed source address register_0	DMAFIXSAR_0	R/W	H'E670 8010	32
DMA fixed destination address register_0	DMAFIXDAR_0	R/W	H'E670 8014	32
DMA fixed descriptor base address register_0	DMAFIXDP BASE_0	R/W	H'E670 8060	32
DMA source address register_1	DMASAR_1	R/W	H'E670 8080 H'E670 80A0*	32
DMA destination address register_1	DMADAR_1	R/W	H'E670 8084 H'E670 80A4*	32
DMA transfer count register_1	DMATCR_1	R/W	H'E670 8088	32
DMA transfer size register_1	DMATSR_1	R/W	H'E670 80A8*	32
DMA channel control register_1	DMACHCR_1	R/W	H'E670 808C H'E670 80AC*	32
DMA transfer count register B_1	DMATCRB_1	R/W	H'E670 8098	32
DMA transfer size register B_1	DMATSRB_1	R/W	H'E670 80B8*	32
DMA channel control register B_1	DMACHCRB_1	R/W	H'E670 809C	32
DMA extended resource selector_1	DMARS_1	R/W	H'E670 80C0	16

Name	Abbreviation	R/W	Address	Access Size
DMA buffer control register_1	DMABUFCR_1	R/W	H'E670 80C8	32
DMA descriptor base address register_1	DMADPBASE_1	R/W	H'E670 80D0	32
DMA descriptor control register_1	DMADPCR_1	R/W	H'E670 80D4	32
DMA fixed descriptor base address register_1	DMAFIXDPBASE_1	R/W	H'E670 80E0	32
DMA fixed source address register_1	DMAFIXSAR_1	R/W	H'E670 8090	32
DMA fixed destination address register_1	DMAFIXDAR_1	R/W	H'E670 8094	32
DMA source address register_2	DMASAR_2	R/W	H'E670 8100 H'E670 8120*	32
DMA destination address register_2	DMADAR_2	R/W	H'E670 8104 H'E670 8124*	32
DMA transfer count register_2	DMATCR_2	R/W	H'E670 8108	32
DMA transfer size register_2	DMATSR_2	R/W	H'E670 8128*	32
DMA channel control register_2	DMACHCR_2	R/W	H'E670 810C H'E670 812C*	32
DMA transfer count register B_2	DMATCRB_2	R/W	H'E670 8118	32
DMA transfer size register B_2	DMATSRB_2	R/W	H'E670 8138*	32
DMA channel control register B_2	DMACHCRB_2	R/W	H'E670 811C	32
DMA extended resource selector_2	DMARS_2	R/W	H'E670 8140	16
DMA buffer control register_2	DMABUFCR_2	R/W	H'E670 8148	32
DMA descriptor base address register_2	DMADPBASE_2	R/W	H'E670 8150	32
DMA descriptor control register_2	DMADPCR_2	R/W	H'E670 8154	32
DMA fixed source address register_2	DMAFIXSAR_2	R/W	H'E670 8110	32
DMA fixed destination address register_2	DMAFIXDAR_2	R/W	H'E670 8114	32
DMA fixed descriptor base address register_2	DMAFIXDPBASE_2	R/W	H'E670 8160	32
DMA source address register_3	DMASAR_3	R/W	H'E670 8180 H'E670 81A0*	32
DMA destination address register_3	DMADAR_3	R/W	H'E670 8184 H'E670 81A4*	32
DMA transfer count register_3	DMATCR_3	R/W	H'E670 8188	32
DMA transfer size register_3	DMATSR_3	R/W	H'E670 81A8*	32
DMA channel control register_3	DMACHCR_3	R/W	H'E670 818C H'E670 81AC*	32
DMA transfer count register B_3	DMATCRB_3	R/W	H'E670 8198	32
DMA transfer size register B_3	DMATSRB_3	R/W	H'E670 81B8*	32
DMA channel control register B_3	DMACHCRB_3	R/W	H'E670 819C	32
DMA extended resource selector_3	DMARS_3	R/W	H'E670 81C0	16
DMA buffer control register_3	DMABUFCR_3	R/W	H'E670 81C8	32
DMA descriptor base address register_3	DMADPBASE_3	R/W	H'E670 81D0	32
DMA descriptor control register_3	DMADPCR_3	R/W	H'E670 81D4	32
DMA fixed source address register_3	DMAFIXSAR_3	R/W	H'E670 8190	32
DMA fixed destination address register_3	DMAFIXDAR_3	R/W	H'E670 8194	32
DMA fixed descriptor base address register_3	DMAFIXDPBASE_3	R/W	H'E670 81E0	32
DMA source address register_4	DMASAR_4	R/W	H'E670 8200 H'E670 8220*	32

Name	Abbreviation	R/W	Address	Access Size
DMA destination address register_4	DMADAR_4	R/W	H'E670 8204 H'E670 8224*	32
DMA transfer count register_4	DMATCR_4	R/W	H'E670 8208	32
DMA transfer size register_4	DMATSR_4	R/W	H'E670 8228*	32
DMA channel control register_4	DMACHCR_4	R/W	H'E670 820C H'E670 822C*	32
DMA transfer count register B_4	DMATCRB_4	R/W	H'E670 8218	32
DMA transfer size register B_4	DMATSRB_4	R/W	H'E670 8238*	32
DMA channel control register B_4	DMACHCRB_4	R/W	H'E670 821C	32
DMA extended resource selector_4	DMARS_4	R/W	H'E670 8240	16
DMA buffer control register_4	DMABUFCR_4	R/W	H'E670 8248	32
DMA descriptor base address register_4	DMADPBASE_4	R/W	H'E670 8250	32
DMA descriptor control register_4	DMADPCR_4	R/W	H'E670 8254	32
DMA fixed source address register_4	DMAFIXSAR_4	R/W	H'E670 8210	32
DMA fixed destination address register_4	DMAFIXDAR_4	R/W	H'E670 8214	32
DMA fixed descriptor base address register_4	DMAFIXDPBASE_4	R/W	H'E670 8260	32
DMA source address register_5	DMASAR_5	R/W	H'E670 8280 H'E670 82A0*	32
DMA destination address register_5	DMADAR_5	R/W	H'E670 8284 H'E670 82A4*	32
DMA transfer count register_5	DMATCR_5	R/W	H'E670 8288	32
DMA transfer size register_5	DMATSR_5	R/W	H'E670 82A8*	32
DMA channel control register_5	DMACHCR_5	R/W	H'E670 828C H'E670 82AC*	32
DMA transfer count register B_5	DMATCRB_5	R/W	H'E670 8298	32
DMA transfer size register B_5	DMATSRB_5	R/W	H'E670 82B8*	32
DMA channel control register B_5	DMACHCRB_5	R/W	H'E670 829C	32
DMA extended resource selector_5	DMARS_5	R/W	H'E670 82C0	16
DMA buffer control register_5	DMABUFCR_5	R/W	H'E670 82C8	32
DMA descriptor base address register_5	DMADPBASE_5	R/W	H'E670 82D0	32
DMA descriptor control register_5	DMADPCR_5	R/W	H'E670 82D4	32
DMA fixed source address register_5	DMAFIXSAR_5	R/W	H'E670 8290	32
DMA fixed destination address register_5	DMAFIXDAR_5	R/W	H'E670 8294	32
DMA fixed descriptor base address register_5	DMAFIXDPBASE_5	R/W	H'E670 82E0	32
DMA source address register_6	DMASAR_6	R/W	H'E670 8300 H'E670 8320*	32
DMA destination address register_6	DMADAR_6	R/W	H'E670 8304 H'E670 8324*	32
DMA transfer count register_6	DMATCR_6	R/W	H'E670 8308	32
DMA transfer size register_6	DMATSR_6	R/W	H'E670 8328*	32
DMA channel control register_6	DMACHCR_6	R/W	H'E670 830C H'E670 832C*	32
DMA transfer count register B_6	DMATCRB_6	R/W	H'E670 8318	32
DMA transfer size register B_6	DMATSRB_6	R/W	H'E670 8338*	32
DMA channel control register B_6	DMACHCRB_6	R/W	H'E670 831C	32

Name	Abbreviation	R/W	Address	Access Size
DMA extended resource selector_6	DMARS_6	R/W	H'E670 8340	16
DMA buffer control register_6	DMABUFCR_6	R/W	H'E670 8348	32
DMA descriptor base address register_6	DMADPBASE_6	R/W	H'E670 8350	32
DMA descriptor control register_6	DMADPCR_6	R/W	H'E670 8354	32
DMA fixed source address register_6	DMAFIXSAR_6	R/W	H'E670 8310	32
DMA fixed destination address register_6	DMAFIXDAR_6	R/W	H'E670 8314	32
DMA fixed descriptor base address register_6	DMAFIXDPBASE_6	R/W	H'E670 8360	32
DMA source address register_7	DMASAR_7	R/W	H'E670 8380 H'E670 83A0*	32
DMA destination address register_7	DMADAR_7	R/W	H'E670 8384 H'E670 83A4*	32
DMA transfer count register_7	DMATCR_7	R/W	H'E670 8388	32
DMA transfer size register_7	DMATSR_7	R/W	H'E670 83A8*	32
DMA channel control register_7	DMACHCR_7	R/W	H'E670 838C H'E670 83AC*	32
DMA transfer count register B_7	DMATCRB_7	R/W	H'E670 8398	32
DMA transfer size register B_7	DMATSRB_7	R/W	H'E670 83B8*	32
DMA channel control register B_7	DMACHCRB_7	R/W	H'E670 839C	32
DMA extended resource selector_7	DMARS_7	R/W	H'E670 83C0	16
DMA buffer control register_7	DMABUFCR_7	R/W	H'E670 83C8	32
DMA descriptor base address register_7	DMADPBASE_7	R/W	H'E670 83D0	32
DMA descriptor control register_7	DMADPCR_7	R/W	H'E670 83D4	32
DMA fixed source address register_7	DMAFIXSAR_7	R/W	H'E670 8390	32
DMA fixed destination address register_7	DMAFIXDAR_7	R/W	H'E670 8394	32
DMA fixed descriptor base address register_7	DMAFIXDPBASE_7	R/W	H'E670 83E0	32
DMA source address register_8	DMASAR_8	R/W	H'E670 8400 H'E670 8420*	32
DMA destination address register_8	DMADAR_8	R/W	H'E670 8404 H'E670 8424*	32
DMA transfer count register_8	DMATCR_8	R/W	H'E670 8408	32
DMA transfer size register_8	DMATSR_8	R/W	H'E670 8428*	32
DMA channel control register_8	DMACHCR_8	R/W	H'E670 840C H'E670 842C*	32
DMA transfer count register B_8	DMATCRB_8	R/W	H'E670 8418	32
DMA transfer size register B_8	DMATSRB_8	R/W	H'E670 8438*	32
DMA channel control register B_8	DMACHCRB_8	R/W	H'E670 841C	32
DMA extended resource selector_8	DMARS_8	R/W	H'E670 8440	16
DMA buffer control register_8	DMABUFCR_8	R/W	H'E670 8448	32
DMA descriptor base address register_8	DMADPBASE_8	R/W	H'E670 8450	32
DMA descriptor control register_8	DMADPCR_8	R/W	H'E670 8454	32
DMA fixed source address register_8	DMAFIXSAR_8	R/W	H'E670 8410	32
DMA fixed destination address register_8	DMAFIXDAR_8	R/W	H'E670 8414	32
DMA fixed descriptor base address register_8	DMAFIXDPBASE_8	R/W	H'E670 8460	32

Name	Abbreviation	R/W	Address	Access Size
DMA source address register_9	DMASAR_9	R/W	H'E670 8480 H'E670 84A0*	32
DMA destination address register_9	DMADAR_9	R/W	H'E670 8484 H'E670 84A4*	32
DMA transfer count register_9	DMATCR_9	R/W	H'E670 8488	32
DMA transfer size register_9	DMATSR_9	R/W	H'E670 84A8*	32
DMA channel control register_9	DMACHCR_9	R/W	H'E670 848C H'E670 84AC*	32
DMA transfer count register B_9	DMATCRB_9	R/W	H'E670 8498	32
DMA transfer size register B_9	DMATSRB_9	R/W	H'E670 84B8*	32
DMA channel control register B_9	DMACHCRB_9	R/W	H'E670 849C	32
DMA extended resource selector_9	DMARS_9	R/W	H'E670 84C0	16
DMA buffer control register_9	DMABUFCR_9	R/W	H'E670 84C8	32
DMA descriptor base address register_9	DMADPBASE_9	R/W	H'E670 84D0	32
DMA descriptor control register_9	DMADPCR_9	R/W	H'E670 84D4	32
DMA fixed source address register_9	DMAFIXSAR_9	R/W	H'E670 8490	32
DMA fixed destination address register_9	DMAFIXDAR_9	R/W	H'E670 8494	32
DMA fixed descriptor base address register_9	DMAFIXDPBASE_9	R/W	H'E670 84E0	32
DMA source address register_10	DMASAR_10	R/W	H'E670 8500 H'E670 8520*	32
DMA destination address register_10	DMADAR_10	R/W	H'E670 8504 H'E670 8524*	32
DMA transfer count register_10	DMATCR_10	R/W	H'E670 8508	32
DMA transfer size register_10	DMATSR_10	R/W	H'E670 8528*	32
DMA channel control register_10	DMACHCR_10	R/W	H'E670 850C H'E670 852C*	32
DMA transfer count register B_10	DMATCRB_10	R/W	H'E670 8518	32
DMA transfer size register B_10	DMATSRB_10	R/W	H'E670 8538*	32
DMA channel control register B_10	DMACHCRB_10	R/W	H'E670 851C	32
DMA extended resource selector_10	DMARS_10	R/W	H'E670 8540	16
DMA buffer control register_10	DMABUFCR_10	R/W	H'E670 8548	32
DMA descriptor base address register_10	DMADPBASE_10	R/W	H'E670 8550	32
DMA descriptor control register_10	DMADPCR_10	R/W	H'E670 8554	32
DMA fixed source address register_10	DMAFIXSAR_10	R/W	H'E670 8510	32
DMA fixed destination address register_10	DMAFIXDAR_10	R/W	H'E670 8514	32
DMA fixed descriptor base address register_10	DMAFIXDPBASE_10	R/W	H'E670 8560	32
DMA source address register_11	DMASAR_11	R/W	H'E670 8580 H'E670 85A0*	32
DMA destination address register_11	DMADAR_11	R/W	H'E670 8584 H'E670 85A4*	32
DMA transfer count register_11	DMATCR_11	R/W	H'E670 8588	32
DMA transfer size register_11	DMATSR_11	R/W	H'E670 85A8*	32
DMA channel control register_11	DMACHCR_11	R/W	H'E670 858C H'E670 85AC*	32
DMA transfer count register B_11	DMATCRB_11	R/W	H'E670 8598	32

Name	Abbreviation	R/W	Address	Access Size
DMA transfer size register B_11	DMATSRB_11	R/W	H'E670 85B8*	32
DMA channel control register B_11	DMACHCRB_11	R/W	H'E670 859C	32
DMA extended resource selector_11	DMARS_11	R/W	H'E670 85C0	16
DMA buffer control register_11	DMABUFCR_11	R/W	H'E670 85C8	32
DMA descriptor base address register_11	DMADPBASE_11	R/W	H'E670 85D0	32
DMA descriptor control register_11	DMADPCR_11	R/W	H'E670 85D4	32
DMA fixed source address register_11	DMAFIXSAR_11	R/W	H'E670 8590	32
DMA fixed destination address register_11	DMAFIXDAR_11	R/W	H'E670 8594	32
DMA fixed descriptor base address register_11	DMAFIXDPBASE_11	R/W	H'E670 85E0	32
DMA source address register_12	DMASAR_12	R/W	H'E670 8600 H'E670 8620*	32
DMA destination address register_12	DMADAR_12	R/W	H'E670 8604 H'E670 8624*	32
DMA transfer count register_12	DMATCR_12	R/W	H'E670 8608	32
DMA transfer size register_12	DMATSR_12	R/W	H'E670 8628*	32
DMA channel control register_12	DMACHCR_12	R/W	H'E670 860C H'E670 862C*	32
DMA transfer count register B_12	DMATCRB_12	R/W	H'E670 8618	32
DMA transfer size register B_12	DMATSRB_12	R/W	H'E670 8638*	32
DMA channel control register B_12	DMACHCRB_12	R/W	H'E670 861C	32
DMA extended resource selector_12	DMARS_12	R/W	H'E670 8640	16
DMA buffer control register_12	DMABUFCR_12	R/W	H'E670 8648	32
DMA descriptor base address register_12	DMADPBASE_12	R/W	H'E670 8650	32
DMA descriptor control register_12	DMADPCR_12	R/W	H'E670 8654	32
DMA fixed source address register_12	DMAFIXSAR_12	R/W	H'E670 8610	32
DMA fixed destination address register_12	DMAFIXDAR_12	R/W	H'E670 8614	32
DMA fixed descriptor base address register_12	DMAFIXDPBASE_12	R/W	H'E670 8660	32
DMA source address register_13	DMASAR_13	R/W	H'E670 8680 H'E670 86A0*	32
DMA destination address register_13	DMADAR_13	R/W	H'E670 8684 H'E670 86A4*	32
DMA transfer count register_13	DMATCR_13	R/W	H'E670 8688	32
DMA transfer size register_13	DMATSR_13	R/W	H'E670 86A8*	32
DMA channel control register_13	DMACHCR_13	R/W	H'E670 868C H'E670 86AC*	32
DMA transfer count register B_13	DMATCRB_13	R/W	H'E670 8698	32
DMA transfer size register B_13	DMATSRB_13	R/W	H'E670 86B8*	32
DMA channel control register B_13	DMACHCRB_13	R/W	H'E670 869C	32
DMA extended resource selector_13	DMARS_13	R/W	H'E670 86C0	16
DMA buffer control register_13	DMABUFCR_13	R/W	H'E670 86C8	32
DMA descriptor base address register_13	DMADPBASE_13	R/W	H'E670 86D0	32
DMA descriptor control register_13	DMADPCR_13	R/W	H'E670 86D4	32
DMA fixed source address register_13	DMAFIXSAR_13	R/W	H'E670 8690	32
DMA fixed destination address register_13	DMAFIXDAR_13	R/W	H'E670 8694	32

Name	Abbreviation	R/W	Address	Access Size
DMA fixed descriptor base address register_13	DMAFIXDPBASE_13	R/W	H'E670 86E0	32
DMA source address register_14	DMASAR_14	R/W	H'E670 8700 H'E670 8720*	32
DMA destination address register_14	DMADAR_14	R/W	H'E670 8704 H'E670 8724*	32
DMA transfer count register_14	DMATCR_14	R/W	H'E670 8708	32
DMA transfer size register_14	DMATSR_14	R/W	H'E670 8728*	32
DMA channel control register_14	DMACHCR_14	R/W	H'E670 870C H'E670 872C*	32
DMA transfer count register B_14	DMATCRB_14	R/W	H'E670 8718	32
DMA transfer size register B_14	DMATSRB_14	R/W	H'E670 8738*	32
DMA channel control register B_14	DMACHCRB_14	R/W	H'E670 871C	32
DMA extended resource selector_14	DMARS_14	R/W	H'E670 8740	16
DMA buffer control register_14	DMABUFCR_14	R/W	H'E670 8748	32
DMA descriptor base address register_14	DMADPBASE_14	R/W	H'E670 8750	32
DMA descriptor control register_14	DMADPCR_14	R/W	H'E670 8754	32
DMA fixed source address register_14	DMAFIXSAR_14	R/W	H'E670 8710	32
DMA fixed destination address register_14	DMAFIXDAR_14	R/W	H'E670 8714	32
DMA fixed descriptor base address register_14	DMAFIXDPBASE_14	R/W	H'E670 8760	32
Descriptor memory (for lower-numbered channels)	DescriptorMEM	R/W	H'E670 A000 to H'E670 A7FC	32
DMA interrupt status register (for higher-numbered channels)	DMAISTA_U	R	H'E672 0020	32
DMA secure control register (for higher-numbered channels)	DMASEC_U	R/W	H'E672 0030	32
DMA operation register (for higher-numbered channels)	DMAOR_U	R/W	H'E672 0060	16
DMA channel clear register (for higher-numbered channels)	DMACHCLR_U	W	H'E672 0080	32
DPRAM secure control register (for higher-numbered channels)	DMADPSEC_U	R/W	H'E672 00A0	32
DMA source address register_15	DMASAR_15	R/W	H'E672 8000 H'E672 8020*	32
DMA destination address register_15	DMADAR_15	R/W	H'E672 8004 H'E672 8024*	32
DMA transfer count register_15	DMATCR_15	R/W	H'E672 8008	32
DMA transfer size register_15	DMATSR_15	R/W	H'E672 8028	32
DMA channel control register_15	DMACHCR_15	R/W	H'E672 800C H'E672 802C*	32
DMA transfer count register B_15	DMATCRB_15	R/W	H'E672 8018	32
DMA transfer size register B_15	DMATSRB_15	R/W	H'E672 8038	32
DMA channel control register B_15	DMACHCRB_15	R/W	H'E672 801C	32
DMA extended resource selector_15	DMARS_15	R/W	H'E672 8040	16
DMA buffer control register_15	DMABUFCR_15	R/W	H'E672 8048	32
DMA descriptor base address register_15	DMADPBASE_15	R/W	H'E672 8050	32
DMA descriptor control register_15	DMADPCR_15	R/W	H'E672 8054	32

Name	Abbreviation	R/W	Address	Access Size
DMA fixed source address register_15	DMAFIXSAR_15	R/W	H'E672 8010	32
DMA fixed destination address register_15	DMAFIXDAR_15	R/W	H'E672 8014	32
DMA fixed descriptor base address register_15	DMAFIXDPBASE_15	R/W	H'E672 8060	32
DMA source address register_16	DMASAR_16	R/W	H'E672 8080 H'E672 80A0*	32
DMA destination address register_16	DMADAR_16	R/W	H'E672 8084 H'E672 80A4*	32
DMA transfer count register_16	DMATCR_16	R/W	H'E672 8088	32
DMA transfer size register_16	DMATSR_16	R/W	H'E672 80A8*	32
DMA channel control register_16	DMACHCR_16	R/W	H'E672 808C H'E67280AC*	32
DMA transfer count register B_16	DMATCRB_16	R/W	H'E672 8098	32
DMA transfer size register B_16	DMATSRB_16	R/W	H'E672 80B8*	32
DMA channel control register B_16	DMACHCRB_16	R/W	H'E672 809C	32
DMA extended resource selector_16	DMARS_16	R/W	H'E672 80C0	16
DMA buffer control register_16	DMABUFCR_16	R/W	H'E672 80C8	32
DMA descriptor base address register_16	DMADPBASE_16	R/W	H'E672 80D0	32
DMA descriptor control register_16	DMADPCR_16	R/W	H'E672 80D4	32
DMA fixed descriptor base address register_16	DMAFIXDPBASE_16	R/W	H'E672 80E0	32
DMA fixed source address register_16	DMAFIXSAR_16	R/W	H'E672 8090	32
DMA fixed destination address register_16	DMAFIXDAR_16	R/W	H'E672 8094	32
DMA source address register_17	DMASAR_17	R/W	H'E672 8100 H'E672 8120*	32
DMA destination address register_17	DMADAR_17	R/W	H'E672 8104 H'E672 8124*	32
DMA transfer count register_17	DMATCR_17	R/W	H'E672 8108	32
DMA transfer size register_17	DMATSR_17	R/W	H'E672 8128*	32
DMA channel control register_17	DMACHCR_17	R/W	H'E672 810C H'E672 812C*	32
DMA transfer count register B_17	DMATCRB_17	R/W	H'E672 8118	32
DMA transfer size register B_17	DMATSRB_17	R/W	H'E672 8138*	32
DMA channel control register B_17	DMACHCRB_17	R/W	H'E672 811C	32
DMA extended resource selector_17	DMARS_17	R/W	H'E672 8140	16
DMA buffer control register_17	DMABUFCR_17	R/W	H'E672 8148	32
DMA descriptor base address register_17	DMADPBASE_17	R/W	H'E672 8150	32
DMA descriptor control register_17	DMADPCR_17	R/W	H'E672 8154	32
DMA fixed source address register_17	DMAFIXSAR_17	R/W	H'E672 8110	32
DMA fixed destination address register_17	DMAFIXDAR_17	R/W	H'E672 8114	32
DMA fixed descriptor base address register_17	DMAFIXDPBASE_17	R/W	H'E672 8160	32
DMA source address register_18	DMASAR_18	R/W	H'E672 8180 H'E672 81A0*	32
DMA destination address register_18	DMADAR_18	R/W	H'E672 8184 H'E672 81A4*	32
DMA transfer count register_18	DMATCR_18	R/W	H'E672 8188	32
DMA transfer size register_18	DMATSR_18	R/W	H'E672 81A8*	32

Name	Abbreviation	R/W	Address	Access Size
DMA channel control register_18	DMACHCR_18	R/W	H'E672 818C H'E672 81AC*	32
DMA transfer count register B_18	DMATCRB_18	R/W	H'E672 8198	32
DMA transfer size register B_18	DMATSRB_18	R/W	H'E672 81B8*	32
DMA channel control register B_18	DMACHCRB_18	R/W	H'E672 819C	32
DMA extended resource selector_18	DMARS_18	R/W	H'E672 81C0	16
DMA buffer control register_18	DMABUFCR_18	R/W	H'E672 81C8	32
DMA descriptor base address register_18	DMADPBASE_18	R/W	H'E672 81D0	32
DMA descriptor control register_18	DMADPCR_18	R/W	H'E672 81D4	32
DMA fixed source address register_18	DMAFIXSAR_18	R/W	H'E672 8190	32
DMA fixed destination address register_18	DMAFIXDAR_18	R/W	H'E672 8194	32
DMA fixed descriptor base address register_18	DMAFIXDPBASE_18	R/W	H'E672 81E0	32
DMA source address register_19	DMASAR_19	R/W	H'E672 8200 H'E672 8220*	32
DMA destination address register_19	DMADAR_19	R/W	H'E672 8204 H'E672 8224*	32
DMA transfer count register_19	DMATCR_19	R/W	H'E672 8208	32
DMA transfer size register_19	DMATSR_19	R/W	H'E672 8228*	32
DMA channel control register_19	DMACHCR_19	R/W	H'E672 820C H'E672 822C*	32
DMA transfer count register B_19	DMATCRB_19	R/W	H'E672 8218	32
DMA transfer size register B_19	DMATSRB_19	R/W	H'E672 8238*	32
DMA channel control register B_19	DMACHCRB_19	R/W	H'E672 821C	32
DMA extended resource selector_19	DMARS_19	R/W	H'E672 8240	16
DMA buffer control register_19	DMABUFCR_19	R/W	H'E672 8248	32
DMA descriptor base address register_19	DMADPBASE_19	R/W	H'E672 8250	32
DMA descriptor control register_19	DMADPCR_19	R/W	H'E672 8254	32
DMA fixed source address register_19	DMAFIXSAR_19	R/W	H'E672 8210	32
DMA fixed destination address register_19	DMAFIXDAR_19	R/W	H'E672 8214	32
DMA fixed descriptor base address register_19	DMAFIXDPBASE_19	R/W	H'E672 8260	32
DMA source address register_20	DMASAR_20	R/W	H'E672 8280 H'E672 82A0*	32
DMA destination address register_20	DMADAR_20	R/W	H'E672 8284 H'E672 82A4*	32
DMA transfer count register_20	DMATCR_20	R/W	H'E672 8288	32
DMA transfer size register_20	DMATSR_20	R/W	H'E672 82A8*	32
DMA channel control register_20	DMACHCR_20	R/W	H'E672 828C H'E672 82AC*	32
DMA transfer count register B_20	DMATCRB_20	R/W	H'E672 8298	32
DMA transfer size register B_20	DMATSRB_20	R/W	H'E672 82B8*	32
DMA channel control register B_20	DMACHCRB_20	R/W	H'E672 829C	32
DMA extended resource selector_20	DMARS_20	R/W	H'E672 82C0	16
DMA buffer control register_20	DMABUFCR_20	R/W	H'E672 82C8	32
DMA descriptor base address register_20	DMADPBASE_20	R/W	H'E672 82D0	32

Name	Abbreviation	R/W	Address	Access Size
DMA descriptor control register_20	DMADPCR_20	R/W	H'E672 82D4	32
DMA fixed source address register_20	DMAFIXSAR_20	R/W	H'E672 8290	32
DMA fixed destination address register_20	DMAFIXDAR_20	R/W	H'E672 8294	32
DMA fixed descriptor base address register_20	DMAFIXDPBASE_20	R/W	H'E672 82E0	32
DMA source address register_21	DMASAR_21	R/W	H'E672 8300 H'E672 8320*	32
DMA destination address register_21	DMADAR_21	R/W	H'E672 8304 H'E672 8324*	32
DMA transfer count register_21	DMATCR_21	R/W	H'E672 8308	32
DMA transfer size register_21	DMATSR_21	R/W	H'E672 8328*	32
DMA channel control register_21	DMACHCR_21	R/W	H'E672 830C H'E672 832C*	32
DMA transfer count register B_21	DMATCRB_21	R/W	H'E672 8318	32
DMA transfer size register B_21	DMATSRB_21	R/W	H'E672 8338*	32
DMA channel control register B_21	DMACHCRB_21	R/W	H'E672 831C	32
DMA extended resource selector_21	DMARS_21	R/W	H'E672 8340	16
DMA buffer control register_21	DMABUFCR_21	R/W	H'E672 8348	32
DMA descriptor base address register_21	DMADPBASE_21	R/W	H'E672 8350	32
DMA descriptor control register_21	DMADPCR_21	R/W	H'E672 8354	32
DMA fixed source address register_21	DMAFIXSAR_21	R/W	H'E672 8310	32
DMA fixed destination address register_21	DMAFIXDAR_21	R/W	H'E672 8314	32
DMA fixed descriptor base address register_21	DMAFIXDPBASE_21	R/W	H'E672 8360	32
DMA source address register_22	DMASAR_22	R/W	H'E672 8380 H'E672 83A0*	32
DMA destination address register_22	DMADAR_22	R/W	H'E672 8384 H'E672 83A4*	32
DMA transfer count register_22	DMATCR_22	R/W	H'E672 8388	32
DMA transfer size register_22	DMATSR_22	R/W	H'E672 83A8*	32
DMA channel control register_22	DMACHCR_22	R/W	H'E672 838C H'E672 83AC*	32
DMA transfer count register B_22	DMATCRB_22	R/W	H'E672 8398	32
DMA transfer size register B_22	DMATSRB_22	R/W	H'E672 83B8*	32
DMA channel control register B_22	DMACHCRB_22	R/W	H'E672 839C	32
DMA extended resource selector_22	DMARS_22	R/W	H'E672 83C0	16
DMA buffer control register_22	DMABUFCR_22	R/W	H'E672 83C8	32
DMA descriptor base address register_22	DMADPBASE_22	R/W	H'E672 83D0	32
DMA descriptor control register_22	DMADPCR_22	R/W	H'E672 83D4	32
DMA fixed source address register_22	DMAFIXSAR_22	R/W	H'E672 8390	32
DMA fixed destination address register_22	DMAFIXDAR_22	R/W	H'E672 8394	32
DMA fixed descriptor base address register_22	DMAFIXDPBASE_22	R/W	H'E672 83E0	32
DMA source address register_23	DMASAR_23	R/W	H'E672 8400 H'E672 8420*	32
DMA destination address register_23	DMADAR_23	R/W	H'E672 8404 H'E672 8424*	32
DMA transfer count register_23	DMATCR_23	R/W	H'E672 8408	32

Name	Abbreviation	R/W	Address	Access Size
DMA transfer size register_23	DMATSR_23	R/W	H'E672 8428*	32
DMA channel control register_23	DMACHCR_23	R/W	H'E672 840C H'E672 842C*	32
DMA transfer count register B_23	DMATCRB_23	R/W	H'E672 8418	32
DMA transfer size register B_23	DMATSRB_23	R/W	H'E672 8438*	32
DMA channel control register B_23	DMACHCRB_23	R/W	H'E672 841C	32
DMA extended resource selector_23	DMARS_23	R/W	H'E672 8440	16
DMA buffer control register_23	DMABUFCR_23	R/W	H'E672 8448	32
DMA descriptor base address register_23	DMADPBASE_23	R/W	H'E672 8450	32
DMA descriptor control register_23	DMADPCR_23	R/W	H'E672 8454	32
DMA fixed source address register_23	DMAFIXSAR_23	R/W	H'E672 8410	32
DMA fixed destination address register_23	DMAFIXDAR_23	R/W	H'E672 8414	32
DMA fixed descriptor base address register_23	DMAFIXDPBASE_23	R/W	H'E672 8460	32
DMA source address register_24	DMASAR_24	R/W	H'E672 8480 H'E672 84A0*	32
DMA destination address register_24	DMADAR_24	R/W	H'E672 8484 H'E672 84A4*	32
DMA transfer count register_24	DMATCR_24	R/W	H'E672 8488	32
DMA transfer size register_24	DMATSR_24	R/W	H'E672 84A8*	32
DMA channel control register_24	DMACHCR_24	R/W	H'E672 848C H'E672 84AC*	32
DMA transfer count register B_24	DMATCRB_24	R/W	H'E672 8498	32
DMA transfer size register B_24	DMATSRB_24	R/W	H'E672 84B8*	32
DMA channel control register B_24	DMACHCRB_24	R/W	H'E672 849C	32
DMA extended resource selector_24	DMARS_24	R/W	H'E672 84C0	16
DMA buffer control register_24	DMABUFCR_24	R/W	H'E672 84C8	32
DMA descriptor base address register_24	DMADPBASE_24	R/W	H'E672 84D0	32
DMA descriptor control register_24	DMADPCR_24	R/W	H'E672 84D4	32
DMA fixed source address register_24	DMAFIXSAR_24	R/W	H'E672 8490	32
DMA fixed destination address register_24	DMAFIXDAR_24	R/W	H'E672 8494	32
DMA fixed descriptor base address register_24	DMAFIXDPBASE_24	R/W	H'E672 84E0	32
DMA source address register_25	DMASAR_25	R/W	H'E672 8500 H'E672 8520*	32
DMA destination address register_25	DMADAR_25	R/W	H'E672 8504 H'E672 8524*	32
DMA transfer count register_25	DMATCR_25	R/W	H'E672 8508	32
DMA transfer size register_25	DMATSR_25	R/W	H'E672 8528*	32
DMA channel control register_25	DMACHCR_25	R/W	H'E672 850C H'E672 852C*	32
DMA transfer count register B_25	DMATCRB_25	R/W	H'E672 8518	32
DMA transfer size register B_25	DMATSRB_25	R/W	H'E672 8538*	32
DMA channel control register B_25	DMACHCRB_25	R/W	H'E672 851C	32
DMA extended resource selector_25	DMARS_25	R/W	H'E672 8540	16
DMA buffer control register_25	DMABUFCR_25	R/W	H'E672 8548	32

Name	Abbreviation	R/W	Address	Access Size
DMA descriptor base address register_25	DMADPBASE_25	R/W	H'E672 8550	32
DMA descriptor control register_25	DMADPCR_25	R/W	H'E672 8554	32
DMA fixed source address register_25	DMAFIXSAR_25	R/W	H'E672 8510	32
DMA fixed destination address register_25	DMAFIXDAR_25	R/W	H'E672 8514	32
DMA fixed descriptor base address register_25	DMAFIXDPBASE_25	R/W	H'E672 8560	32
DMA source address register_26	DMASAR_26	R/W	H'E672 8580 H'E672 85A0*	32
DMA destination address register_26	DMADAR_26	R/W	H'E672 8584 H'E672 85A4*	32
DMA transfer count register_26	DMATCR_26	R/W	H'E672 8588	32
DMA transfer size register_26	DMATSR_26	R/W	H'E672 85A8*	32
DMA channel control register_26	DMACHCR_26	R/W	H'E672 858C H'E672 85AC*	32
DMA transfer count register B_26	DMATCRB_26	R/W	H'E672 8598	32
DMA transfer size register B_26	DMATSRB_26	R/W	H'E672 85B8*	32
DMA channel control register B_26	DMACHCRB_26	R/W	H'E672 859C	32
DMA extended resource selector_26	DMARS_26	R/W	H'E672 85C0	16
DMA buffer control register_26	DMABUFCR_26	R/W	H'E672 85C8	32
DMA descriptor base address register_26	DMADPBASE_26	R/W	H'E672 85D0	32
DMA descriptor control register_26	DMADPCR_26	R/W	H'E672 85D4	32
DMA fixed source address register_26	DMAFIXSAR_26	R/W	H'E672 8590	32
DMA fixed destination address register_26	DMAFIXDAR_26	R/W	H'E672 8594	32
DMA fixed descriptor base address register_26	DMAFIXDPBASE_26	R/W	H'E672 85E0	32
DMA source address register_27	DMASAR_27	R/W	H'E672 8600 H'E672 8620*	32
DMA destination address register_27	DMADAR_27	R/W	H'E672 8604 H'E672 8624*	32
DMA transfer count register_27	DMATCR_27	R/W	H'E672 8608	32
DMA transfer size register_27	DMATSR_27	R/W	H'E672 8628*	32
DMA channel control register_27	DMACHCR_27	R/W	H'E672 860C H'E672 862C*	32
DMA transfer count register B_27	DMATCRB_27	R/W	H'E672 8618	32
DMA transfer size register B_27	DMATSRB_27	R/W	H'E672 8638*	32
DMA channel control register B_27	DMACHCRB_27	R/W	H'E672 861C	32
DMA extended resource selector_27	DMARS_27	R/W	H'E672 8640	16
DMA buffer control register_27	DMABUFCR_27	R/W	H'E672 8648	32
DMA descriptor base address register_27	DMADPBASE_27	R/W	H'E672 8650	32
DMA descriptor control register_27	DMADPCR_27	R/W	H'E672 8654	32
DMA fixed source address register_27	DMAFIXSAR_27	R/W	H'E672 8610	32
DMA fixed destination address register_27	DMAFIXDAR_27	R/W	H'E672 8614	32
DMA fixed descriptor base address register_27	DMAFIXDPBASE_27	R/W	H'E672 8660	32
DMA source address register_28	DMASAR_28	R/W	H'E672 8680 H'E672 86A0*	32
DMA destination address register_28	DMADAR_28	R/W	H'E672 8684 H'E672 86A4*	32

Name	Abbreviation	R/W	Address	Access Size
DMA transfer count register_28	DMATCR_28	R/W	H'E672 8688	32
DMA transfer size register_28	DMATSR_28	R/W	H'E672 86A8*	32
DMA channel control register_28	DMACHCR_28	R/W	H'E672 868C H'E672 86AC*	32
DMA transfer count register B_28	DMATCRB_28	R/W	H'E672 8698	32
DMA transfer size register B_28	DMATSRB_28	R/W	H'E672 86B8*	32
DMA channel control register B_28	DMACHCRB_28	R/W	H'E672 869C	32
DMA extended resource selector_28	DMARS_28	R/W	H'E672 86C0	16
DMA buffer control register_28	DMABUFCR_28	R/W	H'E672 86C8	32
DMA descriptor base address register_28	DMADPBASE_28	R/W	H'E672 86D0	32
DMA descriptor control register_28	DMADPCR_28	R/W	H'E672 86D4	32
DMA fixed source address register_28	DMAFIXSAR_28	R/W	H'E672 8690	32
DMA fixed destination address register_28	DMAFIXDAR_28	R/W	H'E672 8694	32
DMA fixed descriptor base address register_28	DMAFIXDPBASE_28	R/W	H'E672 86E0	32
DMA source address register_29	DMASAR_29	R/W	H'E672 8700 H'E672 8720*	32
DMA destination address register_29	DMADAR_29	R/W	H'E672 8704 H'E672 8724*	32
DMA transfer count register_29	DMATCR_29	R/W	H'E672 8708	32
DMA transfer size register_29	DMATSR_29	R/W	H'E672 8728*	32
DMA channel control register_29	DMACHCR_29	R/W	H'E672 870C H'E672 872C*	32
DMA transfer count register B_29	DMATCRB_29	R/W	H'E672 8718	32
DMA transfer size register B_29	DMATSRB_29	R/W	H'E672 8738*	32
DMA channel control register B_29	DMACHCRB_29	R/W	H'E672 871C	32
DMA extended resource selector_29	DMARS_29	R/W	H'E672 8740	16
DMA buffer control register_29	DMABUFCR_29	R/W	H'E672 8748	32
DMA descriptor base address register_29	DMADPBASE_29	R/W	H'E672 8750	32
DMA descriptor control register_29	DMADPCR_29	R/W	H'E672 8754	32
DMA fixed source address register_29	DMAFIXSAR_29	R/W	H'E672 8710	32
DMA fixed destination address register_29	DMAFIXDAR_29	R/W	H'E672 8714	32
DMA fixed descriptor base address register_29	DMAFIXDPBASE_29	R/W	H'E672 8760	32
Descriptor memory (for higher-numbered channels)	DescriptorMEM	R/W	H'E672 A000 to H'E672 A7FC	32

Note: The base address of registers for the lower-numbered channels (0 to 14) is H'E670 0000.
The base address of registers for the higher-numbered channels (15 to 29) is H'E672 0000.
* This address is used in total size transmission (see section 16.4.6, Total Size Transmission).

Table 16.2 States of SYS-DMAC Registers in each Operating Mode

Abbreviation	Power-On Reset	Module Standby
DMAISTA_L/DMAISTA_U	Initialized	Retained
DMASEC_L/DMASEC_U	Initialized	Retained
DMAOR_L/DMAOR_U	Initialized	Retained
DMACHCLR_L/DMACHCLR_U	Initialized	Retained
DMADPSEC_L/DMADPSEC_U	Initialized	Retained
DMASAR_0 to DMASAR_29	Initialized	Retained
DMADAR_0 to DMADAR_29	Initialized	Retained
DMATCR_0 to DMATCR_29	Initialized	Retained
DMATSR_0 to DMATSR_29	Initialized	Retained
DMACHCR_0 to DMACHCR_29	Initialized	Retained
DMATCRB_0 DMATCRB_29	Initialized	Retained
DMATSRB_0 to DMATSRB_29	Initialized	Retained
DMACHCRB_0 to DMACHCRB_29	Initialized	Retained
DMABUFCR_0 to DMABUFCR_29	Initialized	Retained
DMARS_0 to DMARS_29	Initialized	Retained
DMADPBASE_0 to DMADPBASE_29	Initialized	Retained
DMADPCR_0 DMADPCR_29	Initialized	Retained
DMAFIXSAR_0 to DMAFIXSAR_29	Initialized	Retained
DMAFIXDAR_0 to DMAFIXDAR_29	Initialized	Retained
DMAFIXDPBASE_0 to DMAFIXDPBASE_29	Initialized	Retained
DescriptorMEM	Undefined	Retained

16.3.1 DMA Interrupt Status Register for Lower-Numbered Channels (DMAISTA_L)

DMAISTA_L is a 32-bit readable register that indicates the states of the interrupt signals for each of the lower-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	I14	I13	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	I14	0	R	Interrupt State in Channel 14 0: An interrupt is not present. 1: An interrupt is present.
13	I13	0	R	Interrupt State in Channel 13 0: An interrupt is not present. 1: An interrupt is present.
12	I12	0	R	Interrupt State in Channel 12 0: An interrupt is not present. 1: An interrupt is present.
11	I11	0	R	Interrupt State in Channel 11 0: An interrupt is not present. 1: An interrupt is present.
10	I10	0	R	Interrupt State in Channel 10 0: An interrupt is not present. 1: An interrupt is present.
9	I9	0	R	Interrupt State in Channel 9 0: An interrupt is not present. 1: An interrupt is present.
8	I8	0	R	Interrupt State in Channel 8 0: An interrupt is not present. 1: An interrupt is present.
7	I7	0	R	Interrupt State in Channel 7 0: An interrupt is not present. 1: An interrupt is present.
6	I6	0	R	Interrupt State in Channel 6 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
5	I5	0	R	Interrupt State in Channel 5 0: An interrupt is not present. 1: An interrupt is present.
4	I4	0	R	Interrupt State in Channel 4 0: An interrupt is not present. 1: An interrupt is present.
3	I3	0	R	Interrupt State in Channel 3 0: An interrupt is not present. 1: An interrupt is present.
2	I2	0	R	Interrupt State in Channel 2 0: An interrupt is not present. 1: An interrupt is present.
1	I1	0	R	Interrupt State in Channel 1 0: An interrupt is not present. 1: An interrupt is present.
0	I0	0	R	Interrupt State in Channel 0 0: An interrupt is not present. 1: An interrupt is present.

16.3.2 DMA Interrupt Status Register for Higher-Numbered Channels (DMAISTA_U)

DMAISTA_U is a 32-bit readable register that indicates the states of the interrupt signals for each of the higher-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	I29	I28	I27	I26	I25	I24	I23	I22	I21	I20	I19	I18	I17	I16	I15
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	I29	0	R	Interrupt State in Channel 29 0: An interrupt is not present. 1: An interrupt is present.
13	I28	0	R	Interrupt State in Channel 28 0: An interrupt is not present. 1: An interrupt is present.
12	I27	0	R	Interrupt State in Channel 27 0: An interrupt is not present. 1: An interrupt is present.
11	I26	0	R	Interrupt State in Channel 26 0: An interrupt is not present. 1: An interrupt is present.
10	I25	0	R	Interrupt State in Channel 25 0: An interrupt is not present. 1: An interrupt is present.
9	I24	0	R	Interrupt State in Channel 24 0: An interrupt is not present. 1: An interrupt is present.
8	I23	0	R	Interrupt State in Channel 23 0: An interrupt is not present. 1: An interrupt is present.
7	I22	0	R	Interrupt State in Channel 22 0: An interrupt is not present. 1: An interrupt is present.
6	I21	0	R	Interrupt State in Channel 21 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
5	I20	0	R	Interrupt State in Channel 20 0: An interrupt is not present. 1: An interrupt is present.
4	I19	0	R	Interrupt State in Channel 19 0: An interrupt is not present. 1: An interrupt is present.
3	I18	0	R	Interrupt State in Channel 18 0: An interrupt is not present. 1: An interrupt is present.
2	I17	0	R	Interrupt State in Channel 17 0: An interrupt is not present. 1: An interrupt is present.
1	I16	0	R	Interrupt State in Channel 16 0: An interrupt is not present. 1: An interrupt is present.
0	I15	0	R	Interrupt State in Channel 15 0: An interrupt is not present. 1: An interrupt is present.

16.3.3 DMA Secure Control Register for Lower-Numbered Channels (DMASEC_L)

DMASEC_L is a 32-bit readable/writeable register that controls the security attribute of each of the lower-numbered channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	S14	S13	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	S14	0	R/W	Secure Mode Setting for Channel 14 0: Non-secure mode 1: Secure mode
13	S13	0	R/W	Secure Mode Setting for Channel 13 0: Non-secure mode 1: Secure mode
12	S12	0	R/W	Secure Mode Setting for Channel 12 0: Non-secure mode 1: Secure mode
11	S11	0	R/W	Secure Mode Setting for Channel 11 0: Non-secure mode 1: Secure mode
10	S10	0	R/W	Secure Mode Setting for Channel 10 0: Non-secure mode 1: Secure mode
9	S9	0	R/W	Secure Mode Setting for Channel 9 0: Non-secure mode 1: Secure mode
8	S8	0	R/W	Secure Mode Setting for Channel 8 0: Non-secure mode 1: Secure mode
7	S7	0	R/W	Secure Mode Setting for Channel 7 0: Non-secure mode 1: Secure mode

Bit	Bit Name	Initial Value	R/W	Descriptions
6	S6	0	R/W	Secure Mode Setting for Channel 6 0: Non-secure mode 1: Secure mode
5	S5	0	R/W	Secure Mode Setting for Channel 5 0: Non-secure mode 1: Secure mode
4	S4	0	R/W	Secure Mode Setting for Channel 4 0: Non-secure mode 1: Secure mode
3	S3	0	R/W	Secure Mode Setting for Channel 3 0: Non-secure mode 1: Secure mode
2	S2	0	R/W	Secure Mode Setting for Channel 2 0: Non-secure mode 1: Secure mode
1	S1	0	R/W	Secure Mode Setting for Channel 1 0: Non-secure mode 1: Secure mode
0	S0	0	R/W	Secure Mode Setting for Channel 0 0: Non-secure mode 1: Secure mode

16.3.4 DMA Secure Control Register Higher-Numbered Channels (DMASEC_U)

DMASEC_U is a 32-bit readable/writeable register that controls the security attribute of each of the higher-numbered channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	S29	S28	S27	S26	S25	S24	S23	S22	S21	S20	S19	S18	S17	S16	S15
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	S29	0	R/W	Secure Mode Setting for Channel 29 0: Non-secure mode 1: Secure mode
13	S28	0	R/W	Secure Mode Setting for Channel 28 0: Non-secure mode 1: Secure mode
12	S27	0	R/W	Secure Mode Setting for Channel 27 0: Non-secure mode 1: Secure mode
11	S26	0	R/W	Secure Mode Setting for Channel 26 0: Non-secure mode 1: Secure mode
10	S25	0	R/W	Secure Mode Setting for Channel 25 0: Non-secure mode 1: Secure mode
9	S24	0	R/W	Secure Mode Setting for Channel 24 0: Non-secure mode 1: Secure mode
8	S23	0	R/W	Secure Mode Setting for Channel 23 0: Non-secure mode 1: Secure mode
7	S22	0	R/W	Secure Mode Setting for Channel 22 0: Non-secure mode 1: Secure mode

Bit	Bit Name	Initial Value	R/W	Descriptions
6	S21	0	R/W	Secure Mode Setting for Channel 21 0: Non-secure mode 1: Secure mode
5	S20	0	R/W	Secure Mode Setting for Channel 20 0: Non-secure mode 1: Secure mode
4	S19	0	R/W	Secure Mode Setting for Channel 19 0: Non-secure mode 1: Secure mode
3	S18	0	R/W	Secure Mode Setting for Channel 18 0: Non-secure mode 1: Secure mode
2	S17	0	R/W	Secure Mode Setting for Channel 17 0: Non-secure mode 1: Secure mode
1	S16	0	R/W	Secure Mode Setting for Channel 16 0: Non-secure mode 1: Secure mode
0	S15	0	R/W	Secure Mode Setting for Channel 15 0: Non-secure mode 1: Secure mode

16.3.5 DMA Operation Register for Lower-Numbered Channels (DMAOR_L)

DMAOR_L is a 16-bit readable/writable register that enables DMA transfer on all lower-numbered channels and specifies the method used to determine the priority levels for all lower-numbered DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]		—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH0 > CH1 > ... > CH13 > CH14 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: A SYS-DMAC address error interrupt is not present. [Clearing condition] (*) Writing CAE = 0 after reading CAE = 1 1: A SYS-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR_L must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels. 0: Disables DMA transfers on all channels 1: Enables DMA transfers on all channels

16.3.6 DMA Operation Register for Higher-Numbered Channels (DMAOR_U)

DMAOR_U is a 16-bit readable/writable register that enables DMA transfer on all higher-numbered channels and specifies the method used to determine the priority levels for all higher-numbered DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]		—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH15 > CH16 > ... > CH28 > CH29 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: A SYS-DMAC address error interrupt is not present. [Clearing condition] (*) Writing CAE = 0 after reading CAE = 1 1: A SYS-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR_U must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels. 0: Disables DMA transfers on all channels 1: Enables DMA transfers on all channels

16.3.7 DMA Channel Clear Register for Lower-Numbered Channels (DMACHCLR_L)

DMACHCLR_L is a 32-bit writable register that initializes each of the lower-numbered channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.
This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CLR[14:0]														
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 0	CLR[14:0]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[0] 0: Ignored 1: All registers for channel 0 are cleared. CLR[1] 0: Ignored 1: All registers for channel 1 are cleared. CLR[2] 0: Ignored 1: All registers for channel 2 are cleared. ... CLR[14] 0: Ignored 1: All registers for channel 14 are cleared. When writing to this register, confirm that the DE bit is set to 0.

16.3.8 DMA Channel Clear Register for Higher-Numbered Channels (DMACHCLR_U)

DMACHCLR_U is a 32-bit writable register that initializes each of the higher-numbered channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.
This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CLR[29:15]														
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 0	CLR[29:15]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[15] 0: Ignored 1: All registers for channel 15 are cleared. CLR[16] 0: Ignored 1: All registers for channel 16 are cleared. ... CLR[29] 0: Ignored 1: All registers for channel 29 are cleared. When writing to this register, confirm that the DE bit is set to 0.

16.3.9 DPRAM Secure Control Register for Lower-Numbered Channels (DMADPSEC_L)

DMADPSEC_L is a 32-bit readable/writeable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SEC	—	—	—	—	—	—	SA[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SM[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 16.4.

16.3.10 DPRAM Secure Control Register for Higher-Numbered Channels (DMADPSEC_U)

DMADPSEC_U is a 32-bit readable/writeable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SEC	—	—	—	—	—	—	SA[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SM[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 16.4.

16.3.11 DMA Source Address Registers 0 to 29 (DMASAR_0 to DMASAR_29)

DMASAR is a 32-bit readable/writable register that specifies the source address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next source address.

When the address mode is increment, sources in memory only have byte boundaries. For details, refer to Table 16.3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.12 DMA Destination Address Registers 0 to 29 (DMADAR_0 to DMADAR_29)

DMADAR is 32-bit readable/writable register that specify the destination address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next destination address.

When the address mode is increment, destinations in memory only have byte boundaries. For details, refer to Table 16.3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 16.3 SAR/DAR Address Restriction

Resource Selection	Address Mode	Restriction
Auto request	Increment	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/DAR, Reception/SAR	All	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/SAR, Reception/DAR	Increment	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size

16.3.13 DMA Transfer Count Registers 0 to 29 (DMATCR_0 to DMATCR_29)

DMATCR is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF (the maximum). During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in reading.

The eight higher-order bits of DMATCR are always read as 0, and the write value should always be 0.

The value of this register should be set before DMA transfer starting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCR[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.14 DMA Transfer Count Registers B_0 to 29 (DMATCRB_0 to DMATCRB_29)

DMATCRB is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001, 16,777,215 when the setting is H'00FFFFFF (the maximum). During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in writing.

The eight higher-order bits of DMATCRB are always read as 0, and the write value should always be 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCR[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.15 DMA Transfer Size Registers 0 to 29 (DMATSR_0 to DMATSR_29)

DMATSR is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967,295 bytes when the setting is H'FFFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the read transfer size.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.16 DMA Transfer Size Registers B_0 to 29 (DMATSRB_0 to DMATSRB_29)

DMATSRB is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967,295 bytes when the setting is H'FFFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The SYS-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the write transfer size.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.17 DMA Channel Control Registers 0 to 29 (DMACHCR_0 to DMACHCR_29)

DMACHCR is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAE	CAIE	DPM[1:0]		RPT[2:0]			—	—	DPB	TS[3:2]		DSE	DSIE	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/(W)*	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]				—	—	—	TS[1:0]		IE	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	CAE	0	R/(W)*	Channel Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the CAE bit, write 0 to the CAE bit after reading 1 from it or clear the AE bit in DMAOR. Clearing the CAE bit clears the channel address error bits for all channels. 0: A SYS-DMAC address error interrupt is not present. [Clearing condition] (*)Writing CAE = 0 after reading CAE = 1 1: A SYS-DMAC address error interrupt being generated during DMA transfer.
30	CAIE	0	R/W	Channel Address Error Interrupt Enable Enables or disables the generation of interrupt requests for the CPU when address errors occur. When the CAIE bit is set to 1, if the CAE bit is also set, an interrupt (DEI 0 to 29) from the corresponding channel will be generated for the CPU in response to address errors. Note: An address error interrupt (DADERR) is also asserted simultaneously. See section 11, Interrupt Controller for AP-System Core (INTC-SYS) for more details. 0: Interrupt requests are disabled. 1: Interrupt requests are enabled.
29, 28	DPM[1:0]	00	R/W	Operating Mode of Descriptor Memory Enable or disable the descriptor memory and specify its operating mode. 00: Disabled (normal use) 01: Enabled (normal mode) 10: Enabled (repeat mode) 11: Enabled (read-out interrupt mode, infinite repeat mode)

Bit	Bit Name	Initial Value	R/W	Descriptions
27 to 25	RPT[2:0]	000	R/W	Descriptor Setting Update Specify the parameters to be updated from the descriptor memory. RPT[2]: Enables or disables updating of the source address register RPT[1]: Enables or disables updating of the destination address register RPT[0]: Enables or disables updating of the transfer count register 0: Disabled 1: Enabled
24, 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	DPB	0	R/W	Descriptor Start Specifies configuration to be loaded when transfer under control of the descriptor memory begins. This bit is cleared after the descriptor memory is read. 0: Processing starts with the values in DMASAR, DMADAR, and DMATCR. 1: Processing starts after the first set of descriptors is read out.
21, 20	TS[3:2]	00	R/W	DMA Transfer Size In combination with TS[1:0], these bits specify the DMA transfer size. When the transfer source or transfer destination is a register of an on-chip peripheral module for which a transfer size is specified, be sure to select the specified transfer size. For the transfer source or destination address specified by DMASAR or DMADAR, an appropriate boundary address should be set according to the transfer data size. Note. Transfer size must be specified to satisfy both source and destination access sizes. For example, the MSIOF must be accessed by 4-byte unit (TS [3:0] = B'0010) only except for SITSCR. TS[3:2] + TS[1:0] (“+” here indicates concatenation, not addition) 0000: Transfer is in byte units. 0001: Transfer is in word (2-byte) units. 0010: Transfer is in longword (4-byte) units. 0011: Transfer is in 16-byte units. 0100: Transfer is in 32-byte units. 0101: Transfer is in 64-byte units. 0111: Transfer is in 8-byte units. Other than above: Setting prohibited
19	DSE	0	R/(W)*	Descriptor Stage End (*)When the DSIE bit is set to 1 and the descriptor memory is enabled, the DSE bit is set to 1 on completion of the DMA transfer. This bit is not set when the DPM bit is set to 0 (descriptors are disabled). To clear the DSE bit, start by reading it as 1, and then write 0 to the bit. 0: DMA transfer is still running or has been aborted. 1: Transfer under the control of one stage of the descriptor memory has been completed.

Bit	Bit Name	Initial Value	R/W	Descriptions
18	DSIE	0	R/W	Descriptor Stage End Interrupt Enable Specifies whether an interrupt request is generated for the CPU on completion of transfer under the control of one stage of the descriptor memory. When this bit is set to 1, an interrupt (DEI) is generated for the CPU whenever the DSE is set to 1. 0: Interrupt requests are disabled. 1: Interrupt requests are enabled.
17, 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15, 14	DM[1:0]	00	R/W	Destination Address Mode Specify whether the DMA destination address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment. 00: Destination address is fixed. 01: Destination addresses are incremented. + 1 when transfer is in byte units. + 2 when transfer is in word units. + 4 when transfer is in longword units. + 8 when transfer is in 8-byte units. + 16 when transfer is in 16-byte units. + 32 when transfer is in 32-byte units. + 64 when transfer is in 64-byte units. 10: Destination addresses are decremented. – 1 when transfer is in byte units. – 2 when transfer is in word units. – 4 when transfer is in longword units. Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units. 11: Setting Prohibited
13, 12	SM[1:0]	00	R/W	Source Address Mode Specify whether the DMA source address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment. 00: Source address is fixed. 01: Source addresses are incremented. + 1 when transfer is in byte units. + 2 when transfer is in word units. + 4 when transfer is in longword units. + 8 when transfer is in 8-byte units. + 16 when transfer is in 16-byte units. + 32 when transfer is in 32-byte units. + 64 when transfer is in 64-byte units. 10: Source addresses are decremented. – 1 when transfer is in byte units. – 2 when transfer is in word units. – 4 when transfer is in longword units. Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units. 11: Setting Prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	RS[3:0]	0000	R/W	Resource Selection Specify the source of transfer requests. Only change the transfer request source while the DMA enable bit (DE) is set to 0. 0100: Auto request 1000: Source is selected by the DMA extended resource selector. Other than above: Settings prohibited
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4, 3	TS[1:0]	00	R/W	DMA Transfer Size See the description of TS[3:2] (bits 21 and 20).
2	IE	0	R/W	Interrupt Enable Specifies whether or not an interrupt request is generated for the CPU on completion of DMA transfer. When this bit is set to 1, an interrupt request (DEI) for the CPU is generated whenever the TE bit is set to 1. 0: Interrupt request is disabled. 1: Interrupt request is enabled.
1	TE	0	R/(W)*	Transfer End Flag When the descriptor memory is not in use, the TE bit is set to 1 when DMATCR and DMATSR become 0 on completion of the DMA transfer. When the descriptor memory is in use, the TE bit is set to 1 on completion of all transfers set up in the descriptor memory. The TE bit is not set to 1 in the following cases. • DMA transfer ends due to a DMA address error before DMATCR and DMATSR become 0. • DMA transfer is aborted by clearing the DE and DME bits in DMAOR. To clear the TE bit, start by reading it as 1, and then write 0 to it. When the TE bit is set to 1, transfer is not possible even if the DE bit is set to 1. 0: DMA transfer is in progress or was aborted [Clearing condition] (*)Writing of 0 after reading of 1 1: DMA transfer ended on the specified count (TCR = 0 and TSR = 0)
0	DE	0	R/W	DMA Enable Enables or disables DMA transfer. In the auto request mode, a DMA transfer is started by setting the DE and DME bits in DMAOR to 1. At this time, the setting of both the AE and TE bits in DMAOR must be 0. In a peripheral module request, a DMA transfer starts if the transfer request is generated by the selected device or on-chip peripheral module after setting the DE and DME bits to 1. In this case too, the settings of both the TE and AE bits must be 0. Clearing the DE bit to 0 aborts all DMA transfer. Note: Ensure that the setting of the DE bit is actually 0 after clearing it. 0: DMA transfer is disabled. 1: DMA transfer is enabled.

Note: * Writing 0 is possible to clear the flag.

16.3.18 DMA Channel Control Register B_0 to 29 (DMACHCRB_0 to DMACHCRB_29)

DMACHCRB is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCNT[7:0]								DPTR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRST	—	—	—	—	—	—	DTS	SLM[3:0]				PRI[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DCNT[7:0]	H'00	R/W	Number of Stages of Descriptor Memory Specify the number of stages of the descriptor memory as DCNT + 1. When the descriptor memory is enabled, a transfer end (TE) interrupt is only generated for the CPU on completion of transfer under control of the specified number of stages.
23 to 16	DPTR[7:0]	H'00	R	Descriptor Pointer This bit indicates the pointer to the next descriptor to be read. It is cleared to 0 when the last descriptor of the number of stages specified by DCNT[7:0] is read. It is also cleared to 0 when 1 is written to DRST.
15	DRST	0	W	Descriptor Reset Resets the descriptor pointer. Before the descriptor memory is used, the pointer must be reset by writing 1 to this bit. This bit is always read as 0.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DTS	0	R/W	Total Size Transmission under Descriptor Control This bit is only effective when total size transmission is selected. 0: The TCR fields of the descriptors are used as transfer count settings. 1: The TCR fields of the descriptors are used as total size settings.
7 to 4	SLM[3:0]	0000	R/W	DMA Transfer Low-Speed Mode Specify the number of cycles of the clock (ZS) for the DMA transfer. One round of DMA transfer is executed in the number of cycles of the clock specified by this bit. 0000: Normal mode 1000: On round in 256 cycles of the clock. 1001: On round in 512 cycles of the clock. 1010: On round in 1024 cycles of the clock. : 1111: On round in 32768 cycles of the clock. Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
3 to 0	PRI[3:0]	0000	R/W	Channel Request Priority Setting These bits set the priority of requests for transfer on the given channel. 1111: Highest priority : 0111 to 0000: Lowest priority

16.3.19 DMA Buffer Control Registers 0 to 29 (DMABUFCR_0 to DMABUFCR_29)

DMABUFCR is a 32-bit readable/writable register that controls the upper limit on buffer size in and burst unit for the SDRAM.

Use this register when the upper limit on buffering requires control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	MBU[8:0]								
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ULB[9:0]									
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	MBU[8:0]	H'080	R/W	Maximum Burst Unit for SDRAM This register is only effective for SDRAM access, and everything other than that is under control of the transfer size (unit). Settings bigger than UBL are prohibited. Power-of-two settings are recommended. Maximum value is 256 (bytes).
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	ULB[9:0]	H'100	R/W	Upper Limit on Buffer Size This register controls the upper limit value for buffering. Power-of-two settings are recommended. Maximum value is 512 (bytes).

16.3.20 DMA Extended Resource Selectors 0 to 29 (DMARS_0 to DMARS_29)

DMARS is a 16-bit readable/writable register that specifies the on-chip peripheral module to be the source of the DMA transfer request for the given channel. DMARS_0 specifies the source for channel 0, DMARS_1 specifies the source for channel 1 and so on.

When bits MID and RID are set to a value other than the values listed in Table 16.4, the operation of this LSI is not guaranteed. Transfer requests from the source selected in DMARS are only valid when the resource selection bits (RS[3:0]) in DMACHCR have been set to B'1000. Otherwise, even if DMARS has been set, requests from the corresponding transfer request source are not accepted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MID[5:0]						RID[1:0]	
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 8	—	—	R	Reserved These bits are always read as an undefined value. The write value should always be 0.
7 to 2	MID[5:0]	000000	R/W	DMA Request Source Adoption ID5 to ID0 (MID) See Table 16.4.
1, 0	RID[1:0]	00	R/W	DMA Request Source Adoption ID1 and ID0 (RID) See Table 16.4.

16.3.21 DMA Descriptor Base Address Registers 0 to 29 (DMADPBASE_0 to DMADPBASE_29)

DMADPBASE specifies the base address of the descriptor memory. The address range of the descriptor memory is specified by setting this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPBASE[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPBASE[15:4]												—	—	—	SEL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	DPBASE[31:4]	All 0	R/W	Base Address of Descriptor Memory Place each stage of the descriptor memory on a 16-byte boundary. Setting example: When Built-in memory is used, [SYS-DMAC Lower]: H'E670 A00 to H'E670 A7F [SYS-DMAC Higher]: H'E672 A00 to H'E672 A7F When External memory is used, Other memory area on a 16-byte boundary
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SEL	0	R/W	Descriptor Memory Selection Selects the memory to be used as descriptor memory. 0: Setting Prohibited 1: Built-in memory or External memory is used.

16.3.22 DMA Descriptor Control Registers 0 to 29 (DMADPCR_0 to DMADPCR_29)

DMADPCR is a 32-bit readable/writable register that controls the timing with which interrupts are output in read-out interrupt mode (descriptor mode 3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIPT[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DIPT[7:0]	All 0	R/W	Descriptor Read-out Interrupt Pointer The number of stages for which descriptor read-out interrupts are generated in descriptor mode 3. DIPT + 1 specifies the number of descriptor stages.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

16.3.23 DMA Fixed Source Address Registers 0 to 29 (DMAFIXSAR_0 to DMAFIXSAR_29)

DMAFIXSAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit source address for a DMA transfer.

This register is not incremented by carrying when DMASAR overflows.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SAR[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.24 DMA Fixed Destination Address Registers 0 to 29 (DMAFIXDAR_0 to DMAFIXDAR_29)

DMAFIXDAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit destination address for a DMA transfer.

This register is not incremented by carrying when DMADAR overflows.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DAR[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.25 DMA Fixed Descriptor Base Address Registers 0 to 29 (DMAFIXDPBASE_0 to DMAFIXDPBASE_29)

DMAFIXDPBASE is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit descriptor base address for a DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DPBASE[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

16.3.26 Descriptor Memory (DescriptorMEM)

See section 16.4.4, Descriptor Memory.

16.4 Operation

When there is a DMA transfer request, the DMAC starts the transfer according to the predetermined channel priority; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto request and on-chip peripheral module request. The bus mode can be selected from normal speed mode and slow speed mode.

16.4.1 DMA Transfer Requests

Most commonly, DMA transfer requests are generated by either the source or destination for transfer, but they can also be generated by on-chip peripheral modules that are neither the source nor the destination. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. The request mode is selected for each channel by DMARS.

(1) Auto-Request Mode

When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, auto-request mode allows the SYS-DMAC to automatically generate a transfer request signal internally. When the DE bit in DMACHCR and the DME bit in DMAOR are set to 1 for the target channel, the transfer begins so long as the CAE bit in DMACHCR is 0.

(2) On-Chip Peripheral Module Request Mode

In this mode, a transfer is performed at the transfer request signal of an on-chip peripheral module. The source (on-chip peripheral module) of the DMA transfer request is specified by DMARS.

When this mode is selected, if the DMA transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0), a transfer is performed upon the input of a transfer request signal.

When a transmit data empty transfer request of the SCIF is set as the transfer request, the transfer destination must be the SCIF's transmit data register. Likewise, when receive data full transfer request of the SCIF is set as the transfer request, the transfer source must be the SCIF's receive data register. These conditions also apply to the other on-chip peripheral modules.

The number of the receive FIFO triggers can be set as a transfer request depending on an on-chip peripheral module. Data needs to be read after the DMA transfer is ended, because data may be left in the receive FIFO when the receive FIFO trigger condition is not satisfied.

Table 16.4 Selecting On-Chip Peripheral Module Request Modes

DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination
H'39	HSCIF0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'3A	HSCIF0 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'4D	HSCIF1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'4E	HSCIF1 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'3B	HSCIF2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'3C	HSCIF2 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'29	SCIF0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'2A	SCIF0 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'2D	SCIF1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'2E	SCIF1 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'2B	SCIF2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'2C	SCIF2 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'2F	SCIF3 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'30	SCIF3 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'FB	SCIF4 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'FC	SCIF4 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'FD	SCIF5 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	Data register
H'FE	SCIF5 receiver	RXI (Receive FIFO data full)	Data register	Arbitrary
H'51	MSIOF0 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR
H'52	MSIOF0 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary
H'55	MSIOF1 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR
H'56	MSIOF1 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary
H'41	MSIOF2 transmitter	TXI (Transmit FIFO data empty)	Arbitrary	SITDR
H'42	MSIOF2 receiver	RXI (Receive FIFO data full)	SIRDR	Arbitrary
H'17	QSPI0 transmitter	Transmit	Arbitrary	Data register
H'18	QSPI0 receiver	Receive	Data register	Arbitrary
H'D1	QSPI1 transmitter	Transmit	Arbitrary	Data register
H'D2	QSPI1 receiver	Receive	Data register	Arbitrary
H'CD	SDHI0	Transmit empty transfer request	Arbitrary	Data register
H'CE	SDHI0	Receive full transfer request	Data register	Arbitrary
H'D3	SDHI2	Transmit empty transfer request	Arbitrary	Data register
H'D4	SDHI2	Receive full transfer request	Data register	Arbitrary

Table 16.5 Data Length of DMA Transfer for Each of the On-Chip Peripheral Modules

Module	1 Byte	2 Bytes	4 Bytes	8 Bytes	16 Bytes	32 Bytes	64 Bytes
HSCIF0/1/2	√						
SCIF0/1/2/3/4/5	√						
MSIOF0/1/2			√				
QSPI0/1	√	√	√				
SDHI0/2		√	√		√	√	

Note: Module request mode will be used for data transfer.

16.4.2 Channel Priority

When the SYS-DMAC receives simultaneous transfer requests on two or more channels, it transfers data according to a predetermined priority. Two modes (fixed mode and round-robin mode) are selected by the PR[1:0] bits in DMAOR.

(1) Fixed Mode

In this mode, the priority levels among the channels remain fixed.

CH0 > CH1 > ... > CH13 > CH14, CH15 > CH16 > ... > CH28 > CH29

(2) Round-Robin Mode

In round-robin mode, each time data of one transfer unit (byte, word, long-word, 8-byte, or 16-byte units) is transferred on one channel, the priority is rotated. The channel on which the transfer was just finished rotates to the bottom of the priority. The priority of round-robin mode is CH0 > CH1 > ... > CH13 > CH14 and CH15 > CH16 > ... > CH28 > CH29 immediately after reset.

16.4.3 Slow Speed Mode

In the slow-speed mode, a single round of DMA transfer is performed every time the number of clock cycles specified by the SLM bits in DMACHCRB elapse. This mode can be selected per DMA channel. Transfer on other channels can proceed after each round of transfer for a channel in the slow-speed mode is completed.

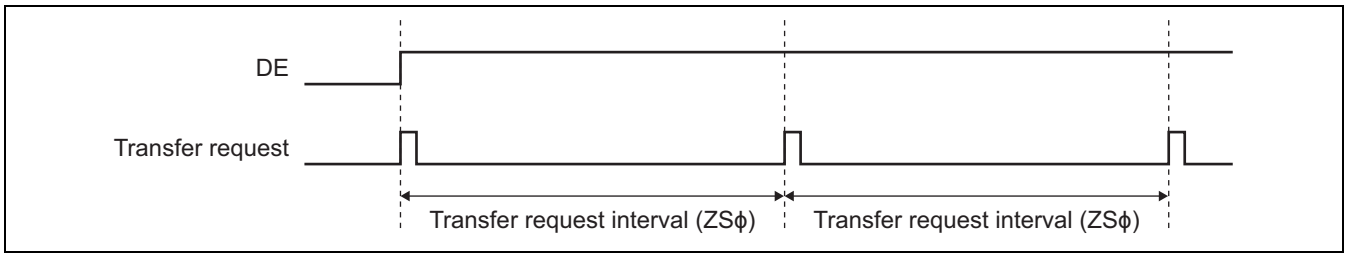


Figure 16.2 Slow Speed Mode

16.4.4 Descriptor Memory

The descriptor memory function is selected by setting the DPM[1:0] bits in DMACHCR to B'01, B'10, or B'11. When DMATCR is set to 0 and the DMA transfer is completed, the next set of settings is read, and if only a single channel is enabled, the contents defined by up to 128 stages of descriptor memory can be consecutively transferred when the built-in descriptor memory is used. External memory can also be used as the descriptor memory. In that case, the contents defined by up to 256 stages of descriptor memory can be transferred.

The following initial settings are required to use the descriptor memory.

- Set the base address of the descriptor memory for the DMA transfer in DMADPBASE.
- Set the DRST bit in DMACHCRB to reset the descriptor memory.
- Set the number of stages of the descriptor memory in the DCNT bits of DMACHCRB.

The descriptor memory is shared between all channels. Ensure that the areas of descriptor memory for use by each of the channels do not overlap. It is necessary to arrange each stage of the descriptor memory on a 16-byte boundary.

There are two methods to activate the descriptor memory as follows.

- Specify the first DMA transfer settings in DMASAR, DMADAR, and DMATCR, and specify the subsequent settings in the descriptor memory. Then, set the DPB bit in DMACHCR to 0 to activate the descriptor memory. In this case, after completion of the transfer specified in DMASAR, DMADAR, and DMATCR, transfer continues after new settings are read from the descriptor memory. Note, however, that when the operating mode of the descriptor memory is set to the repeat mode, the values specified in DMASAR, DMADAR, and DMATCR are not read, and the transfer starts and is repeated from the head of the descriptor memory.
- Write the DMA transfer settings to the descriptor memory, and write 1 to the DPB bit in DMACHCR to activate the descriptor memory. In this case, the DMA transfer starts from the first settings in the descriptor memory.

There are three operating modes of the descriptor memory, which can be selected by setting the DPM bits in DMACHCR.

For details on these operating modes, see the descriptions of each operating mode in this section.

(1) Configuration of Descriptor Memory

Figure 16.3 shows the configuration of the built-in descriptor memory.

The capacity of the built-in descriptor memory is 16 bytes per stage × 128 stages.

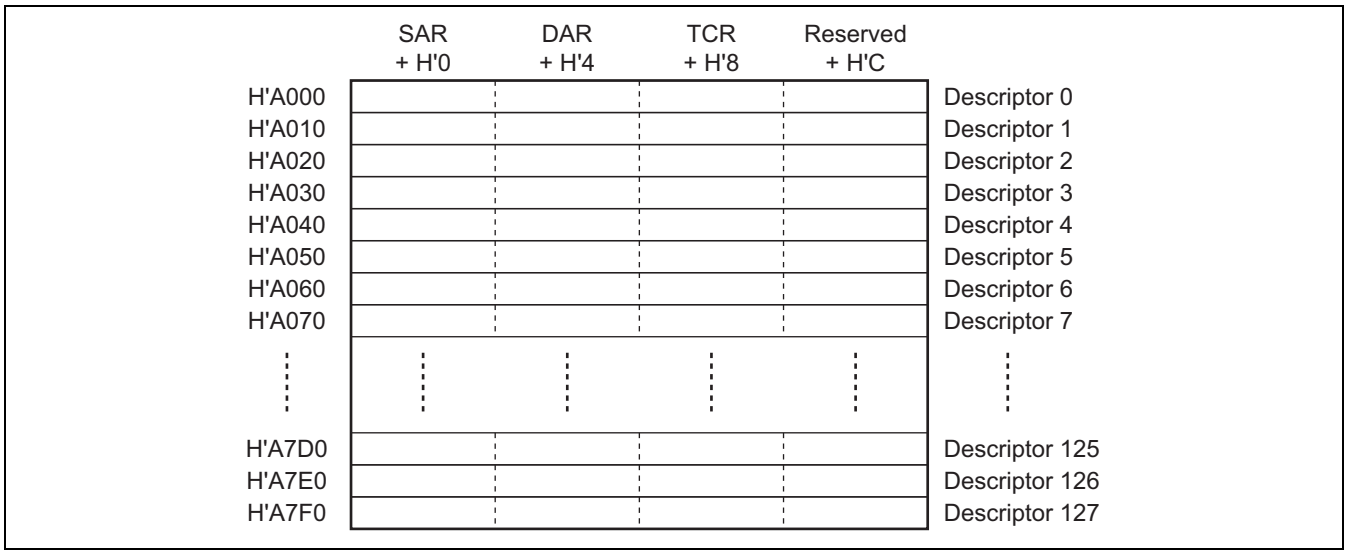


Figure 16.3 Configuration of Built-in Descriptor Memory

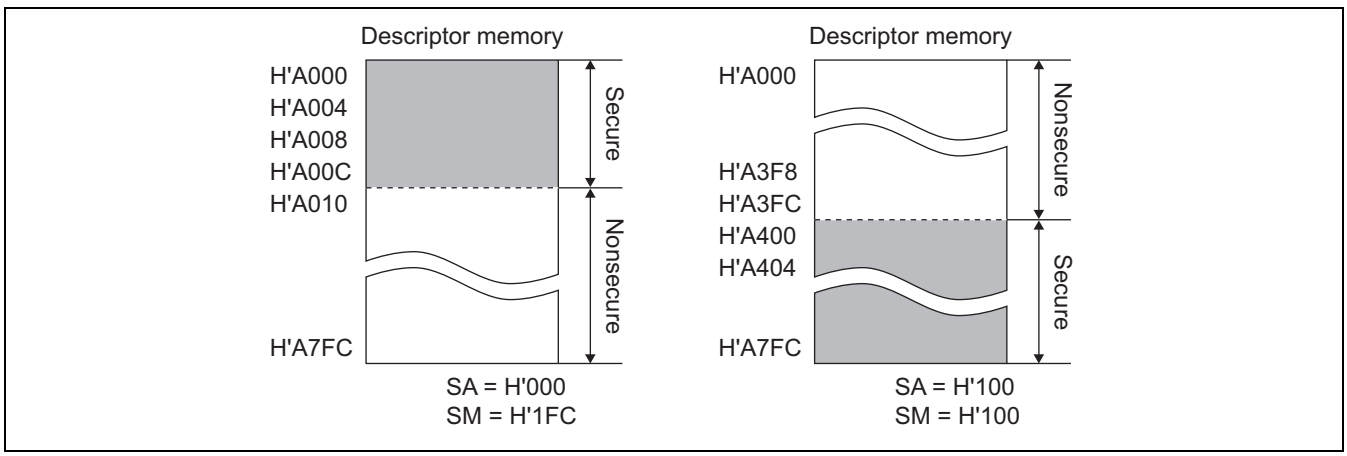


Figure 16.4 Example of DMADPSEC Setting

(2) Flow of Updating from Descriptor Memory

The RPT bits in DMACHCR can be used to specify which registers are to be updated from the descriptor memory.

The DPTR bits in DMACHCRB are incremented when updating from the descriptor memory is completed. If the DPTR value matches the DCNT value, the DPTR value is reset to 0.

This flow is automatically processed by hardware.

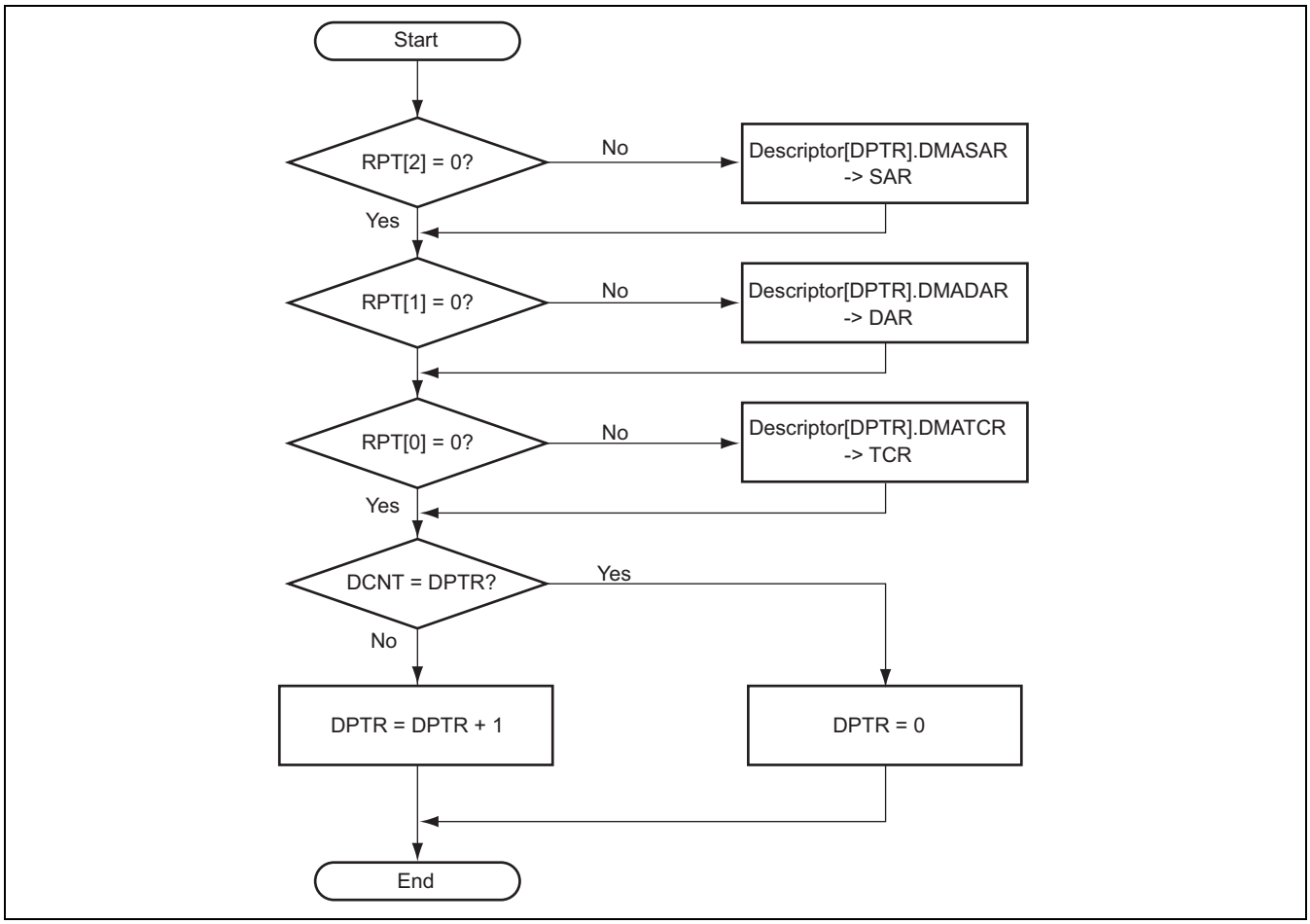


Figure 16.5 Flow of Updating from Descriptor Memory

(3) Operating Mode 1 of Descriptor Memory

Set the DPM bits in DMACHCR to B'01 to select operating mode 1 (normal mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, the DMA transfer is complete when the TE bit in DMACHCR is set to 1 after transfer under control of the number of stages of the descriptor memory specified in the DCNT bits in DMACHCRB.

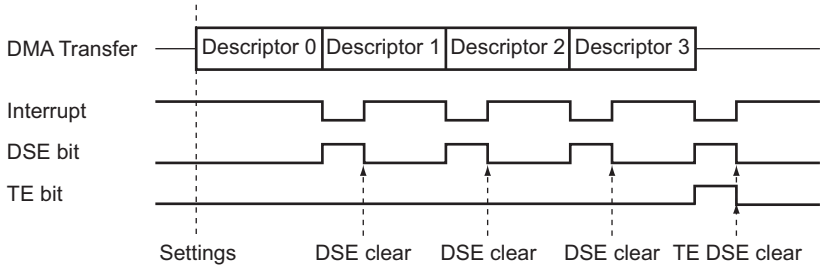
When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

Figure 16.6 is an example of transfer when operating mode 1 is selected and the TE and DSE bits are set to 1.

Figure 16.7 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 1 is selected and the TE and DSE bits are set to 1.

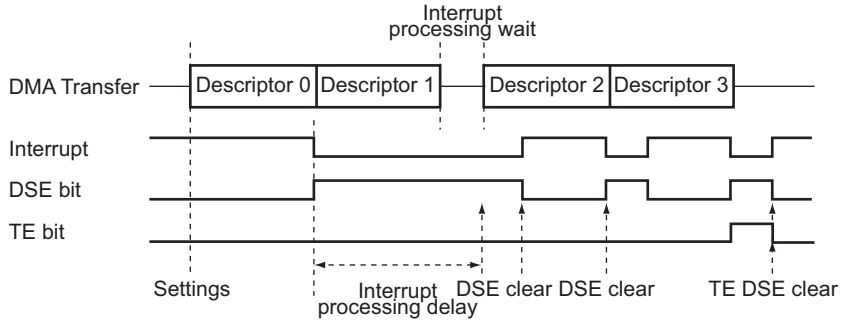
Figure 16.8 is an example of transfer when operating mode 1 is selected and the TE bit is set to 1.

In each example, there are four descriptor stages.



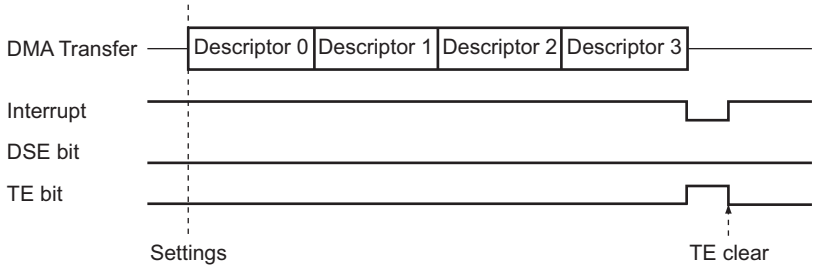
Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 16.6 Operating Mode 1 (Example 1)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 16.7 Operating Mode 1 (Example 2)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'1).

Figure 16.8 Operating Mode 1 (Example 3)

(4) Operating Mode 2 of Descriptor Memory

Set the DPM bits in DMACHCR to B'10 to select operating mode 2 (repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

When the DSIE bit in DMACHCR is set to 0, after transfer under control of all stages of the descriptor memory is complete, the TE bit in DMACHCR is set to 1 and a TE interrupt is generated. If a TE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the TE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

To end operation in mode 2, change the mode to mode 1 by using the TE interrupt processing. When the mode is changed to mode 1, the DMA transfer is completed when the next TE interrupt is generated.

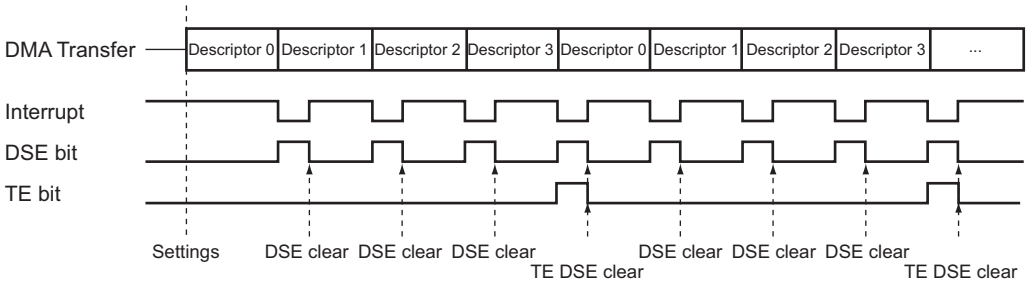
Figure 16.9 is an example of transfer when operating mode 2 is selected and the TE and DSE bits are set to 1.

Figure 16.10 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE and DSE bits are set to 1.

Figure 16.11 is an example of transfer when operating mode 2 is selected and the TE bit is set to 1.

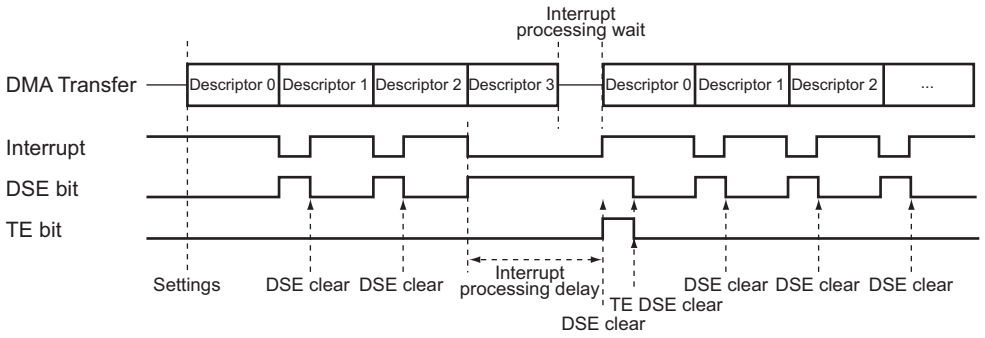
Figure 16.12 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE is set to 1.

In each example, there are four descriptor stages.



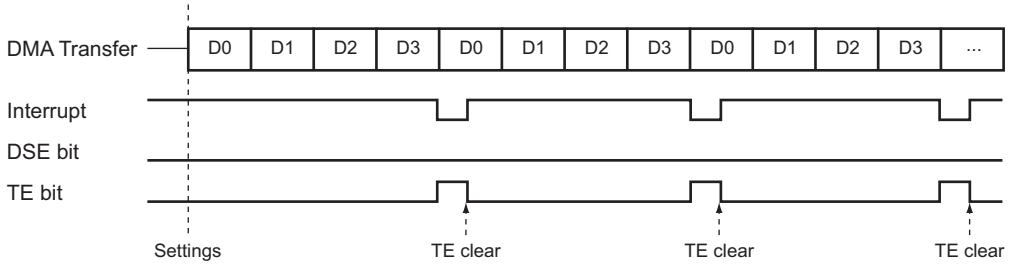
Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 16.9 Operating Mode 2 (Example 1)



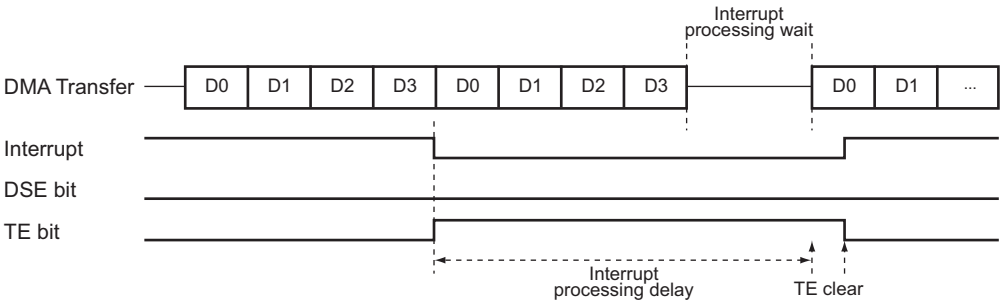
Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 16.10 Operating Mode 2 (Example 2)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'1).

Figure 16.11 Operating Mode 2 (Example 3)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'1).

Figure 16.12 Operating Mode 2 (Example 4)

(5) Operating Mode 3 of Descriptor Memory

Set the DPM bits in DMACHCR to B'11 to select operating mode 3 (infinite repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

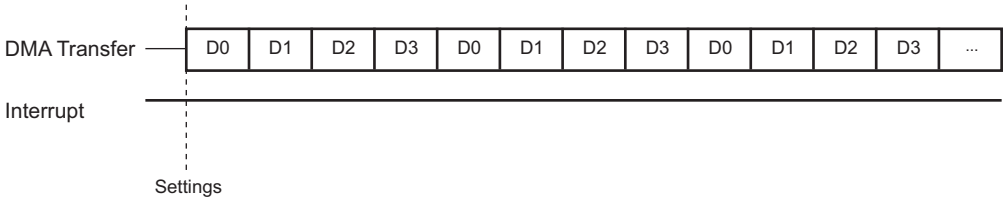
In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. Even if a first DSE interrupt has not been processed when a further DSE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of DSE interrupts that have been generated, the TE bit can be cleared by writing to it once. Similarly, even if a first TE interrupt has not been processed when a further TE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of TE interrupts that have been generated, the TE bit can be cleared by writing to it once.

Figure 16.13 is an example of transfer when infinite repeat mode is selected.

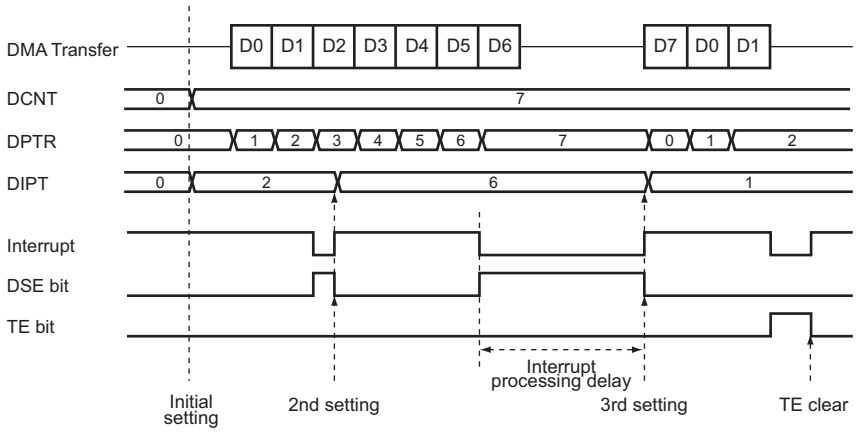
Figure 16.14 is an example of transfer when read-out interrupt mode is selected.

In each example, there are four descriptor stages.



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'11, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'0).

Figure 16.13 Operating Mode 3 (Infinite Repeat Mode)



Initial setting:
1. Set the DMACHCRB register (DCNT = 7).
2. The descriptor has three setting (DMASAR, DMADAR, DMATCR) stages.
3. Set the DMADPCR register (DIPT = 2).
4. Set the DMACHCR register (DPM = B'11, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'0).

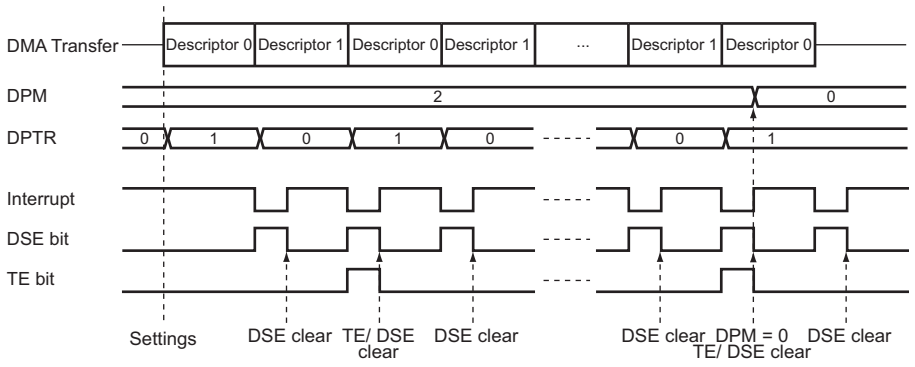
2nd setting:
1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMADPCR register (DIPT = 6).
   (3 stages + 4 stages -1) mod 8 = 6
3. Clear DSE.

3rd setting: (Transfer end)
1. The descriptor has three setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMADPCR register (DIPT =1).
   (3 stages + 4 stages + 3 stages -1) mod 8 = 1
3. Clear the DSE bit and set the DMACHCR register (DPM = B'11, DB = B'0, DSIE = B'0, IE = B'1).

Figure 16.14 Operating Mode 3 (Read-Out Interrupt Mode)

(6) Using the Descriptor Memory for Double Buffering

To use the descriptor memory for double buffering, set the number of stages of descriptor memory to 2, set the buffer configuration to the descriptor memory, and activate the memory in operating mode 2. The DSE interrupt is used in double buffering. To end the use of double buffering, disable the descriptor operating mode, which stops the transfer on completion of the transfer currently in progress.



Settings: 1. The descriptor has two setting (buffer A, buffer B) stages.
2. Set the DMACHCRB register (DCNT = 1).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'0).

Figure 16.15 Using the Descriptor Memory for Double Buffering

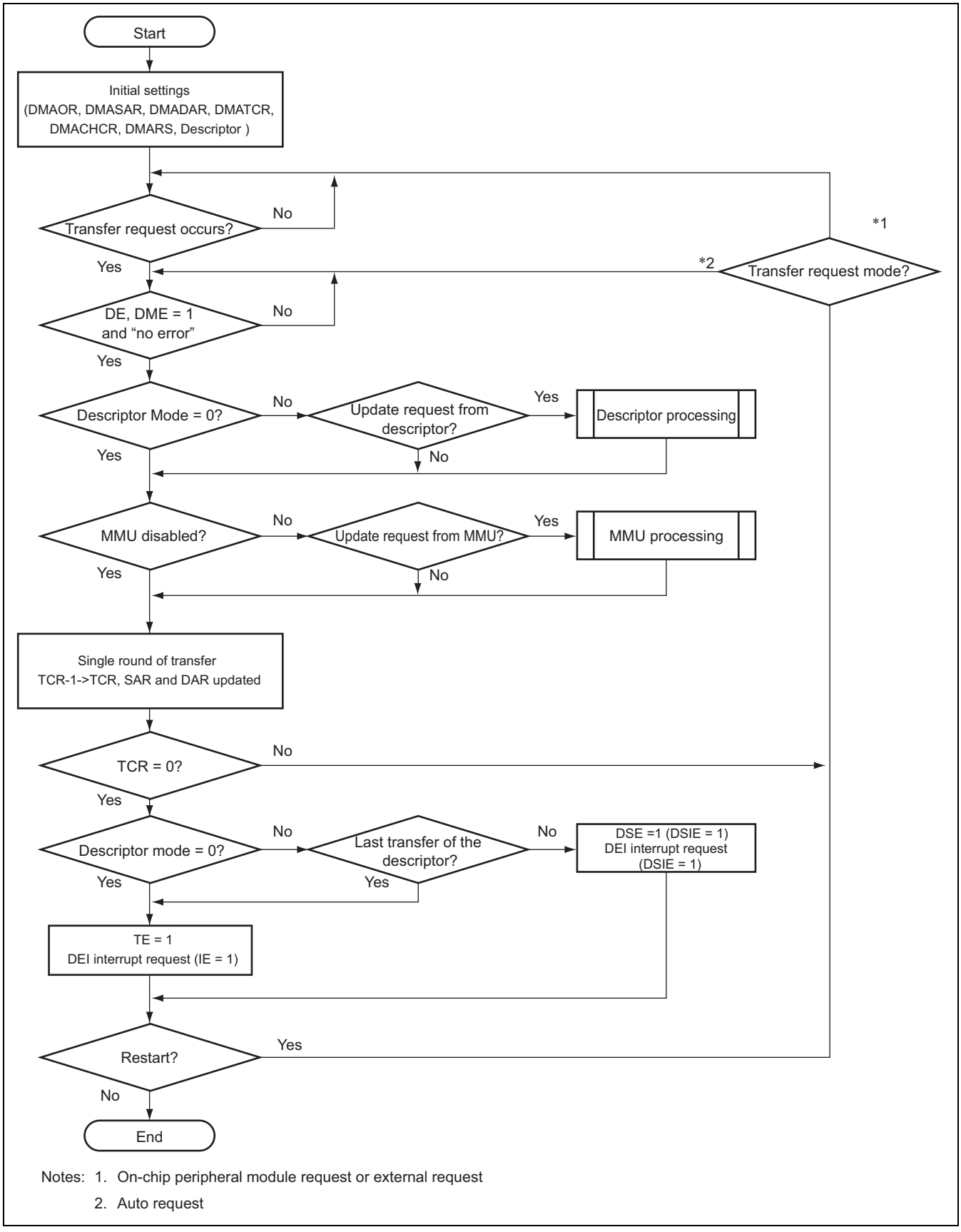
16.4.5 Transmission Flow

Set the transfer conditions as required in the following registers:

DMA source address register (DMASAR), DMA destination address register (DMADAR), DMA transfer count register (DMATCR), DMA Channel control register (DMACHCR), DMA operation register (DMAOR) and DMA extended resource selector (DMARS)

The DMAC then transmits data in the following order.

- A transfer request is generated and the controller checks whether the transfer is allowed (DE = 1, DME = 1, TE = 0, DSE = 0, CAE = 0). When a channel is in the auto request mode, the transfer starts automatically.
- The controller checks whether updating from the descriptor memory is required.
  Updating from the descriptor memory proceeds when the DPB bit in DMACHCR is set to 1 or the descriptor memory is enabled, if DMATCR is set to 0.
  For updating by using the descriptor memory, see section 16.4.4, Descriptor Memory.
- Check whether address translation by the IPMMU is required.
  Address translation by the IPMMU proceeds if the address exceeds the effective size for address translation when the DE bit in DMACHCR is enabled and updating of transfer settings from the descriptor memory is executed.
- Each time a transfer request is generated, the amount of data for a single round of transfer (specified by the TS[3:0] bits) is transmitted. The value in DMATCR is decremented by 1 every time the DMA transfer is completed.
- When the specified number of rounds of transfer are completed (the value in DMATCR is set to 0), the transfer ends normally. A TE interrupt is generated for the CPU upon the end of the transfer if the IE bit in DMACHCR is set to 1. If the descriptor memory is enabled, the processing differs with the mode of the descriptor memory. For more details, see section 16.4.4, Descriptor Memory.
- Transfer is aborted when the DMAC encounters an address error. Transfer is also aborted when the DE bit in DMACHCR or the DME bit in DMAOR is set to 0.



Notes: 1. On-chip peripheral module request or external request
2. Auto request

Figure 16.16 Transmission Flow

16.4.6 Total Size Transmission

The amount of data for total size transmission can be set in DMATSR (in bytes), and this setting is effective regardless of the size specified in the TS bits in DMACHCR. Thereby, the desired size can be transmitted in a single round of DMA transfer.

To use this function, make the settings for total size transmission in DMASAR, DMADAR, DMATSR, DMATSRB and DMACHCR.

Total size is set in the TCR (TSR) field of descriptors and 1 is set in DMACHCRB.DTS when total size transmission and descriptors are in use.

16.5 Usage Notes

Pay attention to the following notes when using the SYS-DMAC.

16.5.1 DMA Transfer for Peripheral Modules

When executing DMA transfer for an on-chip peripheral module, set addresses on the appropriate boundary (in terms of the amount of data for each round of transfer) for the transfer source and destination addresses. Otherwise, an address error may occur.

16.5.2 Module Stop

While the SYS-DMAC is operating, the module stop register (MSTPCR2) should not be set to stop the SYS-DMAC. If the SYS-DMAC is stopped in this way, results of the transfer that was in progress cannot be guaranteed.

16.5.3 Address Error

When a DMA address error is generated, reset the registers of the channel on which the error has occurred and then start transfer anew.

16.5.4 Aborting DMA Transfer

To abort a DMA transfer, disable the interrupt signal and set the DE bit in the DMA channel control register (DMACHCR) to 0 to disable the DMA transfer. If the TE and DSE bits are set when DMA transfer is aborted, these bits should be initialized. There is a possibility that TE and DSE will not be set with synchronized timing after transmission, so it's necessary to recognize the following three possibilities and take measures accordingly.

1. The DSE and TE bits are set to 1 before initialization of DMACHCR, but after the interrupt was disabled.
   The TE and DSE bits are initialized within the DMA transfer initialization sequence.
2. The DSE and TE bits are set to1 and the controller fails to abort the transfer, after the interrupt was disabled.
   When the DE bit has become 0 after DMA transfer initialization, check the TE and DSE bits. If the TE or DSE bit is 1, go through the DMA transfer initialization process.
3. The TE and DSE bits are not cleared to 0 but the transfer is aborted, after the interrupt is disabled.
   The TE or DSE bits are not set because data for transfer still remain after transfer is aborted.

Note: Initialization of DMA transfer during execution of the last transfer leads to a delay in setting of the TE and DSE bits, so include a dummy read.

Figure 16.17 shows an example of processing to abort DMA transfer.

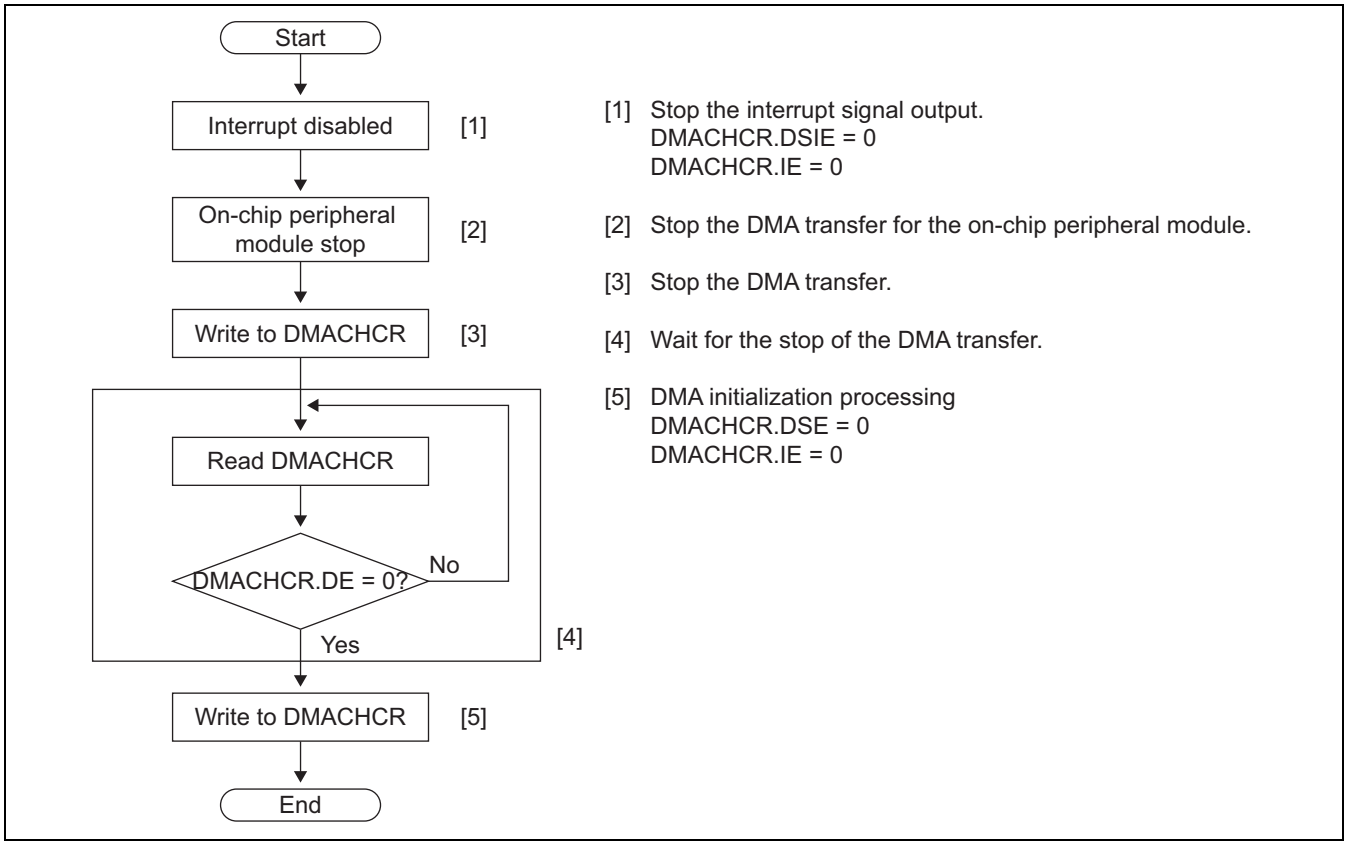


Figure 16.17 Example of Processing to Abort DMA Transfer

17. LBSC-DMAC

17.1 Overview

The LBSC-DMAC performs DMA transfer between the external bus (EX-BUS) and DDR3-SDRAM. The LBSC-DMAC is assigned channel numbers 0 to 2. These DMA channels are capable of independent parallel operation and a different transfer destination can be selected for each.

Different data transfer modes are selectable for each channel. In this section, the character "n" refers to one of the 3 DMA channels of the DMACs.

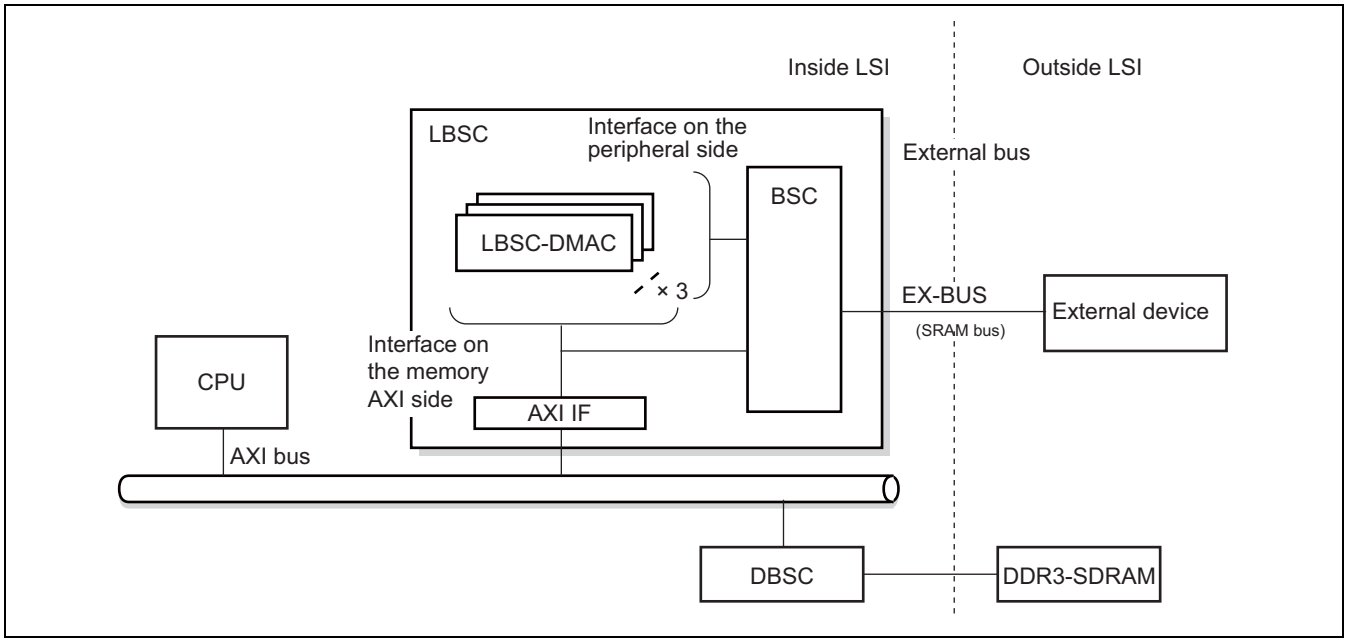


Figure 17.1 Context of LBSC-DMAC

Figure 17.1 shows the context of the LBSC-DMAC. The DMACs are connected to DDR3-SDRAM outside the chip via the DBSC, connected via a memory-side (AXI-bus) interface, and to peripherals connected to the external bus via the peripheral-side interface. Register settings within each of the DMACs select the connected (source and destination) peripheral module or memory. Of these, the LBSC-DMAC supports DMA transfers with general-purpose external devices on the EX-BUS (SRAM bus), and transfer can be performed under handshaking control by the DMA request and DMA acknowledge signals (these channels also support an auto-request mode with no handshaking).

17.2 Features

The LBSC-DMAC has the following features.

- Number of channels: Three channels (channels 0 to 2)
- Address space: Physical address space
- Transfer direction: Capable of transfer from a peripheral module to a memory (AXI bus), or from a memory (AXI bus) to a peripheral module
- Transfer data length:
  - For peripherals: Selectable from 1, 2, or 4 bytes.
  - For memory (AXI bus):

    When the SWMD bit in the DCR register is cleared to 0: Access size specified for a memory (AXI bus) (For details on each channel access size, see section 17.4.8, DMA Control Register (DCR).)
    When the SWMD bit in the DCR register is set to 1: 4 bytes
    When final packing processing is performed while the PKMD bit in the DCR register is set to 1: 1 byte or the access size specified for a memory (AXI bus)
- Transfer burst length: 1 or 8 (Transfer with a burst length of 8 is supported only for channels 0 and 1.)
- Transfer count:
  - Maximum: 16 M (16,777,216) or 64 M (67,108,864) times (64 M is supported only for channel 0 of LBSC-DMAC.)
  - Minimum: One time
- Address mode: Dual address mode
  - Dual address mode

    Both the transfer source and transfer destination are accessed by using addresses.

    Values set in the DMAC's internal registers indicate the addresses for both the transfer source and the transfer destination. (Registers: DMA source address register (DSAR0 or DSAR1), DMA destination address register (DDAR0 or DDAR1), and DMA control register (DCR; bits SPDAM and DPDAM))
- Transfer requests: The external requests, peripheral requests, auto-requests, and timer requests are supported.
  - External requests

    Requests from three external DREQ pins. Low or high level detection or edge detection can be specified for the request signals (DREQ) in the LBSC register. Either the active high or active low logic can be specified by LBSC for the request acknowledge level signal (DRACK) and the acknowledge level signal (DACK). (DRACK is supported for only channel 0 of the LBSC-DMAC.)
  - Peripheral request

    Transfer requests from on-chip peripheral modules.
  - Auto-request
  - Initiates DMA transfer according to the DMAC internal timing.
  - Timer request

    A transfer request is generated at an interval specified by a timer in the DMAC.
- Transfer modes: Single transfer and continuous transfer modes are supported.
  - Single transfer mode

    DMA transfer ends when transfer is completed for the transfer count specified by the DMA transfer count register.
  - Continuous transfer mode

    Available in all channels. If there is a next DMA transfer request (DNXT) when transfer is completed for the transfer count specified by the DMA transfer count register, the next DMA transfer information is fetched and the next DMA transfer is continued. If no next DMA transfer request (DNXT) is found, the DMAC waits until a next DMA transfer request is specified. The continuous transfer mode is terminated by the DQEND bit in the DMA command register (DCMDR).

- DMA information can be specified in two modes: one mode uses one of two sets of DMA information registers (registers in which the offset of the address is in the range from H'0000_0000 to H'0000_0014) repeatedly, and the other uses the two sets alternately.
- The DMAC also provides the automatic continuous transfer mode. The automatic continuous transfer mode is enabled by setting the ACMD bit in the DMA control register (DCR) to 1 while the continuous transfer mode is enabled (the CT bit in DCR is set to 1). In this mode, when transfer is completed for the transfer count specified by the DMA transfer count register, the DMAC fetches the next DMA transfer information and continues DMA transfer regardless of whether there is a next DMA transfer request (DNXT). This mode is terminated by the DQEND bit in the DMA command register (DCMDR).
- Transfer end interrupt: An interrupt request can be sent to the CPU on completion of the number of transfers specified for each DMA information unit.

17.3 DMA Transfer Method in LBSC-DMAC

The relation of each DMA channel to peripherals is shown below. Transfers can be performed with between various functional blocks over different channels, but if destination is on the memory (AXI) side, DDR3-SDRAM via the DBSC and so on becomes the destination for transfer according to the address setting.

Channel	Application	Communication Type	Selection of Transfer Destination (On-Chip Peripheral Function)
LBSC-DMA00	Communication with general-purpose device via EX-BUS	Dual address transfer, single transfer or 8-burst transfer, DREQ/DACK handshake (Channel 0 can select DRACK	DREQ/DACK number and DMA channel number correspond. External bus spaces allocated to each DMAC are specified in the LBSC internal register.
LBSC-DMA01			
LBSC-DMA02		Dual address transfer single transfer, DREQ/DACK handshake	

17.4 Register Descriptions

Registers shown below can be accessed from both ARM CPUs. The DMAC has three channels; some registers are prepared for each individual channel and some are used by all channels in common.

17.4.1 LBSC-DMAC Register Map

Table 17.1 List of LBSC-DMAC Registers

Register Name		Abbr.	Access Type	Address	Access Size
DMA source address register 0	DMA information register set 0	DSAR0	R/W	H'FEC01000 + H'40 × [n]	32
DMA destination address register 0		DDAR0	R/W	H'FEC 01004 + H'40 × [n]	32
DMA transfer count register 0		DTCR0	R/W	H'FEC 01008 + H'40 × [n]	32
DMA source address register 1	DMA information register set 1	DSAR1	R/W	H'FEC 0100C + H'40 × [n]	32
DMA destination address register 1		DDAR1	R/W	H'FEC 01010 + H'40 × [n]	32
DMA transfer count register 1		DTCR1	R/W	H'FEC 01014 + H'40 × [n]	32
DMA source address status register		DSASR	R	H'FEC 01018 + H'40 × [n]	32
DMA destination address status register		DDASR	R	H'FEC 0101C + H'40 × [n]	32
DMA transfer count status register		DTCSR	R	H'FEC 01020 + H'40 × [n]	32
DMA control register		DCR	R/W	H'FEC 01028 + H'40 × [n]	32
DMA command register		DCMDR	—/W	H'FEC 0102C + H'40 × [n]	32
DMA forced stop register		DSTPR	—/W	H'FEC 01030 + H'40 × [n]	32
DMA status register		DSTSR	R	H'FEC 01034 + H'40 × [n]	32
DMA channel debugging register		DDBGR	R/W	H'FEC 01038 + H'40 × [n]	32
DMA channel debugging register 2		DDBGR2	R/W	H'FEC 0103C + H'40 × [n]	32
DMA timer control register		DTIMR	R/W	H'FEC 01400	32
DMA request mask control register		DRMSKR	R/W	H'FEC 01404	32
DMA memory access priority level control register		DMLVLR	R/W	H'FEC 0140C	32
DMA transfer end interrupt status register		DINTSR	R	H'FEC 01410	32
DMA transfer end interrupt status clear register		DINTCR	—/W	H'FEC 01414	32
DMA transfer end interrupt enable register		DINTMR	R/W	H'FEC 01418	32
DMA activation status register		DACTSR	R	H'FEC 01420	32
DMA00 to DMA02 channel software-reset register		LSRSTR0 to LSRSTR2	R/WC1	H'FEC 01424 to H'FEC 0142C	32
External-DMA data alignment control register		DMALGR	R/W	H'FEC 01480	32
LBSC-DMA AXI priority control register		LBSC-DMASPR	R/W	H'FEC 01490	32

Notes: 1. n: LBSC-DMAC channel number
2. The CPU should access the above register in long word units (32 bits). The CPU should not access the above register in byte or word units.
3. Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than listed above are undefined.

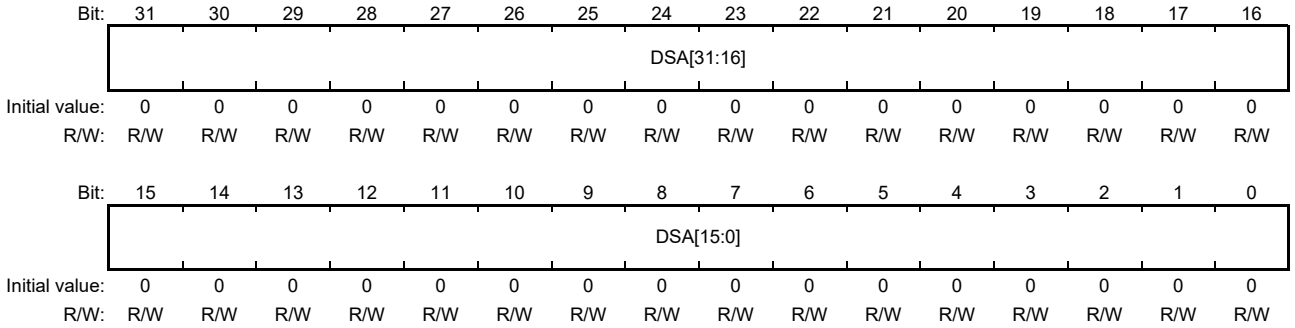
[Legend]

Initial value:	Register value after a reset
—:	Undefined value
R/W:	Readable/writable. The written value can be read.
R/WC1:	Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.
R:	Read-only. The write value should always be 0.
—/W:	Write-only. The read value is undefined.

All signals for the control registers and status registers are active-high.

17.4.2 DMA Source Address Registers 0, 1 (DSAR0, DSAR1)

Function: Each register specifies the DMA start address of the transfer source.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSA	All 0	R/W	DMA Transfer Source Start Address The transfer source start address indicates a memory address, a peripheral module address, or an external module address according to the SMDL bit value in the DMA control register (DCR). When SMDL = 0: Transfer source address = Memory (AXI bus) address When SMDL = 1: Transfer source address = Peripheral address or external module address

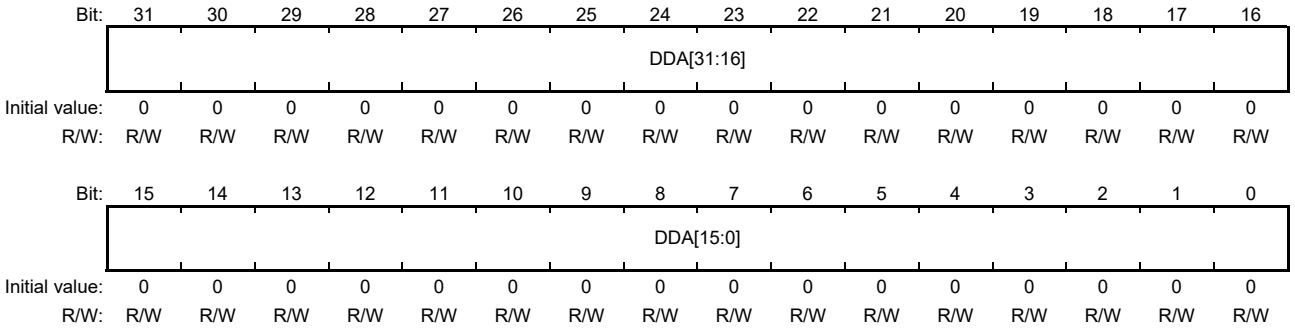
Notes: 1. When the address setting is a memory address, the following address boundary should be used.

	LBSC-DMAC Channel Number	
SWMD Bit in the DCR Register	Channels 0 and 1	Channel 2
0	32-byte boundary	16-byte boundary
1	4-byte boundary	

2. When the address set is an external module address, and in addition the SPDS or DPDS bit in DCR selects an 8-bit access size, up to an 8-bit boundary can be set.
3. In the case of note 2, when the DMAC external module data access size is smaller than the external bus width setting in LBSC, the DMALGR register in the DMAC can be used to specify whether there is a change in data alignment (data access byte lane according to the address value). See section 17.4.22, External DMA Data Alignment Control Register (DMALGR) and specifications of section 14, LBSC within Bus Bridge.
4. When an address setting is an external module address, the upper address bits 31 to 26 are not connected to the external bus. These are provided for ease in understanding the contents of software settings. Also, CS1 identification using these upper bits is not performed. DMAC access destination space is identified through the LBSC external DMAC channel area allocation register.
5. When an address setting is for a peripheral device, the upper address is provided for ease of understanding of the contents of software settings, and is not used for identification of access destination space specific to the peripheral.

17.4.3 DMA Destination Address Registers 0, 1 (DDAR0, DDAR1)

Function: Each register specifies the DMA start address of the transfer destination.

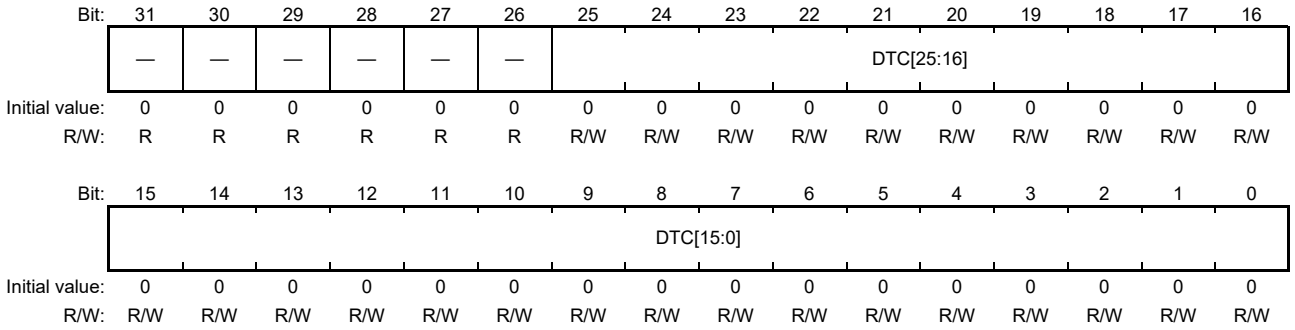


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DDA	All 0	R/W	DMA Transfer Destination Start Address The transfer destination start address indicates a memory address, a peripheral module address, or an external module address according to the DMDL bit value in the DMA control register (DCR). When DMDL = 0: Transfer destination address = Memory (AXI bus) address When DMDL = 1: Transfer destination address = Peripheral module or external module address

Note: See the notes 1 to 5 in section 17.4.2, DMA Source Address Registers 0, 1 (DSAR0, DSAR1). Those notes also apply to this register.

17.4.4 DMA Transfer Count Registers 0, 1 (DTCR0, DTCR1)

Function: Each register specifies the DMA transfer count.

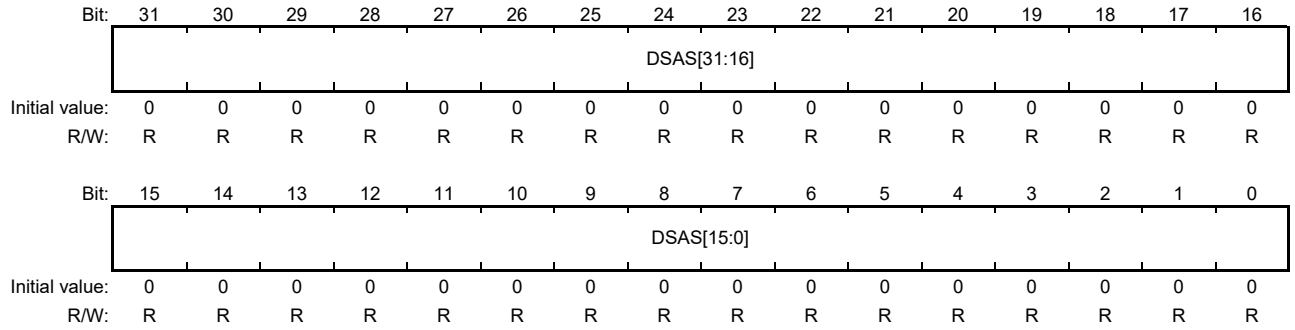


Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	DTC	All 0	R/W	DMA Transfer Count These bits specify the DMA transfer count (number of bytes, words, or long words). LBSC-DMAC channel 0: The maximum count is DTC = H'0, which indicates 64 M (67,108,864) times. Other than LBSC-DMAC channel 0: The maximum count is DTC = H'0, which indicates 16 M (16,777,216) times.

Note: This register specifies the transfer count on the peripheral side for transfer from a peripheral to a memory (AXI bus) or from a memory (AXI bus) to a peripheral. For 8-burst DMA operation, one count for each 8-burst operation.

17.4.5 DMA Source Address Status Register (DSASR)

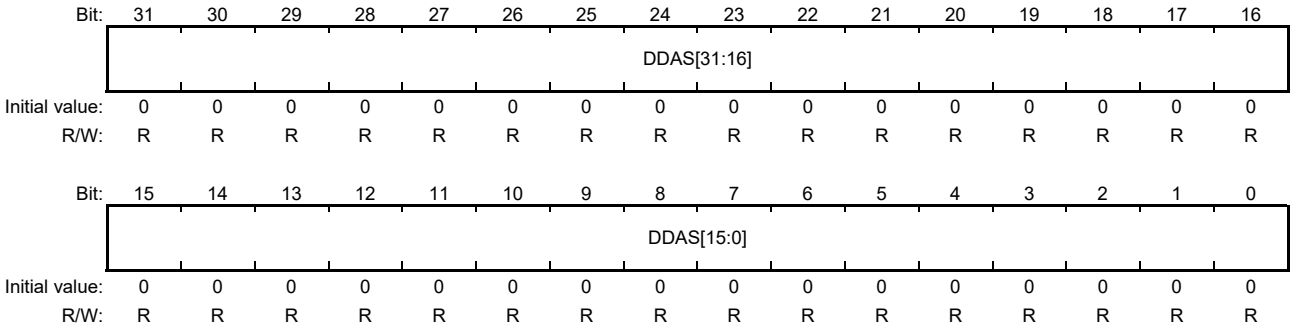
Function: DSASR indicates the transfer source address.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSAS	All 0	R	These bits indicate the latest source address for which DMA transfer has been completed.

17.4.6 DMA Destination Address Status Register (DDASR)

Function: DDASR indicates the transfer destination address.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DDAS	All 0	R	These bits indicate the latest destination address for which DMA transfer has been completed.

17.4.7 DMA Transfer Count Status Register (DTCSR)

Function: DTCSR indicates the remaining count of the current transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	DTCS[25:16]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTCS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	DTCS	All 0	R	Remaining DMA Transfer Count These bits indicate the remaining count of the current DMA transfer (number of bytes, words, or long words). Note that bits 25 to 0 are used only for the LBSC-DMAC channel 0 and bits 23 to 0 are used for the other channels. The number of transferred bytes depends on the peripheral's data bus width.

Note: This register indicates the remaining transfer count on the peripheral side for transfer from a peripheral to a memory (AXI bus) or from a memory (AXI bus) to a peripheral.

17.4.8 DMA Control Register (DCR)

Function: DCR specifies the transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	DTAMD	DTAC	DTAU	DTAU1	SWMD	BTMD	PKMD	—	CT	ACMD	DIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SMDL	SPDAM	SDRMD		SPDS		—	—	DMDL	DPDAM	DDRMD		DPDS	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26	DTAMD	0	R/W	Specifies the data alignment conversion mode when a memory is accessed in DMA transfer (see section 17.5.7, Data Alignment in AXI Bus Interface). 0: Conversion according to the combination of the input pin (little: endian mode) and the AXI width. 1: Conversion according to the combination of DTAC (DMA data alignment conversion), DTAU (DMA data alignment unit), and DTAU1 (8-byte conversion in 4-byte units).
25	DTAC	0	R/W	Enables or disables data alignment conversion when a memory is accessed in DMA transfer (see section 17.5.7, Data Alignment in AXI Bus Interface). This setting is valid when DTAMD = 1. 0: Disables data alignment conversion. 1: Enables data alignment conversion.
24	DTAU	0	R/W	Specifies the unit for data alignment conversion (see section 17.5.7, Data Alignment in AXI Bus Interface). This setting is valid when DTAMD = 1. 0: Byte units 1: Word units
23	DTAU1	0	R/W	Specifies whether 8-byte data alignment is performed in 4 bytes unit (see section 17.5.7, Data Alignment in AXI Bus Interface). The setting value is valid when DTAMD = 1. 0: Not performed. 1: Performed.
22	SWMD	0	R/W	Specifies memory (AXI bus) access size. 0: * (Clearing this bit to 0 is recommended when DDR3-SDRAM is specified.) 1: 4 bytes
21	BTMD	0	R/W	Specifies the burst DMA transfer (only for LBSC-DMAC channels 0 and 1). Burst DMA transfer is performed for peripherals. 0: Does not transfer in burst mode. 1: Transfers in burst mode (burst length is fixed to eight).

Bit	Bit Name	Initial Value	R/W	Description
20	PKMD	0	R/W	Enables or disables packing of data read from a peripheral for DMA transfer from the peripheral to the AXI bus. 0: Disables packing. 1: Enables packing.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18	CT	0	R/W	Specifies continuous DMA transfer. 0: Does not transfer in continuous mode. 1: Transfers in continuous mode.
17	ACMD	0	R/W	Specifies automatic continuous DMA transfer (valid only when CT = 1). 0: Does not transfer in automatic continuous mode (checks DNXT = 1 in DCMDR). 1: Transfers in automatic continuous mode (regardless of the DNXT bit in DCMDR).
16	DIP	0	R/W	Specifies the valid DMA information set(s). 0: Uses one DMA information set repeatedly. 1: Uses two DMA information sets alternately.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	SMDL	0	R/W	Selects the transfer source module. 0: Memory (AXI bus) 1: Peripheral
12	SPDAM	0	R/W	Specifies whether to fix or increment the transfer source peripheral address. 0: Fixes the peripheral address at the value specified in DSAR0 or DSAR1. 1: Increments the peripheral address (increments by one for 8-bit transfer, by two for 16-bit transfer, or by 4 for 32-bit transfer). When SMDL = 0, the address for memory access (via the AXI bus) is incremented regardless of the setting of this bit.
11, 10	SDRMD	00	R/W	These bits specify the DMA request mode for the transfer source. 00: Module request (external request or peripheral module request) 01: Auto-request 10: Timer request 11: Setting prohibited When SMDL = 0, clear the SDRMD bits to B'00 or set them to the same value as that of the DDRMD bits.
9, 8	SPDS	00	R/W	These bits specify the data bus width for the transfer source peripheral. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When SMDL = 0, clear the SPDS bits to B'00 or set them to the same value as that of the DPDS bits.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	DMDL	0	R/W	Selects the transfer destination module. 0: Memory (AXI bus) 1: Peripheral

Bit	Bit Name	Initial Value	R/W	Description
4	DPDAM	0	R/W	Specifies whether to fix or increment the transfer destination peripheral address. 0: Fixes the peripheral address at the value specified in DDAR0 or DDAR1. 1: Increments the peripheral address (increments by one for 8-bit transfer, by two for 16-bit transfer, or by 4 for 32-bit transfer). When DMDL = 0, the address for memory access (via the AXI bus) is incremented regardless of the setting of this bit.
3, 2	DDRMD	00	R/W	These bits specify the DMA request mode for the transfer destination. 00: Module request (external request or peripheral module request) 01: Auto-request 10: Timer request 11: Setting prohibited When DMDL = 0, clear the DDRMD bits to B'00 or set them to the same value as that of the SDRMD bits.
1, 0	DPDS	00	R/W	These bits specify the data bus width for the transfer destination peripheral. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When DMDL = 0, clear the DPDS bits to B'00 or set them to the same value as that of the SPDS bits.

Notes: 1. When SMDL and DMDL = 1 and 0, data is transferred from a peripheral to a memory.
When SMDL and DMDL = 0 and 1, data is transferred from a memory to a peripheral.
Setting SMDL and DMDL = "1 and 1" or "0 and 0" is prohibited.

2. Not all DMAC functions can be applied to every peripheral. DMAC functions must be specified appropriately according to the functions and restrictions of each peripheral.

3. Since the width of the EX-BUS is 16 bits, setting of the SPDS or DPDS bits for the LBSC-DMAC to B'10 (selecting a transfer source or destination width of 32 bits, respectively) is prohibited.

* The following table summarizes the memory (AXI) access size in each DMAC channel when SWMD bit is cleared to 0.

	LBSC-DMAC Channel Number	
SWMD Bit in DCR Register	Channels 0 and 1	Channel 2
0	32 bytes	16 bytes

17.4.9 DMA Command Register (DCMDR)

Function: DCMDR activates or stops DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BDOUT	DQSPD	DQSPC	DMSPD	DMSPC	DQEND	DNXT	DMEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	BDOUT	0	—/W	1: Forcibly writes the data read from a peripheral to the AXI bus side (Transfer direction: from a peripheral to the AXI bus). Writing 1 to this bit forcibly writes to the AXI bus side, and then terminates DMA transfer.
6	DQSPD	0	—W	1: Temporarily stops transfer in DMA information units.
5	DQSPC	0	—/W	1: Cancels temporary transfer stop in DMA information units.
4	DMSPD	0	—/W	1: Temporarily stops transfer in bus cycle units.
3	DMSPC	0	—/W	1: Cancels temporary transfer stop in bus cycle units.
2	DQEND	0	—/W	1: Terminates continuous DMA transfer mode. Only the DMA information specified before is transferred, and then continuous transfer mode is terminated.
1	DNXT	0	—/W	1: Requests the next DMA transfer. In continuous transfer mode, after the current DMA information is transferred, the next DMA information is transferred.
0	DMEN	0	—/W	1: Activates DMA transfer.

Note: For use of BDOUT, see sections 17.5.3, Packing Data Read from Peripheral or External Module and 17.5.4, Limitations on Packing of Data Read from Peripheral or External Module.

17.4.10 DMA Forced Stop Register (DSTPR)

Function: DSTPR forcibly terminates DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DMSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DMSTP	0	—/W	1: Forcibly terminates DMA transfer. After the current bus cycle is completed, DMA transfer is terminated. (Values set for the DMA transfer status registers (DSASR, DDASR, and DTCSR) are retained.)

17.4.11 DMA Status Register (DSTSR)

Function: DSTSR indicates the DMA transfer status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

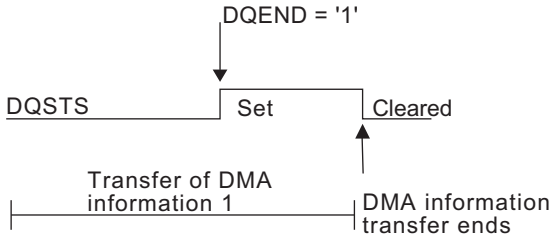
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	NDP1	NDP0	DQSPS	DMSPS	DQSTS	DRSTS	DMSTS
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	NDP1	0	R	Next DMA Transfer Information Register Status 1 0: Does not transfer DMA information in DMA information register set 1 in the next DMA information transfer. 1: Transfers DMA information in DMA information register set 1 in the next DMA information transfer.
5	NDP0	1	R	Next DMA Transfer Information Register Status 0 0: Does not transfer DMA information in DMA information register set 0 in the next DMA information transfer. 1: Transfers DMA information in DMA information register set 0 in the next DMA information transfer.
4	DQSPS	0	R	Temporary Stop Status of DMA Information Updating 0: Normal operation 1: DMA information updating is temporarily stopped.
3	DMSPS	0	R	Temporary Stop Status of DMA Transfer 0: Normal operation 1: DMA transfer is temporarily stopped.
2	DQSTS	0	R	DMA Acceptance End Status 0: DMA information can be accepted. 1: DMA information acceptance is stopped.
1	DRSTS	0	R	DMA Transfer Request Status 0: Next DMA transfer has not been requested. 1: Next DMA transfer has been requested.
0	DMSTS	0	R	DMA Status 0: DMA transfer has been completed. 1: DMA transfer is active.

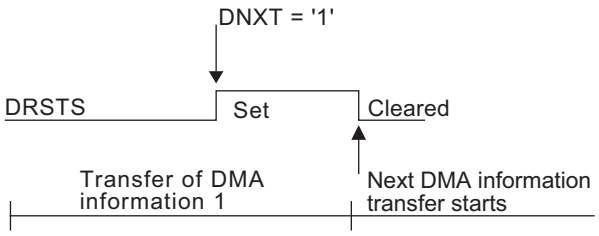
Note: Either NDP0 or NDP1 (next DMA transfer information register status 0 or 1) is always set to 1.

The following shows the transition of each bit status in DSTSR.

		Conditions of Status Transition	
	0 ⟶	1 ⟶	0
NDP1	Initial state	Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 0 is in progress.	Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 1 is in progress.
NDP0	—	1. Initial state 2. Single transfer mode: Always 3. Continuous transfer mode is selected and information register set 0 is used repeatedly (DIP in DCR = 0): Always 4. Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 1 is in progress.	Continuous transfer mode is selected and information register sets 0 and 1 are used alternately (DIP in DCR = 1): DMA transfer for information register set 0 is in progress.
DQSPS	Initial state	DMA transfer is temporarily stopped in DMA information units (DQSPD in DCMDR = 1) and the current information transfer is completed.	Temporary stop of DMA transfer in DMA information units is canceled (DQSPC in DCMDR = 1).
DMSPS	Initial state	DMA transfer is temporarily stopped in bus cycle units (DMSPD in DCMDR = 1) and the current bus cycle is completed.	Temporary stop of DMA transfer in bus cycle units is canceled (DMSPC in DCMDR = 1).
DQSTS	Initial state	Continuous transfer mode is selected (CT in DCR = 1) and DMA continuous transfer is terminated (DQEND = 1) during transfer of DMA information 1.	Transfer of DMA transfer information ends.

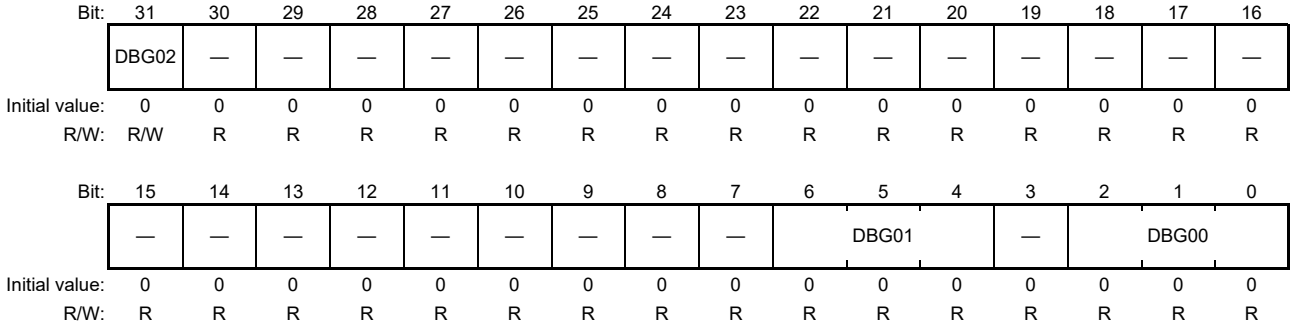


		Conditions of Status Transition 0 → 1	1 → 0
DRSTS	Initial state	Continuous transfer mode is selected (CT in DCR = 1) and next DMA transfer information is requested (DNXT = 1) during transfer of DMA information 1.	Next DMA information transfer is started.
DMSTS	Initial state	DMA is activated (DMEN in DCMDR = 1).	End state (remains in the idle state). 1. Transfer end a. Single transfer mode: Transfer of one DMA information set is completed. b. Continuous transfer mode: DRSTS = 0 and DQSTS = 1 in DSTSR and transfer of current DMA information is completed. 2. Forced stop DMSTP in DSTPR is set to 1 and DMA transfer is terminated after the current bus cycle is completed.



17.4.12 DMA Channel Debugging Register (DDBGR)

Function: DDBGR is used for debugging.



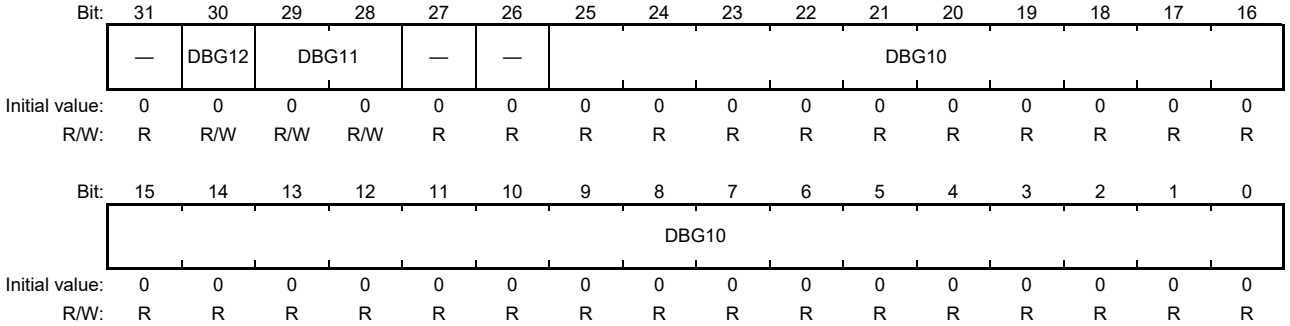
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DBG02	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DBG01			—	DBG00		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	DBG02	0	R/W	Test Bit This bit is a test bit and cannot be written to. If this bit is written to, correct operation cannot be guaranteed.
30 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 4	DBG01	All 0	R	Test Bits
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	DBG00	All 0	R	Test Bits

17.4.13 DMA Channel Debugging Register 2 (DDBGR2)

Function: DDBGR2 is used to for debugging.



Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	DBG12	0	R/W	Test Bit This bit is a test bit and cannot be written to. If this bit is written to, correct operation cannot be guaranteed.
29, 28	DBG11	All 0	R/W	Test Bits These bits are test bits and cannot be written to. If these bits are written to, correct operation cannot be guaranteed.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	DBG10	All 0	R	Test Bits

17.4.14 DMA Timer Control Register (DTIMR)

Function: DTIMR specifies the timer cycle in the DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DTIM[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	DTIM	All 0	R/W	DMAC Internal Timer Cycle Set Request mode: Specify the DMA request interval in timer request mode. Request interval: DTIM × peripheral-side bus clock cycle (ns) Peripheral-side bus clock cycle (ns) for LBSC-DMAC: Approximately 15 ns (EX-BUS frequency 65.00 MHz) Note: Even in timer request mode, operation is the same as that in auto-request mode when the value of DTIM is 0.

17.4.15 DMA Request Mask Control Register (DRMSKR)

Function: DRMSKR0 specifies the timing for detecting DMA requests in the external-bus DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DRMSK2[3:0]				DRMSK1[3:0]				DRMSK0[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	DRMSK2	All 0	R/W	These bits specify the number of clock cycles from the completion of a DMA transfer (at the time of CS# signal negation) until the next DMA request is detected, for each DMAC channel corresponding to each field. Request detection cycle: DRMSK × external bus clock cycle (ns)
7 to 4	DRMSK1	All 0	R/W	
3 to 0	DRMSK0	All 0	R/W	

Note: Settings for DRMSK2 to DRMSK0 are only valid when level-detection is specified for the external DREQ signal (specified by EXDMCRy in the LBSC) for the channel. In edge-detection mode, set the bits to 0.

17.4.16 DMA Memory Access Priority Level Control Register (DMLVLR)

Function: DMLVLR specifies the access priority level (1 or 2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DMLV2	DMLV1	DMLV0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DMLV2	0	R/W	These bits specify the external bus arbitration priority group for each DMAC channel which corresponds to each bit. 0: Level 2 (Low: Group 2) 1: Level 1 (High: Group 1)
1	DMLV1	0	R/W	
0	DMLV0	0	R/W	

17.4.17 DMA Transfer End Interrupt Status Register (DINTSR)

Function: DINTSR indicates the DMA transfer end interrupt status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DTE2	DTE1	DTE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DTE2	0	R	DMA Transfer End Interrupt Status Each bit indicates the DMA transfer status (n: DMA channel number). 0: Initial state or data is being transferred before the count specified by DTCR is reached. 1: Transfer has been completed for the count specified by DTCR.
1	DTE1	0	R	
0	DTE0	0	R	

17.4.18 DMA Transfer End Interrupt Status Clear Register (DINTCR)

Function: DINTCR clears the DMA transfer end interrupt status.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DTEC2	DTEC1	DTEC0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W	—/W	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DTEC2	0	—/W	DMA Transfer End Interrupt Status Clear Writing 1 to each bit clears the corresponding DMA transfer end interrupt status (n: DMAC channel number) Writing 0 to these bits is ignored. Each bit is always read as 0.
1	DTEC1	0	—/W	
0	DTEC0	0	—/W	

17.4.19 DMA Transfer End Interrupt Enable Register (DINTMR)

Function: DINTMR controls output of DMA transfer end interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DTEM2	DTEM1	DTEM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DTEM2	0	R/W	DMA Transfer End Interrupt Output Control An interrupt signal is output as a level signal (n: DMA channel number). 0: Does not output an interrupt on completion of a DMA transfer. 1: Outputs an interrupt on completion of a DMA transfer.
1	DTEM1	0	R/W	
0	DTEM0	0	R/W	

17.4.20 DMA Activation Status Register (DACTSR)

Function: DACTSR indicates the activation status of each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	DS2	DS1	DS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	DS2	0	R	DMA Channel n Status (n: DMA channel number) 0: Idle state 1: Active state
1	DS1	0	R	
0	DS0	0	R	

17.4.21 Software-Reset Registers (LSRSTR0 to LSRSTR2)

Function: Each register resets DMA channel n.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRST	0	R/WC1	Software Reset Resets DMA channel n. 0: Writing 0 is ignored. 1: Resets DMA channel n. This register is always read as 0.

Note: Writing 1 resets the DMAC regardless of the DMA transfer status. The same registers are reset as when a power-on reset is performed. Accordingly, a software reset should be used only while DMA transfer is not in progress (e.g., during system debugging). To stop operation, forced termination or temporary stop should be specified instead of software reset. In the registers used by all channels in common (DMA transfer end interrupt status register (DINTSR) and DMA transfer end interrupt enable register (DINTMR)), only the bits corresponding to the software-reset channel are initialized.

17.4.22 External DMA Data Alignment Control Register (DMALGR)

Function: DMALGR specifies whether there is a data alignment conversion in external bus access by the external bus DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DMLG2				DMLG1				DMLG0			
					exbwe	exac	exbw		exbwe	exac	exbw		exbwe	exac	exbw	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	DMLGn exbwe	0	R/W	Specifies whether there is an EX-BUS data alignment conversion for each DMAC channel (n: DMAC channel number). When the DMAC/DCR setting DMA access bus width is smaller than the external bus width for the relevant DMA area set in LBSC. 0: Access byte lanes fixed 1: Access byte lanes variable
	DMLGn exac	0	R/W	Specifies endian setting when there is alignment conversion with the exbwe bit set to 1 (n: DMAC channel number). 0: Big endian 1: Little endian
	DMLGn exbw	00	R/W	Specifies the unit for data alignment conversion with the exbwe bit set to 1 (n: DMAC channel number). 00: 8 bits 01: 16 bits 10: Setting prohibited 11: Invalid

Note: Does not need to be set when the bus width set in LBSC and the DMA access size set in DMAC/DCR are the same. For details, see section 14.7.3 (1), Data Alignment during LBSC-DMAC Access in specifications for LBSC within Bus Bridge.

17.4.23 LBSC-DMA AXI Priority Control Register (LBSC-DMASPR)

Function: LBSC-DMASPR specifies the AXI bus access priority level for external DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SPRR2				SPRR1				SPRR0			
Initial value:	0	0	0	0	1	0	0	0	1	0	0	0	1	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	SPRRn	H'8	R/W	Specify the AXI bus access priority level for each DMAC channel (n: DMAC channel number). Priority: H'0 (lowest) to H'F (highest)

Note: Since AXI bus access priority level settings relate to priority control for the AXI bus overall, priority levels with other access modules must be confirmed when making settings.

17.5 Operation

17.5.1 DMA Transfer Procedure

The following describes the DMA transfer procedure.

1. Making the initial setting for the DMAC
   Specify transfer conditions in the DMA control register (DCR).
2. Specifying DMA transfer information
   Make appropriate settings in the following registers according to the DIP bit setting (input mode: using one information set repeatedly or two information sets alternately) in DCR:
   DMA source address register (DSAR)
   DMA destination address register (DDAR)
   DMA transfer count register (DTCR)
   When the DIP bit specifies that one information set is used repeatedly, make the appropriate settings in DSAR0, DDAR0, and DTCR0.
3. Activating the DMAC
   Activate the DMAC by setting the DMEN bit in the DMA command register (DCMDR).
4. Reading the specified DMA transfer information
   The specified DMA transfer information is read from DMA information registers 0 and 1 in that order.
5. Clearing the DMA transfer request
   The DMA transfer request status signal is cleared.
6. Starting DMA transfer
   When the auto-request mode is selected as the transfer request mode, transfer automatically starts at the DMAC transfer timing after the transfer information is obtained.
   When the external request or peripheral request mode is selected, DMA transfer is performed for one bus access cycle when a transfer request is accepted.
   When the timer request is selected, transfer automatically starts at the intervals specified in the DMAC internal timer after the transfer information is obtained.
7. Issuing an interrupt for the end of a specified number of transfers
   In single transfer mode, DMA transfer stops when transfer is completed for the specified number of times, and the CPU is notified of the end of transfer through an interrupt.
   In continuous transfer mode, the CPU is notified of the end of transfer in DMA transfer information units through an interrupt.
   The interrupt signal is controlled according to the setting in the DMA transfer end interrupt enable register (DINTMR).
8. Reading the next DMA transfer information (continuous transfer mode)
   If the next DMA transfer request is specified, the information of the transfer is read and data is transferred in the same way as described in step 6.
   If no additional DMA transfer request is specified (DRSTS = 0), the continuous DMA transfer mode is terminated when DQSTS = 1, or the next DMA transfer request is waited for when DQSTS = 0.
9. Adding DMA transfer information (continuous transfer mode)
   If new DMA transfer information should be added, specify the information in the DMA transfer information set that will be used for the next transfer (the next DMA transfer information set can be checked with the NDP1 and NDP0 bits in the DMA status register (DSTSR)).
   If no DMA transfer information should be added, write 1 to the DQEND bit in the DMA command register (DCMDR) to terminate the continuous transfer mode.

Note: Actually, the source bus and destination bus operate independently.

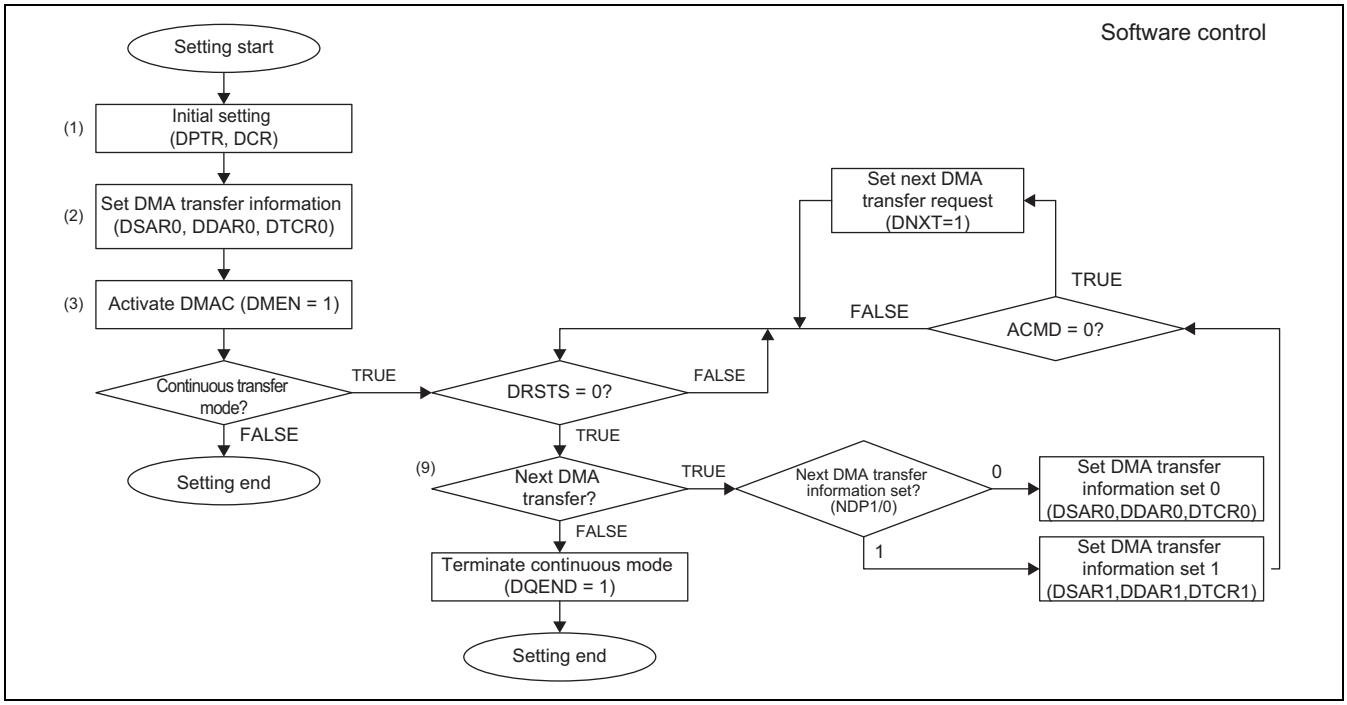


Figure 17.2 DMA Transfer Flowchart (1)

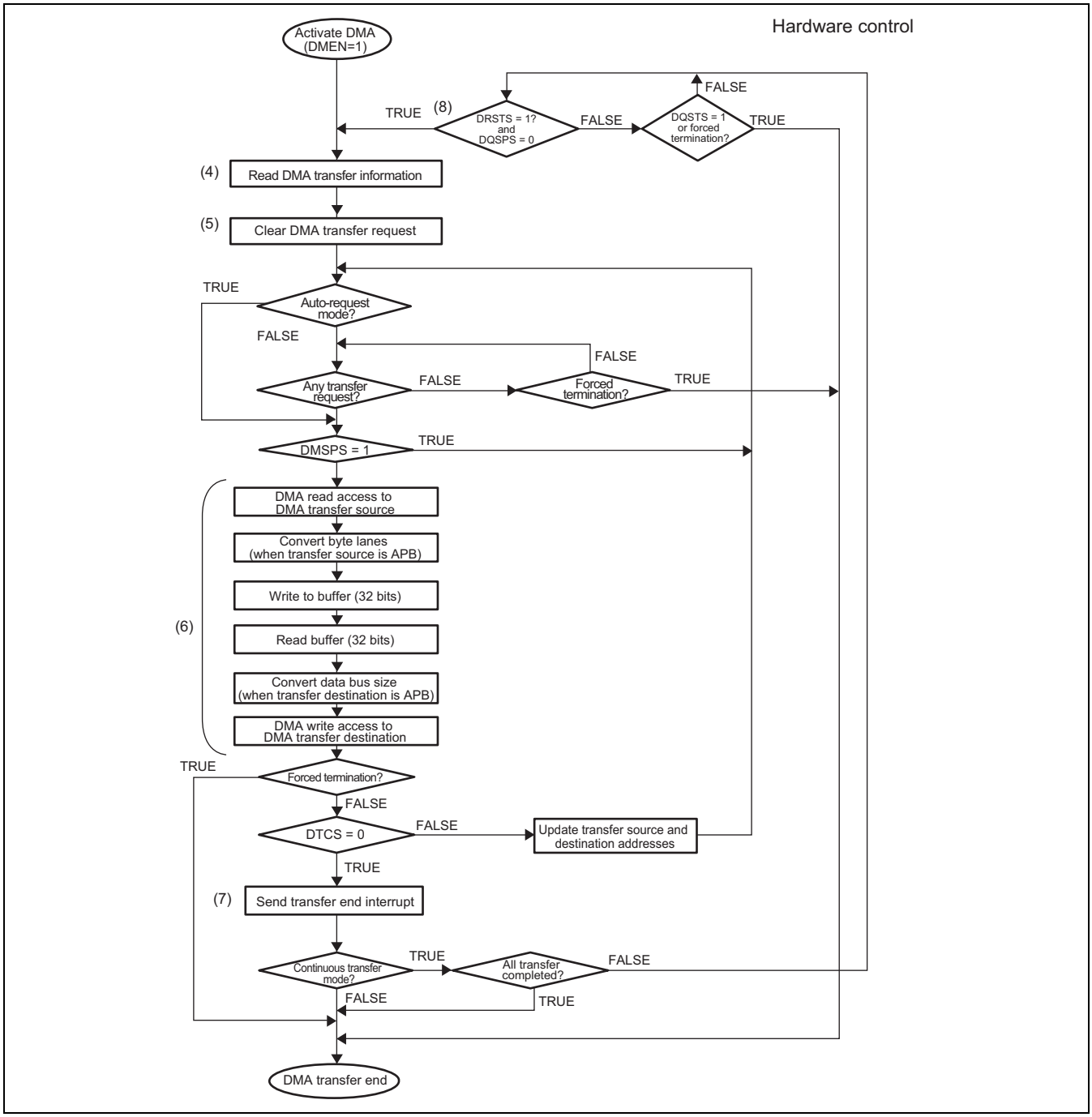


Figure 17.3 DMA Transfer Flowchart (2)

17.5.2 Continuous DMA Transfer Operation

The following shows the relationship between addition of DMA transfer information by software and DMA transfer information read and data transfer operation by hardware, which are described in step 9 in section 17.5.1, DMA Transfer Procedure. Figures 17.4 and 17.5 show transfer using DMA information set 0 repeatedly, and Figures 17.6 and 17.7 show transfer using DMA information sets 0 and 1 alternately.

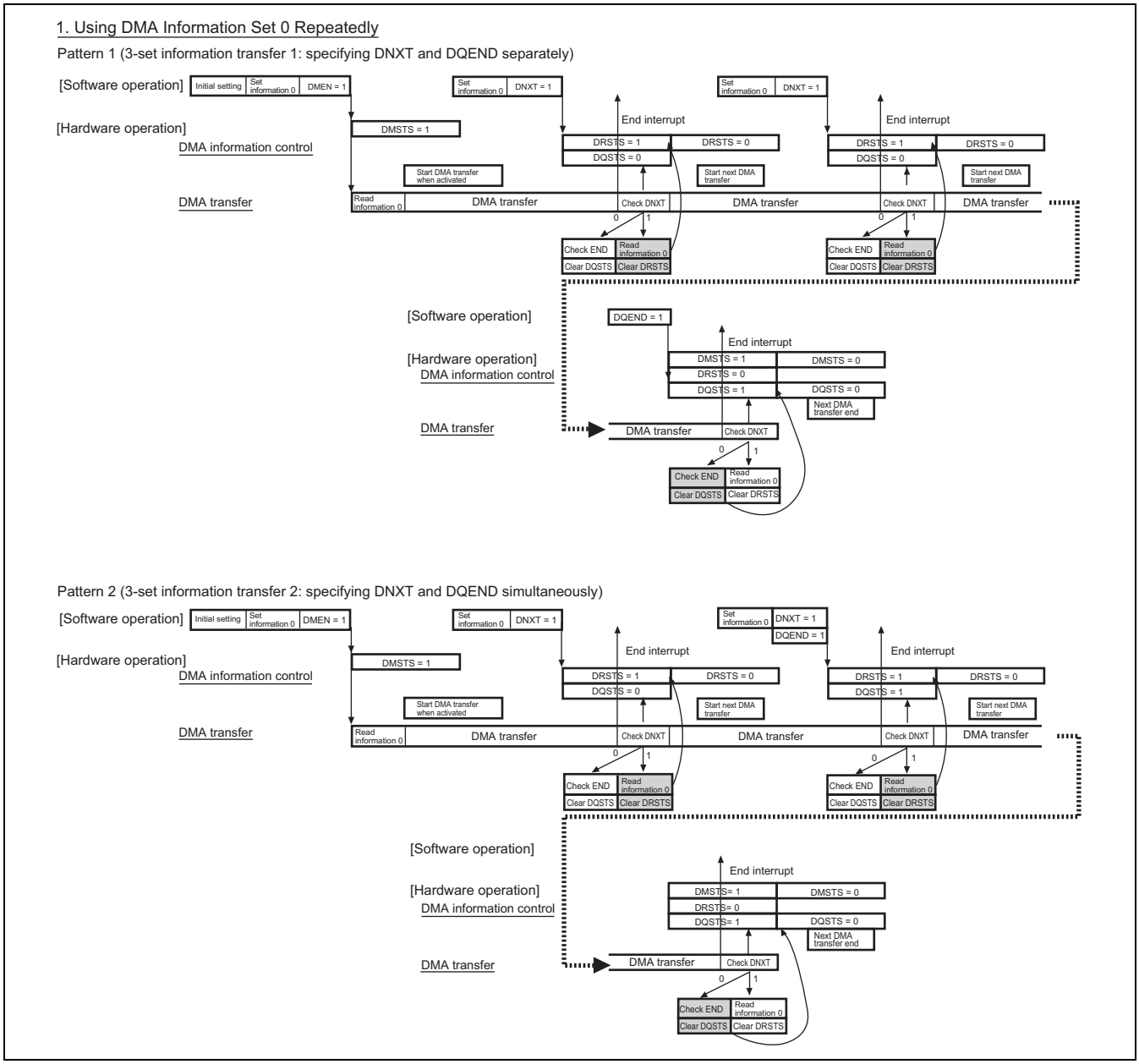


Figure 17.4 Transfer Using DMA Information Set 0 Repeatedly (1)

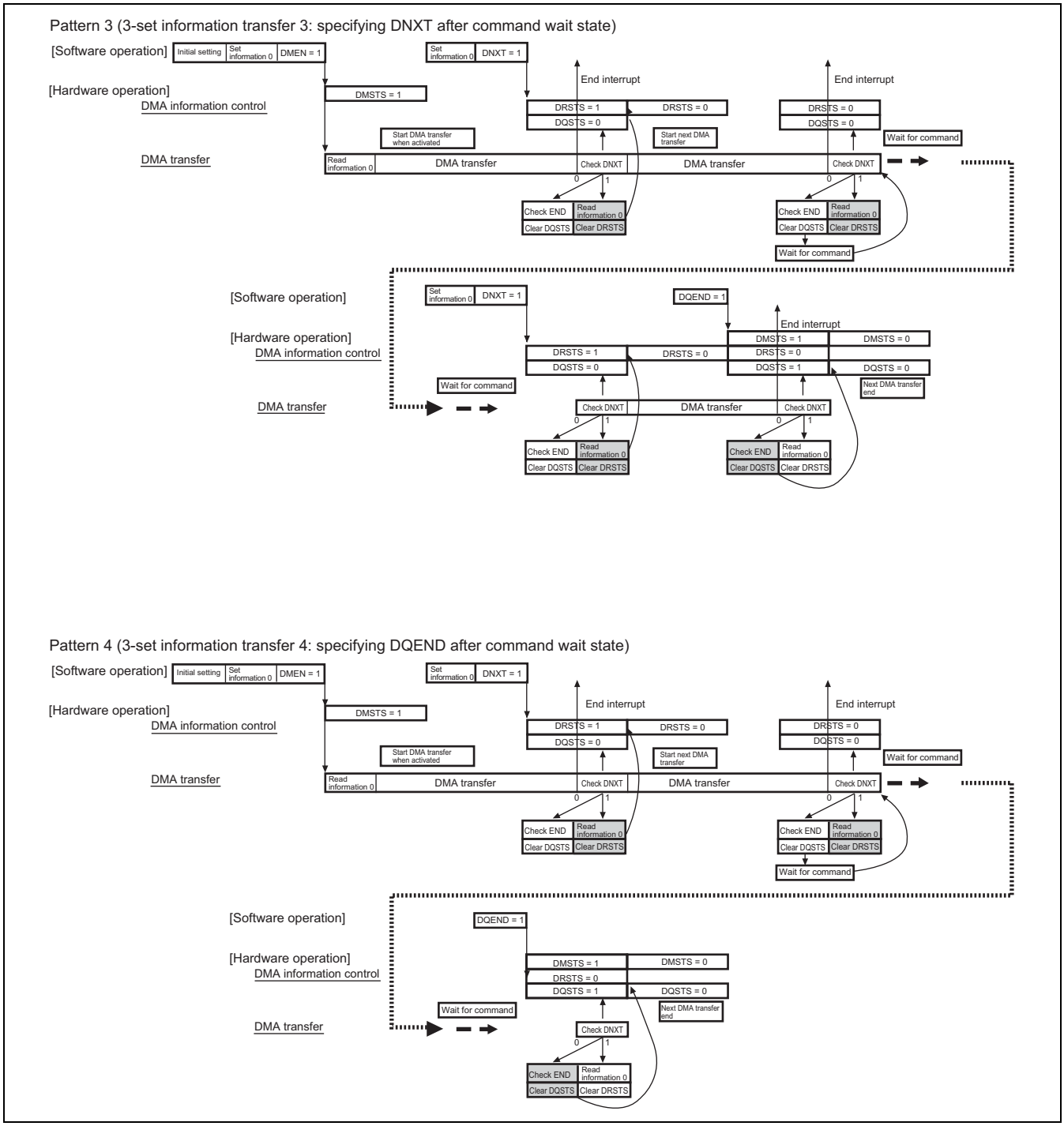


Figure 17.5 Using DMA Information Set 0 Repeatedly (2)

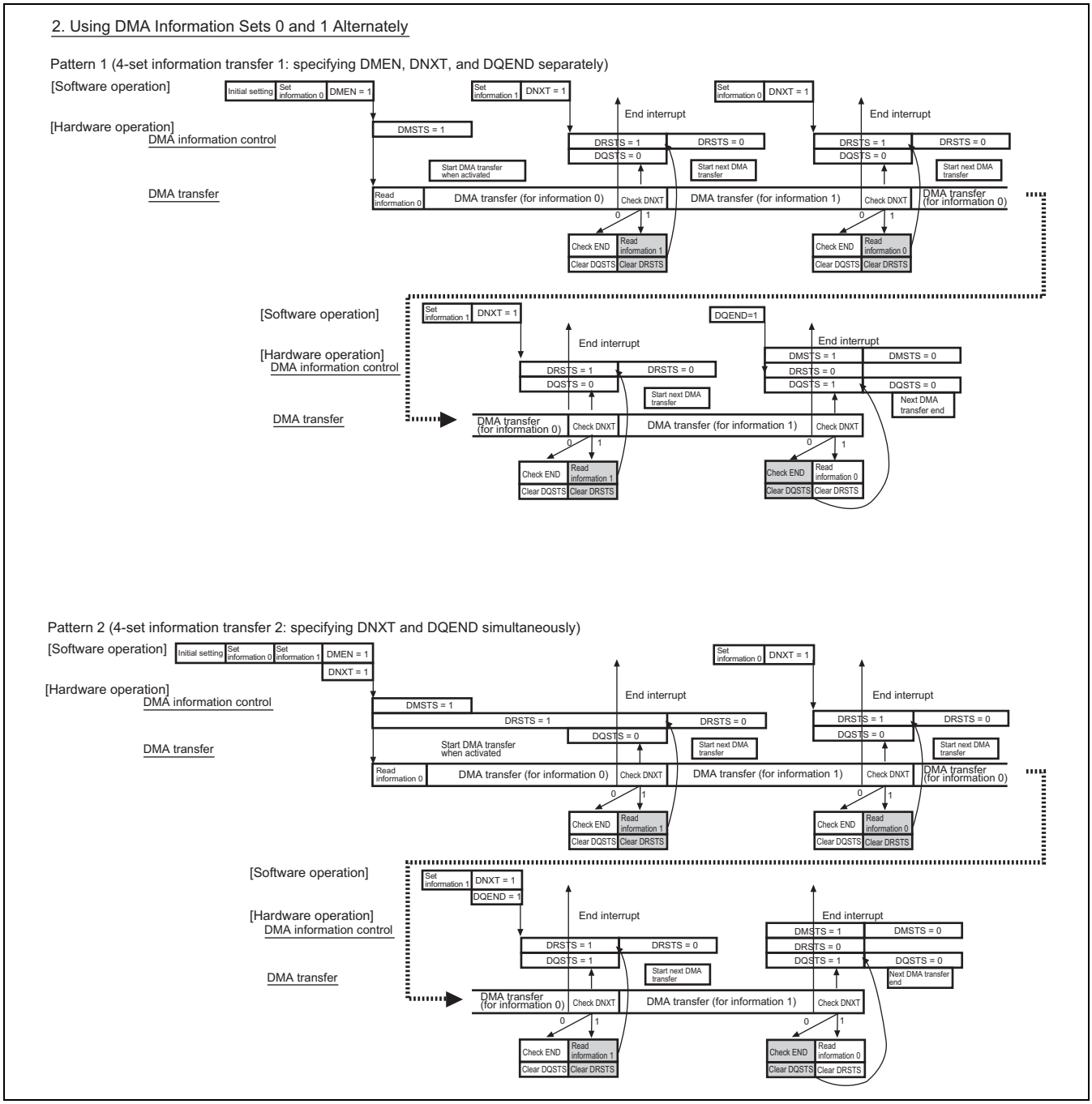


Figure 17.6 Using DMA Information Sets 0 and 1 Alternately (1)

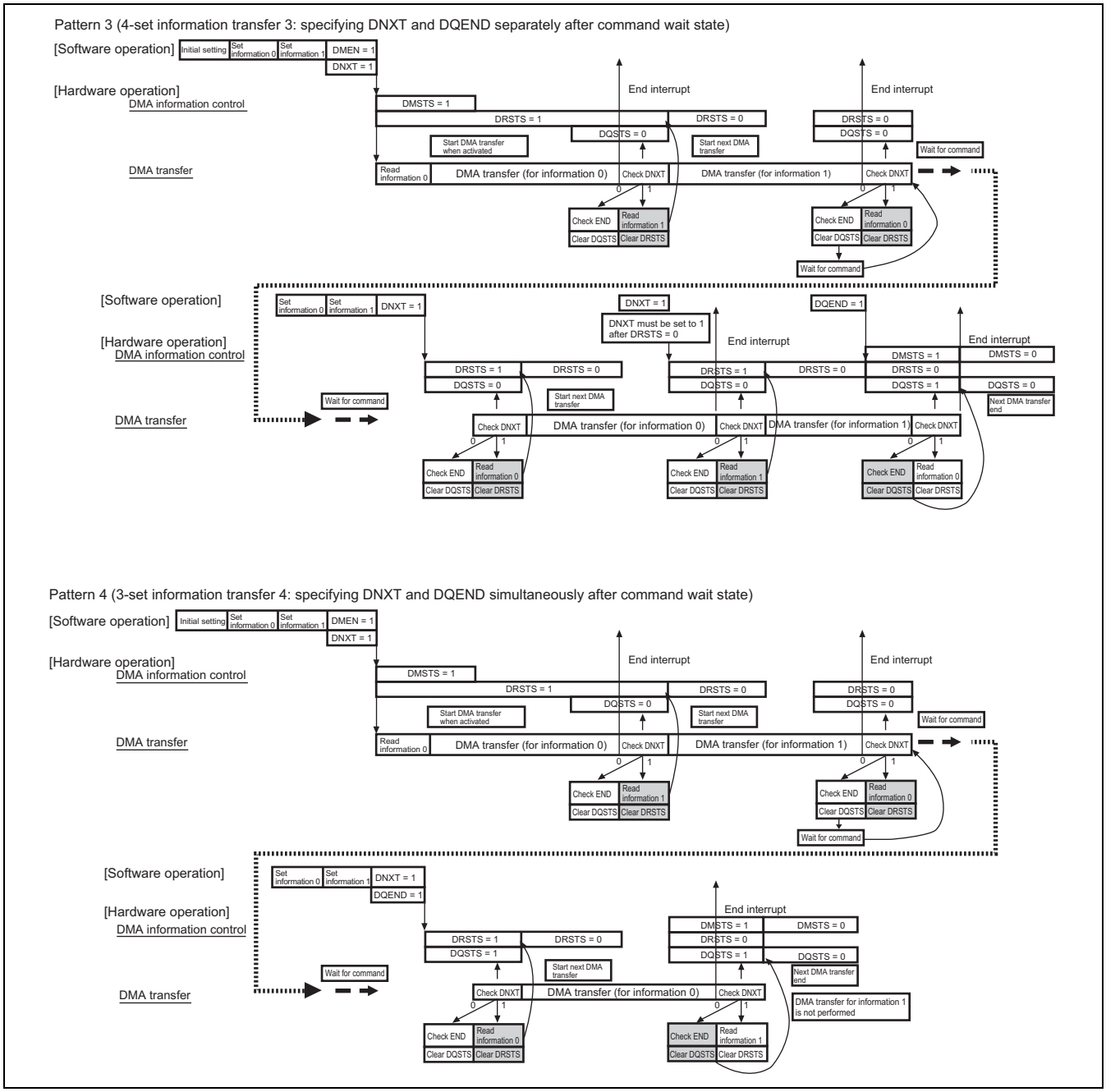


Figure 17.7 Using DMA Information Sets 0 and 1 Alternately (2)

17.5.3 Packing Data Read from Peripheral or External Module

Writing 1 to the PKMD bit when making necessary settings in the DMA control register (DCR) in the usual DMA activation procedure enables packing of data read from a peripheral or external module and then writing the data to memory (the AXI bus). Packing size can be specified to either 4 bytes or byte units shown in * in the DCR register description by the SWMD bit in DCR. However, when the transfer destination on the AXI side is memory (DDR-DRAM), packing size in a byte unit shown in * in the DCR register description is recommended in order to use memory and the AXI efficiently. The data packing of an access size when SWMD in DCR = 0 cannot be specified for the LBSC-DMAC (for details on access size in each channel, see * in the DCR register description), because size of data written from peripheral modules connected to the APB to registers is equal to or less than 4 bytes when the transfer destination on the AXI side is one of the units connected to the APB.

During the packing operation, even if the DMAC holds data less than the specified packing size when the DMAC completes the specified count of transfer, the DMAC writes fetched data to memory and indicates the end of DMA transfer by setting the DTEn bit in the DMA transfer end interrupt status register (DINTSR). If the peripheral or external module completes a DMA request before the specified transfer count is reached, DMA transfer can be terminated by writing 1 to the BDOUT bit in the DMA command register (DCMDR). In this case, if data which is being packed remains in the DMAC, the DMAC writes the data to memory (AXI). The DTE[n] bit in the DMA transfer end interrupt status register (DINTSR) is set and a transfer end interrupt is generated. Note that zero padding does not occur during write to memory. If no data remains in the DMAC, the DMAC terminates DMA transfer without accessing memory and generates a transfer end interrupt in the same way as when data remains in the DMAC.

When transfer is terminated by the BDOUT bit setting in continuous transfer mode, the DMAC transfers the next DMA information if the next DMA information transfer is requested through the DNXT bit in DCMDR, and then terminates DMA transfer in the continuous transfer mode termination procedure. In this mode, DMA requests (DREQ) from peripheral or external modules are masked (not accepted) before a transfer end interrupt occurs after the BDOUT bit is set to 1.

17.5.4 Limitations on Packing of Data Read from Peripheral or External Module

The transfer count is specified in DMA transfer count registers 0 and 1 (DTCR0 and DTCR1) in the DMAC.

If DMA transfer from a peripheral or external module is completed before the specified transfer count is reached, the DMAC cannot distinguish whether data is being transferred or the transfer has been completed, and data of less than packing size may remain in the DMAC internal buffer. When the size of remaining data is the same as the specified packing size, the data is transferred to memory.

Data remaining in the DMAC internal buffer is written to memory through a forced write executed by setting the BDOUT bit in the DMA command register (DCMDR). (Zero padding does not occur because the transfer destination is memory. For example, if 3-byte data remains in the DMAC un-transferred to memory, the 3-byte data is written to the memory as is.)

A forced write can be triggered by a communication completion interrupt from a peripheral or external module. Note that whether DMA transfer from the peripheral or external module is completed when the communication end interrupt occurs depends on the specifications of the peripheral or external module. Accordingly, check the specifications of the module before executing a forced write.

17.5.5 Notification of the End of DMA Transfer

The DMAC notifies the CPU of the end of transfer by outputting transfer end interrupt signal (a level signal) through INTC (SYS) when transfer is completed for the transfer count specified in DMA transfer information in single transfer mode. In continuous transfer mode, the DMAC outputs transfer end interrupt signal every time transfer is completed for the transfer count specified in one DMA transfer information set.

The transfer end interrupt signal is controlled according to the setting in the DMA transfer end interrupt enable register (DINTMR). Writing 1 to the DMA transfer end interrupt status clear register (DINTCR) clears the transfer end interrupt signal.

17.5.6 DMA Transfer Stop, and Resume Procedures

This section describes the procedures for stopping, and resuming DMA transfer.

- To stop (cancel) DMA transfer during operation

Step	Overview	Register Operation	Operation after Register Write
1 ↓	Specify forced termination for DMAC.	Write 1 to DMSTP of DSTPR in DMAC.	The DMAC stops DMA transfer as soon as the current DMA bus cycle is completed, and then enters the idle state. Unfinished transfer data remaining in the buffer is discarded. The registers retain the values. No end interrupt is issued.
2 ↓	Check that the DMAC has entered the idle state.	If DMSTS of DSTSR in DMAC is 0, the DMAC is in the idle state.	—
3	Specify forced termination for external devices.	(Depends on the external devices.)	The external devices stop sending DMA requests.

Note: Step 2 can be done after step 3.

- To temporarily stop (pause) DMA transfer during operation and then resume it

Step	Overview	Register Operation	Operation after Register Write
1 ↓	Specify temporary stop for DMAC.	Write 1 to DMSPD of DCMDR in DMAC.	The DMAC temporarily stops DMA transfer as soon as the current DMA bus cycle is completed. The DMAC retains its internal status, including unfinished transfer data remaining in the buffer, without change.
2 ↓	Check that the DMAC has entered the temporary stop state.	If DMSPS of DSTSR in DMAC is 1, the DMAC is in the suspended state.	—
3 ↓	A certain period of time has elapsed (the LBSC may detect a DREQ signal from an external device during this period, but the DMAC keeps the temporary stop and the external devices continue to wait for DMA transfer).		
4	Specify cancel of temporary stop (resume transfer).	Write 1 to DMSPC of DCMDR in DMAC.	The paused state is canceled, and the DMAC resumes its operation with the DMA transfer for the DREQ detected by the LBSC.

Note: Step 2 can be done between steps 3 and 4.

- To temporarily stop (pause) DMA transfer during operation and then terminate (cancel) operation

Step	Overview	Register Operation	Operation after Register Write
1 ↓	Specify temporary stop for DMAC.	Write 1 to DMSPD of DCMDR in DMAC.	The DMAC temporarily stops DMA transfer as soon as the current DMA bus cycle is completed. The DMAC retains its internal status, including unfinished transfer data remaining in the buffer, without change.
2 ↓	Check that the DMAC has entered the temporary stop state.	If DMSPS of DSTSR in DMAC is 1, the DMAC is in the suspended state.	—
3 ↓	A certain period of time has elapsed (the LBSC may detect a DREQ signal from an external device during this period, but the DMAC keeps the temporary stop and the external devices continue to wait for DMA transfer).		
4 ↓	Specify forced termination for DMAC.	Write 1 to DMSTP of DSTPR in DMAC.	The DMAC exits the temporary stop state and enters the idle state. Unfinished transfer data remaining in the buffer is discarded. The registers retain the values. No end interrupt is issued.
5 ↓	Check that the DMAC has entered the idle state.	If DMSTS of DSTSR in DMAC is 0, the DMAC is in the idle state.	—
6	Specify forced termination for external devices.	(Depends on the external devices.)	The external devices stop sending DMA requests.

Notes: 1. Step 2 can be done between steps 3 and 4.
2. Step 5 can be done after step 6.

17.5.7 Data Alignment in AXI Bus Interface

The AXI bus is always accessed through a handshake using an access request and a request acknowledge. Alignment of data read or written during the access to memory through the AXI bus is always converted.

When the DTAMD bit in the DMA control register (DCR) is 0, the AXI bus data alignment is converted according to the endian mode signal (DMAC input signal: little) and the peripheral data bus width (the SPDS1 and SPDS0 bits or DPDS1 and DPDS0 bits in DCR). When the DTAMD bit in DCR is 1, data alignment is converted according to the DTAC, DTAU, and DTAU1 bit settings in DCR.

The following table shows the AXI bus data alignment control according to the DTAMD bit in DCR, endian mode signal (DMAC input signal: little), peripheral data bus width (the SPDS1 and SPDS0 bits or DPDS1 and DPDS0 bits in DCR), and DTAC, DTAU, and DTAU1 bits in DCR.

Table 17.2 Data Alignment Control According to Bit and Signal Settings

No.	DTAMD	little (MD[8])	PDS [1:0]	DTAC	DTAU	DTAU1	Data Alignment of 4 Bytes	Unit for 4-Byte Data Alignment	8-Byte Data Alignment in 4-Byte Unit	Conversion Pattern	Remarks
1	0	0	00 (8 bits)	*	*	*	Not controlled	8 bits	Not controlled	CP1 (3)	Standard conversion (Software must specify only PDS[1:0])
2	0	0	01 (16 bits)	*	*	*	Not controlled	16 bits	Not controlled	CP2 (3)	
3	0	0	10 (32 bits)	*	*	*	Not controlled	8 bits	Not controlled	CP3 (2)	
4	0	1	00 (8 bits)	*	*	*	Controlled	8 bits	Controlled	CP1 (1)	
5	0	1	01 (16 bits)	*	*	*	Controlled	16 bits	Controlled	CP2 (1)	
6	0	1	10 (32 bits)	*	*	*	Not controlled	8 bits	Controlled	CP3 (1)	
7	1	*	*	0	0	0	Not controlled	8 bits	Not controlled	CP1 (3)	Special conversion (Software must specify the alignment mode)
8	1	*	*	0	0	1	Not controlled	8 bits	Controlled	CP3 (1)	
9	1	*	*	0	1	0	Not controlled	16 bits	Not controlled	CP2 (3)	
10	1	*	*	0	1	1	Not controlled	16 bits	Controlled	CP3 (1)	
11	1	*	*	1	0	0	Controlled	8 bits	Not controlled	CP1 (2)	
12	1	*	*	1	0	1	Controlled	8 bits	Controlled	CP1 (1)	
13	1	*	*	1	1	0	Controlled	16 bits	Not controlled	CP2 (2)	
14	1	*	*	1	1	1	Controlled	16 bits	Controlled	CP2 (1)	

*: Don't care

The following shows data alignment conversion in the DMAC. Conversion pattern numbers in the table above correspond to the conversion numbers below.

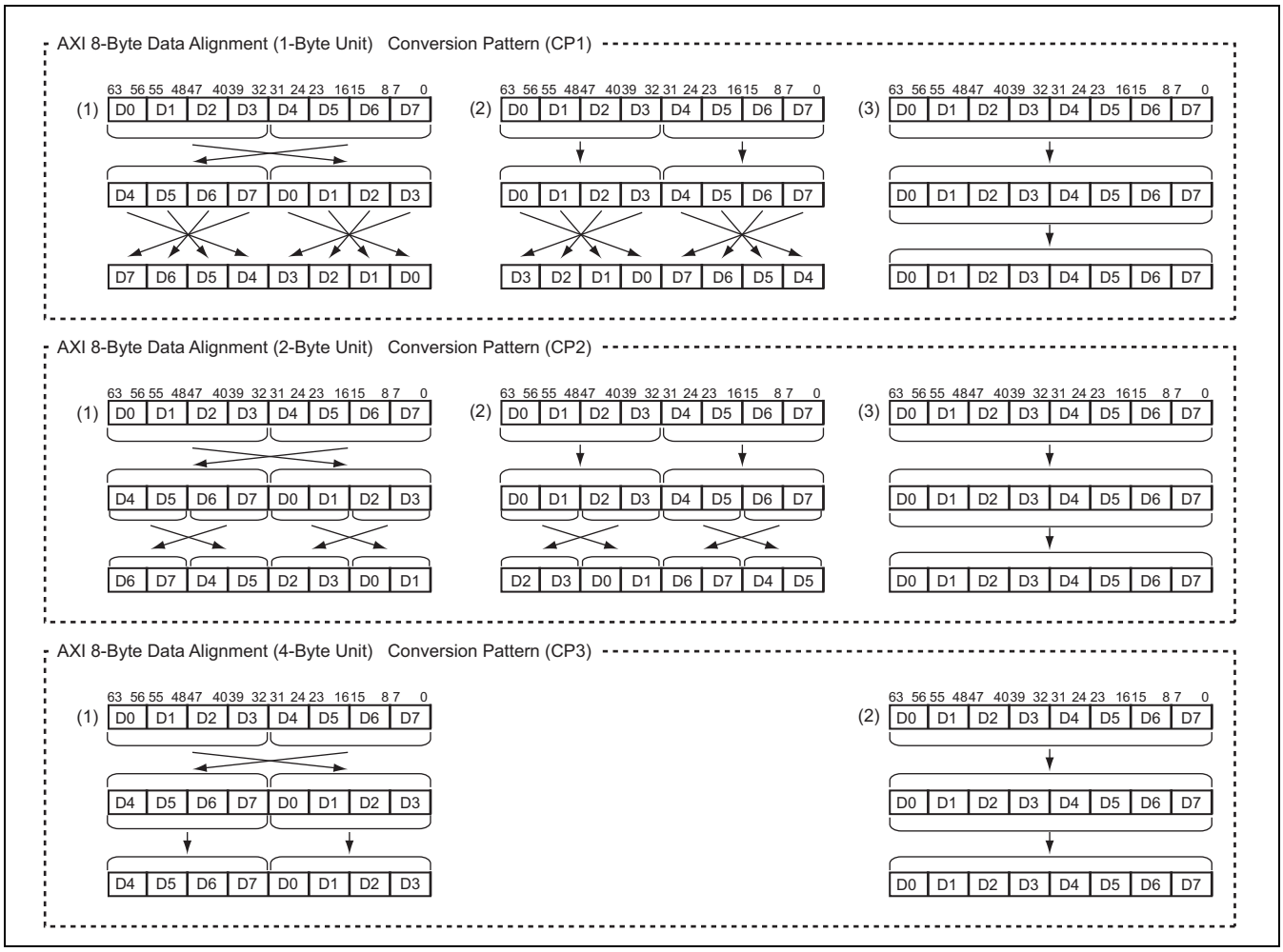


Figure 17.8 Data Alignment Conversion in the DMAC

17.5.8 Data Alignment in EX-BUS Interface

Setting the DMALGR register in the DMAC allows variable alignment mode for the external bus access as the mode of alignment conversion. For the CPU operation in a variable alignment mode, see section 14.7.3 (1), Data Alignment during LBSC-DMAC Access, in section 14, LBSC within Bus Bridge.

17.5.9 Timing Charts

Timing charts are given for DMA operation during the external SRAM bus operation. In the timing charts, the DREQ, DRACK, and DACK signal polarity is indicated as negative; however, these polarity settings, assertion of either the CS# or DACK signal, and switching DREQ to a level signal or to edge detection mode, can be set. In all cases these settings should be made using LBSC internal registers.

(1) EX-BUS DMA single-read/write operation

In SRAM bus operation, upon receiving a DREQ signal a DRACK is asserted to send notification of detection of a DMA request. There are no DRACK signals for other than LBSC-DMAC channel 0. In these cases, the device which is the DMA request source must negate the DREQ signal until the end of the bus operation through the DACK signal indicating that the DMA transfer has actually started. The DMAC starts the next DREQ sampling from the next clock cycle after the end of the DMA bus transfer (LBSC-DMAC DMA request mask control register (DRMSKR) settings can be used to delay the start of the next sampling), and upon detection, starts the next DMA transfer bus operation.

In DMA single read and write operations, the number of clock cycles from CS# assertion to RD# (or WE#) signal assertion, the number of RD# (or WE#) pulse clock cycles, and the number of clock cycles from RD# (or WE#) negation to CS# negation, can be set through the LBSC internal register. During the period of RD# (or WE#) assertion, if a WAIT signal from the DMA request source is detected, then during the WAIT assertion period, the RD# (or WE#) pulse width is extended. With respect to specification of WAIT signal sampling also, the internal LBSC register should be used.

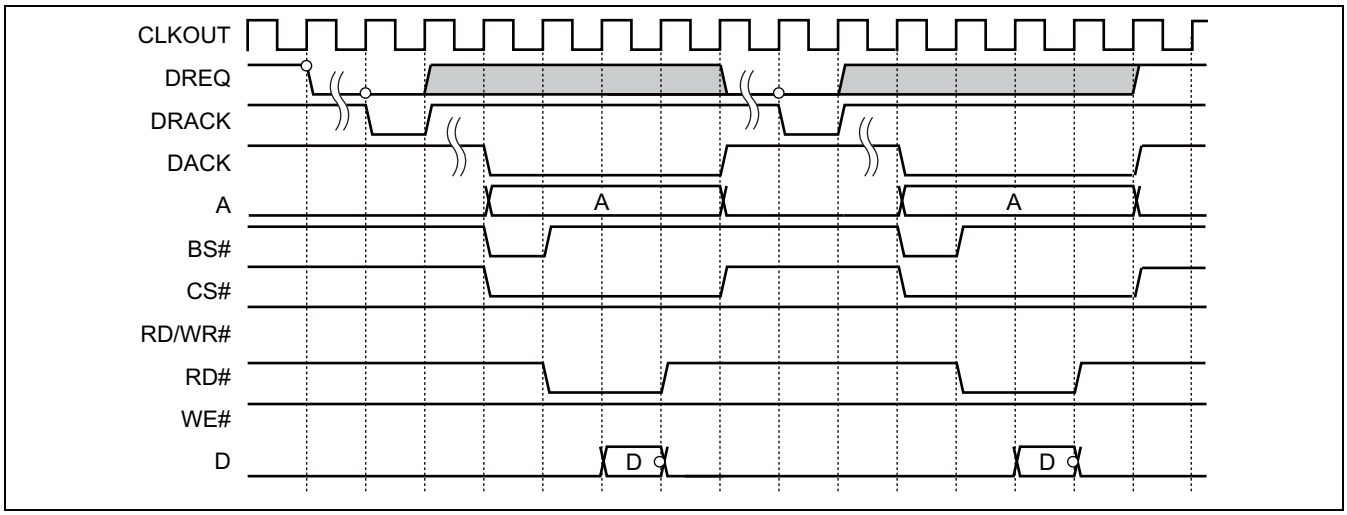


Figure 17.9 External Bus DMA Read Operation (SRAM Bus Single Read)

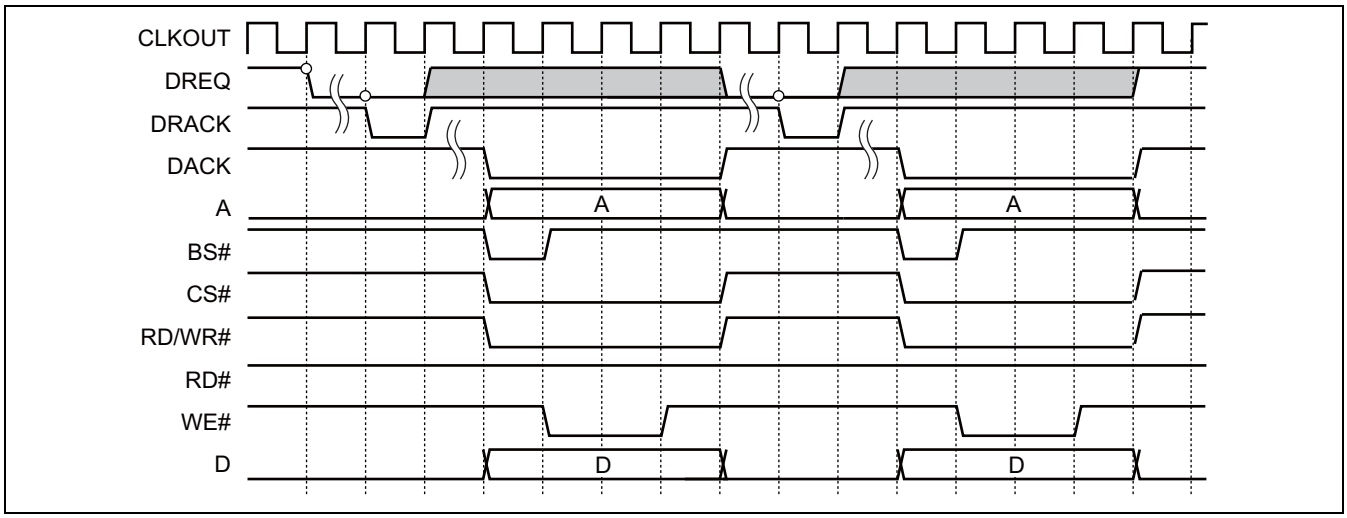


Figure 17.10 External Bus DMA Write Operation (SRAM Bus Single Write)

(2) EX-BUS DMA 8-burst read/write operation

In DMA 8-burst operation, 8-burst bus transfer operation is performed upon detection of a single DREQ signal. In SRAM bus operation, upon receiving a DREQ signal a DRACK is asserted to send notification of detection of a DMA request. There are no DRACK signals for other than LBSC-DMAC channel 0, so that in these cases the device which is the DMA request source must negate the DREQ signal until the end of the 8-burst bus operation through the DACK signal indicating that the DMA transfer has actually started. The DMAC starts the next DREQ sampling from the next clock cycle after the end of the DMA bus operation (LBSC-DMAC DMA request mask control register (DRMSKR) settings can be used to delay the start of the next sampling), and upon detection, starts 8-burst bus operation for the next DMA transfer.

Also in DMA 8-burst operations, the number of clock cycles from CS# assertion to RD# (or WE#) signal assertion, the number of RD# (or WE#) pulse clock cycles, and the number of clock cycles from RD# (or WE#) negation to CS# negation, can be set through the LBSC internal register. During the period of RD# (or WE#) assertion, if a WAIT signal from the DMA request source is detected, then during the WAIT assertion period, the RD# (or WE#) pulse width can be extended. With respect to WAIT signal control also, the internal LBSC register should be used.

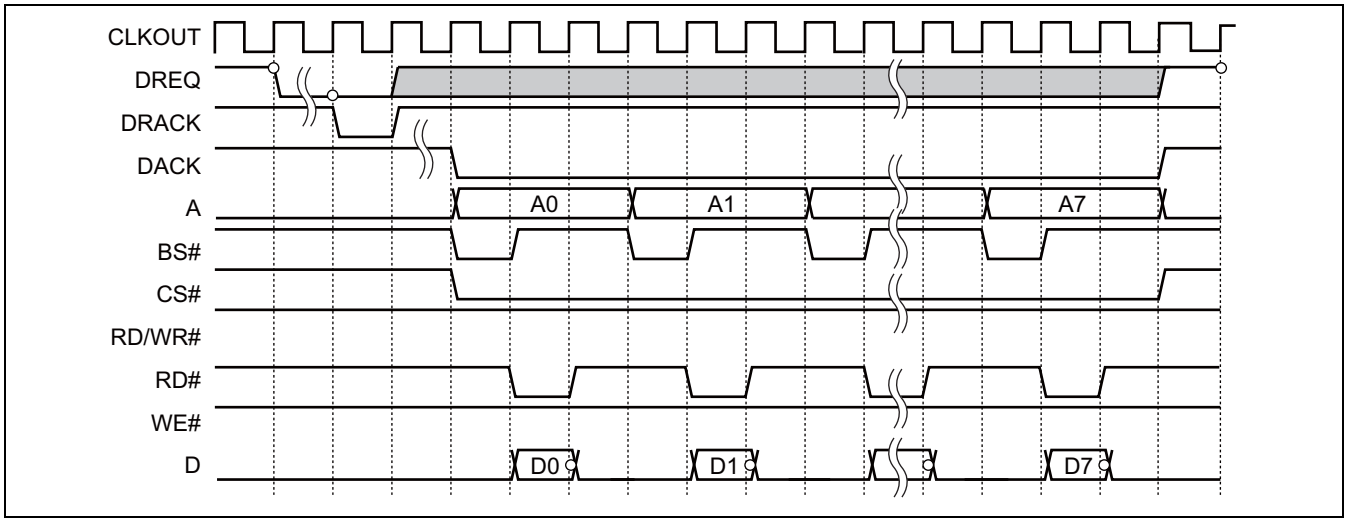


Figure 17.11 External Bus DMA Read Operation (SRAM Bus Burst Read)

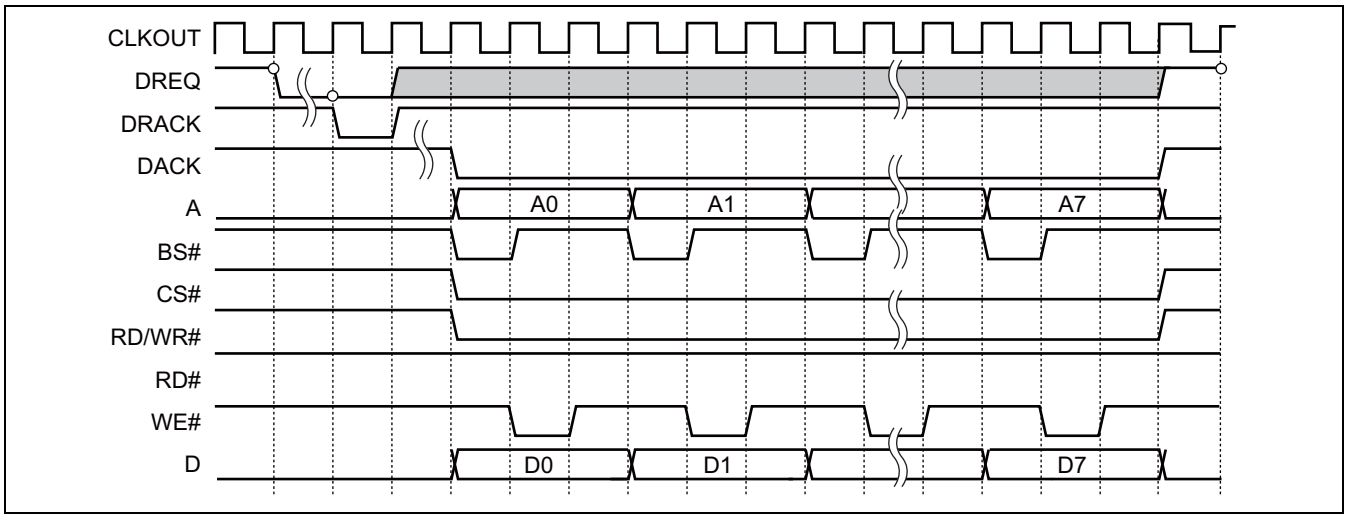


Figure 17.12 External Bus DMA Write Operation (SRAM Bus Burst Write)

18. Booting

18.1 Overview

In this product, the levels on the MD7 and MD6 pins can be set to select the master boot processor. When the Cortex-A7 is selected as the master boot processor, the levels on the MD[3:1] pins can select booting up from the serial flash ROM connected to the QSPI or from devices connected to the eMMC.

18.2 Features

- The levels on the MD7 and MD6 pins can select the Cortex-A7 as the master boot processor.
- The external boot device can be selected as either external ROM (area 0) or on-chip ROM by the levels on the MD3 to MD1 pins.

- Booting from the serial flash ROM connected to the QSPI is supported.
  - The master boot processor (if this is the Cortex-A7) executes the instructions in the on-chip ROM, and the specified amount of data are transferred from the serial flash ROM to the on-chip RAM at the specified QSPI clock frequency. After transfer, execution jumps to the top address of the on-chip RAM.
  - After 16 or 4 Kbytes of code are transferred to the on-chip RAM at 39 MHz, execution jumps to the top address of the on-chip RAM.
  - After 16 Kbytes of code are transferred to the on-chip RAM at 48.75 MHz, execution jumps to the top address of the on-chip RAM.

- Booting from the eMMC device connected to the MMC0 (SDHI1) is supported.
  - The master boot processor (if this is the Cortex-A7) executes the instructions in the on-chip ROM, and the specified amount of data are transferred from the eMMC device to the on-chip RAM at the specified MMC clock frequency. After transfer, execution jumps to the top address of the on-chip RAM.
  - After 16 Kbytes of code are transferred to the on-chip RAM, execution jumps to the top address of the on-chip RAM.

18.3 Input/Output Pins

Table 18.1 Mode Pin Configuration

Name	Pin Name	I/O	Function
Mode pin	MD7 and MD6	Input	Select a master boot processor.

MD7	MD6	Description
0	0	Setting prohibited
0	1	Booted through CPU0 in Cortex-A7
1	0	Reserved
1	1	Setting prohibited

Name	Pin Name	I/O	Function
Mode pin	MD3 to MD1	Input	Select a boot device.

MD3	MD2	MD1	Description
0	0	0	External ROM boot (area 0)
0	0	1	eMMC boot via SDHI1; 16 Kbytes transferred.
0	1	0	Serial flash ROM boot via QSPI; 16 Kbytes transferred at 48.75 MHz
0	1	1	Reserved
1	0	0	Serial flash ROM boot via QSPI; 16 Kbytes transferred at 39 MHz
1	0	1	Reserved
1	1	0	Serial flash ROM boot via QSPI; 4 Kbytes transferred at 39 MHz
1	1	1	Reserved

18.4 Operation

18.4.1 Booting Up

Figure 18.1 shows the flow of booting up.

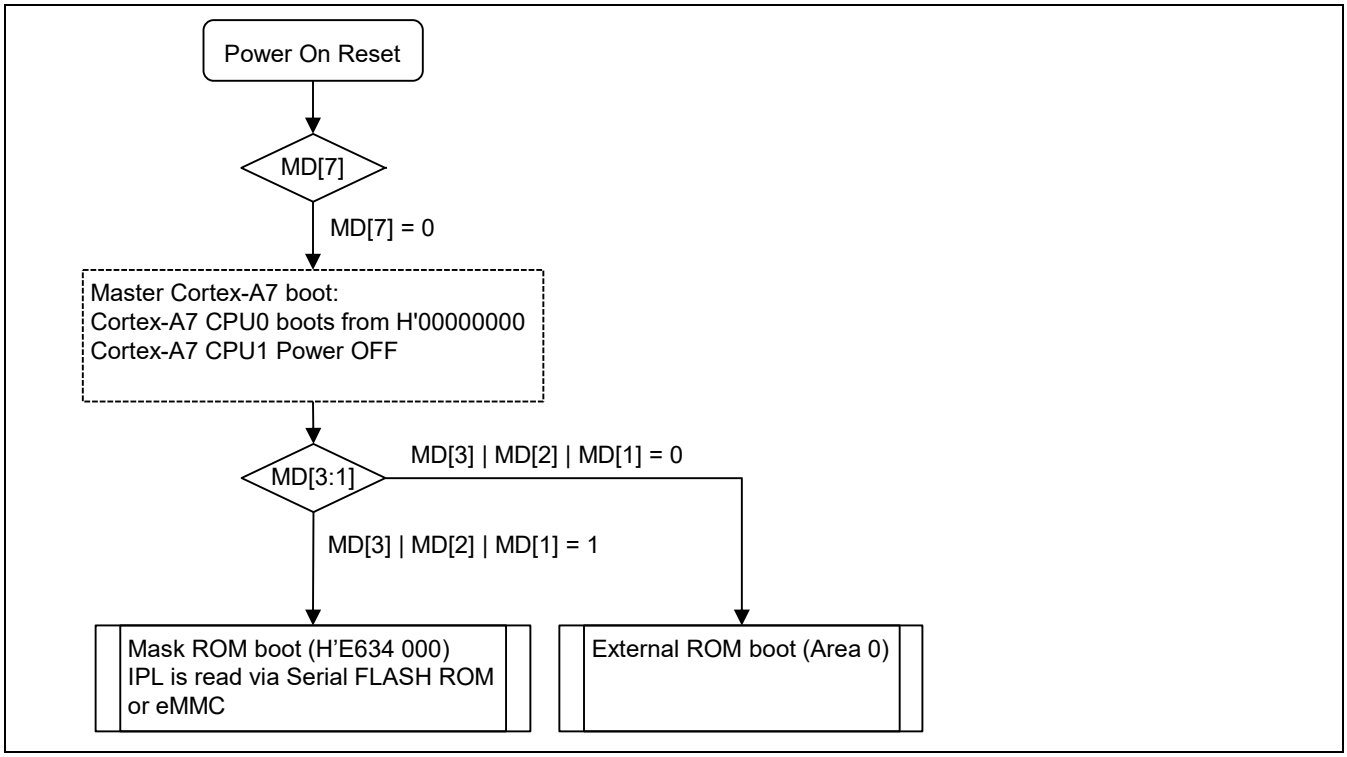


Figure 18.1 Flow of Booting Up

18.5 Serial Flash ROM Boot

18.5.1 Serial Flash ROM Boot [QSPI]

In QSPI boot, the boot program in the on-chip ROM starts up the QSPI and SYS-DMAC channel 1, and transfers the loader program previously stored in the serial flash ROM to the on-chip RAM via the QSPI module. Here, the QSPI module reads the serial flash ROM with the fast read mode. After loader program is transferred, the program automatically jumps to the top address of the loader program. The amount of data to be transferred and QSPI IF frequency depend on the MD[3:1] pin setting. Controlling the device-specific quad serial flash ROM through the loader program enables reduction of program load time after loader program transfer.

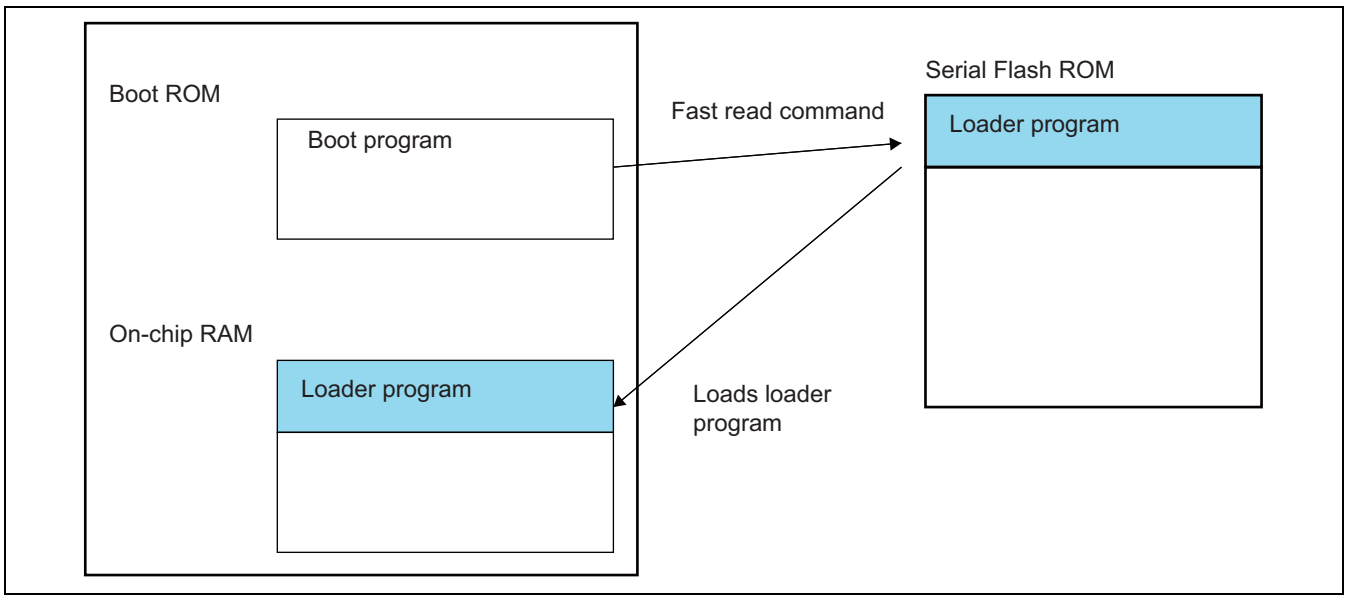


Figure 18.2 Address Space in Serial Flash Memory Boot Mode

18.5.2 Usage of QSPI Pins

Table 18.2 QSPI Pin Configuration

Name	Pin Name	Function Name	I/O	Function
Serial clock	QSPI0_SPCLK	SPCLK	Output	Outputs serial clock.
Transmit data	QSPI0_MOSI_IO0	MOSI	Output	Outputs transmit data.
Receive data	QSPI0_MISO_IO1	MISO	Input	Inputs receive data.
Chip select	QSPI0_SSL	SSL	Output	Outputs chip select signal. To be set to active low using boot ROM code

Note: IO2 (QSPI0_IO2) and IO3 (QSPI0_IO3) pins are set in High level by the boot program in the on-chip ROM.

18.5.3 Serial Flash ROM Boot Flow

Figure 18.3 shows the serial flash ROM boot flow by the on-chip ROM boot program.

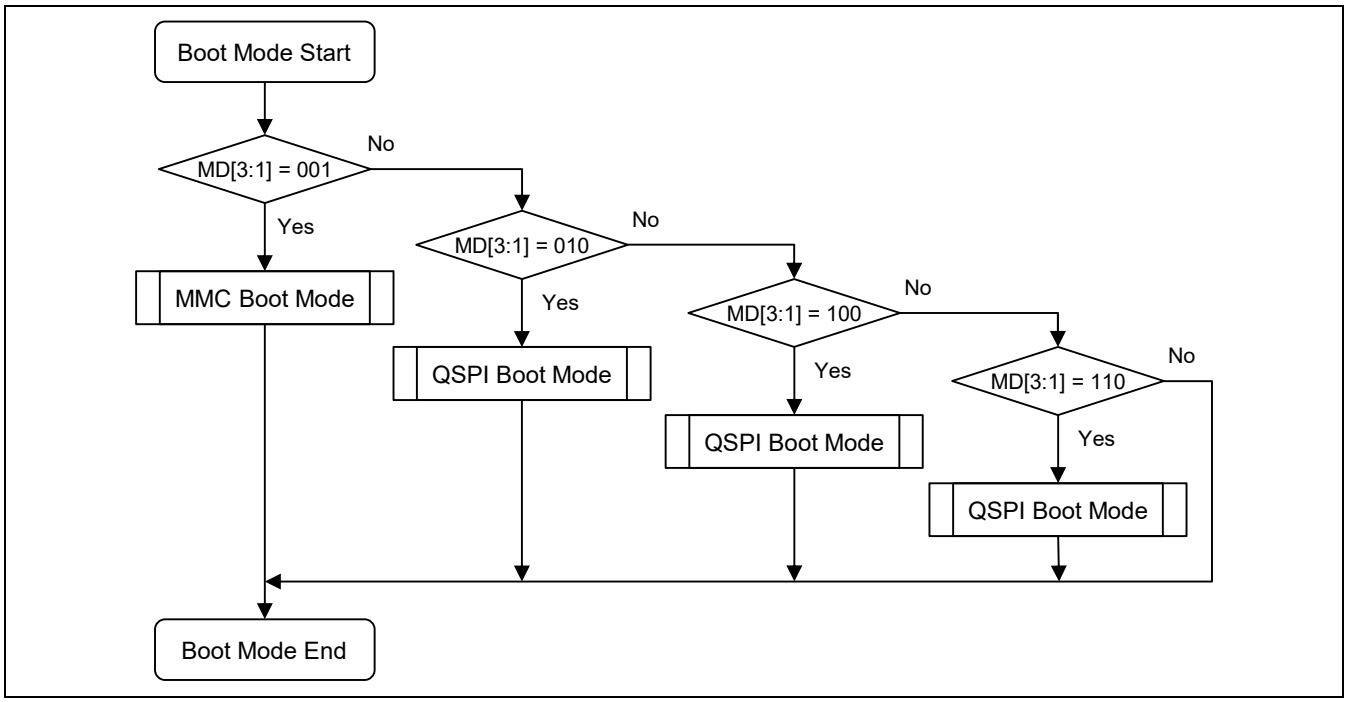


Figure 18.3 Serial Flash ROM Boot Flow by the On-chip ROM Boot Program

18.5.4 Note

The boot ROM program does not issue a reset command or mode bit reset command to the serial flash ROM; using a serial flash ROM with a reset pin is recommended.

18.6 eMMC Boot

18.6.1 Features

This LSI has three SD card interfaces (SDHI0 to SDHI2), one of which can also be used as MMC interfaces (SDHI1).

In eMMC Boot, this LSI would execute eMMC Boot operation using SDHI1.

18.6.2 Usage of SDHI1(MMC) Pins

Table 18.3 eMMC Pin Configuration

Name	Pin Name	Function Name	I/O	Function
Clock	MMC0_CLK	CLK	Output	Output clock
Command	MMC0_CMD	CMD	Input/Output	eMMC command data
DATA[7]	MMC0_D7	DATA[7]	Input/Output	eMMC data
DATA[6]	MMC0_D6	DATA[6]	Input/Output	eMMC data
DATA[5]	MMC0_D5	DATA[6]	Input/Output	eMMC data
DATA[4]	MMC0_D4	DATA[4]	Input/Output	eMMC data
DATA[3]	MMC0_D3	DATA[3]	Input/Output	eMMC data
DATA[2]	MMC0_D2	DATA[2]	Input/Output	eMMC data
DATA[1]	MMC0_D1	DATA[1]	Input/Output	eMMC data
DATA[0]	MMC0_D0	DATA[0]	Input/Output	eMMC data

18.6.3 Boot operation

Cortex-A7 master boot processor executes the instructions in the on-chip ROM, and 16K byte data are transferred from eMMC to the on-chip RAM. After transfer, the program jumps to the top address of loader program of the on-chip RAM.

Note: A Loader program of eMMC boot has no offset address. (H'00000000)

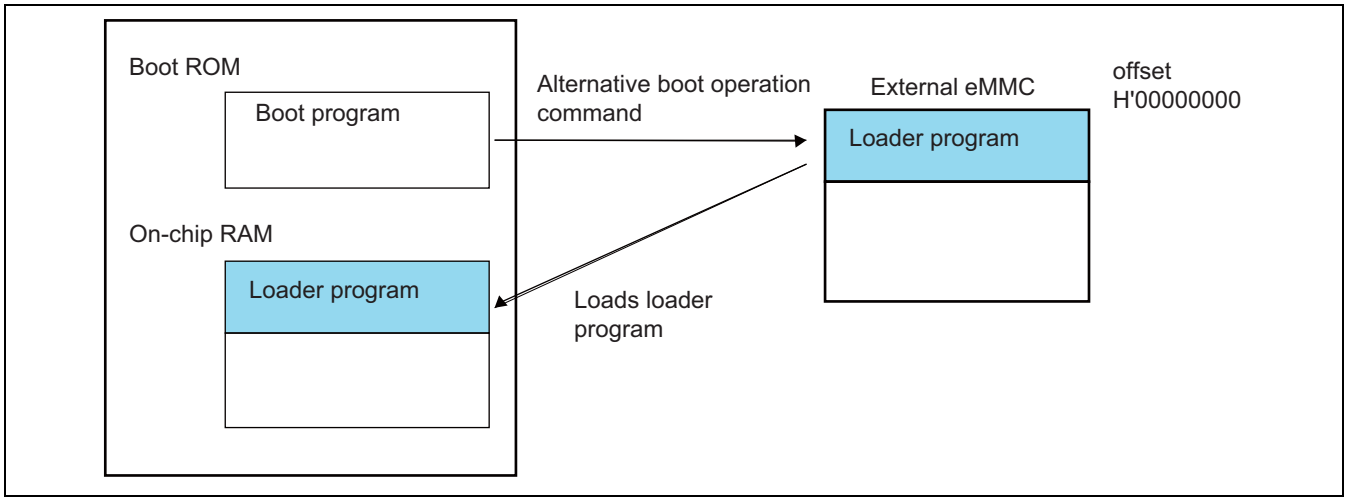


Figure 18.4 Address Space in eMMC Boot Mode

Data transfer specification in eMMC boot with Boot mode is the followings.

- eMMC 4.41 (JESD84-A441) standard
- Alternative boot operation
- Use Boot partition 1 or 2
- MMC0_CLK 48.75 MHz
- 8-bit bus width

Also, the eMMC device needs to meet the following conditions (a) and (b).

(a) BOOT_PARTITION_ENABLE in PARTITION_CONFIG of EXT_CSD must be set to H'1 or H'2.

(b) BOOT_BUS_WIDTH of EXT_CSD must be set to H'2 (8-bit bus). And BOOT_MODE of EXT_CSD must be set to H'1 (0x1: Use single data rate + high speed timings in boot operation mode).

18.7 Boot Program in On-Chip ROM

The on-chip ROM contains the program to control QSPI and eMMC as the standard boot ROM program. Modifying the ROM code enables booting through another peripheral module.

19. 3D Graphics Engine

19.1 Overview

This section only introduces the features of SGX531. The graphics processing performed by graphics engine is provided as the graphics driver software.

19.2 PowerVR Series5 SGX531

The description of this section is quoted from ‘POWERVR SGX Series5 Factsheet’.

(PowerVR_SGX_Series5_IP_Core_Family_[3.4].pdf, available at www.imgtec.com).

19.2.1 Features of POWERVR SGX Series5

The POWERVR SGX Series5 GPU IP core family is a series of highly efficient graphics acceleration IP cores that meet the multimedia requirements of the next generation of consumer, communications and computing applications.

POWERVR SGX Series5 architecture is fully scalable for a wide range of area and performance requirements, enabling it to target markets from low cost feature-rich mobile multimedia products to very high performance consoles and computing devices.

The family incorporates the revolutionary Universal Scalable Shader Engine (USSE), with a feature set that exceeds the requirements of OpenGL 2.0 and Microsoft Shader Model 3, enabling 2D, 3D and general purpose (GP-GPU) processing in a single core.

- Most comprehensive IP core family and roadmap in the industry
- Series5 shader-driven tile-based deferred rendering (TBDR) architecture
- Fully programmable GPU using unique USSE architecture
- Support for all industry standard mobile and desktop graphics APIs and operating systems
- Fully backwards compatible with PowerVR MBX

19.2.2 Register Base Address

Base address of registers is allocated to H'FD80 0000.

20. Display Unit (DU)

20.1 Overview

20.1.1 Features

(1) Display Channel

Two independently controllable channels are provided. Using the DU0 and DU1, different images or the same image can be displayed on two monitors.

(2) Plane

The display surfaces normally called the foreground, background, and cursor, are called planes in this section. Parameters for each plane can be set independently through the settings of an internal register. The internal register settings can also be used to set the display priority order.

- Display size
- Display position
- Display data format (8-bit/pixel, 16-bit/pixel, 32-bit/pixel, ARGB, or YC)
- Plane superpositioning
- Scrolling
- Wrapping-around
- Blinking
- Buffering control

The internal register settings can be used to select four different control modes.

- Auto rendering mode (double buffering)
- Manual display change mode (double buffering)
- Auto display change mode (double buffering)
- Video capture mode (triple buffering)

(3) Type and Number of Planes

In the DU0 or DU1, there are eight planes (display planes) available, each using both image data and an alpha ratio. Also, there are two special planes (alpha-ratio planes) available, each using only an alpha ratio.

Up to eight display planes can be superposed on each other. Correspondences between the DU0 and DU1 planes are not fixed but can be selected as desired through register settings.

For the number of planes which can be used at the same time, refer to the description in section 1, Overview.

(4) Synchronization Method

Internal register settings can be used to select any of three synchronization modes for the display output timing.

- Master mode (internal sync mode)
- TV sync mode (external sync mode)
- Sync method switching mode

(5) CRT Scan Mode (CRT Scan Method)

Internal register settings can be used to select from among three scan modes.

- Non-interlaced mode
- Interlaced sync mode
- Interlaced sync & video mode

(6) YC → RGB Color Space Conversion Functions

Image data stored in YC format can be converted into the RGB color space and displayed in a window. The conversion coefficients can be set in a register.
However, data for two or more pixels cannot be converted into the RGB color space at the same time.
Data in YUV422 and YUV420 format are convertible into the RGB color space.

(7) RGB → YC Color Space Conversion Functions

Display data superposed in RGB format can be converted into the YC color space and output from either the DU0 pin or the DU1 pin as the YC data.

(8) Color Palette

Four internal color palette planes are provided, capable of simultaneously displaying 256 colors out of 262 thousand colors

Eight-bit blending ratios are provided for every 256 colors. The color palettes are only accessible by superposition processors 0

(9) Display Capture

The RGB-888 or RGB-666 data for output on the two display channels is convertible into ARGB-888 or RGB-565 or ARGB-1555 data for separate storage in external memory.

(10) Register Access Control

The module has internal control registers; these are writable/readable by the APB protocol over the APB. The unit of access is fixed to 32 bits.

(11) VSP1 Connection

Connection with the VSP1 allows the image data processed by the VSP1 to be output directly to the display unit without an external memory. VSP1 has been connected with plane1 for the DU0 or DU1.

(12) LVDS Connection

Connection with the LVDS allows the output of image data from the LVDS. Either the DU0 or the DU1 can be connected with the LVDS.

(13) DPAD Connection

Connection with the DPAD allows the output of the digital RGB data from a pin.

Connection with the DPAD allows the output of the digital RGB data from a pin separately for each channel.

(14) Digital video encoder Connection

Connection with the Digital video encoder allows the out put of the analog output composite signal. Ether the DU0 or the DU1 can be connected with the Digital video encoder.

20.1.2 Block Diagram

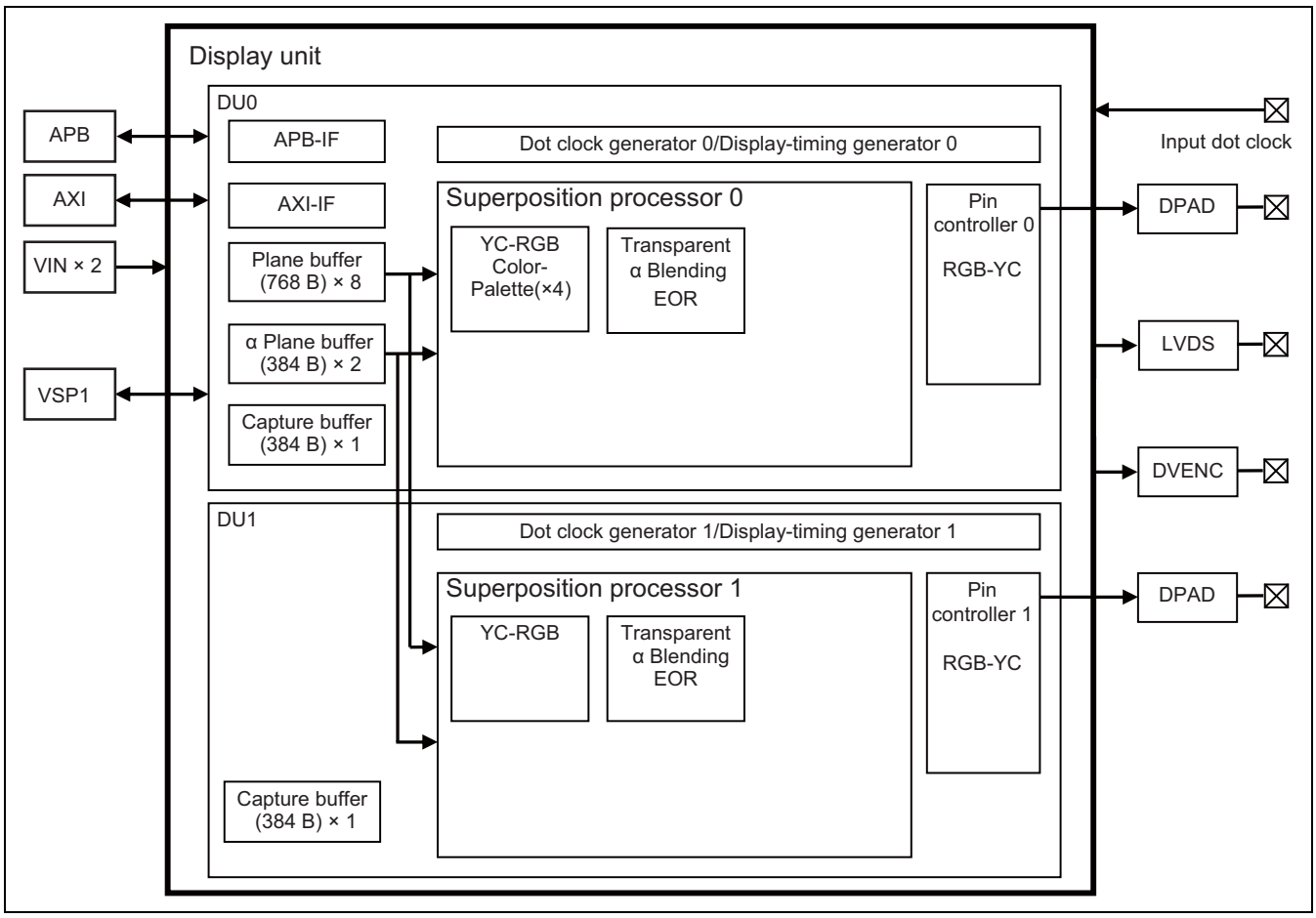


Figure 20.1 Block Diagram of the Display Unit (DU)

20.1.3 Input/Output Pins

Table 20.1a Pin Functions (DU0)

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU0 input dot clock	DU0_DOTCLKIN	Input	DU0 input dot clock (Initial value) DU1 input dot clock	DCLKIN
DU0 output dot clock 0	DU0_DOTCLKOUT0	Output	DU0 output dot clock (normal phase)	DCLKOUT
DU0 output dot clock 1	DU0_DOTCLKOUT1	Output	DU0 output dot clock (counter phase)	DCLKOUTB
DU0 external horizontal synchronous output/DU0 horizontal synchronous input	DU0_EXHSYNC/ DU0_HSYNC	I/O	DU0 composite synchronous output signal	CSYNC
			DU0 horizontal synchronous output/DU0 external horizontal synchronous input	HSYNC or EXHSYNC*1
DU0 external vertical synchronous output/DU0 vertical synchronous output	DU0_EXVSYNC/ DU0_VSYNC	I/O	DU0 vertical synchronous output/DU0 external vertical synchronous input	VSYNC or EXVSYNC*1
			DU0 composite synchronous output signal	CSYNC
DU0 odd/even field	DU0_EXODDF/ DU0_ODDF/ DISP/ CDE	I/O	DU0 odd/even field	ODDF or EXODDF*1
			DU0 CLAMP output signal	CLAMP
			DU0 display interval	DISP
			DU0 color detection	CDE
DU0 display interval	DU0_DISP	Output	DU0 display interval	DISP
			DU0 composite synchronous output signal	CSYNC
			DU0 DE output signal	DE
DU0 color detection	DU0_CDE	Output	DU0 color detection	CDE
DU0 display data	DU0_DR0	Output	DU0 digital red 0/green 4 DU1 digital red 0	Digital RGB or YC*5
	DU0_DR1	Output	DU0 digital red 1/green 5 DU1 digital red 1	
	DU0_DR2	Output	DU0 digital red 2/green 6 DU1 digital red 2	
	DU0_DR3	Output	DU0 digital red 3/green 7 DU1 digital red 3	
	DU0_DR4	Output	DU0 digital red 4/blue 0 DU1 digital red 4	
	DU0_DR5	Output	DU0 digital red 5/blue 1 DU1 digital red 5	
	DU0_DR6	Output	DU0 digital red 6/blue 2 DU1 digital red 6	
	DU0_DR7	Output	DU0 digital red 7/blue 3 DU1 digital red 7	
	DU0_DG0	Output	DU0 digital green 0/blue 4 DU1 digital green 0	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU0 display data	DU0_DG1	Output	DU0 digital green 1/blue 5 DU1 digital green 1	Digital RGB or YC*5
	DU0_DG2	Output	DU0 digital green 2/blue 6 DU1 digital green 2	
	DU0_DG3	Output	DU0 digital green 3/blue 7 DU1 digital green 3	
	DU0_DG4	Output	DU0 digital green 4 DU1 digital green 4	
	DU0_DG5	Output	DU0 digital green 5 DU1 digital green 5	
	DU0_DG6	Output	DU0 digital green 6 DU1 digital green 6	
	DU0_DG7	Output	DU0 digital green 7 DU1 digital green 7	
	DU0_DB0	Output	DU0 digital blue 0 DU1 digital blue 0	
	DU0_DB1	Output	DU0 digital blue 1 DU1 digital blue 1	
	DU0_DB2	Output	DU0 digital blue 2 DU1 digital blue 2	
	DU0_DB3	Output	DU0 digital blue 3 DU1 digital blue 3	
	DU0_DB4	Output	DU0 digital blue 4 DU1 digital blue 4	
	DU0_DB5	Output	DU0 digital blue 5 DU1 digital blue 5	
	DU0_DB6	Output	DU0 digital blue 6 DU1 digital blue 6	
	DU0_DB7	Output	DU0 digital blue 7 DU1 digital blue 7	

Notes: 1. These are expressed as EXHSYNC, EXVSYNC, and EXODDF in explanations of the functions as input signals and as HSYNC, VSYNC and ODDF otherwise.
2. When DU0 and DU1 are output at the same time, DU0 and DU1 are output in synchronization with rising and falling edges of the dot clock, respectively.
3. Synchronization for the output of digital 0 only is in accord with the setting of the output signal timing adjustment register 0 (OTAR0).
4. In this section, unless otherwise noted, "dot clock" refers to the output dot clock.
5. In YC format display, please refer to Table 20.39.

Table 20.1b Pin Functions (DU1)

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU1 input dot clock	DU1_DOTCLKIN	Input	DU0 input dot clock DU1 input dot clock (Initial value)	DCLKIN
DU1 output dot clock 0	DU1_DOTCLKOUT0	Output	DU1 output dot clock (normal phase)	DCLKOUT
DU1 output dot clock 1	DU1_DOTCLKOUT1	Output	DU1 output dot clock (counter phase)	DCLKOUTB
DU1 external horizontal synchronous output/DU1 horizontal synchronous input	DU1_EXHSYNC/ DU1_HSYNC	I/O	DU1 composite synchronous output signal	CSYNC
			DU1 horizontal synchronous output/DU1 external horizontal synchronous input	HSYNC or EXHSYNC*1
DU1 external vertical synchronous output/DU1 vertical synchronous output	DU1_EXVSYNC/ DU1_VSYNC	I/O	DU1 vertical synchronous output/ DU1 external vertical synchronous input	VSYNC or EXVSYNC*1
			DU1 composite synchronous output signal	CSYNC
DU1 odd/even field	DU1_EXODDF/ DU1_ODDF/ DISP/ CDE	I/O	DU1 odd/even field	ODDF or EXODDF*1
			DU1 CLAMP output signal	CLAMP
			DU1 display interval	DISP
			DU1 color detection	CDE
DU1 display interval	DU1_DISP	Output	DU1 display interval	DISP
			DU1 composite synchronous output signal	CSYNC
			DU1 DE output signal	DE
DU1 color detection	DU1_CDE	Output	DU1 color detection	CDE
DU1 display data	DU1_DR0	Output	DU1 digital red 0/green 4	Digital RGB or YC *4
	DU1_DR1	Output	DU1 digital red 1/green 5	
	DU1_DR2	Output	DU1 digital red 2/green 6	
	DU1_DR3	Output	DU1 digital red 3/green 7	
	DU1_DR4	Output	DU1 digital red 4/blue 0	
	DU1_DR5	Output	DU1 digital red 5/blue 1	
	DU1_DR6	Output	DU1 digital red 6/blue 2	
	DU1_DR7	Output	DU1 digital red 7/blue 3	
	DU1_DG0	Output	DU1 digital green 0/blue 4	
	DU1_DG1	Output	DU1 digital green 1/blue 5	
	DU1_DG2	Output	DU1 digital green 2/blue 6	
	DU1_DG3	Output	DU1 digital green 3/blue 7	
	DU1_DG4	Output	DU1 digital green 4	
	DU1_DG5	Output	DU1 digital green 5	
	DU1_DG6	Output	DU1 digital green 6	
	DU1_DG7	Output	DU1 digital green 7	
	DU1_DB0	Output	DU1 digital blue 0	
	DU1_DB1	Output	DU1 digital blue 1	

Name	Pin Name	I/O	Function	Signal Name Used in This Section
DU1 display data	DU1_DB2	Output	DU1 digital blue 2	Digital RGB or YC *4
	DU1_DB3	Output	DU1 digital blue 3	
	DU1_DB4	Output	DU1 digital blue 4	
	DU1_DB5	Output	DU1 digital blue 5	
	DU1_DB6	Output	DU1 digital blue 6	
	DU1_DB7	Output	DU1 digital blue 7	

Notes: 1. These are expressed as EXHSYNC, EXVSYNC, and EXODDF in explanations of the functions as input signals and as HSYNC, VSYNC and ODDF otherwise.
2. Synchronization for the output of digital 1 only is in accord with the setting of the output signal timing adjustment register 1 (OTAR1).
3. In this section, unless otherwise noted, "dot clock" refers to the output dot clock.
4. In YC format display, please refer to Table 20.39.

20.2 Register Configuration

In the display unit (DU), register update methods include external update and internal update.

(1) External Update

An "external update" is an update which reflects the address-mapped register settings made by the CPU after the end of CPU access. Registers related to display control (for example, the display unit system control register) and the settings of which are updated through external updates can be overwritten without display flicker by using bits 11 and 14 in the display unit status register n (DSSRn) *2 indicating the start position of the vertical blanking interval.

(2) Internal Update

An "internal update" is an update that reflects the address-mapped register settings with the internal update timing of the display unit (DU). Hence in the case of a register with an internal update function, even when the CPU overwrites address-mapped registers related to display operation without being aware of the display timing, display flicker can be prevented.

An internal update is performed during the interval in which the display reset (DRES) bit in the display unit system control register 0 (DSYSR0) is 1 and at the beginning of each frame. The internal update performed at the beginning of each frame is disabled using the internal update disable (IUPD) bit in the display unit system control register 0 (DSYSR0).

Bits which are internally updated in response to setting of the display reset (DRES) bit in the display unit system control register 0 (DSYSR0) are listed in the column headed "Bit with Internal Update Function" in tables on the following pages.

The registers for the X and Y start positions for plane n in the interlaced sync & video mode (PnSPXR*1, PnSPYR*1) are also internally updated at the beginning of a field.

Updates are performed at the falling edge of VSYNC output when the sync method of the display unit system control register n (DSYSRn)*2 is master mode (bit 7 = 0, bit 6 = 0), or at the falling edge of EXVSYNC detected in TV sync mode (bit 7 = 1, bit 6 = 0). In sync transition mode (bit 7 = 0, bit 6 = 1), internal updates are not performed.

However, plane n display area start address 0 register (PnDSA0R*1), plane n display area start address 1 register (PnDSA1R*1), and plane n display area start address 2 register (PnDSA2R*1) are internally updated in display operation and externally updated when the video data and rendering data are written to addresses specified for these registers.

The address-mapped registers with an internal update function are shown in Tables 20.2 to 20.23. The initial settings for these registers should be made during the interval in which the DRES bit in DSYSR0 is 1.

Notes: 1. n = 1 to 8
2. n = 0 and 1

(3) Register Configuration

The suffixes n which are added to the register names and their abbreviations represent the DU channel numbers (n = 0 and 1).

(a) Display Unit System Control Register Configuration

Table 20.2 Display Unit System Control Register Configuration (1)

Base address: DU0: H'FEB0 0000 (suffix 0)
DU1: H'FEB3 0000 (suffix 1)

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Display unit system control register 0	DSYSR0	R/W	H'0000	32 bits	DSEC (bit 20) DEN (bit 8)
Display unit system control register 1	DSYSR1	R/W	H'0000	32 bits	DSEC2 (bit 20)
Display unit mode register n	DSMRn	R/W	H'0004	32 bits	All bits However, the following bits are updated with DRES: VSPM (bit 28) ODPM (bit 27) DIPM (bits 26, 25) CSPM (bit 24) DIL (bit 19) VSL (bit 18) HSL (bit 17)
Display unit status register n	DSSRn	R	H'0008	32 bits	None
Display unit status register clear register n	DSRCRn	W	H'000C	32 bits	None
Display unit interrupt enable register n	DIERn	R/W	H'0010	32 bits	None
Color palette control register	CPCR	R/W	H'0014	32 bits	All bits
Display plane priority register	DPPR	R/W	H'0018	32 bits	All bits
Display unit extensional function control register 0	DEFR0	R/W	H'0020	32 bits	The following bits are updated with DRES: DODF (bits 9, 8)
Display unit extensional function control register 1	DEFR1	R/W	H'0020	32 bits	The following bits are updated with DRES: EXSL1 (bit 12) DODF1 (bits 9, 8) VCUP1 (bit 4)
Display alpha ratio plane control register	DAPCR	R/W	H'0024	32 bits	All bits
Display capture control register	DCPCR	R/W	H'0028	32 bits	All bits
Display unit extensional function control 2 register	DEF2R	R/W	H'0034	32 bits	All bits Updated with DRES
Display unit extensional function control 3 register	DEF3R	R/W	H'0038	32 bits	All bits Updated with DRES
Display unit extensional function control 4 register	DEF4R	R/W	H'003C	32 bits	All bits Updated with DRES
Display unit video capture status register	DVCSR	R	H'00D0	32 bits	None

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Display unit extensional function control 5 register	DEF5R	R/W	H'00E0	32 bits	All bits However, the following bit is updated with DRES: DEFE5 (bit 0)
Display unit data latency adjustment register	DDLTR	R/W	H'00E4	32 bits	All bits Updated with DRES
Display unit extensional function control 6 register	DEF6R	R/W	H'00E8	32 bits	All bits Updated with DRES

Base address: DU0 (suffix 0) and DU1 (suffix 1) common: H'FEB2 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Display unit domain 1 status register 0	DD1SSR0	R	H'0008	32 bits	None
Display unit domain 1 status register 1	DD1SSR1	R	H'8008	32 bits	None
Display unit domain 1 status register clear register 0	DD1SRCR0	W	H'000C	32 bits	None
Display unit domain 1 status register clear register 1	DD1SRCR1	W	H'800C	32 bits	None
Display unit domain 1 interrupt enable register 0	DD1IER0	R/W	H'0010	32 bits	None
Display unit domain 1 interrupt enable register 1	DD1IER1	R/W	H'8010	32 bits	None
Display unit extensional function control 8 register	DEF8R	R/W	H'0020	32 bits	All bits Updated with DRES
Display unit output signal fixed level register	DOFLR	R/W	H'0024	32 bits	None
Display unit input dot clock select register	DIDSR	R/W	H'0028	32 bits	All bits Updated with DRES

Notes: 1. n = 0 and 1
2. The register available code is excluded. There is no internal update function for the register available code.

Table 20.3 Display Unit System Control Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Display unit system control register 0	DSYSR0	H'******8*
Display unit system control register 1	DSYSR1	H'******8*
Display unit mode register n	DSMRn	H'*0*00***
Display unit status register 0	DSSR0	H'3*00**00
Display unit status register 1	DSSR1	H'********
Display unit status register clear register n	DSRCRn	H'********
Display unit interrupt enable register 0	DIER0	H'******00
Display unit interrupt enable register 1	DIER1	H'********
Color palette control register	CPCR	H'***0****
Display plane priority register	DPPR	H'76543210
Display unit extensional function control register 0	DEFR0	H'********
Display unit extensional function control register 1	DEFR1	H'********
Display alpha ratio plane control register	DAPCR	H'********
Display capture control register	DCPCR	H'********
Display unit extensional function control 2 register	DEF2R	H'********
Display unit extensional function control 3 register	DEF3R	H'********
Display unit extensional function control 4 register	DEF4R	H'********
Display unit video capture status register	DVCSR	H'***0***0
Display unit extensional function control 5 register	DEF5R	H'******0*
Display unit data latency adjustment register	DDLTR	H'********
Display unit extensional function control 6 register	DEF6R	H'*****0**
Display unit domain 1 status register 0	DD1SSR0	H'******00
Display unit domain 1 status register 1	DD1SSR1	H'********
Display unit domain 1 status register clear register 0	DD1SRCR0	H'********
Display unit domain 1 status register clear register 1	DD1SRCR1	H'********
Display unit domain 1 interrupt enable register 0	DD1IER0	H'******00
Display unit domain 1 interrupt enable register 1	DD1IER1	H'********
Display unit extensional function control 8 register	DEF8R	H'********
Display unit output signal fixed level register	DOFLR	H'*****0*0
Display unit input dot clock select register	DIDSR	H'*****0*0

Note: n = 0 and 1

(b) Display Timing Generation Register Configuration

Table 20.4 Display Timing Generation Register Configuration (1)

Base address: DU0: H'FEB0 0000 (suffix 0)
DU1: H'FEB3 0000 (suffix 1)

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
Horizontal display start register n	HDSR0	R/W	H'0040	32 bits	All bits
	HDSR1				
Horizontal display end register n	HDER0	R/W	H'0044	32 bits	All bits
	HDER1				
Vertical display start register n	VDSR0	R/W	H'0048	32 bits	All bits
	VDSR1				
Vertical display end register n	VDER0	R/W	H'004C	32 bits	All bits
	VDER1				
Horizontal cycle register n	HCR0	R/W	H'0050	32 bits	All bits
	HCR1				
Horizontal sync width register n	HSWR0	R/W	H'0054	32 bits	All bits
	HSWR1				
Vertical cycle register n	VCR0	R/W	H'0058	32 bits	All bits
	VCR1				
Vertical sync point register n	VSPR0	R/W	H'005C	32 bits	All bits
	VSPR1				
Equal pulse width register n	EQWR0	R/W	H'0060	32 bits	All bits
	EQWR1				
Serration width register n	SPWR0	R/W	H'0064	32 bits	All bits
	SPWR1				
CLAMP signal start register n	CLAMPSR0	R/W	H'0070	32 bits	All bits
	CLAMPSR1				
CLAMP signal width register n	CLAMPWR0	R/W	H'0074	32 bits	All bits
	CLAMPWR1				
DE signal start register n	DESR0	R/W	H'0078	32 bits	All bits
	DESR1				
DE signal width register n	DEWR0	R/W	H'007C	32 bits	All bits
	DEWR1				

Note: n = 0 and 1

Table 20.5 Display Timing Generation Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Horizontal display start register n	HDSR0	H'********
	HDSR1	
Horizontal display end register n	HDER0	H'********
	HDER1	
Vertical display start register n	VDSR0	H'********
	VDSR1	
Vertical display end register n	VDER0	H'********
	VDER1	
Horizontal cycle register n	HCR0	H'********
	HCR1	
Horizontal sync width register n	HSWR0	H'********
	HSWR1	
Vertical cycle register n	VCR0	H'********
	VCR1	
Vertical sync point register n	VSPR0	H'********
	VSPR1	
Equal pulse width register n	EQWR0	H'********
	EQWR1	
Serration width register n	SPWR0	H'********
	SPWR1	
CLAMP signal start register n	CLAMPSR0	H'********
	CLAMPSR1	
CLAMP signal width register n	CLAMPWR0	H'********
	CLAMPWR1	
DE signal start register n	DESR0	H'********
	DESR1	
DE signal width register n	DEWR0	H'********
	DEWR1	

Note: n = 0 and 1

(c) Display Attribute Register Configuration

Table 20.6 Display Attribute Register Configuration (1)

Base address: DU0: H'FEB0 0000 (suffix 0)
DU1: H'FEB3 0000 (suffix 1)

Register Name	Abbr.	R/W	Address in P4	Access Size	Bit with Internal Update Function*
Color palette 1 transparent color register	CP1TR	R/W	H'0080	32 bits	All bits
Color palette 2 transparent color register	CP2TR	R/W	H'0084	32 bits	All bits
Color palette 3 transparent color register	CP3TR	R/W	H'0088	32 bits	All bits
Color palette 4 transparent color register	CP4TR	R/W	H'008C	32 bits	All bits
Display off mode output register n	DOOR0	R/W	H'0090	32 bits	All bits
	DOOR1				
Color detection register n	CDER0	R/W	H'0094	32 bits	All bits
	CDER1				
Background plane output register n	BPOR0	R/W	H'0098	32 bits	All bits
	BPOR1				
Raster interrupt offset register n	RINTOFSR0	R/W	H'009C	32 bits	All bits
	RINTOFSR1				

Notes: 1. n = 0 and 1
2. The register available code is excluded. There is no internal update function for the register available code.

Table 20.7 Display Attribute Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Color palette 1 transparent color register	CP1TR	H'****0000
Color palette 2 transparent color register	CP2TR	H'****0000
Color palette 3 transparent color register	CP3TR	H'****0000
Color palette 4 transparent color register	CP4TR	H'****0000
Display off mode output register n	DOOR0	H'********
	DOOR1	
Color detection register n	CDER0	H'********
	CDER1	
Background plane output register n	BPOR0	H'********
	BPOR1	
Raster interrupt offset register n	RINTOFSR0	H'********
	RINTOFSR1	

Note: n = 0 and 1

(d) Display Plane Register Configuration

Table 20.8 Display Plane Register Configuration (1)

Base address: DU0: H'FEB0 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Plane 1 mode register	P1MR	R/W	H'0100	32 bits	All bits
Plane 1 memory width register	P1MWR	R/W	H'0104	32 bits	All bits
Plane 1 blending ratio register	P1ALPHAR	R/W	H'0108	32 bits	All bits
Plane 1 display size X register	P1DSXR	R/W	H'0110	32 bits	All bits
Plane 1 display size Y register	P1DSYR	R/W	H'0114	32 bits	All bits
Plane 1 display position X register	P1DPXR	R/W	H'0118	32 bits	All bits
Plane 1 display position Y register	P1DPYR	R/W	H'011C	32 bits	All bits
Plane 1 display area start address 0 register	P1DSA0R	R/W	H'0120	32 bits	All bits
Plane 1 display area start address 1 register	P1DSA1R	R/W	H'0124	32 bits	All bits
Plane 1 display area start address 2 register	P1DSA2R	R/W	H'0128	32 bits	All bits
Plane 1 start position X register	P1SPXR	R/W	H'0130	32 bits	All bits
Plane 1 start position Y register	P1SPYR	R/W	H'0134	32 bits	All bits
Plane 1 wrap-around start position register	P1WASPR	R/W	H'0138	32 bits	All bits
Plane 1 wrap-around memory width register	P1WAMWR	R/W	H'013C	32 bits	All bits
Plane 1 blinking time register	P1BTR	R/W	H'0140	32 bits	All bits
Plane 1 transparent color 1 register	P1TC1R	R/W	H'0144	32 bits	All bits
Plane 1 transparent color 2 register	P1TC2R	R/W	H'0148	32 bits	All bits
Plane 1 transparent color 3 register	P1TC3R	R/W	H'014C	32 bits	All bits
Plane 1 memory length register	P1MLR	R/W	H'0150	32 bits	All bits
Plane 1 swap control register	P1SWAPR	R/W	H'0180	32 bits	All bits
Plane 1 display data control register	P1DDCR	R/W	H'0184	32 bits	All bits
Plane 1 display data control 2 register	P1DDC2R	R/W	H'0188	32 bits	All bits
Plane 1 display data control 4 register	P1DDC4R	R/W	H'0190	32 bits	All bits
Plane 2 mode register	P2MR	R/W	H'0200	32 bits	All bits
Plane 2 memory width register	P2MWR	R/W	H'0204	32 bits	All bits
Plane 2 blending ratio register	P2ALPHAR	R/W	H'0208	32 bits	All bits
Plane 2 display size X register	P2DSXR	R/W	H'0210	32 bits	All bits
Plane 2 display size Y register	P2DSYR	R/W	H'0214	32 bits	All bits
Plane 2 display position X register	P2DPXR	R/W	H'0218	32 bits	All bits
Plane 2 display position Y register	P2DPYR	R/W	H'021C	32 bits	All bits
Plane 2 display area start address 0 register	P2DSA0R	R/W	H'0220	32 bits	All bits
Plane 2 display area start address 1 register	P2DSA1R	R/W	H'0224	32 bits	All bits
Plane 2 display area start address 2 register	P2DSA2R	R/W	H'0228	32 bits	All bits
Plane 2 start position X register	P2SPXR	R/W	H'0230	32 bits	All bits
Plane 2 start position Y register	P2SPYR	R/W	H'0234	32 bits	All bits
Plane 2 wrap-around start position register	P2WASPR	R/W	H'0238	32 bits	All bits
Plane 2 wrap-around memory width register	P2WAMWR	R/W	H'023C	32 bits	All bits
Plane 2 blinking time register	P2BTR	R/W	H'0240	32 bits	All bits
Plane 2 transparent color 1 register	P2TC1R	R/W	H'0244	32 bits	All bits

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Plane 2 transparent color 2 register	P2TC2R	R/W	H'0248	32 bits	All bits
Plane 2 transparent color 3 register	P2TC3R	R/W	H'024C	32 bits	All bits
Plane 2 memory length register	P2MLR	R/W	H'0250	32 bits	All bits
Plane 2 swap control register	P2SWAPR	R/W	H'0280	32 bits	All bits
Plane 2 display data control register	P2DDCR	R/W	H'0284	32 bits	All bits
Plane 2 display data control 2 register	P2DDC2R	R/W	H'0288	32 bits	All bits
Plane 2 display data control 4 register	P2DDC4R	R/W	H'0290	32 bits	All bits
Plane 3 mode register	P3MR	R/W	H'0300	32 bits	All bits
Plane 3 memory width register	P3MWR	R/W	H'0304	32 bits	All bits
Plane 3 blending ratio register	P3ALPHAR	R/W	H'0308	32 bits	All bits
Plane 3 display size X register	P3DSXR	R/W	H'0310	32 bits	All bits
Plane 3 display size Y register	P3DSYR	R/W	H'0314	32 bits	All bits
Plane 3 display position X register	P3DPXR	R/W	H'0318	32 bits	All bits
Plane 3 display position Y register	P3DPYR	R/W	H'031C	32 bits	All bits
Plane 3 display area start address 0 register	P3DSA0R	R/W	H'0320	32 bits	All bits
Plane 3 display area start address 1 register	P3DSA1R	R/W	H'0324	32 bits	All bits
Plane 3 display area start address 2 register	P3DSA2R	R/W	H'0328	32 bits	All bits
Plane 3 start position X register	P3SPXR	R/W	H'0330	32 bits	All bits
Plane 3 start position Y register	P3SPYR	R/W	H'0334	32 bits	All bits
Plane 3 wrap-around start position register	P3WASPR	R/W	H'0338	32 bits	All bits
Plane 3 wrap-around memory width register	P3WAMWR	R/W	H'033C	32 bits	All bits
Plane 3 blinking time register	P3BTR	R/W	H'0340	32 bits	All bits
Plane 3 transparent color 1 register	P3TC1R	R/W	H'0344	32 bits	All bits
Plane 3 transparent color 2 register	P3TC2R	R/W	H'0348	32 bits	All bits
Plane 3 transparent color 3 register	P3TC3R	R/W	H'034C	32 bits	All bits
Plane 3 memory length register	P3MLR	R/W	H'0350	32 bits	All bits
Plane 3 swap control register	P3SWAPR	R/W	H'0380	32 bits	All bits
Plane 3 display data control register	P3DDCR	R/W	H'0384	32 bits	All bits
Plane 3 display data control 2 register	P3DDC2R	R/W	H'0388	32 bits	All bits
Plane 3 display data control 4 register	P3DDC4R	R/W	H'0390	32 bits	All bits
Plane 4 mode register	P4MR	R/W	H'0400	32 bits	All bits
Plane 4 memory width register	P4MWR	R/W	H'0404	32 bits	All bits
Plane 4 blending ratio register	P4ALPHAR	R/W	H'0408	32 bits	All bits
Plane 4 display size X register	P4DSXR	R/W	H'0410	32 bits	All bits
Plane 4 display size Y register	P4DSYR	R/W	H'0414	32 bits	All bits
Plane 4 display position X register	P4DPXR	R/W	H'0418	32 bits	All bits
Plane 4 display position Y register	P4DPYR	R/W	H'041C	32 bits	All bits
Plane 4 display area start address 0 register	P4DSA0R	R/W	H'0420	32 bits	All bits
Plane 4 display area start address 1 register	P4DSA1R	R/W	H'0424	32 bits	All bits
Plane 4 display area start address 2 register	P4DSA2R	R/W	H'0428	32 bits	All bits
Plane 4 start position X register	P4SPXR	R/W	H'0430	32 bits	All bits
Plane 4 start position Y register	P4SPYR	R/W	H'0434	32 bits	All bits
Plane 4 wrap-around start position register	P4WASPR	R/W	H'0438	32 bits	All bits

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Plane 4 wrap-around memory width register	P4WAMWR	R/W	H'043C	32 bits	All bits
Plane 4 blinking time register	P4BTR	R/W	H'0440	32 bits	All bits
Plane 4 transparent color 1 register	P4TC1R	R/W	H'0444	32 bits	All bits
Plane 4 transparent color 2 register	P4TC2R	R/W	H'0448	32 bits	All bits
Plane 4 transparent color 3 register	P4TC3R	R/W	H'044C	32 bits	All bits
Plane 4 memory length register	P4MLR	R/W	H'0450	32 bits	All bits
Plane 4 swap control register	P4SWAPR	R/W	H'0480	32 bits	All bits
Plane 4 display data control register	P4DDCR	R/W	H'0484	32 bits	All bits
Plane 4 display data control 2 register	P4DDC2R	R/W	H'0488	32 bits	All bits
Plane 4 display data control 4 register	P4DDC4R	R/W	H'0490	32 bits	All bits
Plane 5 mode register	P5MR	R/W	H'0500	32 bits	All bits
Plane 5 memory width register	P5MWR	R/W	H'0504	32 bits	All bits
Plane 5 blending ratio register	P5ALPHAR	R/W	H'0508	32 bits	All bits
Plane 5 display size X register	P5DSXR	R/W	H'0510	32 bits	All bits
Plane 5 display size Y register	P5DSYR	R/W	H'0514	32 bits	All bits
Plane 5 display position X register	P5DPXR	R/W	H'0518	32 bits	All bits
Plane 5 display position Y register	P5DPYR	R/W	H'051C	32 bits	All bits
Plane 5 display area start address 0 register	P5DSA0R	R/W	H'0520	32 bits	All bits
Plane 5 display area start address 1 register	P5DSA1R	R/W	H'0524	32 bits	All bits
Plane 5 display area start address 2 register	P5DSA2R	R/W	H'0528	32 bits	All bits
Plane 5 start position X register	P5SPXR	R/W	H'0530	32 bits	All bits
Plane 5 start position Y register	P5SPYR	R/W	H'0534	32 bits	All bits
Plane 5 wrap-around start position register	P5WASPR	R/W	H'0538	32 bits	All bits
Plane 5 wrap-around memory width register	P5WAMWR	R/W	H'053C	32 bits	All bits
Plane 5 blinking time register	P5BTR	R/W	H'0540	32 bits	All bits
Plane 5 transparent color 1 register	P5TC1R	R/W	H'0544	32 bits	All bits
Plane 5 transparent color 2 register	P5TC2R	R/W	H'0548	32 bits	All bits
Plane 5 transparent color 3 register	P5TC3R	R/W	H'054C	32 bits	All bits
Plane 5 memory length register	P5MLR	R/W	H'0550	32 bits	All bits
Plane 5 swap control register	P5SWAPR	R/W	H'0580	32 bits	All bits
Plane 5 display data control register	P5DDCR	R/W	H'0584	32 bits	All bits
Plane 5 display data control 2 register	P5DDC2R	R/W	H'0588	32 bits	All bits
Plane 5 display data control 4 register	P5DDC4R	R/W	H'0590	32 bits	All bits
Plane 6 mode register	P6MR	R/W	H'0600	32 bits	All bits
Plane 6 memory width register	P6MWR	R/W	H'0604	32 bits	All bits
Plane 6 blending ratio register	P6ALPHAR	R/W	H'0608	32 bits	All bits
Plane 6 display size X register	P6DSXR	R/W	H'0610	32 bits	All bits
Plane 6 display size Y register	P6DSYR	R/W	H'0614	32 bits	All bits
Plane 6 display position X register	P6DPXR	R/W	H'0618	32 bits	All bits
Plane 6 display position Y register	P6DPYR	R/W	H'061C	32 bits	All bits
Plane 6 display area start address 0 register	P6DSA0R	R/W	H'0620	32 bits	All bits
Plane 6 display area start address 1 register	P6DSA1R	R/W	H'0624	32 bits	All bits
Plane 6 display area start address 2 register	P6DSA2R	R/W	H'0628	32 bits	All bits

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Plane 6 start position X register	P6SPXR	R/W	H'0630	32 bits	All bits
Plane 6 start position Y register	P6SPYR	R/W	H'0634	32 bits	All bits
Plane 6 wrap-around start position register	P6WASPR	R/W	H'0638	32 bits	All bits
Plane 6 wrap-around memory width register	P6WAMWR	R/W	H'063C	32 bits	All bits
Plane 6 blinking time register	P6BTR	R/W	H'0640	32 bits	All bits
Plane 6 transparent color 1 register	P6TC1R	R/W	H'0644	32 bits	All bits
Plane 6 transparent color 2 register	P6TC2R	R/W	H'0648	32 bits	All bits
Plane 6 transparent color 3 register	P6TC3R	R/W	H'064C	32 bits	All bits
Plane 6 memory length register	P6MLR	R/W	H'0650	32 bits	All bits
Plane 6 swap control register	P6SWAPR	R/W	H'0680	32 bits	All bits
Plane 6 display data control register	P6DDCR	R/W	H'0684	32 bits	All bits
Plane 6 display data control 2 register	P6DDC2R	R/W	H'0688	32 bits	All bits
Plane 6 display data control 4 register	P6DDC4R	R/W	H'0690	32 bits	All bits
Plane 7 mode register	P7MR	R/W	H'0700	32 bits	All bits
Plane 7 memory width register	P7MWR	R/W	H'0704	32 bits	All bits
Plane 7 blending ratio register	P7ALPHAR	R/W	H'0708	32 bits	All bits
Plane 7 display size X register	P7DSXR	R/W	H'0710	32 bits	All bits
Plane 7 display size Y register	P7DSYR	R/W	H'0714	32 bits	All bits
Plane 7 display position X register	P7DPXR	R/W	H'0718	32 bits	All bits
Plane 7 display position Y register	P7DPYR	R/W	H'071C	32 bits	All bits
Plane 7 display area start address 0 register	P7DSA0R	R/W	H'0720	32 bits	All bits
Plane 7 display area start address 1 register	P7DSA1R	R/W	H'0724	32 bits	All bits
Plane 7 display area start address 2 register	P7DSA2R	R/W	H'0728	32 bits	All bits
Plane 7 start position X register	P7SPXR	R/W	H'0730	32 bits	All bits
Plane 7 start position Y register	P7SPYR	R/W	H'0734	32 bits	All bits
Plane 7 wrap-around start position register	P7WASPR	R/W	H'0738	32 bits	All bits
Plane 7 wrap-around memory width register	P7WAMWR	R/W	H'073C	32 bits	All bits
Plane 7 blinking time register	P7BTR	R/W	H'0740	32 bits	All bits
Plane 7 transparent color 1 register	P7TC1R	R/W	H'0744	32 bits	All bits
Plane 7 transparent color 2 register	P7TC2R	R/W	H'0748	32 bits	All bits
Plane 7 transparent color 3 register	P7TC3R	R/W	H'074C	32 bits	All bits
Plane 7 memory length register	P7MLR	R/W	H'0750	32 bits	All bits
Plane 7 swap control register	P7SWAPR	R/W	H'0780	32 bits	All bits
Plane 7 display data control register	P7DDCR	R/W	H'0784	32 bits	All bits
Plane 7 display data control 2 register	P7DDC2R	R/W	H'0788	32 bits	All bits
Plane 7 display data control 4 register	P7DDC4R	R/W	H'0790	32 bits	All bits
Plane 8 mode register	P8MR	R/W	H'0800	32 bits	All bits
Plane 8 memory width register	P8MWR	R/W	H'0804	32 bits	All bits
Plane 8 blending ratio register	P8ALPHAR	R/W	H'0808	32 bits	All bits
Plane 8 display size X register	P8DSXR	R/W	H'0810	32 bits	All bits
Plane 8 display size Y register	P8DSYR	R/W	H'0814	32 bits	All bits
Plane 8 display position X register	P8DPXR	R/W	H'0818	32 bits	All bits
Plane 8 display position Y register	P8DPYR	R/W	H'081C	32 bits	All bits

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function*
Plane 8 display area start address 0 register	P8DSA0R	R/W	H'0820	32 bits	All bits
Plane 8 display area start address 1 register	P8DSA1R	R/W	H'0824	32 bits	All bits
Plane 8 display area start address 2 register	P8DSA2R	R/W	H'0828	32 bits	All bits
Plane 8 start position X register	P8SPXR	R/W	H'0830	32 bits	All bits
Plane 8 start position Y register	P8SPYR	R/W	H'0834	32 bits	All bits
Plane 8 wrap-around start position register	P8WASPR	R/W	H'0838	32 bits	All bits
Plane 8 wrap-around memory width register	P8WAMWR	R/W	H'083C	32 bits	All bits
Plane 8 blinking time register	P8BTR	R/W	H'0840	32 bits	All bits
Plane 8 transparent color 1 register	P8TC1R	R/W	H'0844	32 bits	All bits
Plane 8 transparent color 2 register	P8TC2R	R/W	H'0848	32 bits	All bits
Plane 8 transparent color 3 register	P8TC3R	R/W	H'084C	32 bits	All bits
Plane 8 memory length register	P8MLR	R/W	H'0850	32 bits	All bits
Plane 8 swap control register	P8SWAPR	R/W	H'0880	32 bits	All bits
Plane 8 display data control register	P8DDCR	R/W	H'0884	32 bits	All bits
Plane 8 display data control 2 register	P8DDC2R	R/W	H'0888	32 bits	All bits
Plane 8 display data control 4 register	P8DDC4R	R/W	H'0890	32 bits	All bits

Note: The register available code is excluded. There is no internal update function for the register available code.

Table 20.9 Display Plane Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Plane 1 mode register	P1MR	H'********
Plane 1 memory width register	P1MWR	H'********
Plane 1 blending ratio register	P1ALPHAR	H'********
Plane 1 display size X register	P1DSXR	H'********
Plane 1 display size Y register	P1DSYR	H'********
Plane 1 display position X register	P1DPXR	H'********
Plane 1 display position Y register	P1DPYR	H'********
Plane 1 display area start address 0 register	P1DSA0R	H'********
Plane 1 display area start address 1 register	P1DSA1R	H'********
Plane 1 display area start address 2 register	P1DSA2R	H'********
Plane 1 start position X register	P1SPXR	H'********
Plane 1 start position Y register	P1SPYR	H'********
Plane 1 wrap-around start position register	P1WASPR	H'********
Plane 1 wrap-around memory width register	P1WAMWR	H'********
Plane 1 blinking time register	P1BTR	H'****0101
Plane 1 transparent color 1 register	P1TC1R	H'********
Plane 1 transparent color 2 register	P1TC2R	H'********
Plane 1 transparent color 3 register	P1TC3R	H'********
Plane 1 memory length register	P1MLR	H'****0000
Plane 1 swap control register	P1SWAPR	H'*******0
Plane 1 display data control register	P1DDCR	H'********
Plane 1 display data control 2 register	P1DDC2R	H'********
Plane 1 display data control 4 register	P1DDC4R	H'********
Plane 2 mode register	P2MR	H'********
Plane 2 memory width register	P2MWR	H'********
Plane 2 blending ratio register	P2ALPHAR	H'********
Plane 2 display size X register	P2DSXR	H'********
Plane 2 display size Y register	P2DSYR	H'********
Plane 2 display position X register	P2DPXR	H'********
Plane 2 display position Y register	P2DPYR	H'********
Plane 2 display area start address 0 register	P2DSA0R	H'********
Plane 2 display area start address 1 register	P2DSA1R	H'********
Plane 2 display area start address 2 register	P2DSA2R	H'********
Plane 2 start position X register	P2SPXR	H'********
Plane 2 start position Y register	P2SPYR	H'********
Plane 2 wrap-around start position register	P2WASPR	H'********
Plane 2 wrap-around memory width register	P2WAMWR	H'********
Plane 2 blinking time register	P2BTR	H'****0101
Plane 2 transparent color 1 register	P2TC1R	H'********
Plane 2 transparent color 2 register	P2TC2R	H'********
Plane 2 transparent color 3 register	P2TC3R	H'********
Plane 2 memory length register	P2MLR	H'****0000

Register Name	Abbr.	Power-on Reset
Plane 2 swap control register	P2SWAPR	H'*******0
Plane 2 display data control register	P2DDCR	H'********
Plane 2 display data control 2 register	P2DDC2R	H'********
Plane 2 display data control 4 register	P2DDC4R	H'********
Plane 3 mode register	P3MR	H'********
Plane 3 memory width register	P3MWR	H'********
Plane 3 blending ratio register	P3ALPHAR	H'********
Plane 3 display size X register	P3DSXR	H'********
Plane 3 display size Y register	P3DSYR	H'********
Plane 3 display position X register	P3DPXR	H'********
Plane 3 display position Y register	P3DPYR	H'********
Plane 3 display area start address 0 register	P3DSA0R	H'********
Plane 3 display area start address 1 register	P3DSA1R	H'********
Plane 3 display area start address 2 register	P3DSA2R	H'********
Plane 3 start position X register	P3SPXR	H'********
Plane 3 start position Y register	P3SPYR	H'********
Plane 3 wrap-around start position register	P3WASPR	H'********
Plane 3 wrap-around memory width register	P3WAMWR	H'********
Plane 3 blinking time register	P3BTR	H'****0101
Plane 3 transparent color 1 register	P3TC1R	H'********
Plane 3 transparent color 2 register	P3TC2R	H'********
Plane 3 transparent color 3 register	P3TC3R	H'********
Plane 3 memory length register	P3MLR	H'****0000
Plane 3 swap control register	P3SWAPR	H'*******0
Plane 3 display data control register	P3DDCR	H'********
Plane 3 display data control 2 register	P3DDC2R	H'********
Plane 3 display data control 4 register	P3DDC4R	H'********
Plane 4 mode register	P4MR	H'********
Plane 4 memory width register	P4MWR	H'********
Plane 4 blending ratio register	P4ALPHAR	H'********
Plane 4 display size X register	P4DSXR	H'********
Plane 4 display size Y register	P4DSYR	H'********
Plane 4 display position X register	P4DPXR	H'********
Plane 4 display position Y register	P4DPYR	H'********
Plane 4 display area start address 0 register	P4DSA0R	H'********
Plane 4 display area start address 1 register	P4DSA1R	H'********
Plane 4 display area start address 2 register	P4DSA2R	H'********
Plane 4 start position X register	P4SPXR	H'********
Plane 4 start position Y register	P4SPYR	H'********
Plane 4 wrap-around start position register	P4WASPR	H'********
Plane 4 wrap-around memory width register	P4WAMWR	H'********
Plane 4 blinking time register	P4BTR	H'****0101
Plane 4 transparent color 1 register	P4TC1R	H'********
Plane 4 transparent color 2 register	P4TC2R	H'********

Register Name	Abbr.	Power-on Reset
Plane 4 transparent color 3 register	P4TC3R	H'********
Plane 4 memory length register	P4MLR	H'****0000
Plane 4 swap control register	P4SWAPR	H'*******0
Plane 4 display data control register	P4DDCR	H'********
Plane 4 display data control 2 register	P4DDC2R	H'********
Plane 4 display data control 4 register	P4DDC4R	H'********
Plane 5 mode register	P5MR	H'********
Plane 5 memory width register	P5MWR	H'********
Plane 5 blending ratio register	P5ALPHAR	H'********
Plane 5 display size X register	P5DSXR	H'********
Plane 5 display size Y register	P5DSYR	H'********
Plane 5 display position X register	P5DPXR	H'********
Plane 5 display position Y register	P5DPYR	H'********
Plane 5 display area start address 0 register	P5DSA0R	H'********
Plane 5 display area start address 1 register	P5DSA1R	H'********
Plane 5 display area start address 2 register	P5DSA2R	H'********
Plane 5 start position X register	P5SPXR	H'********
Plane 5 start position Y register	P5SPYR	H'********
Plane 5 wrap-around start position register	P5WASPR	H'********
Plane 5 wrap-around memory width register	P5WAMWR	H'********
Plane 5 blinking time register	P5BTR	H'****0101
Plane 5 transparent color 1 register	P5TC1R	H'********
Plane 5 transparent color 2 register	P5TC2R	H'********
Plane 5 transparent color 3 register	P5TC3R	H'********
Plane 5 memory length register	P5MLR	H'****0000
Plane 5 swap control register	P5SWAPR	H'*******0
Plane 5 display data control register	P5DDCR	H'********
Plane 5 display data control 2 register	P5DDC2R	H'********
Plane 5 display data control 4 register	P5DDC4R	H'********
Plane 6 mode register	P6MR	H'********
Plane 6 memory width register	P6MWR	H'********
Plane 6 blending ratio register	P6ALPHAR	H'********
Plane 6 display size X register	P6DSXR	H'********
Plane 6 display size Y register	P6DSYR	H'********
Plane 6 display position X register	P6DPXR	H'********
Plane 6 display position Y register	P6DPYR	H'********
Plane 6 display area start address 0 register	P6DSA0R	H'********
Plane 6 display area start address 1 register	P6DSA1R	H'********
Plane 6 display area start address 2 register	P6DSA2R	H'********
Plane 6 start position X register	P6SPXR	H'********
Plane 6 start position Y register	P6SPYR	H'********
Plane 6 wrap-around start position register	P6WASPR	H'********
Plane 6 wrap-around memory width register	P6WAMWR	H'********
Plane 6 blinking time register	P6BTR	H'****0101

Register Name	Abbr.	Power-on Reset
Plane 6 transparent color 1 register	P6TC1R	H'********
Plane 6 transparent color 2 register	P6TC2R	H'********
Plane 6 transparent color 3 register	P6TC3R	H'********
Plane 6 memory length register	P6MLR	H'****0000
Plane 6 swap control register	P6SWAPR	H'*******0
Plane 6 display data control register	P6DDCR	H'********
Plane 6 display data control 2 register	P6DDC2R	H'********
Plane 6 display data control 4 register	P6DDC4R	H'********
Plane 7 mode register	P7MR	H'********
Plane 7 memory width register	P7MWR	H'********
Plane 7 blending ratio register	P7ALPHAR	H'********
Plane 7 display size X register	P7DSXR	H'********
Plane 7 display size Y register	P7DSYR	H'********
Plane 7 display position X register	P7DPXR	H'********
Plane 7 display position Y register	P7DPYR	H'********
Plane 7 display area start address 0 register	P7DSA0R	H'********
Plane 7 display area start address 1 register	P7DSA1R	H'********
Plane 7 display area start address 2 register	P7DSA2R	H'********
Plane 7 start position X register	P7SPXR	H'********
Plane 7 start position Y register	P7SPYR	H'********
Plane 7 wrap-around start position register	P7WASPR	H'********
Plane 7 wrap-around memory width register	P7WAMWR	H'********
Plane 7 blinking time register	P7BTR	H'****0101
Plane 7 transparent color 1 register	P7TC1R	H'********
Plane 7 transparent color 2 register	P7TC2R	H'********
Plane 7 transparent color 3 register	P7TC3R	H'********
Plane 7 memory length register	P7MLR	H'****0000
Plane 7 swap control register	P7SWAPR	H'*******0
Plane 7 display data control register	P7DDCR	H'********
Plane 7 display data control 2 register	P7DDC2R	H'********
Plane 7 display data control 4 register	P7DDC4R	H'********
Plane 8 mode register	P8MR	H'********
Plane 8 memory width register	P8MWR	H'********
Plane 8 blending ratio register	P8ALPHAR	H'********
Plane 8 display size X register	P8DSXR	H'********
Plane 8 display size Y register	P8DSYR	H'********
Plane 8 display position X register	P8DPXR	H'********
Plane 8 display position Y register	P8DPYR	H'********
Plane 8 display area start address 0 register	P8DSA0R	H'********
Plane 8 display area start address 1 register	P8DSA1R	H'********
Plane 8 display area start address 2 register	P8DSA2R	H'********
Plane 8 start position X register	P8SPXR	H'********
Plane 8 start position Y register	P8SPYR	H'********
Plane 8 wrap-around start position register	P8WASPR	H'********

Register Name	Abbr.	Power-on Reset
Plane 8 wrap-around memory width register	P8WAMWR	H'********
Plane 8 blinking time register	P8BTR	H'****0101
Plane 8 transparent color 1 register	P8TC1R	H'********
Plane 8 transparent color 2 register	P8TC2R	H'********
Plane 8 transparent color 3 register	P8TC3R	H'********
Plane 8 memory length register	P8MLR	H'****0000
Plane 8 swap control register	P8SWAPR	H'*******0
Plane 8 display data control register	P8DDCR	H'********
Plane 8 display data control 2 register	P8DDC2R	H'********
Plane 8 display data control 4 register	P8DDC4R	H'********

(e) Alpha-ratio Plane Register Configuration

Table 20.10 Alpha-ratio Plane Register Configuration (1)

Base address: DU0: H'FEB0 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
Alpha-ratio plane 1 mode register	AP1MR	R/W	H'A100	32 bits	All bits
Alpha-ratio plane 1 memory width register	AP1MWR	R/W	H'A104	32 bits	All bits
Alpha-ratio plane 1 display size X register	AP1DSXR	R/W	H'A110	32 bits	All bits
Alpha-ratio plane 1 display size Y register	AP1DSYR	R/W	H'A114	32 bits	All bits
Alpha-ratio plane 1 display position X register	AP1DPXR	R/W	H'A118	32 bits	All bits
Alpha-ratio plane 1 display position Y register	AP1DPYR	R/W	H'A11C	32 bits	All bits
Alpha-ratio plane 1 display area start address 0 register	AP1DSA0R	R/W	H'A120	32 bits	All bits
Alpha-ratio plane 1 display area start address 1 register	AP1DSA1R	R/W	H'A124	32 bits	All bits
Alpha-ratio plane 1 start position X register	AP1SPXR	R/W	H'A130	32 bits	All bits
Alpha-ratio plane 1 start position Y register	AP1SPYR	R/W	H'A134	32 bits	All bits
Alpha-ratio plane 1 wrap-around start position register	AP1WASPR	R/W	H'A138	32 bits	All bits
Alpha-ratio plane 1 wrap-around memory width register	AP1WAMWR	R/W	H'A13C	32 bits	All bits
Alpha-ratio plane 1 blinking time register	AP1BTR	R/W	H'A140	32 bits	All bits
Alpha-ratio plane 1 memory length register	AP1MLR	R/W	H'A150	32 bits	All bits
Alpha-ratio plane 1 swap control register	AP1SWAPR	R/W	H'A180	32 bits	All bits
Alpha-ratio plane 2 mode register	AP2MR	R/W	H'A200	32 bits	All bits
Alpha-ratio plane 2 memory width register	AP2MWR	R/W	H'A204	32 bits	All bits
Alpha-ratio plane 2 display size X register	AP2DSXR	R/W	H'A210	32 bits	All bits
Alpha-ratio plane 2 display size Y register	AP2DSYR	R/W	H'A214	32 bits	All bits
Alpha-ratio plane 2 display position X register	AP2DPXR	R/W	H'A218	32 bits	All bits
Alpha-ratio plane 2 display position Y register	AP2DPYR	R/W	H'A21C	32 bits	All bits
Alpha-ratio plane 2 display area start address 0 register	AP2DSA0R	R/W	H'A220	32 bits	All bits
Alpha-ratio plane 2 display area start address 1 register	AP2DSA1R	R/W	H'A224	32 bits	All bits
Alpha-ratio plane 2 start position X register	AP2SPXR	R/W	H'A230	32 bits	All bits
Alpha-ratio plane 2 start position Y register	AP2SPYR	R/W	H'A234	32 bits	All bits
Alpha-ratio plane 2 wrap-around start position register	AP2WASPR	R/W	H'A238	32 bits	All bits
Alpha-ratio plane 2 wrap-around memory width register	AP2WAMWR	R/W	H'A23C	32 bits	All bits
Alpha-ratio plane 2 blinking time register	AP2BTR	R/W	H'A240	32 bits	All bits
Alpha-ratio plane 2 memory length register	AP2MLR	R/W	H'A250	32 bits	All bits
Alpha-ratio plane 2 swap control register	AP2SWAPR	R/W	H'A280	32 bits	All bits
Alpha-ratio plane n display data control 4 register	APnDDC4R	R/W	H'A#90	32 bits	All bits

Note: #: Replaces n (in hexadecimal) in addresses.
n = 1, 2

Table 20.11 Alpha-ratio Plane Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Alpha-ratio plane 1 mode register	AP1MR	H'********
Alpha-ratio plane 1 memory width register	AP1MWR	H'********
Alpha-ratio plane 1 display size X register	AP1DSXR	H'********
Alpha-ratio plane 1 display size Y register	AP1DSYR	H'********
Alpha-ratio plane 1 display position X register	AP1DPXR	H'********
Alpha-ratio plane 1 display position Y register	AP1DPYR	H'********
Alpha-ratio plane 1 display area start address 0 register	AP1DSA0R	H'********
Alpha-ratio plane 1 display area start address 1 register	AP1DSA1R	H'********
Alpha-ratio plane 1 start position X register	AP1SPXR	H'********
Alpha-ratio plane 1 start position Y register	AP1SPYR	H'********
Alpha-ratio plane 1 wrap-around start position register	AP1WASPR	H'********
Alpha-ratio plane 1 wrap-around memory width register	AP1WAMWR	H'********
Alpha-ratio plane 1 blinking time register	AP1BTR	H'****0101
Alpha-ratio plane 1 memory length register	AP1MLR	H'****0000
Alpha-ratio plane 1 swap control register	AP1SWAPR	H'*******0
Alpha-ratio plane 2 mode register	AP2MR	H'********
Alpha-ratio plane 2 memory width register	AP2MWR	H'********
Alpha-ratio plane 2 display size X register	AP2DSXR	H'********
Alpha-ratio plane 2 display size Y register	AP2DSYR	H'********
Alpha-ratio plane 2 display position X register	AP2DPXR	H'********
Alpha-ratio plane 2 display position Y register	AP2DPYR	H'********
Alpha-ratio plane 2 display area start address 0 register	AP2DSA0R	H'********
Alpha-ratio plane 2 display area start address 1 register	AP2DSA1R	H'********
Alpha-ratio plane 2 start position X register	AP2SPXR	H'********
Alpha-ratio plane 2 start position Y register	AP2SPYR	H'********
Alpha-ratio plane 2 wrap-around start position register	AP2WASPR	H'********
Alpha-ratio plane 2 wrap-around memory width register	AP2WAMWR	H'********
Alpha-ratio plane 2 blinking time register	AP2BTR	H'****0101
Alpha-ratio plane 2 memory length register	AP2MLR	H'****0000
Alpha-ratio plane 2 swap control register	AP2SWAPR	H'*******0
Alpha-ratio plane n display data control 4 register	APnDDC4R	H'********

(f) Display Capture Register Configuration

Table 20.12 Display Capture Register Configuration (1)

Base address: DU0: H'FEB0 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
Display capture mode register	DCMR	R/W	H'C100	32 bits	All bits
Display capture memory width register	DCMWR	R/W	H'C104	32 bits	All bits
Display capture area start address register	DCSAR	R/W	H'C120	32 bits	All bits
Display capture memory length register	DCMLR	R/W	H'C150	32 bits	All bits
Display capture 2 mode register	DC2MR	R/W	H'C200	32 bits	All bits
Display capture 2 memory width register	DC2MWR	R/W	H'C204	32 bits	All bits
Display capture 2 area start address register	DC2SAR	R/W	H'C220	32 bits	All bits
Display capture 2 memory length register	DC2MLR	R/W	H'C250	32 bits	All bits

Table 20.13 Display Capture Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Display capture mode register	DCMR	H'****00**
Display capture memory width register	DCMWR	H'********
Display capture area start address register	DCSAR	H'********
Display capture memory length register	DCMLR	H'****0000
Display capture 2 mode register	DC2MR	H'****00**
Display capture 2 memory width register	DC2MWR	H'********
Display capture 2 area start address register	DC2SAR	H'********
Display capture 2 memory length register	DC2MLR	H'****0000

(g) Color Palette Register Configuration

Table 20.14 Color Palette Register Configuration (1)

Base address: DU0: H'FEB0 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
Color palette 1_000 register	CP1_000R	R/W	H'1000	32 bits	All bits
		to			
Color palette 1_255 register	CP1_255R	R/W	H'13FC	32 bits	All bits
Color palette 2_000 register	CP2_000R	R/W	H'2000	32 bits	All bits
		to			
Color palette 2_255 register	CP2_255R	R/W	H'23FC	32 bits	All bits
Color palette 3_000 register	CP3_000R	R/W	H'3000	32 bits	All bits
		to			
Color palette 3_255 register	CP3_255R	R/W	H'33FC	32 bits	All bits
Color palette 4_000 register	CP4_000R	R/W	H'4000	32 bits	All bits
		to			
Color palette 4_255 register	CP4_255R	R/W	H'43FC	32 bits	All bits

Table 20.15 Color Palette Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Color palette 1_000 register	CP1_000R	H'********
	to	
Color palette 1_255 register	CP1_255R	H'********
Color palette 2_000 register	CP2_000R	H'********
	to	
Color palette 2_255 register	CP2_255R	H'********
Color palette 3_000 register	CP3_000R	H'********
	to	
Color palette 3_255 register	CP3_255R	H'********
Color palette 4_000 register	CP4_000R	H'********
	to	
Color palette 4_255 register	CP4_255R	H'********

(h) External Synchronization Control Register Configuration

Table 20.16 External Synchronization Control Register Configuration (1)

Base address: DU0: H'FEB1 0000 (suffix 0)
DU1: H'FEB3 1000 (suffix 1)

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
External synchronization control register n	ESCR0	R/W	H'0000	32 bits	None
	ESCR1				
Output signal timing adjustment register n	OTAR0	R/W	H'0004	32 bits	All bits updated with DRES
	OTAR1				

Note: n = 0 and 1

Table 20.17 External Synchronization Control Register Configuration (2)

Register Name	Abbr.	Power-on Reset
External synchronization control register n	ESCR0	H'*******0
	ESCR1	
Output signal timing adjustment register n	OTAR0	H'********
	OTAR1	

Note: n = 0 and 1

(i) Dual Display Output Control Register Configuration

Table 20.18 Dual Display Output Control Register Configuration (1)

Base address: DU0: H'FEB1 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
Display unit output route control register	DORCR	R/W	H'1000	32 bits	All bits updated with DRES
Display plane timing select register	DPTSR	R/W	H'1004	32 bits	All bits updated with DRES
Display alpha-ratio plane timing select register	DAPTSR	R/W	H'1008	32 bits	All bits updated with DRES
Display superimpose 0 priority register	DS0PR	R/W	H'1020	32 bits	All bits
Display superimpose 1 priority register	DS1PR	R/W	H'1024	32 bits	All bits

Table 20.19 Dual Display Output Control Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Display unit output route control register	DORCR	H'********
Display plane timing select register	DPTSR	H'**00**00
Display alpha-ratio plane timing select register	DAPTSR	H'********
Display superimpose 0 priority register	DS0PR	H'00000000
Display superimpose 1 priority register	DS1PR	H'00000000

(j) YC-RGB Conversion Coefficient Register Configuration

Table 20.20 YC-RGB Conversion Coefficient Register Configuration (1)

Base address: DU0: H'FEB1 1000

Register Name	Abbr.	R/W	Address in P4	Access Size	Bit with Internal Update Function
Y normalization coefficient register	YNCR	R/W	H'80	32 bits	All bits
Y normalization offset register	YNOR	R/W	H'84	32 bits	All bits
Cr normalization offset register	CRNOR	R/W	H'88	32 bits	All bits
Cb normalization offset register	CBNOR	R/W	H'8C	32 bits	All bits
Red Cr coefficient register	RCRCR	R/W	H'90	32 bits	All bits
Green Cr coefficient register	GCRCR	R/W	H'94	32 bits	All bits
Green Cb coefficient register	GCBCR	R/W	H'98	32 bits	All bits
Blue Cb coefficient register	BCBCR	R/W	H'9C	32 bits	All bits

Table 20.21 YC-RGB Conversion Coefficient Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Y normalization coefficient register	YNCR	H'*800*800
Y normalization offset register	YNOR	H'**00**00
Cr normalization offset register	CRNOR	H'**80**80
Cb normalization offset register	CBNOR	H'**80**80
Red Cr coefficient register	RCRCR	H'*AF0*AF0
Green Cr coefficient register	GCRCR	H'*590*590
Green Cb coefficient register	GCBCR	H'*2B0*2B0
Y Blue Cb coefficient register	BCBCR	H'*DE0*DE0

(k) RGB-YC Conversion Coefficient Register Configuration

Table 20.22 RGB-YC Conversion Coefficient Register Configuration (1)

Base address: DU0: H'FEB1 0000

Register Name	Abbr.	R/W	Offset Address	Access Size	Bit with Internal Update Function
Y calculation R coefficient register	YCLRP	R/W	H'4000	32 bits	All bits
Y calculation G coefficient register	YCLGP	R/W	H'4004	32 bits	All bits
Y calculation B coefficient register	YCLBP	R/W	H'4008	32 bits	All bits
Y calculation addition constant register	YCLAP	R/W	H'400C	32 bits	All bits
Cb calculation R coefficient register	CBCLRP	R/W	H'4010	32 bits	All bits
Cb calculation G coefficient register	CBCLGP	R/W	H'4014	32 bits	All bits
Cb calculation B coefficient register	CBCLBP	R/W	H'4018	32 bits	All bits
Cb calculation addition constant register	CBCLAP	R/W	H'401C	32 bits	All bits
Cr calculation R coefficient register	CRCLRP	R/W	H'4020	32 bits	All bits
Cr calculation G coefficient register	CRCLGP	R/W	H'4024	32 bits	All bits
Cr calculation B coefficient register	CRCLBP	R/W	H'4028	32 bits	All bits
Cr calculation addition constant register	CRCLAP	R/W	H'402C	32 bits	All bits

Table 20.23 RGB-YC Conversion Coefficient Register Configuration (2)

Register Name	Abbr.	Power-on Reset
Y calculation R coefficient register	YCLRP	H'*264*264
Y calculation G coefficient register	YCLGP	H'*4B2*4B2
Y calculation B coefficient register	YCLBP	H'*0E9*0E9
Y calculation addition constant register	YCLAP	H'**10**10
Cb calculation R coefficient register	CBCLRP	H'*15A*15A
Cb calculation G coefficient register	CBCLGP	H'*2A5*2A5
Cb calculation B coefficient register	CBCLBP	H'*400*400
Cb calculation addition constant register	CBCLAP	H'**80**80
Cr calculation R coefficient register	CRCLRP	H'*400*400
Cr calculation G coefficient register	CRCLGP	H'*35A*35A
Cr calculation B coefficient register	CRCLBP	H'*0A5*0A5
Cr calculation addition constant register	CRCLAP	H'**80**80

20.3 Register Description

Legend for Register Description

Initial value: Register value after a reset.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R: Read-only. The write value should always be 0.

—/W: Write-only. The read value is undefined.

Plane n: Indicates plane 1 to plane 8

Note: Do not access locations that appear empty in the address map. Operation is not guaranteed in case of access to change the value at any location other than those of the registers listed in Tables 20.2 to 20.23.

20.3.1 Display Unit System Control Registers

20.3.1.1 Display Unit System Control Register 0 (DSYSR0)

Address: DU0: H'FEB0 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	ILTS	—	—	—	—	—	—	—	—	DSEC	—	—	—	IUPD
Initial value:	—	—	0	—	—	—	—	—	—	—	—	0	—	—	—	0
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	DRES	DEN	TVM		SCM		—	—	—	—
Initial value:	—	—	—	—	—	—	1	0	1	0	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
29	ILTS	0	R/W	Not available	Input Pad Latch Timing Select To enable this bit, the DEFE bit in the display unit extensional function control register 0 (DEFR0) should be set to 1. In the initial state, this bit is fixed to 0. 0: A signal of the input pad is latched at the DCLKIN rising edge. 1: A signal of the input pad is latched at the DCLKIN falling edge. Electrical characteristics do not apply.
28 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	DSEC	0	R/W	Available	Display Data Endian Change For details on data swapping, see section 20.4.7, Endian Conversion. 0: Display data on memory is not swapped in byte or word units. 1: Display data on memory is swapped in byte or word units.
19 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16	IUPD	0	R/W	Not available	Internal Updating Disable When DRES = 1, internal register updating occurs regardless of this bit setting. For details on internal updating, see section 20.2 (2), Internal Update. 0: Internal register updating occurs for each vertical synchronous signal (VSYNC) assertion. 1: If this bit is set to 1, internal register updating does not occur. • If this bit is set to 0, register updating occurs according to the next vertical synchronous signal (VSYNC). • This bit is shared by DU0 and DU1.
15 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	DRES	1	R/W	Not available	Display Reset
8	DEN	0	R/W	Available	Display Enable 00: Display synchronous operation starts. If any register has not been set yet, the display unit may perform unexpected operation, thus set DRES to 0 after setting all registers in the display unit. For DEN = 0, the display data becomes values set with the display off mode output register n (DOORn). 01: Display synchronous operation starts. If any register has not been set yet, the display unit may perform unexpected operation, thus set DRES = 0, DEN = 1 after setting all registers in the display unit. To re-set DRES to 1 following the start of operations for synchronization of the display with this setting, proceed with steps 1 and 2 in section 20.6.2, Transition to Module Standby Mode before doing so. For DEN = 1, the display data becomes values stored on the unified memory from the next frame. 10: Display operation stops. Display operation and synchronization operation stop. The set values except for the following bits in the display unit status register n (DSSRn) are retained. In this setting, the following operations occur: 1. All 0s are output as display data. 2. The following bits of the display unit status register n (DSSRn) are cleared to 0: TV synchronization signal error flag (TVR and TVR1) Frame flag (FRM and FRM1) Vertical blanking flag (VBK and VBK1) Raster interrupt flag (RINT and RINT1) Horizontal blanking flag (HBK and HBK1) 3. HSYNC, VSYNC, and ODDF pins function as inputs. However, the ODDF pin functions as a CLAMP output when the ODPM bit in the display unit mode register 0 (DSMR0) is 1. 11: Setting prohibited • This bit is shared by DU0 and DU1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7, 6	TVM	10	R/W	Not available	TV Synchronized Mode 00: Master Mode HSYNC, VSYNC, and CSYNC are output. 01: The switching mode of synchronous mode is set. Use this mode if necessary when switching from TV synchronized mode to master mode or vice versa is performed. In this mode, display operation forcibly stops and the DISP pin outputs the low level. Moreover, clock supply to DCLKIN can be stopped (input invalid) (the inside of the LSI is fixed to the high level). The EXHSYNC, EXVSYNC, and EXODDF pins are used as input pins. 10: TV synchronized mode EXHSYNC, EXVSYNC, and EXODDF are input. When the ODPM bit in the display unit mode register 0 (DSMR0) is set to 1, the ODDF pin functions as an output pin. 11: Setting prohibited
5, 4	SCM	00	R/W	Not available	Scan Mode 00: Non-interlaced mode 01: Setting prohibited 10: Interlace sync mode 11: Interlace sync & video mode
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: n = 0 and 1

20.3.1.2 Display Unit System Control Register 1 (DSYSR1)

Address: DU1: H'FEB3 0000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	ILTS1	—	—	—	—	—	—	—	—	DSEC1	—	—	—	—
Initial value:	—	—	0	—	—	—	—	—	—	—	—	0	—	—	—	—
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TVM1		SCM1		—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

- Bits 16, 9, and 8 of display unit system control register 0 (DSYSR0) are shared by DU0 and DU1. Thus, the bits in this register do not have a function.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
29	ILTS1	0	R/W	Not available	Input Pad Latch Timing Select 1 To enable this bit, the DEFE bit in the display unit extensional function control register 0 (DEFR0) should be set to 1. In the initial state, this bit is fixed to 0. 0: A signal of the input pad is latched at the DCLKIN rising edge. 1: A signal of the input pad is latched at the DCLKIN falling edge. Electrical characteristics do not apply.
28 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	DSEC1	0	R/W	Available	Display Data Endian Change 1 For details on data swapping, see section 20.4.7, Endian Conversion. 0: Display data on memory is not swapped in byte or word units. 1: Display data on memory is swapped in byte or word units.
19 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7, 6	TVM1	10	R/W	Not available	TV Synchronized Mode 1 00: Master Mode HSYNC, VSYNC, and CSYNC are output. 01: The switching mode of synchronous mode is set. Use this mode if necessary when switching from TV synchronized mode to master mode or vice versa is performed. In this mode, display operation forcibly stops and the DISP pin outputs the low level. Moreover, clock supply to DCLKIN can be stopped (input invalid) (the inside of the LSI is fixed to the high level). The EXHSYNC, EXVSYNC, and EXODDF pins are used as input pins. 10: TV synchronized mode EXHSYNC, EXVSYNC, and EXODDF are input. When the ODPM bit in the display unit mode register 1 (DSMR1) is set to 1, the ODDF pin functions as an output pin. 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5, 4	SCM1	00	R/W	Not available	Scan Mode 1 00: Non-interlaced mode 01: Setting prohibited 10: Interlace sync mode 11: Interlace sync & video mode
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.3 Display Unit Mode Register n (DSMRn)

Note: n = 0 and 1

Address: DU0: H'FEB0 0004, DU1: H'FEB3 0004

All bit in this register setting is also available for the display data output via the LVDS.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VSPM	ODPM	DIPM		CSPM	—	—	—	—	DIL	VSL	HSL	DDIS
Initial value:	—	—	—	0	0	0	0	0	—	—	—	—	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDEL	CDEM		CDED	—	—	—	ODEV	CSY		—	—	—	—	—	—
Initial value:	0	0	0	0	—	—	—	0	0	0	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28	VSPM	0	R/W	DRES	VSYNC Pin Mode 0: The VSYNC signal is output to the VSYNC pin. 1: The CSYNC signal is output to the VSYNC pin. "VSYNC pin" refers to the DU0_VSYNC/DU0_EXVSYNC pin indicated in Table 20.1a or the DU1_VSYNC/DU1_EXVSYNC pin indicated in Table 20.1b.
27	ODPM	0	R/W	DRES	ODDF Pin Mode 0: The ODDF signal is output to the ODDF pin. 1: The CLAMP signal is output to the ODDF pin. Even if bits 7 and 6 in the display unit system control register n (DSYSRn) indicate TV synchronized mode, the ODDF pin becomes an output. "ODDF pin" refers to the DU0_ODDF/DU0_EXODDF pin indicated in Table 20.1a or the DU1_ODDF/DU1_EXODDF pin indicated in Table 20.1b.
26, 25	DIPM	00	R/W	DRES	DISP Pin Mode 00: The DISP signal is output to the DISP pin. 01: The CSYNC signal is output to the DISP pin. 10: Setting prohibited. (Fixed to 0.) 11: The DE signal is output to the DISP pin. "DISP pin" refers to the DU0_ DISP pin indicated in Table 20.1a or the DU1_ DISP pin indicated in Table 20.1b.
24	CSPM	0	R/W	DRES	CSYNC Pin Mode 0: The CSYNC signal is output to the CSYNC pin. 1: The HSYNC signal is output to the CSYNC pin. "CSYNC pin" refers to the DU0_HSYNC/DU0_EXHSYNC pin indicated in Table 20.1a or the DU1_HSYNC/DU1_EXHSYNC pin indicated in Table 20.1b.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
23 to 20	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
19	DIL	0	R/W	DRES	DISP Polarity Select 0: The DISP signal becomes a high level during display period. 1: The polarity of the DISP signal is inverted.
18	VSL	0	R/W	DRES	VSYNC Polarity Select 0: The VSYNC signal becomes active low. 1: The polarity of VSYNC is inverted.
17	HSL	0	R/W	DRES	HSYNC Polarity Select 0: The HSYNC signal becomes active low. 1: The polarity of the HSYNC signal is inverted.
16	DDIS	0	R/W	Available	DISP Disable 0: The DISP signal is output. 1: The DISP signal is not output.
15	CDEL	0	R/W	Available	CDE Polarity Select 0: The CDE signal becomes high when the output display data and color detection register n (CDERn) match. 1: The polarity of the CDE signal is inverted.
14, 13	CDEM	00	R/W	Available	CDE Output Mode 00: The CDE signal is output as is. 01: The CDE signal is output as is. 10: The low level is output outside the display period. 11: The high level is output outside the display period.
12	CDED	0	R/W	Available	CDE Disable 0: The CDE signal is output. 1: The CDE signal output is prohibited.
11 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8	ODEV	0	R/W	Available	Odd Even Location for ODDF Signal 0: The odd field (ODDF = low) is located in the first half of the same frame of the interlace display. 1: The odd field (ODDF = low) is located in the second half of the same frame of the interlace display.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7, 6	CSY	00	R/W	Available	CSYNC Mode 00: A waveform obtained by performing exclusive logical OR for VSYNC and HSYNC is output as CSYNC. 01: Setting prohibited 10: During intervals of 3 rasters from the VSYNC falling edge, the equalizing pulse is output. After that, during intervals of 3 rasters, the serration pulse is output. After that, during intervals of 3 rasters, the equalizing pulse is output. During other intervals, the HSYNC waveform is output as CSYNC. 11: After 1/2 rasters from the VSYNC falling edge, the equalizing pulse is output during intervals of 2.5 rasters. After that, during intervals of 2.5 rasters, the serration pulse is output. After that, during intervals of 2.5 rasters, the equalizing pulse is output. During other intervals, the HSYNC waveform is output as CSYNC.
5 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.4 Display Unit Status Register 0 (DSSR0)

Address: DU0: H'FEB0 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	VC1FB		VC0FB		—		DFB10	DFB9	DFB8	DFB7	DFB6	DFB5	DFB4	DFB3	DFB2	DFB1
Initial value:	0	0	1	1	—	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR	FRM	—	BUF	VBK	—	RINT	HBK	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1
Initial value:	0	0	—	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * For reserved bit (bit name: —), initial value is undefined. For details, refer to following table.

- Video capture is the same as video input.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31, 30	VC1FB	00	R	Not available	Video Capture 1 Frame Buffer Flag Set the DEFE bit in the display unit extensional function control register 0 (DEFR0) to 1 to enable bits 31 and 30. In the initial state, bits 31 and 30 are fixed to 0. 00: In the plane set for video capture 1, the address indicated with PnDSA0R* is in use as the display area start address. 01: In the plane set for video capture 1, the address indicated with PnDSA1R* is in use as the display area start address. 10: In the plane set for video capture 1, the address indicated with PnDSA2R* is in use as the display area start address. 11: The video capture 1 module is in the initial state.
29, 28	VC0FB	11	R	Not available	Video Capture 0 Frame Buffer Flag 00: In the plane set for video capture 0, the address indicated with PnDSA0R* is in use as the display area start address. 01: In the plane set for video capture 0, the address indicated with PnDSA1R* is in use as the display area start address. 10: In the plane set for video capture 0, the address indicated with PnDSA2R* is in use as the display area start address. 11: The video capture 0 module is in the initial state.
27, 26	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
25	DFB10	0	R	Not available	Display Frame Buffer 10 Flag 0: In α plane 2, the address indicated with AP2DSA0R is in use as the display area start address. 1: In α plane 2, the address indicated with AP2DSA1R is in use as the display area start address.
24	DFB9	0	R	Not available	Display Frame Buffer 9 Flag 0: In α plane 1, the address indicated with AP1DSA0R is in use as the display area start address. 1: In α plane 1, the address indicated with AP1DSA1R is in use as the display area start address.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
23	DFB8	0	R	Not available	Display Frame Buffer 8 Flag 0: In plane 8, the address indicated with P8DSA0R is in use as the display area start address. 1: In plane 8, the address indicated with P8DSA1R is in use as the display area start address.
22	DFB7	0	R	Not available	Display Frame Buffer 7 Flag 0: In plane 7, the address indicated with P7DSA0R is in use as the display area start address. 1: In plane 7, the address indicated with P7DSA1R is in use as the display area start address.
21	DFB6	0	R	Not available	Display Frame Buffer 6 Flag 0: In plane 6, the address indicated with P6DSA0R is in use as the display area start address. 1: In plane 6, the address indicated with P6DSA1R is in use as the display area start address.
20	DFB5	0	R	Not available	Display Frame Buffer 5 Flag 0: In plane 5, the address indicated with P5DSA0R is in use as the display area start address. 1: In plane 5, the address indicated with P5DSA1R is in use as the display area start address.
19	DFB4	0	R	Not available	Display Frame Buffer 4 Flag 0: In plane 4, the address indicated with P4DSA0R is in use as the display area start address. 1: In plane 4, the address indicated with P4DSA1R is in use as the display area start address.
18	DFB3	0	R	Not available	Display Frame Buffer 3 Flag 0: In plane 3, the address indicated with P3DSA0R is in use as the display area start address. 1: In plane 3, the address indicated with P3DSA0R is in use as the display area start address.
17	DFB2	0	R	Not available	Display Frame Buffer 2 Flag 0: In plane 2, the address indicated with P2DSA0R is in use as the display area start address. 1: In plane 2, the address indicated with P2DSA1R is in use as the display area start address.
16	DFB1	0	R	Not available	Display Frame Buffer 1 Flag 0: In plane 1, the address indicated with P1DSA0R is in use as the display area start address. 1: In plane 1, the address indicated with P1DSA1R is in use as the display area start address.
15	TVR	0	R	Not available	TV Synchronization Error Flag 0: Indicates that, after the TVR bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL bit of the display unit status register clear register 0 (DSRCR0), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0). 1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0). The TVR bit retains its status until it is cleared with the DRES or TVCL bit.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
14	FRM	0	R	Not available	Frame Flag 0: Indicates the period from the time when the FRM bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL bit of the display unit status register clear register 0 (DSRCR0) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync & video mode. 1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM bit is cleared by the DRES or FRCL bit, to the time when the FRM bit is cleared again.
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUF	0	R	Not available	Buffer Underflow Flag Set the DEFE8 bit in the display unit extensional function control register (DEF8R) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: The buffer underflow has not occurred. 1: The buffer underflow has occurred.
11	VBK	0	R	Not available	Vertical Blanking Flag 0: Indicates the period from the time when the VBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL bit of the display unit status register clear register 0 (DSRCR0) to the time when display of the next field is completed. 1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK bit is cleared by the DRES or VBCL bit, to the time when the VBK bit is cleared again.
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RINT	0	R	Not available	Raster Interrupt Flag 0: Indicates the period from the time when the RINT bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL bit of the display unit status register clear register 0 (DSRCR0) to the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display. 1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display after the RINT bit is cleared by the DRES or RICL bit, to the time when the RINT bit is cleared again.
8	HBK	0	R	Not available	Horizontal Blanking Flag 0: Indicates the period from the time when the HBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL bit of the display unit status register clear register 0 (DSRCR0) to the time of the next HSYNC assertion. 1: Indicates the period from the start of the first horizontal blanking period after the HBK bit is cleared by the DRES or HBCL bit, to the time when the HBK bit is cleared again.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
7	ADC8	0	R	Not available	Auto Rendering Display Change Flag 8 0: Indicates that the frame buffer for plane 8 has not been switched. 1: Indicates that the frame buffer for plane 8 has been switched. The ADC8 bit state is held until it is cleared.
6	ADC7	0	R	Not available	Auto Rendering Display Change Flag 7 0: Indicates that the frame buffer for plane 7 has not been switched. 1: Indicates that the frame buffer for plane 7 has been switched. The ADC7 bit state is held until it is cleared.
5	ADC6	0	R	Not available	Auto Rendering Display Change Flag 6 0: Indicates that the frame buffer for plane 6 has not been switched. 1: Indicates that the frame buffer for plane 6 has been switched. The ADC6 bit state is held until it is cleared.
4	ADC5	0	R	Not available	Auto Rendering Display Change Flag 5 0: Indicates that the frame buffer for plane 5 has not been switched. 1: Indicates that the frame buffer for plane 5 has been switched. The ADC5 bit state is held until it is cleared.
3	ADC4	0	R	Not available	Auto Rendering Display Change Flag 4 0: Indicates that the frame buffer for plane 4 has not been switched. 1: Indicates that the frame buffer for plane 4 has been switched. The ADC4 bit state is held until it is cleared.
2	ADC3	0	R	Not available	Auto Rendering Display Change Flag 3 0: Indicates that the frame buffer for plane 3 has not been switched. 1: Indicates that the frame buffer for plane 3 has been switched. The ADC3 bit state is held until it is cleared.
1	ADC2	0	R	Not available	Auto Rendering Display Change Flag 2 0: Indicates that the frame buffer for plane 2 has not been switched. 1: Indicates that the frame buffer for plane 2 has been switched. The ADC2 bit state is held until it is cleared.
0	ADC1	0	R	Not available	Auto Rendering Display Change Flag 1 0: Indicates that the frame buffer for plane 1 has not been switched. 1: Indicates that the frame buffer for plane 1 has been switched. The ADC1 bit state is held until it is cleared.

Note: * n = 1 to 8

- Description of the ADC bits

  For animation, although the display of moving images can be performed in auto rendering mode, at this time

  1. A check for a TRAP interrupt proceeds,
  2. A check for a VBK interrupt proceeds, and
  3. Rendering starts after a VBK interrupt has occurred, so two rounds of flag checking are required before this.

  With these flag bits (ADC), an ADC interrupt is generated after a single flag check, and rendering can then start.

20.3.1.5 Display Unit Status Register 1 (DSSR1)

Address: DU1: H'FEB3 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR1	FRM1	—	—	VBK1	—	RINT1	HBK1	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * For reserved bit (bit name: —), initial value is undefined. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR1	0	R	Not available	TV Synchronization Error Flag 1 0: Indicates that, after the TVR1 bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL1 bit of the display unit status register clear register 1 (DSRCR1), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1). 1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1). The TVR1 bit retains its status until it is cleared with the DRES or TVCL1 bit.
14	FRM1	0	R	Not available	Frame Flag 1 0: Indicates the period from the time when the FRM1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL1 bit of the display unit status register clear register 1 (DSRCR1) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync & video mode. 1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM1 bit is cleared by the DRES or FRCL1 bit, to the time when the FRM1 bit is cleared again.
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	VBK1	0	R	Not available	Vertical Blanking Flag 1 0: Indicates the period from the time when the VBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL1 bit of the display unit status register clear register 1 (DSRCR1) to the time when display of the next field is completed. 1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK1 bit is cleared by the DRES or VBCL1 bit, to the time when the VBK1 bit is cleared again.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RINT1	0	R	Not available	Raster Interrupt Flag 1 0: Indicates the period from the time when the RINT1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL1 bit of the display unit status register clear register 1 (DSRCR1) to the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFSR1) has elapsed after the beginning of the next field display. 1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFS1) has elapsed after the beginning of the next field display after the RINT1 bit is cleared by the DRES or RICL1 bit, to the time when the RINT1 bit is cleared again.
8	HBK1	0	R	Not available	Horizontal Blanking Flag 1 0: Indicates the period from the time when the HBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL1 bit of the display unit status register clear register 1 (DSRCR1) to the time of the next HSYNC assertion. 1: Indicates the period from the start of the first horizontal blanking period after the HBK1 bit is cleared by the DRES or HBCL1 bit, to the time when the HBK1 bit is cleared again.
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.6 Display Unit Status Register Clear Register 0 (DSRCR0)

Address: DU0: H'FEB0 000C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVCL	FRCL	—	BUFL	VBCL	—	RICL	HBCL	ADCL8	ADCL7	ADCL6	ADCL5	ADCL4	ADCL3	ADCL2	ADCL1
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	R	—/W	—/W	R	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVCL	—	—/W	Not available	TV Synchronization Signal Error Flag Clear 0: Does not change the TVR flag in the display unit status register 0 (DSSR0). 1: Clears the TVR flag in the display unit status register 0 (DSSR0).
14	FRCL	—	—/W	Not available	Frame Flag Clear 0: Does not change the FRM flag in the display unit status register 0 (DSSR0). 1: Clears the FRM flag in the display unit status register 0 (DSSR0).
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUFL	—	—/W	Not available	Buffer Underflow Flag Clear Set the DEFE8 bit in the display unit extensional function control 8 register (DEF8R) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: Does not change the BUF flag in the display unit status register 0 (DSSR0). 1: Clear the BUF flag in the display unit status register 0 (DSSR0).
11	VBCL	—	—/W	Not available	Vertical Blanking Flag Clear 0: Does not change the VBK flag in the display unit status register 0 (DSSR0). 1: Clears the VBK flag in the display unit status register 0 (DSSR0).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RICL	—	—/W	Not available	Raster Interrupt flag clear 0: Does not change the RINT flag in the display unit status register 0 (DSSR0). 1: Clears the RINT flag in the display unit status register 0 (DSSR0).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
8	HBCL	—	—/W	Not available	HBK flag clear 0: Does not change the HBK flag in the display unit status register 0 (DSSR0). 1: Clears the HBK flag in the display unit status register 0 (DSSR0).
7	ADCL8	—	—/W	Not available	Auto Rendering Display Change Flag Clear 8 0: Does not change the ADC flag 8 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 8 in the display unit status register 0 (DSSR0).
6	ADCL7	—	—/W	Not available	Auto Rendering Display Change Flag Clear 7 0: Does not change the ADC flag 7 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 7 in the display unit status register 0 (DSSR0).
5	ADCL6	—	—/W	Not available	Auto Rendering Display Change Flag Clear 6 0: Does not change the ADC flag 6 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 6 in the display unit status register 0 (DSSR0).
4	ADCL5	—	—/W	Not available	Auto Rendering Display Change Flag Clear 5 0: Does not change the ADC flag 5 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 5 in the display unit status register 0 (DSSR0).
3	ADCL4	—	—/W	Not available	Auto Rendering Display Change Flag Clear 4 0: Does not change the ADC flag 4 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 4 in the display unit status register 0 (DSSR0).
2	ADCL3	—	—/W	Not available	Auto Rendering Display Change Flag Clear 3 0: Does not change the ADC flag 3 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 3 in the display unit status register 0 (DSSR0).
1	ADCL2	—	—/W	Not available	Auto Rendering Display Change Flag Clear 2 0: Does not change the ADC flag 2 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 2 in the display unit status register 0 (DSSR0).
0	ADCL1	—	—/W	Not available	Auto Rendering Display Change Flag Clear 1 0: Does not change the ADC flag 1 in the display unit status register 0 (DSSR0). 1: Clears the ADC flag 1 in the display unit status register 0 (DSSR0).

20.3.1.7 Display Unit Status Register Clear Register 1 (DSRCR1)

Address: DU1: H'FEB3 000C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVCL1	FRCL1	—	—	VBCL1	—	RICL1	HBCL1	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	R	R	—/W	R	—/W	—/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVCL1	—	—/W	Not available	TV Synchronization Signal Error Flag 1 Clear 0: Does not change the TVR flag 1 in the display unit status register 1 (DSSR1). 1: Clears the TVR flag 1 in the display unit status register 1 (DSSR1).
14	FRCL1	—	—/W	Not available	Frame Flag 1 Clear 0: Does not change the FRM flag 1 in the display unit status register 1 (DSSR1). 1: Clears the FRM flag 1 in the display unit status register 1 (DSSR1).
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	VBCL1	—	—/W	Not available	Vertical Blanking Flag 1 Clear 0: Does not change the VBK flag 1 in the display unit status register 1 (DSSR1). 1: Clears the VBK flag 1 in the display unit status register 1 (DSSR1).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RICL1	—	—/W	Not available	Raster Interrupt Flag 1 Clear 0: Does not change the RINT flag 1 in the display unit status register 1 (DSSR1). 1: Clears the RINT flag 1 in the display unit status register 1 (DSSR1).
8	HBCL1	—	—/W	Not available	HBK1 Flag Clear 0: Does not change the HBK flag 1 in the display unit status register 1 (DSSR1). 1: Clears the HBK flag 1 in the display unit status register 1 (DSSR1).
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.8 Display Unit Interrupt Enable Register 0 (DIER0)

Address: DU0: H'FEB0 0010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVE	FRE	—	BUE	VBE	—	RIE	HBE	ADCE8	ADCE7	ADCE6	ADCE5	ADCE4	ADCE3	ADCE2	ADCE1
Initial value:	0	0	—	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The display unit interrupt enable register 0 (DIER0) allows the generation of interrupts for the CPU by aspects of the internal state of the display unit as reflected in bits of the display unit status register 0 (DSSR0) as the sources. When a bit of this register is set, setting of the bit in the same position within DSSR 0 will lead to the generation of an interrupt for the CPU.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVE	0	R/W	Not available	TV Synchronization Signal Error Interrupt Enable 0: Disables the TVR flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the TVR flag interrupt of the display unit status register 0 (DSSR0).
14	FRE	0	R/W	Not available	Frame Flag Interrupt Enable 0: Disables the FRM flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the FRM flag interrupt of the display unit status register 0 (DSSR0).
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUE	0	R/W	Not available	Buffer Underflow Flag Interrupt Enable Set the DEFE8 bit in the display unit extensional function control 8 register (DEF8R) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: Disables the BUF flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the BUF flag interrupt of the display unit status register 0 (DSSR0).
11	VBE	0	R/W	Not available	Vertical Blanking Flag Interrupt Enable 0: Disables the VBK flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the VBK flag interrupt of the display unit status register 0 (DSSR0).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RIE	0	R/W	Not available	Raster Interrupt Flag Interrupt Enable 0: Disables the RINT flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the RINT flag interrupt of the display unit status register 0 (DSSR0).
8	HBE	0	R/W	Not available	HBK Flag Interrupt Enable 0: Disables the HBK flag interrupt of the display unit status register 0 (DSSR0). 1: Enables the HBK flag interrupt of the display unit status register 0 (DSSR0).
7	ADCE8	0	R/W	Not available	Auto Rendering Display Change Flag 8 Interrupt Enable 0: Disables the ADC flag 8 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 8 interrupt of the display unit status register 0 (DSSR0).
6	ADCE7	0	R/W	Not available	Auto Rendering Display Change Flag 7 Interrupt Enable 0: Disables the ADC flag 7 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 7 interrupt of the display unit status register 0 (DSSR0).
5	ADCE6	0	R/W	Not available	Auto Rendering Display Change Flag 6 Interrupt Enable 0: Disables the ADC flag 6 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 6 interrupt of the display unit status register 0 (DSSR0).
4	ADCE5	0	R/W	Not available	Auto Rendering Display Change Flag 5 Interrupt Enable 0: Disables the ADC flag 5 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 5 interrupt of the display unit status register 0 (DSSR0).
3	ADCE4	0	R/W	Not available	Auto Rendering Display Change Flag 4 Interrupt Enable 0: Enables the ADC flag 4 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 4 interrupt of the display unit status register 0 (DSSR0).
2	ADCE3	0	R/W	Not available	Auto Rendering Display Change Flag 3 Interrupt Enable 0: Disables the ADC flag 3 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 3 interrupt of the display unit status register 0 (DSSR0).
1	ADCE2	0	R/W	Not available	Auto Rendering Display Change Flag 2 Interrupt Enable 0: Disables the ADC flag 2 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 2 interrupt of the display unit status register 0 (DSSR0).
0	ADCE1	0	R/W	Not available	Auto Rendering Display Change Flag 1 Interrupt Enable 0: Enables the ADC flag 1 interrupt of the display unit status register 0 (DSSR0). 1: Enables the ADC flag 1 interrupt of the display unit status register 0 (DSSR0).

The following are conditions, based on DSSR0, DIER0, DSSR1, and DIER1, for issuing an interrupt to the CPU from the DU0/DU1.
Conditions for issuing an interrupt from the DU0/DU1 = a + b + c + d + e + f + g + h + i + j + k+ l + m + n + o + p + q + r + s + t

- a = TVR & TVE
- b = FRM & FRE
- c = VBK & VBE
- d = RINT & RIE
- e = HBK & HBE
- f = ADC6 & ADCE6
- g = ADC5 & ADCE5
- h = ADC4 & ADCE4
- i = ADC3 & ADCE3
- j = ADC2 & ADCE2
- k = ADC1 & ADCE1
- l = ADC8 & ADCE8
- m = ADC7 & ADCE7
- n = TVR1 & TVE1
- o = FRM1 & FRE1
- p = VBK1 & VBE1
- q = RINT1 & RIE1
- r = HBK1 & HIBE1
- s = BUF & BUE
- t = BUK1 & BUE1

20.3.1.9 Display Unit Interrupt Enable Register 1 (DIER1)

Address: DU1: H'FEB3 0010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVE1	FRE1	—	—	VBE1	—	RIE1	HBE1	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R	R	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R

The display unit interrupt enable register 1 (DIER1) allows the generation of interrupts for the CPU by aspects of the internal state of the display unit as reflected in bits of the display unit status register 1 (DSSR1) as the sources. When a bit of this register is set, setting of the bit in the same position within DSSR1 will lead to the generation of an interrupt for the CPU.

For conditions for issuing an interrupt to the CPU from the display unit, see section 20.3.1.10, Display Unit Interrupt Enable Register 0 (DIER0).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVE1	0	R/W	Not available	TV Synchronization Signal Error Flag 1 Interrupt Enable 0: Disables the TVR flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the TVR flag 1 interrupt of the display unit status register 1 (DSSR1).
14	FRE1	0	R/W	Not available	Frame Flag 1 Interrupt Enable 0: Disables the FRM flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the FRM flag 1 interrupt of the display unit status register 1 (DSSR1).
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	VBE1	0	R/W	Not available	Vertical Blanking Flag 1 Interrupt Enable 0: Disables the VBK flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the VBK flag 1 interrupt of the display unit status register 1 (DSSR1).
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RIE1	0	R/W	Not available	Raster Interrupt Flag 1 Interrupt Enable 0: Disables the RINT flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the RINT flag 1 interrupt of the display unit status register 1 (DSSR1).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
8	HBE1	0	R/W	Not available	HBK Flag 1 Interrupt Enable 0: Disables the HBK flag 1 interrupt of the display unit status register 1 (DSSR1). 1: Enables the HBK flag 1 interrupt of the display unit status register 1 (DSSR1).
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.10 Display Unit Domain 1 Status Register 0 (DD1SSR0)

Address: DU0: H'FEB2 0008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR	FRM	—	BUF	VBK	—	RINT	HBK	ADC8	ADC7	ADC6	ADC5	ADC4	ADC3	ADC2	ADC1
Initial value:	0	0	—	0	0	—	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR	0	R	Not available	TV Synchronization Error Flag 0: Indicates that, after the TVR bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0). 1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 0 (VCR0). The TVR bit retains its status until it is cleared with the DRES or TVCL bit.
14	FRM	0	R	Not available	Frame Flag 0: Indicates the period from the time when the FRM bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync & video mode. 1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM bit is cleared by the DRES or FRCL bit, to the time when the FRM bit is cleared again.
13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	BUF	0	R	Not available	Buffer Underflow Flag Set the DEFE8 bit in the display unit extensional function control 8 register (DEF8R) to 1 to enable bit 12. In the initial state, bit 12 is fixed to 0. 0: The buffer underflow has not occurred. 1: The buffer underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	VBK	0	R	Not available	Vertical Blanking Flag 0: Indicates the period from the time when the VBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time when display of the next field is completed. 1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK bit is cleared by the DRES or VBCL bit, to the time when the VBK bit is cleared again.
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9	RINT	0	R	Not available	Raster Interrupt Flag 0: Indicates the period from the time when the RINT bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display. 1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 0 (RINTOFSR0) has elapsed after the beginning of the next field display after the RINT bit is cleared by the DRES or RICL bit, to the time when the RINT bit is cleared again.
8	HBK	0	R	Not available	Horizontal Blanking Flag 0: Indicates the period from the time when the HBK bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL bit of the display unit domain 1 status register clear register 0 (DD1SRCR0) to the time of the next HSYNC assertion. 1: Indicates the period from the start of the first horizontal blanking period after the HBK bit is cleared by the DRES or HBCL bit, to the time when the HBK bit is cleared again.
7	ADC8	0	R	Not available	Auto Rendering Display Change Flag 8 0: Indicates that the frame buffer for plane 8 has not been switched. 1: Indicates that the frame buffer for plane 8 has been switched. The ADC8 bit state is held until it is cleared.
6	ADC7	0	R	Not available	Auto Rendering Display Change Flag 7 0: Indicates that the frame buffer for plane 7 has not been switched. 1: Indicates that the frame buffer for plane 7 has been switched. The ADC7 bit state is held until it is cleared.
5	ADC6	0	R	Not available	Auto Rendering Display Change Flag 6 0: Indicates that the frame buffer for plane 6 has not been switched. 1: Indicates that the frame buffer for plane 6 has been switched. The ADC6 bit state is held until it is cleared.
4	ADC5	0	R	Not available	Auto Rendering Display Change Flag 5 0: Indicates that the frame buffer for plane 5 has not been switched. 1: Indicates that the frame buffer for plane 5 has been switched. The ADC5 bit state is held until it is cleared.
3	ADC4	0	R	Not available	Auto Rendering Display Change Flag 4 0: Indicates that the frame buffer for plane 4 has not been switched. 1: Indicates that the frame buffer for plane 4 has been switched. The ADC4 bit state is held until it is cleared.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
2	ADC3	0	R	Not available	Auto Rendering Display Change Flag 3 0: Indicates that the frame buffer for plane 3 has not been switched. 1: Indicates that the frame buffer for plane 3 has been switched. The ADC3 bit state is held until it is cleared.
1	ADC2	0	R	Not available	Auto Rendering Display Change Flag 2 0: Indicates that the frame buffer for plane 2 has not been switched. 1: Indicates that the frame buffer for plane 2 has been switched. The ADC2 bit state is held until it is cleared.
0	ADC1	0	R	Not available	Auto Rendering Display Change Flag 1 0: Indicates that the frame buffer for plane 1 has not been switched. 1: Indicates that the frame buffer for plane 1 has been switched. The ADC1 bit state is held until it is cleared.

20.3.1.11 Display Unit Domain 1 Status Register 1 (DD1SSR1)

Address: DU1: H'FEB2 8008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TVR1	FRM1	—	—	VBK1	—	RINT1	HBK1	—	—	—	—	—	—	—	—
Initial value:	0	0	—	—	0	—	0	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	TVR1	0	R	Not available	TV Synchronization Error Flag 1 0: Indicates that, after the TVR1 bit is cleared with the DRES bit of the display unit system control register 0 (DSYSR0) or the TVCL1 bit of the display unit domain 1 status register clear register 1 (DD1SRCR1), the EXVSYNC rising edge is detected every time within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1). 1: Indicates that, in TV synchronized mode, the EXVSYNC rising edge was not detected within the vertical cycle determined with the setting of the vertical cycle register 1 (VCR1). The TVR1 bit retains its status until it is cleared with the DRES or TVCL1 bit.
14	FRM1	0	R	Not available	Frame Flag 1 0: Indicates the period from the time when the FRM1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the FRCL1 bit of the display unit domain 1 status register clear register 1 (DD1SRCR1) to the time when display of the next field is completed in the non-interlaced mode, or when display of the next even field is completed in interlace sync mode or interlace sync & video mode. 1: Indicates the period (in units of frames) from the start of the vertical blanking period of the first even field after the FRM1 bit is cleared by the DRES or FRCL1 bit, to the time when the FRM1 bit is cleared again.
13, 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	VBK1	0	R	Not available	Vertical Blanking Flag 1 0: Indicates the period from the time when the VBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the VBCL1 bit of the display unit domain 1 status register clear register 1 (DD1SRCR1) to the time when display of the next field is completed. 1: Indicates the period (in units of fields) from the start of the first vertical blanking period after the VBK1 bit is cleared by the DRES or VBCL1 bit, to the time when the VBK1 bit is cleared again.
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9	RINT1	0	R	Not available	Raster Interrupt Flag 1 0: Indicates the period from the time when the RINT1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the RICL1 bit of the display unit domain 1 status register clear register 1 (DD1SRCR1) to the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFSR1) has elapsed after the beginning of the next field display. 1: Indicates the period from the time when the period of the rasters set in the raster interrupt offset register 1 (RINTOFS1) has elapsed after the beginning of the next field display after the RINT1 bit is cleared by the DRES or RICL1 bit, to the time when the RINT1 bit is cleared again.
8	HBK1	0	R	Not available	Horizontal Blanking Flag 1 0: Indicates the period from the time when the HBK1 bit is cleared by the DRES bit of the display unit system control register 0 (DSYSR0) or by the HBCL1 bit of the display unit domain 1 status register clear register 1 (DD1SRCR1) to the time of the next HSYNC assertion. 1: Indicates the period from the start of the first horizontal blanking period after the HBK1 bit is cleared by the DRES or HBCL1 bit, to the time when the HBK1 bit is cleared again.
7 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.12 Display Unit Domain 1 Status Register Clear Register 0 (DD1SRCR0)

Address: DU0: H'FEB2 000C

The specifications shown in section 20.3.1.7, Display Unit Status Register Clear Register 0 (DSRCR0), are also applied to this register.

20.3.1.13 Display Unit Domain 1 Status Register Clear Register 1 (DD1SRCR1)

Address: DU1: H'FEB2 800C

The specifications shown in section 20.3.1.8, Display Unit Status Register Clear Register 1 (DSRCR1), are also applied to this register.

20.3.1.14 Display Unit Domain 1 Interrupt Enable Register 0 (DD1IER0)

Address: DU0: H'FEB2 0010

The specifications shown in section 20.3.1.10, Display Unit Interrupt Enable Register 0 (DIER0), are also applied to this register.

20.3.1.15 Display Unit Domain 1 Interrupt Enable Register 1 (DD1IER1)

Address: DU1: H'FEB2 8010

The specifications shown in section 20.3.1.11, Display Unit Interrupt Enable Register 1 (DIER1), are also applied to this register.

20.3.1.16 Color Palette Control Register (CPCR)

Address: DU0: H'FEB0 0014

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	CP4CE	CP3CE	CP2CE	CP1CE
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 20	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
19	CP4CE	0	R/W	Available	Color Palette 4 Change Enable 0: The color palette 4 is not switched. 1: The color palette 4 is switched. Switching occurs when the DRES bit of the display unit system control register 0 (DSYSR0) is set to 0 from 1 or when internal updating is performed. This bit is valid only when it is set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 4 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.
18	CP3CE	0	R/W	Available	Color Palette 3 Change Enable 0: The color palette 3 is not switched. 1: The color palette 3 is switched. Switching occurs when the DRES bit of the display unit system control register 0 (DSYSR0) is set to 0 from 1 or when internal updating is performed. This bit is valid only when it is set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 3 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.
17	CP2CE	0	R/W	Available	Color Palette 2 Change Enable 0: The color palette 2 is not switched. 1: The color palette 2 is switched. Switching occurs when the DRES bit of the display unit system control register 0 (DSYSR0) is set to 0 from 1 or when internal updating is performed. This bit is valid only when it is set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 2 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
16	CP1CE	0	R/W	Available	Color Palette 1 Change Enable 0: The color palette 1 is not switched. 1: The color palette 1 is switched. Switching occurs when the DRES bit of the display unit system control register 0 (DSYSR0) is set to 0 from 1 or when internal updating is performed. This bit is valid only when set to 1. Setting this bit to 0 is invalid. This bit is cleared to 0 after the color palette 1 is switched. If setting of 1 and clearing to 0 occur at the same time, clearing to 0 is given priority.
15 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.17 Display Plane Priority Register (DPPR)

Address: DU0: H'FEB0 0018

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPE8	DPS8			DPE7	DPS7			DPE6	DPS6			DPE5	DPS5		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPE4	DPS4			DPE3	DPS3			DPE2	DPS2			DPE1	DPS1		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Defines the order of planes in image composition and turns the display of planes on or off
- When the DPRS bit in the display unit output route control register (DORCR) is 0, the display of planes from among planes 1 to 8 for which display is enabled is switched on.
- This register can only be used to set the priority order for superposition processor m. To use superposition processor 1, set the DPRS bit in the display unit output route control register (DORCR) to 1 and make other settings as required in the display superimpose 1 priority register.
- After setting a desired value in a register listed in section 20.3.4, Display Plane Registers (Alpha-ratio Plane Registers), set the corresponding bit in the DPPR (bit 31, 27, 23, 19, 15, 11, 7, or 3) to 1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31	DPE8	0	R/W	Available	Display Plane Priority 8 Enable
30 to 28	DPS8	111	R/W	Available	Display Plane Priority 8 Select 1000: Assigns priority 8 to plane 1 and displays plane 1. 1001: Assigns priority 8 to plane 2 and displays plane 2. 1010: Assigns priority 8 to plane 3 and displays plane 3. 1011: Assigns priority 8 to plane 4 and displays plane 4. 1100: Assigns priority 8 to plane 5 and displays plane 5. 1101: Assigns priority 8 to plane 6 and displays plane 6. 1110: Assigns priority 8 to plane 7 and displays plane 7. 1111: Assigns priority 8 to plane 8 and displays plane 8. 0---: Priority 8 is not displayed.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
27	DPE7	0	R/W	Available	Display Plane Priority 7 Enable
26 to 24	DPS7	110	R/W	Available	Display Plane Priority 7 Select 1000: Assigns priority 7 to plane 1 and displays plane 1. 1001: Assigns priority 7 to plane 2 and displays plane 2. 1010: Assigns priority 7 to plane 3 and displays plane 3. 1011: Assigns priority 7 to plane 4 and displays plane 4. 1100: Assigns priority 7 to plane 5 and displays plane 5. 1101: Assigns priority 7 to plane 6 and displays plane 6. 1110: Assigns priority 7 to plane 7 and displays plane 7. 1111: Assigns priority 7 to plane 8 and displays plane 8. 0---: Priority 7 is not displayed.
23	DPE6	0	R/W	Available	Display Plane Priority 6 Enable
22 to 20	DPS6	101	R/W	Available	Display Plane Priority 6 Select 1000: Assigns priority 6 to plane 1 and displays plane 1. 1001: Assigns priority 6 to plane 2 and displays plane 2. 1010: Assigns priority 6 to plane 3 and displays plane 3. 1011: Assigns priority 6 to plane 4 and displays plane 4. 1100: Assigns priority 6 to plane 5 and displays plane 5. 1101: Assigns priority 6 to plane 6 and displays plane 6. 1110: Assigns priority 6 to plane 7 and displays plane 7. 1111: Assigns priority 6 to plane 8 and displays plane 8. 0---: Priority 6 is not displayed.
19	DPE5	0	R/W	Available	Display Plane Priority 5 Enable
18 to 16	DPS5	100	R/W	Available	Display Plane Priority 5 Select 1000: Assigns priority 5 to plane 1 and displays plane 1. 1001: Assigns priority 5 to plane 2 and displays plane 2. 1010: Assigns priority 5 to plane 3 and displays plane 3. 1011: Assigns priority 5 to plane 4 and displays plane 4. 1100: Assigns priority 5 to plane 5 and displays plane 5. 1101: Assigns priority 5 to plane 6 and displays plane 6. 1110: Assigns priority 5 to plane 7 and displays plane 7. 1111: Assigns priority 5 to plane 8 and displays plane 8. 0---: Priority 5 is not displayed.
15	DPE4	0	R/W	Available	Display Plane Priority 4 Enable
14 to 12	DPS4	011	R/W	Available	Display Plane Priority 4 Select 1000: Assigns priority 4 to plane 1 and displays plane 1. 1001: Assigns priority 4 to plane 2 and displays plane 2. 1010: Assigns priority 4 to plane 3 and displays plane 3. 1011: Assigns priority 4 to plane 4 and displays plane 4. 1100: Assigns priority 4 to plane 5 and displays plane 5. 1101: Assigns priority 4 to plane 6 and displays plane 6. 1110: Assigns priority 4 to plane 7 and displays plane 7. 1111: Assigns priority 4 to plane 8 and displays plane 8. 0---: Priority 4 is not displayed.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	DPE3	0	R/W	Available	Display Plane Priority 3 Enable
10 to 8	DPS3	010	R/W	Available	Display Plane Priority 3 Select 1000: Assigns priority 3 to plane 1 and displays plane 1. 1001: Assigns priority 3 to plane 2 and displays plane 2. 1010: Assigns priority 3 to plane 3 and displays plane 3. 1011: Assigns priority 3 to plane 4 and displays plane 4. 1100: Assigns priority 3 to plane 5 and displays plane 5. 1101: Assigns priority 3 to plane 6 and displays plane 6. 1110: Assigns priority 3 to plane 7 and displays plane 7. 1111: Assigns priority 3 to plane 8 and displays plane 8. 0---: Priority 3 is not displayed.
7	DPE2	0	R/W	Available	Display Plane Priority 2 Enable
6 to 4	DPS2	001	R/W	Available	Display Plane Priority 2 Select 1000: Assigns priority 2 to plane 1 and displays plane 1. 1001: Assigns priority 2 to plane 2 and displays plane 2. 1010: Assigns priority 2 to plane 3 and displays plane 3. 1011: Assigns priority 2 to plane 4 and displays plane 4. 1100: Assigns priority 2 to plane 5 and displays plane 5. 1101: Assigns priority 2 to plane 6 and displays plane 6. 1110: Assigns priority 2 to plane 7 and displays plane 7. 1111: Assigns priority 2 to plane 8 and displays plane 8. 0---: Priority 2 is not displayed.
3	DPE1	0	R/W	Available	Display Plane Priority 1 Enable
2 to 0	DPS1	000	R/W	Available	Display Plane Priority 1 Select 1000: Assigns priority 1 to plane 1 and displays plane 1. 1001: Assigns priority 1 to plane 2 and displays plane 2. 1010: Assigns priority 1 to plane 3 and displays plane 3. 1011: Assigns priority 1 to plane 4 and displays plane 4. 1100: Assigns priority 1 to plane 5 and displays plane 5. 1101: Assigns priority 1 to plane 6 and displays plane 6. 1110: Assigns priority 1 to plane 7 and displays plane 7. 1111: Assigns priority 1 to plane 8 and displays plane 8. 0---: Priority 1 is not displayed.

20.3.1.18 Display Unit Extensional Function Control Register 0 (DEFR0)

Address: DU0: H'FEB0 0020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EXSL	EXVL	—	—	—	—	—	EXUP	VCUP	—	—	—	DEFE
Initial value:	—	—	—	0	0	—	—	—	—	—	0	0	—	—	—	0
R/W:	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEFR0 Enabling Code (register available code) For a value written to DEFR0 to be effective, the value must include H'7773 in these bits.
15 to 13	—	—	R	—	Reserved. The read value is undefined. The write value should always be 0.
12	EXSL	0	R/W	DRES	External Sync Signal Select 0: External SYNC signals (EXVSYNC, EXHSYNC) allow signals from the pins to be directly read in terms of post-division clocks. 1: External SYNC signals (EXVSYNC, EXHSYNC) allow the signals that were read in terms of pre-division clock to be read again as post-division clocks.
11	EXVL	0	R/W	Not available	External Vsync Latch Select 0: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched every clock cycle. 1: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched at the rising edge of the external HSYNC signal.
10 to 6	—	—	R	—	Reserved. The read value is undefined. The write value should always be 0.
5	EXUP	0	R/W	DRES	External Updating Mode 0: Internally updates the internal update function bit. 1: Externally updates the internal update function bit without updating it internally. This bit takes precedence over the display unit system control register 0 (DSYSR0)/IUPD.
4	VCUP	0	R/W	DRES	Vertical Cycle Register Update Timing Select 0: The internal updating is based on the falling VSYNC. 1: The internal updating is based on the rising VSYNC. By setting the internal updating of the vertical scanning cycle register as a VSYNC rise, any disturbance of VSYNC signals during vertical scanning cycle register switching can be prevented.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
0	DEFE	0	R/W	DRES	Display Unit Extensional Function Enable 0: Disables the extensional functions 1: Enables the following extensional functions: Enables bits 27 and 26 in the plane n mode register (PnMR*1). Enables bits 31 to 29 of plane n display area start address 0 to 2 registers (P2DSA0R to P2DSA2R*1) and display capture n area start address register (DCnSAR*2). Enables bits 25 and 5 in the external synchronization control register m (ESCRm*3). Enables bit 10 in the plane n blending ratio register (PnALPHAR*1). Enables bit 29 in the display unit system control register m (DSYSRm*3).

Notes: 1. n = 1 to 8
2. n = no number or 2
3. m = 0 and 1

20.3.1.19 Display Unit Extensional Function Control Register 1 (DEFR1)

Address: DU1: H'FEB3 0020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EXSL1	EXV1L	—	DODF1		—	—	—	VCUP1	—	—	—	—
Initial value:	—	—	—	0	0	—	0	0	—	—	—	0	—	—	—	—
R/W:	R	R	R	R/W	R/W	R	R/W	R/W	R	R	R	R/W	R	R	R	R

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

- Since the bits 5 and 0 of the display expanded-function control register 0 (DEFR0) are made to serve a double purpose by DU0 and DU1, this register does not have a function.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEFR1 Enabling Code (register available code) For a value written to DEFR1 to be effective, the value must include H'7773 in these bits.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12	EXSL1	0	R/W	DRES	External Sync Signal Select 1 0: External SYNC signals (EXVSYNC, EXHSYNC) allow signals from the pins to be directly read in terms of post-division clocks. 1: External SYNC signals (EXVSYNC, EXHSYNC) allow the signals that were read in terms of pre-division clock to be read again as post-division clocks.
11	EXV1L	0	R/W	Not available	External Vsync Latch Select 1 0: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched every clock cycle. 1: External VSYNC signal (EXVSYNC) allows the signal from the pin to be latched at the rising edge of the external HSYNC signal.
10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
9, 8	DODF1	00	R/W	DRES	Display Output Data Format. 00: Sets the DU1 display output to RGB data format. 01: Setting prohibited 10: Sets the DU1 display output to non-multiplexed YC data format. Y (luminance) and C (chrominance) are output in parallel. 11: Sets the DU1 display output to multiplexed YC data format. Y (luminance) and C (chrominance) are output in multiplexed format. When YC format is displayed by the timing as shown in Figure 20.22 and Figure 20.23, set 1 bits to DCKOSEL and FRQSEL (division by 2) in the external synchronization control register 1 (ESCR1). Non-multiplexed YC format can be displayed in Figure 20.22a and Figure 20.22b, this setting is not required.
7 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	VCUP1	0	R/W	DRES	Vertical cycle register update timing select 0: The internal updating is based on the falling VSYNC. 1: The internal updating is based on the rising VSYNC. By setting the internal updating of the vertical scanning cycle register as a VSYNC rise, any disturbance of VSYNC signals during vertical scanning cycle register switching can be prevented.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.20 Display Alpha Ratio Plane Control Register (DAPCR)

Address: DU0: H'FEB0 0024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	AP2E	—	—	—	AP1E
Initial value:	—	—	—	—	—	—	—	—	—	—	—	0	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

After setting a desired value in a register listed in section 20.3.4, Display Plane Registers (Alpha-ratio Plane Registers), set the corresponding bit in the DAPCR to 1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DAPCR Enabling Code (register available code) For a value written to DAPCR to be effective, the value must include H'7773 in these bits.
15 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	AP2E	0	R/W	Available	Alpha Ratio Plane 2 Enable 0: α plane 2 cannot be used. 1: α plane 2 can be used.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	AP1E	0	R/W	Available	Alpha Ratio Plane 1 Enable 0: α plane 1 cannot be used. 1: α plane 1 can be used.

20.3.1.21 Display Capture Control Register (DCPCR)

Address: DU0: H'FEB0 0028

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—		CA2B	CD2F	—	—	—	DC2E	—		CAB	CDF	—	—	—	DCE
Initial value:	0	0	0	0	—	—	—	0	—	—	0	0	—	—	—	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R	R	R	R/W

After setting a desired value in a register listed in section 20.3.5, Display Capture Registers, set the corresponding bit in the DCPCR (bit 8 or 0) to 1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DCPCR Enabling Code (register available code) For a value written to DCPCR to be effective, the value must include H'7773 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13	CA2B	0	R/W	Available	Display Capture A Bit 2 Function Select To enable this bit, DEFE3 bit in the display unit extensional function control 3 register (DEF3R) should be set to 1. In the initial state, this bit is fixed to 0. 0: When the display capture data 2 format is ARGB1555, the A value is 0. 1: When the display capture data 2 format is ARGB1555, the A value is 1.
12	CD2F	0	R/W	Available	Display Capture Data 2 Format To enable this bit, the DEFE3 bit in the display unit extensional function control 3 register (DEF3R) should be set to 1. In the initial state, this bit is fixed to 0. 0: Display capture data format in the superposition processor 1 is RGB565. 1: Display capture data format in the superposition processor 1 is ARGB1555. The A value is determined by bit 13 in this register.
11 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
8	DC2E	0	R/W	Available	Display Capture 2 Enable To enable this bit, DEFE3 bit in the display unit extensional function control 3 register (DEF3R) should be set to 1. In the initial state, this bit is fixed to 0. 0: Display data in the superposition processor 1 is not captured. 1: Display data in the superposition processor 1 is captured when the DRES and DEN bits in the display unit system control register 0 (DSYSR0) are B'01. After this bit is set to 1, data capture is started in the subsequent frame.
7, 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	CAB	0	R/W	Available	Display Capture A Bit Function Select To enable this bit, the DEFE2G bit in the display unit extensional function control 2 register (DEF2R) should be set to 1. In the initial state, this bit is fixed to 0. 0: When the display capture data format is ARGB1555, the A value is 0. 1: When the display capture data format is ARGB1555, the A value is 1.
4	CDF	0	R/W	Available	Display Capture Data Format To enable this bit, the DEFE2G bit in the display unit extensional function control 2 register (DEF2R) should be set to 1. In the initial state, this bit is fixed to 0. 0: Display capture data format in the superposition processor m is RGB565. 1: Display capture data format in the superposition processor m is ARGB1555. The A value is determined by bit 5 in this register.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DCE	0	R/W	Available	Display Capture Enable 0: Display data in the superposition processor 0 is not captured. 1: Display data in the superposition processor 0 is captured when the DRES and DEN bits in the display unit system control register 0 (DSYSR0) are B'01. After this bit is set to 1, data capture is started in the subsequent frame.

20.3.1.22 Display Unit Extensional Function Control 2 Register (DEF2R)

Address: DU0: H'FEB0 0034

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DEFE2G
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF2R Enabling Code (register available code) For a value written to DEF2R to be effective, the value must include H'7775 in these bits.
15 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE2G	0	R/W	DRES	Display Unit Extensional Function Enable 2G 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional functions are enabled. Bits 13 and 12 in the plane n blending ratio register (PnALPHAR*) Bits 5 and 4 in the display capture control register (DCPCR)

Note: * n = 1 to 8

20.3.1.23 Display Unit Extensional Function Control 3 Register (DEF3R)

Address: DU0: H'FEB0 0038

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DEFE3
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF3R Enabling Code (register available code) For a value written to DEF3R to be effective, the value must include H'7776 in these bits.
15 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE3	0	R/W	DRES	Display Unit Extensional Function Enable 3 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional functions are enabled. Bits 13, 12 and 8 in the display capture control register (DCPCR) Display video capture status register (DVCSR)

20.3.1.24 Display Unit Extensional Function Control 4 Register (DEF4R)

Address: DU0: H'FEB0 003C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	LRUO	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	0	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF4R Enabling Code (register available code) For a value written to DEF4R to be effective, the value must include H'7777 in these bits.
15 to 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	LRUO	0	R/W	DRES	LRU Function Off 0: Requests for the AXI from the individual planes are arbitrated by the LRU system. 1: Requests for the AXI from the individual planes are arbitrated according to the following decreasing order of priority: plane 1, plane 2, plane 3, plane 4, plane 5, plane 6, plane 7, plane 8, α plane 1, α plane 2, display capture1, and display capture 2. When the display is 32-bit/pixel, set this bit to 1.
4 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.25 Display Unit Video Capture Status Register (DVCSR)

Address: DU0: H'FEB0 00D0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	VC1FB1		VC0FB1	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	VC1FB		VC0FB	
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * For reserved bit (bit name: —), initial value is undefined. For details, refer to following table.

- To enable this register, set the DEFE3 bit in the display unit extensional function control 3 register (DEF3R) to 1. The value read from this register in its initial state is fixed to 0. Video Capture is the same as VideoInput.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 20	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
19, 18	VC1FB1	00	R	Not available	Video Capture 1 Frame Buffer Flag 1 These bits are updated with the same timing as internal updating of timing generator 1. 00: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA0R. 01: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA1R. 10: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA2R. 11: The video capture 1 module is in its initial state.
17, 16	VC0FB1	00	R	Not available	Video Capture 0 Frame Buffer Flag 1 These bits are updated with the same timing as internal updating of timing generator 1. 00: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA0R. 01: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA1R. 10: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA2R. 11: The video capture 0 module is in its initial state.
15 to 4	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
3, 2	VC1FB	00	R	Not available	Video Capture 1 Frame Buffer Flag These bits are updated with the same timing as internal updating of timing generator 0. 00: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA0R. 01: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA1R. 10: In the plane set for video capture 1, the display area starts at the address indicated by PnDSA2R. 11: The video capture 1 module is in its initial state.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
1, 0	VC0FB	00	R	Not available	Video Capture 0 Frame Buffer Flag These bits are updated with the same timing as internal updating of timing generator 0. 00: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA0R. 01: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA1R. 10: In the plane set for video capture 0, the display area starts at the address indicated by PnDSA2R. 11: The video capture 0 module is in its initial state.

20.3.1.26 Display Unit Extensional Function Control 5 Register (DEF5R)

Address: DU0: H'FEB0 00E0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE								—	—	—	—	—	NTEE	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	0	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	R	R	R	R	R	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RGBYC1		RGBYC0		—	—	—	DEFE5
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CODE	—	—/W	Not available	DEF5R Enabling Code (register available code) For a value written to DEF5R to be effective, the value must include H'66 in these bits.
23 to 19	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
18	NTEE	0	R/W	DRES	DVENC Enable 0: DVENC (Digital video encoder) is disabled. 1: DVENC (Digital video encoder) is enabled.
17 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7, 6	RGBYC1	00	R/W	DRES	RGB-YC Converted Output 1 00: DU1 display output is RGB data format. 01: DU1 display output is RGB-YC converted multiplexed YC data format. 10: DU1 display output is RGB-YC converted non-multiplexed YC data format. 11: Setting prohibited For YC data format, set to 1 bits DCKOSEL and FRQSEL (division by 2) in the External Synchronization Control Register 0 (ESCR1). For performing RGB-YC conversion, the display capture function (section 20.4.18) or the color detection function (section 20.5.4) cannot be used.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5, 4	RGBYC0	00	R/W	DRES	RGB-YC Converted Output 0 00: DU0 display output is RGB data format. 01: DU0 display output is RGB-YC converted multiplexed YC data format. 10: DU0 display output is RGB-YC converted non-multiplexed YC data format. 11: Setting prohibited For YC data format, set to 1 bits DCKOSEL and FRQSEL (division by 2) in the External Synchronization Control Register 0 (ESCR0). For performing RGB-YC conversion, the display capture function (section 20.4.18) or the color detection function (section 20.5.4) cannot be used.
3 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DEFE5	0	R/W	DRES	Display Unit Extensional Function Enable 5 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional function is enabled. The number of bits is increased by one for the following registers: Display timing generation registers HDSRn*1, HDERn*1, VDERn*1, HCRn*1, VCRn*1, VSPRn*1, CLAMPSRn*1, CLAMPWRn*1, DESRn*1, and DEWRn*1 Display attribute registers RINTOFSRn*1 Display plane registers (alpha-ratio plane registers) PnDSXR*2, PnDSYR*2, PnDPXR*2, and PnDPYR*2

Notes: 1. n = 0 and 1.
2. n = 1 to 8

20.3.1.27 Display Unit Data Latency Adjustment Register (DDLTR)

Address: DU0: H'FEB0 00E4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DLAR1	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	0	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

This register is used to adjust the latency of two display data items output from the DU0 and DU1 when two image data items are output from the DU pins on both edges (rising and falling edges) of the output dot clock. This register should not be changed from its initial value when the DR0D bit in the display unit output route control register (DORCR) is 0. When the DR0D bit is set to 1 (when two image data items are output from the DU pins on both edges of the output dot clock), set the necessary bits in this register to 1.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DDLTR Enabling Code (register available code) For a value written to DDLTR to be effective, the value must include H'7766 in these bits.
15 to 7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
6	DLAR1	0	R/W	DRES	Display Data Latency Adjustment RGBYC1 Set this bit to 1 in order to adjust the latency on the DU1 side when the RGBYC0 bit in the display unit extensional function control 5 register (DEF5R) is set to B'10 (RGB-YC conversion is performed). 0: DU1 display data is output without delay. 1: DU1 display data is output with a delay corresponding to the latency of RGB-YC conversion on the DU0 side.
5 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.28 Display Unit Extensional Function Control 6 Register (DEF6R)

Address: DU0: H'FEB0 00E8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	ODPM12		ODPM02		—	—	—	—	MLOS1	MLOS0	—	—
Initial value:	—	—	—	—	0	0	0	0	—	—	—	—	0	0	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R	R

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF6R Enabling Code (register available code) For a value written to DEF6R to be effective, the value must include H'7778 in these bits.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11, 10	ODPM12	00	R/W	DRES	ODDF Pin Mode 12 00: The ODDF pin function is determined by the ODPM bit in the display unit mode register 1 (DSMR1). 01: Setting prohibited. 10: The DISP signal is output to the ODDF pin, which is a DU1 pin. Even if the TVM1 bits in the display unit system control register 1 (DSYSR1) indicate TV synchronized mode, the ODDF pin becomes an output. 11: The CDE signal is output to the ODDF pin, which is a DU1 pin. Even if the TVM1 bits in the display unit system control register 1 (DSYSR1) indicate TV synchronized mode, the ODDF pin becomes an output. "ODDF pin" refers to the DU1_ODDF/DU1_EXODDF pin indicated in Table 20.1b.
9, 8	ODPM02	00	R/W	DRES	ODDF Pin Mode 02 00: The ODDF pin function is determined by the ODPM bit in the display unit mode register 0 (DSMR0). 01: Setting prohibited. 10: The DISP signal is output to the ODDF pin, which is a DU0 pins. Even if the TVM bits in display unit system control register 0 (DSYSR0) indicate TV synchronized mode, the ODDF pin becomes an output. 11: The CDE signal is output to the ODDF pin, which is a DU0 pins. Even if the TVM bits in display unit system control register 0 (DSYSR0) indicate TV synchronized mode, the ODDF pin becomes an output. "ODDF pin" refers to the DU0_ODDF/DU0_EXODDF pin indicated in Table 20.1a.
7 to 4	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
3	MLOS1	0	R/W	DRES	Multiple Output Select 1 0: DU1 pins function as a 24-bit non-multiple output. 1: DU1 pins output 12-bit data generated by multiplexing 24-bit data. When this bit is set to 1, set the DCKOINV bit in the external synchronization control register 1 (ESCR1) to 1.
2	MLOS0	0	R/W	DRES	Multiple Output Select 0 0: DU0 pins function as a 24-bit non-multiple output. 1: DU0 pins output 12-bit data generated by multiplexing 24-bit data. When this bit is set to 1, set the DCKOINV bit in the external synchronization control register 0 (ESCR0) to 1.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.1.29 Display Unit Extensional Function Control 8 Register (DEF8R)

Address: DU0: H'FEB2 0020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	YCOD	DEFE8
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DEF8R Enabling Code (register available code) For a value written to DEF8R to be effective, the value must include H'7790 in these bits.
15 to 2	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
1	YCOD	0	R/W	DRES	YC Off mode Output Data 0: When data is displayed in YC format, UV data in YC off mode is H'00. 1: When data is displayed in YC format, UV data in YC off mode is H'80.
0	DEFE8	0	R/W	DRES	Display Unit Extensional Function Enable 8 0: Extensional functions are disabled. 1: Extensional functions are enabled. The following extensional functions are enabled. Bit 12 in the display unit status register 0 (DSSR0) Bit 13 in the plane n display data control 4 register (PnDDC4R*)

Note: * n = 1 to 8

20.3.1.30 Display Unit Output Signal Fixed Level Register (DOFLR)

Address: DU0: H'FEB2 0024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	HSYCFL1	VSYCFL1	ODDFL1	DISPFL1	CDEFL1	RGBFL1	—	—	HSYCFL0	VSYCFL0	ODDFL0	DISPFL0	CDEFL0	RGBFL0
Initial value:	—	—	0	0	0	0	0	0	—	—	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DOFLR Enabling Code (register available code) For a value written to DOFLR to be effective, the value must include H'7790 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13	HSYCFL1	0	R/W	Not available	HSYNC (DU1) Signal Fixed Low Level 0: HSYNC (DU1) output is normal. 1: HSYNC (DU1) output is fixed low. This bit setting is effective only in master mode.
12	VSYCFL1	0	R/W	Not available	VSYNC (DU1) Signal Fixed Low Level 0: VSYNC (DU1) output is normal. 1: VSYNC (DU1) output is fixed low. This bit setting is effective only in master mode.
11	ODDFL1	0	R/W	Not available	ODDF (DU1) Signal Fixed Low Level 0: ODDF (DU1) output is normal. 1: ODDF (DU1) output is fixed low. This bit setting is effective only in master mode.
10	DISPFL1	0	R/W	Not available	DISP (DU1) Signal Fixed Low Level 0: DISP (DU1) output is normal. 1: DISP (DU1) output is fixed low.
9	CDEFL1	0	R/W	Not available	CDE (DU1) Signal Fixed Low Level 0: CDE (DU1) output is normal. 1: CDE (DU1) output is fixed low.
8	RGBFL1	0	R/W	Not available	RGB (DU1) Signal Fixed Low Level 0: RGB (DU1) output is normal. 1: RGB (DU1) output is fixed low.
7, 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	HSYCFL0	0	R/W	Not available	HSYNC (DU0) Signal Fixed Low Level 0: HSYNC (DU0) output is normal. 1: HSYNC (DU0) output is fixed low. This bit setting is effective only in master mode.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
4	VSYCFL0	0	R/W	Not available	VSYNC (DU0) Signal Fixed Low Level 0: VSYNC (DU0) output is normal. 1: VSYNC (DU0) output is fixed low. This bit setting is effective only in master mode.
3	ODDFL0	0	R/W	Not available	ODDF (DU0) Signal Fixed Low Level 0: ODDF (DU0) output is normal. 1: ODDF (DU0) signal at fixed low level. This bit setting is effective only in master mode.
2	DISPFL0	0	R/W	Not available	DISP (DU0) Signal Fixed Low Level 0: DISP (DU0) output is normal. 1: DISP (DU0) output is fixed low.
1	CDEFL0	0	R/W	Not available	CDE (DU0) Signal Fixed Low Level 0: CDE (DU0) output is normal. 1: CDE (DU0) output is fixed low.
0	RGBFL0	0	R/W	Not available	RGB (DU0) Signal Fixed Low Level 0: RGB (DU0) output is normal. 1: RGB (DU0) output is fixed low.

20.3.1.31 Display Unit Input Dot Clock Select Register (DIDSR)

Address: H'FEB2 0028

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LDCS1		LDCS0		—	—	—	—	PDCS1		PDCS0	
Initial value:	—	—	—	—	0	0	0	0	—	—	—	—	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DIDSR Enabling Code (register available code) For a value written to DIDSR to be effective, the value must include H'7790 in these bits.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11, 10	LDCS1	00	R/W	DRES	DU1 LVDS Dot Clock Select 0-: The DU1 input dot clock source is the DU1_DOTCLKIN pin. 10: The DU1 input dot clock source is the LVDS pin*1. 11: The DU1 input dot clock source is the DVENC pin*2.
9, 8	LDCS0	00	R/W	DRES	DU0 LVDS Dot Clock Select 0-: The DU0 input dot clock source is the DU0_DOTCLKIN pin. 10: The DU0 input dot clock source is the LVDS pin*1. 11: The DU0 input dot clock source is the DVENC pin*2.
7 to 4	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
3, 2	PDCS1	00	R/W	DRES	DU1 Pad Dot Clock Select -0: The DU1 input dot clock source is the DU1_DOTCLKIN pin. 01: The DU1 input dot clock source is the DU0_DOTCLKIN pin. 11: Setting prohibited.
1, 0	PDCS0	00	R/W	DRES	DU0 Pad Dot Clock Select -0: The DU0 input dot clock source is the DU0_DOTCLKIN pin. 01: The DU0 input dot clock source is the DU1_DOTCLKIN pin. 11: Setting prohibited.

Notes: 1. LVDS pin means the equivalence clock of the internal clock from the LVDS PLL. When setting B'10, the LVDS must be enabled.

2. DVENC pin means the equivalence clock of the internal clock from the VIDEO_X1. When setting B'11, the DVENC must be enabled.

20.3.2 Display Timing Generation Registers

The sets of display timing generation registers are for the respective channels and have the same functions; they are described as one here.

In section 20.3.2, n = 0 and 1 for this product.

20.3.2.1 Horizontal Display Start Register n (HDSRn)

Address: DU0: H'FEB0 0040, DU1: H'FEB3 0040

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	HDS									
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9 to 0	HDS	—	R/W	Available	Horizontal Display Start To enable bit 9, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 9 cannot be written to. These bits are used to set the horizontal display start position in dot clock units. The set value is retained at a reset.

20.3.2.2 Horizontal Display End Register n (HDERn)

Address: DU0: H'FEB0 0044, DU1: H'FEB3 0044

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HDE											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	HDE	—	R/W	Available	Horizontal Display End To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the horizontal display end position in dot clock units. The set value is retained at a reset.

20.3.2.3 Vertical Display Start Register n (VDSRn)

Address: DU0: H'FEB0 0048, DU1: H'FEB3 0048

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VDS								
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8 to 0	VDS	—	R/W	Available	Vertical Display Start These bits are used to set the vertical display start position in raster line units. The set value is retained at a reset.

20.3.2.4 Vertical Display End Register n (VDERn)

Address: DU0: H'FEB0 004C, DU1: H'FEB3 004C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VDE										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	VDE	—	R/W	Available	Vertical Display End To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the vertical display end position in raster line units. The set value is retained at a reset.

20.3.2.5 Horizontal Cycle Register n (HCRn)

Address: DU0: H'FEB0 0050, DU1: H'FEB3 0050

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HC											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	HC	—	R/W	Available	Horizontal Cycle To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set one horizontal scan cycle including the horizontal blanking period in dot clock units. In TV synchronized mode, set this register so that the HSYNC cycle set with this register is equal to or greater than the EXHSYNC cycle. The set value is retained at a reset.

20.3.2.6 Horizontal Sync Width Register n (HSWRn)

Address: DU0: H'FEB0 0054, DU1: H'FEB3 0054

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	HSW								
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 9	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
8 to 0	HSW	—	R/W	Available	Horizontal Sync Width These bits are used to set the low-level pulse width of the horizontal synchronous signal in dot clock units. The set value is retained at a reset.

20.3.2.7 Vertical Cycle Register n (VCRn)

Address: DU0: H'FEB0 0058, DU1: H'FEB3 0058

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VC										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	VC	—	R/W	Available	Vertical Cycle To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the vertical scan cycle including the vertical blanking period in raster line units. In TV synchronized mode, set the time limit of the EXVSYNC rising edge detection. If the EXVSYNC rising edge is not detected within the time limit, the result is reflected in bit 15 of the display unit status register n (DSSRn). The set value is retained at a reset.

20.3.2.8 Vertical Sync Point Register n (VSPRn)

Address: DU0: H'FEB0 005C, DU1: H'FEB3 005C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VSP										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	VSP	—	R/W	Available	Vertical Sync Point To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the vertical synchronous signal start position in raster line units. In TV synchronized mode, set this register so that the VSYNC falling edge setting position set with this register is the same as or comes after that of the EXVSYNC falling edge. The set value is retained at a reset.

20.3.2.9 Equal Pulse Width Register n (EQWRn)

Address: DU0: H'FEB0 0060, DU1: H'FEB3 0060

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	EQW						
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
6 to 0	EQW	—	R/W	Available	Equal Pulse Width These bits are used to set the low-level equalizing pulse width of the CSYNC signal in dot clock units. To validate this setting, set bit 7 in the display unit mode register n (DSMRn)/CSYNC mode (CSY) to 1. The set value is retained at a reset.

20.3.2.10 Serration Width Register n (SPWRn)

Address: DU0: H'FEB0 0064, DU1: H'FEB3 0064

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SPW									
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9 to 0	SPW	—	R/W	Available	Serration Width These bits are used to set the low-level serration pulse width of the CSYNC signal in dot clock units. Set a value smaller than 1/2 of HC. To validate this setting, set bit 7 in the display unit mode register n (DSMRn)/CSYNC mode (CSY) to 1. The set value is retained at a reset.

20.3.2.11 CLAMP Signal Start Register n (CLAMPSRn)

Address: DU0: H'FEB0 0070, DU1: H'FEB3 0070

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLAMPS											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	CLAMPS	—	R/W	Available	CLAMP Signal Start To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the CLAMP signal rising edge position in dot clock units, using as the reference the HSYNC signal falling edge. The CLAMP signal rises (setting value + 1) cycle after the HSYNC signal falls. Therefore, the CLAMP signal cannot rise in the same cycle as the HSYNC signal falling edge. The set value is retained at a reset.

20.3.2.12 CLAMP Signal Width Register n (CLAMPWRn)

Address: DU0: H'FEB0 0074, DU1: H'FEB3 0074

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CLAMPW											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	CLAMPW	—	R/W	Available	CLAMP Signal Width To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the high-level width of the CLAMP signal in dot clock units. When the CLAMP signal is high, if the HSYNC signal falls, the CLAMP signal falls. The set value is retained at a reset.

20.3.2.13 DE Signal Start Register n (DESRn)

Address: DU0: H'FEB0 0078, DU1: H'FEB3 0078

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DES											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	DES	—	R/W	Available	DE Signal Start To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the DE signal rising edge position in dot clock units, using as the reference the HSYNC signal falling edge. The DE signal rises (setting value + 1) cycle after the HSYNC signal falls. Therefore, the DE signal cannot rise in the same cycle as the HSYNC signal falling edge. During a vertical blanking period, the DE signal is fixed to the low level. The set value is retained at a reset.

20.3.2.14 DE Signal Width Register n (DEWRn)

Address: DU0: H'FEB0 007C, DU1: H'FEB3 007C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	DEW											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	DEW	—	R/W	Available	DE Signal Width To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. These bits are used to set the high-level width of the DE signal in dot clock units. When the DE signal is high, if the HSYNC signal falls, the DE signal falls. The set value is retained at a reset.

20.3.3 Display Attribute Registers

In section 20.3.3, n = 0 and 1 for this product.

20.3.3.1 Color Palette 1 Transparent Color Register (CP1TR)

Address: DU0: H'FEB0 0080

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP1IF	CP1IE	CP1ID	CP1IC	CP1IB	CP1IA	CP1I9	CP1I8	CP1I7	CP1I6	CP1I5	CP1I4	CP1I3	CP1I2	CP1I1	CP1I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP1IF	0	R/W	Available	Color Palette 1 Index F This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index F to the transparent color. 1: Sets the color of the color palette 1 index F to the transparent color.
14	CP1IE	0	R/W	Available	Color Palette 1 Index E This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index E to the transparent color. 1: Sets the color of the color palette 1 index E to the transparent color.
13	CP1ID	0	R/W	Available	Color Palette 1 Index D This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index D to the transparent color. 1: Sets the color of the color palette 1 index D to the transparent color.
12	CP1IC	0	R/W	Available	Color Palette 1 Index C This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index C to the transparent color. 1: Sets the color of the color palette 1 index C to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	CP1IB	0	R/W	Available	Color Palette 1 Index B This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index B to the transparent color. 1: Sets the color of the color palette 1 index B to the transparent color.
10	CP1IA	0	R/W	Available	Color Palette 1 Index A This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index A to the transparent color. 1: Sets the color of the color palette 1 index A to the transparent color.
9	CP1I9	0	R/W	Available	Color Palette 1 Index 9 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 9 to the transparent color. 1: Sets the color of the color palette 1 index 9 to the transparent color.
8	CP1I8	0	R/W	Available	Color Palette 1 Index 8 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 8 to the transparent color. 1: Sets the color of the color palette 1 index 8 to the transparent color.
7	CP1I7	0	R/W	Available	Color Palette 1 Index 7 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 7 to the transparent color. 1: Sets the color of the color palette 1 index 7 to the transparent color.
6	CP1I6	0	R/W	Available	Color Palette 1 Index 6 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 6 to the transparent color. 1: Sets the color of the color palette 1 index 6 to the transparent color.
5	CP1I5	0	R/W	Available	Color Palette 1 Index 5 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 5 to the transparent color. 1: Sets the color of the color palette 1 index 5 to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
4	CP1I4	0	R/W	Available	Color Palette 1 Index 4 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 4 to the transparent color. 1: Sets the color of the color palette 1 index 4 to the transparent color.
3	CP1I3	0	R/W	Available	Color Palette 1 Index 3 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 3 to the transparent color. 1: Sets the color of the color palette 1 index 3 to the transparent color.
2	CP1I2	0	R/W	Available	Color Palette 1 Index 2 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 2 to the transparent color. 1: Sets the color of the color palette 1 index 2 to the transparent color.
1	CP1I1	0	R/W	Available	Color Palette 1 Index 1 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 1 to the transparent color. 1: Sets the color of the color palette 1 index 1 to the transparent color.
0	CP1I0	0	R/W	Available	Color Palette 1 Index 0 This bit is used to specify the color palette 1 transparent color. 0: Does not set the color of the color palette 1 index 0 to the transparent color. 1: Sets the color of the color palette 1 index 0 to the transparent color.

20.3.3.2 Color Palette 2 Transparent Color Register (CP2TR)

Address: DU0: H'FEB0 0084

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP2IF	CP2IE	CP2ID	CP2IC	CP2IB	CP2IA	CP2I9	CP2I8	CP2I7	CP2I6	CP2I5	CP2I4	CP2I3	CP2I2	CP2I1	CP2I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP2IF	0	R/W	Available	Color Palette 2 Index F This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index F to the transparent color. 1: Sets the color of the color palette 2 index F to the transparent color.
14	CP2IE	0	R/W	Available	Color Palette 2 Index E This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index E to the transparent color. 1: Sets the color of the color palette 2 index E to the transparent color.
13	CP2ID	0	R/W	Available	Color Palette 2 Index D This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index D to the transparent color. 1: Sets the color of the color palette 2 index D to the transparent color.
12	CP2IC	0	R/W	Available	Color Palette 2 Index C This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index C to the transparent color. 1: Sets the color of the color palette 2 index C to the transparent color.
11	CP2IB	0	R/W	Available	Color Palette 2 Index B This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index B to the transparent color. 1: Sets the color of the color palette 2 index B to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	CP2IA	0	R/W	Available	Color Palette 2 Index A This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index A to the transparent color. 1: Sets the color of the color palette 2 index A to the transparent color.
9	CP2I9	0	R/W	Available	Color Palette 2 Index 9 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 9 to the transparent color. 1: Sets the color of the color palette 2 index 9 to the transparent color.
8	CP2I8	0	R/W	Available	Color Palette 2 Index 8 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 8 to the transparent color. 1: Sets the color of the color palette 2 index 8 to the transparent color.
7	CP2I7	0	R/W	Available	Color Palette 2 Index 7 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 7 to the transparent color. 1: Sets the color of the color palette 2 index 7 to the transparent color.
6	CP2I6	0	R/W	Available	Color Palette 2 Index 6 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 6 to the transparent color. 1: Sets the color of the color palette 2 index 6 to the transparent color.
5	CP2I5	0	R/W	Available	Color Palette 2 Index 5 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 5 to the transparent color. 1: Sets the color of the color palette 2 index 5 to the transparent color.
4	CP2I4	0	R/W	Available	Color Palette 2 Index 4 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 4 to the transparent color. 1: Sets the color of the color palette 2 index 4 to the transparent color.
3	CP2I3	0	R/W	Available	Color Palette 2 Index 3 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 3 to the transparent color. 1: Sets the color of the color palette 2 index 3 to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
2	CP2I2	0	R/W	Available	Color Palette 2 Index 2 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 2 to the transparent color. 1: Sets the color of the color palette 2 index 2 to the transparent color.
1	CP2I1	0	R/W	Available	Color Palette 2 Index 1 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 1 to the transparent color. 1: Sets the color of the color palette 2 index 1 to the transparent color.
0	CP2I0	0	R/W	Available	Color Palette 2 Index 0 This bit is used to specify the color palette 2 transparent color. 0: Does not set the color of the color palette 2 index 0 to the transparent color. 1: Sets the color of the color palette 2 index 0 to the transparent color.

20.3.3.3 Color Palette 3 Transparent Color Register (CP3TR)

Address: DU0: H'FEB0 0088

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP3IF	CP3IE	CP3ID	CP3IC	CP3IB	CP3IA	CP3I9	CP3I8	CP3I7	CP3I6	CP3I5	CP3I4	CP3I3	CP3I2	CP3I1	CP3I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP3IF	0	R/W	Available	Color Palette 3 Index F This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index F to the transparent color. 1: Sets the color of the color palette 3 index F to the transparent color.
14	CP3IE	0	R/W	Available	Color Palette 3 Index E This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index E to the transparent color. 1: Sets the color of the color palette 3 index E to the transparent color.
13	CP3ID	0	R/W	Available	Color Palette 3 Index D This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index D to the transparent color. 1: Sets the color of the color palette 3 index D to the transparent color.
12	CP3IC	0	R/W	Available	Color Palette 3 Index C This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index C to the transparent color. 1: Sets the color of the color palette 3 index C to the transparent color.
11	CP3IB	0	R/W	Available	Color Palette 3 Index B This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index B to the transparent color. 1: Sets the color of the color palette 3 index B to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	CP3IA	0	R/W	Available	Color Palette 3 Index A This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index A to the transparent color. 1: Sets the color of the color palette 3 index A to the transparent color.
9	CP3I9	0	R/W	Available	Color Palette 3 Index 9 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 9 to the transparent color. 1: Sets the color of the color palette 3 index 9 to the transparent color.
8	CP3I8	0	R/W	Available	Color Palette 3 Index 8 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 8 to the transparent color. 1: Sets the color of the color palette 3 index 8 to the transparent color.
7	CP3I7	0	R/W	Available	Color Palette 3 Index 7 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 7 to the transparent color. 1: Sets the color of the color palette 3 index 7 to the transparent color.
6	CP3I6	0	R/W	Available	Color Palette 3 Index 6 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 6 to the transparent color. 1: Sets the color of the color palette 3 index 6 to the transparent color.
5	CP3I5	0	R/W	Available	Color Palette 3 Index 5 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 5 to the transparent color. 1: Sets the color of the color palette 3 index 5 to the transparent color.
4	CP3I4	0	R/W	Available	Color Palette 3 Index 4 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 4 to the transparent color. 1: Sets the color of the color palette 3 index 4 to the transparent color.
3	CP3I3	0	R/W	Available	Color Palette 3 Index 3 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 3 to the transparent color. 1: Sets the color of the color palette 3 index 3 to the transparent color.
2	CP3I2	0	R/W	Available	Color Palette 3 Index 2 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 2 to the transparent color. 1: Sets the color of the color palette 3 index 2 to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
1	CP3I1	0	R/W	Available	Color Palette 3 Index 1 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 1 to the transparent color. 1: Sets the color of the color palette 3 index 1 to the transparent color.
0	CP3I0	0	R/W	Available	Color Palette 3 Index 0 This bit is used to specify the color palette 3 transparent color. 0: Does not set the color of the color palette 3 index 0 to the transparent color. 1: Sets the color of the color palette 3 index 0 to the transparent color.

20.3.3.4 Color Palette 4 Transparent Color Register (CP4TR)

Address: DU0: H'FEB0 008C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP4IF	CP4IE	CP4ID	CP4IC	CP4IB	CP4IA	CP4I9	CP4I8	CP4I7	CP4I6	CP4I5	CP4I4	CP4I3	CP4I2	CP4I1	CP4I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15	CP4IF	0	R/W	Available	Color Palette 4 Index F This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index F to the transparent color. 1: Sets the color of the color palette 4 index F to the transparent color.
14	CP4IE	0	R/W	Available	Color Palette 4 Index E This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index E to the transparent color. 1: Sets the color of the color palette 4 index E to the transparent color.
13	CP4ID	0	R/W	Available	Color Palette 4 Index D This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index D to the transparent color. 1: Sets the color of the color palette 4 index D to the transparent color.
12	CP4IC	0	R/W	Available	Color Palette 4 Index C This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index C to the transparent color. 1: Sets the color of the color palette 4 index C to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11	CP4IB	0	R/W	Available	Color Palette 4 Index B This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index B to the transparent color. 1: Sets the color of the color palette 4 index B to the transparent color.
10	CP4IA	0	R/W	Available	Color Palette 4 Index A This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index A to the transparent color. 1: Sets the color of the color palette 4 index A to the transparent color.
9	CP4I9	0	R/W	Available	Color Palette 4 Index 9 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 9 to the transparent color. 1: Sets the color of the color palette 4 index 9 to the transparent color.
8	CP4I8	0	R/W	Available	Color Palette 4 Index 8 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 8 to the transparent color. 1: Sets the color of the color palette 4 index 8 to the transparent color.
7	CP4I7	0	R/W	Available	Color Palette 4 Index 7 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 7 to the transparent color. 1: Sets the color of the color palette 4 index 7 to the transparent color.
6	CP4I6	0	R/W	Available	Color Palette 4 Index 6 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 6 to the transparent color. 1: Sets the color of the color palette 4 index 6 to the transparent color.
5	CP4I5	0	R/W	Available	Color Palette 4 Index 5 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 5 to the transparent color. 1: Sets the color of the color palette 4 index 5 to the transparent color.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
4	CP4I4	0	R/W	Available	Color Palette 4 Index 4 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 4 to the transparent color. 1: Sets the color of the color palette 4 index 4 to the transparent color.
3	CP4I3	0	R/W	Available	Color Palette 4 Index 3 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 3 to the transparent color. 1: Sets the color of the color palette 4 index 3 to the transparent color.
2	CP4I2	0	R/W	Available	Color Palette 4 Index 2 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 2 to the transparent color. 1: Sets the color of the color palette 4 index 2 to the transparent color.
1	CP4I1	0	R/W	Available	Color Palette 4 Index 1 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 1 to the transparent color. 1: Sets the color of the color palette 4 index 1 to the transparent color.
0	CP4I0	0	R/W	Available	Color Palette 4 Index 0 This bit is used to specify the color palette 4 transparent color. 0: Does not set the color of the color palette 4 index 0 to the transparent color. 1: Sets the color of the color palette 4 index 0 to the transparent color.

20.3.3.5 Display Off Mode Output Register n (DOORn)

Address: DU0: H'FEB0 0090, DU1: H'FEB3 0090

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DOR						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DOG						—	—	DOB						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

The two registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 18	DOR	—	R/W	Available	Display Off Mode Output Red These bits are used to set the red display data to be output when the display is off (DRES and DEN bits in the display unit system control register 0 (DSYSR0) are B'00). The set value is retained at a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	DOG	—	R/W	Available	Display Off Mode Output Green These bits are used to set the green display data to be output when the display is off (DRES and DEN bits in the display unit system control register 0 (DSYSR0) are B'00). The set value is retained at a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	DOB	—	R/W	Available	Display Off Mode Output Blue These bits are used to set the blue display data to be output when the display is off (DRES and DEN bits in the display unit system control register 0 (DSYSR0) are B'00). The set value is retained at a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.3.6 Color Detection Register n (CDERn)

Address: DU0: H'FEB0 0094, DU1: H'FEB3 0094

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CDR						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDG						—	—	CDB						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

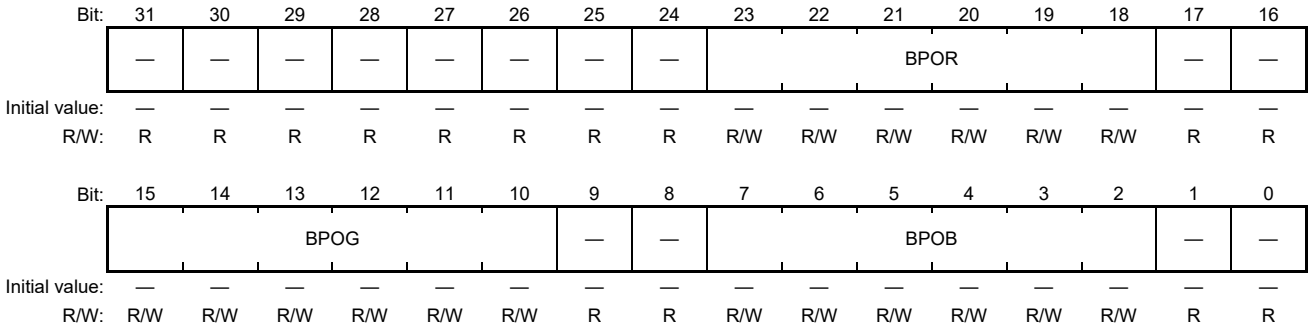
The two registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 18	CDR	—	R/W	Available	Color Detection Red These bits are used to set the red data for color detection. The set value is retained at a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CDG	—	R/W	Available	Color Detection Green These bits are used to set the green data for color detection. The set value is retained at a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CDB	—	R/W	Available	Color Detection Blue These bits are used to set the blue data for color detection. The set value is retained at a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: When output data matches the setting value of this register, the high level is output from the CDE pin. For details about the output color data format, see section 20.4.6, Data Formats for Output and Display Capture.

20.3.3.7 Background Plane Output Register n (BPORn)

Address: DU0: H'FEB0 0098, DU1: H'FEB3 0098



The two registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 18	BPOR	—	R/W	Available	Background Plane Output Red These bits are used to set the red color to be displayed if no plane to be displayed exists due to a display size, transparent color, and so on. The set value is retained at a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	BPOG	—	R/W	Available	Background Plane Output Green These bits are used to set the green color to be displayed if no plane to be displayed exists due to a display size, transparent color, and so on. The set value is retained at a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	BPOB	—	R/W	Available	Background Plane Output Blue These bits are used to set the blue color to be displayed if no plane to be displayed exists due to a display size, transparent color, and so on. The set value is retained at a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.3.8 Raster Interrupt Offset Register n (RINTOFSRn)

Address: DU0: H'FEB0 009C, DU1: H'FEB3 009C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	RINTOFS										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The two registers are for the respective channels and have the same functions.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved
10 to 0	RINTOFS	—	R/W	Available	Raster Interrupt Offset To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 10 cannot be written to. These bits are used to set the raster offset value (number of Hs) that is based on the number of rasters set with the vertical display start register n (VDSRn). If the offset value is assumed to be n, bit 9 in the display unit status register n (DSSRn) is set to 1 at the HSYNC falling edge after the horizontal display period of (VDS + n-th raster). The set value is retained at a reset.

Note: n = 0 and 1.

20.3.4 Display Plane Registers (Alpha-ratio Plane Registers)

In descriptions of registers that are common to planes 1 to 8, the planes are generically referred to as plane n. The meanings of characters n and # are given below.

n: 1 to 8 for this product.

#: Replaces n (in hexadecimal) in addresses. For example, address H'FEB00#00 for the plane 3 mode register corresponds to H'FEB00300.

Descriptions of the registers for the alpha-ratio planes are also given in this section, because a given register for the alpha-ratio planes has almost the same functionality as the corresponding register for the display planes.

Register names:

The names of corresponding registers for the alpha-ratio planes start with the string "Alpha".

Abbreviation:

Abbreviations of the names of corresponding registers for the alpha-ratio planes start with "A".
For alpha-ratio plane registers, n is given as follows;
n: 1, 2 for this product.

Address:

The addresses of registers for the alpha-ratio planes are given to the right of the address information for the corresponding display-plane registers (# = 1, 2 for this product).

The plane n memory width register (PnMWR) for the alpha-ratio planes, for example, is the alpha-ratio plane n memory width register (APnMWR).

The alpha-ratio plane n mode register (APnMR) is described separately because its functionality differs from that of a plane n mode register (PnMR).

20.3.4.1 Plane n Mode Register (PnMR)

Address: DU0: H'FEB00#00 (for alpha-ratio planes; refer to section 20.3.4.24, Alpha-ratio Plane n Mode Register (APnMR))

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PnVISL		—	—	—	—	—	Pn YCDF	—	—	PnTC	PnWAE
Initial value:	—	—	—	—	0	0	—	—	—	—	—	0	—	—	0	0
R/W:	R	R	R	R	R/W	R/W	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PnSPIM			—	PnCPSL			PnDC	—	PnBM		—	—	PnDDF	
Initial value:	—	0	0	0	—	0	0	0	0	—	0	0	—	—	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R	R	R/W	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27, 26	PnVISL	00	R/W	Available	Plane n Video Input Select To enable these bits, set the DEFE bit in the display unit extensional function control register 0 (DEFR0) to 1. In the initial state, these bits cannot be set to 1. 00: Video input 0 (VIN0) is selected. 01: Video input 1 (VIN1) is selected. 10: Setting prohibited 11: Setting prohibited
25 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	PnYCDF	0	R/W	Available	Plane n YC Data Format 0: Sets the alignment of YC data to UYVY format. 1: Sets the alignment of YC data to YUYV format.
19, 18	—	—	R	—	Reserved The setting is invalid when an 8-bit/pixel display has not been selected.
17	PnTC	0	R/W	Available	Plane n Transparent Color 0: When an 8-bit/pixel display has been selected, the transparent color is that indicated by the value of PnTC1R 1: When an 8-bit/pixel display has been selected, the transparent color is that indicated by the value of CPT1R to CPT4R The setting is invalid when an 8-bit/pixel display has not been selected. For details, refer to section 20.4.9 (2), Transparent Colors.
16	PnWAE	0	R/W	Available	Plane n Wrap-Around Enable 0: Wrapping-around for plane n is disabled. 1: Wrapping-around for plane n is enabled.
15	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
14 to 12	PnSPIM	000	R/W	Available	Plane n Super Impose Mode 000: Transparent color processing is performed for plane n. When plane n is in the transparent color, the lower plane is displayed. 001: α blending of plane n and the lower plane is performed. When plane n is the transparent color, α blending is not performed, and the lower plane is displayed. 010: An EOR operation is performed on plane n and the lower plane. When plane n is the transparent color the EOR operation is not performed, and the lower plane is displayed. 011: Setting prohibited 100: Transparent color processing is not performed for plane n. Plane n is displayed. 101: α blending of plane n and the lower plane is performed. The transparent color specification for plane n is ignored, and α blending is performed between all the pixels of plane n and the lower plane. 110: An EOR operation is performed on plane n and the lower plane. The transparent color specification for plane n is ignored, and EOR operation is performed on all the pixels of plane n and the lower plane. 111: Setting prohibited Transparent color processing for YC data is not possible. Transparent color processing is not possible when the PnLRGB1 bit or PnLRGB0 bit in the plane n display data control register (PnDDCR) specifies 32-bit/pixel data. Transparent color processing is possible when 32-bit/pixel data is specified by plane n display data control 4 register (PnDDC4R).
11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 8	PnCPSL	000	R/W	Available	Plane n Color Palette Select These bits indicate whether the color palette is to be used when the value of the PnDDF bits is B'00 (i.e. the plane n display data format is 8-bit/pixel). 000: Use color palette 1 001: Use color palette 2 010: Use color palette 3 011: Use color palette 4 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited
7	PnDC	0	R/W	Available	Plane n Display Area Change 0: In manual display change mode, switching of the frame buffer is not performed. 1: In manual display change mode, switching of the frame buffer is performed. When the PnDC bit is 0, bit setting is possible. Switching is performed in frame units. After frame buffer switching (after vertical blanking detection), this bit is cleared to 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5, 4	PnBM	00	R/W	Available	Plane n Buffer Mode 00: Manual display change mode 01: Auto rendering mode 10: Auto display change mode (blinking mode) 11: Video capture mode In manual display change mode, auto rendering mode, or auto display change mode (blinking mode), double-buffering control is performed using addresses 0 and 1, respectively indicated by the PnDSA0 and PnDSA1 bits in PnDSA0R and PnDSA1R. In video capture mode, triple-buffering control is performed using addresses 0 to 2 indicated by bits 31 to 26 of the display unit status register 0 (DSSR0) or the display unit video capture status register (DVCSR).
3, 2	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
1, 0	PnDDF	00	R/W	Available	Plane n Display Data Format 00: 8-bit/pixel 01: 16-bit/pixel 10: ARGB (ARGB1555) 11: YC (YUV422 is converted to RGB888). When bits 9 and 8 in the display unit extensional function control register 1 (DEFR1) are set to B'10 or B'11, conversion to RGB888 is not performed. In the case of 32-bit/pixel data, set these bits to B'01.

20.3.4.2 Plane n Memory Width Register (PnMWR)

Address: DU0: H'FEB00#04 (Alpha ratio plane address: DU0: H'FEB0A#04)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	PnMWX									—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 4	PnMWX	—	R/W	Available	Plane n Memory Width X The plane n memory width should be set in the range 16 pixels to 4096 pixels, in 16-pixel units. If the image data are in 32-bit/pixel format, and the scan mode is set as the interlaced sync & video mode, specify a value corresponding to double the desired size in the PnMWX bits. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.4.3 Plane n Blending Ratio Register (PnALPHAR)

Address: DU0: H'FEB00#08 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PnABIT		—	PnBRSL			PnALPHA							
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13, 12	PnABIT	—	R/W	Available	Plane n A Bit Function Select This facility is not available for 32-bit/pixel data. In the initial state, these bits are fixed to 0. To enable these bits, set the DEFE2G bit in DEF2R to 1. 00: In ARGB mode (i.e. when the value of the PnDDF bits in PnMR is B'10), α blending is performed when the value of A is 1. 01: In ARGB mode (i.e. when the value of the PnDDF bits in PnMR is B'10), α blending is performed when the value of A is 0. 1-: In ARGB mode (i.e. when the value of the PnDDF bits in PnMR is B'10), α blending is performed regardless of the value of A. The value is retained during a reset.
11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	PnBRSL	—	R/W	Available	Plane n Blending Ratio Select This bit is valid when the value of the PnSPIM bits in PnMR allows α blending. In the initial state, bit 10 is fixed to 0. To enable bit 10, set the DEFE bit in DEFR0 to 1. -00: The value of bits 7 to 0 in this register is taken to be the alpha ratio. -01: Setting prohibited -10: Bits 31 to 24 of the color palette register specified by the PnCPSL bits in PnMR are taken to be the alpha ratio. Note: This setting is only effective when the display data format specified by the PnDDF bits in PnMR is 8-bit/pixel. For formats other than 8-bit/pixel, the value of bits 7 to 0 in this register is taken to be the alpha ratio. 011: The display data for the plane specified by bits 2 to 0 in this register is taken to be the alpha ratio. Bits 2 to 0 = 000: Display data for plane 1 is the alpha ratio Bits 2 to 0 = 001: Display data for plane 2 is the alpha ratio Bits 2 to 0 = 010: Display data for plane 3 is the alpha ratio Bits 2 to 0 = 011: Display data for plane 4 is the alpha ratio Bits 2 to 0 = 100: Display data for plane 5 is the alpha ratio Bits 2 to 0 = 101: Display data for plane 6 is the alpha ratio Bits 2 to 0 = 110: Display data for plane 7 is the alpha ratio Bits 2 to 0 = 111: Display data for plane 8 is the alpha ratio Notes: 1. When the register's own plane is specified, the value of bits 7 to 0 in this register is taken to be the alpha ratio. 2. The specified plane should satisfy the following conditions. If the conditions are not satisfied, the alpha ratio is undefined. - The display should be turned on by using DPPR. - The display data format should be set to 8-bit/pixel. - The display size should be greater than or equal to the size of the plane for this register. - Ensure that display positions (X and Y) are the same as those in the plane for this register.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	PnBRSL	—	R/W	Available	111: The display data for the alpha-ratio plane specified by bits 2 to 0 in this register is taken to be the alpha ratio. Bits 2 to 0 = 000: Display data for α plane 1 is the alpha ratio Bits 2 to 0 = 001: Display data for α plane 2 is the alpha ratio Take the following steps before setting PnBRSL = 111. 1. Set the desired value in a register listed in section 20.3.4, Display Plane Registers (Alpha-ratio Plane Registers) 2. Set the AP1E or AP2E bit in DAPCR to 1. 3. Make the timing and dot clock settings in DPTSR and DAPTSR. The settings in DPTSR and DAPTSR should be the same. The value is retained during a reset.
7 to 0	PnALPHA	—	R/W	Available	Plane n Blending Ratio These bits indicate the alpha ratio (α), which determines the blending ratio for plane n. This facility is not available for 32-bit/pixel data. Blending result ≈ (plane n × α/255) + lower plane × (1 - α/255) (Approximation) Note: Blending result, α, plane n, and lower plane in the above formula are all 8-bit data. The value is retained during a reset.

20.3.4.4 Plane n Display Size X Register (PnDSXR)

Address: DU0: H'FEB00#10 (Alpha ratio plane address: DU0: H'FEB0A#10)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PnDSX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnDSX	—	R/W	Available	Plane n Display Size X To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. The horizontal-direction display size of plane n should be set in dot clock units. Note: When YC has been selected by the PnDDF bits in PnMR, this value should be set to an even number. The value is retained during a reset.

20.3.4.5 Plane n Display Size Y Register (PnDSYR)

Address: DU0: H'FEB00#14 (Alpha ratio plane address: DU0: H'FEB0A#14)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	PnDSY										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
10 to 0	PnDSY	—	R/W	Available	Plane n Display Size Y To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 10 cannot be written to. The vertical-direction display size of plane n should be set in raster line units. The value is retained during a reset.

20.3.4.6 Plane n Display Position X Register (PnDPXR)

Address: DU0: H'FEB00#18 (Alpha ratio plane address: DU0: H'FEB0A#18)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PnDPX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnDPX	—	R/W	Available	Plane n Display Position X To enable bit 11, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 11 cannot be written to. The horizontal start position on the display monitor of plane n should be set in dot clock units, taking as the origin the upper-left corner of the display monitor. Note: When YC has been selected by the RGBYC0 bit in the display unit extensional function control 5 register (DEF5R) during display output from DU0, this value should be set to an even number. When YC has been selected by the DODF1 bit in the display unit extensional function control register 1 (DEFR1) / DODF1 during display output from DU1, this value should be set to an even number. The value is retained during a reset.

20.3.4.7 Plane n Display Position Y Register (PnDPYR)

Address: DU0: H'FEB00#1C (Alpha ratio plane address: DU0: H'FEB0A#1C)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	PnDPY										
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 0	PnDPY	—	R/W	Available	Plane n Display Position Y To enable bit 10, set the DEFE5 bit in the display unit extensional function control 5 register (DEF5R) to 1. In the initial state, bit 10 cannot be written to. The vertical start position on the display monitor of plane n should be set in raster line units, taking as the origin the upper-left corner of the display monitor. For interlaced sync & video display, the display starts at the position one bit shifted from the PnDPY bit setting value. PnDPY Vertical start position 0 0 1 0 2 1 3 1 4 2 For non-interlaced and interlaced sync display, the display starts at the position specified by the PnDPY bit. • When you set one or more values to this register at the time of interlace sync & video, please add one half of the preset values of this register to the VDE bits of the vertical display end register n (VDERn) (n = 0 and 1). Add further 1, when the number of preset values is odd -- when you have set up by two or more planes, please add the maximum. Adding to the value of VDERn can lead to the effects described against (1) and (2) below. Depending on the monitor, these may make display impossible. Use of this register when such cases arise in interlace sync & video mode is prohibited. (1) Although the DISP signal was originally at the low level in the vertical blanking interval, the DISP signal will be at the high level until the next falling edges of the VSYNC and HSYNC signals. (2) Although all bits of the data for display were 0 in the vertical blanking interval, values become non-zero in the same interval as effect (1). This becomes the value of the DDR for the display data if settings of the PnDSY and PnDPY bit fields cause the display to jut out in the vertical direction and the value of the BPORn field if the display does not jut out (n is 0 or 1). In the case of a non-interlace and an interlace sync, the necessity for addition is not. The value is retained during a reset.

20.3.4.8 Plane n Display Area Start Address 0 Register (PnDSA0R)

Address: DU0: H'FEB00#20 (Alpha ratio plane address: DU0: H'FEB0A#20)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PnDSA0															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnDSA0												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	PnDSA0	—	R/W	Available	Plane n Display Area Start Address 0 To enable bits 31 to 29, the DEFE bit in DEFR0 must be set to 1. In the initial state, these bits are not enabled. When the buffer mode for plane n is manual display, auto rendering, auto display change, or video capture, the area indicated by this register is used as frame buffer 0. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.4.9 Plane n Display Area Start Address 1 Register (PnDSA1R)

Address: DU0: H'FEB00#24 (Alpha ratio plane address: DU0: H'FEB0A#24)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PnDSA1															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnDSA1												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	PnDSA1	—	R/W	Available	Plane n Display Area Start Address 1 To enable bits 31 to 29, the DEFE bit in DEFR0 must be set to 1. In the initial state, these bits are not enabled. When the buffer mode for plane n is manual display, auto rendering, auto display change, or video capture, the area indicated by this register is used as frame buffer 1. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.4.10 Plane n Display Area Start Address 2 Register (PnDSA2R)

Address: DU0: H'FEB00#28 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PnDSA2															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnDSA2												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	PnDSA2	—	R/W	Available	Plane n Display Area Start Address 2 To enable bits 31 to 29, the DEFE bit in DEFR0 must be set to 1. In the initial state, these bits are not enabled. When the buffer mode for plane n is video capture, the area indicated by this register is used as frame buffer 2. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.4.11 Plane n Start Position X Register (PnSPXR)

Address: DU0: H'FEB00#30 (Alpha ratio plane address: DU0: H'FEB0A#30)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PnSPX											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnSPX	—	R/W	Available	Plane n Start Position X Specify the distance in the X direction to the position where plane n starts in memory. Notes: 1. When YC has been selected by the PnDDF bits in PnMR, the value should be even. 2. Setting of a value greater than twice the value of the PnMWX bits is prohibited. The value is retained during a reset.

20.3.4.12 Plane n Start Position Y Register (PnSPYR)

Address: DU0: H'FEB00#34 (Alpha ratio plane address: DU0: H'FEB0A#34)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnSPY															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 0	PnSPY	—	R/W	Available	Plane n Start Position Y Specify the distance in the Y direction to the position where plane n starts in memory. If an image data is in 32-bit/pixel data format, specify a value that is twice a desired value to the PnSPY bit. If memory length has been specified in PnMLR, add a desired value for the start position to the PnMLY bit setting value. Note: Setting of a value greater than twice {the value of the PnWASPY bits + the value of the PnWAMWY bits} is prohibited. The value is retained during a reset.

20.3.4.13 Plane n Wrap-Around Start Position Register (PnWASPR)

Address: DU0: H'FEB00#38 (Alpha ratio plane address: DU0: H'FEB0A#38)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PnWASPY										—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13 to 4	PnWASPY	—	R/W	Available	Plane n Wrap-Around Start Position Y The Y direction start position of one wrap-around area should be set with reference to the address specified in PnDSA0R, PnDSA1R and PnDSA2R. The position where wrapping-around is to start can be set in 16-pixel units (bits 3 to 0: Fixed to 0). If an image data is in 32-bit/pixel data format, specify a value that is twice a desired value to the PnWASPY bit. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.4.14 Plane n Wrap-Around Memory Width Register (PnWAMWR)

Address: DU0: H'FEB00#3C (Alpha ratio plane address: DU0: H'FEB0A#3C)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	PnWAMWY											
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	PnWAMWY	—	R/W	Available	Plane n Wrap-Around Memory Width Y The memory width for wrap-around in the Y-direction should be set to a number corresponding to a value in the range from 240 to 4095 raster lines. If an image data is in 32-bit/pixel data format, specify a value that is twice a desired value to the PnWAMWY bit. The value is retained during a reset.

20.3.4.15 Plane n Blinking Time Register (PnBTR)

Address: DU0: H'FEB00#40 (Alpha ratio plane address: DU0: H'FEB0A#40)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnBTA								PnBTB							
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 8	PnBTA	0000 0001	R/W	Available	Plane n Blinking Time A
7 to 0	PnBTB	0000 0001	R/W	Available	Plane n Blinking Time B

Note: When the PnBM bits in PnMR are set to select the auto display change mode (blinking mode), specify, as numbers of fields, the times over which plane n display area start address registers 0 and 1 (PnDSA0R and PnDSA1R) are to be displayed. Blinking operation employs the settings in PnDSA0R and PnDSA1R.
Setting this register to 1 (the value should be other than 0) leads to switching between the buffers at the addresses indicated by the plane n display area start address registers 0 and 1 (PnDSA0R and PnDSA1R) on each field unit.

20.3.4.16 Plane n Transparent Color 1 Register (PnTC1R)

Address: DU0: H'FEB00#44 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PnTC1							
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	PnTC1	—	R/W	Available	Plane n Transparent Color 1 for 8-bit/pixel This setting is for a transparent color for plane n in the 8-bit/pixel data format. To enable the transparent color setting in this register, the PnTC bit in PnMR must be set to 0. The value is retained during a reset.

20.3.4.17 Plane n Transparent Color 2 Register (PnTC2R)

Address: DU0: H'FEB00#48 (unused for the alpha-ratio planes)

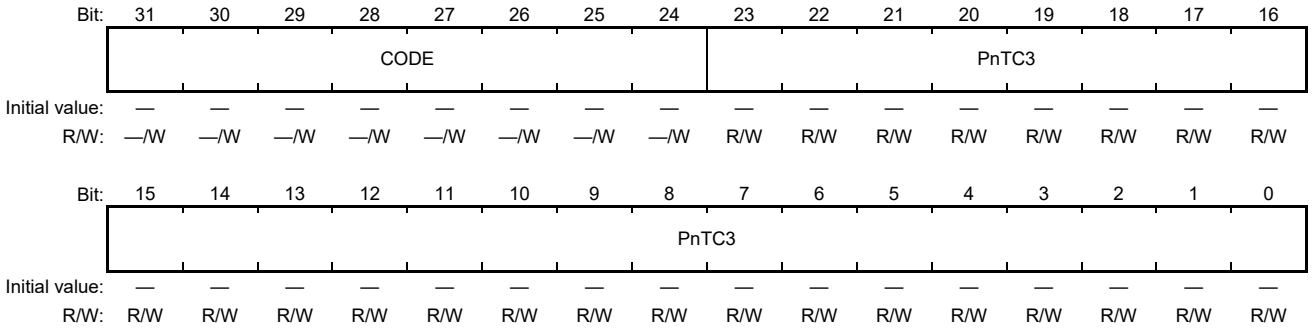
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnTC2															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 0	PnTC2	—	R/W	Available	Plane n Transparent Color 2 for 16-bit/pixel This setting is for a transparent color for plane n in the 16-bit/pixel or ARGB data format. In the case of ARGB, comparison is with bits 14 to 0 of this register, i.e. bit 15 is ignored. The value is retained during a reset.

20.3.4.18 Plane n Transparent Color 3 Register (PnTC3R)

Address: DU0: H'FEB00#4C (unused for the alpha-ratio planes)



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CODE	—	—/W	Not available	PnTC3R Enabling Code (register available code) For a value written to PnTC3R to be effective, the value must include H'66 in these bits.
23 to 0	PnTC3	—	R/W	Available	Plane n Transparent Color 3 These bits are used to specify the transparent color for the ARGB8888, RGB888, or RGB666 data format. See Table 20.24 for the bits to be compared.

Table 20.24 Data Comparison by Plane n Transparent Color 3 Register (PnTC3R)

Bits in PnTC3R	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
ARGB8888 or RGB888	R7	R6	R5	R4	R3	R2	R1	R0	G7	G6	G5	G4	G3	G2	G1	G0	B7	B6	B5	B4	B3	B2	B1	B0
RGB666	R5	R4	R3	R2	R1	R0	X	X	G5	G4	G3	G2	G1	G0	X	X	B5	B4	B3	B2	B1	B0	X	X

Note: "X" is not compared.

20.3.4.19 Plane n Memory Length Register (PnMLR)

Address: DU0: H'FEB00#50 (Alpha ratio plane address: DU0: H'FEB0A#50)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PnMLY
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PnMLY															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16 to 0	PnMLY	H'00000	R/W	Available	Plane n Memory Length Y These bits indicate the length in memory (memory area in the Y-direction) of plane n. When the actual display is beyond this area, the data selected in BPORn will be displayed. When the value is 0 (initial value), the area is handled as an infinite area. Thus the data selected in BPORn will never be displayed. (n = 0 and 1) If an image data is in 32-bit/pixel data format and a value other than 0 is specified in PnSPYR, add a value that is half the PnSPYR bit setting value to this bit value.

20.3.4.20 Plane n SWAP Control Register (PnSWAPR)

Address: DU0: H'FEB00#80 (Alpha ratio plane address: DU0: H'FEB0A#80)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	Pn DIGN	Pn SPQW	Pn SPLW	Pn SPWD	Pn SPBY
Initial value:	—	—	—	—	—	—	—	—	—	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnSWAPR Enabling Code (register available code) For a value written to PnSWAPR to be effective, the value must include H'7775 in these bits.
15 to 5	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
4	PnDIGN	0	R/W	Available	Plane n Display Data Format Invalid This bit is used in combination with bit 0 to control swapping of data in byte (8-bit) units. Also see the description of bit 0. The setting of this bit does not affect the values of bits 3 to 1.
3	PnSPQW	0	R/W	Available	Plane n Quadword Swap Enable 0: Data are not swapped. 1: Data are swapped in quadword (64-bit) units if bit 20 of DSYSRn is 0. (n = 0 and 1)
2	PnSPLW	0	R/W	Available	Plane n Longword Swap Enable 0: Data are not swapped. 1: Data are swapped in longword (32-bit) units if bit 20 of DSYSRn is 0. (n = 0 and 1)
1	PnSPWD	0	R/W	Available	Plane n Word Swap Enable 0: Data are not swapped. 1: Data are swapped in word (16-bit) units if bit 20 of DSYSRn is 0. (n = 0 and 1)
0	PnSPBY	0	R/W	Available	Plane n Byte Swap Enable This bit is used in combination with bit 4 to control swapping of data in byte (8-bit) units. The following combinations of values are possible when bit 20 of DSYSRn is 0. (n = 0 and 1) 00: Data are not swapped. 01: Data are not swapped. 10: Data are swapped in byte (8-bit) units if the value of the PnDDF bits in PnMR is 00 or 11. In other cases, data are not swapped. 11: Data are swapped in byte (8-bit) units.

Note: The settings of bit 20 (DSEC) of the display unit system control register n (DSYSRn), the PnDDF bit of the plane n mode register (PnMR), and this register are listed with their results below (n = 0 and 1).

All combinations of the values of the bits in PnSWAPR, the DSEC bit in DSYSRn, and the PnDDF bits in PnMR are shown below.

Table 20.25 Summary of Endian Conversion

DSEC	PnSPQW	PnSPLW	PnSPWD	PnSPBY	PnDIGN	PnDDF	Data Format	Swap Unit
1	—	—	—	—	—	00	8-bit/pixel	128 bits in byte units
						01	16-bit/pixel (RGB data)	128 bits in word units
						10	ARGB	128 bits in word units
						11	YC	128 bits in byte units
0	0	0	0	0	—	—	—	No conversion
	1	—	—	—	—	—	—	64 bits units
	—	1	—	—	—	—	—	32 bits units
	—	—	1	—	—	—	—	16 bits units
	—	—	—	1	0	00	8-bit/pixel	8 bits units
						01	16-bit/pixel (RGB data)	No conversion
						10	ARGB	No conversion
						11	YC	8 bits units
					1	—	—	8 bits units

20.3.4.21 Plane n Display Data Control Register (PnDDCR)

Address: DU0: H'FEB00#84 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	Pn LRGB1	Pn LRGB0	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	0	0	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnDDCR Enabling Code (register available code) For a value written to PnDDCR to be effective, the value must include H'7775 in these bits.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11	PnLRGB1	0	R/W	Available	Plane n 32-bit/pixel display control 1 (Plane n Long (32 bits) RGB1) 0: Data are not handled as 32-bit/pixel (ARGB8888). 1: Data in the plane are used as the lower-order bits (G: 8 bits and B: 8 bits) of 32-bit/pixel data (ARGB8888). When a 32-bit/pixel display is specified with this bit, the following restrictions apply. When specifying a 32-bit/pixel display with the PnEDF bits in plane n display data control 4 register (PnDDC4R), refer to the description of the PnEDF bits. Only ARGB8888 can be specified for 32-bit/pixel data. This bit must be set for plane n after setting of bit 10 for plane n–1 to 1. For example, if bit 10 of P1DDCR is set to 1, bit 11 of P2DDCR must be set to 1. The value of the PnDDF bits in PnMR must be 01. Do not set bits 11 and 10 to 1 at the same time. When bit 10 is set to 1, data are handled as 32-bit/pixel even if bit 11 is set to 0, and thus the function that bit 10 is set to 1 is realized. Since transparent color processing is not possible with 32-bit/pixel data, set the PnSPIM bit in PnMR to 1. α blending or EOR operations for 32-bit/pixel data and a lower plane must be performed in an area where the lower plane exists. If there is no lower plane, display of 32-bit/pixel data will not be possible after α blending or an EOR operation.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10	PnLRGB0	0	R/W	Available	Plane n Long (32 Bits) RGB 0 0: Data are not handled as 32-bit/pixel (ARGB8888). 1: Data in the plane are used as the higher-order bits (A: 8 bits and R: 8 bits) of 32-bit/pixel data (ARGB8888). When a 32-bit/pixel display is specified with this bit, the following restrictions apply. When specifying a 32-bit/pixel display with the PnEDF bits in plane n display data control 4 register (PnDDC4R), refer to the description of the PnEDF bits. Only ARGB8888 can be specified for 32-bit/pixel data. The value of A (8 bits) will be used as the alpha ratio. This means that the alpha ratio selected in the plane n blending ratio register (PnALPHAR) is invalid. Also, the value of the PnDDF bits in PnMR must be B'01. Use planes 1 and 2 for a 32-bit/pixel display. Do not set bits 11 and 10 to 1 at the same time. When bit 11 is set to 1, data are handled as 32-bit/pixel even if bit 10 is set to 0, and thus the function that bit 11 is set to 1 is realized. Since transparent color processing is not possible with 32-bit/pixel data, set the PnSPIM bit in PnMR to 1. α blending or EOR operations for 32-bit/pixel data and a lower plane must be performed in an area where the lower plane exists. If there is no lower plane, display of 32-bit/pixel data will not be possible after α blending or an EOR operation.
9 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Use planes 1 and 2 if the display is to have 32-bit/pixel. In this display unit, a 32-bit/pixel display by a single plane is possible. For a 32-bit/pixel display using a single plane, refer to the description of the PnEDF bits in plane n display data control 4 register (PnDDC4R). Register settings for using planes 1 and 2 in a 32-bit/pixel display are given below. Note that the setting of (d) shown below must be made at the last. All other settings can be made in any order.

(a) Set the LRUO bit in display unit extensional function control 4 register (DEF4R) to 1.

(b) The settings for this register are shown below.

Bit:	15	14	13	12	11	10	9	8
					PnLRGB1	PnLRGB0		
Plane 1 (A, R)	—	—	—	—	0	1	—	—
Plane 2 (G, B)	—	—	—	—	1	0	—	—

(c) The same settings should be made in the plane 1 and plane 2 registers of display plane registers other than this register.

(d) Turn on the display of planes 1 and 2, and give plane 2 the next order of priority for processing after plane 1. For details on turning on the display, see section 20.4.2, Display On/Off.

(e) A 32-bit/pixel display should always be specified in lower-numbered planes. For example, when the 32- and 16-bit /pixel display planes are to be superimposed, the 32-bit/pixel display should be specified in planes 1 and 2, and the 16-bit/pixel display should be specified in plane 3 or in higher-numbered planes.

(f) When the video input module is to be used, refer to the specifications for the video input module.

(g) If the DU operates in big-endian, set bits 3 and 2 in the plane n swap control register (PnSWAPR) to 1 and bits 1 and 0 to 0. Bit 4 may be set to either 1 or 0. Set bit 20 in the display system control register n (DSYSRn) to 0 (n = 0 and 1).

20.3.4.22 Plane n Display Data Control 2 Register (PnDDC2R)

Address: DU0: H'FEB00#88 (unused for the alpha-ratio planes)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	Pn NV21	Pn Y420	—	—	Pn DIVU	Pn DIVY
Initial value:	—	—	—	—	—	—	—	—	—	—	0	0	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	PnDDC2R Enabling Code (register available code) For a value written to PnDDC2R to be effective, the value must include H'7776 in these bits.
15 to 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5	PnNV21	0	R/W	Available	Plane n NV21 Data Format This bit is only effective when bits 1 and 4 have been set to 1. 0: When YUV420 data are divided up for storage in memory, the order of the UV portion is NV12. 1: When YUV420 data are divided up for storage in memory, the order of the UV portion is NV21.
4	PnY420	0	R/W	Available	Plane n YUV420 Data Format This bit is only effective if bit 1 has been set to 1. When bit 1 is 0, the data format will be YUV422. 0: The YUV data to be divided up for storage in memory is YUV422. 1: The YUV data to be divided up for storage in memory is YUV420. For divided YUV display, see section 20.4.20, Divided YUV Display.
3, 2	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
1	PnDIVU	0	R/W	Available	Plane n UV Data from Divided YUV 0: The data format will be determined by the setting of the PnDDF bits in PnMR. 1: The setting of the PnDDF bits in PnMR is ineffective and the plane contains the UV data from YUV data that have been divided up for storage in memory. To validate the YC→RGB color space functions, set the PnDDF bits in PnMR to B'11 (YC format). Do not set bits 1 and 0 in this register at the same time. When bit 0 is set to 1, the data format will not be determined by the setting of the PnDDF bits in PnMR even if this bit is set to 0. The data format will be determined by bit 0 in this register being set to 1. For divided YUV display, see section 20.4.20, Divided YUV Display.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
0	PnDIVY	0	R/W	Available	Plane n Y Data from Divided YUV 0: The data format will be determined by the setting of the PnDDF bits in PnMR. 1: The setting of the PnDDF bits in PnMR is ineffective and the data format is the Y data from YUV data that have been divided up for storage in memory. To validate the YC→RGB color space functions, set the PnDDF bits in PnMR to B'11 (YC format). Do not set bits 1 and 0 in this register at the same time. When bit 1 is set to 1, the data format will not be determined by the setting of the PnDDF bits in PnMR even if this bit is set to 0. The data format will be determined by bit 1 in this register being set to 1. For divided YUV display, see section 20.4.20, Divided YUV Display.

20.3.4.23 Plane n Display Data Control 4 Register (PnDDC4R)

Address: DU0: H'FEB00#90 (Alpha ratio plane address: DU0: H'FEB0A#90)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CODE															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W	—/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PnVSPS	—	—	—	—	—	—	—	—	—	—	PnEDF		
Initial value:	—	—	0	—	—	—	—	—	—	—	—	—	—	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Note: * For reserved bit (bit name: —), initial value is undefined, writing is not available and writing value should be specified. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—	Not available	PnDDC4R Enabling Code (register available code) For a value written to PnDDC4R to be effective, the value must include H'7766 in these bits.
15, 14	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
13	PnVSPS	0	R/W	Available	Plane n VSP1 Select To enable bit 13, set the DEFE8 bit in the display unit extensional function control 8 register (DEF8R) to 1. Bit 13 is fixed to 0 in its initial state. 0: Uses image data in memory. 1: Uses image data in VSP1. This data can be used only in plane 1. Transparent color processing for VSP1 data is not possible. The format of the pixel data is either ARGB8888 or RGB888. Only the value A for VSP1 is applied as the alpha value in ARGB8888.
12 to 3	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
2 to 0	PnEDF	000	R/W	Available	Plane n Extensional Data Format 000: The data format will be determined by the PnDDF bits in PnMR, the PnLRGB1 or PnLRGB0 bit in PnDDCR, or the PnDIVU or PnDIVY bit in PnDDC2R. 001: ARGB8888 010: RGB888 011: RGB666 100: Setting prohibited 101: Setting prohibited 110: Setting prohibited 111: Setting prohibited This data format cannot be used for alpha-ratio planes. If the DU operates in big-endian, set bits 3 and 2 in PnSWAPR to 1 and bits 1 and 0 to 0. Bit 4 may be set to either 1 or 0. Set bit 20 in DSYSRn to 0 (n = 0 and 1).

20.3.4.24 Alpha-ratio Plane n Mode Register (APnMR)

Address: DU0: H'FEB0A#00

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PnWAE
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	PnDC	—	PnBM		—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	0	—	0	0	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16	PnWAE	0	R/W	Available	Plane n Wrap-Around Enable 0: Wrapping-around for plane n is disabled. 1: Wrapping-around for plane n is enabled.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7	PnDC	0	R/W	Available	Plane n Display Area Change 0: In manual display change mode, switching of the frame buffer is not performed. 1: In manual display change mode, switching of the frame buffer is performed. When the PnDC bit is 0, bit setting is possible. Switching is performed in frame units. After frame buffer switching (after vertical blanking detection), this bit is cleared to 0.
6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5, 4	PnBM	00	R/W	Available	Plane n Buffer Mode 00: Manual display change mode 01: Setting prohibited 10: Auto display change mode (blinking mode) 11: Setting prohibited In manual display change mode or auto display change mode (blinking mode), double-buffering control is performed using addresses 0 and 1, respectively indicated by the PnDSA0 and PnDSA1 bits in PnDSA0R and PnDSA1R.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

The functions of the plane n mode register (PnMR) are partially unavailable in the alpha-ratio plane n mode register (APnMR) because the functions of the planes dedicated to the α value are limited more than those of the display planes. The following bits are unavailable, and thus absent.

Bit 20 (PnYCDF) is absent because the display data format is fixed to 8-bit/pixel.

Bit 17 (PnTC) is absent because the alpha ratios cannot be treated as a transparent color.

Bits 14 to 12 (PnSPIM) are absent because superpositioning is not available.
Bits 10 to 8 (PnCPSL) are absent because the use of a color palette is not possible.
Bits 1 and 0 (PnDDF) are absent because the display data format is fixed to 8-bit/pixel.

20.3.5 Display Capture Registers

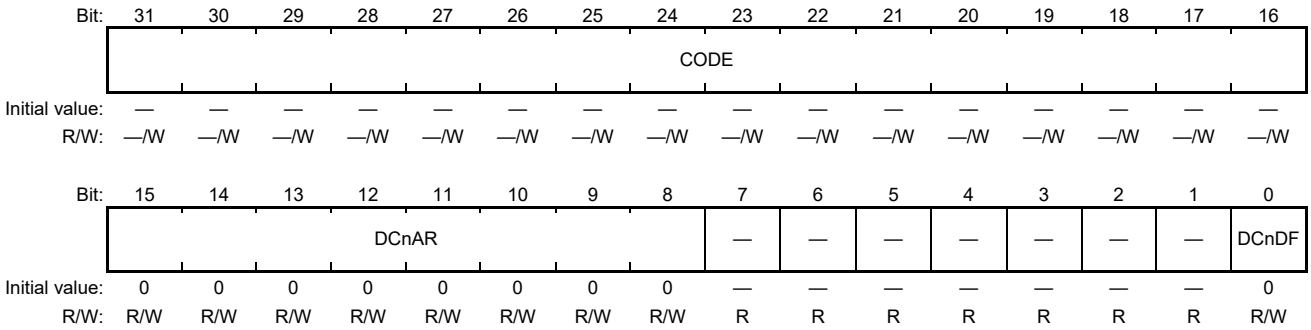
In descriptions that are common to display capture units 1 and 2, the display capture units are generically referred to as display capture n. This meaning of character n and the meaning of # are given below.

n: no number or 2

#: Corresponds to n but represents a hexadecimal digit in an address. For example, address H'FEB0C#04 for the capture 1 memory width register corresponds to H'FEB0C104.

20.3.5.1 Display Capture n Mode Register (DCnMR)

Address: DU0: H'FEB0C#00



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 16	CODE	—	—/W	Not available	DCnMR Enabling Code (register available code) For a value written to DCnMR to be effective, the value must include H'7790 in these bits.
15 to 8	DCnAR	0	R/W	Available	Display Capture n Alpha Ratio This bit is effective when bit 0 in this register is set to 1.
7 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DCnDF	0	R/W	Available	Display Capture n Data Format 0: The data format is determined by bits 5 and 4 in DCPCR. 1: The data format is ARGB8888. The “A” value is specified by bits 15 to 8 in this register.

20.3.5.2 Display Capture n Memory Width Register (DCnMWR)

Address: DU0: H'FEB0C#04

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	DCnMWX									—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 4	DCnMWX	—	R/W	Available	Display Capture n Memory Width X Select the memory width for display capture n to a value between 16 and 4096 pixels, in 16-pixel units. When the width of captured data exceeds this size, the excess data will not be captured. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.5.3 Display Capture n Area Start Address Register (DCnSAR)

Address: DU0: H'FEB0C#20

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCnSA															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCnSA												—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 4	DCnSA	—	R/W	Available	Display Capture n Area Start Address To enable bits 31 to 29, the DEFE bit in DEFR0 must be set to 1. In the initial state, these bits are not enabled. The value is retained during a reset.
3 to 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

20.3.5.4 Display Capture n Memory Length Register (DCnMLR)

Address: DU0: H'FEB0C#50

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DCnMLY
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCnMLY															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
16 to 0	DCnMLY	H'0 0000	R/W	Available	Display Capture n Memory Length Y Select the memory length (Y-direction memory area) for display capture n. When the value of these bits is 0 (default), the size is unlimited.

20.3.6 Color Palette Registers

20.3.6.1 Color Palette 1 (000 to 255) Register (CP1_000R to CP1_255R)

Address: DU0: H'FEB01000 to H'FEB013FC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CP1_000A								CP1_000R						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP1_000G						—	—	CP1_000B						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

..

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CP1_255A								CP1_255R						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP1_255G						—	—	CP1_255B						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP1_000A to CP1_255A	—	R/W	Available	Color Palette 1_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHAR are B'10, the value is the alpha ratio, which is the α blending ratio. The value is retained during a reset.
23 to 18	CP1_000R to CP1_255R	—	R/W	Available	Color Palette 1_000 to 255 Red Red-color data of color palette 1. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP1_000G to CP1_255G	—	R/W	Available	Color Palette 1_000 to 255 Green Green-color data of color palette 1. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP1_000B to CP1_255B	—	R/W	Available	Color Palette 1_000 to 255 Blue Blue-color data of color palette 1. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: CP1_000R to CP1_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.

After the CP1CE bit in CPCR has been set to 1, settings for CP1_000R to CP1_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP1CE bit has been set to 1. The color palette is accessible in longword units.

20.3.6.2 Color Palette 2 (000 to 255) Register (CP2_000R to CP2_255R)

Address: DU0: H'FEB02000 to H'FEB023FC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CP2_000A								CP2_000R						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP2_000G						—	—	CP2_000B						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

..

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CP2_255A								CP2_255R						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R

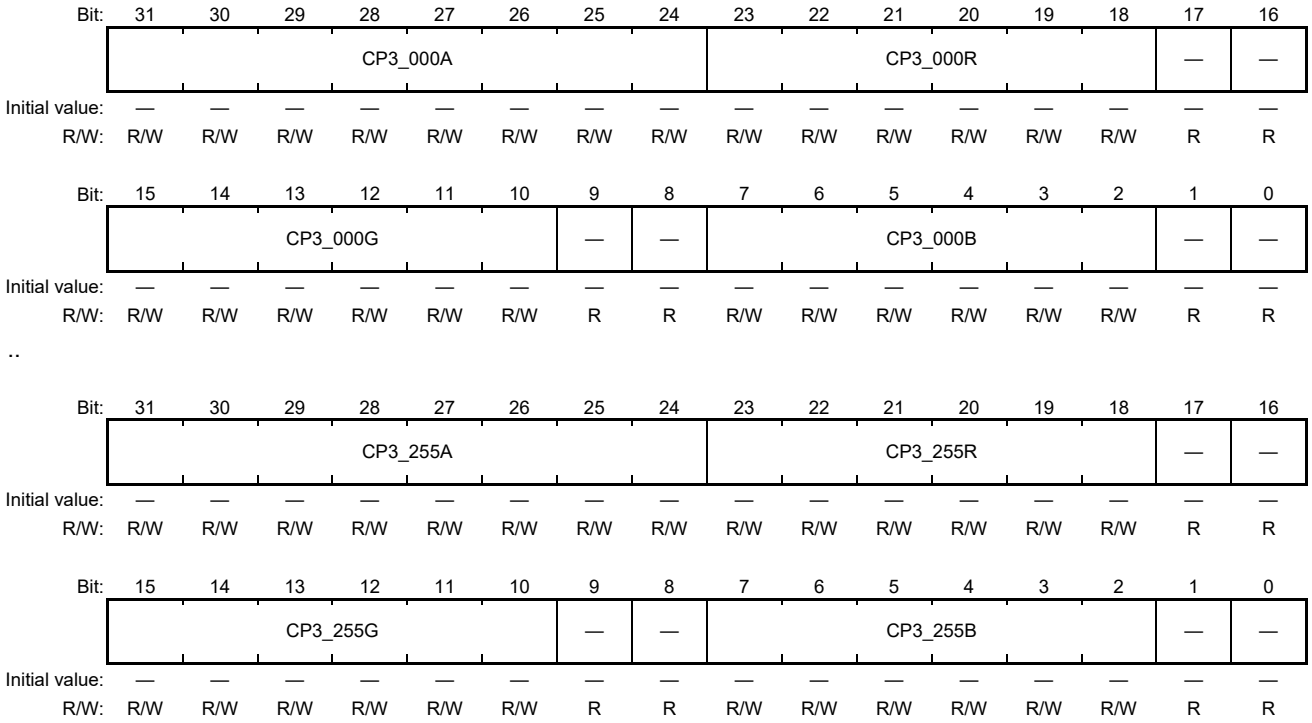
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CP2_255G						—	—	CP2_255B						—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP2_000A to CP2_255A	—	R/W	Available	Color Palette 2_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHAR are B'10, the value is the alpha ratio, which is the α blending ratio. The value is retained during a reset.
23 to 18	CP2_000R to CP2_255R	—	R/W	Available	Color Palette 2_000 to 255 Red Red-color data of color palette 2. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP2_000G to CP2_255G	—	R/W	Available	Color Palette 2_000 to 255 Green Green-color data of color palette 2. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP2_000B to CP2_255B	—	R/W	Available	Color Palette 2_000 to 255 Blue Blue-color data of color palette 2. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: CP2_000R to CP2_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.
After the CP2CE bit in CPCR has been set to 1, settings for CP2_000R to CP2_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP2CE bit has been set to 1. The color palette is accessible in longword units.

20.3.6.3 Color Palette 3 (000 to 255) Register (CP3_000R to CP3_255R)

Address: DU0: H'FEB03000 to H'FEB033FC

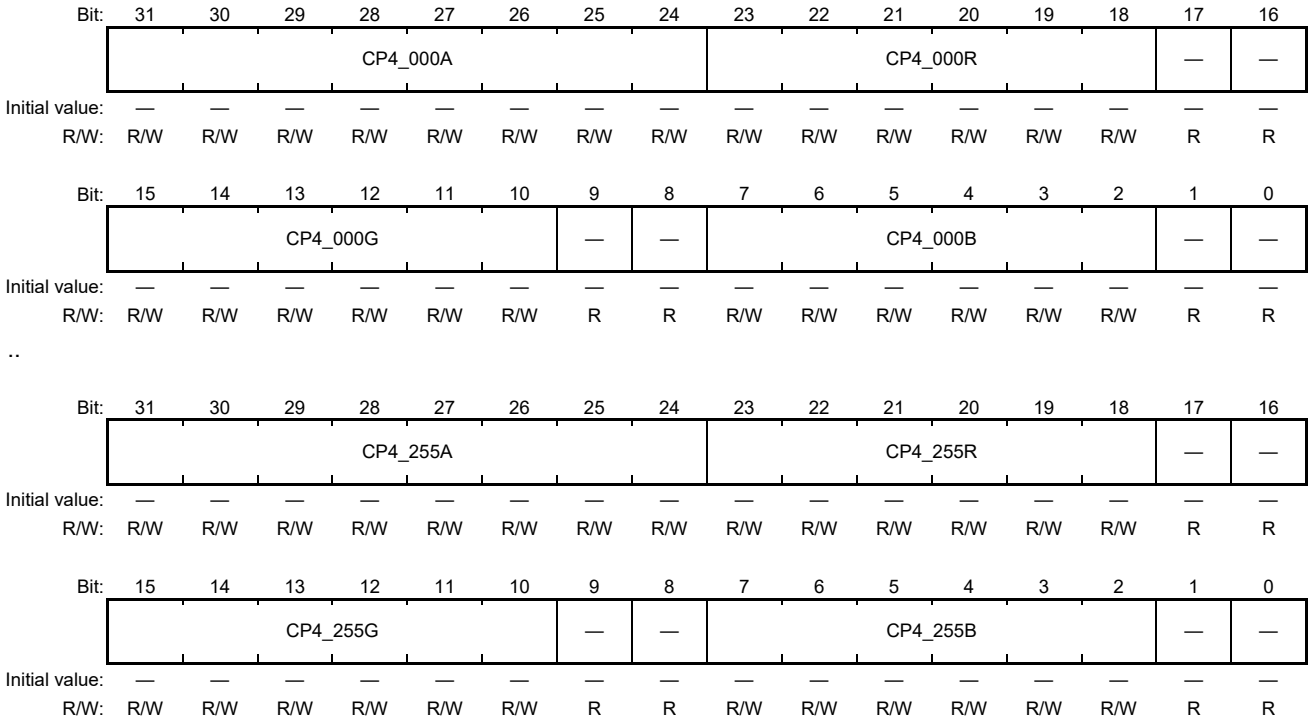


Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP3_000A to CP3_255A	—	R/W	Available	Color Palette 3_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHAR are B'10, the value is the alpha ratio, which is the α blending ratio. The value is retained during a reset.
23 to 18	CP3_000R to CP3_255R	—	R/W	Available	Color Palette 3_000 to 255 Red Red-color data of color palette 3. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP3_000G to CP3_255G	—	R/W	Available	Color Palette 3_000 to 255 Green Green-color data of color palette 3. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP3_000B to CP3_255B	—	R/W	Available	Color Palette 3_000 to 255 Blue Blue-color data of color palette 3. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: CP3_000R to CP3_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.
After the CP3CE bit in CPCR has been set to 1, settings for CP3_000R to CP3_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP3CE bit has been set to 1. The color palette is accessible in longword units.

20.3.6.4 Color Palette 4 (000 to 255) Register (CP4_000R to CP4_255R)

Address: DU0: H'FEB04000 to H'FEB043FC



Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	CP4_000A to CP4_255A	—	R/W	Available	Color Palette 4_000 to 255 Blending Ratio When the PnBRSL bits in PnALPHAR are B'10, the value is the alpha ratio, which is the α blending ratio. The value is retained during a reset.
23 to 18	CP4_000R to CP4_255R	—	R/W	Available	Color Palette 4_000 to 255 Red Red-color data of color palette 4. The value is retained during a reset.
17, 16	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
15 to 10	CP4_000G to CP4_255G	—	R/W	Available	Color Palette 4_000 to 255 Green Green-color data of color palette 4. The value is retained during a reset.
9, 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 2	CP4_000B to CP4_255B	—	R/W	Available	Color Palette 4_000 to 255 Blue Blue-color data of color palette 4. The value is retained during a reset.
1, 0	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Note: CP4_000R to CP4_255R form a group of 256 registers in which six bits are set for each of the R, G, and B components of a color, setting up the color palette of 256 colors from among the 262 thousand colors for display. The values are valid for 8-bit/pixel data display.
After the CP4CE bit in CPCR has been set to 1, settings for CP4_000R to CP4_255R become effective on the next falling edge of VSYNC (timing of an internal update) or when the display is reset. When you update the color palette, rewrite the entire palette. Reading of the color palette by the CPU must proceed before the CP4CE bit has been set to 1. The color palette is accessible in longword units.

20.3.7 External Synchronization Control Registers

The three sets of external synchronization control registers are for the respective channels and have the same functions; they are described as one here.

In section 20.3.7, n = 0 and 1 for this product.

20.3.7.1 External Synchronization Control Register n (ESCRn)

Address: DU0: H'FEB10000, DU1: H'FEB31000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	DCKOINV	DCKOSEL	—	—	—	DCLKSEL	—	—	—	DCLKDIS
Initial value:	—	—	—	—	—	—	0	0	—	—	—	0	—	—	—	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SYNCSEL		—	—	FRQSEL					
Initial value:	—	—	—	—	—	—	0	0	—	—	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Note: * Value of reserved bit (bit name: —) is undefined. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 26	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
25	DCKOINV	0	R/W	Not available	DCLKOUT Invert To enable this bit, set the DEFE bit in the display unit extensional function control register 0 (DEFR0) to 1. In the initial state, this bit is fixed to 0. 0: DCLKOUT is output in normal phase. 1: DCLKOUT is output in counter phase.
24	DCKOSEL	0	R/W	Not available	Output Dot Clock Select (DCLKOUT Select) To enable this bit, set DEFE to 1 in the display unit extensional function control register 0 (DEFR0). In the initial state, this bit is fixed at 0. Set this bit to 1 to specify display output in YC data format. 0: The DCLKOUT division ratio is determined by bits 5 to 0 in this register. 1: DCLKIN is used as DCLKOUT, regardless of the division ratio.
23 to 21	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
20	DCLKSEL	0	R/W	Not available	DCLKIN Select 0: The input dot clock source is the DCLKIN pin 1: The input dot clock source is the ZXϕ clock. If this setting is made, ensure that the frequency of the input dot clock is divided by two or a greater value (so that the result of dividing the frequency is more than or equal to half the ZXϕ frequency).
19 to 17	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
16	DCLKDIS	0	R/W	Not available	DCLKOUT Disable 0: DCLKOUT is output. 1: DCLKOUT is not output. DCLKOUT is fixed to low level.
15 to 10	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
9, 8	SYNCSEL	00	R/W	Not available	SYNC Select 00: Phases are not synchronized 01: Phases are not synchronized 10: Phases are synchronized by using the EXVSYNC signal 11: Phases are synchronized by using the EXHSYNC signal
7, 6	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
5 to 0	FRQSEL	000000	R/W	Not available	Frequency Select To enable bit 5, the DEFE bit in DEFR0 must be set to 1. In the initial state, bit 5 is fixed to 0. If frequency division is by an odd number, the duty cycle of the frequency divided dot clock will be below 50%. 000000: Frequency division of the input dot clock (clock for division) is not performed. 000001: Division by 2 of the input dot clock (clock for division) 000010: Division by 3 of the input dot clock (clock for division) 000011: Division by 4 of the input dot clock (clock for division) 000100: Division by 5 of the input dot clock (clock for division) 000101: Division by 6 of the input dot clock (clock for division) 000110: Division by 7 of the input dot clock (clock for division) 000111: Division by 8 of the input dot clock (clock for division) 001000: Division by 9 of the input dot clock (clock for division) 001001: Division by 10 of the input dot clock (clock for division) 001010: Division by 11 of the input dot clock (clock for division) 001011: Division by 12 of the input dot clock (clock for division) 001100: Division by 13 of the input dot clock (clock for division) 001101: Division by 14 of the input dot clock (clock for division) 001110: Division by 15 of the input dot clock (clock for division) 001111: Division by 16 of the input dot clock (clock for division) 010000: Division by 17 of the input dot clock (clock for division) 010001: Division by 18 of the input dot clock (clock for division) 010010: Division by 19 of the input dot clock (clock for division) 010011: Division by 20 of the input dot clock (clock for division) 010100: Division by 21 of the input dot clock (clock for division) 010101: Division by 22 of the input dot clock (clock for division) 010110: Division by 23 of the input dot clock (clock for division) 010111: Division by 24 of the input dot clock (clock for division) 011000: Division by 25 of the input dot clock (clock for division) 011001: Division by 26 of the input dot clock (clock for division) 011010: Division by 27 of the input dot clock (clock for division) 011011: Division by 28 of the input dot clock (clock for division) 011100: Division by 29 of the input dot clock (clock for division)

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
5 to 0	FRQSEL	000000	R/W	Not available	011101: Division by 30 of the input dot clock (clock for division) 011110: Division by 31 of the input dot clock (clock for division) 011111: Division by 32 of the input dot clock (clock for division) 100000: Division by 33 of the input dot clock (clock for division) 100001: Division by 34 of the input dot clock (clock for division) 100010: Division by 35 of the input dot clock (clock for division) 100011: Division by 36 of the input dot clock (clock for division) 100100: Division by 37 of the input dot clock (clock for division) 100101: Division by 38 of the input dot clock (clock for division) 100110: Division by 39 of the input dot clock (clock for division) 100111: Division by 40 of the input dot clock (clock for division) 101000: Division by 41 of the input dot clock (clock for division) 101001: Division by 42 of the input dot clock (clock for division) 101010: Division by 43 of the input dot clock (clock for division) 101011: Division by 44 of the input dot clock (clock for division) 101100: Division by 45 of the input dot clock (clock for division) 101101: Division by 46 of the input dot clock (clock for division) 101110: Division by 47 of the input dot clock (clock for division) 101111: Division by 48 of the input dot clock (clock for division) 110000: Division by 49 of the input dot clock (clock for division) 110001: Division by 50 of the input dot clock (clock for division) 110010: Division by 51 of the input dot clock (clock for division) 110011: Division by 52 of the input dot clock (clock for division) 110100: Division by 53 of the input dot clock (clock for division) 110101: Division by 54 of the input dot clock (clock for division) 110110: Division by 55 of the input dot clock (clock for division) 110111: Division by 56 of the input dot clock (clock for division) 111000: Division by 57 of the input dot clock (clock for division) 111001: Division by 58 of the input dot clock (clock for division) 111010: Division by 59 of the input dot clock (clock for division) 111011: Division by 60 of the input dot clock (clock for division) 111100: Division by 61 of the input dot clock (clock for division) 111101: Division by 62 of the input dot clock (clock for division) 111110: Division by 63 of the input dot clock (clock for division) 111111: Division by 64 of the input dot clock (clock for division)

20.3.7.2 Output Signal Timing Adjustment Register n (OTARn)

Address: DU0: H'FEB10004, DU1: H'FEB31004

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	DEA			—	CLAMPA			—	DRGBA			—	—	—	—
Initial value:	—	0	0	0	—	0	0	0	—	0	0	0	—	—	—	—
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	CDEA			—	DISPA			—	SYNCA		
Initial value:	—	—	—	—	—	0	0	0	—	0	0	0	—	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
30 to 28	DEA	000	R/W	DRES	DE Output Timing Adjustment 000: Adjustment of output timing is not performed. The DE signal is output on the rising edge of the dot clock, with the reference timing. 001: The DE signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The DE signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The DE signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The DE signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The DE signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The DE signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The DE signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.
27	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
26 to 24	CLAMPA	000	R/W	DRES	CLAMP Output Timing Adjustment 000: Adjustment of output timing is not performed. The CLAMP signal is output on the rising edge of the dot clock, with the reference timing. 001: The CLAMP signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The CLAMP signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The CLAMP signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The CLAMP signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The CLAMP signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The CLAMP signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The CLAMP signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.
23	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
22 to 20	DRGBA	000	R/W	DRES	Digital RGB Output Timing Adjustment 000: Adjustment of output timing is not performed. The digital RGB signal is output on the rising edge of the dot clock, with the reference timing. 001: The digital RGB signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The digital RGB signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The digital RGB signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The digital RGB signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The digital RGB signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The digital RGB signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The digital RGB signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing. If you intend to use the output dot clock to control the timing of the switching of data for display, do not select the falling edge (i.e. do not set bit 22 to 1). The value of bits 22 to 20 of output signal timing adjustment register 0 (OTAR0) must be the same as that of bits 22 to 20 in output signal timing adjustment register 1 (OTAR1).
19 to 11	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
10 to 8	CDEA	000	R/W	DRES	CDE Output Timing Adjustment 000: Adjustment of output timing is not performed. The CDE signal is output on the rising edge of the dot clock, with the reference timing. 001: The CDE signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The CDE signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The CDE signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The CDE signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The CDE signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The CDE signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The CDE signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.
7	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
6 to 4	DISPA	000	R/W	DRES	DISP Output Timing Adjustment 000: Adjustment of output timing is not performed. The DISP signal is output on the rising edge of the dot clock, with the reference timing. 001: The DISP signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The DISP signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The DISP signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The DISP signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The DISP signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The DISP signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The DISP signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing.
3	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
2 to 0	SYNCA	000	R/W	DRES	SYNC* Output Timing Adjustment 000: Adjustment of output timing is not performed. The SYNC* signal is output on the rising edge of the dot clock, with the reference timing. 001: The SYNC* signal is output on the rising edge, delayed one dot clock cycle relative to the reference timing. 010: The SYNC* signal is output on the rising edge, delayed two dot clock cycles relative to the reference timing. 011: The SYNC* signal is output on the rising edge, delayed three dot clock cycles relative to the reference timing. 100: The SYNC* signal is output on the falling edge, preceding the reference timing by 1/2 dot clock cycle. 101: The SYNC* signal is output on the falling edge, delayed 1/2 dot clock cycle relative to the reference timing. 110: The SYNC* signal is output on the falling edge, delayed (1+1/2) dot clock cycles relative to the reference timing. 111: The SYNC* signal is output on the falling edge, delayed (2+1/2) dot clock cycles relative to the reference timing. Note: * HSYNC, VSYNC, CSYNC, and ODDF signals

Note: When signals are to be output on the falling edge, the electrical characteristics do not apply.

20.3.8 Dual Display Output Control Registers

20.3.8.1 Display Unit Output Route Control Register (DORCR)

Address: DU0: H'FEB11000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PG1T	—	DK1S	—	—	PG1D		—	—	DR0D	—	—	—	PG0D	
Initial value:	—	1	—	1	—	—	0	1	—	—	0	—	—	—	0	0
R/W:	R	R/W	R	R/W	R	R	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DPRS
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
30	PG1T	1	R/W	DRES	Pin Generate 1 Timing Select Selects the source of timing for pin controller 1. 0: Display-timing generator 0 1: Display-timing generator 1
29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28	DK1S	1	R/W	DRES	Dot Clock Select 1 0: Dot-clock generator 0 supplies the dot clock for display-timing generator 1 and pin controller 1. 1: Dot-clock generator 1 supplies the dot clock for display-timing generator 1 and pin controller 1. When the TVM1 bits in the display unit system control register 1 (DSYSR1) are set to TV synchronized mode, do not set this bit to 0.
27, 26	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
25, 24	PG1D	01	R/W	DRES	Pin Generate 1 Input Data Select Selects the source of input data for pin controller 1. 00: Data from superposition processor 0 are input to pin controller 1. For the timing of superposition processor 1, refer to section 20.4.19 (4), Combinations of Blocks for Dual Display Output. 01: Data from superposition processor 1 are input to pin controller 1. For the timing of superposition processor 1, refer to section 20.4.19 (4), Combinations of Blocks for Dual Display Output. 10: Input to pin controller 1 is fixed to 0. The value of the CDE pin is fixed to 0. 11: The value of DOOR1 is input to pin controller 1. The value of the CDE pin is fixed to 0. The combination of the DRES and DEN bits of DSYSR0 determines the data to be superposed. DRES/DEN = 00: The value of DOOR1 DRES/DEN = 01: The data in unified memory DRES/DEN = 10: 0 DRES/DEN = 11: Setting prohibited (data: 0)
23, 22	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
21	DR0D	0	R/W	DRES	Display Output Route 0 Data Select 0: Data from pin controller 0 are output from the DU0 pins. 1: On the DU0 pins, data from pin controller 0 are output on rising edges of the output dot clock and data from pin controller 1 are output on falling edges of the output dot clock. If this setting is made, the frequency of the output dot clock has to be at least half of the frequency of the input dot clock.
20 to 18	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
17, 16	PG0D	00	R/W	DRES	Pin Generate 0 Input Data Select Selects the source of input data for pin controller 0. 00: Data from superposition processor 0 are input to pin controller 0. For the timing of superposition processor 0, refer to section 20.4.19 (4), Combinations of Blocks for Dual Display Output. 01: Data from superposition processor 1 are input to pin controller 0. For the timing of superposition processor 1, refer to section 20.4.19 (4), Combinations of Blocks for Dual Display Output. 10: Input to pin controller 0 is fixed to 0. The value of the CDE pin is fixed to 0. 11: The value of DOOR0 is input to pin controller 0. The value of the CDE pin is fixed to 0. The combination of the DRES and DEN bits of DSYSR0 determines the data to be superposed. DRES/DEN = 00: The value of DOOR0 DRES/DEN = 01: The data in unified memory DRES/DEN = 10: 0 DRES/DEN = 11: Setting prohibited (data: 0)

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
15 to 1	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
0	DPRS	0	R/W	DRES	Display Priority Register Select 0: The order of priority for the planes is set in DPPR. Superposition processor 0 can be used to superpose planes 1 to 8. Superposition processor 1 is not available. 1: The order of priority for the planes is set in DS0PR or DS1PR. Superposition processors 0 and 1 can be used to superpose planes 1 to 8.

20.3.8.2 Display Unit Plane Timing Select Register (DPTSR)

Address: DU0: H'FEB11004

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	P8DK	P7DK	P6DK	P5DK	P4DK	P3DK	P2DK	P1DK
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	P8TS	P7TS	P6TS	P5TS	P4TS	P3TS	P2TS	P1TS
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23	P8DK	0	R/W	DRES	Plane 8 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
22	P7DK	0	R/W	DRES	Plane 7 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
21	P6DK	0	R/W	DRES	Plane 6 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
20	P5DK	0	R/W	DRES	Plane 5 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
19	P4DK	0	R/W	DRES	Plane 4 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
18	P3DK	0	R/W	DRES	Plane 3 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
17	P2DK	0	R/W	DRES	Plane 2 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
16	P1DK	0	R/W	DRES	Plane 1 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7	P8TS	0	R/W	DRES	Plane 8 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
6	P7TS	0	R/W	DRES	Plane 7 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
5	P6TS	0	R/W	DRES	Plane 6 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
4	P5TS	0	R/W	DRES	Plane 5 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
3	P4TS	0	R/W	DRES	Plane 4 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
2	P3TS	0	R/W	DRES	Plane 3 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
1	P2TS	0	R/W	DRES	Plane 2 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
0	P1TS	0	R/W	DRES	Plane 1 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1

20.3.8.3 Display Unit Alpha-ratio Plane Timing Select Register (DAPTSR)

Address: DU0: H'FEB11008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AP2DK	AP1DK
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	AP2TS	AP1TS
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Note: * Value of reserved bit (bit name: —) is undefined. For details of bit description, refer to following table.

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 18	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
17	AP2DK	0	R/W	DRES	α Plane 2 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
16	AP1DK	0	R/W	DRES	α Plane 1 Dot Clock Select 0: Dot-clock generator 0 1: Dot-clock generator 1
15 to 2	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
1	AP2TS	0	R/W	DRES	α Plane 2 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1
0	AP1TS	0	R/W	DRES	α Plane 1 Timing Select 0: Display-timing generator 0 1: Display-timing generator 1

20.3.8.4 Display Superimpose 0 Priority Register (DS0PR)

Address: DU0: H'FEB11020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	S0S8				S0S7				S0S6				S01S5			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S0S4				S0S3				S0S2				S0S1			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- The setting of this register is valid when the DPRS bit in the display unit output route control register (DORCR) is 1.
- After setting a desired value in a register listed in section 20.3.4, Display Plane Registers (Alpha-ratio Plane Registers), set DS0PR to the value indicating the plane number (0001 to 1000).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	S0S8	0000	R/W	Available	Display Superimposition 0 Priority 8 Select 0000: Priority level 8 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 8 in display generation by superposition processor 0. 0010: Plane 2 has priority level 8 in display generation by superposition processor 0. 0011: Plane 3 has priority level 8 in display generation by superposition processor 0. 0100: Plane 4 has priority level 8 in display generation by superposition processor 0. 0101: Plane 5 has priority level 8 in display generation by superposition processor 0. 0110: Plane 6 has priority level 8 in display generation by superposition processor 0. 0111: Plane 7 has priority level 8 in display generation by superposition processor 0. 1000: Plane 8 has priority level 8 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
27 to 24	S0S7	0000	R/W	Available	Display Superimposition 0 Priority 7 Select 0000: Priority level 7 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 7 in display generation by superposition processor 0. 0010: Plane 2 has priority level 7 in display generation by superposition processor 0. 0011: Plane 3 has priority level 7 in display generation by superposition processor 0. 0100: Plane 4 has priority level 7 in display generation by superposition processor 0. 0101: Plane 5 has priority level 7 in display generation by superposition processor 0. 0110: Plane 6 has priority level 7 in display generation by superposition processor 0. 0111: Plane 7 has priority level 7 in display generation by superposition processor 0. 1000: Plane 8 has priority level 7 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited
23 to 20	S0S6	0000	R/W	Available	Display Superimposition 0 Priority 6 Select 0000: Priority level 6 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 6 in display generation by superposition processor 0. 0010: Plane 2 has priority level 6 in display generation by superposition processor 0. 0011: Plane 3 has priority level 6 in display generation by superposition processor 0. 0100: Plane 4 has priority level 6 in display generation by superposition processor 0. 0101: Plane 5 has priority level 6 in display generation by superposition processor 0. 0110: Plane 6 has priority level 6 in display generation by superposition processor 0. 0111: Plane 7 has priority level 6 in display generation by superposition processor 0. 1000: Plane 8 has priority level 6 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
19 to 16	S0S5	0000	R/W	Available	Display Superimposition 0 Priority 5 Select 0000: Priority level 5 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 5 in display generation by superposition processor 0. 0010: Plane 2 has priority level 5 in display generation by superposition processor 0. 0011: Plane 3 has priority level 5 in display generation by superposition processor 0. 0100: Plane 4 has priority level 5 in display generation by superposition processor 0. 0101: Plane 5 has priority level 5 in display generation by superposition processor 0. 0110: Plane 6 has priority level 5 in display generation by superposition processor 0. 0111: Plane 7 has priority level 5 in display generation by superposition processor 0. 1000: Plane 8 has priority level 5 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited
15 to 12	S0S4	0000	R/W	Available	Display Superimposition 0 Priority 4 Select 0000: Priority level 4 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 4 in display generation by superposition processor 0. 0010: Plane 2 has priority level 4 in display generation by superposition processor 0. 0011: Plane 3 has priority level 4 in display generation by superposition processor 0. 0100: Plane 4 has priority level 4 in display generation by superposition processor 0. 0101: Plane 5 has priority level 4 in display generation by superposition processor 0. 0110: Plane 6 has priority level 4 in display generation by superposition processor 0. 0111: Plane 7 has priority level 4 in display generation by superposition processor 0. 1000: Plane 8 has priority level 4 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11 to 8	S0S3	0000	R/W	Available	Display Superimposition 0 Priority 3 Select 0000: Priority level 3 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 3 in display generation by superposition processor 0. 0010: Plane 2 has priority level 3 in display generation by superposition processor 0. 0011: Plane 3 has priority level 3 in display generation by superposition processor 0. 0100: Plane 4 has priority level 3 in display generation by superposition processor 0. 0101: Plane 5 has priority level 3 in display generation by superposition processor 0. 0110: Plane 6 has priority level 3 in display generation by superposition processor 0. 0111: Plane 7 has priority level 3 in display generation by superposition processor 0. 1000: Plane 8 has priority level 3 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited
7 to 4	S0S2	0000	R/W	Available	Display Superimposition 0 Priority 2 Select 0000: Priority level 2 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 2 in display generation by superposition processor 0. 0010: Plane 2 has priority level 2 in display generation by superposition processor 0. 0011: Plane 3 has priority level 2 in display generation by superposition processor 0. 0100: Plane 4 has priority level 2 in display generation by superposition processor 0. 0101: Plane 5 has priority level 2 in display generation by superposition processor 0. 0110: Plane 6 has priority level 2 in display generation by superposition processor 0. 0111: Plane 7 has priority level 2 in display generation by superposition processor 0. 1000: Plane 8 has priority level 2 in display generation by superposition processor 0. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
3 to 0	S0S1	0000	R/W	Available	Display Superimposition 0 Priority 1 Select 0000: Priority level 1 is not used in display generation by superposition processor 0. 0001: Plane 1 has priority level 1 in display generation by superposition processor 0. 0010: Plane 2 has priority level 1 in display generation by superposition processor 0. 0011: Plane 3 has priority level 1 in display generation by superposition processor 0. 0100: Plane 4 has priority level 1 in display generation by superposition processor 0. 0101: Plane 5 has priority level 1 in display generation by superposition processor 0. 0110: Plane 6 has priority level 1 in display generation by superposition processor 0. 0111: Plane 7 has priority level 1 in display generation by superposition processor 0. 1000: Plane 8 has priority level 1 in display generation by superposition processor 0 1001: Setting prohibited Others: Setting prohibited

20.3.8.5 Display Superimpose 1 Priority Register (DS1PR)

Address: DU1: H'FEB11024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	S1S8				S1S7				S1S6				S1S5			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	S1S4				S1S3				S1S2				S1S1			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- The setting of this register is valid when the DPRS bit in the display unit output route control register (DORCR) is 1.
- After setting a desired value in a register listed in section 20.3.54, Display Plane Registers (Alpha-ratio Plane Registers), set DS1PR to the value indicating the plane number (0001 to 1000).

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	S1S8	0000	R/W	Available	Display Superimposition 1 Priority 8 Select 0000: Priority level 8 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 8 in display generation by superposition processor 1. 0010: Plane 2 has priority level 8 in display generation by superposition processor 1. 0011: Plane 3 has priority level 8 in display generation by superposition processor 1. 0100: Plane 4 has priority level 8 in display generation by superposition processor 1. 0101: Plane 5 has priority level 8 in display generation by superposition processor 1. 0110: Plane 6 has priority level 8 in display generation by superposition processor 1. 0111: Plane 7 has priority level 8 in display generation by superposition processor 1. 1000: Plane 8 has priority level 8 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
27 to 24	S1S7	0000	R/W	Available	Display Superimposition 1 Priority 7 Select 0000: Priority level 7 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 7 in display generation by superposition processor 1. 0010: Plane 2 has priority level 7 in display generation by superposition processor 1. 0011: Plane 3 has priority level 7 in display generation by superposition processor 1. 0100: Plane 4 has priority level 7 in display generation by superposition processor 1. 0101: Plane 5 has priority level 7 in display generation by superposition processor 1. 0110: Plane 6 has priority level 7 in display generation by superposition processor 1. 0111: Plane 7 has priority level 7 in display generation by superposition processor 1. 1000: Plane 8 has priority level 7 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited
23 to 20	S1S6	0000	R/W	Available	Display Superimposition 1 Priority 6 Select 0000: Priority level 6 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 6 in display generation by superposition processor 1. 0010: Plane 2 has priority level 6 in display generation by superposition processor 1. 0011: Plane 3 has priority level 6 in display generation by superposition processor 1. 0100: Plane 4 has priority level 6 in display generation by superposition processor 1. 0101: Plane 5 has priority level 6 in display generation by superposition processor 1. 0110: Plane 6 has priority level 6 in display generation by superposition processor 1. 0111: Plane 7 has priority level 6 in display generation by superposition processor 1. 1000: Plane 8 has priority level 6 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
19 to 16	S1S5	0000	R/W	Available	Display Superimposition 1 Priority 5 Select 0000: Priority level 5 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 5 in display generation by superposition processor 1. 0010: Plane 2 has priority level 5 in display generation by superposition processor 1. 0011: Plane 3 has priority level 5 in display generation by superposition processor 1. 0100: Plane 4 has priority level 5 in display generation by superposition processor 1. 0101: Plane 5 has priority level 5 in display generation by superposition processor 1. 0110: Plane 6 has priority level 5 in display generation by superposition processor 1. 0111: Plane 7 has priority level 5 in display generation by superposition processor 1. 1000: Plane 8 has priority level 5 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited
15 to 12	S1S4	0000	R/W	Available	Display Superimposition 1 Priority 4 Select 0000: Priority level 4 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 4 in display generation by superposition processor 1. 0010: Plane 2 has priority level 4 in display generation by superposition processor 1. 0011: Plane 3 has priority level 4 in display generation by superposition processor 1. 0100: Plane 4 has priority level 4 in display generation by superposition processor 1. 0101: Plane 5 has priority level 4 in display generation by superposition processor 1. 0110: Plane 6 has priority level 4 in display generation by superposition processor 1. 0111: Plane 7 has priority level 4 in display generation by superposition processor 1. 1000: Plane 8 has priority level 4 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
11 to 8	S1S3	0000	R/W	Available	Display Superimposition 1 Priority 3 Select 0000: Priority level 3 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 3 in display generation by superposition processor 1. 0010: Plane 2 has priority level 3 in display generation by superposition processor 1. 0011: Plane 3 has priority level 3 in display generation by superposition processor 1. 0100: Plane 4 has priority level 3 in display generation by superposition processor 1. 0101: Plane 5 has priority level 3 in display generation by superposition processor 1. 0110: Plane 6 has priority level 3 in display generation by superposition processor 1. 0111: Plane 7 has priority level 3 in display generation by superposition processor 1. 1000: Plane 8 has priority level 3 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited
7 to 4	S1S2	0000	R/W	Available	Display Superimposition 1 Priority 2 Select 0000: Priority level 2 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 2 in display generation by superposition processor 1. 0010: Plane 2 has priority level 2 in display generation by superposition processor 1. 0011: Plane 3 has priority level 2 in display generation by superposition processor 1. 0100: Plane 4 has priority level 2 in display generation by superposition processor 1. 0101: Plane 5 has priority level 2 in display generation by superposition processor 1. 0110: Plane 6 has priority level 2 in display generation by superposition processor 1. 0111: Plane 7 has priority level 2 in display generation by superposition processor 1. 1000: Plane 8 has priority level 2 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
3 to 0	S1S1	0000	R/W	Available	Display Superimposition 1 Priority 1 Select 0000: Priority level 1 is not used in display generation by superposition processor 1. 0001: Plane 1 has priority level 1 in display generation by superposition processor 1. 0010: Plane 2 has priority level 1 in display generation by superposition processor 1. 0011: Plane 3 has priority level 1 in display generation by superposition processor 1. 0100: Plane 4 has priority level 1 in display generation by superposition processor 1. 0101: Plane 5 has priority level 1 in display generation by superposition processor 1. 0110: Plane 6 has priority level 1 in display generation by superposition processor 1. 0111: Plane 7 has priority level 1 in display generation by superposition processor 1. 1000: Plane 8 has priority level 1 in display generation by superposition processor 1. 1001: Setting prohibited Others: Setting prohibited

20.3.9 YC-RGB Conversion Coefficient Registers

Registers at addresses H'FEB11080 to H'FEB1109C is for the YC→RGB conversion circuit located in the initial stage of the superposition processor in Figure 20.1.

20.3.9.1 Y Normalization Coefficient Register (YNCR)

Address: DU0: H'FEB11080

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	YNC1											
Initial value:	—	—	—	—	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	YNC0											
Initial value:	—	—	—	—	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	YNC1	H'800	R/W	Available	Y Normalization Coefficient 1 This coefficient is for normalization of Y values in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	YNC0	H'800	R/W	Available	Y Normalization Coefficient 0 This coefficient is for normalization of Y values in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.

20.3.9.2 Y Normalization Offset Register (YNOR)

Address: DU0: H'FEB11084

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	YNO1							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	YNO0							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	YNO1	H'00	R/W	Available	Y Normalization Offset 1 This offset is to be subtracted from Y values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The offset is an unsigned 8-bit integer. Its default value is 0.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	YNO0	H'00	R/W	Available	Y Normalization Offset 0 This offset is to be subtracted from Y values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The offset is an unsigned 8-bit integer. Its default value is 0.

20.3.9.3 Cr Normalization Offset Register (CRNOR)

Address: DU0: H'FEB11088

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CRNO1							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CRNO0							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	CRNO1	H'80	R/W	Available	Cr Normalization Offset 1 This offset is to be subtracted from Cr values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The offset is an unsigned 8-bit integer. Its default value is 128.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CRNO0	H'80	R/W	Available	Cr Normalization Offset 0 This offset is to be subtracted from Cr values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The offset is an unsigned 8-bit integer. Its default value is 128.

20.3.9.4 Cb Normalization Offset Register (CBNOR)

Address: DU0: H'FEB1108C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CBNO1							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CBNO0							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	CBNO1	H'80	R/W	Available	Cb Normalization Offset 1 This offset is to be subtracted from Cb values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The offset is an unsigned 8-bit integer. Its default value is 128.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CBNO0	H'80	R/W	Available	Cb Normalization Offset 0 This offset is to be subtracted from Cb values before they are normalized in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The offset is an unsigned 8-bit integer. Its default value is 128.

20.3.9.5 Red Cr Coefficient Register (RCRCR)

Address: DU0: H'FEB11090

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	RCRC1											
Initial value:	—	—	—	—	1	0	1	0	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	RCRC0											
Initial value:	—	—	—	—	1	0	1	0	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	RCRC1	H'AF0	R/W	Available	Red Cr Coefficient 1 Cr is multiplied by this coefficient to create the red component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.37.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	RCRC0	H'AF0	R/W	Available	Red Cr Coefficient 0 Cr is multiplied by this coefficient to create the red component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.37.

20.3.9.6 Green Cr Coefficient Register (GCRCR)

Address: DU0: H'FEB11094

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	GCRC1											
Initial value:	—	—	—	—	0	1	0	1	1	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	GCRC0											
Initial value:	—	—	—	—	0	1	0	1	1	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	GCRC1	H'590	R/W	Available	Green Cr Coefficient 1 Cr is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.698.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	GCRC0	H'590	R/W	Available	Green Cr Coefficient 0 Cr is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.698.

20.3.9.7 Green Cb Coefficient Register (GCBCR)

Address: DU0: H'FEB11098

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	GCBC1											
Initial value:	—	—	—	—	0	0	1	0	1	0	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	GCBC0											
Initial value:	—	—	—	—	0	0	1	0	1	0	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	GCBC1	H'2B0	R/W	Available	Green Cb Coefficient 1 Cb is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.336.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	GCBC0	H'2B0	R/W	Available	Green Cb Coefficient 0 Cb is multiplied by this coefficient to create the green component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 0.336.

20.3.9.8 Blue Cb Coefficient Register (BCBCR)

Address: DU0: H'FEB1109C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BCBC1											
Initial value:	—	—	—	—	1	1	0	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BCBC0											
Initial value:	—	—	—	—	1	1	0	1	1	1	1	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 28	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
27 to 16	BCBC1	H'DE0	R/W	Available	Blue Cb Coefficient 1 Cb is multiplied by this coefficient to create the blue component in YC-RGB conversion by the YC-RGB conversion generation by superposition processor 1. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.73.
15 to 12	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
11 to 0	BCBC0	H'DE0	R/W	Available	Blue Cb Coefficient 0 Cb is multiplied by this coefficient to create the blue component in YC-RGB conversion by the YC-RGB conversion generation by superposition processors 0. The coefficient is a fixed-point 12-bit value. The 11th bit represents the integer one or zero and the 10th to 0th bits represent the value below the fixed point. The default value is 1.73.

20.3.10 RGB-YC Conversion Coefficient Registers

20.3.10.1 Y Calculation R Coefficient Register (YCLRP)

Address: DU0: H'FEB14000

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	YCLRP1												
Initial value:	—	—	—	0	0	0	1	0	0	1	1	0	0	1	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLRP0												
Initial value:	—	—	—	0	0	0	1	0	0	1	1	0	0	1	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	YCLRP1	H'0264	R/W	Available	Y Calculation R Coefficient 1 This coefficient is for R to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'264. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	YCLRP0	H'0264	R/W	Available	Y Calculation R Coefficient 0 This coefficient is for R to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'264. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.2 Y Calculation G Coefficient Register (YCLGP)

Address: DU0: H'FEB14004

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	YCLGP1												
Initial value:	—	—	—	0	0	1	0	0	1	0	1	1	0	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLGP0												
Initial value:	—	—	—	0	0	1	0	0	1	0	1	1	0	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	YCLGP1	H'04B2	R/W	Available	Y Calculation G Coefficient 1 This coefficient is for G to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'4B2. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	YCLGP0	H'04B2	R/W	Available	Y Calculation G Coefficient 0 This coefficient is for G to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'4B2. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.3 Y Calculation B Coefficient Register (YCLBP)

Address: DU0: H'FEB14008

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	YCLBP1												
Initial value:	—	—	—	0	0	0	0	0	1	1	1	0	1	0	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLBP0												
Initial value:	—	—	—	0	0	0	0	0	1	1	1	0	1	0	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	YCLBP1	H'00E9	R/W	Available	Y Calculation B Coefficient 1 This coefficient is for B to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'E9. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	YCLBP0	H'00E9	R/W	Available	Y Calculation B Coefficient 0 This coefficient is for B to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'E9. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.4 Y Calculation Addition Constant Register (YCLAP)

Address: DU0: H'FEB1400C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	YCLAP1							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	YCLAP0							
Initial value:	—	—	—	—	—	—	—	—	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	YCLAP1	H'10	R/W	Available	Y Calculation Addition Constant 1 This addition constant is used to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. This addition constant is an unsigned 8-bit integer. The default value is H'10.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	YCLAP0	H'10	R/W	Available	Y Calculation Addition Constant 0 This addition constant is used to generate the Y values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. This addition constant is an unsigned 8-bit integer. The default value is H'10.

20.3.10.5 Cb Calculation R Coefficient Register (CBCLRP)

Address: DU0: H'FEB14010

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBCLRP1												
Initial value:	—	—	—	1	0	0	0	1	0	1	0	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLRP0												
Initial value:	—	—	—	1	0	0	0	1	0	1	0	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	CBCLRP1	H'115A	R/W	Available	Cb Calculation R Coefficient 1 This coefficient is for R to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'115A. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CBCLRP0	H'115A	R/W	Available	Cb Calculation R Coefficient 0 This coefficient is for R to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'115A. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.6 Cb Calculation G Coefficient Register (CBCLGP)

Address: DU0: H'FEB14014

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBCLGP1												
Initial value:	—	—	—	1	0	0	1	0	1	0	1	0	0	1	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLGP0												
Initial value:	—	—	—	1	0	0	1	0	1	0	1	0	0	1	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	CBCLGP1	H'12A5	R/W	Available	Cb Calculation G Coefficient 1 This coefficient is for G to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'12A5. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CBCLGP0	H'12A5	R/W	Available	Cb Calculation G Coefficient 0 This coefficient is for G to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'12A5. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.7 Cb Calculation B Coefficient Register (CBCLBP)

Address: DU0: H'FEB14018

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBCLBP1												
Initial value:	—	—	—	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLBP0												
Initial value:	—	—	—	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	CBCLBP1	H'0400	R/W	Available	Cb Calculation B Coefficient 1 This coefficient is for B to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'400. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CBCLBP0	H'0400	R/W	Available	Cb Calculation B Coefficient 0 This coefficient is for B to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'400. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.8 Cb Calculation Addition Constant Register (CBCLAP)

Address: DU0: H'FEB1401C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CBCLAP1							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CBCLAP0							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	CBCLAP1	H'80	R/W	Available	Cb Calculation Addition Constant 1 This addition constant is used to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. This addition constant is an unsigned 8-bit integer. The default value is H'80.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CBCLAP0	H'80	R/W	Available	Cb Calculation Addition Constant 0 This addition constant is used to generate the Cb values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. This addition constant is an unsigned 8-bit integer. The default value is H'80.

20.3.10.9 Cr Calculation R Coefficient Register (CRCLRP)

Address: DU0: H'FEB14020

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CRCLRP1												
Initial value:	—	—	—	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLRP0												
Initial value:	—	—	—	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	CRCLRP1	H'0400	R/W	Available	Cr Calculation R Coefficient 1 This coefficient is for R to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'400. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CRCLRP0	H'0400	R/W	Available	Cr Calculation R Coefficient 0 This coefficient is for R to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'400. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.10 Cr Calculation G Coefficient Register (CRCLGP)

Address: DU0: H'FEB14024

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CRCLGP1												
Initial value:	—	—	—	1	0	0	1	1	0	1	0	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLGP0												
Initial value:	—	—	—	1	0	0	1	1	0	1	0	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	CRCLGP1	H'135A	R/W	Available	Cr Calculation G Coefficient 1 This coefficient is for G to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'135A. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CRCLGP0	H'135A	R/W	Available	Cr Calculation G Coefficient 0 This coefficient is for G to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'135A. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.11 Cr Calculation B Coefficient Register (CRCLBP)

Address: DU0: H'FEB14028

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CRCLBP1												
Initial value:	—	—	—	1	0	0	0	0	1	0	1	0	0	1	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLBP0												
Initial value:	—	—	—	1	0	0	0	0	1	0	1	0	0	1	0	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 29	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
28 to 16	CRCLBP1	H'10A5	R/W	Available	Cr Calculation B Coefficient 1 This coefficient is for B to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. The default value is H'10A5. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.
15 to 13	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
12 to 0	CRCLBP0	H'10A5	R/W	Available	Cr Calculation B Coefficient 0 This coefficient is for B to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. The default value is H'10A5. The coefficient is a 13-bit value of 1 sign bit + 12 fixed-point bits. The 12th bit represents the sign, the 11th bit represents the integer, and the 10th to 0th bits represent the value below the fixed point. 12th sign bit 0: + 1: - 11th to 0th bits A fixed-point absolute value should be set.

20.3.10.12 Cr Calculation Addition Constant Register (CRCLAP)

Address: DU0: H'FEB1402C

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CRCLAP1							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CRCLAP0							
Initial value:	—	—	—	—	—	—	—	—	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Internal Update	Description
31 to 24	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
23 to 16	CRCLAP	H'80	R/W	Available	Cr Calculation Addition Constant 1 This addition constant is used to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 1. This addition constant is an unsigned 8-bit integer. The default value is H'80.
15 to 8	—	—	R	—	Reserved The read value is undefined. The write value should always be 0.
7 to 0	CRCLAP0	H'80	R/W	Available	Cr Calculation Addition Constant 0 This addition constant is used to generate the Cr values in RGB-YC conversion by the RGB-YC conversion circuit by superposition processor 0. This addition constant is an unsigned 8-bit integer. The default value is H'80.

20.4 Display Function

Note: From section 20.4 on, descriptions of suffixes n and m are provided as the last paragraph or a note for the last table in each subsection.

20.4.1 Configuration of Output Screen

The display unit (DU) executes window displays with up to a maximum of eight window layers. Each of these windows is called a "plane", and the order of stacking of the planes can be set arbitrarily. For each plane, display can be turned on and off, and the display data format (8-bit/pixel, 16-bit/pixel, 32-bit/pixel, ARGB, YC), blending functions, and other settings can be changed independently. In addition to the window display plane, a plane that is dedicated to the α value can be synthesized (a maximum of one layer).

Each plane has a double-buffer configuration (triple buffer only for a video capture plane), so that smooth display is possible.

Note: In cases of high-resolution display, the unified memory traffic volume may be considerable depending on the number of combined planes and display size, and constraints may arise owing to the traffic volume; but there are no constraints on display functions.

Table 20.26 Display Functions of Planes

		Display Data Format										
	Display On/Off	**8-bit/ pixel**	**16-bit/ pixel**	**ARGB**	**YC**	**32-bit/ pixel**	**Super-positioning**	**Blinking**	**Size**	**Scroll-ing**	**Wrap-around**	**α-Ratio Plane**
Plane 1	✓	✓*1	✓	✓	✓*2	✓*5	α blending/ transparent color*5/ EOR operation	✓	X, Y (as desired)	✓	✓	✓
Plane 2	✓	✓*1	✓	✓	✓*2	✓*5	Same as above	✓	Same as above	✓	✓	✓
Plane 3	✓	✓*1	✓	✓	✓*2	✓*5	Same as above	✓	Same as above	✓	✓	✓
Plane 4	✓	✓*1	✓	✓	✓*2	✓*5	Same as above	✓	Same as above	✓	✓	✓
Plane 5	✓	✓*1	✓	✓	✓	✓*5	Same as above	✓	Same as above	✓	✓	✓
Plane 6	✓	✓*1	✓	✓	✓	✓*5	Same as above	✓	Same as above	✓	✓	✓
Plane 7	✓	✓*1	✓	✓	✓	✓*5	Same as above	✓	Same as above	✓	✓	✓
Plane 8	✓	✓*1	✓	✓	✓	✓*5	Same as above	✓	Same as above	✓	✓	✓
α plane 1	✓	✓	—	—	—	—	—	✓	Same as above	✓	✓	✓
α plane 2	✓	✓	—	—	—	—	—	✓	Same as above	✓	✓	✓
Back-ground color*3	—	—	—	—	—	—	—	—	—	—	—	—

Notes: 1. Any among color palettes 1, 2, 3, and 4 is selected.
2. YC → RGB conversion can be performed only for the YUV data of the uppermost plane.
3. The data format for background color is RGB666.

4. A 32-bit/pixel display specified with the PnLRGB1 or PnLRGB0 bit in the plane n display data control register (PnDDCR) involves the use of two planes. For example, planes 1 and 2 are combined to display 32-bit/pixel. When the PnEDF bits in plane n display data control 4 register (PnDDC4R) are used to specify a 32-bit/pixel display, only one plane is used.
5. Transparent color processing is not possible for a 32-bit/pixel display specified with the PnLRGB1 or PnLRGB0 bit in PnDDCR. Transparent color processing is possible when the PnEDF bits in PnDDC4R are used to specify a 32-bit/pixel display.
6. n = 1 to 8

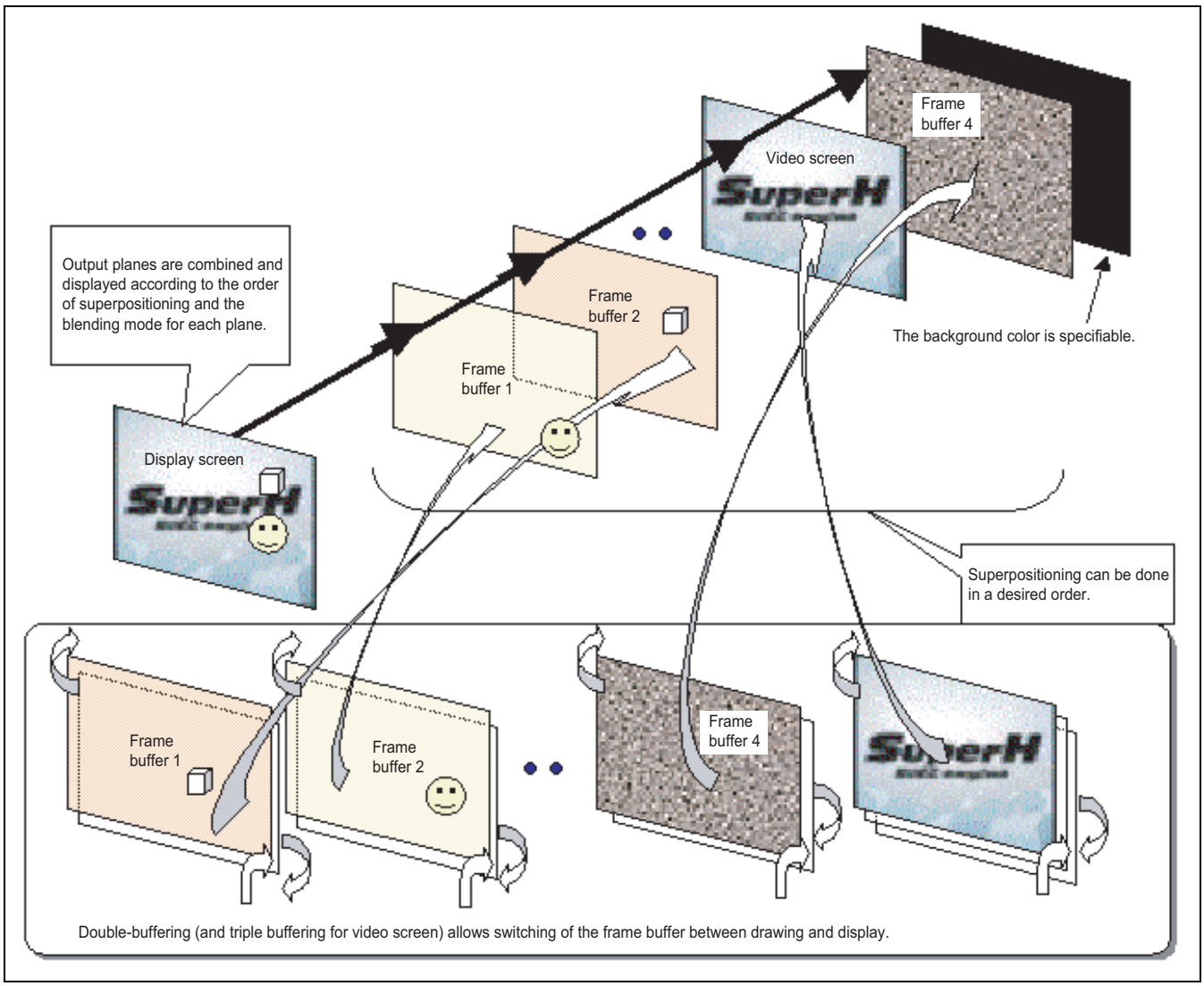


Figure 20.2 Block Diagram of Plane Configuration and Superpositioning

20.4.2 Display On/Off

All plane display can be turned on and off using the DEN bit in DSYSR0. When the DEN bit is 0, the display data set in DOORn*1 is displayed.

When the value of the DPRS bit in DORCR is 0, DPPR is used to turn the display of planes 1 to 8 on and off. When the value of the DPRS bit in DORCR is 1, on the other hand, DS0PR and DS1PR are used to turn the display of planes 1 to 8 on and off. Under the following display conditions, display data set in BPORn*1 is displayed.

1. When display of all planes 1 to 8 is turned off
2. In an area with no plane for display, due to the display size and display position
3. When the pixels in a plane for display are all a transparent color

Table 20.27 Turning On and Off the Display of Planes 1 to 8 (when the DPRS Bit of DORCR is 0)

Display Plane	Display Plane Priority Register (DPPR)
Plane 1	Plane 1 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 2	Plane 2 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 3	Plane 3 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 4	Plane 4 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 5	Plane 5 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 6	Plane 6 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 7	Plane 7 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1
Plane 8	Plane 8 is selected in one among priority positions 1 to 8, and the corresponding enable bit is set to 1

Table 20.28 Turning On and Off the Display of Planes 1 to 8 (when the DPRS Bit of DORCR is 1)

Display Plane	Display Superimpose 0 Priority Register (DS0PR) Display Superimpose 1 Priority Register (DS1PR)
Plane 1	Plane 1 is selected in one among priority positions 1 to 8 (setting to select the plane: 0001)
Plane 2	Plane 2 is selected in one among priority positions 1 to 8 (setting to select the plane: 0010)
Plane 3	Plane 3 is selected in one among priority positions 1 to 8 (setting to select the plane: 0011)
Plane 4	Plane 4 is selected in one among priority positions 1 to 8 (setting to select the plane: 0100)
Plane 5	Plane 5 is selected in one among priority positions 1 to 8 (setting to select the plane: 0101)
Plane 6	Plane 6 is selected in one among priority positions 1 to 8 (setting to select the plane: 0110)
Plane 7	Plane 7 is selected in one among priority positions 1 to 8 (setting to select the plane: 0111)
Plane 8	Plane 8 is selected in one among priority positions 1 to 8 (setting to select the plane: 1000)

Note: Even if display on is set using DPPR, DS0PR, or DS1PR under the following conditions, the setting is handled as display off, and the corresponding plane is not displayed.

- Planes for which the value set in PnDPXR*2 is greater than the screen size (horizontal display end (HDE) - horizontal display start (HDS))
- Planes for which the value set in PnDPYR*2 is greater than the screen size (vertical display end (VDE) - vertical display start (VDS))
- Planes for which the value set in PnDSXR*2 is 0
- Planes for which the value set in PnDSYR*2 is 0
- Planes for which the value set in PnMWR*2 is 0
- Planes for which the value set in PnSPXR*2 is equal to or greater than twice the value set in PnMWR*2

1. n = 0 and 1
2. n = 1 to 8

20.4.3 Plane Parameter

For each plane, a display area start position, memory width, display start position, and display size are set using registers.

The followings are the schematic diagram of start positions and sizes related to planes and the registers used for setting start positions and sizes.

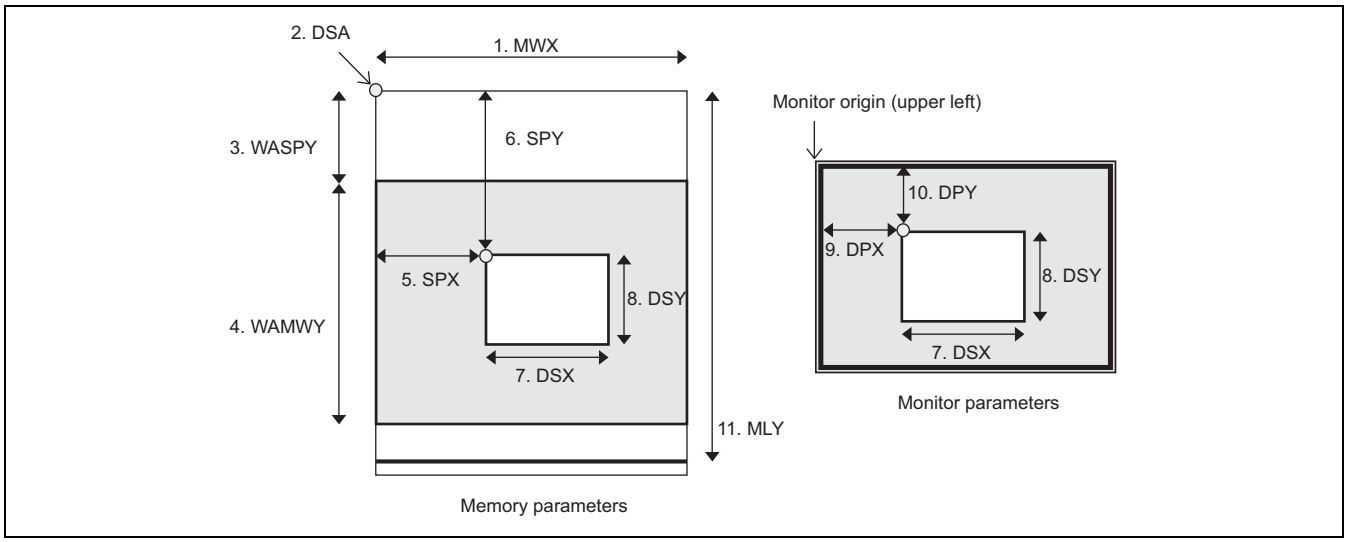


Figure 20.3 Parameters

Table 20.29 Memory Parameter/Monitor Parameter Setting Registers

No.	Name Used in the Figure	Register	Description
1	MWX (Plane memory width)	PnMWR	The plane X-direction memory width is set between 16 and 4096 pixels, in 16 pixel units.
2	DSA (Display area start address)	PnDSA0R to PnDSA2R	The start address in memory area is set for plane.
3	WASPY (Wrap-around start position)	PnWASPR	The Y direction start position of the wrap-around area is set in line units, with the address set by DSA as reference.
4	WAMWY (Wrap-around memory width)	PnWAMWR	The wrap-around Y-direction memory width is set to a desired value in the range from 240 to 4095 (representing line units).
5	SPX (Start position X)	PnSPXR	The distance in the X direction to the display start position is set in pixel units, taking the address set by DSA as the origin.
6	SPY (Start position Y)	PnSPYR	The distance in the Y direction to the display start position is set in raster line units, taking the address set by DSA as the origin.
7	DSX (Display size X)	PnDSXR	The X-direction display size of plane is set in dot-clock units.
8	DSY (Display size Y)	PnDSYR	The Y-direction display size of plane is set in raster line units.
9	DPX (Display position X)	PnDPXR	The X-direction distance to the display position is set in dot-clock units, taking the upper-left corner of the monitor as the origin.
10	DPY (Display position Y)	PnDPYR	The Y-direction distance to the display position is set in raster line units, taking the upper-left corner of the monitor as the origin.
11	MLY (Memory length Y)	PnMLR	The Y-direction memory area of plane is set in line units.

Note: n = 1 to 8

20.4.4 Memory Allocation

A display start address for the display screen, drawing screen 1, and drawing screen 2 used for video display can be set individually for each plane. The start addresses for the memory areas used are set in each of the display area start address registers.

In the display unit (DU), when the display plane is video captured, the display area start addresses 0, 1, and 2 for each plane are used to perform triple-buffering control and display the plane. When the display plane is not video captured, the display area start addresses 0 and 1 for each plane are used to perform double-buffering control and display the plane.

The double-buffering control can be performed for alpha-ratio planes. In display capture, only a single area can be set to store the data.

Below is a list of display area start address registers used for each of the planes.

Table 20.30 Memory Allocation Registers

Display Screen	Register Name	
Plane n	Plane n display area start address 0 register	PnDSA0R
	Plane n display area start address 1 register	PnDSA1R
	Plane n display area start address 2 register	PnDSA2R
α plane m	Alpha-ratio plane m display area start address 0 register	APmDSA0R
	Alpha-ratio plane m display area start address 1 register	APmDSA1R
Display capture	Display capture area start address register	DCSAR
Display capture 2	Display capture 2 area start address register	DC2SAR

Notes: n = 1 to 8
m = 1 and 2

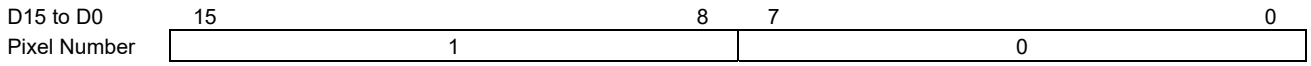
20.4.5 Display Data Format

The following format is used for color data used in display. A data configuration is shown in which data is allocated to the unified memory in little endian.

(1) 8-bit/pixel

A color palette index is used. The color palette is used to convert and display image data into RGB data with 6 bits for each RGB color (RGB666).

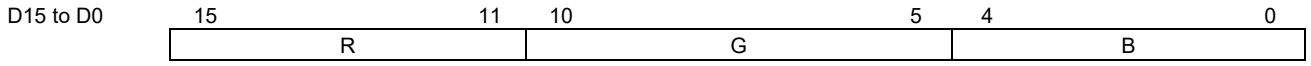
8-bit/pixel data (index color)



(2) 16-bit/pixel: RGB

The RGB levels are represented using 5 bits for R, 6 bits for G, and 5 bits for B (RGB565).

16-bit/pixel data (RGB data) format

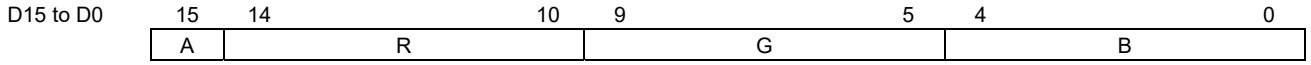


(3) 16-bit/pixel: ARGB

Levels for A, R, G, and B are represented by 1, 5, 5, and 5 bits respectively (ARGB1555). In addition to the R, G, and B values, this format includes a bit that represents α blending control. In this section, "ARGB" indicates ARGB1555 and "ARGB8888" indicates the 32-bit/pixel format unless otherwise specified.

α blending control using the A value is valid when the PnSPIM* bit in PnMR* is set to perform α blending. When the PnABIT* bits of PnALPHAR* are B'00, α blending is performed when A = 1. When the PnABIT* bits are B'01, α blending is performed when A = 0. When the PnABIT* bits are B'10 or B'11, α blending is performed regardless of the A value. When the PnSPIM* bit is not set to perform α blending, α blending is not performed regardless of the A value.

16-bit/pixel data (ARGB data) format



(4) YC: YUV422

Image data has the format YC (YCbCr) = 4:2:2. A calculation circuit is used to convert each of the 8 bits of the RGB colors (RGB888) of image data. Transparent color processing is not possible.

The YC data order corresponds to the UYVY format and YUYV format. The UYVY format and YUYV format can be selected using the PnYCDF* bits in PnMR*.

The formulae for YC-RGB conversion are given below. The underlined coefficients are defined by the settings in the corresponding registers.

$$R = YNC \times (Y - YNO) + RCRC \times (Cr - CRNO)$$
$$G = YNC \times (Y - YNO) - GCRCR \times (Cr - CRNO) - GCBC \times (Cb - CBNO)$$
$$B = YNC \times (Y - YNO) + BCBC \times (Cb - CBNO)$$

The formulae for YC-RGB conversion in the default state are thus as follows.

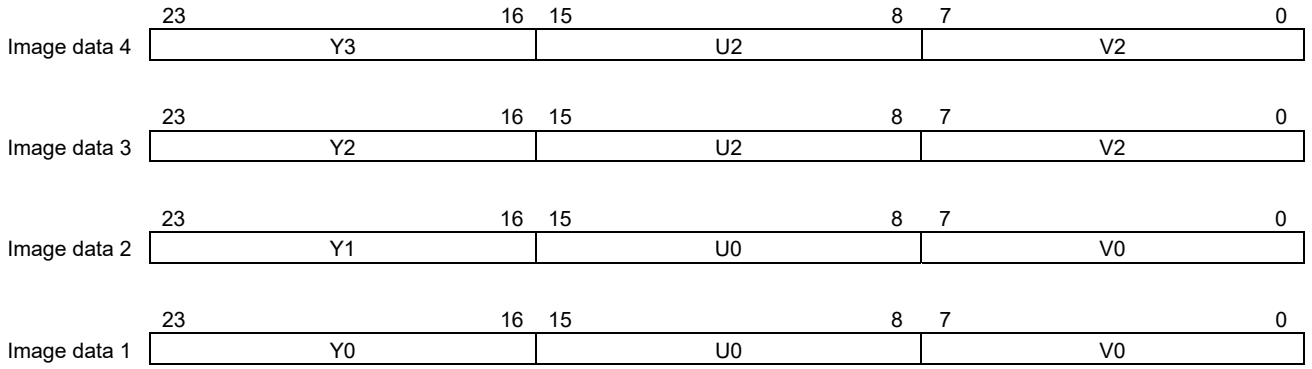
$$R = Y + 1.37 \times (Cr - 128)$$

$$G = Y - 0.698 \times (Cr - 128) - 0.336 \times (Cb - 128)$$
$$B = Y + 1.73 \times (Cb - 128)$$

(a) UYVY format

(b) YUYV format

(c) RGB color-space conversion format



(5) YC: YUV420

Image data has the format YC (YCbCr) = 4:2:0. A calculation circuit is used to convert each of the 8 bits of the RGB colors (RGB888) of image data. Transparent color processing is not possible.

The UV data order corresponds to the NV12 format and NV21 format. The NV12 format and NV21 format can be selected using the PnNV21* bit in PnDDC2R*.

The formulae for YC-RGB conversion are the same as those for YC:YUV422.

(a) Y data

	63	56	55	48
D63 to D48 Image data 8 and 7	Y7		Y6	

	47	40	39	32
D47 to D32 Image data 6 and 5	Y5		Y4	

	31	24	23	16
D31 to D16 Image data 4 and 3	Y3		Y2	

	15	8	7	0
D15 to D0 Image data 2 and 1	Y1		Y0	

(b) UV data (NV12)

	63	56	55	48
D63 to D48 Image data 8 and 7	V6		U6	

	47	40	39	32
D47 to D32 Image data 6 and 5	V4		U4	

	31	24	23	16
D31 to D16 Image data 4 and 3	V2		U2	

	15	8	7	0
D15 to D0 Image data 2 and 1	V0		U0	

(c) UV data (NV21)

	63	56	55	48
D63 to D48 Image data 8 and 7	U6		V6	

	47	40	39	32
D47 to D32 Image data 6 and 5	U4		V4	

	31	24	23	16
D31 to D16 Image data 4 and 3	U2		V2	

	15	8	7	0
D15 to D0 Image data 2 and 1	U0		V0	

(d) RGB color-space conversion format

	23	16	15	8	7	0
Image data 4 (Line 0)	Y3 (Line 0)		U2 (Line 0)		V2 (Line 0)	
Image data 3 (Line 0)	Y2 (Line 0)		U2 (Line 0)		V2 (Line 0)	
Image data 2 (Line 0)	Y1 (Line 0)		U0 (Line 0)		V0 (Line 0)	
Image data 1 (Line 0)	Y0 (Line 0)		U0 (Line 0)		V0 (Line 0)	
Image data 4 (Line 1)	Y3 (Line 1)		U2 (Line 0)		V2 (Line 0)	
Image data 3 (Line 1)	Y2 (Line 1)		U2 (Line 0)		V2 (Line 0)	
Image data 2 (Line 1)	Y1 (Line 1)		U0 (Line 0)		V0 (Line 0)	
Image data 1 (Line 1)	Y0 (Line 1)		U0 (Line 0)		V0 (Line 0)	

(6) 32-bit/pixel: ARGB8888

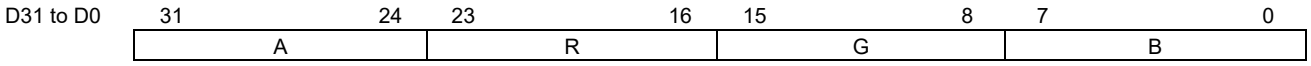
Levels for A, R, G, and B are represented by 8 bits each (ARGB8888). Note that the format includes a setting for alpha ratio in addition to the R, G, and B values. In this section, "32-bit/pixel" refers to the ARGB8888 format unless otherwise specified.

α blending control using the A value is valid when the PnSPIM* bit in PnMR* is set so that α blending is performed. This means that the blending ratio selected in the plane n blending ratio register (PnALPHAR*) is invalid.

A 32-bit/pixel (ARGB8888) display should be specified with the PnLRGB1* or PnLRGB0* bit in the plane n display data control register (PnDDCR*) or the PnEDF* bits in plane n display data control 4 register (PnDDC4R*). When using the PnLRGB1* or PnLRGB0* bit in PnDDCR*, the following restrictions apply.

- Two planes, plane 1 and plane 2, need to be used.
- Transparent color processing is not possible.
- α blending or EOR operations must be performed in an area where a lower plane exists. If the setting of the PnSPIM* bits allows α blending or an EOR operation but there is no lower plane, display of 32-bit/pixel data will not be possible without superposition.

32-bit/pixel data (ARGB8888 data) format

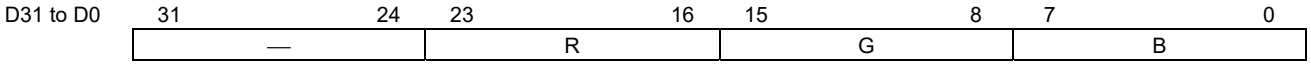


(7) 32-bit/pixel: RGB888

Levels for R, G, and B are represented by 8 bits each (RGB888). "—" indicates any desired value.

A 32-bit/pixel (RGB888) display should be specified with the PnEDF* bits in plane n display data control 4 register (PnDDC4R*).

32-bit/pixel data (RGB888 data) format

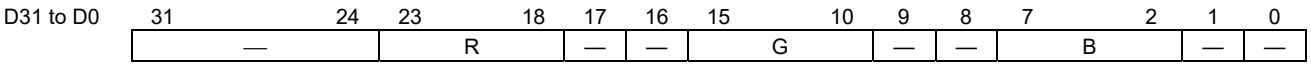


(8) 32-bit/pixel: RGB666

Levels for R, G, and B are represented by 6 bits each (RGB666). "—" indicates any desired value.

A 32-bit/pixel (RGB666) display should be specified with the PnEDF* bits in plane n display data control 4 register (PnDDC4R*).

32-bit/pixel data (RGB666 data) format



Note: * n = 1 to 8

20.4.6 Data Formats for Output and Display Capture

In the case of digital RGB output from a display unit (DU), superpositioning in the form of α blending and EOR operations is performed after the display data format has been expanded into the RGB888 format, and then the data are output. In data capture, display data are captured and stored as RGB888 or the five higher-order bits from both the red pins and blue pins and six bits from the green pins. The supplementary formats and data formats in the case of expansion to RGB888 are as indicated in the following table.

Table 20.31 Output Data Format

		Red								Green								Blue							
		7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
Expanded data	8-bit/pixel (after conversion from a color palette)	R (6 bits)						0	0	G (6 bits)						0	0	B (6 bits)						0	0
	16-bit/pixel	R (5 bits)					0	0	0	G (6 bits)					0	0	0	B (5 bits)					0	0	0
	ARGB	R (5 bits)					0	0	0	G (5 bits)					0	0	0	B (5 bits)					0	0	0
	YC after RGB conversion	R (8 bits)								G (8 bits)								B (8 bits)							
	32-bit/pixel (ARGB8888)	R (8 bits)								G (8 bits)								B (8 bits)							
	32-bit/pixel (RGB888)	R (8 bits)								G (8 bits)								B (8 bits)							
	32-bit/pixel (RGB666)	R (6 bits)						0	0	G (6 bits)						0	0	B (6 bits)						0	0
After superpositioning		R (8 bits)								G (8 bits)								B (8 bits)							
DU0 display data		R (8 bits)								G (8 bits)								B (8 bits)							
DU1 display data		R (8 bits)								G (8 bits)								B (8 bits)							

20.4.7 Endian Conversion

The display unit (DU) can perform big-endian/little-endian conversion according to the setting of bit 20 in DSYSRn*1. If image data are in 32-bit/pixel format, big-endian/little-endian conversion for the data involves the use of the plane n swap control register (PnSWAPR*2). Then set bit 20 in DSYSRn*1 to 0.

The internal data format in the display unit (DU) is fixed to little-endian; by setting bit 20 in DSYSRn*1 to 1, image data arranged in big-endian format in memory are converted into little-endian format and read.

The unit for endian conversion (byte/word) is determined by the setting of the PnDDF*2 bits in PnMR*2.

Table 20.32 Endian Conversion

PnMR/PnDDF*2	Data Format	Units for Endian Conversion
B'00	8-bit/pixel	Byte
B'01	16-bit/pixel	Word
B'10	ARGB	Word
B'11	YC	Byte

Endian conversion in each of the units indicated below is shown in Figure 20.4.

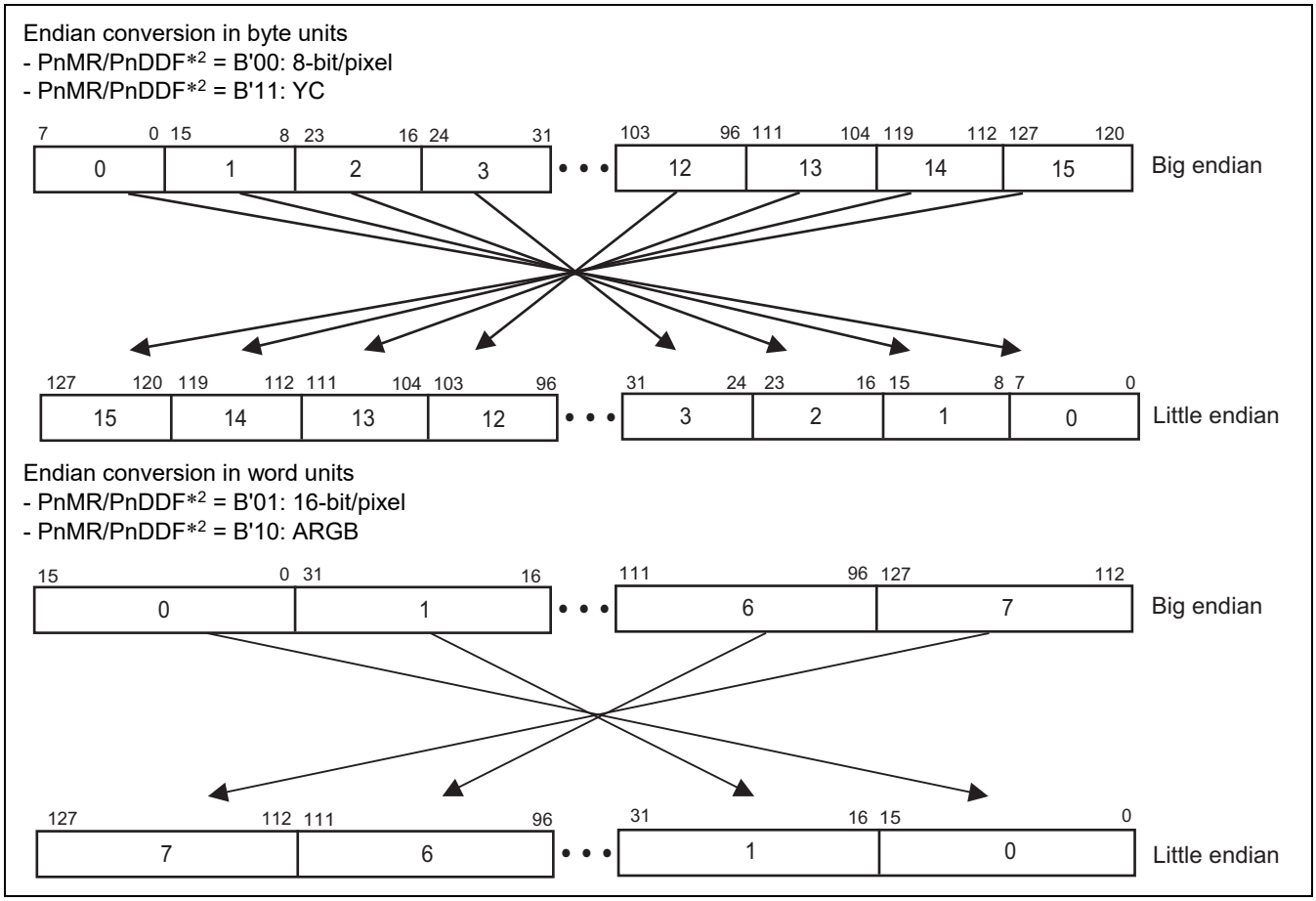


Figure 20.4 Endian Conversion

Since bits 3 and 2 in the plane n swap control register (PnSWAPR*2) are set to 1 and bits 1 and 0 in PnSWAPR*2 are set to 0 in the 32-bit/pixel case, the endian must be converted as shown in the figure below. Bit 4 in PnSWAPR*2 may be set to either 1 or 0. At this time, set bit 20 in the display unit system control register n (DSYSRn*1) to 0.

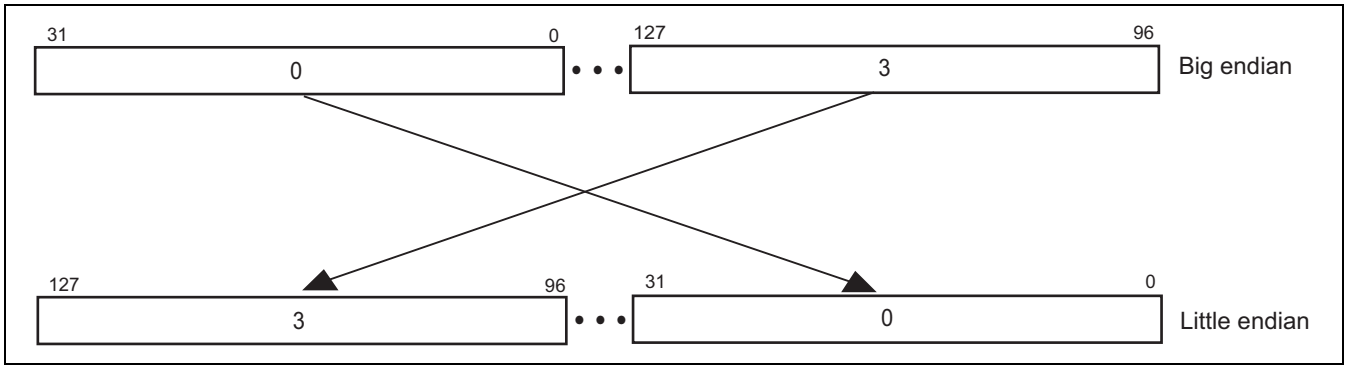


Figure 20.5 Endian Conversion for 32-bit/pixel

Notes: 1. n = 0 and 1
2. n = 1 to 8

20.4.8 Color Palette

8-bit/pixel data employs color palettes. The DU has four color palettes which are only accessible to superposition processors 0.

The color palette for use in plane n is determined by the setting of the PnCPSL* bits in PnMR*. Each of the color palettes consists of two alternate buffers; one serves as a display buffer, and the other is for CPU access. After setting each color palette, by setting the color palette switching enable bit CP4CE, CP3CE, CP2CE, or CP1CE in CPCR to 1, the color palette thus set becomes valid at the next VSYNC falling edge (internal update timing), or upon display reset (when the DRES bit in DSYSR0 is changed from 1 to 0).

(1) Notes on Use of Color Palettes

1. Because palettes consist of alternate buffers, complete overwriting is necessary upon a color palette update. However, when the details of color palette updates are being managed, there is no problem with overwriting only the relevant part.
2. Upon completion of color palette settings, the switching enable bit must always be set to 1.
3. When reading a color palette from the CPU, reading should be performed before setting the switching enabled bit to 1.

(2) Procedure for Setting a Color Palette

(a) Procedure for switching from the initial state

The initial state (after power-on reset) is the display reset state.

1 Set the display unit system control register.
2. Set color palette 1, 2, 3, or 4.
3. After setting the color palette, set the color palette switching enable bit to 1.
4. Cancel the display reset.

(b) Procedure for switching from display state

In the display state, the DRES bit and DEN bit in DSYSR0 are 0 and 1 respectively.

1. Confirm that the color palette switching enable bit is 0.

2. Set color palette 1, 2, 3, or 4.
3. After setting the color palette, set the color palette switching enable bit to 1.

Note: * n = 1 to 8

20.4.9 Superpositioning of Planes

For each plane, three types of combined superpositioning are possible: α blending, transparent colors, and EOR operations. By setting the PnSPIM*3 bits in PnMR*3, the superpositioned display type can be selected.

However, α blending and EOR operation cannot be performed simultaneously on the same plane.

Transparent color processing for YC data is not possible.

When 32-bit/pixel data is specified with the PnLRGB1*3 or PnLRGB0*3 bit in the plane n display data control register (PnDDCR*3), the following restrictions apply to superpositioning. These restrictions do not apply when using the PnEDF*3 bits in plane n display data control 4 register (PnDDC4R*3).

- Transparent color processing is not possible. Bit 2 in PnSPIM*3 must be set to 1.
- When α blending or an EOR operation has been specified but all of the lower planes are off, the display of 32-bit/pixel data is not possible.
- The alpha ratio of the 32-bit/pixel data (ARGB8888) can only be the higher-order eight bits (A value).

Table 20.33 Superpositioning

PnSPIM	Superpositioning	YC Data or 32-bit/pixel Data*2
B'000	Transparent color processing is performed for the specified plane. When the specified plane is a transparent color, the lower plane is displayed. (Default)	Prohibited
B'001	Blending of the specified plane with the lower plane is performed. When the specified plane is a transparent color, blending is not performed and the lower plane is displayed.	Prohibited
B'010	EOR operation of the specified plane and the lower plane is performed. When the specified plane is a transparent color, EOR operation is not performed and the lower plane is displayed.	Prohibited
B'011	Setting prohibited (The lower plane is displayed.)	Prohibited
B'100	Transparent color processing is not performed for the specified plane. The specified plane is displayed.	Possible
B'101	Blending of the specified plane with the lower plane is performed. Transparent color specification for the specified plane is ignored, and blending of all the pixels in the specified plane with the lower plane is performed.	Possible*1
B'110	EOR operation of the specified plane and the lower plane is performed. Transparent color specification for the specified plane is ignored, and EOR operation of all the pixels in the specified plane and the lower plane is performed	Possible*1
B'111	Setting prohibited (The lower plane is displayed.)	Prohibited

After the image data format has been expanded to RGB888, α blending or EOR operation is performed. The complementary format of each display data format is shown in Table 20.31. α blending and EOR operation are performed in the sequence of the lower plane to the upper plane. The block diagram is shown below.

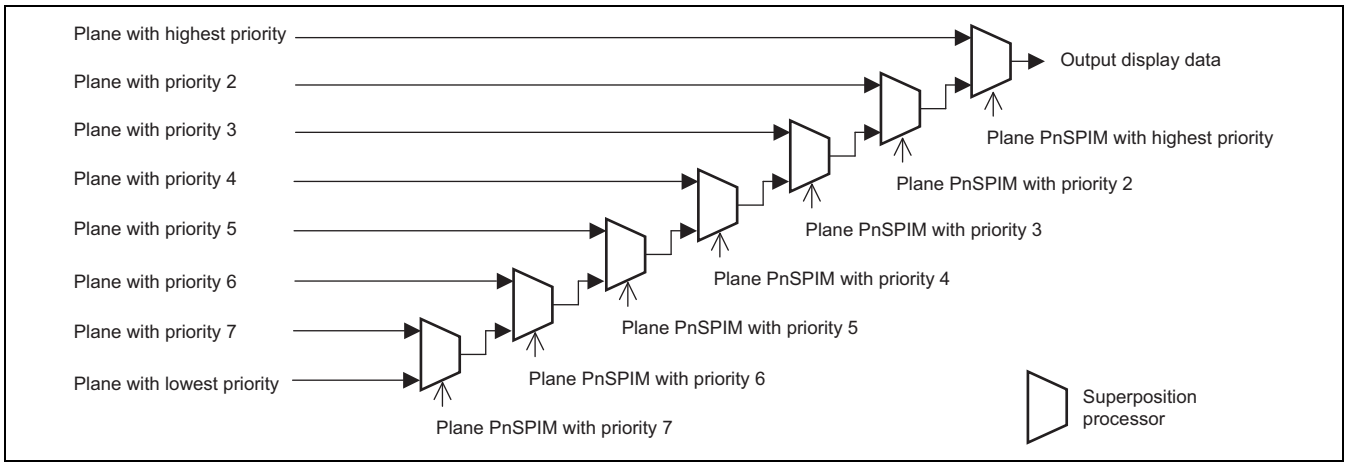


Figure 20.6 Plane Processing Sequence in α Blending and EOR Operation

When the format of display data for α blending or EOR operation is 8-bit/pixel, after selection in advance of the color palette to be used, the α blending or EOR operation on/off should be specified. At this time, when both planes for α blending or for EOR operation have the same color palette selected (color palette contention), only the specified plane is displayed, with no α blending or EOR operation performed. When display of all lower planes is turned off, the specified plane is displayed. That is, α blending or EOR operation of the specified plane with the image data specified in BPORn*3 is not performed. Note however that when a 32-bit/pixel display is set by the PnLRGB1*3 or PnLRGB0*3 bit in the plane n display data control register (PnDDCR*3), display of 32-bit/pixel data is not possible when α blending or an EOR operation has been specified but all of the lower planes are off.

(1) α Blending

In α blending, blending processing is performed according to the alpha (α) ratio set by the PnALPHA*3 bits in PnALPHAR*3, the alpha (α) ratio set by the blending ratio bits in the color palette, the alpha (α) ratio of the image data of the display plane, or the data in an α plane.

In the case of 32-bit/pixel data (ARGB8888), the alpha ratio can only be the higher-order eight bits (A value) of the 32-bit/pixel data (ARGB8888).

$$\text{Result of blending} \approx (\text{specified plane} \times \alpha/255 + \text{lower plane} \times (1 - \alpha/255) \quad \text{(Approximation)}$$

In the above formula, the blending result, α, the specified plane, and the lower plane are all given as 8-bit data.

When the alpha ratio is set to H'00, only the lower plane is displayed. When the alpha ratio is set to H'FF, only the specified plane is displayed. When the PnDDF*3 bits in PnMR*3 are set to ARGB, and moreover the PnSPIM*3 bit in PnMR*3 is set to perform α blending, α blending is performed according to the A value of the ARGB data format and by the α value specified by the PnALPHA*3 bits in PnALPHAR*3.

When the PnABIT*3 bits of PnALPHAR*3 are B'00, α blending is performed when the A value is 1. When the PnABIT*3 bits are B'01, α blending is performed when the A value is 0. When the PnABIT*3 bits are B'10 or B'11, α blending is performed regardless of the A value.

(2) Transparent Colors

For each plane, transparent color processing can be performed between the specified plane and the lower plane by setting PnSPIM*3 bit in PnMR*3 to 0. However, transparent color processing cannot be performed for YC data and 32-bit/pixel data (when set with the PnLRGB1*3 or PnLRGB0*3 bit in PnDDCR*3).

(a) 8-bit/pixel Mode

When the PnTC*3 bit in PnMR*3 is 0 (initial value), transparent color processing is performed according to the setting in the plane n transparent color 1 register (PnTC1R*3). When the PnTC*3 bit in PnMR*3 is 1, CP1TR*3 to CP4TR*3 can be used to set up to 16 colors in each of color palettes 1 to 4 as transparent colors. Only the indexes H'00 to H'0F can be specified as transparent colors; H'10 to H'FF cannot be specified as transparent colors.

The color palette 1 to 4 transparent color registers (CP1TR*3 to CP4TR*3) can be selected using the PnCPSL*3 bits in PnMR*3.

(b) 16-bit/pixel Mode and ARGB Mode

Transparent color processing is performed according to PnTC2R*3, regardless of the setting of the PnTC*3 bit in PnMR*3.

In the case of ARGB, bits 14 to 0 of PnTC2R*3 are compared, and bit 15 is ignored.

(c) 32-bit/pixel Mode

Transparent color processing is performed according to PnTC3R*3, regardless of the setting of the PnTC*3 bit in PnMR*3.

For the bits to be compared, see Table 20.24.

The above is summarized in Table 20.34, which indicates the transparent color specification registers which are valid when the PnTC*3 bit is 0 and 1.

Table 20.34 Transparent Color Specification Registers

Data Format	Transparent Color Specification Bit (PnMR*3) /PnTC*3	Color Palette Select Bit (PnMR*3) /PnCPSL*3	Transparent Color Specification Register
8-bit/pixel	0	—	PnTC1R*3
	1	B'000	CP1TR
	1	B'001	CP2TR
	1	B'010	CP3TR
	1	B'011	CP4TR
16-bit/pixel	—	—	PnTC2R*3
ARGB	—	—	PnTC2R*3
32-bit/pixel	—	—	PnTC3R*3

(3) EOR Operation

EOR operation of the specified plane with the lower plane is performed.

Notes: 1. Display of 32-bit/pixel data is not possible when all of the lower planes are off.
2. When a 32-bit/pixel display is set by the PnLRGB1*3 or PnLRGB0*3 bit in PnDDCR*3.
3. n = 1 to 8

20.4.10 Contention

(1) Contention for a Color Palette

When the same color palette has been specified for two or more planes in the 8-bit/pixel format, contention for that color palette between the planes may arise in α blending and EOR operations. Whether or not contention has occurred is judged on a per-pixel rather than per-plane basis.

In the figure below, planes 1 to 3 are in 8-bit/pixel format with α blending specified for plane 1 and an EOR operation specified for planes 2 and 3. The figure shows the results in cases where contention has arisen because the same color palette has been specified for all of the planes (we assume that none of these planes includes transparent-color pixels).

In the event of contention, α blending and EOR operations do not proceed and the uppermost plane is displayed.

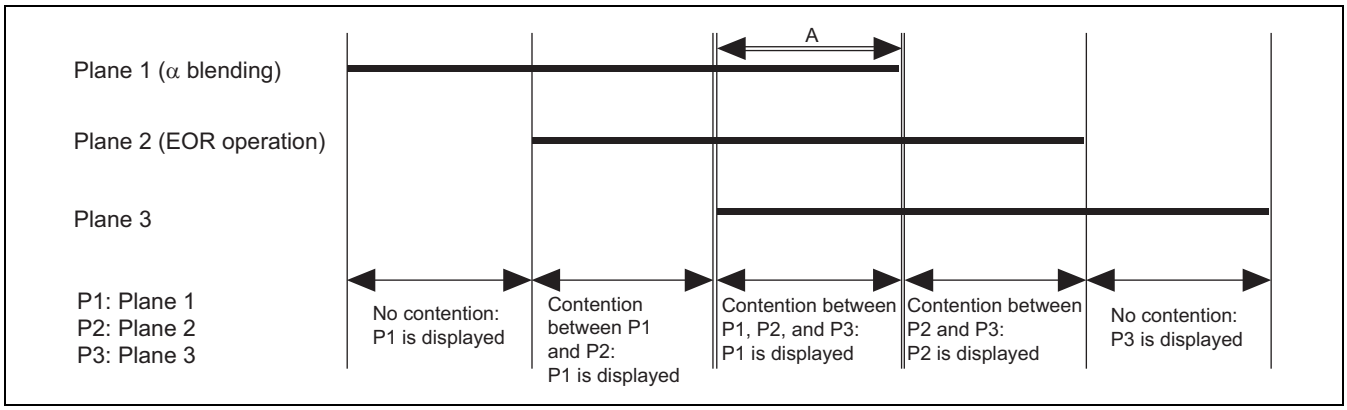


Figure 20.7 Contention for a Color Palette (When Multiple Planes Have the Same Color Palette)

Figure 20.8 shows the results of all patterns of contention and the presence of transparent colors to be displayed during period A in the above figure.

- P1 α P2 indicates α blending of planes 1 and 2.
- P2 ⊙ P3 indicates an EOR operation for planes 2 and 3.
- P1 α (P2 ⊙ P3) indicates α blending of plane 1 with the result of the EOR operation for planes 2 and 3.
- BPOR indicates data specified by the background plane output register n (BPORn*).

Note: * n = 0 and 1.

				✓: Contention, —: No contention				
				P1	✓	✓	✓	—	—
				P2	✓	✓	—	✓	—
				P3	✓	—	✓	✓	—
○: Transparent, ●: Non-transparent	P1	P2	P3						
	●	●	●		P1	P1	P1 α P2	P1 α P2	P1 α (P2⊙P3)
	●	●	○		P1	P1	P1 α P2	P1 α P2	P1 α P2
	●	○	●		P1	P1 α P3	P1	P1 α P3	P1 α P3
	●	○	○		P1	P1	P1	P1	P1
	○	●	●		P2	P2⊙P3	P2⊙P3	P2	P2⊙P3
	○	●	○		P2	P2	P2	P2	P2
	○	○	●		P3	P3	P3	P3	P3
	○	○	○		BPOR	BPOR	BPOR	BPOR	BPOR

Figure 20.8 Contention for a Color Palette and Transparent Colors

(2) YC Data Contention

The display unit (DU) has only one YC-RGB conversion circuit internally, and so YC-RGB conversion cannot be performed simultaneously for two or more planes. When there are pixels requiring YC-RGB conversion on two or more planes simultaneously, the pixels on the uppermost plane are YC-RGB converted, and the lower plane is not displayed. Figure 20.9 describes YC-RGB conversion when the data for three planes is in YC format.

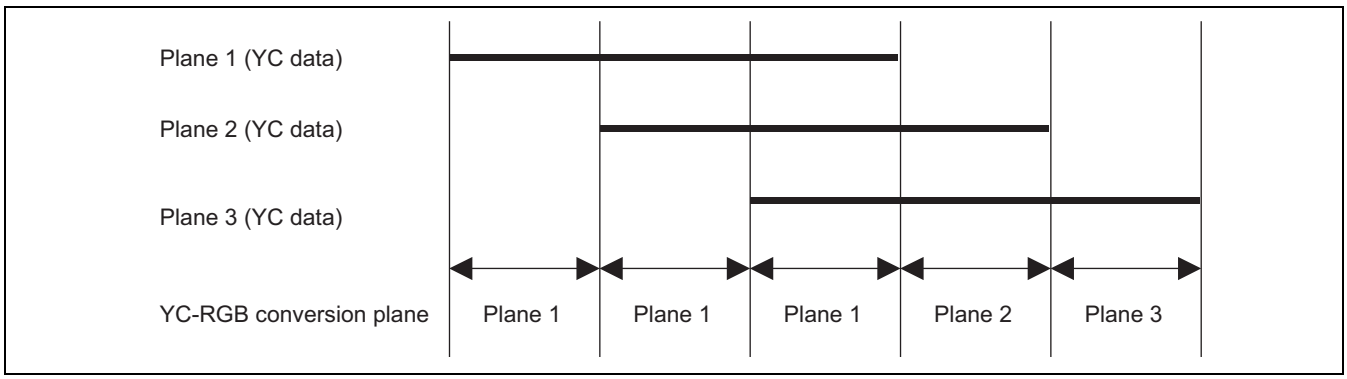


Figure 20.9 YC Data Contention

(3) Plane Priority Order

The display priority order for planes is set using DPPR, DS0PR, or DS1PR; if one plane is set in two or more places in the priority order, the place with highest priority is selected.

For example, if the setting in DPPR is H'00CB_D888, then the results of the priority order and display on/off settings are as follows.

Plane with priority 1	Plane 1
Plane with priority 2	No corresponding plane
Plane with priority 3	No corresponding plane
Plane with priority 4	Plane 6
Plane with priority 5	Plane 4
Plane with lowest priority	Plane 5
Display off planes	Plane 2, plane 3, plane 7, and plane 8

20.4.11 Blinking

For each plane, blinking operation can be performed by using the display area start addresses 0 and 1.

Usually, double-buffering control is performed for each plane according to the setting of the PnBM* bit in PnMR*. However, blinking is performed with the period specified by the PnBTA* and PnBTB* bits in PnBTR* by setting the PnBM* bits in PnMR* to B'10 (auto display change mode (blinking mode)). When the blinking period is set to 1, the display area start addresses 0 and 1 can be switched for every VSYNC; the same function as the auto display change mode can be achieved.

Note: Set a value other than 0 to the PnBTA* and PnBTB* bits in PnBTR*.
* n = 1 to 8

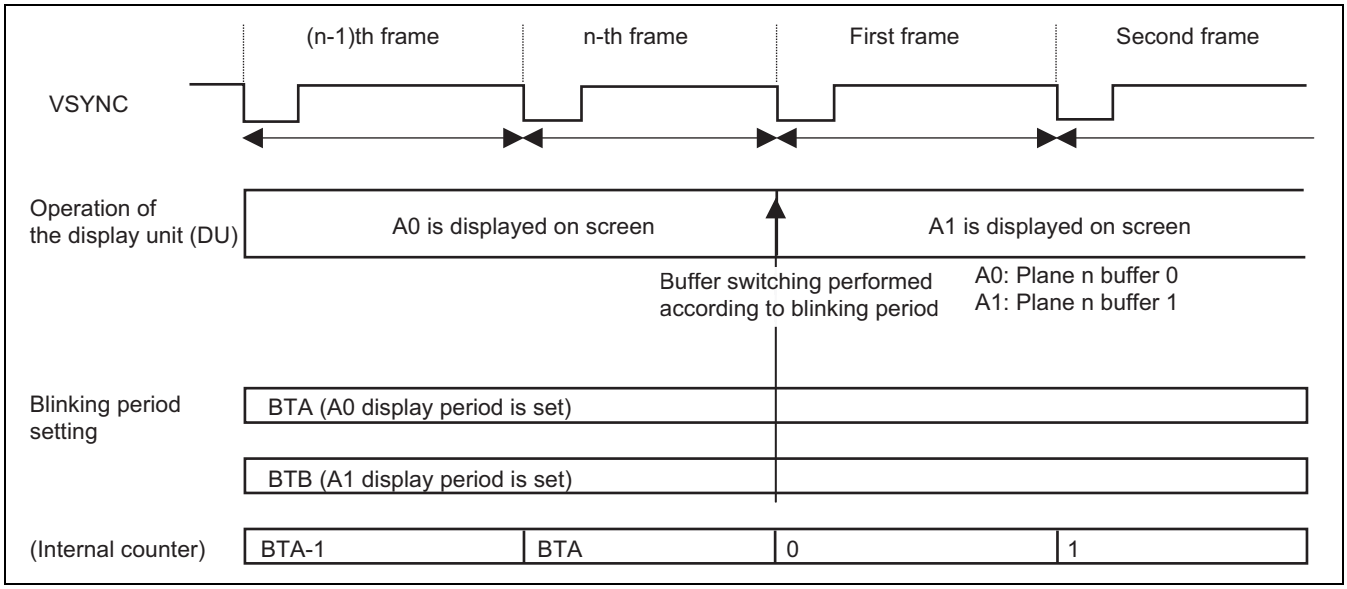


Figure 20.10 Blinking

20.4.12 Scroll Display

By setting display area and display screen sizes and start positions independently for each plane, smooth scroll processing can be performed independently for each plane.

The display can be scrolled by cyclically setting the values of display start positions X and Y (coordinates specified by PnSPXR* and PnSPYR*), taking as the origin the start address in memory specified by PnDSA0R* to PnDSA2R* for each plane.

Figure 20.11 summarizes display scrolling. The display is scrolled by setting the display start position from A to B.

Note: Display sizes and other area settings for each plane should be set such that there is no data display outside the memory configuration area.

* n = 1 to 8

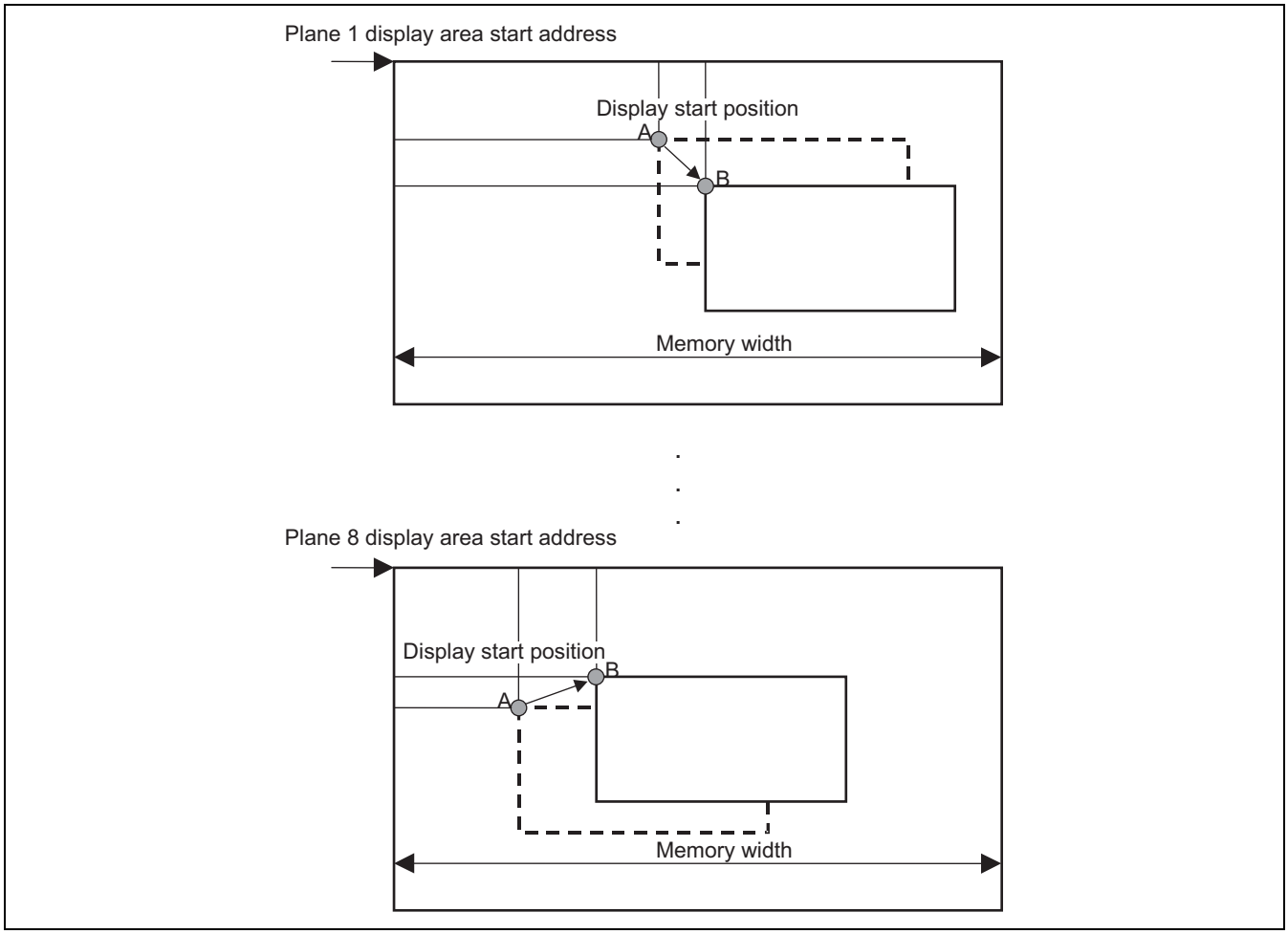


Figure 20.11 Schematic Diagram of Scroll Display

20.4.13 Wrap-Around Display

In addition to display scrolling, wrap-around display, which can be used in spherical scrolling, is possible for each plane. When enabling wrap-around display, the PnWAE*1 bit in PnMR*1 is set to 1. As a result of changing the values of display start positions X and Y (the plane n start position X set in PnSPXR*1 and the plane n start position Y set in PnSPYR*1) in order to scroll the display, even when plane n overflows the wrap-around area, the wrap-around area is seen as a spherical surface in wrap-around display, as in Figure 20.12, and the part overflowing is complemented and displayed. The method used to specify the wrap-around area is described below.

1. The start address of the memory used for plane n is specified in PnDSA0R*1 to PnDSA2R*1.
2. With the beginning of the specified memory as origin, the upper-left coordinates of the wrap-around area are specified in PnWASPR*1. The X-direction width of the wrap-around area is the memory width set in PnMWR*1.
3. The Y-direction width of the wrap-around area is set in PnWAMWR*1.

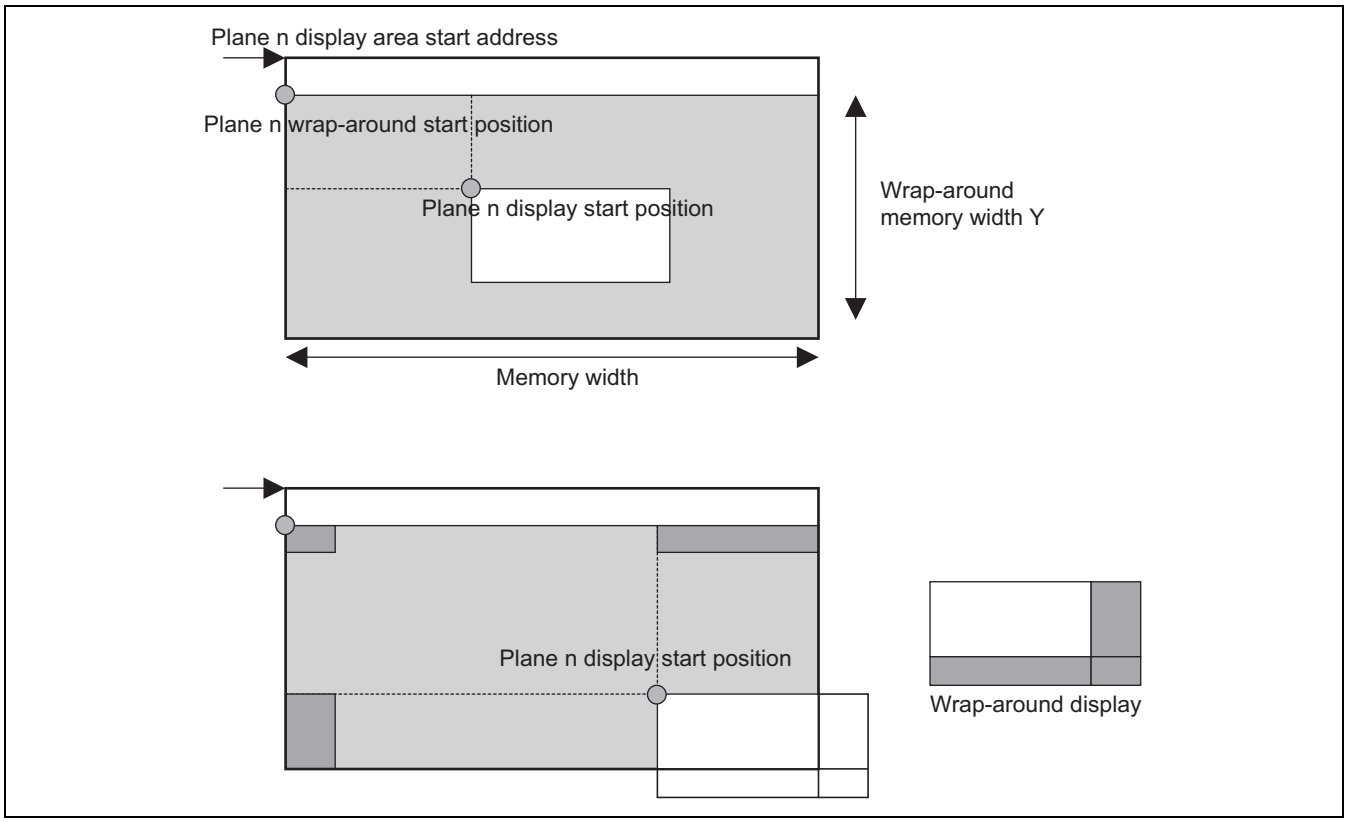


Figure 20.12 Schematic Diagram of Wrap-Around Display

Notes: When wrap-around display is disabled (when the PnWAE*1 bit in PnMR*1 is 0), the part overflowing the wrap-around area becomes the color specified by BPORn*2, and superposition processing using this color is performed.

1. n = 1 to 8
2. n = 0 and 1

20.4.14 Upper-Left Overflow Display

For each plane, a display start position in memory (PnSPXR*, PnSPYR*) and display size (PnDSXR*, PnDSYR*) can be set arbitrarily, so that by combining and using these registers, areas overflowing the upper-left relative to the monitor origin (upper-left corner) can be displayed without overwriting display data in memory.

For a picture of size (DSX, DSY) and with start position (SPX, SPY), by setting the size to (DSX-ΔX, DSY-ΔY) and the start position to (SPX+ΔX, SPY+ΔY), the ΔX part overflowing on the left side and the ΔY part overflowing on top can be displayed. At this time, the display position (PnDPXR*, PnDPYR*) is fixed at 0.

Note: * n = 1 to 8

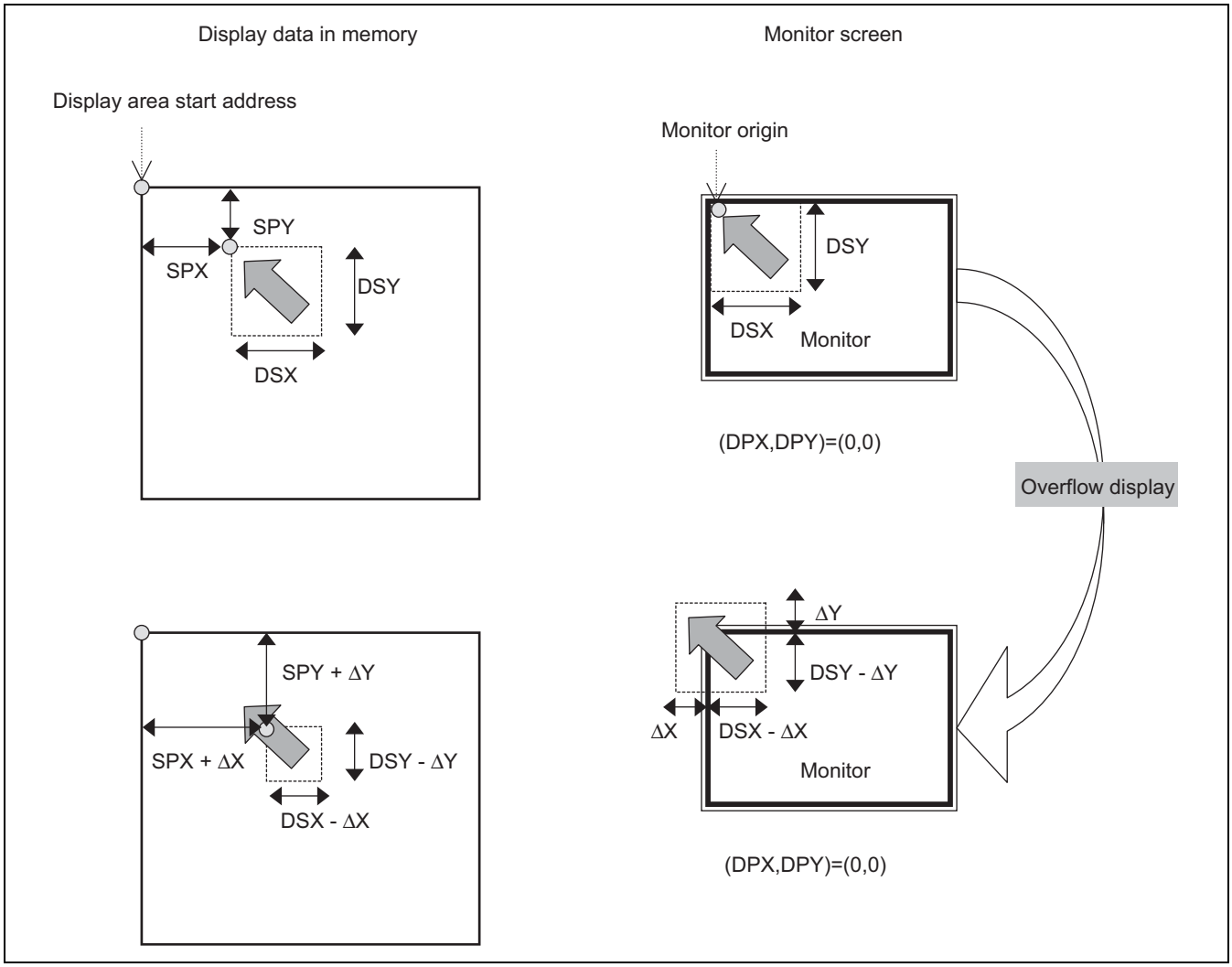


Figure 20.13 Schematic Diagram of Upper-Left Overflow Display

20.4.15 Double-Buffering Control

The double-buffering control of the display unit (DU) includes four types of functions, which are an auto rendering mode that does not switch the display until drawing is completed, a manual display change mode in which display or drawing switching is all controlled by software, an auto display change mode that realize blinking, and a video capture mode that is based on a frame ID of the video input (VIN) module.

In the case of auto rendering mode and manual display change mode, the display change is performed in frame units for non-interlaced and interlaced sync display, and in field units for interlaced sync & video display. In the case of auto display change mode, all switching is performed in field units. For video capture mode, all switching is performed in frame units.

Auto Rendering Mode: In auto rendering mode, display is not switched until drawing is completed. Even if drawing is not completed within a single frame period, drawing operation continues as it is.

Manual Display Change Mode: In manual display change mode, display frame switching and start of drawing are controlled by software. Display switching can either be performed by software using the PnDC* bit in PnMR*, or by setting the buffer 0 or buffer 1 start address in PnDSA0R* and PnDSA1R* indicated by the DFBn* bit in DSSR0.

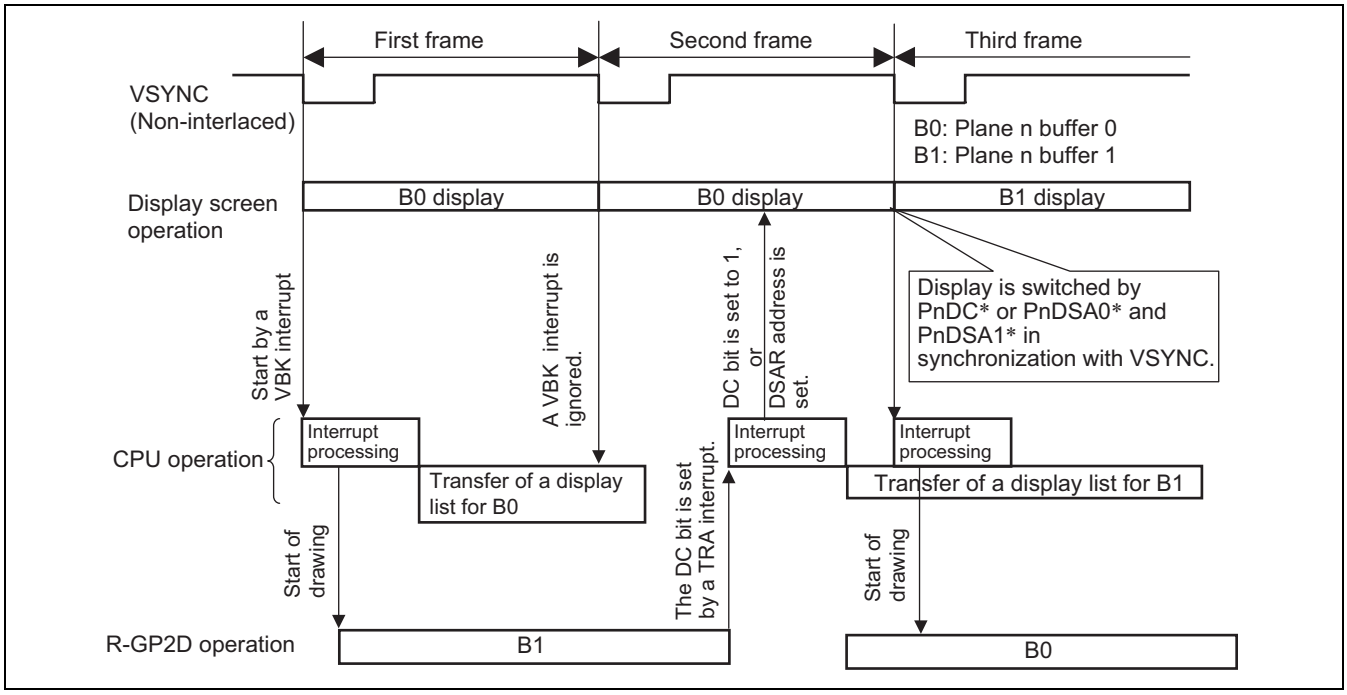


Figure 20.14 Manual Display Change Mode

Auto Display Change Mode: For information on the auto display change mode, refer to section 20.4.11, Blinking.

Video Capture Mode: In video capture mode, a display frame buffer is switched in frame units according to a frame ID, indicating the latest capture frame, output from the video input modules 0 to 1 (VIN0 to VIN1).

The video input modules 0 to 1 (VIN0 to VIN1) are selected by the PnVISL* bit in the plane n mode register (PnMR*).

Note: * n = 1 to 8

20.4.16 Sync Mode

In order to facilitate synchronization with external equipment, in addition to master mode, a TV synchronization function is provided. Selection of master mode and TV sync mode is performed using bits 7 and 6 in DSYSRn*. In master mode (internal sync mode), the position of the falling edge of the vertical sync signal (VSYNC) set by VSPRn* is detected. In TV sync mode (external sync mode), the position of the falling edge of the EXVSYNC signal is detected. The results are then reflected in the bits 14 and 11 of DSSRn*.

Master Mode (Internal Sync Mode): By setting the period and pulse width of the horizontal and vertical sync signals (HSYNC, VSYNC) in the display timing generation registers, the corresponding waveforms are output. Also, display data is output in sync with these signals.

In interlaced sync mode and interlaced sync & video mode, a signal is output to the ODDF pin indicating odd/even fields.

TV Sync Mode (External Sync Mode): In TV sync mode, display data is output in sync with a horizontal sync signal and vertical sync signal (EXHSYNC, EXVSYNC) input from a TV, video, or other external sync signal generation circuit. Display data is output with reference to the falling edge of the EXHSYNC signal and the rising edge of the EXVSYNC signal.

The horizontal sync signal, vertical sync signal, and clock signal from the external sync signal generation circuit are input to the EXHSYNC, EXVSYNC, and DCLKIN pins, respectively. CSYNC is at high level. In interlaced sync mode and interlaced sync & video mode, a signal should be input to the EXODDF pin indicating odd/even fields. In non-interlaced mode, the input to the EXODDF pin should be fixed at low level or at high level.

When operating the unit in TV sync mode also, values must be set in horizontal sync width register n (HSWRn*), horizontal cycle register n (HCRn*), vertical sync point register n (VSPRn*), and vertical cycle register n (VCRn*) in section 20.3.2, Display Timing Generation Registers.

When the EXVSYNC signal is input, either before or after completion of display of the display size portion set in the display unit (DU), the display unit (DU) performs vertical display completion operation and transitions to control for the next screen. When the EXVSYNC signal is not input, the unit continues to wait for the EXVSYNC signal while remaining in the vertical blanking interval (auto-control is not performed). Similarly, when the EXHSYNC signal is input the display unit (DU) performs horizontal display completion operation and transitions to control for the next raster line; but if the EXHSYNC signal is not input, the unit continues to wait for the EXHSYNC signal while remaining in the horizontal blanking interval (auto-control is not performed).

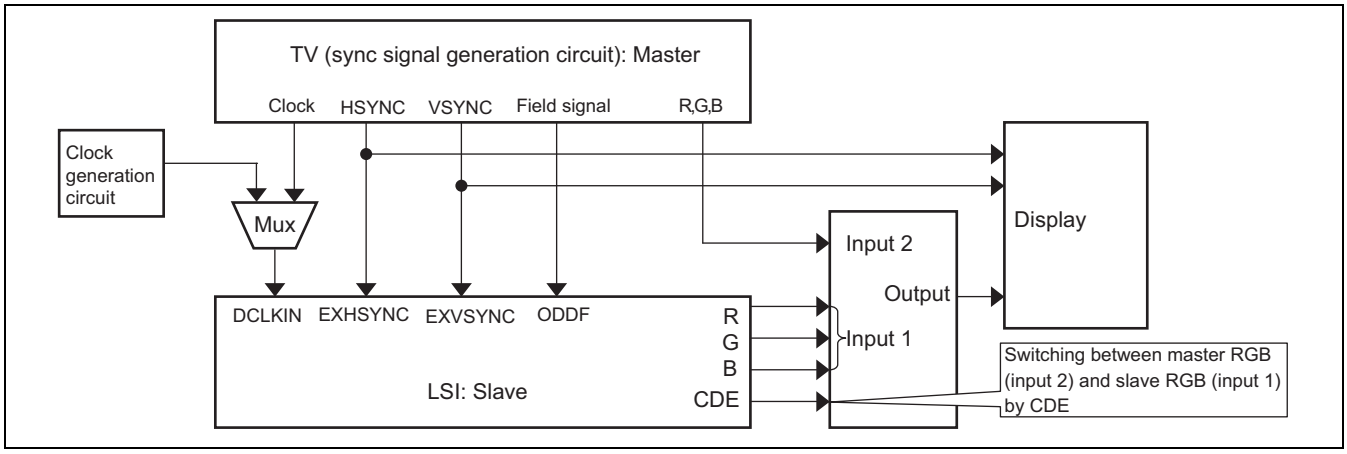


Figure 20.15 Signal Flow in TV Sync Mode

Sync Method Switching Mode: When switching from master mode into TV sync mode, or from TV sync mode into master mode, when necessary this mode should be switched into first. Even if a transition to this mode is not made first, switching of the synchronization method is possible.

In this mode, input/output pins connected to the display unit (DU) are for input, and so collision of pin signals can be avoided. Also, in this mode the internal dot clock is stopped, so that disorder in the input dot clock has no effect on display operation.

Note: * n = 0 and 1

20.4.17 Alpha-Ratio Planes

α blending can be performed by using the eight planes (display planes) that can display the current image data with the alpha ratio, plus two planes for the alpha ratio (alpha-ratio planes). Data in the alpha ratio planes are limited to the alpha ratio; they cannot be composed as display data.

To enable the alpha-ratio planes, set the AP1E or AP2E bit of DAPCR to 1. PnALPHAR* is used to select the alpha-ratio planes. Set the PnBRSL* bits in PnALPHAR* to B'111 and bits 2 to 0 in PnALPHA* to B'000, B'001 or B'010.

Notes: These alpha-ratio planes are not usable when 32-bit/pixel data are being displayed.
* n = 1 to 8

20.4.18 Display Capture

In display capture, display data (RGB888 or RGB666) that have been composed for output on the relevant pins are converted to ARGB888, RGB565 or ARGB1555 data, stored in a buffer having the same configuration as the read buffer, and then stored in the area specified by DCnSAR* via AXI. To capture the display data, set the DCE or DC2E bit of DCPCR to 1. Capturing starts from the next frame after this setting has been made. The specifications for display capturing are as follows:

Data formats: Refer to Table 20.31, Output Data Format. In the case of ARGB1555, the A value is determined by the setting of DCPCR. In the case of ARGB8888, the A value is determined by the setting of DCnMR.

Capture area start address: Only a single address can be specified.

Capture size X: The same as the monitor size (horizontal display end position (HDE) – horizontal display start position (HDS)

Capture size Y: The same as the monitor size (vertical display end position (VDE) – vertical display start position (VDS)

Memory width X: Specified by a register. Writing to the buffer ends when the memory width is exceeded.

Memory length Y: Specified by a register. Storage of data in the memory ends when the memory length (in lines) is exceeded.

When the following display functions are set, the display capture function cannot be used.

- RGB-YC conversion performed by setting the RGBYC0 bits in the display unit extensional function control 5 register (DEF5R)

Note: * n = no number or 2.

20.4.19 Dual Display Output

The display unit (DU) has superposition processors, display-timing generators, pin controllers, and dot-clock generators, each of which is independently controllable. The DU0 and DU1 realize various types of display because two channels are available for selecting from among the eight display planes and two alpha-ratio planes.

This section describes the dual display output using the DU0 and DU1.

(1) Independent Display

Different images can be displayed with different sizes by specifying different superposition processors, display-timing generators, pin controllers, and dot-clock generators. Captured video data can also be separately stored.
However, separate output images cannot be produced from a single plane. To display a single set of image data in separate output images, two planes must be used.
It is impossible to output the image data only via the LVDS pins or DVENC pins since they both are only one channel available for each. Combination of both digital RGB pins, digital RGB pins and LVDS pins, digital RGB pins and DVENC pins, LVDS pins and DVENC pins can be used.

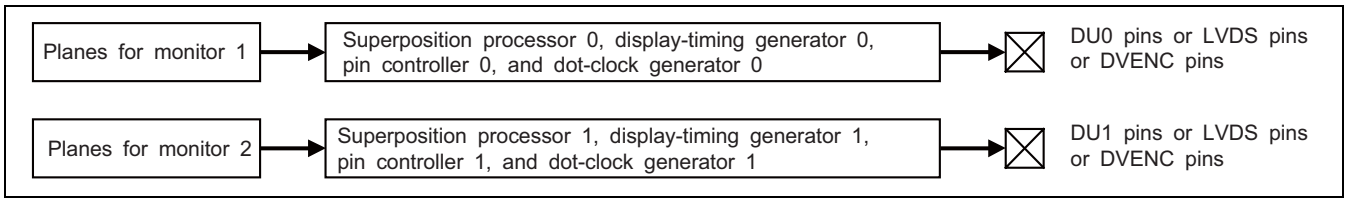


Figure 20.16 Independent Display

(2) Display of Different Images on Monitors of the Same Size

Different images can be displayed on monitors of the same size when the same display-timing generator and dot-clock generator have been specified but the superposition processors and pin controllers are different. Captured video data can also be separately stored.

Images can be output to two monitors through a single set of pins by switching the display data in synchronization with the output dot clock. Output through two sets of pins is also possible.

When images are output to two monitors through a single set of pins, the image data can be output only via the digital RGB or LVDS.

When images are output through two sets of pins, it is impossible to output the image data only via the LVDS pins; the image data is output only via the digital RGB pins or via both the LVDS pins and digital RGB pins.

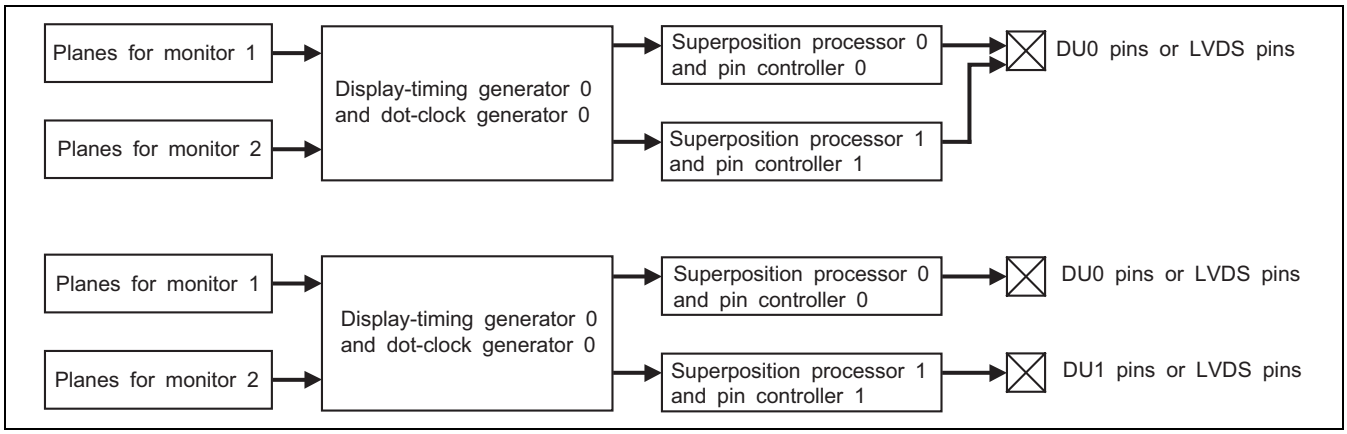


Figure 20.17 Display of Different Images on Monitors of the Same Size

(3) Display of the Same Image on Monitors of the Same Size

The same image can be displayed on different monitors when the same superposition processor, display-timing generator, and dot-clock generator have been specified but the pin controllers are different.

Images can be output to two monitors through a single set of pins by switching the display data in synchronization with the output dot clock. Output through two sets of pins is also possible.

When images are output to two monitors through a single set of pins, the image data can be output only via the digital RGB.

When images are output through two sets of pins, it is impossible to output the image data only via the LVDS pins; the image data is output via both the LVDS pins and digital RGB pins

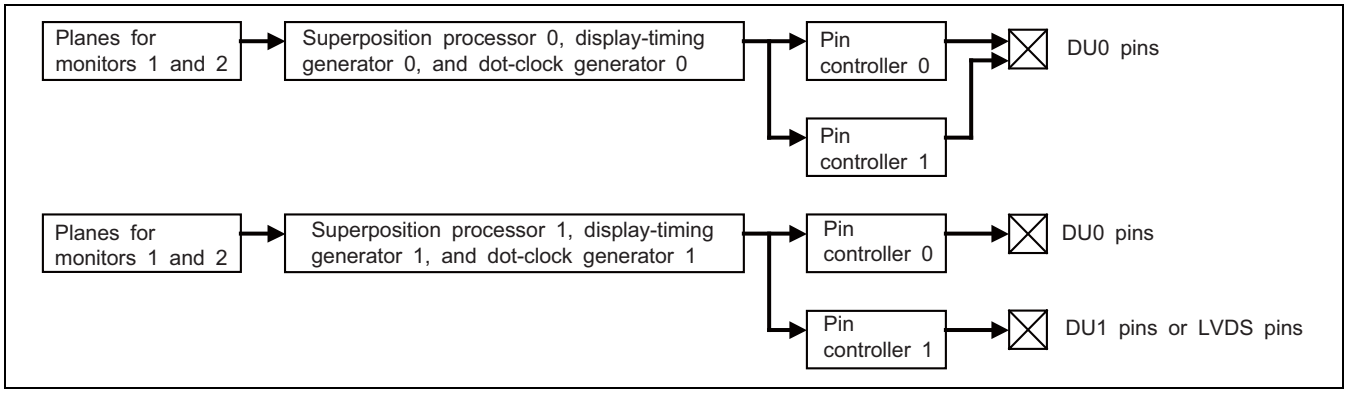


Figure 20.18 Display of the Same Image on Monitors of the Same Size

The timing for switching of display data in synchronization with the output dot clock is shown below. This feature is only supported by DU0 or DU0 via LVDS.

With the DU1 pin, data cannot be displayed by switching in synchronization with the output dot clock. For switching display data in synchronization with the output dot clock, the output dot clock should be set to be division by two or more of the input dot clock.

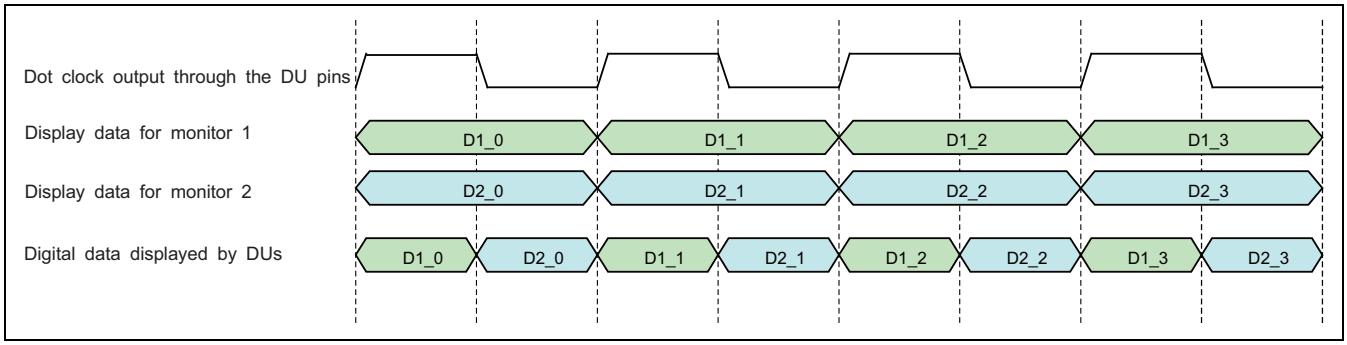


Figure 20.19 Switching Display Data in Synchronization with the Output Dot Clock

(4) Combinations of Blocks for Dual Display Output

For dual display output, the dot clock to be supplied to blocks in the display unit (DU), timing signals including SYNC, and display data are specifiable by setting the corresponding registers. Table 20.35 is a matrix of the combinations of blocks, and Table 20.36 gives the meanings of the symbols used in Table 20.35.

When the input block is superposition processor 0, for example, the information indicated in the table is as follows.

- The dot clock is that from dot-clock generator 0 or 1 as selected by the DR0D and DK1S bits of DORCR (No. 5 in the table).
- The timing signal is that from display-timing generator 0 or 1 as selected by the DR0D and PG1T bits of DORCR (No. 3 in the table).
- The planes for superpositioning of data are selected in DS0PR (No. 15 in the table).

Take care with register settings because timing signals such as the dot clock, sync signals and so on are freely specifiable, but if the dot clock or other timing signals differ from block to block, a normal display will not be possible.

Table 20.35 Combinations of Blocks

		Output Block															
		Dot-clock generator 0(clock)	Dot-clock generator 0 (external SYNC)	Dot-clock generator 1 (clock)	Dot-clock generator 1 (external SYNC)	Display-timing generator 0	Display-timing generator 1	Superposition processor 0	Superposition processor 1	Pin controller (output timing adjustment) 0	Pin controller (output timing adjustment) 1	Planes 1 to 8	Alpha-ratio planes 1 to 2	Display capture 1	Display capture 2	DU0 pins	DU1 pins
Input Block	Dot-clock generator 0 (clock)		—	—	—	—	—	—	—	—	—	—	—	—	—	✓	—
	Dot-clock generator 0 (external SYNC)	—		—	—	—	—	—	—	—	—	—	—	—	—	✓	—
	Dot-clock generator 1 (clock)	—	—		—	—	—	—	—	—	—	—	—	—	—	—	✓
	Dot-clock generator 1 (external SYNC)	—	—	—		—	—	—	—	—	—	—	—	—	—	—	✓
	Display-timing generator 0	✓	✓	—	—		—	—	—	—	—	—	—	—	—	—	—
	Display-timing generator 1	1	—	1	✓	—		—	—	—	—	—	—	—	—	—	—
	Superposition processor 0	4	—	4	—	2	2		—	—	—	13	△	—	—	—	—
	Superposition processor 1	5	—	5	—	3	3	—		—	—	14	△	—	—	—	—
	Pin controller (output timing adjustment) 0	✓	—	—	—	✓	—	6	6		—	—	—	—	—	—	—
	Pin controller (output timing adjustment) 1	1	—	1	—	8	8	7	7	—		—	—	—	—	—	—
	Planes 1 to 8	9	—	9	—	10	10	—	—	—	—		—	—	—	—	—
	Alpha-ratio planes 1 to 2	11	—	11	—	12	12	—	—	—	—	—		—	—	—	—
	Display capture 1	4	—	4	—	2	2	✓	—	—	—	—	—		—	—	—
	Display capture 2	5	—	5	—	3	3	—	✓	—	—	—	—	—		—	—
	DU0 pins	—	—	—	—	—	—	—	—	✓	—	—	—	—	—		—
	DU1 pins	—	—	—	—	—	—	—	—	—	✓	—	—	—	—	—	

Table 20.36 Meanings of Symbols and Numbers

Symbol or No.	Register Name	Bit Name	Description
✓	—	—	One-to-one combination
—	—	—	No combination
△	—	—	Depends on the values in DS0PR, DS1PR, and PnALPHAR*.
1	Display unit output route control register (DORCR)	DK1S	0: Dot-clock generator 0 (clock) 1: Dot-clock generator 1 (clock)
2	Display unit output route control register (DORCR)	PG0D PG1T	Other than 01_1: Display-timing generator 0 01_1: Display-timing generator 1
3	Display unit output route control register (DORCR)	PG0D PG1T	Other than 00_1: Display-timing generator 0 00_1: Display-timing generator 1
4	Display unit output route control register (DORCR)	PG0D DK1S	Other than 01_1: Dot-clock generator 0 (clock) 01_1: Dot-clock generator 1 (clock)
5	Display unit output route control register (DORCR)	PG0D DK1S	Other than 00_1: Dot-clock generator 0 (clock) 00_1: Dot-clock generator 1 (clock)
6	Display unit output route control register (DORCR)	PG0D	00: Superposition processor 0 01: Superposition processor 1 10: Fixed to 0 11: The value of DOOR0
7	Display unit output route control register (DORCR)	PG1D	00: Superposition processor 0 01: Superposition processor 1 10: Fixed to 0 11: The value of DOOR1
8	Display unit output route control register (DORCR)	PG1T	0: Display-timing generator 0 1: Display-timing generator 1
9	Display unit plane timing select register (DPTSR)	P1DK to P8DK	0: Dot-clock generator 0 (clock) 1: Dot-clock generator 1 (clock)
10	Display unit plane timing select register (DPTSR)	P1TS to P8TS	0: Display-timing generator 0 1: Display-timing generator 1
11	Display unit alpha-ratio plane timing select register (DAPTSR)	AP1DK to AP2DK	0: Dot-clock generator 0 (clock) 1: Dot-clock generator 1 (clock)
12	Display unit alpha-ratio plane timing select register (DAPTSR)	AP1TS to AP2TS	0: Display-timing generator 0 1: Display-timing generator 1
13	Display superimpose 0 priority register (DS0PR)	—	See the description of DS0PR.
14	Display superimpose 1 priority register (DS1PR)	—	See the description of DS1PR.

Note: * n = 1 to 8

20.4.20 Divided YUV Display

An image that has been divided up into separate Y and UV data for separate storage in memory can be displayed as YUV422 or YUV420 data by using two planes.

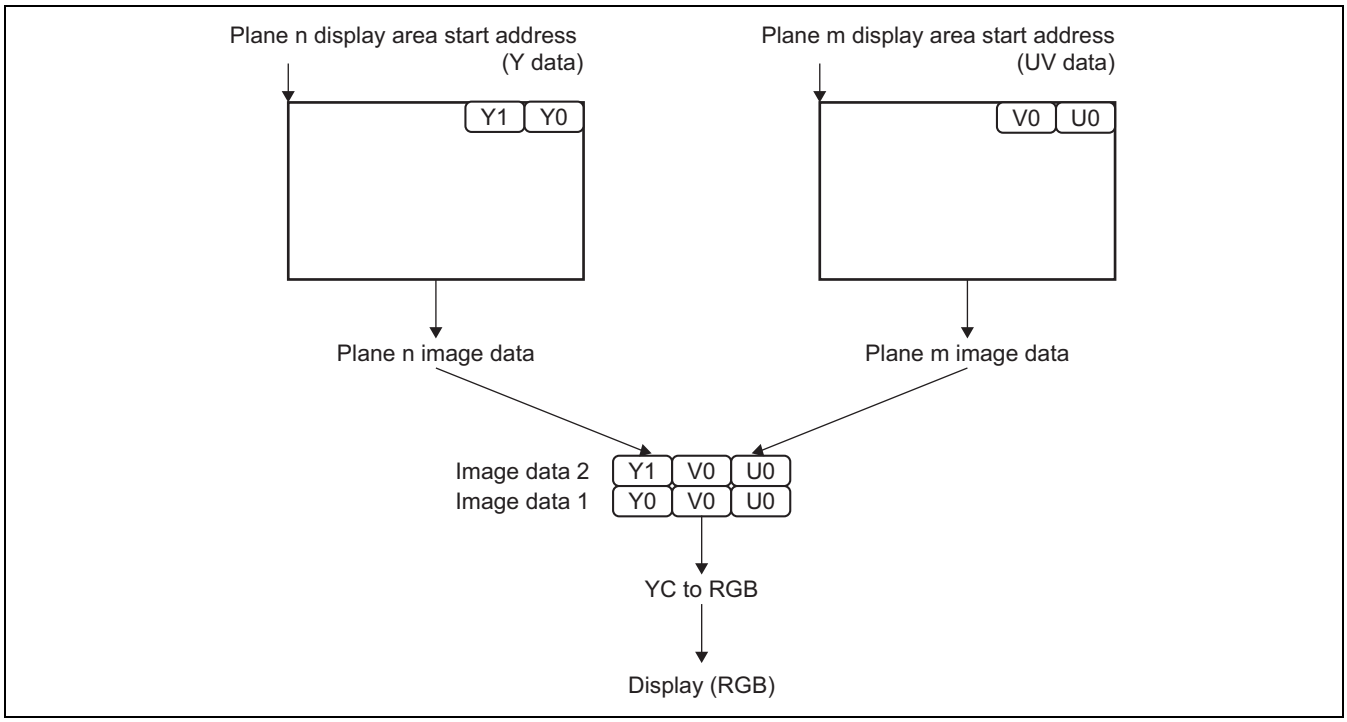


Figure 20.20 Overview of Divided YUV Display Function (Little Endian)

(1) Image Data Format

The following figures show the configuration of YUV422 data divided for separate storage in little endian in memory. The configuration of YUV420 data is the same as that shown in section 20.4.5 (5), YC: YUV420.

The formulae for YC-RGB conversion are the same as those shown in section 20.4.5 (4), YC: YUV422.

(a) Y data

	31	24	23	16
D31 to D16 Image data 4 and 3	Y3		Y2	

	15	8	7	0
D15 to D0 Image data 2 and 1	Y1		Y0	

(b) UV data

	31	24	23	16
D31 to D16 Image data 4 and 3	V2		U2	

	15	8	7	0
D15 to D0 Image data 2 and 1	V0		U0	

(2) Register Setting Examples

Two planes are used to display the divided YUV data. The methods for specifying Y data in plane 1 and UV data in plane 2 to display the divided YUV data are described below.

1. The following is the setting made by the plane n display data control 2 register (PnDDC2R[*1]).

YUV422 data

Bit :	7	6	5	4	3	2	1	0
			PnNV21	PnY420			PnDIVU	PnDIVY
Plane 1 (Y data)	–	–	0	0	–	–	0	1
Plane 2 (UV data)	–	–	0	0	–	–	1	0

YUV420 data

Bit :	7	6	5	4	3	2	1	0
			PnNV21	PnY420			PnDIVU	PnDIVY
Plane 1 (Y data)	–	–	0	0	–	–	0	1
Plane 2 (UV data)	–	–	0/1	1	–	–	1	0

2. Set the start address of Y data in the plane 1 display area start address 0 to 2 registers (P1DSA0R to P1DSA2R).
3. Set the start address of UV data in the plane 2 display area start address 0 to 2 registers (P2DSA0R to P2DSA2R).
4. The same settings should be made in the plane 1 and plane 2 registers of display plane registers other than the registers described above (PnDDC2R*[1], P1DSA0R to P1DSA2R, and P2DSA0R to P2DSA2R). Set the PnDDF[*1] bits in the plane n mode register (PnMR[*1]) to B'11.
5. Set bit 20 in the display unit system control register n (DSYSRn[*2]) to 1 if data is stored in big endian in memory.
6. Turn on the display of planes 1 and 2, and give plane 2 the next order of priority for processing after plane 1. For details on turning on the display, see section 20.4.2, Display On/Off.

(3) Combinations of Planes

Display as YUV422 or YUV420 data is obtained by using the combinations of planes listed below. UV data should be on the plane immediately below that for the Y data.

Table 20.37 Possible Combinations of Planes

Y Data Obtained by Dividing up YUV	UV Data Obtained by Dividing up YUV
Plane 1	Plane 2
Plane 2	Plane 3
Plane 3	Plane 4
Plane 4	Plane 5
Plane 5	Plane 6
Plane 6	Plane 7
Plane 7	Plane 8
Plane 8	Plane 1

Notes: 1. n = 1 to 8
2. n = 0 and 1.

20.4.21 Multiple Output Display

The 24-bit data of the DU0/DU1 display digital data (RGB888) can be multiplexed 12 bits each and output. For a DU0 multiple output, set both the MLOS0 bit in display unit extensional function control 6 register (DEF6R) and the DCKOINV bit in the external synchronization control register 0 (ESCR0) to 1. For a DU1 multiple output, set both the MLOS1 bit in display unit extensional function control 6 register (DEF6R) and the DCKOINV bit in the external synchronization control register 1(ESCR1) to 1.

The output dot clock should be set so that its frequency is equal to or smaller than half of the input dot clock frequency. The pin functions for a multiple output display are shown in Table 20.38.

Figure 20.21 shows the timing of the output dot clock, display control signal, and display digital data. The display control signal is output in synchronization with the falling edge of the output dot clock. As for display digital data, the Df data (Table 20.38) is output in synchronization with the falling edge of the output dot clock and the Dr data (Table 20.38) is output in synchronization with the rising edge.

Table 20.38 Pin Functions of Multiple Output Display

	DU0 Display Digital Data	
Pin Name	**Df Data**	**Dr Data**
DU0_DR0	DU0 digital red 0	DU0 digital green 4
DU0_DR1	DU0 digital red 1	DU0 digital green 5
DU0_DR2	DU0 digital red 2	DU0 digital green 6
DU0_DR3	DU0 digital red 3	DU0 digital green 7
DU0_DR4	DU0 digital red 4	DU0 digital blue 0
DU0_DR5	DU0 digital red 5	DU0 digital blue 1
DU0_DR6	DU0 digital red 6	DU0 digital blue 2
DU0_DR7	DU0 digital red 7	DU0 digital blue 3
DU0_DG0	DU0 digital green 0	DU0 digital blue 4
DU0_DG1	DU0 digital green 1	DU0 digital blue 5
DU0_DG2	DU0 digital green 2	DU0 digital blue 6
DU0_DG3	DU0 digital green 3	DU0 digital blue 7

	DU1 Display Digital Data	
Pin Name	**Df Data**	**Dr Data**
DU1_DR0	DU1 digital red 0	DU1 digital green 4
DU1_DR1	DU1 digital red 1	DU1 digital green 5
DU1_DR2	DU1 digital red 2	DU1 digital green 6
DU1_DR3	DU1 digital red 3	DU1 digital green 7
DU1_DR4	DU1 digital red 4	DU1 digital blue 0
DU1_DR5	DU1 digital red 5	DU1 digital blue 1
DU1_DR6	DU1 digital red 6	DU1 digital blue 2
DU1_DR7	DU1 digital red 7	DU1 digital blue 3
DU1_DG0	DU1 digital green 0	DU1 digital blue 4
DU1_DG1	DU1 digital green 1	DU1 digital blue 5
DU1_DG2	DU1 digital green 2	DU1 digital blue 6
DU1_DG3	DU1 digital green 3	DU1 digital blue 7

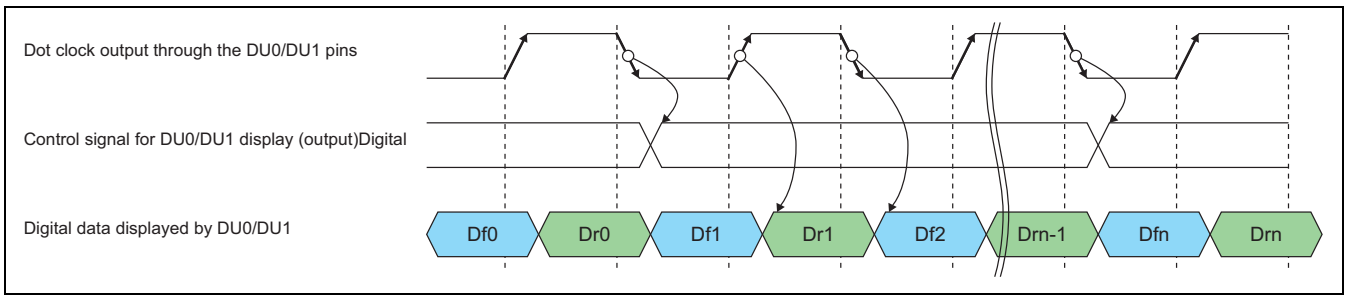


Figure 20.21 Multiple Output Display Timing

20.4.22 YC Format Display

In addition to RGB format display, data stored in YC format can be displayed unmodified in YC format. RGB format display data can also be RGB-YC converted and displayed as YC format. Data stored in YC format cannot be superpositioned; however, different planes can be displayed on the different display areas in the divided screen.

In DU1, to display data stored in YC format unmodified in YC format, select YC format rather than RGB format by setting bits 9 and 8 in the display unit extended function control register 1 (DEFR1). Bits 9 and 8 setting of B'10 selects 16-bit YC format display (non-multiplexed), and a setting of B'11 selects 8-bit YC format display (multiplexed). A setting of B'00 selects RGB format.

In DU0, to use RGB-YC conversion for YC format display, set the RGBYC0 bits in display unit extended function control 5 register (DEF5R). A RGBYC0 setting of B'10 selects 18-bit display (non-multiplexed), and a setting of B'01 selects 10-bit display (multiplexed).

When YC format is displayed by the timing as shown in Figure 20.22 and Figure 20.23, input 2 clocks to DCLKIN and specify division by 2. Also output 2 clocks from DCLKOUT. Both 2 clocks output and division by 2 are specified by settings in the external synchronization control register n (ESCRn*2). Non-multiplexed YC format can be displayed in Figure 20.22a and Figure 20.22b, this setting is not required.

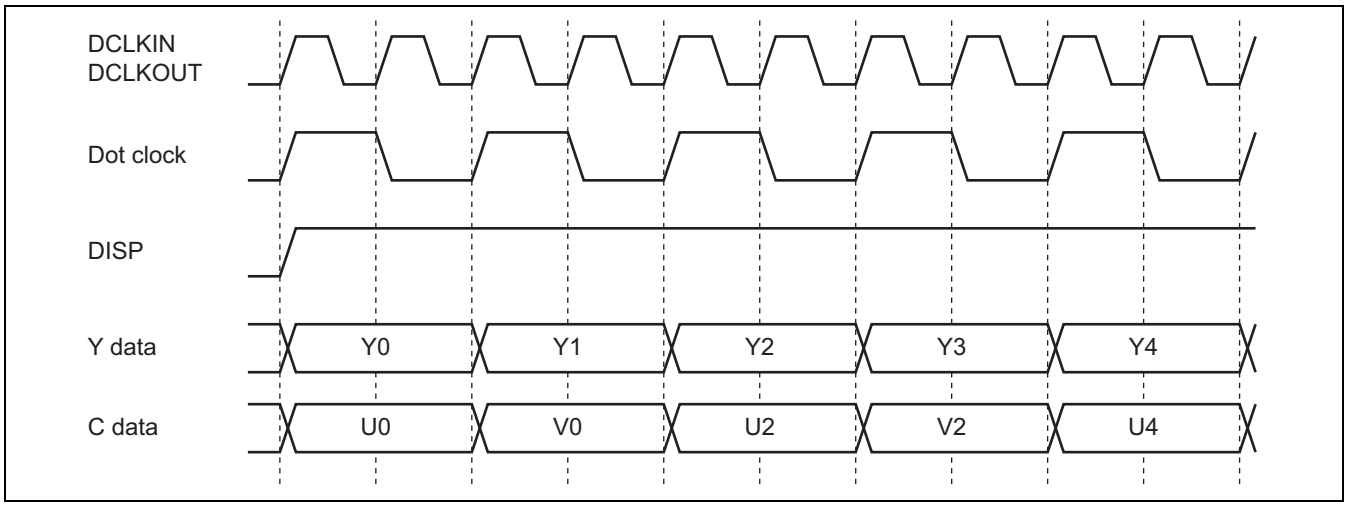


Figure 20.22 YC Non-Multiplexed

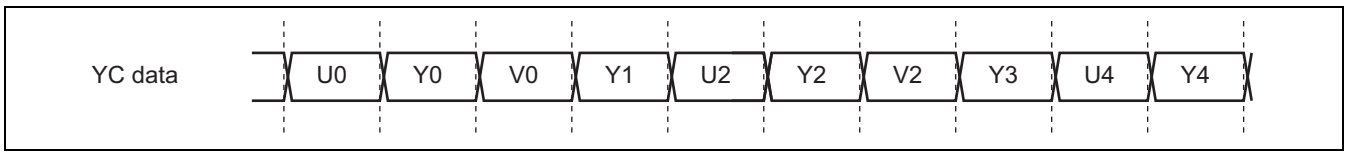


Figure 20.23 YC Multiplexed

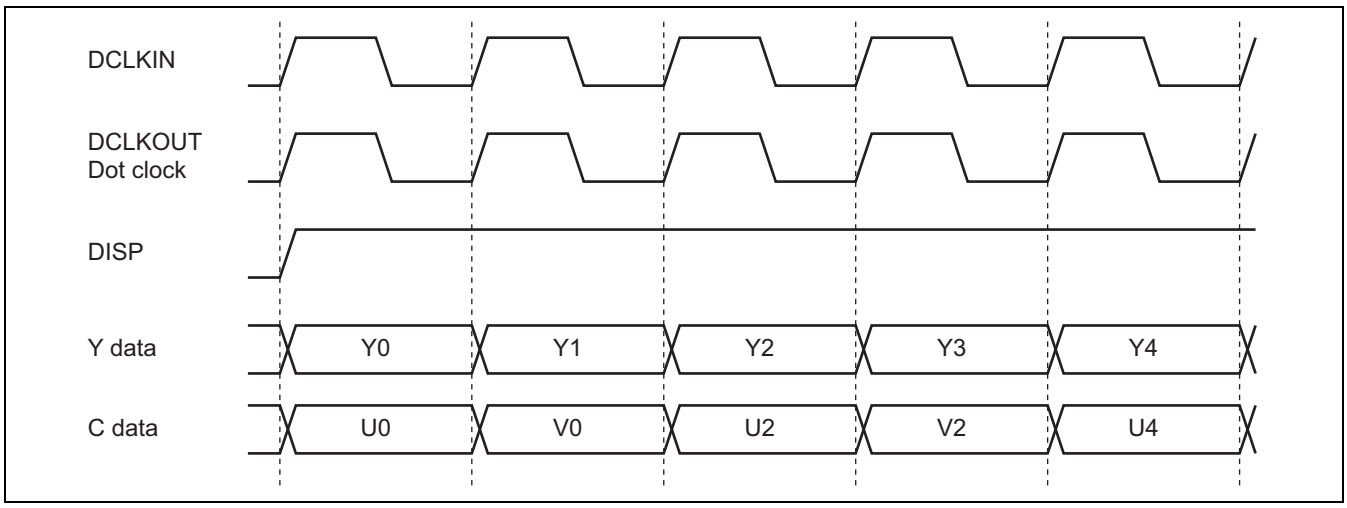


Figure 20.22a YC Non-Multiplexed (no division)

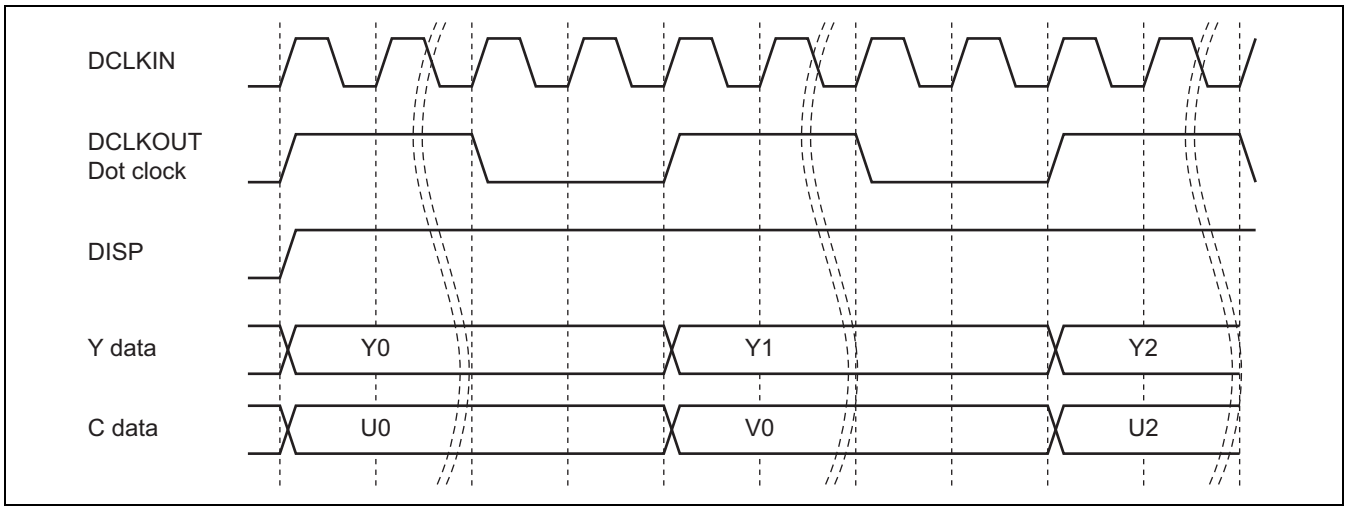


Figure 20.22b YC Non-Multiplexed (division by x)

Table 20.39 Pin Names and YC Data for YC Format Display

		YC Format Display (Only for DU1 Pin)		RGB-YC Conversion Display (Only for DU0 Pin)	
DU0 Pin Name	**DU1 Pin Name**	**Non-Multiplexed**	**Multiplexed**	**Non-Multiplexed**	**Multiplexed**
DU0_DR2	DU1_DR2	Y2	Y2, C2	Y4	Y4, C4
DU0_DR3	DU1_DR3	Y3	Y3, C3	Y5	Y5, C5
DU0_DR4	DU1_DR4	Y4	Y4, C4	Y6	Y6, C6
DU0_DR5	DU1_DR5	Y5	Y5, C5	Y7	Y7, C7
DU0_DR6	DU1_DR6	Y6	Y6, C6	Y8	Y8, C8
DU0_DR7	DU1_DR7	Y7	Y7, C7	Y9	Y9, C9
DU0_DG2	DU1_DG2	C6	—	C8	—
DU0_DG3	DU1_DG3	C7	—	C9	—
DU0_DG4	DU1_DG4	—	—	Y0	Y0, C0
DU0_DG5	DU1_DG5	—	—	Y1	Y1, C1
DU0_DG6	DU1_DG6	Y0	Y0, C0	Y2	Y2, C2
DU0_DG7	DU1_DG7	Y1	Y1, C1	Y3	Y3, C3
DU0_DB2	DU1_DB2	C0	—	C2	—
DU0_DB3	DU1_DB3	C1	—	C3	—
DU0_DB4	DU1_DB4	C2	—	C4	—
DU0_DB5	DU1_DB5	C3	—	C5	—
DU0_DB6	DU1_DB6	C4	—	C6	—
DU0_DB7	DU1_DB7	C5	—	C7	—

20.4.23 RGB → YC Color Space Conversion Formula

The formulae for RGB-YC conversion are given below. The underlined coefficients are defined by the settings in the corresponding registers.

$$Y = YCLRP \times R + YCLGP \times G + YCLBP \times B + YCLAP$$
$$Cb = CBCLRP \times R + CBCLGP \times G + CBCLBP \times B + CBCLAP$$
$$Cr = CRCLRP \times R + CRCLGP \times G + CRCLBP \times B + CRCLAP$$

Values to be set for full scale to ITU-R BT.601 conversion are as follows.

$$Y = 0.257 \times R + 0.504 \times G + 0.098 \times B + 16$$
$$Cb = -0.148 \times R - 0.291 \times G + 0.439 \times B + 128$$
$$Cr = 0.439 \times R - 0368 \times G - 0.071 \times B + 128$$

Values to be set for full scale to full scale conversion are as follows.

$$Y = 0.299 \times R + 0.587 \times G + 0.114 \times B + 0$$
$$Cb = -0.169 \times R - 0.331 \times G + 0.550 \times B + 128$$
$$Cr = 0.500 \times R - 0419 \times G - 0.081 \times B + 128$$

20.5 Display Control

20.5.1 Display Timing Generation

In the display unit (DU), display timing is generated for the horizontal direction and vertical direction of the display screen. Display timing is set by using display timing generation registers in section 20.3.2. Figure 20.24 shows the display timing in non-interlaced mode. Here, the display screen is defined in terms of the variables of Table 20.40.

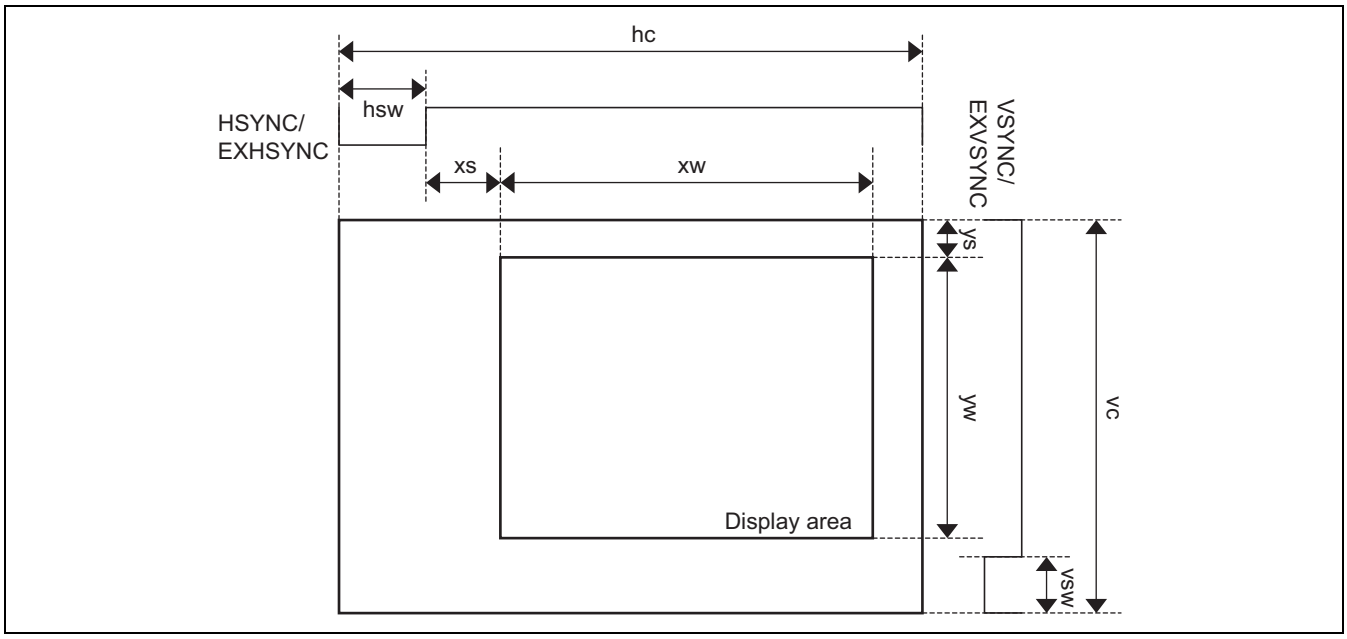


Figure 20.24 Display Timing Generation for Horizontal Direction and Vertical Direction of Display Screen

Table 20.40 Variables Defined in Display Screen

Variables	Contents	Units
hc*1	Horizontal scan period	Dot clock
hsw	Horizontal sync pulse width	Dot clock
xs	From rise of HSYNC to display start position in the horizontal direction of the display screen	Dot clock
xw	Display width per 1 raster of display screen	Dot clock
vc*2	Vertical scan period	Raster line
vsw	Vertical sync pulse width	Raster line
ys	From rise of VSYNC to display start position in the vertical direction of the display screen	Raster line
yw	Vertical display period of display screen	Raster line

Notes: 1. Should be set such that hsw + xs + xw < hc
2. Should be set such that vsw + ys + yw < vc

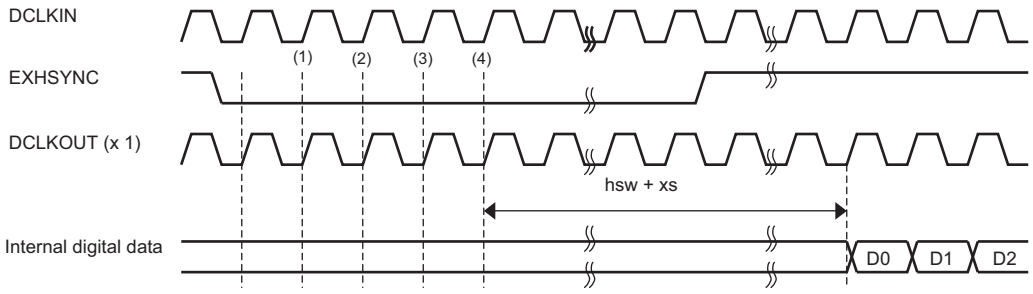
The display timing generation register settings are different depending on the scan method and synchronization method. Hence the value of the display timing generation registers should be set after performing calculations like those indicated in Table 20.41.

Table 20.41 Correspondence Table of Settings of Display Timing Generation Registers

		Synchronization Method	
Register Name	**Bit Name**	**Master Mode**	**TV Sync Mode**
Horizontal display start register n (HDSRn)	HDS	hsw + xs – 19*5, (hsw + xs – 19 – 1 when DVENC is used)	hsw + xs - 25*2*5
Horizontal display end register n (HDERn)	HDE	hsw + xs – 19*5 + xw, (hsw + xs – 19 – 1 + xw when DVENC is used)	hsw + xs – 25 + xw*2*5
Vertical display start register n (VDSRn)	VDS	ys – 2*3	ys – 2*3
Vertical display end register n (VDERn)	VDE	ys – 2 + yw	ys – 2 + yw
Horizontal synch width register n (HSWRn)	HSW	hsw – 1	hsw – 1
Horizontal cycle register n (HCRn)	HC	hc – 1	hc – 1
Vertical synch point register n (VSPRn)	VSP	vc – vsw – 1	vc – vsw – 1
Vertical cycle register n (VCRn)	VC	vc – 1	vc – 1

Notes: n = 0 and 1

1. In all scan modes, VDS, VDE, VSP, VC settings are in single-field units.
2. The values of HDS and HDE are from the fourth rising edge of DCLKOUT after detection of the falling edge of EXHSYNC through the rising edge of DCLKOUT.



3. VDS should be set to 1 or greater.
4. HC should be set so as to satisfy HC > HDE.
5. If the function below is used, the following correction value is subtracted from both HDS and HDE in Table 20.41.

When using the RGB-YC conversion function (RGBYC0 or RGBYC1 bits in the display unit extensional function control 5 register (DEF5R) are set to 1), 3 should be subtracted.

20.5.2 CSYNC

In master mode, a CSYNC (composite sync) signal is output. EQWRn* is used to set the low-level pulse width of the CSYNC equivalent pulse. SPWRn* is used to set the low-level pulse width of the CSYNC serration pulse.

The CSYNC waveform is selected using the CSY bit in DSMRn*.

Note: * n = 0 and 1

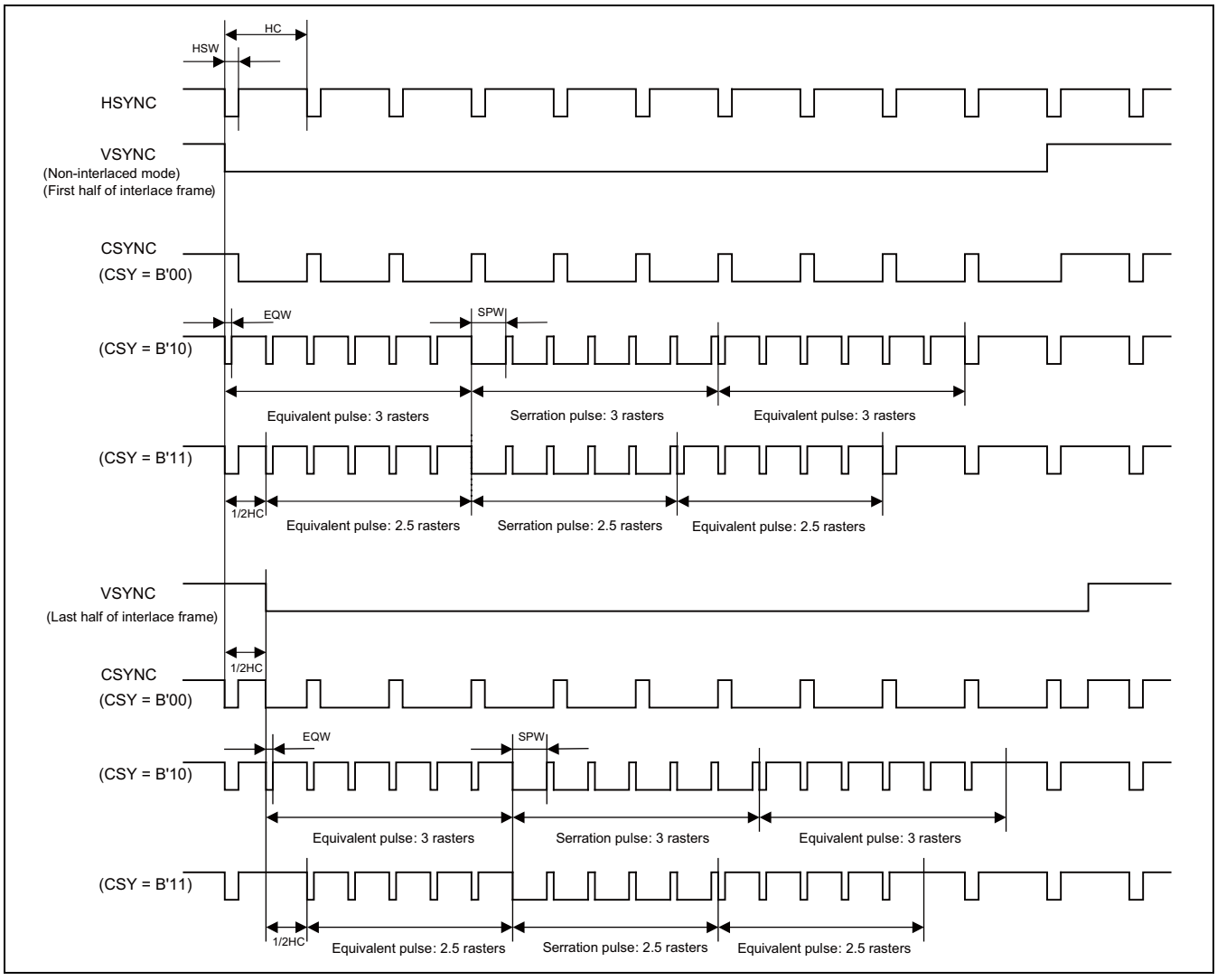


Figure 20.25 CSYNC Timing Chart

20.5.3 Scan Method

The scan method can be selected from among non-interlaced mode, interlaced sync mode, and interlaced sync & video mode. The mode is selected using bit 5 and bit 4 in DSYSRn*.

- Non-interlaced mode
  In this scan method, one frame consists of a single field.
- Interlaced sync mode
  In this scan method, one frame consists of two fields. The two fields are an even field and an odd field, displaying the same data.
- Interlaced sync & video mode
  In this scan method, one frame consists of two fields. The two fields are an even field and an odd field, displaying different data.

The ODEV bit in DSMRn* is used to set the display order of fields in interlaced sync mode and in interlaced sync & video mode. When the ODEV bit is 0, the display order for one frame is odd field, then even field; when the ODEV bit is 1, the order for one frame is even field, then odd field.

In master mode, high level is output from the ODDF pin during even field display, and low level is output during odd field display. In TV sync mode, high level is input to the EXODDF pin to cause display of the even field, and low level is input to cause display of the odd field.

Note: When non-interlaced mode is selected in TV sync mode, the EXODDF pin should be fixed at low level or high level.

* n = 0 and 1.

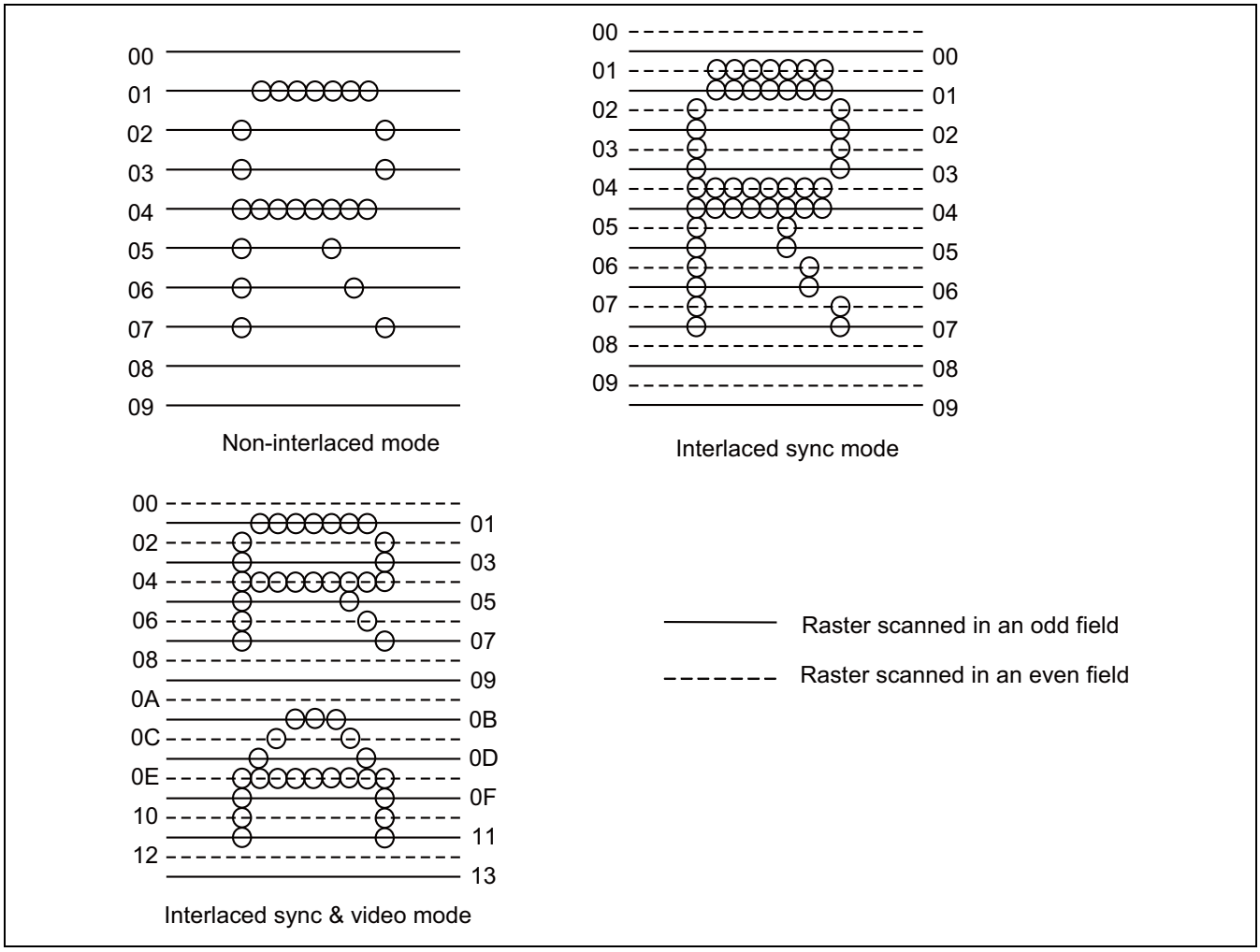


Figure 20.26 Example of Display in Each Scan Mode

- Example of vertical scan period
  Non-interlaced mode: 1/60 second/field, 1/30 second/field
  Interlaced sync mode: 1/30 second/frame
  Interlaced sync & video mode: 1/30 second/frame
- Display in non-interlaced method
  In this method, all lines are displayed at once without providing intervals between input video signals.
  This input method is for monitors capable of high-resolution display.

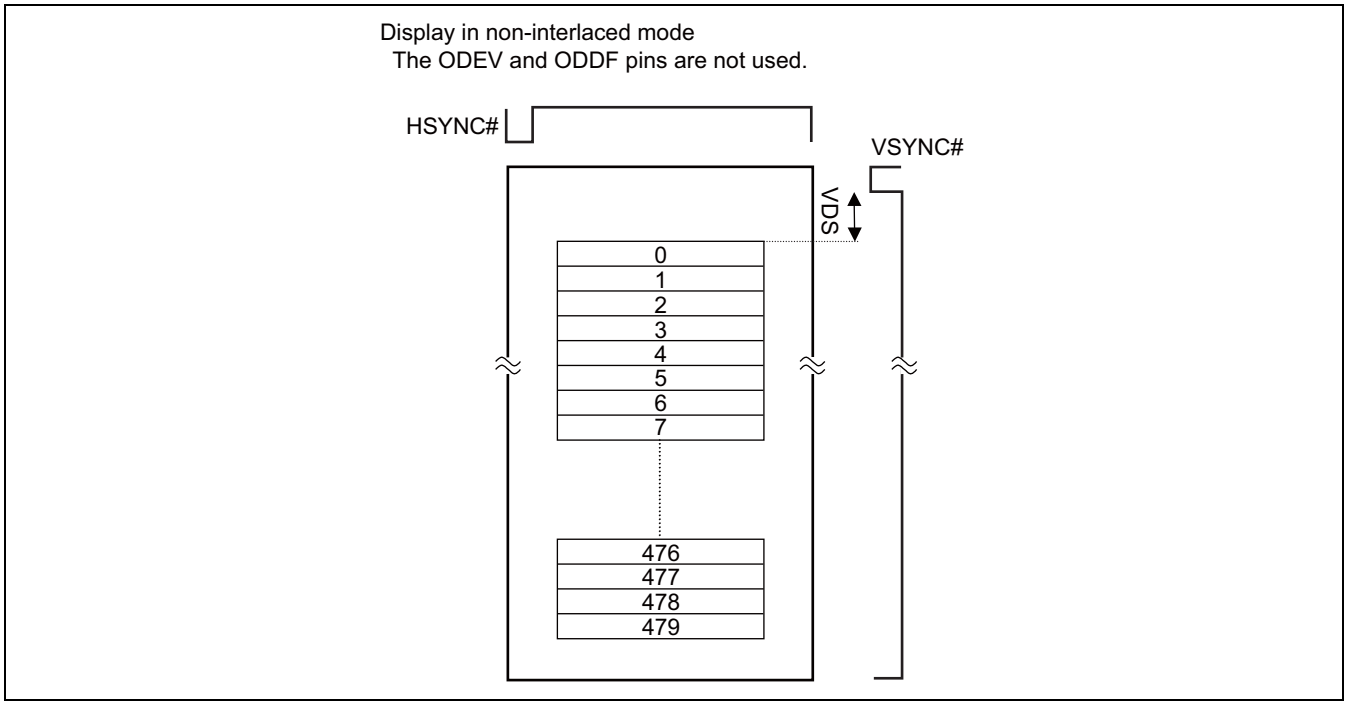


Figure 20.27 Display in Non-Interlaced Method

- Display in interlaced method

  At every scan period VC of the input video signal, even lines and odd lines are switched and displayed in alternation, and a single screen (one frame) is combined and displayed (with the afterimage of the preceding VC) with a period of 2VC. This is a basic TV input method.

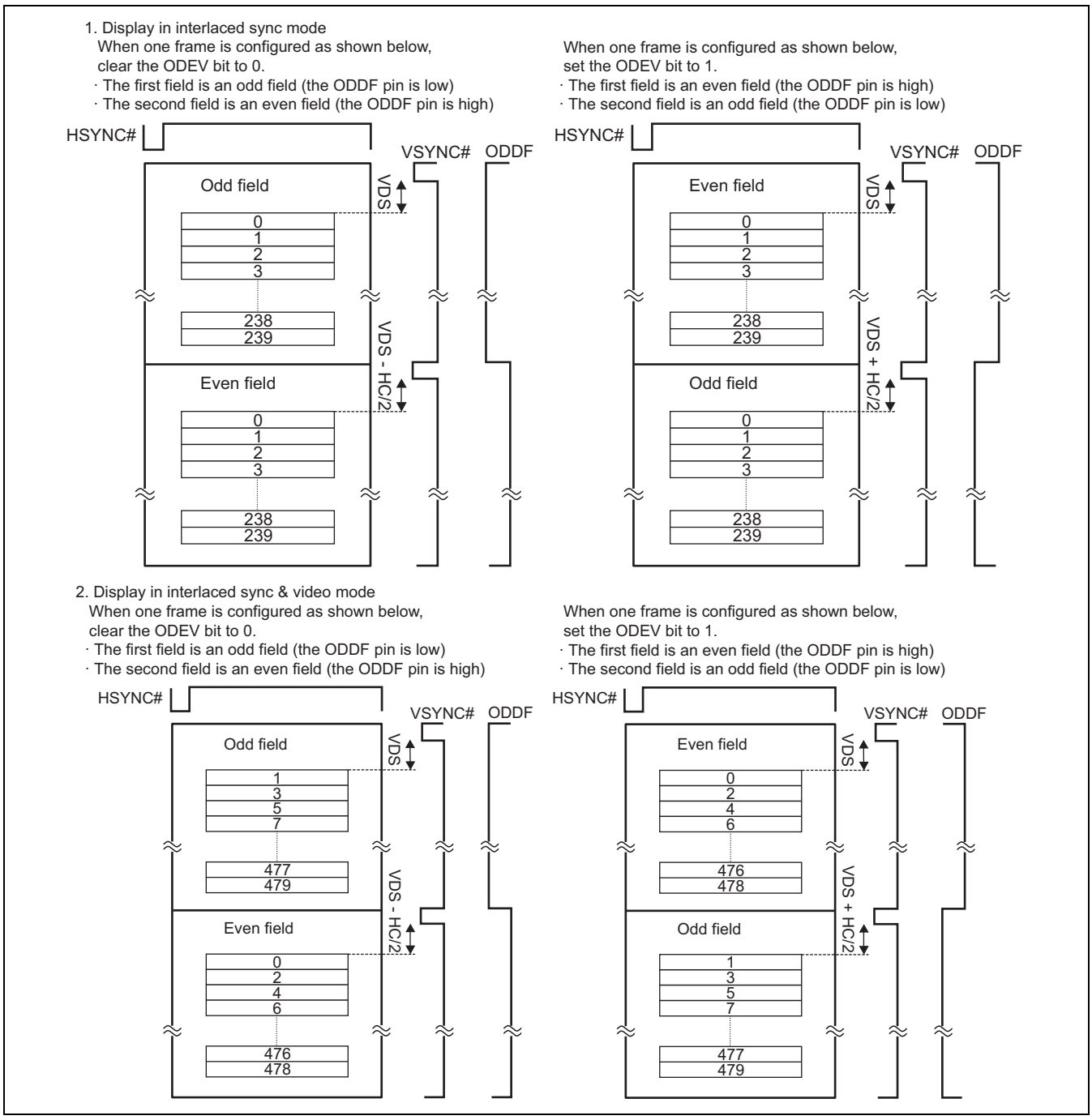


Figure 20.28 Display in Interlaced Method

20.5.4 Color Detection

When output display data matches a color set in CDERn*, high level is output from the CDE pin. The CDEM bit in DSMRn* can be used to fix the level outside display intervals. Also, the CDEL bit in DSMRn* can be used to select the polarity of the output level.

When the following display functions are set, the color detection function cannot be used.

- RGBYC processing performed by setting the RGBYC0 or RGBYC1 bits in the display unit extensional function control 5 register (DEF5R)

Note: * n = 0 and 1.

Table 20.42 Output Level of the CDE Pin

		The CDE pin in display intervals		The CDE pin outside display intervals	
		Result of Comparison of Output Display Data and Color Detection Register		Value of Color Detection Register*	
CDEL	CDEM	Same	Different	0	Other than 0
0	B'00	High level	Low level	High level	Low level
0	B'01	High level	Low level	High level	Low level
0	B'10	High level	Low level	Low level	Low level
0	B'11	High level	Low level	High level	High level
1	B'00	Low level	High level	Low level	High level
1	B'01	Low level	High level	Low level	High level
1	B'10	Low level	High level	High level	High level
1	B'11	Low level	High level	Low level	Low level

Note: * Output display data is 0 outside display intervals.

20.5.5 External Sync Control

In TV-sync mode, the display unit (DU) is capable of using an externally input dot clock (clock signal for frequency multiplication: DCLKIN) to generate a dot clock (output dot clock: DCLKOUT) that is in accord with external synchronizing signals (EXHSYNC, EXVSYNC). Supply the externally input dot clock (multiplication clock: DCLKIN) and set the following parameters in ESCRn*.

Table 20.43 External Sync Control Parameters

Variable	Function
ESCRn*/SYNCSEL	Selects the sync signal (EXHSYNC or EXVSYNC) to use in phase matching of the dot clock.
ESCRn*/FRQSEL	Selects the dot-clock division ratio.

1. Use the SYNCSEL bits of ESCRn* to set the sync timing of the dot clock (output dot clock: DCLKOUT) generated from the internal dot clock.
2. Use the FRQSEL bits of ESCRn* to set the division ratio for generation of the internal dot clock. The following figure shows the internal dot clock timing where the input dot clock has been synchronized with EXHSYNC and then divided by four.

Note * n = 0 and 1.

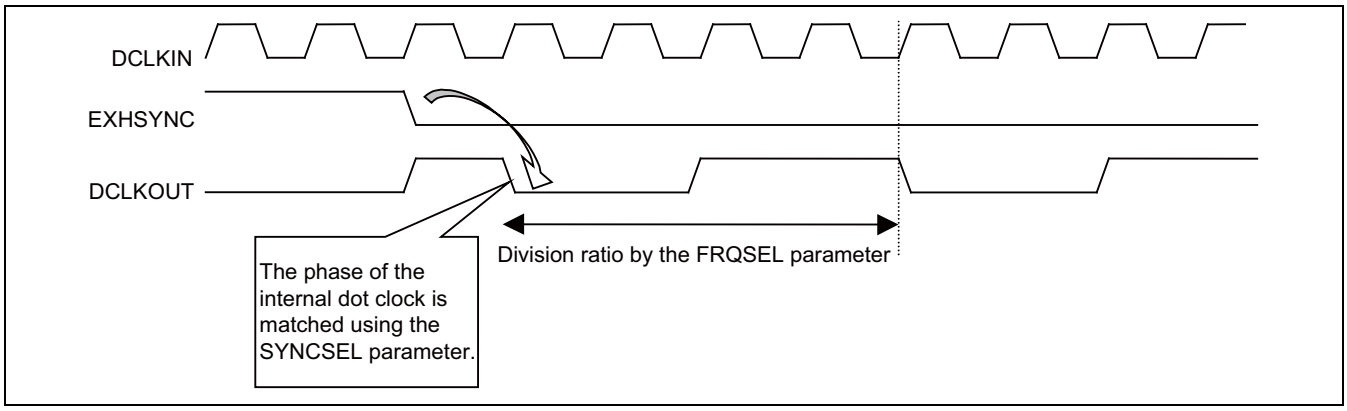


Figure 20.29 DCLKOUT Timing Chart where DCLKIN Synchronized with EXHSYNC is divided by Four

20.5.6 Output Signal Timing Adjustment

The display unit (DU) enables selection of output timing, with respect to the output dot clock, of the various output signals (the four sync signals HSYNC, VSYNC, CSYNC, ODDF, as well as DISP, CDE, CLAMP, DE, digital RGB signals). Timing is selected by setting OTARn*.

Note: * n = 0 and 1.

Table 20.44 Output Signal Timing Setting Parameters

Variable	Description
SYNCA	Sets output timing of the HSYNC, VSYNC, CSYNC, ODDF signal
DISPA	Sets output timing of the DISP signal
CDEA	Sets output timing of the CDE signal
DRGBA	Sets output timing of digital RGB signal
CLAMPA	Sets output timing of the CLAMP signal
DEA	Sets output timing of the DE signal

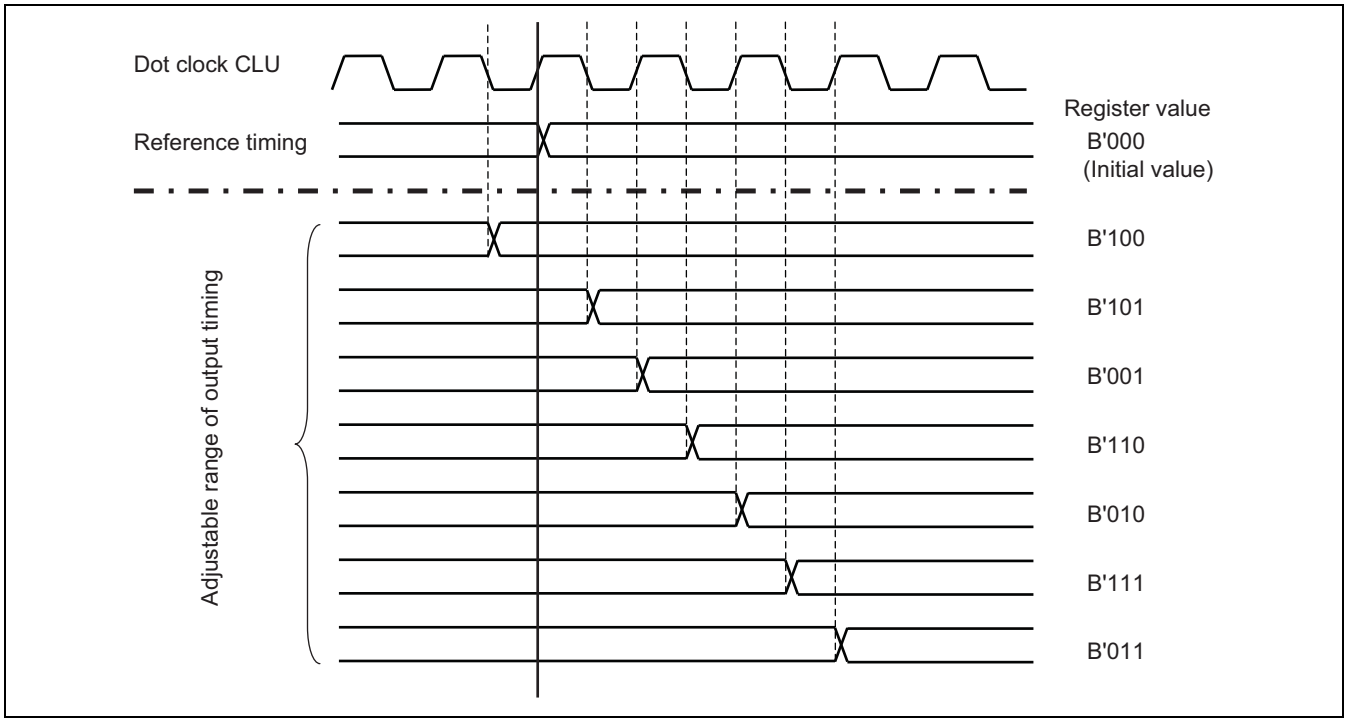


Figure 20.30 Adjustable Range of Output Timing

20.6 Notes on Usage

20.6.1 Module Standby Mode

Module Standby mode, in which supply of the clock signal to the display unit (DU) is stopped, is supported.

Even when the display unit (DU) enters the standby mode, the register values are retained. Do not access the display unit (DU) during periods in standby mode.

20.6.2 Transition to Module Standby Mode

1. Set both the DEN and DRES bits in DSYSR0 to 0 to stop access to the AXI.
2. Test bit 11 in DSSRn* to confirm the next VBK flag. The setting made in step 1 becomes effective with the timing of VBK and access to AXI is stopped. The value of the display data becomes the value set in DOORn*
   When DU0 and DU1 are running, test bit 11 of both DSSR0 and DSSR1.
3. Stop the clock.

Note: * n = 0 and 1.

20.6.3 Release from Module Standby Mode and Restarting Display

1. Start the clock.
2. Make settings to turn the display on by setting the DEN and DRES bits in DSYSR0 to 1 and 0 respectively.

20.6.4 Acquisition of External Sync Signal

The following three ways of acquiring the external SYNC signal are available.

(a) The SYNC signal is acquired on rising edges of DCLKIN (or the frequency-divided clock signal derived from this if division has been set up).
(b) The SYNC signal is acquired on falling edges of DCLKIN (or the frequency-divided clock signal derived from this if division has been set up).
(c) Assuming that division has been set up, the SYNC signal that is acquired by the pre-division clock signal is latched on edges of the frequency-divided clock signal.

The electrical characteristics (AC spec.) are only guaranteed for case (a) above. There is no guarantee of electrical characteristics (AC spec.) for cases (b) and (c).

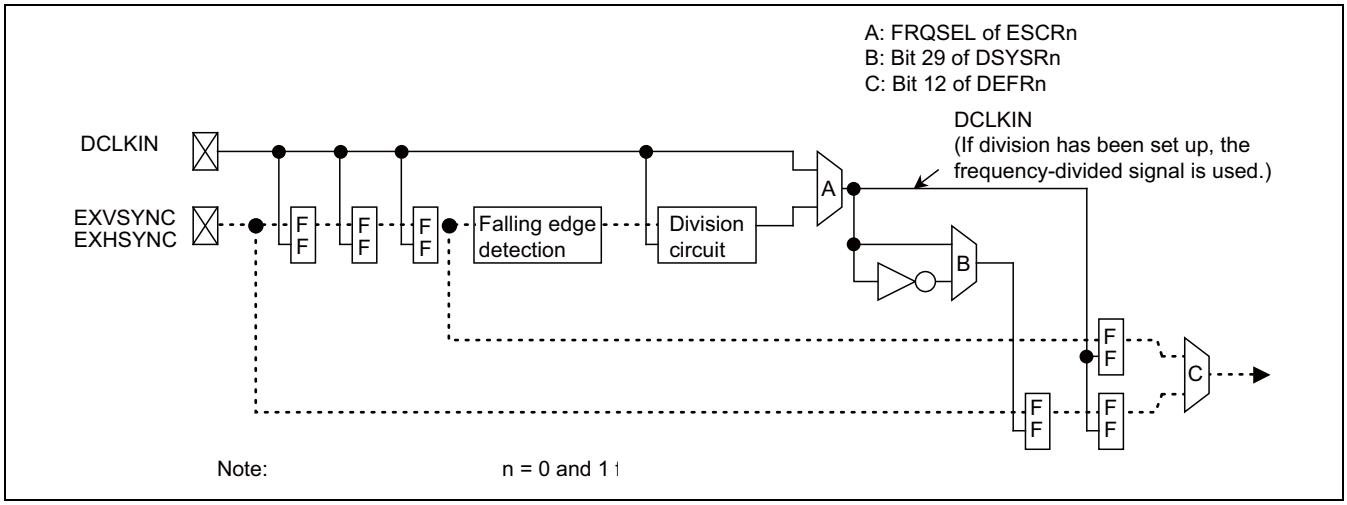


Figure 20.31 Diagram of Circuit that Generates the Display Timing from an External Sync Signal

20.6.5 Restrictions on Changing the Synchronization of the External SYNC Signal

When electrical characteristics (AC spec.) related to the acquisition of an external signal are not satisfied, ensure an interval of at least two cycles between changes of EXHSYNC or EXVSYNC, i.e. the external SYNC signals.

The frequency-divided dot clock is used as the basis of the cycle period when bit 12 of DEFRn* is 0. The pre-division dot clock is used when bit 12 is 1.

Note: * n = 0 and 1.

20.6.6 Note on Register Settings

At the time of a reset, some registers of the DU have fixed initial values but others do not. The initial values of the latter when the power for the LSI is turned on can be either 0 or 1. From the initial state after power is switched on, be sure to set all of the registers in the DU to the desired values before starting synchronization of the display*[1].

If turning on the display*[2], α planes*[3], or capturing*[4] is attempted while values in registers are unknown, operation may be incorrect due to access by the DU to areas other than those intended (the DU is capable of access to any area).

Notes: 1. Setting (a) or (b) starts synchronization of the display.
(a) The DRES and DEN bits in DSYSR0 are B'00.
(b) The DRES and DEN bits in DSYSR0 are B'01.

2. Setting (a) or (b) turns the display on.
(a) When the DPRS bit in DORCR is 0:
With setting (b) in note 1, setting any of bits DPE8 to DPE1 in DPPR to 1.
(b) When the DPRS bit in DORCR is 1:
With setting (b) in note 1, setting bits S0S8 to S0S1 in DS0PR or bits S1S8 to S1S1 in DS1PR to any value from B'0001 to B'1000.

3. α planes are turned on by the combination of setting (b) in note 1 and any of bits AP2E or AP1E in DAPCR being set to 1.

4. Capturing is turned on by the combination of setting (b) in note 1 and the DC2E or DCE bit in DCPCR being set to 1.

20A. Digital Video Encoder

20A.1 Overview

This module (DVENC) incorporates the interlace DENC and outputs the encoded data to the Video DAC. The interlace DENC generates analog output composite Y/C from the input data (8 bits for each of Y and CB/CR). The DVENC supports the internal image quality adjustment function with 12-bit accuracy.

The D/A converter uses a p-channel source follower with an R-string D/A converter. It latches the 10-bit digital signal output from the NTSC/PAL encoder for conversion on rising edges of the 27-MHz clock signal and outputs a voltage corresponding to the input digital signal via the analog output pin, VO.

20A.1.1 Functions

- NTSC, PAL, PAL-M, PAL-N, and PAL-60 encode processing
- Y1+C composite (CVBS) signal generation
- Image quality adjustment function (12 bits)
  Color
  TINT
  Skin tone correction
  Brightness
  Contrast
  Black stretch
  Sharpness/ unsharpness
  γ correction
- Superimposition of CGMS (525i) or WSS (625i)
- Superimposition of closed caption
- BPF processing for chroma (C) signal
- Total gain control in response to changes in the full-scale voltage from the DAC
- The input signal from DU is 4:4:4 format only.
- Supports the NTSC/PAL composite output.
- Analog macro output voltage: 1.30 Vp-p (typ.)
  Caution: VCCQA_DAC = 3.3 V; Rload ≥ 10 kΩ; Cload ≤ 20 pF
  Refer to the section 20A.6 for the DAC pin connection example.
- Low-power-consumption function (power-down mode).

20A.1.2 Block Diagram

Figure 20A.1 shows a block diagram of the DVENC (The DU is connected to the DENC).

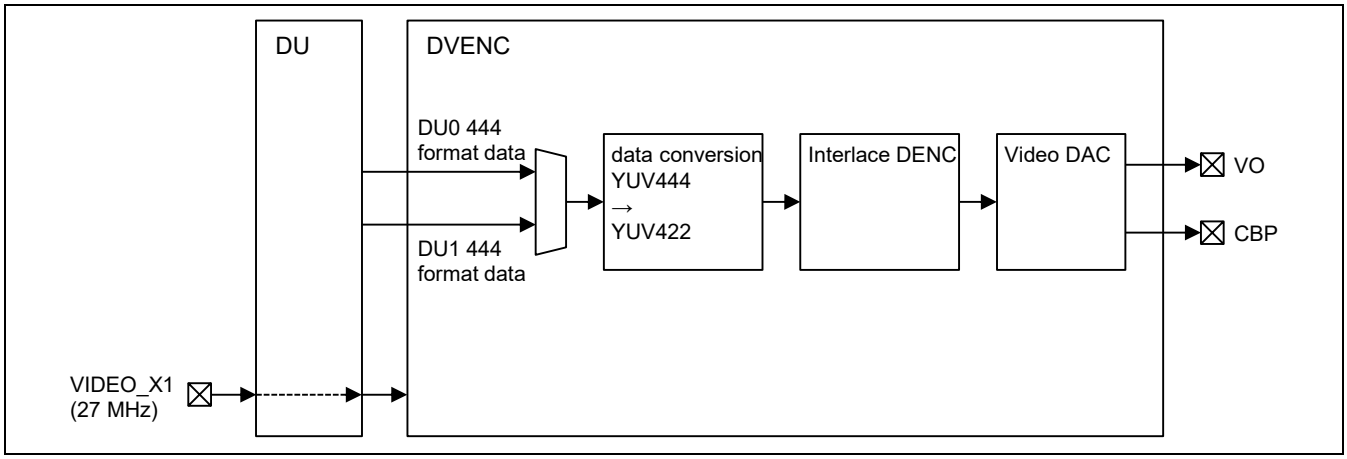


Figure 20A.1 DVENC Block Diagram

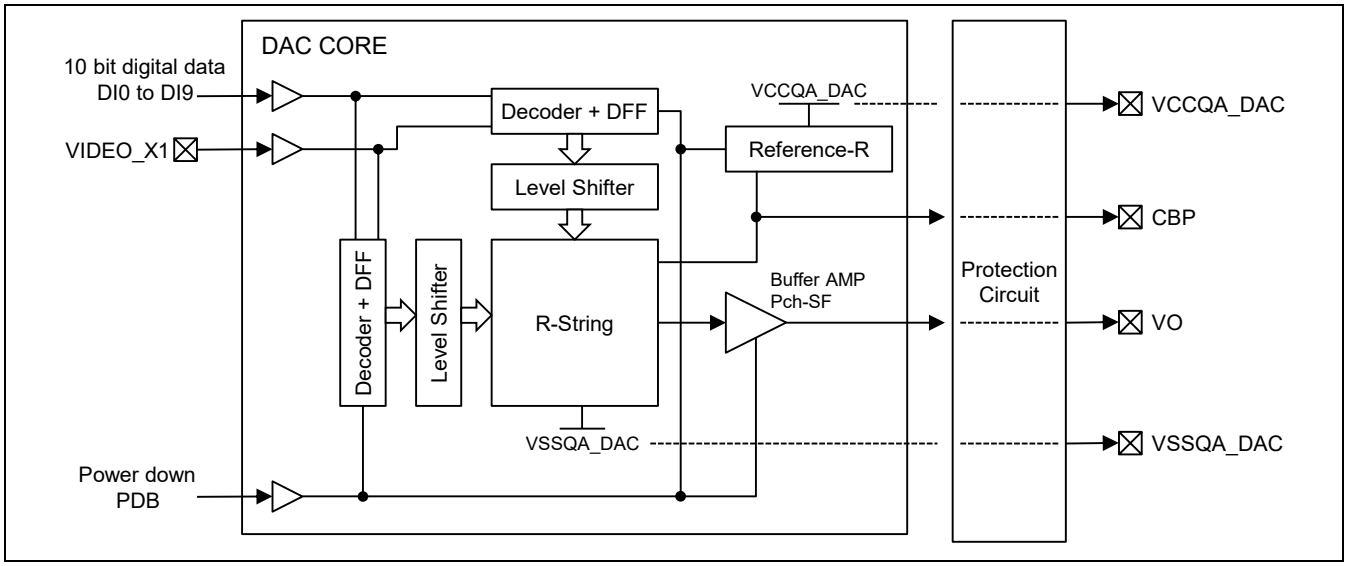


Figure 20A.2 DAC Block Diagram

20A.1.3 Input/Output Pins

Table 20A.1 Pin Configuration

Name	Pin Name	I/O	Function
Voltage output	VO	O	Video DAC signal output (NTSC/PAL composite)
Bypass capacity port	CBP	O	Bypass capacity port
External clock	VIDEO_X1	I	Clock 27 MHz

20A.1.4 Register Configuration

Table 20A.2 shows the DENC register configuration. Table 20A.2 shows the register state in each processing mode.

Base address: H'FEB8 0000

Table 20A.2 Register Configuration

Register Name	Abbreviation	R/W	Offset Address	Initial Value	Access Size
DVENC setting register	VSET	W	H'0120	H'0000	16
DAC output setting register	DENCOUT	R/W	H'0300	H'0000	16
DAC output setting register	DENCOUT2	R/W	H'0302	H'0000	16
DENC output select register	DENCO20	R/W	H'0308	H'03FF	16
NTSC/PAL encoder operating mode setting register 1	IDENCMD1	R/W	H'00C0	H'0000	16
NTSC/PAL encoder operating mode setting register 2	IDENCMD2	R/W	H'00C2	H'0000	16
TINT burst amplitude setting register for interlace output	ITNTBLEV	R/W	H'00C4	H'C900	16
Subcarrier frequency (MSB) setting register	IFSCH	R/W	H'00C6	H'21F0	16
Subcarrier frequency (LSB) setting register	IFSCL	R/W	H'00C8	H'7C1F	16
Delay amount setting register for interlace output	IDLYSET	R/W	H'00CA	H'0000	16
Luminance signal synchronization level setting register for interlace output	ISYNSET	R/W	H'00CC	H'15DB	16
Closed-caption, CGMS, WSS setting mode register for interlace output	ICCCGWS	R/W	H'00CE	H'0000	16
CVBS closed-caption data (1st field) setting register	ICCD1	R/W	H'00D0	H'0000	16
CVBS closed-caption data (2nd field) setting register	ICCD2	R/W	H00D2	H'0000	16
CVBS CGMS/WSS data setting register for interlace output	ICGWSD	R/W	H'00D4	H'0000	16
Black stretch and sharpness setting register for interlace output	IBLKSHP	R/W	H'00D6	H'0000	16
Sharpness setting register for interlace output	ISHRPSET	R/W	H'00D8	H'0000	16
Brightness and contrast setting register for interlace output	IBRTCON	R/W	H'00DA	H'0080	16
Skin tone setting register for interlace output	IHADA	R/W	H'00DC	H'0000	16
Color and TINT setting register for interlace output	ITNTCOL	R/W	H'00DE	H'0040	16
Output color difference (C) gain adjustment register for interlace output	ICGAIN	R/W	H'00F4	H'0000	16
Burst insertion position setting register for interlace output	IBURST	R/W	H'00F8	H'4567	16
Burst advanced start position setting register for interlace output	ICSP	R/W	H'00FA	H'003E	16
Output luminance gain adjustment register for interlace output	IY1GAIN	R/W	H'0108	H'0000	16
DAC power down and DU data select control	MOD_SEL5	R/W	H'E606 00D0*	H'0000 0000	32

Note: * A base address is different from DVENC register. Pin Function Controller (PFC) register (MOD_SEL5).

Table 20A.3 Register State in Each Processing Mode

	Power-On Reset	Module Standby
All registers	Initialized	Retained

20A.1.5 Low-Power-Consumption Mode

In addition to normal operating mode, this module has a low-power-consumption mode (power-down mode) in which the D/A converter is stopped. The module is placed in power-down mode by setting the DACPDB bit (bit4) to 0 in Pin Function Controller (PFC) register (MOD_SEL5). Similarly, the module is placed in power-down mode by setting the MSTP727 bit to 1 in module stop control register 7 (MSTPCR7). The module is released from the mode by setting the DACPDB bit to 1 and the MSTP727 bit to 0.

D/A conversion is restarted when the specified power up time (tup) has elapsed after setting of the DACPDB bit in MOD_SEL5 to 1 and the MSTP727 bit in MSTPCR7 to 0.

Table 20A.4 DACPDB, MSTP Bit and Operating Mode

MSTP727 Bit	DACPDB Bit	Operating Mode	Operation
0	1	Normal operating mode	D/A conversion is continued.
Others		Power-down mode	D/A conversion is stopped and the module is placed in low-power-consumption mode.

Note: default: MSTP727 = 1, DACPDB = 0

20A.2 Register Description

20A.2.1 DVENC Setting Register (VSET)

This address is “Write only”. Do not "Read".

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	VESEL	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	W	Reserved. The write value should always be 0.
14	VESEL	0	W	NTE* output of DU is input the encoder. When using the Digital video encoder, set this bit to ‘1’.
13 to 0	—	All 0	W	Reserved. The write value should always be 0.

Note: * for Digital video encoder

20A.2.2 DAC Output Setting Register (DENCOUT)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.

20A.2.3 DAC Output Setting Register (DENCOUT2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	HDPD0[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
3 to 0	HDPD0[3:0]	0000	R/W	DAC Output Pin Output Select To output data to Video DAC, set to B'0011.

20A.2.4 DENC Output Select Register (DENCO20)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	YSEL[9:0]									
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved. These bits are always read as 0. The write value should always be 0.
9 to 0	YSEL[9:0]	H'3FF	R/W	DAC Output Select All 0: Outputs data to DAC. All 1: Initial state Other than above: Setting prohibited

20A.2.5 NTSC/PAL Encoder Operating Mode Setting Register 1 (IDENCMD1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	R12	—	—	R9	R8	—	R6	R5	R4	—	—	R1	R0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	—	0	R	Reserved. When using this module, set 1 to this bit.
12	R12	0	R/W	Slew Rate Limiter (CVBS) 0: Slew rate limiter disabled 1: Slew rate limiter enabled
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	R9	0	R/W	Field 2 Closed Caption Data Transfer Flag (CVBS) 0: Data update is set. 1: Data transfer is completed. Closed Caption data is updated in line 21 by writing 0 to this bit. After update is complete, R9 is set to 1.
8	R8	0	R/W	Field 1 Closed Caption Data Transfer Flag (CVBS) 0: Data update is set. 1: Data transfer is completed. Closed Caption data is updated in line 21 by writing 0 to this bit. After update is complete, R8 is set to 1.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	R6	0	R/W	WSS ON/OFF (CVBS) 0: OFF 1: ON (Set 0 for the 525-line/60-Hz operation.)
5	R5	0	R/W	Subcarrier Frequency 0: 3.58 MHz 1: 4.43 MHz
4	R4	0	R/W	Subcarrier Phase Control 0: Control ON 1: Control OFF (free-running)
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	R1	0	R/W	Field Frequency 0: 525 lines/60 Hz 1: 625 lines/ 50 Hz

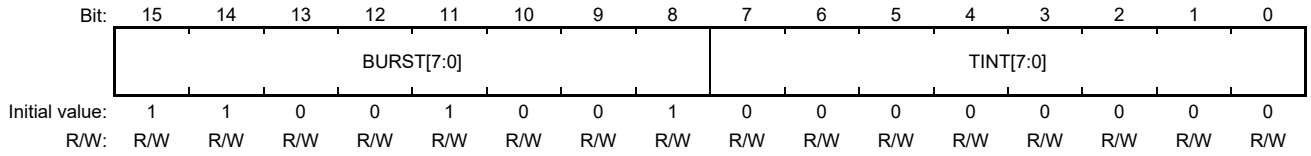
Bit	Bit Name	Initial Value	R/W	Description
0	R0	0	R/W	NTSC/PAL Color-Difference Modulation 0: NTSC 1: PAL

20A.2.6 NTSC/PAL Encoder Operating Mode Register 2 (IDENCMD2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R15	R14	R13	R12	R11	R10	R9	R8	—	—	—	—	—	—	Y1SETUP	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

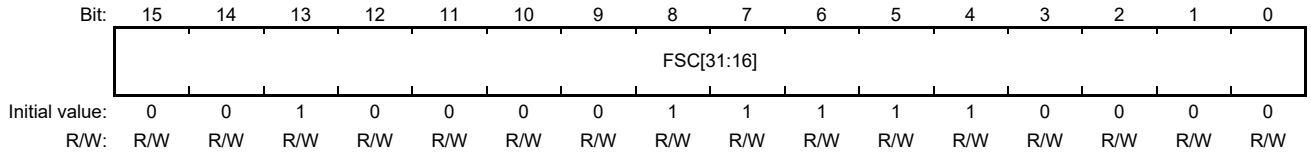
Bit	Bit Name	Initial Value	R/W	Description
15	R15	0	R/W	Upper Limit ON/OFF of Color Difference Signal after Image Quality Adjustment 0: Limit OFF 1: Limit ON
14	R14	0	R/W	Lower Limit ON/OFF of Color Difference Signal after Image Quality Adjustment 0: Limit OFF 1: Limit ON
13	R13	0	R/W	Upper Limit ON/OFF of Luminance Signal after Image Quality Adjustment 0: Limit OFF 1: Limit ON
12	R12	0	R/W	Lower Limit ON/OFF of Luminance Signal after Image Quality Adjustment 0: Limit OFF 1: Limit ON
11	R11	0	R/W	Upper Limit ON/OFF of Input Color Difference Signal 0: Limit OFF 1: Limit ON
10	R10	0	R/W	Lower Limit ON/OFF of Input Color Difference Signal 0: Limit OFF 1: Limit ON
9	R9	0	R/W	Upper Limit ON/OFF of Input Luminance Signal 0: Limit OFF 1: Limit ON
8	R8	0	R/W	Lower Limit ON/OFF of Input Luminance Signal 0: Limit OFF 1: Limit ON
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	Y1SETUP [1:0]	00	R/W	Luminance Signal Setup (CVBS) 00: Setup OFF 01: +7.5IRE Setup 10: -7.5IRE Setup 11: Setting prohibited

20A.2.7 TINT Burst Amplitude Setting Register for Interlace Output (ITNTBLEV)



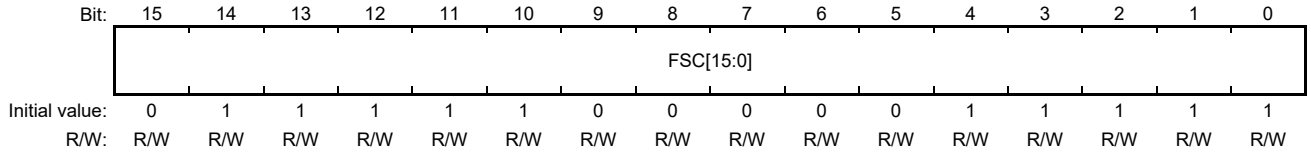
Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BURST[7:0]	H'C9	R/W	Burst Amplitude Level Amplitude = (BURST – 256) × 16/4095 × Vp-p (for NTSC)
7 to 0	TINT[7:0]	H'00	R/W	Color Difference Signal (C) TINT (Hue) Hue (degree) = (TINT – ICSP[15:8]) × 1.4 Settable range: 0 to 357 [degrees]

20A.2.8 Subcarrier Frequency (MSB) Setting Register (IFSCH)



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	FSC[31:16]	H'21F0	R/W	Subcarrier Frequency *1: Refer to a “20A.2.9 Note *”.

20A.2.9 Subcarrier Frequency (LSB) Setting Register (IFSCL)



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	FSC[15:0]	H'7C1F	R/W	Subcarrier Frequency *

Note: * FSC [31:0] = {IFSCH Register, IFSCL Register}
Frequency = (27/232) × FSC [31:0]
M-NTSC: H'21F07C1F
B/G/I-PAL: H'2A098ACB
M-PAL: H'21E6EFE3
N-PAL: H'21F69447

20A.2.10 Delay Amount Setting Register for Interlace Output (IDLYSET)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Y1DLY[5:0]						—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	Y1DLY[5:0]	000000	R/W	Luminance Signal (Y on CVBS) Output Delay from C (indicated by 2's complement)
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

20A.2.11 Luminance Signal Synchronization Level Setting Register for Interlace Output (ISYNSET)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SYNDLY[4:0]					Y1SYNC LEVEL[7:0]							
Initial value:	0	0	0	1	0	1	0	1	1	1	0	1	1	0	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

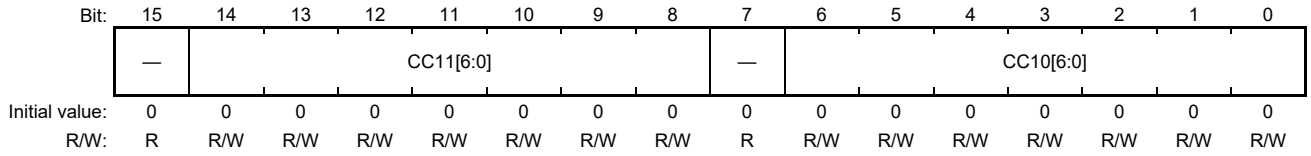
Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	SYNDLY [4:0]	H'15	R/W	Synchronization Setting Set to H'15.
7 to 0	Y1SYNC LEVEL[7:0]	H'DB	R/W	Luminance Signal (CVBS) Synchronization Amplitude Level Synchronization signal amplitude = SYNCLEVEL × 4/4095 × Vp-p

20A.2.12 Closed-Caption, CGMS, WSS Setting Mode Register for Interlace Output (ICCCGWS)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	R6	R5	—	—	Y1CC[1:0]		R0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	R6	0	R/W	Closed Caption Automatic Null Code Generation ON/OFF (CVBS) 0: ON 1: OFF
5	R5	0	R/W	VBI Bypass Setting (CVBS) 0: Bypasses the VBI signal multiplexed to lines 10 to 19 or lines 273 to 282 during the 525-line/60-Hz operation. Bypasses the VBI signal multiplexed to lines 6 to 22 or lines 318 to 335 during the 625- line/50-Hz operation. 1: Outputs the above lines as blanking levels. Note: Set the R5 bit to 1 for interlace output.
4, 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2, 1	Y1CC[1:0]	00	R/W	Closed Caption Setting (CVBS) 00: OFF 01: For field 1 only 10: For field 2 only 11: For both fields
0	R0	0	R/W	CGMS ON/OFF Setting (CVBS) 0: OFF 1: ON Set the R0 bit to 0 for the 625-line/50-Hz operation (field frequency setting).

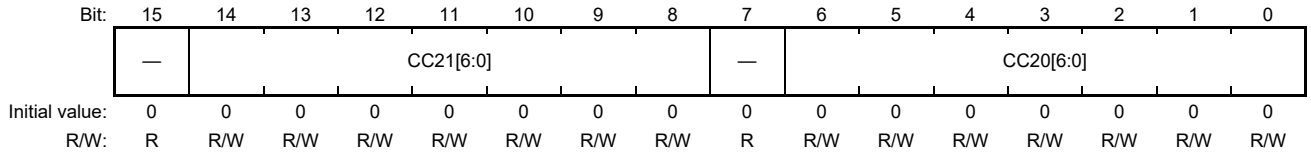
20A.2.13 CVBS Closed-Caption Data (1st Field) Setting Register (ICCD1)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CC11[6:0]							—	CC10[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	CC11[6:0]	H'00	R/W	Second-Byte Closed Caption Data to be Multiplexed to First Field (The odd parity is computed in the LSI using 7-bit data.)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	CC10[6:0]	H'00	R/W	First-Byte Closed Caption Data to be Multiplexed to First Field (The odd parity is computed in the LSI using 7-bit data.)

20A.2.14 CVBS Closed-Caption Data (2nd Field) Setting Register (ICCD2)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CC21[6:0]							—	CC20[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	CC21[6:0]	H'00	R/W	Second-Byte Closed Caption Data to be Multiplexed to Second Field (The odd parity is computed in the LSI using 7-bit data.)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	CC20[6:0]	H'00	R/W	First-Byte Closed Caption Data to be Multiplexed to Second Field (The odd parity is computed in the LSI using 7-bit data.)

20A.2.15 CVBS CGMS/WSS Data Setting Register for Interlace Output (ICGWSD)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CGWS[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

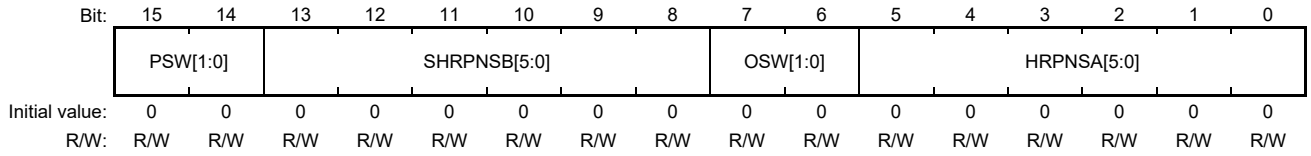
Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	CGWS[13:0]	H'0000	R/W	Sets the CGMS or WSS data. During the 525-line/60-Hz operation: CGMS data is set. (CRCC is computed in the LSI using 6-bit data.) During the 625-line/50-Hz operation: WSS data is set.

20A.2.16 Black Stretch and Sharpness Setting Register for Interlace Output (IBLKSHP)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R15	SHLMT[6:0]							GAMMA_MODE[4:0]					—	BKPNT[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

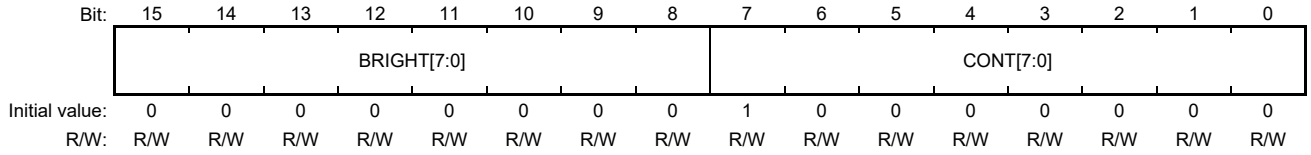
Bit	Bit Name	Initial Value	R/W	Description
15	R15	0	R/W	Unsharpness Function 0: OFF 1: ON
14 to 8	SHLMT[6:0]	H'00	R/W	Sharpness Operation Limit Level Sharpness correction is ON when the signal change amount is larger than SHLMT.
7 to 3	GAMMA_ MODE[4:0]	00000	R/W	γ Correction Mode (γ value) 00000: γ correction OFF When GAMMA_MODE[4] = 0, the γ value is: Y = 1/(1 + 0.05 × N) N = 1, 2, 3, 4, 5, 6, 8, 12, 20, or 40 B'0001: ≤ GAMMA_MODE[3:0] ≤ B'1010 When GAMMA_MODE[4] = 1, the γ value is: Y = 1 + 0.05 × N N = 1, 2, 3, 4, 5, 6, 8, 12, 20, or 40 B'0001: ≤ GAMMA_MODE[3:0] ≤ B'1010
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	BKPNT[1:0]	00	R/W	Black Stretch Operating Mode 00: Black stretch OFF 01: Black stretch mode 1 10: Black stretch mode 2 11: Black stretch mode 3

20A.2.17 Sharpness Setting Register for Interlace Output (ISHRPSET)



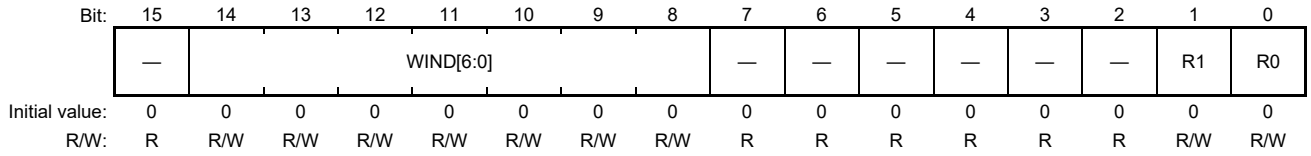
Bit	Bit Name	Initial Value	R/W	Description
15, 14	PSW[1:0]	00	R/W	Pre-Shoot Width Setting 00: 0T 01: 1T Other than above: 2T (T = 13.5 MHz, 1 clock)
13 to 8	SHRPNSB [5:0]	000000	R/W	Pre-Shoot Amplitude Setting Amplitude = (signal change amount) × SHRPNSB/128
7, 6	OSW[1:0]	00	R/W	Over-Shoot Width Setting 00: 0T 01: 1T Other than above: 2T (T = 13.5 MHz, 1 clock)
5 to 0	SHRPNSA [5:0]	000000	R/W	Over-Shoot Amplitude Setting Amplitude = (signal change amount) × SHRPNSA/128

20A.2.18 Brightness and Contrast Setting Register for Interlace Output (IBRTCON)



Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BRIGHT[7:0]	H'00	R/W	Brightness Setting (2's complement) Output = Input + BRIGHT × 16
7 to 0	CONT[7:0]	H'80	R/W	Contrast Setting Output = (Input – 256) × CONT/128 + 256

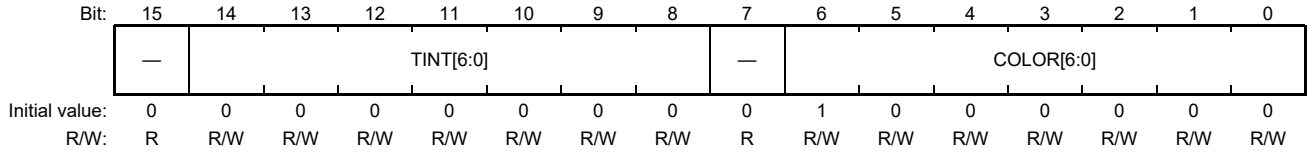
20A.2.19 Skin Tone Setting Register for Interlace Output (IHADA)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	WIND[6:0]							—	—	—	—	—	—	R1	R0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	WIND[6:0]	H'00	R/W	Skin Tone Correction Area Setting A window is set when WIND > | R + B |
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	R1	0	R/W	Skin Tone Correction Area B Control 0: Area B OFF 1: Area B ON
0	R0	0	R/W	Skin Tone Correction Area A Control 0: Area A OFF 1: Area A ON

20A.2.20 Color and TINT Setting Register for Interlace Output (ITNTCOL)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TINT[6:0]							—	COLOR[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	TINT[6:0]	H'00	R/W	TINT (Phase) of Color Difference Signal Sets TINT in the unit of degrees (2's complement). Settable range: -45 to +45 degrees
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	COLOR[6:0]	H'40	R/W	Color Saturation of Color Difference Signal Cout = Cinput × COLOR/64

20A.2.21 Output Color Difference (C) Gain Adjustment Register for Interlace Output (ICGAIN)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CGAIN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CGAIN[11:0]	H'000	R/W	Output Color Difference (C) Gain Adjustment (indicated by 2's complement) Output = (Input – 2048) × (1 + CGAIN/4096) + 2048

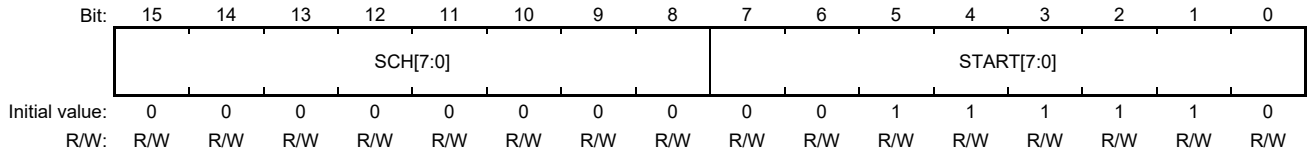
20A.2.22 Burst Insertion Position Setting Register for Interlace Output (IBURST)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	START[7:0]								END[7:0]							
Initial value:	0	1	0	0	0	1	0	1	0	1	1	0	0	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	START[7:0]	H'45	R/W	Burst Start Position Sets the period from Hsync to the burst start position. START + 4/13.5 MHz
7 to 0	END[7:0]	H'67	R/W	Burst End Position Sets the period from Hsync to the burst end position. END + 4/13.5 MHz

Recommended value: NTSC IBURST = H'4565
PAL-M IBURST = H'496B
PAL-60 IBURST = H'4765
PAL IBURST = H'4765
PAL-N IBURST = H'4765

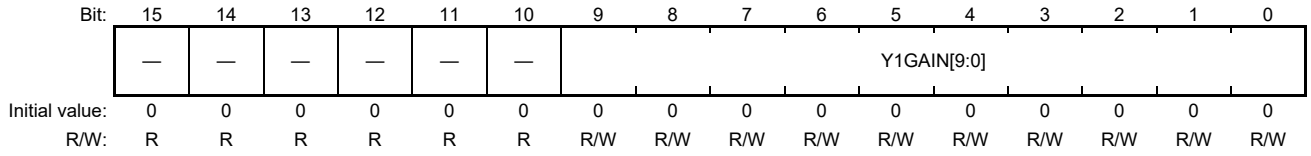
20A.2.23 Burst Advanced Start Position Setting Register for Interlace Output (ICSP)



Bit	Bit Name	Initial Value	R/W	Description
15 to 8	SCH[7:0]	H'00	R/W	SCH Timing Adjustment Adjusts the SCH in 1.4° steps. H'00 is recommended during NTSC operation.
7 to 0	START[7:0]	H'3E	R/W	Burst Advanced Start Position (START + 3.5)/13.5 MHz

Recommended value: NTSC ICSP = H'003D
PAL-M ICSP = H'0042
PAL-60 ICSP = H'0041
PAL ICSP = H'0041
PAL-N ICSP = H'0041

20A.2.24 Output Luminance Gain Adjustment Register for Interlace Output (IY1GAIN)



Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	Y1GAIN[9:0]	H'000	R/W	Output Luminance (Y1) Gain Adjustment (indicated by 2's complement) Output = (Input – 1024) × (1 + Y1GAIN/4096) + 1024

20A.2.25 DAC power down and DU data select control (MOD_SEL5)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	DACPDB	—	—	—	DU1_SEL_MODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
32 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DACPDB	0	R/W	Controls power-down for the DAC. 0: Power-down state 1: Normal operation
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DU1_SEL_MODE	0	R/W	DU data select 0: DU0 YUV 444 format data select 1: DU1 YUV 444 format data select Note: DU0/1 change make select in the state that stopped DU module.

Note: Setting mask register (H'E606 0000) immediately before setting this register. Write the inversion of the value to set.

20A.3 Operation

20A.3.1 Input/Output Specifications

The input/output video signal levels of the DENC block are shown below:

Input Video Signal

- 720 dots × 480 lines 4:2:2 format
- Y = 8 bits/27 Mbps 16 to 235 straight binary
- Cb/Cr = 8 bits/27 Mbps 16 to 240 128 offset binary

Output Video Signal

- 720 dots × 480 lines 4:4:4 format
- CVBS = 10 bits/27 Mbps 256 to 985 straight binary + Sync (pedestal = 256)

[Supplementary Note]

Figure 20A.3 shows the input waveform of the 525i.

In this LSI, the input signal to the DVENC is generate by the DU (DU0/DU1).

DU setting the following register is required.

Case when the 525i setting: DU0

```
// DU0 clock setting
DIDSR = H'77900300     : When you use the DU0, set this by all means.
DEFR0 = H'77730001     : bit0 DEFE DU0/1 common setting
ESCR0 = H'00000001     : select input clock, division setting
DSMR0 = H'01000100     : DU terminal setting
DEF5R = H'66040021     : Interface behaviour of the NTSC encoder, selected non-multiplexed YC

// DU0 timing setting
HDSR0 = H'00000066     : 102, Horizontal display start point
HDER0 = H'00000336     : 822, Horizontal display end point
VDSR0 = H'0000000A     : 10, Vertical display start point
VDER0 = H'000000FA     : 250, Vertical display end point
HSWR0 = H'0000003B     : 59, Horizontal sync pulse width
HCR0 = H'00000359      : 857, Horizontal scanning period
VSPR0 = H'000000FF     : 255, Vertical sync point
VCR0 = H'00000105      : 261, Vertical scanning sync point

// DU0 sample of setting from RGB to YUV conversion factor
YCLRP = H'0000020E
YCLGP = H'00000408
YCLBP = H'000000C9
YCLAP = H'00000010;
CBCLRP = H'0000112F;
CBCLGP = H'00001254;
CBCLBP = H'00000383;
CBCLAP = H'00000080;
```

```
CRCLRP = H'00000383;
CRCLGP = H'000012F2;
CRCLBP = H'00001091;
CRCLAP = H'00000080;

// DU0 data selector (Chapter 5.Pin Function Controller (PFC) Register: MOD_SEL5 bit0 DU1_SEL_MODE)
// DU1_SEL_MODE = 0 (DU0 select Register default)
H'E6060000 = H'FFFFFFEF;
H'E60600D0 = H'00000010;
```

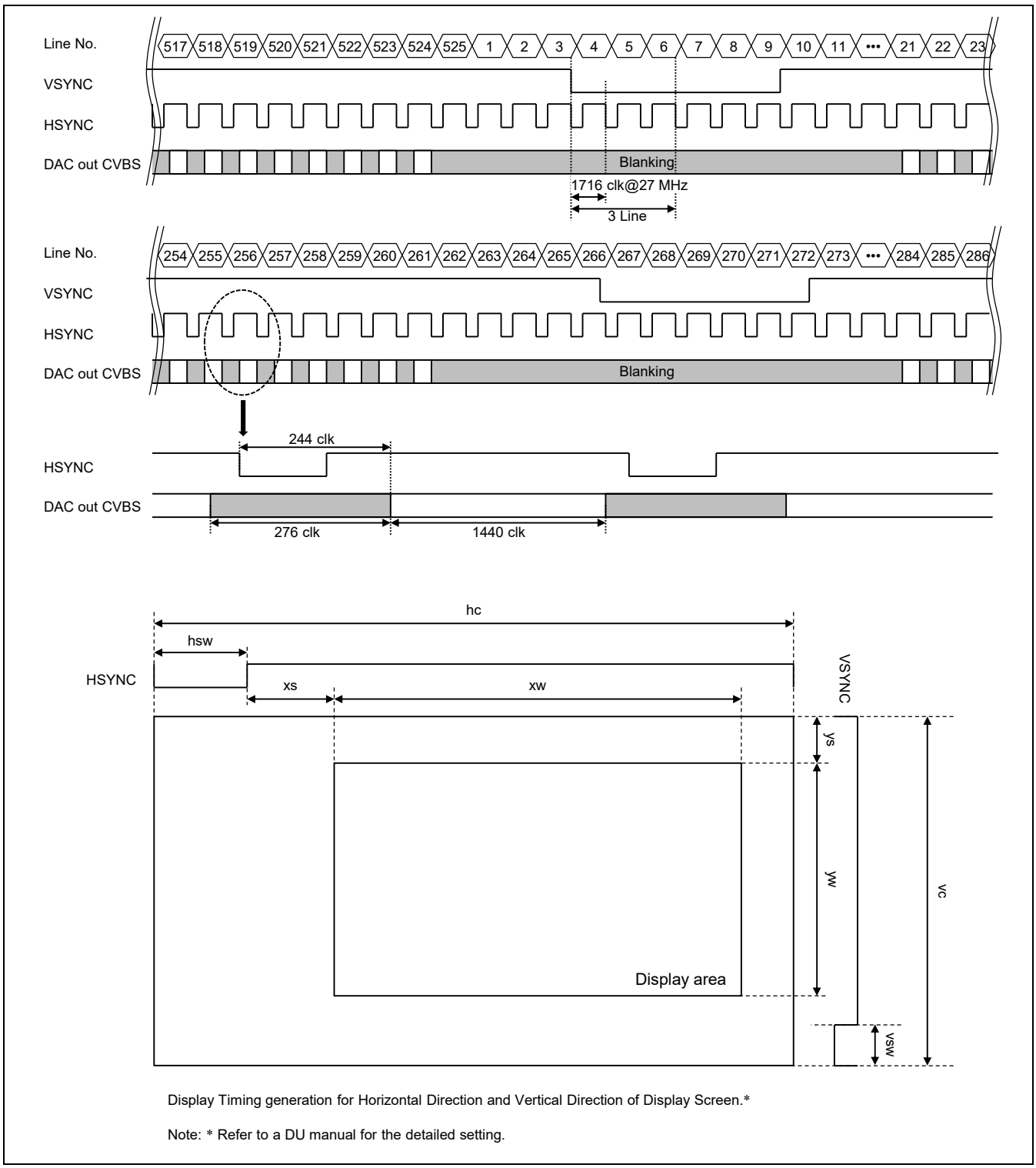
Case when the 525i setting: DU1

```
// DU1 clock setting
DIDSR = H'77900C00     : When you use the DU1, set this by all means.
DEFR0 = H'77730001     : bit0 DEFE DU0/1 common setting
ESCR1 = H'00000001     : select input clock, division setting
DSMR1 = H'01000100     : DU terminal setting
DEF5R = H'66040081     : Interface behaviour of the NTSC encoder, selected non-multiplexed YC

// DU1 timing setting
HDSR1 = H'00000066     : 102, Horizontal display start point
HDER1 = H'00000336     : 822, Horizontal display end point
VDSR1 = H'0000000A     : 10, Vertical display start point
VDER1 = H'000000FA     : 250, Vertical display end point
HSWR1 = H'0000003B     : 59, Horizontal sync pulse width
HCR1 = H'00000359      : 857, Horizontal scanning period
VSPR1 = H'000000FF     : 255, Vertical sync point
VCR1 = H'00000105      : 261, Vertical scanning sync point

// DU1 sample of setting from RGB to YUV conversion factor
YCLRP = H'020E0000
YCLGP = H'04080000
YCLBP = H'00C90000
YCLAP = H'00100000;
CBCLRP = H'112F0000;
CBCLGP = H'12540000;
CBCLBP = H'03830000;
CBCLAP = H'00800000;
CRCLRP = H'03830000;
CRCLGP = H'12F20000;
CRCLBP = H'10910000;
CRCLAP = H'00800000;

// DU1 data selector (Chapter 5.Pin Function Controller (PFC) Register: MOD_SEL5 bit0 DU1_SEL_MODE)
// DU1_SEL_MODE = 1 (DU1 select)
H'E6060000 = H'FFFFFFEE;
H'E60600D0 = H'00000011;
```



Display Timing generation for Horizontal Direction and Vertical Direction of Display Screen.*

Note: * Refer to a DU manual for the detailed setting.

Figure 20A.3 input waveform of the 525i

20A.4 Specifications for the Inside of Interlace DENC

This section describes the specifications for blocks of the interlace DENC.

20A.4.1 Input/Output Specifications

This module performs limiter processing depending upon the settings of bits R8, R9, R10, and R11 of the IDENCMD2 register. The processing is skipped when these bits are set to 0 (through).

IDENCMD2.R11 = 1: C ≤ 240 (H'F0)

IDENCMD2.R10 = 1: 16 (H'10) ≤ C

IDENCMD2.R9 = 1: Y ≤ 235 (H'EB)

IDENCMD2.R8 = 1: 16 (H'10) ≤ Y

In addition, the block multiplexes into one signal in a time division manner the color difference signals that are separately input as Cb/Cr (a signal that indicates the distinction between Cb/Cr is also output).

20A.4.2 Image Quality Adjustment Functions

Of the image quality adjustment functions, the sharpness, contrast, brightness, and γ correction adjustments are performed on luminance signals; and the color correction, TINT correction, and skin tone correction adjustments are performed on color difference signals.

20A.4.3 Video Signal Generation Function

With respect to the luminance and color difference signals that have undergone image quality adjustments, the block performs modulation processing based upon various video signal standards. The output signal for the later-stage oversampling filter unit is 10-bit Y1/C (CVBS).

20A.4.4 Color Matrix

This block performs the standardization of the R/G/B and color difference signals; it does not perform any processing on Y or C (U/V).

20A.4.5 SYNC/Blanking Addition of Luminance Signals

This block performs the standardization, blanking, slew-rate limiter processing, and C-SYNC addition processing on luminance signals. These processing operations are the same as the progressive SYNC/Blanking additions.

20A.4.6 Blanking Addition of Color Difference Signals

In this block, the output of color difference signals during the blanking period is fixed to the blanking level (2048).

20A.4.7 Burst Addition

This block performs U/V conversion and standardization, blanking, and burst signal addition with respect to color difference signals.

(1) U/V conversion and standardization

The standardization of luminance signals can vary in terms of processing depending upon the settings of the Y1SETUP[1:0] bits of IDENCMD2 register, as follows:

B'00: ± 0IRE Setup, B'10: -7.5IRE Setup

→ $U = (Cb \times 219/224 \times 1.772/2.03) \times 0.625$

$V = (Cr \times 219/224 \times 1.402/1.14) \times 0.625$

B'01: + 7.5IRE Setup

→ $U = (Cb \times 219/224 \times 1.772/2.03) \times 0.625 \times 0.925$

$V = (Cr \times 219/224 \times 1.402/1.14) \times 0.625 \times 0.925$

B'11: Setting prohibited

The above conversions are implemented in the RTL in terms of the following processing operations:

B'00: ± 0IRE Setup, B'10: -7.5IRE Setup

→ $U = (2^{-1} + 2^{-5} + 2^{-9}) \times Cb \times 0.625$

$V = (2^{-1} + 2^{-2} + 2^{-10}) \times Cr \times 0.625$

B'01: + 7.5IRE Setup

→ $U = (2^{-1} - 2^{-7} + 2^{-10}) \times Cb \times 0.625$

$V = (2^{-1} + 2^{-2} - 2^{-4} + 2^{-7}) \times Cr \times 0.625$

(2) Blanking

The output during the U/V blanking period is fixed to the blanking level (0).

(3) Burst signal addition

The amplitude of the burst signal to be added can be adjusted in terms of BURSTLVL[7:0] bits.

NTSC: amplitude = (BURSTLVL[7:0] – 256) × 4

Note: Because the value of (BURSTLVL[7:0] – 256) × 2, after addition in the U direction, is modulated by U × sinα+ V × cosα, the amplitude is further multiplied by 2 (for a total of 4x).

PAL: amplitude = (BURSTLVL[7:0] – 256) × 4√2

Note: Because the value of (BURSTLVL[7:0] - 256) × 2, after addition in the U and V directions, respectively, is modulated by U × sinα+ V × cosα, the amplitude is further multiplied by 2√2 (for a total of 4√2x).

20A.4.8 Subcarrier Generation

By the setting of the IFSCH[15:0] and IFSCL[15:0] bits that determine the frequency and by the operation of the NCO adder, this block generates subcarriers for the modulation of the chroma. A subcarrier generation circuit diagram and a timing chart are shown in Figure 20A.4.

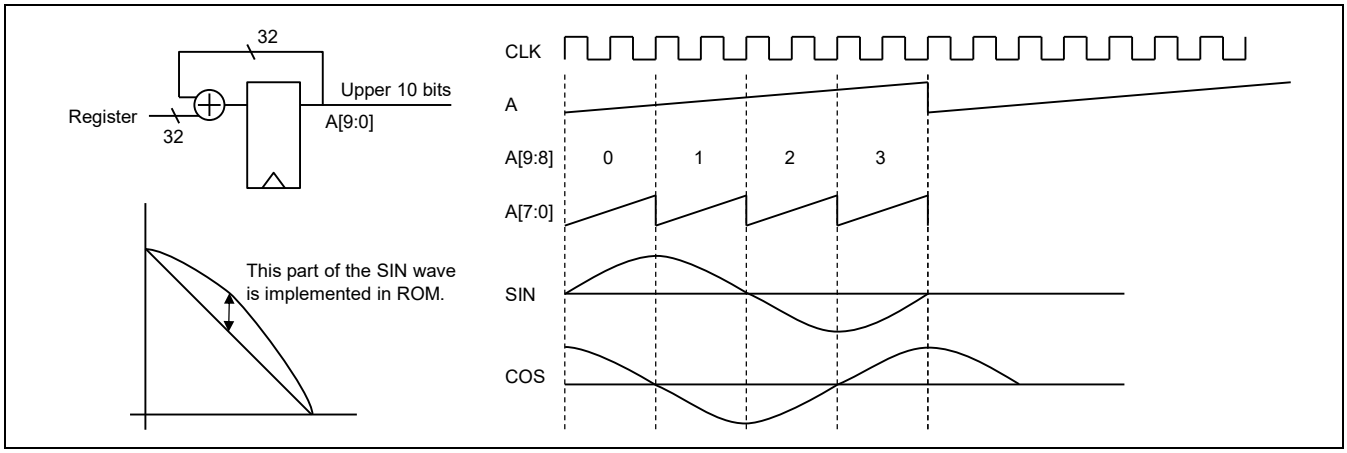


Figure 20A.4 Subcarrier Generation Circuit Diagram and Timing Chart

As indicated in the timing chart, the position in which the NCO adder overflows is the subcarrier frequency. Therefore, the following subcarrier formula applies:

Register settings × 27/232 [MHz]

In order to reduce the circuit size, of the SIN wave/COS wave, only the part shown in Figure 20A.4 is implemented in ROM, the part is divided into cases in terms of the upper 2 bits of the NCO adder output A[9:0], and SIN/COS waveforms are generated. The generated subcarrier is used by the subsequent-stage chroma encoder for the modulation of color signals (chroma).

20A.4.9 Chroma Encoder

This block performs the following processing:

(1) Chroma encoding

Using a subcarrier, the block performs chroma encoding (modulating) according to the following equation:

$C = U \times \sin A + V \times \cos A$

(2) BPF

Using a BPF, the block removes the harmonic components generated by the chroma encoding. The BPF has the following filter coefficients:

For NTSC (3.58 [MHz]):

$\rightarrow -5 \times Z^{-4} - 6 \times Z^{-3} - 1 \times Z^{-2} + 6 \times Z^{-1} + 4 \times Z^{0} + 6 \times Z^{1} - 1 \times Z^{2} - 6 \times Z^{3} - 5 \times Z^{4}$

For PAL (4.43 [MHz]):

$\rightarrow -1 \times Z^{-4} - 7 \times Z^{-3} - 3 \times Z^{-2} + 2 \times Z^{-1} + 12 \times Z^{0} + 2 \times Z^{1} - 3 \times Z^{2} - 7 \times Z^{3} - 1 \times Z^{4}$

20A.4.10 Video ID Addition

The block multiplexes the video ID signal, similar to the progressive case, in lines 20/283 in the luminance signal during a 525-line/60-Hz operation. The multiplexing can be turned ON/OFF and video ID data can be set by setting ICCCGWS register and CGWS [13:0] bits of ICGWSD register. The video ID data that is actually multiplexed on the output signal is created by generating a 6-bit error correction code (CRC) from the 14-bit register settings data and adding it to the end of the 14-bit data for a total of 20 bits, and the resultant data is modulated and multiplexed.

By setting the ICCCGWS register, the CGMS that is multiplexed in the luminance signal can be output as is.

Figure 20A.5 shows an example of a multiplexed video ID signal.

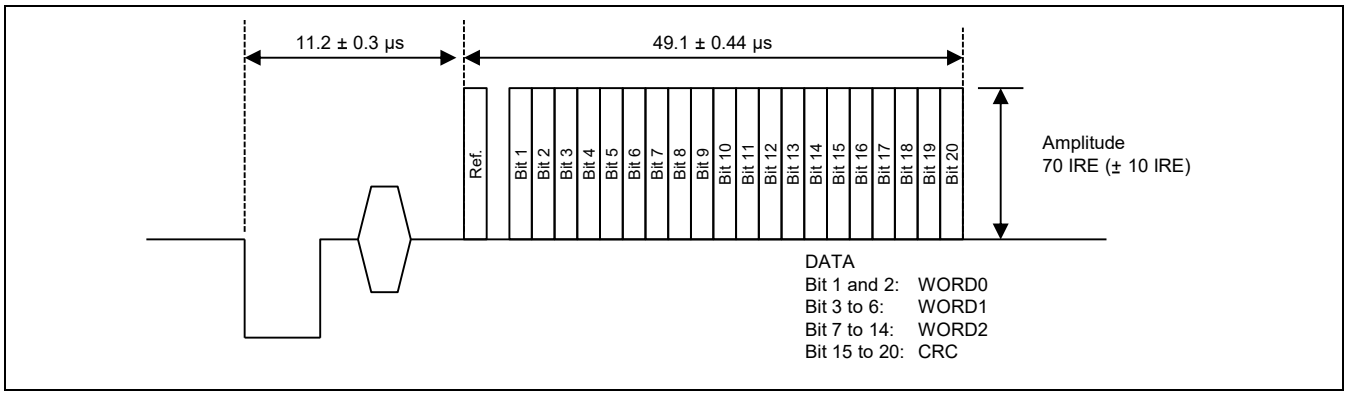


Figure 20A.5 Video ID Signal waveforms

20A.4.11 WSS Addition

This block multiplexes the WSS (Wide Screen Signaling), similar to the progressive case, to line 23 in the luminance signal during a 625-line/50-Hz operation. The multiplexing process can be turned ON/OFF and the WSS data can be set by appropriately setting the WSS and CGWS[13:0] bits. For the WSS data that is actually multiplexed to the output signal, the 14-bit data in the register settings are used to generate data Run-in, Start-code, Aspect-ratio, Enhanced-service, Subtitles, and Others for a total of 43 bits, and the results are modulated and multiplexed.

By setting the ICCCGWS register, the WSS that is multiplexed in the luminance signal can be output as is.

Figure 20A.6 shows an example of a multiplexed WSS signal.

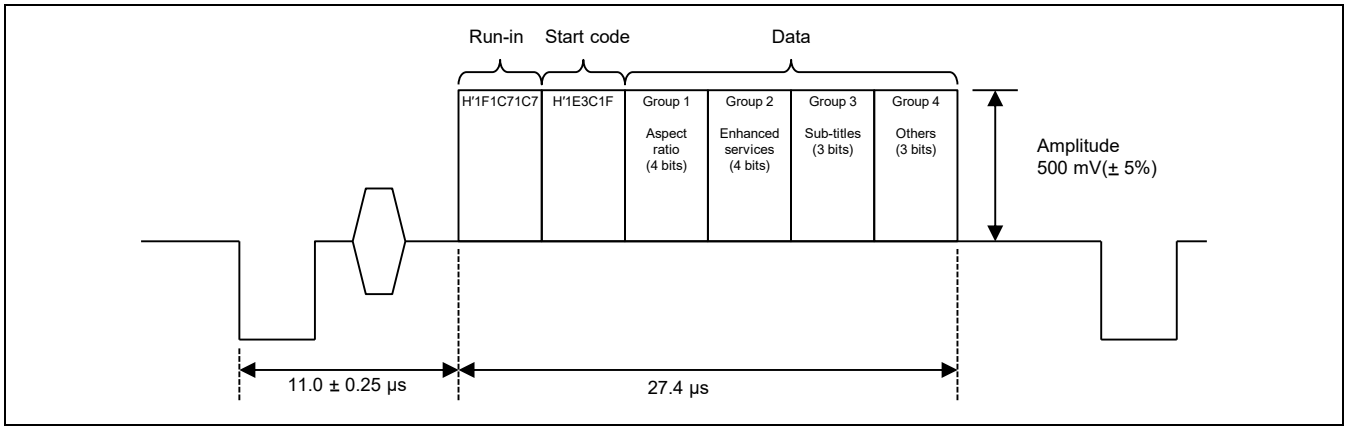


Figure 20A.6 WSS waveforms

20A.4.12 CC Addition

The CC (Closed Caption) signal represents a technology developed for hearing-impaired persons, wherein character information is transmitted by inserting it into NTSC broadcasting signals; it is multiplexed in lines 21/284 of the luminance signal. The CC data that is actually multiplexed to the output signal is created by generating ODD parity from the 7-bit (x4 set) of the register settings, modulating the resulting 8-bit (x4 set) total data, and multiplexing it to lines 21/284. By bit settings, the following functions can be provided:

1. Y1CC[1:0], Y2CC[1:0]: CC multiplexing ON/OFF settings
   (B'00 = OFF, B'01 = set exclusively to field 1, B'10 = set exclusively to field 2, B'11 = set to both fields)
2. y{1,2}cc{10, 11, 20, 21, 30, 31, 40, 41}[6:0]: set CC data
3. y{1,2}ccmode: when ON (1), automatically multiplexes Null codes until a CC updating signal is generated.
4. y{1,2}cc_if: outputs the CC data as is that is multiplexed in the luminance signal.

Figure 20A.7 shows an example of a CC signal that is multiplexed.

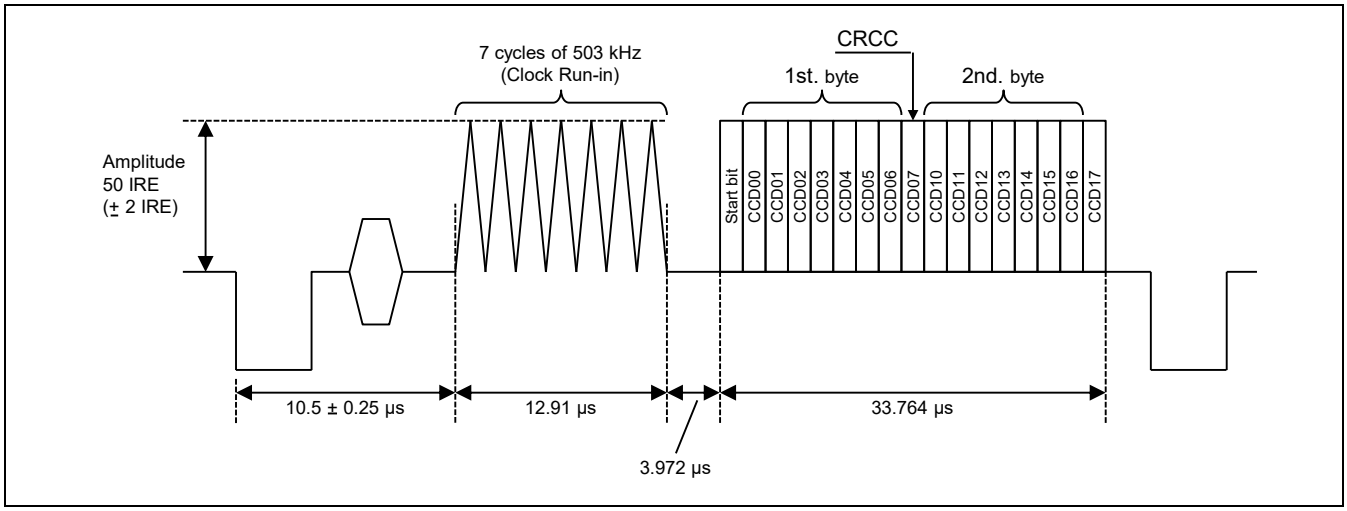


Figure 20A.7 CC Signal waveforms

20A.4.13 Output Gains Adjustment

In order to provide an adequate amount of width to the full-scale voltage compatibility of the DAC, gain adjustments can be performed in the following ranges by the GAIN[9:0] bits ([11:0] for C) and GTHR[15:0] bits (none for C/Cb/Cr):

Y1 = (din - 4(256)) × (1 + IY1GAIN[9:0]/4096) + 4(256)

C = (din - 2048) × (1 + CGAIN[11:0]/4096) + 2048

20A.5 Recommended register values

Recommended values for setting the interlace registers are listed in Table 20A.5.

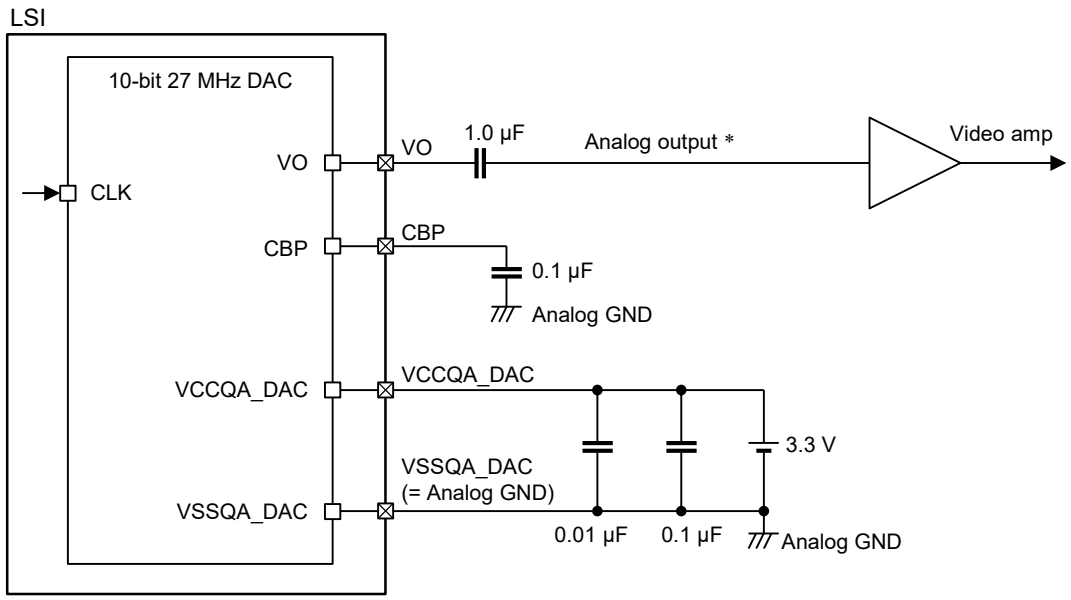
Table 20A.5 is a recommended value of the NTSC/PAL system.

Table 20A.5 Interlace Register Settings

Mnemonic	NTSC(10:4)	PAL-M(10:4)	PAL-60(7:3)	PAL(7:3)	PAL-N(7:3)
IDENCMD1	H'3000	H'3001	H'3031	H'3023	H'3003
IDENCMD2	H'FF00	H'FF00	H'FF00	H'FF00	H'FF00
ITNTBLEV	H'C900	H'D900	H'D700	H'D700	H'D700
IFSCH	H'21F0	H'21E6	H'2A09	H'2A09	H'21F6
IFSCL	H'7C1F	H'EFE3	H'8ACB	H'8ACB	H'9447
IDLYSET	H'0000	H'0000	H'0000	H'0000	H'0000
ISYNSET	H'15DB	H'15DB	H'15EA	H'15EA	H'15EA
ICCCGWS	H'0020	H'0020	H'0020	H'0020	H'0020
ICCD1	H'0000	H'0000	H'0000	H'0000	H'0000
ICCD2	H'0000	H'0000	H'0000	H'0000	H'0000
ICGWSD	H'0000	H'0000	H'0000	H'0000	H'0000
IBLKSHP	H'0000	H'0000	H'0000	H'0000	H'0000
ISHPSET	H'0000	H'0000	H'0000	H'0000	H'0000
IBRTCON	H'0080	H'0080	H'0080	H'0080	H'0080
IHADA	H'0000	H'0000	H'0000	H'0000	H'0000
ITNTCOL	H'0040	H'0040	H'0040	H'0040	H'0040
IBURST	H'4565	H'496B	H'4765	H'4765	H'4765
ICSP	H'003D	H'0042	H'0041	H'0041	H'0041
IY1GAIN	H'0000	H'0000	H'0000	H'0000	H'0000
ICGAIN	H'0000	H'0000	H'0000	H'0000	H'0000

20A.6 Connection Example

Figure 20A.8 shows a pin connection example of DAC.



Note: * A 1.0-µF external capacitor should be connected with VO output by capacitive coupling and input impedance of the connected device should be more than 10 kΩ.
Buffer device like video amplifier is recommended to be connected with capacitor.

Figure 20A.8 Pin Connection Example

20B. Digital Video Decoder

20B.1 Overview

20B.1.1 Features

This LSI incorporates one channel of digital video decoder. This module consists of an A/D converter for video signal input, a sync separator circuit, a burst controlled oscillator (BCO), a 2D Y/C separator circuit, chroma decoding circuit, a digital clamp circuit, and an output gain adjustment circuit. Table 20B.1 shows the digital video decoder functions.

Table 20B.1 Digital Video Decoder Functions

Item	Function
Input signal	Video signal • Composite video signal (CVBS)
Functional outline	• A/D converter for video signal input — VIN1A and VIN2A pin input selection — Low-pass filter (LPF) — Sync tip clamp — Programmable gain amplifier (PGA) (0 to 6.021 dB) — 10-bit precision pipelined A/D converter • Sync separation — Noise reduction LPS, auto level control sync slicer, horizontal auto frequency control (AFC), vertical count-down, interlace detection, auto gain control (AGC)/peak limiter control • Burst controlled oscillator (BCO) — Color sub-carrier reproduction, color system detection (For details, see Table 20B.3.) • Y/C separation (For details, see Table 20B.2.) — Supporting NTSC 2D, PAL 2D, SECAM 1D • Chroma decoding — Supporting NTSC, PAL SECAM — Color killer, auto color control (ACC), TINT correction, R-Y axis correction • Digital clamp — Pedestal clamp (Y), center clamp (Cb/Cr), noise detection • Output gain adjustment — Contrast adjustment: 0 to approx. two times — Color adjustment (Cb/Cr independent): 0 to approx. two times • Selecting input Signals for video input module (VIN) — The input controller selects either video decoder output signals or signals supplied via external input pins.

Table 20B.2 Supported Y/C Separation Operation

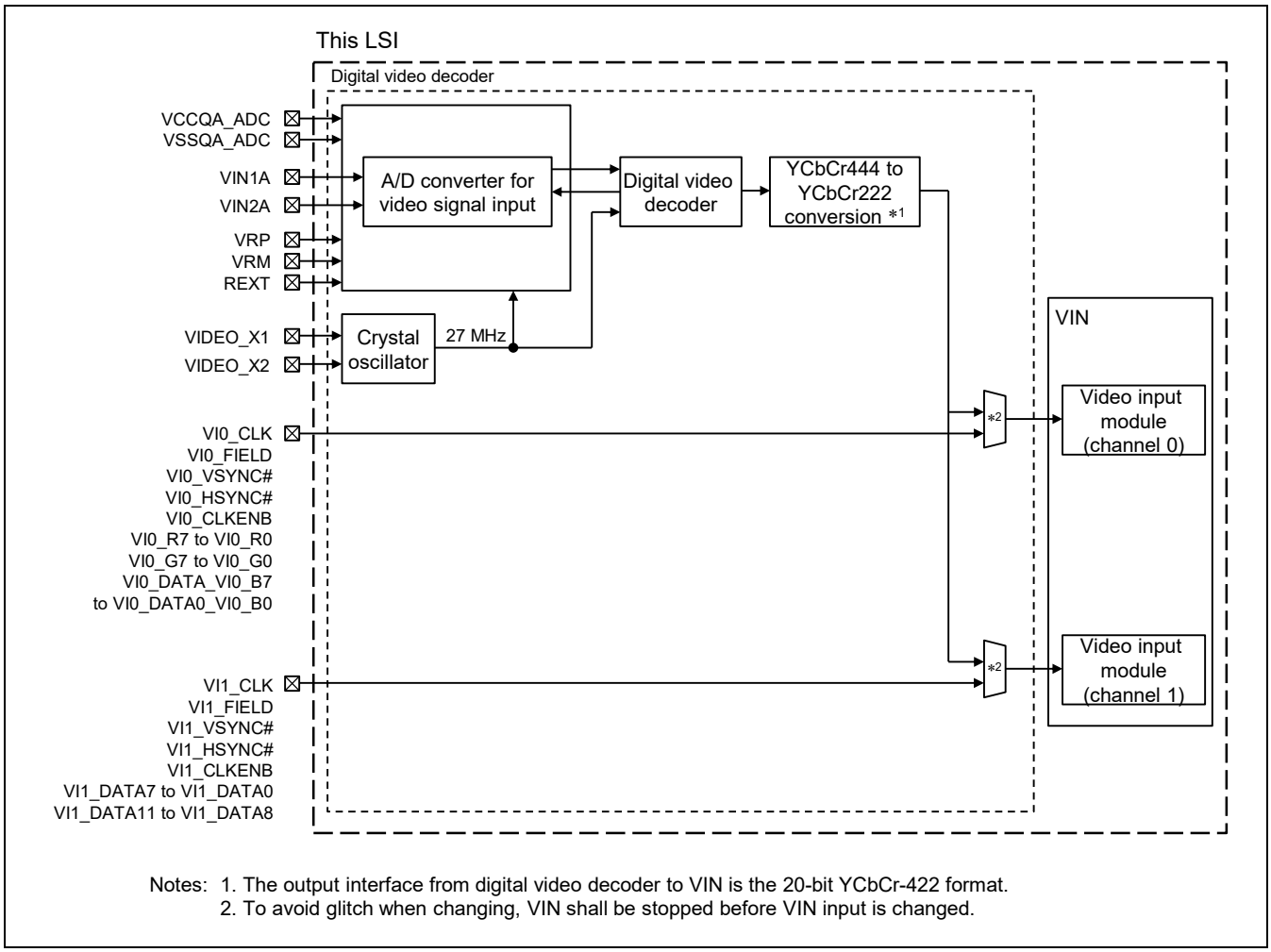
Color System	Y/C Separation Operation
NTSC-3.58	Two dimensional
NTSC-4.43	Two dimensional
PAL-M	Two dimensional
PAL-N	Two dimensional
PAL-4.43	Two dimensional
SECAM	One dimensional

Table 20B.3 Color System Detection

COLORSY[1:0]	FSCMODE	FVMODE	Detection Result
0: NTSC	0: 3.58 MHz	Don't care	NTSC-M
0: NTSC	1: 4.43 MHz	Don't care	NTSC-4.43
1: PAL	0: 3.58 MHz	0: 50 Hz	PAL-N
1: PAL	0: 3.58 MHz	1: 60 Hz	PAL-M
1: PAL	1: 4.43 MHz	0: 50 Hz	PAL-B, H, I, G, D
1: PAL	1: 4.43 MHz	1: 60 Hz	PAL-60
2: SECAM	—	—	SECAM
3: Unknown	—	—	Cannot be detected

20B.1.2 Block Diagram

Figure 20B.1 shows a block diagram of this module.



Notes: 1. The output interface from digital video decoder to VIN is the 20-bit YCbCr-422 format.
2. To avoid glitch when changing, VIN shall be stopped before VIN input is changed.

Figure 20B.1 Block Diagram

Figure 20B.2 shows a block diagram (A/D converter and digital video decoder).

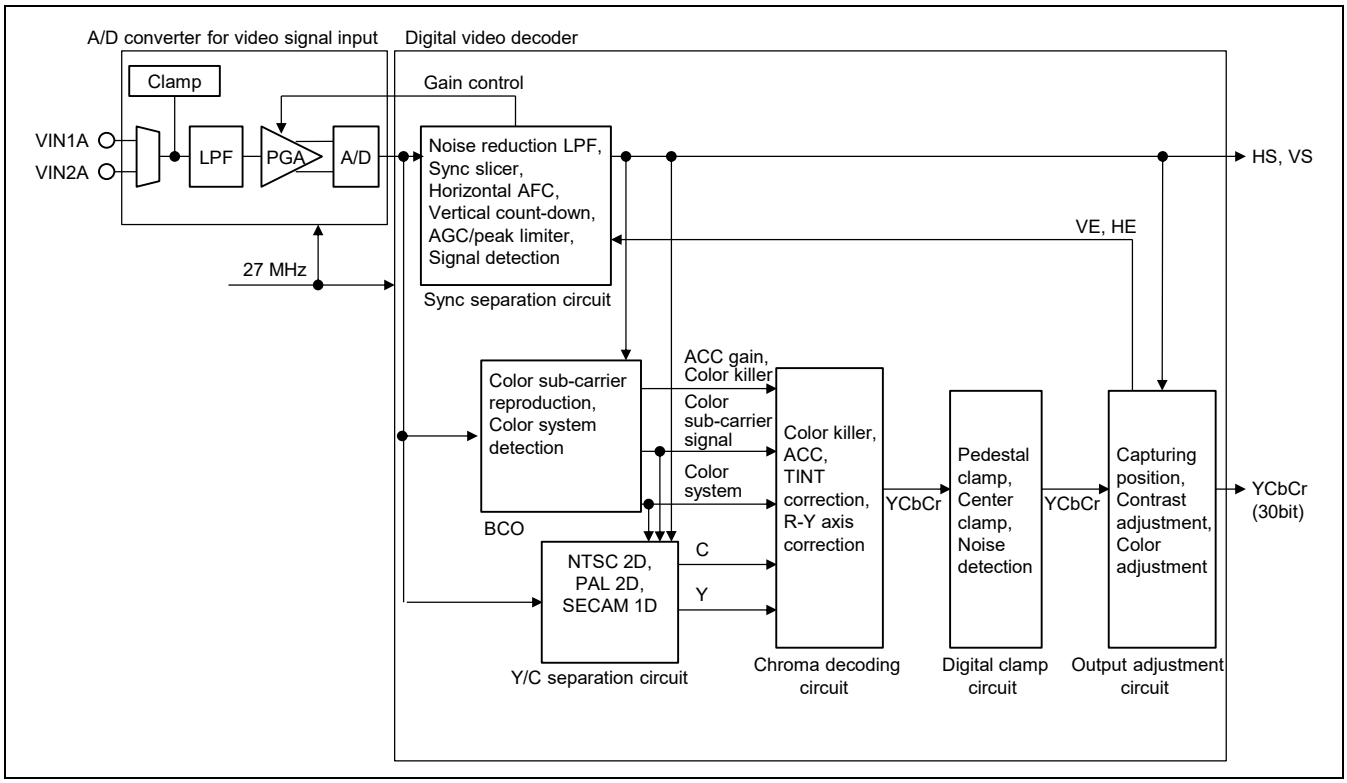


Figure 20B.2 Block Diagram (A/D converter and Digital video decoder)

20B.1.3 Input/Output Pins

Table 20B.4 shows the pin configuration.

Table 20B.4 Pin Configuration

Name	Pin Symbol	I/O	Description
Composite video signal input	VIN1A	Input	Composite video signal (CVBS) input pin 1
	VIN2A	Input	Composite video signal (CVBS) input pin 2
Crystal oscillator/ external clock	VIDEO_X1	Input	Connect to a crystal resonator for the digital video decoder. The VIDEO_X1 pin can also be used for external clock input.
	VIDEO_X2	Output	
TOP reference voltage	VRP	Output	TOP reference voltage pin for the A/D converter for video signal input Connect to the VSSQA_ADC via a 0.1-µF capacitor.
BOTTOM reference voltage	VRM	Output	BOTTOM reference voltage pin for the A/D converter for video signal input Connect to the VSSQA_ADC via a 0.1-µF capacitor.
Reference voltage	REXT	Output	Reference voltage pin for the A/D converter for video signal input Connect to the VSSQA_ADC via a 22-kΩ ±1% resistor.
Analog power supply	VCCQA_ADC	Input	Power supply pin for the A/D converter for video signal input
Analog ground	VSSQA_ADC	Input	Ground pin for the A/D converter for video signal input

20B.1.4 Register Configuration

Table 20B.5 shows the register configuration.

Table 20B.5 Register Configuration

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
ADC control register 1	ADCCR1	R/W	H'FEB81008	H'0000	16
Timing generation control register 1	TGCR1	R/W	H'FEB8100E	H'013C	16
Timing generation control register 2	TGCR2	R/W	H'FEB81010	H'50E8	16
Timing generation control register 3	TGCR3	R/W	H'FEB81012	H'0500	16
Sync separation control register 1	SYNSCR1	R/W	H'FEB8101A	H'6C0A	16
Sync separation control register 2	SYNSCR2	R/W	H'FEB8101C	H'03CA	16
Sync separation control register 3	SYNSCR3	R/W	H'FEB8101E	H'3C92	16
Sync separation control register 4	SYNSCR4	R/W	H'FEB81020	H'03CA	16
Sync separation control register 5	SYNSCR5	R/W	H'FEB81022	H'2C92	16
Horizontal AFC control register 1	HAFCCR1	R/W	H'FEB81024	H'62B4	16
Horizontal AFC control register 2	HAFCCR2	R/W	H'FEB81026	H'02E6	16
Horizontal AFC control register 3	HAFCCR3	R/W	H'FEB81028	H'8A82	16
Vertical countdown control register 1	VCDWCR1	R/W	H'FEB8102A	H'028A	16
Digital clamp control register 1	DCPCR1	R/W	H'FEB81030	H'8000	16
Digital clamp control register 2	DCPCR2	R/W	H'FEB81032	H'0000	16
Digital clamp control register 3	DCPCR3	R/W	H'FEB81034	H'5000	16
Digital clamp control register 4	DCPCR4	R/W	H'FEB81036	H'4000	16
Digital clamp control register 5	DCPCR5	R/W	H'FEB81038	H'4000	16
Digital clamp control register 6	DCPCR6	R/W	H'FEB8103A	H'3600	16
Digital clamp control register 7	DCPCR7	R/W	H'FEB8103C	H'A200	16
Digital clamp control register 8	DCPCR8	R/W	H'FEB8103E	H'1B00	16
Noise detection control register	NSDCR	R/W	H'FEB81040	H'0000	16
Burst lock/chroma decoding control register	BTLCR	R/W	H'FEB81042	H'5800	16
Burst gate pulse control register	BTGPCR	R/W	H'FEB81044	H'2482	16
ACC control register 1	ACCCR1	R/W	H'FEB81046	H'8124	16
ACC control register 2	ACCCR2	R/W	H'FEB81048	H'0100	16
ACC control register 3	ACCCR3	R/W	H'FEB8104A	H'5412	16
TINT control register	TINTCR	R/W	H'FEB8104C	H'0000	16
Y/C delay/chroma decoding control register	YCDCR	R/W	H'FEB8104E	H'0002	16
AGC control register 1	AGCCR1	R/W	H'FEB81050	H'0AEC	16
AGC control register 2	AGCCR2	R/W	H'FEB81052	H'CA40	16
Peak limiter control register	PKLIMITCR	R/W	H'FEB81054	H'2000	16
Over-range control register 1	RGORCR1	R/W	H'FEB81056	H'03FF	16
Over-range control register 2	RGORCR2	R/W	H'FEB81058	H'0000	16
Over-range control register 3	RGORCR3	R/W	H'FEB8105A	H'03FF	16
Over-range control register 4	RGORCR4	R/W	H'FEB8105C	H'0000	16
Over-range control register 5	RGORCR5	R/W	H'FEB8105E	H'03FF	16
Over-range control register 6	RGORCR6	R/W	H'FEB81060	H'0000	16

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
Over-range control register 7	RGORCR7	R/W	H'FEB81062	H'0001	16
Feedback control register for horizontal AFC phase comparator	AFCPFCR	R/W	H'FEB8107C	H'0005	16
Register update enable register	RUPDCR	R/W	H'FEB8107E	H'0000	16
Sync separation status/vertical cycle read register	VSYNCSR	R	H'FEB81080	H'0000	16
Horizontal cycle read register	HSYNCSR	R	H'FEB81082	H'0000	16
Digital clamp read register 1	DCPSR1	R	H'FEB81084	H'0000	16
Digital clamp read register 2	DCPSR2	R	H'FEB81086	H'0000	16
Noise detection read register	NSDSR	R	H'FEB8108C	H'0000	16
Chroma decoding read register 1	CROMASR1	R	H'FEB8108E	H'0000	16
Chroma decoding read register 2	CROMASR2	R	H'FEB81090	H'0000	16
Sync separation read register	SYNCSSR	R	H'FEB81092	H'0000	16
AGC control read register 1	AGCCSR1	R	H'FEB81094	H'0000	16
AGC control read register 2	AGCCSR2	R	H'FEB81096	H'0040	16
Y/C separation control register 3	YCSCR3	R/W	H'FEB81104	H'2204	16
Y/C separation control register 4	YCSCR4	R/W	H'FEB81106	H'3401	16
Y/C separation control register 5	YCSCR5	R/W	H'FEB81108	H'4006	16
Y/C separation control register 6	YCSCR6	R/W	H'FEB8110A	H'1006	16
Y/C separation control register 7	YCSCR7	R/W	H'FEB8110C	H'6325	16
Y/C separation control register 8	YCSCR8	R/W	H'FEB8110E	H'C000	16
Y/C separation control register 9	YCSCR9	R/W	H'FEB81110	H'8000	16
Y/C separation control register 11	YCSCR11	R/W	H'FEB81114	H'D803	16
Y/C separation control register 12	YCSCR12	R/W	H'FEB81116	H'0605	16
Digital clamp control register 9	DCPCR9	R/W	H'FEB81180	H'FC00	16
Chroma filter TAP coefficient (WA_F0) register for Y/C separation	YCTWA_F0	R/W	H'FEB81192	H'0018	16
Chroma filter TAP coefficient (WA_F1) register for Y/C separation	YCTWA_F1	R/W	H'FEB81194	H'002C	16
Chroma filter TAP coefficient (WA_F2) register for Y/C separation	YCTWA_F2	R/W	H'FEB81196	H'0014	16
Chroma filter TAP coefficient (WA_F3) register for Y/C separation	YCTWA_F3	R/W	H'FEB81198	H'1034	16
Chroma filter TAP coefficient (WA_F4) register for Y/C separation	YCTWA_F4	R/W	H'FEB8119A	H'1080	16
Chroma filter TAP coefficient (WA_F5) register for Y/C separation	YCTWA_F5	R/W	H'FEB8119C	H'1080	16
Chroma filter TAP coefficient (WA_F6) register for Y/C separation	YCTWA_F6	R/W	H'FEB8119E	H'100C	16
Chroma filter TAP coefficient (WA_F7) register for Y/C separation	YCTWA_F7	R/W	H'FEB811A0	H'0084	16
Chroma filter TAP coefficient (WA_F8) register for Y/C separation	YCTWA_F8	R/W	H'FEB811A2	H'00C8	16
Chroma filter TAP coefficient (WB_F0) register for Y/C separation	YCTWB_F0	R/W	H'FEB811A4	H'100C	16
Chroma filter TAP coefficient (WB_F1) register for Y/C separation	YCTWB_F1	R/W	H'FEB811A6	H'0028	16

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
Chroma filter TAP coefficient (WB_F2) register for Y/C separation	YCTWB_F2	R/W	H'FEB811A8	H'003C	16
Chroma filter TAP coefficient (WB_F3) register for Y/C separation	YCTWB_F3	R/W	H'FEB811AA	H'000C	16
Chroma filter TAP coefficient (WB_F4) register for Y/C separation	YCTWB_F4	R/W	H'FEB811AC	H'1068	16
Chroma filter TAP coefficient (WB_F5) register for Y/C separation	YCTWB_F5	R/W	H'FEB811AE	H'109C	16
Chroma filter TAP coefficient (WB_F6) register for Y/C separation	YCTWB_F6	R/W	H'FEB811B0	H'1040	16
Chroma filter TAP coefficient (WB_F7) register for Y/C separation	YCTWB_F7	R/W	H'FEB811B2	H'0078	16
Chroma filter TAP coefficient (WB_F8) register for Y/C separation	YCTWB_F8	R/W	H'FEB811B4	H'00D0	16
Chroma filter TAP coefficient (NA_F0) register for Y/C separation	YCTNA_F0	R/W	H'FEB811B6	H'0018	16
Chroma filter TAP coefficient (NA_F1) register for Y/C separation	YCTNA_F1	R/W	H'FEB811B8	H'002C	16
Chroma filter TAP coefficient (NA_F2) register for Y/C separation	YCTNA_F2	R/W	H'FEB811BA	H'0014	16
Chroma filter TAP coefficient (NA_F3) register for Y/C separation	YCTNA_F3	R/W	H'FEB811BC	H'1034	16
Chroma filter TAP coefficient (NA_F4) register for Y/C separation	YCTNA_F4	R/W	H'FEB811BE	H'1080	16
Chroma filter TAP coefficient (NA_F5) register for Y/C separation	YCTNA_F5	R/W	H'FEB811C0	H'1080	16
Chroma filter TAP coefficient (NA_F6) register for Y/C separation	YCTNA_F6	R/W	H'FEB811C2	H'100C	16
Chroma filter TAP coefficient (NA_F7) register for Y/C separation	YCTNA_F7	R/W	H'FEB811C4	H'0084	16
Chroma filter TAP coefficient (NA_F8) register for Y/C separation	YCTNA_F8	R/W	H'FEB811C6	H'00C8	16
Chroma filter TAP coefficient (NB_F0) register for Y/C separation	YCTNB_F0	R/W	H'FEB811C8	H'1438	16
Chroma filter TAP coefficient (NB_F1) register for Y/C separation	YCTNB_F1	R/W	H'FEB811CA	H'0AF0	16
Chroma filter TAP coefficient (NB_F2) register for Y/C separation	YCTNB_F2	R/W	H'FEB811CC	H'1CEC	16
Chroma filter TAP coefficient (NB_F3) register for Y/C separation	YCTNB_F3	R/W	H'FEB811CE	H'065C	16
Chroma filter TAP coefficient (NB_F4) register for Y/C separation	YCTNB_F4	R/W	H'FEB811D0	H'05A4	16
Chroma filter TAP coefficient (NB_F5) register for Y/C separation	YCTNB_F5	R/W	H'FEB811D2	H'1CEC	16
Chroma filter TAP coefficient (NB_F6) register for Y/C separation	YCTNB_F6	R/W	H'FEB811D4	H'085C	16
Chroma filter TAP coefficient (NB_F7) register for Y/C separation	YCTNB_F7	R/W	H'FEB811D6	H'0178	16
Chroma filter TAP coefficient (NB_F8) register for Y/C separation	YCTNB_F8	R/W	H'FEB811D8	H'1568	16
Luminance (Y) signal gain control register	YGAINCR	R/W	H'FEB81200	H'0200	16

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
Color difference (Cb) signal gain control register	CBGAINCR	R/W	H'FEB81202	H'0200	16
Color difference (Cr) signal gain control register	CRGAINCR	R/W	H'FEB81204	H'0200	16
PGA register update	PGA_UPDATE	R/W	H'FEB81280	H'0001	16
PGA control register	PGACR	R/W	H'FEB81282	H'1508	16
ADC control register 2	ADCCR2	R/W	H'FEB81284	H'0000	16
ADC control register 3	ADCCR3	R/W	H'FEB81286	H'0210	16
ADC control register 4	ADCCR4	R/W	H'E60600CC	H'00000000	32

20B.2 Register Description

20B.2.1 ADC Control Register 1 (ADCCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	AGC MODE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	AGCMODE	0	R/W	A/D Converter AGC ON/OFF Control 0: AGC OFF 1: AGC ON
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) AGC Control

The AGCMODE bit controls the AGC ON/OFF. When AGCMODE is 1, the AGC operation is performed by detecting the sync amplitude and video peak amplitude and controlling the PGA gain of the ADC.

When PGACR.PGA_GAIN_SEL is 1, the PGA gain can be directly controlled with the PGACR.PGA_GAIN value. At this time, the AGCMODE setting is invalid.

Setting AGCMODE to 0 and PGACR.PGA_GAIN_SEL to 0 simultaneously is prohibited.

20B.2.2 Timing Generation Control Register 1 (TGCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SRCLEFT[8:0]								
Initial value:	0	0	0	0	0	0	0	1	0	0	1	1	1	1	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SRCLEFT[8:0]	H'13C	R/W	Left End of Input Video Signal Capturing Area Set the position from the horizontal sync reference in 27-MHz clock cycle units.

(1) Timing Generation (Horizontal Start Position) Control

SRCLEFT sets the start position of the horizontal enable signal of the output video signal from the horizontal sync reference in 27-MHz clock cycle units.

20B.2.3 Timing Generation Control Register 2 (TGCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRCTOP[5:0]						SRCHEIGHT[9:0]									
Initial value:	0	1	0	1	0	0	0	0	1	1	1	0	1	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	SRCTOP[5:0]	H'14	R/W	Top End of Input Video Signal Capturing Area Set the position from the vertical sync reference in one-line units.
9 to 0	SRCHEIGHT [9:0]	H'0E8	R/W	Height of Input Video Signal Capturing Area Set the vertical active period in one-line units.

Note: All the bits in this register are updated when the vertical sync signal is asserted with the NEWSETTING bit in RUPDCR being 1.

(1) Timing Generation (Vertical Start Position) Control

SRCTOP sets the start position of the vertical enable signal of the output video signal from the vertical sync reference in one-line units.

(2) Timing Generation (Vertical Width) Control

SRCHEIGHT sets the height of the vertical enable signal of the output video signal in one-line units.

20B.2.4 Timing Generation Control Register 3 (TGCR3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SRCWIDTH[10:0]										
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SRCWIDTH [10:0]	H'500	R/W	Width of Input Video Signal Capturing Area Set the horizontal active period in 27-MHz clock cycle units.

Note: All the bits in this register are updated when the vertical sync signal is asserted with the NEWSETTING bit in RUPDCR being 1.

(1) Timing Generation (Horizontal Width) Control

SRCHEIGHT sets the width of horizontal enable signal of the output video signal in 27-MHz clock cycle units.

Figure 20B.3 to Figure 20B.7 show the timings generated with the NTSC (59.94 Hz) and PAL/SECAM (50.00 Hz) formats.

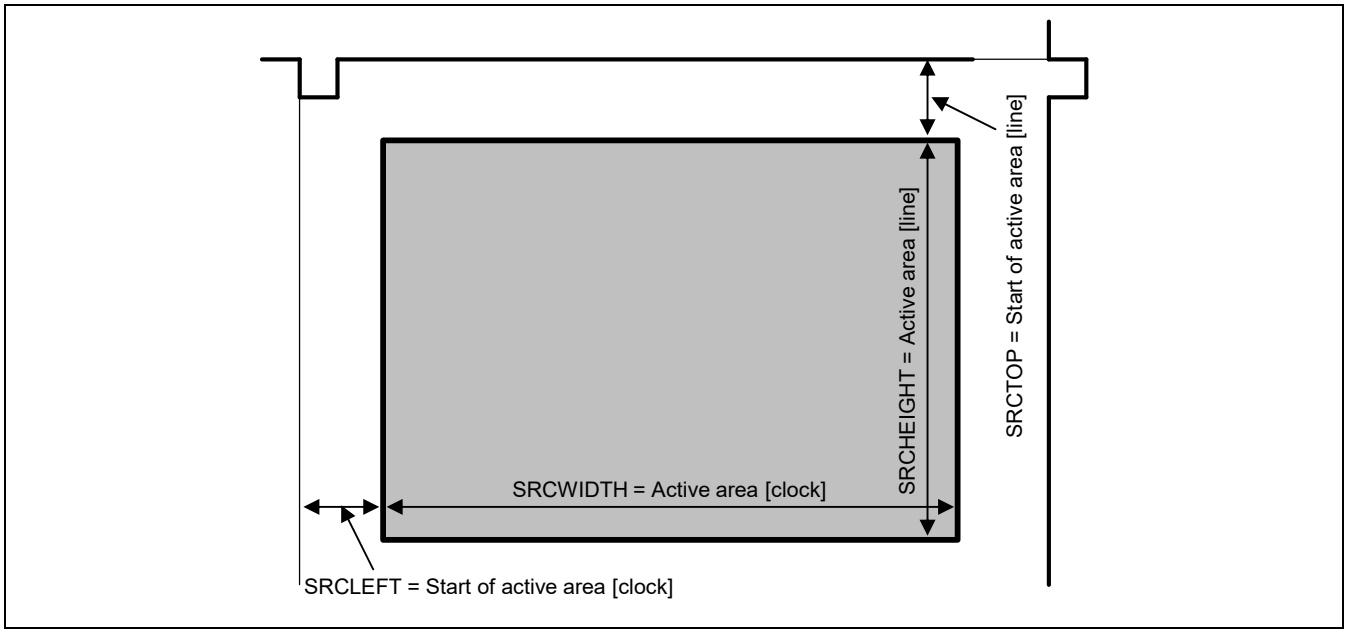


Figure 20B.3 Active Image Area Setting

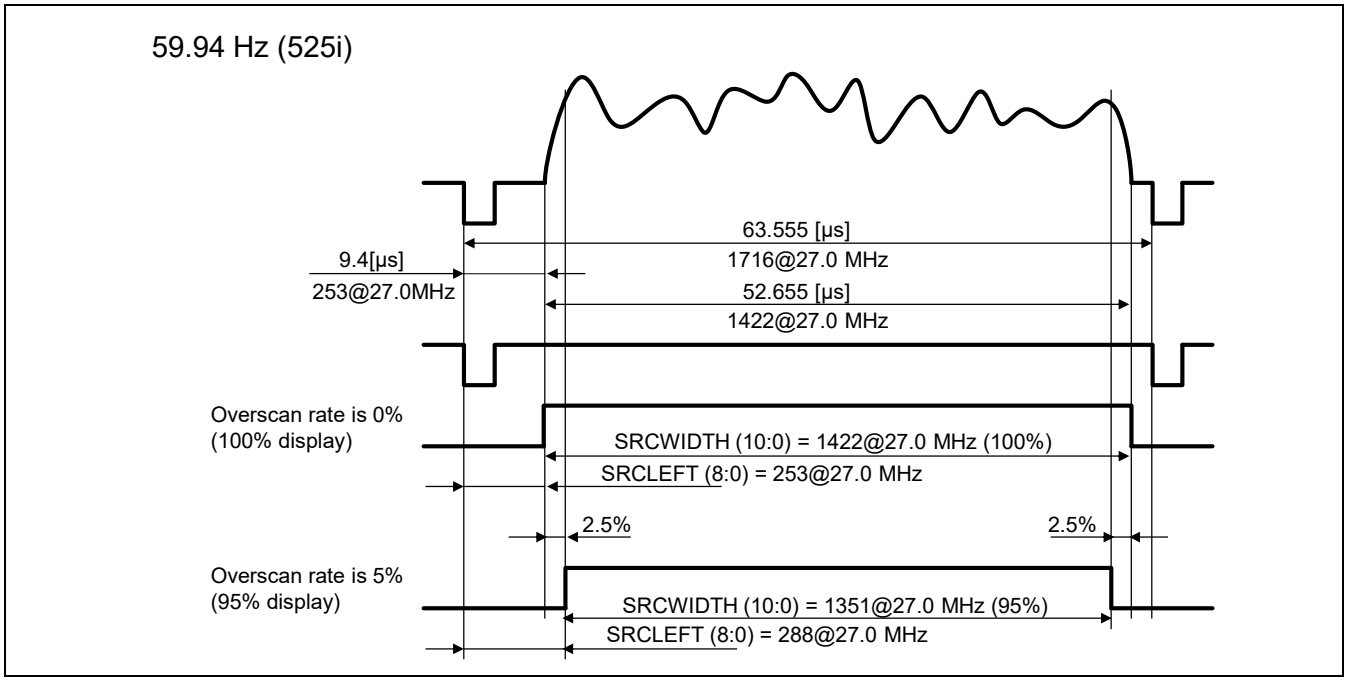


Figure 20B.4 Example of Horizontal Active Image Period (59.94 Hz (525i))

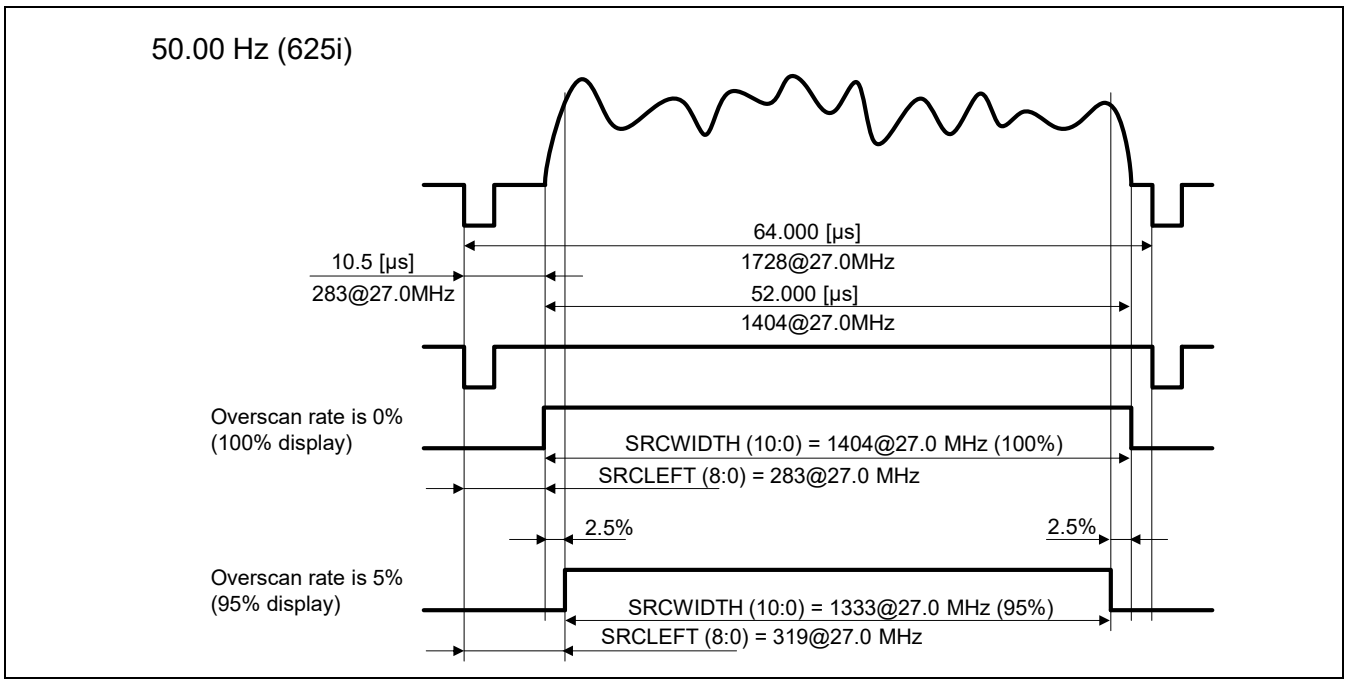


Figure 20B.5 Example of Horizontal Active Image Period (50.00 Hz (625i))

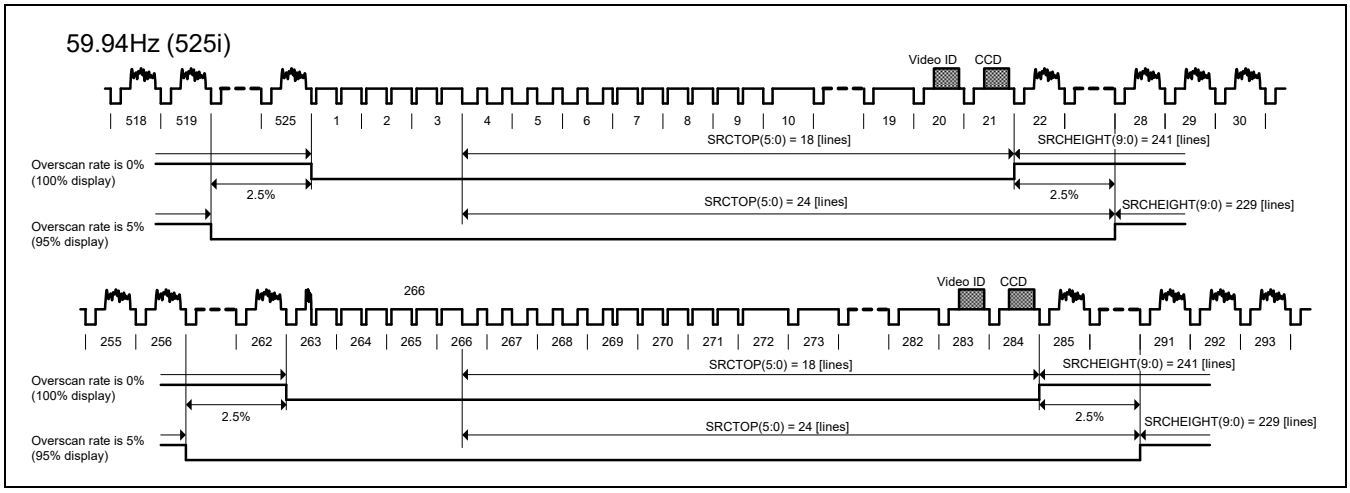


Figure 20B.6 Example of Vertical Active Image Period (59.94 Hz (525i))

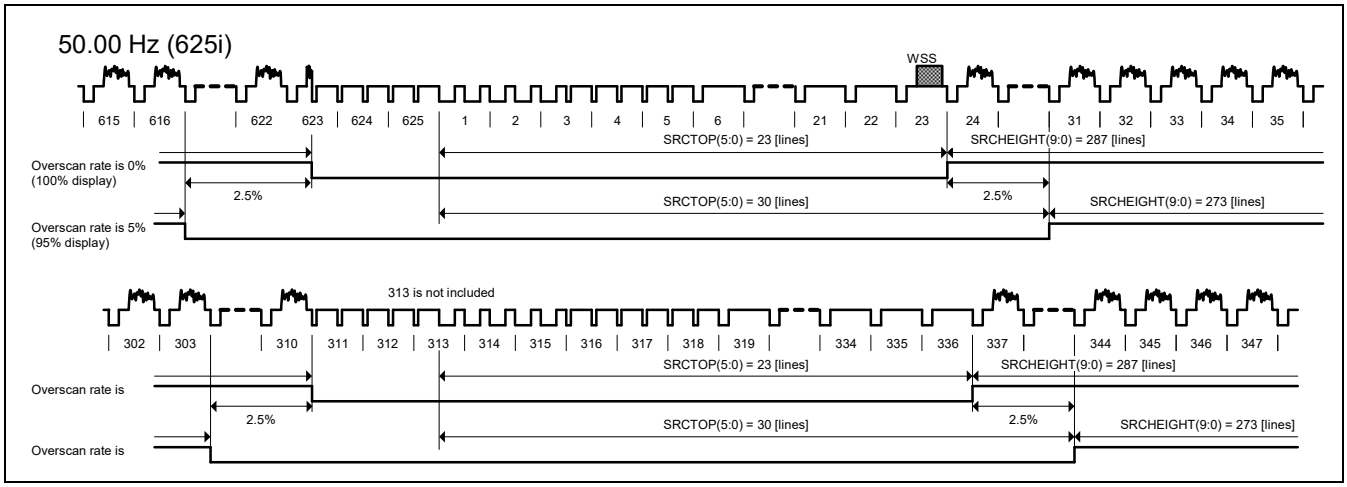
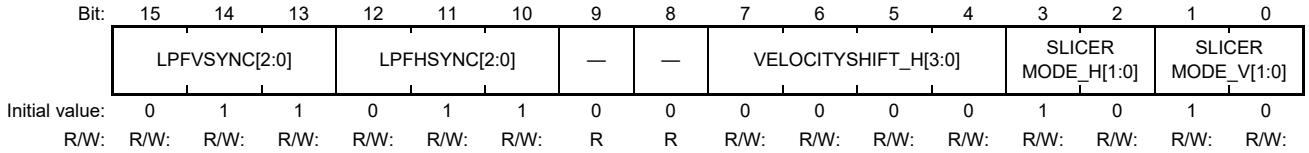


Figure 20B.7 Example of Vertical Active Image Period (50.00 Hz (625i))

The active period width should not be larger than necessary.

The settings of TGCR1 to TGCR3 such as valid period setting for the peak limiter are applied only to this module. To set the display size of the input video, SCL0_DS2 and SCL0_DS3 of the video display controller 5 scaler should be used.

20B.2.5 Sync Separation Control Register 1 (SYNSCR1)



Bit	Bit Name	Initial Value	R/W	Description
15 to 13	LPFVSYNC[2:0]	011	R/W	Low-Pass Filter Cutoff Frequency before Vertical Sync Separation 000: None 001: 0.94 MHz 010: 0.67 MHz 011: 0.54 MHz 100: 0.47 MHz 101: 0.34 MHz 110: 0.27 MHz 111: 0.23 MHz
12 to 10	LPFHSYNC[2:0]	011	R/W	Low-Pass Filter Cutoff Frequency before Horizontal Sync Separation 000: None 001: 2.15 MHz 010: 1.88 MHz 011: 1.34 MHz 100: 1.07 MHz 101: 0.94 MHz 110: 0.67 MHz 111: 0.54 MHz
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	VELOCITYSHIFT_H[3:0]	0000	R/W	Reference Level Operation Speed Control for Composite Sync Separation (for horizontal sync signal) 0000: ×1 0001: ×2 0010: ×4 0011: ×8 0100: ×16 0101: ×32 0110: ×64 0111: ×128 Others: ×256 Standard speed (×1) ↔ High speed (×256)
3, 2	SLICERMODE_H[1:0]	10	R/W	Auto-Slice Level Setting for Composite Sync Separation Circuit (for horizontal sync signal) 00: Manual setting by CSYNCSLICE_H 01: 25% of sync depth (Auto) 10: 50% of sync depth (Auto) 11: 75% of sync depth (Auto)

Bit	Bit Name	Initial Value	R/W	Description
1, 0	SLICERMODE_V [1:0]	10	R/W	Auto-Slice Level Setting for Composite Sync Separation Circuit (for vertical sync signal) 00: Manual setting by CSYNCSLICE_V 01: 25% of sync depth (Auto) 10: 50% of sync depth (Auto) 11: 75% of sync depth (Auto)

(1) Low-Pass Filter Control before Vertical Sync Separation

LPFVSYNC sets the noise reduction low-pass filter for the input video signal fed to a sync separator in order to avoid sync separation error caused by noise. A low-pass filter cutoff frequency should be set not to deteriorate (i.e. to enable to detect) the composite sync signal components.

Table 20B.6 Low-Pass Filter Cutoff Frequency before Vertical Sync Separation

For Vertical Sync Separation

LPFVSYNC[2:0]	t	fc (MHz)
000	—	—
001	0.109375	0.939647766
010	0.078125	0.671176976
011	0.0625	0.536941581
100	0.0546875	0.469823883
101	0.0390625	0.335588488
110	0.003125	0.26847079
111	0.0273438	0.234911942

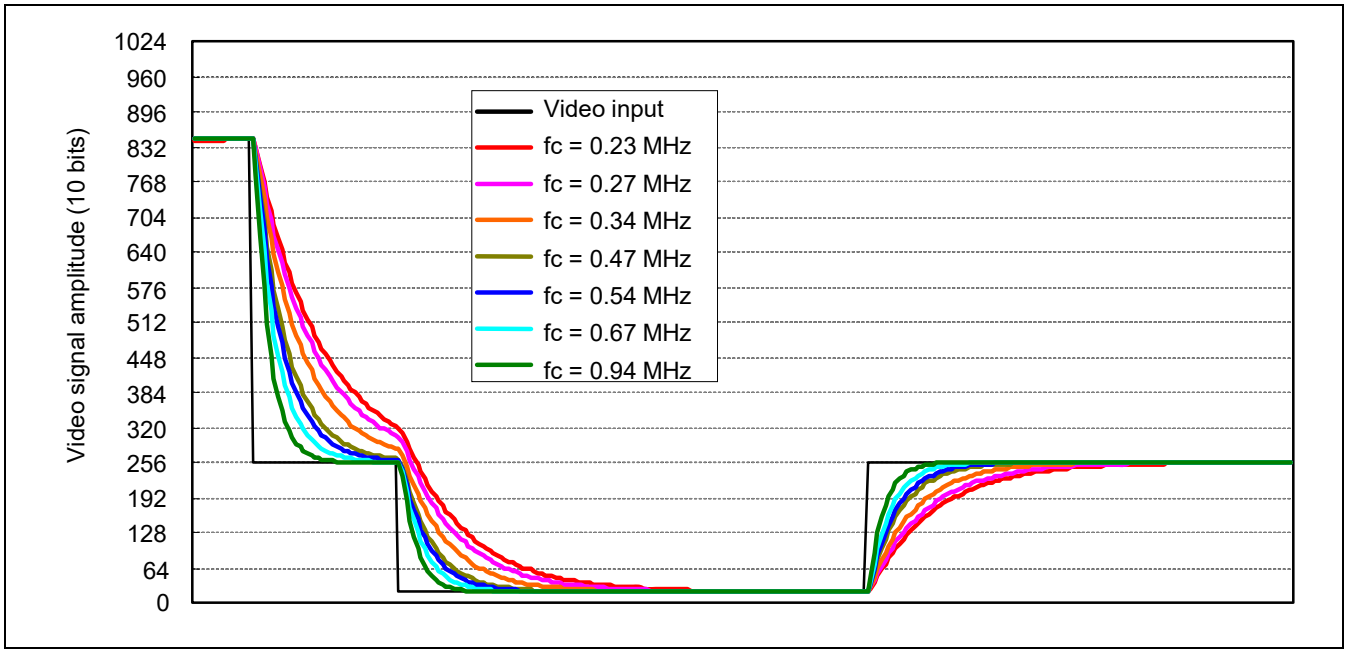


Figure 20B.8 Low-Pass Filter Output Waveform near Vertical Sync Signal during 100% White Signal Input (Vertical: Pattern Diagram)

(2) Low-Pass Filter Control before Horizontal Sync Separation

LPFHSYNC sets the noise reduction low-pass filter for the input video signal fed to a sync separator in order to avoid sync separation error caused by noise. A low-pass filter cutoff frequency should be set not to deteriorate (i.e. to enable to detect) the composite sync signal components.

Table 20B.7 Low-Pass Filter Cutoff Frequency before Horizontal Sync Separation

For Horizontal Sync Separation

LPFHSYNC[2:0]	t	fc (MHz)
000	—	—
001	0.25	2.147766323
010	0.21875	1.879295533
011	0.15625	1.342353952
100	0.125	1.073883162
101	0.10938	0.939647766
110	0.07813	0.671176976
111	0.0625	0.536941581

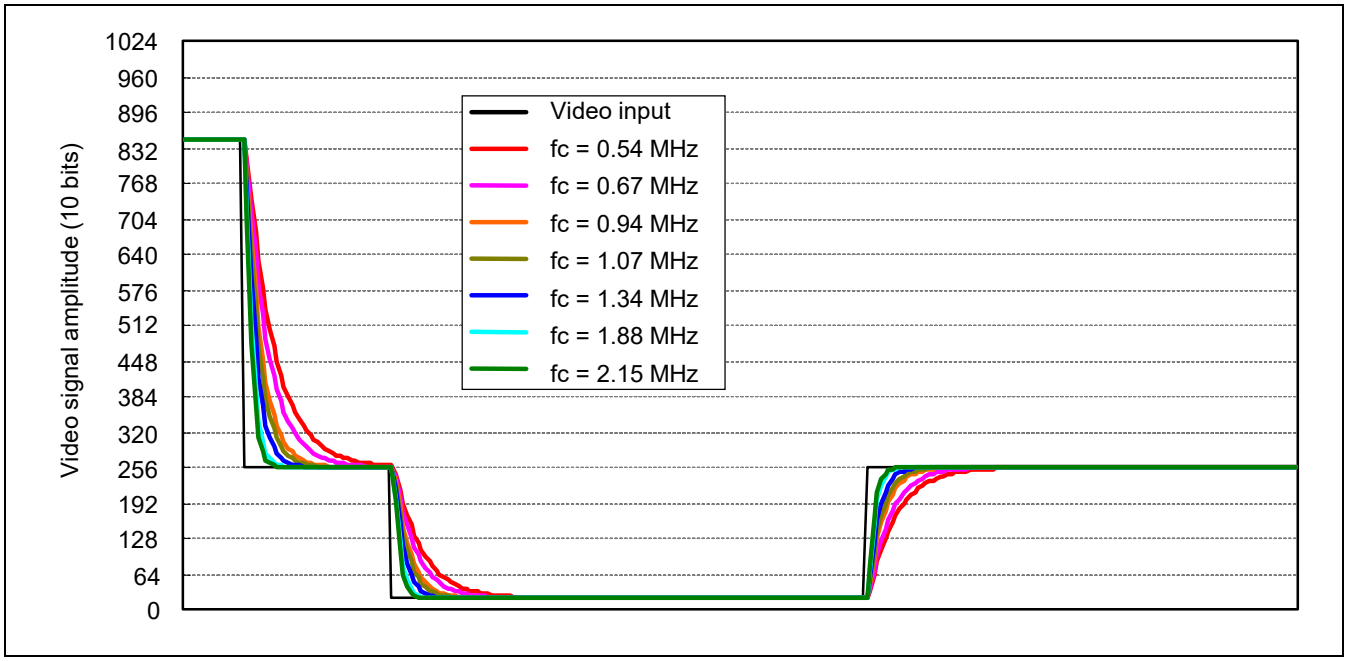


Figure 20B.9 Low-Pass Filter Output Waveform near Horizontal Sync Signal during 100% White Signal Input (Horizontal: Pattern Diagram)

(3) Reference Level Operation Speed Control for Sync Separation

VELOCITYSHIFT_H controls the speed for automatically determining the slice level.

If sync skew is caused by sync sag, it can be improved by raising the determination speed using VELOCITYSHIFT_H.

(4) Horizontal Sync Slicer Control

SLICERMODE_H controls composite sync signal separation from the video signals.

The slice level for composite sync signal separation can be set either manually or automatically. When automatic setting is used, the level is automatically set using the sync signal amplitude detection result, which is described later. The sync slicer can be controlled separately for horizontal and vertical sync signals.

(5) Vertical Sync Slicer Control

SLICERMODE_V controls composite sync signal separation from the video signals.

The slice level for composite sync signal separation can be set either manually or automatically. When automatic setting is used, the level is automatically set using the sync signal amplitude detection result, which is described later. The sync slicer can be controlled separately for horizontal and vertical sync signals.

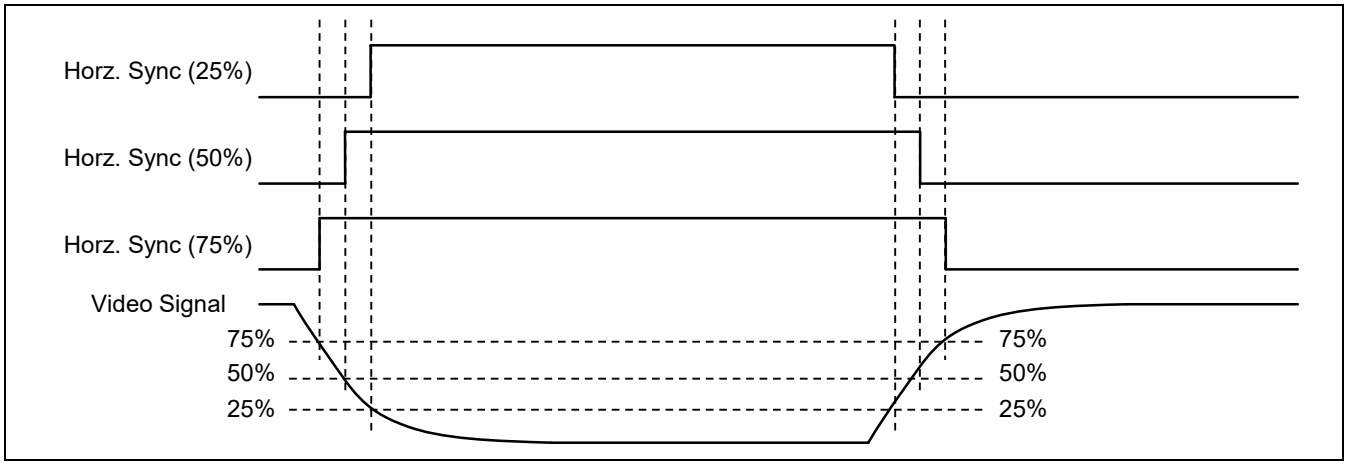


Figure 20B.10 Auto Slice Level Setting

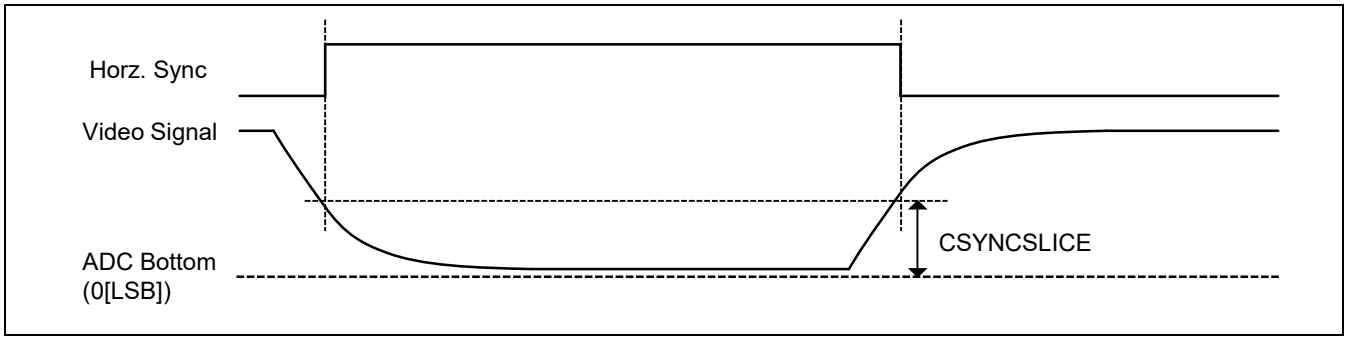
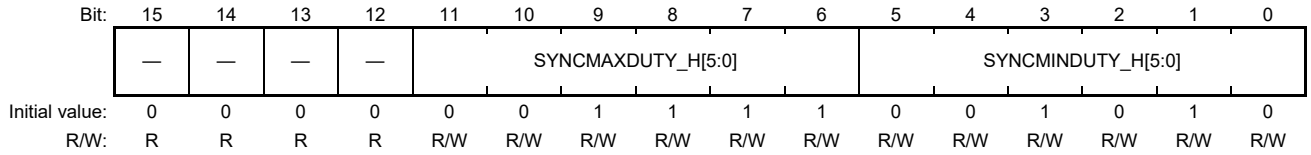


Figure 20B.11 Manual Slice Level Setting

20B.2.6 Sync Separation Control Register 2 (SYNSCR2)



Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 6	SYNCMAXDUTY_H [5:0]	001111	R/W	Max Ratio of Horizontal Cycle to Horizontal Sync Signal Pulse Width Valid when auto slice level setting is active (SLICERMODE_H ≠ 0).
5 to 0	SYNCMINDUTY_H [5:0]	001010	R/W	Min Ratio of Horizontal Cycle to Horizontal Sync Signal Pulse Width Valid when auto slice level setting is active (SLICERMODE_H ≠ 0).

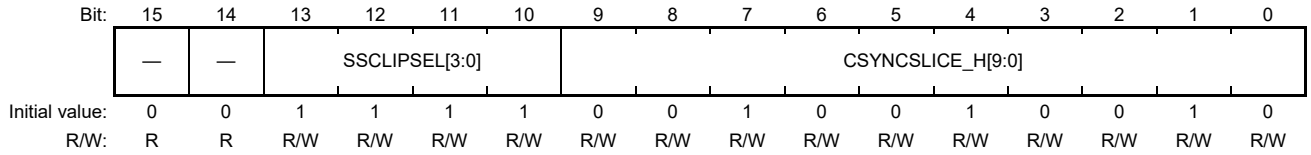
(1) Sync Amplitude Detection Control for Horizontal Sync Separation

SYNCMAXDUTY_H and SYNCMINDUTY_H control the sync signal amplitude detection of composite sync signal included in the video signal.

Table 20B.8 Auto Slice Level Register Settings for Composite Sync Separation

	Horizontal Period (µsec)	Horizontal Sync Width (µsec)	Video Active Period (µsec)	Horizontal Blanking Interval (µsec)	SYNCMAXDUTY_H [5:0] Recommended Value	SYNCMINDUTY_H [5:0] Recommended Value
525i/59.94 Hz	63.56	4.70	52.66	10.90	001111	001010
625i/50 Hz	64.00	4.70	52.00	12.00	001111	001010

20B.2.7 Sync Separation Control Register 3 (SYNSCR3)



Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 10	SSCLIPSEL[3:0]	1111	R/W	Clipping Level Clip the video signal supplied to the vertical/horizontal sync separation low-pass filter Bit value = Clipping level (amplitude 50% to no clipping) 0000: 512, 0001: 546 0010: 580, 0011: 614 0100: 648, 0101: 682 0110: 716, 0111: 750 1000: 785, 1001: 819 1010: 853, 1011: 887 1100: 921, 1101: 955 1110: 989, 1111: 1023
9 to 0	CSYNCSLICE_H[9:0]	0010010010	R/W	Slice Level for Composite Sync Signal Separation (for horizontal sync signal) Valid when manual slice level setting is active (SLICERMODE_H = 0).

(1) Video Signal Clipping Setting for Sync Separation

For input video signals supplied to the sync separator circuit, the level to clip the high tone component of the video signal is specified to reduce amplitude-dependency of the video signal. The video clipping level should be set not to deteriorate (i.e. to enable to detect) the composite sync signal components.

(2) Slice Level Setting for Horizontal Sync Separation

CSYNCSLICE_H sets the slice level for sync separation. This bit is valid only when SLICERMODE_H = 0.

20B.2.8 Sync Separation Control Register 4 (SYNSCR4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SYNCMAXDUTY_V[5:0]						SYNCMINDUTY_V[5:0]					
Initial value:	0	0	0	0	0	0	1	1	1	1	0	0	1	0	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 6	SYNCMAXDUTY_V [5:0]	001111	R/W	Max Ratio of Horizontal Cycle to Vertical Sync Signal Pulse Width Valid when auto slice level setting is active (SLICERMODE_V ≠ 0).
5 to 0	SYNCMINDUTY_V [5:0]	001010	R/W	Min Ratio of Horizontal Cycle to Horizontal Sync Signal Pulse Width Valid when auto slice level setting is active (SLICERMODE_V ≠ 0).

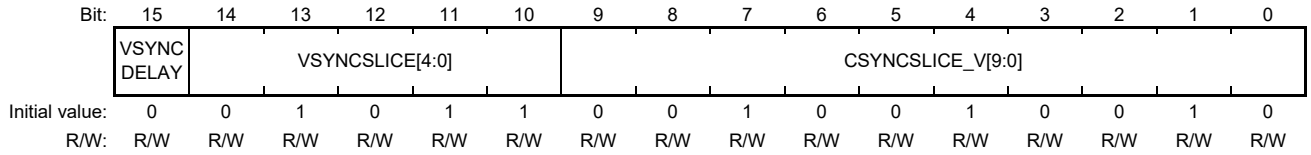
(1) Sync Amplitude Detection Control for Vertical Sync Separation

SYNCMAXDUTY_V and SYNCMINDUTY_V control the sync signal amplitude detection of composite sync signal included in the video signal.

Table 20B.9 Auto Slice Level Register Settings for Composite Sync Separation

	Horizontal Period (µsec)	Horizontal Sync Width (µsec)	Video Active Period (µsec)	Horizontal Blanking Interval (µsec)	SYNCMAXDUTY_V [5:0] Recommended Value	SYNCMINDUTY_V [5:0] Recommended Value
525i59.94 Hz	63.56	4.70	52.66	10.90	001111	001001
625i/50 Hz	64.00	4.70	52.00	12.00	001111	001001

20B.2.9 Sync Separation Control Register 5 (SYNSCR5)



Bit	Bit Name	Initial Value	R/W	Description
15	VSYNCDELAY	0	R/W	Delays the separated vertical sync signal for 1/4 horizontal cycle. 0: Disable 1/4fH delay 1: Enable 1/4fH delay Note: Stability of the field determination result may be improved by changing VSYNCDELAY.
14 to 10	VSYNCSLICE [4:0]	01011	R/W	Threshold for Vertical Sync Separation The greater the value, the wider pulse width is needed.
9 to 0	CSYNCSLICE_ V[9:0]	0010010010	R/W	Slice Level for Composite Sync Signal Separation (for vertical sync signal) Valid when manual slice level setting is active (SLICERMODE_V = 0).

(1) Vertical Sync Separation Control

VSYNCDELAY controls the phases of vertical sync signal and horizontal sync signal. When VSYNCDELAY is 1, the stability of the field determination result may be improved by delaying the vertical sync signal for 1/4 fH.

(2) Vertical Sync Separation Control

VSYNCSLICE controls the threshold for separating vertical sync signal from composite sync signal. The value will be set depending on the serration pulse width of each video signal format. Table 20B.10 shows the recommended set values.

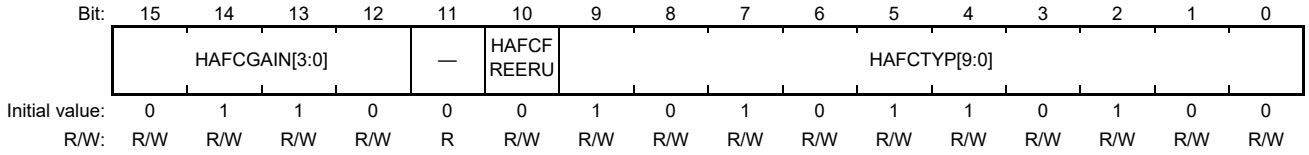
Table 20B.10 Recommended Threshold and Serration Pulse Width (for reference)

	Serration Pulse Width [µsec]	VSYNCSLICE[4:0]
525i/59.94Hz	27.08	01010
625i/50Hz	27.30	01010

(3) Slice Level Setting for Vertical Sync Separation

CSYNCSLICE_V sets the slice level for sync separation. This bit is valid only when SLICERMODE_V = 0.

20B.2.10 Horizontal AFC Control Register 1 (HAFCCR1)



Bit	Bit Name	Initial Value	R/W	Description
15 to 12	HAFCGAIN [3:0]	0110	R/W	Horizontal AFC Loop Gain 0000 to 0101: A smaller value needs a longer time for synchronization. 0110: Standard value 0111 to 1111: A larger value needs a shorter time for synchronization.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	HAFCFREERUN	0	R/W	Horizontal AFC Free-Run Oscillation Mode ON/OFF 0: OFF 1: ON
9 to 0	HAFCTYP[9:0]	1010110100	R/W	Horizontal AFC Center Oscillation Frequency Set an offset from 1024th clock pulse in 27-MHz clock cycle units.

(1) Horizontal AFC Loop Gain Control

HAFCGAIN sets the loop gain (response speed) of the horizontal AFC. The larger the value is, the faster the response speed is. However, setting a larger value will result in higher susceptibility to noise.

(2) Horizontal AFC Free-Run Control

HAFCFREERUN controls the horizontal AFC free-run operation. When HAFCFREERUN is 1, the horizontal AFC operates independently of the inputs and performs free-run operation. HAFCFREERUN should usually be set to 0.

(3) Horizontal AFC Lock Range (Horizontal) Control

HAFCMIN, HAFCTYP, and HAFCMAX set the horizontal AFC center oscillation frequency and lock range. The horizontal AFC function is controlled to stabilize the horizontal sync signal when the signals are deteriorated by trick playback of VCR or a weak electric field.

HAFCMIN[9:0]	Min oscillation frequency of horizontal AFC
HAFCTYP[9:0]	Center oscillation frequency of horizontal AFC
HAFCMAX[9:0]	Max oscillation frequency of horizontal AFC

Horizontal AFC lock range can be indicated by the following formula.

HAFCMIN < HAFCTYP < HAFCMAX …(1)

where

HAFCMIN	= HAFCTYP – allowable deviation
HAFCTYP	= N × M – 1024
HAFCMAX	= HAFCTYP + allowable deviation
M:	Number of clock pulses per horizontal cycle (27MHz sampling)
N:	Double speed setting 2 (double speed): M < 1024 1 (normal speed): M ≥ 1024

The horizontal AFC is locked if the formula indicated by (1) is satisfied.

When the horizontal AFC is locked, FHLOCK in VSYNCSR is set to 1. Otherwise, FHLOCK is 0.

Table 20B.11 Horizontal AFC Lock Range Setting

Signal Format	fH Horizontal Cycle	M fH@ 27.0MHz	N-Times Speed Setting	HAFCMAX [9:0]	HAFCTYP [9:0]	HAFCMIN [9:0]	Deviation		Unit
525i	63.56 [µsec]	1716 [clk]	1	771	692	618	79	-74	[clk]
				15.034	15.734	16.434	-0.700	0.700	[kHz]
625i	64.00 [µsec]	1728 [clk]	1	785	704	629	81	-75	[clk]
				14.925	15.625	16.325	-0.700	0.700	[kHz]

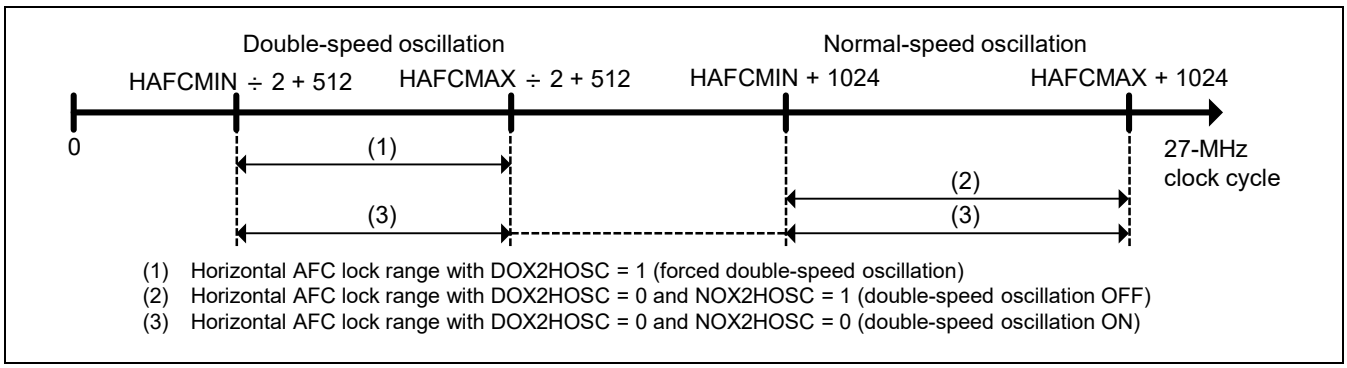


Figure 20B.12 Horizontal AFC Lock Range (Horizontal)

20B.2.11 Horizontal AFC Control Register 2 (HAFCCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HAFCSTART[3:0]				NOX2H OSC	DOX2H OSC	HAFCMAX[9:0]									
Initial value:	0	0	0	0	0	0	1	0	1	1	1	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	HAFCSTART [3:0]	0000	R/W	Start Line of Horizontal AFC Normal Operation (= VBI process end line) Start the phase comparison at the Nth line after the vertical sync signal.
11	NOX2HOSC	0	R/W	Disable of Horizontal AFC Double Speed Detection 0: Auto control 1: Double speed oscillation disabled
10	DOX2HOSC	0	R/W	Horizontal AFC Forced Double-Speed Oscillation 0: Auto control 1: Forced double-speed oscillation
9 to 0	HAFCMAX [9:0]	1011100110	R/W	Maximum Oscillation Frequency of Horizontal AFC Set an offset from 1024th clock pulse in 27-MHz clock cycle units.

(1) Horizontal AFC Lock Range (Vertical) Control

HAFCSTART and HAFCEND specify the horizontal AFC operation range. The horizontal AFC operation should be normally stopped from several lines before the vertical sync signal to the vertical sync signal to avoid a malfunction occurring in the VCR head switch part.

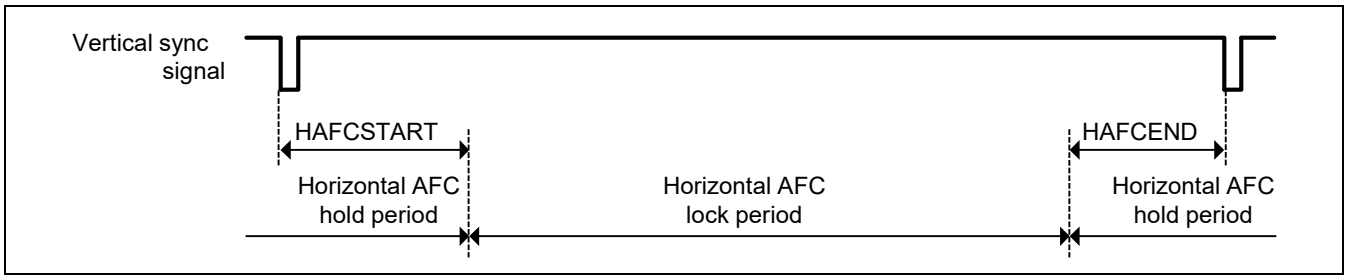
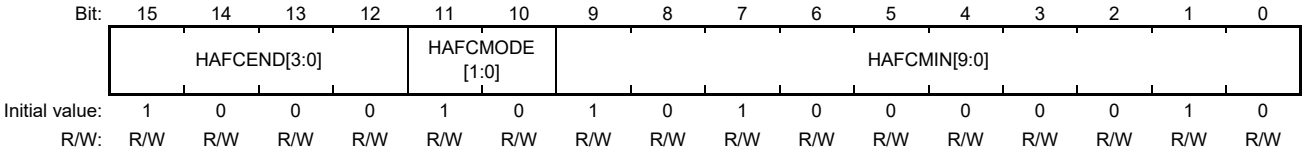


Figure 20B.13 Horizontal AFC Lock Range (Vertical)

(2) Horizontal AFC Double-Speed Control

NOX2HOSC and DOX2HOSC control the horizontal AFC double speed detection. In the NTSC, PAL and SECAM formats, DOX2HOSC should always be 0.

20B.2.12 Horizontal AFC Control Register 3 (HAFCCR3)



Bit	Bit Name	Initial Value	R/W	Description
15 to 12	HAFCEND[3:0]	1000	R/W	End line of Horizontal AFC Normal Operation (= VBI process start line) Stop the phase comparison at the Nth line before the vertical sync signal.
11, 10	HAFCMODE [1:0]	10	R/W	Horizontal AFC VBI Period Operating Mode [1] Loop gain control for low S/N 0: Loop gain is fixed. 1: Loop gain is automatically controlled. [0] Horizontal AFC control during VBI period 0: Phase comparison is stopped during VBI period. 1: Loop gain is reduced during VBI period.
9 to 0	HAFCMIN[9:0]	1010000010	R/W	Min Oscillation Frequency of Horizontal AFC Set an offset from 1024th clock pulse in 27-MHz clock cycle units.

(1) Horizontal AFC Operation Control during VBI Period

The malfunction caused by noise can be avoided by setting HAFCMODE[1] to 1 to reduce the loop gain for low S/N (VSYNCSR.ISNOISY = 1). The recommended value for HAFCMODE[1] is 1.

HAFCMODE[0] controls the horizontal AFC operation during the VBI period. The recommended value for HAFCMODE[0] is 0.

20B.2.13 Vertical Countdown Control Register 1 (VCDWCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VCDFREERUN	NOVCD50	NOVCD60	VCDDEFAULT[1:0]		VCDWINDOW[5:0]						VCDOFFSET[4:0]				
Initial value:	0	0	0	0	0	0	1	0	1	0	0	0	1	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	VCDFREERUN	0	R/W	Vertical Countdown Free-Run Oscillation Mode ON/OFF 0: OFF 1: ON
14	NOVCD50	0	R/W	Vertical Countdown 50-Hz Oscillation Mode OFF 0: 50-Hz oscillation ON 1: 50-Hz oscillation OFF
13	NOVCD60	0	R/W	Vertical Countdown 60-Hz (59.94-Hz) Oscillation Mode OFF 0: 60-Hz oscillation ON 1: 60-Hz oscillation OFF
12, 11	VCDDEFAULT[1:0]	00	R/W	Vertical Countdown Center Oscillation Frequency 00: Auto-detection 01: 50.00 Hz 10: 59.94 Hz 11: 60.00 Hz
10 to 5	VCDWINDOW[5:0]	010100	R/W	Vertical Countdown Sync Area Set a value in 0.1-ms units.
4 to 0	VCDOFFSET[4:0]	01010	R/W	Vertical Countdown Minimum Oscillation Frequency Set the shift from the center frequency in 0.1-ms units.

(1) Vertical Countdown Free-Run Operation Control

VCDFREERUN controls the vertical countdown free-run operation. When VCDFREERUN is 1, the vertical countdown free-run operation is performed independently of the inputs. VCDFREERUN should usually be set to 0.

(2) Vertical Countdown Free-Run Operation Control

NOVD50 controls 50-Hz oscillation. When NOVCD50 is 1, the vertical countdown operation is not locked to 50 Hz.

(3) Vertical Countdown Free-Run Operation Control

NOVD60 controls 60-Hz oscillation. When NOVCD60 is 1, the vertical countdown operation is not locked to 60 Hz.

(4) Vertical Countdown Free-Run Operation Control

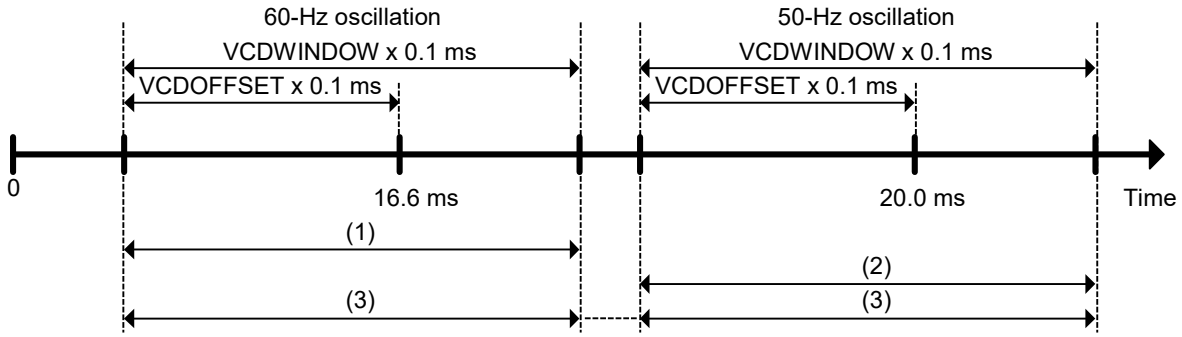
VCDDEFAULT sets the center frequency for the vertical countdown.

Table 20B.12 Vertical Countdown Operating Modes

VCDDEFAULT[1:0]	Operating Mode
00	Auto-detection
01	50.00 Hz
10	59.94 Hz
11	60.00 Hz

(5) Vertical Countdown Lock Range Control

VCDWINDOW and VCDOFFSET control the vertical countdown lock range. Figure 20B.14 shows the bit settings and lock ranges.



(1) Vertical countdown lock range with NOVCD 50 = 1 and NOVCD60 = 0 (60-Hz oscillation mode)
(2) Vertical countdown lock range with NOVCD 50 = 0 and NOVCD60 = 1 (50-Hz oscillation mode)
(3) Vertical countdown lock range with NOVCD 50 = 0 and NOVCD60 = 0 (auto detection mode)

Figure 20B.14 Vertical Countdown Lock Ranges

20B.2.14 Digital Clamp Control Register 1 (DCPCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCPMODE_Y	—	—	—	DCPCHECK	—	BLANKLEVEL_Y[9:0]									
Initial value:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	DCPMODE_Y	1	R/W	Clamp Level Setting Mode (Y signal) 0: Manual clamp level setting 1: Auto clamp level setting
14 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	DCPCHECK	0	R/W	Digital Clamp Pulse Position Check The offset given by BLANKLEVEL is added to the clamp position.
10	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
9 to 0	BLANKLEVEL_Y [9:0]	0000000000	R/W	Clamp Offset Level (Y signal) Set the subtraction value. Set a value in 1-LSB units. 2s complement

(1) Y-Signal Clamp Operation Control

DCPMODE_Y controls the clamp level of Y signal.

When DCPMODE_Y = 0, the value set by BLANKLEVEL_Y is subtracted from the video signal.

Y signal output = Y signal input – BLANKLEVEL_Y

When DCPMODE_Y is 1, the video signal level at the digital clamp pulse position (pedestal level) and BLANKLEVEL_Y are added together and the resulting value is subtracted from the video signal.

Y signal output = Y signal input – (detected value + BLANKLEVEL_Y)

(2) Digital Clamp Pulse Position Check Control

DCPCHECK allows the digital clamp pulse position to be displayed and checked on the screen. The following shows the steps to check the position.

1. Set DCPCHECK (digital clamp pulse position check bit) to 1.
2. Set SRCLEFT (left end of input video signal capturing area bit) and RES_HS[10:0] in SCL0_DS3 of the video display controller 5 scaler to 0.
3. Set clamp offset level of the signal to be monitored to Min value (−512 for BLANKLEVL_Y, (−32 for BLANKLEVL_Cb/Cr).
4. Adjust the pulse position and width using DCPPOS_Y (or DCPPOS_C) and DCPWIDTH.

20B.2.15 Digital Clamp Control Register 2 (DCPCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCPMODE_C	—	—	—	BLANKLEVEL_CB[5:0]						BLANKLEVEL_CR[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	DCPMODE_C	0	R/W	Clamp Level Setting Mode (Cb/Cr signal) 0: Manual clamp level setting 1: Auto clamp level setting
14 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 6	BLANKLEVEL_CB[5:0]	000000	R/W	Clamp Offset Level (Cb signal) Set the subtraction value. Set a value in 1-LSB units. 2s complement
5 to 0	BLANKLEVEL_CR[5:0]	000000	R/W	Clamp Offset Level (Cr signal) Set the subtraction value. Set a value in 1-LSB units. 2s complement

(1) Cb/Cr-Signal Clamp Operation Control

DCPMODE_C controls the clamp level of Cb/Cr-signal.

When DCPMODE_C = 0, the value set by BLANKLEVEL_CB/BLANKLEVEL_CR is subtracted from the video signal.

Cb signal output = Cb signal input – BLANKLEVEL_CB

Cr signal output = Cr signal input – BLANKLEVEL_CR

When DCPMODE_C = 1, sum of the video signal level (center level) in the digital clamp pulse position and BLANKLEVEL_CB/CR is subtracted from the video signal.

Cb signal output = Cb signal input – (detected value + BLANKLEVEL_CB)

Cr signal output = Cr signal input – (detected value + BLANKLEVEL_CR)

20B.2.16 Digital Clamp Control Register 3 (DCPCR3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DCPRESPONSE[2:0]			—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	1	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	DCPRESPONSE [2:0]	101	R/W	Digital Clamp Response Speed The larger the value is, the faster the response speed is. However, that will result in higher susceptibility to noise.
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) Digital Clamp Response Speed

DCPRESPONSE sets the digital clamp response speed.

Though the larger value makes the response faster, that will result in higher susceptibility to noise.

DCPRESPONSE is used in common to Y, Cb, and Cr signals.

20B.2.17 Digital Clamp Control Register 4 (DCPCR4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCPSTART[5:0]						—	—	—	—	—	—	—	—	—	—
Initial value:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	DCPSTART[5:0]	010000	R/W	Digital Clamp Start Line (in 1-line units) Start clamp pulses at the Nth line after the vertical sync signal.
9 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

20B.2.18 Digital Clamp Control Register 5 (DCPCR5)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCPEND[5:0]						—	—	—	—	—	—	—	—	—	—
Initial value:	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	DCPEND [5:0]	010000	R/W	Digital Clamp End Line (in 1-line units) Stop clamp pulses at the Nth line before the vertical sync signal.
9 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) Digital Clamp Pulse Control (Vertical)

DCPSTART and DCPEND control the digital clamp pulses in the vertical direction. Figure 20B.15 shows the bit settings and digital clamp timing.

DCPSTART and DCPEND are used in common to Y, Cb, and Cr signals.

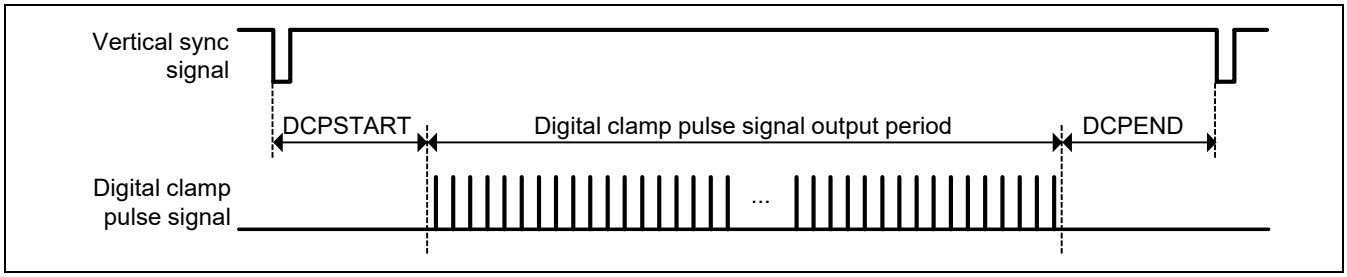


Figure 20B.15 Digital Clamp Timing (Vertical)

20B.2.19 Digital Clamp Control Register 6 (DCPCR6)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DCPWIDTH[6:0]							—	—	—	—	—	—	—	—
Initial value:	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	DCPWIDTH [6:0]	0110110	R/W	Digital Clamp Pulse Width Set a value in 27-MHz clock cycle units.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

20B.2.20 Digital Clamp Control Register 7 (DCPCR7)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCPPOS_Y[7:0]								—	—	—	—	—	—	—	—
Initial value:	1	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	DCPPOS_Y[7:0]	10100010	R/W	Digital Clamp Pulse Horizontal Start Position (Y signal) Set a value in 27-MHz clock cycle units.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

20B.2.21 Digital Clamp Control Register 8 (DCPCR8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DCPPOS_C[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	1	1	0	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	DCPPOS_C[7:0]	00011011	R/W	Digital Clamp Pulse Horizontal Start Position (Cb/Cr signal) Set a value in 27-MHz clock cycle units.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) Digital Clamp Pulse Control (Horizontal)

DCPWIDTH, DCPPOS_Y, and DCPPOS_C control the digital clamp pulses in the horizontal direction. Figure 20B.16 shows the bit settings and digital clamp timing.

DCPPOS_Y is used for Y signal and DCPPOS_C is for Cb/Cr signal. DCPWIDTH is used in common to Y, Cb, and Cr signals.

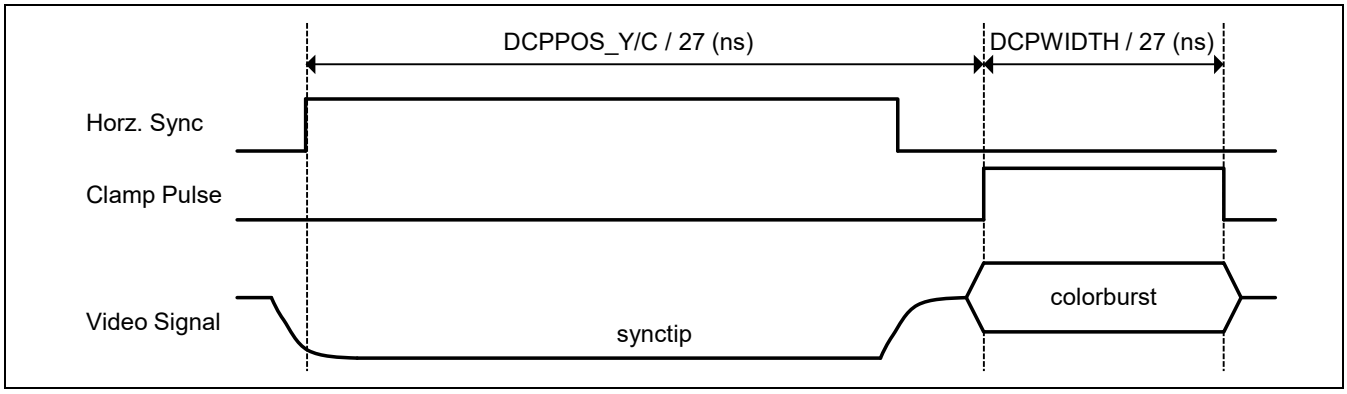


Figure 20B.16 Digital Clamp Timing (Horizontal)

20B.2.22 Noise Detection Control Register (NSDCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	ACFINPUT[1:0]		—	—	—	ACFLAGTIME[4:0]					—	—	ACFFILTER[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	ACFINPUT[1:0]	00	R/W	Video Signal for Autocorrelation Function 00: Y signal 01: Cb signal 10, 11: Cr signal
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 4	ACFLAGTIME [4:0]	00000	R/W	Delay Time for Autocorrelation Function Calculation 0 to 31 clock pulses @ 27-MHz clock The NSDSR.AFCSTRENGTH value almost corresponds to noise power when the delay time is set to 0.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	ACFFILTER[1:0]	00	R/W	Smoothing Parameter of Autocorrelation Function Data The smaller the ACFFILTER value is, the longer the time period is taken. The time period varies from 1 field to several seconds.

(1) Input for Noise Detection

ACFINPUT controls inputs for noise detection.

Table 20B.13 Input Selection for Noise Detection

ACFINPUT[1:0]	Input Signal
00	Y signal
01	Cb signal
10, 11	Cr signal

(2) Autocorrelation Function Control for Noise Detection

ACFLAGTIME controls autocorrelation function for noise detection.

The NSDSR.AFCSTRENGTH value almost corresponds to noise power when the delay time is set to 0.

(3) Smoothing Filter Control for Noise Detection

ACFFILTER controls smoothing function for noise detection inputs.

The smaller the ACFFILTER value is, the larger the field integration is (the longer time period is taken for noise detection).

20B.2.23 Burst Lock/Chroma Decoding Control Register (BTLCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LOCKRANGE [1:0]		LOOPGAIN [1:0]		LOCKLIMIT [1:0]		BCOFREERUN	—	DEFAULTSYS [1:0]		NONTSC358	NONTSC443	NOPALM	NOPALN	NOPAL443	NOSECAM
Initial value:	0	1	0	1	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	LOCKRANGE [1:0]	01	R/W	Burst Lock PLL Lock Range 00: ±400 Hz 01: ±800 Hz 10: ±1200 Hz 11: ±1600 Hz
13, 12	LOOPGAIN[1:0]	01	R/W	Burst Lock PLL Loop Gain The larger value makes the response faster, but the noise is more easily picked up.
11, 10	LOCKLIMIT[1:0]	10	R/W	Level for Burst Lock PLL to Re-Search Free-Run Frequency The larger value more easily unlocks the PLL to start re-search.
9	BCOFREERUN	0	R/W	Burst Lock PLL Free-Run Oscillation Mode ON/OFF 0: OFF 1: ON
8	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
7, 6	DEFAULTSYS [1:0]	00	R/W	Default Color System 00: NTSC 01: PAL 10: SECAM 11: Not specified
5	NONTSC358	0	R/W	NTSC-M Detection Control 0: NTSC-M detection ON 1: NTSC-M detection OFF
4	NONTSC443	0	R/W	NTSC-4.43 Detection Control 0: NTSC-4.43 detection ON 1: NTSC-4.43 detection OFF
3	NOPALM	0	R/W	PAL-M Detection Control 0: PAL-M detection ON 1: PAL-M detection OFF
2	NOPALN	0	R/W	PAL-N Detection Control 0: PAL-N detection ON 1: PAL-N detection OFF
1	NOPAL443	0	R/W	PAL-B, G, H, I, D Detection Control 0: PAL-B, G, H, I, D detection ON 1: PAL-B, G, H, I, D detection OFF
0	NOSECAM	0	R/W	SECAM Detection Control 0: SECAM detection ON 1: SECAM detection OFF

(1) Lock Range of Burst Lock PLL

LOCKRANGE controls the lock range of the burst lock PLL.

Table 20B.14 Lock Range of Burst Lock PLL

LOCKRANGE[1:0]	Lock Range of Burst Lock PLL
00	0: ±400 Hz
01	1: ±800 Hz
10	2: ±1200 Hz
11	3: ±1600 Hz

(2) Burst Lock PLL Loop Gain Control

LOOPGAIN controls the loop gain of the burst lock PLL.

The larger value makes the response faster, but the noise is more easily picked up.

(3) Burst Lock PLL Lock Limit Control

LOCKLIMIT controls the lock limit of the burst lock PLL.

The larger the LOCKLIMIT value is, the more easily the PLL free-run frequency is unlocked to start re-search.

(4) Burst Lock PLL Free-Run Operation Control

BCOFREERUN controls the free-run operation of burst lock PLL.

When BCOFREERUN is 1, the burst lock PLL performs free-run operation independently of the inputs. BCOFREERUN should usually be set to 0.

(5) Default Color System during Chroma Decoding

DEFAULTSYS sets the default color system when automatic judgement of the color system for use in chroma decoding is not possible.

Table 20B.15 Default Color System

DEFAULTSYS[1:0]	Color System for No Signal State
00	NTSC
01	PAL
10	SECAM
11	Not specified

(6) Color System Detection Control

NONTSC358, NONTSC443, NOPALM, NOPALN, NOPAL443, and NOSECAM control the color system detection.

Color system detection can be fully automatic, manual, or semi-automatic (detecting the specified color system only). If the detection result does not apply to any color system type, a color system selected by DEFAULTSYS is used for the operation.

Color system detection can be controlled (ON or OFF) individually for each type. By enabling one particular color system to be detected, the color system can be fixed. Table 20B.16 shows the color system detection control methods.

Table 20B.16 Color System Detection Control

	NOSECAM	NOPAL443	NOPALN	NOPALM	NONTSC443	NONTSC358
Auto	0	0	0	0	0	0
NTSC-3.58(M)	1	1	1	1	1	0
NTSC-4.43	1	1	1	1	0	1
PAL-M	1	1	1	0	1	1
PAL-N	1	1	0	1	1	1
PAL-4.43	1	0	1	1	1	1
SECAM	0	1	1	1	1	1

In auto mode, the color system detection result is stored into the register.

Table 20B.17 and Table 20B.18 show color system detection and detection result setting.

Table 20B.17 Color System Detection Result (1)

COLORSYS[1:0]	FSCMODE	FVMODE	Detection Result
0: NTSC	0: 3.58MHz	don't care	NTSC-M
0: NTSC	1: 4.43MHz	don't care	NTSC-4.43
1: PAL	0: 3.58MHz	0: 50Hz	PAL-N
1: PAL	0: 3.58MHz	1: 60Hz	PAL-M
1: PAL	1: 4.43MHz	0: 50Hz	PAL-B, H, I, G, D
1: PAL	1: 4.43MHz	1: 60Hz	PAL-60
2: SECAM	—	—	SECAM
3: Unknown	—	—	Undetectable

Table 20B.18 Color System Detection Result (2)

	ISNTSC	ISPAL	ISSECAM
Undetectable	0	0	0
NTSC	1	0	0
PAL	0	1	0
SECAM	0	0	1

20B.2.24 Burst Gate Pulse Control Register (BTGPCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BGPCHECK	BGPWIDTH[6:0]							BGPSTART[7:0]							
Initial value:	0	0	1	0	0	1	0	0	1	0	0	0	0	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BGPCHECK	0	R/W	Burst Gate Pulse Position Check Displays the front and end edges of burst gate pulses by white lines.
14 to 8	BGPWIDTH [6:0]	0100100	R/W	Burst Gate Pulse Width Specify the offset from the 64th clock pulse width in 27-MHz clock cycle units.
7 to 0	BGPSTART [7:0]	10000010	R/W	Burst Gate Pulse Start Position Specify the position from the horizontal sync signal reference in 27-MHz clock cycle units.

(1) Burst Gate Pulse Control

BGPWIDTH and BGPSTART control the burst gate pulse timing.

The burst gate pulse position is specified to extract color burst from the video signal which is considered as a reference signal for the burst lock PLL. Usually, the burst gate pulse should be set so that it should start at the latter part of the horizontal sync signal and include the reference position in order to respond to an insert position shift of color burst caused by VCR.

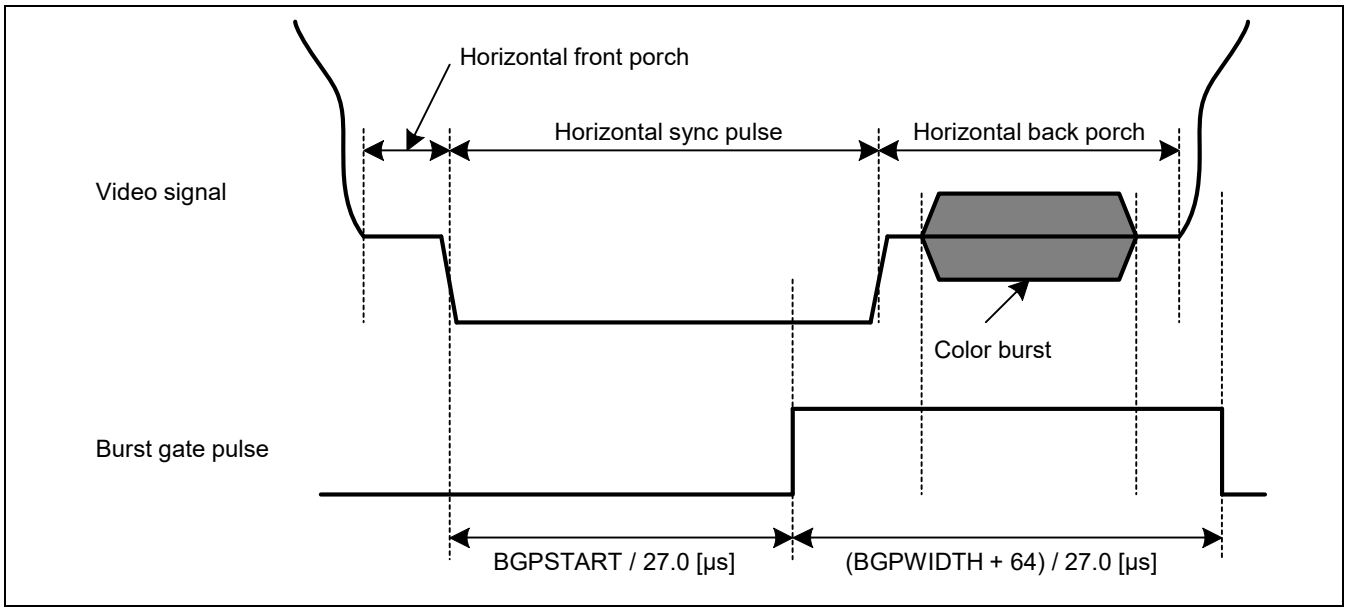


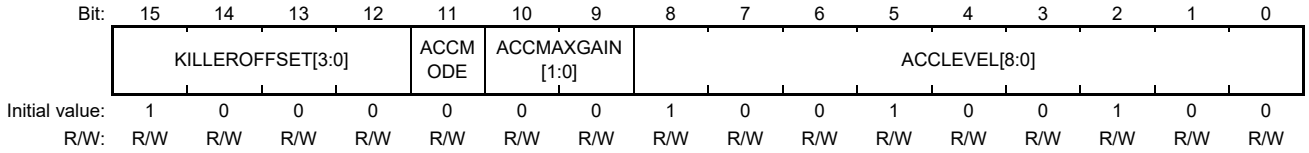
Figure 20B.17 Burst Gate Pulse Generation Timing

(2) Burst Gate Pulse Position Check

BGPCHECK controls the burst gate pulse position check on screen. The following shows the steps to check the position:

- Burst gate position check: Set BGPCHECK to 1.
- Input video signal capturing left end setting: Set SRCLEFT to 0 and RES_HS[10:0] in SCL0_DS3 of the video display controller 5 scaler to 0.
- Adjust the pulse position and width with BGPSTART and BGPWIDTH.

20B.2.25 ACC Control Register 1 (ACCCR1)



Bit	Bit Name	Initial Value	R/W	Description
15 to 12	KILLEROFFSET [3:0]	1000	R/W	The levels of these bits and KILLERLEVEL are added together to be the level to turn off the color killer. This level corresponds to the Peak-to-Peak amplitude of the color burst signal.
11	ACCMODE	0	R/W	ACC Operating Mode 0: Auto gain 1: Manual gain
10, 9	ACCMAXGAIN [1:0]	00	R/W	Maximum ACC Gain Valid when ACCMODE = 0 (auto gain setting). 00: 6 times 01: 8 times 10: 12 times 11: 16 times
8 to 0	ACCLEVEL[8:0]	100100100	R/W	ACC Reference Color Burst Amplitude Valid when ACCMODE = 0 (auto gain setting). Set Peak-to-Peak amplitude in 1-LSB units.

(1) Color Killer Offset Control

KILLEROFFSET sets the hysteresis to make the color killer OFF.

If the KILLEROFFSET value is too large, the color killer cannot be turned off as long as the burst amplitude is not large enough. If the KILLEROFFSET value is too small, the color killer is turned on and off repeatedly due to noise.

The standard value is between 4 and 10.

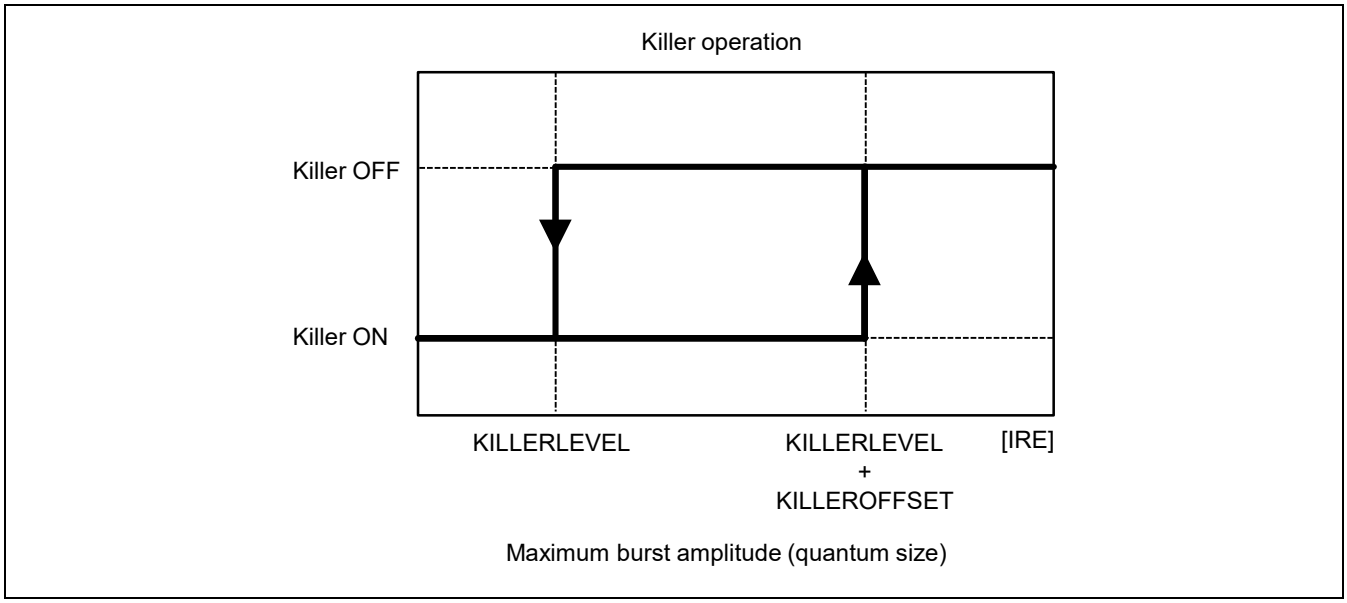


Figure 20B.18 Color Killer Operation

(2) ACC Operation Control

ACCMODE controls the ACC operation.

Table 20B.19 ACC Operating Modes

ACCMODE	Color Gain Adjustment
0	Auto gain
1	Manual gain

(3) Maximum ACC Gain Control

ACCMAXGAIN controls the maximum ACC gain. ACCMAXGAIN is valid only when ACCMODE = 0.

Table 20B.20 Maximum ACC Gain

ACCMAXGAIN[1:0]	Maximum Color Gain
00	6 times
01	8 times
10	12 times
11	16 times

(4) ACC Level Control

ACCLEVEL sets the burst amplitude of the chroma signal after gain correction. ACCLEVEL is valid only when ACCMODE = 1.

The ACC adjusts the gain so that the input chroma signal burst amplitude should be the same level as the ACCLEVEL value.

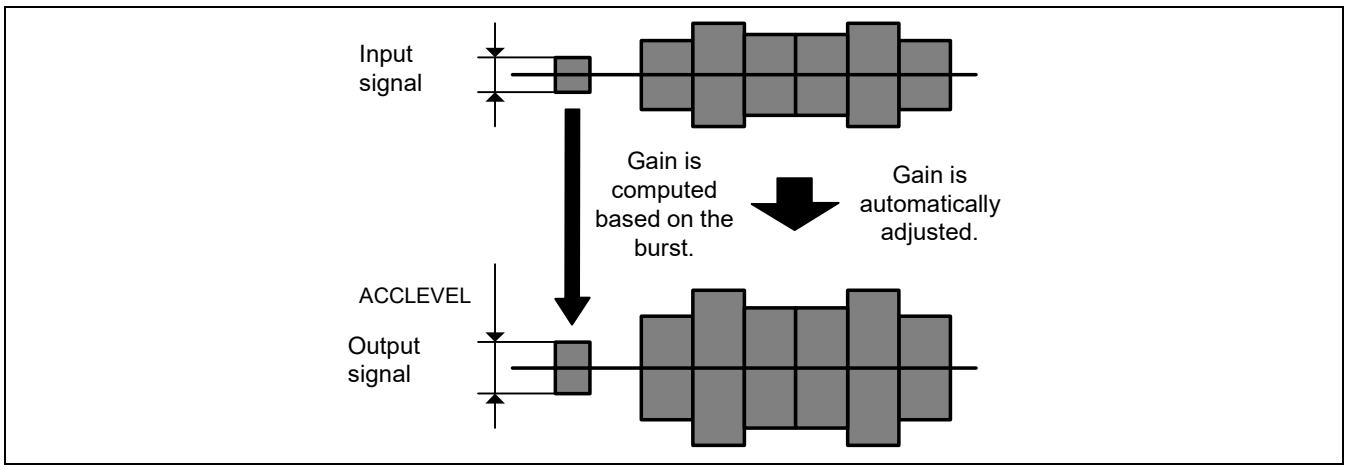


Figure 20B.19 ACC Level Setting

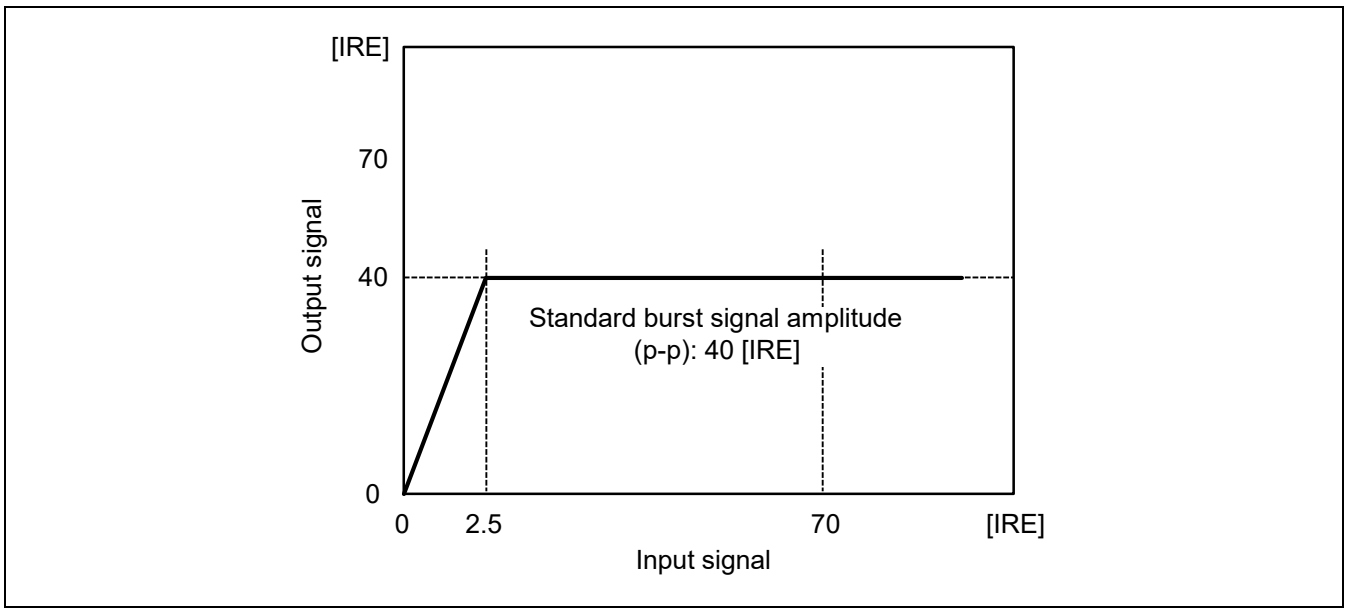


Figure 20B.20 ACC Input/Output Characteristics

Table 20B.21 ACC Characteristics

Input Burst Signal Level	Output Burst Signal Level
More than 24.1 [dB]	Reference amplitude (variable) ± acceptable error (variable)
24.1[dB] or less	Decreased in proportion to input level

20B.2.26 ACC Control Register 2 (ACCCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	CHROMASUBGAIN[1:0]		CHROMAMAINGAIN[8:0]								
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10, 9	CHROMASUBGAIN[1:0]	00	R/W	Chroma Manual Gain (sub) Valid when ACCMODE = 1 (manual gain setting) 00: 1 time 01: 2 times 10: 4 times 11: 8 times
8 to 0	CHROMAMAINGAIN[8:0]	100000000	R/W	Chroma Manual Gain (main) Valid when ACCMODE = 1 (manual gain setting) The value 256 corresponds to 1 time.

(1) Chroma Gain Adjustment (Manual) Control

CHROMASUBGAIN and CHROMAMAINGAIN control the chroma gain. CHROMASUBGAIN and CHROMAMAINGAIN are valid only when ACCMODE is 1.

C signal output = C signal input × (CHROMASUBGAIN + CHROMAMAINGAIN/256)

20B.2.27 ACC Control Register 3 (ACCCR3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ACC RESPONSE[1:0]		ACCPRECIS[5:0]						KILLER MODE	KILLERLEVEL[5:0]						—
Initial value:	0	1	0	1	0	1	0	0	0	0	0	1	0	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	ACCRESPONSE [1:0]	01	R/W	ACC Response Speed The larger value makes the response faster, but the noise is more easily picked up.
13 to 8	ACCPRECIS[5:0]	010100	R/W	ACC Gain Adjustment Accuracy Set the acceptable error level of color burst signal amplitude after ACC adjustment by 1 LSB of 10-bit accuracy.
7	KILLERMODE	0	R/W	Forced Color Killer Mode ON/OFF 0: Auto-detection 1: Killer mode is forcedly ON.
6 to 1	KILLERLEVEL[5:0]	001001	R/W	Color Killer Operation Start Point Set the half value of Peak-to-Peak amplitude by 1 LSB of 10-bit accuracy.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

(1) ACC Response Speed Control

ACCRESPONSE controls the ACC response speed.

The larger value makes the response faster, and the smaller value makes it slower. However, the large value causes the noise to be more easily picked up.

(2) ACC Acceptable Error Range Control

ACCPRECIS controls the acceptable error range of the output burst signal amplitude based on ACCLEVEL (target value).

If ACCLEVEL = 236 and ACCPRECIS = 20, the ACC gain is fixed within the following range:

(236 – 20) < Output signal burst signal amplitude < (236 + 20)

(3) Killer Operating Mode Control

KILLERMODE controls the killer operating mode.

When KILLERMODE = 1, the killer is forcedly turned ON.

(4) Killer Level Control

KILLERLEVEL controls the level to make the killer ON.

For details, see section 20B.2.25(1) Color Killer Offset Control.

20B.2.28 TINT Control Register (TINTCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINTSUB[5:0]						TINTMAIN[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	TINTSUB [5:0]	000000	R/W	Fine Adjustment of R-Y Demodulation Axis (only valid for NTSC/PAL) Set a value by 360/1024 degrees. 2s complement
9 to 0	TINTMAIN [9:0]	0000000000	R/W	Hue Adjustment Level (only valid for NTSC/PAL) Set a value by 360/1024 degrees. 2s complement

(1) R-Y Axis Correction Control

TINTSUB controls the phase of R-Y axis by ±11.25 degrees.

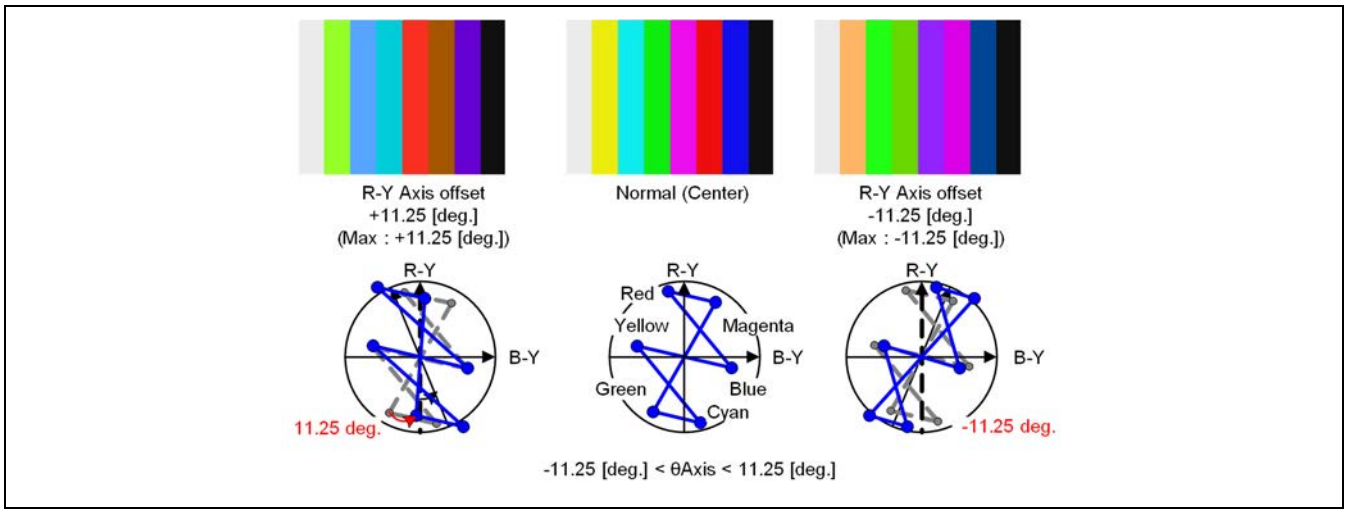


Figure 20B.21 Example of R-Y Axis Correction

(2) Hue Adjustment (TINT) Correction Control

TINTMAIN controls the phase of demodulation axis by 0 to 360 degrees.

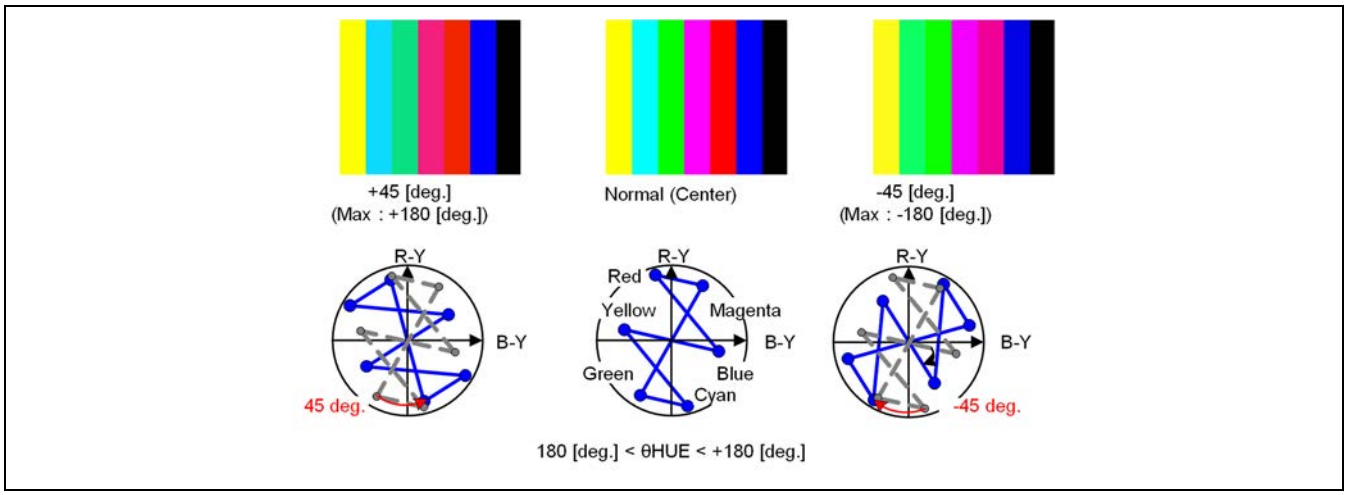


Figure 20B.22 Example of Hue Adjustment (TINT) Correction

20B.2.29 Y/C Delay/Chroma Decoding Control Register (YCDCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	LUMADELAY[4:0]					—	CHRO MALPF	DEMODMODE [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 4	LUMADELAY [4:0]	00000	R/W	Luminance Signal Delay Adjustment –16 to +15 clock pulses Set a value by the 2s complement.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CHROMALPF	0	R/W	LPF for Demodulated Chroma 0: Not used 1: Used
1, 0	DEMODMODE [1:0]	10	R/W	Averaging Processing for Pre-Demodulated Line 00: No processing 01: Setting prohibited 10: For PAL 11: Setting prohibited

(1) Y/C Delay Adjustment Control

LUMADELAY controls the Y/C delay.

Table 20B.22 Y/C Delay Adjustment

LUMADELAY[4:0]	Operation
00000	No delay
00001	Delays Y signal by 1 [clk]
:	:
01111	Delays Y signal by 15 [clk]
10000	Advances Y signal by 16 [clk]
:	:
11111	Advances Y signal by 1 [clk]

(2) Frequency Band Limiting after Demodulation

CHROMALPF turns on or off the frequency band limiting filter after demodulation.

Table 20B.23 Frequency Band Limiting after Demodulation

CHROMALPF	Operation
0	Frequency band-limiting filter OFF
1	Frequency band-limiting filter ON

(3) Chroma Decoding Operation Control

DEMODMODE controls operating modes of chroma demodulation.

Table 20B.24 Chroma Decoding Operation Modes

DEMODMODE[1:0]	Operation
00	One-line demodulation
10	Two-line demodulation for PAL only
01 and 11	Setting prohibited

20B.2.30 AGC Control Register 1 (AGCCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DUREDUCE	NOREDUCE	AGCRESPONSE[2:0]			AGCLEVEL[8:0]								
Initial value:	0	0	0	0	1	0	1	0	1	1	1	0	1	1	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	DUREDUCE	0	R/W	Manual Control of Sync Signal Amplitude Detection during VBI Period 0: Sets sync amplitude to AGC standard value. 1: Sets AGC gain to 3/4 times the normal gain value.
12	NOREDUCE	0	R/W	Control of Sync Signal Amplitude Detection during VBI Period 0: Detects sync amplitude. 1: Does not detect sync amplitude.
11 to 9	AGCRESPONSE [2:0]	101	R/W	AGC Response Speed The larger register value makes the response faster. However, the larger value causes the noise to be more easily picked up.
8 to 0	AGCLEVEL[8:0]	011101100	R/W	Sync Signal Reference Amplitude 10-bit unsigned value

(1) Sync Signal Amplitude Detection during VBI Period

DOREDUCE and NOREDUCE control detection of the AGC sync signal amplitude fluctuation during VBI period.

Table 20B.25 Sync Signal Amplitude Detection Operation during VBI Period

DOREDUCE	Sync Signal Amplitude Detection Operation during VBI Period
0	Sets sync amplitude to AGC standard
1	Sets AGC gain to 3/4 times the normal gain value

Table 20B.26 Sync Signal Amplitude Detection during VBI Period

NOREDUCE	Sync Signal Amplitude Detection during VBI Period
0	Detects sync amplitude.
1	Does not detect sync amplitude.

(2) AGC Response Speed Control

AGCRESPONSE controls the AGC response speed.

The larger register value makes the response faster, and smaller value makes it slower. (The large value causes the noise to be more easily picked up.)

The recommended value is 4 to avoid a malfunction caused by trick playback of VCR (fast-forward play/rewind play) or a weak electric field.

(3) AGC Level Control

AGCLEVEL controls the AGC target level.

When NTSC signals are quantized by a 10-bit A/D converter, sync signal amplitude for full range of the A/D converter can be provided by:

1023[LSB] × (40[IRE] ÷ 173[IRE]) = 236.53179[LSB]

Table 20B.27 shows the ideal AGC level for each input signal format.

Table 20B.27 AGC Level Setting Values (Ideal Values)

Input Signal Format	AGCLEVEL[8:0]
NTSC	236
PAL/SECAM	248

Table 20B.28 AGC Characteristics

Input Sync Signal Level	Output Sync Signal Level
0 or more [dB]	Increased in proportion to input level
–8.52 to 0 [dB]	Reference amplitude (variable) ± acceptable error (variable)
–8.52 or less [dB]	Decreased in proportion to input level

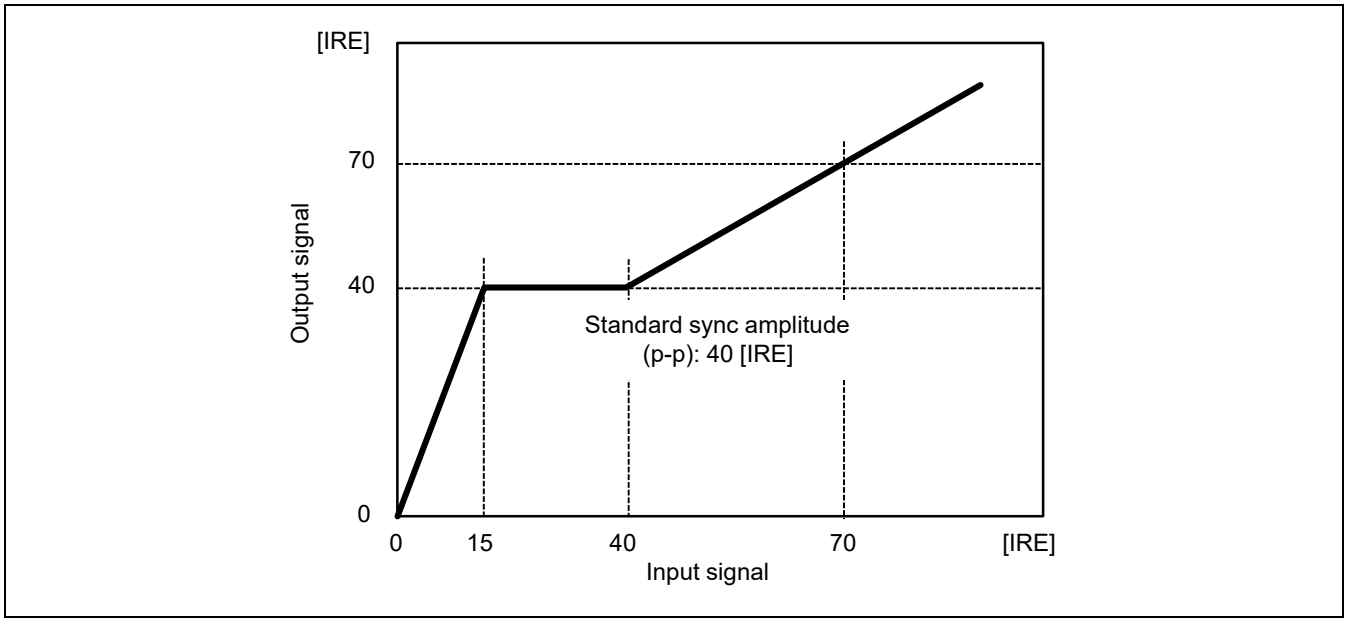


Figure 20B.23 AGC Characteristics (Sync Signal Amplitude Reference)

20B.2.31 AGC Control Register 2 (AGCCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	AGCPRECIS[5:0]						—	—	—	—	—	—	—	—
Initial value:	1	1	0	0	1	0	1	0	0	1	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
13 to 8	AGCPRECIS [5:0]	001010	R/W	AGC Gain Adjustment Accuracy Set acceptable error level for sync pulse amplitude after AGC adjustment by 1 LSB of 10-bit accuracy.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) AGC Acceptable Error Range Control

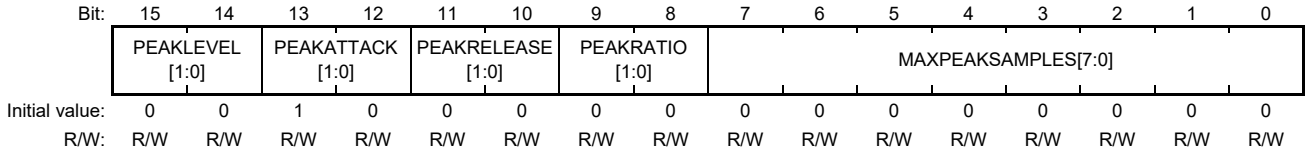
AGCPRECIS controls the acceptable error range of the output sync signal amplitude based on AGCLEVEL (target value).

If AGCLEVEL = 236 and AGCPRECIS = 10, AGC gain is fixed within the following range:

(236 – 10) < Output sync signal amplitude < (236 + 10)

In this case, the PGA gain can fall within a 2-step range. For video image with stabilized sync signal amplitude, AGCPRECIS = 4 is recommended, which enables the PGA gain to fall within a 1-step range, when the electric field is strong. For the above setting, the recommended value is 10 to avoid hunting in a weak electric field.

20B.2.32 Peak Limiter Control Register (PKLIMITCR)



Bit	Bit Name	Initial Value	R/W	Description
15, 14	PEAKLEVEL[1:0]	00	R/W	Peak Luminance Value Limited by Peak Limiter (video signal level) 00: Limiter OFF 01: 1008 LSB 10: 992 LSB 11: 960 LSB Peak limiter is not operated if AGC is OFF irrespective of PEAKLEVEL value.
13, 12	PEAKATTACK [1:0]	10	R/W	Response Speed with Peak Limiter Gain Decreased The larger value makes the response faster.
11, 10	PEAKRELEASE [1:0]	00	R/W	Response Speed with Peak Limiter Gain Increased The larger value makes the response faster.
9, 8	PEAKRATIO[1:0]	00	R/W	Maximum Compression Rate of Peak Limiter 00: Compressed up to 50% 01: Compressed up to 25% 10: Compressed up to 12.5% 11: Compressed up to 0%
7 to 0	MAXPEAK SAMPLES[7:0]	00000000	R/W	Allowable Number of Overflowing Pixels Set a value by 1024 pixels. Exceeding this value will start peak limiter operation.

(1) Peak Limiter Level Control

PEAKLEVEL controls the peak luminance limited by the peak limiter.

If the number of pixels counted exceeds the value set in PEAKLEVEL and there exist pixels more than the value set in MAXPEAKSAMPLES, the peak limiter function is activated to reduce the gain.

Table 20B.29 Peak Limiter Level Control

PEAKLEVEL[1:0]	Output Sync Signal Level
00	Peak limiter OFF
01	Peak limiter is activated at 1008 LSB
10	Peak limiter is activated at 992 LSB
11	Peak limiter is activated at 960 LSB

(2) Peak Limiter Response Speed Control

PEAKATTACK controls the response speed when the peak limiter gain is reduced.

The larger value makes the response faster.

(3) Peak Limiter Response Speed Control

PEAKRELEASE controls the response speed when the peak limiter gain is increased.

The larger value makes the response faster.

(4) Peak Limiter Gain Down Control

PEAKRATIO sets the maximum compression rate of the peak limiter.

Specifically, PEAKRATIO controls the amount of gain reduction (compression ratio) using the peak limiter function.

Table 20B.30 Peak Limiter Gain Down Control

PEAKRATIO[1:0]	Output Sync Signal Level
00	Compressed up to 50%
01	Compressed up to 25%
10	Compressed up to 12.5%
11	Compressed up to 0%

(5) Peak Limiter Determination Control

MAXPEAKSAMPLES controls the number of overflowing pixels allowed.

If the number of pixels counted during the vertical active period exceeds the value set in PEAKLEVEL and there exist pixels more than the value set in MAXPEAKSAMPLES, the peak limiter function is activated to reduce the gain.

The maximum allowable value is obtained by MAXPEAKSAMPLES × 1024.

20B.2.33 Over-Range Control Register 1 (RGORCR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RADJ_O_LEVEL0[9:0]									
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	RADJ_O_LEVEL0 [9:0]	1111111111	R/W	A/D Over-Threshold Level (Between levels 0 and 1) Level 0 (normal) to level 3 (completely over the range) are available.

(1) A/D Over-Threshold Level (Between Levels 0 and 1) Control

RADJ_O_LEVEL0 controls the A/D over-threshold level (between levels 0 and 1).

Figure 20B.24 shows the register values and threshold levels.

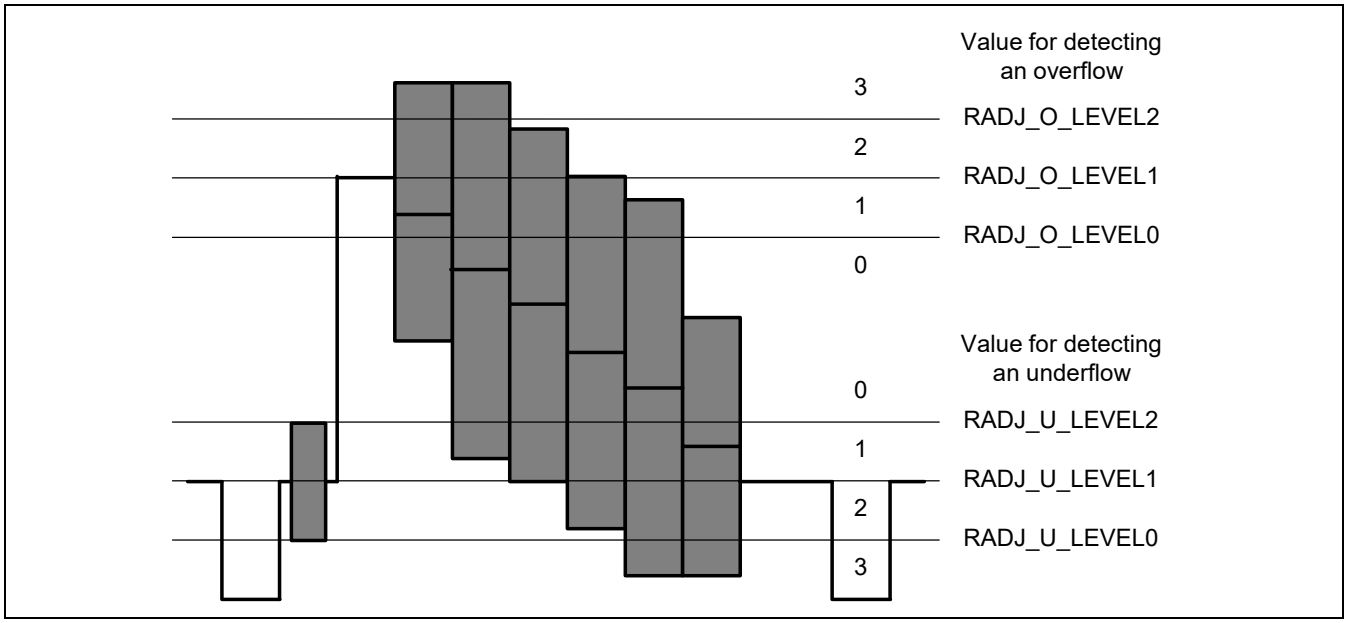


Figure 20B.24 Over-Range Determination Areas

20B.2.34 Over-Range Control Register 2 (RGORCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RADJ_U_LEVEL0[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	RADJ_U_ LEVEL0[9:0]	0000000000	R/W	A/D Under-Threshold Level (Between levels 2 and 3) Level 0 (normal) to level 3 (completely under the range) are available.

(1) A/D Under-Threshold Level (Between Levels 2 and 3) Control

RADJ_U_LEVEL0 controls the A/D under-threshold level (between levels 2 and 3).

For the register values and threshold levels, see section 20B.2.33, Over-Range Control Register 1 (RGORCR1).

20B.2.35 Over-Range Control Register 3 (RGORCR3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RADJ_O_LEVEL1[9:0]									
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	RADJ_O_ LEVEL1[9:0]	1111111111	R/W	A/D Over-Threshold Level (Between levels 1 and 2) Level 0 (normal) to level 3 (completely over the range) are available.

(1) A/D Over-Threshold Level (Between Levels 1 and 2) Control

RADJ_O_LEVEL1 controls the A/D over-threshold level (between levels 1 and 2).

For the register values and threshold levels, see section 20B.2.33, Over-Range Control Register 1 (RGORCR1).

20B.2.36 Over-Range Control Register 4 (RGORCR4)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RADJ_U_LEVEL1[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	RADJ_U_ LEVEL1[9:0]	0000000000	R/W	A/D Under-Threshold Level (Between levels 1 and 2) Level 0 (normal) to level 3 (completely under the range) are available.

(1) A/D Under-Threshold Level (Between Levels 1 and 2) Control

RADJ_U_LEVEL1 controls the A/D under-threshold level (between levels 1 and 2).

For the register values and threshold levels, see section 20B.2.33, Over-Range Control Register 1 (RGORCR1).

20B.2.37 Over-Range Control Register 5 (RGORCR5)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RADJ_O_LEVEL2[9:0]									
Initial value:	0	0	0	0	0	0	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	RADJ_O_ LEVEL2[9:0]	1111111111	R/W	A/D Over-Threshold Level (Between levels 2 and 3) Level 0 (normal) to level 3 (completely over the range) are available.

(1) A/D Over-Threshold Level (Between Levels 2 and 3) Control

RADJ_O_LEVEL2 controls the A/D over-threshold level (between levels 2 and 3).

For the register values and threshold levels, see section 20B.2.33, Over-Range Control Register 1 (RGORCR1).

20B.2.38 Over-Range Control Register 6 (RGORCR6)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RADJ_U_LEVEL2[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	RADJ_U_ LEVEL2[9:0]	0000000000	R/W	A/D Under-Threshold Level (Between levels 0 and 1) Level 0 (normal) to level 3 (completely under the range) are available.

(1) A/D Under-Threshold Level (Between Levels 0 and 1) Control

RADJ_U_LEVEL2 controls the A/D under-threshold level (between levels 0 and 1).

For the register values and threshold levels, see section 20B.2.33, Over-Range Control Register 1 (RGORCR1).

20B.2.39 Over-Range Control Register 7 (RGORCR7)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TEST_MONI[2:0]			RADJ_MIX_K_FIX[2:0]			—	—	—	—	—	—	UCMP_SW	DCMP_SW	HWIDE_SW
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	TEST_MONI[2:0]	000	R/W	Test Mode 000 to 011: Normal operation 100: Level 0 part is output as black. 101: Level 1 part is output as black. 110: Level 2 part is output as black. 111: Level 3 part is output as black.
11 to 9	RADJ_MIX_K_FIX [2:0]	000	R/W	Forced Range Over/Under Mode 000 to 011: Auto detection 100: Fixed to Level 0 (normal state) 101: Fixed to level 1 (almost normal) 110: Fixed to level 2 (almost over the range) 111: Fixed to level 3 (completely over the range)
8 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	UCMP_SW	0	R/W	Over-Range Detection Enable 0: Disables over-range detection 1: Enables over-range detection
1	DCMP_SW	0	R/W	Under-Range Detection Enable 0: Disables under-range detection 1: Enables under-range detection
0	HWIDE_SW	1	R/W	Horizontal Enlargement of Over/Under-Range Level 0: Does not provide horizontal enlargement 1: Provides horizontal enlargement

(1) Over-Range Test Control

TEST_MONI controls the over-range test.

(2) Forced Over/Under-Range Mode Control

RADJ_MIX_K_FIX controls the forced over-/under-range detection.

(3) Over-Range Detection Control

UCMP_SW enables the over-range detection.

(4) Under-Range Detection Control

DCMP_SW enables the under-range detection.

(5) Horizontal Enlargement at Over/Under-Range Level

HWIDE_SW controls the horizontal enlargement of the over/under-range level.

20B.2.40 Feedback Control Register for Horizontal AFC Phase Comparator (AFCPFCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PHDET_FIX	—	PHDET_DIV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PHDET_FIX	0	R/W	Forcible or LOWGAIN Control 0: LOWGAIN determination result used 1: Forcibly controlled (adjusted with PHDET_DIV)
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	PHDET_DIV [2:0]	101	R/W	Phase Comparator Feedback Adjust for Low Sync Signal Lock Stability 000: 1/1 001: 1/2 010: 1/4 011: 1/8 100: 1/16 101: 1/32 110 and 111: Setting prohibited

(1) Phase Comparator Feedback Adjust

PHDET_DEV adjusts the feedback amount as the phase comparison result when the lock stability is low. The greater the denominator is, the slower the reaction speed to the signal is.

Table 20B.31 Phase Comparator Feedback Adjust

LOWGAIN	PHDET_FIX	PHDET_DIV [2:0]	Output
—	1	000	1/1
		001	1/2
		010	1/4
		011	1/8
		100	1/16
		101	1/32
0	0	—	1/1
1	—	000	1/1
		001	1/2
		010	1/4
		011	1/8
		100	1/16
		101	1/32

20B.2.41 Register Update Enable Register (RUPDCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	NEWSETTING	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	NEWSETTING	0	R/W	V Update Enable for TGCR1 to TGCR3 1: Enables update. 0: Disables update.
14 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) V Update Enable for TGCR1 to TGCR3

NEWSETTING enables/disables TGCR1 to TGCR3 to execute V update.

20B.2.42 Sync Separation Status/Vertical Cycle Read Register (VSYNCSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FHCOUNT[0]	FHLOCK	ISNOISY	FHMODE	NOSIGNAL	FVLOCK	FVMODE	INTERLACED	FVCOUNT[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	FHCOUNT[0]	0	R	Horizontal AFC Oscillation Cycle (bit 0) Set a value by 1/64 of 27-MHz clock.
14	FHLOCK	0	R	Horizontal AFC Lock Detection Result 0: Unlocked 1: Locked
13	ISNOISY	0	R	Detection Result of Low S/N Signal by Sync Separation 0: Not low S/N signal 1: Low S/N signal
12	FHMODE	0	R	Speed Detection Result 0: Normal speed (525i/625i, etc.) 1: Multiplied speed (525p/625p, etc.)
11	NOSIGNAL	0	R	No-Signal Detection Result 0: Vertical sync signal detected 1: No vertical sync signal detected
10	FVLOCK	0	R	Vertical Countdown Lock Detection Result 0: Unlocked 1: Locked
9	FVMODE	0	R	Vertical Countdown Oscillation Mode 0: 50Hz 1: 60Hz
8	INTERLACED	0	R	Interlace Detection Result 0: Progressive 1: Interlace
7 to 0	FVCOUNT[7:0]	00000000	R	Vertical Cycle Measurement Result (in 0.1-ms units)

(1) Horizontal AFC Oscillation Cycle Read

FHCOUNT indicates bit 0 of the horizontal AFC oscillation cycle.

(2) Horizontal AFC Lock Detection Result Read

FHLOCK indicates the horizontal AFC lock detection result.

(3) Sync Separation Low S/N Signal Detection Result Read

ISNOISY indicates the detection result of low S/N signal by sync separation.

(4) Speed Detection Result Read

FHMODE indicates the speed detection result.

(5) No-Signal Detection Result Read

NOSIGNAL indicates the no-signal detection result.

(6) Vertical Countdown Lock Detection Result Read

FVLOCK indicates the vertical countdown lock detection result.

(7) Interlace Detection Result Read

INTERFACED indicates the interlace detection result.

(8) Vertical Cycle Measurement Result Read

FVCOUNT indicates the vertical cycle measurement result.

20B.2.43 Horizontal Cycle Read Register (HSYNCSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FHCOUNT[16:1]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	FHCOUNT [16:1]	H'0000	R	Horizontal AFC Oscillation Cycle (bit 16 to bit 1) Set a value by 1/64 of 27-MHz clock.

(1) Horizontal AFC Oscillation Cycle Read

FHCOUNT indicates the upper bits of the horizontal AFC oscillation cycle.

20B.2.44 Digital Clamp Read Register 1 (DCPSR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLAMPLEVEL_CB[5:0]						CLAMPLEVEL_Y[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	CLAMPLEVEL_CB [5:0]	000000	R	Digital Clamp Subtraction Value (Cb signal) Offset from the reference black level Set a value in 1-LSB units. 2s complement
9 to 0	CLAMPLEVEL_Y [9:0]	0000000000	R	Digital Clamp Subtraction Value (Y signal) Offset from the reference black level Set a value in 1-LSB units. 2s complement

(1) Reading Digital Clamp Subtraction Value of Cb Signal

CLAMPLEVEL_CB indicates the digital clamp subtraction value of Cb signal.

(2) Reading Digital Clamp Subtraction Value of Y in Composite Signal

CLAMPLEVEL_Y indicates the digital clamp subtraction value of Y signal.

20B.2.45 Digital Clamp Read Register 2 (DCPSR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CLAMPLEVEL_CR[5:0]						—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	CLAMPLEVEL_CR [5:0]	000000	R	Digital Clamp Subtraction Value (Cr signal) Offset from the reference black level Set a value in 1-LSB units. 2s complement
9 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) Reading Digital Clamp Subtraction Value of Cr Signal

CLAMPLEVEL_CR indicates the digital clamp subtraction value of Cr signal.

20B.2.46 Noise Detection Read Register (NSDSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ACFSTRENGTH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	ACFSTRENGTH [15:0]	H'0000	R	Noise Autocorrelation Strength at Digital Clamp Pulse Position (normally in the pedestal position) When ACFLAGTIME = 0, ACFSTRENGTH almost corresponds to the noise power in the pedestal position. Square root and logarithm of detection result almost correspond to noise amplitude and S/N (relative value), respectively.

(1) Reading Noise Autocorrelation Strength at Digital Clamp Pulse Position

ACFSTRENGTH indicates the noise correlation strength at the digital clamp pulse position (normal pedestal position).

20B.2.47 Chroma Decoding Read Register 1 (CROMASR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COLORSYS[1:0]		FSCMODE	FSCLOCK	NOBURST	ACCSUBGAIN[1:0]		ACCMAINGAIN[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	COLORSYS[1:0]	00	R	Color System Detection Result 00: NTSC 01: PAL 10: SECAM 11: Undetectable
13	FSCMODE	0	R	Color Sub-Carrier Frequency Detection Result 0: 3.58 MHz 1: 4.43 MHz
12	FSCLOCK	0	R	Burst Lock PLL Lock State Detection Result 0: Unlocked 1: Locked
11	NOBURST	0	R	Color Burst Detection Result 0: Color burst present 1: No color burst present
10, 9	ACCSUBGAIN [1:0]	00	R	Current ACC Gain Value (Sub) 00: 1 time 01: 2 times 10: 4 times 11: 8 times
8 to 0	ACCMAINGAIN [8:0]	000000000	R	Current ACC gain value (Main) The value 256 corresponds to 1 time.

(1) Color System Detection Result Read

COLORSYS indicates the color system detection result.

(2) Color Sub-Carrier Frequency Detection Result Read

FSCMODE indicates the color sub-carrier frequency detection result.

(3) Burst Lock PLL Lock State Detection Result Read

FSCLOCK indicates the lock state detection result of the burst lock PLL.

(4) Color Burst Detection Result Read

NOBURST indicates the color burst detection result.

(5) Current ACC Gain (Sub) Value Read

ACCSUBGAIN indicates the current ACC gain (sub) value.

(6) Current ACC Gain (Main) Value Read

ACCMAINGAIN indicates the current ACC gain (main) value.

20B.2.48 Chroma Decode Read Register 2 (CROMASR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ISSECAM	ISPAL	ISNTSC	—	—	LOCKLEVEL[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	ISSECAM	0	R	SECAM Detection Result 0: Not SECAM signal 1: SECAM signal
11	ISPAL	0	R	PAL Detection Result 0: Not PAL signal 1: PAL signal
10	ISNTSC	0	R	NTSC Detection Result 0: Not NTSC signal 1: NTSC signal
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	LOCKLEVEL [7:0]	00000000	R	Low S/N Signal Detection Result by Burst Lock PLL The larger value corresponds to a higher S/N.

(1) SECAM Signal Detection Result Read

ISSECAM indicates the SECAM signal detection result.

(2) PAL Signal Detection Result Read

ISPAL indicates the PAL signal detection result.

(3) NTSC Signal Detection Result Read

ISNTSC indicates the NTSC signal detection result.

(4) Read of Low S/N Signal Detection Result by Burst Lock PLL

LOCKLEVEL indicates the low S/N signal detection result by the burst lock PLL.

20B.2.49 Sync Separation Read Register (SYNCSSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	ISREDUCED	—	—	SYNCDEPTH[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	ISREDUCED	0	R	Sync Amplitude Detection Result during VBI Period 0: Amplitude is larger than that in image active period. 1: Amplitude is equal to that in image active period.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	SYNCDEPTH [9:0]	0000000000	R	Sync Pulse Amplitude Detection Result

(1) Reading Sync Amplitude Detection Result during VBI Period

ISREDUCED indicates the sync amplitude detection result during VBI period.

(2) Reading Sync Pulse Level Amplitude Detection Result

SYNCDEPTH indicates the sync pulse amplitude detection result.

20B.2.50 AGC Control Read Register 1 (AGCCSR1)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HIGHSAMPLES[7:0]								PEAKSAMPLES[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	HIGHSAMPLES[7:0]	00000000	R	Number of Pixels Which Have Larger Luminance Value Than Peak Luminance Limited by Peak Limiter Indicated by 1024 pixels
7 to 0	PEAKSAMPLES[7:0]	00000000	R	Number of Overflowing Pixels Indicated by 1024 pixels

(1) Reading Number of Pixels Which Have Larger Luminance Value Than Peak Luminance Limited by Peak Limiter

HIGHSAMPLES indicates the number of pixels which have larger luminance value than the peak luminance limited by the peak limiter.

(2) Number of Overflowing Pixels

PEAKSAMPLES indicates the number of overflowing pixels.

20B.2.51 AGC Control Read Register 2 (AGCCSR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	AGCCONVERGE	AGCGAIN[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	AGCCONVERGE	0	R	AGC Convergence Detection Result 0: Not converged 1: Converged
7 to 0	AGCGAIN[7:0]	01000000	R	Current AGC Gain Value The value 64 corresponds to ×1.

(1) Reading AGC Convergence Detection Result

AGCCONVERGE indicates the AGC convergence detection result.

(2) Reading Current AGC Gain

AGCGAIN indicates the current AGC gain.

20B.2.52 Y/C Separation Control Register 3 (YCSCR3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	K15[3:0]				K13[5:0]						K11[5:0]					
Initial value:	0	0	1	0	0	0	1	0	0	0	0	0	0	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	K15[3:0]	0010	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the horizontal BPF is applied to the narrower range.
11 to 6	K13[5:0]	001000	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the horizontal BPF is applied to the narrower range.
5 to 0	K11[5:0]	000100	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the horizontal BPF is applied to the narrower range.

(1) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K15 controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(2) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K13 controls the two-dimensional Y/C separation filter select coefficient.

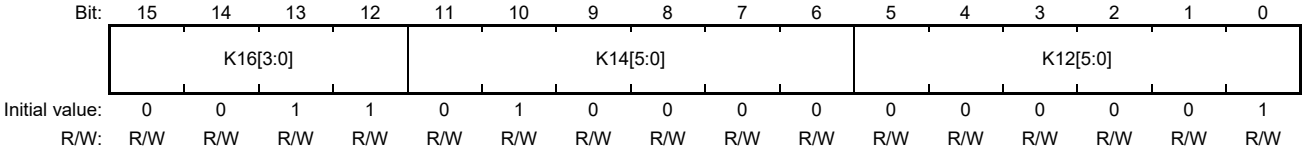
For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(3) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K11 controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

20B.2.53 Y/C Separation Control Register 4 (YCSCR4)



Bit	Bit Name	Initial Value	R/W	Description
15 to 12	K16[3:0]	0011	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the horizontal BPF is applied to the narrower range.
11 to 6	K14[5:0]	010000	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the horizontal BPF is applied to the narrower range.
5 to 0	K12[5:0]	000001	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the horizontal BPF is applied to the narrower range.

(1) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K16 controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(2) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K14 controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(3) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K12 controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

20B.2.54 Y/C Separation Control Register 5 (YCSCR5)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	K22A[7:0]								—	—	K21A[5:0]					
Initial value:	0	1	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	K22A[7:0]	01000000	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the narrower range.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	K21A[5:0]	000110	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the narrower range.

(1) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K22A controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(2) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K21A controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

20B.2.55 Y/C Separation Control Register 6 (YCSCR6)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	K22B[7:0]								—	—	K21B[5:0]					
Initial value:	0	0	0	1	0	0	0	0	0	0	0	0	0	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	K22B[7:0]	00010000	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the narrower range.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	K21B[5:0]	000110	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the narrower range.

(1) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K22B controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(2) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K21B controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

20B.2.56 Y/C Separation Control Register 7 (YCSCR7)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	K23B[3:0]				K23A[3:0]				—	—	—	K24[4:0]				
Initial value:	0	1	1	0	0	0	1	1	0	0	1	0	0	1	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	K23B[3:0]	0110	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the narrower range.
11 to 8	K23A[3:0]	0011	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the narrower range.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
4 to 0	K24[4:0]	00101	R/W	Two-Dimensional Y/C Separation Filter Select Coefficient As the value becomes larger, the vertical BPF is applied to the wider range.

(1) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K23B controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(2) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K23A controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

(3) Two-Dimensional Y/C Separation Filter Select Coefficient Control

K24 controls the two-dimensional Y/C separation filter select coefficient.

For details, refer to section 20B.3.5(3), Horizontal and Vertical Correlation Detection Block.

20B.2.57 Y/C Separation Control Register 8 (YCSCR8)

In two-dimensional Y/C separation, horizontal BPF, vertical BPF, and horizontal/vertical BPF are adaptively switched. For the horizontal BPF and horizontal/vertical BPF, horizontal properties can be selected.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HBPF_NARROW	HVBPF_NARROW	HBPF1_9TAP_ON	HVBPF1_9TAP_ON	HFIL_TAP_SEL	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	HBPF_NARROW	1	R/W	Latter-Stage Horizontal BPF Select 0: Bypass 1: 17 TAP
14	HVBPF_NARROW	1	R/W	Latter-Stage Horizontal/Vertical BPF Select 0: Bypass 1: 17 TAP
13	HBPF1_9TAP_ON	0	R/W	Former-Stage Horizontal BPF Select 0: 17 TAP 1: 9 TAP
12	HVBPF1_9TAP_ON	0	R/W	Former-Stage Horizontal/Vertical BPF Select 0: 17 TAP 1: 9 TAP
11	HFIL_TAP_SEL	0	R/W	Horizontal Filter and Horizontal/Vertical Filter Bandwidth Switch Signal 0: 17 TAP 1: 9 TAP
10 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) Horizontal BPF Select Control

HBPF_NARROW selects the latter-stage horizontal BPF.

For details, refer to section 20B.3.5 (2), Horizontal and Vertical Filter Block.

(2) Horizontal/Vertical BPF Select Control

HVBPF_NARROW selects the latter-stage horizontal/vertical BPF.

For details, refer to section 20B.3.5 (2), Horizontal and Vertical Filter Block.

(3) Horizontal BPF (Broadband) Select Control

HBPF1_9TAP_ON selects the former-stage horizontal BPF.

For details, refer to section 20B.3.5 (2), Horizontal and Vertical Filter Block.

(4) Horizontal/Vertical BPF (Broadband) Select Control

HVBPF1_9TAP_ON selects the former-stage horizontal/vertical BPF.

For details, refer to section 20B.3.5 (2), Horizontal and Vertical Filter Block.

(5) Horizontal BPF Bandwidth Switch Control

HFIL_TAP_SEL switches the horizontal BPF bandwidths used for mixing.

For details, refer to section 20B.3.5 (5), Horizontal and Vertical Signal Mixing Block.

20B.2.58 Y/C Separation Control Register 9 (YCSCR9)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DET2_ON	—	—	—	HSEL_MIX_Y[3:0]				VSEL_MIX_Y[3:0]				HVSEL_MIX_Y[3:0]			
Initial value:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	DET2_ON	1	R/W	Two-Dimensional Filter Mixing Select 0: Signals are not mixed after passing the correlation detection filter. 1: Signals are mixed after passing the correlation detection filter.
14 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	HSEL_MIX_Y[3:0]	0000	R/W	Mixing Ratio of Signal after Passing Horizontal Filter to Signal after Passing Former-Stage Horizontal Filter 0000: Horizontal filter 100.0% 0001: Horizontal filter 87.5% to former-stage horizontal filter 12.5% 0010: Horizontal filter 75.0% to former-stage horizontal filter 25.0% 0011: Horizontal filter 62.5% to former-stage horizontal filter 37.5% 0100: Horizontal filter 50.0% to former-stage horizontal filter 50.0% 0101: Horizontal filter 37.5% to former-stage horizontal filter 62.5% 0110: Horizontal filter 25.0% to former-stage horizontal filter 75.0% 0111: Horizontal filter 12.5% to former-stage horizontal filter 87.5% 1000: Former-stage horizontal filter 100% 1001 to 1111: Setting prohibited
7 to 4	VSEL_MIX_Y[3:0]	0000	R/W	Mixing Ratio of Signal after Passing Vertical Filter to Signal after Passing Former-Stage Horizontal/Vertical Filter 0000: Vertical filter 100.0% 0001: Vertical filter 87.5% to former-stage horizontal/vertical filter 12.5% 0010: Vertical filter 75.0% to former-stage horizontal/vertical filter 25.0% 0011: Vertical filter 62.5% to former-stage horizontal/vertical filter 37.5% 0100: Vertical filter 50.0% to former-stage horizontal/vertical filter 50.0% 0101: Vertical filter 37.5% to former-stage horizontal/vertical filter 62.5% 0110: Vertical filter 25.0% to former-stage horizontal/vertical filter 75.0% 0111: Vertical filter 12.5% to former-stage horizontal/vertical filter 87.5% 1000: Former-stage horizontal/vertical filter 100% 1001 to 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	HVSEL_MIX_Y[3:0]	0000	R/W	Mixing Ratio of Signal after Passing Horizontal/Vertical Filter to Signal after Passing Former-Stage Horizontal/Vertical Filter 0000: Horizontal/vertical filter 100.0% 0001: Horizontal/vertical filter 87.5% to former-stage horizontal/vertical filter 12.5% 0010: Horizontal/vertical filter 75.0% to former-stage horizontal/vertical filter 25.0% 0011: Horizontal/vertical filter 62.5% to former-stage horizontal/vertical filter 37.5% 0100: Horizontal/vertical filter 50.0% to former-stage horizontal/vertical filter 50.0% 0101: Horizontal/vertical filter 37.5% to former-stage horizontal/vertical filter 62.5% 0110: Horizontal/vertical filter 25.0% to former-stage horizontal/vertical filter 75.0% 0111: Horizontal/vertical filter 12.5% to former-stage horizontal/vertical filter 87.5% 1000: Former-stage horizontal/vertical filter 100% 1001 to 1111: Setting prohibited

(1) Two-Dimensional Filter Mixing Select Control

DET2_ON selects two-dimensional filter mixing.

For details, refer to section 20B.3.5(5), Horizontal and Vertical Signal Mixing Block.

(2) Control of Mixing Ratio of Signal after Passing Horizontal Filter to Signal after Passing Former-Stage Horizontal Filter

HSEL_MIX_Y controls the mixing ratio of the signal after passing a horizontal filter to the signal after passing the former-stage horizontal filter.

For details, refer to section 20B.3.5(5), Horizontal and Vertical Signal Mixing Block.

(3) Control of Mixing Ratio of Signal after Passing Vertical Filter to Signal after Passing Former-Stage Horizontal/Vertical Filter

VSEL_MIX_Y controls the mixing ratio of the signal after passing a vertical filter to the signal after passing the former-stage horizontal/vertical filter.

For details, refer to section 20B.3.5(5), Horizontal and Vertical Signal Mixing Block.

(4) Control of Mixing Ratio of Signal after Passing Horizontal/Vertical Filter to Signal after Passing Former-Stage Horizontal/Vertical Filter

HVSEL_MIX_Y controls the mixing ratio of the signal after passing a horizontal/vertical filter to the signal after passing the former-stage horizontal/vertical filter.

For details, refer to section 20B.3.5(5), Horizontal and Vertical Signal Mixing Block.

20B.2.59 Y/C Separation Control Register 11 (YCSCR11)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	V_Y_LEVEL[8:0]								
Initial value:	1	1	0	1	1	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
13	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
12, 11	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
10, 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	V_Y_LEVEL [8:0]	000000011	R/W	Vertical Luminance Detection Level for Correlation Detection Filter The luminance is detected when lower than the set value.

(1) Vertical Luminance Detection Level for Correlation Detection Filter

V_Y_LEVEL[8:0] select the vertical luminance detection level for correlation detection filter.

Be sure to set 0 to all the bits in this field when this module is in use.

20B.2.60 Y/C Separation Control Register 12 (YCSCR12)

During two-dimensional Y/C separation, the horizontal bandwidth can be further narrowed using the cascade horizontal BPF after horizontal BPF, vertical BPF, and horizontal/vertical BPF are switched.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DET2_MIX_C[3:0]				DET2_MIX_Y[3:0]				—	—	—	—	FIL2_MODE_2D [1:0]		—	FIL2_NAR ROW_2D
Initial value:	0	0	0	0	0	1	1	0	0	0	0	0	0	1	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	DET2_MIX_C[3:0]	0000	R/W	Mixing Ratio of C Signal after Passing Horizontal/Vertical Adaptive Filter to Signal after Passing Correlation Detection Filter (set 0 when DET2_ON = 0) 0000: Horizontal/vertical adaptive filter 100.0% 0001: Horizontal/vertical adaptive filter 87.5% to correlation detection filter 12.5% 0010: Horizontal/vertical adaptive filter 75.0% to correlation detection filter 25.0% 0011: Horizontal/vertical adaptive filter 62.5% to correlation detection filter 37.5% 0100: Horizontal/vertical adaptive filter 50.0% to correlation detection filter 50.0% 0101: Horizontal/vertical adaptive filter 37.5% to correlation detection filter 62.5% 0110: Horizontal/vertical adaptive filter 25.0% to correlation detection filter 75.0% 0111: Horizontal/vertical adaptive filter 12.5% to correlation detection filter 87.5% 1000: Correlation detection filter 100% 1001 to 1111: Setting prohibited
11 to 8	DET2_MIX_Y[3:0]	0110	R/W	Mixing Ratio of C Signal for Y Generation after Passing Horizontal/Vertical Adaptive Filter to Signal after Passing Correlation Detection Filter (set 0 when DET2_ON = 0) 0000: Horizontal/vertical adaptive filter 100.0% 0001: Horizontal/vertical adaptive filter 87.5% to correlation detection filter 12.5% 0010: Horizontal/vertical adaptive filter 75.0% to correlation detection filter 25.0% 0011: Horizontal/vertical adaptive filter 62.5% to correlation detection filter 37.5% 0100: Horizontal/vertical adaptive filter 50.0% to correlation detection filter 50.0% 0101: Horizontal/vertical adaptive filter 37.5% to correlation detection filter 62.5% 0110: Horizontal/vertical adaptive filter 25.0% to correlation detection filter 75.0% 0111: Horizontal/vertical adaptive filter 12.5% to correlation detection filter 87.5% 1000: Correlation detection filter 100% 1001 to 1111: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	FIL2_MODE_2D[1:0]	01	R/W	Two-Dimensional Cascade/TAKE-OFF Filter Mode Select 00: Bypass 01: Cascade filter 10: TAKE-OFF filter 11: Setting prohibited
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	FIL2_NARROW_2D	1	R/W	Two-Dimensional Cascade Filter Select 0: Bypass 1: 17 TAP

(1) Mixing Ratio of C Signal after Passing Horizontal/Vertical Adaptive Filter to Signal after Passing Correlation Detection Filter

DET2_MIX_C controls the mixing ratio of the chroma signal (after adaptation) to the signal after passing the correlation detection filter.

For details, refer to section 20B.3.5(6), Correlation Detection Value Mixing Block.

(2) Mixing Ratio of C Signal for Y Generation after Passing Horizontal/Vertical Adaptive Filter to Signal after Passing Correlation Detection Filter

For details, refer to section 20B.3.5(6), Correlation Detection Value Mixing Block.

(3) Two-Dimensional Cascade/TAKE-OFF Filter Mode Select

FIL2_MODE_2D selects the two-dimensional cascade/TAKE-OFF filter mode.

For details, refer to section 20B.3.5(8), Cascade Filter Block.

(4) Two-Dimensional Cascade Filter Select

FIL2_NARROW_2D selects the two-dimensional cascade filter.

For details, refer to section 20B.3.5(8), Cascade Filter Block.

20B.2.61 Digital Clamp Control Register 9 (DCPCR9)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CLP_HOLD_ON_Y	CLP_HOLD_ON_CB	CLP_HOLD_ON_CR	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
12	CLP_HOLD_ON_Y	1	R/W	Clamp Data Hold Processing ON/OFF (Y) 0: Hold processing ON 1: Hold processing OFF
11	CLP_HOLD_ON_CB	1	R/W	Clamp Data Hold Processing ON/OFF (Cb) 0: Hold processing ON 1: Hold processing OFF
10	CLP_HOLD_ON_CR	1	R/W	Clamp Data Hold Processing ON/OFF (Cr) 0: Hold processing ON 1: Hold processing OFF
9 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

(1) Clamp Data Hold Processing ON/OFF Control (Y)

CLP_HOLD_ON_Y selects ON/OFF of hold processing for Y signal clamp data.

Be sure to set 0 to this bit when this module is in use.

(2) Clamp Data Hold Processing ON/OFF Control (Cb)

CLP_HOLD_ON_CB selects ON/OFF of hold processing for Cb signal clamp data.

Be sure to set 0 to this bit when this module is in use.

(3) Clamp Data Hold Processing ON/OFF Control (Cr)

CLP_HOLD_ON_CR selects ON/OFF of hold processing for Cr signal clamp data.

Be sure to set 0 to this bit when this module is in use.

20B.2.62 Chroma Filter TAP Coefficient (WA_F0 to WA_F8) Registers for Y/C Separation (YCTWA_F0 to YCTWA_F8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	FIL2_2D_WA_F0 to FIL2_2D_WA_F8[12:0]												
Initial value:	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	FIL2_2D_WA_F0 to FIL2_2D_WA_F8 [12:0]	*	R/W	Two-Dimensional Cascade Broadband (3.58/4.43/SECAM-DR)/TAKE-OFF Filter TAP Coefficients 0 to 8 [12]: Sign [11:0]: Absolute value * Initial values: FIL2_2D_WA_F0: H'0018 FIL2_2D_WA_F1: H'002C FIL2_2D_WA_F2: H'0014 FIL2_2D_WA_F3: H'1034 FIL2_2D_WA_F4: H'1080 FIL2_2D_WA_F5: H'1080 FIL2_2D_WA_F6: H'100C FIL2_2D_WA_F7: H'0084 FIL2_2D_WA_F8: H'00C8

(1) Two-Dimensional Cascade Broadband (3.58/4.43/SECAM-DR)/TAKE-OFF Filter TAP Coefficients 0 to 8 Control

FIL2_2D_WA_F0 to FIL2_2D_WA_F8[12:0] control two-dimensional cascade broadband (3.58/4.43/SECAM-DR)/ TAKE-OFF filter TAP coefficients 0 to 8.

The transfer function is defined as follows:

$$H(z) = \{F0(z^{-8} + z^{+8}) + F1(z^{-7} + z^{+7}) + F2(z^{-6} + z^{+6}) + F3(z^{-5} + z^{+5}) + F4(z^{-4} + z^{+4}) + F5(z^{-3} + z^{+3}) + F6(z^{-2} + z^{+2}) + F7(z^{-1} + z^{+1}) + F8(z^{0})\} /1024$$

The coefficient value is represented using the MSB for a sign and the other bits for the effective value in the absolute value.

Table 20B.32 TAP Coefficient Settings

Most Significant Bit	Other Than MSB	Setting Value
0	0 to 4095	0 to +4095
1	0 to 4095	0 to -4095

For the recommended setting value for each filter, see section 20B.3.5(8), Cascade Filter Block.

20B.2.63 Chroma Filter TAP Coefficient (WB_F0 to WB_F8) Registers for Y/C Separation (YCTWB_F0 to YCTWB_F8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	FIL2_2D_WB_F0 to FIL2_2D_WB_F8[12:0]												
Initial value:	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	FIL2_2D_WB_F0 to FIL2_2D_WB_F8 [12:0]	*	R/W	Two-Dimensional Cascade Broadband (SECAM-DB) Filter TAP Coefficients 0 to 8 [12]: Sign [11:0]: Absolute value * Initial values: FIL2_2D_WB_F0: H'100C FIL2_2D_WB_F1: H'0028 FIL2_2D_WB_F2: H'003C FIL2_2D_WB_F3: H'000C FIL2_2D_WB_F4: H'1068 FIL2_2D_WB_F5: H'109C FIL2_2D_WB_F6: H'1040 FIL2_2D_WB_F7: H'0078 FIL2_2D_WB_F8: H'00D0

(1) Two-Dimensional Cascade Broadband (SECAM-DB) Filter TAP Coefficients 0 to 8 Control

FIL2_2D_WB_F0 to FIL2_2D_WB_F8[12:0] control two-dimensional cascade broadband (SECAM-DB) filter TAP coefficients 0 to 8.

The transfer function is defined as follows:

$$H(z) = \{F0(z^{-8} + z^{+8}) + F1(z^{-7} + z^{+7}) + F2(z^{-6} + z^{+6}) + F3(z^{-5} + z^{+5}) + F4(z^{-4} + z^{+4}) + F5(z^{-3} + z^{+3}) + F6(z^{-2} + z^{+2}) + F7(z^{-1} + z^{+1}) + F8(z^{0})\} /1024$$

The coefficient value is represented using the MSB for a sign and the other bits for the effective value in the absolute value.

Table 20B.33 TAP Coefficient Settings

Most Significant Bit	Other Than MSB	Setting Value
0	0 to 4095	0 to +4095
1	0 to 4095	0 to -4095

For the recommended setting value for each filter, see section 20B.3.5(8), Cascade Filter Block.

20B.2.64 Chroma Filter TAP Coefficient (NA_F0 to NA_F8) Registers for Y/C Separation (YCTNA_F0 to YCTNA_F8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	FIL2_2D_NA_F0 to FIL2_2D_NA_F8[12:0]												
Initial value:	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	FIL2_2D_NA_F0 to FIL2_2D_NA_F8[12:0]	*	R/W	Two-Dimensional Cascade Narrowband (3.58/4.43/SECAM-DR) Filter TAP Coefficients 0 to 8 [12]: Sign [11:0]: Absolute value * Initial values: FIL2_2D_NA_F0: H'0018 FIL2_2D_NA_F1: H'002C FIL2_2D_NA_F2: H'0014 FIL2_2D_NA_F3: H'1034 FIL2_2D_NA_F4: H'1080 FIL2_2D_NA_F5: H'1080 FIL2_2D_NA_F6: H'100C FIL2_2D_NA_F7: H'0084 FIL2_2D_NA_F8: H'00C8

(1) Two-Dimensional Cascade Narrowband (3.58/4.43/SECAM-DR) Filter TAP Coefficients 0 to 8 Control

FIL2_2D_NA_F0 to FIL2_2D_NA_F8[12:0] control two-dimensional cascade narrowband (3.58/4.43/SECAM-DR) filter TAP coefficients 0 to 8.

The transfer function is defined as follows:

$$H(z) = \{F0(z^{-8} + z^{+8}) + F1(z^{-7} + z^{+7}) + F2(z^{-6} + z^{+6}) + F3(z^{-5} + z^{+5}) + F4(z^{-4} + z^{+4}) + F5(z^{-3} + z^{+3}) + F6(z^{-2} + z^{+2}) + F7(z^{-1} + z^{+1}) + F8(z^{0})\} /1024$$

The coefficient value is represented using the MSB for a sign and the other bits for the effective value in the absolute value.

Table 20B.34 TAP Coefficient Settings

Most Significant Bit	Other Than MSB	Setting Value
0	0 to 4095	0 to +4095
1	0 to 4095	0 to -4095

For the recommended setting value for each filter, see section 20B.3.5(8), Cascade Filter Block.

20B.2.65 Chroma Filter TAP Coefficient (NB_F0 to NB_F8) Registers for Y/C Separation (YCTNB_F0 to YCTNB_F8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	FIL2_2D_NB_F0 to FIL2_2D_NB_F8[12:0]												
Initial value:	0	0	0	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	FIL2_2D_NB_F0 to FIL2_2D_NB_F8[12:0]	*	R/W	Two-Dimensional Cascade Narrowband (SECAM-DB) Filter TAP Coefficients 0 to 8 [12]: Sign [11:0]: Absolute value * Initial values: FIL2_2D_NB_F0: H'1438 FIL2_2D_NB_F1: H'0AF0 FIL2_2D_NB_F2: H'1CEC FIL2_2D_NB_F3: H'065C FIL2_2D_NB_F4: H'05A4 FIL2_2D_NB_F5: H'1CEC FIL2_2D_NB_F6: H'085C FIL2_2D_NB_F7: H'0178 FIL2_2D_NB_F8: H'1568

(1) Two-Dimensional Cascade Narrowband (SECAM-DB) Filter TAP Coefficients 0 to 8 Control

FIL2_2D_NB_F0 to FIL2_2D_NB_F8[12:0] control two-dimensional cascade narrowband (SECAM-DB) filter TAP coefficients 0 to 8.

The transfer function is defined as follows:

$$H(z) = \{F0(z^{-8} + z^{+8}) + F1(z^{-7} + z^{+7}) + F2(z^{-6} + z^{+6}) + F3(z^{-5} + z^{+5}) + F4(z^{-4} + z^{+4}) + F5(z^{-3} + z^{+3}) + F6(z^{-2} + z^{+2}) + F7(z^{-1} + z^{+1}) + F8(z^{0})\} /1024$$

The coefficient value is represented using the MSB for a sign and the other bits for the effective value in the absolute value.

Table 20B.35 TAP Coefficient Settings

Most Significant Bit	Other Than MSB	Setting Value
0	0 to 4095	0 to +4095
1	0 to 4095	0 to -4095

For the recommended setting value for each filter, see section 20B.3.5(8), Cascade Filter Block.

20B.2.66 Luminance (Y) Signal Gain Control Register (YGAINCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	Y_GAIN2[9:0]									
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	Y_GAIN2 [9:0]	1000000000	R/W	Y Signal Gain Coefficient (0 = 0 times, 512 = 1.0 times, 1023 ≈ 2.0 times)

(1) Y Signal Output Gain Control Y Signal Output Gain Control

Y_GAIN2 controls the Y signal output gain.

Y signal output = Y signal after decoding × (Y_GAIN2/512)

20B.2.67 Color Difference (Cb) Signal Gain Control Register (CBGAINCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CB_GAIN2[9:0]									
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	CB_GAIN2 [9:0]	1000000000	R/W	Cb Signal Gain Coefficient (0 = 0 times, 512 = 1.0 times, 1023 ≈ 2.0 times)

(1) Cb Signal Output Gain Control

CB_GAIN2 controls the Cb signal output gain.

Cb signal output = Cb signal after decoding × (CB_GAIN2/512)

20B.2.68 Color Difference (Cr) Signal Gain Control Register (CRGAINCR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CR_GAIN2[9:0]									
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	CR_GAIN2 [9:0]	1000000000	R/W	Cr Signal Gain Coefficient (0 = 0 times, 512 = 1.0 times, 1023 ≈ 2.0 times)

(1) Cr Signal Output Gain Control

CR_GAIN2 controls the Cr signal output gain.

Cr signal output = Cr signal after decoding × (CR_GAIN2/512)

20B.2.69 PGA Register Update (PGA_UPDATE)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PGA_ VEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PGA_VEN	1	R/W	PGACR Register V Update Enable 1: Enable 0: Disable

(1) PGACR Register V Update Enable

PGA_VEN enables or disables V update of PGACR register.

20B.2.70 PGA Control Register (PGACR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PGA_GAIN_SEL	PGA_GAIN[5:0]						—	—	—	—	—	—	—	—
Initial value:	0	0	0	1	0	1	0	1	0	0	0	0	1	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	PGA_GAIN_SEL	0	R/W	PGA Switch 0: Automatic (AGC) 1: Manual (refer to the PGA_GAIN description below.)
13 to 8	PGA_GAIN[5:0]	010101	R/W	PGA Gain 0 (0.8 Vpp) to 63 (1.6 Vpp)
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: All the bits in this register are updated when the vertical sync signal is asserted with PGA_VEN in PGA_UPDATE being 1.

(1) PGA Switch

When PGA_GAIN_SEL is 0 and ADCCR1.AGCMODE is 1, the AGC-controlled value is reflected on the PGA gain. When PGA_GAIN_SEL is 1, the PGA_GAIN value is directly reflected on the PGA gain. In this case, the ADCCR1.AGCMODE setting is invalid.

Setting ADCCR1.AGCMODE to 0 and PGA_GAIN_SEL to 0 simultaneously is prohibited.

(2) PGA Gain

When PGA_GAIN_SEL is 1, the PGA_GAIN value is reflected on the PGA gain. One of 64 levels of gain values can be set for the PGA of this LSI.

20B.2.71 ADC Control Register 2 (ADCCR2)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ADC_VINSEL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ADC_VINSEL	0	R/W	Input Pin Control 0: VIN1A pin input 1: VIN2A pin input

(1) Input Pin Control

ADC_VINSEL selects the pin for inputting composite video signals.

20B.2.72 ADC Control Register 3 (ADCCR3)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PSAVON	—	—	—	—
Initial value:	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	—	1	R	Reserved These bits are always read as 1. The write value should always be 1.
8 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PSAVON	1	R/W	When the PSAVON bit is set to 1, the clock supply to the A/D converter is halted. 0: The A/D converter runs. 1: Clock supply to the A/D converter is halted.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: When Video decoder output signals are not used, set PSAVON to 1.

(1) The clock supply control to the A/D converter

When PSAVON is 1, the clock supply to the A/D converter is halted.

When PSAVON is 0, the A/D converter runs.

20B.2.73 ADC Control Register 4 (ADCCR4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VIN1 SEL	VIN0 SEL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W:	R/W:

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	VIN1SEL	0	R/W	Video Input Module channel 1 input Select *1, *3 0: Signals supplied via the external input pins 1: Video decoder output signals *2
0	VIN0SEL	0	R/W	Video Input Module channel 0 input Select *1, *3 0: Signals supplied via the external input pins 1: Video decoder output signals *2

Notes: 1. To enable this register to be set, appropriately set the LSI multiplexed pin setting mask register (PMMR) immediately before setting this register.
2. The output interface from digital video decoder to VIN is the 20-bit YCbCr-422 format.
3. To avoid glitch when changing, VIN shall be stopped before VIN input is changed.

(1) Video Input Module channel 1 input Control

VIN1SEL selects input for the channel 1 of Video Input module. The following shows the steps to select video the decoder output signals for the input.

1. Set PMMR to H'FFFFFFFD (32 bit access size).
2. Set ADCCR4 to H'00000002 (32 bit access size).

(2) Video Input Module channel 0 input Control

VIN0SEL selects input for the channel 0 of Video Input module. The following shows the steps to select video the decoder output signals for the input.

1. Set PMMR to H'FFFFFFFE (32 bit access size).
2. Set ADCCR4 to H'00000001 (32 bit access size).

20B.3 Operation

20B.3.1 Overview

This module decodes composite video signals (CVBS) and separates them into horizontal/vertical sync signals, luminance signals (Y), and color difference signals (Cb/Cr). Supported color systems are NTSC, PAL, and SECAM. This module consists of an A/D converter for video signal input, sync separator circuit, burst controlled oscillator (BCO), a Y/C separator circuit, a chroma decoding circuit, a digital clamp circuit, and an output gain adjustment circuit. Figure 20B.25 shows an overall block diagram.

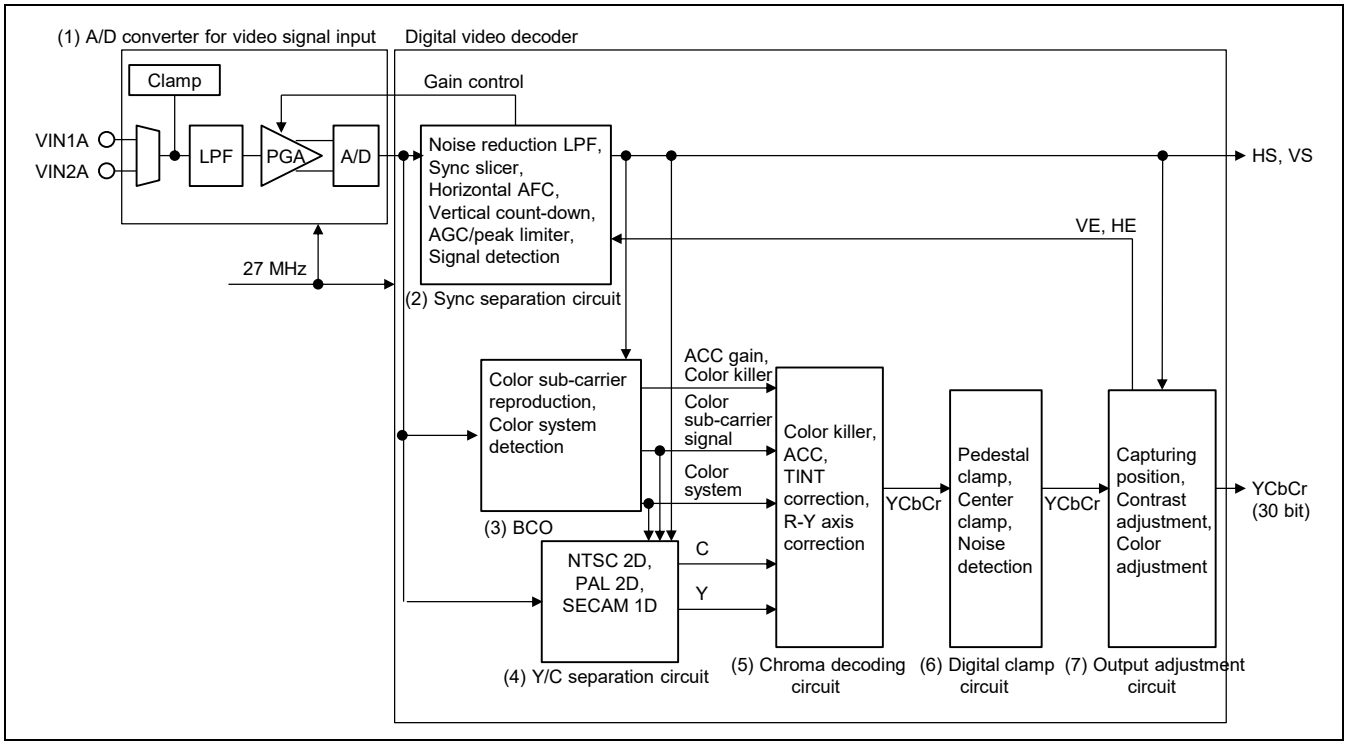


Figure 20B.25 Overall Block Diagram

(1) A/D Converter for Video Signal Input

The A/D converter processes the composite video signal (CVBS) using the sync tip clamp block, the low-pass filter (LPF), and the programmable gain amplifier (PGA) and then A/D-converts the signal. The composite video signals from either VIN1A or VIN2A pin are selected.

(2) Sync Separator Circuit

The sync separator circuit extracts the horizontal and vertical sync signals from the composite video signal. This circuit also detects the amplitude of the sync signals and automatically adjusts the PGA gain (Automatic Gain Control = AGC).

(3) Burst Controlled Oscillator (BCO)

The BCO extracts the color burst signal from the composite video signal and reproduces the color sub-carrier signal required for color demodulation. The BCO also acquires phase and frequency information from the color burst signal and detects the color system used.

(4) Y/C Separator Circuit

The Y/C separator circuit separates the composite video signal of the NTSC, PAL, or SECAM format into the Y and C signals. Two-dimensional adaptive separation is used for NTSC and PAL and one-dimensional separation for SECAM.

(5) Chroma Decoding Circuit

The chroma decoding circuit demodulates the C signal extracted by the Y/C separator circuit into the Cb/Cr signal. This circuit has the automatic color control function (ACC), in which the amplitude of the color burst signal is detected to adjust the color gain automatically and also has the TINT/R-Y axis correction function, in which hue is adjusted at demodulation.

(6) Digital Clamp Circuit

The digital clamp circuit provides pedestal clamp for the Y signals and center clamp for the Cb/Cr signals at any position. This circuit also detects the amount of noise using the autocorrelation function.

(7) Output Adjustment Circuit

The output adjustment circuit sets the capturing position and adjusts the contrast and color.

20B.3.2 A/D Converter for Video Signal Input

The A/D converter processes the composite video signal (CVBS) using the sync tip clamp block, the low-pass filter (LPF), and the programmable gain amplifier (PGA) and then A/D-converts the signal.

Figure 20B.26 shows the block diagram of the A/D converter for video signal input.

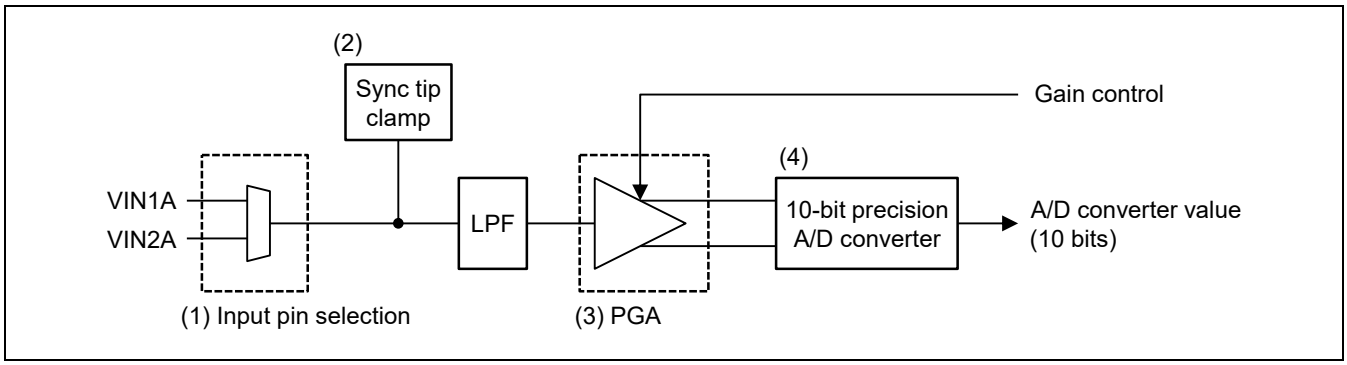


Figure 20B.26 Block Diagram of A/D Converter for Video Signal Input

Figure 20B.27 shows the waveforms when a video signal is A/D-converted.

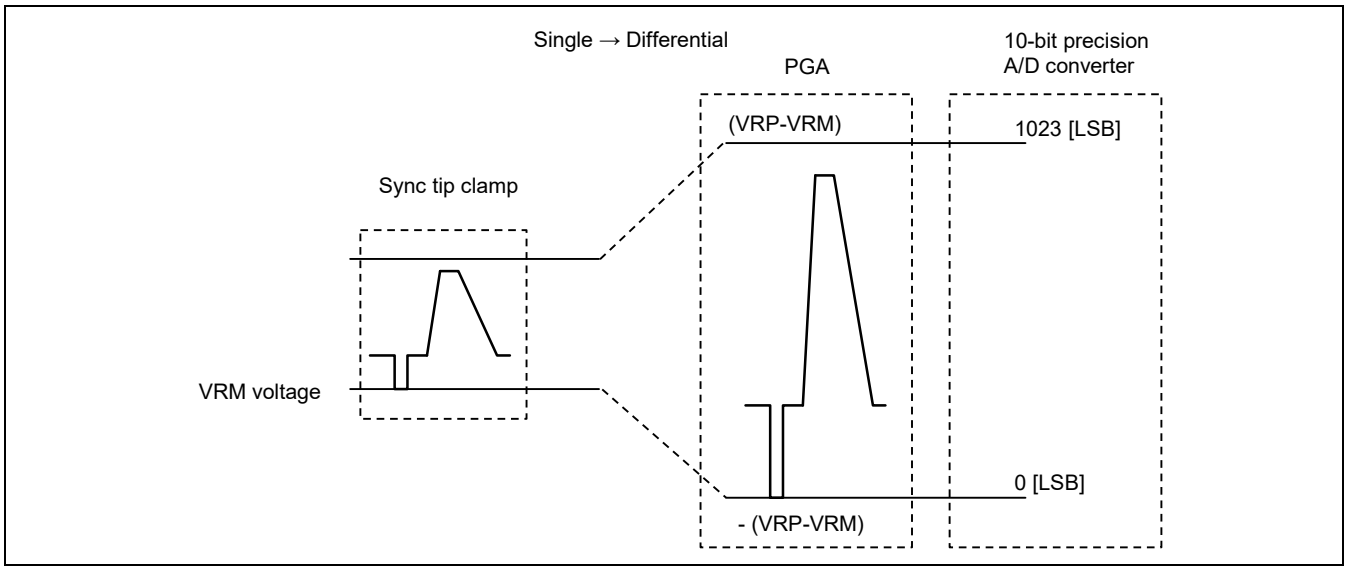


Figure 20B.27 A/D Conversion Image

(1) Input Pin Selection Block

The input pin selection block selects either the VIN1A or VIN2A pin for inputting the signal according to the ADCCR2.ADC_VINSEL setting.

(2) Sync Tip Clamp Block

The sync tip clamp block clamps the sync tip level to about 0.5 V.

(3) Programmable Gain Amplifier (PGA)

The PGA adjusts the gain so that the input video signal voltage (≈ 0.8 Vpp to 1.6 Vpp) should be the level to be input to the A/D converter (≈ 2.0 Vpp). One of 64 levels of gain values can be set. One level corresponds to gain of 0.1 dB (typ.). The minimum gain is 0 dB (typ.) and maximum gain is 6.02 dB (typ.).

Table 20B.36 shows the PGA gain setting and gain values.

Table 20B.36 PGA Gain Setting and Gain Values (dB)

PGA Gain Setting	Input Range (Vpp)	Gain Value (dB)
0	1.600	0
1	1.587	0.069
2	1.575	0.138
3	1.562	0.209
4	1.549	0.280
5	1.537	0.351
6	1.524	0.423
7	1.511	0.496
8	1.498	0.569
9	1.486	0.643
:	:	:
59	0.851	5.48
60	0.838	5.61
61	0.825	5.74
62	0.813	5.88
63	0.800	6.02

The PGA gain can be set using PGACR.PGA_GAIN[5:0] with PGACR.PGA_GAIN_SEL = 1. When the AGC function is on (ADCCR1.AGCMODE = 1), the gain is automatically set.

(4) 10-Bit Precision A/D Converter

The 10-bit precision A/D converter receives the gain-adjusted video signal from the PGA and A/D-converts the signal. The converter has 10-bit resolution and performs sampling at 27 MHz, which is the frequency of the clock signal input via VIDEO_X1 or VIDEO_X2.

20B.3.3 Sync Separator Circuit

The sync separator circuit extracts the horizontal and vertical sync signals from the composite video signal. This circuit also detects the amplitude of the sync signals and automatically adjusts the PGA gain (Automatic Gain Control = AGC).

Figure 20B.28 shows the block diagram of the sync separator circuit.

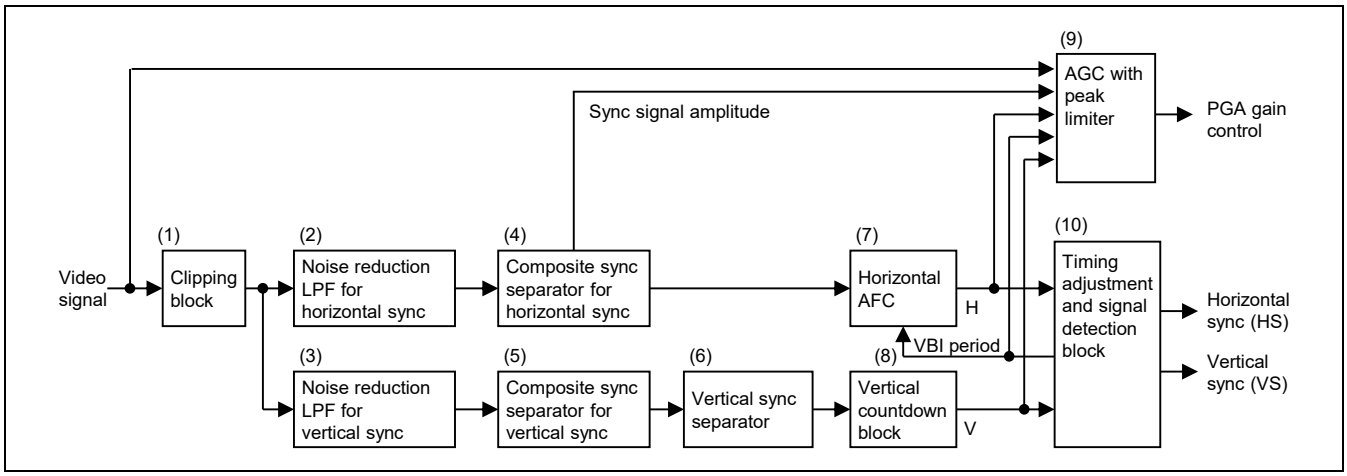


Figure 20B.28 Block Diagram of Sync Separator Circuit

(1) Clipping Block

The clipping block clips the high tone component of the video signal to reduce amplitude-dependency of the video signal. The specific clipping level can be set using SYNSCR3.SSCLIPSEL[3:0].

The clipping level should be within the range so that the composite sync signal component should not be deteriorated (should be detectable).

(2) Noise Reduction Low-Pass Filter (LPF) for Horizontal Sync

The noise reduction LPF reduces the superimposed noise on the video signals before composite sync signal separation. The LPFs can be separately set for the horizontal sync and vertical sync. The cutoff frequency of the horizontal sync LPF can be set using SYNSCR1.LPFHSYNC[2:0]. The cutoff frequency should be within the range so that the composite sync signal component should not be deteriorated (should be detectable).

(3) Noise Reduction Low-Pass Filter (LPF) for Vertical Sync

The noise reduction LPF reduces the superimposed noise on the video signals before composite sync signal separation. The LPFs can be separately set for the horizontal sync and vertical sync. The cutoff frequency of the vertical sync LPF can be set using SYNSCR1.LPFVSYNC[2:0]. The cutoff frequency should be within the range so that the composite sync signal component should not be deteriorated (should be detectable).

(4) Composite Sync Separator for Horizontal Sync

The composite sync separator separates the composite sync signal from the video signal according to the slice level. The composite sync slice levels can be separately set for the horizontal and vertical sync signals. The slice level can be set either automatically or manually according to the SYNSCR1.SLICERMODE_H[1:0] setting.

When automatic setting is used, the slice level is automatically set according to the SYNSCR1.SLICERMODE_H[1:0], SYNSCR2.SYNCMAXDUTY_H[5:0], and SYNSCR2.SYNCMINDUTY_H[5:0] setting. The slice level detection speed can be set using SYNSCR1.VELOCITYSHIFT_H[3:0].

When manual setting is used, the slice level is determined by SYNSCR3.CSYNCSLICE_H[9:0].

(5) Composite Sync Separator for Vertical Sync

The composite sync separator separates the composite sync signal from the video signal according to the slice level. The composite sync slice levels can be separately set for the horizontal and vertical sync signals. The slice level can be set either automatically or manually according to the SYNSCR1.SLICERMODE_V[1:0] setting.

When automatic setting is used, the slice level is automatically set according to the SYNSCR1.SLICERMODE_V[1:0], SYNSCR4.SYNCMAXDUTY_V[5:0], and SYNSCR4.SYNCMINDUTY_V[5:0] setting.

When manual setting is used, the slice level is determined by SYNSCR5.CSYNCSLICE_V[9:0].

(6) Vertical Sync Separator

The vertical sync separator extracts the vertical sync signal from the composite video signal separated using (5) above. The threshold value for separating the vertical sync signal can be set using SYNSCR5.VSYNCSLICE[4:0]. The value should be set depending on the serration pulse width of each video signal format.

(7) Horizontal Automatic Frequency Control (AFC) Block

The horizontal AFC, which is a digital PLL, extracts the horizontal sync signal from the composite video signal separated using (4) above. The AFC removes the pseudo horizontal sync signal and interpolates the incomplete horizontal sync signal to generate a stable horizontal sync signal.

The center frequency and lock range of the horizontal AFC can be set using HAFCCR1.HAFCTYP[9:0], HAFCCR2.HAFCMAX[9:0], and HAFCCR3.HAFCMIN[9:0]. If the horizontal AFC is locked, VSYNCSR.FHLOCK becomes 1; and if the horizontal AFC is unlocked, VSYNCSR.FHLOCK becomes 0. The horizontal AFC oscillation cycle can be checked by reading HSYNCSR.FHCOUNT[16:1] and VSYNCSR.FHCOUNT[0].

The loop gain (response speed) of the horizontal AFC can be set using HAFCCR1.HAFCCGAIN[3:0]. As the speed is increased, the lockup time becomes shorter. However, the horizontal oscillation frequency will be more susceptible to noise. With HAFCCR3.HAFCMODE[1], AFCPFCR.PHDET_FIX, and AFCPFCR.PHDET_DIV[2:0], the loop gain can be reduced when S/N is low to prevent malfunction attributed to noise. Whether S/N is low or not can be checked with VSYNCSR.ISNOISY.

The loop gain during the vertical blanking period (VBI) can be set using HAFCCR2.HAFCSTART[3:0], HAFCCR3.HAFCEND[3:0], and HAFCCR3.HAFCMODE[0]. This is usually used to avoid malfunction in the VCR head switch.

(8) Vertical Countdown Block

The vertical countdown block removes the pseudo vertical sync signal from the vertical sync signal separated using (6) above and interpolates the incomplete vertical sync signal to generate a stable vertical sync signal.

The oscillation cycle of the vertical countdown block can be set using VCDWCR1.VCDDEFAULT[1:0]. When set to 0, the input vertical sync signal is detected and the oscillation cycle is automatically set appropriately. The detection result of the input vertical sync signal is indicated by VSYNCSR.FVMODE. When set to 1, 50.00-Hz oscillation mode is set. Here, it is recommended to set VCDWCR1.NOVCD60 to 1 (60-Hz oscillation off) to avoid unexpected malfunction. When set to 2 or 3, 59.94-/60.00-Hz oscillation mode is set. Here, it is recommended to set VCDWCR1.NOVCD50 to 1 (50-Hz oscillation off) to avoid unexpected malfunction.

The lock range of the vertical countdown block can be set using VCDWCR1.VCDWINDOW[5:0] and VCDWCR1.VCDOFFSET[4:0]. If the vertical countdown block is locked, VSYNCSR.FVLOCK becomes 1; and if the vertical countdown block is unlocked, VSYNCSR.FVLOCK becomes 0.

The cycle of the input vertical sync signal can be checked by reading VSYNCSR.FVCOUNT[7:0]. When the vertical sync signal input cannot be detected, VSYNCSR.NOSIGNAL is set to 1.

(9) Automatic Gain Control (AGC) Block with Peak Limiter

The AGC block detects the amplitude of the sync signal and automatically controls the PGA gain to the target value. The AGC function is activated with ADCCR1.AGCMODE = 1.

- Gain Control according to Sync Amplitude

  The target sync signal amplitude can be set using AGCCR1.AGCLEVEL[8:0] and AGCCR2.AGCPRECIS[5:0]. For example, when NTSC signals are quantized by the 10-bit A/D converter, the sync signal amplitude for the full range of the A/D converter can be provided by:

  $1023[LSB] \times (40[IRE] \div 173[IRE]) = 236.53179[LSB]$

  Therefore, 236[LSB] should be set to AGCCR1.AGCLEVEL[8:0]. The gain is fixed when it falls within the following range.

  Target value (= AGCCR1.AGCLEVEL[8:0]) ± AGCCR2.AGCPRECIS[5:0]

  Whether the gain is fixed or not can be checked by reading AGCCSR2.AGCCONVERGE. The detected sync signal amplitude can be checked using SYNCSSR.SYNCDEPTH[9:0]. The AGC response speed can be set using AGCCR1.AGCRESPONSE[2:0]. As the speed is increased, the input signal is tracked more quickly; however, it will result in higher susceptibility to noise.

  The currently set gain value can be checked using AGCCSR2.AGCGAIN[7:0]. The actual PGA gain setting can be roughly calculated as follows:

  $1.203008 \times (AGCCSR2.AGCGAIN[7:0] - 48)$

  For example, when AGCCSR2.AGCGAIN[7:0] is 64 (corresponding to ×1),

  $PGA\ gain\ setting = 1.203008 \times (64 - 48) \approx 19.24$

  As a result, the PGA gain setting is 19 or 20. One of 0 to 63 can be set as the PGA gain value.

  The gain during vertical blanking period (VBI) can be set using AGCCR1.DOREDUCE and AGCCR1.NOREDUCE. The sync amplitude detection result during VBI can be read from SYNCSSR.ISREDUCED.

- Peak Limiter

  The peak limiter works when the ratio of the video signal amplitude to the sync signal amplitude is inappropriate. If the ratio is smaller than expected, the PGA gain becomes smaller, and the video signal after gain adjustment becomes smaller than the full range of the A/D converter. Contrarily, if the ratio is larger than expected, the PGA gain becomes larger, and the video signal after gain adjustment becomes larger than the full range of the A/D converter.

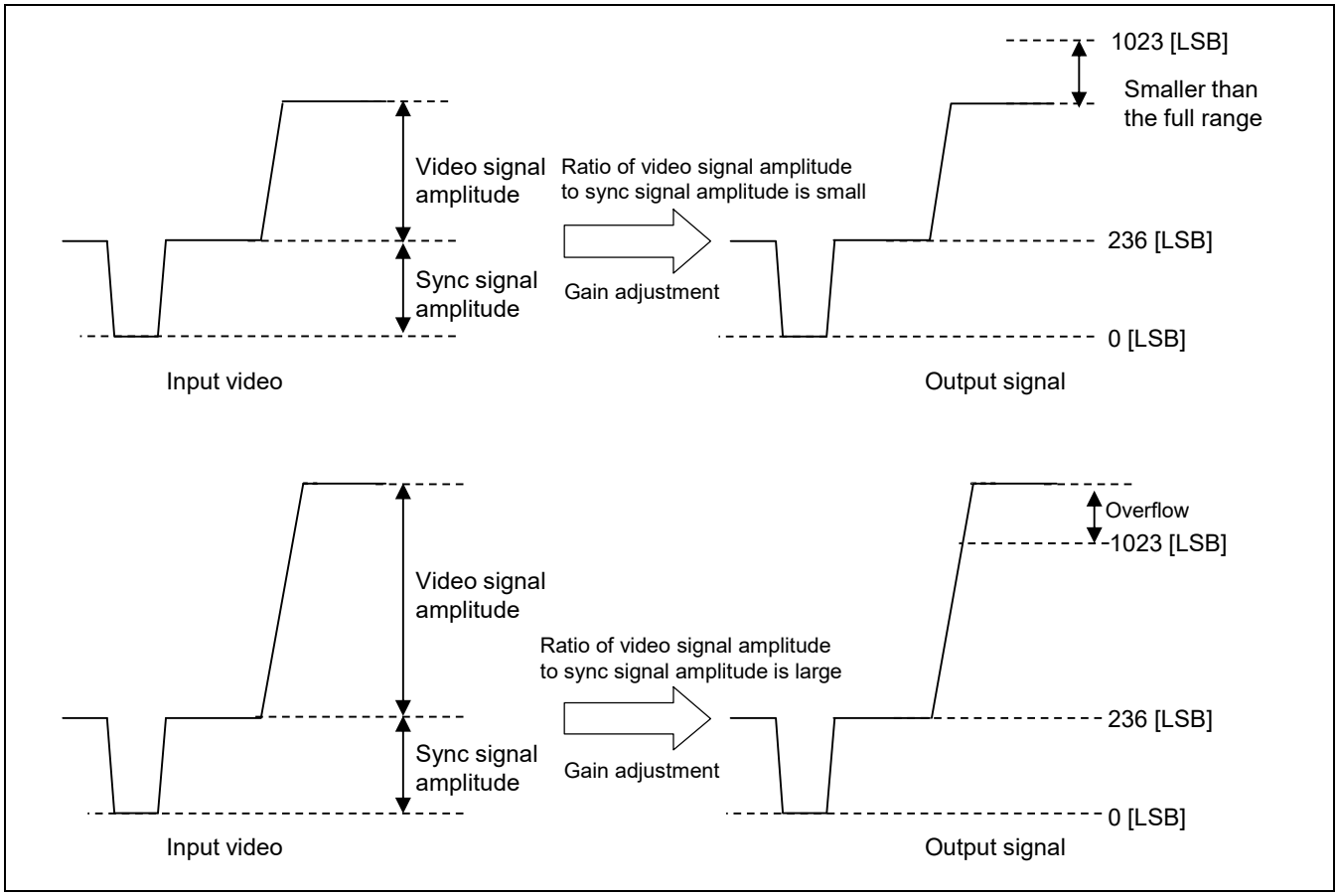


Figure 20B.29 Cases in which Ratio of Video Signal Amplitude to Sync Signal Amplitude is Inappropriate

To deal with this problem, the peak limiter adjusts the PGA gain based on the sampled video signal peak value. The peak value used to control the gain can be set using PKLIMITCR.PEAKLEVEL[1:0]. When the peak value of the sampled video signal is smaller than the value set using PKLIMITCR.PEAKLEVEL[1:0], the gain is increased. Contrarily, when the peak value of the sampled video signal is larger than the value set using PKLIMITCR.PEAKLEVEL[1:0] exceeding the maximum allowable value set using PKLIMITCR.MAXPEAKSAMPLES[7:0], the gain is decreased.

The gain increase/decrease response speed and maximum compression ratio can be set using PKLIMITCR.PEAKATTACK[1:0], PKLIMITCR.PEAKRELEASE[1:0], and PKLIMITCR.PEAKRATIO[1:0]. The number of pixels with the peak value larger than the value set using PKLIMITCR.PEAKLEVEL[1:0] can be checked with AGCCSR1.HIGHSAMPLES[7:0]; and the number of overflowing pixels (exceeding 1023[LSB]) can be checked with AGCCSR1.PEAKSAMPLES[7:0].

- Manual Setting

  Manual setting of the PGA gain can be enabled by setting PGACR.PGA_GAIN_SEL to 1. Here, the value set using PGACR.PGA_GAIN[5:0] is actually set as the PGA gain. When PGACR.PGA_GAIN_SEL is 1, ADCCR1.AGCMODE setting is invalid. Setting PGACR.PGA_GAIN_SEL to 0 (automatic setting) and ADCCR1.AGCMODE to 0 (AGC off) simultaneously is prohibited.

(10) Timing Adjustment and Signal Detection Block

The timing adjustment and signal detection block adjusts the output timing of the horizontal and vertical sync signals generated using (7) and (8) above. This block also detects the field; whether the interlaced or progressive system is used can be checked with VSYNCSR.INTERLACED. If the field detection function is unstable, setting SYNSCR5.VSYNCDELAY to 1 may improve the function.

20B.3.4 Burst Controlled Oscillator (BCO)

The BCO extracts the color burst signal from the composite video signal and reproduces the color sub-carrier signal required for color demodulation. It also acquires the phase and frequency information from the color burst signal and detects the color system used.

Figure 20B.30 shows the block diagram of the BCO.

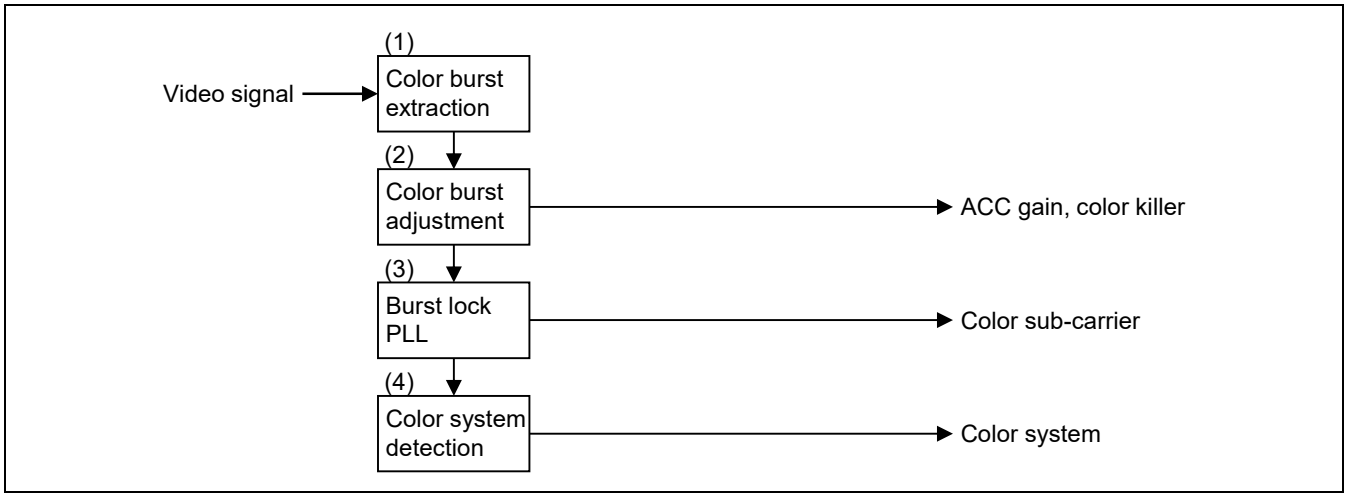


Figure 20B.30 Block Diagram of Burst Controlled Oscillator

(1) Color Burst Extraction Block

The color burst extraction block extracts the color burst signal. The position of the color burst signal to be extracted can be adjusted using BTGPCR.BGPWIDTH[6:0] and BTGPCR.BGPSTART[7:0]. The extraction result of the color burst signal can be checked by reading CROMASR1.NOBURST.

(2) Color Burst Adjustment Block

The color burst adjustment block adjusts the amplitude of the extracted color burst signal. For details, refer to section 20B.3.6(1), Automatic Color Control (ACC) Block. This block also outputs the signal to turn on or off the color killer according to the amplitude of the input color burst signal. For details, refer to section 20B.3.6(2), Color Killer.

(3) Burst Lock PLL

The burst lock PLL is a digital PLL which reproduces the color sub-carrier signal from the adjusted color burst signal.

The lock range of the burst lock PLL can be set using BTLCR.LOCKRANGE[1:0]. If the burst lock PLL is locked, CROMASR1.FSCLOCK becomes 1; and if unlocked, CROMASR1.FSCLOCK becomes 0.

The loop gain of the burst lock PLL can be set using BTLCR.LOOPGAIN[1:0] and BTLCR.LOCKLIMIT[1:0]. As the response speed is increased and the frequency search is started earlier, the lockup time becomes shorter. However, the PLL becomes unstable and unlocked more easily due to noise.

The S/N of the color burst signal can be checked using CROMASR2.LOCKLEVEL[7:0].

(4) Color System Detection Block

The color system detection block detects the color system of the input video signal based on the oscillation frequency of the burst lock PLL and phase information of the color burst signal. The color system can be detected using BTLCR.NONTSC358, BTLCR.NONTSC443, BTLCR.NOPALM, BTLCR.NOPALN, BTLCR.NOPAL443, and BTLCR.NOSECAM. Color system detection can be set to fully automatic, manual, or semi-automatic (detecting the specified color system only). If the detection result does not apply to any color system type, the color system selected with BTLCR.DEFAULTSYS[1:0] is assumed.

When an NTSC, PAL, or SECAM signal is detected, 1 is read from CROMASR2.ISNTSC, CROMASR2.ISPAL, or CROMASR2.ISSEAM, respectively. The currently used color system can be checked by reading CROMASR1.COLORSYS[1:0].

The color sub-carrier frequency can be checked by reading CROMASR1.FSCMODE.

20B.3.5 Y/C Separator Circuit

The Y/C separator circuit separates the composite video signal of the NTSC, PAL, or SECAM format into the Y and C signals. Two-dimensional adaptive separation is used for NTSC and PAL and one-dimensional separation for SECAM.

Figure 20B.31 shows a block diagram of the Y/C separator circuit.

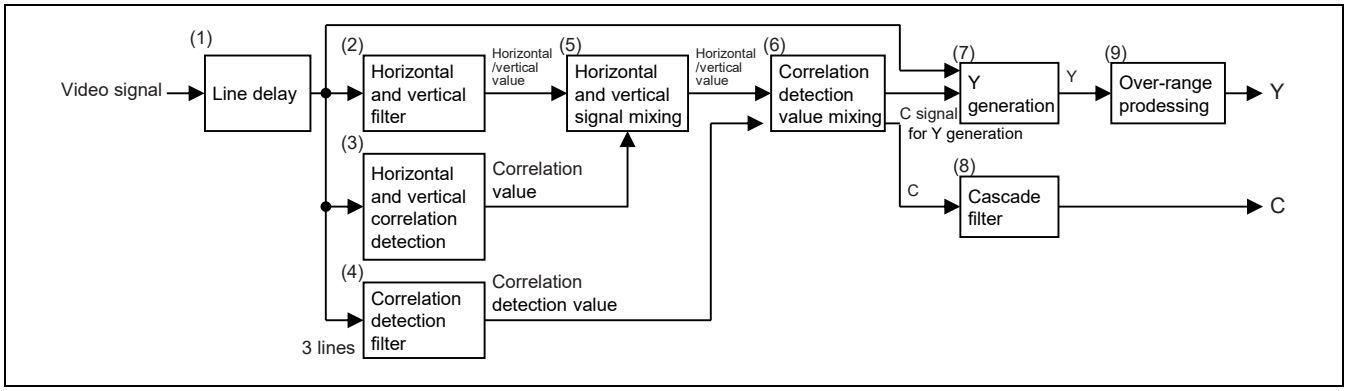


Figure 20B.31 Block Diagram of Y/C Separator Circuit

Table 20B.37 shows the operation of the Y/C separator circuit for each color format.

Table 20B.37 Y/C Separation Operation for Each Color Format

Color Format	YC Separation Operation
NTSC-3.58	Two dimensional
NTSC-4.43	Two dimensional
PAL-M	Two dimensional
PAL-N	Two dimensional
PAL-4.43	Two dimensional
SECAM	One dimensional

(1) Line Delay Block

In two-dimensional Y/C separation, three lines of data is required (directly adjacent three lines for NTSC and adjacent three lines on every second line for PAL). This block delays video signals to hold three lines of data.

(2) Horizontal and Vertical Filter Block

In two-dimensional adaptive Y/C separation, the horizontal band pass filter (BPF), vertical band pass filter (BPF), and horizontal/vertical band pass filter (BPF) are adaptively switched according to the correlation between the horizontally-/vertically-adjacent pixels. This block processes the input signals using the horizontal BPF, vertical BPF, or horizontal/vertical BPF. In one-dimensional Y/C separation, only the horizontal BPF is used. Figure 20B.32 shows the filter configuration.

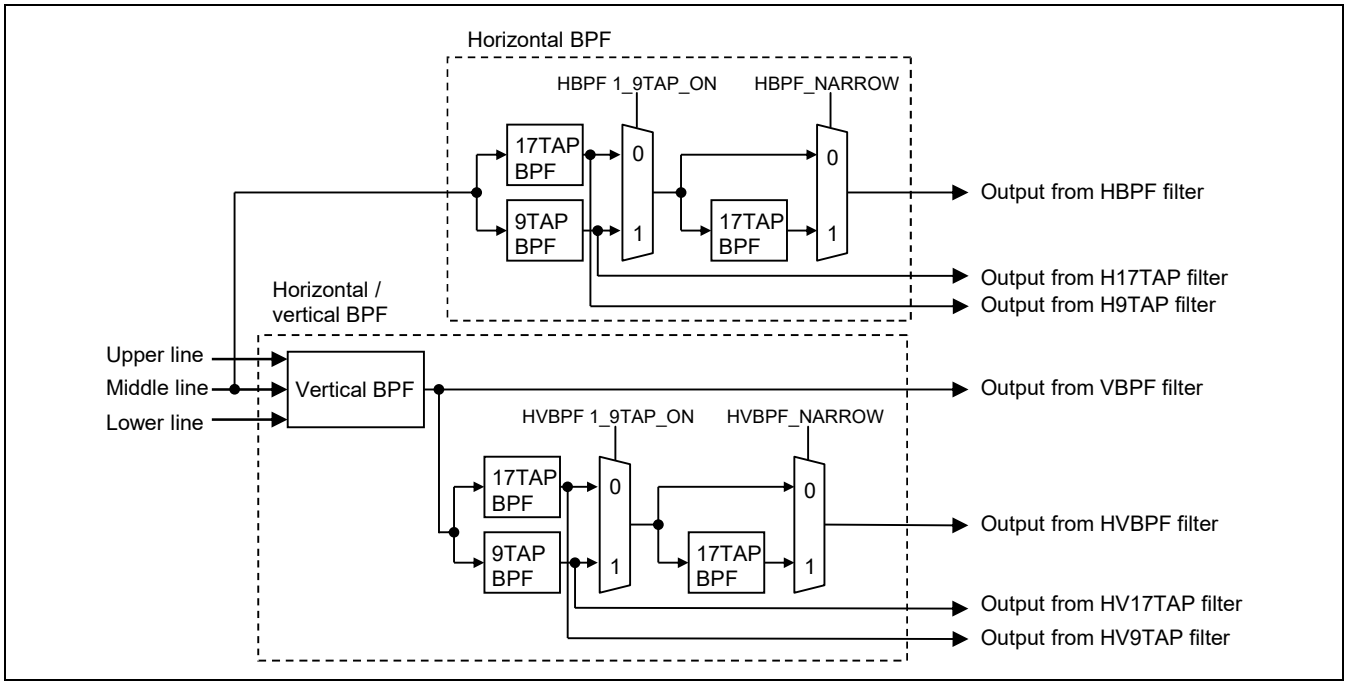


Figure 20B.32 Horizontal and Vertical Filter Configuration

The horizontal BPF is composed of two stages. Either the 9-TAP or 17-TAP BPF is selected at the former stage. When YCSCR8.HBPF1_9TAP_ON/HVBPF1_9TAP_ON is 0, the 17-TAP BPF is selected; and when 1, the 9-TAP BPF is selected. Either bypass operation or the 17-TAP BPF is selected at the latter stage. When YCSCR8.HBPF_NARROW/HVBPF_NARROW is 0, bypass operation is selected; and when 1, the 17-TAP BPF is selected.

(3) Horizontal and Vertical Correlation Detection Block

The horizontal and vertical correlation detection block detects the correlation value between the horizontal pixels, vertical pixels, and horizontal/vertical pixels. The value obtained by mixing the detected correlation value and the two-dimensional Y/C separation filter select coefficient is used for selecting the appropriate horizontal, vertical, or horizontal/vertical filter.

Table 20B.38 shows the two-dimensional Y/C separation filter select coefficients.

Table 20B.38 Two-Dimensional Y/C Separation Filter Select Coefficients

Category	Bit Name	Description	Bit Correlation
Vertical Y/C separation select coefficients	YCSCR5.K21A[5:0]	As the value becomes larger, the vertical BPF is applied to the narrower range.	There is correlation between these bits. When horizontal dot crawl is conspicuous, make the bit field value smaller (make the K24 value larger). However, when the value is too small (K24 is too large), vertical dot crawl is produced.
	YCSCR5.K22A[7:0]	As the value becomes larger, the vertical BPF is applied to the narrower range.	
	YCSCR7.K23A[3:0]	As the value becomes larger, the vertical BPF is applied to the narrower range.	
	YCSCR7.K24[4:0]	As the value becomes larger, the vertical BPF is applied to the wider range.	
	YCSCR6.K21B[5:0]	As the value becomes larger, the vertical BPF is applied to the narrower range.	There is correlation between these bits. When horizontal dot crawl is conspicuous, make the bit field value smaller. However, when the value is too small, vertical dot crawl is produced.
	YCSCR6.K22B[7:0]	As the value becomes larger, the vertical BPF is applied to the narrower range.	
	YCSCR7.K23B[3:0]	As the value becomes larger, the vertical BPF is applied to the narrower range.	
Horizontal Y/C separation select coefficients	YCSCR3.K11[5:0]	As the value becomes larger, the horizontal BPF is applied to the narrower range.	There is correlation between these bits. When vertical dot crawl is conspicuous, make the bit field value smaller. However, when the value is too small, horizontal dot crawl is produced.
	YCSCR3.K13[5:0]	As the value becomes larger, the horizontal BPF is applied to the narrower range.	
	YCSCR3.K15[3:0]	As the value becomes larger, the horizontal BPF is applied to the narrower range.	
	YCSCR4.K12[5:0]	As the value becomes larger, the horizontal BPF is applied to the narrower range.	There is correlation between these bits. When vertical dot crawl is conspicuous, make the bit field value smaller. However, when the value is too small, horizontal dot crawl is produced.
	YCSCR4.K14[5:0]	As the value becomes larger, the horizontal BPF is applied to the narrower range.	
	YCSCR4.K16[3:0]	As the value becomes larger, the horizontal BPF is applied to the narrower range.	

(4) Correlation Detection Filter Block

The correlation detection filter block, specific to this module, attaches greater importance to the correlation between lines to reduce dot crawl, especially at the intersection of a cross. By mixing the signals after correlation detection filter block, dot crawl can be reduced when dot crawl is not fully removed by the horizontal and vertical filter block.

(5) Horizontal and Vertical Signal Mixing Block

The horizontal and vertical signal mixing block mixes the signals output from the horizontal, vertical, and horizontal/vertical filter blocks with the signals output from the horizontal and horizontal/vertical filters of the former stage. After that, the appropriate signal is selected from among the signals output from the horizontal, vertical, and horizontal/vertical filters according to the correlation value obtained using (3). Figure 20B.33 shows the configuration of the horizontal and vertical signal mixing block.

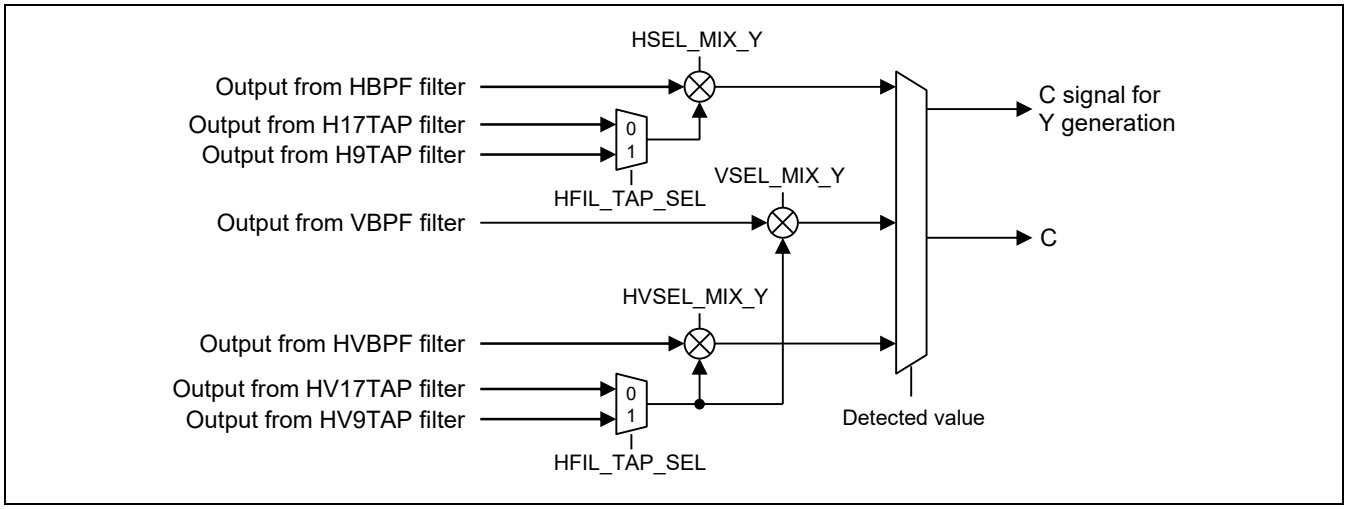


Figure 20B.33 Configuration of Horizontal and Vertical Signal Mixing Block

The signal to be mixed, which is output from either the horizontal or horizontal/vertical filter of the former stage, can be selected with YCSCR8.HFIL_TAP_SEL. When YCSCR8. HFIL_TAP_SEL is 0, the signal output from the 17-TAP filter is selected; and when 1, the signal output from the 9-TAP filter is selected.

This block mixes the signals output from the horizontal filter with the signals output from the above described horizontal filter of the former stage. The mixing ratio can be set with YCSCR9.HSEL_MIX_Y[3:0]. Similarly, this block mixes the signals output from the vertical or horizontal/vertical filter with the signals output from the above described horizontal/vertical filter of the former stage. The mixing ratio can be set with YCSCR9.VSEL_MIX_Y[3:0] and YCSCR9.HVSEL_MIX_Y[3:0].

This block selects the appropriate signal from among the signals output from the horizontal, vertical, and horizontal/vertical filters according to the correlation value obtained using (3).

(6) Correlation Detection Value Mixing Block

The correlation detection value mixing block mixes the C signal for Y generation and the C signal generated using (5) with the signals after correlation detection filter block (4).

Figure 20B.34 shows the configuration of the correlation detection value mixing block.

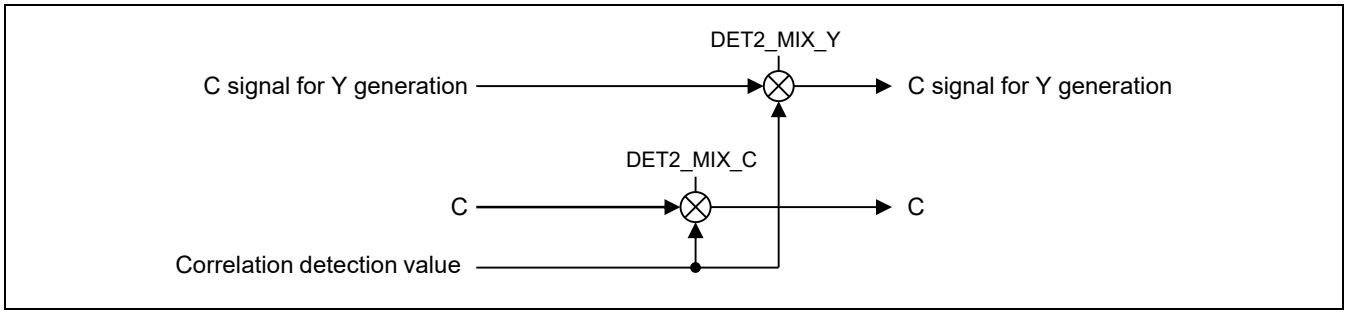


Figure 20B.34 Configuration of Correlation Detection Value Mixing Block

When YCSCR9.DET2_ON is 1, this block mixes the signal after the correlation detection filter block. The mixing ratio of the C signal for Y generation to the signal after the correlation detection filter block can be set with YCSCR12.DET2_MIX_Y[3:0]. Similarly, the mixing ratio of the C signal to the signal after the correlation detection filter block can be set with YCSCR12.DET2_MIX_C[3:0].

When YCSCR9.DET2_ON is 0, this block outputs the signal after the horizontal and vertical filter block without mixing.

(7) Y Generation Block

The Y generation block generates the Y signal by subtracting the C signal for Y generation from the video signal.

(8) Cascade Filter Block

The cascade filter block allows the C signal to pass through the cascade filter or TAKE-OFF filter to further narrow the bandwidth.

Figure 20B.35 shows the configuration of the cascade filter block.

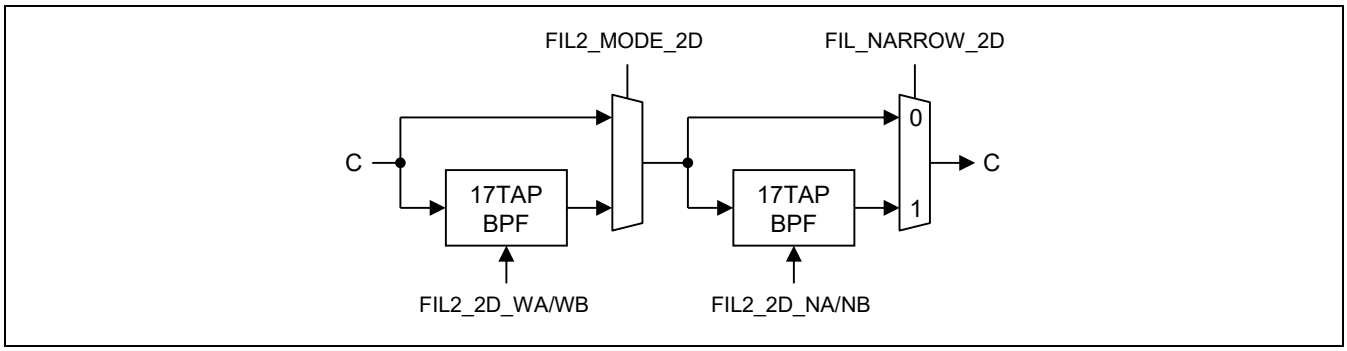


Figure 20B.35 Configuration of Cascade Filter Block

The cascade filter block is composed of two stages. Either bypass operation or 17-TAP filter is selected at the former stage. Bypass operation, cascade, or TAKE-OFF filter can be selected at the former stage with YCSCR12.FIL2_MODE_2D[1:0].

Similarly, either bypass operation or 17-TAP filter can be selected at the latter stage with YCSCR12.FIL2_NARROW_2D.

Both of the former- and latter-stage filters are universal and can be set with YCTWA_F0 to YCTWA_F8, YCTWB_F0 to YCTWB_F8, YCTNA_F0 to YCTNA_F8, and YCTNB_F0 to YCTNB_F8.

Table 20B.39 to Table 20B.41 show the recommended setting for each filter.

Table 20B.39 Recommended Settings for Two-Dimensional Y/C Filters (NTSC)

	NTSC						NTSC				
		Cascade Filter		TAKE-OFF Filter				Cascade Filter		TAKE-OFF Filter	
Bit Name	Bypass Operation	1 Stage	2 Stages	Broad-band	Narrow-band	Bit Name	Bypass Operation	1 Stage	2 Stages	Broad-band	Narrow-band
FIL2_MODE_2D	0	1		2		FIL2_MODE_2D	0	1		2	
FIL2_NARROW_2D	—	0	1	—	—	FIL2_NARROW_2D	—	0	1	—	—
FIL2_2D_WA_F0	—	24	24	0	0	FIL2_2D_NA_F0	—	—	24	—	—
FIL2_2D_WA_F1	—	44	44	0	-48	FIL2_2D_NA_F1	—	—	44	—	—
FIL2_2D_WA_F2	—	20	20	0	-20	FIL2_2D_NA_F2	—	—	20	—	—
FIL2_2D_WA_F3	—	-52	-52	-28	160	FIL2_2D_NA_F3	—	—	-52	—	—
FIL2_2D_WA_F4	—	-128	-128	96	232	FIL2_2D_NA_F4	—	—	-128	—	—
FIL2_2D_WA_F5	—	-128	-128	228	-116	FIL2_2D_NA_F5	—	—	-128	—	—
FIL2_2D_WA_F6	—	-12	-12	-916	-900	FIL2_2D_NA_F6	—	—	-12	—	—
FIL2_2D_WA_F7	—	132	132	-204	-4	FIL2_2D_NA_F7	—	—	132	—	—
FIL2_2D_WA_F8	—	200	200	1648	1392	FIL2_2D_NA_F8	—	—	200	—	—
FIL2_2D_WB_F0	—	—	—	—	—	FIL2_2D_NB_F0	—	—	—	—	—
FIL2_2D_WB_F1	—	—	—	—	—	FIL2_2D_NB_F1	—	—	—	—	—
FIL2_2D_WB_F2	—	—	—	—	—	FIL2_2D_NB_F2	—	—	—	—	—
FIL2_2D_WB_F3	—	—	—	—	—	FIL2_2D_NB_F3	—	—	—	—	—
FIL2_2D_WB_F4	—	—	—	—	—	FIL2_2D_NB_F4	—	—	—	—	—
FIL2_2D_WB_F5	—	—	—	—	—	FIL2_2D_NB_F5	—	—	—	—	—
FIL2_2D_WB_F6	—	—	—	—	—	FIL2_2D_NB_F6	—	—	—	—	—
FIL2_2D_WB_F7	—	—	—	—	—	FIL2_2D_NB_F7	—	—	—	—	—
FIL2_2D_WB_F8	—	—	—	—	—	FIL2_2D_NB_F8	—	—	—	—	—

Table 20B.40 Recommended Settings for Two-Dimensional Y/C Filters (PAL)

	NTSC						NTSC				
		Cascade Filter		TAKE-OFF Filter				Cascade Filter		TAKE-OFF Filter	
Bit Name	Bypass Operation	1 Stage	2 Stages	Broad-band	Narrow-band	Bit Name	Bypass Operation	1 Stage	2 Stages	Broad-band	Narrow-band
FIL2_MODE_2D	0	1		2		FIL2_MODE_2D	0	1		2	
FIL2_NARROW_2D	—	0	1	—	—	FIL2_NARROW_2D	—	0	1	—	—
FIL2_2D_WA_F0	—	-20	-20	0	0	FIL2_2D_NA_F0	—	—	-20	—	—
FIL2_2D_WA_F1	—	24	24	0	0	FIL2_2D_NA_F1	—	—	24	—	—
FIL2_2D_WA_F2	—	64	64	0	-23	FIL2_2D_NA_F2	—	—	64	—	—
FIL2_2D_WA_F3	—	40	40	16	-46	FIL2_2D_NA_F3	—	—	40	—	—
FIL2_2D_WA_F4	—	-76	-76	59	145	FIL2_2D_NA_F4	—	—	-76	—	—
FIL2_2D_WA_F5	—	-164	-164	85	409	FIL2_2D_NA_F5	—	—	-164	—	—
FIL2_2D_WA_F6	—	-84	-84	-498	-918	FIL2_2D_NA_F6	—	—	-84	—	—
FIL2_2D_WA_F7	—	108	108	-101	-363	FIL2_2D_NA_F7	—	—	108	—	—
FIL2_2D_WA_F8	—	216	216	878	1592	FIL2_2D_NA_F8	—	—	216	—	—
FIL2_2D_WB_F0	—	—	—	—	—	FIL2_2D_NB_F0	—	—	—	—	—
FIL2_2D_WB_F1	—	—	—	—	—	FIL2_2D_NB_F1	—	—	—	—	—
FIL2_2D_WB_F2	—	—	—	—	—	FIL2_2D_NB_F2	—	—	—	—	—
FIL2_2D_WB_F3	—	—	—	—	—	FIL2_2D_NB_F3	—	—	—	—	—
FIL2_2D_WB_F4	—	—	—	—	—	FIL2_2D_NB_F4	—	—	—	—	—
FIL2_2D_WB_F5	—	—	—	—	—	FIL2_2D_NB_F5	—	—	—	—	—
FIL2_2D_WB_F6	—	—	—	—	—	FIL2_2D_NB_F6	—	—	—	—	—
FIL2_2D_WB_F7	—	—	—	—	—	FIL2_2D_NB_F7	—	—	—	—	—
FIL2_2D_WB_F8	—	—	—	—	—	FIL2_2D_NB_F8	—	—	—	—	—

Table 20B.41 Recommended Settings for Two-Dimensional Y/C Filters (SECAM)

	NTSC					NTSC			
		Cascade Filter					Cascade Filter		
Bit Name	Bypass Operation	1 Stage	2 Stages	TAKE-OFF Filter	Bit Name	Bypass Operation	1 Stage	2 Stages	TAKE-OFF Filter
FIL2_MODE_2D	0	1		2	FIL2_MODE_2D	0	1		2
FIL2_NARROW_2D	—	0	1	—	FIL2_NARROW_2D	—	0	1	—
FIL2_2D_WA_F0	—	-20	-20	0	FIL2_2D_NA_F0	—	—	-1008	—
FIL2_2D_WA_F1	—	24	24	-12	FIL2_2D_NA_F1	—	—	1976	—
FIL2_2D_WA_F2	—	64	64	-18	FIL2_2D_NA_F2	—	—	-2024	—
FIL2_2D_WA_F3	—	40	40	38	FIL2_2D_NA_F3	—	—	444	—
FIL2_2D_WA_F4	—	-76	-76	100	FIL2_2D_NA_F4	—	—	1868	—
FIL2_2D_WA_F5	—	-164	-164	88	FIL2_2D_NA_F5	—	—	-2864	—
FIL2_2D_WA_F6	—	-84	-84	-508	FIL2_2D_NA_F6	—	—	1352	—
FIL2_2D_WA_F7	—	108	108	-114	FIL2_2D_NA_F7	—	—	1376	—
FIL2_2D_WA_F8	—	216	216	852	FIL2_2D_NA_F8	—	—	-2240	—
FIL2_2D_WB_F0	—	-12	-12	—	FIL2_2D_NB_F0	—	—	-1080	—
FIL2_2D_WB_F1	—	40	40	—	FIL2_2D_NB_F1	—	—	2800	—
FIL2_2D_WB_F2	—	60	60	—	FIL2_2D_NB_F2	—	—	-3308	—
FIL2_2D_WB_F3	—	12	12	—	FIL2_2D_NB_F3	—	—	1628	—
FIL2_2D_WB_F4	—	-104	-104	—	FIL2_2D_NB_F4	—	—	1444	—
FIL2_2D_WB_F5	—	-156	-156	—	FIL2_2D_NB_F5	—	—	-3308	—
FIL2_2D_WB_F6	—	-64	-64	—	FIL2_2D_NB_F6	—	—	2140	—
FIL2_2D_WB_F7	—	120	120	—	FIL2_2D_NB_F7	—	—	376	—
FIL2_2D_WB_F8	—	208	208	—	FIL2_2D_NB_F8	—	—	-1384	—

(9) Over-Range Control Block

If overflow or underflow occurs at the top or bottom of the color amplitude of video signals, Y/C separation may not be correctly performed thus causing vertical lines to appear as dot crawl. To reduce this phenomenon, the over-range control block automatically inserts the low-pass filter for Y signals (cuts off the frequency components of the vertical lines) Setting RGORCR7.UCMP_SW to 1 enables over-range control, and setting RGORCR7.DCMP_SW to 1 enables under-range control. One of four over-range levels can be set with RGORCR1.RADJ_O_LEVEL0[9:0], RGORCR3.RADJ_O_LEVEL1[9:0], and RGORCR5.RADJ_O_LEVEL2[9:0]. Similarly, one of four under-range levels can be set with RGORCR2.RADJ_U_LEVEL0[9:0], RGORCR4.RADJ_U_LEVEL1[9:0], and RGORCR6.RADJ_U_LEVEL2[9:0]. The filter to be inserted is appropriately selected according to the over-range and under-range levels.

Setting HWIDE_SW to 1 enables detection of the maximum (minimum) level of five pixels in the horizontal direction in addition to the currently processed pixel to detect over-range or under-range occurrence.

20B.3.6 Chroma Decoding Circuit

The chroma decoding circuit demodulates the C signal extracted by the Y/C separator circuit into the Cb/Cr signal. This circuit has the automatic color control function (ACC), in which the amplitude of the color burst signal is detected to adjust the color gain automatically and also has the TINT/R-Y axis correction function, in which hue is adjusted at demodulation.

Figure 20B.36 shows the block diagram of the chroma decoding circuit.

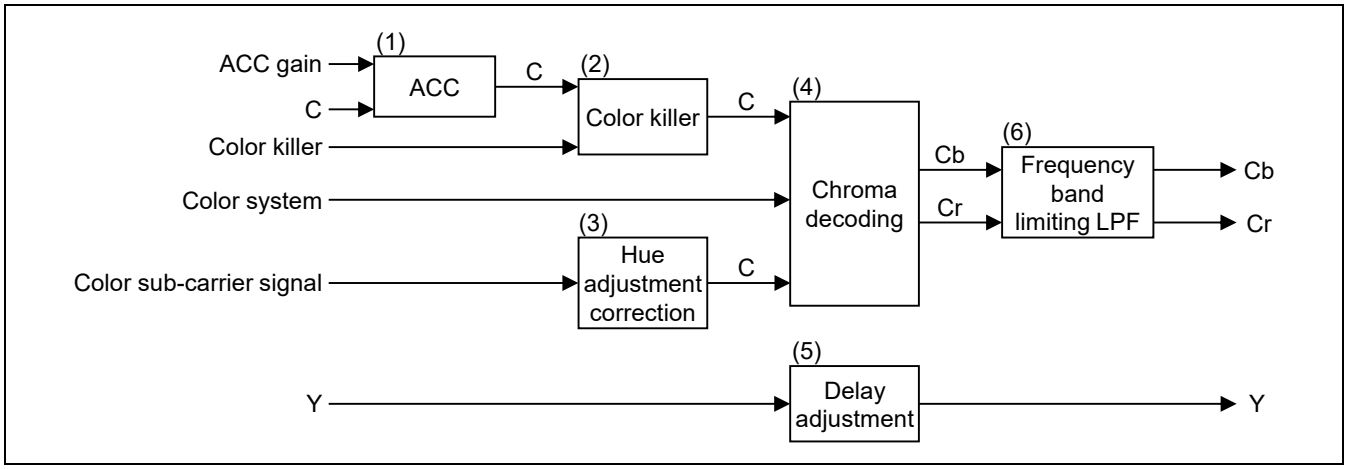


Figure 20B.36 Block Diagram of Chroma Decoding Circuit

(1) Automatic Color Control (ACC) Block

The ACC block detects the amplitude of the color burst signal and automatically controls the C signal gain so that the amplitude should be controlled to the target value. The ACC function is activated with ACCCR1.ACCMODE = 0. The target amplitude of the color burst signal can be set with ACCCR1.ACCLEVEL[8:0]. The gain is fixed when the amplitude falls within ACCCR1.ACCLEVEL[8:0] ± ACCCR3.ACCPRECIS[5:0]. The maximum ACC gain can be controlled with ACCCR1.ACCMAXGAIN[1:0]. The currently set gain value can be checked by reading CROMASR1.ACCMAINGAIN[8:0] (main) and CROMASR1.ACCSUBGAIN[1:0] (sub).

The C signal gain can also be set manually by setting ACCCR1.ACCMODE to 1. The specific gain value can be set with ACCCR2.CHROMAMAINGAIN[8:0] (main) and ACCCR2.CHROMASUBGAIN[1:0] (sub).

(2) Color Killer

The color killer deletes color information when the color bust signal amplitude is small in a weak electric field. The color killer is turned on or off based on the hysteresis; specifically, it is turned on when the amplitude reaches the value set with ACCCR3.KILLERLEVEL[5:0] and turned off when the amplitude reaches the value determined by ACCCR3.KILLERLEVEL[5:0] + ACCCR1.KILLEROFFSET[3:0].

The color killer can also be turned on forcibly by so setting ACCCR3.KILLERMODE.

(3) Hue Adjustment Correction Block

The hue adjustment correction block adjusts the color sub-carrier signal phase to adjust the Cb/Cr hue after chroma decoding. This function can be used only for the NTSC and PAL systems. The phase of the demodulation axis is controlled with TINTCR.TINTMAIN[9:0] and the phase of the R-Y axis is controlled with TINTCR.TINTSUB[5:0].

(4) Chroma Decoding Block

The chroma decoding block demodulates the Cb/Cr signal from the C signal. Line averaging can be carried out before demodulation according to YCDCR.DEMODMODE[1:0] setting. YCDCR.DEMODMODE[1:0] should usually be set to 2 (two-line demodulation for PAL only; one-line demodulation for NTSC).

(5) Delay Adjustment Block

The delay adjustment block delays the Y signal to adjust the Y/C signal delay. The Y signal can be delayed by -16 to 15 clock pulses with YCDCR.LUMADELAY[4:0].

(6) Frequency Band Limiting LPF

The frequency band limiting LPF limits the frequency band of the Cb/Cr signal after chroma decoding. This LPF is turned on or off according to YCDCR.CHROMALPF setting.

20B.3.7 Digital Clamp Circuit

The digital clamp circuit provides pedestal clamp for the Y signals and center clamp for the Cb/Cr signals at any position. This circuit also detects the amount of noise using the autocorrelation function.

Figure 20B.37 shows the block diagram of the digital clamp circuit.

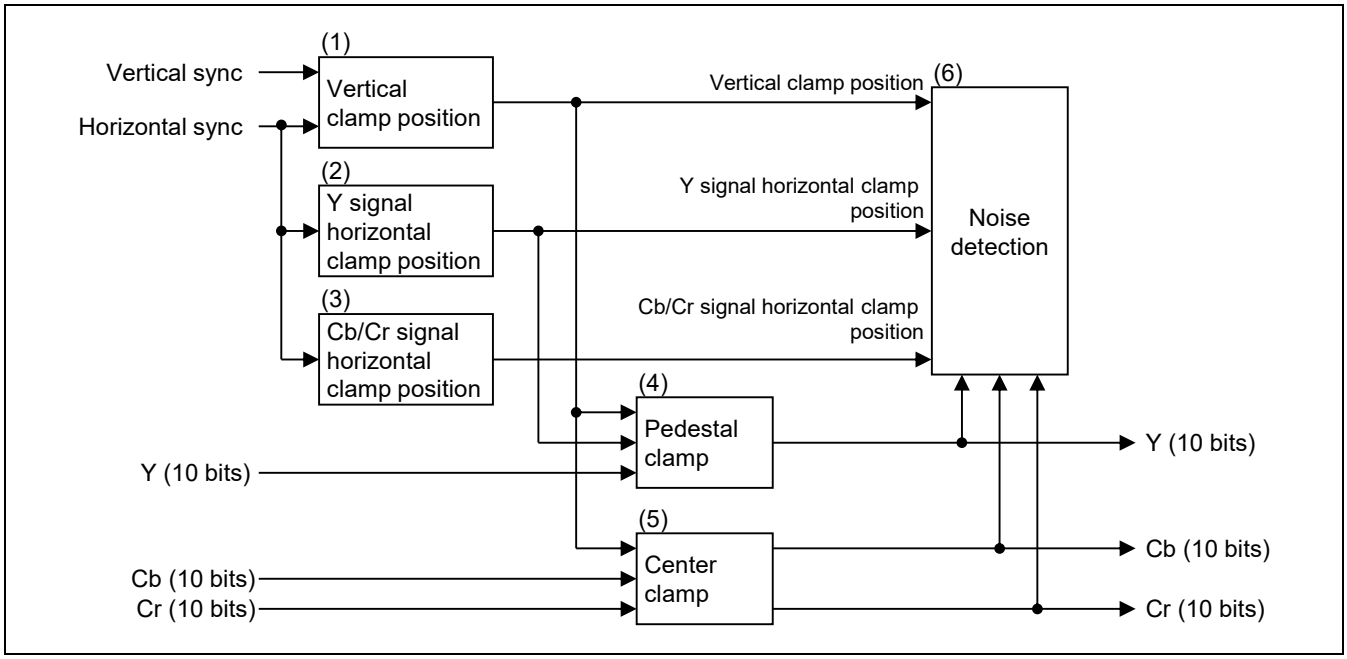


Figure 20B.37 Block Diagram of Digital Clamp Circuit

(1) Vertical Clamp Position Control Block

The vertical clamp position can be set with DCPCR4.DCPSTART[5:0] and DCPCR5.DCPEND[5:0]. The setting is used in common to Y, Cb, and Cr signals.

(2) Y Signal Horizontal Clamp Position Control Block

The horizontal clamp start position of the Y signal can be set with DCPCR7.DCPPOS_Y[7:0]. The horizontal clamp width can be set with DCPCR6.DCPWIDTH[6:0].

The horizontal clamp width setting is used in common to Y, Cb, and Cr signals.

(3) Cb/Cr Signal Horizontal Clamp Position Control Block

The horizontal clamp start position of the Cb/Cr signal can be set with DCPCR8.DCPPOS_C[7:0]. The horizontal clamp width can be set with DCPCR6.DCPWIDTH[6:0].

The horizontal clamp width setting is used in common to Y, Cb, and Cr signals.

(4) Pedestal Clamp Control Block

The pedestal clamp control block stabilizes the Y signal pedestal level.

When DCPCR1.DCPMODE_Y is 0, the value set with DCPCR1.BLANKLEVEL_Y[9:0] is subtracted from the Y signal, which is expressed as:

Y signal output = Y signal input – DCPCR1.BLANKLEVEL_Y[9:0]

When DCPCR1.DCPMODE_Y is 1, the Y signal level detected at the set clamp position and DCPCR1.BLANKLEVEL_Y[9:0] are added together and the resulting value is subtracted from the Y signal, which is expressed as:

Y signal output = Y signal input – (detected value + DCPCR1.BLANKLEVEL_Y[9:0])

The detected value can be read from DCPSR1.CLAMPLEVEL_Y[9:0].

The clamp response speed can be set with DCPCR3.DCPRESPONSE[2:0]. The setting is used in common to Y, Cb, and Cr signals.

(5) Center Clamp Control Block

The center clamp control block stabilizes the Cb/Cr signal center level.

When DCPCR2.DCPMODE_C is 0, the value set with DCPCR2.BLANKLEVEL_CB/DCPCR2.BLANKLEVEL_CR[5:0] is subtracted from the Cb/Cr signal, which is expressed as:

Cb signal output = Cb signal input – DCPCR2.BLANKLEVEL_CB[5:0]

Cr signal output = Cr signal input – DCPCR2.BLANKLEVEL_CR[5:0]

When DCPCR2.DCPMODE_C is 1, the Cb/Cr signal level detected at the set clamp position and DCPCR2.BLANKLEVEL_CB/DCPCR2.BLANKLEVEL_CR[5:0] are added together and the resulting value is subtracted from the Cb/Cr signal, which is expressed as:

Cb signal output = Cb signal input – (detected value + DCPCR2.BLANKLEVEL_CB[5:0])

Cr signal output = Cr signal input – (detected value + DCPCR2.BLANKLEVEL_CR[5:0])

The detected value can be read from DCPSR1.CLAMPLEVEL_CB[5:0] and DCPSR2.CLAMPLEVEL_CR[5:0].

The clamp response speed can be set with DCPCR3.DCPRESPONSE[2:0]. The setting is used in common to Y, Cb, and Cr signals.

(6) Noise Detection Block

Using the autocorrelation function, the noise amount at the set clamp position can be detected. With NSDCR.ACFINPUT[1:0], either Y, Cb, or Cr signal can be selected for which to calculate the autocorrelation function. The delay time for autocorrelation function calculation can be set with NSDCR.ACFLAGTIME[4:0] and accumulated field amount of autocorrelation function can be set with NSDCR.ACFFILTER[1:0]. The autocorrelation function (correlation coefficient) can be read from NSDSR.ACFSTRENGTH[15:0].

20B.3.8 Output Control Circuit

The output control circuit sets the signal capturing position and adjusts the contrast and color.

Figure 20B.38 shows the block diagram of the output control circuit.

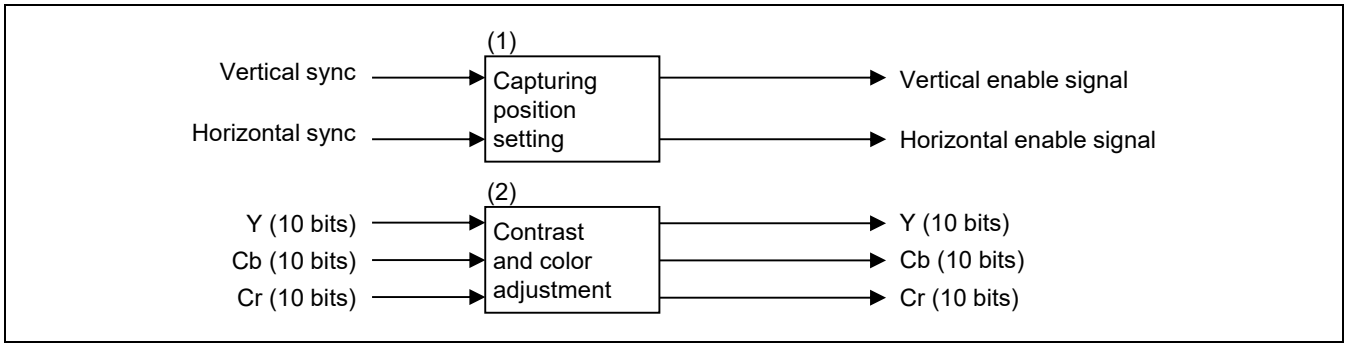


Figure 20B.38 Block Diagram of Output Control Circuit

(1) Capturing Position Setting Block

The capturing position setting block sets the position to capture the input video signals. The position can be set with TGCR1.SRCLEFT[8:0], TGCR2.SRCTOP[5:0], TGCR2.SRCHEIGHT[9:0], and TGCR3.SRCWIDTH[10:0]. These settings are applied only to this module. To set the display size of the input video signals, the vertical capture size register (SCL0_DS2) and horizontal capture size register (SCL0_DS3) of the scaler of video display controller 5 should be used.

(2) Contrast and Color Adjustment Block

The contrast and color adjustment block adjusts the gain of the output Y/Cb/Cr signals. The contrast (Y signal gain) can be adjusted with YGAINCR.Y_GAIN2[9:0] and the color (Cb/Cr signal gain) can be adjusted with CBGAINCR.CB_GAIN2[9:0] and CRGAINCR.CR_GAIN2[9:0].

20B.4 Usage Notes

20B.4.1 Recommended Setting

Table 20B.42 and Table 20B.43 show the recommended setting for this module.

Table 20B.42 Recommended Setting Common to Various Color Formats

Register	Bit	Initial Value (Decimal)	Recommended Value (Decimal)	Remarks
ADCCR1	AGCMODE	0	1	AGC on
SYNSCR1	LPFVSYNC	3	3	
	LPFHSYNC	3	5	
	VELOCITYSHIFT_H	0	2	
	SLICERMODE_H	2	2	Automatic slicing
	SLICERMODE_V	2	2	Automatic slicing
SYNSCR2	SYNCMAXDUTY_H	15	15	
	SYNCMINDUTY_H	10	10	
SYNSCR3	SSCLIPSEL	15	15	
	CSYNCSLICE_H	146	146	
SYNSCR4	SYNCMAXDUTY_V	15	15	
	SYNCMINDUTY_V	10	9	
SYNSCR5	VSYNCDELAY	0	0	
	VSYNCSLICE	11	10	
	CSYNCSLICE_V	146	146	
HAFCCR1	HAFCGAIN	6	12	
	HAFCFREERUN	0	0	
HAFCCR2	HAFCSTART	0	0	
	NOX2HOSC	0	1	
	DOX2HOSC	0	0	
HAFCCR3	HAFCEND	8	8	
	HAFCMODE	2	2	Comparison disabled during VBI period
VCDWCR1	VCDFREERUN	0	0	
DCPCR1	DCPMODE_Y	1	1	Automatic clamp setting
	DCPCHECK	0	0	
	BLANKLEVEL_Y	0	-40 (984)	
DCPCR2	DCPMODE_C	0	0	
	BLANKLEVEL_CB	0	0	
	BLANKLEVEL_CR	0	0	
DCPCR3	DCPRESPONSE	5	0	
DCPCR4	DCPSTART	16	16	
DCPCR5	DCPEND	16	16	
DCPCR6	DCPWIDTH	54	27	
DCPCR7	DCPPOS_Y	162	162	
DCPCR8	DCPPOS_C	27	54	

Register	Bit	Initial Value (Decimal)	Recommended Value (Decimal)	Remarks
NSDCR	ACFINPUT	0	0	
	ACFLAGTIME	0	0	
	ACFFILTER	0	3	
BTLCR	LOCKRANGE	1	1	
	LOOPGAIN	1	3	
	LOCKLIMIT	2	1	
	BCOFREERUN	0	0	
BTGPCR	BGPCHECK	0	0	
	BGPWIDTH	36	54	
	BGPSTART	130	110	
ACCCR1	KILLEROFFSET	8	5	
	ACCMODE	0	0	ACC on
	ACCMAXGAIN	0	0	
ACCCR2	CHROMASUBGAIN	0	0	
	CHROMAMAINGAIN	256	210	
ACCCR3	ACCRESPONSE	1	1	
	ACCPRECIS	20	8	
	KILLERMODE	0	0	
	KILLERLEVEL	9	4	
TINTCR	TINTSUB	0	0	
	TINTMAIN	0	0	
YCDCR	LUMADELAY	0	0	
	CHROMALPF	0	0	
	DEMODMODE	2	2	
AGCCR1	DOREDUCE	0	0	
	NOREDUCE	0	0	
	AGCRESPONSE	5	4	
AGCCR2	AGCPRECIS	10	10	
PKLIMITCR	PEAKLEVEL	0	2	Peak limiter on
	PEAKATTACK	2	2	
	PEAKRELEASE	0	3	
	PEAKRATIO	0	0	
	MAXPEAKSAMPLES	0	20	
RGORCR1	RADJ_O_LEVEL0	1023	928	
RGORCR2	RADJ_U_LEVEL0	0	32	
RGORCR3	RADJ_O_LEVEL1	1023	960	
RGORCR4	RADJ_U_LEVEL1	0	48	
RGORCR5	RADJ_O_LEVEL2	1023	992	
RGORCR6	RADJ_U_LEVEL2	0	64	

Register	Bit	Initial Value (Decimal)	Recommended Value (Decimal)	Remarks
RGORCR7	TEST_MONI	0	0	
	RADJ_MIX_K_FIX	0	0	
	UCMP_SW	0	1	Over-range detection enabled
	DCMP_SW	0	1	Under-range detection enabled
	HWIDE_SW	1	1	
AFCPFCR	PHDET_FIX	0	0	
	PHDET_DIV	5	5	
RUPDCR	NEWSETTING	0	1	
YCSCR8	HBPF_NARROW	1	0	
	HVBPF_NARROW	1	0	
	HBPF1_9TAP_ON	0	0	
	HVBPF1_9TAP_ON	0	0	
	HFIL_TAP_SEL	0	0	
YCSCR11	V_Y_LEVEL	3	0	
DCPCR9	CLP_HOLD_ON_Y	1	0	
	CLP_HOLD_ON_CB	1	0	
	CLP_HOLD_ON_CR	1	0	
YCTWA_F0 to YCTWA_F8	FIL2_2D_WA_F0 to FIL2_2D_WA_F8	Refer to 20B.3.5(8), Cascade Filter Block.		
YCTWB_F0 to YCTWB_F8	FIL2_2D_WB_F0 to FIL2_2D_WB_F8	Refer to 20B.3.5(8), Cascade Filter Block.		
YCTNA_F0 to YCTNA_F8	FIL2_2D_NA_F0 to FIL2_2D_NA_F8	Refer to 20B.3.5(8), Cascade Filter Block.		
YCTNB_F0 to YCTNB_F8	FIL2_2D_NB_F0 to FIL2_2D_NB_F8	Refer to 20B.3.5(8), Cascade Filter Block.		
YGAINCR	Y_GAIN2	512	816	
CBGAINCR	CB_GAIN2	512	663	
CRGAINCR	CR_GAIN2	512	663	
PGA_UPDATE	PGA_VEN	1	1	
PGACR	PGA_GAIN_SEL	0	0	
	PGA_GAIN	0	0	
ADCCR2	ADC_VINSEL	0	0	

Table 20B.43 Recommended Setting for Each Color Format

Register	Bit	NTSC-3.58	NTSC-4.43	PAL-4.43	PAL-M	PAL-N	SECAM	NTSC- 443 (60 Hz)	PAL-60
Capturing position setting									
TGCR1	SRCLEFT	256	256	256	256	256	256	256	256
TGCR2	SRCTOP	16	19	19	16	19	19	16	16
	SRCHEIGHT	241	288	288	241	288	288	241	241
TGCR3	SRCWIDTH	1428	1412	1412	1428	1412	1412	1428	1428
Horizontal AFC setting									
HAFCCR1	HAFCTYP	692	704	704	692	704	704	692	692
HAFCCR2	HAFCMAX	792	785	785	792	785	785	792	792
HAFCCR3	HAFCMIN	592	630	630	592	630	630	592	592
Vertical countdown setting									
VCDWCR1	NOVCD50	1	0	0	1	0	0	1	1
	NOVCD60	0	1	1	0	1	1	0	0
	VCDDEFAULT	2	1	1	2	1	1	2	2
	VCDWINDOW	30	30	30	30	30	30	30	30
	VCDOFFSET	15	15	15	15	15	15	15	15
BCO setting									
BTLCR	DEFAULTSYS	0	0	1	1	1	2	0	1
	NONTSC358	0	1	1	1	1	1	1	1
	NONTSC443	1	0	1	1	1	1	0	1
	NOPALM	1	1	1	0	1	1	1	1
	NOPALN	1	1	1	1	0	1	1	1
	NOPAL443	1	1	0	1	1	1	1	0
	NOSECAM	1	1	1	1	1	0	1	1
ACC level setting									
ACCCR1	ACCLEVEL	220	220	220	230	230	220	220	230
AGC level setting									
AGCCR1	AGCLEVEL	230	230	242	242	242	242	230	242
Y/C separation setting									
YCSCR3	K15	2	2	2	2	2	2	2	2
	K13	8	8	8	8	8	8	8	8
	K11	4	4	3	3	3	4	4	3
YCSCR4	K16	3	3	4	4	4	3	3	4
	K14	16	16	63	63	63	16	16	63
	K12	8	8	2	2	2	1	8	2
YCSCR5	K22A	32	32	32	32	32	32	32	32
	K21A	6	6	10	10	10	6	6	10
YCSCR6	K22B	8	8	15	15	15	15	8	15
	K21B	6	6	10	10	10	6	6	10
YCSCR7	K23B	6	6	3	3	3	3	6	3
	K23A	3	3	3	3	3	3	3	3
	K24	5	5	8	8	8	8	5	8

Register	Bit	NTSC-3.58	NTSC-4.43	PAL-4.43	PAL-M	PAL-N	SECAM	NTSC- 443 (60 Hz)	PAL-60
YCSCR9	DET2_ON	1	1	0	0	0	1	1	0
	HSEL_MIX_Y	6	6	0	0	0	6	6	0
	VSEL_MIX_Y	6	6	0	0	0	6	6	0
	HVSEL_MIX_Y	0	0	0	0	0	0	0	0
YCSCR12	DET2_MIX_C	0	0	0	0	0	0	0	0
	DET2_MIX_Y	2	2	0	0	0	0	2	0
	FIL2_MODE_2D	1	1	0	0	0	1	1	0
	FIL2_NARROW_2D	1	1	1	1	1	1	1	1

20B.4.2 Connection Example

Figure 20B.39 shows a pin connection example of this module.

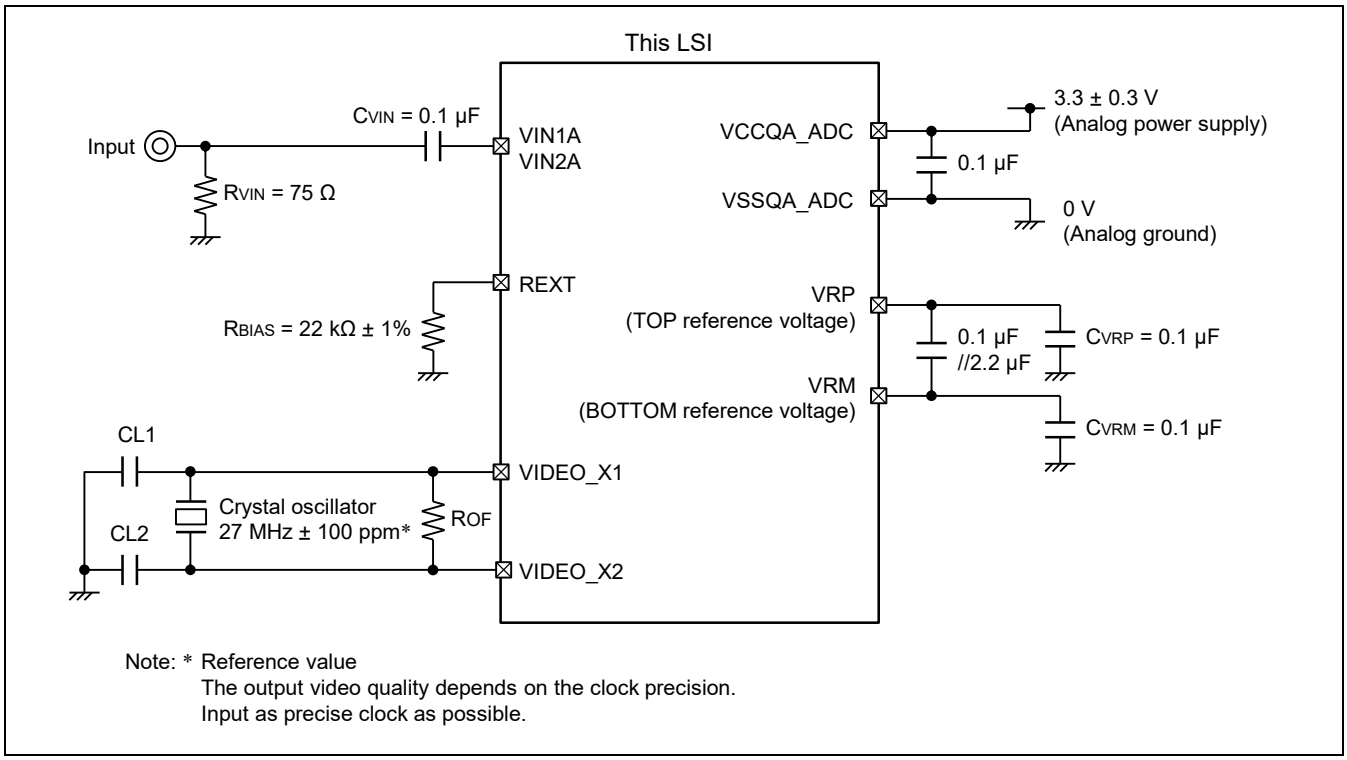


Figure 20B.39 Pin Connection Example

21. LVDS Interface

21.1 Overview

The LVDS (low voltage differential signaling) module converts an RGB signal output by the DU module to the LVDS format and outputs those signals.

The LVDS interface supports 8 output data formats with the conversion formats selected by register settings. The output control signals can also be selected freely.

It has a dedicated phase-locked loop (PLL) circuit, which can generate a clock with a desired frequency by dividing or multiplying the input clock frequency.

This PLL is called LVDS PLL in this section.

21.1.1 Features

- Five pairs of differential output conforming to the TIA/EIA-644 standard (four pairs for data and one pair for the clock)
- LVDS PLL for generating a clock with a desired frequency
- LVDS PLL power-down function
- Support eight output data formats
- Operating frequency: A maximum dot clock frequency of 13.40 to 87 MHz

21.1.2 Block Diagram

Figure 21.1 shows a block diagram of the LVDS output interface configuration.

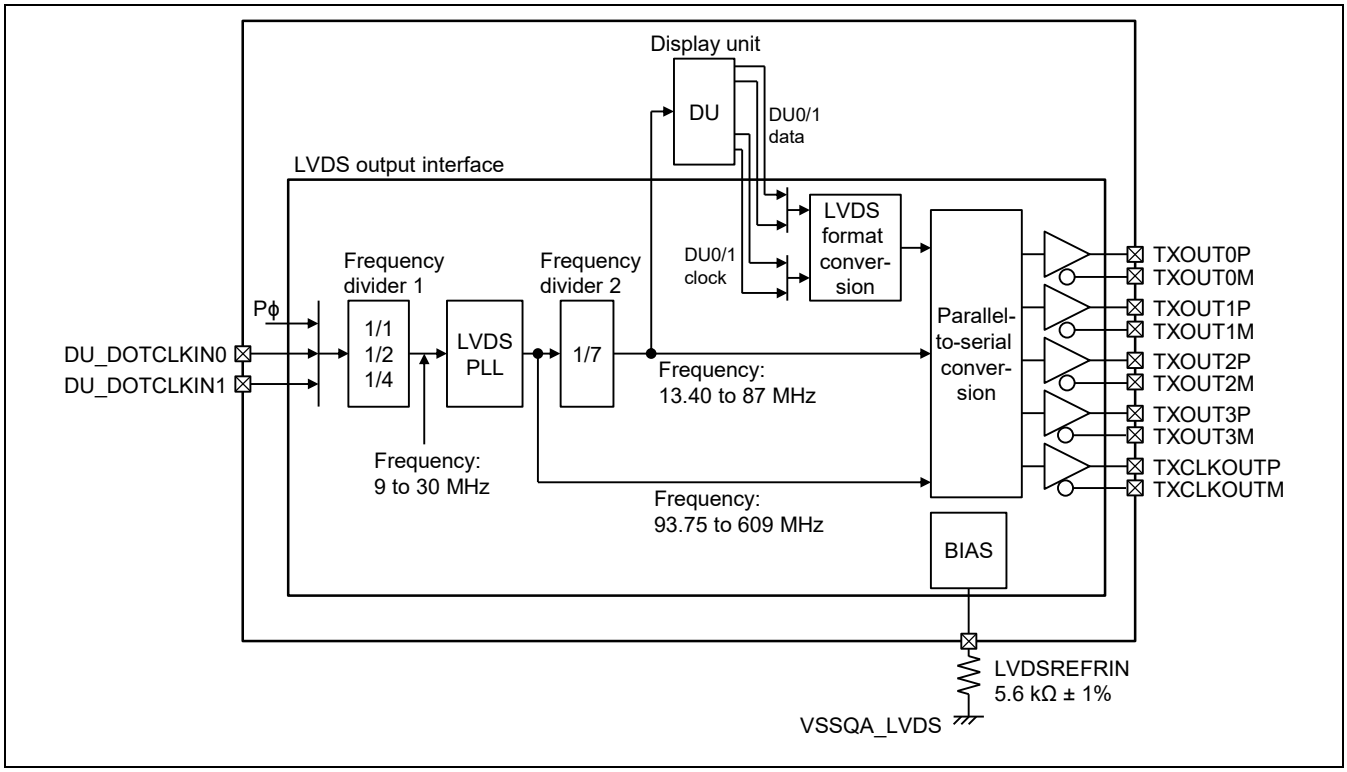


Figure 21.1 Block Diagram of LVDS Output Interface Configuration

21.1.3 Input/Output Pins

Table 21.1 shows the pin configuration.

Table 21.1 Pin Configuration

Name	Pin Name	I/O	Function
LVDS analog power supply pin	VCCQA_LVDS	Input	Power supply pin for LVDS output
LVDS analog ground pin*	VSSQA_LVDS	Input	Ground pin for LVDS output
LVDS PLL power supply pin	VDDA_LVDSPLL	Input	Power supply pin for LVDS PLL
LVDS resistor connection pin	LVDSREFRIN	Input	Reference resistor connection pin Connect to VSSQA_LVDS via a resistor with a value of 5.6 kΩ ± 1%.
LVDS data output pin 0P	TXOUT0P	Output	LVDS Ch0 data output pins (positive)
LVDS data output pin 0M	TXOUT0M	Output	LVDS Ch0 data output pins (negative)
LVDS data output pin 1P	TXOUT1P	Output	LVDS Ch1 data output pins (positive)
LVDS data output pin 1M	TXOUT1M	Output	LVDS Ch1 data output pins (negative)
LVDS data output pin 2P	TXOUT2P	Output	LVDS Ch2 data output pins (positive)
LVDS data output pin 2M	TXOUT2M	Output	LVDS Ch2 data output pins (negative)
LVDS data output pin 3P	TXOUT3P	Output	LVDS Ch3 data output pins (positive)
LVDS data output pin 3M	TXOUT3M	Output	LVDS Ch3 data output pins (negative)
LVDS clock output pin CP	TXCLKOUTP	Output	LVDS clock output pins (positive)
LVDS clock output pin CM	TXCLKOUTM	Output	LVDS clock output pins (negative)

21.1.4 Register Configuration

Table 21.2 shows the register configuration.

Base address: H'FEB9 0000

Table 21.2 Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
LVDS clock select register	LCLKSELR	R/W	H’FEB9 0000	H’00000000	32
LVDSPLL setting register	LPLLSETR	R/W	H’FEB9 0004	H’00000001	32
LVDS PLL Monitor Register	LPLLMONR	R	H’FEB9 0008	H’00000000	32
LVDS Interface Control Register 0	LVDCR0	R/W	H’FEB9 0010	H’00000000	32
CTR Control Register	LVDCTRCR	R/W	H’FEB9 0014	H’00000000	32
CH Control Register	LVDCHCR	R/W	H’FEB9 0018	H’00000000	32

21.2 Register Description

21.2.1 LVDS Clock Select Register (LCLKSELR)

LCLKSELR specifies the input clock, the frequency dividing values for frequency dividers 1, and controls power-down in the LVDS BIAS.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	LVDS_IN_CLK_SEL[2:0]			—	—	—	—	—	—	LVDS_NIDIV_SET[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	LVDS_CLK_EN	—	—	LVDS_BIAS_PDN	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26, 25	LVDS_IN_CLK_SEL [2:1]	00	R/W	These bits select the clock input to frequency divider 1. 00: Pϕ When you choose this clock(Pϕ), set “bit17,16 LVDS_NIDIV_SET[1:0] = 10(NIDIV = 4)” by all means. 01: DU_DOTCLKIN0 10: DU_DOTCLKIN1 11: Setting prohibited
24	LVDS_IN_CLK_SEL [0]	0	R/W	These bits select the clock input of DU data. 0: DU0 clock (“LVDCR0.DUSEL = 0” is necessary) Choose it at the time of DU0 use. Set the DU register as follows at the same time. DIDSR(H’FEB20028) = H’77900200 1: DU1 clock (“LVDCR0.DUSEL = 1” is necessary) Choose it at the time of DU1 use. Set the DU register as follows at the same time. DIDSR(H’FEB20028) = H’77900800
23 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	LVDS_NIDIV_SET [1:0]	00	R/W	These bits specify the frequency dividing value (NIDIV) for frequency divider 1. NIDIV = 1, 2, or 4 00: NIDIV = 1 01: NIDIV = 2 10: NIDIV = 4 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	LVDS_CLK_EN	0	R/W	Enables the LVDS PLL output. 0: Output from the PLL is disabled. 1: Output from the PLL is enabled. Note: Be sure to clear this bit to 0 before making settings in any other register described in this section. In addition, before modifying this bit, be sure to clear the enable bits in DU(display unit) to 0.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	LVDS_BIAS_PDN	0	R/W	Controls power-down for the LVDS BIAS. 0: Power-down state 1: Normal operation
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

21.2.2 LVDS PLL Setting Register (LPLLSETR)

LPLLSETR specifies the frequency dividing value and controls power-down in the LVDS PLL.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LVDSPLL_BP	—	—	—	—	LVDSPLL_FD[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LVDSPLL_RD[4:0]					—	—	LVDSPLL_OD[1:0]		—	—	—	LVDSPLL_PD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	LVDSPLL_BP	0	R	Makes the input signal bypass the LVDS PLL and outputs it without change. 0: Normal operation 1: Bypass output Note: When selecting the bypass output, set LVDSPLL_OD = 0.
30 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	LVDSPLL_FD[10:0]	All 0	R/W	These bits specify the frequency dividing value (NFD) for the feedback frequency in the LVDS PLL. 24 to 2047: NFD = LVDSPLL_FD value 0 to 23: Setting prohibited Note: The following values are also prohibited: 28 to 31, 37 to 39, 46, 47, and 55
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	LVDSPLL_RD[4:0]	All 0	R/W	These bits specify the frequency dividing value (NRD) for the input frequency in the LVDS PLL. NRD = LVDSPLL_RD value + 1
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	LVDSPLL_OD[1:0]	All 0	R/W	These bits specify the frequency dividing value (NOD) for the output frequency in the LVDS PLL. NOD = 2 ^ LVDSPLL_OD value
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	LVDSPLL_PD	1	R/W	Controls power-down for the LVDS PLL. 0: Normal operation 1: Power-down state

21.2.3 LVDS PLL Monitor Register (LPLLMONR)

LPLLMONR monitors the status of the LVDS PLL.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LVDSPLL_LD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	LVDSPLL_LD	0	R	Detects the locked state of the LVDS PLL. 0: Unlocked 1: Locked

21.2.4 LVDS Interface Control Register 0 (LVDCR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DUSEL	—	—	—	LVMD[3:0]				—	—	—	—	—	—	—	LVRES
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	DUSEL	0	R/W	DU Channel Select Selects the DU channel for LVDS input. 0: DU0 is selected (“LCLKSELR.LVDS_IN_CLK_SEL[0] = 0” is necessary) 1: DU1 is selected (“LCLKSELR.LVDS_IN_CLK_SEL[0] = 1” is necessary)
14 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	LVMD[3:0]	0000	R/W	LVDS Interface Mode Selects the LVDS Interface module output data format (see Figure 21.4). 0000: MODE0 0001: MODE1 0010: MODE2 0011: MODE3 0100: MODE4 0101: MODE5 0110: MODE6 0111: MODE7 All other values: Setting prohibited
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	LVRES	0	R/W	LVDS Interface Reset Bit Controls the LVDS output. 0: Output off 1: Output on

21.2.5 CTR Control Register (LVDCTRCR)

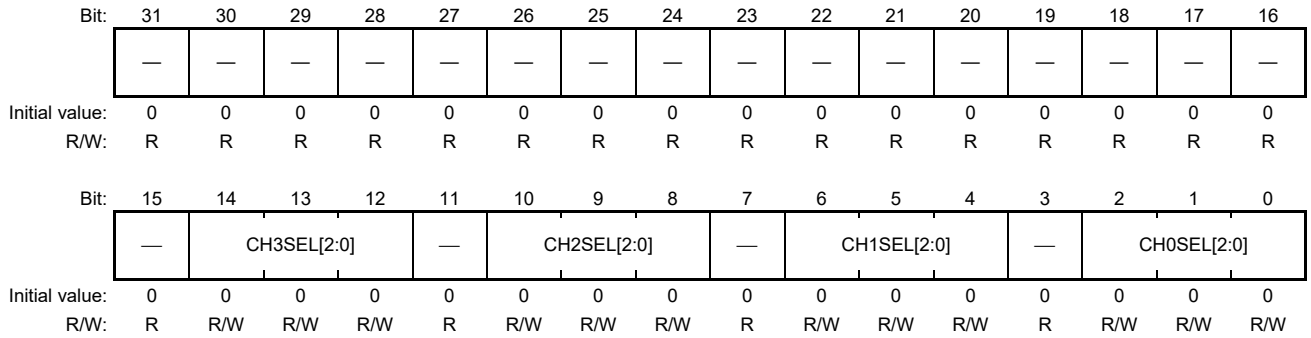
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	CTR3SEL[2:0]			—	CTR2SEL[2:0]			—	CTR1SEL[2:0]			—	CTR0SEL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	CTR3SEL [2:0]	000	R/W	Ctrl3 Select Selects data to be output to Ctrl3 (see section 21.3.3 Ctrl Signal Selection). 000: 0 001: Odd/even 010: CDE Other settings are prohibited.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	CTR2SEL [2:0]	000	R/W	Ctrl2 Select Selects data to be output to Ctrl2 (see section 21.3.3 Ctrl Signal Selection). 000: DISP 001: Odd/even 010: CDE 011: HSYNC 100: VSYNC Other settings are prohibited.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	CTR1SEL [2:0]	000	R/W	Ctrl1 Select Selects data to be output to Ctrl1 (see section 21.3.3 Ctrl Signal Selection). 000: VSYNC 001: DISP 010: Odd/even 011: CDE 100: HSYNC Other settings are prohibited.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CTR0SEL [2:0]	000	R/W	Ctrl0 Select Selects data to be output to Ctrl0 (see section 21.3.3 Ctrl Signal Selection). 000: HSYNC 001: VSYNC 020: DISP 010: Odd/even 100: CDE Other settings are prohibited.

21.2.6 CH Control Register (LVDCHCR)



Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14 to 12	CH3SEL	000	R/W	CH3 Select Selects data to be output to LVDS0_CH3_P/N (see section 21.3.4 CH Selection). 000: CH3 001: CH0 010: CH1 011: CH2 Other settings are prohibited.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	CH2SEL	000	R/W	CH2 Select Selects data to be output to LVDS0_CH2_P/N (see section 21.3.4 CH Selection). 000: CH2 001: CH3 010: CH0 011: CH1 Other settings are prohibited.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	CH1SEL	000	R/W	CH1 Select Selects data to be output to LVDS0_CH1_P/N (see section 21.3.4 CH Selection). 000: CH1 001: CH2 010: CH3 011: CH0 Other settings are prohibited.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CH0SEL	000	R/W	CH0 Select Selects data to be output to LVDS0_CH0_P/N (see section 21.3.4 CH Selection). 000: CH0 001: CH1 010: CH2 011: CH3 Other settings are prohibited.

21.3 Operation

This module receives the RGB888 signals output from display unit(DU) and the SYNC signal, converts the video signals to the LVDS format, and outputs them. The operating clock is generated in the LVDS PLL.

21.3.1 LVDS PLL Settings

The input clock select circuit, frequency dividers 1, 2, and LVDS PLL circuit are used to generate operating clocks. For input and output of each circuit, allowable frequency ranges are determined; be sure to make appropriate settings to generate input and output frequencies within the ranges.

Before modifying various setting registers, check that clock operation in display unit(DU) is disabled and the LVDS PLL output is disabled (LPLLSETR.LVDS_CLK_EN = 0).

Figure 21.2 shows a block diagram of the LVDS PLL and its peripheral circuits.

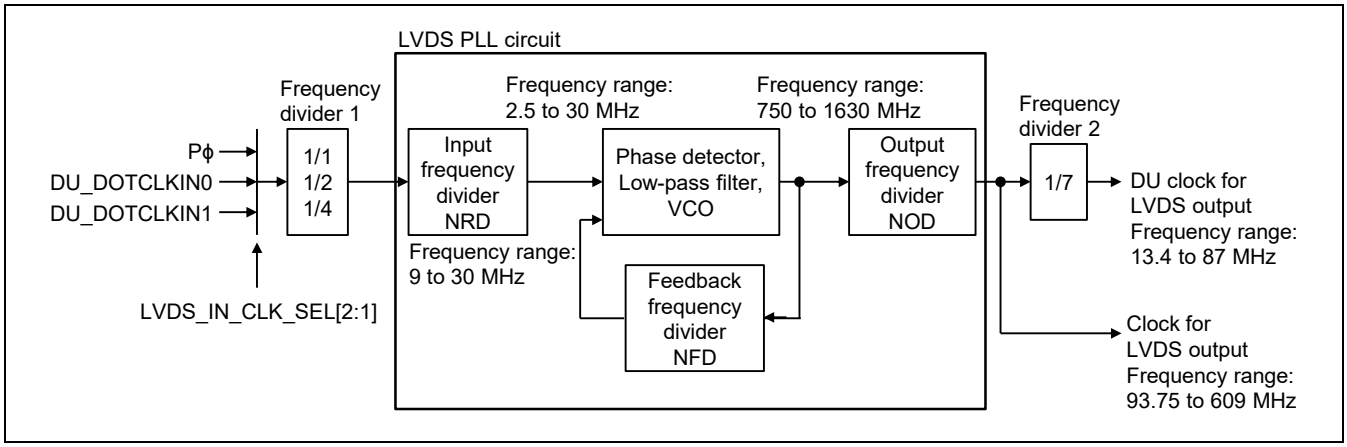


Figure 21.2 Block Diagram of LVDS PLL and Peripheral Circuits

(1) Clock Input to LVDS PLL

The clock input to the LVDS PLL can be selected from among Pϕ, DU_DOTCLKIN0, and DU_DOTCLKIN1 clocks through the LVDS_IN_CLK_SEL[2:1] bit setting in LVDS_CLKSELR.

The frequency of this input clock should be within the range from 9 to 30 MHz. When the input clock frequency is higher than the upper limit of this range, use frequency divider 1 placed before the LVDS PLL and reduce the frequency so that it is within the allowed range.

(2) LVDS PLL Frequency Setting

The LVDS PLL has three internal frequency dividers: input frequency divider NRD, feedback frequency divider NFD, and output frequency divider NOD.

The frequency of the clock output from the LVDS PLL is calculated by the following equations. Note that the reference frequency, VCO output frequency, LVDS PLL input frequency, and LVDS PLL output frequency should be within the respective ranges shown below the equations.

FVCO = FIN × NFD / NRD (VCO output frequency)
FOUT = FIN × NFD / (NRD × NOD) (LVDS PLL output frequency)

Note: FVCO: VCO output frequency. Frequency range = 750 MHz to 1630 MHz
FIN: LVDS PLL input frequency. Frequency range = 9 MHz to 30 MHz
FOUT: LVDS PLL output frequency. Frequency range = 609 MHz max.

(3) LVDS PLL Frequency Setting Timing

Before making settings for each frequency divider in the PLL circuit described in (2), place the PLL in the power-down state (PD = 1) and wait for at least 0.5 µs. After making frequency divider settings, wait for a retention period of at least 0.5 µs and release the power-down state (PD = 0). Figure 21.3 shows this timing.

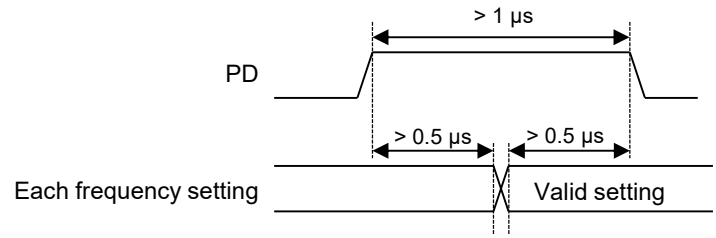


Figure 21.3 PLL Setting Timing

(4) LVDS PLL Output Enable Timing

Output of the clock from the LVDS PLL can be enabled or disabled through the LVDS_CLK_EN bit setting in LCLKSELR.

To allow time for stabilization of oscillation by the PLL, wait for at least 200 us after release from the power-down state before enabling the LVDS PLL output. The LVDS_CLK_EN bit in LCLKSELR should be modified only while the clock operation in display unit(DU) is disabled.

(5) LVDS PLL Output Clock Frequency Setting

When using the clock output from the LVDS PLL as the clock for the LVDS output interface, select the clock from frequency divider 2 (divided by 7) as the clock for display unit(DU).

21.3.2 Mode Selection

The mode is selected by the LVMD bits in the LVDS Interface control register 0. Figure 21.4 shows the modes that can be set.

Here, R0 to R7, G0 to G7, and B0 to B7 are the RGB signals and Ctrl0 to Ctrl3 are control signals (such as HSYNC and VSYNC). The Ctrl signals can be set by the CTR control register.

CH0, CH1, CH2 and CH3 are buffers that hold data temporarily. The default is for the CH0, CH1, CH2 and CH3 data to be output directly without change to TXOUT0P/M, TXOUT1P/M, TXOUT2P/M and TXOUT3P/M. The CH assignment can be switched with the CH control register settings.

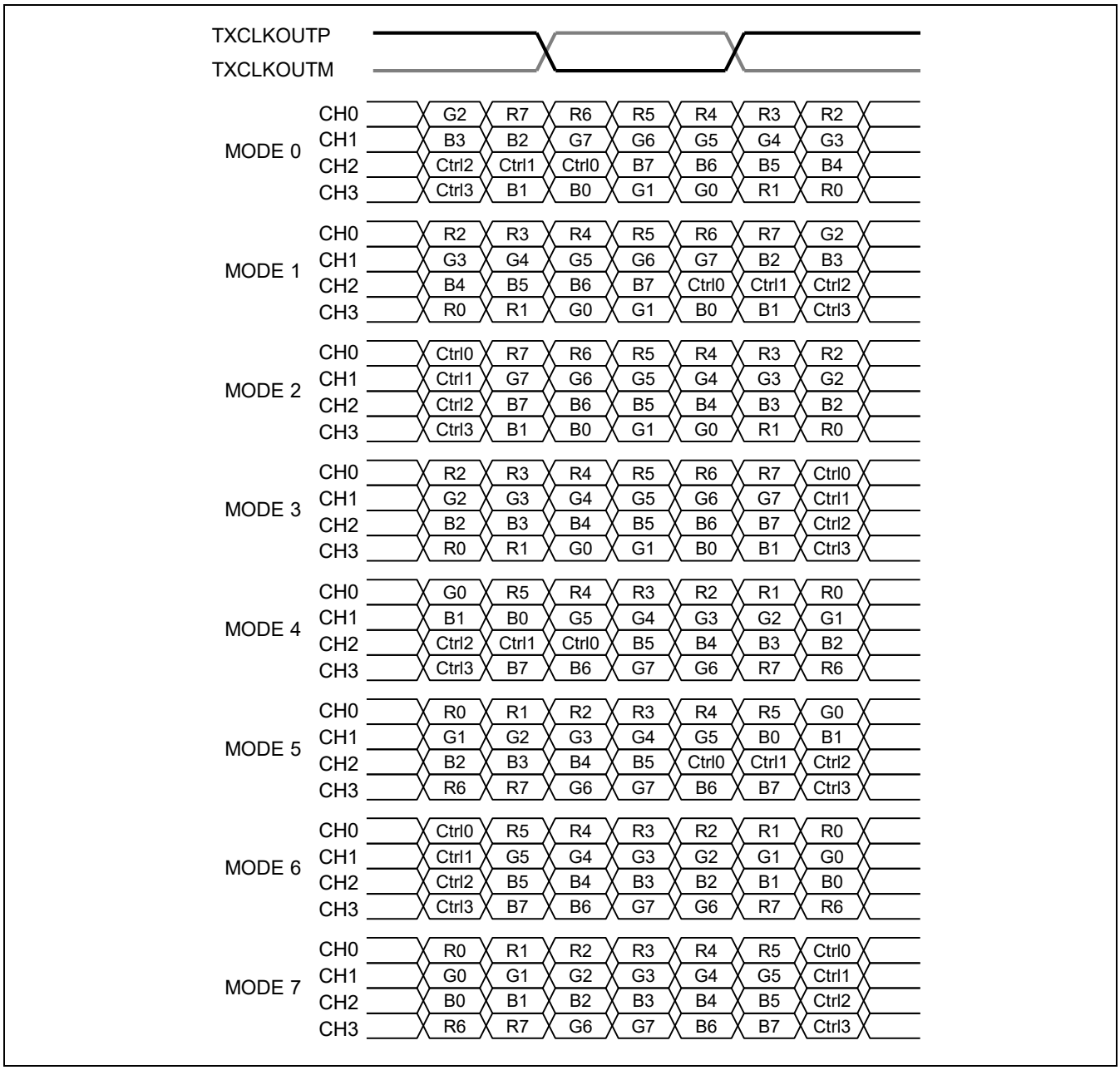


Figure 21.4 Output Data Format

21.3.3 Ctrl Signal Selection

The two stage settings shown below are required to select the Ctrl signals.

(1) DU Output Signal Selection

The DU output ports are multiplexed. The signals that you want to output are set up with the corresponding register. The specified signals are input to the LVDS Interface module ports.

(2) LVDS Port Selection

The LVDS ports used to output to the Ctrl signals are selected with the CTR control register (LVDCTRCR). This results in the signals input to the LVDS ports being output as Ctrl signals.

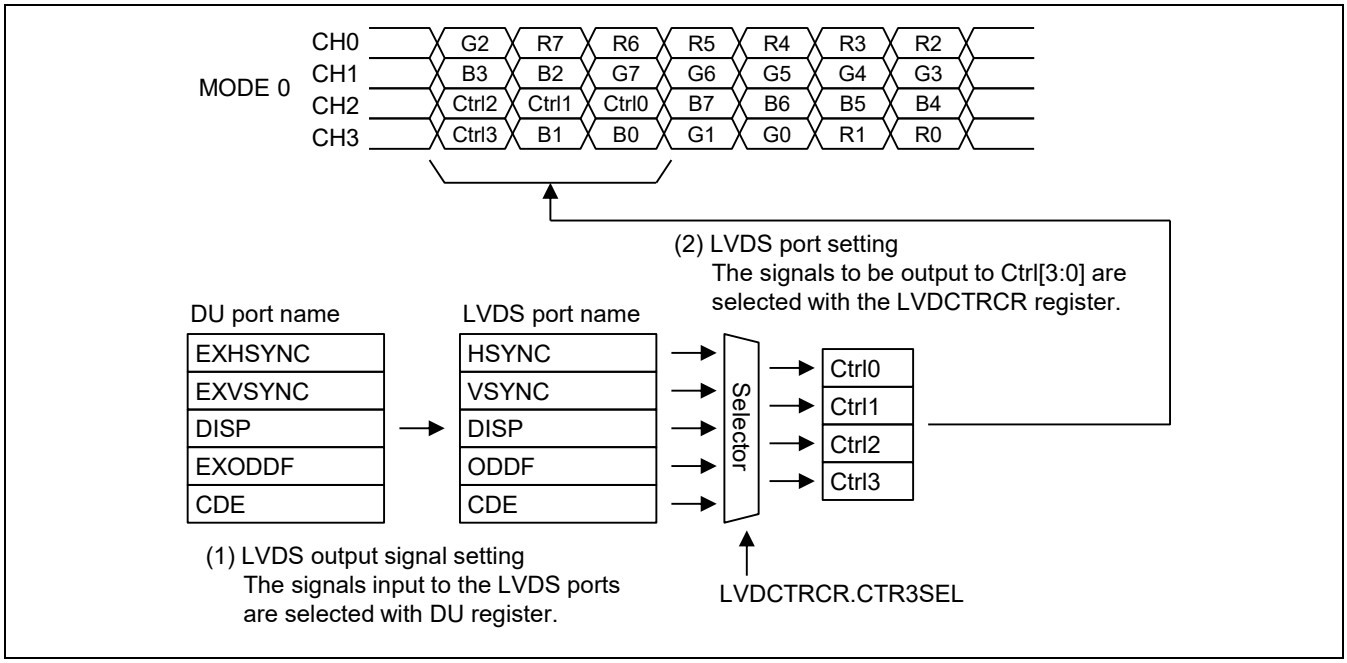


Figure 21.5 Ctrl Signal Selection

Set the desired Ctrl signal characteristics with the DU registers.

For example, to reverse the polarity of the HSYNC signal, the polarity must be set with DU register settings. (The LVDS Interface module only converts the signals output from DU to the LVDS format.)

An example of Ctrl signal settings is shown below.

(1) Ctrl0 = HSYNC, Ctrl1 = VSYNC, and Ctrl2 = DISP

Set the DU registers so that HSYNC, VSYNC, and DISP are output.

Then set the CTR control register (LVDCTRCR) so that CTR0SEL = B'000, CTR1SEL = B'000, and CTR2SEL = B'000.

(2) Ctrl0 = CSYNC, Ctrl1 = ODDF, and Ctrl2 = CDE

Set the DU registers so that CSYNC, ODDF, and CDE are output.

Then set the LVDS Interface register (LVDCTRCR) so that CTR0SEL = B'000, CTR1SEL = B'010, and CTR2SEL = B'010.

(Note that since CSYNC can also be output from other ports, CTR0SEL must be set to match the port from which DU outputs CSYNC.)

21.3.4 CH Selection

The LVDS Interface module stores the RGB signal data in CH0, CH1, CH2, and CH3 according to the mode selection and Ctrl signal selection registers.

21.3.5 Dot clock Settings

The LVDS Interface module dot clock frequency is determined by LVDS PLL setting. This section describes how this frequency is set.

The individual settings are made with the DU (Display Unit) and LVDS registers. Refer to the corresponding sections for details on the registers, notes, and other information on these settings.

(1) Clock source selection

The clock source can be selected to be either the internal clock or an external input (LCLKSELR).

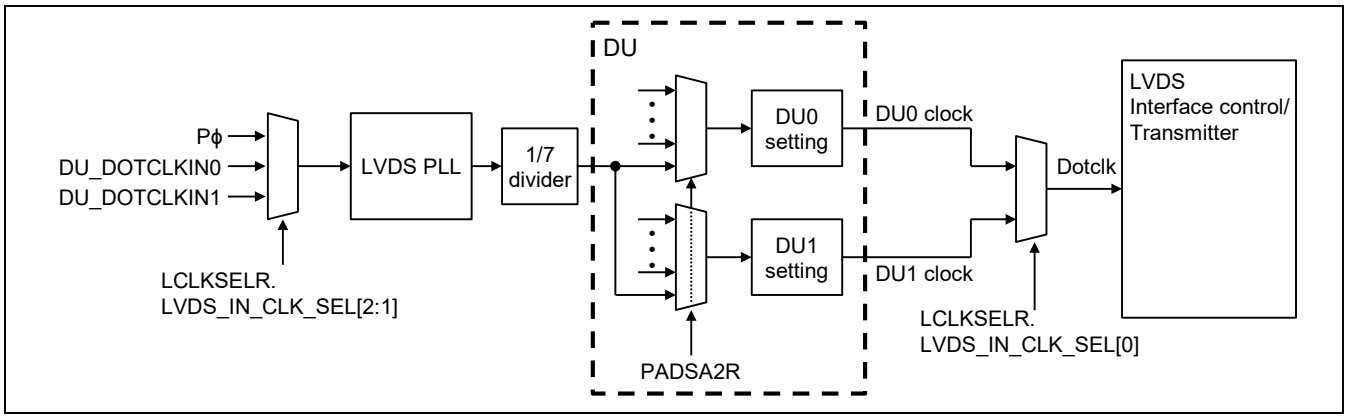
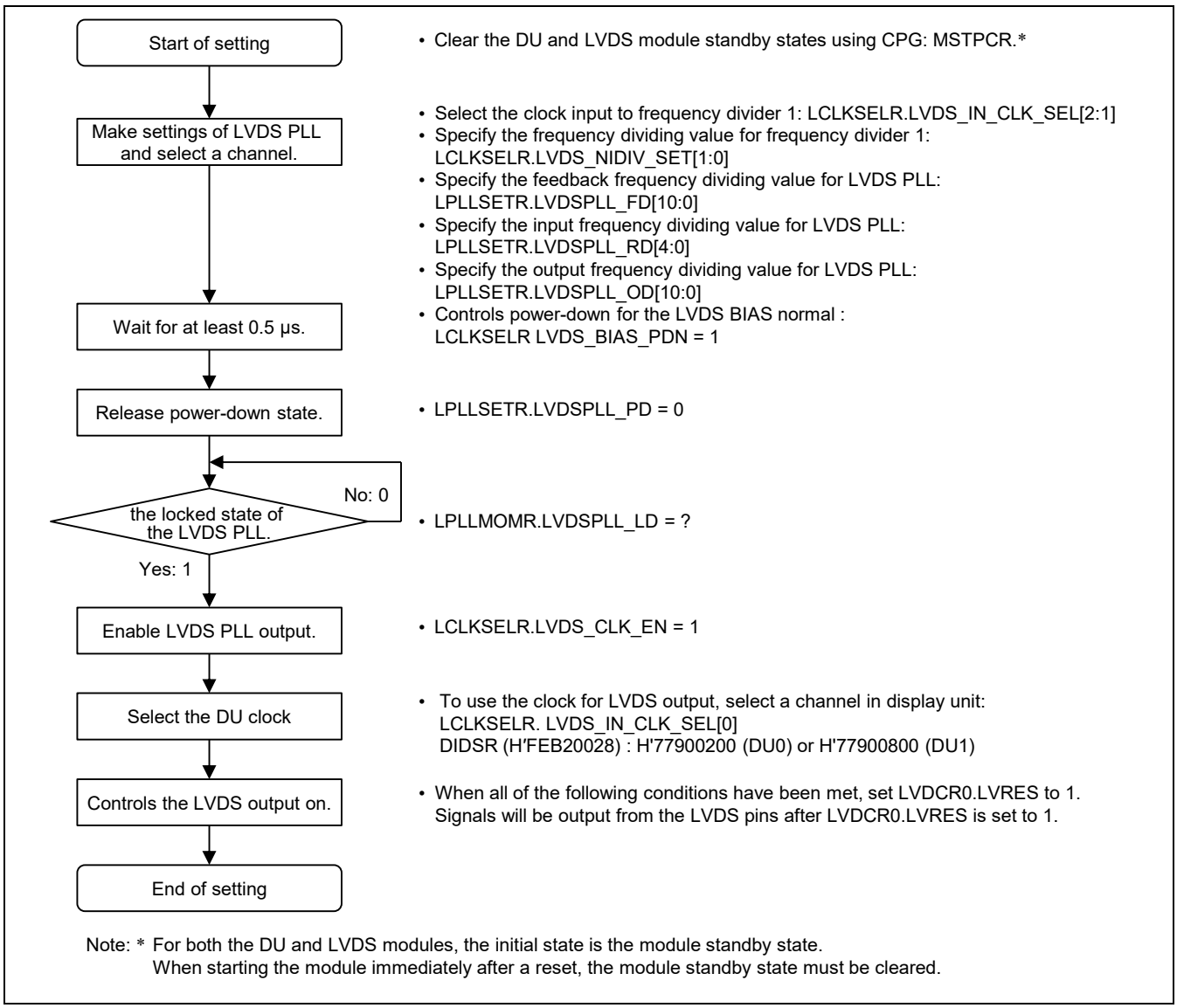


Figure 21.6 Dotclk Settings

21.3.6 Procedures for Register Settings

(1) Initial Settings after Power-on Reset

The following shows an example of initial settings after a power-on reset.



Note: * For both the DU and LVDS modules, the initial state is the module standby state.
When starting the module immediately after a reset, the module standby state must be cleared.

Figure 21.7 Example of Initial Settings after Power-On Reset

(2) Frequency Modification Settings

The following shows an example of modifying frequencies.

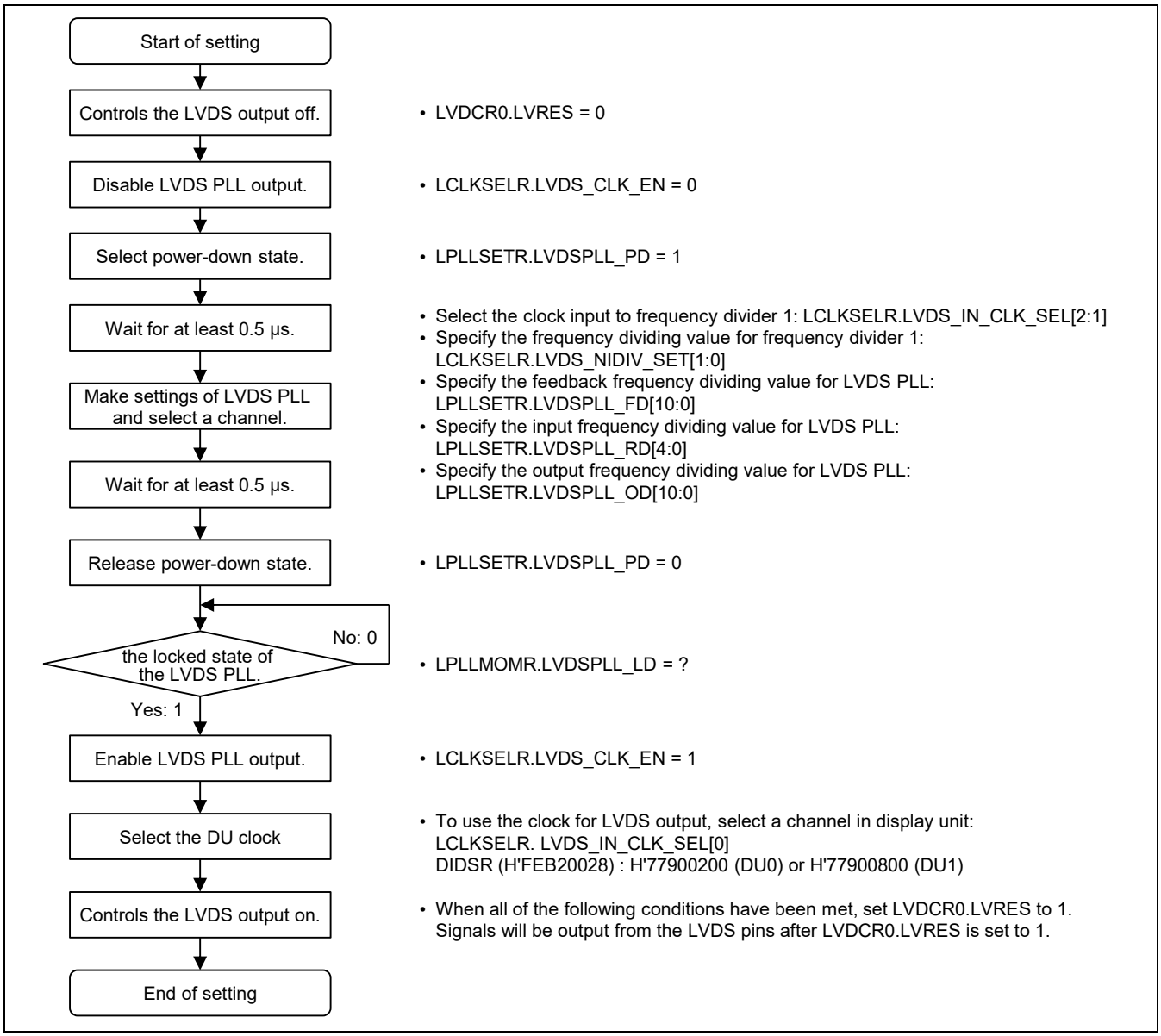


Figure 21.8 Example of Modifying Frequencies for LVDS Output

21.4 Usage Notes

The following notes must be observed when using the LVDS Interface module.

Incorrect operation and damage to the device itself may occur if these notes are not followed.

- Since the LVDS interface module includes logic that operates from the dot clock (Dotclk) signal output by the DU module, incorrect operation may occur if the DU registers are not set appropriately. Also, do not change any DU register values during LVDS interface operation. (If Dotclk output is not stable, thus operation cannot be guaranteed.) There are two DU registers related to Dotclk: Display unit SYStem control Register n (DSYSRn, n = 0, 1) and External Synchronization Control Register n (ESCRn, n = 0, 1). These registers must not be changed during LVDS operation.
- Set the Dotclk signal input to the LVDS interface module to a frequency within the LVDS interface module's guaranteed operating range (13.4 to 87 MHz).
- Set the clock signal input to the LVDS PLL module to a frequency within the LVDS PLL module's guaranteed operating range (9 to 30 MHz).
- Application systems should be implemented in a failsafe manner, such as by connecting the LVDS outputs to a failsafe receiver or by connecting terminators, so that no problems in or damage to the application can occur if the LVDS pins become unstable (for example, going to the high-impedance state or the differential outputs going to the same level).

22. Video Input Module (VIN)

22.1 Overview

The video input module (hereinafter abbreviated as VIN) is a video capture module that stores in external memory YCbCr-422 data through the ITU-R BT.601, ITU-R BT.656, or ITU-R BT.709 interface and RGB data through the ITU-R BT.601 or ITU-R BT.709 interface.

The module has up to six video channels that can independently control the capture of data into a capture area of up to 2048 × 2048 pixels. It can also provide vertical and horizontal scaling of the data by up to three and two times, respectively.

For captured video data, the VIN provides a color space conversion function from YCbCr-422 to RGB, a format conversion function from RGB to ARGB.

As the VIN internally generates a field signal, it can capture progressive data.

Notes: 1. The maximum frequency of the video clock is 100 MHz when bit 31 (FAST) in the main control register is set to support the 100 MHz clock input, except during vertical or horizontal scaling up.
2. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.
3. The number of video input channels for each product is as follows:
2 channels

22.1.1 Features

(1) Video Channel 0

The following input interfaces can be selected for these channels.

Table 22.1 Input Interface for Video Channel 0

Interface	Data Width	Data Type
ITU-R BT.601/BT.709*1, *3	8/10/12 bits	YCbCr-422 data (UYVY format)
ITU-R BT.601/BT.709*3/BT.1358*2	16/20/24 bits	YCbCr-422 data (8/10/12 bits (Y) + 8/10/12 bits (CbCr) format)
ITU-R BT.656*1	8/10/12 bits	YCbCr-422 data (UYVY format)
ITU-R BT.601/BT.709*3	18 bits	RGB-666 data
ITU-R BT.601/BT.709*3	24 bits	RGB-888 data

Notes: 1. Disable the XY scaling settings when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.656 interface (only the 100% scaling is enabled).
2. Disable the XY scaling settings when using the 20/24-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.1358 interface (only the 100% scaling is enabled).
3. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.

(2) Video Channel 1

The following input interfaces can be selected for this channel.

Table 22.2 Input Interface for Video Channel 1

Interface	Data Width	Data Type
ITU-R BT.601*1/BT.709*2	8/10/12 bits	YCbCr-422 data (UYVY format)
ITU-R BT.656*1	8/10/12 bits	YCbCr-422 data (UYVY format)

Notes: 1. Disable the XY scaling settings when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT.656 interface. (Only the 100% scaling is enabled.)
2. When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.

(3) Internal Sync Signal Generation

For video data capturing through the ITU-R BT.601 or ITU-R BT.709 interface, the field signal can be internally generated even if the input sync signals stop (In video data capture through the ITU-R BT.656 interface, only the field signal is generated).

(4) Capture Mode

The following four modes can be selected to capture the interlace images. In addition, single frame capture or continuous frame capture mode can be selected.

Triple-buffering control is provided in accordance with the captured field image and frame image to coordinate with the video capture mode of the display module.

The channel that the cooperation control with the display module is possible becomes 2 channels from VIN0 to VIN1 (for details of the cooperation control with the display module, see section 20, Display Unit (DU)).

- Odd-field capture mode
- Even-/odd-field capture mode
- Even-field capture mode
- Full interlace capture mode

(5) Vertical and Horizontal Scaling

The image can be scaled up and down up to three times in the vertical and two times in the horizontal directions.

(6) Size Clipping

The VIN has two clipping circuits, which independently handle images with up to 2048 × 2048 pixels. Any capture size within this limit can be specified before or after scaling.

(7) Color Space Conversion

Color space conversion can be performed from YC to RGB or from RGB to YC. Desired conversion coefficients can be specified through registers to adjust colors.

(8) Lookup Table (LUT) Density Conversion

The lookup table (LUT) density can be converted from 10 bits to 8 bits for each pixel according to the color space conversion result.

Note: When the density conversion function is not used, the upper 8 bits of data are output.

(9) Image Data Format Conversion

To the density-converted YCbCr444 or RGB888 image data, the following data format conversions are available:

- YCbCr image data
  - Y/Cb/Cr 8-bit multiplex conversion
  - YCbCr444 → YC separation (separated into Y and CbCr components.)
  - YCbCr444 → Y component extraction
- RGB image data
  - RGB-888 → 32 bits/pixel conversion
  - RGB-888 → RGB-565 (16 bits/pixel) conversion
  - RGB-888 → ARGB-1555 (16 bits/pixel) conversion
  - RGB-888 → ARGB-888 (32 bits/pixel) conversion

Note: The lookup table is common to the YCbCr and RGB formats.

(10) Memory Output Data Format

Format-converted image data can be transferred to the memory. The following shows the available formats of the data stored.

- YCbCr image data
  - Y/Cb/Cr, 8-bit multiplexed
  - YC separation, YCbCr422, Y, 8-bit Cb/Cr, 8-bit multiplexed
  - YC separation, YCbCr422, Y, 10-bit Cb/Cr, 8-bit multiplexed
  - YC separation, YCbCr422, Y, 12-bit Cb/Cr, 8-bit multiplexed
  - YC separation, Y data, 8-bit
  - YC separation, Y data, 10-bit
  - YC separation, Y data, 12-bit
- RGB image data
  - RGB-565 (16 bits/pixel)
  - ARGB-1555 (16 bits/pixel)
  - RGB-888 (32 bits/pixel)
  - ARGB-8888 (32 bits/pixel)

22.1.2 Block Diagram

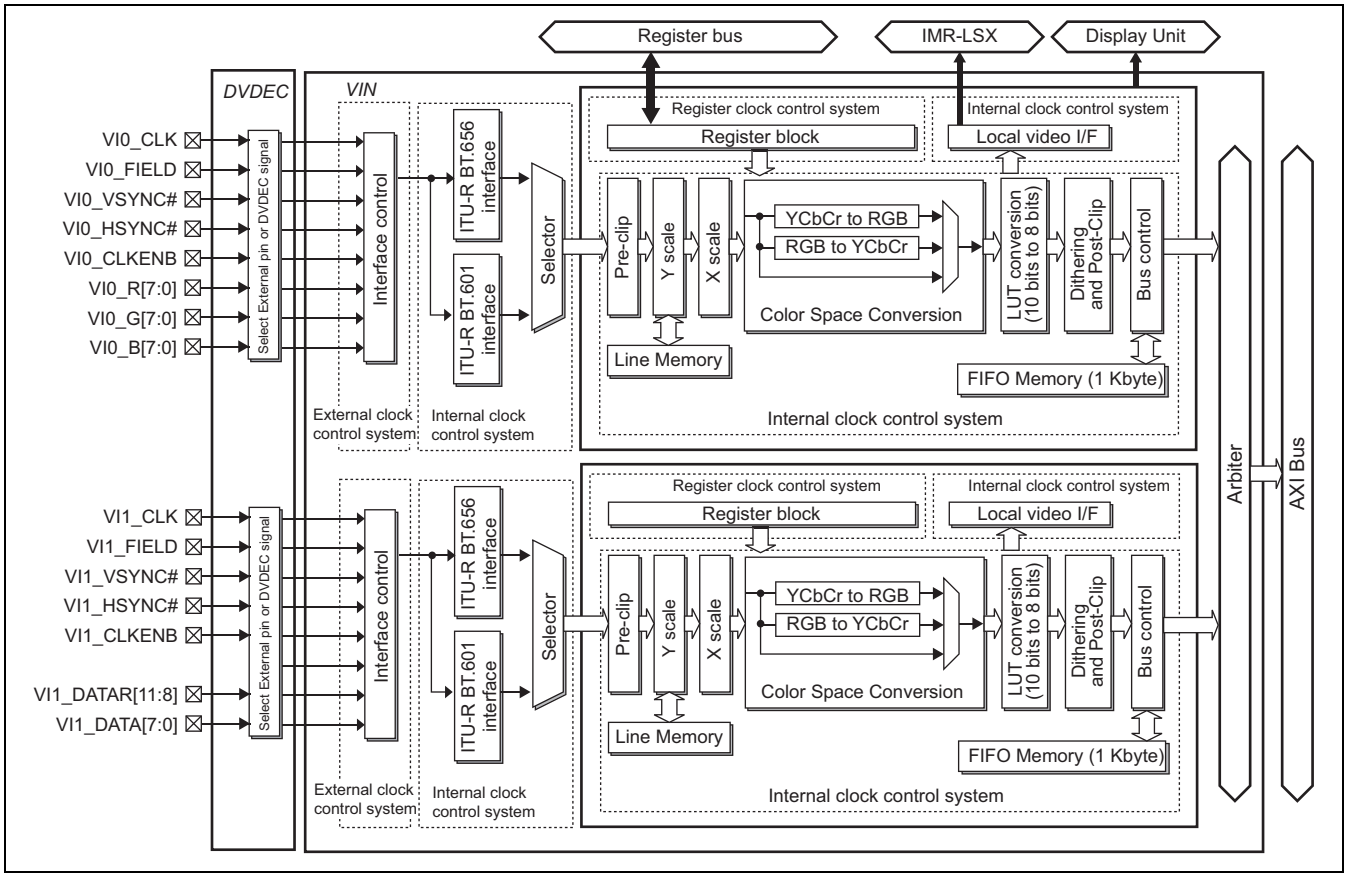


Figure 22.1 VIN Channel n (VINn) Functional Block Diagram

22.1.3 Input/Output Pins

Table 22.3 Pin Configuration

Function	Pin Name	I/O	Description
VIN0 video clock (clock)	VI0_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface
VIN0 field signal (control)	VI0_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.
VIN0 vertical sync signal (control)	VI0_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.
VIN0 horizontal sync signal (control)	VI0_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.
VIN0 data enable (control)	VI0_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.
VIN0 video data (video data)	VI0_R7 to VI0_R0 VI0_G7 to VI0_G0 VI0_DATA7/VI0_B7 to VI0_DATA0/VI0_B0		Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.
VIN1 video clock (clock)	VI1_CLK	Input	External video clock in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface
VIN1 field signal (control)	VI1_FIELD	Input	Field signal in the ITU-R BT.601 or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.
VIN1 vertical sync signal (control)	VI1_VSYNC#	Input	Vertical sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.
VIN1 horizontal sync signal (control)	VI1_HSYNC#	Input	Horizontal sync signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used.
VIN1 data enable (control)	VI1_CLKENB	Input	Data enable signal in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface Fix this pin high or low when the pin is not used. If the signal is not present in the ITU-R BT.601, ITU-R BT.1358, or ITU-R BT.709 interface, connect the pin to a horizontal sync signal.
VIN1 video data (video data)	VI1_DATA7 to VI1_DATA0 VI1_DATA11 to VI1_DATA8 (VI1_G3_B to VI1_G0_B)		Data signals in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface Fix these pins high or low respectively when these pins are not used in whole or in part.

Table 22.4 Channel 0 Data Pin Connections

Input data format	VI0_R[7:0]								VI0_G[7:0]								VI0_DATA[7:0]/VI0_B[7:0]							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 0)	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]							
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR2/YDS = 1)	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]								*	*	*	*	*	*	*	*
ITU-R BT.601/BT.709/BT.656 10-bit YCbCr-422	*	*	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[9:0]									
ITU-R BT.601/BT.709/BT.656 12-bit YCbCr-422	*	*	*	*	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[11:0]											
ITU-R BT.601/BT.709/BT.1358 16-bit YCbCr-422	*	*	*	*	*	*	*	*	Y video data[7:0]								Cb/Cr video data[7:0]							
ITU-R BT.601/BT.709/BT.1358 20-bit YCbCr-422	*	*	*	*	Y video data[9:0]												Cb/Cr video data[9:0]							
ITU-R BT.601/BT.709/BT.1358 24-bit YCbCr-422	Y video data[11:0]																Cb/Cr video data[11:0]							
ITU-R BT.601/BT.709 RGB-666	R video data[5:0]						*	*	G video data[5:0]						*	*	B video data[5:0]						*	*
ITU-R BT.601/BT.709 24-bit RGB-888	R video data[7:0]								G video data[7:0]								B video data[7:0]							

Note: * Fix the pins at a high or low level.

Table 22.5 Channel 1 Data Pin Connections

Input data format	VI1_DATA[11:8]								VI1_DATA[7:0]							
	7	6	5	4	3	2	1	0	7	6	5	4	3	2	1	0
ITU-R BT.601/BT.709/BT.656 8-bit YCbCr-422 (VnDMR/YMODE = B'000)	*	*	*	*	*	*	*	*	Y/Cb/Cr video data[7:0]							
ITU-R BT.601/BT.709/BT.656 10-bit YCbCr-422	*	*	*	*	*	*	Y/Cb/Cr video data[9:0]									
ITU-R BT.601/BT.709/BT.656 12-bit YCbCr-422	*	*	*	*	Y/Cb/Cr video data[11:0]											

Note: * Fix the pins at a high or low level.

22.1.4 Register Configuration

Table 22.6 (1) through Table 22.6 (2) show the VIN register configuration for each channel.

Notes: Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

* For the internal update mode, refer to the description of the VUP bit in the main control register (VnMC).

Δ: The internal update mode supports VnMC.FAST, VnMC.CLP[1:0], VnMC.FOC and VnMC.LUTE bit only.

(1) Channel 0

Table 22.6 (1) VIN Registers

Channel 0

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
0	Video 0 main control register	V0MC	R/W	H'E6EF0000	H'00000000	32	Δ
	Video 0 module status register	V0MS	R	H'E6EF0004	H'00000018	32	—
	Video 0 frame capture register	V0FC	R/W	H'E6EF0008	H'00000000	32	—
	Video 0 start line pre-clip register	V0SLPrC	R/W	H'E6EF000C	H'00000000	32	Supported
	Video 0 end line pre-clip register	V0ELPrC	R/W	H'E6EF0010	H'00000000	32	Supported
	Video 0 start pixel pre-clip register	V0SPPrC	R/W	H'E6EF0014	H'00000000	32	Supported
	Video 0 end pixel pre-clip register	V0EPPrC	R/W	H'E6EF0018	H'00000000	32	Supported
	Video 0 start line post-clip register	V0SLPoC	R/W	H'E6EF001C	H'00000000	32	Supported
	Video 0 end line post-clip register	V0ELPoC	R/W	H'E6EF0020	H'00000000	32	Supported
	Video 0 start pixel post-clip register	V0SPPoC	R/W	H'E6EF0024	H'00000000	32	Supported
	Video 0 end pixel post-clip register	V0EPPoC	R/W	H'E6EF0028	H'00000000	32	Supported
	Video 0 image stride register	V0IS	R/W	H'E6EF002C	H'00000000	32	Supported
	Video 0 memory base 1 register	V0MB1	R/W	H'E6EF0030	H'00000000	32	Supported
	Video 0 memory base 2 register	V0MB2	R/W	H'E6EF0034	H'00000000	32	Supported
	Video 0 memory base 3 register	V0MB3	R/W	H'E6EF0038	H'00000000	32	Supported
	Video 0 line count register	V0LC	R	H'E6EF003C	H'00000000	32	—
	Video 0 interrupt enable register	V0IE	R/W	H'E6EF0040	H'00000000	32	—

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
0	Video 0 interrupt status register	V0INTS	R/W	H'E6EF0044	H'00000000	32	—
	Video 0 scanline interrupt register	V0SI	R/W	H'E6EF0048	H'00000000	32	Supported
	Video 0 memory transfer control register	V0MTC	R/W	H'E6EF004C	H'0A080108	32	Supported
	Video 0 Y scale register	V0YS	R/W	H'E6EF0050	H'00000000	32	Supported
	Video 0 X scale register	V0XS	R/W	H'E6EF0054	H'00000000	32	Supported
	Video 0 data mode register	V0DMR	R/W	H'E6EF0058	H'00000000	32	Supported
	Video 0 data mode register 2	V0DMR2	R/W	H'E6EF005C	H'00000000	32	—
	Video 0 UV address offset register	V0UVAOF	R/W	H'E6EF0060	H'00000000	32	Supported
	Video 0 color space change coefficient 1 register	V0CSCC1	R/W	H'E6EF0064	H'01291080	32	Supported
	Video 0 color space change coefficient 2 register	V0CSCC2	R/W	H'E6EF0068	H'019800D0	32	Supported
	Video 0 color space change coefficient 3 register	V0CSCC3	R/W	H'E6EF006C	H'00640204	32	Supported
	Video 0 coefficient set C1A register	V0C1A	R/W	H'E6EF0080	H'00000000	32	—
	Video 0 coefficient set C1B register	V0C1B	R/W	H'E6EF0084	H'00000000	32	—
	Video 0 coefficient set C1C register	V0C1C	R/W	H'E6EF0088	H'00000000	32	—
	Video 0 coefficient set C2A register	V0C2A	R/W	H'E6EF0090	H'00000000	32	—
	Video 0 coefficient set C2B register	V0C2B	R/W	H'E6EF0094	H'00000000	32	—
	Video 0 coefficient set C2C register	V0C2C	R/W	H'E6EF0098	H'00000000	32	—
	Video 0 coefficient set C3A register	V0C3A	R/W	H'E6EF00A0	H'00000000	32	—
	Video 0 coefficient set C3B register	V0C3B	R/W	H'E6EF00A4	H'00000000	32	—
	Video 0 coefficient set C3C register	V0C3C	R/W	H'E6EF00A8	H'00000000	32	—
	Video 0 coefficient set C4A register	V0C4A	R/W	H'E6EF00B0	H'00000000	32	—
	Video 0 coefficient set C4B register	V0C4B	R/W	H'E6EF00B4	H'00000000	32	—
	Video 0 coefficient set C4C register	V0C4C	R/W	H'E6EF00B8	H'00000000	32	—
	Video 0 coefficient set C5A register	V0C5A	R/W	H'E6EF00C0	H'00000000	32	—
	Video 0 coefficient set C5B register	V0C5B	R/W	H'E6EF00C4	H'00000000	32	—
	Video 0 coefficient set C5C register	V0C5C	R/W	H'E6EF00C8	H'00000000	32	—

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
0	Video 0 coefficient set C6A register	V0C6A	R/W	H'E6EF00D0	H'00000000	32	—
	Video 0 coefficient set C6B register	V0C6B	R/W	H'E6EF00D4	H'00000000	32	—
	Video 0 coefficient set C6C register	V0C6C	R/W	H'E6EF00D8	H'00000000	32	—
	Video 0 coefficient set C7A register	V0C7A	R/W	H'E6EF00E0	H'00000000	32	—
	Video 0 coefficient set C7B register	V0C7B	R/W	H'E6EF00E4	H'00000000	32	—
	Video 0 coefficient set C7C register	V0C7C	R/W	H'E6EF00E8	H'00000000	32	—
	Video 0 coefficient set C8A register	V0C8A	R/W	H'E6EF00F0	H'00000000	32	—
	Video 0 coefficient set C8B register	V0C8B	R/W	H'E6EF00F4	H'00000000	32	—
	Video 0 coefficient set C8C register	V0C8C	R/W	H'E6EF00F8	H'00000000	32	—
	Video 0 lookup table pointer	V0LUTP	R/W	H'E6EF0100	H'00000000	32	—
	Video 0 lookup table data register	V0LUTD	R/W	H'E6EF0104	H'xxxxxxxx	32	—
	Video 0 RGB→Y calculation setting register 1	V0YCCR1	R/W	H'E6EF0228	H'00000107	32	Supported
	Video 0 RGB→Y calculation setting register 2	V0YCCR2	R/W	H'E6EF022C	H'00640204	32	Supported
	Video 0 RGB→Y calculation setting register 3	V0YCCR3	R/W	H'E6EF0230	H'0A000010	32	Supported
	Video 0 RGB→Cb calculation setting register 1	V0CBCCR1	R/W	H'E6EF0234	H'00001F68	32	Supported
	Video 0 RGB→Cb calculation setting register 2	V0CBCCR2	R/W	H'E6EF0238	H'01C21ED6	32	Supported
	Video 0 RGB→Cb calculation setting register 3	V0CBCCR3	R/W	H'E6EF023C	H'0A000080	32	Supported
	Video 0 RGB→Cr calculation setting register 1	V0CRCCR1	R/W	H'E6EF0240	H'000001C2	32	Supported
	Video 0 RGB→Cr calculation setting register 2	V0CRCCR2	R/W	H'E6EF0244	H'1FB71E87	32	Supported
	Video 0 RGB→Cr calculation setting register 3	V0CRCCR3	R/W	H'E6EF0248	H'0A000080	32	Supported
	Video 0 YC→RGB calculation setting register 1	V0CSCE1	R/W	H'E6EF0300	H'0000129F	32	Supported
	Video 0 YC→RGB calculation setting register 2	V0CSCE2	R/W	H'E6EF0304	H'01000800	32	Supported
	Video 0 YC→RGB calculation setting register 3	V0CSCE3	R/W	H'E6EF0308	H'19890D02	32	Supported
	Video 0 YC→RGB calculation setting register 4	V0CSCE4	R/W	H'E6EF030C	H'06452045	32	Supported

(2) Channel 1

Table 22.6 (2) VIN Registers

Channel 1

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
1	Video 1 main control register	V1MC	R/W	H'E6EF1000	H'00000000	32	Δ
	Video 1 module status register	V1MS	R	H'E6EF1004	H'00000018	32	—
	Video 1 frame capture register	V1FC	R/W	H'E6EF1008	H'00000000	32	—
	Video 1 start line pre-clip register	V1SLPrC	R/W	H'E6EF100C	H'00000000	32	Supported
	Video 1 end line pre-clip register	V1ELPrC	R/W	H'E6EF1010	H'00000000	32	Supported
	Video 1 start pixel pre-clip register	V1SPPrC	R/W	H'E6EF1014	H'00000000	32	Supported
	Video 1 end pixel pre-clip register	V1EPPrC	R/W	H'E6EF1018	H'00000000	32	Supported
	Video 1 start line post-clip register	V1SLPoC	R/W	H'E6EF101C	H'00000000	32	Supported
	Video 1 end line post-clip register	V1ELPoC	R/W	H'E6EF1020	H'00000000	32	Supported
	Video 1 start pixel post-clip register	V1SPPoC	R/W	H'E6EF1024	H'00000000	32	Supported
	Video 1 start pixel pre-clip register	V1SPPrC	R/W	H'E6EF1014	H'00000000	32	Supported
	Video 1 end pixel pre-clip register	V1EPPrC	R/W	H'E6EF1018	H'00000000	32	Supported
	Video 1 start line post-clip register	V1SLPoC	R/W	H'E6EF101C	H'00000000	32	Supported
	Video 1 end line post-clip register	V1ELPoC	R/W	H'E6EF1020	H'00000000	32	Supported
	Video 1 start pixel post-clip register	V1SPPoC	R/W	H'E6EF1024	H'00000000	32	Supported
	Video 1 end pixel post-clip register	V1EPPoC	R/W	H'E6EF1028	H'00000000	32	Supported
	Video 1 image stride register	V1IS	R/W	H'E6EF102C	H'00000000	32	Supported
	Video 1 memory base 1 register	V1MB1	R/W	H'E6EF1030	H'00000000	32	Supported
	Video 1 memory base 2 register	V1MB2	R/W	H'E6EF1034	H'00000000	32	Supported
	Video 1 memory base 3 register	V1MB3	R/W	H'E6EF1038	H'00000000	32	Supported
	Video 1 line count register	V1LC	R	H'E6EF103C	H'00000000	32	—

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
1	Video 1 interrupt enable register	V1IE	R/W	H'E6EF1040	H'00000000	32	—
	Video 1 interrupt status register	V1INTS	R/W	H'E6EF1044	H'00000000	32	—
	Video 1 scanline interrupt register	V1SI	R/W	H'E6EF1048	H'00000000	32	Supported
	Video 1 memory transfer control register	V1MTC	R/W	H'E6EF104C	H'0A080108	32	Supported
	Video 1 Y scale register	V1YS	R/W	H'E6EF1050	H'00000000	32	Supported
	Video 1 X scale register	V1XS	R/W	H'E6EF1054	H'00000000	32	Supported
	Video 1 data mode register	V1DMR	R/W	H'E6EF1058	H'00000000	32	Supported
	Video 1 data mode register 2	V1DMR2	R/W	H'E6EF105C	H'00000000	32	—
	Video 1 UV address offset register	V1UVAOF	R/W	H'E6EF1060	H'00000000	32	Supported
	Video 1 color space change coefficient 1 register	V1CSCC1	R/W	H'E6EF1064	H'01291080	32	Supported
	Video 1 color space change coefficient 2 register	V1CSCC2	R/W	H'E6EF1068	H'019800D0	32	Supported
	Video 1 color space change coefficient 3 register	V1CSCC3	R/W	H'E6EF106C	H'00640204	32	Supported
	Video 1 coefficient set C1A register	V1C1A	R/W	H'E6EF1080	H'00000000	32	—
	Video 1 coefficient set C1B register	V1C1B	R/W	H'E6EF1084	H'00000000	32	—
	Video 1 coefficient set C1C register	V1C1C	R/W	H'E6EF1088	H'00000000	32	—
	Video 1 coefficient set C2A register	V1C2A	R/W	H'E6EF1090	H'00000000	32	—
	Video 1 coefficient set C2B register	V1C2B	R/W	H'E6EF1094	H'00000000	32	—
	Video 1 coefficient set C2C register	V1C2C	R/W	H'E6EF1098	H'00000000	32	—
	Video 1 coefficient set C3A register	V1C3A	R/W	H'E6EF10A0	H'00000000	32	—
	Video 1 coefficient set C3B register	V1C3B	R/W	H'E6EF10A4	H'00000000	32	—
	Video 1 coefficient set C3C register	V1C3C	R/W	H'E6EF10A8	H'00000000	32	—
	Video 1 coefficient set C4A register	V1C4A	R/W	H'E6EF10B0	H'00000000	32	—
	Video 1 coefficient set C4B register	V1C4B	R/W	H'E6EF10B4	H'00000000	32	—
	Video 1 coefficient set C4C register	V1C4C	R/W	H'E6EF10B8	H'00000000	32	—
	Video 1 coefficient set C5A register	V1C5A	R/W	H'E6EF10C0	H'00000000	32	—
	Video 1 coefficient set C5B register	V1C5B	R/W	H'E6EF10C4	H'00000000	32	—

Channel	Name	Symbol	R/W	Address	Initial Value	Access Size	Internal Update Mode Support*
1	Video 1 coefficient set C5C register	V1C5C	R/W	H'E6EF10C8	H'00000000	32	—
	Video 1 coefficient set C6A register	V1C6A	R/W	H'E6EF10D0	H'00000000	32	—
	Video 1 coefficient set C6B register	V1C6B	R/W	H'E6EF10D4	H'00000000	32	—
	Video 1 coefficient set C6C register	V1C6C	R/W	H'E6EF10D8	H'00000000	32	—
	Video 1 coefficient set C7A register	V1C7A	R/W	H'E6EF10E0	H'00000000	32	—
	Video 1 coefficient set C7B register	V1C7B	R/W	H'E6EF10E4	H'00000000	32	—
	Video 1 coefficient set C7C register	V1C7C	R/W	H'E6EF10E8	H'00000000	32	—
	Video 1 coefficient set C8A register	V1C8A	R/W	H'E6EF10F0	H'00000000	32	—
	Video 1 coefficient set C8B register	V1C8B	R/W	H'E6EF10F4	H'00000000	32	—
	Video 1 coefficient set C8C register	V1C8C	R/W	H'E6EF10F8	H'00000000	32	—
	Video 1 lookup table pointer	V1LUTP	R/W	H'E6EF1100	H'00000000	32	—
	Video 1 lookup table data register	V1LUTD	R/W	H'E6EF1104	H'xxxxxxxx	32	—
	Video 1 RGB→Y calculation setting register 1	V1YCCR1	R/W	H'E6EF1228	H'00000107	32	Supported
	Video 1 RGB→Y calculation setting register 2	V1YCCR2	R/W	H'E6EF122C	H'00640204	32	Supported
	Video 1 RGB→Y calculation setting register 3	V1YCCR3	R/W	H'E6EF1230	H'0A000010	32	Supported
	Video 1 RGB→Cb calculation setting register 1	V1CBCCR1	R/W	H'E6EF1234	H'00001F68	32	Supported
	Video 1 RGB→Cb calculation setting register 2	V1CBCCR2	R/W	H'E6EF1238	H'01C21ED6	32	Supported
	Video 1 RGB→Cb calculation setting register 3	V1CBCCR3	R/W	H'E6EF123C	H'0A000080	32	Supported
	Video 1 RGB→Cr calculation setting register 1	V1CRCCR1	R/W	H'E6EF1240	H'000001C2	32	Supported
	Video 1 RGB→Cr calculation setting register 2	V1CRCCR2	R/W	H'E6EF1244	H'1FB71E87	32	Supported
	Video 1 RGB→Cr calculation setting register 3	V1CRCCR3	R/W	H'E6EF1248	H'0A000080	32	Supported
	Video 1 YC→RGB calculation setting register 1	V1CSCE1	R/W	H'E6EF1300	H'0000129F	32	Supported
	Video 1 YC→RGB calculation setting register 2	V1CSCE2	R/W	H'E6EF1304	H'01000800	32	Supported
	Video 1 YC→RGB calculation setting register 3	V1CSCE3	R/W	H'E6EF1308	H'19890D02	32	Supported
	Video 1 YC→RGB calculation setting register 4	V1CSCE4	R/W	H'E6EF130C	H'06452045	32	Supported

22.2 Register Descriptions

[Legend]

—: Reserved. The write value should always be 0.

Initial value: Register value after a reset

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

Vn: Video Channel n

22.2.1 Video n Main Control Register (VnMC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FAST	—	CLP[1:0]		—	—	—	—	—	—	FOC	LUTE	YCAL	INF[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DC[1:0]		EXINF[1:0]		—	VUP	—	—	—	EN	EC	IM[1:0]		—	BPS	ME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FAST	0	R/W	High-Speed Video Clock Support Mode Set this bit to 1 to input 100-MHz video clock. 0: 100-MHz video clock input is not supported. 1: 100-MHz video clock input is supported. Note: Do not perform vertical or horizontal scaling up when this bit is 1.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	CLP[1:0]	00	R/W	Pixel Data Clipping When the input image data is in the YCbCr format, these bits specify the data clip value for clipping the YCbCr-RGB color conversion input data to the nominal range prescribed in the ITU-R BT.601 standard.

CLP	Luminance	Color Difference	
00	No clipping	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	Initial value
01	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	16 or a smaller value is clipped to 16. 240 or a greater value is clipped to 240.	
10	No clipping	16 or a smaller value is clipped to 128. 240 or a greater value is clipped to 128.	
11	No clipping	No clipping	

Note: These bits support the internal update mode.

Bit	Bit Name	Initial Value	R/W	Description
27 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	FOC	0	R/W	Field Order Control This bit controls the field order for full interlace capturing. 0: Top field = Odd field (field 1) 1: Top field = Even field (field 2) Note: This bit supports the internal update mode.

Bit	Bit Name	Initial Value	R/W	Description
20	LUTE	0	R/W	Lookup Table Enable This bit enables lookup table conversion from 10 bits to 8 bits. 0: LUT is not used. 1: LUT is used. Notes: 1. To perform LUT conversion, the conversion table should be set with VnLUTP and VnLUTD. 2. This bit supports the internal update mode.
19	YCAL	0	R/W	YCbCr-422 Input Data Alignment This bit controls data alignment for YCbCr-422 input. 0: When the multiplexed CbCr interface is set, capturing is performed with Y in the upper bits and CbCr in the lower bits. 1: When the multiplexed CbCr interface is set, capturing is performed with CbCr in the upper bits and Y in the lower bits.
18 to 16	INF[2:0]	000	R/W	Input Interface Format These bits specify the image format input to the VIN. 000: ITU-R BT.656 8-bit YCbCr-422 or ITU-R BT.656 8-bit YCbCr422 4-bit input*1 001: ITU-R BT.601/BT.709 8-bit YCbCr-422 or ITU-R BT.601/BT.709 8-bit YCbCr422 4-bit input *1 010: ITU-R BT.656 10/12-bit YCbCr-422*1 011: ITU-R BT.601/BT.709 10/12-bit YCbCr-422*1 100: Setting prohibited 101: ITU-R BT.601/BT.1358 16-bit YCbCr-422 or ITU-R BT.601/BT.709/BT.656 8-bit YCbCr422 8-bit input*1 110: ITU-R BT.601/BT.709 24-bit RGB-888*1 111: ITU-R BT.601/BT.709 18-bit RGB-666 or ITU-R BT.601/BT.709 RGB-888 12-bit input*1
15, 14	DC[1:0]	00	R/W	Dithering Mode Control These bits select the dithering mode for conversion from RGB888 to RGB565/ARGB1565. 00: Dithering with cumulative addition 01: Ordered dithering 10: Setting prohibited 11: Setting prohibited
13, 12	EXINF[1:0]	00	R/W	Extension Interface Select 00: Data extension is not performed 01: Combined with the INF setting, 8-bit data extension is performed. 10: Combined with the INF setting, 10-bit data extension is performed. 11: Combined with the INF setting, 12-bit data extension is performed.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	VUP	0	R/W	VIN Register Update Control This bit specifies the internal register update timing after register writing. See the list of registers for applicable registers. 0: The register contents are updated immediately after register writing. 1: The register contents are updated after a valid field is detected in the ITU-R BT.601 data or the field (F) bit changes in the ITU-R BT.656 data.
9 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	EN	0	R/W	Endian Type This bit specifies the endian type for data to be output to external memory. 0: Image data is packed and allocated in little endian. 1: Image data is packed and allocated in big endian. Note: When allocating the YCbCr422 (UYVY format) data in big endian, be sure to set the BPSM bit in VnDMR to 1.
5	EC	0	R/W	Error Correction Control This bit specifies whether error correction with the parity bit is performed on the ITU-R BT.656 input. 0: Error correction is not performed on the ITU-R BT.656 input. 1: Error correction with the parity bit is performed on the ITU-R BT.656 input. Error correction must not be performed in the following cases: • When data is captured in the ITU-R BT.601 interface • When input data does not meet the standard of the ITU-R BT.656 parity bit
4, 3	IM[1:0]	00	R/W	Interlace Mode These bits specify the capture mode. Do not modify this setting during capture operation. 00: Odd-field (field 1) capture mode Handles only odd fields as frames and stores them in external memory. 01: Odd-/even-field capture mode Handles odd and even fields as separate frames and stores them in external memory. This mode is available only in continuous frame capture mode. 10: Even-field (field 2) capture mode Handles only even fields as frames and stores them in external memory. 11: Full interlace mode Handles combinations of odd and even fields as single frames and stores them in external memory.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	BPS	0	R/W	Color Space Conversion Bypass Mode 0: The input YCbCr data is converted into the RGB color space and RGB data is converted into the YCbCr color space*2. 1: Color space conversion is not performed. Note: YCbCr→RGB or RGB→YCbCr conversion is performed with the coefficients specified by the YC-RGB conversion coefficient register or RGB-YC coefficient register.
0	ME	0	R/W	Module Enable This is the enable bit for the VIN. Set this bit before setting the Frame Capture (VnFC) register. 0: The module operation is stopped. 1: The module operation is enabled. *3

Notes: 1. Table 22.7 shows the combinations of interfaces which can be set by the input interface format (the INF bits in VnMC) and extension interface select (the EXINF bit in VnMC). Do not make the other settings.
2. Table 22.8 shows the image data which can be converted according to the color space conversion bypass mode settings (set by the BPS bit in VnMC).
3. To stop capturing operation, only set the ME bit to 0. Do not change the other bit settings.

Table 22.7 Capture Interface Settings

Interface		VnMC/EXINF	VnMC/INF
ITU-R BT.656 (multiplexed YCbCr422)	8 bits	00	000
	10 bits	00	010
	12 bits	11	010
ITU-R BT.601/BT.709 (multiplexed YCbCr422)	8 bits	00	001
	10 bits	00	011
	12 bits	11	011
ITU-R BT.601/BT.709/BT.1358 (non-multiplexed Y/multiplexed CbCr)	16 bits	00	101
	20 bits	10	101
	24 bits	11	101
ITU-R BT.601/BT.709 (RGB666)	18 bits	00	111
ITU-R BT.601/BT.709 (RGB888)	24 bits	00	110

Table 22.8 Captured Data Formats

Input Data Format	VnMC/INF	VnMC/BPS	Captured Data Format
ITU-R BT.656/BT.601/BT.709/BT.1358 YCbCr	000/001 010/011 100/101	0	RGB format
		1	YCbCr format
ITU-R BT.601/BT.709 RGB	110/111	0	YCbCr format
		1	RGB format

22.2.2 Video n Module Status Register (VnMS)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	FBS[1:0]		FS	AV	CA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4, 3	FBS[1:0]	11	R	Frame Buffer Status These bits show the frame buffer status. 00: The latest valid frame buffer has the base address defined by the memory base 1 register. 01: The latest valid frame buffer has the base address defined by the memory base 2 register. 10: The latest valid frame buffer has the base address defined by the memory base 3 register. 11: There is no valid frame buffer.
2	FS	0	R	Field Status This bit shows the type of the current capture field. 0: The current field is an odd field (field 1). 1: The current field is an even field (field 2).
1	AV	0	R	Active Video Status This bit shows whether the current field is in the active video area defined by the pre-clipping register. 0: The current field is not in the active video area. 1: The current field is in the active video area. Note: This bit will be 0 if no input data is captured.
0	CA	0	R	Video Capture Active Status This bit shows the current video capture operation status. This bit is updated by the captured field signal. 0: Video capture is not operating. 1: Video capture is operating. Note: In field capture mode, this bit is set to 1 even for the field that does not capture data.

22.2.3 Video n Frame Capture Register (VnFC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CC	SC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	CC	0	R/W	Continuous Frame Capture Mode This bit specifies the continuous frame capture mode. In this mode, the first capture frame is written into the memory address specified by the memory base 1 (VnMB1) register. After that, the capture operation is repeated in the order of MB2, MB3, MB1, MB2, and such. Writing 0 into this bit during continuous capture operation will immediately terminate the capture operation if the current frame is completed or it has not been captured. 0: The continuous frame capture mode is not set. 1: The continuous frame capture mode is set.
0	SC	0	R/W	Single Frame Capture Mode This bit specifies the single frame capture mode. In this mode, the capture frame is written into the memory address specified by the memory base 1 (VnMB1) register. Immediately after this bit is set to 1, the frame buffer status (FBS) bits in MS are initialized and the SC bit is also cleared to 0. 0: The single frame capture mode is not set. 1: The single frame capture mode is set. Note: Do not set this bit to 1 when the interlace mode (IM) bits in the main control register (VnMC) are set to 01 (odd-/even-field capture mode).

Note: Do not specify the single frame capture mode and continuous frame capture mode at the same time.

22.2.4 Video n Start Line Pre-Clip Register (VnSLPrC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SLPrC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SLPrC[10:0]	H'000	R/W	Start Line Pre-Clip These bits specify the (pre-clipping start line – 1) value in line units. This value is used before scaling. Specify a value in the range from 0 to 2046 so that the number of lines after pre-clipping will be 2 or more. (The value of 0 indicates the first valid line.)

22.2.5 Video n End Line Pre-Clip Register (VnELPrC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	ELPrC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	ELPrC[10:0]	H'000	R/W	End Line Pre-Clip These bits specify the (pre-clipping end line – 1) value in line units. This value is used before scaling. Specify a value in the range from 1 to 2047 so that the number of lines after pre-clipping will be 2 or more.

22.2.6 Video n Start Pixel Pre-Clip Register (VnSPPrC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPPrC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SPPrC[10:0]	H'000	R/W	Start Pixel Pre-Clip These bits specify the (pre-clipping start pixel – 1) value in pixel units. This value is used before scaling. Specify a value in the range from 0 to 2042 so that the number of pixels after pre-clipping will be an even number than 6. Notes: 1. When SPPrC is set to 0x0, the first valid pixel is specified. 2. Specify an even number. 3. The capacity of the internal buffer is limited, so if the horizontal scaling up function is in use, the value here should be such that EPPrC – SPPrC is no greater than 2048 pixels.

22.2.7 Video n End Pixel Pre-Clip Register (VnEPPrC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	EPPrC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	EPPrC[10:0]	H'000	R/W	End Pixel Pre-Clip These bits specify the (pre-clipping end pixel – 1) value in pixel units. This value is used before scaling. Specify a value in the range from 5 to 2047 so that the number of pixels after pre-clipping will be an even number than 6. Notes: 1. Set this bit so that the (EPPrC – SPPrC) value is an odd number. 2. The capacity of the internal buffer is limited, so if the horizontal scaling up function is in use, the value here should be such that EPPrC – SPPrC is no greater than 2048 pixels.

22.2.8 Video n Start Line Post-Clip Register (VnSLPoC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SLPoC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SLPoC[10:0]	H'000	R/W	Start Line Post-Clip These bits specify the (post-clipping start line – 1) value in line units. This value is used after scaling. Specify a value in the range from 0 to 2046 so that the number of lines after post-clipping will be 2 or more. (The value of 0 indicates the start line after scaling.)

22.2.9 Video n End Line Post-Clip Register (VnELPoC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	ELPoC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	ELPoC[10:0]	H'000	R/W	End Line Post-Clip These bits specify the (post-clipping end line – 1) value in line units. This value is used after scaling. Specify a value in the range from 1 to 2047 so that the number of lines after post-clipping will be 2 or more.

22.2.10 Video n Start Pixel Post-Clip Register (VnSPPoC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPPoC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SPPoC[10:0]	H'000	R/W	Start Pixel Post-Clip These bits specify the (post-clipping start pixel – 1) value in pixel units. This value is used after scaling. Specify a value in the range from 0 to 2042 so that the number of pixels after post-clipping will be 5 or more.

22.2.11 Video n End Pixel Post-Clip Register (VnEPPoC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	EPPoC[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	EPPoC[10:0]	H'000	R/W	End Pixel Post-Clip These bits specify the (post-clipping end pixel – 1) value in pixel units. This value is used after scaling. Specify a value in the range from 5 to 2047 so that the number of pixels after post-clipping will be 5 or more.

Note: When the output format is YCbCr-422, even if the settings produce a post-clipping size in pixels that is an odd number, the output to memory will be in even pixel units. Note that if the clipping values specify an odd size (i.e. if EPPoC – SPPoC is odd), one will be added to round the value up to an even number.

Example: When SPPoC is set to 0 and EPPoC is set to 62:

The actual processing is done for 64 pixels.
62 - 0 = 62 (63 pixels)
63 pixels + 1 = 64 pixels

22.2.12 Video n Image Stride Register (VnIS)

Note: Availability of channels:
n = 0 to 1

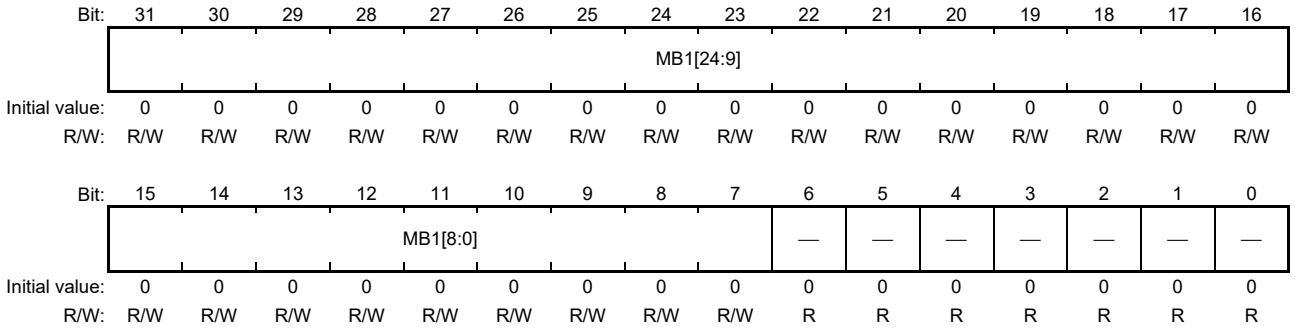
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IS[8:0]									—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 4	IS[8:0]	H'000	R/W	Image Stride These bits specify the width of the transfer destination memory. Specify a value no less than the post-clipping width (EPPoC - SPPoC) and aligned with a 32-byte boundary (i.e. bit 4 should be specified as 0). For 16 bits/pixel data, word addresses are generated. For 8 bits/pixel data in YC separation mode, byte addresses are generated.
3 to 0	—	All 0	R	Reserved bits that indicate the lower-order four bits of the image stride. These bits are always read as 0. The write value should always be 0.

22.2.13 Video n Memory Base 1 Register (VnMB1)

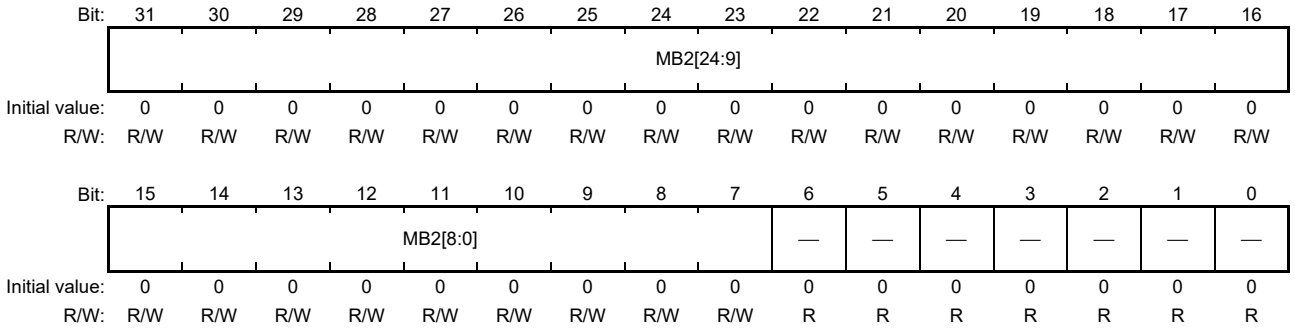
Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	MB1[24:0]	H'0000000	R/W	Memory Base Address 1 These bits specify the transfer start address in frame buffer 1. Specify a value for physical address bits [31:7] in units of 128 bytes. If the module is in continuous frame capture mode, this value is used as the MB1 address in the following capture sequence: MB1 → MB2 → MB3 → MB1 → MB2 → MB3. In single frame capture mode, this value is used as the capture address. Specify a memory address taking into account the image size so that the image data does not exceed an area boundary on the address map.
6 to 0	—	All 0	R	Reserved bits that indicate the lower-order seven bits of memory base address 1 (a multiple of 128 bytes). These bits are always read as 0. The write value should always be 0.

22.2.14 Video n Memory Base 2 Register (VnMB2)

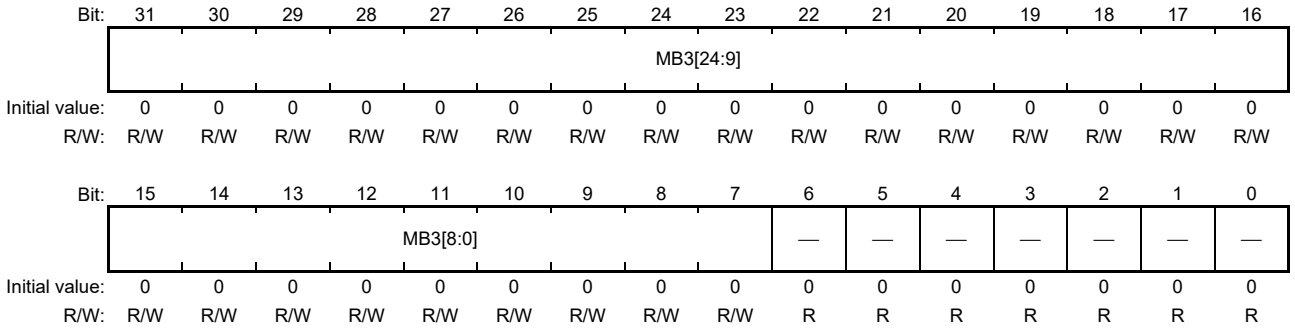
Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	MB2[24:0]	H'0000000	R/W	Memory Base Address 2 These bits specify the transfer start address in frame buffer 2. Specify a value for physical address bits [31:7] in units of 128 bytes. If the module is in continuous frame capture mode, this value is used as the MB2 address in the following capture sequence: MB1 → MB2 → MB3 → MB1 → MB2 → MB3. Specify a memory address taking into account the image size so that the image data does not exceed an area boundary on the address map.
6 to 0	—	All 0	R	Reserved bits that indicate the lower-order seven bits of memory base address 2 (a multiple of 128 bytes). These bits are always read as 0. The write value should always be 0.

22.2.15 Video n Memory Base 3 Register (VnMB3)

Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31 to 7	MB3[24:0]	H'0000000	R/W	Memory Base Address 3 These bits specify the transfer start address in frame buffer 3. Specify a value for physical address bits [31:7] in units of 128 bytes. If the module is in continuous frame capture mode, this value is used as the MB3 address in the following capture sequence: MB1 → MB2 → MB3 → MB1 → MB2 → MB3. Specify a memory address taking into account the image size so that the image data does not exceed an area boundary on the address map.
6 to 0	—	All 0	R	Reserved bits that indicate the lower-order seven bits of memory base address 3 (a multiple of 128 bytes). These bits are always read as 0. The write value should always be 0.

22.2.16 Video n Line Count Register (VnLC)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LC[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	LC[11:0]	All 0	R	Line Count These bits show the line position in the current capture field.

22.2.17 Video n Interrupt Enable Register (VnIE)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIE2	—	—	—	—	—	—	—	—	—	—	—	—	—	VFE	VRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	FIE	CEE	SIE	EFE	FOE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FIE2	0	R/W	Field Interrupt Enable 2 This bit enables or disables INTC output for field interrupts. Interrupt signals by this enable bit is asserted irrespective of whether capture is taking place. 0: Field interrupts are disabled. 1: Field interrupts are enabled.
30 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	VFE	0	R/W	VSYNC Falling Edge Detect Interrupt Enable This bit enables or disables VSYNC falling edge detect interrupts. Interrupt signals by this enable bit is asserted irrespective of whether capture is taking place. 0: VSYNC falling edge detect interrupts are disabled. 1: VSYNC falling edge detect interrupts are enabled.
16	VRE	0	R/W	VSYNC Rising Edge Detect Interrupt Enable This bit enables or disables VSYNC rising edge detect interrupts. Interrupt signals by this enable bit is asserted irrespective of whether capture is taking place. 0: VSYNC rising edge detect interrupts are disabled. 1: VSYNC rising edge detect interrupts are enabled.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FIE	0	R/W	Field Interrupt Enable This bit enables or disables field-switching interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1. 0: Field-switching interrupts are disabled. 1: Field-switching interrupts are enabled.
3	CEE	0	R/W	Correction Error Interrupt Enable This bit enables or disables interrupts due to error correction in the timing reference code (SAV/EAV) described in the ITU-R BT.656 specification. This interrupt enable setting is valid when the CA bit in VnMS is 1. 0: ITU-R BT.656 timing reference code error interrupts are disabled. 1: ITU-R BT.656 timing reference code error interrupts are enabled.

Bit	Bit Name	Initial Value	R/W	Description
2	SIE	0	R/W	Scanline Interrupt Enable This bit enables or disables scanline interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1. 0: Scanline interrupts are disabled. 1: Scanline interrupts are enabled.
1	EFE	0	R/W	End of Frame Interrupt Enable This bit enables or disables end of frame interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1. 0: End of frame interrupts are disabled. 1: End of frame interrupts are enabled.
0	FOE	0	R/W	FIFO Overflow Interrupt Enable This bit enables or disables FIFO overflow interrupts. This interrupt enable setting is valid when the CA bit in VnMS is 1. 0: FIFO overflow interrupts are disabled. 1: FIFO overflow interrupts are enabled.

22.2.18 Video n Interrupt Status Register (VnINTS)

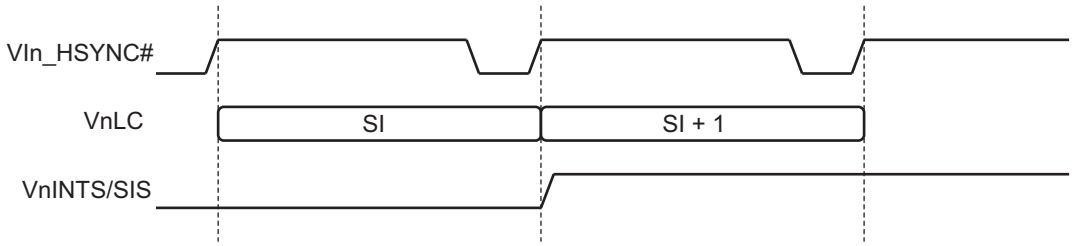
Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIS2	—	—	—	—	—	—	—	—	—	—	—	—	—	VFS	VRS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	FIS	CES	SIS	EFS	FOS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FIS2	0	R/W	Field Interrupt Status 2 This bit shows that the field has changed. This bit is set to 1 when a valid field is detected in the ITU-R BT.601 interface or the F bit defined in ITU-R BT.656 changes. After being set to 1, this bit is cleared to 0 by writing 1. Note: This bit is set to 1 irrespective of whether or not capture is taking place. Be sure to clear this bit to 0 before using it.
30 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	VFS	0	R/W	VSYNC Falling Edge Detect Interrupt Status This bit shows that a VSYNC falling edge has been detected in the ITU-R BT.601 input. After being set to 1, this bit is cleared to 0 by writing 1. Note: This bit is set to 1 irrespective of whether or not capture is taking place. Be sure to clear this bit to 0 before using it.
16	VRS	0	R/W	VSYNC Rising Edge Detect Interrupt Status This bit shows that a VSYNC rising edge has been detected in the ITU-R BT.601 input. After being set to 1, this bit is cleared to 0 by writing 1. Note: This bit is set to 1 irrespective of whether or not capture is taking place. Be sure to clear this bit to 0 before using it.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	FIS	0	R/W	Field Interrupt Status This bit shows that a field has been captured in the active capture operation. This bit is set to 1 when a valid field is detected in the ITU-R BT.601 interface or the F bit defined in ITU-R BT.656 changes. After being set to 1, this bit is cleared to 0 by writing 1.
3	CES	0	R/W	Correction Error Interrupt Status This bit shows that the timing reference code in the active capture operation has an error involving at least two bits. After being set to 1, this bit is cleared to 0 by writing 1. This bit is set to 1 if the EC bit in VnMC is enabled and the timing reference code has an error involving at least two bits. If a 1-bit error occurs when the EC bit is enabled, this bit is not set to 1.

Bit	Bit Name	Initial Value	R/W	Description
2	SIS	0	R/W	Scanline Interrupt Status This bit shows that the number of lines specified by VnSI has been reached in the active capture operation. After being set to 1, this bit is cleared to 0 by writing 1. This bit is set to 1 at the next line start timing after the value in the VnLC register matches the VnSI register setting. This timing is shown in Figure 22.2, Scanline Interrupt Status Generation Timing.
1	EFS	0	R/W	End of Frame Interrupt Status This bit shows that the last frame has been reached in the active capture operation. This bit is set to 1 at the end of even field (field 2). After being set to 1, this bit is cleared to 0 by writing 1.
0	FOS	0	R/W	FIFO Overflow Interrupt Status This bit shows that the FIFO has overflowed in the active capture operation. After being set to 1, this bit is cleared to 0 by writing 1. If the FIFO overflows, the FIFO data is overwritten by the pixel data captured after the overflow, and the resultant data is sent to the frame buffer.



Note:The SIS bit is set at the next line start timing after the VnSI value is reached.

Figure 22.2 Scanline Interrupt Status Generation Timing

22.2.19 Video n Scanline Interrupt Register (VnSI)

Note: Availability of channels:
n = 0 to 1

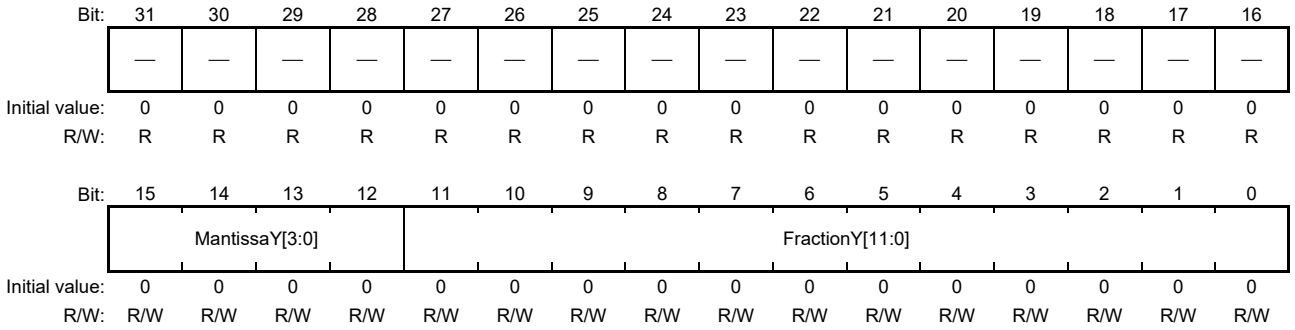
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SI[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	SI[11:0]	All 0	R/W	Scanline Interrupt Setting These bits specify a value to be compared with the VnLC register value in each field while the SIE bit in the VnIE register is set to 1. When this value matches the VnLC register value, an interrupt signal is asserted.

22.2.20 Video n Y Scale Register (VnYS)

Note: Availability of channels:
n = 0 to 1

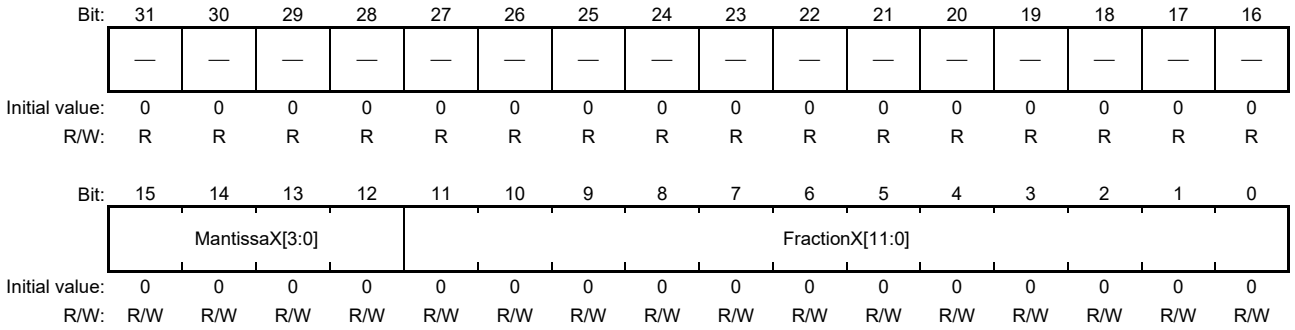


Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	MantissaY [3:0]	H'0	R/W	The scaling ratio in the Y direction should be specified through MantissaY and FractionY. This register specifies the value of (number of lines output to memory per field) / (number of capture lines per field) and it is calculated from MantissaY and FractionY by the following equation. Y scaling = 4096/(4096 × MantissaY + FractionY) For example, to obtain a Y scaling ratio of 1/2, specify MantissaY = H'2 and FractionY = H'000. Note that the maximum scaling-up ratio is × 3. When both MantissaY and FractionY are set to 0, the scaling function is disabled. To specify a scaling ratio of × 1, disabling of the scaling function is recommended.
11 to 0	FractionY [11:0]	H'000	R/W	

Notes: 1. Do not make the scaling-up setting when the FAST bit in MC is set to enable the applicable function.
2. Disable the scaling function when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT656 interface or the 20/24-bit YCbCr-422 format in the ITU-R BT.1358 interface.
3. The minimum scaling-down ratio is:
Mantissa[3:0] = H'E, Fraction[11:0] = H'FFF

22.2.21 Video n X Scale Register (VnXS)

Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	MantissaX [3:0]	H'0	R/W	The scaling ratio in the X direction should be specified through MantissaX and FractionX. This register specifies the value of (number of pixels output to memory per line) / (number of input pixels per line) and it is calculated from MantissaX and FractionX by the following equation. X scaling = 4096/(4096 × MantissaX + FractionX) As the multiphase filter specified by the coefficient set CmA (m = 1 to 8) registers are used for scaling, be sure to specify the coefficient set registers for scaling. Note that the maximum scaling-up ratio is ×2. When both MantissaX and FractionX are set to 0, the scaling function is disabled. To specify a scaling ratio of ×1, set both the mantissaX and fractionX to 0. Typical examples of this register setting and scaling ratio for 720 input pixels are shown in Table 22.13.
11 to 0	FractionX [11:0]	H'000	R/W	

Notes: 1. Do not make the scaling-up setting when the FAST bit in MC is set to enable the applicable function.
2. Disable the scaling function when using the 10/12-bit YCbCr-422 format in the ITU-R BT.601, BT.709, or BT656 interface or the 20/24-bit YCbCr-422 format in the ITU-R BT.1358 interface.

Table 22.9 Examples of Scaling Setting (Input Pixels: 720 Pixels)

Output Pixels	Scaling Ratio	Setting
680	0.943	H'10F8
800	1.111	H'0E68
854	1.185	H'0D80

22.2.22 Video n Data Mode Register (VnDMR)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	A8BIT[7:0]								—	—	—	—	—	—	—	EVA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	YMODE[2:0]			—	—	—	EXRGB	—	—	—	BPSM	—	ABIT	DTMD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R	R/W	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	A8BIT[7:0]	H'00	R/W	Alpha 8 These bits set the alpha value for the ARGB8888 format output.
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	EVA	0	R/W	Even Field Address Offset This bit specifies the address offset of the even field (field 2) in memory in odd-/even-field capture mode. 0: Data are stored from the base address in external memory. 1: Data are stored from the base address plus the memory width in external memory.
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	YMODE[2:0]	000	R/W	YC Data Transfer Mode These bits specify the transfer method of Y/CbCr when the data conversion mode (DTMD) is 10 (YC separation). 000: Both Y and CbCr data are transferred to memory 001: Only Y data is transferred to memory as 8-bit data 010: 10-bit Y data is converted to 16-bit data and both Y and CbCr data are transferred to memory. 011: 10-bit Y data is converted to 16-bit data and only Y data is transferred to memory. 100: 12-bit Y data is converted to 16-bit data and both Y and CbCr data are transferred to memory. 101: 12-bit Y data is converted to 16-bit data and only Y data is transferred to memory. 110: Setting prohibited 111: Setting prohibited
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	EXRGB	0	R/W	Extension RGB Conversion Mode 0: RGB data extension processing is not performed. 1: Data is extended to 32-bit RGB conversion when DTMD[1:0] is set to 00 or 01 as the data conversion mode.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	BPSM	0	R/W	Output Data Byte Swap Mode 0: Bytes are not swapped in output data. 1: Bytes are swapped in output data. Note: When YCbCr-422 data is output in big endian, data is transferred in the YUYV format in most cases. To transfer data in the UYVY format, set this bit to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ABIT	0	R/W	Alpha Bit This bit specifies the alpha value for data in ARGB-1555 output mode. 0: The alpha value is set to 0. 1: The alpha value is set to 1.
1, 0	DTMD[1:0]	00	R/W	Data Conversion Mode These bits set the format for storing RGB888 or YCbCr444 data after LUT conversion, in the external memory.*1 00: Data is not converted. 01: RGB is converted to ARGB before output. 10: YC is separated before output.*2 11: Setting prohibited.

Notes: 1. The data conversion modes that can be set are shown in Table 22.13. Do not set any other mode that is not listed in the table. RGB and YCbCr data after LUT conversion should be set as shown in Tables 22.11 and 22.12.

2. Do not set for any other data format except for YCbCr422; set YC separation only for YCbCr data format.

Table 22.10 Data Conversion Settings

- RGB Data Conversion Modes

Format of Data Stored in Memory	VnDMR/ YMODE[2:0]	VnDMR/ EXRGB	VnDMR/ DTMD[1:0]	Remarks
RGB-565 (16 bits/pixel) format	000	0	00	
RGB-888 (32 bits/pixel) format	000	1	00	
ARGB-1555 (16 bits/pixel) format	000	0	01	The alpha bit is set with the ABIT bit in VnDMR.
ARGB-8888 (32 bits/pixel) format	000	1	01	The alpha bit is set with the A8BIT bit in VnDMR.

- YCbCr Data Conversion Modes

Format of Data Stored in Memory	VnDMR/ YMODE[2:0]	VnDMR/ EXRGB	VnDMR/ DTMD[1:0]	Remarks
YCbCr-422 (8 bits) transfer	000	0	00	Set the BPSM bit in VnDMR to 1 to transfer in UYVY format in big endian.
Y (8 bits)/CbCr separation transfer	000	0	10	CbCr transfer destination is determined by the VnUVAOF register setting.
Y (8 bits) transfer	001	0	10	
Y (16 bits)/CbCr separation transfer	010/100	0	10	CbCr transfer destination is determined by the VnUVAOF register setting.
Y (16 bits) transfer	011/101	0	10	

Note: If any combination of values not listed above is specified, correct operation is not guaranteed.

22.2.23 Video n Data Mode Register 2 (VnDMR2)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FPS	VPS	HPS	CES	DES	—	—	—	CHS	YDS	—	—	—	—	FT EV	FT EH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VLV[3:0]				HLV[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FPS	0	R/W	Field Signal Polarity Select This bit specifies the polarity of the input field signal in the ITU-R BT.601 interface. 0: 0/1 = Odd field (field 1)/Even field (field 2) 1: 0/1 = Even field (field 2)/Odd field (field 1)
30	VPS	0	R/W	Vsync Signal Polarity Select This bit specifies the polarity of the input vertical sync signal in the ITU-R BT.601 interface. 0: Active low 1: Active high
29	HPS	0	R/W	Hsync Signal Polarity Select This bit specifies the polarity of the input horizontal sync signal in the ITU-R BT.601 interface. 0: Active low 1: Active high
28	CES	0	R/W	Clock Enable Signal Polarity Select This bit specifies the polarity of the input clock enable signal in the ITU-R BT.601. 0: Active high 1: Active low
27	DES	0	R/W	Data Extension Select This bit is used to select how data are expanded to 12 bits within the VIN module. 0: Empty bits in the input data are repeatedly expanded from the highest-order bit. 1: Empty bits will be padded with zeros. This bit must be set to 1 when the YCbCr-422 interface is in use.
26 to 24	—	000	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
23	CHS	0	R/W	Clock Enable Hsync Select The HSYNC signal (VIn_HSYNC#) input from the pin is internally used as the clock enable signal. 0: Clock enable signal (VIn_CLKENB) input from the pin is internally used as the clock enable signal. 1: HSYNC signal (VIn_HSYNC#) input from the pin is internally used as the clock enable signal. Note: When using ITU-R BT.601, BT.709, BT.1358 interface, and the VIn_CLKENB pin is unused, the CHS bit must be set to 1.
22	YDS	0	R/W	YCbCr422 8-bit Data Input Pin Select This bit specifies the YCbCr422 8-bit data input pins. 0: VIn_B[7:0] pins 1: VIn_G[7:0] pins Note: This bit can only be set when the YCbCr-422 interface is in use.
21 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17	FTEV	0	R/W	VSYNC Field Toggle Mode Enable The VSYNC field toggle mode changes the capture field signal level according to the count of input VSYNC signal assertion. As the VIN controls capture operation only when the input field signal level changes, select the VSYNC field toggle mode when capturing progressive images. 0: The field toggle function according to the VSYNC count is disabled. 1: The field toggle function according to the VSYNC count is enabled. The period before a toggle should be specified in the VLV bits. Note: Do not set both FTEH and FTEV at the same time.
16	FTEH	0	R/W	HSYNC Field Toggle Counter Enable 0: The field toggle function according to the capture active line is disabled. 1: The field toggle function according to the capture active line is enabled. The period before a toggle should be specified in the HLV bits. Note: Do not set both FTEH and FTEV at the same time.
15 to 12	VLV[3:0]	H'0	R/W	VSYNC Field Toggle Mode Transition Period These bits specify the count of vertical sync signal input before the VSYNC field toggle mode is entered. After a transition to the VSYNC field toggle mode, the capture field signal is toggled every time VSYNC is input. When a change in the input field signal is detected, the toggle mode is canceled. H'0: The field signal is toggled at every VSYNC input. H'1: Toggle mode is entered after VSYNC is input once. H'2: Toggle mode is entered after VSYNC is input two times. H'3: Toggle mode is entered after VSYNC is input three times. : H'E: Toggle mode is entered after VSYNC is input 14 times H'F: Toggle mode is entered after VSYNC is input 15 times. Note: If the field signal changes while the transition period is counted, the counter is initialized.

Bit	Bit Name	Initial Value	R/W	Description
11 to 0	HLV[11:0]	H'000	R/W	HSYNC Field Toggle Count Value The HSYNC field toggle counter counts the capture active lines. If the external field signal does not change before the prespecified counter value is reached, the capture field signal is toggled. H'000: The field signal is toggled for every valid line. H'001: The field signal is toggled for every single valid line. H'002: The field signal is toggled for every two valid lines. : H'FFF: The field signal is toggled for every 4095 valid lines. Note: For the period before a toggle, specify a value greater than one VSYNC period.

22.2.24 Video n UV Address Offset Register (VnUVAOF)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	UVAOF															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	UVAOF									—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	UVAOF[24:0]	All 0	R/W	UV Data Address Offset These bits specify the transfer offset address for the YC separation YCbCr-422 UV data. Specify bits 31 to 7 of the physical address in 128-byte units. Note: The specified address should be equal to or greater than the Y transfer size. Otherwise, the overwriting of Y data occurs.
6 to 0	—	All 0	R	Reserved bits that indicate the 128-byte boundary of the UVAOF value. These bits are always read as 0. The write value should always be 0.

22.2.25 YC-RGB Conversion Coefficient Registers

YC→RGB color space conversion is performed with the following formula. Each of the coefficients can be set through the registers. Here, if 8-bit data format is set, the coefficient registers set with the YMUL, CSUB, and YSUB bits in the VnCSCC1 register, RCRMU and GCRMUL bits in the VnCSCC2 register and GCBMUL and BCBMUL bits in the VnCSCC3 register are used to convert the color space. When 10-bit/12-bit data format is set, the YMUL2 bit in the VnCSCE1 register, CSUB2 and YSUB2 bits in the VnCSCE2 register, RCRMUL2 and GCRMUL2 bits in the VnCSCE3 register, GCBMUL2 and BCBMUL2 bits in the VnCSCE4 register are used in color space conversion.

$$R = \left(\begin{array}{c}VnCSCC1/\\YMUL[9:0]\\or\\VnCSCE1/\\YMUL2[13:0]\end{array}\right) \times (Y - \left(\begin{array}{c}VnCSCC1/\\YSUB[7:0]\\or\\VnCSCE1/\\YSUB2[11:0]\end{array}\right)) + \left(\begin{array}{c}VnCSCC2/\\RCRMUL[9:0]\\or\\VnCSCE3/\\RCRMUL2[13:0]\end{array}\right) \times (Cr - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right))$$

$$G = \left(\begin{array}{c}VnCSCC1/\\YMUL[9:0]\\or\\VnCSCE1/\\YMUL2[13:0]\end{array}\right) \times (Y - \left(\begin{array}{c}VnCSCC1/\\YSUB[7:0]\\or\\VnCSCE1/\\YSUB2[11:0]\end{array}\right)) - \left(\begin{array}{c}VnCSCC2/\\GCRMUL[9:0]\\or\\VnCSCE3/\\GCRMUL2[13:0]\end{array}\right) \times (Cr - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right)) - \left(\begin{array}{c}VnCSCC3/\\GCBMUL[9:0]\\or\\VnCSCE4/\\GCBMUL2[13:0]\end{array}\right) \times (Cb - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right))$$

$$B = \left(\begin{array}{c}VnCSCC1/\\YMUL[9:0]\\or\\VnCSCE1/\\YMUL2[13:0]\end{array}\right) \times (Y - \left(\begin{array}{c}VnCSCC1/\\YSUB[7:0]\\or\\VnCSCE1/\\YSUB2[11:0]\end{array}\right)) + \left(\begin{array}{c}VnCSCC3/\\BCBMUL[9:0]\\or\\VnCSCE4/\\BCBMUL2[13:0]\end{array}\right) \times (Cb - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right))$$

Note: Set the coefficients for ITU-R BT.601 (8 bits) as the initial value.

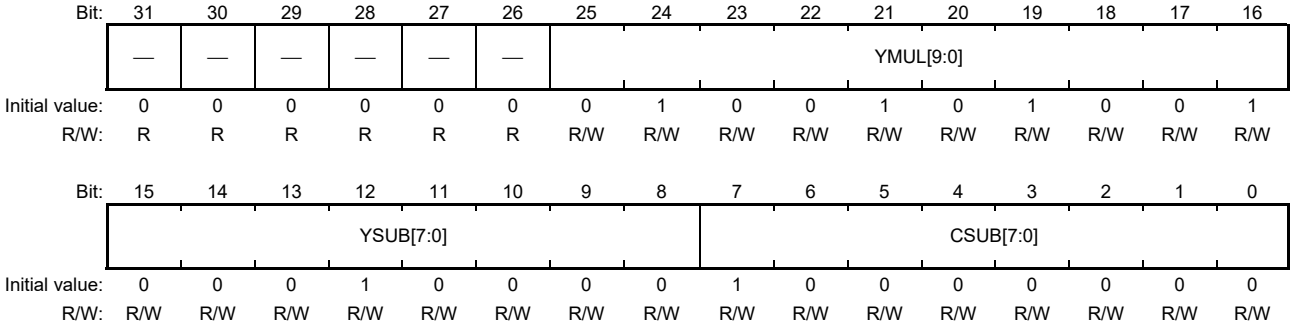
$R = 1.164 \times (Y - 16) + 1.596 \times (Cr - 128)$

$G = 1.164 \times (Y - 16) - 0.813 \times (Cr - 128) - 0.392 \times (Cb - 128)$

$B = 1.164 \times (Y - 16) + 2.017 \times (Cb - 128)$

22.2.25.1 Video n Color Space Change Coefficient 1 Register (VnCSCC1)

Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	YMUL[9:0]	H'129	R/W	Y Data Multiplication Coefficient These bits specify the multiplication coefficient for Y data in YCbCr-444 → RGB-888 color space conversion. (Initial value: 1.164) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.
15 to 8	YSUB[7:0]	H'10	R/W	Y Data Subtraction Coefficient These bits specify the subtraction coefficient for Y data in YCbCr-444 → RGB-888 color space conversion. (Initial value: H'16) Specify an unsigned 8-bit integer.
7 to 0	CSUB[7:0]	H'80	R/W	CbCr Data Subtraction Coefficient These bits specify the subtraction coefficient for Cb and Cr data in YCbCr-444 → RGB-888 color space conversion. (Initial value: H'128) Specify an unsigned 8-bit integer.

22.2.25.2 Video n Color Space Change Coefficient 2 Register (VnCSCC2)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	RCRMUL[9:0]									
Initial value:	0	0	0	0	0	0	0	1	1	0	0	1	1	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	GCRMUL[9:0]									
Initial value:	0	0	0	0	0	0	0	0	1	1	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	RCRMUL [9:0]	H'198	R/W	Cr Multiplication Coefficient for R Data Calculation These bits specify the Cr multiplication coefficient for the R data calculation equation in YCbCr-444 → RGB-888 color space conversion. (Initial value: 1.596) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	GCRMUL [9:0]	H'0D0	R/W	Cr Multiplication Coefficient for G Data Calculation These bits specify the Cr multiplication coefficient for the G data calculation equation in YCbCr-444 → RGB-888 color space conversion. (Initial value: 0.813) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.

22.2.25.3 Video n Color Space Change Coefficient 3 Register (VnCSCC3)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	GCBMUL[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	BCBMUL[9:0]									
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 16	GCBMUL [9:0]	H'064	R/W	Cb Multiplication Coefficient for G Data Calculation These bits specify the Cb multiplication coefficient for the G data calculation equation in YCbCr-444 → RGB-888 color space conversion. (Initial value: 0.392) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	BCBMUL [9:0]	H'204	R/W	Cb Multiplication Coefficient for B Data Calculation These bits specify the Cb multiplication coefficient for the B data calculation equation in YCbCr-444 → RGB-888 color space conversion. (Initial value: 2.017) Specify an unsigned 10-bit integer obtained by multiplying the desired coefficient value by 256.

22.2.25.4 Video n YC → RGB Calculation Setting Extension Register 1 (VnCSCE1)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	YMUL2[13:0]													
Initial value:	0	0	0	1	0	0	1	0	1	0	0	1	1	1	1	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	YMUL2[13:0]	H'129F	R/W	Y Multiplication Coefficient 2 for RGB Calculation These bits specify the multiplication coefficient for Y data in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 1.164) Specify an unsigned 12-bit integer obtained by multiplying the desired coefficient value by 4096.

22.2.25.5 Video n YC → RGB Calculation Setting Extension Register 2 (VnCSCE2)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	YSUB2[11:0]											
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CSUB2[11:0]											
Initial value:	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	YSUB[11:0]	H'100	R/W	Y Subtraction Coefficient 2 for RGB Calculation These bits specify the subtraction coefficient for Y data in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 256) Specify an unsigned 12-bit integer.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CSUB[11:0]	H'800	R/W	CbCr Subtraction Coefficient 2 for RGB Calculation These bits specify the subtraction coefficient for Cb and Cr data in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 2048) Specify an unsigned 12-bit integer.

22.2.25.6 Video n YC → RGB Calculation Setting Extension Register 3 (VnCSCE3)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	RCRMUL2[13:0]													
Initial value:	0	0	0	1	1	0	0	1	1	0	0	0	1	0	0	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	GCRMUL2[13:0]													
Initial value:	0	0	0	0	1	1	0	1	0	0	0	0	0	0	1	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	RCRMUL2[13:0]	H'1989	R/W	Cr Multiplication Coefficient 2 for R Calculation These bits specify the Cr multiplication coefficient for the R data calculation equation in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 1.596) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	GCRMUL2[13:0]	H'0D02	R/W	Cr Multiplication Coefficient 2 for G Calculation These bits specify the Cr multiplication coefficient for the G data calculation equation in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 0.813) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.

22.2.25.7 Video n YC → RGB Calculation Setting Extension Register 4 (VnCSCE4)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	GCBMUL2[13:0]													
Initial value:	0	0	0	0	0	1	1	0	0	1	0	0	0	1	0	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	BCBMUL2[13:0]													
Initial value:	0	0	1	0	0	0	0	0	0	1	0	0	0	1	0	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	GCBMUL2[13:0]	H'0645	R/W	Cb Multiplication Coefficient 2 for G Calculation These bits specify the Cb multiplication coefficient for the G data calculation equation in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 0.392) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	BCBMUL2[13:0]	H'2045	R/W	Cb Multiplication Coefficient 2 for B Calculation These bits specify the Cb multiplication coefficient for the B data calculation equation in YCbCr-444 → RGB-101010/RGB121212 color space conversion. (Initial value: 2.017) Specify an unsigned 14-bit integer obtained by multiplying the desired coefficient value by 4096.

22.2.26 Video n Coefficient Set Registers

The coefficient set registers specify the coefficients used for calculation of X scaling specified in XS. The X scaling function processes input pixels with 8-step resolution and generates scaled pixels by using nine calculation coefficients (nine taps) around the determined pixel.

The following is an overview of nine tap coefficients. The MSB of each coefficient is a sign bit.

Table 22.11 Bit Count for Tap Coefficients

Register Name (m = 1 to 8)	CmA			CmC			CmB		
Nine tap coefficients	L1	L2	L3	L4	M	R4	R3	R2	R1
Bit width	10	10	10	10	10	10	10	10	10

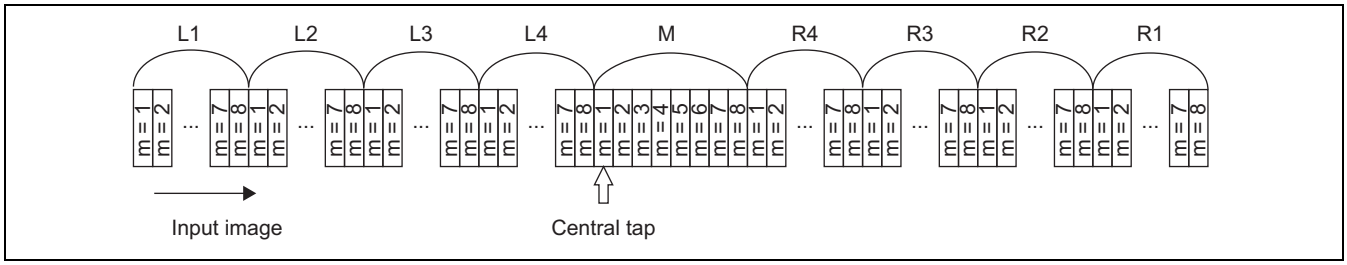
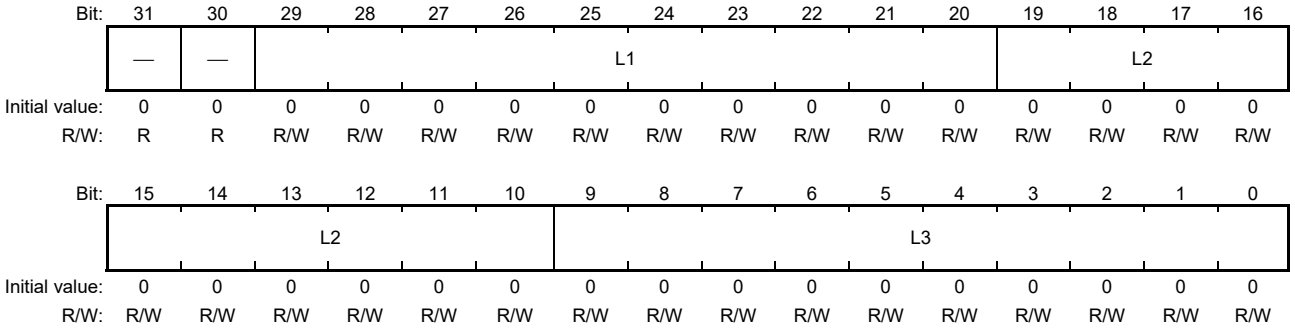


Figure 22.3 Bit Count for Tap Coefficients

22.2.26.1 Video n Coefficient Set CmA Register (VnCmA) (m = 1 to 8)

Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	L1[9:0]	H'000	R/W	L1 coefficient
19 to 10	L2[9:0]	H'000	R/W	L2 coefficient
9 to 0	L3[9:0]	H'000	R/W	L3 coefficient

22.2.26.2 Video n Coefficient Set CmB Register (VnCmB) (m = 1 to 8)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	R1										R2			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R2						R3									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	R1[9:0]	H'000	R/W	R1 coefficient
19 to 10	R2[9:0]	H'000	R/W	R2 coefficient
9 to 0	R3[9:0]	H'000	R/W	R3 coefficient

22.2.26.3 Video n Coefficient Set CmC Register (VnCmC) (m = 1 to 8)

Note: Availability of channels:
n = 0 to 1

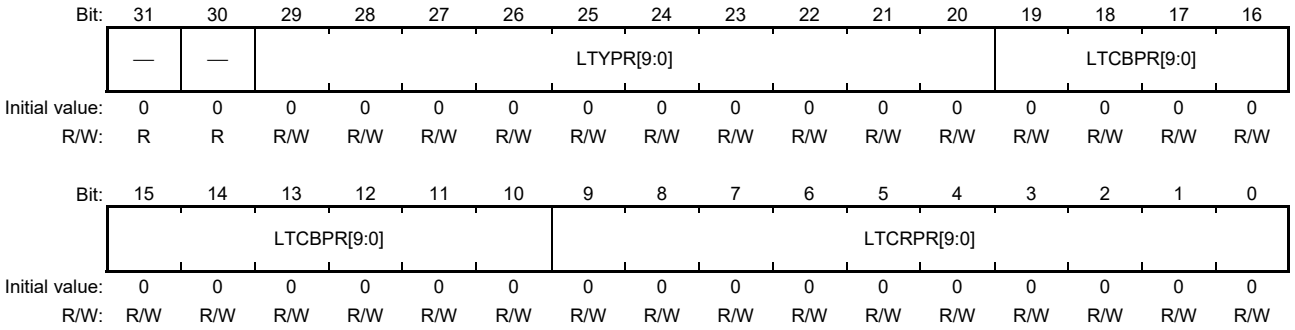
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	R4										L4			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	L4						M									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	R4[9:0]	H'000	R/W	R4 coefficient
19 to 10	L4[9:0]	H'000	R/W	L4 coefficient
9 to 0	M[9:0]	H'000	R/W	M coefficient

22.2.27 Video n Lookup Table Pointer (VnLUTP)

Note: Availability of channels:
n = 0 to 1



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 20	LTYPR[9:0]	All 0	R/W	Lookup Table Y Pointer These bits set the LUT pointer to Y and R data after color space conversion.
19 to 10	LTCBPR[9:0]	All 0	R/W	Lookup Table Cb Pointer These bits set the LUT pointer to Cb and G data after color space conversion.
9 to 0	LTCRPR[9:0]	All 0	R/W	Lookup Table Cr Pointer These bits set the LUT pointer to Cr and G data after color space conversion.

Note: Set the LUT pointer to the upper 10 bits of the 12-bit data for the color space conversion result.
The access pointer to the LUT will be automatically incremented by writing to the VnLUTD register.
There will be no automatic increment at read access.

22.2.28 Video n Lookup Table Data Register (VnLUTD)

Note: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	LTYDT[7:0]							
Initial value:	0	0	0	0	0	0	0	0	x	x	x	x	x	x	x	x
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LTCBDT[7:0]								LTCRDT[7:0]							
Initial value:	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x	x
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	LTYDT[7:0]	H'x	R/W	Lookup Table Y Data These bits set the LUT conversion data for Y and R data after color space conversion.
15 to 8	LTCBDT[7:0]	H'x	R/W	Lookup Table Cb Data These bits set the LUT conversion data for Cb and G data after color space conversion.
7 to 0	LTCRDT[7:0]	H'x	R/W	Lookup Table Cr Data These bits set the LUT conversion data for Cr and B data after color space conversion.

Note: The 8-bit data after LUT conversion is subjected to upper shift to carry out capture control as 12-bit data.
As for reading from the VnLUTD register, the data read the second time, including dummy read, after the VnLUTP register has been set is valid.

22.2.29 RGB-YC Conversion Coefficient Registers

Color space conversion from RGB to YC is done with the following formula. Each of the coefficients can be set with the registers.

$$Y = YCLRP \times R + YCLGP \times G + YCLBP \times B + YCLAP$$
$$Cb = CBCLRP \times R + CBCLGP \times G + CBCLBP \times B + CBCLAP$$
$$Cr = YCLRP \times R + YCLGP \times G + YCLBP \times B + YCLAP$$

Note: Set the coefficients for ITU-R BT.601 (8 bits) as the initial value.

$$Y = 0.257 \times R + 0.504 \times G + 0.098 \times B + 16$$
$$Cb = -0.148 \times R - 0.291 \times G + 0.439 \times B + 128$$
$$Cr = 0.439 \times R - 0.368 \times G - 0.071 \times B + 128$$

22.2.29.1 Video n RGB → YC Calculation Setting Register 1 (VnYCCR1)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLRP[12:0]												
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	1	1	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YCLRP[12:0]	H'0107	R/W	R Multiplication Coefficient for Y Calculation These bits specify the R multiplication coefficient for the Y data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: 263) The MSB is a sign bit.

22.2.29.2 Video n RGB → YC Calculation Setting Register 2 (VnYCCR2)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	YCLBP[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	1	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YCLGP[12:0]												
Initial value:	0	0	0	0	0	0	1	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	YCLBP[12:0]	H'0064	R/W	B Multiplication Coefficient for Y Calculation These bits specify the B multiplication coefficient for the Y data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: 100) The MSB is a sign bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YCLGP[12:0]	H'0204	R/W	G Multiplication Coefficient for Y Calculation These bits specify the G multiplication coefficient for the Y data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: 516) The MSB is a sign bit.

22.2.29.3 Video n RGB → YC Calculation Setting Register 3 (VnYCCR3)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	YEXPEN	—	—	YCLSFT[4:0]					YCLHEN	—	—	—	—	—	—	YCLCEN
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	YCLAP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	YEXPEN	0	R/W	Y Calculation Sign Extension Enable This bit controls the sign extension for Y data calculation in RGB888 → YCbCr444 color space conversion. 0: Disables YC conversion sign bit. 1: Enables YC conversion sign bit.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	YCLSFT[4:0]	H'0A	R/W	Y Calculation Shift Down Volume These bits set the amount of down shift for Y calculation in RGB888 → YCbCr444 color space conversion (Initial value: 10) Unit: Bit shift count
23	YCLHEN	0	R/W	Y Calculation Shift Down Result Round-Off Enable This bit enables round-off process for Y data calculation in RGB888 → YCbCr444 color space conversion 0: Round down to down shift process 1: Round-off to down shift process is enabled.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	YCLCEN	0	R/W	Y Calculation Data Clip Enable This bit enables data clipping process for Y data calculation in RGB888 → YCbCr444 color space conversion. 0: Data clipping process is disabled. 1: Data clipping process is enabled.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	YCLAP[11:0]	H'010	R/W	Y Calculation Data Normalized Additional Value These bits set the Y data addition constant for RGB888 → YCbCr444 color space conversion. (Initial value: 16)

22.2.29.4 Video n RGB → Cb Calculation Setting Register 1 (VnCBCCR1)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLRP[12:0]												
Initial value:	0	0	0	1	1	1	1	1	0	1	1	0	1	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CBCLRP[12:0]	H'1F68	R/W	R Multiplication Coefficient for Cb Calculation These bits specify the R multiplication coefficient for the Cb data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: -152) The MSB is a sign bit.

22.2.29.5 Video n RGB → Cb Calculation Setting Register 2 (VnCBCCR2)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBCLBP[12:0]												
Initial value:	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CBCLGP[12:0]												
Initial value:	0	0	0	1	1	1	1	0	1	1	0	1	0	1	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	CBCLBP[12:0]	H'01C2	R/W	B Multiplication Coefficient for Cb Calculation These bits specify the B multiplication coefficient for the Cb data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: 450) The MSB is a sign bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CBCLGP[12:0]	H'1ED6	R/W	G Multiplication Coefficient for Cb Calculation These bits specify the B multiplication coefficient for the Cb data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: -298) The MSB is a sign bit.

22.2.29.6 Video n RGB → Cb Calculation Setting Register 3 (VnCBCCR3)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBEXPEN	—	—	CBCLSFT[4:0]					CBCLHEN	—	—	—	—	—	—	CBCLCEN
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CBCLAP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CBEXPEN	0	R/W	Cb Calculation Sign Extension Enable This bit controls the sign extension for Cb data calculation in RGB888→YCbCr444 color space conversion. 0: Disables YC conversion sign bit. 1: Enables YC conversion sign bit.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	CBCLSFT[4:0]	H'0A	R/W	Cb Calculation Shift Down Volume These bits set the amount of down shift for Cb calculation in RGB888 → YCbCr444 color space conversion (Initial value: 10) Unit: Bit shift count
23	CBCLHEN	0	R/W	Cb Calculation Shift Down Result Round-Off Enable This bit enables round-off process for Cb data calculation in RGB888 → YCbCr444 color space conversion 0: Round down to down shift process 1: Round-off to down shift process is enabled.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CBCLCEN	0	R/W	Cb Calculation Data Clip Enable This bit enables data clipping process for Cb data calculation in RGB888 → YCbCr444 color space conversion. 0: Data clipping process is disabled. 1: Data clipping process is enabled.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CBCLAP[11:0]	H'080	R/W	Cb Calculation Data Normalized Additional Value These bits set the Cb data addition constant for RGB888 → YCbCr444 color space conversion. (Initial value: 128)

22.2.29.7 Video n RGB → Cr Calculation Setting Register 1 (VnCRCCR1)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLRP[12:0]												
Initial value:	0	0	0	0	0	0	0	1	1	1	0	0	0	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CRCLRP[12:0]	H'01C2	R/W	R Multiplication Coefficient for Cr Calculation These bits specify the R multiplication coefficient for the Cr data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: 450) The MSB is a sign bit.

22.2.29.8 Video n RGB → Cr Calculation Setting Register 2 (VnCRCCR2)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CRCLBP[12:0]												
Initial value:	0	0	0	1	1	1	1	1	1	0	1	1	0	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CRCLGP[12:0]												
Initial value:	0	0	0	1	1	1	1	0	1	0	0	0	0	1	1	1
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	CRCLBP[12:0]	H'1FB7	R/W	B Multiplication Coefficient for Cr Calculation These bits specify the B multiplication coefficient for the Cr data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: -73) The MSB is a sign bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CRCLGP[12:0]	H'1E87	R/W	G Multiplication Coefficient for Cr Calculation These bits specify the B multiplication coefficient for the Cr data calculation equation in RGB-888 → YCbCr-444 color space conversion. (Initial value: -377) The MSB is a sign bit.

22.2.29.9 Video n RGB → Cr Calculation Setting Register 3 (VnCRCCR3)

Note: Availability of channels:
n = 0 only

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CREXPEN	—	—	CRCLSFT[4:0]					CRCLHEN	—	—	—	—	—	—	CRCLCEN
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CRCLAP[11:0]											
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CREXPEN	0	R/W	Cr Calculation Sign Extension Enable This bit controls the sign extension for Cr data calculation in RGB888 → YCbCr444 color space conversion. 0: Disables YC conversion sign bit. 1: Enables YC conversion sign bit.
30, 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	CRCLSFT[4:0]	H'0A	R/W	Cr Calculation Shift Down Volume These bits set the amount of down shift for Cr calculation in RGB888 → YCbCr444 color space conversion (Initial value: 10) Unit: Bit shift count
23	CRCLHEN	0	R/W	Cr Calculation Shift Down Result Round-Off Enable This bit enables round-off process for Cr data calculation in RGB888 → YCbCr444 color space conversion 0: Round down to down shift process 1: Round-off to down shift process is enabled.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CRCLCEN	0	R/W	Cr Calculation Data Clip Enable This bit enables data clipping process for Cr data calculation in RGB888 → YCbCr444 color space conversion. 0: Data clipping process is disabled. 1: Data clipping process is enabled.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CRCLAP[11:0]	H'080	R/W	Cr Calculation Data Normalized Additional Value These bits set the Cr data addition constant for RGB888 → YCbCr444 color space conversion. (Initial value: 128)

22.2.30 Video n Memory Transfer Control Register (VnMTC)

Notes: Availability of channels:
n = 0 to 1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	PRIH[3:0]				—	—	—	—	PRIL[3:0]			
Initial value:	0	0	0	0	1	0	1	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SIZE	—	—	—	—	BSIZE[3:0]			
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 24	PRIH[3:0]	H'A	R/W	Priority High Level Value Setting These bits specify priority high level for second packet from VIN I/F. Please do not change value from H'A.
23 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19 to 16	PRIL[3:0]	H'8	R/W	Priority Low Level Value Setting. These bits specify priority low level for first packet from VIN I/F. H'8: normal priority H'9: high priority than other VIN channel. Set these bits to H'9 on high bit rate channel when a system input video data more than two channel.
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	SIZE	1	R/W	Transaction Size Unit setting. 0: 16-Byte unit 1: 32-Byte unit (default) These bits set the LUT conversion data for Cr and B data after color space conversion.
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	BSIZE[3:0]	H'8	R/W	Burst Size Setting These bits specify VIN's burst transaction size. When bit SIZE is set to 0: H'0: No transfer (prohibited) H'1: 16-Byte H'2: 32-Byte … H'F: 240-Byte When bit SIZE is set to 1: H'0: No transfer (prohibited) H'1: 32-Byte H'2: 64-Byte (recommended setting) … H'8: 256-Byte (default) … H'F: 480-Byte (prohibited) Set these bits to specify burst size less than 256-Byte. SIZE = 1, BSIZE[3:0] = H'2 is recommended setting to consider VIN capture stability.

22.3 Operation

22.3.1 Input Interface

The VIN captures video data in the ITU-R BT.601, ITU-R BT.656, ITU-R BT.1358, or ITU-R BT.709 interface and stores it in external memory. The module has four input-interface channels. The interface and data format can be set as desired for each video channel.

The following tables show the interface and data format supported in each product and its channels.

Note: When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.

Table 22.12 Video Channels and Supported Interfaces

				Channel 0	Channel 1
Input interface	ITU-R BT.656	YCbCr-422	8 bits	Supported	Supported
			10 bits	Supported	Supported
			12 bits	Supported	Supported
	ITU-R BT.1358/ ITU-R BT.601/ ITU-R BT.709	YCbCr-422	16 bits	Supported	—
			20 bits	Supported	—
			24 bits	Supported	—
	ITU-R BT.601/ ITU-R BT.709	YCbCr-422	8 bits	Supported	Supported
			10 bits	Supported	Supported
			12 bits	Supported	Supported
		RGB-666	18 bits	Supported	—
		RGB-888	24 bits	Supported	—
Output interface	RGB output	RGB-565	16 bits	Supported	Supported
		ARGB-1555	16 bits	Supported	Supported
		RGB-888	32 bits	Supported	Supported
		ARGB-8888	32 bits	Supported	Supported
	YCbCr output	YCbCr-422 multiplexed	8 bits	Supported	Supported
		YCbCr-422 separated Y/CbCr	Y: 8 bits CbCr: 8 bits	Supported	Supported
			Y: 10 bits CbCr: 8 bits	Supported	Supported
			Y: 12 bits CbCr: 8 bits	Supported	Supported
		YCbCr-422 separated Only Y	8 bits	Supported	Supported
			10 bits	Supported	Supported
			12 bits	Supported	Supported

Notes: 1. When capturing progressive images, be sure to enable the internal field signal generation function.
2. Dithering is performed for RGB-888→RGB-565 conversion.
3. RGB data is converted and transferred to memory from the video module after 8-bit precision conversion.
4. For details of output interfaces, see section 22.3.10, Output Data Format.

(1) Multiplexed YCbCr-422 Data Format in ITU-R BT.601 Interface

Data in the multiplexed YCbCr-422 format is a UYVY format (U0Y0V0Y1 format) YCbCr data. The Y, Cb, Cr image data is captured at the rising edges of the input video clock signal.

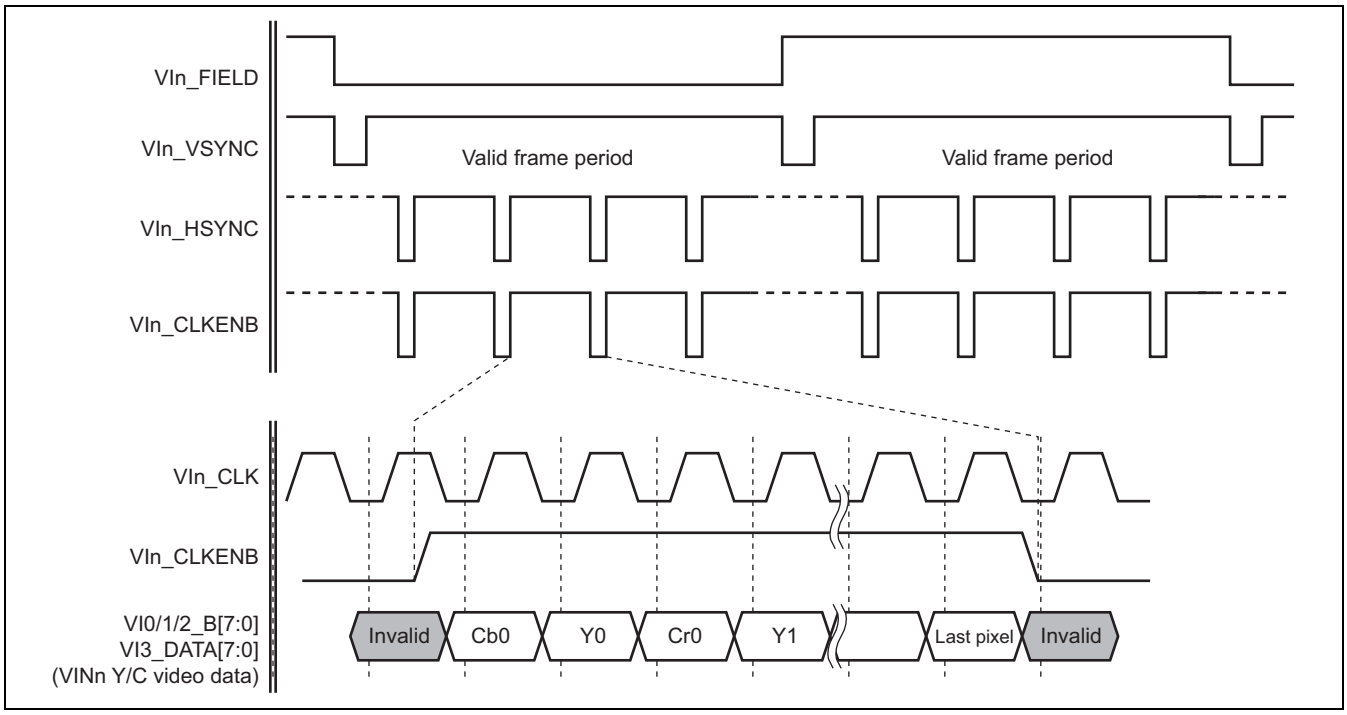


Figure 22.4 Multiplexed YCbCr-422 Data Format

(2) CbCr Multiplexed YCbCr-422 Data Format in ITU-R BT.601/1358 Interface

Data in the CbCr multiplexed YCbCr-422 format is YCbCr data with only the CbCr data being multiplexed. The Y and CbCr image data are captured at the rising edges of the input video clock signal.

Setting the YCAL bit in VnMC to 1 enables the capturing of image data with CbCr data in the upper bits and Y data in the lower bits.

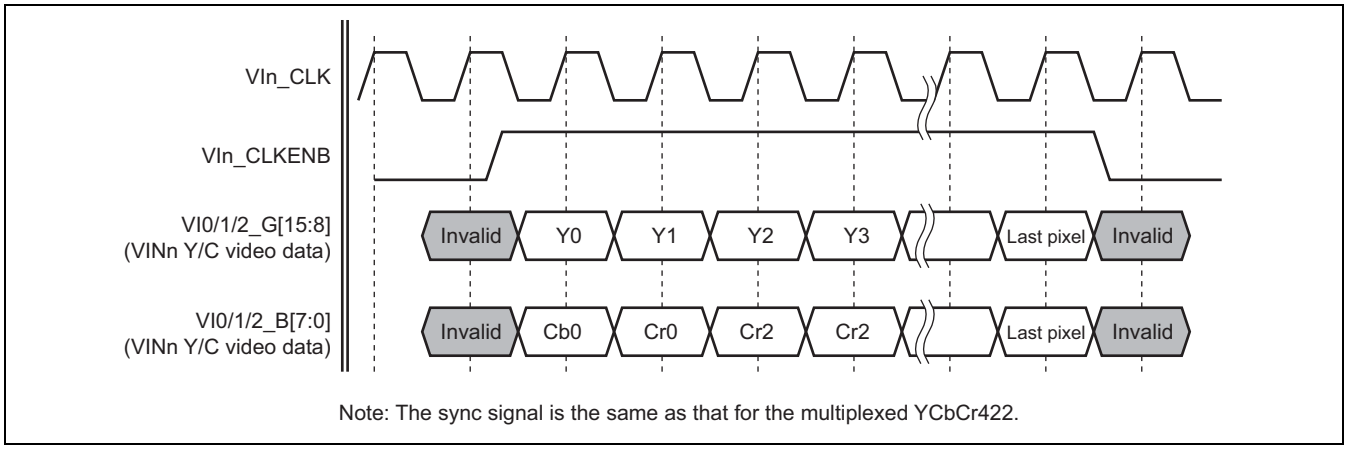


Figure 22.5 CbCr Multiplexed YCbCr-422 Data Format (Y Data in Upper Bits)

(3) RGB-666 Data Format in ITU-R BT.601 Interface

This data format can be used for the color conversion space in the RGB=4:4:4 format defined in the ITU-R BT.601 standard. The R, G, B image data are captured at the rising edges of the input video clock signal.

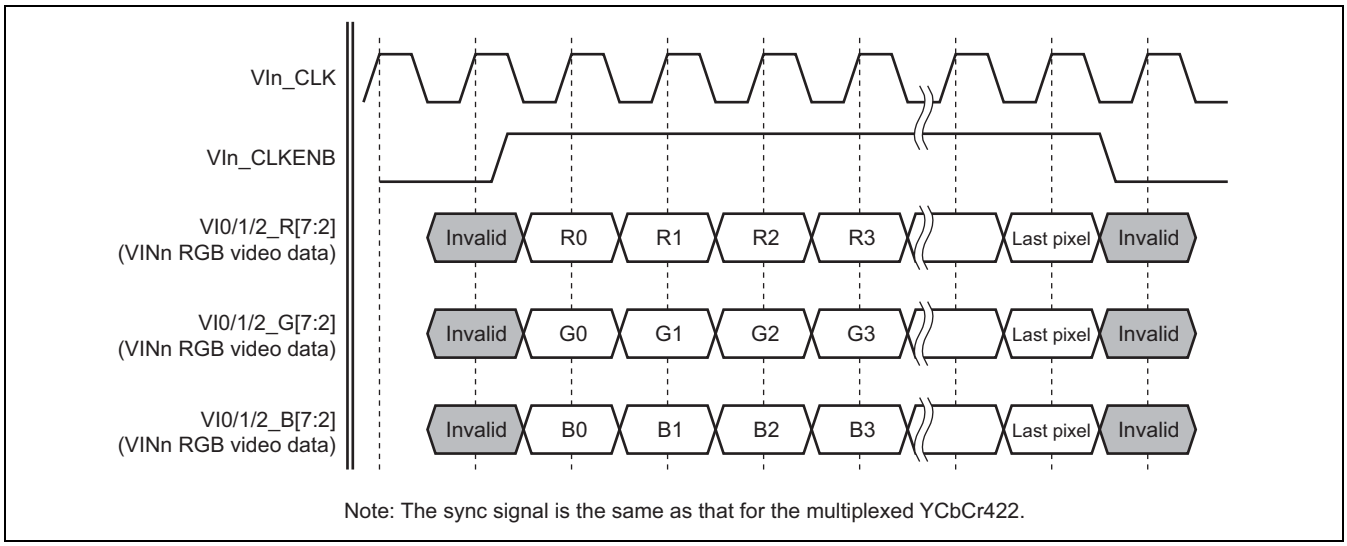


Figure 22.6 RGB-666 Data Format

(4) RGB-888 (24 bits) Data Format in ITU-R BT.601 Interface

This data format can be used for the color conversion space in the RGB=4:4:4 format defined in the ITU-R BT.601. The R, G, B image data are captured at the rising edges of the input video clock signal.

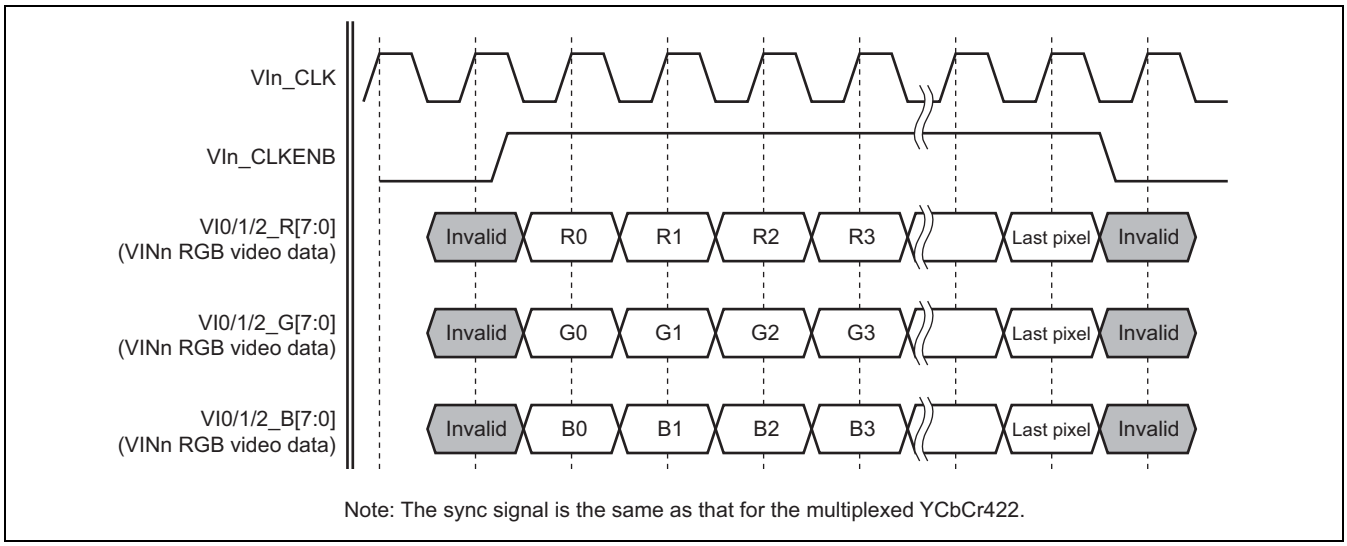


Figure 22.7 RGB-888 (24 Bits) Data Format

(5) Multiplexed YCbCr-422 Data Format in ITU-R BT.656 Interface

In the ITU-R BT.656 interface, active data between the start of active video (SAV) and the end of active video (EAV) indicated with the timing reference code is captured.

Table 22.13 Video Timing Reference Code

VINn Image Data			First Word	Second Word	Third Word	Fourth Word (XY)	
12 bits	10 bits	8 bits					
VIn_G[3]	VIn_G[1]	VIn_B[7]	1	0	0	1	
VIn_G[2]	VIn_G[0]	VIn_B[6]	1	0	0	F	0: Field 1 1: Field 2
VIn_G[1]	VIn_B[7]	VIn_B[5]	1	0	0	V	0: elsewhere 1: Field Blanking
VIn_G[0]	VIn_B[6]	VIn_B[4]	1	0	0	H	0: SAV 1: EAV
VIn_B[7]	VIn_B[5]	VIn_B[3]	1	0	0	P3	Protection bit 3
VIn_B[6]	VIn_B[4]	VIn_B[2]	1	0	0	P2	Protection bit 2
VIn_B[5]	VIn_B[3]	VIn_B[1]	1	0	0	P1	Protection bit 1
VIn_B[4]	VIn_B[2]	VIn_B[0]	1	0	0	P0	Protection bit 0
VIn_B[3]	VIn_B[1]	—	1	0	0	0	
VIn_B[2]	VIn_B[0]	—	1	0	0	0	
VIn_B[1]	—	—	1	0	0	0	
VIn_B[0]	—	—	1	0	0	0	

Active data is available with the multiplexed YCbCr-422 data format in the UYVY (U0Y0V0Y1) format. In this interface, timing reference and Y, Cb, Cr image data are captured at the rising edges of the input clock signal.

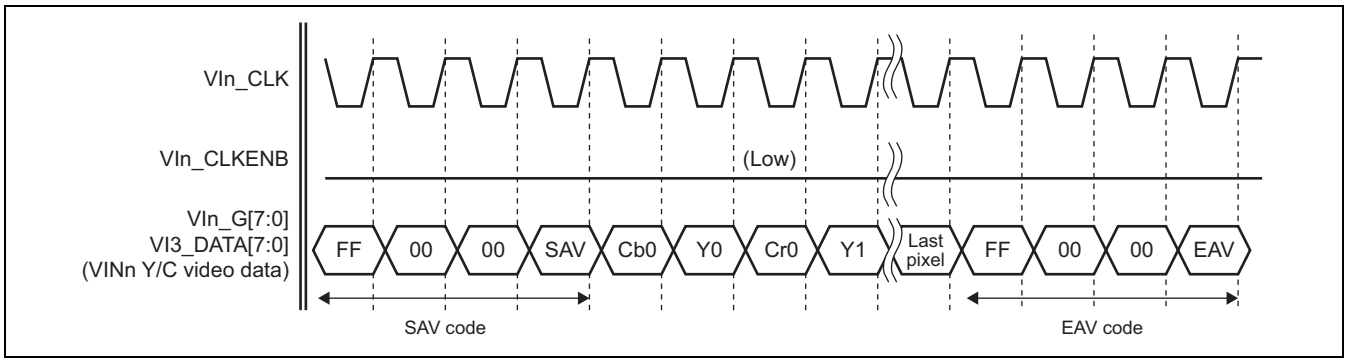


Figure 22.8 Multiplexed YCbCr-422 Data Format

Capturing is controlled based on field information. Therefore, the field signal and timing reference codes should be correct.

22.3.2 Error Correction

At the time of capturing with ITU-R BT.656, the VIN allows errors to be corrected with the timing reference code (SAV/EAV). The timing reference code (SAV/EAV) of ITU-R BT.656 has four protection bits, which can be used to correct only one-bit errors in the interface.

If the VIN cannot correct errors while the CEE bit in the interrupt enable register (VnIE) has been set to 1, an interrupt signal is generated as soon as the CES bit in the interrupt status (VnINTS) register is set. Note that no interrupt signal is generated if errors can be corrected.

22.3.3 Capture Mode

With the VIN, either of the single frame capture mode or continuous frame capture mode can be selected.

Specifying the capture field in IM bits of the main control (VnMC) register and then setting the SC bit in the frame capture (VnFC) register to 1 provides single frame capture mode. In this mode, the current frame is captured when the SC bit write timing (current scanline position) is smaller than the value of the start line pre-clip (VnSLPrC) register, or the next frame is captured in other cases. The capture data is transferred to the memory address that is set in the memory base 1 (VnMB1) register.

Specifying the capture field in IM bits of VnMC and then setting the CC bit of VnFC to 1 provides continuous frame capture mode, in which capture data is sequentially transferred to the addresses that are set in MB1 to MB3. In this case, the latest captured frame ID is shown in the FBS bits in the module status (VnMS) register.

When the IM bits in VnMC are set to the full interlace mode, data in the capture start field is stored in every other line in the memory as the odd field (field 1) data and then data in the next field is stored as the even field (field 2) between the written lines so that the top and bottom field lines alternate with each other for interlace composition. The capture start field (top field) can be changed through the FOC bit in VnMC.

The following is a schematic diagram of capturing in full interlace mode when the odd field (field 1) is selected as the top field, the memory width is set to H'200, and VnMB1 is set to H'0000.

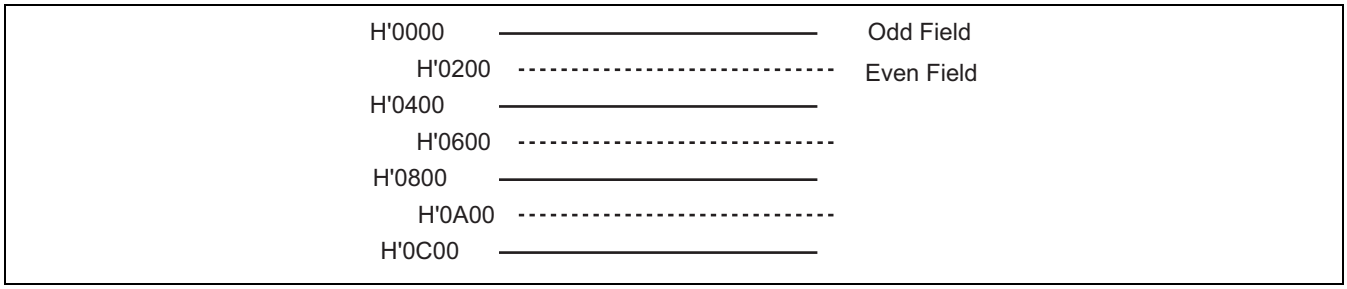


Figure 22.9 Example of Capturing Full Interlace

The VIN starts capture operation after detecting a frame signal switching in the ITU-R BT.601 or 656 interface. When capturing progressive data, in which the field signal does not change, use the internal field signal generation function to toggle the internal field signal.

22.3.4 Size Clipping

Image data that has been captured is pre-clipped according to the settings of the following registers: start line pre-clip (VnSLPrC), end line pre-clip (VnELPrC), start pixel pre-clip (VnSPPrC), and end pixel pre-clip (VnEPPrC).

After the horizontal and vertical scaling, post-clipping takes place according to the settings of the following registers: start line post-clip (VnSLPoC), end line post-clip (VnELPoC), start pixel post-clip (VnSPPoC), and end pixel post-clip (VnEPPoC). The following shows an example of size clipping.

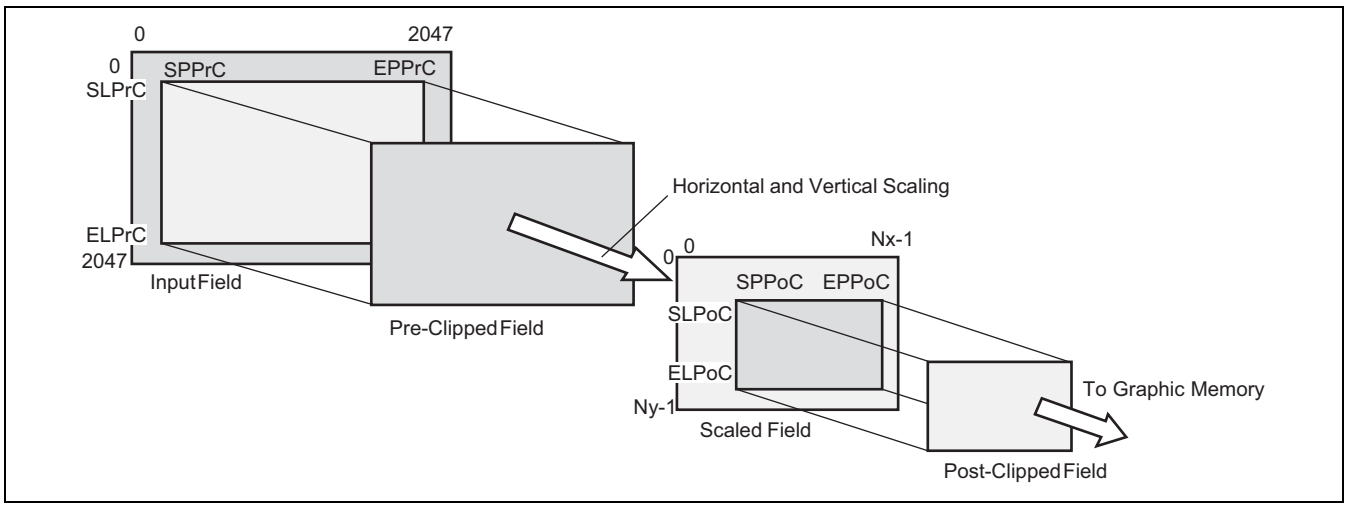


Figure 22.10 Example of Clipping

For all the post-clipped lines, the lengths of individual lines written into the memory are defined by the image stride (VnIS) register. The setting can be larger than the post-clipped frame width, but cannot be smaller than the width. The VnIS register must be filled with a value larger than the horizontal post-clipping width. The input field in the above figure shows an effective image area from the video decoder; the VIN does not allow anything exceeding the image area to be captured.

Note: Each of the following registers specifies a distance from the starting point in the effective image area: start line pre-clip (VnSLPrC), end line pre-clip (VnELPrC), start pixel pre-clip (VnSPPrC), and end pixel pre-clip (VnEPPrC). Specifically, in ITU-R BT.601, the distance is from the starting point of VIn_CLKENB (data enable); in ITU-R BT.656, the distance is from the SAV (start of active video) signal.

22.3.5 Vertical Scaling

The vertical scaling function in the VIN creates lines by scaling up or down in the vertical direction through interpolation between two points in the neighborhood of captured lines. With the combinations of mantissaY and fractionY in the Y scaling (VnYS) register, the vertical scaling creates new lines by selecting line positions from captured lines.

The Y scaling function is disabled if mantissaY and fractionY are both cleared to 0 in VnYS.

Scaling down is implemented by creating fewer lines than captured lines. Examples of scaling up and down are shown in the following figure.

Note: When vertical scaling up is specified in full interlace capture mode, the scaling-up processing is applied separately to each field before full interlace composition on memory. Accordingly, the top and bottom field lines are inverted in some cases depending on the scaling ratio. Be sure to evaluate the scaled image quality before practical application.

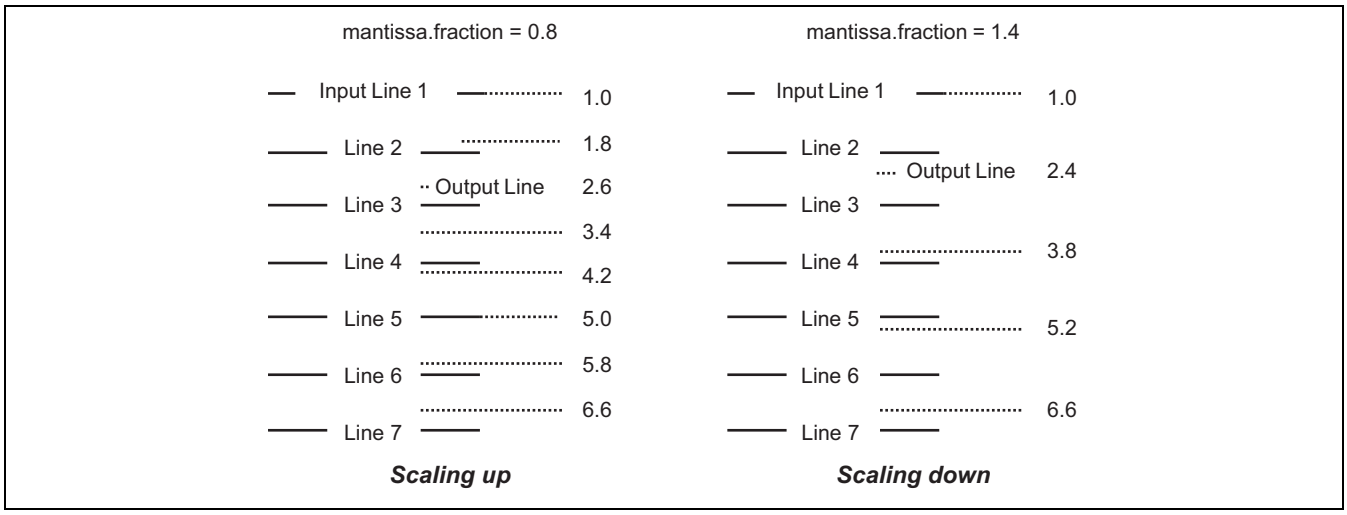


Figure 22.11 Examples of Scaling Up and Down in Vertical Direction

The number of lines created by the vertical scaling block is expressed by the following equation:

$$Ny = \begin{cases} \dfrac{4096 \times (ELPrC - SLPrC)}{4096 \times MantissaY + FractionY} - 1, \\ \qquad \text{when } \{4096 \times (ELPrC - SLPrC)\}\%(4096 \times MantissaY + FractionY) = 0 \\ Int\left(\dfrac{4096 \times (ELPrC - SLPrC)}{4096 \times MantissaY + FractionY}\right), \text{ otherwise} \end{cases}$$

where:
ELPrC is the value in the end line pre-clip (VnELPrC) register.
SLPrC is the value in the start line pre-clip (VnSLPrC) register.
MantissaY and FractionY are the values in VnYS.

22.3.6 Horizontal Scaling

Using a 9-tap multiphase filter, the VIN creates pixels by scaling down in the horizontal direction. The horizontal scaling-up doubles the number of input pixels captured and provides the function of expansion of up to two-fold by the scaling-down in the 9-tap multiphase filter. The horizontal scaling, which is set through combinations of mantissaX and fractionX in the X scale (VnXS) register, determines the position of new pixels with a poly-phase filter. The selected coefficient, which is one of the eight coefficients, is determined by the position of output pixels.

In the example shown below, mantissaX and fractionX are set at 1.2. In this case, coefficient set C2 is selected.

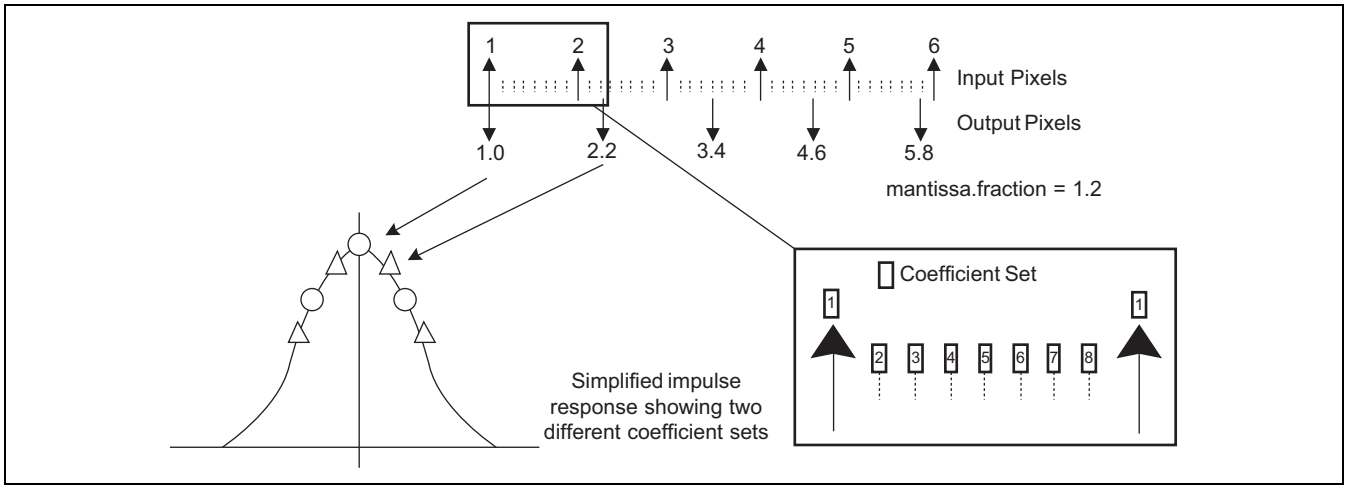


Figure 22.12 Pixel Position and Coefficient Set

The following figure shows an example in which different coefficient sets are used for different output pixel positions. Nine coefficient sets are assigned to each. A total of 72 coefficients are used in the horizontal scaling. Each of the coefficients in these sets has a width of 10 bits, where the MSB serves as the sign bit. By setting the same coefficients into the entire eight coefficient set registers, the horizontal scaling allows the use of a multiphase filter just like a single-phase filter.

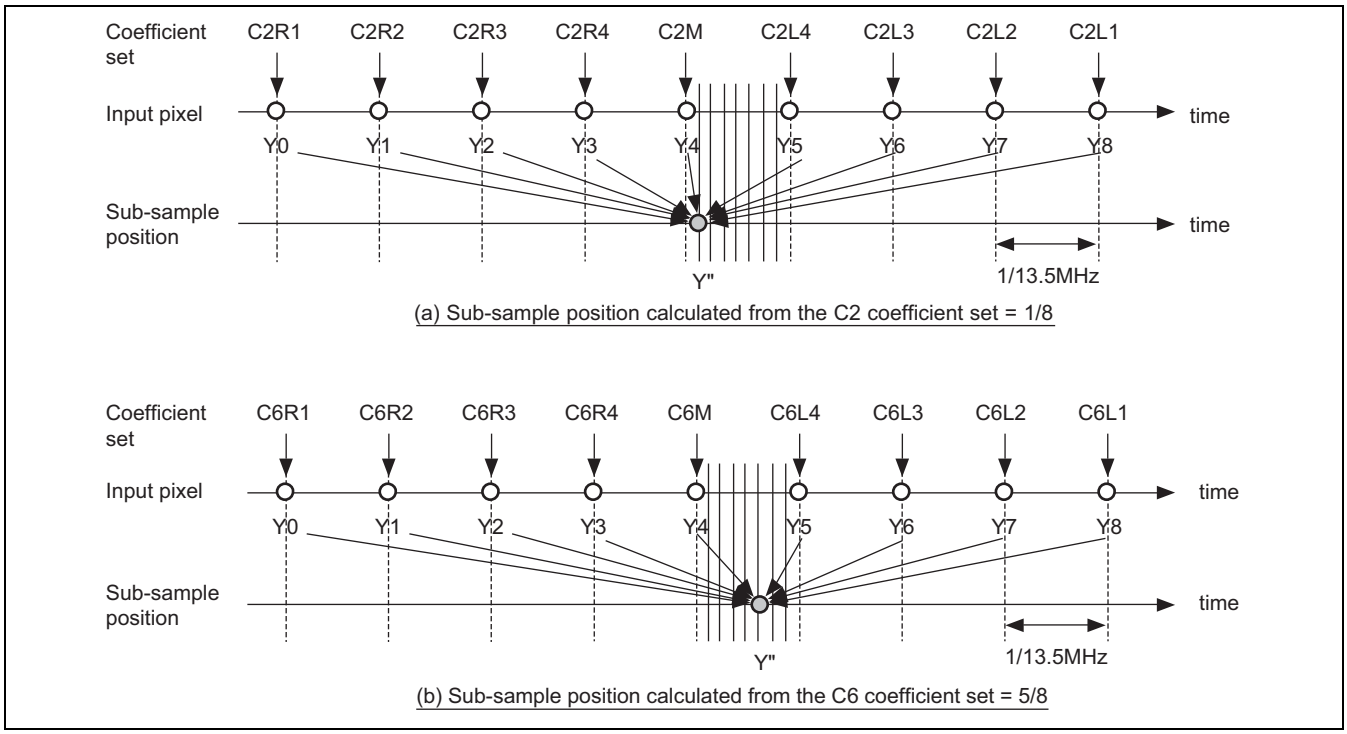


Figure 22.13 Example of Coefficients in Selected Coefficient Set

This scaling mechanism requires different coefficient values dependent on the scaling ratio. Here is an example of coefficient sets to be selected. The coefficients, CmM, CmLi, and CmRi (m = 1, 2, 3, - - -, 8; i = 1, 2, 3, and 4), are determined by the following equations:

$$C_nM = \beta \times h(-(n-1))$$

$$C_nRi = \beta \times h(-(n-1) - 8(5-i))$$

$$C_nLi = \beta \times h(-(n-1) + 8(5-i))$$

$$h(t) = \frac{\sin\left(\frac{\pi t}{T}\right)}{\frac{\pi t}{T}} \times \frac{\cos\left(\frac{\alpha\pi t}{T}\right)}{1 - \frac{4\alpha^2 t^2}{T^2}}$$

$$T = 8 \times MantissaX + FractionX\ [11:9]$$

Mantissa X and Fraction X are the values in VnXS.

The parameter β is a standardized one. In the equation, h(t) follows the cosine characteristic and is executed with a 9-tap filter if the value of α is in the $0 < \alpha \leq 1$ range.

Obtaining dependable scale images requires you to use and meet the following equation in which all the coefficient sets are standardized.

This must be executed with the inherent β value that has been selected from the equation above.

$$CnM + \sum_{i=1}^{4} CnRi + \sum_{i=1}^{4} CnLi = 512$$

The number of pixels created by the horizontal scaling block is calculated by the following equation.

$$Nx = Int\left(\frac{4096 \times (EPPrC - SPPrC)}{4096 \times MantissaX + FractionX}\right) + 1$$

where:
EPPrC is the value in the end pixel pre-clip (VnEPPrC) register.
SPPrC is the value in the start pixel pre-clip (VnSPPrC) register.
Mantissa X and Fraction X are the values in VnXS.

22.3.7 Color Conversion Function

(1) YC-RGB Color Conversion

When the data input format is YCbCr, set the BPS bit in the VnMC register to 0 to convert YCbCr data to RGB data. If an 8-bit data format is used for the capture interface, the color conversion is carried out according to the matrix coefficients set in the VnCSCC1, VnCSCC2, and VnCSCC3 registers. Otherwise, it is carried out according to the matrix coefficients set in the VnCSCE1, VnCSCE2, VnCSCE3, and VnCSCE4 registers. All of the input YCbCr data is extended to 12-bit data before carrying out color conversion.

Here, if the BPS bit in VnMC is set to 1, the data is stored in memory as it is in YCbCr format.

$$R = \left(\begin{array}{c}VnCSCC1/\\YMUL[9:0]\\or\\VnCSCE1/\\YMUL2[13:0]\end{array}\right) \times \left(Y - \left(\begin{array}{c}VnCSCC1/\\YSUB[7:0]\\or\\VnCSCE1/\\YSUB2[11:0]\end{array}\right)\right) + \left(\begin{array}{c}VnCSCC2/\\RCRMUL[9:0]\\or\\VnCSCE3/\\RCRMUL2[13:0]\end{array}\right) \times \left(Cr - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right)\right)$$

$$G = \left(\begin{array}{c}VnCSCC1/\\YMUL[9:0]\\or\\VnCSCE1/\\YMUL2[13:0]\end{array}\right) \times \left(Y - \left(\begin{array}{c}VnCSCC1/\\YSUB[7:0]\\or\\VnCSCE1/\\YSUB2[11:0]\end{array}\right)\right) - \left(\begin{array}{c}VnCSCC2/\\GCRMUL[9:0]\\or\\VnCSCE3/\\GCRMUL2[13:0]\end{array}\right) \times \left(Cr - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right)\right) - \left(\begin{array}{c}VnCSCC3/\\GCBMUL[9:0]\\or\\VnCSCE4/\\GCBMUL2[13:0]\end{array}\right) \times \left(Cb - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right)\right)$$

$$B = \left(\begin{array}{c}VnCSCC1/\\YMUL[9:0]\\or\\VnCSCE1/\\YMUL2[13:0]\end{array}\right) \times \left(Y - \left(\begin{array}{c}VnCSCC1/\\YSUB[7:0]\\or\\VnCSCE1/\\YSUB2[11:0]\end{array}\right)\right) + \left(\begin{array}{c}VnCSCC3/\\BCBMUL[9:0]\\or\\VnCSCE4/\\BCBMUL2[13:0]\end{array}\right) \times \left(Cb - \left(\begin{array}{c}VnCSCC1/\\CSUB[7:0]\\or\\VnCSCE1/\\CSUB2[11:0]\end{array}\right)\right)$$

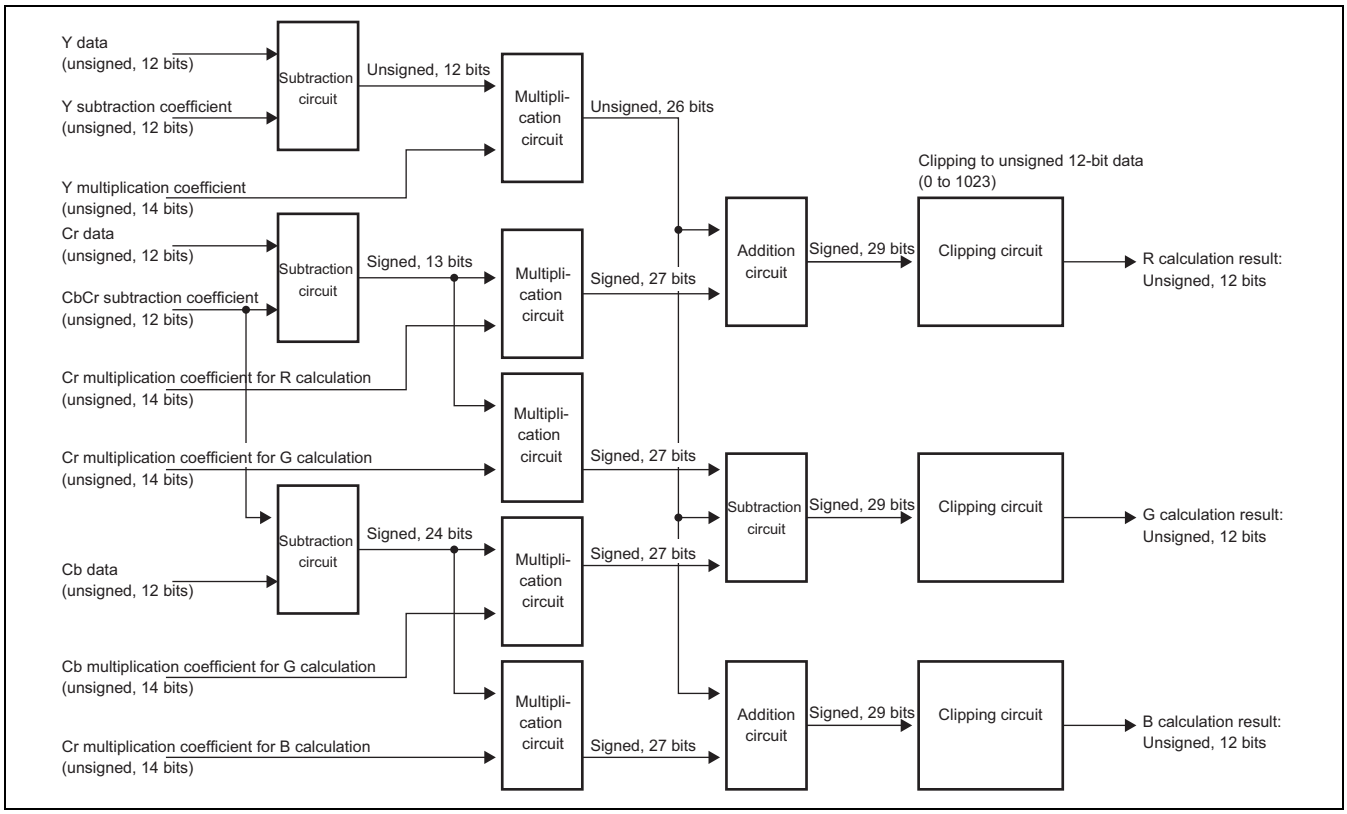


Figure 22.14 YCbCr → RGB Calculation Circuit Configuration

Examples of color space that can be set in YC-RGB conversion coefficient registers are shown below. See the register descriptions for details of the coefficients.

Table 22.14 Examples of YC-RGB Conversion Coefficient Register Settings

YC-RGB Conversion Coefficient	YMUL	YSUB	CSUB	RCRMUL	GCRMUL	GCBMUL	BCBMUL
ITU-R BT.601 (initial value) 16 ≤ Y ≤ 235, 16 ≤ Cb, Cr ≤ 240	1.164	16	128	1.596	0.813	0.392	2.017
Luminance expansion example 1 ≤ Y ≤ 254, 16 ≤ Cb, Cr ≤ 240	1.008	1	128	1.596	0.392	0.813	2.017

Specify an integer in each addition coefficient bit field. For each multiplication coefficient, specify a value obtained by multiplying the desired coefficient value by 256.

Example: When the desired multiplication coefficient is 1.164

$1.164 \times 256 = 297$ (set value: B'0100101001)

Notes: 1. In order to process the data outside the range prescribed by the ITU-R BT.601 standard, set the CLP[1:0] bits in VnMC to 11. The data is clipped to the specified value before color space conversion.
2. The YC-RGB color conversion data is unconditionally rounded to the 0 ≤ R, G, B ≤ 255 range.

(2) RGB-YC Color Conversion

When the data input format is RGB, set the BPS bit in VnMC to 0 for color conversion of RGB data into YCbCr data format. Color conversion from RGB to YCbCr is done according to the matrix coefficients set in RGB-YC conversion coefficient registers (VnYCCR1-VnYCCR3/VnCBCCR1-VnCBCCR3/VnCRCCR1-VnCRCCR3). All of the input RGB data is extended to 12-bit data before color conversion.

If 1 is set to the BPS bit in VnMC, the data will be stored in the memory as it is in RGB format.

$$Y = ((YCLRP \times R + YCLGP \times G + YCLGP \times B) \times 2^{YCLSFT}) + YCALP$$
$$Cb = ((CBCLRP \times R + CBCLGP \times G + CBCLGP \times B) \times 2^{CBCLSFT}) + CBCALP$$
$$Cr = ((CRCLRP \times R + CRCLGP \times G + CRCLGP \times B) \times 2^{CRCLSFT}) + CRCALP$$

The following data rounding functions of RGB-YCbCr color conversion function can be independently set to each pixel. The circuit configuration of Y data is given below.

Table 22.15 Data Rounding Functions of RGB-YC Color Conversion Function

Function	Symbol	Description
Sign extension enable	YEXPEN	Enables/disables signed bits of the matrix multiplication result.
Multiplication result shift down amount	YCLSFT[4:0]	Amount of shift down in the matrix multiplication result
Rounding off enable	YCLHEN	Enables/disables rounding off to the shift down amount.
Clipping enable	YCLCEN	Enables/disables data rounding process between 0 to 1023 of the output data.

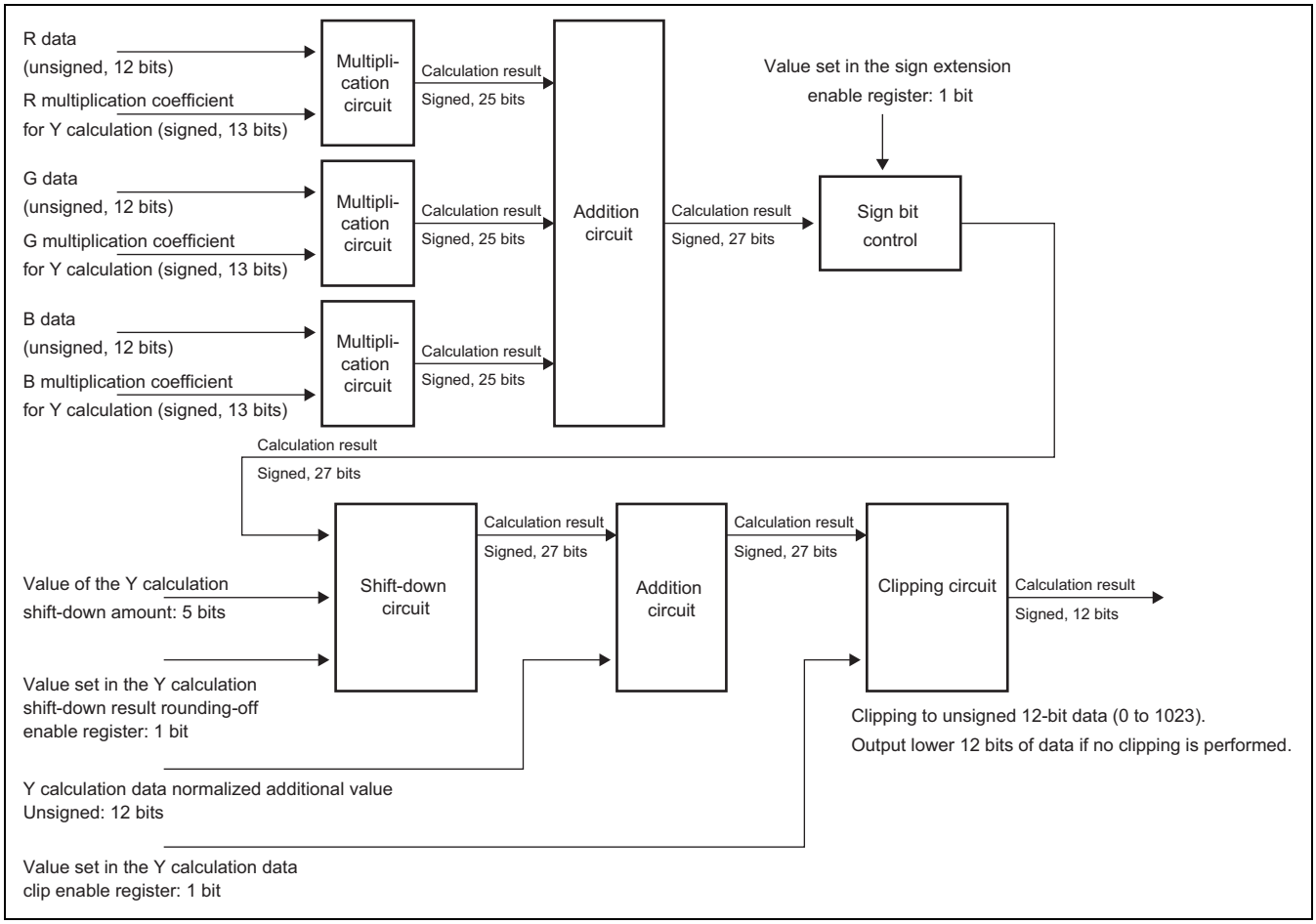


Figure 22.15 Y Data Circuit Configuration of RGB → YCbCr Color Conversion Function

22.3.8 Image Data Format Conversion Functions

(1) Lookup Table (LUT) Density Conversion Function

Set the LUTE bit in VnMC to 1 to enable table conversion of each pixel data of Y, Cb, Cr and R, G, B data after color conversion.

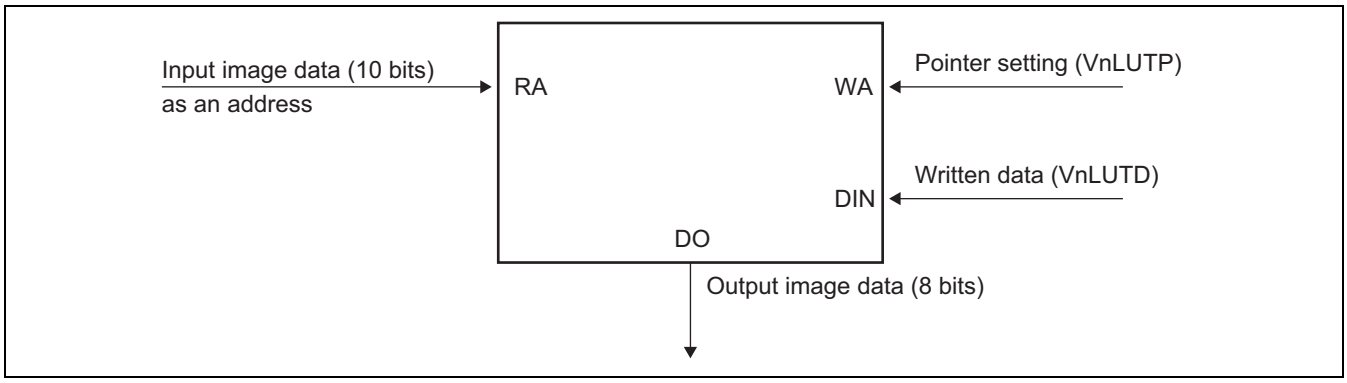


Figure 22.16 Lookup Table

Pointer Access:

The pointer is incremented every time a write access to the VnLUTD register is made.

The incremented data is read when the VnLUTP register is read. Since data is not incremented at read access, the pointer should be set just before reading.

The procedure given below must be followed to access the lookup table.

The lookup table cannot be accessed from the CPU during the conversion process.

(For write/read access to the LUT from the CPU, the LUTE bit in VnMC should be 0.)

Write access:

1. Write the access destination address in VnLUTP.
2. Write the data in VnLUTD.
   Thereby the data will be reflected in the lookup table.
   Also the pointer will automatically increase by 1.
3. Writing to VnLUTD will consecutively update the lookup table.

Read Access:

1. Write the access destination address in VnLUTP.
2. Read VnLUTD. This is dummy read; thus the read data needs to be discarded.
3. Read VnLUTD. This reading allows the address data written in VnLUTP to be acquired.

[Notes on Using the Lookup Table]

1. Set the lookup table only after capture operation has stopped.
2. Rewrite all before using the lookup table.
3. Data set to the lookup table should be within the range compatible to the input bit width.

(2) YCbCr444 → YC Separation Function

When transferring YCbCr data to memory, Y data and CbCr data can be separated and transferred to different address spaces.

To perform YCbCr separation transfer, set the DTMD[1:0] bits in the VnDMR register to B'10. In this case, the Y data will be transferred to the address set in the memory base address register and CbCr data will be transferred to the address obtained by adding the value set in the VnUVAOF register to the memory base address register.

If the YMODE[2:0] bits in the VnDMR register are set, only Y data will be transferred to memory and CbCr data is not transferred to memory.

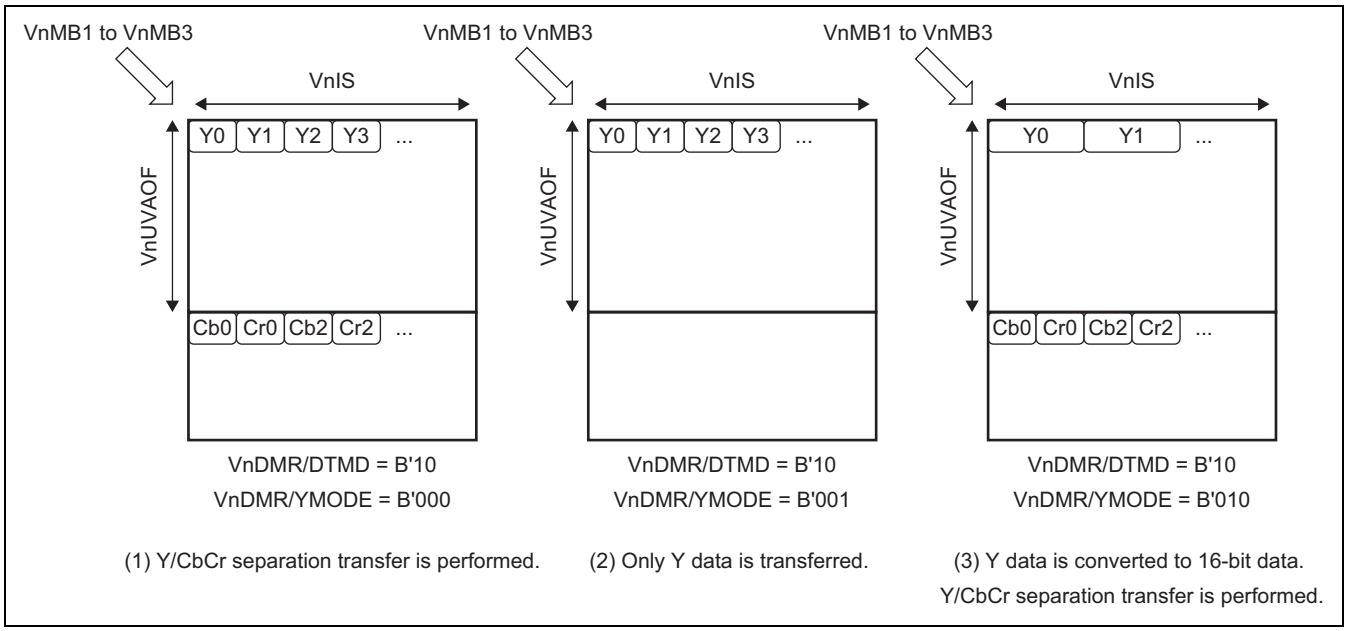


Figure 22.17 Y/Cb/Cr Separation in Big Endian

(3) Dithering Function

Dithering is performed when the internal RGB-888 format after color space conversion is converted to the RGB-565 or RGB-1555 format. The dithering mode can be selected with the DC[1:0] bits in VnMC.

(a) Dithering with Cumulative Addition

Set the DC[1:0] bits in VnMC to B'00 to perform dithering using the cumulative addition method in horizontal pixel units.

$$R_n\,[7:3] \leq (R_x[7:0]) + R_{n-1}[2:0]) >> 3$$
$$G_n\,[7:2] \leq (G_x[7:0]) + G_{n-1}[1:0]) >> 2$$
$$B_n\,[7:3] \leq (B_x[7:0]) + B_{n-1}[2:0]) >> 3$$

Where:
(R_n, G_n, B_n) = Output RGB-565 pixel
(R_x, G_x, B_x) = Input RGB-888 pixel
(R_{n-1}, G_{n-1}, B_{n-1}) = Pseudo random error (LSB of the cumulative error)

(b) Ordered Dithering

Set the DC[1:0] bits in VnMC to B'01 to perform dithering using the ordered dithering method.

$$R_n\,[7:3] \leq (R_x[7:0]) + D\,42_{xy}) >> 3$$
$$G_n\,[7:2] \leq (G_x[7:0]) + D\,22_{xy}) >> 2$$
$$B_n\,[7:3] \leq (B_x[7:0]) + D\,42_{xy}) >> 3$$

Where:
(R_n, G_n, B_n) = Output RGB-565 pixel
(R_x, G_x, B_x) = Input RGB-888 pixel
($D22_{xy}$, $D42_{xy}$) = Input x, y coordinate dithering matrix result

$$D22 = \begin{bmatrix} 0 & 3 \\ 2 & 1 \end{bmatrix}, D42 = \begin{bmatrix} 0 & 3 & 4 & 7 \\ 2 & 1 & 6 & 5 \end{bmatrix}$$

22.3.9 Internal Field Signal Generation

As the video input module controls capture of data in interlaced mode, correct capture control is not achieved if the external field signal level does not change.

Through the internal field signal generation function, the VIN can control the capture field signal even when the input field signal does not change, such as during progressive data capturing. The following settings can be made for the internal field generation function through the FTEV and FTEH bits in the data mode register 2 (VnDMR2).

- VSYNC field toggle mode (FTEV = 1 in VnDMR2)
  When this setting is made, the VSYNC field toggle mode is entered for capture field signal control if the input field signal does not change for the VSYNC cycles specified by the VLV bits in VnDMR2. The toggle mode is canceled when a change in the external field signal level is detected (the capture operation is controlled according to the input field signal).
- HSYNC field toggle counter (FTEH = 1 in VnDMR2)
  This counter counts the capture active lines. If the external field signal does not change until the count reaches the HLV setting in VnDMR2, the capture field signal is controlled.

Notes: 1. Do not set both the FTEV and FTEH bits in VnDMR2 at the same time.
2. Immediately after cancellation of the toggle mode, capture control is skipped for one VSYNC cycle in some cases depending on the input field signal state.

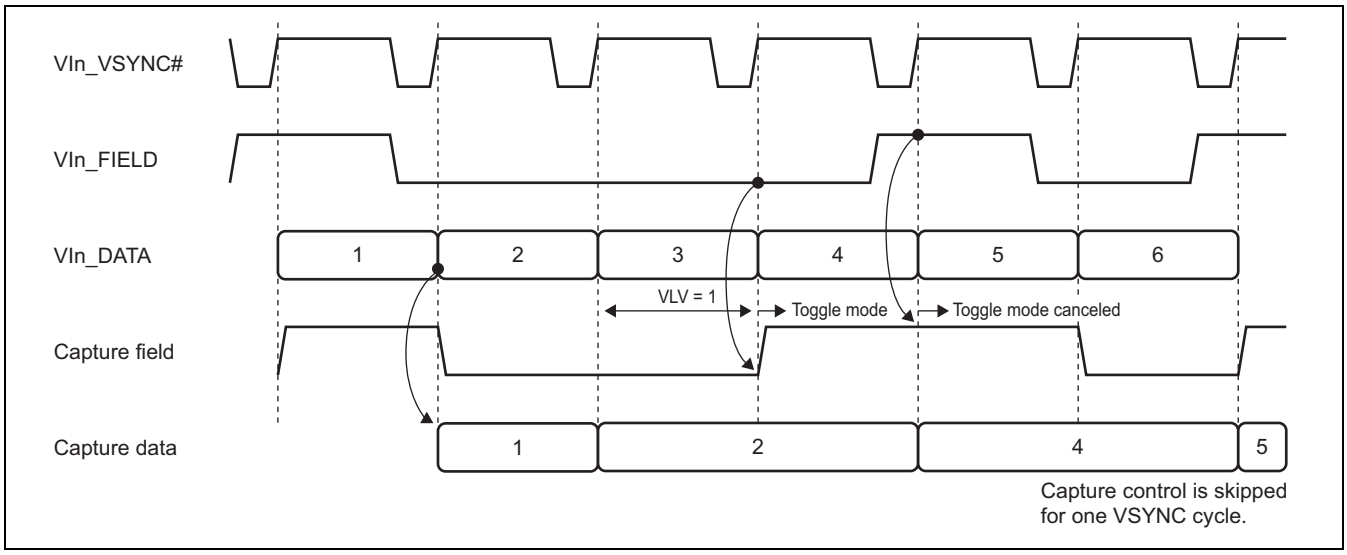


Figure 22.18 Overview and Notes of VSYNC Field Toggle Mode

22.3.10 Output Data Format

The VIN can output image data in the following formats. The figures in this section assume that data is stored in unified memory in little endian.

(1) YC: YCbCr-422, 8 bits

The 8-bit YUV image data in the YC (YCbCr) = 4:2:2 format is shown below. YC data can be switched between the UYVY format and YUYV format through the BPSM bit in VnDMR.

- BPSM = 0 in VnDMR: UYVY format

8-bit YCbCr-422 data (UYVY format)

	63	56	55	48
D63 to D48				
Image data 3 and 4	Y3[7:0]		Cr2[7:0]	
D47 to D32	47	40	39	32
Image data 3 and 4	Y2[7:0]		Cb2[7:0]	
D31 to D16	31	24	23	16
Image data 1 and 2	Y1[7:0]		Cr0[7:0]	
D15 to D0	15	8	7	0
Image data 1 and 2	Y0[7:0]		Cb0[7:0]	

- BPSM = 1 in VnDMR: YUYV format

8-bit YCbCr-422 data (YUYV format)

	63	56	55	48
D63 to D48				
Image data 3 and 4	Cr2[7:0]		Y3[7:0]	
D47 to D32	47	40	39	32
Image data 3 and 4	Cb2[7:0]		Y2[7:0]	
D31 to D16	31	24	23	16
Image data 1 and 2	Cr0[7:0]		Y1[7:0]	
D15 to D0	15	8	7	0
Image data 1 and 2	Cb0[7:0]		Y0[7:0]	

(2) YC: YC Separation YCbCr-422, 8 bits

This is 8-bit YUV image data in the YC separated YC (YCbCr) = 4:2:2 format. UV data is supported by the NV12 format only.

If the YMODE[2:0] bits in the data mode register (VnDMR) are set to B'000 or B'001, setting the DTMD[1:0] bits in VnDMR to B'10 changes the format to 4:2:2 and transfers the UV data to an address which is specified by the addition of the value set in the UV address offset register (VnUVAOF) to the Memory Base. If the YMODE[2:0] bits in VnDMR are set to B'001, only Y data can be transferred and UV data cannot be transferred.

Y data

D31 to D16	31	24	23	16
Image data 3 and 4	Y3[7:0]		Y2[7:0]	

D15 to D0	15	8	7	0
Image data 1 and 2	Y1[7:0]		Y0[7:0]	

Cb, Cr data

D31 to D16	31	24	23	16
Image data 3 and 4	Cr2[7:0]		Cb2[7:0]	

D15 to D0	15	8	7	0
Image data 1 and 2	Cr0[7:0]		Cb0[7:0]	

(3) YC: YC Separation YCbCr-422, 10 bits

This is 10-bit YUV image data in the YC separated YC (YCbCr) = 4:2:2 format. UV data is supported by the NV12 format only.

If the YMODE[2:0] bits in the data mode register (VnDMR) are set to B'010 or B'011, setting the DTMD[1:0] bits in VnDMR to B'10 converts 10-bit Y data to 16-bit and changes the format to 4:2:2. UV data is transferred to the address obtained by adding the value set in the UV address offset register (VnUVAOF) to Memory Base. If the YMODE[2:0] bits in VnDMR are set to B'011, only Y data can be transferred and UV data cannot be transferred.

Notes: 1. A word address is output for Y data according to the VnIS register setting.
2. A byte address is output for CbCr data according to the VnIS register setting.

Y data

D31 to D16	31					26	25									16
Image data 3 and 4	0	0	0	0	0	0	Y1[9:0]									

D15 to D0	15					10	9									0
Image data 1 and 2	0	0	0	0	0	0	Y0[9:0]									

Cb, Cr data

D31 to D16	31								24	23							16
Image data 3 and 4	Cr2[7:0]									Cb2[7:0]							

D15 to D0	15								8	7							0
Image data 1 and 2	Cr0[7:0]									Cb0[7:0]							

(4) YC: YC Separation YCbCr-422, 12 bits

This is 12-bit YUV image data in the YC separated YC (YCbCr) = 4:2:2 format. UV data is supported by the NV12 format only.

If the YMODE[2:0] bits in the data mode register (VnDMR) are set to B'100 or B'101, setting the DTMD[1:0] bits in VnDMR to B'10 converts 12-bit Y data to 16-bit and changes the format to 4:2:2. UV data is transferred to the address obtained by adding the value set in the UV address offset register (VnUVAOF) to Memory Base. If the YMODE[2:0] bits in VnDMR are set to B'101, only Y data can be transferred and UV data cannot be transferred.

Notes: 1. A word address is output for Y data according to the VnIS register setting.
2. A byte address is output for CbCr data according to the VnIS register setting.

Y data

D31 to D16	31			28	27											16
Image data 3 and 4	0	0	0	0	Y1[11:0]											

D15 to D0	15			12	11											0
Image data 1 and 2	0	0	0	0	Y0[11:0]											

Cb, Cr data

D31 to D16	31							24	23							16
Image data 3 and 4	Cr2[7:0]								Cb2[7:0]							

D15 to D0	15							8	7							0
Image data 1 and 2	Cr0[7:0]								Cb0[7:0]							

(5) 16 Bits/Pixel: RGB-565

The RGB levels are expressed through 5 bits for R, 6 bits for G, and 5 bits for B.

16 bits/pixel data (RGB data) format

D15 to D0	15				11	10				5	4				0
Image data	R[4:0]					G[5:0]					B[4:0]				

(6) 16 Bits/Pixel: ARGB-1555

The ARGB levels are expressed through 1 bit for A, 5 bits for R, 5 bits for G, and 5 bits for B. For data conversion to ARGB-1555, the lowest bit of the G data in RGB-565 data is truncated, and the A value specified through the register is added.

Set the DTMD[1:0] bits in the data mode register (VnDMR) to B'01 to specify conversion to ARGB-1555, and specify the A value in the ABIT bit in VnDMR.

16 bits/pixel data (ARGB data) format

D15 to D0	15	14				10	9				5	4				0
Image data	A	R[4:0]					G[4:0]					B[4:0]				

(7) 32 Bits/Pixel: RGB-888

The RGB levels are expressed through 8 bits for R, 8 bits for G, and 8 bits for B. Bits 31 to 24 are fixed to 0.

32 bits/pixel data (RGB data) format

D31 to D16	31							24	23							16
Image data	0	0	0	0	0	0	0	0	R[7:0]							

D15 to D0	15							8	7							0
Image data	G[7:0]								B[7:0]							

(8) 32 Bits/Pixel: ARGB-8888

The ARGB levels are expressed through 8 bits for A, 8 bits for R, 8 bits for G, and 8 bits for B. The A value specified by the A8BIT[7:0] bits in VnDMR is set in bits 31 to 24.

32 bits/pixel data (ARGB data) format

D31 to D16	31							24	23							16
Image data	A[7:0]								R[7:0]							

D15 to D0	15							8	7							0
Image data	G[7:0]								B[7:0]							

22.3.11 Endian Conversion

The VIN stores captured data in memory in little endian with the initial settings. Set the EN bit in the main control register (VnMC) to 1 to convert data into big endian before storing in memory.

Endian conversion in word units is controlled through the EN bit in VnMC, and swapping in byte units is controlled through the BPSM bit in the data mode register (VnDMR). For conversion to big endian, specify the BPSM bit as shown in the following table according to the data format specified through the DTMD bits in VnDMR and BPS bit in VnMC.

Table 22.16 Endian Conversion Unit

Data Format	BPS in VnMC	DTMD[1:0] in VnDMR	EXRGB in VnDMR	BPSM in VnDMR	Endian Conversion Unit
RGB-565	0	00	0	0	Word units
RGB-888	0	00	1	0	Longword units
YCbCr-422	1	00	0	1	Byte units
ARGB-1555	0	01	0	0	Word units
ARGB-8888	0	01	1	0	Longword units
YC	1	10	0	0	Byte units

The following figures show endian conversions in byte, word, and longword units.

Endian conversion in byte units:

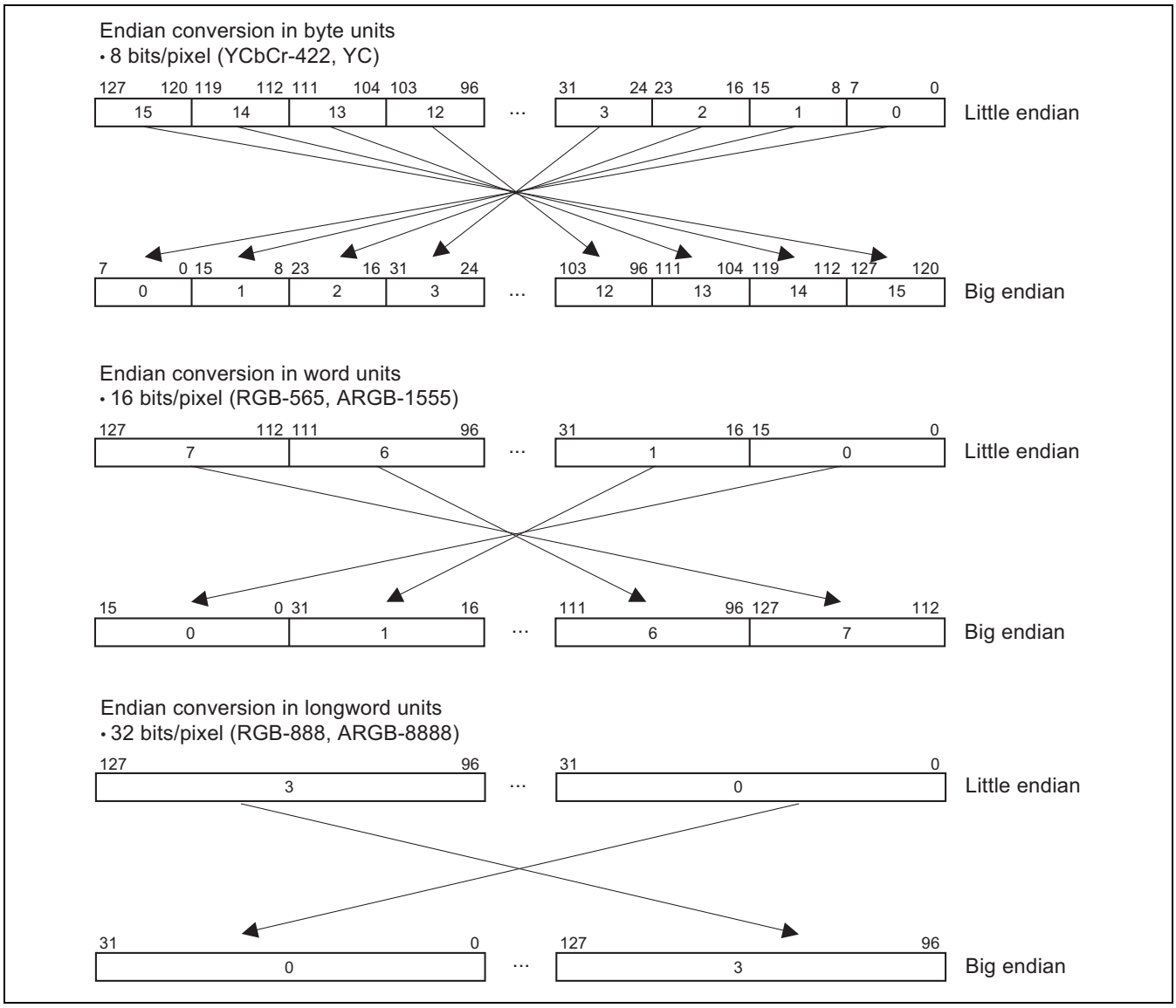


Figure 22.19 Data Alignment Conversion from Little Endian to Big Endian

22.4 Usage Notes

22.4.1 Module Standby Mode

The LSI supports module standby mode in which clock supply to the VIN is stopped. The video input module should not be accessed during module standby mode.

22.4.2 Transition to Module Standby Mode

1. Clear the module enable (ME) bit in the main control register (VnMC) and the continuous frame capture (CC) bit and the single frame capture (SC) bit in the frame capture register (VnFC) to 0 to stop the video input module.
2. Confirm that the capture active (CA) bit in the module status register (VnMS) is cleared to 0.
3. Stop the clock supply.

22.4.3 Cancellation of Module Standby Mode and Restarting of Video Input Module

1. Start the clock supply.
2. Set the module enable (ME) bit in the main control register (VnMC) to 1 to start the video input module.
3. Set the continuous frame capture (CC) bit or the single frame capture (SC) bit in the frame capture register (VnFC) to 1.

22.4.4 Limitations on Usage

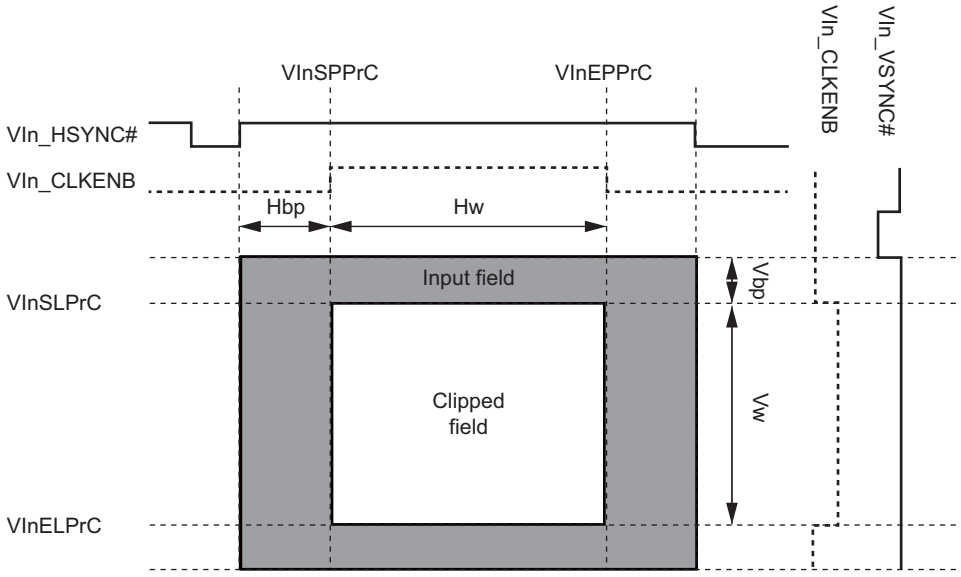
The VIN does not operate correctly in some cases depending on the usage. The following shows cases that require attention.

Table 22.17 Limitations on Usage

<table>
<tr><th>Item</th><th>Description</th></tr>
<tr><td>Limits on input video clock</td><td>The upper limit on frequency of the input video clock varies with the clock mode, capture interface and scaling ratio. The upper limits on frequency of the video clock for this module as a stand-alone unit are shown below. Usage of other modules may make reaching the upper limits impossible. Fully evaluate performance before deciding on the settings for the input video clock, particularly if you are using magnification.
Upper limits on video-clock frequency for this module as a stand-alone unit
<table>
<tr><th rowspan="2">Capture Mode</th><th rowspan="2">Horizontal Scaling Ratio XS</th><th rowspan="2">VnMC. FAST Mode</th><th colspan="3">Vertical Scaling Ratio YS</th></tr>
<tr><th>0.0 ≤ YS ≤ 1.0</th><th>1.0 < YS ≤ 2.0</th><th>2.0 < YS ≤ 3.0</th></tr>
<tr><td rowspan="4">ITU-R BT.601, YCbCr-422, 8 bits
ITU-R BT.656, YCbCr-422, 8 bits</td><td rowspan="2">0.0 ≤ XS ≤ 1.0</td><td>1</td><td>100 MHz</td><td>Setting prohibited</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>80 MHz</td><td>80 MHz</td><td>80 MHz</td></tr>
<tr><td rowspan="2">1.0 < XS ≤ 2.0</td><td>1</td><td>Setting prohibited</td><td>Setting prohibited</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>70 MHz</td><td>70 MHz</td><td>50 MHz</td></tr>
<tr><td rowspan="4">ITU-R BT.1358, YCbCr-422, 16 bits</td><td rowspan="2">0.0 ≤ XS ≤ 1.0</td><td>1</td><td>100 MHz</td><td>Setting prohibited</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>60 MHz</td><td>60 MHz</td><td>60 MHz</td></tr>
<tr><td rowspan="2">1.0 < XS ≤ 2.0</td><td>1</td><td>Setting prohibited</td><td>Setting prohibited</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>30 MHz</td><td>30 MHz</td><td>20 MHz</td></tr>
<tr><td rowspan="4">ITU-R BT.601, RGB-888, 12 bits
ITU-R BT.601, RGB-666, 18 bits
ITU-R BT.601, RGB-888, 24 bits</td><td rowspan="2">0.0 ≤ XS ≤ 1.0</td><td>1</td><td>100 MHz</td><td>Setting prohibited</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>80 MHz</td><td>80 MHz</td><td>60 MHz</td></tr>
<tr><td rowspan="2">1.0 < XS ≤ 2.0</td><td>1</td><td>Setting prohibited</td><td>Setting prohibited</td><td>Setting prohibited</td></tr>
<tr><td>0</td><td>20 MHz</td><td>20 MHz</td><td>20 MHz</td></tr>
</table>
</td></tr>
<tr><td>ITU-R BT.709 interface</td><td>When the ITU-R BT.709 interface is in use, the maximum frequency of the video clock is 74.5 MHz.</td></tr>
<tr><td>Capture in progressive mode</td><td>Use the internal field signal generation function in combination with an input interface in progressive mode.</td></tr>
<tr><td>Limitation on register update</td><td>If a register is updated during capture, data captured immediately after the register update cannot be guaranteed. To update a register which supports the internal update mode as shown in Table 22.10, VIN Registers, specify an internal update for VIN registers by using the MC/VUP bit. To update other registers, stop capture operation and then update them.</td></tr>
<tr><td>Field capture mode image quality</td><td>Images of odd-numbered, odd/even-numbered and even-numbered fields, captured by VnMC/IM interlace mode bit settings, contain every other line from the input interlace images. Therefore, note that the horizontal resolution for video display is in units of fields.</td></tr>
<tr><td>Full interlace mode image quality</td><td>In full interlace composition mode, horizontal stripe noise (such as combing noise) is generated in composite images as fields based on different timelines are combined in memory due to the interlacing method.</td></tr>
<tr><td>Limitation on vertical scaling</td><td>For vertical scaling and full interlace composition, the capture lines are inverted in some cases depending on the scaling ratio because the scaling processing is applied before interlace composition in memory. Be sure to evaluate the image quality before practical application.</td></tr>
<tr><td>Interrupt event timing</td><td>Interrupt event asserted by this module indicates the time when an interrupt event occurs in VIN, not the time when the transfer of capture data to memory is completed.</td></tr>
</table>

Item	Description
Pixel post-clip setting	When the output format is YCbCr-422, after pixel post-clip setting is performed for the clipping data, this data is transferred in YCbCr-422 data format to memory. Therefore, if the EPPoC-SPPoC clipping size is an odd number, it is normalized to an even size which is the sum of that odd number and 1.
Coefficient settings for color space conversion	Specify appropriate values in the color space change coefficient 1 to 3 registers (VnCSCC1 to VnCSCC3) to keep the RGB image data within the range 0 ≤ R', G', B' ≤ 255. After calculation for color space conversion, minus pixel data is normalized to 0 and pixel data more than or equal to 255 is normalized to 255.
Scaling up	When horizontal and vertical scaling up is specified, the amount of memory transfer becomes greater with an increase in traffic. Note the amount of traffic on the entire system when using the scaling-up function because the overall transfer efficiency of the system might degrade due to the increased use of the internal buses.
YC Restrictions on YC separation function	Set the offset register that stores UV data (VnUVAOF) such that the storage areas of Y and UV data are not the same. If the same storage area is set for both data, Y data will be overwritten.
	It is not allowed to set the YC separate transfer or Y transfer with the vertical scaling-up.
RGB-888→RGB-565 conversion function	In the dithering process by cumulative addition, if the same color is captured as in blue back image, periodic noise may be generated by the cumulative addition process (carried by addition). In this case, set the DC[1:0] bits in VnMC to the ordered dithering.
Video display operation	This module performs capture control based on the external input synchronization signal. Note that it is not synchronous to the timing of frame update set in the Display Unit and thus video display in sync with the capture frame is disabled.

Item	Description
The maximum size that can be captured when the HSYNC signal is connected to the VIn_CLKENB pin (including the case where the CHS bit of the VnDMR2 register is set to 1).	



Hbp: Horizontal back porch period
Hw: Horizontal valid pixels
Vbp: Vertical back porch period
Vw: Vertical valid lines

Capture area when the HSYNC signal is connected to the VIn_CLKENB pin

When the ITU-R BT.601/709/1358 interface is in use, so the HSYNC signal is connected to the VIn_CLKENB pin (including the case where the CHS bit of the VnDMR2 register is set to 1), the VIN also captures data during the horizontal and vertical back porch periods (Hbp and Vbp). Thus, capturing only the valid data is required by setting the clipping registers as shown below.

- VnSLPrC (start line pre-clip register) = vertical back porch period (Vbp)
- VnELPrC (end line pre-clip register) = vertical back porch period (Vbp) + number of valid lines (Vw) – 1
- VnSPPrC (start pixel pre-clip register) = horizontal back porch period (Hbp)
- VnEPPrC (end pixel pre-clip register) = horizontal back porch period (Hbp) + number of valid pixels (Hw) – 1

The maximum number of lines and pixels that can be captured at this time is as shown below. When this size is exceeded, use the VIN with the data enable signal connected to the VIn_CLKENB pin.

- The maximum number of lines that can be captured = 2048 (the maximum value of the clipping register) – vertical back porch period (Vbp)
- The maximum number of pixels that can be captured = 2048 (the maximum value of the clipping register) – horizontal back porch period (Hbp)

22.5 Supplementary Information

22.5.1 Example of Coefficient Set Register Settings for Horizontal Scaling

Table 22.18 shows the example of coefficient set register settings for horizontal (X) scaling (Recommended values).

Table 22.18 Coefficient Set Register Settings

- α = 0.6 and X Scale (XS) = H'0000 1600

n	CmA	CmB	CmC
1	H'0000 0BDD	H'0000 0BDD	H'0651 9578
2	H'3FF0 07DA	H'0000 0BE3	H'03C2 4973
3	H'3FF0 03D9	H'0000 0BE9	H'01B3 0D5F
4	H'3FFF F7DF	H'0010 03F1	H'0003 C542
5	H'000F DFEC	H'0010 03F7	H'3EC4 711D
6	H'000F C400	H'002F FFFD	H'3DF5 04F1
7	H'001F A81A	H'002F FC00	H'3D95 78C3
8	H'002F 8C3C	H'0010 0000	H'3DB5 C492

- α = 0.6 and X Scale (XS) = H'0000 2000

n	CmA	CmB	CmC
1	H'000F A400	H'000F A400	H'0962 5902
2 to 8	H'0000 0000	H'0000 0000	H'0000 0000

23. VCP3

23.1 Overview

The VCP3 is a multi-codec module which provides encoding and decoding capabilities on the basis of multiple video coding schemes, e.g., H.264/AVC, MPEG-4, MPEG-2 and VC-1. This module is a multi codec that processes the frame or each field by controlling software for VCP3 executed on host CPU.

23.1.1 Features

The VCP3 has the following excellent features.

- Support for multiple codecs
  - H.264/MPEG-4 AVC HP (High Profile) and MVC SHP (Stereo High Profile) encoding and decoding
  - H.262/MPEG-2 MP (Main Profile) decoding
  - MPEG-4 ASP (Advanced Simple Profile) decoding
  - VC-1 SP/MP/AP (Simple, Main, Advanced Profile) decoding
  - H.263 Baseline and decoding
  - AVS Jizhun Profile decoding
  - VP8 decoding Support for HDTV resolutions
  - 1,920 pixels × 1,080 lines @ 60 frames/second
- Number of channels
  - One channel
- Data handling on a picture-by-picture basis
  - Encode/decode data one picture (frame or field) at a time.
- High picture quality
  - Support the H.264 high-efficiency coding tools (CABAC, 8 × 8 frequency conversion, and quantization matrix).
  - High-efficiency motion vector detection by a combination of discrete search and trace search
  - Highly efficient real-time intra-prediction by Prediction from Original Image (POI)
  - Optimal-mode selection by Rate-Distortion (RD) cost evaluation
  - Picture quality control based on activity analysis results which match visual models
- Dedicated cache memory for VCP3 is integrated on this LSI. (64 Kbytes)

Table 23.1 Main Function of VCP3

Item	Description
Encoding standard supported	• H.264/AVC High Profile@Level 4.2, Main Profile@Level 4.2, Baseline Profile@Level 3 • H.264/MVC Stereo High Profile@Level 4.1
Decoding standard supported	• H.264/AVC High Profile@Level 4.2, Main Profile@Level 4.2, Baseline Profile@Level 3, Constrained Baseline Profile@Level 4.2 H.264/MVC (Error resilience tools (ASO, FMO, and RS) are not supported.) Stereo High Profile@Level 4.1 • MPEG-2 Main Profile@High Level • MPEG-4 Advanced Simple Profile3@Level 5 (GMC and QMC are not supported), Simple Profile@Level 6 • VC-1 Simple Profile@Medium Level, Main Profile@High Level, Advanced Profile@Level 3 • H.263 Baseline@Level 40 • VP8 • AVS Jizhun Profile@Level 6.2 (picture format 4:2:0 only)
Maximum throughput	1,920 × 1,080p, 60 frame In VP8 decoding, the maximum ratio of non-display frame is once every five frames.
Maximum bit rate	80 Mbps (40 Mbps × 2 ch). For MPEG-4 Data Partition, and VP8, the maximum bit rate is 60 (30 Mbps × 2 ch).
Picture size supported	Minimum: Horizontal 80 pixels × Vertical 80 lines (except for H.263), 128 pixels × Vertical 96 lines (H.263) Maximum: Horizontal 1,920 pixels × Vertical 1,088 lines Horizontal size is a multiple of 2 pixels, and vertical size is a multiple of 2 lines. 1,080 × 1,920 and 1,088 × 1,920 are supported.
Color format	YCbCr 4:2:0 format NV12, NV21, YV12 and IYUV are supported.
Bit stream format	Video elementary stream. Table 23.2 shows the range of data which can be encoded and decoded. Function to add/remove the emulation prevention byte in the H.264 VCL-NAL unit. (VCL (Video Coding Layer), NAL (Network Abstraction Layer)) Function to remove the emulation prevention byte in the VC-1 AP bit stream data unit. Function to remove the emulation prevention bit for AVS.
Picture structure	Frame structure and field structure

Item	Description
Motion detection	Motion search accuracy: 1/4 pixels (1/2 pixels for MPEG-2. MPEG-4, and H.263) Motion search range: 1. frame reference Horizontal ± 64 pixels, Vertical ± 32 lines 2. frame references (Wide side) Horizontal ± 48 pixels, Vertical ± 24 lines (Narrow side) Horizontal ± 32 pixels, Vertical ± 16 lines

Table 23.2 Data Format Handled by the VCP3

Standard	Encoding Range	Decoding Range
MPEG-4	Not supported	Video packet header/Motion shape texture and subsequent data
H.264	Slice header and subsequent data	Slice header and subsequent data (Except for first slice header in a picture)
H.263	Not supported	Macroblock and subsequent data
MPEG-2	Not supported	Picture data and subsequent data
MPEG-1	Not supported	Picture data and subsequent data
VC-1	Not supported	Slice data and subsequent data
AVS	Not supported	Picture data and subsequent data
VP8	Not supported	Frame header and subsequent data

23A. Video Processing Unit Cache (VPC)

23A.1 Overview

This LSI incorporates cache memory exclusively for use in image reference by the VCP3. This can reduce the amount of bus access for decoding.

23A.1.1 Features

The video processing unit cache (VPC) has the following features.

- 64-Kbyte cache
- Eight-way set-associative cache
- Line size: 64 or 128 bytes
- Number of entries: 128 entry/way (64-byte line size) or 64 entry/way (128-byte line size)
- Exclusively for reading
- FIFO (first-in first-out) replacement algorithm

23A.1.2 Block Diagram

Figure 23A.1 shows connection between VCP3, VPC, and system bus.

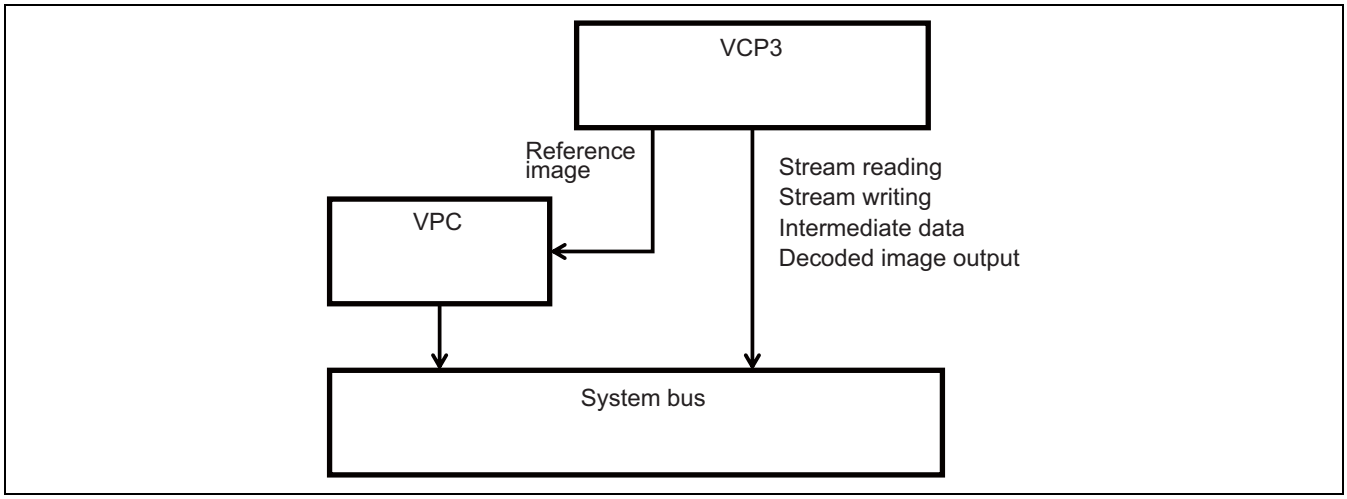


Figure 23A.1 Connection between VCP3, VPC, and System Bus

23A.1.3 Register Configuration

Table 23A.1 shows the VPC register configuration and Table 23A.2 shows the states of the registers in each of the processing modes. The registers can be accessed only in longwords.

Base address:

VPC for VCP3 (VPC0_BASE): H'FE90 8000

Table 23A.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
VPC control register	VPCCTL	R/W	VPC0_BASE + H'0004	32
VPC status register	VPCSTS	R	VPC0_BASE + H'0008	32
VPC configuration register	VPCCFG	R/W	VPC0_BASE + H'0078	32
VPC XY setting register for ch0	VPC0XY	R/W	H'FE96 0380	32

Note: Do not access addresses other than those listed above. Operations cannot be guaranteed if access is attempted.

Table 23A.2 States of Registers in Each Processing Mode

Register Abbreviation	Power-On Reset	Module Standby
All registers	Initialized	Retained

23A.2 Register Descriptions

23A.2.1 VPC Control Register (VPCCTL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	F64	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	LWS WAP	—	—	—	—	—	—	—	—	STRIDE		CLR	ENB
Initial value:	0	0	0	0	1	0	1	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved The write value should always be 0.
28	F64	0	R/W	64 Byte/Line Cache Mode When this bit is set to 1, the cache is configured as 64 bytes per line mode. 128 bytes per line mode is selected as initial value setting. On this product, this bit should be set to 1.
27 to 13	—	All 0	R	Reserved The write value should always be 0.
12	LWSWAP	0	R/W	Longword Swap 0: No longword swap 1: Longword swap When 8-, 16-, or 32-byte access is made with this bit set to 1, the read data is swapped in longwords.
11 to 8	—	H'A	R	Reserved Modifying these bits may affect the performance; usually leave the initial value unmodified.
7 to 4	—	H'8	R	Reserved Modifying these bits may affect the performance; usually leave the initial value unmodified.
3, 2	STRIDE	00	R/W	VPC Stride Setting These bits set the stride for VPC operation. 00: 256-byte stride mode 01: 512-byte stride mode 10: 1024-byte stride mode 11: 2048-byte stride mode The VPC access hit ratio depends on this setting; set these bits appropriately for the size to be processed. Note: XY mode case by setting VPCCFG.MODE to 1. Be sure the stride size of VCP3 is same as this setting.

Bit	Bit Name	Initial Value	R/W	Description
1	CLR	0	R/W	VPC Clear Clears the VPC state. 0: VPC operates normally. 1: VPC is cleared. Before modifying the VPC stride setting, write 1 to this bit to clear the VPC. After the VPC is cleared by writing 1 to this bit, this bit automatically returns to 0.
0	ENB	0	R/W	VPC Enable Enables the VPC. 0: Disables the VPC 1: Enables the VPC Set this bit to 1 to use the VPC. Do not modify this bit during VCP3 operation; otherwise, correct operation cannot be guaranteed. (Modify this bit after checking the VPCSTS register.)

23A.2.2 VPC Status Register (VPCSTS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	IDL
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	—	R	Reserved The read value is undefined. The write value should be 0 or 1, which has been read immediately before writing (read-modify-write).
0	IDL	—	R	VPC Idle 0: VPC is operating. 1: VPC is in the idle state. Indicates the VPC processing state. Confirm that this bit is 1 before clearing the cache.

23A.2.3 VPC Configuration Register (VPCCFG)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CTLH			CTLW		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	YTLH			YTLW			TL	MODE
Initial value:	0	0	0	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved The write value should always be 0.
21 to 19	CTLH	000	R/W	Tile Height Size Setting for Chroma (CbCr) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.
18 to 16	CTLW	000	R/W	Tile Width Size Setting for Chroma (CbCr) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.
15 to 8	—	H'03	R	Reserved The write value should always be H'03.
7 to 5	YTLH	000	R/W	Tile Height Size Setting for Luminance (Y) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.

Bit	Bit Name	Initial Value	R/W	Description
4 to 2	YTLW	000	R/W	Tile Width Size Setting for Luminance (Y) data 000: 32 001: 64 010: 128 011: 256 100: 512 101: 16 Others: Settings are prohibited.
1	TL	0	R/W	Tile Mode Setting 0: Linear Mode 1: Tile Mode
0	MODE	0	R/W	VPC addressing mode select 0: Linear addressing 1: XY addressing

23A.2.4 VPC XY Setting Register for ch0 (VPC0XY)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	STRIDE								AC	—	BT	AD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved The write value should always be 0.
11 to 4	STRIDE	H'00	R/W	This value should always be set as same as VPCCTL.STRIDE.
3	AC	0	R/W	This value should always be set to 0.
2	—	0	R	Reserved. The write value should always be 0.
1	BT	1	R/W	This value should be set based on the value of VPCCFG.MODE VPCCFG.MODE = 1 set this bit to 1. VPCCFG.MODE = 0 set this bit to 0.
0	AD	1	R/W	This value should be set based on the value of VPCCFG.MODE VPCCFG.MODE = 1 set this bit to 1. VPCCFG.MODE = 0 set this bit to 0.

23A.3 Operation

23A.3.1 Initialization

When using the VPC, before accessing the VPC from the VCP3, be sure to make the necessary settings as described in 1 to 4 below.

1. Set the stride and cache line size.
   Set the stride appropriate for the image size to be processed. (Set as same stride size as VCP3 stride size)
   The stride can be set using bits 3 and 2 in the VPCCTL register.
   Set the cache line size to 64 byte / line by setting bit 29 in VPCCTL register to 1.
2. Set the VPC mode
   Set the VPC mode by setting VPCCFG.MODE.
   VPCCFG.MODE = 0
      Set H'0000 0000 to VPC0XY register.
      Set bits[11:8] in S3CTRL.XYMODECONF to H'F.
   VPCCFG.MODE = 1
      Set bits [11:8] in S3CTRL.XYMODECONF to H'F
3. Set the tile size
   Set appropriate tile size in the VPCCFG register
   The tile size can be set using bit 21 to 16 and bit 7 to 2 for Chroma data and Luminance data respectively.
3. Clear the VPC.
   Clear the VPC after confirming that bit 0 in the VPCSTS register is 1.
   The VPC can be cleared by writing 1 to bit 1 in the VPCCTL register.
4. Enable the VPC.
   Enable the VPC after confirming that bit 0 in the VPCSTS register is 1.
   The VPC can be enabled by writing 1 to bit 0 in the VPCCTL register.

23A.3.2 Clearing VPC at the Beginning of a Frame

Before accessing the beginning of a frame, clear the VPC following steps 1 and 2 below.

1. Check the status.
   Confirm that bit 0 in the VPCSTS register is 1.
2. Clear the VPC.
   Clear the VPC by writing 1 to bit 1 in the VPCCTL register.

23A.4 Usage Notes

23A.4.1 Coherency

At the beginning of a frame, be sure to clear the VPC according to the procedure given in section 23A.3.2, Clearing VPC at the Beginning of a Frame.

23A.4.2 Tile Size

Appropriate tile size for this LSI: 128 × 32

24. Fine Display Processor (FDP1)

24.1 Functional Description

24.1.1 Overview

The FDP1 is the de-interlacing module which converts the interlaced video to progressive video. This product provides one channel. This module has the following features.

1. Supports various data formats
   - Input: YCbCr444/422/420
   - Output: YCbCr444/422/420 and RGB/αRGB
2. Full HD video processing performance
   - Can process maximum Full-HD 60i to 60p at 266 MHz operating frequency.
3. High image-quality de-interlacing algorithm (basing on luma component only)
   - Motion adaptive de-interlacing
   - Accurate still detection
   - Diagonal line interpolation (DLI)

24.1.2 FDP1 Architecture

Figure 24.1 shows the block diagram of the FDP1. In this figure, "Previous field image" and "Next field Image" are luma image only.

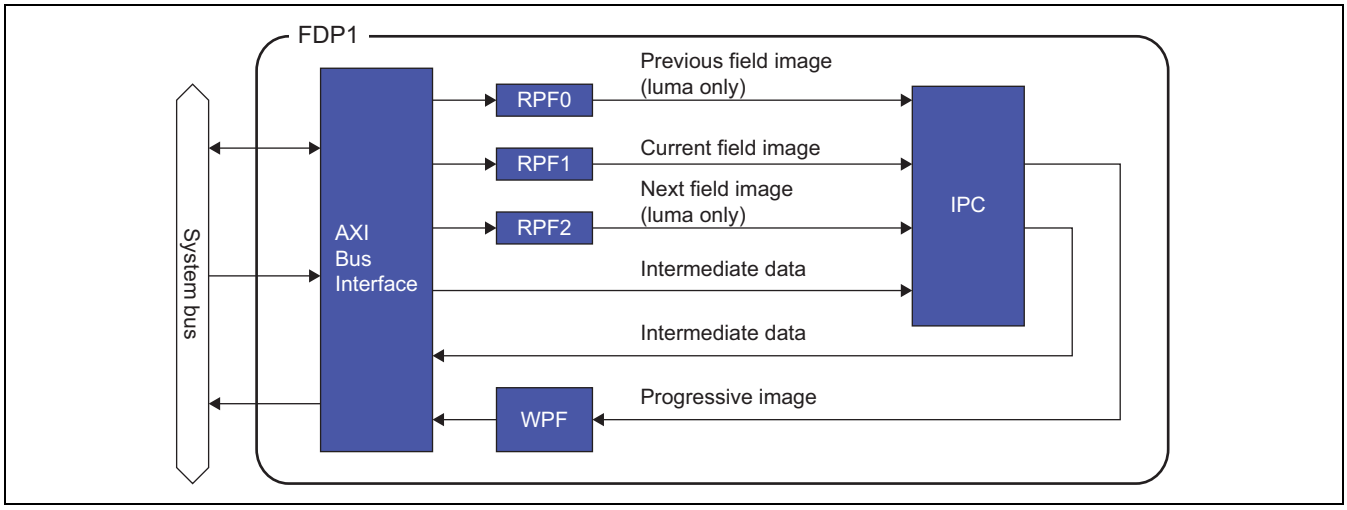


Figure 24.1 FDP1 Block Diagram

The following gives an overview of each block function shown in Figure 24.1. The operation of these functions is determined by the register setting explained in section 24.3. Refer to section 24.3 for the relationship between the register setting and the functional behavior.

(1) ABI (AXI Bus Interface)

The FDP1 applies processing to the image data stored in the external memory and writes the resultant data back to the external memory. The data transfer between the external memory and FDP1 necessary for this operation is done by the ABI, which works as the bus master, according to the register settings. The ABI executes this data transfer between the external memory and FDP1.

(2) RPF (Read Pixel Formatter)

The RPF reads image data from the external memory through the ABI, unpacks data according to the specified format, and outputs the resultant data to the IPC. The input format unpacking unit expands the image data input from the ABI into the image format for internal processing.

The FDP1 provides three RPF modules (RPF0 to RPF2). RPF0 reads the previous field, RPF1 reads the current field and RPF2 reads the next field for processing de-interlacing operation.

(3) IPC (Interlace to Progressive Converter)

The IPC is the de-interlacing module which reads the field image through RPFn and writes back the progressive image to the external memory through WPF. The IPC uses the motion adaptive algorithm which enhances the image resolution of still pixels compared with conventional 2D de-interlacing.

Note: The motion adaptive algorithm is applied to only luma component. Conventional 2D de-interlacing is applied to chroma component.

(4) WPF (Write Pixel Formatter)

The WPF is an output module that receives image data from the IPC, converts the color space, number of colors, and format of the data, and outputs the results of FDP1 image processing to external memory through the ABI. The WPF is mainly configured from a color space converter and an output format converter (the packing unit).

The color space converter converts the color space between RGB and YCbCr, and the packing unit converts the format into the picture plane storing format. The FDP1 provides one WPF.

24.2 Function List

Table 24.1 shows a functional overview of the FDP1 module.

Table 24.1 Function List

Read Pixel Formatter (RPF)

Number of channels			Three channels (RPF0 to RPF2)
Image Format	Input*3	YCbCr	YCbCr444-PL, SP, ILV*1 YCbCr422-PL, SP, ILV*1 YCbCr420-PL, SP*1
		Maximum size	H2048 × V2048 pixels (Frame) H2048 × V1024 pixels (Field)
		Minimum size	H80 × V80 pixel (Frame) H80 × V40 pixel (Field)
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.

Write Pixel Formatter (WPF)

Number of channels			One channel (WPF)
Image format	Output	RGB	RGB332, RGB444, RGB565, RGB666, RGB888, αRGB8666, αRGB8888, αRGB4444, αRGB1555 α value is fixed.
		YCbCr	YCbCr444-PL, SP, ILV*1 YCbCr422-PL, SP, ILV*1 YCbCr420-PL, SP*1
		Maximum size	H2048 × V2048 pixels
		Minimum size	H80 × V80 pixel
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
Color space conversion	YCbCr to RGB	Conversion expression	BT.601 (16, 235/240) to RGB (0, 255) BT.709 (16, 235/240) to RGB (0, 255) BT.601 (0, 255) to RGB (0, 255) BT.709 (16, 235/240) to RGB (16, 235)
Changing number of colors	Output	Reducing RGB color depth	Dithering, lower-order bit truncation, or rounding
		YCbCr422/420	CbCr skipping or CbCr vertical skipping and horizontal skipping

Interlace to Progressive Converter (IPC)

De-interlacing	Mode	Frame rate	Equal rate (60i to 60p) Half rate (60i to 30p)
		Interpolation (luma)	2D-3D adaptive*2 2D fixed 3D fixed*2
		Interpolation (chroma)	2D fixed
	Algorithm		Motion adaptive (luma only)
Diagonal line interpolation			Supported (luma only)

Notes: 1. PL: Planar, SP: Semi-planar, ILV: Interleaved
2. Source picture structures (field-structure or frame-structure) should be the same structure among the all input pictures.
3. Chroma component (Cb, Cr or U, V) of RPF0, RPF2 is not read from bus in case of planar or semi-planar format and discarded after reading in package with luma component in case of interleaved format because it is processed in fixed 2D de-interlacing.

Preface

Definition of operators and functions

The following operators, notations are defined for explaining the functions of the FDP1.

$\langle x \rangle$

Discard decimal places of value x

H'

The notation “H'” is used as prefix for hexadecimal numbers. For example, H'80 means 80 in hexadecimal and 128 in decimal.

B'

The notation “B'” is used as prefix for binary numbers. For example, B'10000000 means 80 in hexadecimal and 128 in decimal. When a number is used without prefix, it means decimal number.

_

The notation “_” is used as a separator of binary digit for binary number. There is no functional and logical meaning. The meaning of B'10101 and B'1_0101 is the same.

[msb:lsb]

This notation specifies a part of bits or all bits of registers and signals. For example, eval[3:0] means bits 3 to 0 of the signal or register whose name is “eval”.

clip0 (*x*)

Clip to 0 value if x is less than 0. [x = (x < 0)? 0 : x]

clip3 (min., max., x)

The value x shall be clipped so that x shall be min. < x < max. [x = (x < min)? min : ((x > max)? max : x)]

Unit

The unit is defined here for explaining FDP1’s functions.

[bpp]: bits per pixel

The FDP1 can handle a number of image formats. Each image format has different number of data bits. The unit [bpp] shows a number of data bits for one pixel. For example, RGB 8 bpp means that its format is RGB and the pixel consists of 8 data bits.

24.3 Registers

24.3.1 Access Restrictions

FDP1 supports only 32-bit access to read or write all addresses in FDP1 area. Do not access any of otherwise access units.

24.3.2 Register Type Definitions

There are 3 types of registers in FDP1: immediate register, V-update Register and V-update Status Register. The values of immediate registers are reflected to H/W behavior immediately after the changing its values. Hence, do not change these immediate registers while FDP1 is processing unless this manual allows it explicitly. The values of V-update registers are reflected to H/W behavior at the timing of V-interruption (at the timing of FD1_CTL_IRQSTA.VINT is set to 1). Users can change these V-update registers while FDP1 is processing. To reflect V-update registers to the H/W, users have to set FD1_CTL_REGEND.REGEND to 1 after the all V-update registers which are intended to be changed are completely set. The values of V-update Status Registers are updated at the timing of V-interruption. Therefore, the status (FD1_CTL_STATUS) of de-interlacing process which is conducted before a V-interruption must be referred after that V-interruption.

To confirm the types of registers, refer to Table 24.4.

24.3.3 Notational Conventions for Registers and Bit Fields

This document uses the following notational conventions for the FDP1 registers and bit fields.

1. The names of registers and bits are written in uppercase.
2. A bit or bit field in a register is indicated as [register name.bit name]. For example, the STRCMD bit in the FD1_CTL_CMD register is indicated as FD1_CTL_CMD.STRCMD.
3. Lowercase "n" in a register name or a bit name indicates an integer and the range of value n is defined when necessary. For example, FD1_RPFn_ADDR_Y.PSRC_ADDR (n = 0, 1, 2) indicates the PSRC_ADDR bits in three registers FD1_RPF0_ADDR_Y.PSRC_ADDR and FD1_RPF1_ADDR_Y.PSRC_ADDR, and FD1_RPF2_ADDR_Y.PSRC_ADDR. For RPFn when the range of value n is not defined, RPFn (n = 0, 1, 2) are assumed.
4. In each subsection for register description in section 24.3, when only a bit name is written without showing its register name, the bit is in the register described in that subsection.
5. A wildcard (*) indicates any characters in a name and represents all registers or bits that match the specified first part of a name. For example, when there are three registers FD1_RPF0_ADDR_Y, FD1_RPF1_ADDR_C0 and FD1_RPF1_ADDR_C1, FD1_RPF1_ADDR_* indicates three registers.

24.3.4 Register Configuration

The FDP1 registers are arranged in the following order; the general control registers control the operation of the entire FDP1, and the other registers control each image processing and specify parameters for the processing. The functions of the registers are described in this order starting from section 24.3.7.

1. General control registers (FD1_CTL_*)
2. RPF control registers (FD1_RPF_*)
3. WPF control registers (FD1_WPF_*)
4. IPC control registers (FD1_IPC_*)

24.3.5 Restrictions on Access to Registers and Lookup Tables

The FDP1 has control registers and lookup tables. When accessing the addresses where these registers and lookup tables are allocated, the following restrictions should be satisfied. If any restriction is violated, the FDP1 will not operate correctly.

1. For the read-only bits and reserved bits in all FDP1 registers, writing 1 is prohibited unless otherwise specified.
2. Addresses undefined in section 24.3.7, Memory Map, are reserved areas and write access is prohibited in these areas.
3. For all immediate registers and lookup tables, except FD1_CTL_SGCMD, FD1_CTL_SRESET and FD1_CTL_IRQ*, modifying register values during operation of the module is prohibited. Modify registers while the FDP1 is stopped. For the operating status of the FDP1, refer to section 24.3.8.8.

24.3.6 Procedure of FDP1 Start and Stop

24.3.6.1 Register usages for FDP1 Start and Stop

Registers FD1_CTL_CMD, FD1_CTL_SGCMD, and FD1_CTL_REGEND must be used correctly in the procedures of FDP1 start and stop as specified in Tables 24.2 and 24.3.

Table 24.2 Register Usages for Starting FDP1

Register	Start the First Frame (FR[0])	Start the Second or Later Frame (FR[f], f = 1, 2, 3, …)
FD1_CTL_SGCMD.SGEN	After all registers have been set completely, it must be set as 1 to generate V-Interruption.	It must be kept as 1 from the previous frame FR[f-1].
FD1_CTL_REGEND.REGEND	After all registers except FD1_CTL_SGCMD.SGEN have been set completely, it must be set 1. As the results, at the first V-interruption, all V-update registers are reflected for hardware reference, FD1_CTL_CMD.STRCMD is referred to start the first frame.	After V-interruption of starting the previous frame FR[f-1], it must be set 1 after all registers about FR[f] have been set completely. As the results, at the V-interruption of the end of frame FR[f-1], the V-update registers will be reflected to hardware reference, FD1_CTL_CMD.STRCMD is referred to start the frame FR[f].
FD1_CTL_CMD.STRCMD	It must be set 1 when all registers except FD1_CTL_SGCMD.SGEN, FD1_CTL_REGEND.REGEND are set. At the first V-Interruption it is referred by hardware to start the frame.	It must be set 1 when all registers except FD1_CTL_REGEND.REGEND are set At the next V-Interruption (boundary between FR[t-1] and FR[t]) it is referred by hardware to start the frame.

Table 24.3 Register Usages for Stopping FDP1

Register	Stopping Immediately by Software Reset	Stopping after Current Process Finished
FD1_CTL_SGCMD.SGEN	It must be cleared before setting the value of FD1_CTL_SRESET.SRST as 1 so that no more V-Interruption after FDP1 stopped.	After V-interruption at the final frame end (FD1_CTL_IRQSTA.FRE is set as 1) occurred, it must be cleared so that no more V-Interruption is generated after FDP1 stopped
FD1_CTL_REGEND.REGEND		No Interrupt Mode After V-interruption of starting the final frame, it must be set 1 right after clearing FD1_CTL_CMD.STRCMD so that the final V-interruption occurs and operation status of the final frame is updated to V-update status registers for Software reference. Other modes Right after V-interruption at starting the final frame, it must be set 1 right after clearing FD1_CTL_CMD.STRCMD so that operation status of the final frame is updated to V-update status registers for Software reference.
FD1_CTL_CMD.STRCMD	After FDP1 stopped successfully (FD1_CTL_IRQSTA.FRE is set as 1), it must be cleared to prevent wrong operation when the FDP1 is restarted.	After V-interruption of starting the final frame, it must be cleared to prevent wrong operation when the FDP1 is restarted.

24.3.6.2 Register Setting Order for FDP1 Start and Stop

(1) Interrupt Mode or Best Effort Mode

(a) To start the first frame of FDP1 process, set registers in following order.

1. Set all registers other than FD1_CTL_CMD, FD1_CTL_SGCMD, and FD1_CTL_REGEND.
   Set FD1_CTL_CMD.STRCMD to the value 1.
2. Set FD1_CTL_REGEND.REGEND to the value 1.
3. Set FD1_CTL_SGCMD.SGEN to the value 1, then FDP1 starts its process. FD1_CTL_SGCMD.SGEN must be not cleared to continue the second or later frames.

(b) To start the second or later frame, set registers in following order:

1. After V-interruption of the previous frame start timing occurred, set all registers other than FD1_CTL_CMD and FD1_CTL_REGEND.
2. Set FD1_CTL_CMD.STRCMD to the value 1.
3. Set FD1_CTL_REGEND.REGEND to the value 1.
4. At the V-interruption of the previous frame end timing, FDP1 starts the target frame. The V-interruption of the previous frame end timing and the one of the target frame start timing are the same.

(c) To stop FDP1 operation after currently frame finished, set registers as the following.

1. After V-interruption of the current frame start timing occurred, set FD1_CTL_CMD.STRCMD to the value 0. Set FD1_CTL_REGEND.REGEND to the value 1. If this register was completed before the V-Interruption of frame end timing, FDP1 stops its operation and currently frame becomes the last frame of the image sequence. If these register setting could not be completed before the V-Interruption of frame end timing, FDP1 stops its operation in the next V-

interruption. In the latter case, V-update status registers are not updated at V-interruption of frame end but at the next V-interruption at which DF1_CTL_REGEND.REGEND is set as 1.

2. Set FD1_CTL_SGCMD.SGEN to the value 0, then FDP1 will stop generating V-interruption.

(d) To stop FDP1 operation immediately, set registers as the following.

1. Set FD1_CTL_SGCMD.SGEN to the value 0, then FDP1 will stop generating V-interruption.
2. Set FD1_CTL_SRESET.SRST to the value 1. FDP1 will invoke termination process immediately.
3. Wait frame end interrupt from FDP1 or until the register bit FD1_CTL_IRQSTA.FRE is set to 1. After it occurs, FDP1 have finished its processing. With this operation, FDP1 can stop its process quickly, but the output frame of the last frame is corrupted.

(2) No interrupt mode

(a) To start the first frame, set registers in following order.

Same as (1) (a).

(b) To start the second or later frame, set registers in following order.

Same as (1) (b).

(c) To stop FDP1 operation after current frame finished, set registers as the following.

1. After V-interruption of the current frame start timing occurred, set FD1_CTL_CMD.STRCMD to the value 0.
2. Set FD1_CTL_REGEND.REGEND to the value 1. At the V-Interruption of frame end timing, FDP1 stops its operation and current frame becomes the last frame of the image sequence.
3. Set FD1_CTL_SGCMD.SGEN to the value 0, then FDP1 will stop generating V-interruption.

(d) To stop FDP1 operation after current frame finished, set registers as the following.

Same as (1) (d).

24.3.7 Memory Map

Table 24.4 shows the FDP1 memory map. Immediate registers are specified as “Imm”, the V-update registers are indicated as “Vupdt” and the V-update status registers are indicated as “VupdtSt” in register type column in Table 24.4.

Base address of each FDP1:

Ch0: H'FE94 0000

Table 24.4 FDP1 Memory Map

Space	Register Type	Register Name	Abbreviation	Relative Address	Register Type
Register	General control registers	FDP1 Start Register	FD1_CTL_CMD	H'0000	Imm
		Sync Generator Register	FD1_CTL_SGCMD	H'0004	Imm
		Register Set End Register	FD1_CTL_REGEND	H'0008	Imm
		Channel Activation Register	FD1_CTL_CHACT	H'000C	Vupdt
		Operation Mode Register	FD1_CTL_OPMODE	H'0010	Vupdt
		V-Period Register	FD1_CTL_VPERIOD	H'0014	Vupdt
		Software Reset Register	FD1_CTL_SRESET	H'001C	Imm
		Operating Status Register	FD1_CTL_STATUS	H'0024	VupdtSt
		V-Cycles Status Register	FD1_CTL_VCYCLE_STAT	H'0028	VupdtSt
		Interrupt Enable Register	FD1_CTL_IRQENB	H'0038	Imm
		Interrupt Status Register	FD1_CTL_IRQSTA	H'003C	Imm
	RPF control registers	Source Picture Size Register	FD1_RPF_SIZE	H'0060	Vupdt
		Source Picture Format Register	FD1_RPF_FORMAT	H'0064	Vupdt
		Source Picture Stride Register	FD1_RPF_PSTRIDE	H'0068	Vupdt
		RPFn Source Component-Y Address Register (n = 0, 1, 2)	FD1_RPFn_ADDR_Y	H'006C + H'C × n	Vupdt
		RPF1 Source Component-C0 Address Register	FD1_RPF1_ADDR_C0	H'007C	Vupdt
		RPF1 Source Component-C1 Address Register	FD1_RPF1_ADDR_C1	H'0080	Vupdt
		Still Mask Address Register	FD1_RPF_SMSK_ADDR	H'0090	Vupdt
		RPF Data Swap Register	FD1_RPF_SWAP	H'0094	Vupdt
	WPF control registers	Destination Picture Format Register	FD1_WPF_FORMAT	H'00C0	Vupdt
		Destination Picture Rounding Control Register	FD1_WPF_RNDCTL	H'00C4	Vupdt
		Destination Picture Stride Register	FD1_WPF_PSTRIDE	H'00C8	Vupdt
		Destination Component-Y Address Register	FD1_WPF_ADDR_Y	H'00CC	Vupdt
		Destination Component-C0 Address Register	FD1_WPF_ADDR_C0	H'00D0	Vupdt
		Destination Component-C1 Address Register	FD1_WPF_ADDR_C1	H'00D4	Vupdt
		WPF Data Swap Register	FD1_WPF_SWAP	H'00D8	Vupdt

Space	Register Type	Register Name	Abbreviation	Relative Address	Register Type
Register	IPC control registers	IPC Mode Register	FD1_IPC_MODE	H'0100	Vupdt
		Still Mask Threshold Register	FD1_IPC_SMSK_THRESH	H'0104	Vupdt
		Comb Detection Parameter Register	FD1_IPC_COMB_DET	H'0108	Vupdt
		Motion Decision Parameter Register	FD1_IPC_MOTDEC	H'010C	Vupdt
		DLI Blend Parameter Register	FD1_IPC_DLI_BLEND	H'0120	Vupdt
		DLI Horizontal Frequency Gain Register	FD1_IPC_DLI_HGAIN	H'0124	Vupdt
		DLI Suppression Parameter Register	FD1_IPC_DLI_SPRS	H'0128	Vupdt
		DLI Angle Parameter Register	FD1_IPC_DLI_ANGLE	H'012C	Vupdt
		DLI Isolated Pixel Parameter Register 0	FD1_IPC_DLI_ISOPIX0	H'0130	Vupdt
		DLI Isolated Pixel Parameter Register 1	FD1_IPC_DLI_ISOPIX1	H'0134	Vupdt
		IPC Sensor Threshold Register 0	FD1_IPC_SENSOR_TH0	H'0140	Vupdt
		IPC Sensor Threshold Register 1	FD1_IPC_SENSOR_TH1	H'0144	Vupdt
		Sensor Control Register 0	FD1_SENSOR_CTL0	H'0170	Vupdt
		Sensor Control Register 1	FD1_SENSOR_CTL1	H'0174	Vupdt
		Sensor Control Register 2	FD1_SENSOR_CTL2	H'0178	Vupdt
		Sensor Control Register 3	FD1_SENSOR_CTL3	H'017C	Vupdt
	IPC control registers	Sensor Register m (m = 0 to 17)	FD1_SENSOR_m	H'0180 + H'4 × m	—
		Line Memory Pixel Number Register	FD1_IPC_LMEM	H'01E0	—
		IP Internal Data Register	FD1_IP_INDATA	H'0800	—
LUT	DIF_ADJM		FD1_DIF_ADJ_00 ↓ FD1_DIF_ADJ_FF	H'1000 ↓ H'13FF	
	SAD_ADJ		FD1_SAD_ADJ_00 ↓ FD1_SAD_ADJ_FF	H'1400 ↓ H'17FF	
	BLD_GAIN		FD1_BLD_GAIN_00 ↓ FD1_BLD_GAIN_FF	H'1800 ↓ H'1BFF	
	DIF_GAIN		FD1_DIF_GAIN_00 ↓ FD1_DIF_GAIN_FF	H'1C00 ↓ H'1FFF	
	MDET		FD1_MDET_00 ↓ FD1_MDET_FF	H'2000 ↓ H'23FF	

24.3.8 General Control Registers

24.3.8.1 FDP1 Start Register (FD1_CTL_CMD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR CMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STRCMD	0	R/W	Start Command FDP1 starts the de-interlacing processing if this bit is set to 1. Set this bit after all relevant registers are surely set except for FD1_CTL_REGEND and FD1_CTL_SGCMD. Set this bit to 1 before the FD1_CTL_REGEND.REGEND and FD1_CTL_SGCMD. if FDP1 has to execute process. This bit will keep the value 1 after the set. To clear this bit, write the value 0 to this bit. 0: NOP or stops process at the next timing of V-Interruption. 1: Start FDP1 process at the next timing of V-Interruption. Note that setting of this register is valid if the register FD1_CTL_REGEND.REGEND is set to the value 1 at the timing of next V-Interruption.

24.3.8.2 Sync Generator Register (FD1_CTL_SGCMD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SGEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SGEN	0	R/W	V-Interruption Generator Enable This bit controls V-Interruption. This bit should be set to the value 1 after other all registers are set, and only at the first field of the sequence. Set this bit to the value 1 to execute process in all V-Interruption modes described in section 24.3.8.5. 0: Disable V-Interruption 1: Enable V-Interruption [Important] In case of software reset (FD1_CTL_SRESET.SRST), set this SGEN bit to the value 0. If this bit is cleared during process V-interruption will not occur after FDP1 finished current frame. As a result, FDP1 will not start the next frame because STRCMD is not captured and V-update status registers will not be updated about process information of current frame.

24.3.8.3 Register Set End Register (FD1_CTL_REGEND)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	REG END
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	REGEND	0	R/W	Register Setting Ready Flag Set the value 1 to this bit after completing the setting of parameter registers. Do not write the value 0 to this bit. This bit will be cleared by FDP1 automatically. 0: Writing 0 is prohibited except for after the completion of S/W reset sequence. 1: Registers which are set by SW is ready to be reflected for Hardware reference. The V-update status registers is ready to be reflected for Software reference. The second or later V-interruption in the case No interrupt mode can be generated.

24.3.8.4 Channel Activation Register (FD1_CTL_CHACT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SMW	WR	—	—	—	—	SMR	RD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	SMW	0	R/W	Refer to Table 24.5 for setting these register fields. The setting of each register field depends on the setting of FD1_IPC_MODE.DIM register bits. Do not set the other values which are specified in Table 24.5.
8	WR	0	R/W	
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SMR	0	R/W	Refer to Table 24.5 for setting these register fields. The setting of each register field depends on the setting of FD1_IPC_MODE.DIM register bits. Do not set the other values which are specified in Table 24.5.
2 to 0	RD[2:0]	000	R/W	

Table 24.5 FD1_CTL_CHACT Setting for FD1_IPC_MODE.DIM Parameter

PRG*1	DIM [2:0]*2		SMW	WR	SMR	RD2	RD1	RD0	LWord Expression
0 (Interlace Mode)	B’000 (Adaptive 2D/3D)	First field	1	1	0	0	1	0	H'0000 0302
		Second field	1	1	0	1	1	1	H'0000 0307
		Final field	0	1	0	0	1	0	H'0000 0102
		Otherwise	1	1	1	1	1	1	H'0000 030F
	B’010 (Fixed 3D)	First field	0	1	0	0	1	0	H'0000 0102
		Second field	0	1	0	1	1	1	H'0000 0107
		Final field	0	1	0	0	1	0	H'0000 0102
		Otherwise	0	1	0	1	1	1	H'0000 0107
	B’001 (Fixed 2D)		0	1	0	0	1	0	H'0000 0102
	B'011 (Previous field)		0	1	0	0(*3)	1	1	H'0000 0103
	B'100 (Next field)		0	1	0	1	1	0(*3)	H'0000 0106
1 (Progressive Mode)	Set DIM [2:0] as B'001		0	1	0	0	1	0	H'0000 0102

Note: Field order means an input field order to the FDP1.
For example, the first field is the first input field to the FDP1; the first field is processed but not output.
(*1) FD1_CTL_OPMODE.PRG, (*2) FD1_CTL_IPC_MODE.DIM [2:0], (*3) Value 1 can be set but the corresponding data is not read

24.3.8.5 Operation Mode Register (FD1_CTL_OPMODE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PRG	—	—	VIMD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PRG	0	R/W	Progressive Mode When the register field is set to 1, the de-interlacing processing is not executed and the incoming image data is passed through IPC module. 0: Interlace Mode 1: Progressive Mode
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	VIMD[1:0]	00	R/W	V-Interruption Mode This register field sets V-Interruption mode of FDP1. Refer to Table 24.6 for detail. 00: Normal 01: Best Effort 10: No interrupt

Table 24.6 V-Interruption Mode

VIMD[1:0]	V-Interruption Mode Timing		STRCMD Captured Timing
	First Time	Second Time or Later	
B'00 (Normal)	V-Interruption occurs when changes FD1_CTL_SGCMD.SGEN from 0 to 1 and FDP1 is not doing de-interlacing process.	Fixed period interrupt specified by FD1_CTL_VPERIOD in spite of the de-interlacing processing.	Captured at V-Interruption
B'01 (Best effort)		Fixed period interrupt specified by FD1_CTL_VPERIOD If the de-interlacing processing is not completed at the timing specified by FD1_CTL_VPERIOD, V-Interruption is deferred to the end of the processing.	
B'10 (No interrupt)		If FD1_CTL_REGEND is set 1 before the end of the processing (frame end interruption FD1_CTL_IRQSTA .FRE is set as 1) V-Interruption occurs right after the end of the processing. If FD1_CTL_REGEND is set 1 after the end of processing (frame end interruption FD1_CTL_IRQSTA .FRE is set as 1) V-Interruption occurs right after FD1_CTL_REGEND is set. If FD1_CTL_REGEND is not set 1 V-Interruption does not occur.	

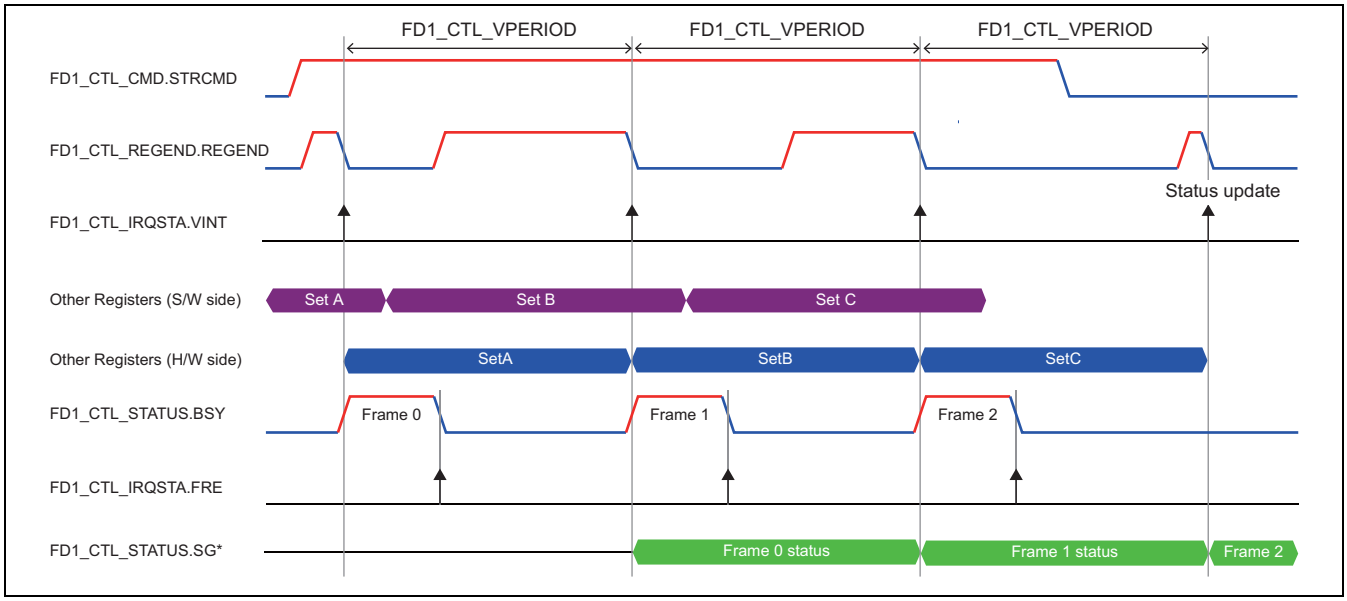


Figure 24.2 Timing Chart of Normal Mode (VIMD = 0) and Best Effort Mode (VIMD = 1)

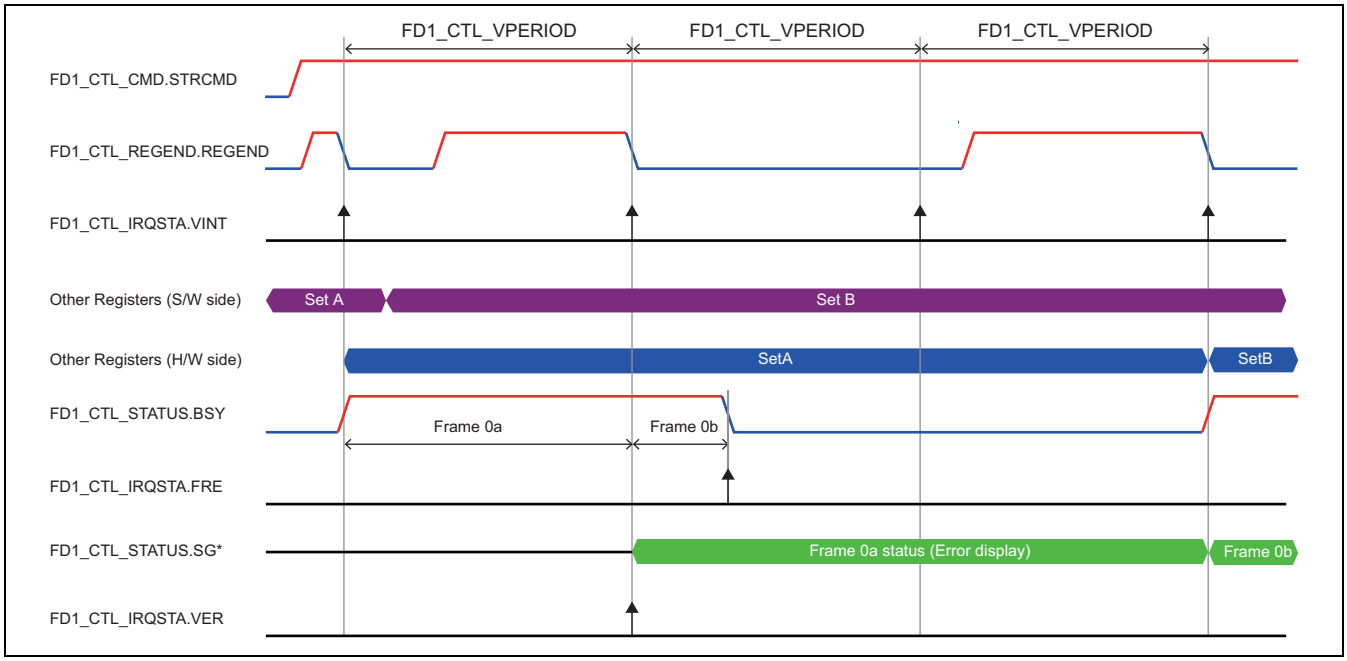


Figure 24.3 Timing Chart of Normal Mode (VIMD = 0) with Error

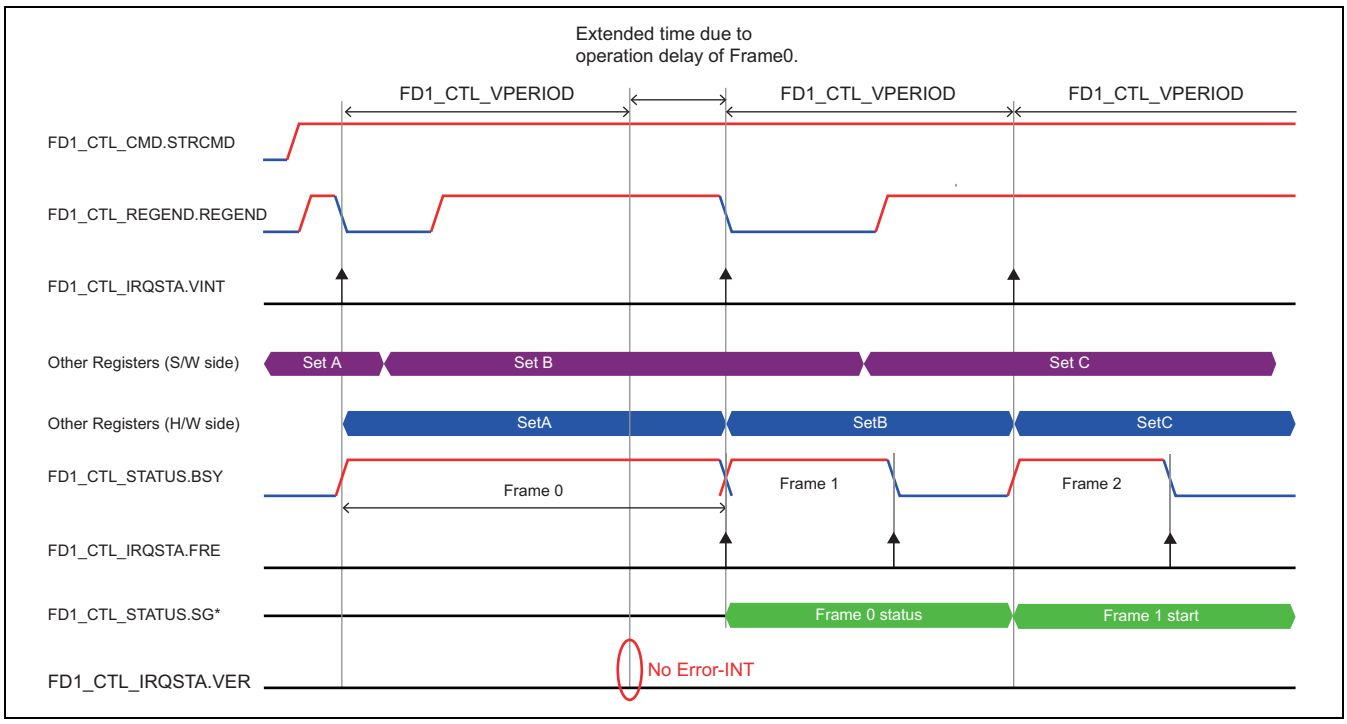


Figure 24.4 Timing Chart of Best Effort Mode (VIMD = 1) (in Case of Error at Normal Mode)

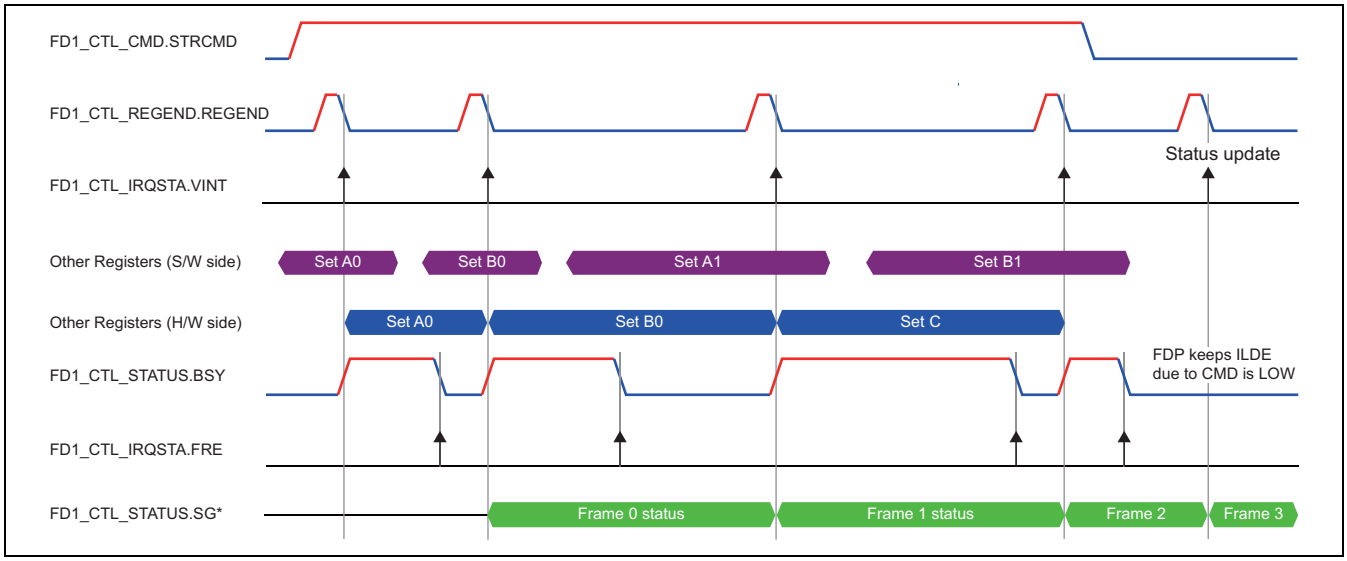
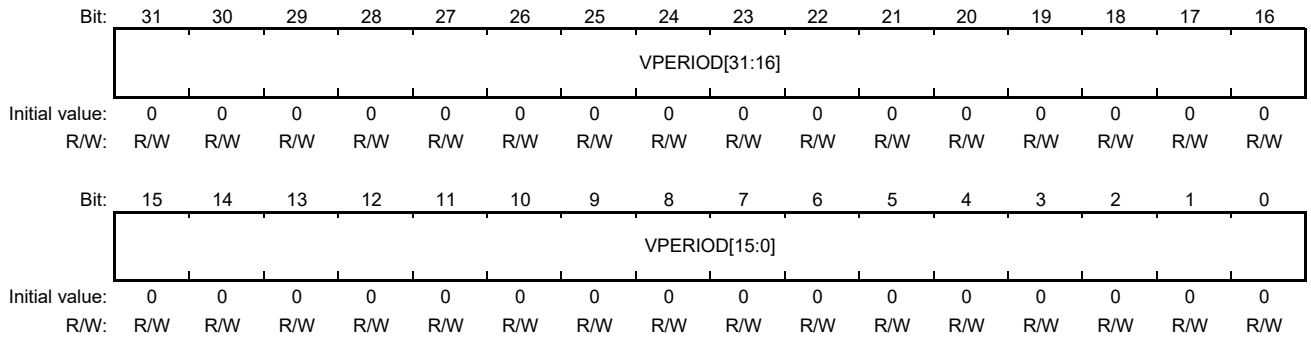


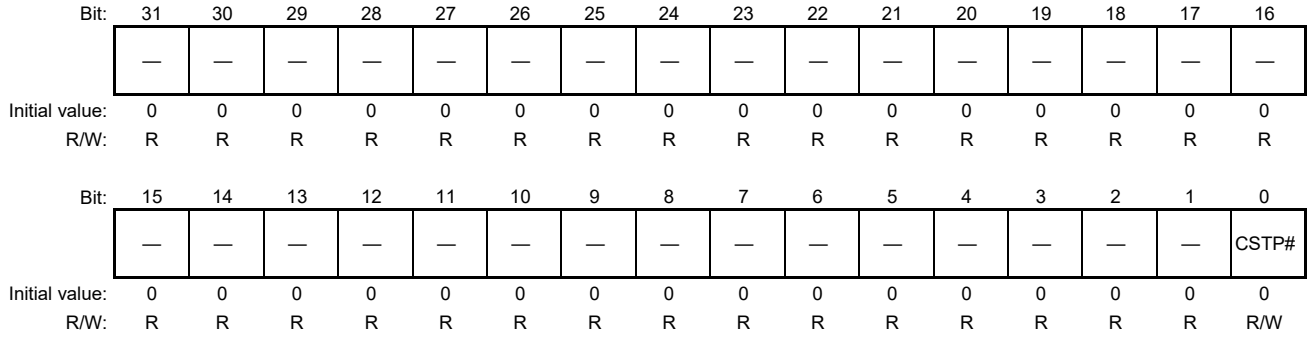
Figure 24.5 Timing Chart of No Interrupt Mode (VIMD = 2)

24.3.8.6 V-Period Register (FD1_CTL_VPERIOD)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VPERIOD [31:0]	All 0	R/W	V-Sync Period Set the period from the V-Sync to the next V-Sync in the unit of FDP1 clock frequency cycles.

24.3.8.7 Clock Control Register (FD1_CTL_CLKCTRL)



Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
0	CSTP#	0	R/W	Set the value 1 to this bit

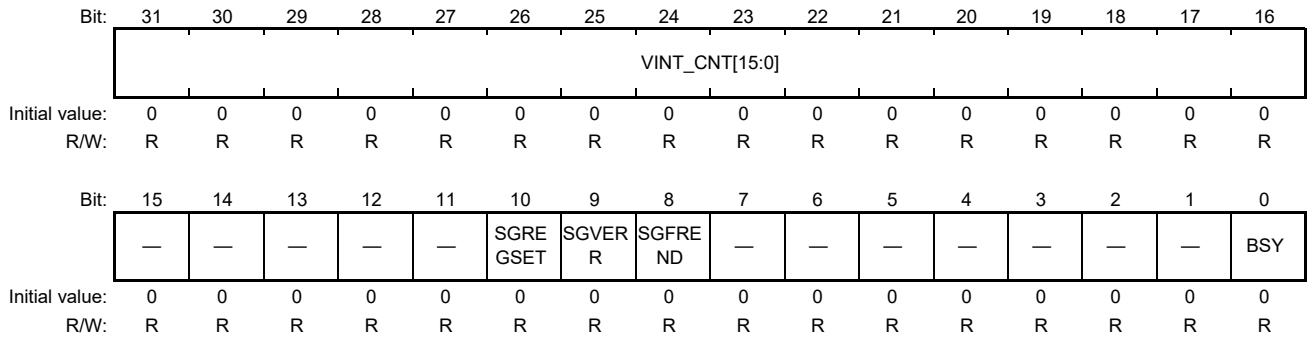
24.3.8.8 Software Reset Register (FD1_CTL_SRESET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

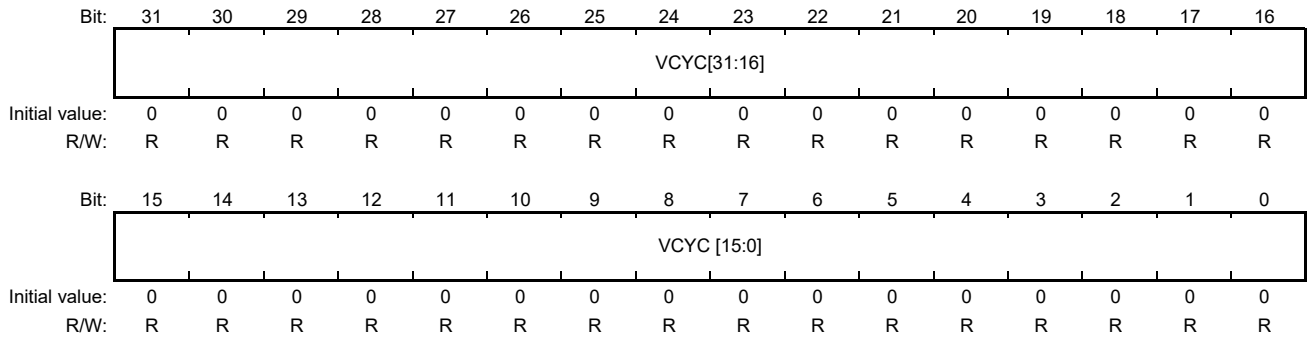
Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRST	0	R/W	FDP1 Software Reset FDP1 stops its operation after this bit is set to 1. FDP1 aborts all processings and quits bus/memory accesses. Do not start next process by FD1_CTL_CMD until the software processing is completed. When this processing is completed, the FD1_CTL_IRQSTA.FRE interrupt source bit is set to 1, when the FRE interrupt is enabled. This interrupt notifies the end of the reset processing. The end of software reset processing is notified through the FRE bit, but the software reset issued while FDP1 is stopped is ignored as NOP. As it takes a while until the reset is actually issued after the reset bit is set, the FDP1 may complete operation before the reset is actually issued. In this case, no interrupt is output for the software reset that is issued after the FDP1 completes operation. But even through in this case, not that the output image may be destroyed due to software reset process. This bit is always read as 0. 0: NOP 1: Software Reset [Important] Set FD1_CTL_SGCMD.SGEN to the value 0 before write 1 to this SRST bit.

24.3.8.9 Operating Status Register (FD1_CTL_STATUS)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	VINT_CNT [15:0]	H'0000	R	V-Sync Interrupt Counter Status This bit field shows the number of interruption times of V-Sync interrupt. Hence, the value of this bit indicates the number of progressive output frames which is generated by FDP1. This counter value is reset to 0 when FD1_CTL_SGCMD.SGEN is set to 1.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10	SGREGSET	0	R	Register Set End Status This bit represents the register set status updated at V-Sync. The status is controlled by FD1_CTL_REGEND.REGEND bit and the internal timing. 0: Registers are not set for the operation 1: Registers are set for the operation
9	SGVERR	0	R	V-Sync End Error Status This bit represents the V-Sync end error status updated at V-Sync. 0: No error 1: V-Sync end error (De-interlacing cannot be finished by the timing of V-Sync)
8	SGFREND	0	R	Frame End Status This bit represents the frame end status updated at V-Sync. 0: The de-interlacing is not finished 1: Frame end (The de-interlacing is finished)
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	BSY	0	R	FDP1 Operating Status This bit indicates the operating or stopped state of control FDP1. 0: FDP1 is stopped. 1: FDP1 is operating.

24.3.8.10 V-Cycles Status Register (FD1_CTL_VCYCLE_STAT)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VCYC[31:0]	H'0000_0000	R	Number of Cycles of the Previous Frame Processing This status register shows the number of cycles of previous frame de-interlacing processing. FDP1 updates this register at the timing of V-Sync interrupt.

24.3.8.11 Interrupt Enable Register (FD1_CTL_IRQENB)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VERE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VINTE	—	—	—	FREE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VERE	0	R/W	Interrupt Enable for V-Sync End Error The interrupt of V-Sync end error is asserted at the timing that FDP1 does not complete the de-interlacing processing at the V-Sync. 0: Interrupt Disabled 1: Interrupt Enabled
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VINTE	0	R/W	Interrupt Enable for V-Sync The interrupt of V-Sync is asserted at the timing of V-Sync specified by FD1_CTL_OPMODE.VIMD register field. If VIMD is set to 2, this interrupt is not asserted. 0: Interrupt Disabled 1: Interrupt Enabled
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FREE	0	R/W	Interrupt Enable for Frame End The interrupt of frame end is asserted at the timing that FDP1 completes the de-interlacing processing. 0: Interrupt Disabled 1: Interrupt Enabled

Each bit controls the interrupt enable of the corresponding interrupt source.

Each bit in FD1_CTL_IRQSTA is set to 1 when the corresponding interrupt source is generated. FD1_CTL_IRQENB specifies whether to output an interrupt signal for the generated source. When an interrupt is disabled in this register, no interrupt signal is generated even when the corresponding bit in FD1_CTL_IRQSTA is set to 1. When an interrupt is enabled in this register, an interrupt signal is output when the corresponding bit in FD1_CTL_IRQSTA is set to 1.

24.3.8.12 Interrupt Status Register (FD1_CTL_IRQSTA)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VINT	—	—	—	FRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VER	0	R/W	Interrupt Status and Clear for V-Sync End Error [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VINT	0	R/W	Interrupt Status and Clear for V-Sync [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FRE	0	R/W	Interrupt Status and Clear for Frame End [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

The read value from each bit is the status of the interrupt source, and the write access to each bit controls the interrupt status.

FD1_CTL_IRQSTA indicates the state of the interrupt sources generated in the FDP1. Whether to output a FDP1 interrupt when an interrupt source is generated and the corresponding bit is set to 1 is determined by the corresponding bit setting in FD1_CTL_IRQENB.

While an interrupt is disabled in FD1_CTL_IRQENB, the FDP1 does not output an interrupt signal even when an interrupt source is generated, but the source flag in this register is set to 1.

24.3.8.13 Interrupt Control Register (FD1_CTL_IRQFSET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	VER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VINT	—	—	—	FRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	VER	0	R/W	Set the value 0 to this bit.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VINT	0	R/W	Set the value 0 to this bit.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FRE	0	R/W	Set the value 0 to this bit.

24.3.9 RPF Control Registers

24.3.9.1 Source Picture Size Register (FD1_RPF_SIZE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	HSIZE[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	VSIZE[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	HSIZE[10:0]	H'000	R/W	Horizontal Source Picture Size Specify the horizontal picture size of each input field in unit of pixels.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	VSIZE[10:0]	H'000	R/W	Vertical Source Picture Size Specify the vertical picture size of each input field in unit of pixels.

24.3.9.2 Source Picture Format Register (FD1_RPF_FORMAT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CIPM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RSPYCS	RSPUVS	—	—	—	CF	—	RDFMT[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CIPM	0	R/W	Set 0 when FD1_CTL_OPMODE.PRG is set to 1, otherwise set the value 1 to this bit.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	RSPYCS	0	R/W	RPF Input Mode Setting 1 When the input format is YUY2, set this bit to 1 and set the RDFMT bits to 71 (H'47). When the input format is YVYU, set this bit and the RSPUVS bit to 1 and set the RDFMT bits to 71 (H'47). In other cases, set this bit to 0.
12	RSPUVS	0	R/W	RPF Input Mode Setting 2 When the input format is NV61, set this bit to 1 and set the RDFMT bits to 65 (H'41). When the input format is NV21, set this bit to 1 and set the RDFMT bits to 66 (H'42). When the input format is YVYU, set this bit and the RSPYCS bit to 1 and set the RDFMT bits to 71 (H'47). In other cases, set this bit to 0.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	CF	0	R/W	Current Field This bit specifies current field parity. Note that the previous or next field pictures should be the opposite parity of the current field specified by this bit. 0: Current field is top field 1: Current field Bottom field
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	RDFMT [6:0]	H'00	R/W	RPF Input Image Format Setting These bits select the format of the image input from the external SDRAM to the RPFn. Select a value corresponding to the desired format from those shown in Table 24.7. Note: Number of input pixels When YCbCr4:2:2 is selected through the RDFMT bits, the horizontal size of the input image should be specified in 2-pixel units. When YCbCr4:2:0 is selected, the vertical and horizontal sizes should be specified in 2-pixel units.

Table 24.7 YCbCr Formats for RPF Input*5 and WPF Output*4

RDFMT[6:0], WRFMT[6:0]	Packed YCbCr Input Format	Reference
H'00 to H'3F	Reserved	—
H'40	YCbCr4:4:4 semi-planar	Figure 24.6
H'41	YCbCr4:2:2 semi-planar (NV16, NV61*1)	
H'42	YCbCr4:2:0 semi-planar (NV12, NV21*1)	
H'43 to H'45	Reserved	—
H'46	YCbCr4:4:4 interleaved	Figure 24.7
H'47	YCbCr4:2:2 interleaved type 0 (UYVY, YUY2*2, YVYU*3)	
H'48	YCbCr4:2:2 interleaved type 1	
H'49	Reserved	
H'4A	YCbCr4:4:4 planar	Figure 24.8
H'4B	YCbCr4:2:2 planar (YV16)	
H'4C	YCbCr4:2:0 planar (YV12, YU12)	
H'4D to H'7F	Reserved	—

Notes: 1. When the input format is NV61 or NV21, set the RSPUVS bit to 1.
2. When the input format is YUY2, set the RSPYCS bit to 1.
3. When the input format is YVYU, set the RSPUVS bit to 1 and RSPYCS bit to 1.
4. The performance of FDP1 depends on the format because of the limited bus buffer size. The following formats may decrease the tolerance of the bus latency and may decrease the performance of FDP1.
   - YCbCr 4:4:4 interleaved
   - YCbCr 4:4:4 semi-planar
   - YCbCr 4:2:2 interleaved type0 and 1
5. Chroma component (Cb, Cr or U, V) of RPF0, RPF2 is not read from bus in case of YCbCr planar, YCbCr semi planar formats, and discarded after reading in package with luma component in case YcbCr interleaved formats because it is processed in fixed 2D de-interlacing.

In write format case shown in section 24.3.10.1, FD1_WPF_FORMAT.WSPYCS and WSPUVS correspond to RSPYCS and RSPUVS, respectively.

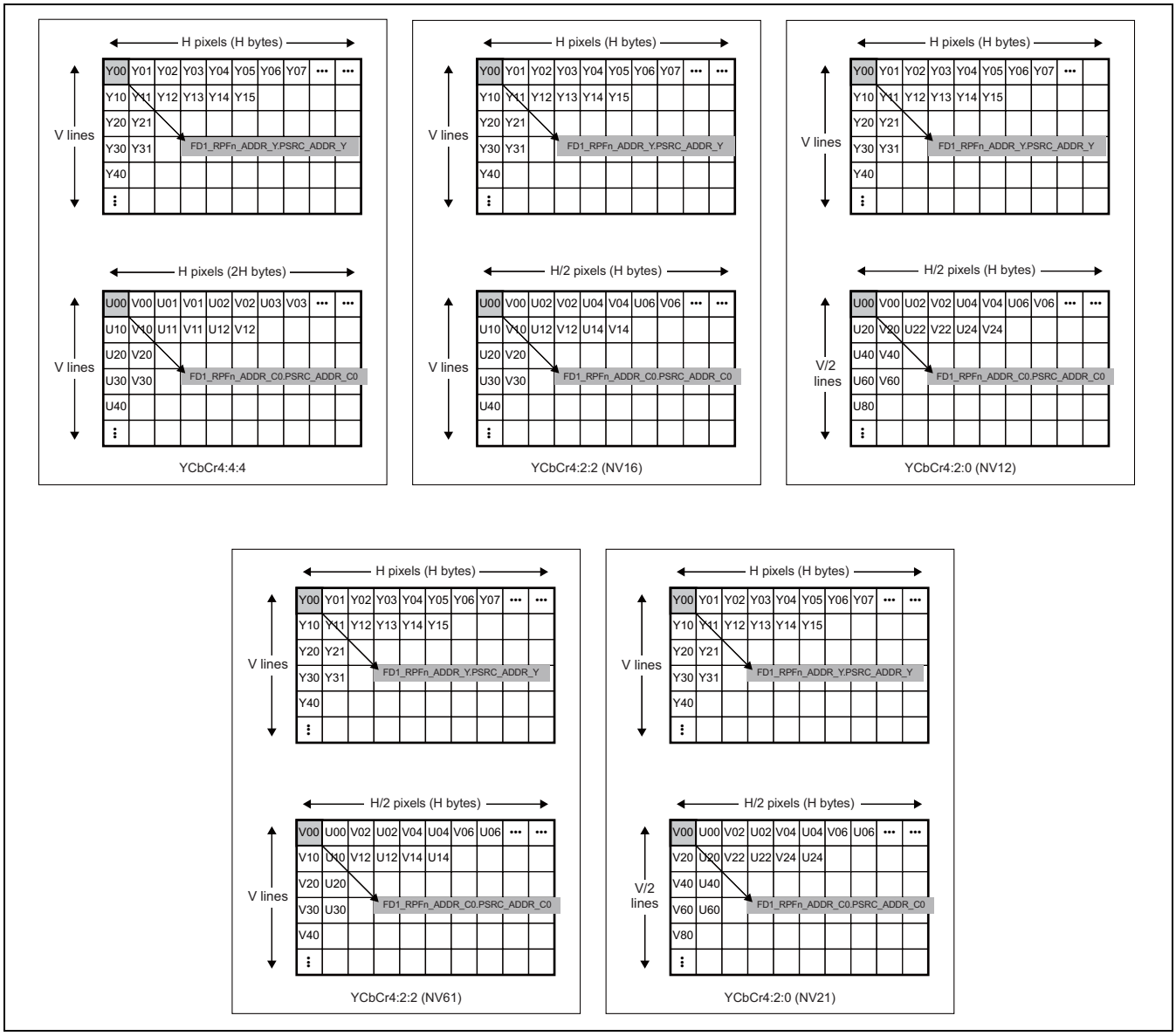


Figure 24.6 YCbCr Semi-Planar Formats

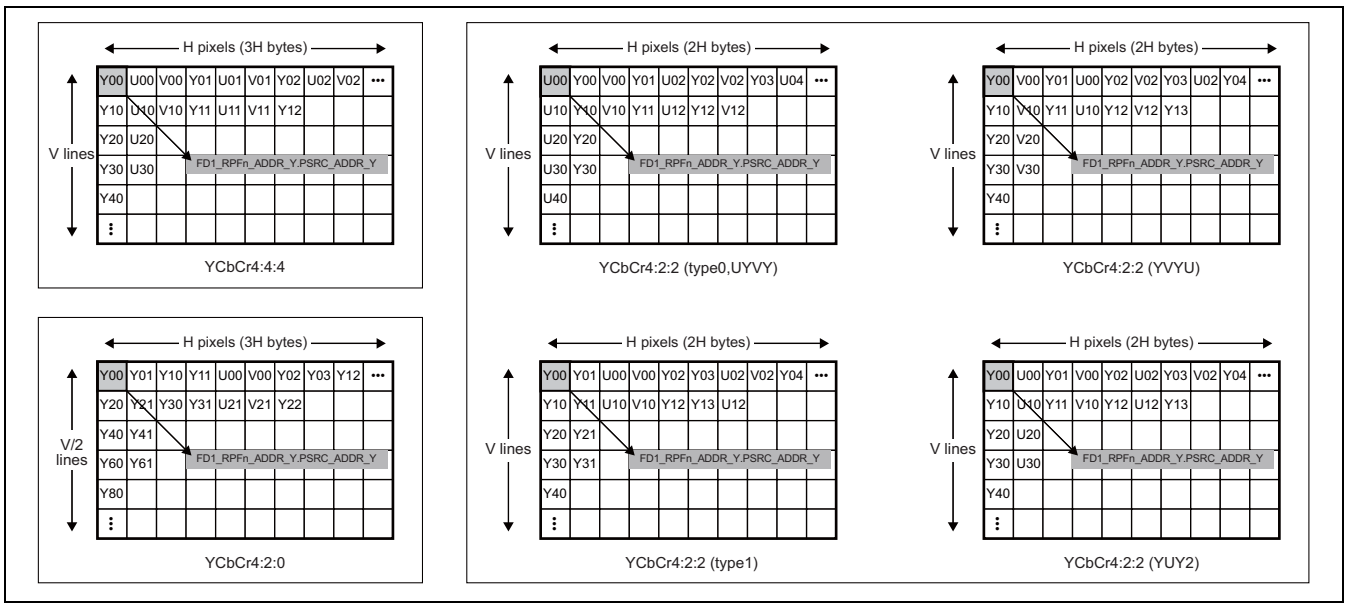


Figure 24.7 YCbCr Interleaved Formats

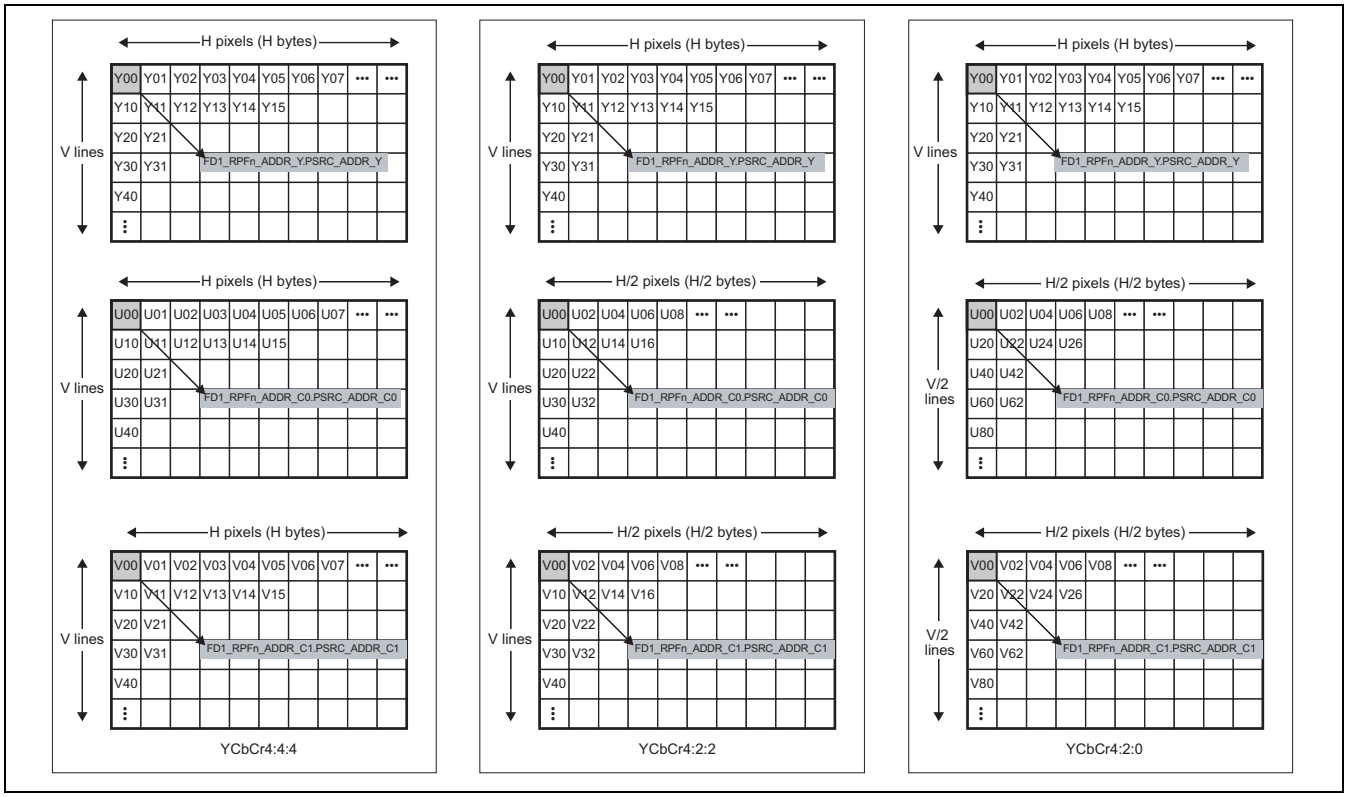
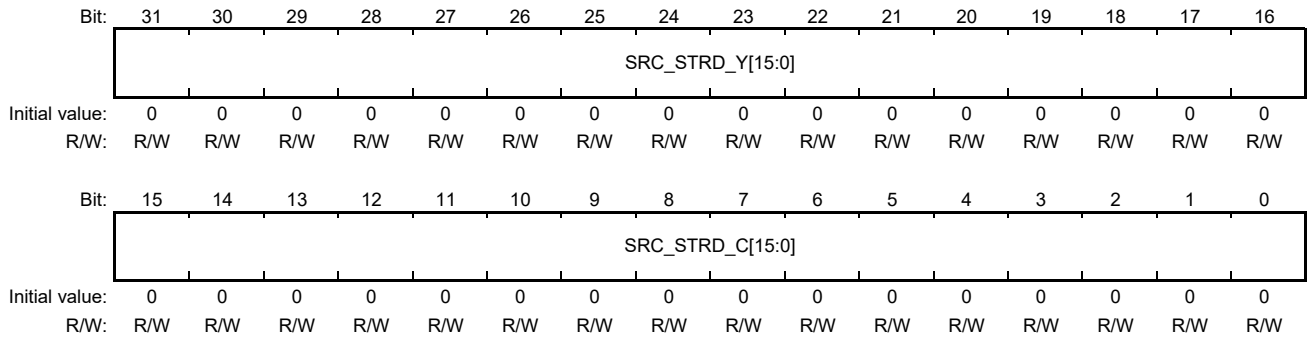


Figure 24.8 YCbCr Planar Formats

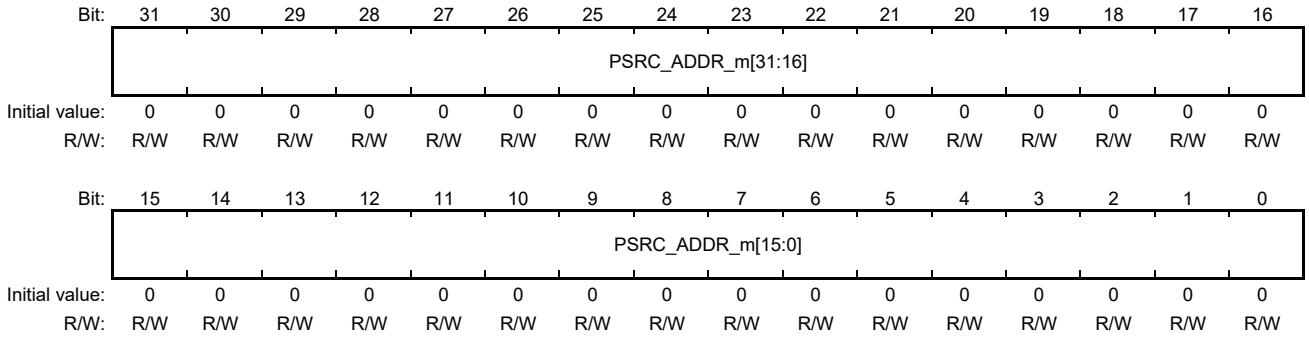
24.3.9.3 Source Picture Stride Register (FD1_RPF_PSTRIDE)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	SRC_STRD_Y [15:0]	H'0000	R/W	Memory Stride of Source Picture Y Plane These bits specify in 1-byte units the memory stride of the source picture Y plane read by the RPFn (n = 0, 1, 2). A value from H'0050 to H'1FFE can be specified.
15 to 0	SRC_STRD_C [15:0]	H'0000	R/W	Memory Stride of Source Picture C Plane These bits specify in 1-byte units the memory stride of the source picture C plane read by the RPF1. A value from H'0050 to H'1FFE can be specified. In the YCbCr planar format, this setting is used as the memory stride of the Cb and Cr planes.

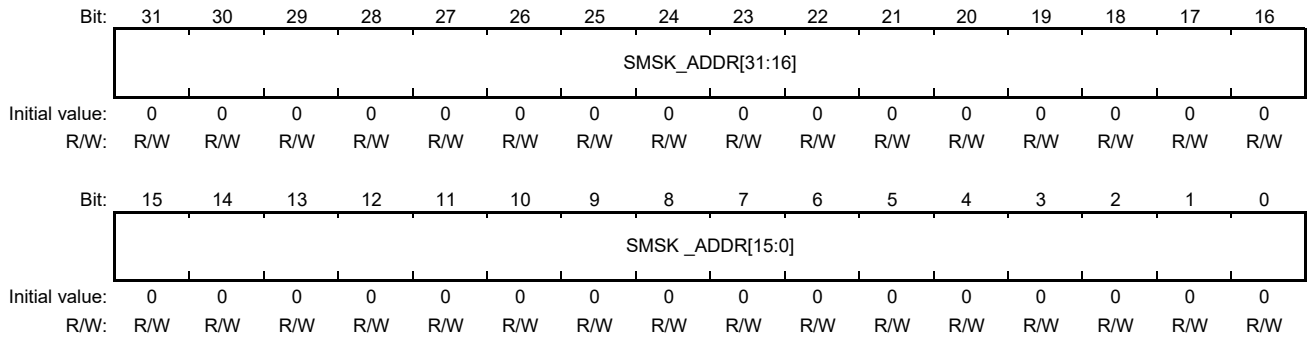
Note: As described above, stride value of source pictures (past, current, future) are common one. Therefore frame structures of all input pictures should be the same format. For example, the case that past picture which is supplied to RPF0 is frame-structure, and other input pictures to RPF1 and 2 are field picture, is prohibited.

24.3.9.4 RPFn Source Component-m Address Register (FD1_RPFn_ADDR_m:{n,m} is one of {0,Y},{1,Y},{1,C0},{1,C1},{2,Y})



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PSRC_ADDR_m [31:0]	H'0000_0000	R/W	RPFn Source Field Address for Component-m ({n,m} is one of {0,Y},{1,Y},{1,C0},{1,C1},{2,Y}) These bits specify in 1-byte units the start address of the source component-m plane read by the RPFn. A value from H'0000_0000 to H'FFFF_FFFF can be specified.

24.3.9.5 Still Mask Address Register (FD1_RPF_SMSK_ADDR)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SMSK_ADDR [31:0]	H'0000_0000	R/W	Still Mask Buffer Address. These bits specify the memory address which the still mask data is located. These bits should be set to a value ranging from H'0000_0000 to H'FFFF_FFFF. The still mask is intermediate data generated during IP conversion only when adaptive 2D/3D (FD1_CTL_OPMODE.PRG = 0 and FD1_CTL_IPC_MODE.DIM [2:0] = 0) is specified. This still mask setting is effective when either of bits FD1_CTL_CHACT.SMW or FD1_CTL_CHACT.SMR is set to 1. The still mask data is generated and repeatedly used by the FDP1. The still mask data should be stored in the SDRAM. The FDP1 needs two separated buffers of the same size for this data, one is common to all top fields and the other is common to all bottom fields. Therefore, the top and bottom fields must have different source addresses. When FD1_RPF_FORMAT.CF is 0, set the buffer address of the top filed in these bits. Otherwise set the buffer address of the bottom filed in these bits. The memory stride of each buffer is expressed as the following equation. 2 × {(FD1_RPF_SIZE.HSIZE + 7)/8} [byte] The memory space of each buffer is expressed as below. 2 × {(FD1_RPF_SIZE.HSIZE + 7)/8} × FD1_RPF_SIZE.VSIZE [byte] The Figure 24.9 shows the usage of the still mask data buffers and Table 24.8 shows how to set this register.

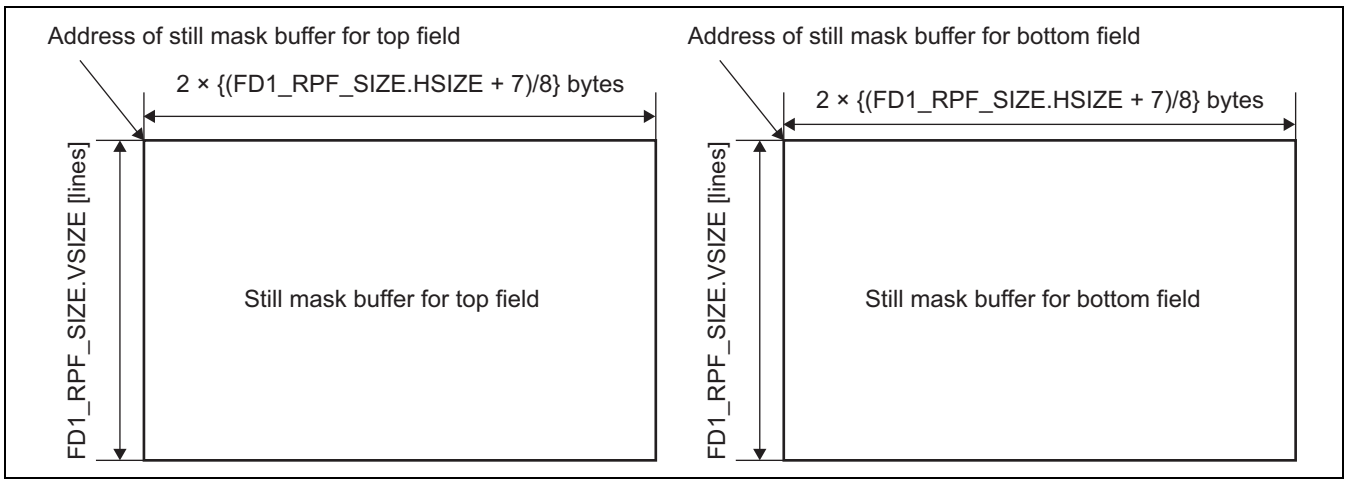


Figure 24.9 Usage of still mask buffers

Table 24.8 Setting of still mask buffer address register

Current Field Parity	FD1_RPF_FORMAT.CF	FD1_RPF_SMSK_ADDR.SMSK_ADDR
Top Field	0	Address of still mask buffer for top field
Bottom Field	1	Address of still mask buffer for bottom field

24.3.9.6 RPF Data Swap Register (FD1_RPF_SWAP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	ISWAP[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	ISWAP[3:0]	H'0	R/W	Input Swap Setting for Image Data This bit field specifies the data swapping function. Each bit corresponds to the following data swapping. Refer to Table 24.9 for the data alignment after data swapping. Bit[3]: Long longword (64-bit) swap Bit[2]: Longword (32-bit) swap Bit[1]: Word (16-bit) swap Bit[0]: Byte (8-bit) swap

Table 24.9 Data Order after Swapping Function

ISWAP[3:0]/OSWAP[3:0]					Changed Order of Data (Each Value Indicates One Byte)															
Bit3	Bit2	Bit1	Bit0	Input →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0	Output →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1		1	0	3	2	5	4	7	6	9	8	11	10	13	12	15	14
0	0	1	0		2	3	0	1	6	7	4	5	10	11	8	9	14	15	12	13
0	0	1	1		3	2	1	0	7	6	5	4	11	10	9	8	15	14	13	12
0	1	0	0		4	5	6	7	0	1	2	3	12	13	14	15	8	9	10	11
0	1	0	1		5	4	7	6	1	0	3	2	13	12	15	14	9	8	11	10
0	1	1	0		6	7	4	5	2	3	0	1	14	15	12	13	10	11	8	9
0	1	1	1		7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
1	0	0	0		8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
1	0	0	1		9	8	11	10	13	12	15	14	1	0	3	2	5	4	7	6
1	0	1	0		10	11	8	9	14	15	12	13	2	3	0	1	6	7	4	5
1	0	1	1		11	10	9	8	15	14	13	12	3	2	1	0	7	6	5	4
1	1	0	0		12	13	14	15	8	9	10	11	4	5	6	7	0	1	2	3
1	1	0	1		13	12	15	14	9	8	11	10	5	4	7	6	1	0	3	2
1	1	1	0		14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1
1	1	1	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

24.3.10 WPF Control Registers

24.3.10.1 Destination Picture Format Register (FD1_WPF_FORMAT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PDV[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WSPYCS	WSPUVS	DITH[1:0]		WRTM[2:0]			CSC	—	WRFMT[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PDV[7:0]	H'00	R/W	PAD Value in Output Packed Data These bits specify the value to be stored in the bit field indicated as PAD or P in the output formats shown in Table 24.7. A value from 0 to 255 can be specified.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	WSPYCS	0	R/W	WPF Output Mode Setting 1 When the output format is YUY2, set this bit to 1 and set the WRFMT bits to 71 (H'47). When the output format is YVYU, set this bit and the WSPUVS bit to 1 and set the WRFMT bits to 71 (H'47). In other cases, set this bit to 0.
14	WSPUVS	0	R/W	WPF Output Mode Setting 2 When the output format is NV61, set this bit to 1 and set the WRFMT bits to 65 (H'41). When the output format is NV21, set this bit to 1 and set the WRFMT bits to 66 (H'42). When the output format is YVYU, set this bit and the WSPYCS bit to 1 and set the WRFMT bits to 71 (H'47). In other cases, set this bit to 0.
13, 12	DITH[1:0]	00	R/W	Dithering Enable/Disable When the output format specified through the WRFMT bits is RGB with 18 bpp (262144 colors) or less, the color reduction processing is applied to match the number of colors. The color reduction processing may generate the artifacts of pseudo gradation, which can be suppressed through dithering. The DITH bits enable or disable dithering during color reduction. When the output format specified through the WRFMT bits is YCbCr, specify 0 in these bits. 00: Dithering is disabled 01: Setting prohibited 10: Setting prohibited 11: Dithering is enabled

Bit	Bit Name	Initial Value	R/W	Description
11 to 9	WRTM[2:0]	000	R/W	CSC Conversion Expression Setting These bits select the expression for color space conversion. The conversion direction is RGB to YCbCr when the format specified in the WRFMT bits is RGB, or YCbCr to RGB when the format is YCbCr. 000: BT.601 YCbCr [16,235/240] → RGB [0,255] 001: BT.601 YCbCr [0,255] → RGB [0,255] 010: BT.709 YCbCr [16,235/240] → RGB [0,255] 011: BT.709 YCbCr [16,235/240] → RGB [16,235] 100 to 111: Setting prohibited
8	CSC	0	R/W	Color Space Conversion Setting Enables or disables YCbCr ↔ RGB color space conversion to be executed in the WPF. The characteristics of color space conversion are determined by the WRTM setting. 0: Color space is not converted. 1: Color space is converted.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	WRFMT[6:0]	H'00	R/W	WPF Output Image Format Setting These bits select the format of the image output from the WPF to the external memory from among those listed in Table 24.10 and Table 24.7. Note: Number of output pixels When YCbCr4:2:2 is specified through WRFMT, the horizontal size of the output image should be a multiple of 2 pixels. When YCbCr4:2:0 is specified, the vertical and horizontal sizes of the output image should be multiples of 2 pixels.

Table 24.10 Packed RGB Formats for WPF Output

WRFMT	Bit per pixel	Phase	Bit field																													
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H'00	8	—	R0	R0	R0	G0	G0	G0	B0	B0	R1	R1	R1	G1	G1	G1	B1	B1	R2	R2	R2	G2	G2	G2	B2	B2	R3	R3	R3	G3	G3	G3	B3	B3
H'01	12	—	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'02		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	0	0	0	0
H'03	—	—	Reserved								Reserved								Reserved								Reserved							
H'04	15	—	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'05		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	0
H'06	16	—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'07	18	—	PAD0								0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'08		—	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	PAD0							
H'09		—	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	PAD0							
H'0A		—	PAD0								R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0
H'0B		—	PAD0								0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0
H'0C		—	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	PAD0							
H'0D		—	PAD0								R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0
H'0E		—	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	PAD0							
H'0F		0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1
		1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2
		2	G2	G2	B2	B2	B2	B2	B2	B2	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3
H'10		0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1	R1	R1	R1	R1	G1	G1
		1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	B2	B2	B2	B2
		2	B2	B2	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	0	0	0	0	0	0
H'11		0	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1
		1	0	0	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2
		2	0	0	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3
H'12		0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	0	0
		1	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	0	0
		2	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	0	0
H'13	24	—	PAD0								R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
H'14		—	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	PAD0							
H'15		0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
		1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
		2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
H'16	18	—	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	0	0	0	0	0	0	0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'17		—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'18	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
		1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
		2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
H'19	12	—	PAD0				R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD1				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'1A		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD0				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	PAD1			
H'1B	15	—	P0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	P1	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'1C		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	P0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	P1
H'1D	12	—	PAD0				B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD1				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1
H'1E		—	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD0				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	PAD1			
H'1F	15	—	P0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P1	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1
H'20		—	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P0	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	P1
H'21	18	0	0	0	B0	B0	B0	B0	B0	B0	0	0	G0	G0	G0	G0	G0	G0	0	0	R0	R0	R0	R0	R0	R0	0	0	B1	B1	B1	B1	B1	B1
		1	0	0	G1	G1	G1	G1	G1	G1	0	0	R1	R1	R1	R1	R1	R1	0	0	B2	B2	B2	B2	B2	B2	0	0	G2	G2	G2	G2	G2	G2
		2	0	0	R2	R2	R2	R2	R2	R2	0	0	B3	B3	B3	B3	B3	B3	0	0	G3	G3	G3	G3	G3	G3	0	0	R3	R3	R3	R3	R3	R3
H'22	24	—	PAD0								B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0
H'23	16	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0
H'24~H'3F	—	—	Reserved								Reserved								Reserved								Reserved							

Refer to Table 24.7 for YCbCr formats.

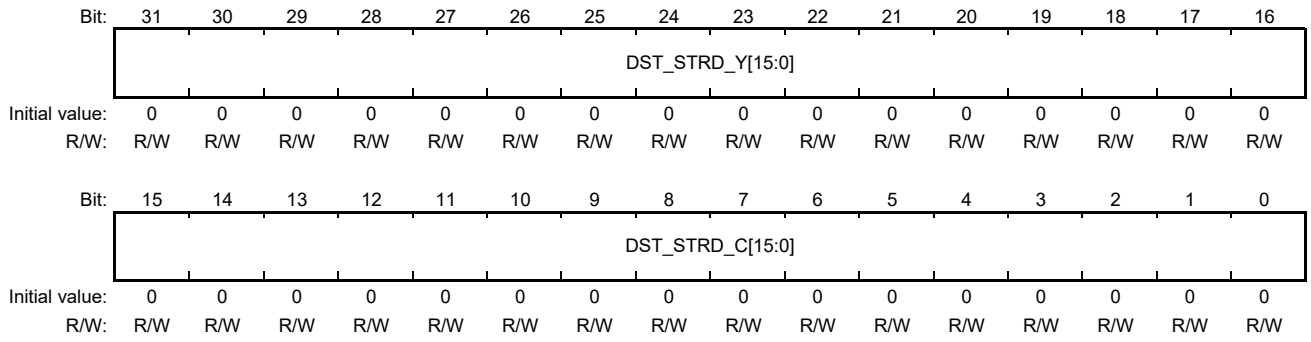
24.3.10.2 Destination Picture Rounding Control Register (FD1_WPF_RNDCTL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBRM	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLMD[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

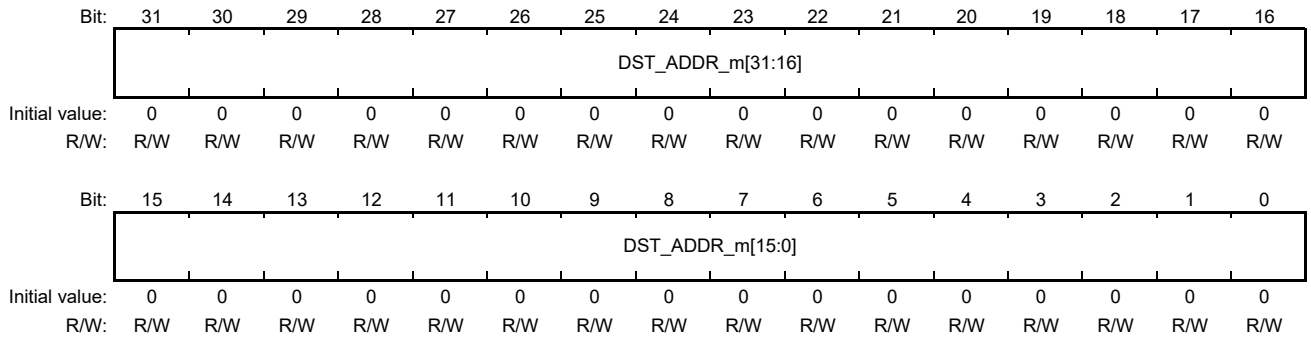
Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	CBRM	0	R/W	Bit Count Reduction Selection for Data Storage in Packed RGB This bit specifies the method for reducing the number of bits when data is stored in the bit fields indicated as R, G, and B in Table 24.10 and the target bit fields are not eight bits. 0: Bit count conversion: The lower-order bits are truncated 1: Bit count conversion: Rounding (rounding off)
27 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13, 12	CLMD[1:0]	00	R/W	Color Data Clipping These bits specify the method for clipping the YCbCr color data output from the WPF. When RGB color data is output from the WPF, specify 0 in these bits. 00: Output value is not clipped (0-255) 01: Output value is clipped: YCbCr mode 1 (16-235 (Y), 16-240 (Cb/Cr)) 10: Output value is clipped: YCbCr mode 2 (Y/Cb/Cr = 1-254) 11: Setting prohibited
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

24.3.10.3 Destination Picture Stride Register (FD1_WPF_PSTRIDE)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DST_STRD_Y [15:0]	H'0000	R/W	Memory Stride of Destination Picture Y/RGB Plane These bits specify in 1-byte units the memory stride of the destination picture in the external memory to be written to by the WPF. A value from H'0050 to H'1FFE can be specified.
15 to 0	DST_STRD_C [15:0]	H'0000	R/W	Memory Stride of Destination Picture C Plane These bits specify in 1-byte units the memory stride for the C plane of the destination picture in the external memory to be written to by the WPF. When the WPF outputs images in an RGB format, this setting is not used. When the WPF outputs images in YCbCr planar format, this setting is applied to both the Cb and Cr planes. A value from H'0050 to H'1FFE can be specified.

24.3.10.4 Destination Component-m Address Register (FD1_WPF_ADDR_m: m = Y, C0, C1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DST_ADDR_m [31:0]	H'0000_0000	R/W	Destination Address for Component-m (m = Y, C0, C1) These bits specify in 1-byte units the address for storing the destination component-m plane to be written to the external memory by the WPF. A value from H'0000_0000 to H'FFFF_FFFF can be specified.

24.3.10.5 WPF Data Swap Register (FD1_WPF_SWAP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SSWAP[3:0]				OSWAP[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	SSWAP[3:0]	H'0	R/W	Set the same value with FD1_RPF_SWAP.ISWAP.
3 to 0	OSWAP[3:0]	H'0	R/W	Output Swap Setting for Image Data This bit field specifies the data swapping function. Each bit corresponds to the following data swapping. Refer to Table 24.8 for the data alignment after data swapping. Bit[3]: Long longword (64-bit) swap Bit[2]: Longword (32-bit) swap Bit[1]: Word (16-bit) swap Bit[0]: Byte (8-bit) swap

24.3.11 IPC Control Registers

Table 24.11 shows registers categorized in function of IPC.

Table 24.11 IPC registers categorized in function

Function	Registers
IP Conversion Control	FD1_IPC_MODE
3D de-interlace	FD1_IPC_COMB_DET
Adaptive 2D/3D de-interlacing	FD1_IPC_MOTDEC
Diagonal line interpolation	FD1_IPC_DLI_BLEND
	FD1_IPC_DLI_HGAIN
	FD1_IPC_DLI_SPRS
	FD1_IPC_DLI_ANGLE
	FD1_IPC_DLI_ISOPIX0
	FD1_IPC_DLI_ISOPIX1
Film detection	FD1_SENSOR_m (m = 0, 1,…, 17)
	FD1_SENSOR_CTL0
	FD1_SENSOR_CTL1
	FD1_SENSOR_CTL2
	FD1_SENSOR_CTL3
	SENSOR_TH0
	SENSOR_TH1

For chroma component, IPC cannot process 3D de-interlace, adaptive 2D/3D de-interlacing, diagonal line interpolation and film detection but can process fixed 2D IP conversion.

24.3.11.1 IPC Mode Register (FD1_IPC_MODE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DLI	—	—	—	—	—	DIM[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DLI	0	R/W	Set the value 1 to this bit.
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	DIM[2:0]	000	R/W	De-Interlacing Mode of luma component as following These bits specify the de-interlacing mode. 000: Adaptive 2D/3D de-interlacing 001: Fixed 2D de-interlacing 010: Fixed 3D de-interlacing 011: Select previous field for interpolated lines 100: Select next field for interpolated lines The de-interlacing process of chroma component is fixed 2D de-interlacing regardless of these bits.

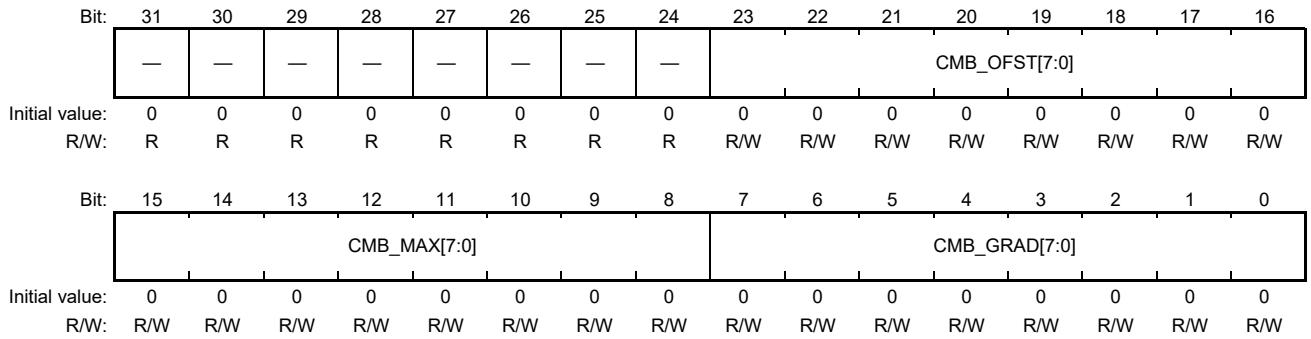
24.3.11.2 Still Mask Threshold Register (FD1_IPC_SMSK_THRESH)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FSM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SMSK_TH[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

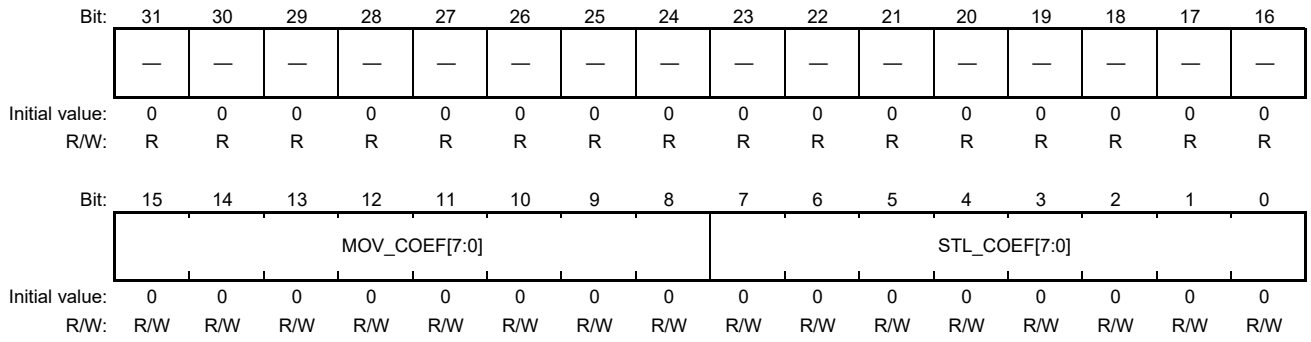
Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	FSM0	0	R/W	Set the value 1 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	SMSK_TH [7:0]	H'00	R/W	Set the value 2 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.3 Comb Detection Parameter Register (FD1_IPC_COMB_DET)



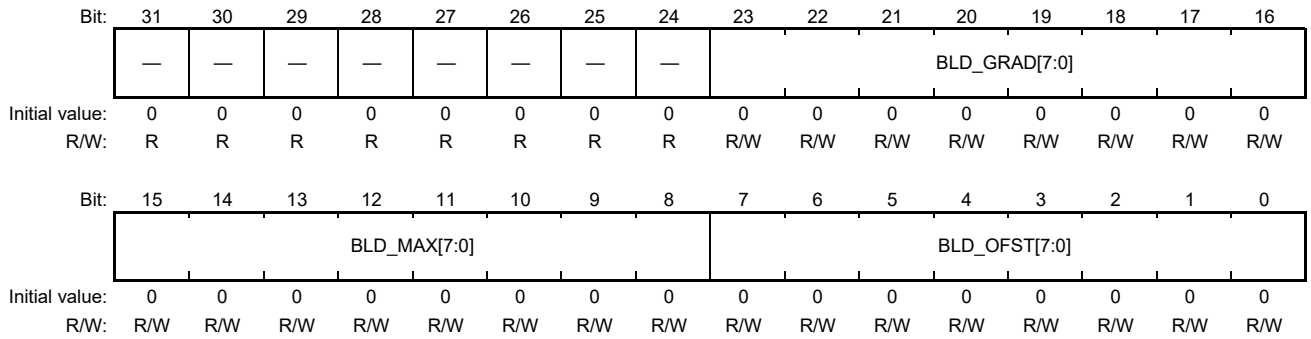
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	CMB_OFST [7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	CMB_ MAX [7:0]	H'00	R/W	Set the value 0 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	CMB_GRAD [7:0]	H'00	R/W	Set the value H'40 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.4 Motion Decision Parameter Register (FD1_IPC_MOTDEC)



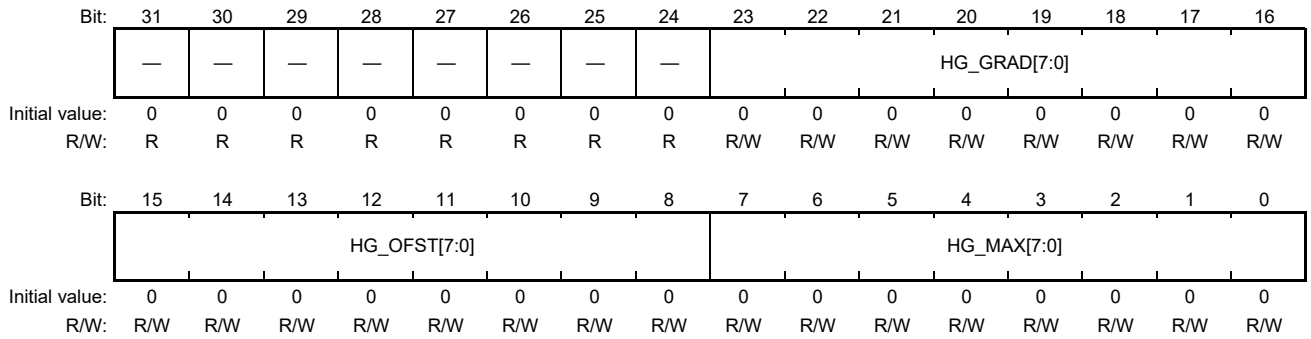
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	MOV_COEF [7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	STL_COEF [7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.5 DLI Blend Parameter Register (FD1_IPC_DLI_BLEND)



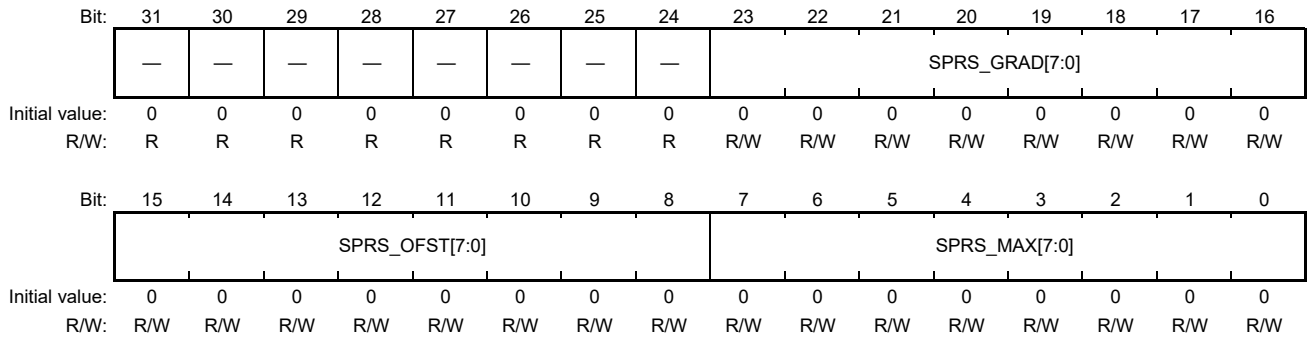
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	BLD_GRAD [7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	BLD_MAX [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	BLD_OFST [7:0]	H'00	R/W	Set the value H'02 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.6 DLI Horizontal Frequency Gain Register (FD1_IPC_DLI_HGAIN)



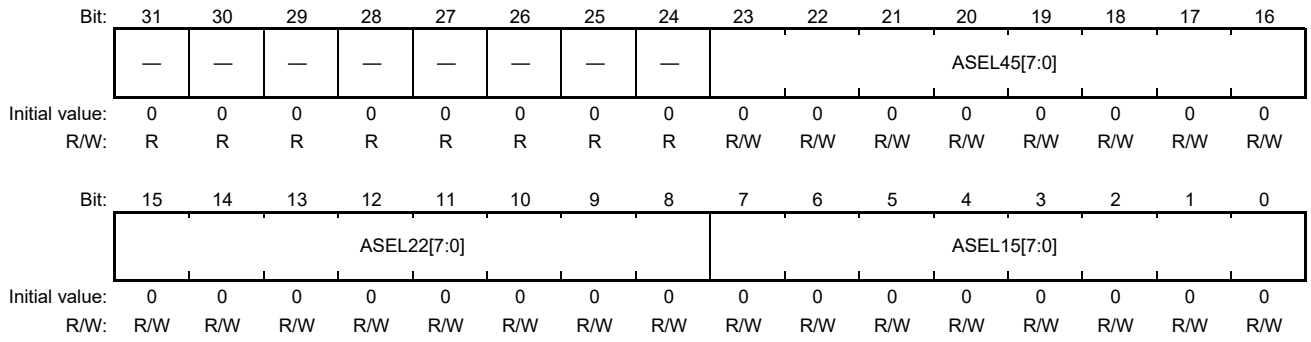
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HG_GRAD [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	HG_OFST [7:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	HG_MAX [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.7 DLI Suppression Parameter register (FD1_IPC_DLI_SPRS)



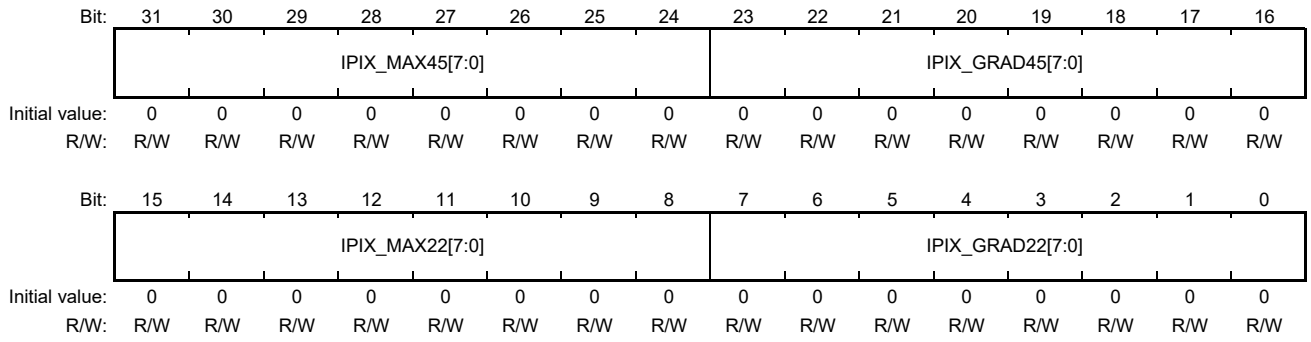
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	SPRS_GRAD [7:0]	H'00	R/W	Set the value H'90 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	SPRS_OFST [7:0]	H'00	R/W	Set the value H'04 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	SPRS_MAX [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.8 DLI Angle Parameter Register (FD1_IPC_DLI_ANGLE)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	ASEL45[7:0]	H'00	R/W	Set the value H'04 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	ASEL22[7:0]	H'00	R/W	Set the value H'08 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	ASEL15[7:0]	H'00	R/W	Set the value H'0C to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.9 DLI Isolated Pixel Parameter Register 0 (FD1_IPC_DLI_ISOPIX0)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	IPIX_MAX45 [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
23 to 16	IPIX_GRAD45 [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	IPIX_MAX22 [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	IPIX_GRAD22 [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

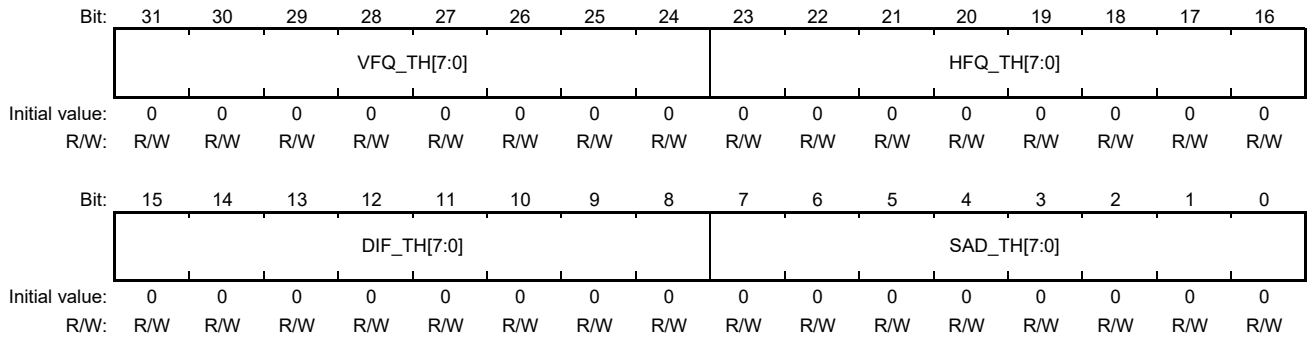
24.3.11.10 DLI Isolated Pixel Parameter Register 1 (FD1_IPC_DLI_ISOPIX1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	IPIX_MAX15[7:0]								IPIX_GRAD15[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

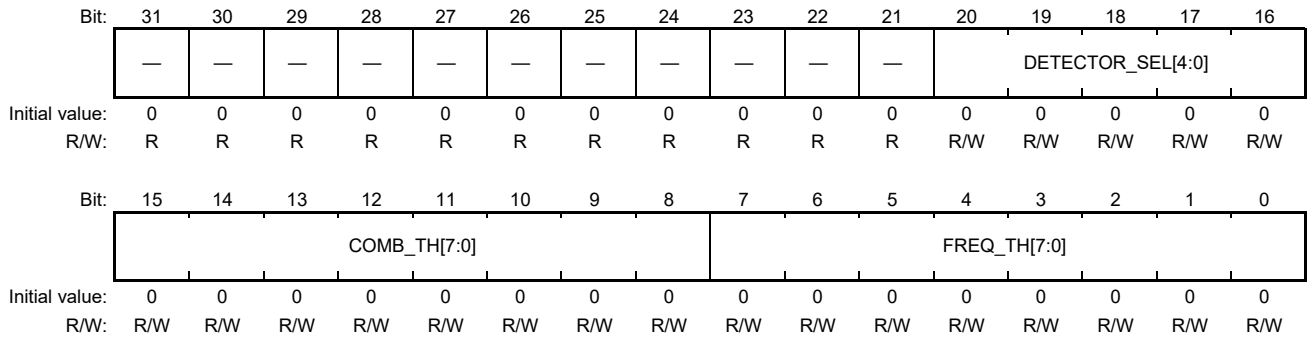
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	IPIX_MAX15 [7:0]	H'00	R/W	Set the value H'FF to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	IPIX_GRAD15 [7:0]	H'00	R/W	Set the value H'10 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.11 IPC Sensor Threshold Register 0 (FD1_IPC_SENSOR_TH0)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	VFQ_TH[7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
23 to 16	HFQ_TH[7:0]	H'00	R/W	Set the value H'20 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	DIF_TH[7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	SAD_TH[7:0]	H'00	R/W	Set the value H'80 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.12 IPC Sensor Threshold Register 1 (FD1_IPC_SENSOR_TH1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	DETECTOR_SEL[4:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 8	COMB_TH[7:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 0	FREQ_TH[7:0]	H'00	R/W	Set the value H'00 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.13 Sensor Control Register 0 (FD1_SENSOR_CTL0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRM_LVTH[3:0]				FLD_LVTH[3:0]				—	—	—	—	—	—	—	FD_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 12	FRM_LVTH [3:0]	H'0	R/W	Set the value 2 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
11 to 8	FLD_LVTH [3:0]	H'0	R/W	Set the value 2 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	FD_EN	0	R/W	Set the value 1 to this bit.

24.3.11.14 Sensor Control Register 1 (FD1_SENSOR_CTL1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	XS[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YS[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	XS[12:0]	H'0000	R/W	Set the value H'0000 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YS[12:0]	H'0000	R/W	Set the value H'0000 to this bit. Other setting value is used for purpose of h/w debugging. Do not set other value.

24.3.11.15 Sensor Control Register 2 (FD1_SENSOR_CTL2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	XE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	YE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	XE[12:0]	H'0000	R/W	Set the value (FD1_RPF_SIZE.HSIZE – 1) to this bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	YE[12:0]	H'0000	R/W	Set the value (FD1_RPF_SIZE.VSIZE – 1) to this bit if input picture is progressive. Set the value (FD1_RPF_SIZE.VSIZE × 2 – 1) to this bit if input picture is interlaced.

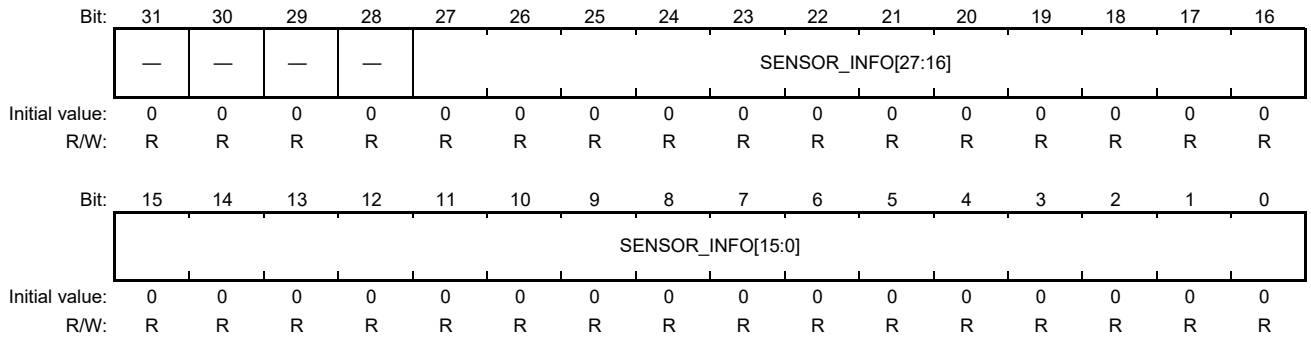
24.3.11.16 Sensor Control Register 3 (FD1_SENSOR_CTL3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	POSX0[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	POSX1[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

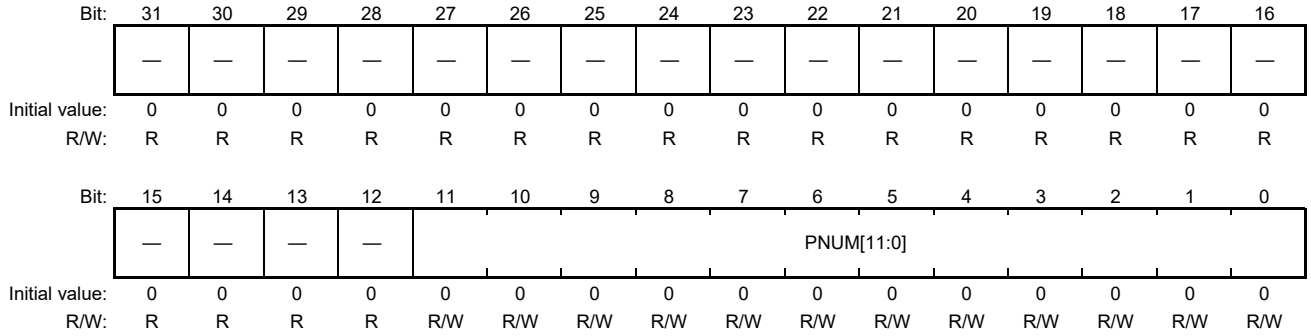
Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	POSX0[12:0]	H'0000	R/W	Set the value INT (FD1_RPF_SIZE.HSIZE/3) to this bit.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	POSX1[12:0]	H'0000	R/W	Set the value INT (2 × FD1_RPF_SIZE.HSIZE/3) to this bit.

24.3.11.17 Sensor Register (FD1_SENSOR_m: m = 0, 1, … 17)



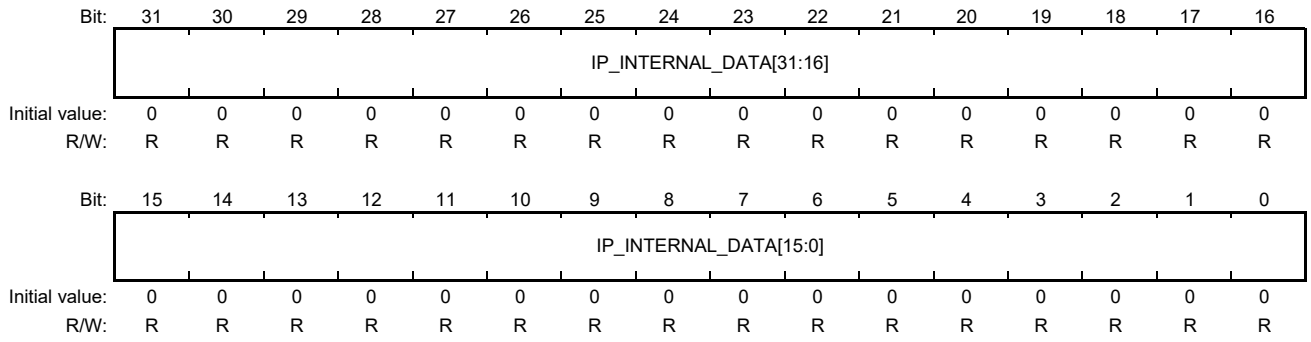
Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 0	SENSOR_INFO[27:0]	H'000 0000	R	Sensor information of FDP1

24.3.11.18 Line Memory Pixel Number Register (FD1_IPC_LMEM)



Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	PNUM[11:0]	H'000	R/W	Specify 1024 in decimal (H'400)

24.3.11.19 IP Internal Data Register (FD1_IP_INDATA)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	IP_INTERNAL_DATA [31:0]	All 0	R	Internal data

24.4 Input/Output Data Format

The FDP1 input/output data should be stored in a format where the address is incremented in the direction from the MSB to the LSB as in big endian. For example, the FDP1 reads and writes data to and from the external memory through the dedicated bus interface with a 128-bit width, and the data that should come first should be stored in the MSB side regardless of the unit data size as shown in Figure 24.10.

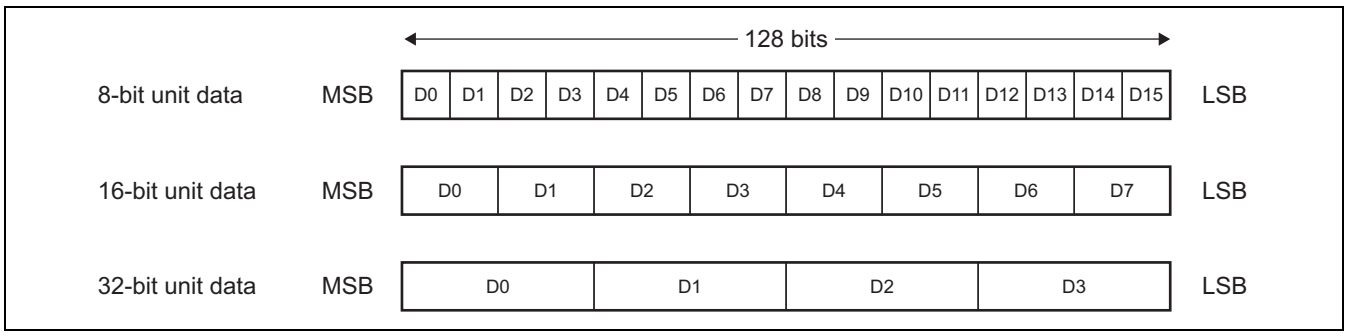


Figure 24.10 FDP1 Input/Output Data Format

However, data may be arranged in a way unexpected by the FDP1 depending on the address handling method (such as little endian) of the FDP1 access destination in some cases as in the external memory format shown in Figure 24.11. In such a case, use the data swapping function (refer to sections 24.3.9.6 and 24.3.10.5) in the FDP1 to convert the data format to be suitable for the FDP1.

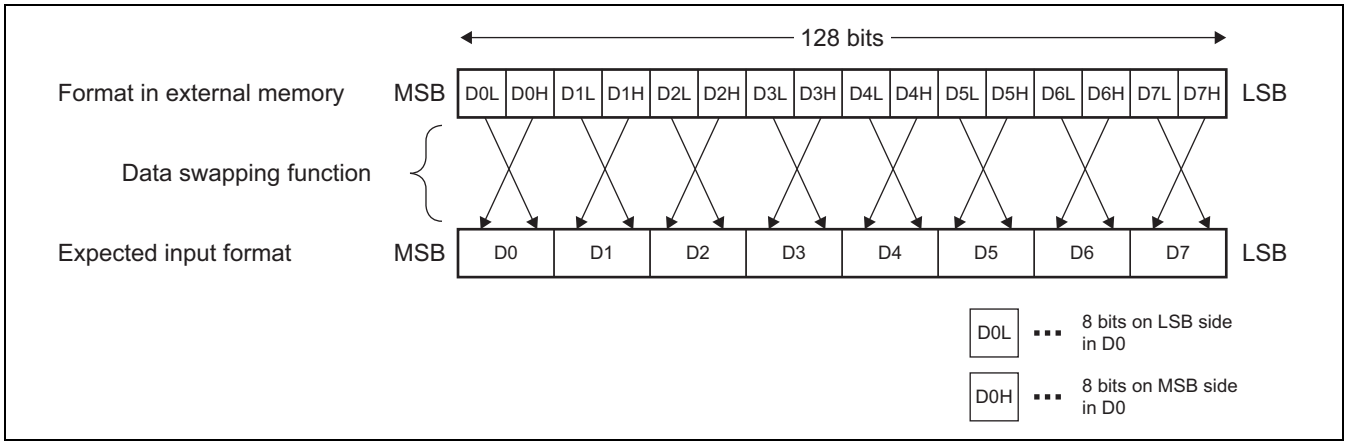


Figure 24.11 Input Data Alignment by Data Swapping Function

24.5 Lookup Table (LUT) Setting

FDP1 has the lookup tables (LUT) shown in Table 24.12 to change the characteristic of the de-interlacing function. The LUT is an 8-bit entry and 8-bit output table. Note that users can access to LUT only by 32 bits access. Do not access other bit length such as 8 bits access or 16 bits access. LUT behaves like immediate registers described in section 24.3.2, so do not change the value in LUT while FDP1 is under processing.

Table 24.12 List of LUT

LUT Name
DIF_ADJ
SAD_ADJ
BLD_GAIN
DIF_GAIN
MDET

The LUT is used for making the non-linear characteristic shown in Figure 24.12 where X and Y are input and output of LUT respectively.

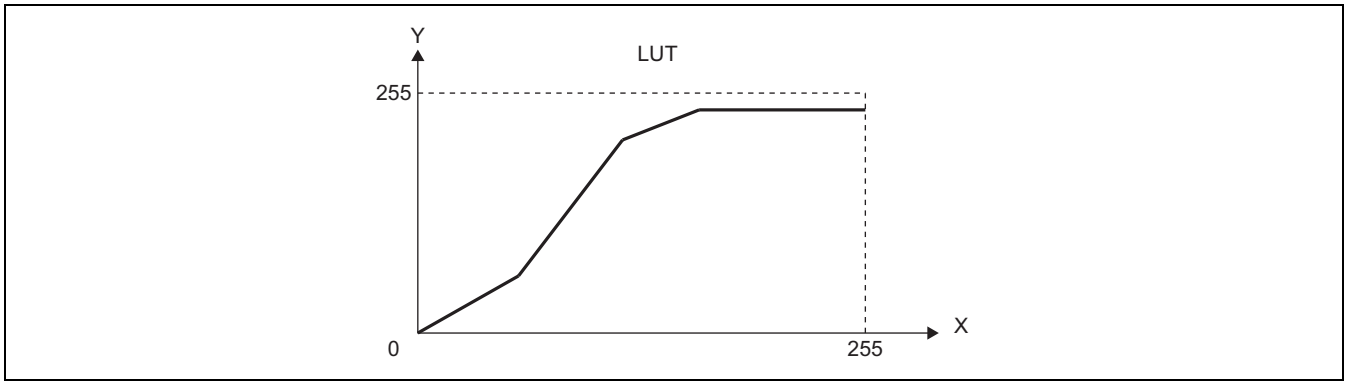


Figure 24.12 LUT for Changing the De-Interlacing Characteristic

For MDET-LUT, the 2D interpolating likelihood is the input to the LUT and the blending coefficient (Alpha) is the output from the LUT. The final output image is expressed by the following equation.

(Output image) = (Alpha/255) × (2D interpolated image) + ((255-Alpha)/255) × (3D interpolated image)

When the output value of the LUT is set to 0 for all input value, the output image from FDP1 is always 3D interpolated image in spite of the motion in the video.

Table 24.13 indicates the setting of each LUT. Note that other setting is used for purpose of h/w debugging. Do not set other value to LUT except for MDET.

Table 24.13 Meaning of X/Y Axis of LUT

Index	DIF_ADJ[ ]	SAD_ADJ[ ]	BLD_GAIN[ ]	DIF_GAIN[ ]	MDET[ ]
0	H'00	H'00	H'80	H'80	H'00
1	H'24	H'24	H'80	H'80	H'01
2	H'43	H'43	H'80	H'80	H'02
3	H'5E	H'5E	H'80	H'80	H'03
4	H'76	H'76	H'80	H'80	H'04
5	H'8C	H'8C	H'80	H'80	H'05
6	H'9E	H'9E	H'80	H'80	H'06
7	H'AF	H'AF	H'80	H'80	H'07
8	H'BD	H'BD	H'80	H'80	H'08
9	H'C9	H'C9	H'80	H'80	H'09
10	H'D4	H'D4	H'80	H'80	H'0A
11	H'DD	H'DD	H'80	H'80	H'0B
12	H'E4	H'E4	H'80	H'80	H'0C
13	H'EA	H'EA	H'80	H'80	H'0D
14	H'EF	H'EF	H'80	H'80	H'0E
15	H'F3	H'F3	H'80	H'80	H'0F
16	H'F6	H'F6	H'80	H'80	H'10
17	H'F9	H'F9	H'80	H'80	H'11
18	H'FB	H'FB	H'80	H'80	H'12
19	H'FC	H'FC	H'80	H'80	H'13
20	H'FD	H'FD	H'80	H'80	H'14
21	H'FE	H'FE	H'80	H'80	H'15
22	H'FE	H'FE	H'80	H'80	H'16
23	H'FF	H'FF	H'80	H'80	H'17
24	H'FF	H'FF	H'80	H'80	H'18
25	H'FF	H'FF	H'80	H'80	H'19
26	H'FF	H'FF	H'80	H'80	H'1A
27	H'FF	H'FF	H'80	H'80	H'1B
28	H'FF	H'FF	H'80	H'80	H'1C
29	H'FF	H'FF	H'80	H'80	H'1D
30	H'FF	H'FF	H'80	H'80	H'1E
31	H'FF	H'FF	H'80	H'80	H'1F
32	H'FF	H'FF	H'80	H'80	H'20
33	H'FF	H'FF	H'80	H'80	H'21
34	H'FF	H'FF	H'80	H'80	H'22
35	H'FF	H'FF	H'80	H'80	H'23
36	H'FF	H'FF	H'80	H'80	H'24
37	H'FF	H'FF	H'80	H'80	H'25
38	H'FF	H'FF	H'80	H'80	H'26
39	H'FF	H'FF	H'80	H'80	H'27
40	H'FF	H'FF	H'80	H'80	H'28
41	H'FF	H'FF	H'80	H'80	H'29

Index	DIF_ADJ[ ]	SAD_ADJ[ ]	BLD_GAIN[ ]	DIF_GAIN[ ]	MDET[ ]
42	H'FF	H'FF	H'80	H'80	H'2A
43	H'FF	H'FF	H'80	H'80	H'2B
44	H'FF	H'FF	H'80	H'80	H'2C
45	H'FF	H'FF	H'80	H'80	H'2D
46	H'FF	H'FF	H'80	H'80	H'2E
47	H'FF	H'FF	H'80	H'80	H'2F
48	H'FF	H'FF	H'80	H'80	H'30
49	H'FF	H'FF	H'80	H'80	H'31
50	H'FF	H'FF	H'80	H'80	H'32
51	H'FF	H'FF	H'80	H'80	H'33
52	H'FF	H'FF	H'80	H'80	H'34
53	H'FF	H'FF	H'80	H'80	H'35
54	H'FF	H'FF	H'80	H'80	H'36
55	H'FF	H'FF	H'80	H'80	H'37
56	H'FF	H'FF	H'80	H'80	H'38
57	H'FF	H'FF	H'80	H'80	H'39
58	H'FF	H'FF	H'80	H'80	H'3A
59	H'FF	H'FF	H'80	H'80	H'3B
60	H'FF	H'FF	H'80	H'80	H'3C
61	H'FF	H'FF	H'80	H'80	H'3D
62	H'FF	H'FF	H'80	H'80	H'3E
63	H'FF	H'FF	H'80	H'80	H'3F
64	H'FF	H'FF	H'80	H'80	H'40
65	H'FF	H'FF	H'80	H'80	H'41
66	H'FF	H'FF	H'80	H'80	H'42
67	H'FF	H'FF	H'80	H'80	H'43
68	H'FF	H'FF	H'80	H'80	H'44
69	H'FF	H'FF	H'80	H'80	H'45
70	H'FF	H'FF	H'80	H'80	H'46
71	H'FF	H'FF	H'80	H'80	H'47
72	H'FF	H'FF	H'80	H'80	H'48
73	H'FF	H'FF	H'80	H'80	H'49
74	H'FF	H'FF	H'80	H'80	H'4A
75	H'FF	H'FF	H'80	H'80	H'4B
76	H'FF	H'FF	H'80	H'80	H'4C
77	H'FF	H'FF	H'80	H'80	H'4D
78	H'FF	H'FF	H'80	H'80	H'4E
79	H'FF	H'FF	H'80	H'80	H'4F
80	H'FF	H'FF	H'80	H'80	H'50
81	H'FF	H'FF	H'80	H'80	H'51
82	H'FF	H'FF	H'80	H'80	H'52
83	H'FF	H'FF	H'80	H'80	H'53
84	H'FF	H'FF	H'80	H'80	H'54
85	H'FF	H'FF	H'80	H'80	H'55

Index	DIF_ADJ[ ]	SAD_ADJ[ ]	BLD_GAIN[ ]	DIF_GAIN[ ]	MDET[ ]
86	H'FF	H'FF	H'80	H'80	H'56
87	H'FF	H'FF	H'80	H'80	H'57
88	H'FF	H'FF	H'80	H'80	H'58
89	H'FF	H'FF	H'80	H'80	H'59
90	H'FF	H'FF	H'80	H'80	H'5A
91	H'FF	H'FF	H'80	H'80	H'5B
92	H'FF	H'FF	H'80	H'80	H'5C
93	H'FF	H'FF	H'80	H'80	H'5D
94	H'FF	H'FF	H'80	H'80	H'5E
95	H'FF	H'FF	H'80	H'80	H'5F
96	H'FF	H'FF	H'80	H'80	H'60
97	H'FF	H'FF	H'80	H'80	H'61
98	H'FF	H'FF	H'80	H'80	H'62
99	H'FF	H'FF	H'80	H'80	H'63
100	H'FF	H'FF	H'80	H'80	H'64
101	H'FF	H'FF	H'80	H'80	H'65
102	H'FF	H'FF	H'80	H'80	H'66
103	H'FF	H'FF	H'80	H'80	H'67
104	H'FF	H'FF	H'80	H'80	H'68
105	H'FF	H'FF	H'80	H'80	H'69
106	H'FF	H'FF	H'80	H'80	H'6A
107	H'FF	H'FF	H'80	H'80	H'6B
108	H'FF	H'FF	H'80	H'80	H'6C
109	H'FF	H'FF	H'80	H'80	H'6D
110	H'FF	H'FF	H'80	H'80	H'6E
111	H'FF	H'FF	H'80	H'80	H'6F
112	H'FF	H'FF	H'80	H'80	H'70
113	H'FF	H'FF	H'80	H'80	H'71
114	H'FF	H'FF	H'80	H'80	H'72
115	H'FF	H'FF	H'80	H'80	H'73
116	H'FF	H'FF	H'80	H'80	H'74
117	H'FF	H'FF	H'80	H'80	H'75
118	H'FF	H'FF	H'80	H'80	H'76
119	H'FF	H'FF	H'80	H'80	H'77
120	H'FF	H'FF	H'80	H'80	H'78
121	H'FF	H'FF	H'80	H'80	H'79
122	H'FF	H'FF	H'80	H'80	H'7A
123	H'FF	H'FF	H'80	H'80	H'7B
124	H'FF	H'FF	H'80	H'80	H'7C
125	H'FF	H'FF	H'80	H'80	H'7D
126	H'FF	H'FF	H'80	H'80	H'7E
127	H'FF	H'FF	H'80	H'80	H'7F
128	H'FF	H'FF	H'80	H'80	H'80
129	H'FF	H'FF	H'80	H'80	H'81

Index	DIF_ADJ[ ]	SAD_ADJ[ ]	BLD_GAIN[ ]	DIF_GAIN[ ]	MDET[ ]
130	H'FF	H'FF	H'80	H'80	H'82
131	H'FF	H'FF	H'80	H'80	H'83
132	H'FF	H'FF	H'80	H'80	H'84
133	H'FF	H'FF	H'80	H'80	H'85
134	H'FF	H'FF	H'80	H'80	H'86
135	H'FF	H'FF	H'80	H'80	H'87
136	H'FF	H'FF	H'80	H'80	H'88
137	H'FF	H'FF	H'80	H'80	H'89
138	H'FF	H'FF	H'80	H'80	H'8A
139	H'FF	H'FF	H'80	H'80	H'8B
140	H'FF	H'FF	H'80	H'80	H'8C
141	H'FF	H'FF	H'80	H'80	H'8D
142	H'FF	H'FF	H'80	H'80	H'8E
143	H'FF	H'FF	H'80	H'80	H'8F
144	H'FF	H'FF	H'80	H'80	H'90
145	H'FF	H'FF	H'80	H'80	H'91
146	H'FF	H'FF	H'80	H'80	H'92
147	H'FF	H'FF	H'80	H'80	H'93
148	H'FF	H'FF	H'80	H'80	H'94
149	H'FF	H'FF	H'80	H'80	H'95
150	H'FF	H'FF	H'80	H'80	H'96
151	H'FF	H'FF	H'80	H'80	H'97
152	H'FF	H'FF	H'80	H'80	H'98
153	H'FF	H'FF	H'80	H'80	H'99
154	H'FF	H'FF	H'80	H'80	H'9A
155	H'FF	H'FF	H'80	H'80	H'9B
156	H'FF	H'FF	H'80	H'80	H'9C
157	H'FF	H'FF	H'80	H'80	H'9D
158	H'FF	H'FF	H'80	H'80	H'9E
159	H'FF	H'FF	H'80	H'80	H'9F
160	H'FF	H'FF	H'80	H'80	H'A0
161	H'FF	H'FF	H'80	H'80	H'A1
162	H'FF	H'FF	H'80	H'80	H'A2
163	H'FF	H'FF	H'80	H'80	H'A3
164	H'FF	H'FF	H'80	H'80	H'A4
165	H'FF	H'FF	H'80	H'80	H'A5
166	H'FF	H'FF	H'80	H'80	H'A6
167	H'FF	H'FF	H'80	H'80	H'A7
168	H'FF	H'FF	H'80	H'80	H'A8
169	H'FF	H'FF	H'80	H'80	H'A9
170	H'FF	H'FF	H'80	H'80	H'AA
171	H'FF	H'FF	H'80	H'80	H'AB
172	H'FF	H'FF	H'80	H'80	H'AC
173	H'FF	H'FF	H'80	H'80	H'AD

Index	DIF_ADJ[ ]	SAD_ADJ[ ]	BLD_GAIN[ ]	DIF_GAIN[ ]	MDET[ ]
174	H'FF	H'FF	H'80	H'80	H'AE
175	H'FF	H'FF	H'80	H'80	H'AF
176	H'FF	H'FF	H'80	H'80	H'B0
177	H'FF	H'FF	H'80	H'80	H'B1
178	H'FF	H'FF	H'80	H'80	H'B2
179	H'FF	H'FF	H'80	H'80	H'B3
180	H'FF	H'FF	H'80	H'80	H'B4
181	H'FF	H'FF	H'80	H'80	H'B5
182	H'FF	H'FF	H'80	H'80	H'B6
183	H'FF	H'FF	H'80	H'80	H'B7
184	H'FF	H'FF	H'80	H'80	H'B8
185	H'FF	H'FF	H'80	H'80	H'B9
186	H'FF	H'FF	H'80	H'80	H'BA
187	H'FF	H'FF	H'80	H'80	H'BB
188	H'FF	H'FF	H'80	H'80	H'BC
189	H'FF	H'FF	H'80	H'80	H'BD
190	H'FF	H'FF	H'80	H'80	H'BE
191	H'FF	H'FF	H'80	H'80	H'BF
192	H'FF	H'FF	H'80	H'80	H'C0
193	H'FF	H'FF	H'80	H'80	H'C1
194	H'FF	H'FF	H'80	H'80	H'C2
195	H'FF	H'FF	H'80	H'80	H'C3
196	H'FF	H'FF	H'80	H'80	H'C4
197	H'FF	H'FF	H'80	H'80	H'C5
198	H'FF	H'FF	H'80	H'80	H'C6
199	H'FF	H'FF	H'80	H'80	H'C7
200	H'FF	H'FF	H'80	H'80	H'C8
201	H'FF	H'FF	H'80	H'80	H'C9
202	H'FF	H'FF	H'80	H'80	H'CA
203	H'FF	H'FF	H'80	H'80	H'CB
204	H'FF	H'FF	H'80	H'80	H'CC
205	H'FF	H'FF	H'80	H'80	H'CD
206	H'FF	H'FF	H'80	H'80	H'CE
207	H'FF	H'FF	H'80	H'80	H'CF
208	H'FF	H'FF	H'80	H'80	H'D0
209	H'FF	H'FF	H'80	H'80	H'D1
210	H'FF	H'FF	H'80	H'80	H'D2
211	H'FF	H'FF	H'80	H'80	H'D3
212	H'FF	H'FF	H'80	H'80	H'D4
213	H'FF	H'FF	H'80	H'80	H'D5
214	H'FF	H'FF	H'80	H'80	H'D6
215	H'FF	H'FF	H'80	H'80	H'D7
216	H'FF	H'FF	H'80	H'80	H'D8
217	H'FF	H'FF	H'80	H'80	H'D9

Index	DIF_ADJ[ ]	SAD_ADJ[ ]	BLD_GAIN[ ]	DIF_GAIN[ ]	MDET[ ]
218	H'FF	H'FF	H'80	H'80	H'DA
219	H'FF	H'FF	H'80	H'80	H'DB
220	H'FF	H'FF	H'80	H'80	H'DC
221	H'FF	H'FF	H'80	H'80	H'DD
222	H'FF	H'FF	H'80	H'80	H'DE
223	H'FF	H'FF	H'80	H'80	H'DF
224	H'FF	H'FF	H'80	H'80	H'E0
225	H'FF	H'FF	H'80	H'80	H'E1
226	H'FF	H'FF	H'80	H'80	H'E2
227	H'FF	H'FF	H'80	H'80	H'E3
228	H'FF	H'FF	H'80	H'80	H'E4
229	H'FF	H'FF	H'80	H'80	H'E5
230	H'FF	H'FF	H'80	H'80	H'E6
231	H'FF	H'FF	H'80	H'80	H'E7
232	H'FF	H'FF	H'80	H'80	H'E8
233	H'FF	H'FF	H'80	H'80	H'E9
234	H'FF	H'FF	H'80	H'80	H'EA
235	H'FF	H'FF	H'80	H'80	H'EB
236	H'FF	H'FF	H'80	H'80	H'EC
237	H'FF	H'FF	H'80	H'80	H'ED
238	H'FF	H'FF	H'80	H'80	H'EE
239	H'FF	H'FF	H'80	H'80	H'EF
240	H'FF	H'FF	H'80	H'80	H'F0
241	H'FF	H'FF	H'80	H'80	H'F1
242	H'FF	H'FF	H'80	H'80	H'F2
243	H'FF	H'FF	H'80	H'80	H'F3
244	H'FF	H'FF	H'80	H'80	H'F4
245	H'FF	H'FF	H'80	H'80	H'F5
246	H'FF	H'FF	H'80	H'80	H'F6
247	H'FF	H'FF	H'80	H'80	H'F7
248	H'FF	H'FF	H'80	H'80	H'F8
249	H'FF	H'FF	H'80	H'80	H'F9
250	H'FF	H'FF	H'80	H'80	H'FA
251	H'FF	H'FF	H'80	H'80	H'FB
252	H'FF	H'FF	H'80	H'80	H'FC
253	H'FF	H'FF	H'80	H'80	H'FD
254	H'FF	H'FF	H'80	H'80	H'FE
255	H'FF	H'FF	H'80	H'80	H'FF

25. VSP1

This section describes the configurations of VSP1 on this LSI. Descriptions in this section show the full-function specifications of the VSP1 IP. Some of the functions described in this section are not available on VSP1 with restrictions written here.

Configurations of VSP1

This LSI incorporates three different types of VSP1 modules (VSPS, VSPD) as image processing systems.

VSPS: VSPS stands for VSP Standard which supports various functions of the VSP1 IP.
VSPD: VSPD stands for VSP for the display unit (DU) which outputs the display data to DU directly. Single channel is supported for RZ/G1C.

Table 25.1 to Table 25.2 show the restrictions of each type of VSP1 unit on this LSI.

All the registers and functions listed in Table 25.1 to Table 25.2 should be treated as un-implemented functions in each VSP1 unit. Do not set any registers related to the restricted function without any statement.

Table 25.1 VSPS Configuration

Category	Restriction Target	Restriction Description
Module	UDS1-2	These modules listed at left column are not implemented on VSPS. Functions and registers cannot be used. In addition, a setting of DPR routing with these modules is prohibited.
Function	RPF/CLUT	CLUT is only available on RPF ch1 and ch2 (not available on ch0, ch3, and ch4). Related register: VI6_RPFn_INFMT.RDFMT, VI6_CLUT0_TBL*, VI6_CLUT3_TBL*, VI6_CLUT4_TBL*

Table 25.2 VSPD Configuration

Category	Restriction Target	Restriction Description
Module	RPF4	These modules listed at left column are not implemented on VSPD. Functions and registers cannot be used. In addition, a setting of DPR routing with these modules is prohibited.
	CLU	
	UDS1-2	
	SRU	
	WPF1-3	
	HGT	
Function	RPF/CLUT	CLUT is only available on RPF ch2 (not available on ch0, ch1, and ch3). Related register: VI6_RPFn_INFMT.RDFMT, VI6_CLUT0_TBL*, VI6_CLUT1_TBL*, VI6_CLUT3_TBL*
	WPF/Vertical Flipping	Vertical flipping function is not implemented. Related register: VI6_WPF0_OUTFMT.FLP

Preface

Terminology

The terminology for VSP1. Refer to section 25.1, Overview for detail.

Read Pixel Formatter (RPF)

The RPF can read image data from external memory such as SDRAM. The RPF supplies image data to the internal sub modules in VSP1. At the same time, RPF can execute format conversion, color space conversion and color keying for each input image source. There are five RPFs in VSP1, and each RPF is called as RPF0, RPF1 and so on.

Virtual RPF

There is an image compositing sub module named as BRU which can execute image blending or raster operation. The BRU has 4 input ports for compositing multiple images. There must be a RPF module as the start of data processing. Each RPF can be a source of data input to BRU. In addition to these RPF modules, the BRU has a function which generates monochrome color image internally. This functionality is useful because the data access to an external memory is not required. This function is called as virtual RPF.

Refer to sections 25.2.8.1, 25.2.16.2, 25.2.16.3 and 25.2.16.4 for virtual RPF.

Write Pixel Formatter (WPF)

The WPF can input image data from internal image processing and output to the external memory such as SDRAM. At the same time, the WPF can execute color space conversion and format conversion. There are four WPFs in VSP1, and each WPF is called as WPF0, WPF1 and so on. The start of VSP1 equals to the start of each WPF by setting registers shown in section 25.2.5.1.

Target WPF

The VSP1 has five RPFs (RPF 0 to 4) and four WPFs (WPF0 to 3) and execute image processing. One data path consists of more than one RPF, one WPF and other image functional modules if necessary. The WPF which is reached from specific RPF(s) in the data path is called as target WPF for the RPF(s). The number of target WPFs is always one for the data path.

Source RPF

The data source in the data path for the specific WPF is called as source RPF for that WPF. The number of source RPFs is not always one, may be more than one for image blend operation or raster operation.

Layer

In case of image composite operation such as image blending or raster operation for multiple images, there is hierarchical relationship for each image. One layer is assigned to one RPF or one virtual RPF indicating one image in hierarchical relationship.

Master Layer

The master layer is a base layer for image compositing of multiple images, and the size of the master layer equals to that of BRU output. When the image compositing is not applied, there is one layer. This layer is also called as the master layer.

Sub Layer

The Layers except the master layer are called as sub layer.

Alpha

The VSP1 can execute both color data and its transparent data. The alpha is 8-bit data and expresses the transparency of pixel. The value H'FF represents opaque pixel, and the value H'00 represents transparent pixel.

Plane

One layer consists of color components such as R/G/B or Y/Cb/Cr, and alpha data representing its transparency of the pixel. The frame which is one of color components and alpha data is called as a plane.

Picture Plane

The picture plane represents color data in one layer.

Alpha Plane

The alpha plane represents transparent data in one layer.

Blending

The image blending means the image composite operation with alpha data. The composite ratio of image blending depends on the relationship of each layer and alpha values.

Raster Operation (ROP)

The bitwise operation such as AND or OR is called as raster operation (ROP).

Color Space Conversion (CSC)

The CSC means the conversion of YCbCr, RGB and HSV color spaces.

Definition of operators and functions

The following operators, notations are defined for explaining the functions of VSP1.

$\langle x \rangle$

Discard decimal places of value x

H'

The notation “H'” is used as prefix for hexadecimal numbers. For example, H'80 means 80 in hexadecimal and 128 in decimal.

B'

The notation “B'” is used as prefix for binary numbers. For example, B'10000000 means 80 in hexadecimal and 128 in decimal. When a number is used without prefix, it means decimal number.

_

The notation “_” is used as a separator of binary digit for binary number. There is no functional and logical meaning. The meaning of B'10101 and B'1_0101 is the same.

[msb:lsb]

This notation specifies a part of bits or all bits of registers and signals. For example, eval[3:0] means bit 3 to 0 of the signal or register which name is “eval” .

clip0 (x)

Clip to 0 value if x is less than 0. [$x = (x < 0)? 0 : x$]

clip3 (min, max, x)

The value x shall be clipped so that x shall be $min < x < max$.
[$x = (x < min)? min : ((x > max)? max : x)$]

Unit

The unit is defined here for explaining VSP1’s functions.

[bpp] : bits per pixel

VSP1 can handle a number of image formats. Each image format has different number of data bits. The unit [bpp] shows a number of data bits for one pixel. For example, RGB 8 bpp means that its format is RGB and the pixel consists of 8 data bits.

25.1 Overview

The VSP1 is the successor IP of Renesas' VIO6-IP series which supports image processing such as image enhancing, up/down scaling, color management function with lookup tables, image blending.

25.1.1 Features

1. Supports Various Data Formats and Conversion
   - Supports YCbCr444/422/420, RGB, αRGB, α plane
   - Color space conversion and changes to the number of colors by dithering
   - Color keying
   - Vertical flipping
2. Full HD Video Processing
   - Up and down scaling with arbitrary scaling ratio
   - Super resolution processing
   - Blending of four picture layers and raster operations (ROPs)
3. Full HD Picture Quality/Color Correction
   - γ correction and gain correction
   - Correction of color (to adjust skin tones or colors in memory)
   - Hue, brightness, and saturation adjustment
   - 1D and 2D histogram
4. Direct Connection to Display Module
   - Display Unit (DU) supported

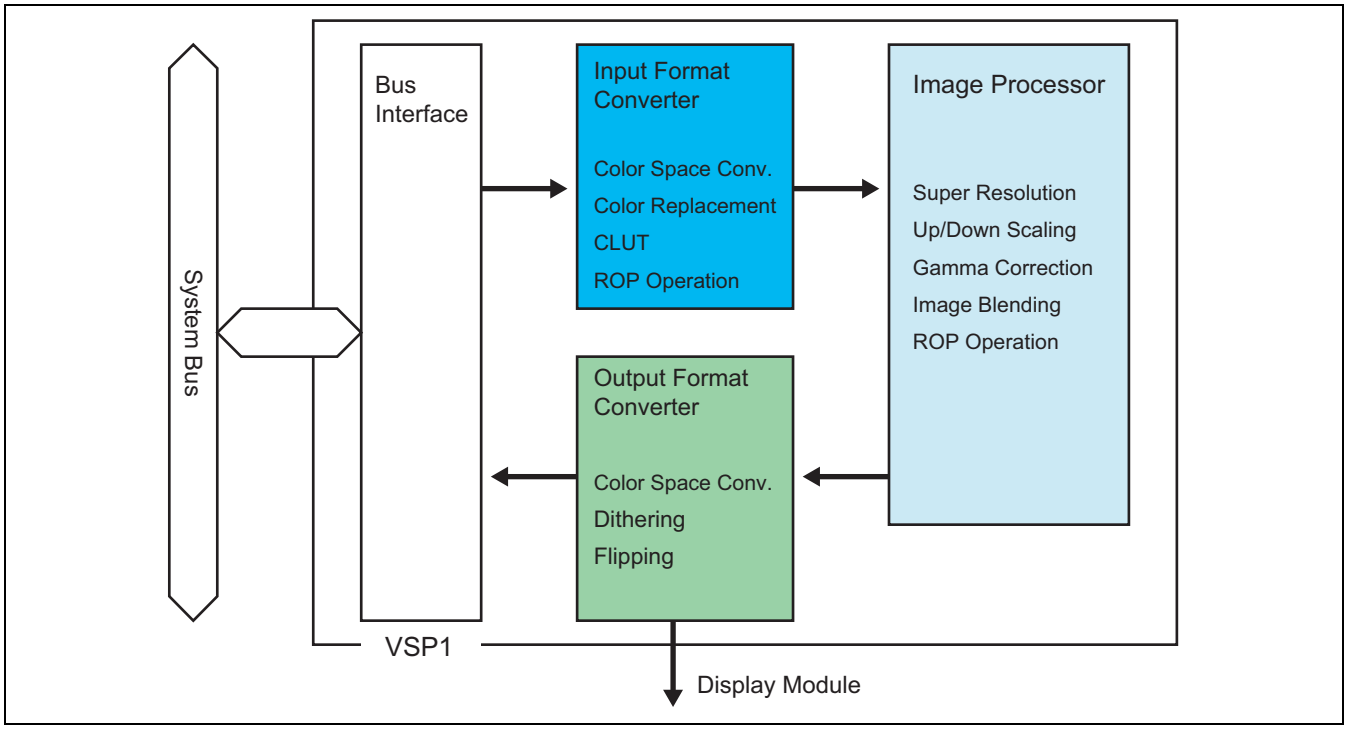


Figure 25.1 Top Level Architecture of VSP1

25.1.2 Block diagram

Figure 25.2 shows the configuration of VSP1 sub modules.

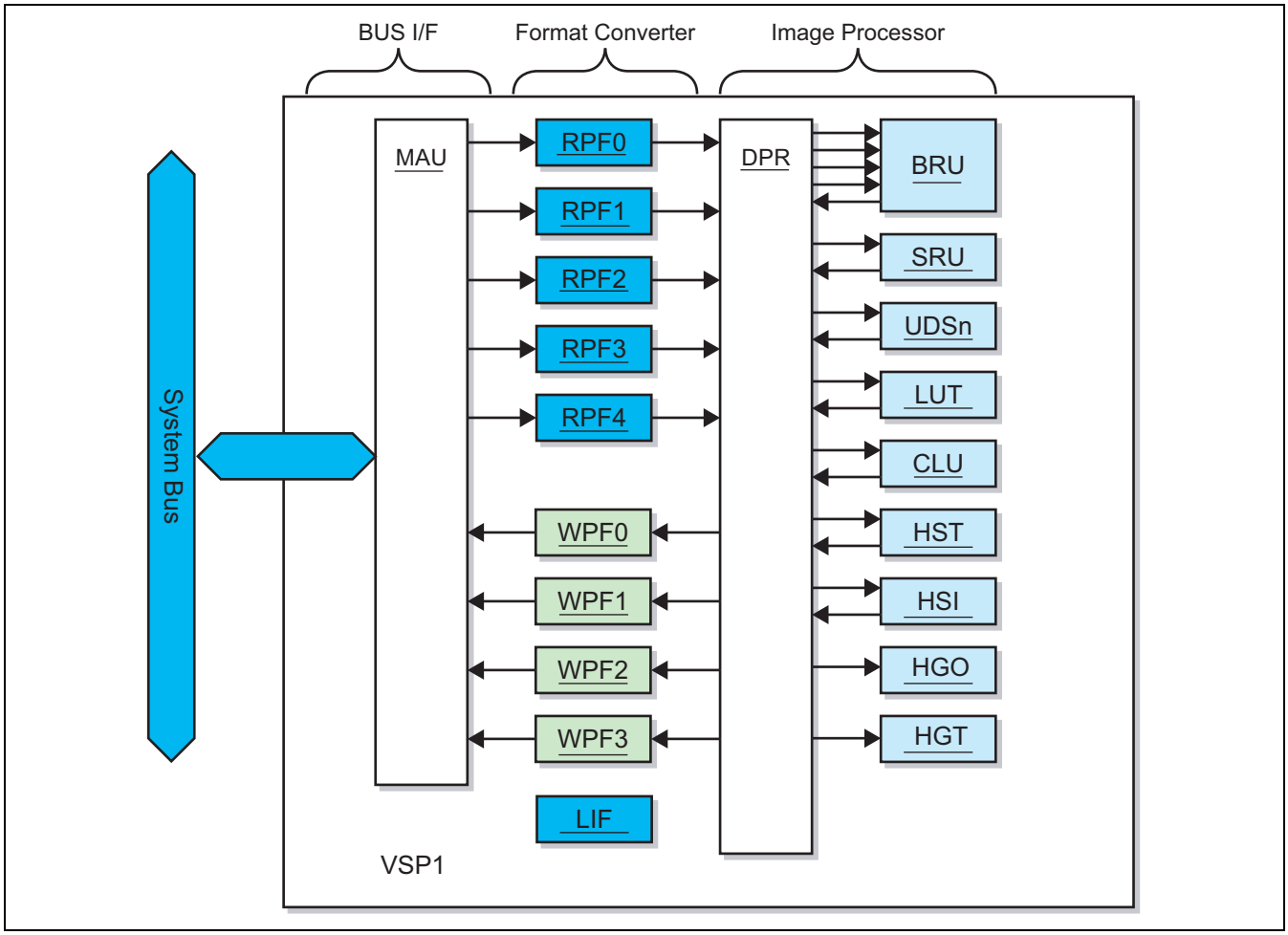


Figure 25.2 VSP1 Module Configuration

The following gives an overview of each block function shown in Figure 25.2. The operation of these functions is determined by the register setting explained in section 25.2. Refer to section 25.2 for the relationship between the register setting and the functional behavior.

(1) Memory Access Unit (MAU)

The VSP1 applies processing to the image data stored in the external memory and writes the resultant data back to the external memory. The data transfer between the external memory and VSP1 necessary for this operation is done by the MAU, which works as the bus master, according to the register settings. The MAU executes this data transfer between the external memory and VSP1.

(2) Command Transfer Unit (CTU)

The VSP1 can directly read register parameters for image processing by display lists stored in external memory. The CTU module is a bus interface and controls display lists when the CTU reads display lists as a bus master.

(3) Read Pixel Formatter (RPF)

The RPF reads image data from the external memory through the MAU, unpacks data according to the specified format, converts the color space, converts the number of colors, executes color keying, ROP operation, and OSD processing, and outputs the resultant data to the DPR. The RPF has an input format unpacking unit, an index color expanding unit (OSD-CLUT), a 1-bit mask generator, a raster operation unit (ROP unit), a color keying unit, and a color space converter. Figure 25.3 shows the processing flow in the RPF.

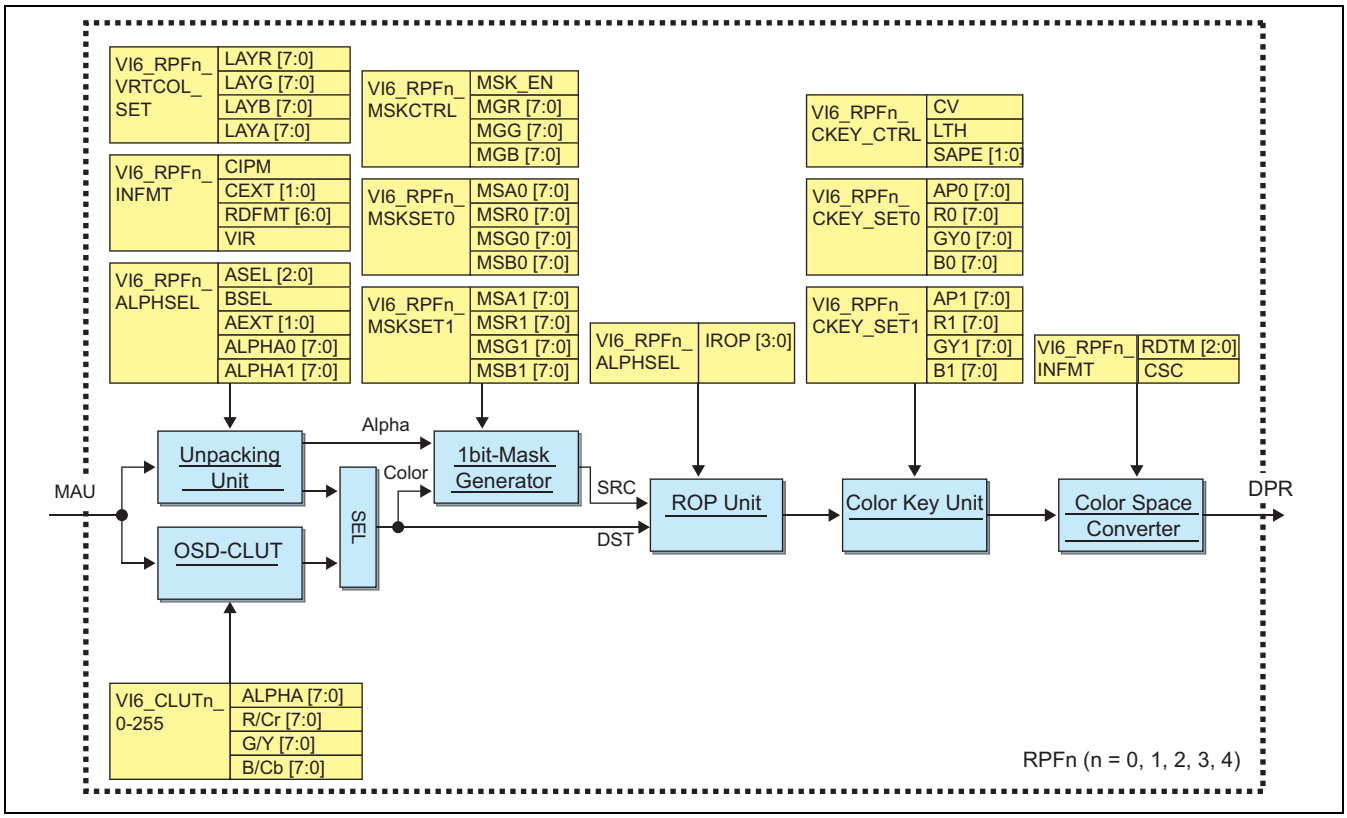


Figure 25.3 RPF Processing Flow

The input format unpacking unit and index color expanding unit (OSD-CLUT) expand the image data input from the MAU into the image format for internal processing, and the 1-bit mask generator generates a 1-bit image mask from the image data expanded through the unpacking unit and OSD-CLUT. Alternately, a 1-bit image mask can be generated from the alpha plane that is different from the picture plane read through the MAU.

The raster operation unit (ROP unit) executes raster operation between the data from the 1-bit mask generator and the image data expanded from the input format, and the color keying unit applies color replacement and specifies the transparent color for the image data input from the ROP unit. The color space converter converts the color space (RGB-YCbCr) of the image data input from the color keying unit as necessary.

The VSP1 provides maximum five RPF modules (RPF0 to RPF4). The implementation of OSD-CLUT depends on the configuration of each LSI.

(4) Data Path Router (DPR)

The DPR controls the data paths among RPFs, function modules, and WPFs. The DPR selects one of the images input from RPFs, outputs it to a function module (BRU, SRU, UDSn (n = 0 to 2), MED, LUT, CLU, HST, HSI, HGO, HGT or ILV), and selects one of WPFs as the destination where the image data processed in the function module will be output. Before output to the WPF, the output from each function module can be input to another function module, which enables multiple image processing functions to be executed continuously without involving the external memory.

(5) Super Resolution Unit (SRU)

The SRU is a module connected to the DPR, which executes the super resolution processing.

(6) Up/Down Scaler (UDS)

The UDS is a module connected to the DPR, which upscales or downscales the image size. It can also upscale or downscale the alpha value.

(7) LUT (LookUp Table)

This is a 1D-LUT that converts each of three color components by using a lookup table. The LUT is connected to the DPR and can be used for gamma correction, negative-positive conversion, posterization, and binarization through desired tone curve settings.

(8) Blend ROP Unit (BRU)

The BRU is a module connected to the DPR, which executes the image blending processing and ROP operation. The BRU has four blend/ROP operation units (blend/ROP unit m, m = A to D), an ROP operation unit, a blend/ROP input switch (SEL) for selecting the input to these operation units, and a divider for normalization (div unit).

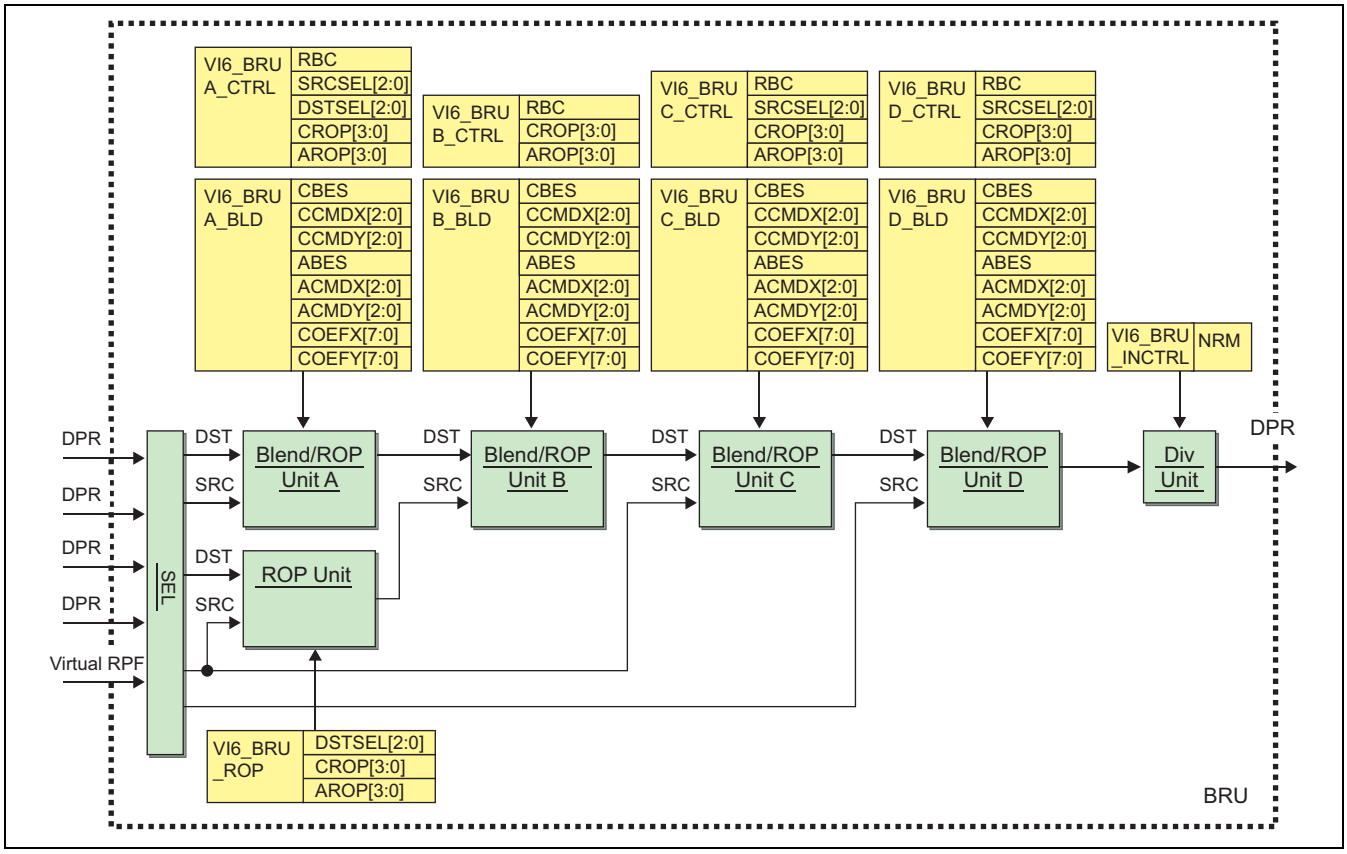


Figure 25.4 BRU Processing Flow

Each of the four blend-ROP operation units (blend/ROP unit m) receives the output from the SEL, blend/ROP Unit m, or ROP unit, and executes blending or raster operation (ROP) of images. The ROP unit receives the output from the SEL and executes 2-input raster operation (ROP2). By combining the ROP operation in the blend/ROP unit m and ROP2 operation in the ROP unit, 256-type 3-input raster operation (ROP3) can be implemented.

The divider for normalization (div unit) divides the pixel value by the α value.

(9) Write Pixel Formatter (WPF)

The WPF is an output module that receives image data from the DPR, converts the color space, number of colors, and format of the data, and outputs the results of VSP1 image processing to external memory through the MAU. The WPF is mainly configured from a color space converter and an output format converter (the packing unit).

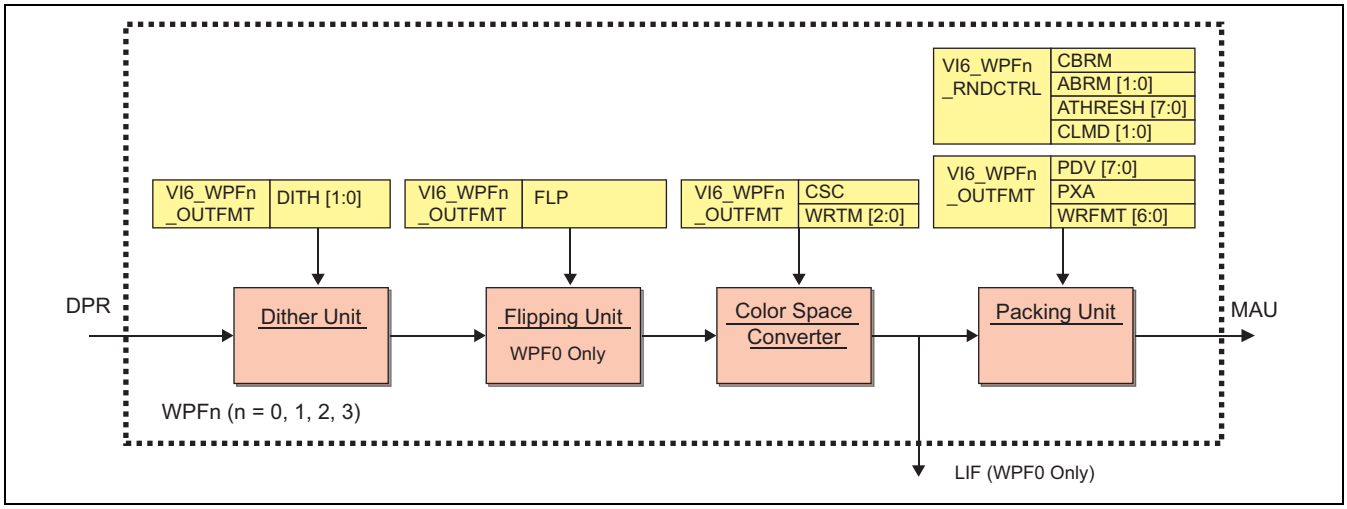


Figure 25.5 WPF Processing Flow

The color space converter converts the color space between RGB and YCbCr, and the packing unit converts the format into the picture plane storing format. The VSP1 provides maximum four WPFs (WPF0 to WPF3). The WPF0 has the output to LIF module after the color space conversion for transferring the video data to the display module.

(10) Cubic LookUp table (CLU)

This is a three-dimensional LUT (3D-LUT) that converts the input three-color-component data into desired three color components by using a lookup table. The 1D-LUT can only control each of three color components separately, but the 3D-LUT can convert a specified color into a different color. The CLU is connected to the DPR and can be used for specific color adjustment, such as correction to memorable color.

(11) Hue Saturation value Transform (HST)

The HST is a module connected to the DPR, which converts the RGB color space into the HSV color space. The HSV color space can represent a color with the hue, saturation, and value (brightness), and it makes color control through the LUT easier than in the RGB color space.

(12) Hue Saturation value Inverse transform (HSI)

The HSI is a module connected to the DPR, which converts the HSV color space into the RGB color space. It executes conversion in the direction opposite to that of the HST.

(13) Histogram Generator-One dimension (HGO)

The HGO is a module connected to the DPR and generates the one-dimensional histogram for the dynamic gamma correction. There is no output port of the image data. The middleware of the dynamic gamma correction will be released by Renesas.

(14) Histogram Generator-Two dimension (HGT)

The HGT is a module connected to the DPR and generates the two-dimensional histogram for the dynamic color correction. There is no output port of the image data. The middleware of the dynamic color correction will be released by Renesas.

(15) Lcdc InterFace (LIF)

The LIF module is used for transferring image data to the display module such as DU (Display Unit). The input port of the LIF module is connected to WPF0, and the output port of the LIF module is connected to DU.

25.1.3 Function List

Table 25.3 shows a functional overview of the VSP1 module.

Table 25.3 Functional Overview of VSP1

Data Transfer Function			
Bus interface	Data alignment	Conversion method	Byte, Word, LW, or LLW data swapping
	Data alignment Input	Channel	Data alignment can be specified separately for each input/output channel
		Address setting	1-byte units
Image memory	Output	Address setting	1-byte units
	Output Supported by RPF0 to RPF4	Memory area	Images can be written to the same memory area where the master layer is stored. Note the restrictions shown in Table 25.4.
Tile transfer mode			Interleaved, planer, or semi-planer

Read Pixel Formatter (RPF)

Number of channels			Five channels (RPF0 to RPF4)
Image format	Input	RGB	RGB888, RGB565, RGB666, αRGB8888, αRGB4444, αRGB1555, α plane (8 bpp, 1 bpp)
		YCbCr	YCbCr4:4:4/YCbCr4:2:2/YCbCr4:2:0 α plane (8 bpp, 1 bpp)
		Maximum size	8,190 × 8,190 pixels. The internal data path modules have separate restrictions on the maximum image size. For details, refer to Table 25.5.
		Minimum size	1 × 1 pixel The internal data path modules have separate restrictions on the minimum image size. For details, refer to Table 25.5.
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
Color keying	Color replacement	Compared data	RGB888 or Y
		Replaced data	αRGB8888 or αYCbCr
		Comparison Mode	Matched color mode
		Input source	RPF0 to RPF4
	Transparent color	Compared data	RGB888 or Y
		Replaced data	α
		Comparison Mode	Matched color mode, luma threshold mode
		Input source	RPF0 to RPF4
OSD/CLUT	Format	Memory storage format	8 bpp
		Image format	αRGB32 or αYCbCr32
	Input channel		RPF0 to RPF4
Raster operation	ROP2 (within input channels)	Operator	16 types (OpenGL2.0 is supported)
		Sources of operation	ROP2 operation between the 1-bpp α plane and RGB/YCbCr data in RPF0 to RPF4. Note that 1-bpp α is converted to αRGB888 or αYCbCr4:4:4.
Color space conversion	RGB to YCbCr	Conversion expression	RGB (0, 255) to BT601 (16, 235/240) RGB (0, 255) to BT709 (16, 235/240) RGB (0, 255) to BT601 (0, 255) RGB (16, 235) to BT709 (16, 235/240)
		Target of conversion	RPF0 to RPF4
	YCbCr to RGB	Conversion expression	BT.601 (16, 235/240) to RGB (0, 255) BT.709 (16, 235/240) to RGB (0, 255) BT.601 (0, 255) to RGB (0, 255) BT.709 (16, 235/240) to RGB (16, 235)
		Target of conversion	RPF0 to RPF4

Read Pixel Formatter (RPF)

Changing number of colors	Reducing RGB color depth	Target format	RGB666, RGB565, RGB555, RGB444, or RGB332
		Target of conversion	RPF0 to RPF4
	Increasing RGB color depth		Padded with 0. Copied from the most significant bits.
	YCbCr444 generation		CbCr copying or CbCr vertical copying and horizontal interpolation.
Virtual display	RPF0 to RPF4	Color format	αRGB8888 or αYCbCr4:4:4 single-color
		Display size	Same as the size of the input channel
	Virtual RPF	Color format	αRGB8888 or αYCbCr4:4:4 single-color
		Display size	Maximum: 8,190 × 8,190 pixels Minimum: 4 × 4 pixels
α bit count conversion	Input	Bit increase	Padded with 0. Copied from the most significant bits.

Write Pixel Formatter (WPF)

Number of channels			Four channels (WPF0 to WPF3)
Image format	Output	RGB	RGB332, RGB444, RGB565, RGB666, RGB888, αRGB8666, αRGB8888, αRGB4444, αRGB1555
		YCbCr	YCbCr4:4:4, YCbCr4:2:2, YCbCr4:2:0
		Maximum size	2,048 × 2,048 The internal data path modules have separate restrictions on the maximum image size. For details, refer to Table 25.5.
		Minimum size	1 × 1 pixel The internal data path modules have separate restrictions on the minimum image size. For details, refer to Table 25.5.
		Size setting unit	YCbCr420: 2-pixel units both horizontally and vertically. YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. In other formats, the size can be set in 1-pixel units.
Color space conversion	RGB to YCbCr	Conversion expression	RGB (0, 255) to BT.601 (16, 235/240) RGB (0, 255) to BT.709 (16, 235/240) RGB (0, 255) to BT.601 (0, 255) RGB (16, 235) to BT.709 (16, 235/240)
		Target of conversion	WPF0 to WPF3
	YCbCr to RGB	Conversion expression	BT.601 (16, 235/240) to RGB (0, 255) BT.709 (16, 235/240) to RGB (0, 255) BT.601 (0, 255) to RGB (0, 255) BT.709 (16, 235/240) to RGB (16, 235)
		Target of conversion	WPF0 to WPF3
Changing number of colors	Output	Reducing RGB color depth	Dithering, lower-order bit truncation, or rounding
		YCbCr422/420	CbCr skipping or CbCr vertical skipping and horizontal skipping
α bit count conversion	Output	Bit reduction	Truncation, rounding, or comparison with threshold (for 1 bpp)

Image Compositing

α blending	Input α value selection	RGB	Pixel α, fixed α value, α plane, or 1-bit α converted from the color specified for pixels
		YCbCr	α plane, fixed α value, or 1-bit α converted from the color specified for pixels
	α blending expression	Plane A: Upper plane Plane B: Lower plane	xA + yB, xA – yB Coefficients x and y should be selected from the following. Fixed α value, (α for plane A), (1 - α for plane A), (α for plane B), (1 - α for plane B)
α blending	Output α value selection	RGB	Fixed α value, x·(α for plane A) + y·(α for plane B), x·(α for plane A) – y·(α for plane B) Coefficients x and y should be selected from the following. Fixed α value, (α for plane A), (1 – α for plane A), (α for plane B), (1 – α for plane B)
	Blending planes	Number of planes	Four planes selected from RPF0 to RPF4 and video processing function output, and virtual RPF; five planes in total
		Order of planes	The order of five planes selected from RPF0 to RPF4, virtual RPF, and video processing function output can be changed as desired.
	α plane	Format	8 bpp or 1 bpp (α value can be specified through register)
		Input source	RPF0 to RPF4
	Fixed α value	Format	8 bpp
		Input source	RPF0 to RPF4, virtual RPF, or video processing function output
Raster operation	ROP2 (between input channels)	Operator	16 types (OpenGL2.0 is supported)
		Sources of operation	RPF0 to RPF4, virtual RPF, and video processing function output
		Operation control	RGB/YCbCr and α are operated separately.
	ROP3 (between input channels)	Operator	256-type ROP3 is available by combining ROP2 operations
		Sources of operation	RPF0 to RPF4, virtual RPF, and video processing function output
		Operation control	RGB/YCbCr and α are operated separately.

Video Processing Functions

Super resolution	Processing method		Processing within one frame
	Scaling ratio		× 1 (same size) or × 2
	Arbitrary scaling ratio		Super resolution processing can be combined with the arbitrary ratio scaling function.
	α processing		Fixed α output
Scaler with arbitrary scaling ratio	Scaling factor		1/16 to 16
	Scaling ratio setting	Expression	1/[Mant.Frac]
		Precision	Mant = 4 bits, Frac = 12 bits
	α processing		Supported (for scale-up or scale-down to 1/4 to 1/1)
Simultaneous processing			All video processing functions and color adjustment functions can be processed simultaneously (the order of function execution is limited).

Color Adjustment Function

1D-LUT	LUT configuration	Independent R/Y, G/Cb, and B/Cr. 256 entries each
3D-LUT	Number of grid points	17 × 17 × 17
HSV color space conversion	RGB to HSV	Eight bits each for H/S/V
	HSV to RGB	Eight bits each for H/S/V
1D Histogram	Letter box detection	Supported
	Number of bins	64 for each color component
2D Histogram	Letter box detection	Supported
	Number of hue areas	6
	Number of bins	32 for each hue area

When the data output from the VSP1 is written back to the same memory area where the input data for the VSP1 has been read, the VSP1 has the following restrictions.

1. The access order and format on the frame memory are the same between the input pixels and output pixels.
2. Specifying a larger output image size than the input image size, either vertically or horizontally or both vertically and horizontally, is prohibited.
3. When the YCbCr4:2:0 format is input, operation between color components is prohibited.

These restrictions are summarized in Table 25.4. Refer to the descriptions of the registers related to each restriction. In the table, RPF_m indicates the RPFn that inputs the master layer, and WPF_{wb} indicates the WPFn that writes back the output image to the source image area for the master layer.

Table 25.4 Restrictions on Use when Output Data is Written Back to Input Data Area

No.	Restriction	Related Registers
Restriction 1	The RPF_m input format and the WPF_{wb} output format should be the same.	VI6_RPFn_INFMT.RDFMT VI6_RPFn_INFMT.VIR
	The RPF_m source image storing address and the WPF_{wb} destination address should be the same.	VI6_RPFn_SRCM_ADDR_*
	The RPF_m source picture memory stride and the WPF_{wb} destination memory stride should be the same.	VI6_RPFn_SRCM_PSTRIDE VI6_RPFn_SRCM_ASTRIDE
	The RPF_m and WPF_{wb} data swapping settings should be the same.	VI6_WPFn_DSWAP
	The image vertical flipping function cannot be used if WPF_{wb} is WPF0.	VI6_WPFn_OUTFMT.FLP
Restriction 2	Super resolution processing with double scale-up by the SRU is prohibited (super resolution processing of the same size is allowed).	VI6_SRU_CTRL0
	Scale-up and color filling by UDSn is prohibited.	VI6_UDSn_SCALE VI6_UDSn_CLIP_SIZE
	The value of scaling filter horizontal and vertical phase registers should be zero in case of using UDSn.	VI6_UDSn_IPC
	The RPF_m basic read size and extended read size should be the same.	VI6_RPFn_SRC_BSIZE VI6_RPFn_SRC_ESIZE
Restriction 3*	Color space conversion is prohibited in RPF_m and WPF_{wb}.	VI6_RPFn_INFMT.CSC VI6_WPFn_OUTFMT.CSC
	Use of the CLU is prohibited. Make sure that the CLU is not used in DPR routing.	VI6_DPR_CLU_ROUTE.RT
	NOP should be specified for IROP operation.	VI6_RPFn_ALPH_SEL.IROP
	Color keying is prohibited.	VI6_RPFn_CKEY_CTRL.CV

Note: * When the input format is not YCbCr4:2:0, restriction 3 in not applied.

25.1.4 VSP1 Input Size

Table 25.5 is a list of input size specifications.

Table 25.5 List of Input Size Specifications

Module	Min. Input Size	Max. Input Size	Restrictions on Setting Unit
RPF	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. YCbCr420: 2-pixel units both horizontally and vertically. Other formats: 1-pixel units both horizontally and vertically. Notes: 1. When the 1-bpp alpha plane*1 is input, the size can always be specified in 8-pixel units both horizontally and vertically regardless of the input format. 2. These restrictions including note 1 are applied to the following. VI6_RPFn_SRC_BSIZE VI6_RPFn_SRC_ESIZE
SRU	4 (horizontal) × 4 (vertical) pixels	Without scaling (same size): 2,048 (horizontal) × 8,190 (vertical) pixels With double scale-up: 1,024 (horizontal) × 4,095 (vertical) pixels	1-pixel units both horizontally and vertically.
UDSn (n = 0, 1, 2)	4 (horizontal) × 4 (vertical) pixels	8,190 (horizontal)*2 × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
LUT	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
CLU	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HST	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HSI	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
BRU	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HGO	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
HGT	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
LIF	1 (horizontal) × 1 (vertical) pixel	8,190 (horizontal) × 8,190 (vertical) pixels	1-pixel units both horizontally and vertically.
WPF	1 (horizontal) × 1 (vertical) pixel	2,048 (horizontal) × 2,048 (vertical) pixels	YCbCr422: 2-pixel units horizontally and 1-pixel units vertically. YCbCr420: 2-pixel units both horizontally and vertically. Other formats: 1-pixel units both horizontally and vertically. Note: This restriction on the WPF only applies to the WPF output size. The WPF input size should be specified in 1-pixel units.

Notes: 1. When VI6_RPFn_ALPH_SEL.ASEL is set to B'011.

2. When the image size is downscaled and the horizontal UDS output size is 2,048 pixels or smaller, the UDS input size can be 2,048 pixels or larger.

The most important restriction shown in Table 25.5 is the setting unit. Make appropriate register settings so that the size of the image input to each module does comply with setting units and does not exceed the limits shown in Table 25.5. Especially for the register settings of SRU and UDSn, where the size can be changed within the modules, be careful not to exceed the input size limit for the module connected behind each of them.

25.1.5 VSP1 Output Size

The size of the output from each WPF is determined by the results of processing in the modules connected with the DPR. As shown in Figure 25.2, the data input to the VSP1 is sent to the WPF output modules through the RPF and the modules connected with the DPR. When there is no processing that changes the image size through this data path, the WPF output size is the same as the RPF input size. Table 25.6 is a list of the processing that changes image size.

Table 25.6 Image Processing that Changes Image Size

Module	Function*1	Related Register	Size of Output from Module
SRU	Super resolution with double scale-up	VI6_SRU_CTRL0	Super resolution without scaling (same size): Input size Super resolution with double scale-up: Input size × 2
UDSn	Output size clipping	VI6_UDSn_CLIP_SIZE	Horizontal output size: VI6_UDSn_CLIP_SIZE.CL_HSIZE setting Vertical output size: VI6_UDSn_CLIP_SIZE.CL_VSIZE setting
WPF	Input size clipping	VI6_WPFn_HSZCLIP VI6_WPFn_VSZCLIP	When this function is disabled, the input size and the output size are the same. When this function is enabled, the output is in the following size. Horizontal output size: VI6_WPFn_HSZCLIP.HCL_SIZE *2 setting Vertical output size: VI6_WPFn_VSZCLIP.VCL_SIZE *2 setting

Notes: 1. For details of each function, refer to the descriptions of the related registers.
2. Refer to section 25.2.1, Notational Conventions for Registers and Bit Fields for explanation of register bit field.

The input image size can be changed only with the modules and functions shown in Table 25.6. With the other modules and functions, the input size and output size are the same. Accordingly, after module connections with the DPR are determined, the VSP1 output size can also be determined through the following steps.

1. The image size (VI6_RPFn_SRC_ESIZE) read from the external memory and sent to the DPR by the RPFn is the initial value.
2. When the module connected with the DPR is not a module (function) shown in Table 25.6, the output size from the module is the same as the input size; the image size does not need to be updated.
3. When a module connected with the DPR is a module (function) shown in Table 25.6, the output image size should be updated to the size shown in the table, which should be used as the input image size for the module connected behind it.
4. When the final image size at the WPFn is determined, this size is the VSP1 output size for that WPFn path.

Figure 25.6 shows how to determine the image size in a sample DPR connection through the above steps. The related conditions that determine the image size are also shown.

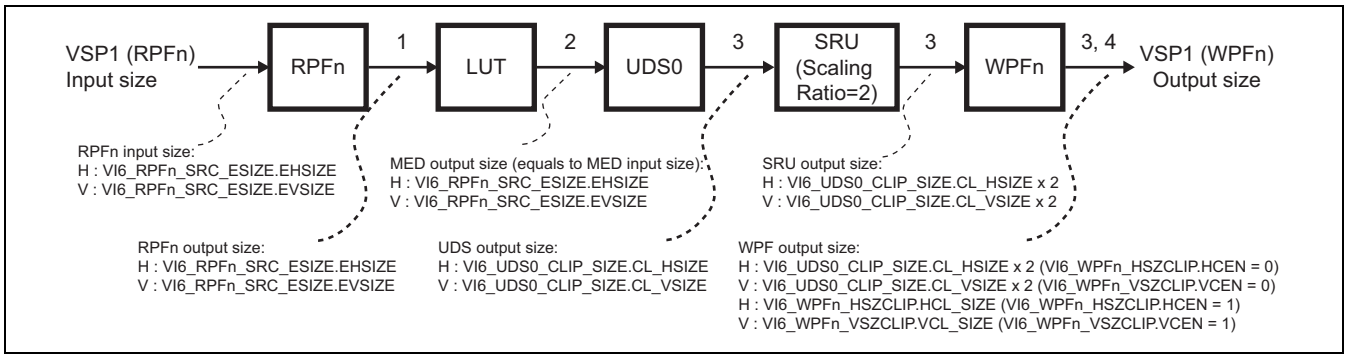


Figure 25.6 Input/Output Size for Each Module in a Sample DPR Connection

Make appropriate register settings in each module so that the VSP1 output image size determined as shown in the figure does not violate the restrictions shown in Table 25.6.

25.1.6 Input/Output Data Format

The VSP1 input/output data should be stored in a format where the address is incremented in the direction from the MSB to the LSB as in big endian. For example, the VSP1 reads and writes data to and from the external memory through the dedicated bus interface with a 128-bit width, and the data that should come first should be stored in the MSB side regardless of the unit data size as shown in Figure 25.7.

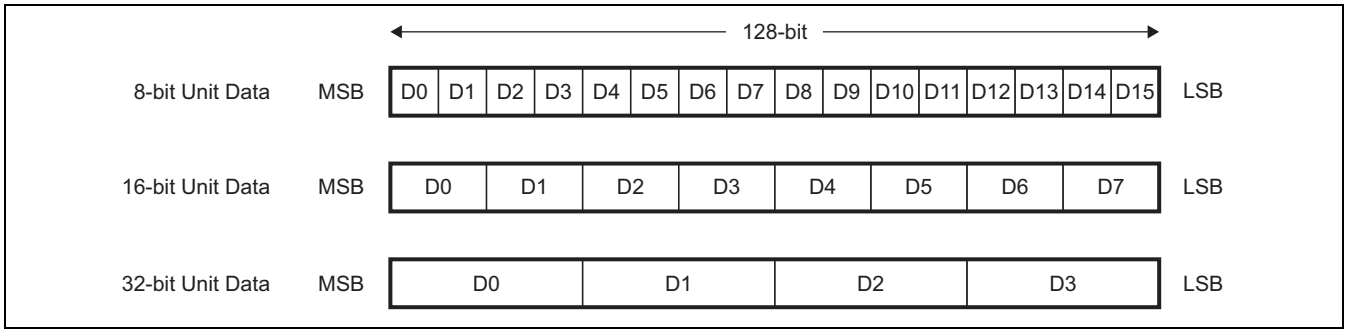


Figure 25.7 VSP1 Input/Output Data Format

However, data may be arranged in a way unexpected by the VSP1 depending on the address handling method (such as little endian) of the VSP1 access destination in some cases as in the external memory format shown in Figure 25.8. In such a case, use the data swapping function (refer to sections 25.2.7.4 and 25.2.8.5) in the VSP1 to convert the data format to be suitable for the VSP1.

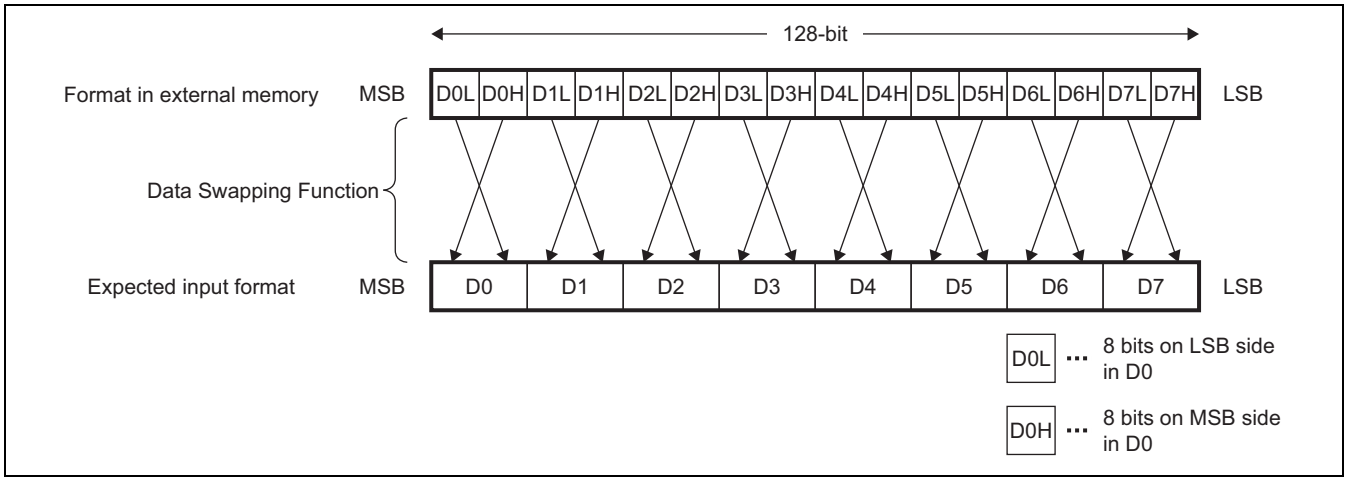


Figure 25.8 Input Data Alignment by Data Swapping Function

25.1.7 Concept of VSP1 Operation Starting and Stopping

The VSP1 provides four channels of image processing. Each channel is started by setting the corresponding start register. Here, starting a processing channel means starting one of WPF0 to WPF3, which are output modules of the VSP1. Use the start registers shown in Table 25.7 to start WPF modules.

After a WPF module is started and specified processing is completed, the corresponding channel stops operation and notifies the end of processing through an end interrupt. End interrupts are generated through the end interrupt source registers shown in Table 25.7; clearing a source register cancels the corresponding interrupt signal (for details of interrupt processing, refer to section 25.1.9, Interrupt Processing). Each of the operating status registers shown in the table indicates the busy state after the corresponding channel is started through the start register until processing is completed and operation stops. Figure 25.9 shows these operation timings.

Table 25.7 Target Module and Corresponding Registers for Starting and Stopping Operation

Target Module	Start Register	End Interrupt Source Register	Operating Status Register
WPF0	VI6_CMD0.STRCMD	VI6_WPF0_IRQ_STA. FRE	VI6_STATUS.SYS0_ACT
WPF1	VI6_CMD1.STRCMD	VI6_WPF1_IRQ_STA. FRE	VI6_STATUS.SYS1_ACT
WPF2	VI6_CMD2.STRCMD	VI6_WPF2_IRQ_STA. FRE	VI6_STATUS.SYS2_ACT
WPF3	VI6_CMD3.STRCMD	VI6_WPF3_IRQ_STA. FRE	VI6_STATUS.SYS3_ACT

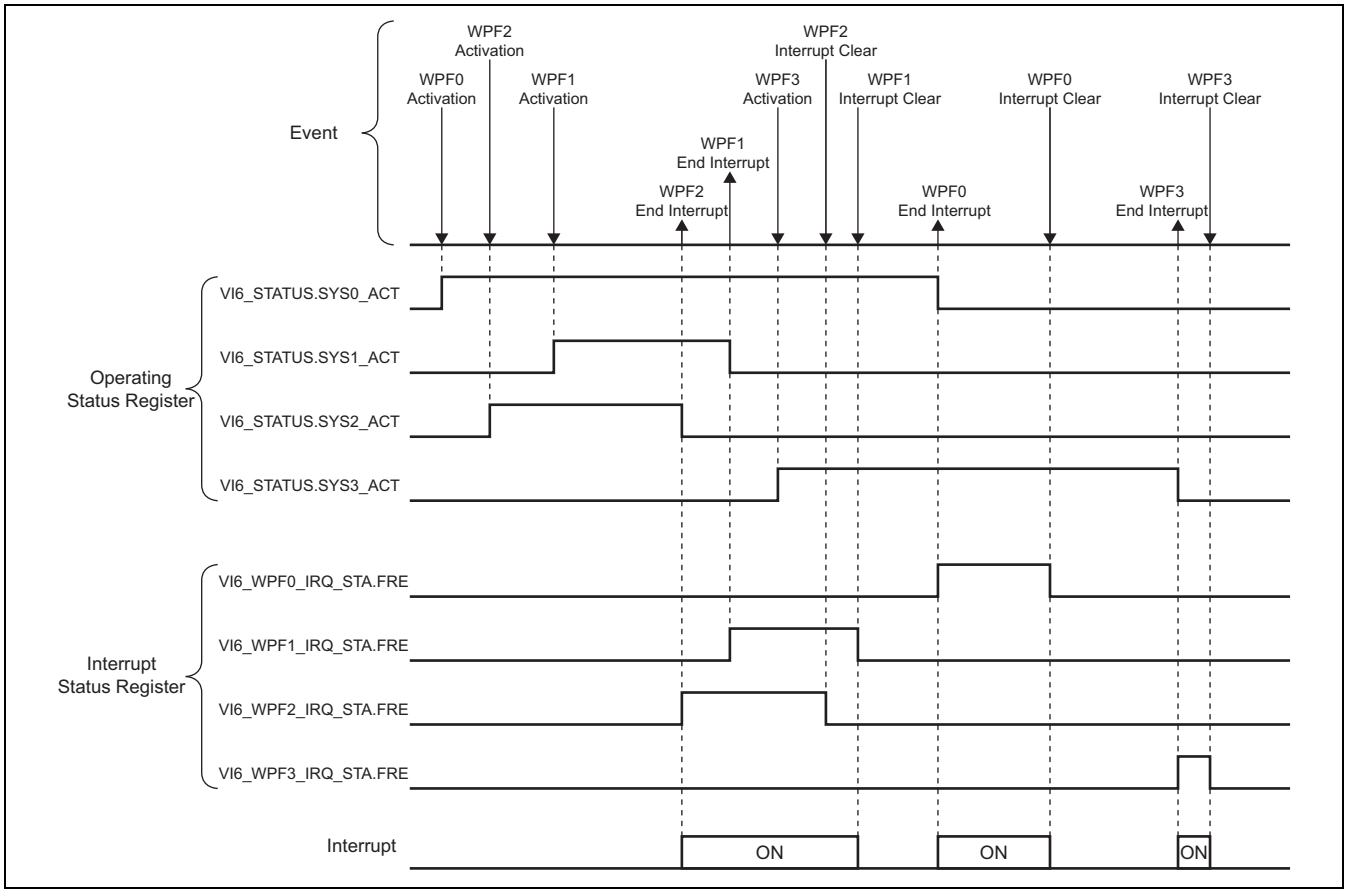


Figure 25.9 VSP1 Startup and Status of Each Register and Interrupt

The following describes the operating states (operating or stopped) of VSP1 internal modules. As described in section 25.1.2, the VSP1 has several image processing modules and the connections between modules are determined by the DPR. Accordingly, the operating state of a module is the same as that of the target WPF for that module. For example, when the target WPF for the CLU is WPF2, the CLU operating state is the same as that of WPF2; that is, the CLU operating state is indicated by the VI6_STATUS.SYS2_ACT as shown in Table 25.7 and the status change timing is shown as VI6_STATUS.SYS 2_ACT in Figure 25.9. Likewise, the operating states of all modules connected to WPF2 are indicated by VI6_STATUS.SYS 2_ACT.

After connections through the DPR are changed and the target WPF for a module is changed, refer to the correct register for the new target WPF to check the operating state of that module. In the above example, after the target WPF for the CLU is changed from WPF2 to WPF0, the CLU operating state is indicated by VI6_STATUS.SYS 0_ACT.

Connections should be changed through the DPR-related registers (described later) while all modules to be affected by any change in connections are stopped. If connections through the DPR are changed during operation, the VSP1 will hang.

25.1.8 Display List

(1) Functional Description

The VSP1 provides the display list function. As a display list, the VSP1 automatically downloads the register settings except for the control registers (sections 25.2.5 and 25.2.6) from external memory and stores the settings in the VSP1 registers. This function is advantageous in that the interrupt processing or register setting modification processing can be executed without CPU intervention during multiple-frame processing because the register settings used for VSP1 processing are prepared in advance in external memory such as SDRAM.

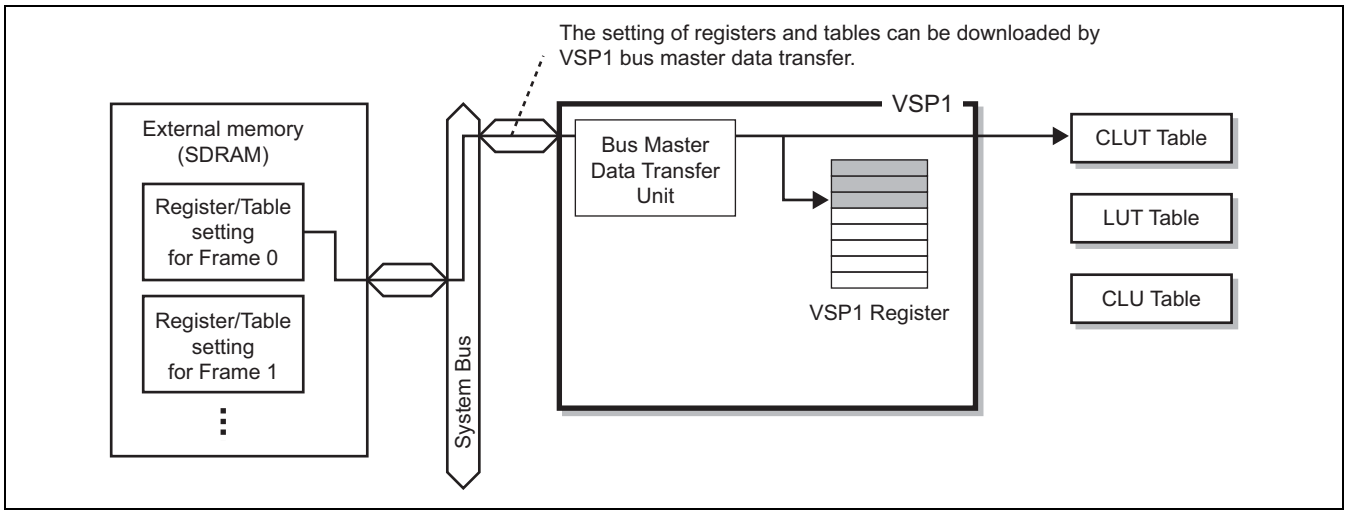


Figure 25.10 Concept of Display List

To use display lists, specify the external memory addresses to the display list control registers described in section 25.2.6. The register settings or various types of information should be stored in external memory in the format described in section 25.1.8 (2).

Figure 25.11 shows the difference between VSP1 operation through normal register settings and through display lists.

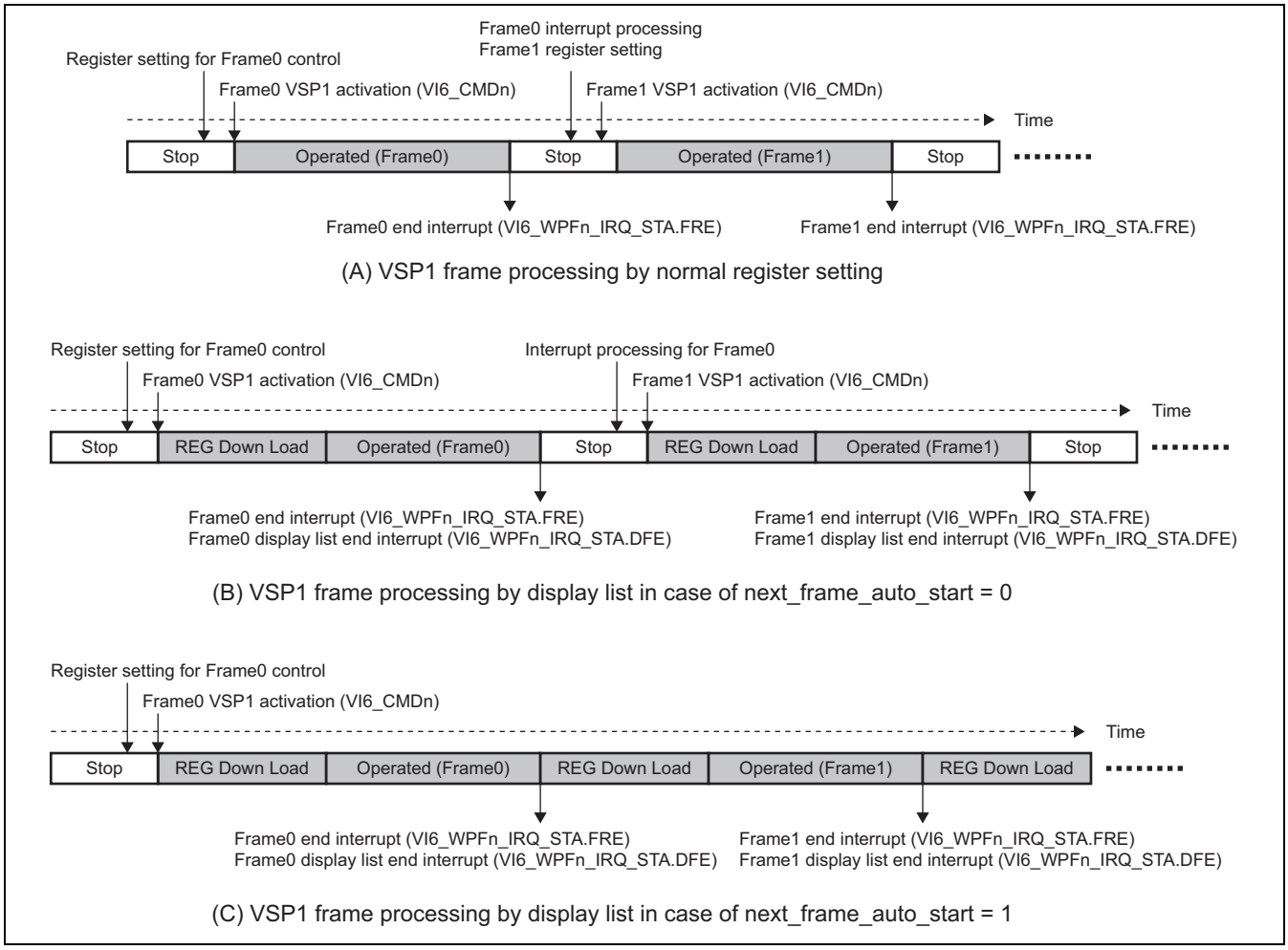


Figure 25.11 Comparison of VSP1 Operation between Normal Register Settings and Display Lists

As shown in Figure 25.11 (A), in the VSP1 processing through normal register settings, all registers should be set up before the VSP1 is started for each frame. After the VSP1 processing is completed, the VSP1 outputs a frame end interrupt (VI6_WPFn_IRQ_STA.FRE). This method requires a certain amount of time for register settings or interrupt processing by the CPU between frames. In contrast, when display lists are used, the VSP1 automatically downloads register settings from external memory as shown in Figure 25.11 (B) and (C), which reduces the load on the CPU between frames.

Figure 25.11 (B) shows the display list usage where the VSP1 stops at the end of every frame; only the VSP1 start processing for each frame is done by the CPU. This is suitable for the cases when the CPU controls synchronization of frame processing in frame buffer management or when the amount of register values or table data to be set in the VSP1 is large. In the case shown in Figure 25.11 (C), as soon as the frame processing ends, the VSP1 automatically begins next frame operation and starts downloading new register settings. This is the fastest operation using display lists.

Table 25.8 shows the modes of the display list and the supported functions for each mode. The detail of each mode is described in the following sections.

Table 25.8 Display List Mode and Supported Functions

Mode	Extended Display List	Continuous Frames
Normal Display List Mode	Supported	Controlled by “next_frame_auto_start” in the header of the display list.
Header-less Display List Mode	Not Supported	Controlled by VI6_DL_CTRL.CFM0 bit.

(2) Normal Display List Mode

The VSP1 display lists include control information as well as simple register settings in order to control multiple-frame processing in an optimum way for each application. Figure 25.12 shows the display list structure.

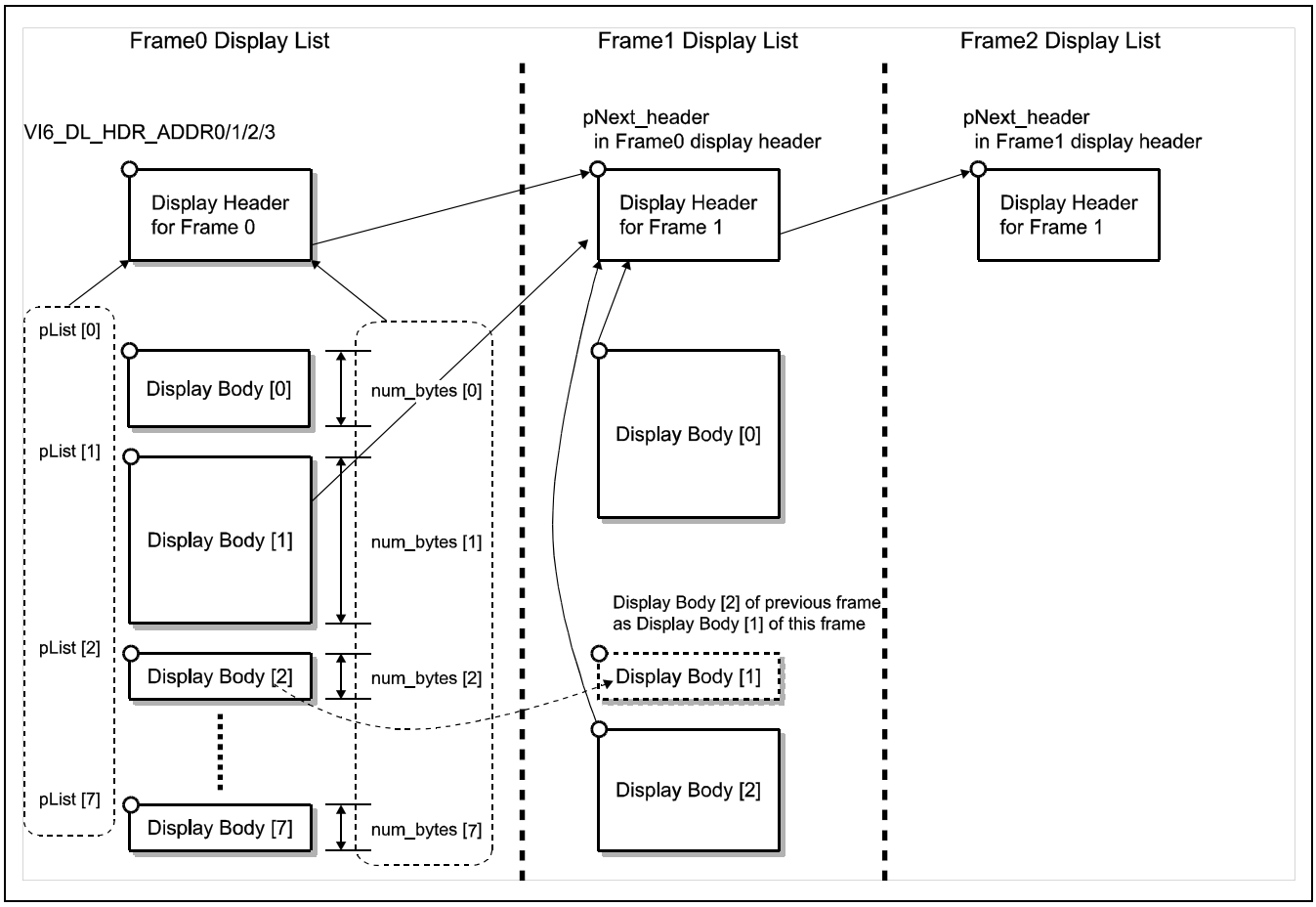


Figure 25.12 Structure and Concept of VSP1 Display List

A VSP1 display list consists of two sections; a header section for storing various information and control flags and a body section for storing register and table settings. A combination of these two sections is defined as a display list for a frame. The register and table settings can be divided and stored in up to eight separate bodies allocated in memory. Therefore, the separate bodies storing the register settings for one frame (for example, frame 0) can have non-sequential start addresses; that is, the bodies for one frame can be allocated to areas distant from each other in memory. To gather these bodies and configure the register settings for one frame, a header is used. A display header stores the number of bodies linked with the header and the start address and size of each body.

The VSP1 analyzes the header to gather register and table settings stored in separate memory areas and reconfigure the complete register settings.

The addresses of display headers should be specified in the VSP1 registers described in section 25.2.6. When activated in a mode that uses display lists, the VSP1 downloads display headers from the addresses specified in VI6_DL_HDR_ADDR0/1/2/3 (numbers 0 to 3 correspond to the WPF channel index numbers), analyzes the numbers of bodies and the address and data size of each body, downloads the bodies, and completes register and table settings. After display list downloading is completed, the VSP1 becomes ready for frame image processing; the VSP1 then starts the actual frame processing.

After processing of a frame ends, the VSP1 proceeds to the next frame processing. Here, there are two modes for starting the next frame processing as shown in Figure 25.11. In one mode, the VSP1 stops operation and waits for the next activation by the CPU in the same way as when display lists are not used. In this mode, the address used for downloading

the display header of the next frame is kept by the internal hardware. Therefore, if valid address information is not stored in the display header for the previous frame, a correct value should be specified in VI6_DL_HDR_ADDR0/1/2/3 while the VSP1 is stopped. When the VSP1 is started after a correct value is specified, the VSP1 starts next frame processing with the same procedure for the previous frame. In contrast to this mode, which stops the VSP1 after the end of one-frame processing, there is another mode for automatically starting next frame processing. In automatic start mode, the VSP1 downloads the next display header as soon as the previous frame processing ends. After downloading ends, the VSP1 starts image processing. The information regarding mode selection, that is, whether to automatically start next frame processing, should be stored in the display header downloaded for the previous frame.

In the automatic start mode, the VSP1 continues processing until the display header for a frame specifies that the next frame should not be started automatically. To stop processing during automatic execution, use a software reset (VI6_SRESET).

To strictly define the display list format described above, the following shows the grammatical structure of a display list using pseudo-code. First, to simplify the description of the display list format in the following pages, Table 25.9 defines a function. Function zero_bits (num_bits) generates a string of one-bit 0s for the number of bits specified by the parameter for the function. By using this function, Table 25.10 defines the header section format of a display list and Table 25.11 defines the body section format.

Table 25.9 Definition of a Function for Simple Description

Syntax	Bit Count
zero_bits (num_bits)	
{	
for (i=0; i<num_bits; i++) {	
zero_bit	1
}	
}	

Bit String	Contents
zero_bit	zero_bit indicates a 1-bit integer having a value of 0.

Table 25.10 Format of Display List Header Section

Syntax	Bit Count
display_header () /* Fixed length */	
{	
zero_bits (29)	
num_list_minus1	3
for (i=0; i<8; i++) {	
zero_bits (15)	
num_bytes [i]	17
pList [i]	32
}	
pNext_header	32
zero_bits (30)	
current_frame_int_enable	1
next_frame_auto_start /* 76 bytes from the beginning of this header*/	1
if (VI6_DL_EXT_CTRL.EXT) {	
zero_bits (32) /* padding zero 4 bytes for alignment */	
zero_bits (6)	
pre_ext_dl_exec	1
post_ext_dl_exec	1
zero_bits (8)	
pre_ext_dl_num_cmd	16
pre_ext_dl_pList	32
zero_bits (16)	
post_ext_dl_num_cmd	16
post_ext_dl_pList /* 96 bytes from the beginning of this header*/	32
}	
}	

Bit String	Contents
num_list_minus1	Specifies the value obtained by subtracting 1 from the total number of display list bodies linked with the display header. For example, when this bit field is set to 0, this display list uses one body.
num_bytes [i]	Specifies the number of bytes in the i-th display list body (indicated by index i). Be sure to specify a multiple of eight bytes. For the bodies that are not defined in num_list_minus1 (for example, i = 5 to 7 when num_list_minus1 is set to 4), specify 0.
pList [i]	Specifies the start address of the i-th display list body (indicated by index i). Be sure to specify an address aligned with an 8-byte boundary (the lower-order three bits are 0). For the bodies that are not defined in num_list_minus1 (for example, i = 5 to 7 when num_list_minus1 is set to 4), specify 0.
pNext_header	Specifies the address of the display list header for the next frame. After display list downloading ends, the VSP1 keeps its value in the internal memory and uses it in the next display list header downloading.
current_frame_int_enable	This is a flag that indicates whether to set the display list end interrupt source (VI6_WPFn_IRQ_STA.DFE) to 1 when the current frame processing ends. If this flag is set to 0, the display list end interrupt source (VI6_WPFn_IRQ_STA.DFE) is not set to 1 when one-frame processing by this display header ends. In this state, even if the display list end interrupt is enabled (VI6_WPFn_IRQ_ENB.DFEE is set to 1), no interrupt will be generated. If this flag is set to 1, the display list end interrupt source (VI6_WPFn_IRQ_STA.DFE) is set to 1 when one-frame processing by this display header ends. In this state, if the display list end interrupt is enabled (VI6_WPFn_IRQ_ENB.DFEE is set to 1), the VSP1 generates an interrupt.
Next_frame_auto_start	Enables or disables automatic start of next frame processing when one-frame processing by this display header ends. If this bit is set to 1, the VSP1 starts next frame processing as soon as one-frame processing by this display header ends, and starts downloading the next frame display header from the pNext_header address specified in this display header. If this bit is set to 0, the VSP1 stops operation when one-frame processing by this display header ends. In this case, start the VSP1 through VI6_CMDn to process the next frame.
pre_ext_dl_exec	Enables execution of the extended display list for frame preprocessing when VI6_DL_EXT_CTRL.EXT is 1. If this bit is set to 1, the VSP1 executes the extended display list for frame preprocessing. The VSP1 does not execute it if this bit is set to 0. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
post_ext_dl_exec	Enables execution of the extended display list for frame post processing when VI6_DL_EXT_CTRL.EXT is 1. If this bit is set to 1, the VSP1 executes the extended display list for frame post processing. The VSP1 does not execute it If this bit is set to 0. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
pre_ext_dl_num_cmd	Specifies the number of commands in the extended display list body section for frame preprocessing when VI6_DL_EXT_CTRL.EXT is 1. The number of commands that can be specified is 1 to 65,535, and a command is 16 bytes. When pre_ext_dl_exec is set to 0, the extended display list for frame preprocessing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
pre_ext_dl_pList	Specifies the start address of the area where the extended display list body section for frame preprocessing is stored when VI6_DL_EXT_CTRL.EXT is 1. Be sure to specify an address aligned with a 16-byte boundary (lower-order four bits are 0). When pre_ext_dl_exec is set to 0, the extended display list for frame preprocessing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.
post_ext_dl_num_cmd	Specifies the number of commands in the extended display list body section for frame post processing when VI6_DL_EXT_CTRL.EXT is 1. The number of commands that can be specified is 1 to 65,535, and a command is 16 bytes. When post_ext_dl_exec is set to 0, the extended display list for frame post processing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.

Bit String	Contents
post_ext_dl_pList	Specifies the start address of the area where the extended display list body section for frame post processing is stored when VI6_DL_EXT_CTRL.EXT is 1. Be sure to specify an address aligned with a 16-byte boundary (lower-order four bits are 0). When post_ext_dl_exec is set to 0, the extended display list for frame post processing is not executed; specify 0 in this bit. This bit setting is ignored when VI6_DL_EXT_CTRL.EXT is 0.

Table 25.11 Format of Display List Body Section

Syntax	Bit Count
display_list (num_bytes) /* Variable length (num_bytes) */	
{	
for (i = 0; i<num_bytes; i+=8) {	
set_address	32
set_data	32
}	
}	

Bit String	Contents
set_address	Specifies the address where the value specified by set_data is to be stored. Specify a register address.
set_data	Specifies the value to be stored in the address specified by set_address. Specify a value to be set in a register.

Table 25.12 Format of Extended Display List Body Section

Syntax	Bit width
ext_dl_display_list (num_llw) /* Variable length (pre/post_ext_dl_num_bytes) */	
{	
for (i = 0; i<num_llw; i+=2) {	
ext_dl_cmd	64
ext_dl_data	64
}	
}	

Bit string	Contents
ext_dl_cmd	ext_dl_cmd specifies a 64-bit control command for the extended display list. The upper-order 32 bits hold a command and the lower-order 32 bits are bits for masking or enabling data to be handled by the command. In the upper-order 32 bits (command), bits 63 to 43 should always be set to 0, bits 42 to 40 specify data swapping during command execution (described later), and bits 39 to 32 specify the command type. Bit 42: Data swapping in long word (32-bit) units during command execution When this bit is 1, the data read or written for command execution is swapped in long word (32-bit) units. Bit 41: Data swapping in word (16-bit) units during command execution When this bit is 1, the data read or written for command execution is swapped in word (16-bit) units. Bit 40: Data swapping in byte (8-bit) units during command execution When this bit is 1, the data read or written for command execution is swapped in byte (8-bit) units. Bits 39 to 32 are H'00: Write Data The value stored in ext_dl_data [31:0] is written to the address stored in ext_dl_data [63:32] specified after this command. In the lower-order 32 bits of this command (ext_dl_cmd [31:0]), specify the bits whose value should be updated with the value of ext_dl_data [31:0]. Specify 1 for the bits whose value should be updated, and specify 0 for the bits whose current value should be retained. Bits 39 to 32 are H'01: Wait Event Until the value stored in the address indicated by ext_dl_data [63:32] specified after this command matches the value stored in ext_dl_data [31:0], processing of this extended display list body section is stalled. The bits used for comparison are masked with the lower-order 32 bits of this command (ext_dl_cmd [31:0]). To compare all bits, the lower-order 32 bits of this command should be set to all 1s.
ext_dl_data	Specifies the data used by ext_dl_cmd [63:0]. When ext_dl_cmd [39:32] is H'0000, specify these bits as follows. ext_dl_data [63:32]: Write destination address ext_dl_data [31:0]: Write data When ext_dl_cmd [39:32] is H'0001, specify these bits as follows. ext_dl_data [63:32]: Reference address ext_dl_data [31:0]: Comparison data

(3) Header-less Display List Mode

The header-less display list does not have the display header listed in Table 25.10, and it has the simplest structure that has only single body. The extended display list function is not available in case of the header-less display list mode. Set the value 1 to VI6_DL_CTRL.NH0 (see section 25.2.6.1) to use the header-less display list. The start address downloaded by the header-less display list should be set to VI6_DL_HDR_ADDR0. And the size of the display body which is originally defined in the display header should be set to VI6_DL_BODY_SIZE0. The header-less display list is available only in WPF0.

(4) Restrictions on Display List Usage

Access to the general control registers and display list control registers through a display list is prohibited. When using display lists, be sure to observe the following restrictions on register access by the CPU.

1. Do not execute write access to the same register (same address) from the CPU and through a display list at the same time. If such a conflict occurs, correct operation of the VSP1 is not guaranteed.
2. Do not execute write access to the same CLUT, CLU, or LUT lookup table from the CPU and through a display list at the same time. If such a conflict occurs, correct operation of the VSP1 is not guaranteed. Here, the same lookup table means the address space having the same space name shown in Table 25.36 or Table 25.37.
3. When read access by the CPU and write access through a display list to the same register (same address) occur at the same time, the read value returned to the CPU is not guaranteed.
4. When read access by the CPU and write access through a display list to the same CLUT, CLU, or LUT lookup table occur at the same time, the read value returned to the CPU is not guaranteed. Here, the same lookup table means the address space having the same space name shown in Table 25.36 or Table 25.37.
5. For other restrictions on values and timing of register setting through display lists, refer to the restrictions on normal register settings described in section 25.2.3.
6. Manipulation and setting of the registers described in sections 25.2.4 and 25.2.6 through a display list is prohibited.
7. Do not use extended display lists on this LSI.

25.1.9 Interrupt Processing

The VSP1 provides multiple image processing channels (WPF0 to WPF3) and they can operate simultaneously in parallel. When a WPF module generates an internal source that should be notified, an interrupt signal is output. As internal sources are generated in each WPF independently, the VSP1 has the following registers to control interrupts in each WPF.

- WPF Interrupt Enable Registers (VI6_WPFn_IRQ_ENB: n = 0, 1, 2, 3) (refer to section 25.2.5.5)
- WPF Interrupt Status Registers (VI6_WPFn_IRQ_STA: n = 0, 1, 2, 3) (refer to section 25.2.5.6)

While multiple WPF modules operate in parallel, they may output interrupt requests at the same time (this is called a multiple interrupt state). Read the WPF Interrupt Status Registers (VI6_WPFn_IRQ_STA: n = 0, 1, 2, 3) in sequence and execute the interrupt response processing for each interrupt source.

Note: To use interrupts, enable them through WPF interrupt enable registers. If an interrupt source register has already been set to 1 for some reason, an unintended interrupt will occur as soon as the corresponding interrupt enable register is set as enabled. To avoid this, before enabling interrupts through WPF interrupt enable registers, be sure to clear all WPF interrupt sources to be enabled to 0. Be careful about this procedure when setting up registers before starting the VSP1.

25.2 Registers Description

25.2.1 Notational Conventions for Registers and Bit Fields

This document uses the following notational conventions for the VSP1 registers and bit fields.

1. The names of registers and bits are written in uppercase.
2. A bit or bit field in a register is indicated as [register name.bit name]. For example, the STRCMD bit in the VI6_CMD0 register is indicated as VI6_CMD0.STRCMD.
3. Lowercase "n" in a register name or a bit name indicates an integer and the range of value n is defined when necessary. For example, VI6_CMDn.STRCMD (n = 0, 1) indicates the STRCMD bit in two registers VI6_CMD0.STRCMD and VI6_CMD1.STRCMD. For RPFn, WPFn, and UDSn, when the range of value n is not defined, RPFn (n = 0, 1, 2, 3, 4), WPFn (n = 0, 1, 2, 3), and UDSn (n = 0, 1, 2) are assumed.
4. In each subsection for register description in section 25.2, when only a bit name is written without showing its register name, the bit is in the register described in that subsection.
5. A wildcard (*) indicates any characters in a name and represents all registers or bits that match the specified first part of a name. For example, VI6_RPF_SRC_* indicates both VI6_RPF_SRC_BSIZE and VI6_RPF_SRC_ESIZE register.

25.2.2 Register Configuration

The VSP1 registers are arranged in the following order; the general control registers to frame sync control registers control operation of the entire R-VSP1, and the other registers control each image processing and specify parameters for the processing. The functions of the registers are described in this order starting from section 25.2.4.

1. General control registers (VI6_CMDn (n = 0, 1, 2, 3), VI6_SRESET, VI6_STATUS, VI6_WPFn_IRQ_* (n = 0, 1, 2, 3))
2. Display list control registers (VI6_DL_*)
3. RPF control registers (VI6_RPFn_* (n = 0, 1, 2, 3, 4))
4. WPF control registers (VI6_WPFn_* (n = 0, 1, 2, 3))
5. DPR control registers (VI6_DPR_*)
6. SRU control registers (VI6_SRU_*)
7. UDSn control registers (VI6_UDSn_* (n = 0, 1, 2))
8. LUT control register (VI6_LUT_CTRL)
9. CLU control register (VI6_CLU_CTRL)
10. HST control register (VI6_HST_CTRL)
11. HSI control register (VI6_HSI_CTRL)
12. BRU control registers (VI6_BRU_*)
13. HGO control registers (VI6_HGO_*)
14. HGT control registers (VI6_HGT_*)
15. LIF control registers (VI6_LIF_*)
16. Security control registers (VI6_SECURE_*)

The VSP1 has five RPF channels and the register configuration is the same for all of RPF0 to RPF4. However, some bit fields have restrictions in certain RPFs. These restrictions are included in the description of the corresponding bit fields and registers. Likewise, the register configuration is the same for all four WPF channels (WPF0 to WPF3), but some bit fields have restrictions in certain WPFs; the restrictions are included in the description of the corresponding bit fields and registers.

For each register address, refer to section 25.2.4, Memory Map.

25.2.3 Restrictions on Access to Registers and Lookup Tables

The VSP1 has control registers and lookup tables. When accessing the addresses where these registers and lookup tables are allocated, the following restrictions should be satisfied. If any restriction is violated, the VSP1 will not operate correctly.

1. For the read-only bits and reserved bits in all VSP1 registers, writing 1 is prohibited unless otherwise specified.
2. Addresses undefined in section 25.2.4, Memory Map, are reserved areas and write access is prohibited in these areas.
3. For all registers and lookup tables, except VI6_SRESET and VI6_*IRQ*, modifying register values during operation of the module is prohibited. Modify registers while the corresponding module is stopped. For the operating status of the target module, refer to section 25.1.7.

Table 25.13 Correspondence between Modules and Register Names

Module Name	Register Name
RPFn (n = 0 to 4)	VI6_RPFn_*
WPFn (n = 0 to 3)	VI6_WPFn_*
DPR	VI6_DPR_*
SRU	VI6_SRU_*
UDSn (n = 0 to 2)	VI6_UDSn_*
LUT	VI6_LUT_CTRL
CLU	VI6_CLU_CTRL
HST	VI6_HST_CTRL
HSI	VI6_HSI_CTRL
BRU	VI6_BRU_*
HGO	VI6_HGO_*
HGT	VI6_HGT_*
LIF	VI6_LIF_*

25.2.4 Memory Map

(1) Base Address

Below are the base addresses of each VSP unit ($VSP_BASE) in this LSI:

VSPS: H'FE92 8000
VSPD0: H'FE93 0000

(2) Register/Table Address

Table 25.14 shows the VSP1 memory map (represents in relative address).

Table 25.14 VSP1 Memory Map

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit
Register	General control registers	VI6_CMD0	$VSP_BASE + H'0000
		VI6_CMD1 (VSPS only)	$VSP_BASE + H'0004
		VI6_CMD2 (VSPS only)	$VSP_BASE + H'0008
		VI6_CMD3 (VSPS only)	$VSP_BASE + H'000C
		VI6_CLK_DCSWT	$VSP_BASE + H'0018
		VI6_SRESET	$VSP_BASE + H'0028
		VI6_STATUS	$VSP_BASE + H'0038
		VI6_WPF0_IRQ_ENB	$VSP_BASE + H'0048
		VI6_WPF0_IRQ_STA	$VSP_BASE + H'004C
		VI6_WPF1_IRQ_ENB (VSPS only)	$VSP_BASE + H'0054
		VI6_WPF1_IRQ_STA (VSPS only)	$VSP_BASE + H'0058
		VI6_WPF2_IRQ_ENB (VSPS only)	$VSP_BASE + H'0060
		VI6_WPF2_IRQ_STA (VSPS only)	$VSP_BASE + H'0064
Register	General control registers	VI6_WPF3_IRQ_ENB (VSPS only)	$VSP_BASE + H'006C
		VI6_WPF3_IRQ_STA (VSPS only)	$VSP_BASE + H'0070
		VI6_DISP_IRQ_ENB	$VSP_BASE + H'0078
		VI6_DISP_IRQ_STA	$VSP_BASE + H'007C
		VI6_WPF0_LINE_CNT	$VSP_BASE + H'0084
		VI6_WPF1_LINE_CNT (VSPS only)	$VSP_BASE + H'0088
		VI6_WPF2_LINE_CNT (VSPS only)	$VSP_BASE + H'008C
		VI6_WPF3_LINE_CNT (VSPS only)	$VSP_BASE + H'0090
	Display list control registers	VI6_DL_CTRL	$VSP_BASE + H'0100
		VI6_DL_HDR_ADDR0	$VSP_BASE + H'0104
		VI6_DL_HDR_ADDR1	$VSP_BASE + H'0108
		VI6_DL_HDR_ADDR2	$VSP_BASE + H'010C
		VI6_DL_HDR_ADDR3	$VSP_BASE + H'0110
		VI6_DL_SWAP	$VSP_BASE + H'0114
		VI6_DL_EXT_CTRL	$VSP_BASE + H'011C
		VI6_DL_BODY_SIZE0	$VSP_BASE + H'0120

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit
Register	RPFn control registers n = 0, 1, 2, 3, 4: (VSPS) n = 0, 1, 2, 3: (VSPD) See Tables 25.1 and 25.2.	VI6_RPFn_SRC_BSIZE	$VSP_BASE + H'0300 + H'0100 × n
		VI6_RPFn_SRC_ESIZE	$VSP_BASE + H'0304 + H'0100 × n
		VI6_RPFn_INFMT	$VSP_BASE + H'0308 + H'0100 × n
		VI6_RPFn_DSWAP	$VSP_BASE + H'030C + H'0100 × n
		VI6_RPFn_LOC	$VSP_BASE + H'0310 + H'0100 × n
		VI6_RPFn_ALPH_SEL	$VSP_BASE + H'0314 + H'0100 × n
		VI6_RPFn_VRTCOL_SET	$VSP_BASE + H'0318 + H'0100 × n
		VI6_RPFn_MSKCTRL	$VSP_BASE + H'031C + H'0100 × n
		VI6_RPFn_MSKSET0	$VSP_BASE + H'0320 + H'0100 × n
		VI6_RPFn_MSKSET1	$VSP_BASE + H'0324 + H'0100 × n
		VI6_RPFn_CKEY_CTRL	$VSP_BASE + H'0328 + H'0100 × n
		VI6_RPFn_CKEY_SET0	$VSP_BASE + H'032C + H'0100 × n
		VI6_RPFn_CKEY_SET1	$VSP_BASE + H'0330 + H'0100 × n
		VI6_RPFn_SRCM_PSTRIDE	$VSP_BASE + H'0334 + H'0100 × n
		VI6_RPFn_SRCM_ASTRIDE	$VSP_BASE + H'0338 + H'0100 × n
		VI6_RPFn_SRCM_ADDR_Y	$VSP_BASE + H'033C + H'0100 × n
		VI6_RPFn_SRCM_ADDR_C0	$VSP_BASE + H'0340 + H'0100 × n
		VI6_RPFn_SRCM_ADDR_C1	$VSP_BASE + H'0344 + H'0100 × n
		VI6_RPFn_SRCM_ADDR_AI	$VSP_BASE + H'0348 + H'0100 × n
	WPFn control registers n = 0, 1 ,2 ,3: (VSPS) n = 0: (VSPD) See Table 25.2.	VI6_WPFn_SRCRPF	$VSP_BASE + H'1000 + H'0100 × n
		VI6_WPFn_HSZCLIP	$VSP_BASE + H'1004 + H'0100 × n
		VI6_WPFn_VSZCLIP	$VSP_BASE + H'1008 + H'0100 × n
		VI6_WPFn_OUTFMT	$VSP_BASE + H'100C + H'0100 × n
		VI6_WPFn_DSWAP	$VSP_BASE + H'1010 + H'0100 × n
		VI6_WPFn_RNDCTRL	$VSP_BASE + H'1014 + H'0100 × n
		VI6_WPFn_DSTM_STRIDE_Y	$VSP_BASE + H'101C + H'0100 × n
		VI6_WPFn_DSTM_STRIDE_C	$VSP_BASE + H'1020 + H'0100 × n
		VI6_WPFn_DSTM_ADDR_Y	$VSP_BASE + H'1024 + H'0100 × n
		VI6_WPFn_DSTM_ADDR_C0	$VSP_BASE + H'1028 + H'0100 × n
		VI6_WPFn_DSTM_ADDR_C1	$VSP_BASE + H'102C + H'0100 × n
	WPF0 control register	VI6_WPF0_WRBCK_CTRL	$VSP_BASE + H'1034
	DPR control registers	VI6_DPR_RPF0_ROUTE	$VSP_BASE + H'2000
		VI6_DPR_RPF1_ROUTE	$VSP_BASE + H'2004
		VI6_DPR_RPF2_ROUTE	$VSP_BASE + H'2008
		VI6_DPR_RPF3_ROUTE	$VSP_BASE + H'200C
		VI6_DPR_RPF4_ROUTE (VSPS only)	$VSP_BASE + H'2010
		VI6_DPR_WPF0_FPORCH	$VSP_BASE + H'2014
		VI6_DPR_WPF1_FPORCH (VSPS only)	$VSP_BASE + H'2018
		VI6_DPR_WPF2_FPORCH (VSPS only)	$VSP_BASE + H'201C
		VI6_DPR_WPF3_FPORCH (VSPS only)	$VSP_BASE + H'2020
		VI6_DPR_SRU_ROUTE (VSPS only)	$VSP_BASE + H'2024
		VI6_DPR_UDS0_ROUTE	$VSP_BASE + H'2028
		VI6_DPR_UDS1_ROUTE	$VSP_BASE + H'202C
		VI6_DPR_UDS2_ROUTE	$VSP_BASE + H'2030
		VI6_DPR_CLU_ROUTE (VSPS only)	$VSP_BASE + H'2040

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit
Register	DPR control registers	VI6_DPR_HST_ROUTE	$VSP_BASE + H'2044
		VI6_DPR_HSI_ROUTE	$VSP_BASE + H'2048
		VI6_DPR_BRU_ROUTE	$VSP_BASE + H'204C
		VI6_DPR_HGO_SMPPT (VSPS only)	$VSP_BASE + H'2054
		VI6_DPR_HGT_SMPPT (VSPS only)	$VSP_BASE + H'2058
	SRU control registers (VSPS only)	VI6_SRU_CTRL0	$VSP_BASE + H'2200
		VI6_SRU_CTRL1	$VSP_BASE + H'2204
		VI6_SRU_CTRL2	$VSP_BASE + H'2208
	UDS0 control registers	VI6_UDS0_CTRL	$VSP_BASE + H'2300
		VI6_UDS0_SCALE	$VSP_BASE + H'2304
		VI6_UDS0_ALPTH	$VSP_BASE + H'2308
		VI6_UDS0_ALPVAL	$VSP_BASE + H'230C
		VI6_UDS0_PASS_BWIDTH	$VSP_BASE + H'2310
		VI6_UDS0_IPC	$VSP_BASE + H'2318
		VI6_UDS0_CLIP_SIZE	$VSP_BASE + H'2324
		VI6_UDS0_FILL_COLOR	$VSP_BASE + H'2328
	LUT control register (VSPS and VSPD)	VI6_LUT_CTRL	$VSP_BASE + H'2800
	CLU control register (VSPS only)	VI6_CLU_CTRL	$VSP_BASE + H'2900
	HST control register	VI6_HST_CTRL	$VSP_BASE + H'2A00
	HSI control register	VI6_HSI_CTRL	$VSP_BASE + H'2B00
	BRU control registers	VI6_BRU_INCTRL	$VSP_BASE + H'2C00
		VI6_BRU_VIRRPF_SIZE	$VSP_BASE + H'2C04
		VI6_BRU_VIRRPF_LOC	$VSP_BASE + H'2C08
		VI6_BRU_VIRRPF_COL	$VSP_BASE + H'2C0C
		VI6_BRUA_CTRL	$VSP_BASE + H'2C10
		VI6_BRUA_BLD	$VSP_BASE + H'2C14
		VI6_BRUB_CTRL	$VSP_BASE + H'2C18
		VI6_BRUB_BLD	$VSP_BASE + H'2C1C
		VI6_BRUC_CTRL	$VSP_BASE + H'2C20
		VI6_BRUC_BLD	$VSP_BASE + H'2C24
		VI6_BRUD_CTRL	$VSP_BASE + H'2C28
		VI6_BRUD_BLD	$VSP_BASE + H'2C2C
		VI6_BRU_ROP	$VSP_BASE + H'2C30

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit
Register	HGO control registers (VSPS and VSPD)	VI6_HGO_OFFSET	$VSP_BASE + H'3000
		VI6_HGO_SIZE	$VSP_BASE + H'3004
		VI6_HGO_MODE	$VSP_BASE + H'3008
		VI6_HGO_LB_TH	$VSP_BASE + H'300C
		VI6_HGO_LB0_H	$VSP_BASE + H'3010
		VI6_HGO_LB0_V	$VSP_BASE + H'3014
		VI6_HGO_LB1_H	$VSP_BASE + H'3018
		VI6_HGO_LB1_V	$VSP_BASE + H'301C
		VI6_HGO_LB2_H	$VSP_BASE + H'3020
		VI6_HGO_LB2_V	$VSP_BASE + H'3024
		VI6_HGO_LB3_H	$VSP_BASE + H'3028
		VI6_HGO_LB3_V	$VSP_BASE + H'302C
		VI6_HGO_R_HISTO_n (n = 0 to 63)	$VSP_BASE + H'3030 + 4n
		VI6_HGO_R_MAXMIN	$VSP_BASE + H'3130
		VI6_HGO_R_SUM	$VSP_BASE + H'3134
		VI6_HGO_R_LB_DET	$VSP_BASE + H'3138
		VI6_HGO_G_HISTO_n (n = 0 to 63)	$VSP_BASE + H'3140 + 4n
		VI6_HGO_G_MAXMIN	$VSP_BASE + H'3240
		VI6_HGO_G_SUM	$VSP_BASE + H'3244
		VI6_HGO_G_LB_DET	$VSP_BASE + H'3248
		VI6_HGO_B_HISTO_n (n = 0 to 63)	$VSP_BASE + H'3250 + 4n
		VI6_HGO_B_MAXMIN	$VSP_BASE + H'3350
		VI6_HGO_B_SUM	$VSP_BASE + H'3354
		VI6_HGO_B_LB_DET	$VSP_BASE + H'3358
		VI6_HGO_REGRST	$VSP_BASE + H'33FC
	HGT control registers (VSPS only)	VI6_HGT_OFFSET	$VSP_BASE + H'3400
		VI6_HGT_SIZE	$VSP_BASE + H'3404
		VI6_HGT_MODE	$VSP_BASE + H'3408
		VI6_HGT_HUE_AREA0	$VSP_BASE + H'340C
		VI6_HGT_HUE_AREA1	$VSP_BASE + H'3410
		VI6_HGT_HUE_AREA2	$VSP_BASE + H'3414
		VI6_HGT_HUE_AREA3	$VSP_BASE + H'3418
		VI6_HGT_HUE_AREA4	$VSP_BASE + H'341C
		VI6_HGT_HUE_AREA5	$VSP_BASE + H'3420
		VI6_HGT_LB_TH	$VSP_BASE + H'3424
		VI6_HGT_LB0 _H	$VSP_BASE + H'3428
		VI6_HGT_LB0_V	$VSP_BASE + H'342C
		VI6_HGT_LB1_H	$VSP_BASE + H'3430
		VI6_HGT_LB1_V	$VSP_BASE + H'3434
		VI6_HGT_LB2_H	$VSP_BASE + H'3438
		VI6_HGT_LB2_V	$VSP_BASE + H'343C
		VI6_HGT_LB3_H	$VSP_BASE + H'3440
		VI6_HGT_LB3_V	$VSP_BASE + H'3444
		VI6_HGT_HISTO_m_n (m = 0 to 5, n = 0 to 31)	$VSP_BASE + H'3450 + 128m + 4n

Space	Register Type	Register Name	Relative Address from Base Address of Each VSP Unit
Register	HGT control registers (VSPS only)	VI6_HGT_MAXMIN	$VSP_BASE + H'3750
		VI6_HGT_SUM	$VSP_BASE + H'3754
		VI6_HGT_LB_DET	$VSP_BASE + H'3758
		VI6_HGT_REGRST	$VSP_BASE + H'37FC
	LIF control registers (VSPD only)	VI6_LIF_CTRL	$VSP_BASE + H'3B00
		VI6_LIF_CSBTH	$VSP_BASE + H'3B04
	Security control registers	VI6_SECURE_CTRL0	$VSP_BASE + H'3D00
		VI6_SECURE_CTRL1	$VSP_BASE + H'3D04
CLUT	RPFn-CLUT n = 1, 2: (VSPS) n = 1: (VSPD) See Tables 25.1 and 25.2.	VI6_CLUTn_TBL0 ↓ VI6_CLUTn_TBL255	$VSP_BASE + H'4000 + H'0400 × n ↓ $VSP_BASE + H'43FF + H'0400 × n
LUT	1D-LUT (VSPS and VSPD)	VI6_LUT_TBL_0 ↓ VI6_LUT_TBL_255	$VSP_BASE + H'7000 ↓ $VSP_BASE + H'73FF
	3D-LUT (VSPS only)	VI6_CLU_ADDR	$VSP_BASE + H'7400
		VI6_CLU_DATA	$VSP_BASE + H'7404

Note: Do not access addresses other than listed above. Operations cannot be guaranteed if access is attempted.

25.2.5 General Control Registers

25.2.5.1 VSP1 Start Registers n (VI6_CMDn: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STRCMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STRCMD	0	R/W	Start Command VSP1 has four output channels (WPFs). Starting WPF0 to WPF3 starts operation of VSP1. Only a single WPF can be started, and all four WPFs can also be started at the same time. VI6_CMD0.STRCMD to VI6_CMD3.STRCMD respectively control WPF0 to WPF3. Writing 1 to this bit starts WPFn in VSP1. Set this bit for activation only after all register settings in each output channel have been completed. This bit is always read as 0. 0: NOP 1: WPFn is started (VSP1 is started).

The basic concept of image processing operation started by activating the VSP1 is shown in Figure 25.13. The actual data input/output is executed by the MAU, which is the bus interface module, as described in section 25.1.2, but conceptually the RPF works as the data entry point to the VSP1 and the WPF works as the data exit point. To process images through the VSP1, the RPF (entrance) and WPF (exit) should be connected and a data path from the RPF to the WPF should be formed.

To connect RPFn to WPFn, specify RPFn as the source RPF for WPFn in VI6_WPFn_SRCRPF, which is a register for WPFn (refer to section 25.2.8.1). This setting determines that RPFn will be started when WPFn is started through VI6_CMDn.

A data path to execute desired image processing should then be formed between the RPF (entrance) and WPF (exit). To form a data path, connect the necessary function modules in the VSP1 between RPF and WPF. This function is provided by the DPR; specify the information for each module connection in data path routing registers VI6_DPR_*_ROUTE (refer to section 25.2.9).

After a data path is formed (RPFn → WPFn) as described above, starting output module WPFn in the VSP1 through VI6_CMDn starts all function modules connected to WPFn and the desired image processing is executed. According to this design concept, starting a WPF module means starting the VSP1.

There are two types of data path configuration in the VSP1; one is "a single input module to a single output module" as shown in Figure 25.13 (A), and the other is "multiple input modules to a single output module" as shown in Figure 25.13 (B). Figure 25.13 (A) shows an example of a configuration where modules with single input and single output are

implemented through the DPR. Figure 25.13 (B) shows another configuration example where the module with multiple input and single output is implemented through the DPR. As shown in the figure, there is no conflict over internal module resources between these two connection examples, and the data paths in Figure 25.13 (A) and (B) can be started at the same time (for details of the DPR, refer to section 25.2.9). To start them together, make the register settings related to the modules used in each data path, and then set VI6_CMD0 and VI6_CMD2 to start WPF0 and WPF2, respectively. These two paths are completely independent. Even if the register settings for path (B) are incomplete, path (A) can be started regardless of the state of path (B) when the register settings for path (A) are complete.

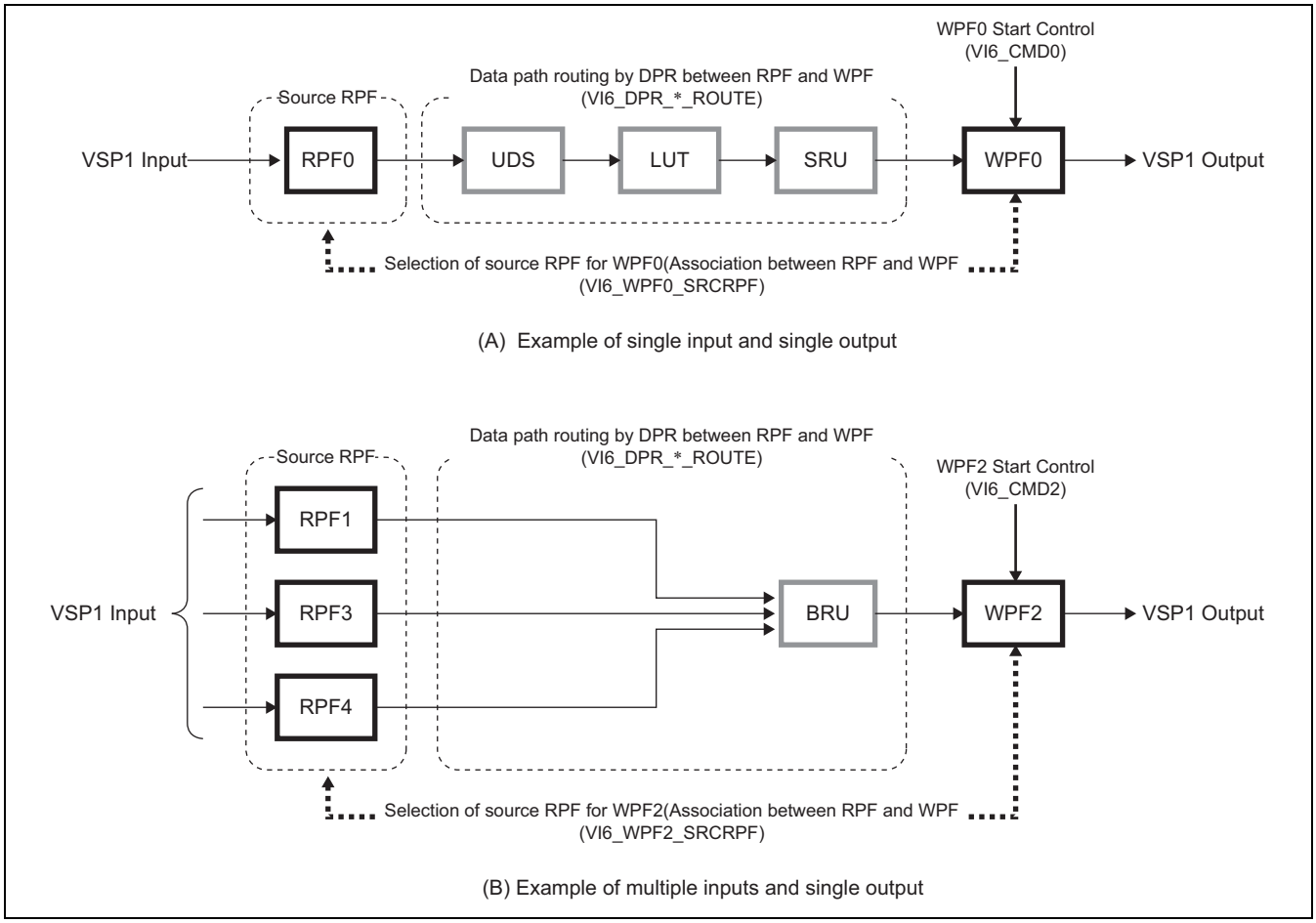


Figure 25.13 Basic Concept of VSP1 Startup

The DPR in the VSP1 can realize more advanced data paths than those shown in Figure 25.13. For example, two activations are necessary for the combination of paths (A) and (B) in Figure 25.13. However, the same processing may be started through one activation by improving the data path configuration, depending on the data processing flow in some cases, as shown in Figure 25.14. When the data path configuration is improved, the capacity of memory used and the amount of bus transfer in the system can be reduced. When determining the starting units in the VSP1, carefully examine the data processing flow and configure an optimal data path.

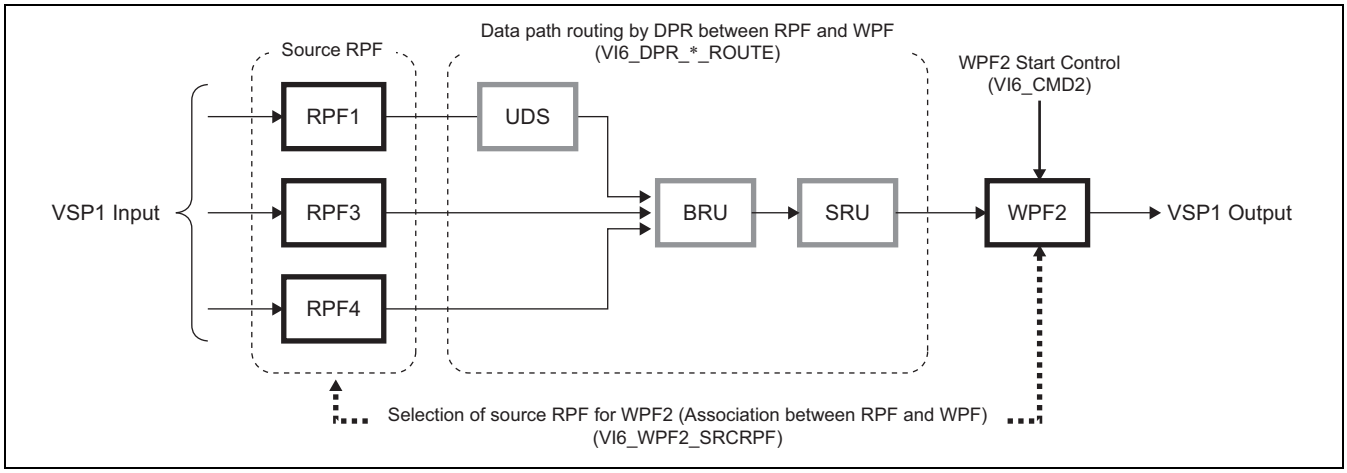
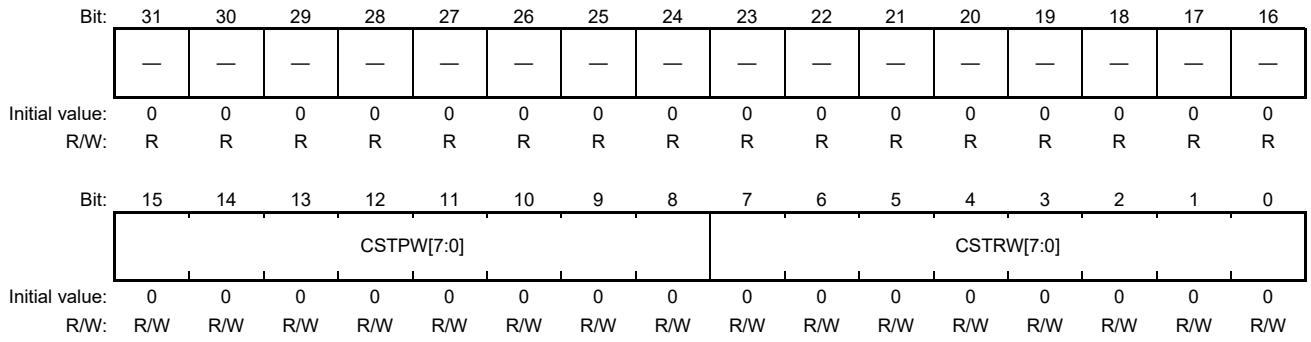


Figure 25.14 Sample Configuration of Combining Data Paths in Figure

25.2.5.2 Dynamic Clock Stop Control Register (VI6_CLK_DCSWT)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CSTPW[7:0]	H'00	R/W	Dynamic Clock Stop Control 1 Always specify 8.
7 to 0	CSTRW[7:0]	H'00	R/W	Dynamic Clock Stop Control 2 Always specify 8.

25.2.5.3 Software Reset Register (VI6_SRESET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SRST3	SRST2	SRST1	SRST0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	SRST3	0	R/W	WPFn Software Reset (SRSTn, n = 0 to 3) Writing 1 to this bit aborts the current processing in WPFn (the partially-completed image undergoing processing is output). The period until this software reset processing is completed depends on the bus state. When this reset processing is completed, the VI6_WPFn_IRQ_STA.FRE interrupt source bit is set to 1; when the FRE interrupt is enabled, the FRE end interrupt is output to notify the end of the reset processing. This bit is always read as 0. 0: NOP 1: WPF3 software reset*
2	SRST2	0	R/W	
1	SRST1	0	R/W	
0	SRST0	0	R/W	

Notes: * Applying a software reset to each WPF has the following restrictions.

1. A software reset can be applied to only one of WPF0 to WPF3 through single write access to VI6_SRESET.
2. After a software reset is issued, no more software reset can be issued to another WPF until the issued software reset processing is completed
3. After a software reset is issued to a channel, correct operation of other channels cannot be guaranteed; apply software reset to all channels in sequence.
4. The end of software reset processing is notified through the FRE bit in VI6_WPFn_IRQ_STA, but the software reset issued while WPF is stopped is ignored as NOP. As it takes a while until the reset is actually issued after the reset bit is set, the VSP1 may complete operation before the reset is actually issued. In this case, no interrupt is output for the software reset that is issued after the VSP1 completes operation.
5. If a software reset is issued during downloading of a display list, the downloading processing is not aborted. After the end of downloading that is in progress when a software reset is issued, a frame end interrupt is output.

25.2.5.4 Operating Status Register (VI6_STATUS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SYS3_ ACT	SYS2_ ACT	SYS1_ ACT	SYS0_ ACT	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are read as 0 or 1. Don’t care about this value. Write access is prohibited.
11	SYS3_ACT	0	R	WPFn Operating Status (SYSn_ACT, n = 0 to 3) Each bit indicates the operating or stopped state of control channel n (WPFn). 0: WPFn is stopped. 1: WPFn is operating.
10	SYS2_ACT	0	R	
9	SYS1_ACT	0	R	
8	SYS0_ACT	0	R	
7 to 4	—	All 0	R	Reserved These bits are read as 0 or 1. Don’t care about this value. Write access is prohibited.
3	—	0	R	WPFn Internal Control Monitor Signal Each bit indicates a value of 0 or 1. Don’t use the value read from this bit.
2	—	0	R	
1	—	0	R	
0	—	0	R	

25.2.5.5 WPF Interrupt Enable Registers (VI6_WPFn_IRQ_ENB: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFEE	FREE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	DFEE	0	R/W	Interrupt Enable for WPFn (n = 0 to 3) Display List Frame End 0: Interrupt Disabled 1: Interrupt Enabled
0	FREE	0	R/W	Interrupt Enable for WPFn (n = 0 to 3) Frame End 0: Interrupt Disabled 1: Interrupt Enabled

Each bit in VI6_WPFn_IRQ_STA is set to 1 when the corresponding interrupt source is generated. VI6_WPFn_IRQ_ENB specifies whether to output an interrupt signal for the generated source. When an interrupt is disabled in this register, no interrupt signal is generated even when the corresponding bit in VI6_WPFn_IRQ_STA is set to 1. When an interrupt is enabled in this register, an interrupt signal is output when the corresponding bit in VI6_WPFn_IRQ_STA is set to 1.

25.2.5.6 WPF Interrupt Status Registers (VI6_WPFn_IRQ_STA: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DFE	FRE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are read as 0 or 1. Don't care about this value. The write value should always be 0.
1	DFE	0	R/W	Interrupt Status and Clear for WPFn (n = 0 to 3) Display List Frame End This interrupt source bit is set to 1 when VSP1 completes one-frame processing while the current_frame_int_enable value stored in the display list header is 1 (refer to section 25.1.8 (2)). When display lists are not used, this bit is not used. In this case, clear VI6_WPFn_IRQ_ENB.DFEE to 0 to mask the interrupt generation by this interrupt source. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
0	FRE	0	R/W	Interrupt Status and Clear for WPFn (n = 0 to 3) Frame End This interrupt source bit is set to 1 when VSP1 completes one-frame processing. This bit is also set to 1 when one-frame processing using a display list is completed. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

VI6_WPFn_IRQ_STA indicates the state of the interrupt sources generated in the VSP1. Whether to output a VSP1 interrupt when an interrupt source is generated and the corresponding bit is set to 1 is determined by the corresponding bit setting in VI6_WPFn_IRQ_ENB. While an interrupt is disabled in VI6_WPFn_IRQ_ENB, the VSP1 does not output an interrupt signal even when an interrupt source is generated, but the source flag in this register is set to 1.

Note that the interrupt source bits in this register cannot be cleared by write access using a display list.

25.2.5.7 Display Interrupt Enable Register (VI6_DISP_IRQ_ENB)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DSTE	—	—	MAEE	LNE4E	LNE3E	LNE2XE	LNE1E	LNE0E
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DSTE	0	R/W	Interrupt Enable for Display Start 0: Interrupt Disabled 1: Interrupt Enabled
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	MAEE	0	R/W	Interrupt Enable for Display Read Data End 0: Interrupt Disabled 1: Interrupt Enabled
4	LNE4E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP4 0: Interrupt Disabled 1: Interrupt Enabled
3	LNE3E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP3 0: Interrupt Disabled 1: Interrupt Enabled
2	LNE2XE	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP2 0: Interrupt Disabled 1: Interrupt Enabled
1	LNE1E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP1 0: Interrupt Disabled 1: Interrupt Enabled
0	LNE0E	0	R/W	Interrupt Enable for 1 Line Data Read End of RFP0 0: Interrupt Disabled 1: Interrupt Enabled

25.2.5.8 Display Interrupt Status Register (VI6_DISP_IRQ_STA)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DST	—	—	MAE	LNE4	LNE3	LNE2X	LNE1	LNE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DST	0	R/W	Interrupt Status and Clear for Display Start This bit is set to 1 when LIF module transfers the first data to the display module at the beginning of each frame. The timing depends on the output buffer status of LIF module. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	MAE	0	R/W	Interrupt Status and Clear for Display Read Data End This bit is set to 1 when all RPFs transfer the last data of the frame to LIF module. The RPF module which is not used by LIF module does not affect this bit. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
4	LNE4	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP4 This bit is set to 1 when RPF4 completes 1-line data transfer. [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

Bit	Bit Name	Initial Value	R/W	Description
3	LNE3	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP3 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
2	LNE2X	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP2 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
1	LNE1	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP1 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value
0	LNE0	0	R/W	Interrupt Status and Clear for 1 Line Data Read End of RFP0 [Read Access] Interrupt Status 0: No interrupt 1: Interrupt activated [Write Access] Interrupt Clear 0: The interrupt status is cleared to 0 1: Hold the interrupt status value

25.2.5.9 WPFn Output Line Count Register (VI6_WPFn_LINE_CNT: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	LINE_CNT[20:16]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LINE_CNT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 0	LINE_CNT [20:0]	All 0	R	Number of WPFn Output Lines From the value read from these bits, the number of lines output from VSP1 can be obtained. The value of these bits can be read only within a limited period; read these bits with the timing described later. These bits indicate the number of lines output from WPFn as an immediate value. In the frame buffer starting from VI6_WPFn_DSTM_ADDR_*, WPFn has completed data output up to the line number indicated in these bits. For example, when these bits are set to 1, valid data is output only in the first line. When one-frame processing is competed correctly, this value indicates the number of lines output from WPFn.

The LINE_CNT value is valid only for the period between a frame end interrupt (section 25.2.5.6) and next frame startup (section 25.2.5.1) or the period between a display list frame end interrupt (section 25.2.5.6) and next frame startup. This register value read outside these periods cannot be used.

The LINE_CNT value depends on the flipping mode (VI6_WPFn_OUTFMT.FLP) as shown in Figure 25.15. This correspondence is shown in Table 25.15.

Table 25.15 VSP1 Output Line Count According to VI6_WPFn_OUTFMT.FLP Setting

VI6_WPFn_OUTFMT.FLP Setting	Corresponding Case Shown in Figure 25.15
0	case 1
1	case 2

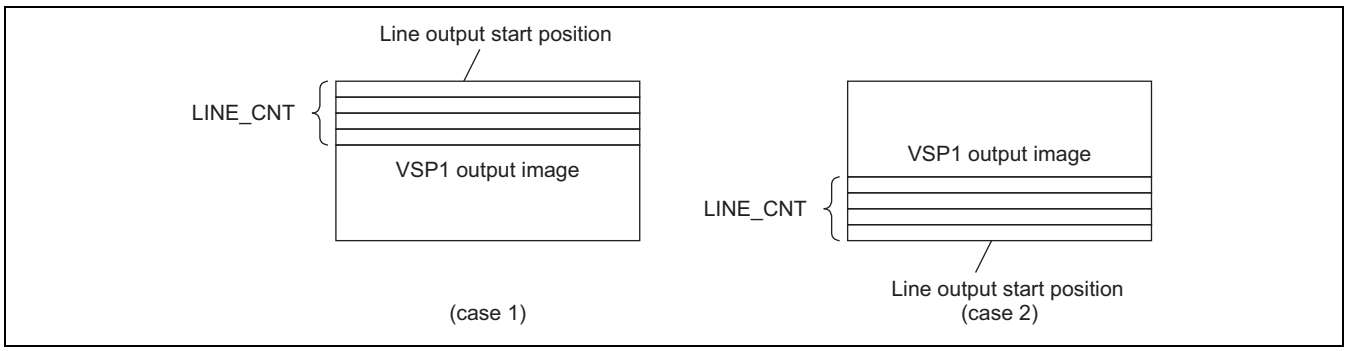
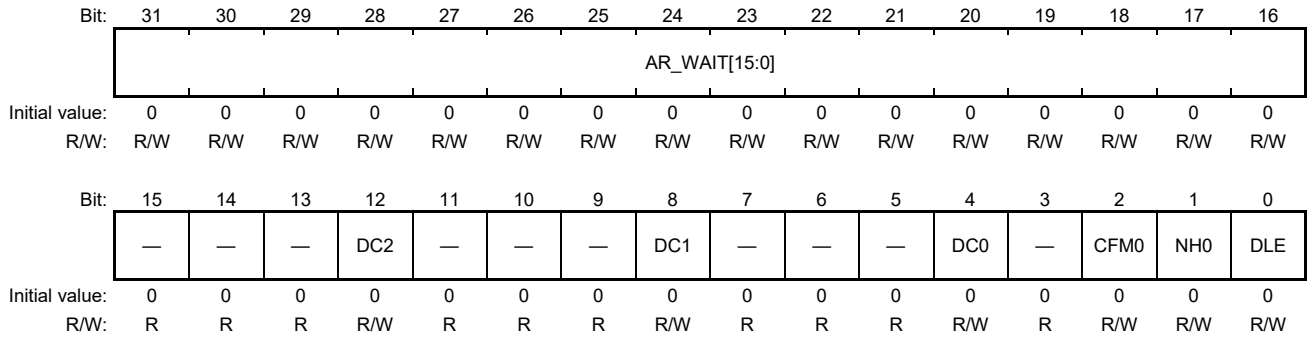


Figure 25.15 Definition of VSP1 Output Line Count

25.2.6 Display List Control Registers

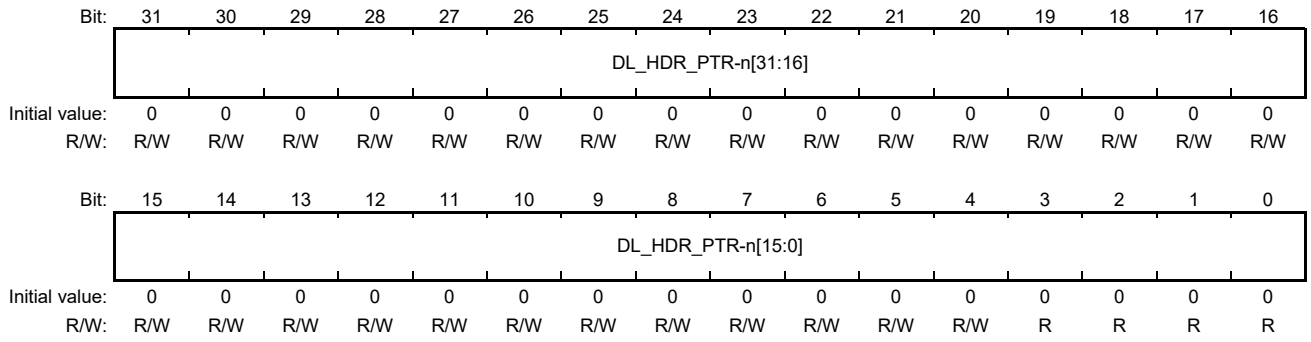
25.2.6.1 Display List Control Register (VI6_DL_CTRL)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	AR_WAIT [15:0]	H'0000	R/W	Display List Control Setting Always specify 256.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	DC2	0	R/W	Display List Control 2 Specify the same value as the DLE bit.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DC1	0	R/W	Display List Control 1 Specify the same value as the DLE bit.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DC0	0	R/W	Display List Control 0 Specify the same value as the DLE bit.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	CFM0	0	R/W	Continuous Frame Mode for Header-less Display List This bit determines whether the next frame is automatically started or not. When the updated flag of the display list, VI6_DL_BODY_SIZE0.UPD0, is not updated, the display list of the next frame is not transferred and the same register values are used for the next frame. When the value of VI6_DL_BODY_SIZE0.UPD0 is updated, the new display list is transferred. 0: Stopped at the end of every frame 1: The next frame is automatically started

Bit	Bit Name	Initial Value	R/W	Description
1	NH0	0	R/W	Header-less Display List Mode This bit is used for specifying the header-less display list mode. In case of header-less mode, the number of the display lists is 1. The address of the display body is set in VI6_DL_HDR_ADDR0 register, and the body size is set in VI6_DL_BODY_SIZE0 register. When this bit is changed, make sure that VSP1 is stopped. And also make sure the following before starting VSP1. - Header Address (VI6_DL_HDR_ADDR0) - Body Size (VI6_DL_BODY_SIZE0) in case of header-less mode 0: Use Display List Header (Normal DL Mode) 1: Don’t use Display List Header (Header-less Mode) Note: Only WPF0 supports header-less display list. WPFn (n = 1 to 3) work as the normal display list mode even if the WPF0 is set to header-less display list mode.
0	DLE	0	R/W	Display List Enable/Disable Enables or disables the VSP1 display list function. When the display list function is enabled through this bit, all WPF processing channels work in display list mode. When using display lists, note the restrictions in section 25.2.3. 0: The display list function is disabled 1: The display list function is enabled

25.2.6.2 Display List-n Header Address Register (VI6_DL_HDR_ADDRn: n = 0, 1, 2, 3)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DL_HDR_PTR-n [31:0]	H'0000 0000	R/W [31:4] R [3:0]	Display List-n Header Address These bits specify the address of the display list header to be read for display list-n in 16-byte units (the lower-order four bits are read-only). When WPFn is first started in display list mode, the display list header is loaded from the address specified in this register. After loading of the header is completed, the register value of the display list address is updated to the next header address stored in the loaded header to prepare for loading of the next display list header. After that, this header address updating is repeated. A value from H'00000000 to H'FFFFFFF0 can be specified.

25.2.6.3 Display List Data Swapping Register (VI6_DL_SWAP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LWS	WDS	BTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LWS	0	R/W	Display List Data Swapping in Longword Units 0: Data swapping in longword (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled
1	WDS	0	R/W	Display List Data Swapping in Word Units 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
0	BTS	0	R/W	Display List Data Swapping in Byte Units 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled

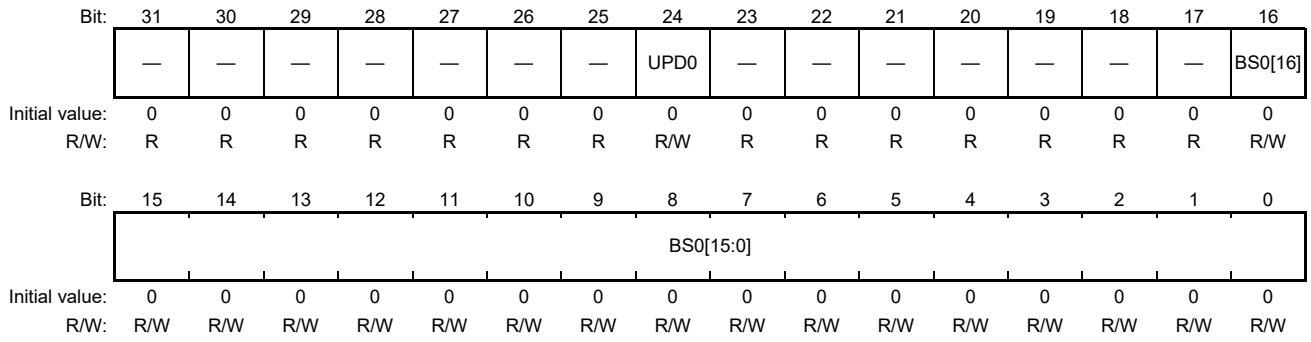
25.2.6.4 Extended Display List Control Register (VI6_DL_EXT_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	NWE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	POLINT[5:0]						—	—	DLPRI	EXPRI	—	—	—	EXT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	NWE	0	R/W	No Wait for Polling When this bit is set to 1, the polling condition for extended display lists is always assumed to be true.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	POLINT[5:0]	All 0	R/W	Extended Display List Command Control Always specify 2.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	DLPRI	0	R/W	Display List Control 0 Always specify 1.
4	EXPRI	0	R/W	Display List Control 1 Always specify 0.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	EXT	0	R/W	Extended Display List Enables or disables the extended display list function. When extended display lists are used, the display list header size is 96 bytes; when they are not used, the header size is 80 bytes. 0: No extended display lists are used 1: Extended display lists are used Note: When using extended display lists, be sure to also use normal display list mode (VI6_DL_CTRL.DLE); executing only extended display lists is not possible. When the header-less display list mode is activated, this bit should be set to 0. The extended display list cannot be used with the header-less display list mode.

25.2.6.5 Display List Body Size Register-n (VI6_DL_BODY_SIZEn: n = 0)



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	UPD0	—	—	—	—	—	—	—	BS0[16]
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BS0[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	UPD0	0	R/W	Update Flag This bit controls the download of the display list at the next downloading timing in case that the header-less display list mode is used. When this bit is set to 1, the value of VI6_DL_HDR_ADDRn and VI6_DL_BODY_SIZEn.BS0 (n = 0) should not be changed. 0: Display List is not downloaded (Registers are not updated) 1: Display List is downloaded (Registers are updated)
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16 to 0	BS0[16:0]	H'00000	R/W	Header-less Display List Body Size (WPFn, n = 0) These bits are used for specifying the body size of the display list in case of header-less display list mode. The unit of the size is byte. The value should be set in multiples of 8.

25.2.7 RPF Control Registers

25.2.7.1 RPFn Basic Read Size Registers (VI6_RPFn_SRC_BSIZE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BHSIZE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	BVSIZE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	BHSIZE [12:0]	H'0000	R/W	Horizontal Size of RPF Basic Read Area These bits specify the horizontal size of the basic area to be read from the external RAM by the RPFn. When the input format is YCbCr4:2:2 or YCbCr4:2:0, specify the size in 2-pixel units. A value from 1 to 8,190 can be specified. Specify a value equal to or smaller than the extended read size (VI6_RPFn_SRC_ESIZE.EHSIZE).
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	BVSIZE [12:0]	H'0000	R/W	Vertical Size of RPF Basic Read Area These bits specify the vertical size of the basic area to be read from the external RAM by the RPFn. When the input format is YCbCr4:2:0, specify the size in 2-pixel units. A value from 1 to 8,190 can be specified. Specify a value equal to or smaller than the extended read size (VI6_RPFn_SRC_ESIZE.EVSIZE).

Figure 25.16 shows the relationship between the basic read size and extended read size. The RPF reads data from the source memory area specified by the basic read size. The RPF repeats reading the basic read area in the horizontal and vertical directions up to the extended read size and sends the read data to the processing modules in the VSP1.

For basic read size reading, the reading start address, called the RPFn source image storing address, should be specified in VI6_RPFn_SRCM_ADDR_*. In the memory area where the basic read area image is stored, the distance (number of bytes) between addresses for lines n and n + 1 of two-dimensional image data, called the memory stride, should be specified in VI6_RPFn_SRCM_PSTRIDE.

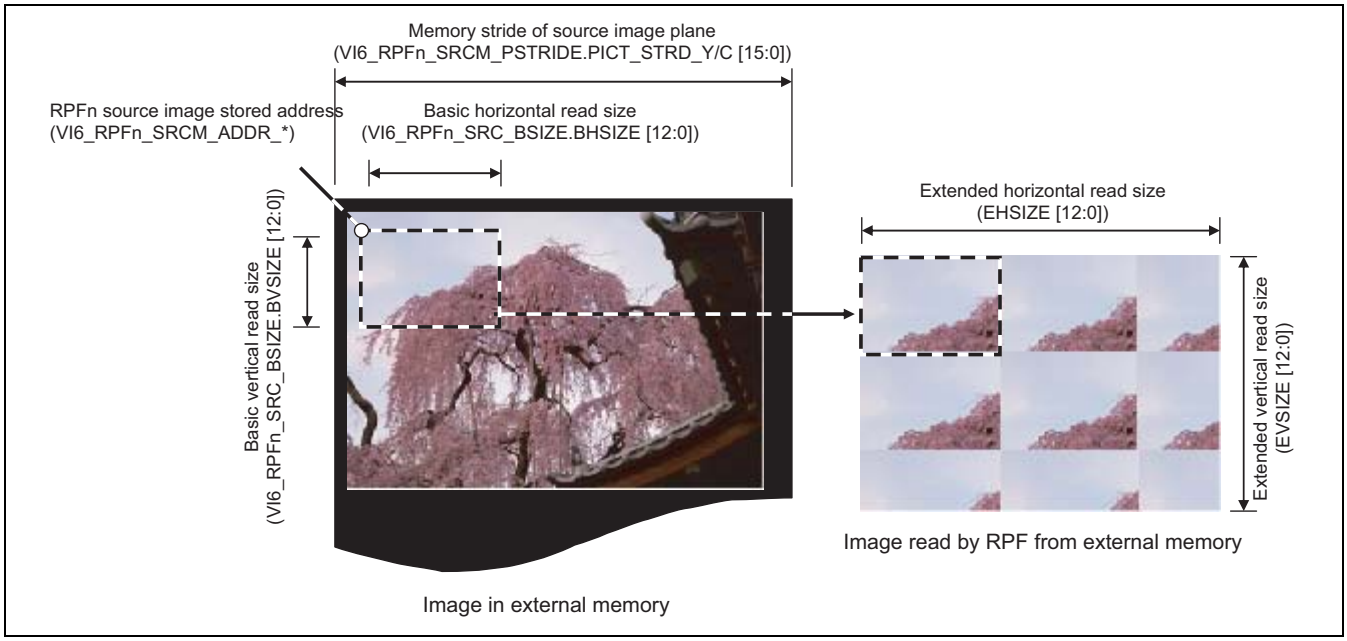


Figure 25.16 Relationship between Basic Read Size and Extended Read Size

Refer also to the following sections.

- Section 25.2.7.2, RPFn Extended Read Size Registers (VI6_RPFn_SRC_ESIZE)
- Section 25.2.7.13, RPFn Source Picture Memory Stride Setting Registers (VI6_RPFn_SRCM_PSTRIDE)
- Section 25.2.7.15, RPFn Source Y/RGB Address Registers (VI6_RPFn_SRCM_ADDR_Y)
- Section 25.2.7.16, RPFn Source Chroma Address Registers 0 (VI6_RPFn_SRCM_ADDR_C0)
- Section 25.2.7.17, RPFn Source Chroma Address Registers 1 (VI6_RPFn_SRCM_ADDR_C1)

25.2.7.2 RPFn Extended Read Size Registers (VI6_RPFn_SRC_ESIZE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	EHSIZE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EVSIZE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	EHSIZE [12:0]	H'0000	R/W	RPF Extended Horizontal Read Size These bits specify the horizontal size of the extended read area to which the RPFn reads data from the external RAM. As shown in Figure 25.16, the basic read area image is repeatedly placed in the extended read area; in the EHSIZE bits, specify a value not smaller than the horizontal size of the basic read area. When the input format is YCbCr4:2:2 or YCbCr4:2:0, specify the size in 2-pixel units (an even value). A value from 1 to 8,190 can be specified.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	EVSIZE [12:0]	H'0000	R/W	RPF Extended Vertical Read Size These bits specify the vertical size of the extended read area to which the RPFn reads data from the external RAM. As shown in Figure 25.16, the basic read area image is repeatedly placed in the extended read area; in the EVSIZE bits, specify a value not smaller than the vertical size of the basic read area. When the input format is YCbCr4:2:0, specify the size in 2-pixel units (en even value). A value from 1 to 8,190 can be specified.

VI6_RPFn_SRC_ESIZE specifies the extended size for RPFn. The extended horizontal and vertical sizes should be equal to or greater than the basic sizes specified in VI6_RPFn_SRC_BSIZE. The RPF internal data processing described later and image processing described in section 25.2.9 and later sections are all applied to the image in the extended read size shown on the right side in Figure 25.16.

25.2.7.3 RPFn Input Format Registers (VI6_RPFn_INFMT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VIR	—	—	—	—	—	—	—	—	—	—	—	CIPM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPYCS	SPUVS	CEXT[1:0]		RDTM[2:0]			CSC	—	RDFMT[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	VIR	0	R/W	Virtual Input Enable Enables or disables the virtual input function of the RPFn. The image to be processed by the RPFn is usually read from the external memory by the MAU. Instead of this input, the virtual input function generates a single-color image within the RPFn and sends it to the modules in VSP1. When the virtual input function is enabled, the fixed value specified in VI6_RPFn_VRTCOL_SET is used as the input to the RPFn. While the virtual input function is enabled, data is not read from the external memory; that is, the α plane is not read and the IROP calculation thus cannot be executed. In this case, set VI6_RPFn_ALPH_SEL.ASEL to 4. Neither the color space conversion through CSC nor the color keying described in section 25.2.7.11 can be used. 0: RPFn uses general input. 1: RPFn uses virtual input.
27 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	CIPM	0	R/W	Horizontal Chrominance Interpolation Method Setting Image data is processed in the YCbCr444 format inside VSP1 in case of YCbCr color space. When the chrominance format of the input image is YCbCr422 or YCbCr420, data is upsampled as shown in Figure 25.17 for internal processing. This bit specifies the method of upsampling for this purpose. 0: The nearest-neighbor method is used for horizontal chrominance interpolation. 1: The bilinear method is used for horizontal chrominance interpolation.
15	SPYCS	0	R/W	RPF Input Mode Setting 1 When the input format is YUY2, set this bit to 1 and set the RDFMT bits to 71 (H'47). When the input format is YVYU, set this bit and the SPUVS bit to 1 and set the RDFMT bits to 71 (H'47). In other cases, set this bit to 0.

Bit	Bit Name	Initial Value	R/W	Description
14	SPUVS	0	R/W	RPF Input Mode Setting 2 When the input format is NV61, set this bit to 1 and set the RDFMT bits to 65 (H'41). When the input format is NV21, set this bit to 1 and set the RDFMT bits to 66 (H'42). When the input format is YVYU, set this bit and the SPYCS bit to 1 and set the RDFMT bits to 71 (H'47). In other cases, set this bit to 0.
13, 12	CEXT[1:0]	00	R/W	Lower-Bit Color Data Extension Method Setting When an RGB input format where each color component is expressed in less than eight bits are selected from Table 25.17 through the RDFMT bits, VSP1 internally extends each color component to eight bits before using the data. These bits select this extension method. 00: Lower-order bits of color data are extended with 0. 01: Upper-order bits of color data are copied to the lower -order bits. 10: Lower-order bits of color data are extended with 0. The maximum value is limited to H'FF. 11: Setting prohibited
11 to 9	RDTM[2:0]	000	R/W	CSC Conversion Expression Setting These bits select the expression used for color space conversion. The conversion direction is RGB → YCbCr when RGB is selected through the RDFMT bits; the direction is YCbCr → RGB when YCbCr is selected. 000: BT.601 YCbCr [16,235/240] ↔ RGB [0,255] 001: BT.601 YCbCr [0,255] ↔ RGB [0,255] 010: BT.709 YCbCr [16,235/240] ↔ RGB [0,255] 011: BT.709 YCbCr [16,235/240] ↔ RGB [16,235] 100 to 111: Setting prohibited
8	CSC	0	R/W	Color Space Conversion Enable Enables or disables color space conversion between YCbCr and RGB to be executed in RPFn. The characteristics of color space conversion are determined by the RDTM bit setting.* When using the virtual input (VIR = 1), specify 0. 0: Color space conversion is disabled. 1: Color space conversion is enabled.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	RDFMT [6:0]	H'00	R/W	RPF Input Image Format Setting These bits select the format of the image input from the external RAM to the RPFn. Select a value corresponding to the desired format from those shown in Table 25.17 and Table 25.18. When the virtual input function is used (VIR = 1), the color information for the virtual input should be specified in VI6_RPFn_VRTCOL_SET. If this color information is in the RGB format, set the RDFMT bits to 19. If the color information is in the YCbCr format, set these bits to 64. Notes: 1. Number of input pixels When YCbCr4:2:2 is selected through the RDFMT bits, the horizontal size of the input image should be specified in 2-pixel units. When YCbCr4:2:0 is selected, the vertical and horizontal sizes should be specified in 2-pixel units. Observe these restrictions when specifying the image size in VI6_RPFn_SRC_BSIZE and VI6_RPFn_SRC_ESIZE. 2. CLUT Setting When the RDFMT bits are set to H'3F, RGB color data should be stored in the CLUT. When these bits are set to H'7F, YCbCr color data should be stored in the CLUT. Note that while the target WPF is operating, the RPF is also operating and the CLUT cannot be read or written to.

Note: * Note on color space settings

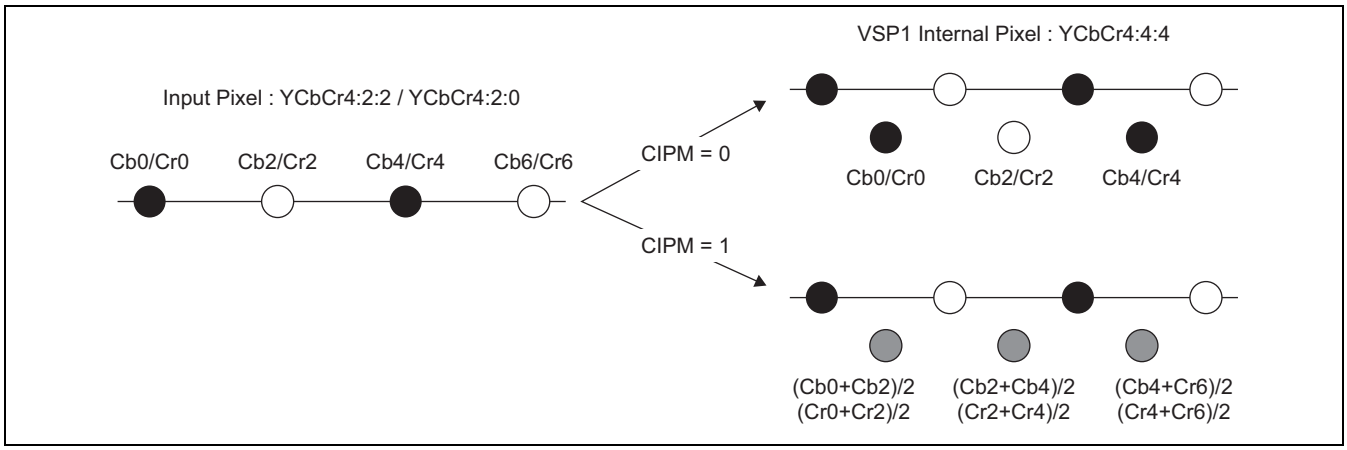


Figure 25.17 Chrominance Interpolation Methods Selectable through CIPM Setting

The color space for the image output from the RPF to VSP1 internal modules is determined by the combination of the color space for the image input to the RPF, which is selected through the VI6_RPFn_INFMT.RDFMT setting, and the enabled or disabled state of the color space conversion function, which is selected through the VI6_RPFn_INFMT.CSC setting (Table 25.16). For example, when the image input to the RPF is in the YCbCr format, the RPF outputs data to VSP1 internal modules in the YCbCr format if color space conversion is disabled through the CSC bit, and the RPF outputs data in the RGB format if color space conversion is enabled. When the image input to the RPF is in the RGB format, the relationship between the output format and the color space conversion setting is the opposite of the YCbCr case. For some VSP1 internal modules, the YCbCr format is recommended for image processing because of the characteristics of the processing, or the same color space needs to be specified between multiple RPF outputs. In these cases, set VI6_RPFn_INFMT.RDFMT and VI6_RPFn_INFMT.CSC appropriately so that the RPFs can output the required color space according to the color space conditions described above.

Table 25.16 RPFn Input Color Space and Output Color Space

RPFn Input Color Space (VI6_RPFn_INFMT. RDFMT)		Color Space Conversion Setting (VI6_RPFn_INFMT.CSC)		RPFn Output Color Space
RGB	(H'00 to H'3F)*	Disabled	(0) *	RGB
		Enabled	(1) *	YCbCr
YCbCr	(H'40 to H'7F)*	Disabled	(0) *	YCbCr
		Enabled	(1) *	RGB

Note: * Value specified in the register

A color space conversion function equivalent to that in the RPFn is also provided by the WPF. As shown in Table 25.16, the color space (YCbCr or RGB) output from the RPF becomes the input format for the WPF. Here, the color space of the output image obtained by the color space conversion function of the WPF must match the color space of the format specified through VI6_WPFn_OUTFMT.WRFMT.

Figure 25.18 shows the relationship between the input/output format and color space. The input color space for the RPF is determined when the input image format for the RPF is specified through the RDFMT bits. The color space for the image output from the RPF to subsequent VSP1 internal modules depends on the combination of the RPF input format and CSC (color space conversion function) enabled or disabled state in the RPF as shown in Table 25.16 and Figure 25.18. The user should first determine whether the image processing in the VSP1 is done in YCbCr or RGB, and then specify the RPF input format and CSC enabled or disabled state to obtain the desired color space. The color space of the RPF output image is also that of the WPF input image; the color space of the data output from the WPF to the outside of VSP1 depends on the combination of the WPF input color space and the enabled or disabled state of the CSC implemented in the WPF as shown in Figure 25.18. The color space of the WPF output image must match that of the WPF output format (determined by VI6_WPFn_OUTFMT.WRFMT). For example, in the flow shown in Figure 25.18, YCbCr should not be specified as the WPF output format regardless of the fact that the color space of the WPF output image is in RGB format.

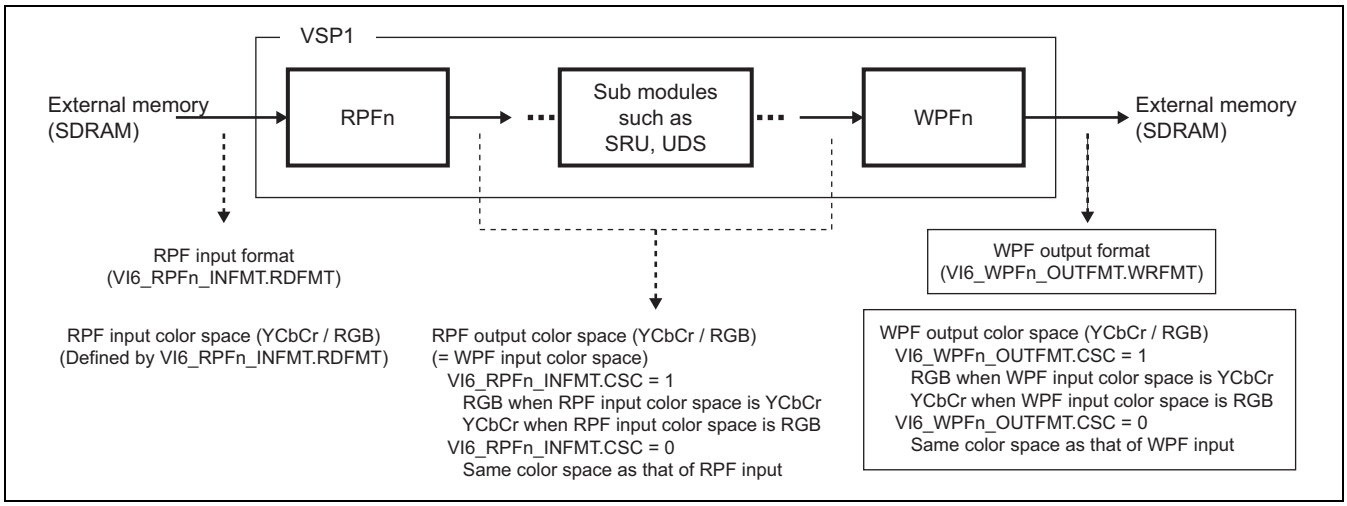


Figure 25.18 Relationship between Input/Output Format and Color Space

Table 25.17 Packed Formats for RPF Input

RDFMT	Bit per pixel	Phase	Bit field																													
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H'00	8	—	R0	R0	R0	G0	G0	G0	B0	B0	R1	R1	R1	G1	G1	G1	B1	B1	R2	R2	R2	G2	G2	G2	B2	B2	R3	R3	R3	G3	G3	G3	B3	B3
H'01	12	—					R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0					R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'02		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0					R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1				
H'03	—	—	Reserved								Reserved								Reserved								Reserved							
H'04	15	—		R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0		R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'05		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0		R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	
H'06	16	—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'07	18	—	A0	A0	A0	A0	A0	A0	A0	A0							R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'08		—	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0							A0	A0	A0	A0	A0	A0	A0	A0
H'09		—							R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	A0	A0	A0	A0	A0	A0	A0	A0
H'0A		—	A0	A0	A0	A0	A0	A0	A0	A0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0						
H'0B		—	A0	A0	A0	A0	A0	A0	A0	A0			R0	R0	R0	R0	R0	R0			G0	G0	G0	G0	G0	G0			B0	B0	B0	B0	B0	B0
H'0C		—			R0	R0	R0	R0	R0	R0			G0	G0	G0	G0	G0	G0			B0	B0	B0	B0	B0	B0	A0	A0	A0	A0	A0	A0	A0	A0
H'0D		—	A0	A0	A0	A0	A0	A0	A0	A0	R0	R0	R0	R0	R0	R0			G0	G0	G0	G0	G0	G0			B0	B0	B0	B0	B0	B0		
H'0E		—	R0	R0	R0	R0	R0	R0			G0	G0	G0	G0	G0	G0			B0	B0	B0	B0	B0	B0			A0	A0	A0	A0	A0	A0	A0	A0
H'0F		0							R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0							R1	R1
		1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1							R2	R2	R2	R2	R2	R2	G2	G2	G2	G2
		2	G2	G2	B2	B2	B2	B2	B2	B2							R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3
H'10		0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0							R1	R1	R1	R1	R1	R1	G1	G1
		1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1							R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	B2	B2	B2	B2
		2	B2	B2							R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3						
H'11		0			R0	R0	R0	R0	R0	R0			G0	G0	G0	G0	G0	G0			B0	B0	B0	B0	B0	B0			R1	R1	R1	R1	R1	R1
		1			G1	G1	G1	G1	G1	G1			B1	B1	B1	B1	B1	B1			R2	R2	R2	R2	R2	R2			G2	G2	G2	G2	G2	G2
		2			B2	B2	B2	B2	B2	B2			R3	R3	R3	R3	R3	R3			G3	G3	G3	G3	G3	G3			B3	B3	B3	B3	B3	B3
H'12		0	R0	R0	R0	R0	R0	R0			G0	G0	G0	G0	G0	G0			B0	B0	B0	B0	B0	B0			R1	R1	R1	R1	R1	R1		
		1	G1	G1	G1	G1	G1	G1			B1	B1	B1	B1	B1	B1			R2	R2	R2	R2	R2	R2			G2	G2	G2	G2	G2	G2		
		2	B2	B2	B2	B2	B2	B2			R3	R3	R3	R3	R3	R3			G3	G3	G3	G3	G3	G3			B3	B3	B3	B3	B3	B3		
H'13	24	—	A0	A0	A0	A0	A0	A0	A0	A0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
H'14		—	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	A0	A0	A0	A0	A0	A0	A0	A0
H'15		0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
		1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
		2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
H'16	18	—							R0	R0	R0	R0	R0	R0	G0	G0	G0									G0	G0	G0	B0	B0	B0	B0	B0	B0
H'17		—															R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'18	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
		1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
		2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
H'19	12	—	A0	A0	A0	A0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	A1	A1	A1	A1	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'1A		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	A0	A0	A0	A0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	A1	A1	A1	A1
H'1B	15	—	A0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A1	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'1C		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	A1
H'1D	12	—	A0	A0	A0	A0	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	A1	A1	A1	A1	B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1
H'1E		—	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	A0	A0	A0	A0	B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	A1	A1	A1	A1
H'1F	15	—	A0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	A1	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1
H'20		—	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	A0	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	A1
H'21	18	0			B0	B0	B0	B0	B0	B0			G0	G0	G0	G0	G0	G0			R0	R0	R0	R0	R0	R0			B1	B1	B1	B1	B1	B1
		1			G1	G1	G1	G1	G1	G1			R1	R1	R1	R1	R1	R1			B2	B2	B2	B2	B2	B2			G2	G2	G2	G2	G2	G2
		2			R2	R2	R2	R2	R2	R2			B3	B3	B3	B3	B3	B3			G3	G3	G3	G3	G3	G3			R3	R3	R3	R3	R3	R3
H'22	24	—	A0	A0	A0	A0	A0	A0	A0	A0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0
H'23	16	—																	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0
H'24~H'3E	—	—	Reserved								Reserved								Reserved								Reserved							
H'3F	—	—	RGB_CLUT_DATA0								RGB_CLUT_DATA1								RGB_CLUT_DATA2								RGB_CLUT_DATA3							

When the RDFMT[6:0] bits are set to H'3F, it is necessary to set up the CLUT in the RGB color space.

Table 25.18 Packed YCbCr Formats for RPF Input

RDFMT [6:0]	Packed YCbCr Input Format	Reference
H'40	YCbCr4:4:4 semi-planar	Figure 25.19
H'41	YCbCr4:2:2 semi-planar (NV16, NV61*1)	
H'42	YCbCr4:2:0 semi-planar (NV12, NV21*1)	
H'43 to H'45	Reserved	—
H'46	YCbCr4:4:4 interleaved	Figure 25.20
H'47	YCbCr4:2:2 interleaved type 0 (UYVY, YUY2*2, YVYU*3)	
H'48	YCbCr4:2:2 interleaved type 1	
H'49	YCbCr4:2:0 interleaved	
H'4A	YCbCr4:4:4 planar	Figure 25.21
H'4B	YCbCr4:2:2 planar (YV16)	
H'4C	YCbCr4:2:0 planar (YV12, YU12)	
H'4D to H'7E	Reserved	—
H'7F	YCBCR_CLUT_DATA*4 *5	—

Notes: 1. When the input format is NV61 or NV21, set the SPUVS bit to 1.
2. When the input format is YUY2, set the SPYCS bit to 1.
3. When the input format is YVYU, set the SPUVS bit to 1 and SPYCS bit to 1.
4. When the RDFMT[6:0] bits are set to H'7F, it is necessary to set up the CLUT in the YCbCr color space.
5. The Monochrome format can be implemented through the CLUT.

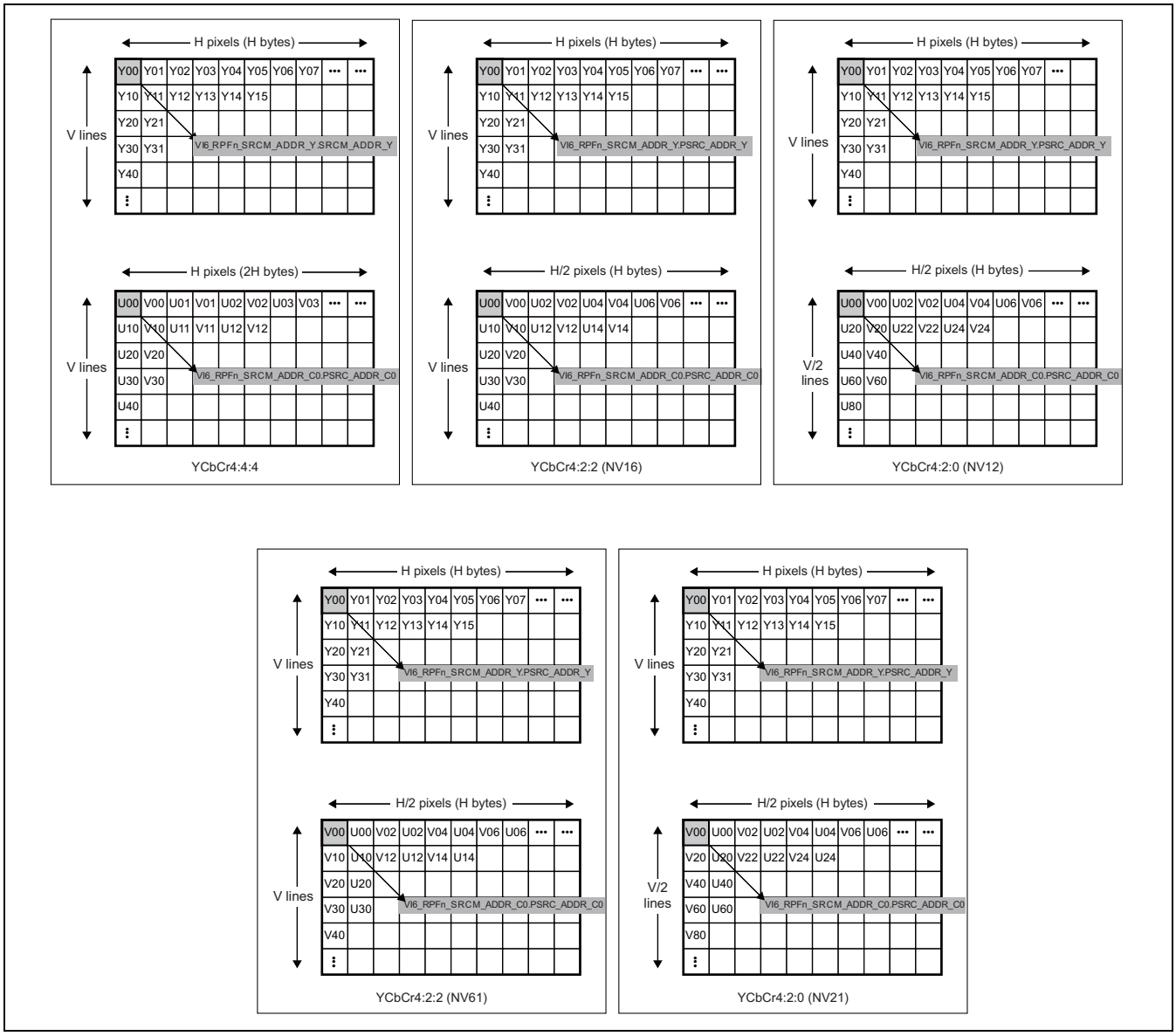


Figure 25.19 YCbCr Semi-Planar Formats

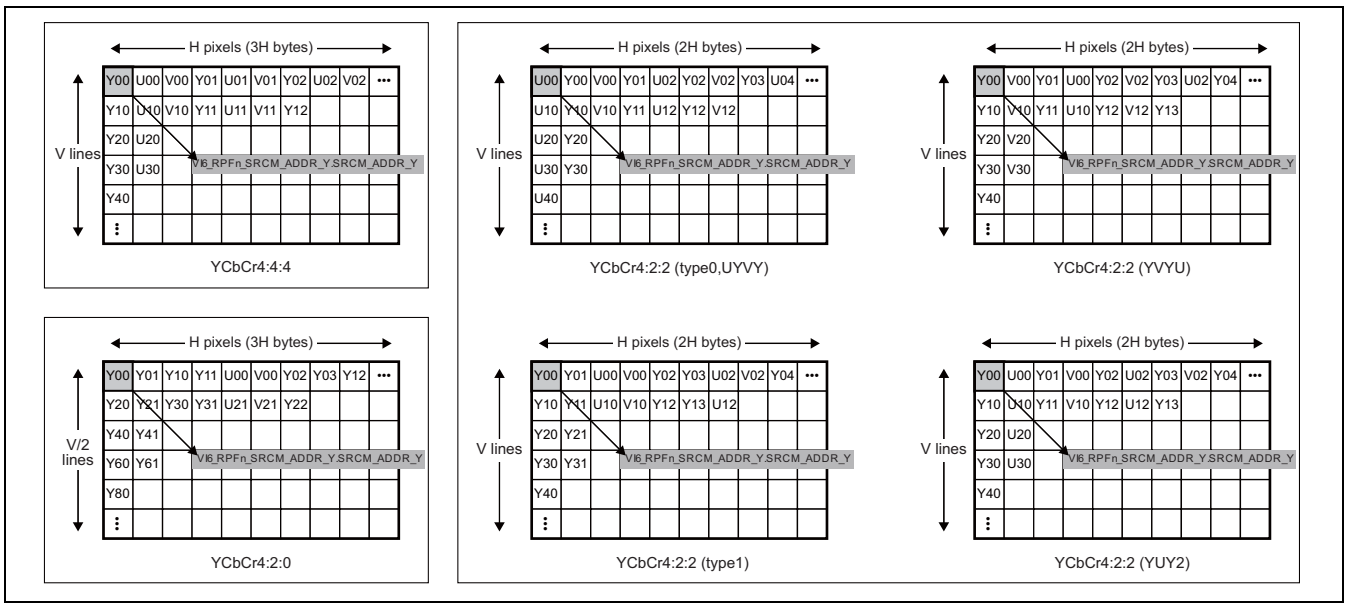


Figure 25.20 YCbCr Interleaved Formats

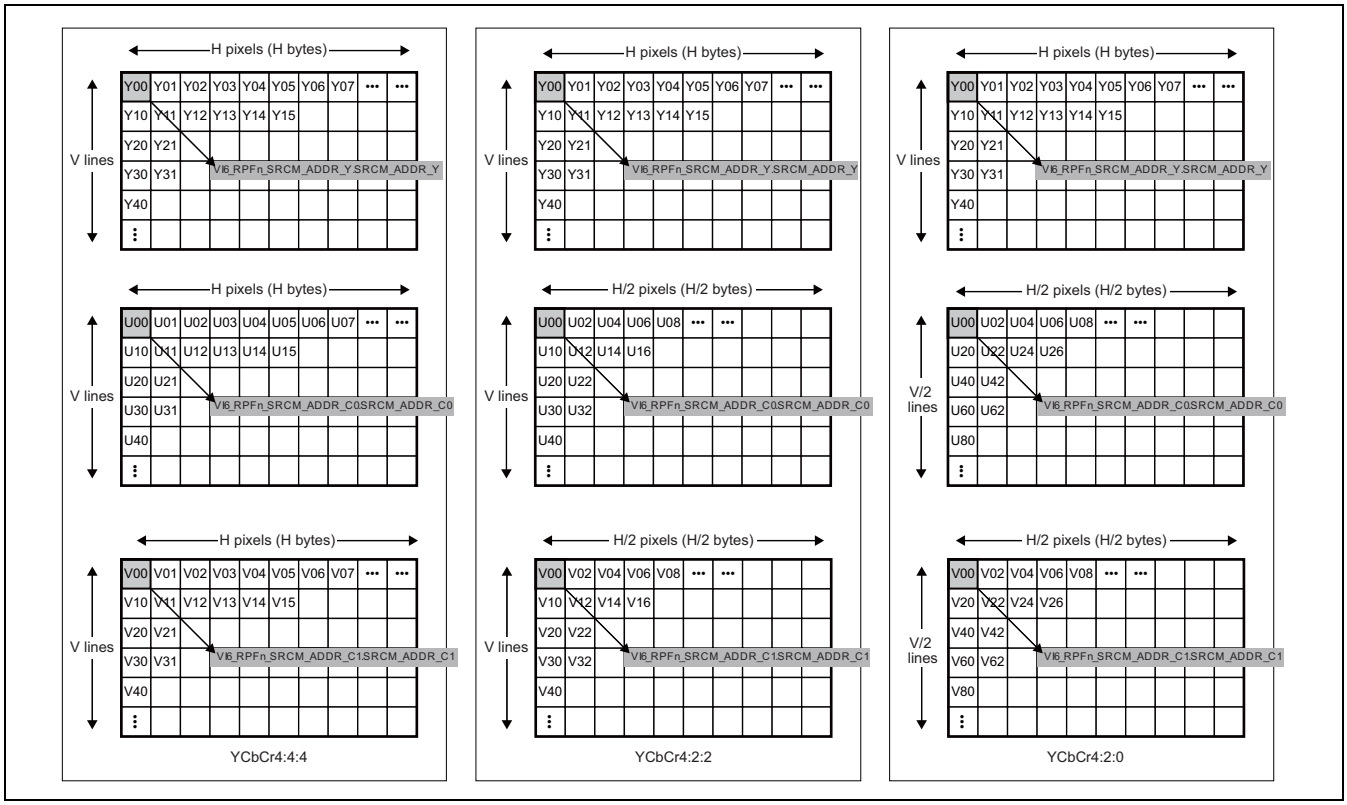


Figure 25.21 YCbCr Planar Formats

[CLUT Setting]

To set up the CLUT, store the values to replace each of R (Cr), G (Y), and B (Cb) components in the CLUT allocated as shown in Table 25.19. The CLUT space has 256 32-bit entries, which should be accessed in 32 bits in the same way as for register access. The address for each entry is obtained from the start address of each space (Table 25.19) + entry number × 4. For example, the CLUT address of entry 7 for RPF2 is $VSP_BASE + H'481C.

Figure 25.22 shows the CLUT format.

Table 25.19 CLUT Space for Each RPF

RPF	Address Area for CLUT Space
RPF0	$VSP_BASE + H'4000 to $VSP_BASE + H'43FF
RPF1	$VSP_BASE + H'4400 to $VSP_BASE + H'47FF
RPF2	$VSP_BASE + H'4800 to $VSP_BASE + H'4BFF
RPF3	$VSP_BASE + H'4C00 to $VSP_BASE + H'4FFF
RPF4	$VSP_BASE + H'5000 to $VSP_BASE + H'53FF

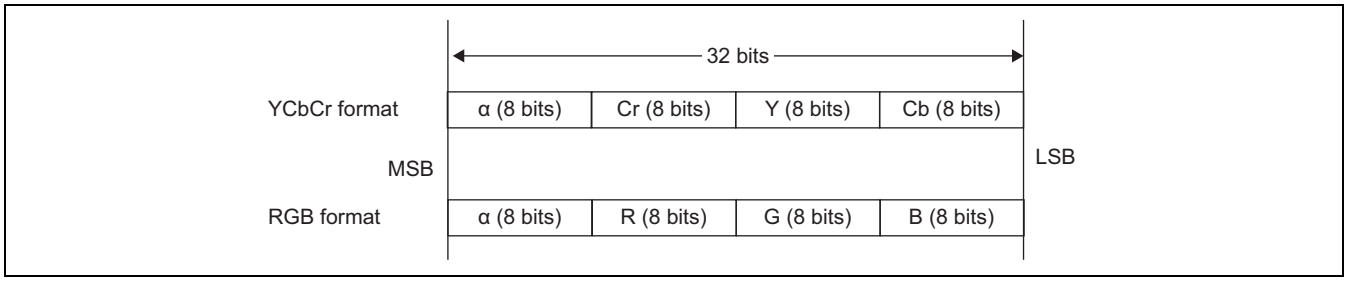


Figure 25.22 CLUT Format

According to the specified 256-entry replacement table (CLUT), input data is replaced as shown in Figure 25.23. Input data is eight bits but output data is 32 bits including α and RGB or YCbCr components.

When writing to an entry in the CLUT, the host CPU writes all components at the same time. Therefore, specify replacement data for all components in the CLUT at the same time as shown in Figure 25.22.

Note that write access to the CLUT space is prohibited while the RPF is operating.

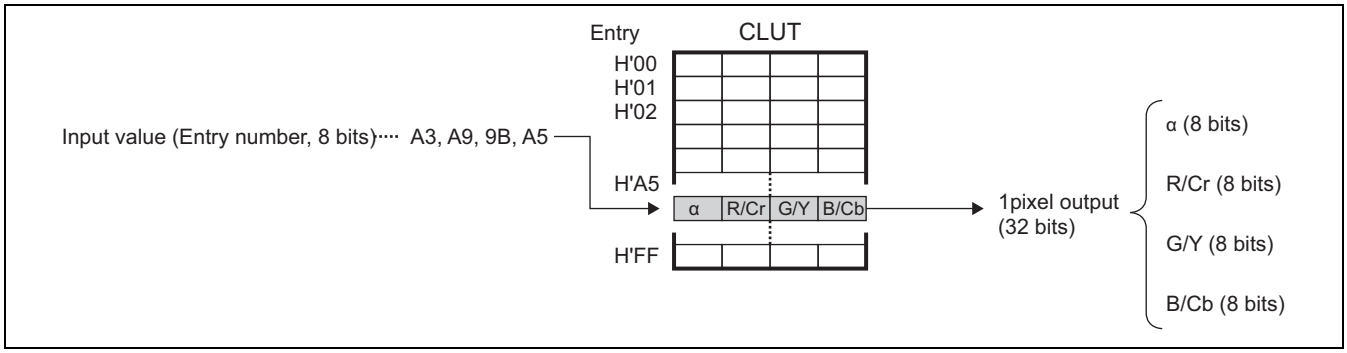


Figure 25.23 Replacement of Input Data with Pixel Values Specified in CLUT

25.2.7.4 RPFn Data Swapping Registers (VI6_RPFn_DSWAP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	A_LLS	A_LWS	A_WDS	A_BTS	—	—	—	—	P_LLS	P_LWS	P_WDS	P_BTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	A_LLS	0	R/W	α Plane Data Swapping in LONG LWORD Units 0: Data swapping in LONG LWORD (64-bit) units is disabled 1: Data swapping in LONG LWORD (64-bit) units is enabled This should be set to 1 in most cases, but when data has been swapped in 64-bit units by another data processing channel, specify 0
10	A_LWS	0	R/W	α Plane Data Swapping in Longword Units 0: Data swapping in long word (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled This should be set to1 in most cases, but when data has been swapped in 32-bit units by another data processing channel, specify 0
9	A_WDS	0	R/W	α Plane Data Swapping in Word Units 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
8	A_BTS	0	R/W	α Plane Data Swapping in Byte Units 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	P_LLS	0	R/W	Picture Plane Data Swapping in LONG LWORD Units 0: Data swapping in LONG LWORD (64-bit) units is disabled 1: Data swapping in LONG LWORD (64-bit) units is enabled This should be set to1 in most cases, but when data has been swapped in 64-bit units by another data processing channel, specify 0
2	P_LWS	0	R/W	Picture Plane Data Swapping in Longword Units 0: Data swapping in longword (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled This should be set to 1in most cases, but when data has been swapped in 32-bit units by another data processing channel, specify 0
1	P_WDS	0	R/W	Picture Plane Data Swapping in Word Units 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled

Bit	Bit Name	Initial Value	R/W	Description
0	P_BTS	0	R/W	Picture Plane Data Swapping in Byte Units 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled

When the virtual input function of the RPFn is used (VI6_RPFn_INFMT.VIR = 1), this register setting is ignored. Swapping of RPF input data can be specified separately for the α plane and picture plane. Table 25.20 shows the data order before and after swapping according to the LONG LWORD, longword, word, and byte swapping settings.

Table 25.20 Data Order after Swapping according to Swapping Register Settings

VI6_PRFn_DSWAP					Changed Order of Data (Each value indicates one byte)															
*_LLS	*_LWS	*_WDS	*_BTS	Input →	0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	0		0	1	2	3	4	5	6	7	8	9	10	11	12	13	14	15
0	0	0	1		1	0	3	2	5	4	7	6	9	8	11	10	13	12	15	14
0	0	1	0		2	3	0	1	6	7	4	5	10	11	8	9	14	15	12	13
0	0	1	1		3	2	1	0	7	6	5	4	11	10	9	8	15	14	13	12
0	1	0	0		4	5	6	7	0	1	2	3	12	13	14	15	8	9	10	11
0	1	0	1		5	4	7	6	1	0	3	2	13	12	15	14	9	8	11	10
0	1	1	0		6	7	4	5	2	3	0	1	14	15	12	13	10	11	8	9
0	1	1	1		7	6	5	4	3	2	1	0	15	14	13	12	11	10	9	8
1	0	0	0	Output→	8	9	10	11	12	13	14	15	0	1	2	3	4	5	6	7
1	0	0	1		9	8	11	10	13	12	15	14	1	0	3	2	5	4	7	6
1	0	1	0		10	11	8	9	14	15	12	13	2	3	0	1	6	7	4	5
1	0	1	1		11	10	9	8	15	14	13	12	3	2	1	0	7	6	5	4
1	1	0	0		12	13	14	15	8	9	10	11	4	5	6	7	0	1	2	3
1	1	0	1		13	12	15	14	9	8	11	10	5	4	7	6	1	0	3	2
1	1	1	0		14	15	12	13	10	11	8	9	6	7	4	5	2	3	0	1
1	1	1	1		15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0

25.2.7.5 RPFn Display Location Registers (VI6_RPFn_LOC)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	HCOORD[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VCOORD[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	HCOORD [12:0]	All 0	R/W	Horizontal Coordinate of Sub layer Display Location on Master Layer These bits specify the left-end location of the sub layer displayed by the RPFn and the subsequent module connected through the DPR. Specify the horizontal coordinate of the location in pixel units with the left-end pixel of the master layer set at coordinate 0. When the RPFn is the master layer, set these bits to 0. If the sub layer extends beyond the master layer according to the HCOORD setting, the extended section is cut off at the right end of the master layer. Even in this case, however, a bus transfer that is unnecessary for output image generation is executed since the whole sub layer data is read from the external memory. Appropriate coordinate setting is recommended so that the sub layer does not extend beyond the right end of the master layer. If the HCOORD value is larger than the horizontal size of the master layer image, the entire sub layer goes outside of the master layer. Such setting is prohibited. A value from 0 to 8,189 can be specified.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	VCOORD [12:0]	All 0	R/W	Vertical Coordinate of Sub layer Display Location on Master Layer These bits specify the top-end location of the sub layer displayed by the RPFn and the subsequent module connected through the DPR. Specify the vertical coordinate of the location in pixel units with the top-end pixel of the master layer set at coordinate 0. When the RPFn is the master layer, set these bits to 0. If the sub layer extends beyond the master layer according to the VCOORD setting, the extended section is cut off at the bottom end of the master layer. Even in this case, however, a bus transfer that is unnecessary for output image generation is executed since the whole sub layer data is read from the external memory. Appropriate coordinate setting is recommended so that the sub layer does not extend beyond the bottom end of the master layer. If the VCOORD value is larger than the vertical size of the master layer image, the entire sub layer goes outside of the master layer. Such setting is prohibited. A value from 0 to 8,189 can be specified.

Figure 25.24 shows an example of RPF1 and RPF2 offsets with respect to master layer RPF0. Although this figure only shows sub layers RPF1 and RPF2, specify offsets for all RPFs other than the master layer in the same way as shown in this example.

Whether an RPFn is the master layer or a sub layer is determined through the selection of the source RPF for WPFn (the VI6_WPFn_SRCRPF setting). For details, refer to section 25.2.8.1.

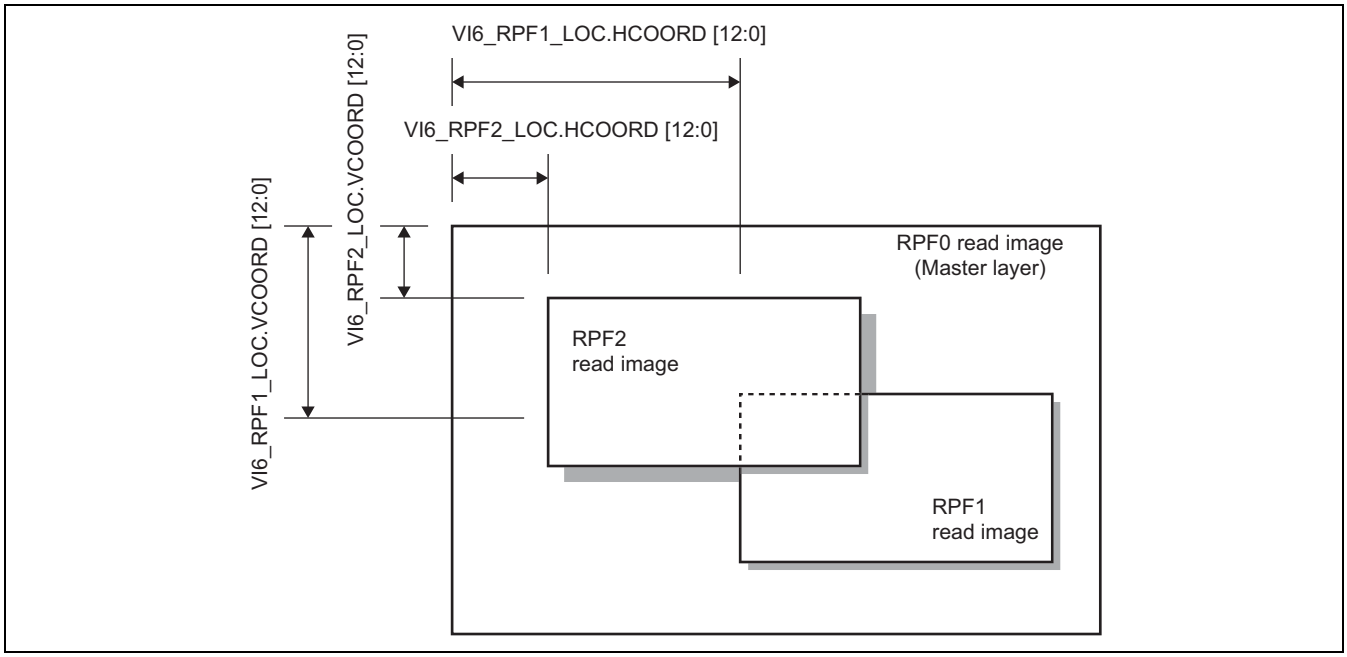
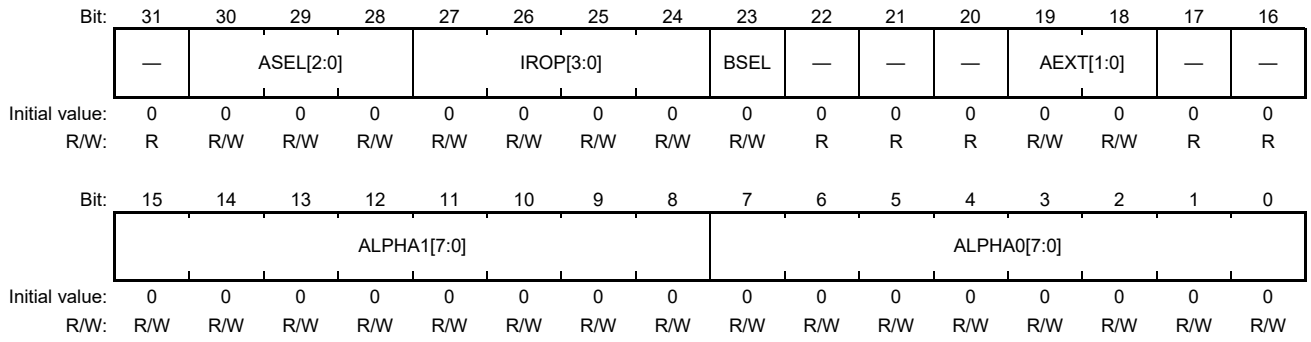


Figure 25.24 RPF1 and RPF2 Offsets from Master Layer

25.2.7.6 RPFn α Plane Selection Control Registers (VI6_RPFn_ALPH_SEL)



Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	ASEL[2:0]	000	R/W	α Format and Processing Method Select These bits select how to handle the α value to be used. The RPF handles two types of α value; 8-bit and 1-bit values. When a 1-bit α value is used, VSP1 assumes that the 1-bpp α value for each pixel is stored in the order from MSB to LSB in each byte (big endian). The α value is used as either transparency information or mask information. Transparency information is included in the α plane read from external memory when the ASEL bits are set to 1 or 3 and in the α value stored in the packed RGB bit field when these bits are set to 0 or 2. The α value as transparency information is sent as the destination value to the IROP as shown in Figure 25.25 and then output to the subsequent modules. The output α value is used, for example, for blending in the BRU. The α value as mask information is used for IROP operation in the RPF. The mask information is included in the α plane read from external RAM when the ASEL bits are set to 0 or 2 and the source value is used in IROP operation (IROP setting other than 0, 5, 10, or 15). This α value is sent as the source value to the IROP as shown in Figure 25.25. Note that the α value selected through the ASEL bits has a lower priority than the VI6_RPFn_CKEY_SET*.AP* value replaced through the color keying function. When the color keying function is used, the α value may be replaced with the VI6_RPFn_CKEY_SET*.AP* value regardless of the ASEL bit setting. When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), specify 4.

Bit	Bit Name	Initial Value	R/W	Description
30 to 28	ASEL[2:0]	000	R/W	000: 1, 4, or 8-bit packed α + plane α (IROP ! = 0, 5, 10, 15) The α bit field in 1, 4, or 8-bit packed α is handled as transparency information. Be sure to specify the packed format that includes α through VI6_RPFn_INFMT.RDFMT. When VI6_RPFn_MSKCTRL.MSK_EN is 0 and the IROP bit value is not 0, 5, 10, or 15, the α plane should be read as mask information. Specify the number of α data bits (BSEL) stored in the α plane and the α plane read start address (VI6_RPFn_SRCM_ADDR_AI). When the IROP bits are set to 0, 5, 10, or 15, the α plane is not read. 001: 8-bit plane α The 8-bit α plane is read from external RAM as transparency information. When the packed RGB format has a bit field for α, the information in the α bit field is discarded. The α plane read start address (VI6_RPFn_SRCM_ADDR_AI) should be specified. The α value goes through the 8-bit transparent α generator shown in Figure 25.25 without change. When VI6_RPFn_MSKCTRL.MSK_EN is 0, IROP operation cannot be executed; set the IROP bits to 0 in this case. When VI6_RPFn_MSKCTRL.MSK_EN is 1. IROP operation can be executed. 010: 1-bit packed α + plane α (IROP ! = 0, 5, 10, 15) The 1-bit packed α input is converted by the 8-bit transparent α generator shown in Figure 25.25 according to the ALPHA0/1 setting into the 8-bit α value as transparency information. Select the packed input format that includes a 1-bit α field. When VI6_RPFn_MSKCTRL.MSK_EN is 0 and the IROP value is not 0, 5, 10, or 15, the α plane should be read as mask information. Specify the number of α data bits (BSEL) stored in the α plane and the α plane read start address (VI6_RPFn_SRCM_ADDR_AI). When the IROP bits are set to 0, 5, 10, or 15, the α plane is not read. 011: 1-bit plane α The 1-bit α plane is read from external RAM and converted by the 8-bit transparent α generator shown in Figure 25.25 according to the ALPHA0/1 setting into the 8-bit α value as transparency information. When the packed RGB format has a bit field for α, the information in the α bit field is discarded. The α plane read start address (VI6_RPFn_SRCM_ADDR_AI) should be specified. When VI6_RPFn_MSKCTRL.MSK_EN is 0, IROP operation cannot be executed; set the IROP bits to 0 in this case. When VI6_RPFn_MSKCTRL.MSK_EN is 1. IROP operation can be executed. 100: Fixed α The fixed α value (VI6_RPFn_VRTCOL_SET.LAYA value) is output from the RPF. IROP operation cannot be executed; set the IROP bits to 0 in this case. 101 to 111: Setting prohibited.

Bit	Bit Name	Initial Value	R/W	Description
27 to 24	IROP[3:0]	0000	R/W	IROP Operation Setting These bits specify the operator to be executed in the IROP operation unit shown in Figure 25.25. The source (S) for the IROP operation is the pixel data and α data specified in the VI6_RPFn_MSKSET0 or VI6_RPFn_MSKSET1 IROP input value register, which is selected according to the value (0 or 1) generated by the 1-bit mask generator. The destination (D) is the image data (RGB/YCbCr) and 8-bit α data output from the unpack/OSD processor. IROP operation is applied both for the image data and α data between the source and destination data. If these bits are set to the operation that involves the source (S) (IROP setting other than 0, 5, 10, or 15) while VI6_RPFn_MSKCTRL.MSK_EN is 0, the α plane is read from the external RAM to be used for the α value for IROP operation; specify the α plane read start address (VI6_RPFn_SRCM_ADDR_A). When the virtual input function is used (VI6_RPFn_INFMT.VIR = 1), IROP operation is not available; set these bits to B'0000. 0000: NOP(D) 0001: AND(S & D) 0010: AND_REVERSE(S & ~D) 0011: COPY(S) 0100: AND_INVERTED(~S & D) 0101: CLEAR(0) 0110: XOR(S ^ D) 0111: OR(S | D) 1000: NOR(~(S | D)) 1001: EQUIV(~(S ^ D)) 1010: INVERT(~D) 1011: OR_REVERSE(S | ~D) 1100: COPY_INVERTED(~S) 1101: OR_INVERTED(~S | D) 1110: NAND(~(S & D)) 1111: SET(all 1)
23	BSEL	0	R/W	α Bit Count Conversion Selection for 1-Bit Mask Generator Specifies the number of bits in the α plane to be read as mask information from the external RAM. The α value in mask information is used for the source (S) in IROP. When α plane data is eight bits, it is converted to one bit through the 1-bit mask generator shown in Figure 25.25. Note that this bit setting is valid when the ASEL bits are set to 0 or 2 and VI6_RPFn_MSKCTRL.MSK_EN is set to 0. In other cases, this bit setting has no effect. 0: 8-bit α is converted to 1-bit α through the 1-bit mask generator. When the 8-bit α value input to the RPF is not 0, it is converted to 1; when the value is 0, it is converted to 0. 1: α value goes through the 1-bit mask generator. The 1-bit α value input to the RPF is output through the 1-bit mask generator without change.
22 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
19, 18	AEXT[1:0]	00	R/W	Lower-Bit α Value Extension Method Set These bits specify the method for extending the input α data to eight bits through the unpack processing. 00: The lower-order bits of α value are extended with 0. 01: The upper-order bits of α value are copied to the lower-order bits. 10: The lower-order bits of α value are extended with 0. The maximum value is limited to H'FF. 11: Setting prohibited
17, 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	ALPHA1 [7:0]	H'00	R/W	8-Bit α Value Output when 1-Bit α Value is 1 These bits specify the 8-bit α value to be output when 1-bit α data is input and the α value input to the 8-bit transparent α generator shown in Figure 25.25 is 1. This setting is valid when the ASEL bits are set to B'010 or B'011. A value from 0 to 255 can be specified.
7 to 0	ALPHA0 [7:0]	H'00	R/W	8-Bit α Value Output when 1-Bit α Value is 0 These bits specify the 8-bit α value to be output when 1-bit α data is input and the α value input to the 8-bit transparent α generator shown in Figure 25.25 is 0. This setting is valid when the ASEL bits are set to B'010 or B'011. A value from 0 to 255 can be specified.

Figure 25.25 shows the relationship between the α selector, IROP operation unit, color keying unit, and related registers (color space conversion is omitted but is behind the color keying unit as shown in Figure 25.3). The IROP operation unit receives two inputs, source and destination. The image data input from the external memory is processed through the unpack processor and 8-bit transparent α generator and then input to the IROP operation unit as destination data. The α plane data input from the external memory is sent to the 8-bit transparent α generator when the ASEL bits are set to 1 or 3, or sent to the 1-bit mask α generator when the ASEL bits are set to 0 or 2. For the pixel data and 8-bit α value on the source side of the IROP operation unit, either the VI6_RPFn_MSKSET0 value or VI6_RPFn_MSKSET1 values will be selected according to the 1-bit α value output by the 1-bit mask α generator.

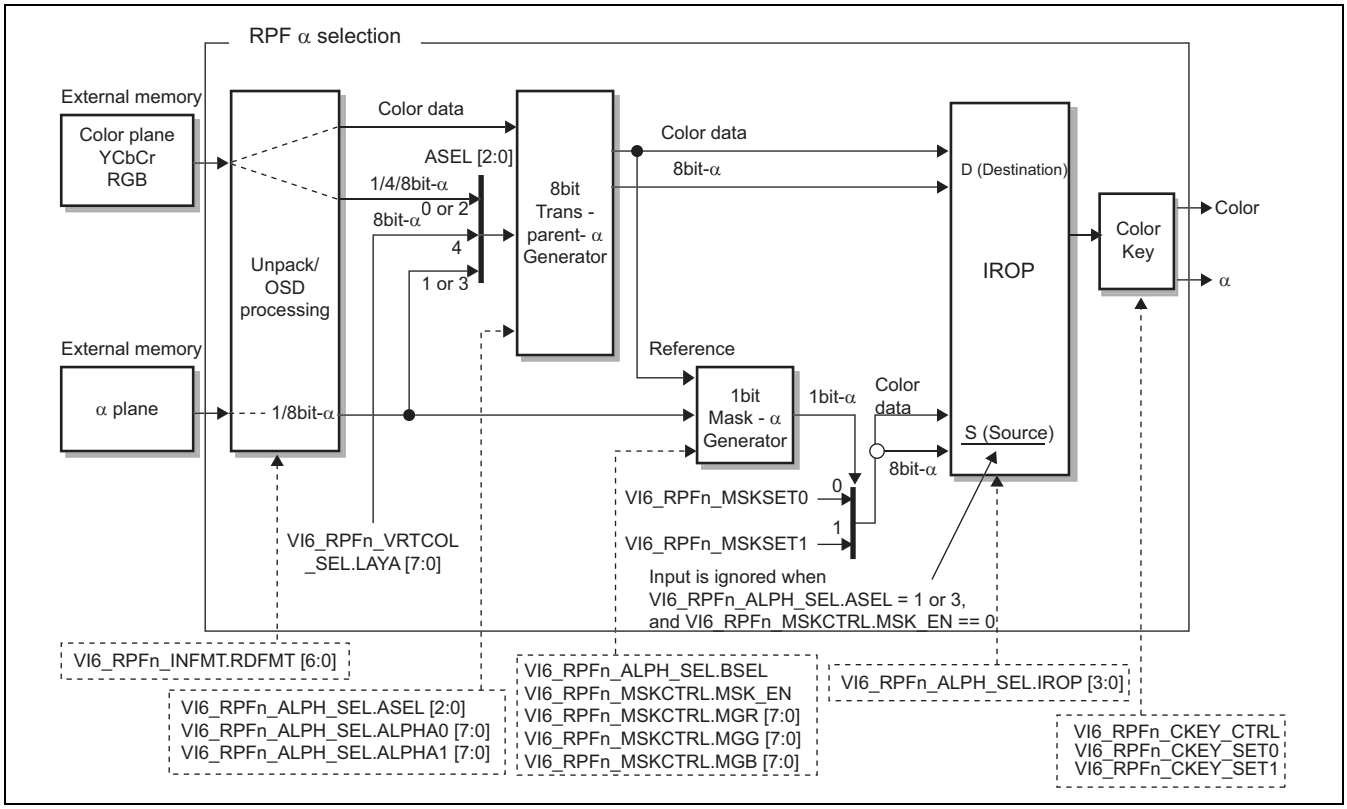


Figure 25.25 Configuration of α Selector and IROP Operation Unit in RPF

The following describes the function of each block shown in Figure 25.25. Read the following while referring to the figure as necessary.

Unpack/OSD processor:

Unpacks each component and α value of the image data according to the packed format specified in VI6_RPFn_INFMT.RDFMT.

8-bit transparent α generator:

Converts the input α value into 8-bit α when the input α is four bits or one bit.

When VI6_RPFn_ALPH_SEL.ASEL are set to 0 (8-, 4-, or 1-bit packed α), this generator outputs the input α value without change if the α bit field in the packed α data is eight bits; if the α bit field is less than eight bits, it is converted to an 8-bit α value by extending the LSB side according to the VI6_RPFn_ALPH_SEL.AEXT setting.

When VI6_RPFn_ALPH_SEL.ASEL are set to 1 (8-bit plane α) or 4 (fixed α), this generator outputs the input 8-bit plane α without change. If a packed α value is included in RGB data, it is discarded.

When VI6_RPFn_ALPH_SEL.ASEL are set to 2 (1-bit packed α) or 3 (8-bit α generated from 1-bit plane α), an 8-bit α value is generated by using the VI6_RPFn_ALPH_SEL.ALPHA0[7:0] value when the input 1-bit α value is 0 or by using the VI6_RPFn_ALPH_SEL.ALPHA1[7:0] value when the input 1-bit α value is 1. When VI6_RPFn_ALPH_SEL.ASEL is set to 3, a packed α value that is included in RGB data is discarded.

1-bit mask α generator:

Generates 1-bit α data from the input 8-bit α data or pixel data. When the input α data is one bit, this generator outputs it without change.

When VI6_RPFn_ALPH_SEL.ASEL are set to 0 (8-, 4-, or 1-bit packed α) or 2 (plane α) and VI6_RPFn_MSKCTRL.MSK_EN is set to 0, the α plane read from the external memory to be used in IROP is converted to 1-bit α data when necessary. When the α plane data read from the external RAM is eight bits (BSEL = 0), if the value is 0, a 1-bit α value of 0 is generated; if the value is not 0, a 1-bit α value of 1 is generated. When the α plane data is one bit (BSEL = 1), this generator outputs it without change.

When the value of the 1-bit α generated by the 1-bit mask α generator is 0, the 8-bit α and pixel data specified in VI6_RPFn_MSKSET0 are output as the source. When the generated 1-bit α value is 1, the 8-bit α and pixel data specified in VI6_RPFn_MSKSET1 are output as the source.

As shown in Figure 25.25, when VI6_RPFn_ALPH_SEL.ASEL are set to 1 (8-bit plane α) or 3 (1-bit plane α), the α plane read from the external RAM is sent to the 8-bit transparent α generator as transparency information. When VI6_RPFn_MSKCTRL.MSK_EN is set to 0, the 1-bit α for masking is generated according to the input α plane (refer to section 25.2.7.8), but the 1-bit mask α generator does not refer to the input α plane because it is input to the 8-bit transparent α generator as transparency information. Accordingly, the 1-bit mask α generator does not generate a 1-bit α for masking and the data on the source side becomes invalid; that is, IROP operation cannot be executed. Set the IROP bits to 0 in this case. In contrast, when VI6_RPFn_MSKCTRL.MSK_EN is set to 1, the 1-bit mask α generator creates α data for masking according to the pixel data instead of the input α plane data, and IROP operation can be executed in this case.

IROP operation unit

Executes ROP operation according to the opcode specified in VI6_RPFn_ALPH_SEL.IROP. For ROP operation (other than NOP), valid values should be input both for the source and destination. As described in the above (description of the 1-bit mask α generator), when VI6_RPFn_ALPH_SEL.ASEL are set to 1 or 3 and VI6_RPFn_MSKCTRL.MSK_EN is set to 0, the source data for the IROP operation unit is treated as invalid; set VI6_RPFn_ALPH_SEL.IROP to 0 (NOP). When VI6_RPFn_ALPH_SEL.ASEL are set to 4, a fixed α value is output from the RFP and IROP operation is not available. In the same way as the above case, set VI6_RPFn_ALPH_SEL.IROP to 0 (NOP).

To specify a valid source value for the IROP operation unit and execute IROP operation (specify an opcode other than NOP in the IROP bits), specify register values as shown in Table 25.21. Where the source input state is indicated as "Valid" in the table, IROP operation can be executed. In the cases where IROP operation is not available, set the IROP bits to 0 (NOP).

Table 25.21 Source Input State in IROP Operation Unit

VI6_RPFn_ALPH_SEL.ASEL [2:0]		VI6_RPFn_MSKCTRL.MSK_EN = 0 (Source data is generated according to input α plane)		VI6_RPFn_MSKCTRL.MSK_EN = 1 (Source data is generated according to the destination-side pixel data)
B'000	(1-, 4-, or 8-bit packed α + plane α)	Valid	(α plane input)	Valid
B'001	(8-bit α plane)	Invalid	(IROP operation is not available; α plane is output to the subsequent modules behind RPF)	Valid
B'010	(8-bit α generated from 1-bit packed α + plane α)	Valid	(α plane input)	Valid
B'011	(8-bit α generated from 1-bit plane α)	Invalid	(IROP operation is not available; α plane is output to the subsequent modules behind RPF)	Valid
B'100	(Fixed α)	Invalid (IROP operation is not available; fixed α is output to the subsequent modules behind RPF)		

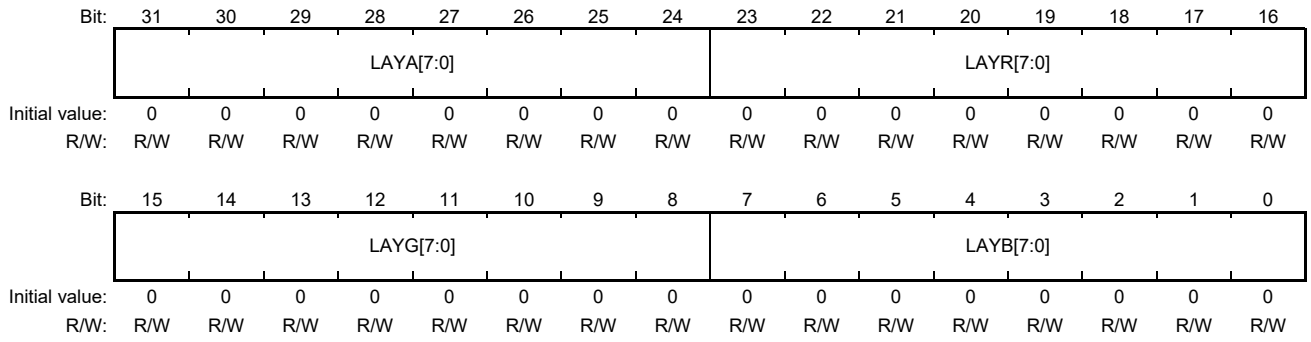
For the handling of the α values shown in Figure 25.25 and Table 25.21, the relationship between the RPF input format and RPF output α value is shown in Table 25.22. Where only bit names are shown in the table, the bits are in VI6_RPFn_ALPH_SEL described in this section.

Table 25.22 α Value Selected and Output according to ASEL Bits in Each Input Format

ASEL Setting		α Value Output for Each Input Format		
		RGB	YCbCr	OSD-CLUT
B'000	(8-, 4-, or 1-bit packed α is input)	1- ,4-, or 8-bit pixel α	H'FF*	α value in CLUT
B'001	(8-bit plane α is input)	8-bit α plane	8-bit α plane	8-bit α plane
B'010	(8-bit α is generated from the 1-bit packed α input)	ALPHA0 or ALPHA1 setting	H'FF*	H'FF
B'011	(8-bit α is generated from the 1-bit plane α input)	ALPHA0 or ALPHA1 setting	ALPHA0 or ALPHA1 setting	ALPHA0 or ALPHA1 setting
B'100	(Fixed α is output)	VI6_RPFn_VRTCOL_SET.LAYA setting		

Note: * Fixed value H'FF is output because packed α is not included in YCbCr.

25.2.7.7 RPFn Virtual Plane Color Information Registers (VI6_RPFn_VRTCOL_SET)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	LAYA[7:0]	H'00	R/W	Virtual-Input Fixed α Value These bits specify the fixed α value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When the virtual input function is disabled (VI6_RPFn_INFMT.VIR = 0), these bits are used to specify the fixed α value to be output from the RPF while VI6_RPFn_ALPH_SEL.ASEL are set to 4. A value from 0 to 255 can be specified.
23 to 16	LAYR[7:0]	H'00	R/W	Virtual-Input Fixed R/Cr Component Value These bits specify the fixed R or Cr value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When VI6_RPFn_INFMT.RDFMT is set to 19, the value specified in these bits is used as the R value. When VI6_RPFn_INFMT.RDFMT is set to 64, the value specified in these bits is used as the Cr value. A value from 0 to 255 can be specified.
15 to 8	LAYG[7:0]	H'00	R/W	Virtual-Input Fixed G/Y Component Value These bits specify the fixed G or Y value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When VI6_RPFn_INFMT.RDFMT is set to 19, the value specified in these bits is used as the G value. When VI6_RPFn_INFMT.RDFMT is set to 64, the value specified in these bits is used as the Y value. A value from 0 to 255 can be specified.
7 to 0	LAYB[7:0]	H'00	R/W	Virtual-Input Fixed B/Cb Component Value These bits specify the fixed B or Cb value generated in the RPFn when the virtual input function is enabled through the VI6_RPFn_INFMT.VIR setting. When VI6_RPFn_INFMT.RDFMT is set to 19, the value specified in these bits is used as the B value. When VI6_RPFn_INFMT.RDFMT is set to 64, the value specified in these bits is used as the Cb value. A value from 0 to 255 can be specified.

25.2.7.8 RPFn Mask Control Registers (VI6_RPFn_MSKCTRL)

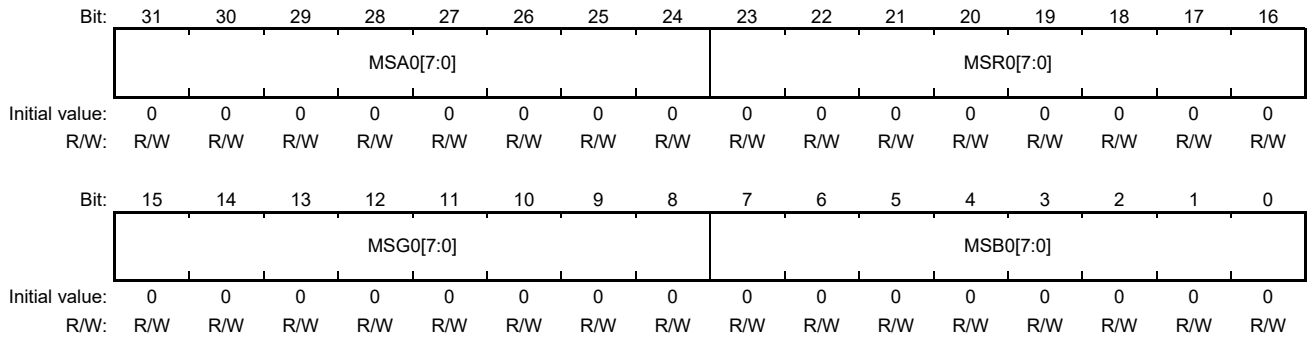
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	MSK_EN	MGR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MGG[7:0]								MGB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	MSK_EN	0	R/W	Mask Generation Specification Specifies the method of α value generation in the 1-bit mask α generator shown in Figure 25.25. 0: A 1-bit mask value is generated according to the input α plane value. When the input α is in the 1-bit format (VI6_RPFn_ALPH_SEL.BSEL = 1), the 1-bit mask value is output without change. When the input α is in the 8-bit format (VI6_RPFn_ALPH_SEL.BSEL = 0), the 1-bit mask value is 0 if the α value is H'00; otherwise, the 1-bit mask value is 1. 1: The R/Cr, G/Y, and B/Cb components of the image input to the destination side of the IROP operation unit are compared with the values specified in the MGR, MGG, and MGB bits, respectively. When all values match, 1 is output as the 1-bit mask value, and in other cases, 0 is output. When the generated 1-bit mask data is not used, set VI6_RPFn_ALPH_SEL.IROP to 0.
23 to 16	MGR[7:0]	H'00	R/W	R/Cr Comparison Value for 1-Bit α Generation These bits specify the R/Cr value to be compared for 1-bit α generation by using the pixel data on the destination side. When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify an R value for comparison. When YCbCr is specified, specify a Cr value for comparison. This setting is ignored when the MSK_EN bit is set 0. A value from 0 to 255 can be specified.
15 to 8	MGG[7:0]	H'00	R/W	G/Y Comparison Value for 1-Bit α Generation These bits specify the G/Y value to be compared for 1-bit α generation by using the pixel data on the destination side. When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a G value for comparison. When YCbCr is specified, specify a Y value for comparison. This setting is ignored when MSK_EN is set to 0. A value from 0 to 255 can be specified.

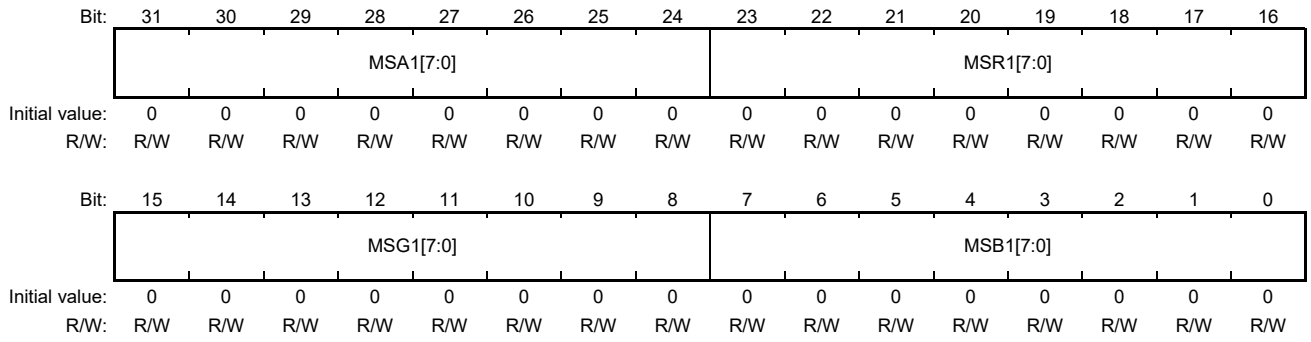
Bit	Bit Name	Initial Value	R/W	Description
7 to 0	MGB[7:0]	H'00	R/W	B/Cb Comparison Value for 1-Bit α Generation These bits specify the B/Cb value to be compared for 1-bit α generation by using the pixel data on the destination side. When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a B value for comparison. When YCbCr is specified, specify a Cb value for comparison. This setting is ignored when MSK_EN is set to 0. A value from 0 to 255 can be specified.

25.2.7.9 RPFn IROP-SRC Input Value Registers 0 (VI6_RPFn_MSKSET0)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MSA0[7:0]	H'00	R/W	IROP-Source Input α Value when 1-Bit α is 0 These bits specify the 8-bit α value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 0 (Figure 25.25). A value from 0 to 255 can be specified.
23 to 16	MSR0[7:0]	H'00	R/W	IROP-Source Input R/Cr Value when 1-Bit α is 0 These bits specify the R/Cr value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 0 (Figure 25.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify an R component value. When YCbCr is specified, specify a Cr component value. A value from 0 to 255 can be specified.
15 to 8	MSG0[7:0]	H'00	R/W	IROP-Source Input G/Y Value when 1-Bit α is 0 These bits specify the G/Y value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 0 (Figure 25.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a G component value. When YCbCr is specified, specify a Y component value. A value from 0 to 255 can be specified.
7 to 0	MSB0[7:0]	H'00	R/W	IROP-Source Input B/Cb Value when 1-Bit α is 0 These bits specify the B/Cb value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 0 (Figure 25.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a B component value. When YCbCr is specified, specify a Cb component value. A value from 0 to 255 can be specified.

25.2.7.10 RPFn IROP-SRC Input Value Registers 1 (VI6_RPFn_MSKSET1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	MSA1[7:0]	H'00	R/W	IROP-Source Input α Value when 1-Bit α is 1 These bits specify the 8-bit α value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 1. A value from 0 to 255 can be specified (Figure 25.25).
23 to 16	MSR1[7:0]	All 0	R/W	IROP-Source Input R/Cr Value when 1-Bit α is 1 These bits specify the R/Cr value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 1 (Figure 25.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify an R component value. When YCbCr is specified, specify a Cr component value. A value from 0 to 255 can be specified.
15 to 8	MSG1[7:0]	All 0	R/W	IROP-Source Input G/Y Value when 1-Bit α is 1 These bits specify the G/Y value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 1 (Figure 25.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a G component value. When YCbCr is specified, specify a Y component value. A value from 0 to 255 can be specified.
7 to 0	MSB1[7:0]	All 0	R/W	IROP-Source Input B/Cb Value when 1-Bit α is 1 These bits specify the B/Cb value to be input as the source to the IROP operation unit when the internal 1-bit α value generated through the 1-bit mask generator is 1 (Figure 25.25). When RGB is specified as the RPFn input format through VI6_RPFn_INFMT.RDFMT, specify a B component value. When YCbCr is specified, specify a Cb component value. A value from 0 to 255 can be specified.

25.2.7.11 RPFn Color Keying Control Registers (VI6_RPFn_CKEY_CTRL)

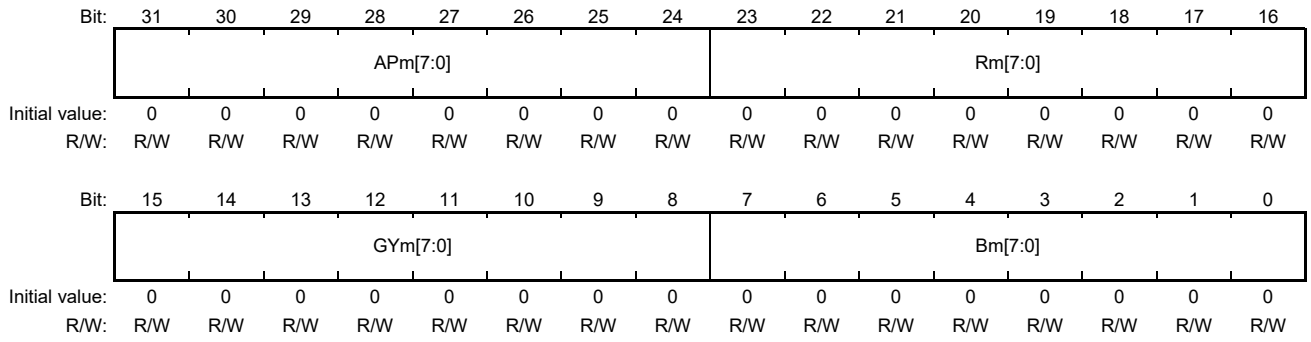
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CV	—	—	SAPE1	SAPE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CV	0	R/W	Color Replacement Control This bit controls the color replacement function in the color keying module shown in Figure 25.3. When an RGB format is specified as the color space of the RPFn input data through VI6_RPFn_INFMT.RDFMT, and if all components of an input pixel match the color components specified in VI6_RPFn_CKEY_SET0, the color replacement function replaces the values of the input α and all RGB components with the α and color components specified in VI6_RPFn_CKEY_SET1. When a YCbCr format is specified as the color space of the RPFn input data through VI6_RPFn_INFMT.RDFMT, only the Y data is compared; if the luminance component of an input pixel matches the value specified in VI6_RPFn_CKEY_SET0.GY0, the color replacement function replaces the values of the input α and all YCbCr components with the α and color components specified in VI6_RPFn_CKEY_SET1. When the CV bit is set to 1, the color replacement function is enabled. When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), set this bit to 0. 0: Color replacement function is disabled (transparent color mode). 1: Color replacement function is enabled.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	SAPE1	0	R/W	Comparison Color Data Setting 1 Enable/Disable This bit enables or disables comparison color data setting 1 in the transparent color-matched color mode for the color keying module. This bit setting is valid only when the CV bit is set to 0 and LTH bit is set to 0; it is ignored when the CV bit is set to 1 or LTH bit is set to 1. In transparent color-matched color mode, color information 1 (VI6_RPFn_CKEY_SET1.R1/GY1/B1) specified in VI6_RPFn_CKEY_SET1 is compared with the input component values. When the input data is in an RGB format, and if all input values match the specified color information, the input α value is replaced with the value specified in VI6_RPFn_CKEY_SET1.AP. When the input data is in YCbCr format, only the Y data is compared. When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), set this bit to 0. 0: Comparison color data setting 1 is disabled. 1: Comparison color data setting 1 is enabled.
0	SAPE0	0	R/W	Comparison Color Data Setting 0 Enable/Disable This bit enables or disables comparison color data setting 0 in the transparent color-matched color mode for the color keying module. This bit setting is valid only when the CV bit is set to 0 and LTH bit is set to 0; it is ignored when the CV bit is set to 1 or LTH bit is set to 1. In transparent color-matched color mode, color information 0 (VI6_RPFn_CKEY_SET0.R0/GY0/B0) specified in VI6_RPFn_CKEY_SET0 is compared with the input component values. When the input data is in an RGB format, and if all input values match the specified color information, the input α value is replaced with the value specified in VI6_RPFn_CKEY_SET0.AP. When the input data is in YCbCr format, only the Y data is compared. When using the virtual input function (VI6_RPFn_INFMT.VIR = 1), clear this bit to 0. 0: Comparison color data setting 0 is disabled. 1: Comparison color data setting 0 is enabled.

25.2.7.12 RPFn Color Keying Color Setting Registers-m (VI6_RPFn_CKEY_SETm: m = 0, 1)

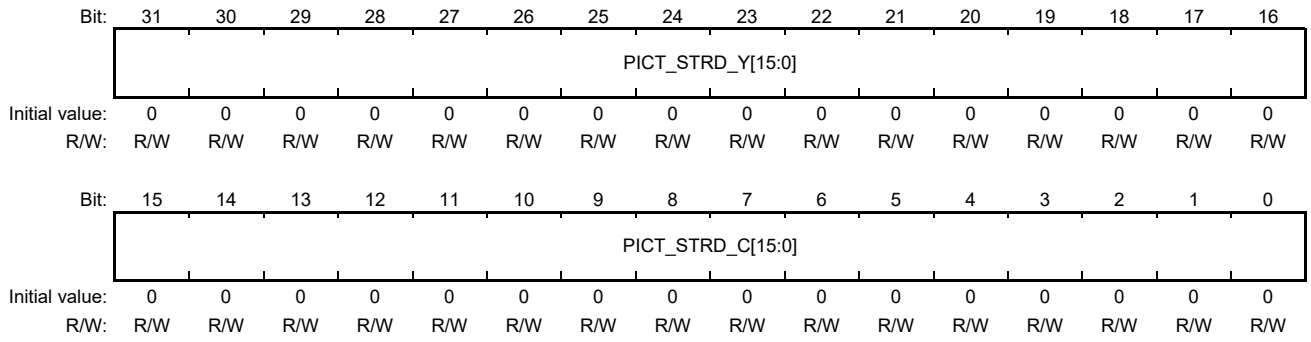


Bit	Bit Name	Initial Value	R/W	Description
31 to 24	APm[7:0]	H'00	R/W	α Data in Color Keying Color Information-m • In transparent color-matched color mode for color keying When the input data matches color setting-m (Rm, GYm, and Bm) for transparent color comparison in the color keying module, the input α value is replaced with the value specified in these bits. Specify the α value to replace the input value. • In transparent color-luma threshold mode for color keying When the input data is in YCbCr format, and if input Y value is equal to or smaller than GY0, the input α value is replaced with the value specified in this bit field (AP0). Specify the α value in this bit field (AP0) to replace the input value. AP1 is not used in this mode. Set AP1 to 0 value. • In color replacement mode for color keying These bits are not used in this mode. Clear them to 0. α value replacement through these bits in transparent color mode for color keying takes priority over the α value selected through the VI6_RPFn_ALPH_SEL.ASEL setting. A value from 0 to 255 can be specified.
23 to 16	Rm[7:0]	H'00	R/W	R*/Cr Component Data in Color Keying Color Information-m • In transparent color-matched color mode for color keying Specify the R component value for comparison enabled through the VI6_RPFn_CKEY_CTRL.SAPEm setting. When the RPFn input is in YCbCr format, the color keying module does not compare the Cr component, and the setting of these bits is ignored. • In transparent color-luma threshold mode for color keying The color keying module does not refer this bit field, and the setting of these bits is ignored. • In color replacement mode for color keying Specify the R component value to be compared with the input data in the color replacement function of the color keying module. A value from 0 to 255 can be specified.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	GYm[7:0]	H'00	R/W	G*/Y Component Data in Color Keying Color Information-m • In transparent color-matched color mode for color keying Specify the G/Y component value for comparison enabled through the VI6_RPFn_CKEY_CTRL.SAPEm setting. • In transparent color-luma threshold mode for color keying Specify the Y component value in the GY0 to be compared. • In color replacement mode for color keying Specify the G/Y component value to be compared with the input data in the color replacement function of the color keying module. A value from 0 to 255 can be specified.
7 to 0	Bm[7:0]	H'00	R/W	B*/Cb Component Data in Color Keying Color Information-m • In transparent color-matched color mode for color keying Specify the B component value for comparison enabled through the VI6_RPFn_CKEY_CTRL.SAPEm setting. When the RPFn input is in YCbCr format, the color keying module does not compare the Cb component, and the setting of these bits is ignored. • In transparent color-luma threshold mode for color keying The color keying module does not refer this bit field, and the setting of these bits is ignored. • In color replacement mode for color keying Specify the B component value to be compared with the input data in the color replacement function of the color keying module. A value from 0 to 255 can be specified.

Note: * When comparison data is specified in an RGB format, if a packed format is selected for RGB input and each of the RGB components is not eight bits, the lower-order bits of input data are extended as specified through VI6_RPFn_INFMT.CEXT before comparison. The RGB components to be compared with the input should also be extended in the same way and the extended values should be specified in this register.

25.2.7.13 RPFn Source Picture Memory Stride Setting Registers (VI6_RPFn_SRCM_PSTRIDE)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PICT_STRD_Y [15:0]	H'0000	R/W	Memory Stride of Source Picture Y/RGB Plane These bits specify in 1-byte units the memory stride of the source picture Y/RGB plane read by the RPFn. A value from 0 to 65,535 can be specified. Refer to Figure 25.26 for settings.
15 to 0	PICT_STRD_C [15:0]	H'0000	R/W	Memory Stride of Source Picture C Plane These bits specify in 1-byte units the memory stride of the source picture C plane read by the RPFn. When an RGB-format picture is read, these bits do not need to be set. A value from 0 to 65,535 can be specified. Refer to Figure 25.26 for settings. In the YCbCr planar format, this setting is used as the memory stride of the Cb and Cr planes.

This register specifies the memory stride of the picture planes in the source area as shown in Figure 25.26. The memory stride of the α plane should be specified through VI6_RPFn_SRCM_ASTRIDE.ALPH_STRD. When the RPF input is in an RGB format, only the RGB plane is read; when the input is in YCbCr format, the Y and C planes are read as shown in Figure 25.26. When the α plane is used, the α plane is also read. According to the image format and the necessity of the α plane, specify the necessary addresses where the source image is stored (VI6_RPFn_SRCM_ADDR_Y, VI6_RPFn_SRCM_ADDR_C, and VI6_RPFn_SRCM_ADDR_AI).

Whether the α plane needs to be read is determined according to the α plane selection method and IROP operation type. For details, refer to section 25.2.7.6.

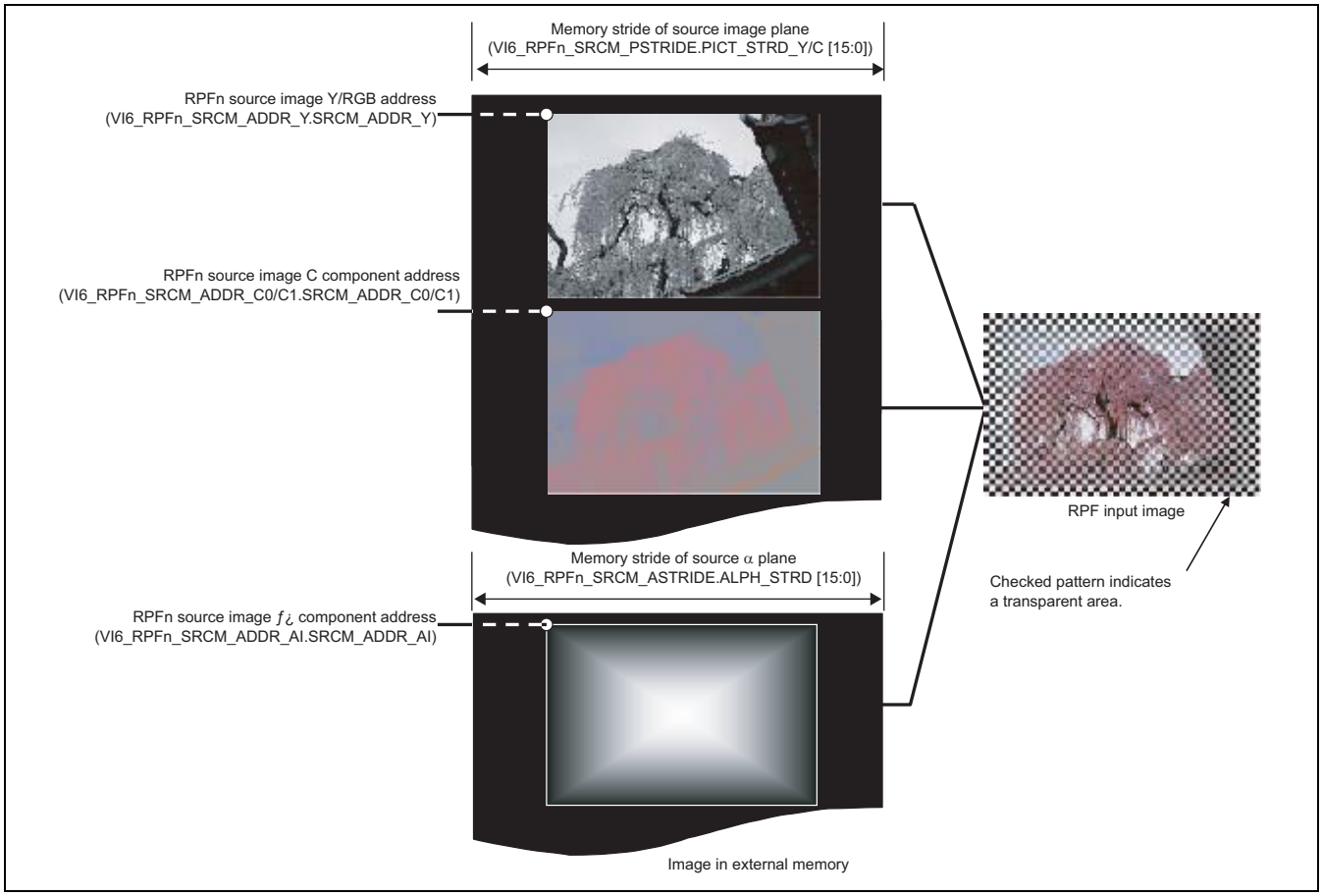
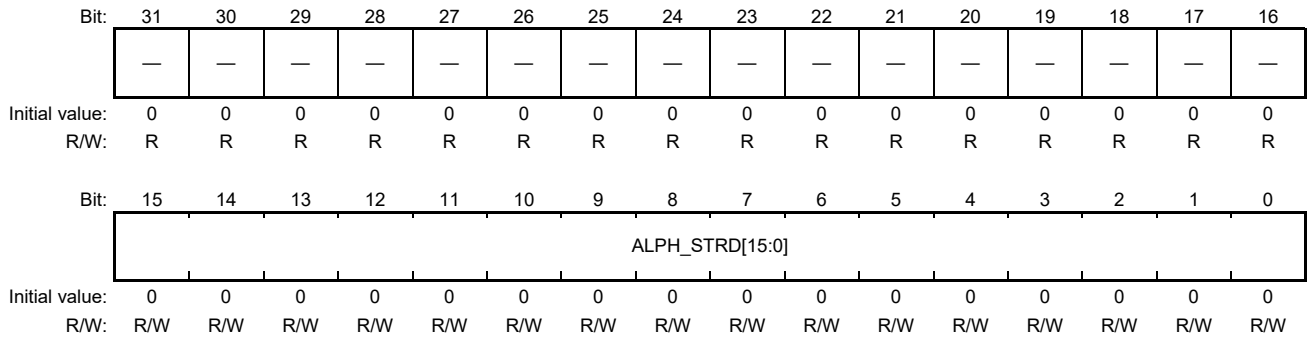


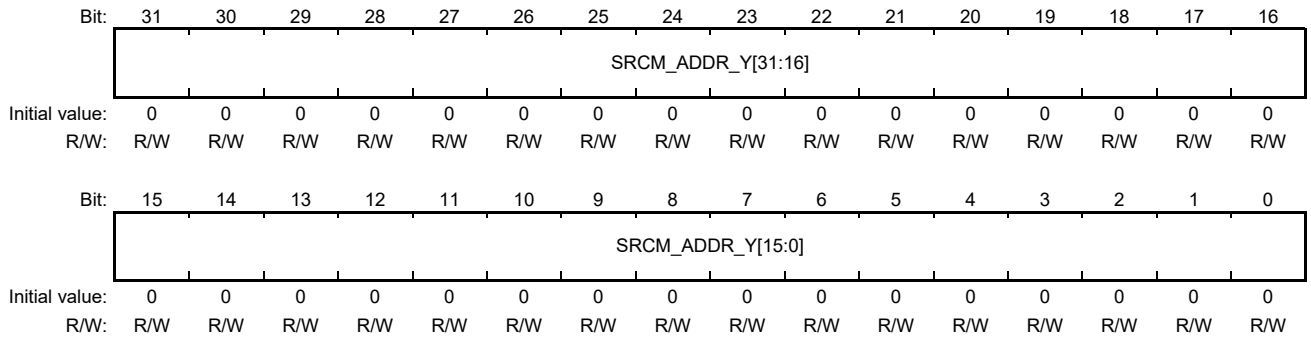
Figure 25.26 Reading an Image from RPFn Source Area

25.2.7.14 RPFn Source α Memory Stride Setting Registers (VI6_RPFn_SRCM_ASTRIDE)



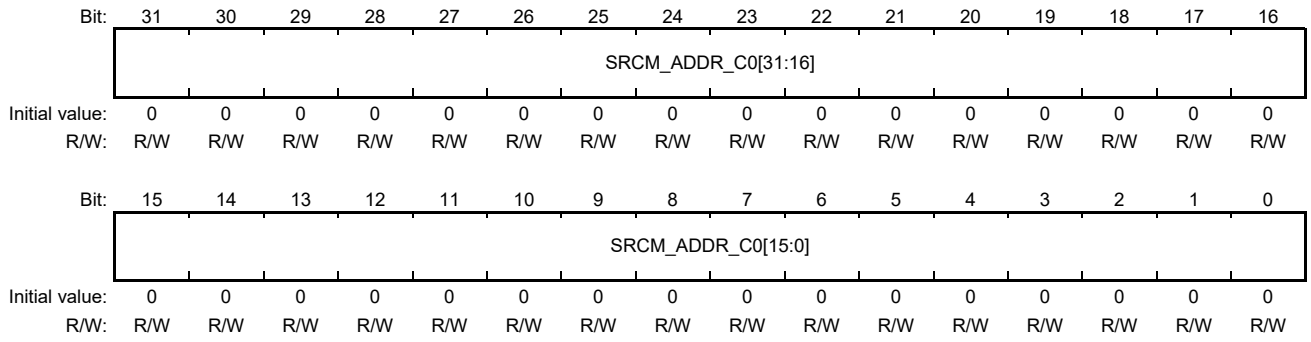
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	ALPH_STRD [15:0]	H'0000	R/W	Memory Stride of Source α Plane These bits specify in 1-byte units the memory stride of the source α plane read by the RPFn. A value from 0 to 65,535 can be specified. Refer to Figure 25.26 for settings.

25.2.7.15 RPFn Source Y/RGB Address Registers (VI6_RPFn_SRCM_ADDR_Y)



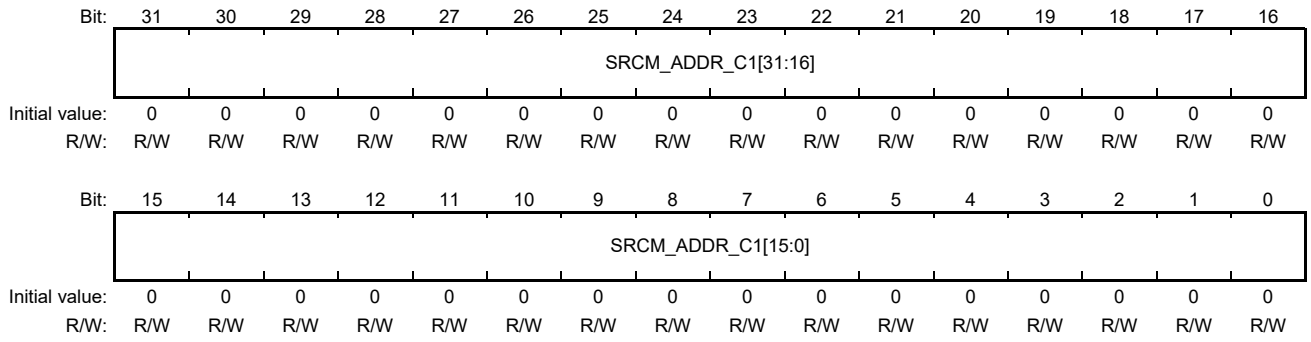
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ ADDR_Y [31:0]	H'0000 0000	R/W	Source Image Y/RGB Plane Storing Address These bits specify in 1-byte units the start address of the source image Y plane and packed RGB plane read by the RPFn. A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 25.26 in section 25.2.7.13 for settings.

25.2.7.16 RPFn Source Chroma Address Registers 0 (VI6_RPFn_SRCM_ADDR_C0)



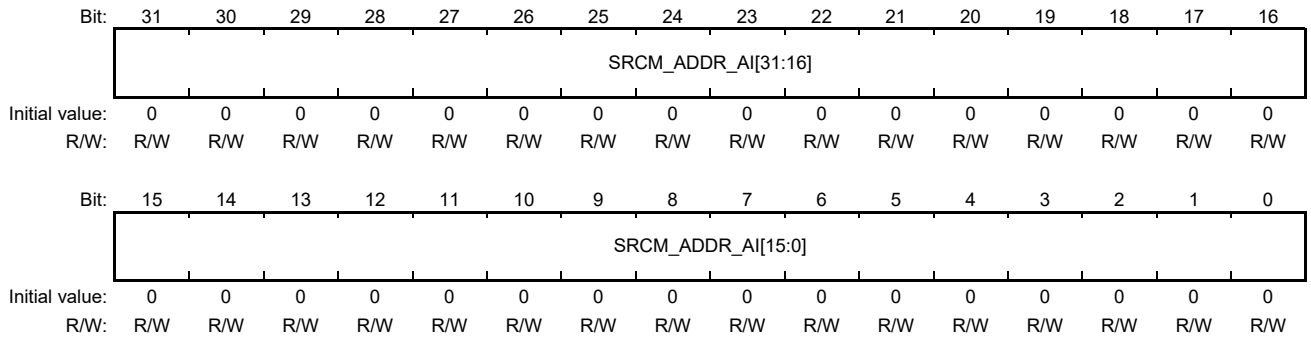
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ ADDR_C0 [31:0]	H'0000 0000	R/W	Source Image C Plane Storing Address 0 These bits specify in 1-byte units the start address of the source image C plane read by the RPFn. Here, the C plane indicates the combined CbCr plane when a semi-planar format is selected from the packed YCbCr formats shown in Table 25.18 or the Cb plane when a planar format is selected. When an interleaved format is selected or the RPF input is in an RGB format, this setting is not used. A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 25.26 in section 25.2.7.13 for settings.

25.2.7.17 RPFn Source Chroma Address Registers 1 (VI6_RPFn_SRCM_ADDR_C1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ ADDR_C1 [31:0]	H'0000 0000	R/W	Source Image C Plane Storing Address 1 These bits specify in 1-byte units the start address of the Cr plane when a planar YCbCr format shown in Table 25.18 is read by the RPFn. This setting is not used when the RPF input is in YCbCr format that is not a planar format or in an RGB format. A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 25.26 in section 25.2.7.13 for settings.

25.2.7.18 RPFn Source α Address Registers (VI6_RPFn_SRCM_ADDR_AI)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRCM_ ADDR_AI [31:0]	H'0000 0000	R/W	Source Image α Plane Storing Address These bits specify in 1-byte units the start address of the α plane of the source image read by the RPFn. Specify in the same way as the start address of the picture plane. When the α plane is not read from the source area, these bits do not need to be set. A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 25.26 in section 25.2.7.13 for settings.

25.2.8 WPF Control Registers

25.2.8.1 WPFn-Source-RPF Registers (VI6_WPFn_SRCRPF)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	VIR_ACT[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	RPF4_ACT[1:0]		RPF3_ACT[1:0]		RPF2_ACT[1:0]		RPF1_ACT[1:0]		RPF0_ACT[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29, 28	VIR_ACT [1:0]	00	R/W	Virtual RPF Start Enable in BRU These bits enable start of the virtual RPF in the BRU as the source RPF for the WPFn when the WPFn is started. For details of the virtual RPF, refer to the following. Section 25.2.16.1, BRU Input Control Register (VI6_BRU_INCTRL) Section 25.2.16.2, Size Register of BRU Input Virtual RPF (VI6_BRU_VIRRPF_SIZE) Section 25.2.16.3, Display Location Register of BRU Input Virtual RPF (VI6_BRU_VIRRPF_LOC) Section 25.2.16.4, Color Information Register of BRU Input Virtual RPF (VI6_BRU_VIRRPF_COL) Note that the virtual RPF is in the BRU as shown in Figure 25.44 and there are no register bits for DPR setting related to the virtual RPF. 00: The virtual RPF in the BRU is not started. 01: The virtual RPF in the BRU is started as a sub layer source RPF for the WPFn. 10: The virtual RPF in the BRU is started as the master-layer source RPF for the WPFn. 11: Setting prohibited
27 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	RPF4_ACT [1:0]	00	R/W	RPFn Start Enable (RPFn_ACT, n = 0 to 4) These bits enable start of RPFn as the source RPF for the WPFn when the WPFn is started. When RPFn is not started by any of the WPF0 to WPF3, set the VI6_DPR_RPFn_ROUTE.RT_RPFn bits to 63 (H'3F). 00: RPFn is not started. 01: RPFn is started as a sub layer source RPF for the WPFn. 10: RPFn is started as the master-layer source RPF for the WPFn. 11: Setting prohibited
7, 6	RPF3_ACT [1:0]	00	R/W	
5, 4	RPF2_ACT [1:0]	00	R/W	
3, 2	RPF1_ACT [1:0]	00	R/W	
1, 0	RPF0_ACT [1:0]	00	R/W	

When the WPFn is started through the VSP1 start register n (VI6_CMDn: n = 0, 1, 2, 3), the RPF and virtual RPF in the BRU specified as the source RPF in this register are also started to supply data to the VSP1 internal modules.

Note the following when specifying the source RPF.

1. Each source RPF can be assigned to only one target WPFn; a single RPF cannot be assigned as the source RPF for multiple WPFs. For example, when setting VI6_WPF0_SRCRPF to H'00000008 and VI6_WPF1_SRCRPF to H'00000004 is attempted, the VSP1 will not operate correctly (these settings are prohibited) because RPF1 is assigned as both the master-layer source RPF for WPF0 and a sub layer source RPF for WPF1.
2. When blending or ROP operation is applied to multiple images through the BRU, multiple source RPFs are necessary for one WPF. When multiple source RPFs are used, images should be classified into a master layer and sub layers; assign one of the source RPFs as the master-layer source RPF and other RPFs as sub layer source RPFs. Do not assign all RPFs as sub layer source RPFs (VI6_WPF1_SRCRPF = H'00000015) or two or more RPFs as the master-layer source RPF (VI6_WPF3_SRCRPF = H'0000025A) (such settings are prohibited).
3. When the BRU is not used, there should be only one source RPF for one WPF. In this case, the source RPF should be assigned as the master-layer source RPF.
4. Calculate the master layer and sub layer sizes as described in section 25.1.5. When the BRU is used and the SRU or UDS is used between the RPF and BRU, the master layer and sub layer sizes may have been upscaled or downscaled before input to the BRU with respect to the sizes output from the source RPF. When determining the relative locations among layers for blending or ROP operation, take account of the size of each image input to the BRU. In particular, be careful not to place the entire sub layer outside the master layer as explained in the description of the HCOORD and VCOORD bits in VI6_RPFn_LOC in section 25.2.7.5.

25.2.8.2 WPFn Horizontal Input Size Clipping Registers (VI6_WPFn_HSZCLIP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	HCEN	—	—	—	—	HCL_OFST[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	HCL_SIZE[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	HCEN	0	R/W	Horizontal Size Clipping Enable/Disable Enables or disables clipping of the horizontal size of the WPFn input image. 0: Horizontal size clipping is disabled 1: Horizontal size clipping is enabled
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HCL_OFST [7:0]	H'00	R/W	Horizontal Size Clipping Offset Value Setting These bits specify the offset size (pixels) from the left end of the image in horizontal size clipping when the HCEN bit is 1 (Figure 25.27). The left side of the image input to the WPF is cut off for the size specified in these bits. When the HCEN bit is 0, this setting is ignored. A value from 0 to 255 can be specified. (HCL_OFST + HCL_SIZE) should not exceed the horizontal size of the WPF input. If the setting shown in the bottom example in Figure 25.27 is made, VSP1 does not operate correctly.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	HCL_SIZE [11:0]	H'000	R/W	Horizontal Clipping Size Setting When the HCEN bit is 1, these bits specify the clipping size for horizontal clipping processing. Through this processing, the area of the horizontal size specified through the HCL_SIZE bits starting from the offset position specified through the HCL_OFST bits is determined as the valid image area. Accordingly, the right-side pixels beyond the (HCL_OFST + HCL_SIZE) size in the WPFn input image are discarded. When the HCEN bit is 0, this setting is ignored. A value from 1 to 2,048 can be specified. (HCL_OFST + HCL_SIZE) should not exceed the horizontal size of the WPF input. If the setting shown in the bottom example in Figure 25.27 is made, VSP1 does not operate correctly. Note: When the WPFn output format is YCbCr4:2:2 or YCbCr4:2:0, specify an even value in these bits.

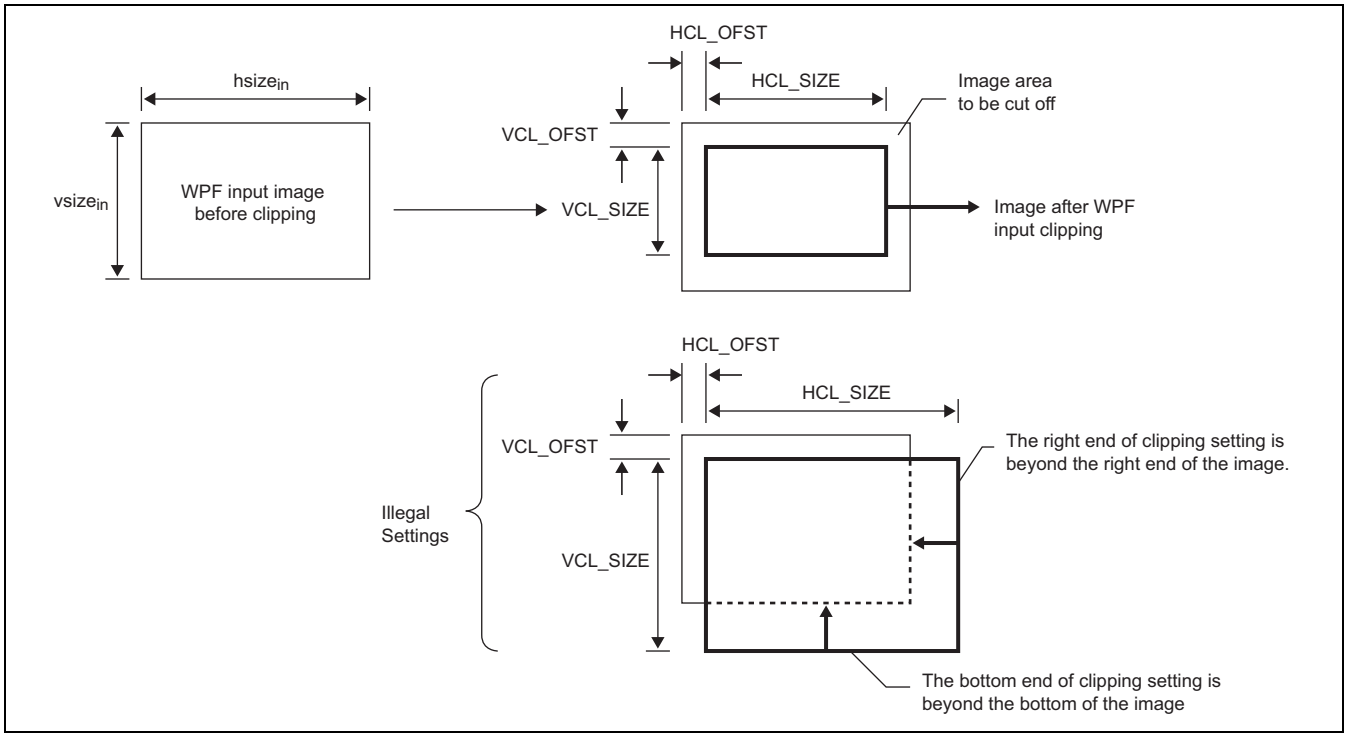


Figure 25.27 Image Clipping in WPF Input Section

25.2.8.3 WPFn Vertical Input Size Clipping Registers (VI6_WPFn_VSZCLIP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VCEN	—	—	—	—	VCL_OFST[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	VCL_SIZE[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	VCEN	0	R/W	Vertical Size Clipping Enable/Disable Enables or disables clipping of the vertical size of the WPFn input image. 0: Vertical size clipping is disabled 1: Vertical size clipping is enabled
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	VCL_OFST [7:0]	H'00	R/W	Vertical Size Clipping Offset Value Setting These bits specify the offset size (pixels) from the top end of the image in vertical size clipping when the VCEN bit is 1 (Figure 25.27). The top of the image input to the WPF is cut off for the size specified in these bits. When the VCEN bit is 0, this setting is ignored. A value from 0 to 255 can be specified. (VCL_OFST + VCL_SIZE) should not exceed the vertical size of the WPF input. If the setting shown in the bottom example in Figure 25.27 is made, VSP1 does not operate correctly.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	VCL_SIZE [11:0]	H'000	R/W	Vertical Clipping Size Setting When the VCEN bit is 1, these bits specify the clipping size for vertical clipping processing. Through this processing, the area of the vertical size specified through the VCL_SIZE bits starting from the offset position specified through the VCL_OFST bits is determined as the valid image area. Accordingly, the bottom pixels beyond the (VCL_OFST + VCL_SIZE) size in the WPFn input image are discarded. When the VCEN bit is 0, this setting is ignored. A value from 1 to 2,048 can be specified. (VCL_OFST + VCL_SIZE) should not exceed the vertical size of the WPF input. If the setting shown in the bottom example in Figure 25.27 is made, VSP1 does not operate correctly. Note: When the WPFn output format is YCbCr4:2:0, specify an even value in these bits.

25.2.8.4 WPFn Output Format Registers (VI6_WPFn_OUTFMT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PDV[7:0]								PXA	—	—	—	—	—	—	FLP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPYCS	SPUVS	DITH[1:0]		WRTM[2:0]			CSC	—	WRFMT[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	PDV[7:0]	H'00	R/W	PAD Value in Output Packed Data These bits specify the value to be stored in the bit field indicated as PAD or P in the output formats shown in Table 25.23. To store this value in PAD, specify 0 in the PXA bit. A value from 0 to 255 can be specified.
23	PXA	0	R/W	PAD Data Select Selects the value to be stored in the bit field indicated as PAD or P in the packed RGB output formats shown in Table 25.23. Both the value specified in the PDV bits and the α data input from the DPR to WPF are eight bits, but some of the PAD and P bit fields shown in Table 25.23 are four bits or one bit. When the target bit field is not eight bits, the number of bits in the PDV value and the α data input from the DPR to WPF is reduced according to the VI6_WPFn_RNDCTRL.ABRM setting. For bit count reduction, refer to Figure 25.28 and the description of VI6_WPFn_RNDCTRL.ABRM. 0: The value specified in the PDV bits is stored in the PAD shown in Table 25.23. 1: The α value output from DPR in pixel units is stored in the PAD shown in Table 25.23.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	FLP	0	R/W	Vertical flipping Select This bit selects the vertical flipping processing to be applied to the WPFn output image. Figure 25.29 shows the correspondence between the original image and the vertical flipping result according to this setting. 0: No vertical flipping 1: vertical flipping Flipping can be specified only in WPF0. In other channels, always specify 0 in these bits. Note that the destination address setting should be changed according to the setting of these bits. For details, refer to section 25.2.8.9. When the LIF module is used (VI6_LIF_CTRL.LIF_EN = 1), set 0 to FLP.

Bit	Bit Name	Initial Value	R/W	Description
15	SPYCS	0	R/W	WPF Output Mode Setting 1 When the output format is YUY2, set this bit to 1 and set the WRFMT bits to 71 (H'47). When the output format is YVYU, set this bit and the SPUVS bit to 1 and set the WRFMT bits to 71 (H'47). In other cases, set this bit to 0.
14	SPUVS	0	R/W	WPF Output Mode Setting 2 When the output format is NV61, set this bit to 1 and set the WRFMT bits to 65 (H'41). When the output format is NV21, set this bit to 1 and set the WRFMT bits to 66 (H'42). When the output format is YVYU, set this bit and the SPYCS bit to 1 and set the WRFMT bits to 71 (H'47). In other cases, set this bit to 0.
13, 12	DITH[1:0]	00	R/W	Dithering Enable/Disable When the output format specified through the WRFMT bits is RGB with 18 bpp (262,144 colors) or less, the color reduction processing is applied to match the number of colors. The color reduction processing may generate the artifacts of pseudo gradation, which can be suppressed through dithering. The DITH bits enable or disable dithering during color reduction. When the output format specified through the WRFMT bits is YCbCr, specify 0 in these bits. And when VI6_WPFn_OUTFMT.CSC is set to 1, specify 0 in these bits even in the case that the output format specified through the WRFMT bits is RGB. 00: Dithering is disabled 11: Dithering is enabled 01, 10: Setting prohibited
11 to 9	WRTM[2:0]	000	R/W	CSC Conversion Expression Setting These bits select the expression for color space conversion. The conversion direction is RGB to YCbCr when the format specified in the WRFMT bits is RGB, or YCbCr to RGB when the format is YCbCr. 000: BT.601 YCbCr [16,235/240] ↔ RGB [0,255] 001: BT.601 YCbCr [0,255] ↔ RGB [0,255] 010: BT.709 YCbCr [16,235/240] ↔ RGB [0,255] 011: BT.709 YCbCr [16,235/240] ↔ RGB [16,235] 100 to 111: Setting prohibited
8	CSC	0	R/W	Color Space Conversion Setting Enables or disables YCbCr ↔ RGB color space conversion to be executed in the WPFn. The characteristics of color space conversion are determined by the WRTM setting. There are some points to be noted about the relationship between the CSC setting and output format (WRFMT). For details refer to section 25.2.7.3, RPFn Input Format Registers (VI6_RPFn_INFMT). 0: Color space is not converted. 1: Color space is converted.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 0	WRFMT[6:0]	H'00	R/W	WPF Output Image Format Setting These bits select the format of the image output from the WPFn to the external memory from among those listed in Table 25.23 and Table 25.24. Notes: 1. Number of output pixels When YCbCr4:2:2 is specified through WRFMT, the horizontal size of the output image should be a multiple of 2 pixels. When YCbCr4:2:0 is specified, the vertical and horizontal sizes of the output image should be multiples of 2 pixels. Specify an appropriate data flow of the source RPF → DPR → target WPF so that the size of the image input to the target WPF satisfies the above restrictions. In particular, when the data flow includes a module or a function that modifies (upscales, downscales, or clips) the image size, take special care about the module or function settings. 2. Output lines in YCbCr4:2:0 In the YCbCr4:2:0 output format, the number of chrominance lines in the vertical direction is one-half the number of luminance lines. For this reason, the WPF outputs only even-numbered chrominance lines (lines 0, 2, 4, 6, ...) (conversion from (A) to (B) in Figure 25.30). When vertical flipping is also specified through the FLP bits, the flipping processing is executed last and the chrominance line locations are inverted (lines 1, 3, 5, 7, …) in the output image ((C) in Figure 25.30).

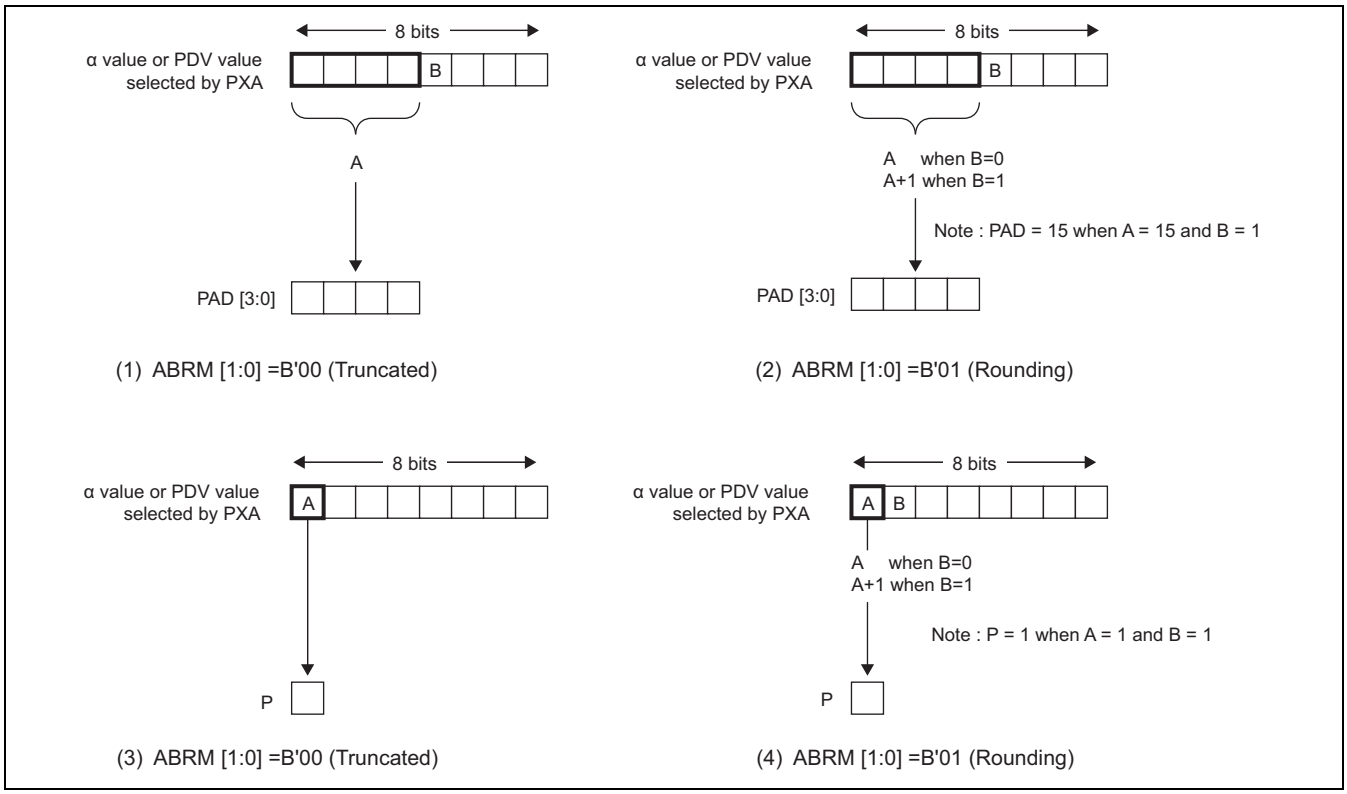


Figure 25.28 Selection of PAD Value and Reduction of Bit Count through PXA Setting

Without flipping (FLP=0)

Vertical flipping

Vertical flipping (FLP=1)

Figure 25.29 Correspondence between Original Image and Vertical Flipping Result according to FLP Setting

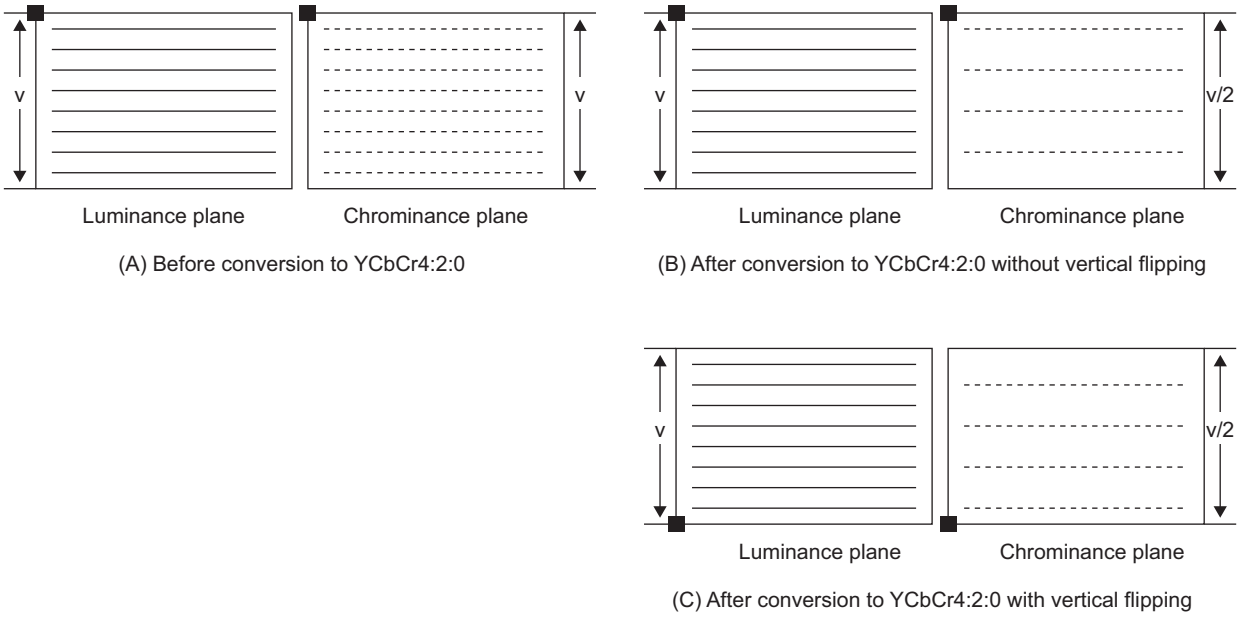


Figure 25.30 Chrominance Output Lines in YCbCr4:2:0 and Vertical Flipping Result

Table 25.23 Packed RGB Formats for WPF Output

WRFMT	Bit per pixel	Phase	Bit field																													
			31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
H'00	8	—	R0	R0	R0	G0	G0	G0	B0	B0	R1	R1	R1	G1	G1	G1	B1	B1	R2	R2	R2	G2	G2	G2	B2	B2	R3	R3	R3	G3	G3	G3	B3	B3
H'01	12	—	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'02		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	0	0	0	0	R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	0	0	0	0
H'03	—	—	Reserved								Reserved								Reserved								Reserved							
H'04	15	—	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'05		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	0
H'06	16	—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'07	18	—	PAD0								0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'08		—	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	PAD0							
H'09		—	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	PAD0							
H'0A		—	PAD0								R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0
H'0B		—	PAD0								0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0
H'0C		—	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	PAD0							
H'0D		—	PAD0								R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0
H'0E		—	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	PAD0							
H'0F		0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1
		1	R1	R1	R1	R1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2
		2	G2	G2	B2	B2	B2	B2	B2	B2	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3
H'10		0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	0	0	0	0	0	0	R1	R1	R1	R1	R1	R1	G1	G1
		1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	0	0	0	0	0	0	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	B2	B2	B2	B2
		2	B2	B2	0	0	0	0	0	0	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	0	0	0	0	0	0
H'11		0	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1
		1	0	0	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2
		2	0	0	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3
H'12		0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1	0	0
		1	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2	0	0
		2	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3	0	0
H'13	24	—	PAD0								R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
H'14		—	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	PAD0							
H'15		0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
		1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
		2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
H'16	18	—	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	0	0	0	0	0	0	0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'17		—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
H'18	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
		1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
		2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
H'19	12	—	PAD0				R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD1				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1
H'1A		—	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0	PAD0				R1	R1	R1	R1	G1	G1	G1	G1	B1	B1	B1	B1	PAD1			
H'1B	15	—	P0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A1	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1
H'1C		—	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	A0	R1	R1	R1	R1	R1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	P1
H'1D	12	—	PAD0				B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD1				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1
H'1E		—	B0	B0	B0	B0	G0	G0	G0	G0	R0	R0	R0	R0	PAD0				B1	B1	B1	B1	G1	G1	G1	G1	R1	R1	R1	R1	PAD1			
H'1F	15	—	A0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P1	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1
H'20		—	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	P0	B1	B1	B1	B1	B1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	P1
H'21	18	0	0	0	B0	B0	B0	B0	B0	B0	0	0	G0	G0	G0	G0	G0	G0	0	0	R0	R0	R0	R0	R0	R0	0	0	B1	B1	B1	B1	B1	B1
		1	0	0	G1	G1	G1	G1	G1	G1	0	0	R1	R1	R1	R1	R1	R1	0	0	B2	B2	B2	B2	B2	B2	0	0	G2	G2	G2	G2	G2	G2
		2	0	0	R2	R2	R2	R2	R2	R2	0	0	B3	B3	B3	B3	B3	B3	0	0	G3	G3	G3	G3	G3	G3	0	0	R3	R3	R3	R3	R3	R3
H'22	24	—	PAD0								B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0
H'23	16	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0
H'24~H'3F	—	—	Reserved								Reserved								Reserved								Reserved							

Table 25.24 Packed YCbCr Formats for WPF Output

WRFMT [6:0]	Packed YCbCr Output Format	Reference
H'40	YCbCr4:4:4 semi-planar	Figure 25.19
H'41	YCbCr4:2:2 semi-planar (NV16, NV61*1)	
H'42	YCbCr4:2:0 semi-planar (NV12, NV21*1)	
H'43 to H'45	Reserved	—
H'46	YCbCr4:4:4 interleaved	Figure 25.20
H'47	YCbCr4:2:2 interleaved type 0 (UYVY, YUY2*2, YVYU*3)	
H'48	YCbCr4:2:2 interleaved type 1	
H'49	YCbCr4:2:0 interleaved	
H'4A	YCbCr4:4:4 planar	Figure 25.21
H'4B	YCbCr4:2:2 planar (YV16)	
H'4C	YCbCr4:2:0 planar (YV12, YU12)	
H'4D to H'7F	Reserved	—

Notes: 1. When the output format is NV61 or NV21, set SPUVS (bit 14) to 1.
2. When the output format is YUY2, set SPYCS (bit 15) to 1.
3. When the output format is YVYU, set SPUVS (bit 14) to 1 and SPYCS (bit 15) to 1.

For details of each YCbCr format, refer to Figure 25.19, Figure 25.20, and Figure 25.21. In these figures, registers for the RPF are indicated; read them as registers for the WPF as follows.

(RPF registers in the figures)	→	(Corresponding WPF registers)
VI6_RPFn_SRCM_ADDR_Y.SRCM_ADDR_Y	→	VI6_WPFn_DSTM_ADDR_Y.DSTM_ADDR_Y
VI6_RPFn_SRCM_ADDR_C0.SRCM_ADDR_C0	→	VI6_WPFn_DSTM_ADDR_C0.DSTM_ADDR_C0
VI6_RPFn_SRCM_ADDR_C1.SRCM_ADDR_C1	→	VI6_WPFn_DSTM_ADDR_C1.DSTM_ADDR_C1

25.2.8.5 WPFn Data Swapping Registers (VI6_WPFn_DSWAP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	P_LLS	P_LWS	P_WDS	P_BTS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	P_LLS	0	R/W	WPF Output Data Swapping in LONG LWORD Units 0: Data swapping in LONG LWORD (64-bit) units is disabled 1: Data swapping in LONG LWORD (64-bit) units is enabled This should be set to 1in most cases, but when data has been swapped in 64-bit units by another data processing channel, specify 0
2	P_LWS	0	R/W	WPF Output Data Swapping in Longword Units 0: Data swapping in longword (32-bit) units is disabled 1: Data swapping in longword (32-bit) units is enabled This should be set to1 in most cases, but when data has been swapped in 32-bit units by another data processing channel, specify 0
1	P_WDS	0	R/W	WPF Output Data Swapping in Word Units The effect of this bit setting is the same as data swapping in the RPF; refer to Table 25.20. 0: Data swapping in word (16-bit) units is disabled 1: Data swapping in word (16-bit) units is enabled
0	P_BTS	0	R/W	WPF Output Data Swapping in Byte Units The effect of this bit setting is the same as data swapping in the RPF; refer to Table 25.20. 0: Data swapping in byte (8-bit) units is disabled 1: Data swapping in byte (8-bit) units is enabled

25.2.8.6 WPFn Rounding Control Registers (VI6_WPFn_RNDCTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	CBRM	—	—	ABRM[1:0]		ATHRESH[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CLMD[1:0]		—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	CBRM	0	R/W	Bit Count Reduction Method Selection for Data Storage in Packed RGB This bit specifies the method for reducing the number of bits when data is stored in the bit fields indicated as R, G, and B in Table 25.23 and the target bit fields are not eight bits. 0: Bit count conversion: The lower-order bits are truncated 1: Bit count conversion: Rounding (rounding off)
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25, 24	ABRM[1:0]	00	R/W	Bit Count Reduction Method Selection for Data Storage in PAD These bits specify the method for reducing the number of bits when the data selected through VI6_WPFn_OUTFMT.PXA is stored in the bit fields indicated as PAD or P in Table 25.23 and the target bit field is four bits or one bit. A value of B'10 can be specified only when the packed RGB format specified through VI6_WPFn_OUTFMT.WRFMT includes a 1-bit P field. In this case, when the data selected through VI6_WPFn_OUTFMT.PXA is greater than the ATHRESH value, 1 is stored in the P field; when the selected data is not greater than the ATHRESH value, 0 is stored. 00: Bit count conversion: The lower-order bits are truncated 01: Bit count conversion: Rounding (rounding off) 10: Bit count conversion: Comparison with the threshold value (this setting is allowed only when the storage field is one bit) 11: Setting prohibited
23 to 16	ATHRESH [7:0]	H'00	R/W	Threshold for Conversion to 1-Bit α Data These bits specify the threshold value used for conversion from 8-bit α data to one bit when the ABRM bits are set to B'10. When the 8-bit α value before bit count reduction is equal to or smaller than the ATHRESH value, 0 is stored as the reduced 1-bit α data. In other cases, 1 is stored as the 1-bit α data. A value from 0 to 255 can be specified.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
13, 12	CLMD[1:0]	00	R/W	Color Data Clipping These bits specify the method for clipping the YCbCr color data output from the WPF. When RGB color data is output from the WPF, specify 0 in these bits. 00: Output value is not clipped (0 to 255) 01: Output value is clipped: YCbCr mode 1 (16 to 235 (Y), 16 to 240 (Cb/Cr)) 10: Output value is clipped: YCbCr mode 2 (Y/Cb/Cr = 1 to 254) 11: Setting prohibited
11 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.2.8.7 WPFn Destination Y Plane Memory Stride Registers (VI6_WPFn_DSTM_STRIDE_Y)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PICT_STRD_Y[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PICT_STRD_Y [15:0]	H'0000	R/W	Memory Stride of Destination Picture Y/RGB Plane These bits specify in 1-byte units the memory stride of the destination picture in the external memory to be written to by the WPFn as shown in Figure 25.31. A value from H'0000 to H'FFFF can be specified.

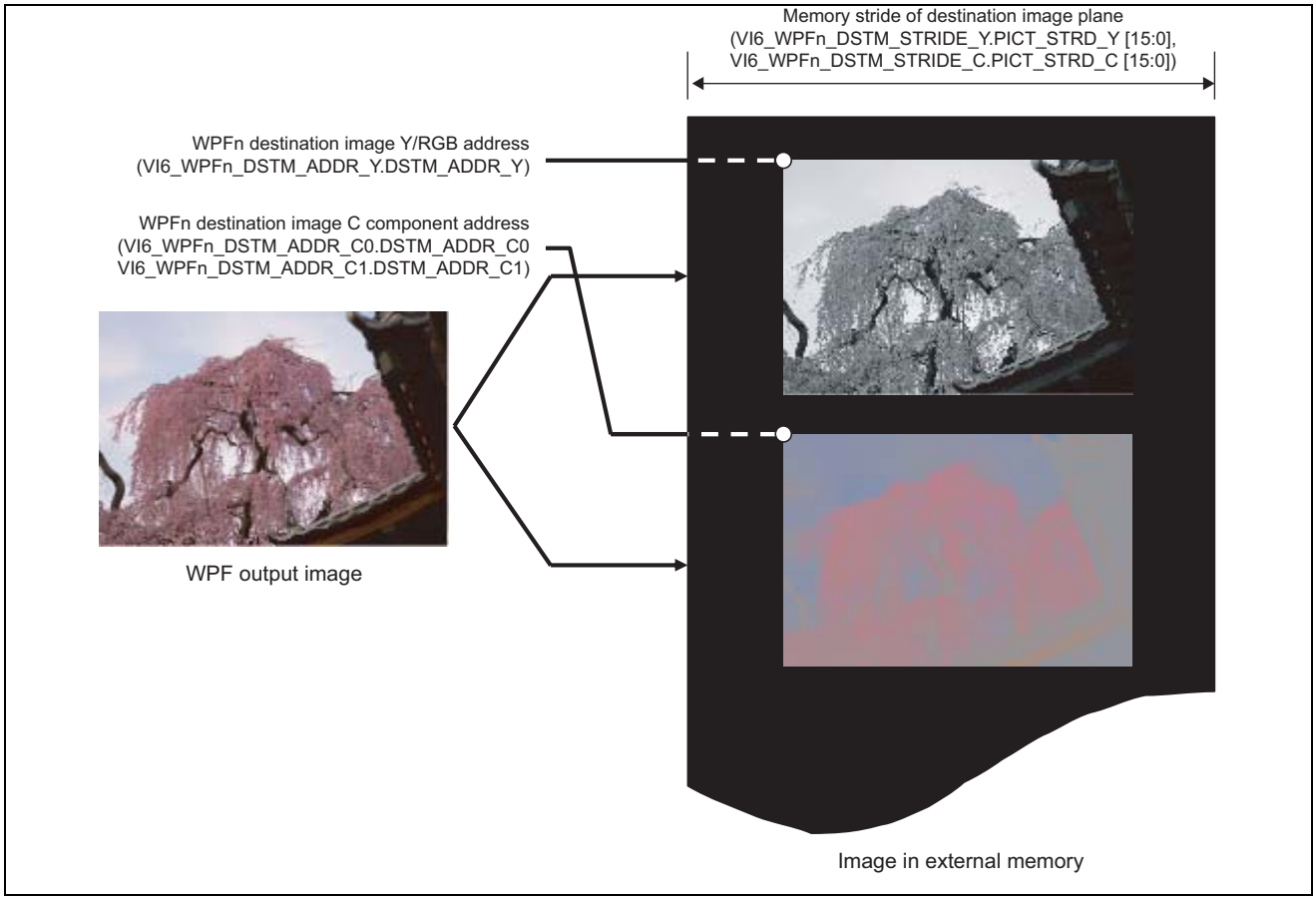
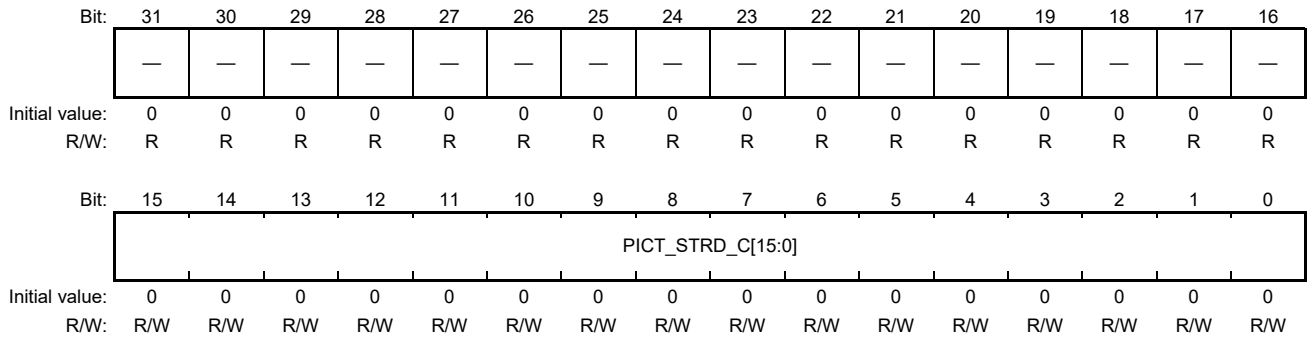


Figure 25.31 Writing Image Data to Destination Area in WPFn

25.2.8.8 WPFn Destination C Plane Memory Stride Registers (VI6_WPFn_DSTM_STRIDE_C)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 0	PICT_STRD_C [15:0]	H'0000	R/W	Memory Stride of Destination Picture C Plane These bits specify in 1-byte units the memory stride for the C plane of the destination picture in the external memory to be written to by the WPFn as shown in Figure 25.31. When the WPFn outputs images in an RGB format, this setting is not used. When the WPFn outputs images in YCbCr planar format, this setting is applied to both the Cb and Cr planes. A value from H'0000 to H'FFFF can be specified.

25.2.8.9 WPFn Destination Y/RGB Address Registers (VI6_WPFn_DSTM_ADDR_Y)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DSTM_ADDR_Y[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DSTM_ADDR_Y[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSTM_ ADDR_Y [31:0]	H'0000 0000	R/W	Destination Image Y/RGB Plane Storing Address These bits specify in 1-byte units the address for storing the destination-image Y plane or packed RGB plane to be written to by the WPFn in the method described later. A value from H'00000000 to H'FFFFFFFF can be specified.

(Destination Address Specification Method)

When flipping is not used, the start address of a frame (address FHA shown in Figure 25.32) should be specified as the destination address. When flipping is used, the destination address is not the frame head address (FHA); one of addresses A0 to A1 shown in Figure 25.32 should be selected according to the combination of desired and flipping (VI6_WPFn_OUTFMT.FLP setting).

To strictly define locations A0 to A1, let the memory stride (VI6_WPFn_DSTM_STRIDE_Y/C setting) be S as shown in Figure 25.32). Calculate the destination address (one of A0 to A1) using the formula shown in Table 25.25 and specify it in the destination address storing register.

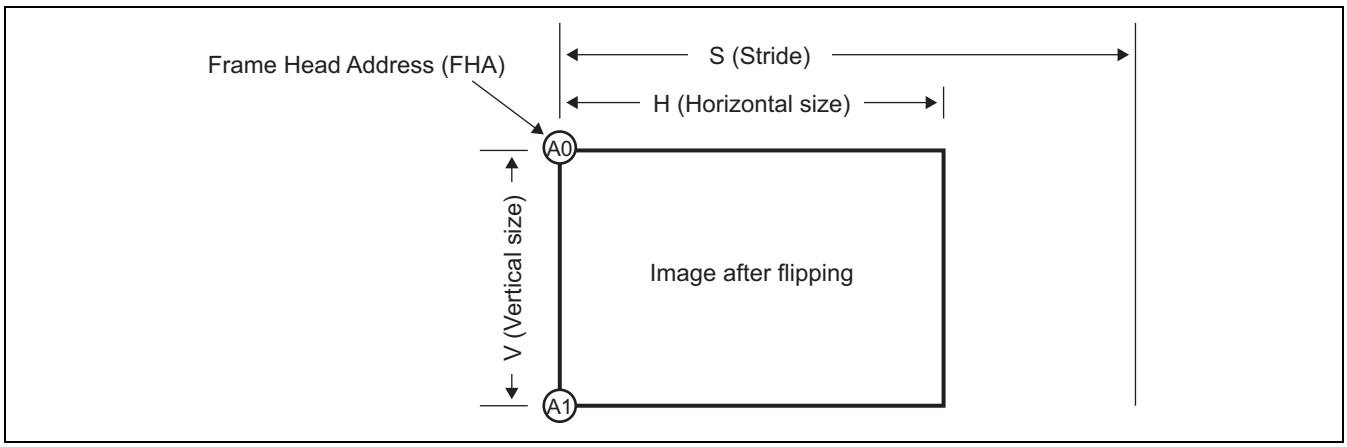


Figure 25.32 Location of Destination Address to be Specified for Vertical Flipping

Table 25.25 Destination Address A_0, and A_1 Calculation Formulas

VI6_WPFn_OUTFMT.FLP Setting	Formula for Calculating Address to be Set in VI6_WPFn_DSTM_ADDR_Y, VI6_WPFn_DSTM_ADDR_C0, and VI6_WPFn_DSTM_ADDR_C1
0	$A_0 = FHA$
1	$A_1 = FHA + (V \times L - 1) \times S$

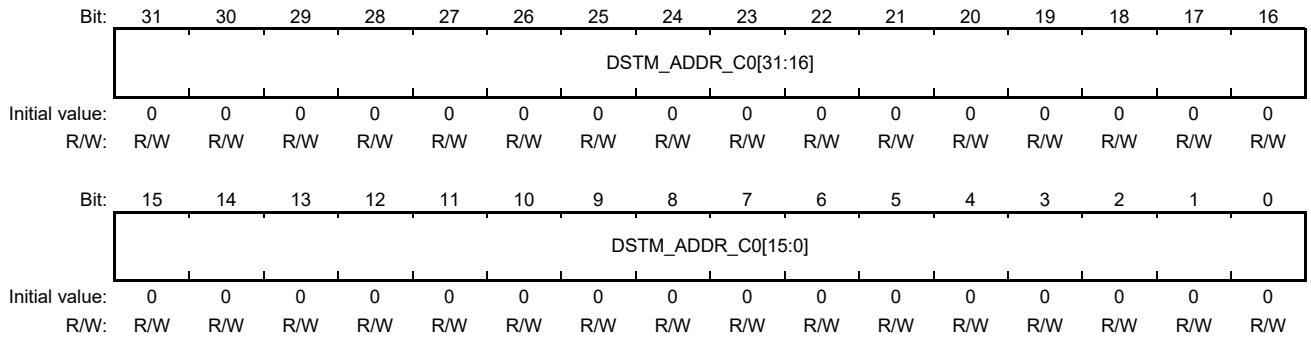
Table 25.25a Value of L according to VI6_WPFn_OUTFMT.WRFMT Setting (for RGB and Luminance Y Address Calculation)

VI6_WPFn_OUTFMT.WRFMT	L
73	0.5
0 to 2, 4 to 35, 64 to 66, 70 to 72, or 74 to 76	1

Table 25.25b Value of L according to VI6_WPFn_OUTFMT.WRFMT Setting (for Chrominance C0 and C1 Address)

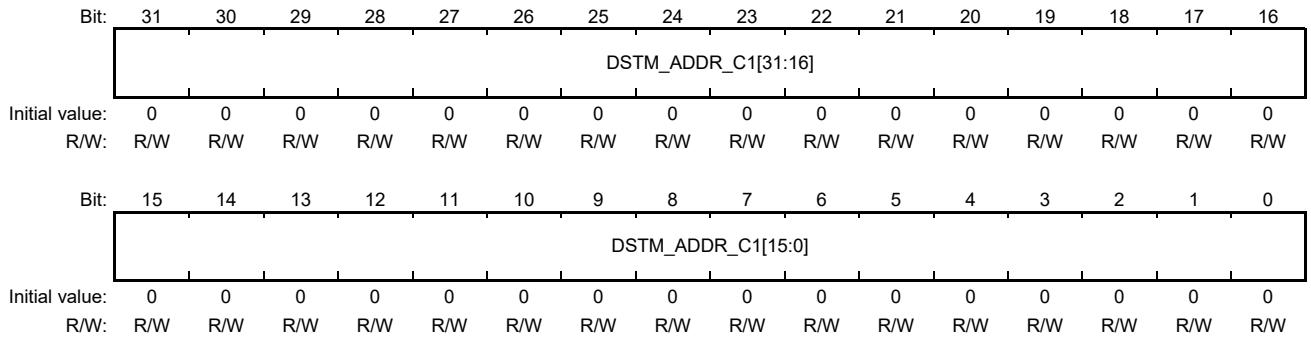
VI6_WPFn_OUTFMT.WRFMT	L
70 to 73	Not defined
66, 76	0.5
64 to 65, 74 to 75	1

25.2.8.10 WPFn Destination Chroma Address Registers 0 (VI6_WPFn_DSTM_ADDR_C0)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSTM_ ADDR_C0 [31:0]	H'0000 0000	R/W	Destination Image C Plane Storing Address 0 These bits specify in 1-byte units the address for storing the destination-image C plane to be written to by the WPFn. Refer to the description of VI6_WPFn_DSTM_ADDR_Y for settings. Here, the C plane indicates the combined CbCr plane when a semi-planar format is selected from the packed YCbCr formats shown in Table 25.24 or the Cb plane when a planar format is selected. When an interleaved format is selected or the output is in an RGB format, this setting is not used. A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 25.32 in section 25.2.8.9 for settings.

25.2.8.11 WPFn Destination Chroma Address Registers 1 (VI6_WPFn_DSTM_ADDR_C1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DSTM_ ADDR_C1 [31:0]	H'0000 0000	R/W	Destination Image C Plane Storing Address 1 These bits specify in 1-byte units the address for storing the Cr plane when the WPFn outputs images to the external memory in YCbCr planar format shown in Table 25.24. Refer to the description of VI6_WPFn_DSTM_ADDR_Y for settings. This setting is not used when the WPF outputs in YCbCr format that is not a planar format or in an RGB format. A value from H'00000000 to H'FFFFFFFF can be specified. Refer to Figure 25.32 in section 25.2.8.9 for settings.

25.2.8.12 WPF0 LIF Write Back Control Registers (VI6_WPF0_WRBCK_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	WBMD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	WBMD[1:0]	00	R/W	Display Data Write Back Control This bit is used for selecting the write back mode when the value of VI6_LIF_CTRL.LIF_EN bit is set to 1. 00: Write Back Disabled 01: Write Back Enabled

25.2.9 DPR Control Registers

25.2.9.1 Concept of DPR Settings

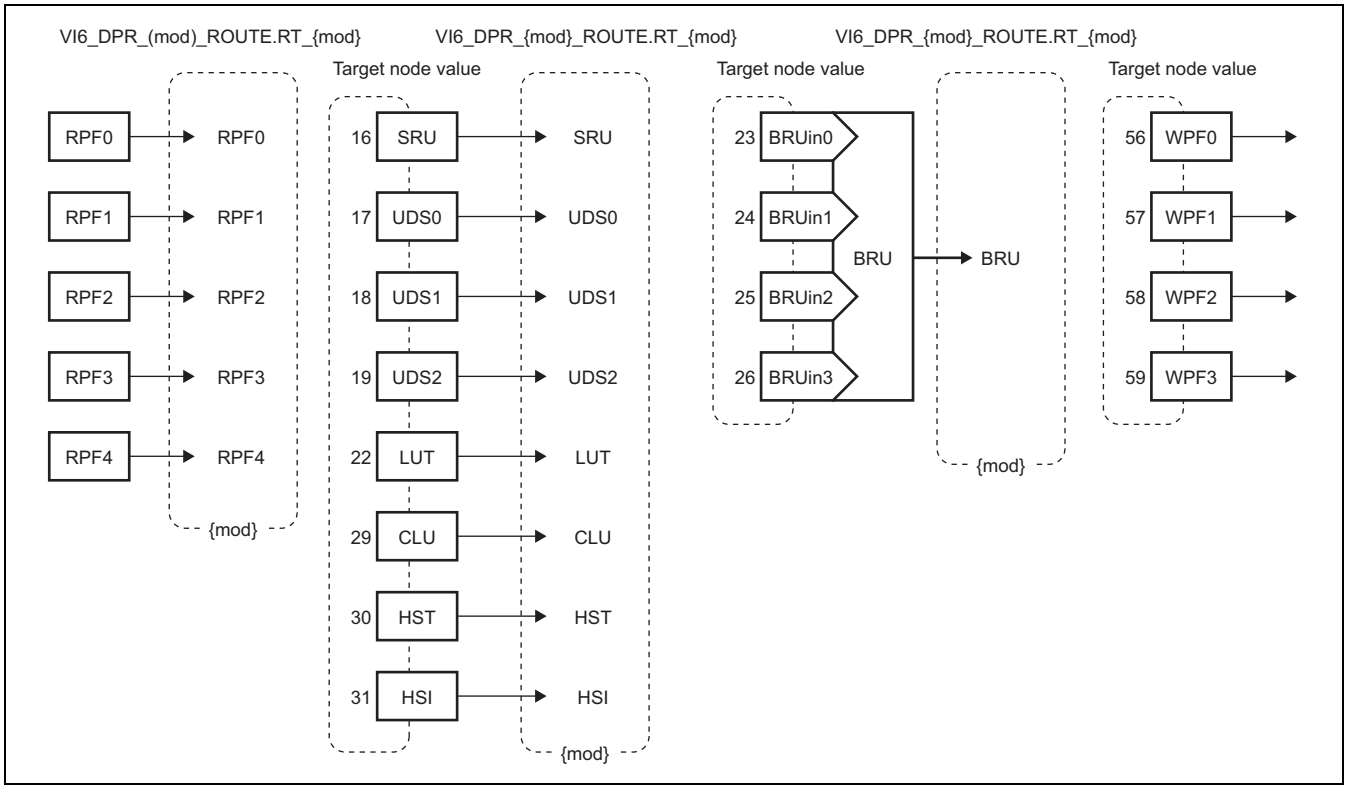


Figure 25.33 Node Register Names and Target Node Values on Data Path Router

In the VSP1 internal data path, the order of processes can be specified as desired. The module for performing each process has a unique node value. Set each bit field in VI6_DPR_*_ROUTE to an appropriate node value shown in Figure 25.33 to specify the target node to be connected behind each module.

For DPR settings, all of the following restrictions should be observed. If any of them is violated, even the WPF paths operating correctly at that time will be affected as well as the WPF paths connected through the DPR, and correct operation will not be guaranteed (for example, if a restriction is violated for the DPR setting related to WPF2, even WPF0 and WPF1 that are operating correctly will be affected).

1. Specify 63 for the output node values of all RPFs and processing modules that are not used in the DPR. Here, make sure that no module is connected to a module for which 63 is specified as the node value.
2. When specifying a value other than 63 for an output node value in the DPR, make sure that valid inputs (RPF0 to RPF4 or virtual RPF) and a target WPF are determined.
3. When a certain module is not implemented due to the LSI-specific restrictions described in Table 25.1 to Table 25.2, specify 63 for the corresponding VI6_DPR_*_ROUTE.RT_*.
4. Only one module can be connected to each module; specifying the same target node value for two or more modules is prohibited.
5. Desired modules can be connected between each RPF and BRU input port, but all RPFs specified as the sources for a BRU input port should have the same target WPF.
6. Make appropriate routing or RPF register settings so that the color space formats (RGB/YCbCr) for all BRU input ports are the same.
7. Connect data paths appropriately so that each of UDS0 to UDS2 is used only once throughout all paths from RPFn (n = 0 to 4) to WPFn (n = 0 to 3). Connecting UDS0 to UDS2 in serial is prohibited even when there is another module between them.

8. When the BRU is connected between RPFn and WPFn, any of UDS0 to UDS2 can be connected in parallel with each path from RPFn to BRU input ports 0 to 3. Note that when any of UDS0 to UDS2 is connected before BRU input ports 0 to 3, UDS0 to UDS2 cannot be used behind the BRU. In such a parallel UDS connection, the performance may be degraded. For details, contact a Renesas Electronics sales representative.
9. Do not connect the output of any module as the input to the same module (in the BRU case, any input port) even when there is another module between the output and input (creating a loop is prohibited).
10. Each node can be used only once throughout all paths from RPFn to WPFn. When a module shown in Figure 25.33 is assigned in one RPF → WPF path, it cannot be used in another RPF → WPF path.
11. While a WPF is operating, modifying the DPR connection settings in VI6_DPR_*_ROUTE is prohibited for modules used by the WPF but allowed for modules not used by the WPF. Be careful not to accidentally modify the settings of the modules included in the WPF path that is operating.

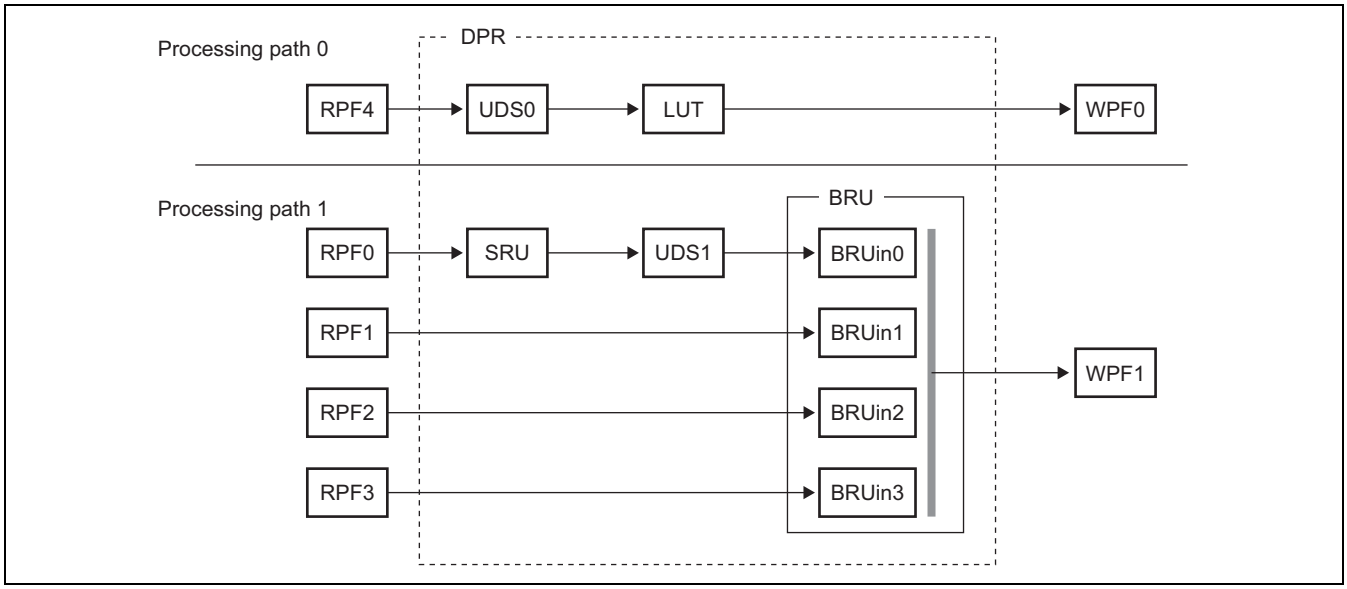


Figure 25.34 Examples of Internal Data Path Routing

Figure 25.34 shows examples of internal data path routing. Path 0 is assigned to WPF0 (RPF4 is the source RPF), and path 1 is assigned to WPF1 (RPF0 to RPF3 are the source RPFs). Each path has the configuration shown in Figure 25.34. Path 0 performs UDS and LUT processing (e.g., up/down scaling and γ correction). Path 1 performs super resolution processing and scaling for input 0 (RPF0) and then applies blending or raster operation between the resultant data and input data 1 to 3 (RPF1 to RPF3). The VI6_ DPR_*_ROUTE settings for these examples are shown in Table 25.26. The bit fields for the modules that are not used in the examples should be set to 63.

Table 25.26 VI6_DPR_*_ROUTE Register Settings in Connection Examples Shown in Figure 25.34

Register Name	Setting	
VI6_DPR_RPF0_ROUTE	16	(To SRU)
VI6_DPR_RPF1_ROUTE	24	(To BRUin1)
VI6_DPR_RPF2_ROUTE	25	(To BRUin2)
VI6_DPR_RPF3_ROUTE	26	(To BRUin3)
VI6_DPR_RPF4_ROUTE	17	(To UDS0)
VI6_DPR_SRU_ROUTE	18	(To UDS1)
VI6_DPR_UDS0_ROUTE	22	(To LUT)
VI6_DPR_UDS1_ROUTE	23	(To BRUin0)
VI6_DPR_UDS2_ROUTE	63	(UNUSED)
VI6_DPR_LUT_ROUTE	56	(To WPF0)
VI6_DPR_CLU_ROUTE	63	(UNUSED)
VI6_DPR_HST_ROUTE	63	(UNUSED)
VI6_DPR_HSI_ROUTE	63	(UNUSED)
VI6_DPR_BRU_ROUTE	57	(To WPF1)

Although both examples shown in Figure 25.34 include operation in image processing modules, connect the RPF to the WPF directly when only image format conversion or packed format conversion is required.

25.2.9.2 RPFn Routing Register (VI6_DPR_RPFn_ROUTE: n = 0, 1, 2, 3, 4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	RT_RPFn[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	RT_RPFn [5:0]	H'00	R/W	RPFn Target Node Value These bits specify the target node value for RPFn. When using RPFn, refer to Figure 25.33 for settings. When RPFn is not started through the VI6_WPFn_SRCRPF setting, specify 63.

25.2.9.3 WPFn Timing Control Register (VI6_DPR_WPFn_FPORCH: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FP_WPFn[5:0]						—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	FP_WPFn [5:0]	H'00	R/W	WPFn Internal Operation Timing Setting Specify 5.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

25.2.9.4 {mod} Routing Register (VI6_DPR_{mod}_ROUTE: {mod} = SRU, UDSn, LUT, CLU, HST, HSI, BRU)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	FXA[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FP[5:0]						—	—	RT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	FXA[7:0]	H'00	R/W	Fixed α Output Value for {mod} The {mod} does not support input/output of the α value. The α value input to the {mod} is discarded, and the fixed α value specified in these bits is always output from the {mod}. A value from 0 to 255 can be specified. These bits are valid for SRU, LUT, CLU, HST and HSI modules. For UDSn, and BRU modules, these bits are reserved.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 8	FP[5:0]	H'00	R/W	{mod} Internal Operation Timing Setting Specify 0.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	RT[5:0]	H'00	R/W	{mod}Target Node Value These bits specify the target node value for the {mod}. When using the {mod}, refer to Figure 25.33 for settings. When not using the {mod}, specify 63.

25.2.9.5 {mod} Sampling Point Register (VI6_DPR_{mod}_SMPPT: {mod} = HGO, HGT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TGW[2:0]			—	—	PT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	TGW[2:0]	000	R/W	Target WPF Index for {mod} These bits are used for specifying the target WPF index of {mod}. If {mod} is not used, set B'111 to these bits.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5 to 0	PT[5:0]	H'00	R/W	Target Node Index for {mod} Histogram Sampling {mod} generates the histogram for the target node specified by these bits. For example, if these bits are set to 0, {mod} module generates the histogram for the output data of RPF0. Refer to Table 25.27 for the target node index which can be used for {mod}. If {mod} is not used, set 63 to these bits.

Table 25.27 Target Node Index for {mod} Module

Node Index	Module for Histogram Generation
0 to 4	RPF0 to 4
16	SRU
17 to 19	UDS0 to 2
22	LUT
27	BRU
29	CLU
30	HST
31	HSI
55	LIF*

Note: * Do not set the value 55 to PT in case of LIF write back is used (i.e. VI6_WPF0_WRBACK_CTRL.WBMD [1:0] = 1).

25.2.10 SRU Control Registers

25.2.10.1 Super Resolution Control Register 0 (VI6_SRU_CTRL0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	SRU_PARAM0[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	SRU_PARAM1[4:0]					—	SRU_MODE[2:0]			SRU_ PARAM2	SRU_ PARAM3	SRU_ PARAM4	SRU_ EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SRU_PARAM0 [8:0]	H'000	R/W	Super Resolution Parameter 0 Specify an appropriate value shown in Table 25.28; do not specify any other value.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	SRU_PARAM1 [4:0]	00000	R/W	Super Resolution Parameter 1 Specify an appropriate value shown in Table 25.28; do not specify any other value.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	SRU_MODE [2:0]	000	R/W	Super Resolution Mode Setting These bits specify a super resolution mode. In super resolution without scaling, the output size is the same as the input size. In super resolution with double scale-up, the output size is twice the input size. 000: Super resolution without scaling 100: Super resolution with double scale-up Other settings are prohibited.
3	SRU_PARAM2	0	R/W	Super Resolution Parameter 2 This parameter setting depends on the color space of the image input to the SRU. Specify an appropriate value shown in Table 25.29; do not specify any other value.
2	SRU_PARAM3	0	R/W	Super Resolution Parameter 3 Specify an appropriate value shown in Table 25.29; do not specify any other value.
1	SRU_PARAM4	0	R/W	Super Resolution Parameter 4 This parameter setting depends on the color space of the image input to the SRU. Specify an appropriate value shown in Table 25.29; do not specify any other value.

Bit	Bit Name	Initial Value	R/W	Description
0	SRU_EN	0	R/W	Super Resolution Processing Enable/Disable Enables or disables super resolution processing. This setting has the highest priority over all other SRU registers. 0: Super resolution processing is disabled (input goes through the SRU without change) 1: Super resolution processing is enabled

YCbCr format is recommended for the super resolution processing. If the super resolution processing is applied to an RGB-format image, adverse effects such as color blur may be generated; when using an RGB format, evaluate the image quality carefully before applying the processing to practical use.

To execute the super resolution processing in YCbCr format, set up the RPF and DPR appropriately so that YCbCr-format image data is input to the SRU. Specifically, make the RPFn output YCbCr-format image data and send the output data to the SRU through the DPR. For details of RPFn input/output settings, refer to section 25.2.7.3. For DPR settings, refer to sections 25.2.9.1 to 25.2.9.4.

Table 25.28 Super Resolution Parameter Setting 1

		VI6_SRU_CTRL0			VI6_SRU_CTRL1	VI6_SRU_CTRL2		
Intensity		SRU _MODE	SRU _PARAM0	SRU _PARAM1	SRU _PARAM5	SRU _PARAM6	SRU _PARAM7	SRU _PARAM8
Weak	1	0 or 4	256	4	H'7FF	24	40	255
	2	0 or 4	256	4	H'7FF	8	16	255
	3	0 or 4	384	5	H'7FF	36	60	255
	4	0 or 4	384	5	H'7FF	12	27	255
	5	0 or 4	511	6	H'7FF	48	80	255
Strong	6	0 or 4	511	6	H'7FF	16	36	255

Table 25.29 Super Resolution Parameter Setting 2

Color Space of SRU Input Image	SRU_PARAM2	SRU_PARAM3	SRU_PARAM4
YCbCr*	0	1	0
RGB	1	1	1

Note: * YCbCr format is recommended for the image input to the SRU.

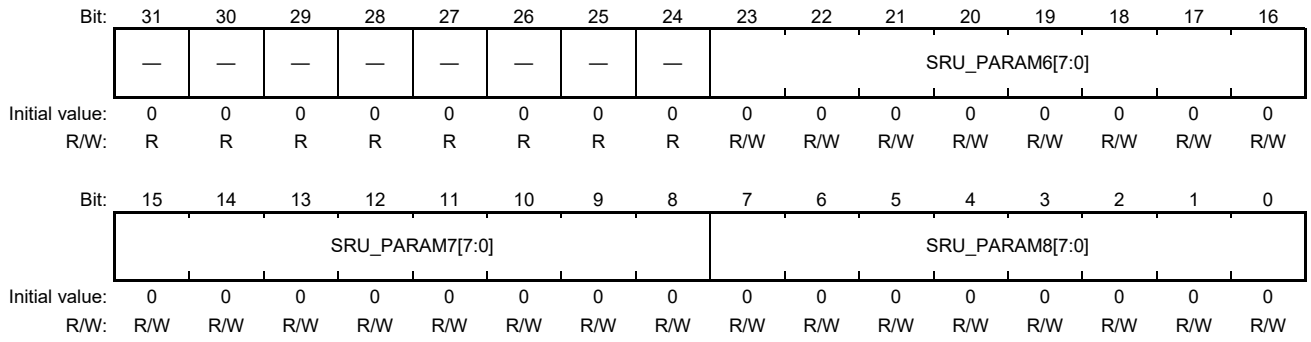
25.2.10.2 Super Resolution Control Register 1 (VI6_SRU_CTRL1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SRU_PARAM5[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	SRU_PARAM5 [10:0]	H'000	R/W	Super Resolution Parameter 5 Specify an appropriate value shown in Table 25.28; do not specify any other value.

25.2.10.3 Super Resolution Control Register 2 (VI6_SRU_CTRL2)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	SRU_PARAM6 [7:0]	H'00	R/W	Super Resolution Parameter 6 Specify an appropriate value shown in Table 25.28; do not specify any other value.
15 to 8	SRU_PARAM7 [7:0]	H'00	R/W	Super Resolution Parameter 7 Specify an appropriate value shown in Table 25.28; do not specify any other value.
7 to 0	SRU_PARAM8 [7:0]	H'00	R/W	Super Resolution Parameter 8 Specify an appropriate value shown in Table 25.28; do not specify any other value.

25.2.11 UDS Control Registers

25.2.11.1 Scaling Control Registers (VI6_UDSn_CTRL)

Note: n = 0 for this product.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	AMD	FMD	BLADV	—	—	AON	ATHON	—	—	—	BC	NE_A	NE_RCR	NE_GY	NE_BCB
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TDIPC	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	AMD	0	R/W	Pixel Count at Scale-Up Specifies the number of pixels generated through scale-up in the UDS. This bit setting is ignored for scale-down. 0: Pixel count after scale-up is 1 + ⟨(n – 1) × scale-up factor⟩ 1: Pixel count after scale-up is ⟨n × scale-up factor⟩ Note: n: Number of pixels input to UDS
29	FMD	0	R/W	Padding for Insufficient Clipping Size When the scaling filter outputs an image that is smaller than the clipping size (VI6_UDSn_CLIP_SIZE), pixels are interpolated to match the clipping size. This bit specifies the pixel filling method. 0: Pixels are filled by copying pixels at the right edge and the bottom edge. 1: Pixels are filled with the color specified by VI6_UDSn_FILL_COLOR.
28	BLADV	0	R/W	Bilinear or Nearest Neighbor Interpolation Characteristic Control Controls the characteristics of bilinear or nearest neighbor interpolation. Setting this bit to 1 improves the aliasing characteristics at × 1/2 to 1/8 scaling (VI6_UDS_SCALE.VMANT/HMANT = 2 to 8). Note that the apparent resolution around edges may deteriorate. In multi-tap mode, this control is not available; to use this control, set the BC bit to 0.
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	AON	0	R/W	Scale-Up/Down of α Plane These bits specify whether to enable or disable scale-up/-down of the α plane when scaling up/down in the RGB format. When the AON bit is set to 0, the UDS outputs the value of the VI6_UDSn_ALPVAL. ALPH_VAL0 bits as a fixed α value. 0: α scale-up/-down is not performed 1: α scale-up/-down is performed

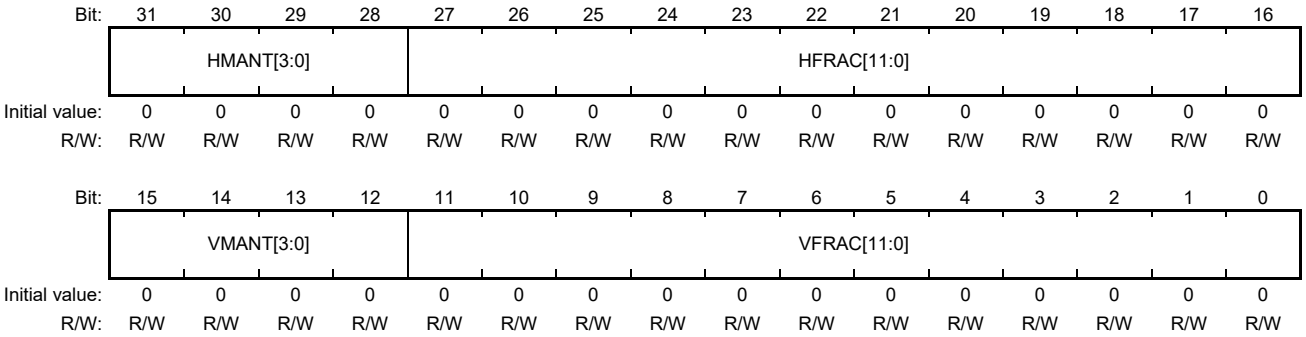
Bit	Bit Name	Initial Value	R/W	Description
24	ATHON	0	R/W	α Output Data Threshold Comparison Enable/Disable Enables or disables comparison with the α output data threshold. When this bit is 1, the output α value is replaced according to the VI6_UDSn_ALPTH and VI6_UDSn_ALPVAL values. When the AON bit is 0 (scale-up/-down of the α plane is disabled), this bit setting has no effect. 0: α output data threshold comparison is disabled 1: α output data threshold comparison is enabled
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	BC	0	R/W	Pixel Component Interpolation Method at Scale-Up/Down Specifies the method for interpolating pixel components at scale-up/-down. 0: Bilinear or nearest neighbor interpolation method is used 1: Interpolation method equivalent to 4 to 17 taps in accordance with the scaling factor is used (multi-tap mode) Note that the α component is interpolated by the method specified in the NE_A bit instead of the multi-tap method. When the BC and AON bits are both set to 1, the scaling shall be scale-up, no scaling, or scale-down with scaling factor 1/1 to 1/2.
19	NE_A	0	R/W	α Interpolation Method Specifies the interpolation method of the α plane. When the AON bit is 0 (scale-up/-down of the α plane is disabled), this bit setting has no effect. 0: Bilinear method 1: Nearest neighbor method*
18	NE_RCR	0	R/W	R/Cr Interpolation Method When Bilinear/Nearest Neighbor Interpolation is Selected Specifies the interpolation method of the R/Cr component when bilinear/nearest neighbor interpolation is selected (BC = 0). 0: Bilinear method 1: Nearest neighbor method*
17	NE_GY	0	R/W	G/Y Interpolation Method When Bilinear/Nearest Neighbor Interpolation is Selected Specifies the interpolation method of the G/Y component when bilinear/nearest neighbor interpolation is selected (BC = 0). 0: Bilinear method 1: Nearest neighbor method*
16	NE_BCB	0	R/W	B/Cb Interpolation Method When Bilinear/Nearest Neighbor Interpolation is Selected Specifies the interpolation method of the B/Cb component when bilinear/nearest neighbor interpolation is selected (BC = 0). 0: Bilinear method 1: Nearest neighbor method*
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	TDIPC	0	R/W	2D-IPC function Enable/Disable Select 0: 2D IPC function Disable 1: 2D IPC function Enable UDSn execute 2D IPC function based on this bit and the setting of VI6_UDSn_IPC register. See section 25.2.11.6, 2D IPC Setting Register (VI6_UDSn_IPC) for more details.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Note: * This method can be used only when the scale-up/-down factor is 1/1 to 1/4.

25.2.11.2 Scaling Factor Registers (VI6_UDSn_SCALE)

Note: n = 0 for this product.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	HMANT[3:0]	H'0	R/W	Multiplier (Integral Part) of Horizontal Scaling Factor These bits specify the integral part of the horizontal scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size. A value from H'0 to H'F can be specified. Select a value within the range shown in Table 25.30.
27 to 16	HFRAC[11:0]	H'000	R/W	Multiplier (Fractional Part) of Horizontal Scaling Factor These bits specify the fractional part of the horizontal scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size. A value from H'100 to H'FFF can be specified when an image is upscaled (the HMANT value is 0) in the horizontal direction. A value from H'000 to H'FFF can be specified when an image is downscaled (the HMANT value is not 0) in the horizontal direction. Select a value within the range shown in Table 25.30.
15 to 12	VMANT[3:0]	H'0	R/W	Multiplier (Integral Part) of Vertical Scaling Factor These bits specify the integral part of the vertical scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size. A value from H'0 to H'F can be specified. Select a value within the range shown in Table 25.30.
11 to 0	VFRAC[11:0]	H'000	R/W	Multiplier (Fractional Part) of Vertical Scaling Factor These bits specify the fractional part of the vertical scaling factor. The image size to be obtained changes according to this setting. Calculate an appropriate value using the formula shown later to obtain a desired image size. A value from H'100 to H'FFF can be specified when an image is upscaled (the VMANT value is 0) in the vertical direction. A value from H'000 to H'FFF can be specified when an image is downscaled (the VMANT value is not 0) in the vertical direction. Select a value within the range shown in Table 25.30.

The HMANT and HFRAC bits set the scale-up/-down factor for an image in the horizontal direction, and the VMANT and VFRAC bits set the scale-up/-down factor for an image in the vertical direction. The UDS operation switches between horizontal scale-up and horizontal scale-down according to the HMANT and HFRAC bit settings, as shown in

Table 25.30. (Setting a value outside the ranges of Table 25.30 in UDS operation is prohibited). Table 25.30 is for the horizontal direction, but it is similar for the vertical direction. In this case, replace HMANT with VMANT and HFRAC with VFRAC when reading.

Note that settings for scaling in the horizontal direction and settings for scaling in the vertical direction can be made independently. Therefore, a setting for scale-up in the horizontal direction and scale-down in the vertical direction is possible. In such a case, because the formula (described later) for obtaining the image size after scale-up/-down is different between scale-up and scale-down, a formula matching the scale-up or scale-down operation should be selected independently for the horizontal direction and vertical direction.

Table 25.30 Switching of Horizontal Scale-Up/Down Operation According to HMANT and HFRAC Bit Settings

HMANT	HFRAC	UDS Operation
H'0	H'100 to H'FFF	Scale-up
H'1	H'000	Same size (no scale-up/-down)
	H'001 to H'FFF	Scale-down
H'2 to H'F	H'000 to H'FFF	

Described here is the method for calculating the size of the upscaled/downscaled image that was obtained based on this register setting. First, define the variables necessary for calculating the horizontal size of the upscaled/downscaled image, as shown below.

$$hscale = \frac{4096}{4096 \times m_h + f_h}$$

m_h is the value of VI6_UDSn_SCALE.HMANT, and f_h is the value of VI6_UDSn_SCALE.HFRAC. This formula expresses the estimate of the scale-up/-down factor processed by the UDS. If the horizontal size of the image before scale-up/-down is set as $hsize_{org}$, the horizontal size of the image after scale-up/-down can be roughly obtained through $hsize_{org} \times hscale$.

Similarly, define the variables necessary for calculating the vertical size of the upscaled/downscaled image.

$$vscale = \frac{4096}{4096 \times m_v + f_v}$$

When setting m_v as the value of VI6_UDSn_SCALE.VMANT , f_v as the value of VI6_UDSn_SCALE.VFRAC, and $vsize_{org}$ as the vertical size of the image before scale-up/-down, the vertical size of the image after scale-up/-down can be roughly obtained through $vsize_{org} \times vscale$.

When the UDSn performs scale-down with the settings of Table 25.30, using the variables defined so far, the horizontal size of the downscaled image $hsize_{down\_scaled}$ and the vertical size of the downscaled image $vsize_{down\_scaled}$ become as follows:

$$hsize_{down\_scaled} = \left\langle 1 + \left(\left\langle 1 + \frac{\langle hsize_{org} - 1 \rangle}{m_h'} \right\rangle - 1 \right) \times m_h' \times hscale \right\rangle$$

$$vsize_{down\_scaled} = \left\langle 1 + \left(\left\langle 1 + \frac{\langle vsize_{org} - 1 \rangle}{m_v'} \right\rangle - 1 \right) \times m_v' \times vscale \right\rangle$$

Since the division of hscale and vscale has to be executed at the end of the above formulas, respectively, formulas considering the order of operation become as follows:

$$hsize_{down\_scaled} = \left\langle 1 + \left\{ \left(\left\langle 1 + \frac{\langle hsize_{org} - 1 \rangle}{m_h'} \right\rangle - 1 \right) \times m_h' \times 4096 \right\} \middle/ \left(4096 \times m_h + f_h \right) \right\rangle$$

$$vsize_{down\_scaled} = \left\langle 1 + \left\{ \left(\left\langle 1 + \frac{\langle vsize_{org} - 1 \rangle}{m_v'} \right\rangle - 1 \right) \times m_v' \times 4096 \right\} \middle/ \left(4096 \times m_v + f_v \right) \right\rangle$$

The value of m_h' or m_v', which is shown in Table 25.31, changes according to the setting of VI6_UDSn_SCALE.HMANT or VI6_UDSn_SCALE.VMANT.

Table 25.31 m_h' or m_v' Setting

VI6_UDSn_SCALE.HMANT Setting (VI6_UDSn_SCALE.VMANT Setting)	m_h' (m_v')
1 to 3	1
4 to 7	2
8 to 15	4

When the UDSn performs scale-up with the settings of Table 25.30 and VI6_UDSn_CTRL.AMD is 0, the horizontal size of the upscaled image $hsize_{up\_scaled}$ and the vertical size of the upscaled image $vsize_{up\_scaled}$ become as follows:

$$hsize_{up\_scaled} = \langle 1 + (hsize_{org} - 1) \times hscale \rangle$$

$$vsize_{up\_scaled} = \langle 1 + (vsize_{org} - 1) \times vscale \rangle$$

Similar to the scale-down case, formulas considering the division of hscale and vscale become as follows:

$$hsize_{up\_scaled} = \langle 1 + ((hsize_{org} - 1) \times 4096) / (4096 \times m_h + f_h) \rangle$$

$$vsize_{up\_scaled} = \langle 1 + ((vsize_{org} - 1) \times 4096) / (4096 \times m_v + f_v) \rangle$$

When VI6_UDSn_CTRL.AMD is 1, the horizontal size of the upscaled image $hsize_{up\_scaled}$ and the vertical size of the upscaled image $vsize_{up\_scaled}$ become as follows:

$$hsize_{up\_scaled} = \langle hsize_{org} \times hscale \rangle$$

$$vsize_{up\_scaled} = \langle vsize_{org} \times vscale \rangle$$

After considering the division of hscale and vscale, the formulas become as follows:

$$hsize_{up\_scaled} = \langle (hsize_{org} \times 4096) / (4096 \times m_h + f_h) \rangle$$

$$vsize_{up\_scaled} = \langle (vsize_{org} \times 4096) / (4096 \times m_v + f_v) \rangle$$

25.2.11.3 α Data Threshold Setting Registers (VI6_UDSn_ALPTH)

Note: n = 0 for this product.

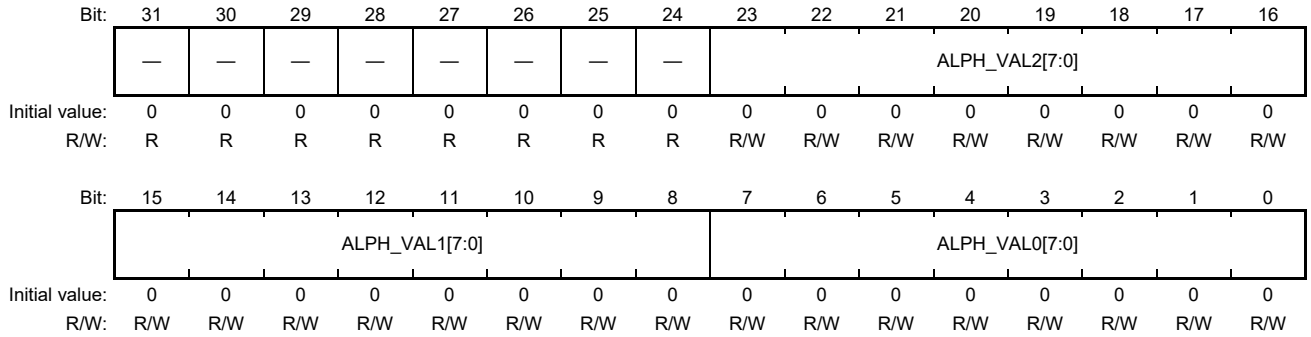
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ALPH_TH1[7:0]								ALPH_TH0[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	ALPH_TH1 [7:0]	H'00	R/W	α Data Threshold Setting 1 When the α value is equal to or greater than the value of the ALPH_TH1 bits, the α value is replaced with that of VI6_UDSn_ALPVAL.ALPH_VAL2. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the α plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.
7 to 0	ALPH_TH0 [7:0]	H'00	R/W	α Data Threshold Setting 0 When the α value is equal to or smaller than the value of the ALPH_TH0 bits, the α value is replaced with that of VI6_UDSn_ALPVAL.ALPH_VAL0. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the α plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.

25.2.11.4 α Data Replacing Value Setting Registers (VI6_UDSn_ALPVAL)

Note: n = 0 for this product.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	ALPH_VAL2 [7:0]	H'00	R/W	Replacing α Value Setting 2 These bits set a value that replaces the α value when it is equal to or greater than the value of VI6_UDSn_ALPTH.ALPH_TH1. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the α plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.
15 to 8	ALPH_VAL1 [7:0]	H'00	R/W	Replacing α Value Setting 1 These bits set a value that replaces the α value when it is greater than the value of VI6_UDSn_ALPTH.ALPH_TH0 and also smaller than that of VI6_UDSn_ALPTH.ALPH_TH1. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the α plane is disabled), the setting of these bits has no effect. A value from H'00 to H'FF can be specified.
7 to 0	ALPH_VAL0 [7:0]	H'00	R/W	Replacing α Value Setting 0 These bits set a value that replaces the α value when it is equal to or smaller than the value of VI6_UDSn_ALPTH.ALPH_TH0. When VI6_UDSn_CTRL.AON is 0 (scale-up/-down of the α plane is disabled), α output value for the UDS is the fixed value specified in these bits. A value from H'00 to H'FF can be specified.

25.2.11.5 Passband Registers (VI6_UDSn_PASS_BWIDTH)

Note: n = 0 for this product.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	BWIDTH_H[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	BWIDTH_V[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 16	BWIDTH_H [6:0]	H'00	R/W	Horizontal Signal Passband at Image Scale-Up/Down Set these bits following the method described later.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	BWIDTH_V [6:0]	H'00	R/W	Vertical Signal Passband at Image Scale-Up/Down Set these bits following the method described later.

The method for setting the passband in the horizontal direction of an image is described. When the VI6_UDSn_SCALE.HMANT bits for horizontal scale-up/-down factor setting are not 0, set the BWIDTH_H bits according to the following formula. When the VI6_UDSn_SCALE.HMANT bits are 0, set 64 in the BWIDTH_H bits.

$$BWIDTH\_H = \left\langle 64 \times \frac{4096 \times m_h'}{4096 \times m_h + f_h} \right\rangle \quad (\text{VI6\_UDSn\_SCALE.HMANT} \neq 0)$$

$$BWIDTH\_H = 64 \quad (\text{VI6\_UDSn\_SCALE.HMANT} = 0)$$

m_h is the value of VI6_UDSn_SCALE.HMANT, and f_h is the value of VI6_UDSn_SCALE.HFRAC. For the m_h' value, see Table 25.31. The method for setting the passband in the vertical direction of an image is similar to that for the horizontal direction described earlier. Since only the correspondence relationship of the registers is changed as shown below, replace the variables in the previous explanation as shown below when reading.

BWIDTH_H → BWIDTH_V
m_h' → m_v'
m_h → m_v
f_h → f_v
VI6_UDSn_SCALE.HMANT → VI6_UDSn_SCALE.VMANT
VI6_UDSn_SCALE.HFRAC → VI6_UDSn_SCALE.VFRAC

25.2.11.6 2D IPC Setting Register (VI6_UDSn_IPC)

Note: n = 0 for this product.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	FIELD	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	FIELD	0	R/W	Top/Bottom Field Select Select Top/Bottom Field of image data when 2D IPC function is enabled (VI6_UDSn_CTRL.TDIPC = 1). 0: Top Field 1: Bottom Field
26 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

1. Set 1 to VI6_UDSn_CTRL.TDIPC.
2. Set appropriate setting of processing image
   Top Field: H'0000 0000
   Bottom Field: H'0800 0000

Notes: 1. Recommend usage case: Frame rate after 2D UPC is more than 50 fps.
2. Be sure to set H'0000 0000 this register and set VI6_UDSn_CTRL.TDIPC

This register can be used for the image division mode or 2D interlace to progressive conversion (2D-IPC). When this register is not used, set VI6_UDSn_CTRL.TDIPC to 00. If the 2D-IPC mode is used, contact to Renesas for detail.

25.2.11.7 UDS Output Size Clipping Registers (VI6_UDSn_CLIP_SIZE)

Note: n = 0 for this product.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CL_HSIZE[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CL_VSIZE[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 16	CL_HSIZE [11:0]	H'000	R/W	Clipping Size of Horizontal Pixel Count after Scale-Up/-Down The horizontal width of an image output from the scaling filter is adjusted (clipped or padded) to match the pixel count set in the CL_HSIZE bits. The setting range is 4 to 2,048 in a scale-down operation (see Table 25.30) and 4 to 2,048 in a scale-up operation. These bits always have to be set when using the UDSn, regardless of the scale-up, scale-down, or no-scaling setting by the VI6_UDSn_SCALE register.
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 0	CL_VSIZE [11:0]	H'000	R/W	Clipping Size of Vertical Pixel Count after Scale-Up/-Down The vertical width of an image output from the scaling filter is adjusted (clipped or padded) to match the pixel count set in the CL_VSIZE bits. The setting range is 4 to 2,048 in a scale-down operation (see Table 25.30) and 4 to 2,048 in a scale-up operation. These bits always have to be set when using the UDSn, regardless of the scale-up, scale-down, or no-scaling setting by the VI6_UDSn_SCALE register.

Figure 25.35 shows the configuration of the UDSn. The UDSn consists of a scaling filter and clipping circuit, such as the configuration shown in Figure 25.35. The scaling filter and clipping circuit are independent of each other.

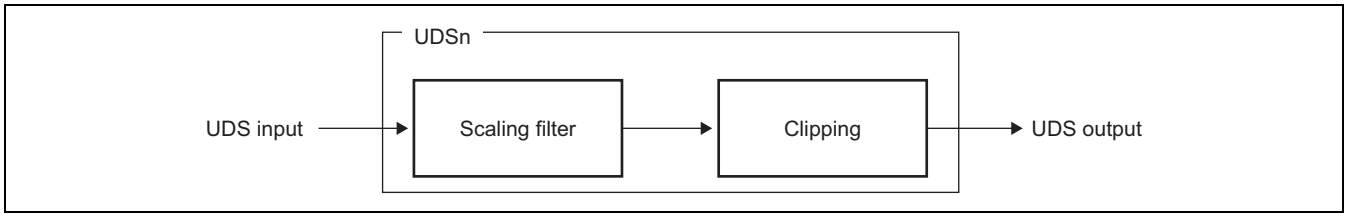


Figure 25.35 UDSn Configuration

The size of the image actually output by the scaling filter (refer to section 25.2.11.2 for calculation) is determined from the size of the image input to the scaling filter and the VI6_UDSn_SCALE setting; that is, three types of image are

output by the UDSn according to the relationship between the size of the image actually output from the scaling filter ($hsize_{scaled}$ and $vsize_{scaled}$) and this register setting as shown in Figure 25.36.

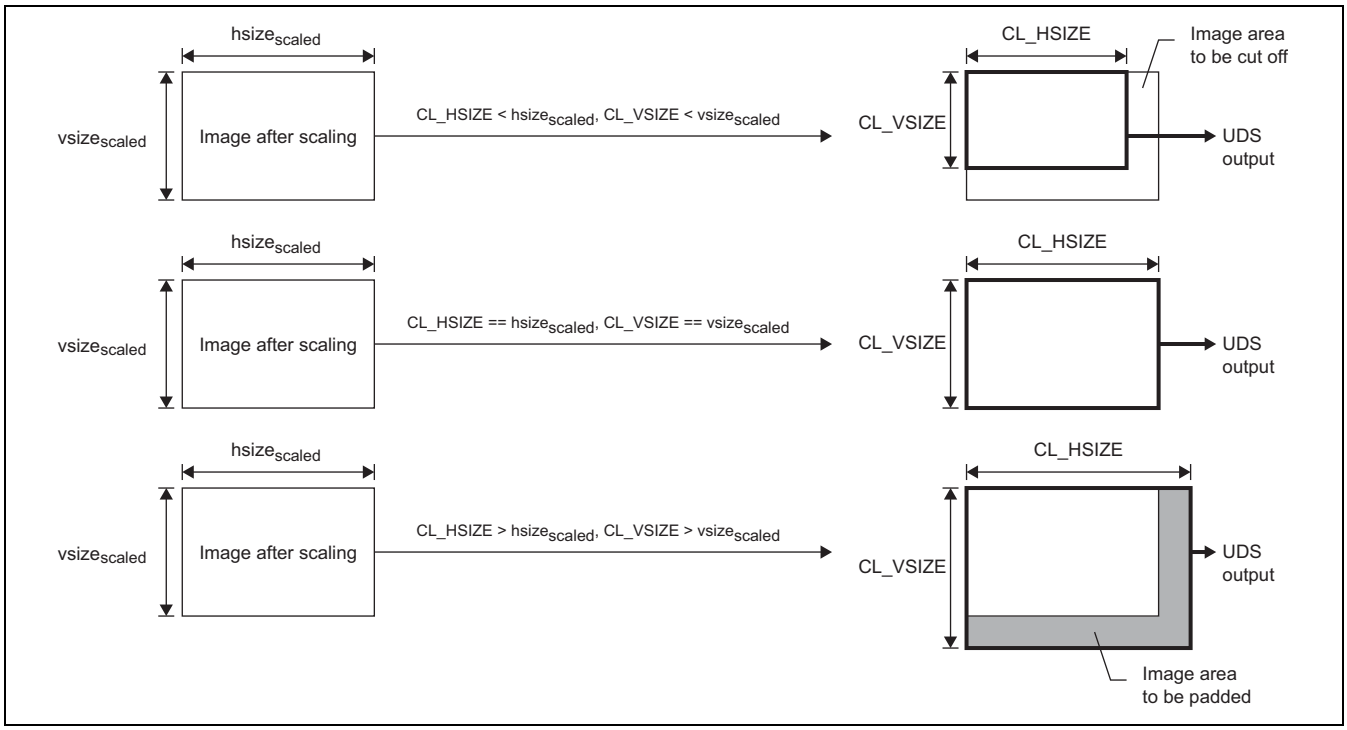


Figure 25.36 UDS Output Image for Each CL_HSIZE/VSIZE Setting

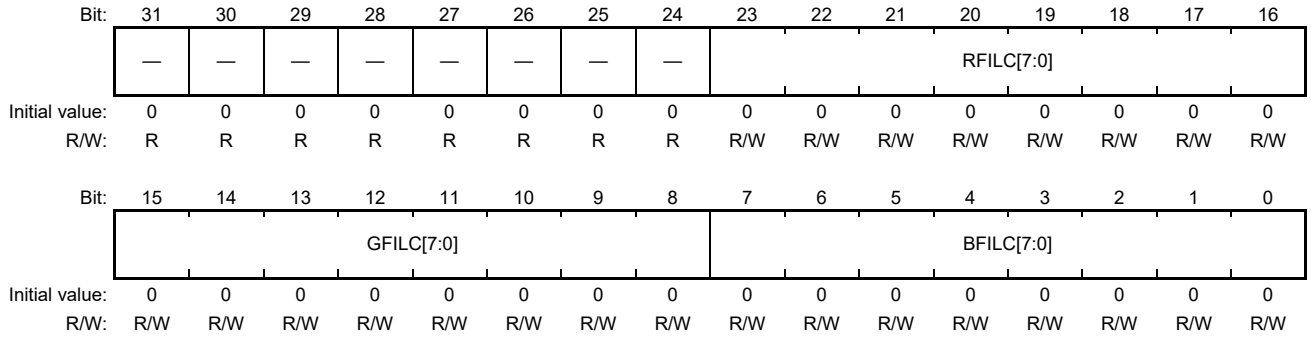
When the settings of the CL_HSIZE and CL_VSIZE bits are smaller than the horizontal and vertical pixel counts ($hsize_{scaled}$ and $vsize_{scaled}$) actually output by the scaling filter, the upscaled/downscaled image is clipped to become the UDSn output image.

When the settings of the CL_HSIZE and CL_VSIZE bits are equal to the horizontal and vertical pixel counts ($hsize_{scaled}$ and $vsize_{scaled}$) actually output by the scaling filter, the image actually output by the scaling filter becomes the UDSn output image without change.

When the settings of the CL_HSIZE and CL_VSIZE bits are greater than the horizontal and vertical pixel counts ($hsize_{scaled}$ and $vsize_{scaled}$) actually output by the scaling filter, in order to obtain the UDSn output image, the image is padded in the mode set by VI6_UDSn_CTRL.FMD for the area in which the settings of the CL_HSIZE and CL_VSIZE bits have exceeded the number of pixels actually output by the scaling filter.

25.2.11.8 Color Fill Register (VI6_UDSn_FILL_COLOR)

Note: n = 0 for this product.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	RFILC[7:0]	H'00	R/W	R/Cr Component of Fill Color A value from H'00 to H'FF can be specified.
15 to 8	GFILC[7:0]	H'00	R/W	G/Y Component of Fill Color A value from H'00 to H'FF can be specified.
7 to 0	BFILC[7:0]	H'00	R/W	B/Cb Component of Fill Color A value from H'00 to H'FF can be specified.

The scaling filter creates an upscaled/downscaled image based on the scaling factor settings of the VI6_UDSn_SCALE register. If the size of the upscaled/downscaled image created by the scaling filter smaller than the clipping size set in the VI6_UDSn_CLIP_SIZE register (lowest case in Figure 25.36) while VI6_UDSn_CTRL.FMD is set to 1, the color specified by this register is used to fill the space until the clipping size is reached.

The α value of the area to be padded by this register is dependent on VI6_UDSn_CTRL.FMD setting. When VI6_UDSn_CTRL.FMD is 0 (repetition), the pixel value at the right edge (bottom edge) of the image is repeated as the α value. When VI6_UDSn_CTRL.FMD is 1 (color information of this register is used), the α value is 0.

25.2.12 LUT Control Register

25.2.12.1 LUT Control Register (VI6_LUT_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LUT_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	LUT_EN	0	R/W	1D-LUT Enable/Disable Enables or disables the 1D-LUT function by the LUT. When the 1D-LUT is used, the color component curve information needs to be set separately in the LUT table. For the LUT table settings, refer to section 25.2.1. 0: 1D-LUT function is disabled 1: 1D-LUT function is enabled

In the LUT, various image processing, such as curves with high operation load (e.g., γ correction), negative-positive conversion, and gain adjustment of images, can be achieved by the data replacement processing by the 1D-LUT. As shown in Figure 25.37, the LUT replaces each component of the input pixel data using the set replacement table of 256 entries. For example, if the LUT is set as in Figure 25.38, when there is an input of 150, the data stored in address 150 of the 1D-LUT is read and output as the LUT output. Figure 25.38 shows a case in which the input and output become equal for convenience in explaining.

In the LUT settings shown in Figure 25.39, the input bits are reversed. This has the effect of negative-positive flipping. In Figure 25.40, γ correction (γ = 1.8 is shown as an example) is possible. As described above, information to be set in the LUT indicates LUT processing characteristics. If the same value is set for each component in the LUT, an equal effect can be obtained for each component of the input image when it is processed. If the LUT is set with different characteristics for each component, the processing characteristics can be changed for each component.

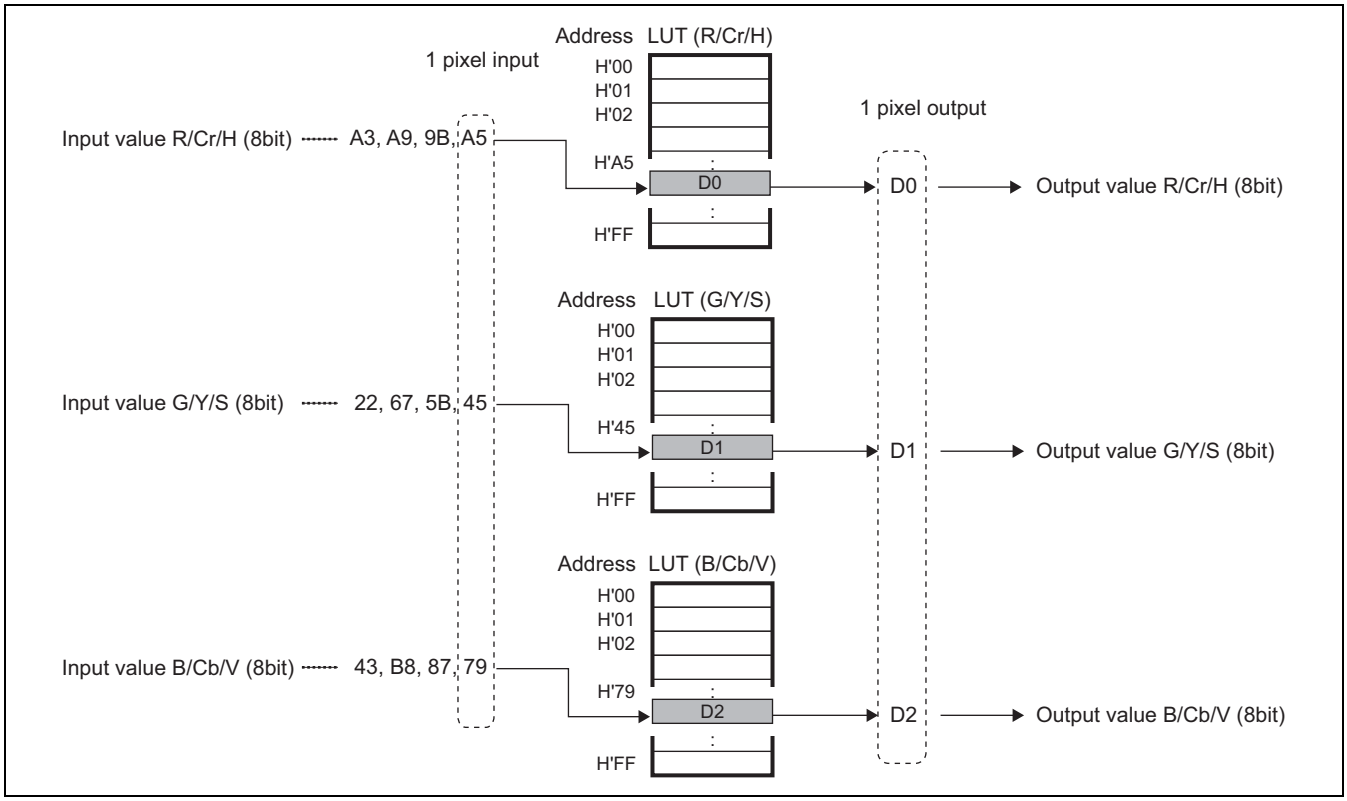


Figure 25.37 Relationship between Input and Output for 1D-LUT Table

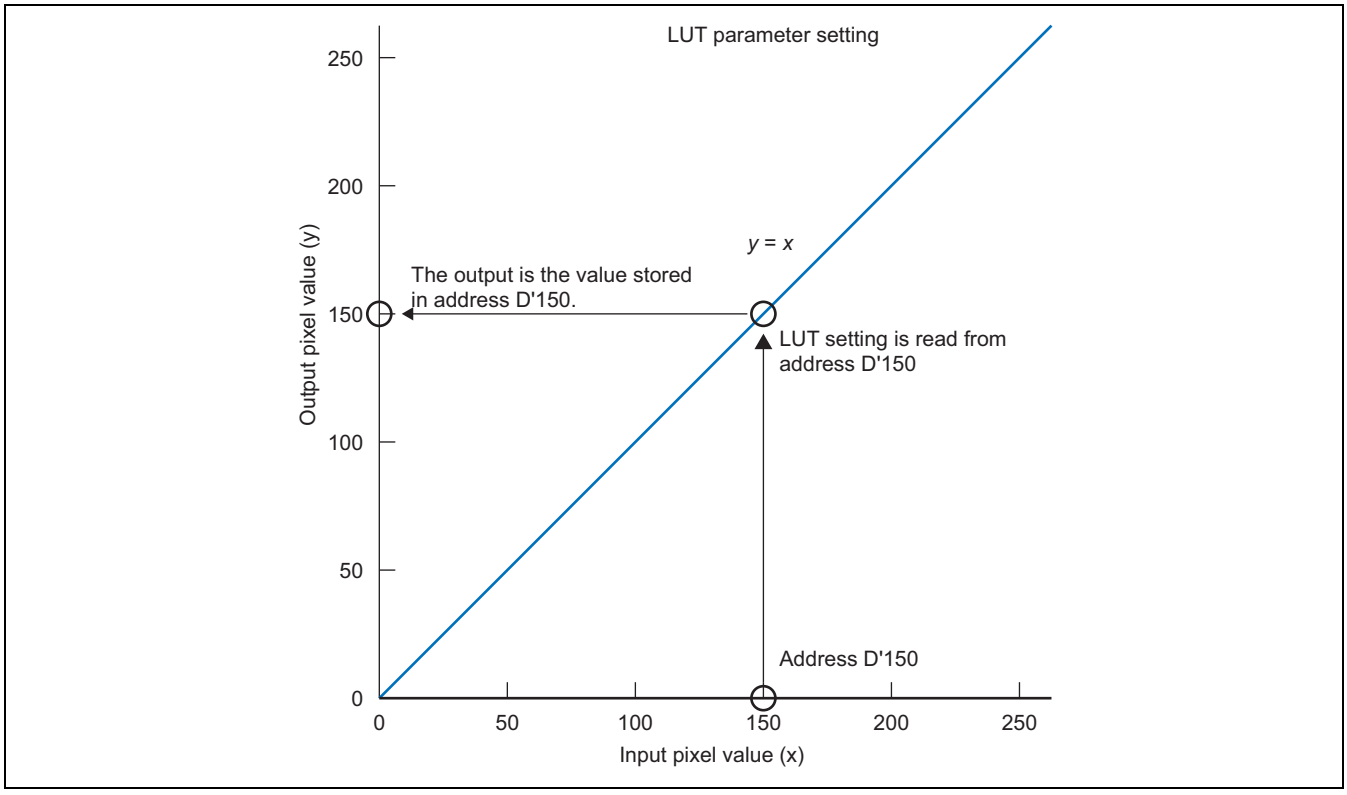


Figure 25.38 Setting Example in Which Output Becomes Equal to Input

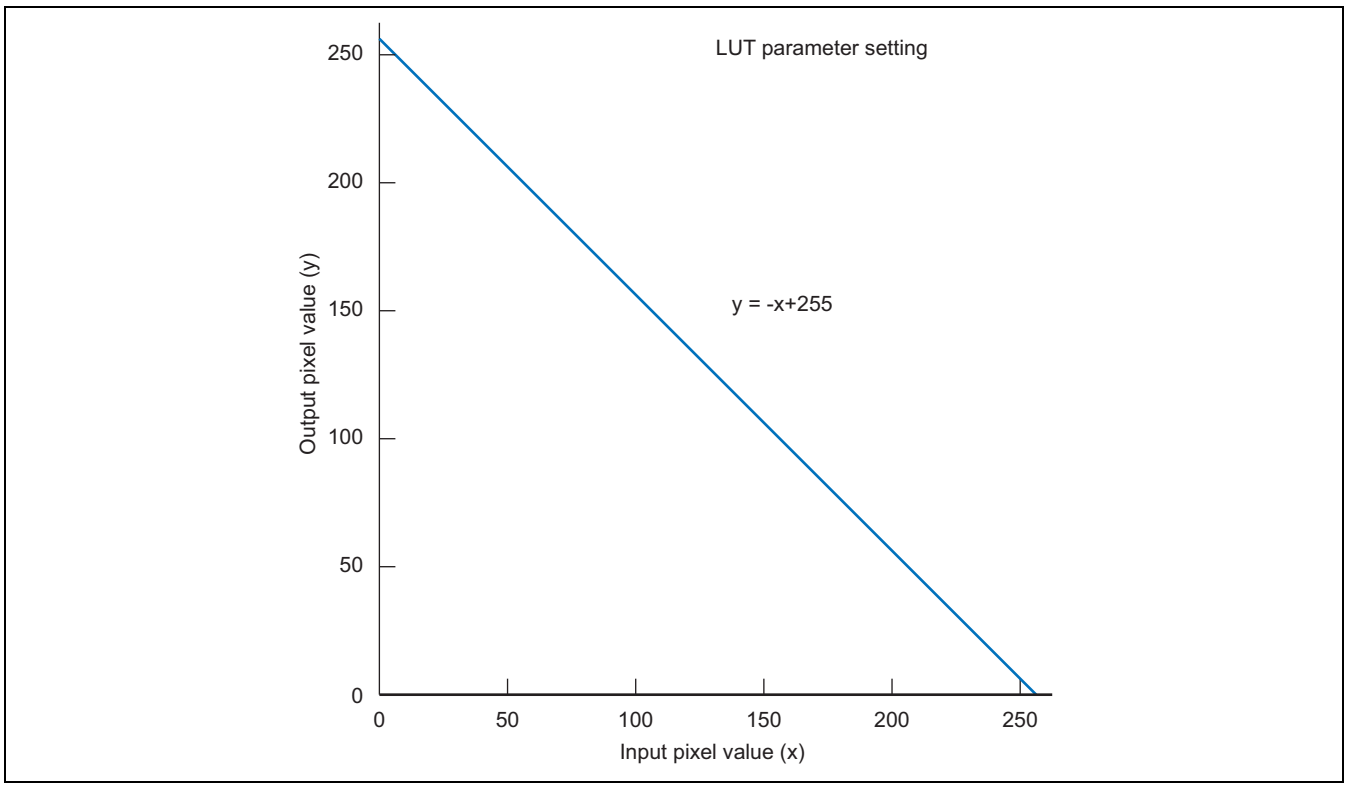


Figure 25.39 Setting Example of Negative-Positive Conversion

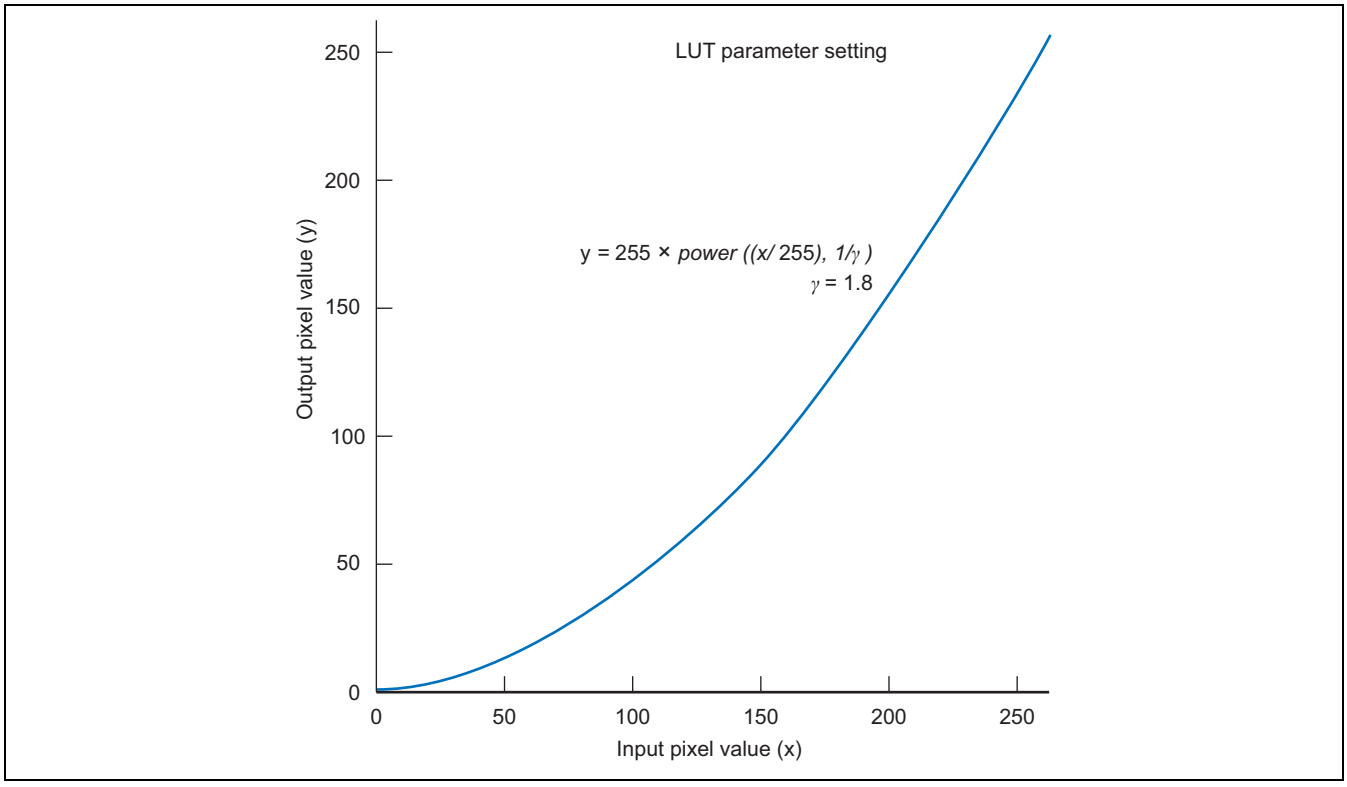


Figure 25.40 Setting Example of γ Correction

25.2.13 CLU Control Register

25.2.13.1 CLU Control Register (VI6_CLU_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	AAI	—	—	—	MVS	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AX1I[1:0]		AX2I[1:0]		—	—	OS0[1:0]		OS1[1:0]		OS2[1:0]		—	—	M2D	CLU_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	AAI	0	R/W	Automatic Table Address Increment Selects whether to specify the CLU table address in VI6_CLU_ADDR (refer to section 25.2.2) every time or update the address automatically. For details, refer to section 25.2.2. 0: CLU table address should be specified every time 1: CLU table address is automatically incremented
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	MVS	0	R/W	Max Value Stretch Select calculation method in max value region. 0: Method 0 (Lower compatible) 1: Method 1 (Improved characteristics)
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15, 14	AX1I[1:0]	00	R/W	Input Control 0 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 3.
13, 12	AX2I[1:0]	00	R/W	Input Control 1 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 1.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	OS0[1:0]	00	R/W	Output Control 0 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 3.
7, 6	OS1[1:0]	00	R/W	Output Control 1 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 1.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	OS2[1:0]	00	R/W	Output Control 2 in 2D Mode When setting the M2D bit to 0, be sure to set these bits to 0. When setting the M2D bit to 1, be sure to set these bits to 3.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	M2D	0	R/W	LUT Dimension Number Specifies the number of LUT dimensions. The details of each mode will be described later. 2D mode can be used only when the CLU input color space is YCbCr. 0: Operates in 3D mode 1: Operates in 2D mode
0	CLU_EN	0	R/W	CLU Processing Enable/Disable Enables or disables the 3D/2D color correction function by the CLU. When the CLU is used, the color component information needs to be set in the CLU table. For how to set data in the CLU table, see section 25.2.2. 0: CLU color correction is disabled 1: CLU color correction is enabled

The CLU handles three-dimensional or two-dimensional LUTs. A three-dimensional LUT is called a 3D-LUT and a two-dimensional LUT is called a 2D-LUT. The 3D or 2D operating mode of the CLU is selected by the M2D bit.

In 3D mode, a three-dimensional space such as that shown in Figure 25.41 (a) is considered. The total number of coordinate points that can exist in this three-dimensional space is the total number of combinations of input data. For the CLU, this becomes the cube of each 8-bit component (= 16,777,216 points). Since it is impractical to have table values (= table memory) for the same number of these coordinate points, the CLU divides the three-dimensional space of Figure 25.41 (a) into grids as shown in Figure 25.41 (b) in 3D mode. The apex in each divided grid is defined as the coordinate point in the three-dimensional space, and a table value with three component values is set for all of these coordinate points. The total number of coordinate points in Figure 25.41 (b) is 173 = 4,913. For the method of setting the table value for these 4,913 points, refer to section 25.2.2.

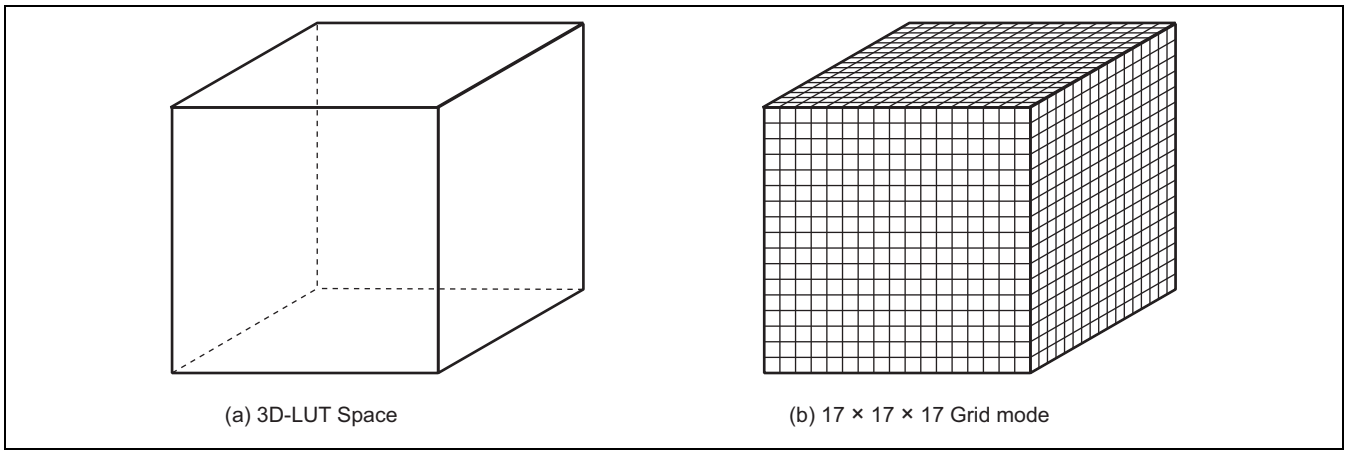


Figure 25.41 Concept and Division Count of a 3-Dimensional LUT

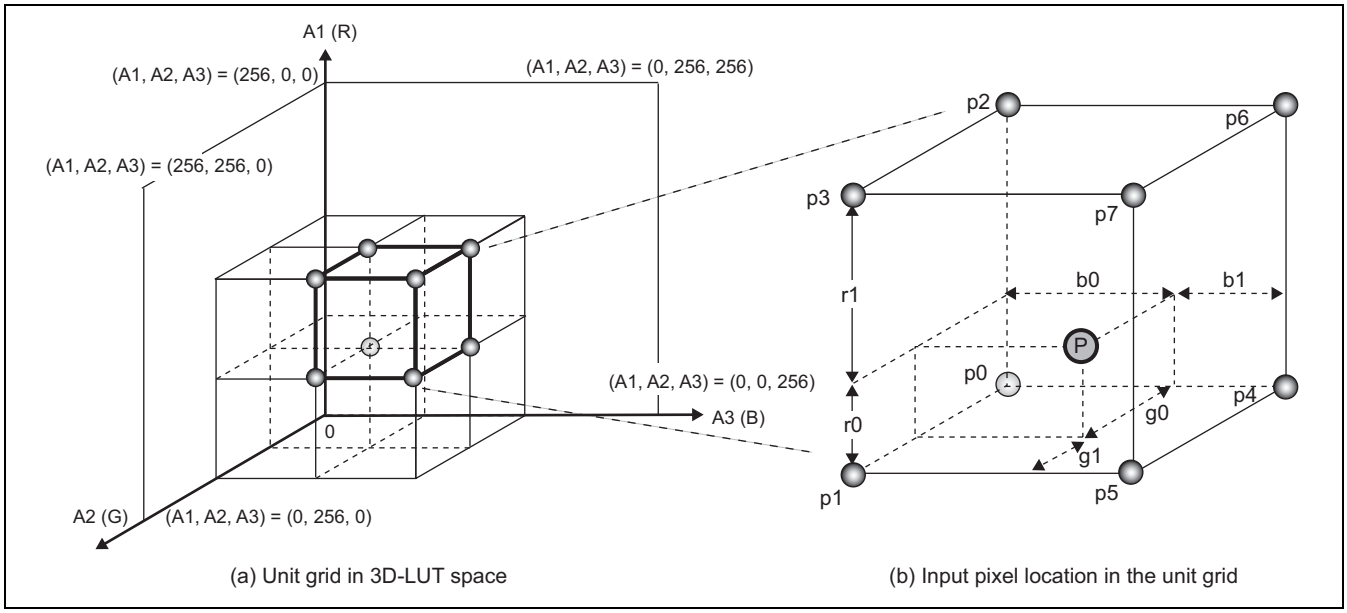


Figure 25.42 Conceptual Diagram of LUT Space When CLU Is in 3D Mode

To express a three-dimensional space such as that shown in Figure 25.41, consider the three-dimensional coordinates and axes shown in Figure 25.42 and define the minimum value and maximum value of each axis as 0 and 256, respectively. In 3D-LUT operation, the CLU forcibly assigns the four components of input data (α, R/Cr/H, G/Y/S, and B/Cb/V) to axes: R, Cr, and H components to the first axis (A1), G, Y, and S components to the second axis (A2), and B, Cb, and V components to the third axis (A3). (The case of 2D mode is described later.) Among multiple components assigned to each axis (e.g., R, Cr, and H components for the first axis), one component is selected according to the format of the data input to the CLU. For example, when the color space of the data input to the CLU is RGB, the first axis (A1) shows the R component, the second axis (A2) shows the G component, and the third axis (A3) shows the B component. In a YCbCr color space, the first axis (A1) shows the Cr component, the second axis (A2) shows the Y component, and the third axis (A3) shows the Cb component.

Each component value of the CLU input data becomes a value on each axis. Since the input data ranges from 0 to 255, the maximum value of 256 is handled as a virtual point in a grid space like that shown in Figure 25.41. In a case where the coordinates obtained by plotting the values of the input three components on axes are exactly on a grid point (e.g., p0 in Figure 25.42 (b)), the 3-component value of the table value (p0) set to that location becomes the CLU output. If the input value of the three components result in an intermediate location between grid points and not on a grid point, such as position P in Figure 25.42 (b), value P of the three components is interpolated from the table values (p0 to p7 in Figure 25.42 (b)) for the eight surrounding grid points and this is used as the CLU output.

By setting arbitrary table value for a three-dimensional LUT space (three-dimensional color space) such as that shown in Figure 25.41 using the processing described above, not only color conversion or color correction for the entire color space, but color conversion or color correction (memory color correction, skin smoothing, etc.) for a particular color area can be achieved.

Next, a 2D-LUT that is used when the CLU is operating in 2D mode is described (M2D bit should be set to 1 for operation in 2D mode). 2D-LUT mode is similar to 3D-LUT mode. However, since the axes for selecting the LUT become two-dimensional, the concept of a 3D-LUT space illustrated in Figure 25.42 changes to a 2D-LUT space like that shown in Figure 25.43.

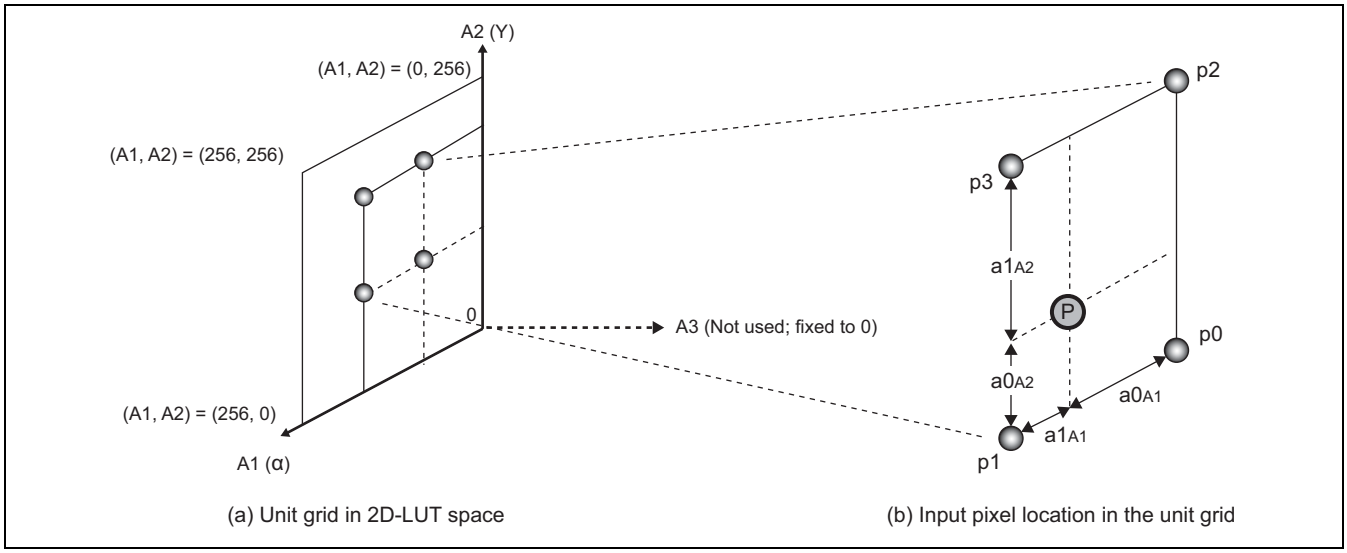


Figure 25.43 Conceptual Diagram of LUT Space when CLU is in 2D Mode

As shown in Figure 25.43 (a), the first axis (A1) and second axis (A2) are used, and the A1-A2 plane becomes the LUT space in 2D mode. Because the third axis (A3) is not used, the CLU always handles the value on the A3 axis as 0.

2D mode can be used only when the CLU input is in the YCbCr color space. The input value of axis A1 is the input α value of the CLU, and the input value of axis A2 is the input luminance Y of the CLU. If the coordinates in the 2D-LUT space which were determined by the input values are exactly on a grid point (e.g., p2 in Figure 25.43 (b)), the table value (p2) set to that location becomes the output value of the 2D-LUT. If the input 2-component value exists at an intermediate location between grid points and not on a grid point, such as position P in Figure 25.43 (b), value P is interpolated from the table values (p0 to p3 in Figure 25.43 (b)) for the four surrounding grid points and this is used as the 2D-LUT output. The interpolated component of the second axis of the 2D-LUT output acquired in this manner becomes the Y component output of the CLU. In 2D mode, the Cb/Cr component is a pass-through output.

For the CLU table values in Figure 25.43 in 2D mode, set a value for only the component value of the second axis, and set 0 for the component values of the first and third axes. For details on the setting method, see section 25.2.2.

25.2.14 HST Control Register

25.2.14.1 HST Control Register (VI6_HST_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HST_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	HST_EN	0	R/W	HSV Conversion (RGB → HSV) Enable/Disable Enables or disables RGB → HSV conversion. H indicates hue, S indicates saturation, and V indicates a value (brightness). 0: RGB → HSV conversion is disabled 1: RGB → HSV conversion is enabled

Various color correction processing can be applied to HSV-format images by combining the 1D-LUT and 3D-LUT. For details on the 1D-LUT and 3D-LUT, see sections 25.2.12.1 and 25.2.13.1.

To return HSV-converted data to RGB data, HSV → RGB conversion is used (see section 25.2.15.1). RGB ↔ HSV conversion causes an operation error. Therefore, even when only just performing conversion of RGB → HSV → RGB, the original RGB value and converted RGB value will not completely match.

25.2.15 HSI Control Register

25.2.15.1 HSI Control Register (VI6_HSI_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HSI_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	HSI_EN	0	R/W	Reversed HSV Conversion (HSV → RGB) Enable/Disable Enables or disables HSV → RGB conversion to return HSV data that was converted by HSV conversion (see section 25.2.14.1) back to RGB data. 0: HSV → RGB conversion is disabled 1: HSV → RGB conversion is enabled

RGB ↔ HSV conversion causes an operation error. Therefore, even when only just performing conversion of RGB → HSV → RGB, the original RGB value and converted RGB value will not completely match.

25.2.16 BRU Control Registers

25.2.16.1 BRU Input Control Register (VI6_BRU_INCTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	NRM	—	—	—	—	—	—	—	—	D3ON	D2ON	D1ON	D0ON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	DITH3[2:0]			—	DITH2[2:0]			—	DITH1[2:0]			—	DITH0[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	NRM	0	R/W	Color Data Normalization Enables or disables division by the α value of the color data in BRU blending operation. This is used when converting the RGB color data format to which the α value is multiplied (premultiplied color) into the RGB color data format to which the α value is not multiplied (non-premultiplied color). Do not use this for the YCbCr format. 0: Divider (DIV unit in Figure 25.44) does not divide the color value by α 1: Divider (DIV unit in Figure 25.44) divides the color value by α
27 to 20	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
19	D3ON	0	R/W	Dithering Enable of BRU Input 3 Enables or disables dithering (color reduction) of BRU input 3 (BRUin3 in Figure 25.44). 0: Dithering of BRUin3 is disabled 1: Dithering of BRUin3 is enabled
18	D2ON	0	R/W	Dithering Enable of BRU Input 2 Enables or disables dithering (color reduction) of BRU input 2 (BRUin2 in Figure 25.44). 0: Dithering of BRUin2 is disabled 1: Dithering of BRUin2 is enabled
17	D1ON	0	R/W	Dithering Enable of BRU Input 1 Enables or disables dithering (color reduction) of BRU input 1 (BRUin1 in Figure 25.44). 0: Dithering of BRUin1 is disabled 1: Dithering of BRUin1 is enabled
16	D0ON	0	R/W	Dithering Enable of BRU Input 0 Enables or disables dithering (color reduction) of BRU input 0 (BRUin0 in Figure 25.44). 0: Dithering of BRUin0 is disabled 1: Dithering of BRUin0 is enabled

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	DITH3[2:0]	000	R/W	Dithering of CH3 Input to BRU These bits specify the number of colors for pixels after dithering (color reduction) when dithering (color reduction) for pixel information is enabled through the D3ON bit. When dithering (color reduction) for pixel information is disabled, specify 0 in these bits. 000: Dithering of BRUin3 input image is disabled 001: Dithering of BRUin3 input image at 18 bpp (RGB666: 262,144 colors) 010: Dithering of BRUin3 input image at 16 bpp (RGB565: 65,536 colors) 011: Dithering of BRUin3 input image at 15 bpp (RGB555: 32,768 colors) 100: Dithering of BRUin3 input image at 12 bpp (RGB444: 4,096 colors) 101: Dithering of BRUin3 input image at 8 bpp (RGB332: 256 colors) 110, 111: Setting prohibited
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10 to 8	DITH2[2:0]	000	R/W	Dithering of CH2 Input to BRU These bits specify how to perform dithering of the CH2 input to the BRU. The setting method is the same as that for the DITH3 bits. Read the description of the DITH3 bits with BRUin2 and D2ON replacing BRUin3 and D3ON, respectively.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	DITH1[2:0]	000	R/W	Dithering of CH1 Input to BRU These bits specify how to perform dithering of the CH1 input to the BRU. The setting method is the same as that for the DITH3 bits. Read the description of the DITH3 bits with BRUin1 and D1ON replacing BRUin3 and D3ON, respectively.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	DITH0[2:0]	000	R/W	Dithering of CH0 Input to BRU These bits specify how to perform dithering of the CH0 input to the BRU. The setting method is the same as that for the DITH3 bits. Read the description of the DITH3 bits with BRUin0 and D0ON replacing BRUin3 and D3ON, respectively.

Figure 25.44 shows the configuration of the BRU. For the BRU inputs, there are four inputs from the DPR and one internal input as a virtual RPF. BRUin0 to BRUin3 are input ports that have the target node values shown in Figure 25.33, and they can be connected to any module on the DPR. The same color space (YCbCr or RGB) has to be used for the four inputs from the DPR to the BRU.

The virtual RPF inside the BRU is an input unit not connected to the DPR. It is called the "virtual RPF" because it outputs images internally created by the BRU. Starting of the virtual RPF is controlled by VI6_WPFn_SRCRPF.VIR_ACT, and the single-color data created at the virtual RPF can be used for blending or raster operation (ROP) with data from the other input units BRUin0 to BRUin3. The color space for the single color to be set

for the virtual RPF needs to match the color space of the four inputs from the DPR to the BRU. For this setting method, see section 25.2.16.4.

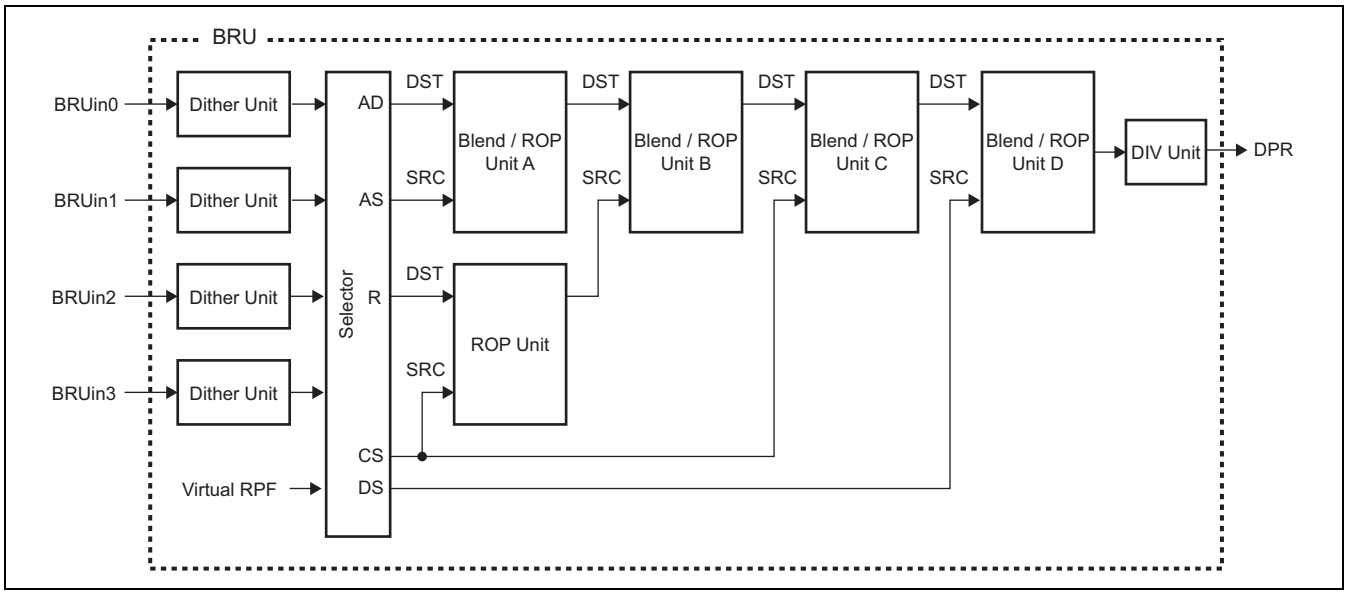


Figure 25.44 BRU Configuration

The selector in Figure 25.44 is used to select the SRC and DST inputs to blending/ROP units A to D and the ROP unit from BRUin0 to BRUin3 which are inputs from the DPR and the virtual RPF. The SRC and DST input sources for blending/ROP units A to D and the ROP unit are either uniquely determined based on the configuration shown in Figure 25.44 (Table 25.32) or selected as desired by registers. The input sources that can be arbitrarily selected by registers are AD, AS, R, CS, and DS, which correspond to the registers shown in Table 25.33.

Table 25.32 SRC and DST with Unique Input Sources

Input	Input Source	Register Bits
Blending/ROP unit B - DST	Output from blending/ROP unit A	—
Blending/ROP unit B - SRC	Output from ROP unit	—
Blending/ROP unit C - DST	Output from blending/ROP unit B	—
Blending/ROP unit D - DST	Output from blending/ROP unit C	—
ROP unit - SRC	CS which is a selector output	VI6_BRUC_CTRL.SRCSEL

Table 25.33 Correspondence between Selector Output Destinations and Register Bits

Selector Output	Output Destination	Register Bits
AD	Blending/ROP unit A - DST	VI6_BRUA_CTRL.DSTSEL
AS	Blending/ROP unit A - SRC	VI6_BRUA_CTRL.SRCSEL
R	ROP unit - DST	VI6_BRU_ROP.DSTSEL
CS	Blending/ROP unit C - SRC	VI6_BRUC_CTRL.SRCSEL
DS	Blending/ROP unit D - SRC	VI6_BRUD_CTRL.SRCSEL

25.2.16.2 Size Register of BRU Input Virtual RPF (VI6_BRU_VIRRPF_SIZE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	VIR_HSIZE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

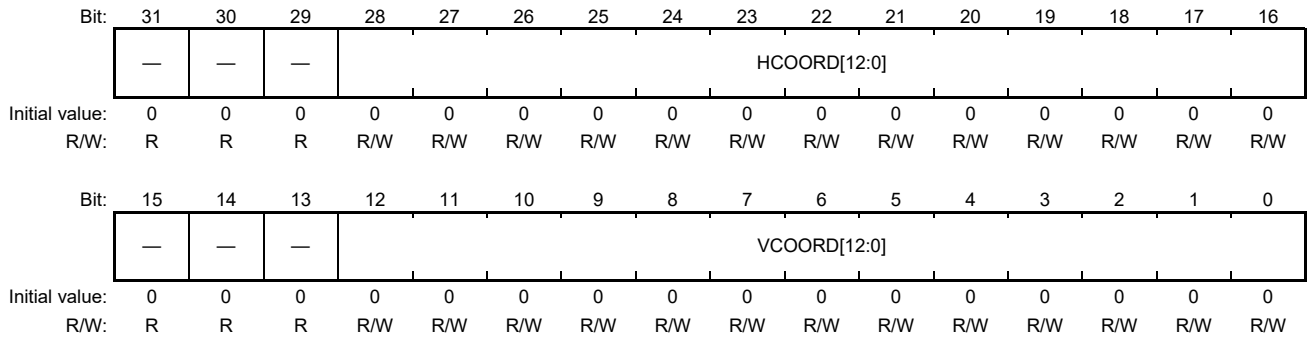
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VIR_VSIZE[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	VIR_HSIZE [12:0]	H'0000	R/W	Virtual RPF Horizontal Size These bits set the horizontal size of an image from the virtual RPF shown in Figure 25.44. A value from 1 to 8,190 can be specified.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	VIR_VSIZE [12:0]	H'0000	R/W	Virtual RPF Vertical Size These bits set the vertical size of an image from the virtual RPF shown in Figure 25.44. A value from 1 to 8,190 can be specified.

The virtual RPF has only a function to output a fixed α value and a fixed pixel value. The virtual RPF can internally create a single-color image without accessing external memory via the MAU. Same as images from the other BRU input ports, a sub layer can be blended on an image created in this manner with the image used as the background (master layer). In turn, when using the image as a sub layer, it can be drawn on the master layer as a window.

Note that the virtual RPF is fixed to input port 5 of the BRU, and the data path route cannot be changed by the DPR.

25.2.16.3 Display Location Register of BRU Input Virtual RPF (VI6_BRU_VIRRPF_LOC)



Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 16	HCOORD [12:0]	H'0000	R/W	Horizontal Coordinate of Virtual RPF Location on Master Layer These bits specify the horizontal coordinate of where to locate the left-edge pixel of the virtual RPF's layer, with the left-edge pixel of the master layer set at coordinate 0. This setting should be made in pixel units. A value from 0 to 8,189 can be specified. When the virtual RPF is specified as the master layer by VI6_WPFn_SRCRPF.VIR_ACT, set these bits to 0.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	VCOORD [12:0]	H'0000	R/W	Vertical Coordinate of Virtual RPF Location on Master Layer These bits specify the vertical coordinate of where to locate the top-edge pixel of the virtual RPF's layer, with the top-edge pixel of the master layer set at coordinate 0. This setting should be made in pixel units. A value from 0 to 8,189 can be specified. When the virtual RPF is specified as the master layer by VI6_WPFn_SRCRPF.VIR_ACT, set these bits to 0.

25.2.16.4 Color Information Register of BRU Input Virtual RPF (VI6_BRU_VIRRPF_COL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	COL_A[7:0]								COL_RCR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COL_GY[7:0]								COL_BCB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	COL_A[7:0]	H'00	R/W	Fixed α of Virtual RPF These bits set the fixed α value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.
23 to 16	COL_RCR [7:0]	H'00	R/W	Fixed R/Cr of Virtual RPF These bits set the fixed R/Cr value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.
15 to 8	COL_GY [7:0]	H'00	R/W	Fixed G/Y of Virtual RPF These bits set the fixed G/Y value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.
7 to 0	COL_BCB [7:0]	H'00	R/W	Fixed B/Cb of Virtual RPF These bits set the fixed B/Cb value when the virtual RPF creates a virtual plane. A value from 0 to 255 can be specified.

The transparency information and color information of the single color that is created by the virtual RPF are set in the bits of this register. As described earlier, the color information is set for the YCbCr or RGB color space. The color space to be set in this register depends on the register settings of the environment and other modules to which the BRU is connected by the DPR. Two cases can be considered. Since the α value (COL_A) is transparency information and irrelevant to the concept of color space, the same setting is made for either the YCbCr or RGB color space.

(Case 1: When an input other than the virtual RPF is used)

When the source RPF is connected to any one of the BRU input ports (BRUin0 to BRUin3) other than the virtual RPF and valid data is being supplied, the same color space data as the color space for the BRU inputs should be set in this register as the color space for the virtual RPF's color information. This is based on the restriction of "all BRU inputs must have the same color space", as described in section 25.2.9.1 or 25.2.16.1.

(Case 2: When only the virtual RPF is used)

When only the virtual RPF is used as the source RPF of WPFn, RPFn is not connected to the BRU, as shown in Figure 25.45. Thus, there is no color space for another input that the color space for the virtual RPF has to follow, as in case 1. This means that the color space of the data output by the BRU is determined by the WPF setting.

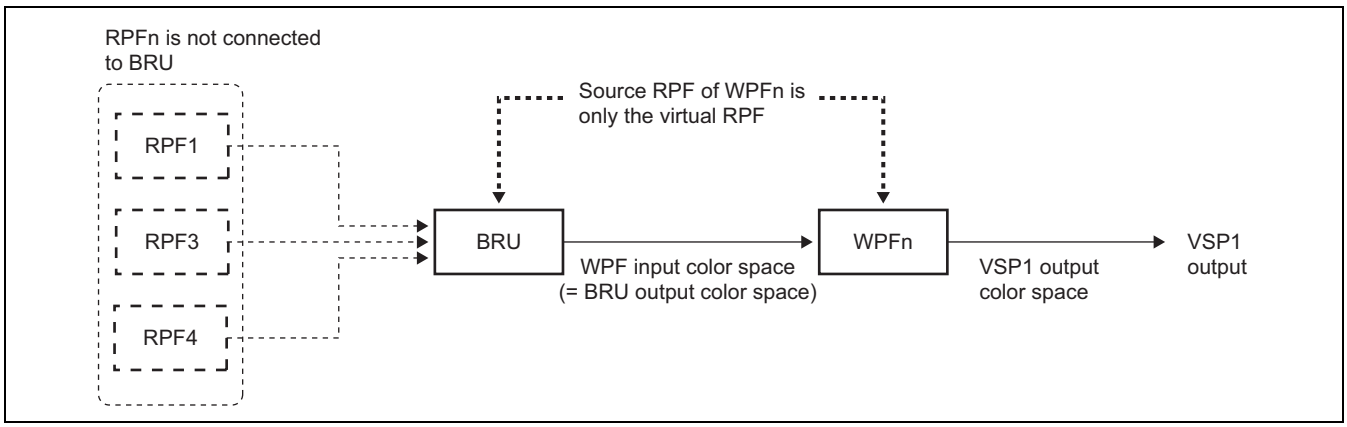


Figure 25.45 Relationship between DPR Connection and Color Space when Only Virtual RPF is Used

As shown in Figure 25.45, the output color space of the VSP1 (= output color space of WPFn) is determined by VI6_WPFn_OUTFMT.WRFMT. When bit 6 in VI6_WPFn_OUTFMT.WRFMT (WRFMT[6]) is 0, the color space is RGB, while when it is 1, the color space is YCbCr. Next, the WPF input color space (= BRU output color space) is determined by the relationship between the WPF output color space and VI6_WPFn_OUTFMT.CSC. When VI6_WPFn_OUTFMT.CSC is 0, the WPF output color space and WPF input color space (= BRU output color space) are the same. When VI6_WPFn_OUTFMT.CSC is 1, the WPF output color space and WPF input color space (= BRU output color space) are the opposite. This relationship is summarized in Table 25.34.

The color space for the virtual RPF's color information should be set in this register according to the "BRU output color space" shown in Table 25.34.

Table 25.34 Relationship between WPF Output Color Space and BRU Output Color Space

VI6_WPFn_OUTFMT Register Bit Settings				BRU Output Color Space (= WPF Input Color Space)
Bit 6 in WRFMT		CSC		
0	(WPF output is RGB)	0	(YCbCr → RGB conversion is disabled)	RGB
0	(WPF output is RGB)	1	(YCbCr → RGB conversion is enabled)	YCbCr
1	(WPF output is YCbCr)	0	(RGB → YCbCr conversion is disabled)	YCbCr
1	(WPF output is YCbCr)	1	(RGB → YCbCr conversion is enabled)	RGB

25.2.16.5 BRU Control Registers (VI6_BRUm_CTRL: m = A, B, C, D)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RBC	—	—	—	—	—	—	—	—	DSTSEL[2:0]			—	SRCSEL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CROP[3:0]				AROP[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RBC	0	R/W	Operation Type of Blending/ROP Unit m (m = A, B, C, D) Specifies the operation type for blending/ROP unit m (m = A, B, C, D) shown in Figure 25.44. 0: ROP (raster operation) 1: Blending operation
30 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	DSTSEL[2:0]	000	R/W	Input Selection for DST Side of Blending/ROP Unit A These bits select the input for the DST side of blending/ROP unit A shown in Figure 25.44. These bits specify the connection between the BRU input port and the DST separately from the setting of connections between other modules and the BRU input port through the DPR. 000: BRU input 0 (BRUin0) is input to DST 001: BRU input 1 (BRUin1) is input to DST 010: BRU input 2 (BRUin2) is input to DST 011: BRU input 3 (BRUin3) is input to DST 100: Virtual RPF is input to DST 101 to 111: Setting prohibited Note: The DSTSEL bits for blending/ROP unit m (m = B, C, D) are reserved according to Table 25.32. The write value should always be 0.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
18 to 16	SRCSEL[2:0]	000	R/W	Input Selection for SRC Side of Blending/ROP Unit m (m = A, C, D) These bits select the input for the SRC side of blending/ROP unit m (m = A, C, D) shown in Figure 25.44. These bits specify the connection between the BRU input port and the SRC separately from the setting of connections between other modules and the BRU input port through the DPR. 000: BRU input 0 (BRUin0) is input to SRC 001: BRU input 1 (BRUin1) is input to SRC 010: BRU input 2 (BRUin2) is input to SRC 011: BRU input 3 (BRUin3) is input to SRC 100: Virtual RPF is input to SRC 101 to 111: Setting prohibited Note: The SRCSEL bits for blending/ROP unit B are reserved according to Table 25.32. The write value should always be 0.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	CROP[3:0]	0000	R/W	Color Data ROP Operator These bits select the ROP operator of the color data in blending/ROP unit m (m = A, B, C, D). Select the opcode for ROP operation from Table 25.35.
3 to 0	AROP[3:0]	0000	R/W	α Data ROP Operator These bits select the ROP operator of the α data in blending/ROP unit m (m = A, B, C, D). Select the opcode for ROP operation from Table 25.35.

Table 25.35 ROP Operator of Blending/ROP Unit m (m = A, B, C, D)

Opcode	Operator
B'0000	NOP(D)
B'0001	AND(S & D)
B'0010	AND_REVERSE(S & ~D)
B'0011	COPY(S)
B'0100	AND_INVERTED(~S & D)
B'0101	CLEAR(0)
B'0110	XOR(S ^ D)
B'0111	OR(S | D)
B'1000	NOR(~(S | D))
B'1001	EQUIV(~(S ^ D))
B'1010	INVERT(~D)
B'1011	OR_REVERSE(S | ~D)
B'1100	COPY_INVERTED(~S)
B'1101	OR_INVERTED(~S | D)
B'1110	NAND(~(S & D))
B'1111	SET(all1)

25.2.16.6 BRU Blend Control Registers (VI6_BRUm_BLD: m = A , B, C, D)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CBES	CCMDX[2:0]			—	CCMDY[2:0]			ABES	ACMDX[2:0]			—	ACMDY[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	COEFX[7:0]								COEFY[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	CBES	0	R/W	Blending Expression Selection Selects the blending expression of the color data in the BRU (VI6_BRUm_CTRL.RBC = 1). Blending coefficients are specified by the CCMDX and CCMDY bits. 0: CCMDX × (DST color data) + CCMDY × (SRC color data) 1: CCMDX × (DST color data) – CCMDY × (SRC color data)
30 to 28	CCMDX[2:0]	000	R/W	Blending Coefficient X Selection These bits specify coefficient X used in the blending expression determined by the CBES bit. 000: DST α data is used as blending coefficient X 001: 255 – (DST α data) is used as blending coefficient X 010: SRC α data is used as blending coefficient X 011: 255 – (SRC α data) is used as blending coefficient X 100: Fixed α value 0 (COEFX setting)
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26 to 24	CCMDY[2:0]	000	R/W	Blending Coefficient Y Selection These bits specify coefficient Y used in the blending expression determined by the CBES bit. 000: DST α data is used as blending coefficient Y 001: 255 – (DST α data) is used as blending coefficient Y 010: SRC α data is used as blending coefficient Y 011: 255 – (SRC α data) is used as blending coefficient Y 100: Fixed α value 1 (COEFY setting)
23	ABES	0	R/W	Blending α Creation Expression Specifies the expression for creating α data after blending by blending/ROP unit m (m = A, B, C, D). α creation coefficients are specified by the ACMDX and ACMDY bits. 0: ACMDX × (DST α data) + ACMDXY × (SRC α data) 1: ACMDX × (DST α data) – ACMDXY × (SRC α data)

Bit	Bit Name	Initial Value	R/W	Description
22 to 20	ACMDX[2:0]	000	R/W	α Creation Coefficient X These bits specify α creation coefficient X used in the α creation expression determined by the ABES bit. 000: (α creation coefficient X) = (DST α data) 001: (α creation coefficient X) = 255 – (DST α data) 010: (α creation coefficient X) = (SRC α data) 011: (α creation coefficient X) = 255 – (SRC α data) 100: (α creation coefficient X) = Fixed α value 0 (COEFX setting) 101 to 111: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	ACMDY[2:0]	000	R/W	α Creation Coefficient Y These bits specify α creation coefficient Y used in the α creation expression determined by the ABES bit. 000: (α creation coefficient Y) = (DST α data) 001: (α creation coefficient Y) = 255 – (DST α data) 010: (α creation coefficient Y) = (SRC α data) 011: (α creation coefficient Y) = 255 – (SRC α data) 100: (α creation coefficient Y) = Fixed α value 1 (COEFY setting) 101 to 111: Setting prohibited
15 to 8	COEFX[7:0]	H'00	R/W	Fixed α Value 0 These bits specify fixed α value 0 used when the CCMDX or ACMDX bits are set to B'100. A value from H'00 to H'FF can be specified.
7 to 0	COEFY[7:0]	H'00	R/W	Fixed α Value 1 These bits specify fixed α value 1 used when the CCMDY or ACMDY bits are set to B'100. A value from H'00 to H'FF can be specified.

25.2.16.7 BRU Raster Operation Control Register (VI6_BRU_ROP)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	DSTSEL[2:0]			—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	CROP[3:0]				AROP[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22 to 20	DSTSEL[2:0]	000	R/W	Input Selection for DST Side of ROP Unit These bits select the input for the DST side of the ROP unit. For the SRC side, the same data as the input for the SRC side of blending/ROP unit C is input. 000: BRU input 0 (BRUin0) is input to DST 001: BRU input 1 (BRUin1) is input to DST 010: BRU input 2 (BRUin2) is input to DST 011: BRU input 3 (BRUin3) is input to DST 100: Virtual RPF is input to DST 101 to 111: Setting prohibited
19 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 4	CROP[3:0]	0000	R/W	Color Data ROP Operator These bits select the ROP operator of the color data in the ROP unit. Select the opcode for ROP operation from Table 25.35.
3 to 0	AROP[3:0]	0000	R/W	α Data ROP Operator These bits select the ROP operator of the α data in the ROP unit. Select the opcode for ROP operation from Table 25.35.

25.2.17 HGO Control Registers

25.2.17.1 HGO Detection Window Offset Register (VI6_HGO_OFFSET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	HOFFSET[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	VOFFSET[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HOFFSET[13:0]	H'0000	R/W	Horizontal Offset of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 25.46). In these bits, specify the value of horizontal offset (hoffset shown in Figure 25.46) in pixel units. A value from 0 to 8,191 can be specified. The value of HOFFSET shall be smaller than that of the input image size of HGO.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VOFFSET[13:0]	H'0000	R/W	Vertical Offset of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 25.46). In these bits, specify the value of vertical offset (voffset shown in Figure 25.46) in pixel units. A value from 0 to 8,191 can be specified. The value of VOFFSET shall be smaller than that of the input image size of HGO.

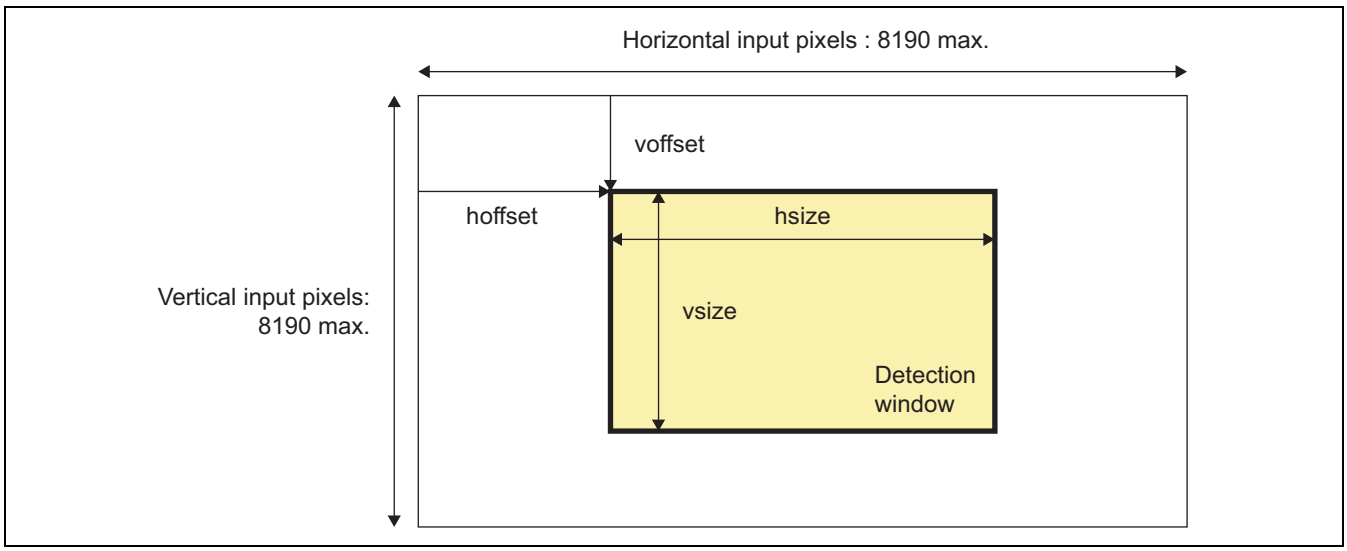
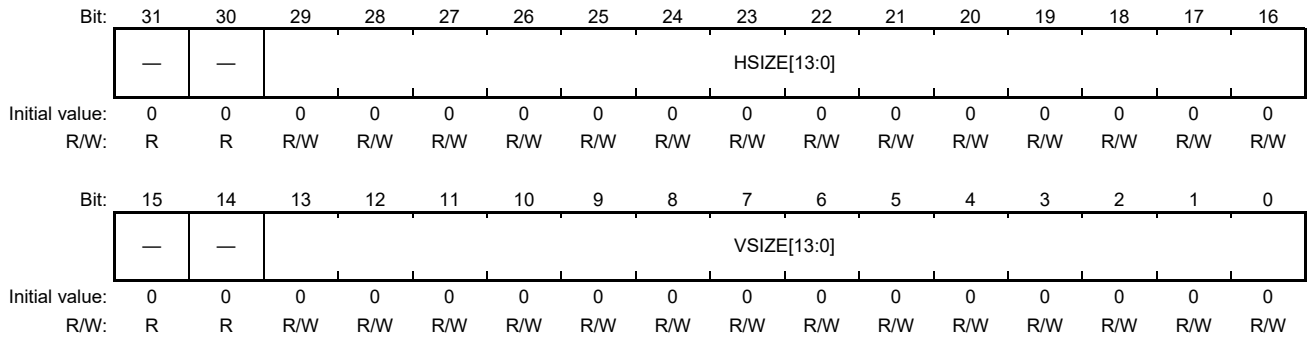


Figure 25.46 Histogram Detection Window of HGO

25.2.17.2 HGO Detection Window Size Register (VI6_HGO_SIZE)



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HSIZE[13:0]	H'0000	R/W	Horizontal Size of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 25.46). In these bits, specify the value of horizontal size (hsize shown in Figure 25.46) in pixel units. A value from 1 to 8,192 can be specified.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VSIZE[13:0]	H'0000	R/W	Vertical Size of Histogram Detection Window The HGO creates a histogram for the detection window in the input image (Figure 25.46). In these bits, specify the value of vertical size (vsize shown in Figure 25.46) in pixel units. A value from 1 to 8,192 can be specified.

25.2.17.3 HGO Mode Register (VI6_HGO_MODE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MAX RGB	OFSB_ R	OFSB_ G	OFSB_ B	HRATIO[1:0]		VRATIO[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	MAXRGB	0	R/W	Histogram Source Component Setting 0: The histogram is generated from 3 color components independently. 1: The histogram is generated from the maximum value of input R, G and B data.
6	OFSB_R	0	R/W	Offset Binary Mode for R/Cr/H Component 0: Straight binary 1: Offset binary In offset binary mode, values are converted to absolute values before they are used to detect the maximum value, minimum value, sum, and black band. Note that values without conversion are always used for histogram creation regardless of this mode setting.
5	OFSB_G	0	R/W	Offset Binary Mode for G/Y/S/max (R, G, B) Component 0: Straight binary 1: Offset binary In offset binary mode, values are converted to absolute values before they are used to detect the maximum value, minimum value, sum, and black band. Note that values without conversion are always used for histogram creation regardless of this mode setting.
4	OFSB_B	0	R/W	Offset Binary Mode for B/Cb/V Component 0: Straight binary 1: Offset binary In offset binary mode, values are converted to absolute values before they are used to detect the maximum value, minimum value, sum, and black band. Note that values without conversion are always used for histogram creation regardless of this mode setting.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	HRATIO[1:0]	00	R/W	Horizontal Pixel Skipping Mode for Histogram Detection 00: No skipping for horizontal pixels. 01: Horizontal 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created. 10: Horizontal 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created. The first pixel in the horizontal direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.
1, 0	VRATIO[1:0]	00	R/W	Vertical Pixel Skipping Mode for Histogram Detection 00: No skipping for vertical pixels. 01: Vertical 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created. 10: Vertical 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created. The first pixel in the vertical direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.

25.2.17.4 HGO LB Detection Threshold Register (VI6_HGO_LB_TH)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BLACK_TH[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	BLACK_TH[7:0]	H'00	R/W	Threshold for Black Level Determination in Letter Box Detection In letter box detection, when all input pixels have the value equal to or smaller than the value specified in these bits, the image data is determined as black. Note that the letter box detection is not affected by the histogram detection window illustrated in Figure 25.46. A value from 0 to 255 can be specified.

25.2.17.5 HGO Horizontal Position Register for LB Detection Zone-n (VI6_HGO_LBn_H: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	HPOS0[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	HPOS1[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HPOS0[13:0]	H'0000	R/W	Horizontal Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box. In these bits, specify the value of hpos0 of the detection zone-n (Figure 25.47) in pixel units. A value from 0 to 8,191 can be specified. HPOS0 ≤ HPOS1 should be satisfied. These bits are valid for Zone-0 and 1. For Zone-2 and 3, these bits are reserved.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	HPOS1[13:0]	H'0000	R/W	Horizontal End Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box. In these bits, specify the value of hpos1 of the detection zone-n (Figure 25.47) in pixel units. A value from 0 to 8,191 can be specified. HPOS0 ≤ HPOS1 should be satisfied.

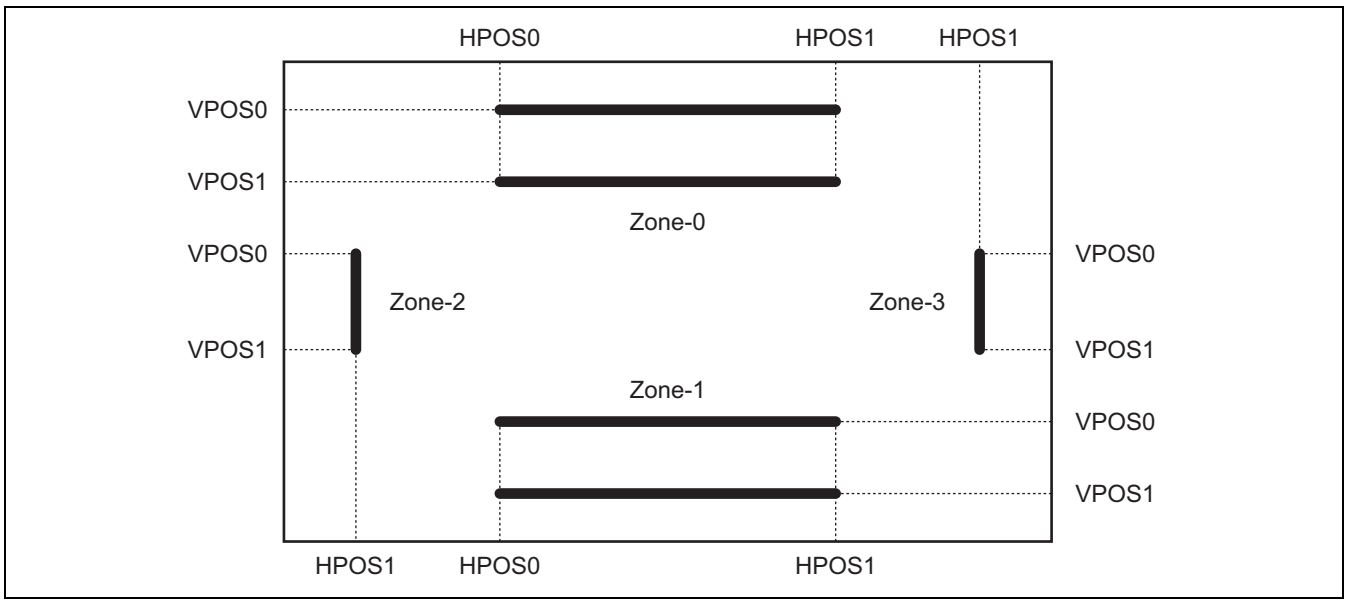


Figure 25.47 Letter Box Detection Position Settings for HGO

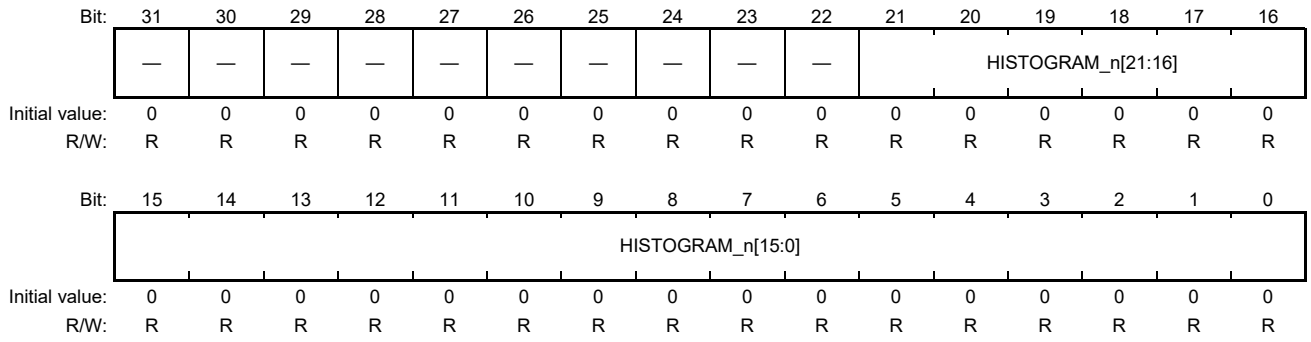
25.2.17.6 HGO Vertical Position Register for LB Detection Zone-n (VI6_HGO_LBn_V: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	VPOS0[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	VPOS1[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	VPOS0[13:0]	H'0000	R/W	Vertical Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box In these bits, specify the value of vpos0 of the detection zone-n (Figure 25.47) in pixel units. A value from 0 to 8,191 can be specified. VPOS0 ≤ VPOS1 should be satisfied.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VPOS1[13:0]	H'0000	R/W	Vertical End Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.47) in the input image have the value equal to or smaller than the threshold value, the HGO determines that there is a letter box. In these bits, specify the value of vpos1 of the detection zone-n (Figure 25.47) in pixel units. A value from 0 to 8,191 can be specified. VPOS0 ≤ VPOS1 should be satisfied.

25.2.17.7 HGO Component-m Histogram Register (VI6_HGO_m_HISTO_n: m = R, G, B, n = 0 to 63)



Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	HISTOGRAM_n [21:0]	H'00 0000	R	Frequency of Component-m in the value range-n From these bits, the count of the pixels whose component-m value (val) satisfies the following condition within the histogram detection window (Figure 25.46) is read (after pixel skipping is applied when skipping mode is selected). $4 \times n \leq val < 4 \times (n + 1)$ Counting starts after the HGO is activated. To read the histogram, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.

The component-m in a color space is determined by the following table.

	Color Space			
	RGB		YCbCr	HSV
Index-m	VI6_HGO_MODE. MAXRGB = 0	VI6_HGO_MODE. MAXRGB = 1	VI6_HGO_MODE. MAXRGB = 0*1	VI6_HGO_MODE. MAXRGB = 0*1
R	R	n/a*2	Cr	H
G	G	max (R, G, B)*3	Y	S
B	B	n/a*2	Cb	V

Notes: 1. When color space of input data is in YCbCr or HSV, set VI6_HGO_MODE.MAXRGB = 0.
2. When VI6_HGO_MODE.MAXRGB = 1, the histogram of index-R / index-B are not ensured.
3. max (R, G, B) indicates maximum value of input R, G and B data.

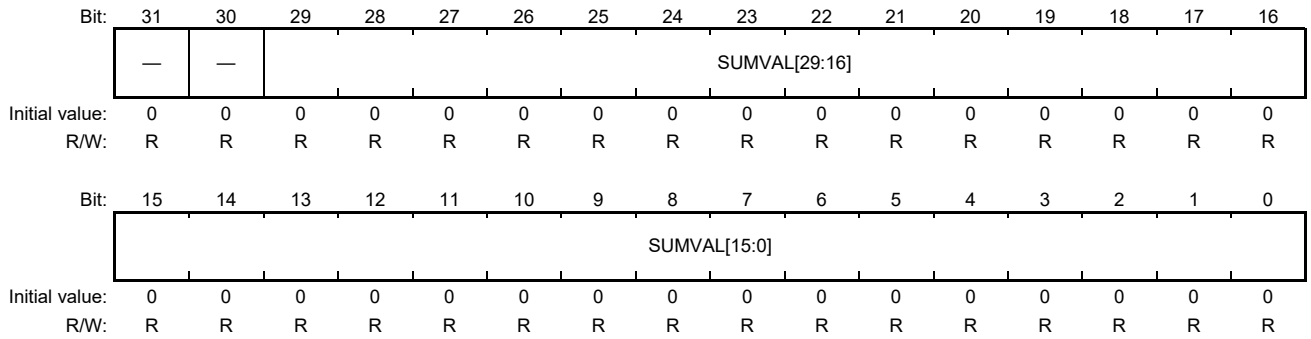
25.2.17.8 HGO Component-m Min/Max Value Register (VI6_HGO_m_MAXMIN: m = R, G, B)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	MAXVAL[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MINVAL[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	MAXVAL[7:0]	H'00	R	Maximum Value of Component-m From these bits, the maximum value of the component-m of the pixels within the histogram detection window (Figure 25.46) is read (after pixel skipping is applied when skipping mode is selected). Maximum value detection starts after the HGO is activated. To read the maximum value, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	MINVAL[7:0]	H'00	R	Minimum Value of Component-m From these bits, the minimum value of the component-m of the pixels within the histogram detection window (Figure 25.46) is read (after pixel skipping is applied when skipping mode is selected). Minimum value detection starts after the HGO is activated. To read the minimum value, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.

25.2.17.9 HGO Component-m Sum Register (VI6_HGO_m_SUM: m = R, G, B)



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 0	SUMVAL[29:0]	H'0000 0000	R	Sum of Component-m From these bits, the sum of the component-m of the pixels within the histogram detection window (Figure 25.46) is read (after pixel skipping is applied when skipping mode is selected). Accumulation starts after the HGO is activated. To read the sum, read these bits after the HGO has completed processing of one screen of data and before the HGO is activated again.

25.2.17.10 HGO Component-m LB Detection Result Register (VI6_HGO_m_LB_DET: m = R, G, B)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LTRBOX1	LTRBOX2	SIDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LTRBOX1	0	R	Letter Box Detection Result #1 of Zone-0/1 for Component-m This bit is set to 1 when none of the component-m of the pixels on the lines of zone-0/vpos0 and zone-1/vpos1 (two lines in total) in Figure 25.47 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGO has completed processing of one screen of data and before the HGO is activated again. The value read during processing is not guaranteed to be correct.
1	LTRBOX2	0	R	Letter Box Detection Result #2 of Zone-0/1 for Component-m This bit is set to 1 when none of the component-m of the pixels on the four lines of zone-0 and 1 in Figure 25.47 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGO has completed processing of one screen of data and before the HGO is activated again. The value read during processing is not guaranteed to be correct.
0	SIDE	0	R	Letter Box Detection Result of Zone-2/3 for Component-m This bit is set to 1 when none of the component-m of the pixels on the two lines of zone-2 and 3 in Figure 25.47 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGO has completed processing of one screen of data and before the HGO is activated again. The value read during processing is not guaranteed to be correct.

25.2.17.11 HGO Parameter Register Reset (VI6_HGO_REGRST)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RCLEA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RCLEA	0	W	Register Reset Writing 1 to this bit resets all read-only registers (sections 25.2.17.7 to 25.2.17.10) to their initial values. This register is write-only and is always read as 0. Note that R/W registers (sections 25.2.17.1 to 25.2.17.6) are not affected by write access to this register.

25.2.18 HGT Control Registers

25.2.18.1 HGT Detection Window Offset Register (VI6_HGT_OFFSET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	HOFFSET[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	VOFFSET[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HOFFSET[13:0]	H'0000	R/W	Horizontal Offset of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 25.48). In these bits, specify the value of horizontal offset (hoffset shown Figure 25.48) in pixel units. A value from 0 to 8,191 can be specified. The value of HOFFSET shall be smaller than that of the input image size of HGT.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VOFFSET[13:0]	H'0000	R/W	Vertical Offset of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 25.48). In these bits, specify the value of vertical offset (voffset shown in Figure 25.48) in pixel units. A value from 0 to 8,191 can be specified. The value of VOFFSET shall be smaller than that of the input image size of HGT.

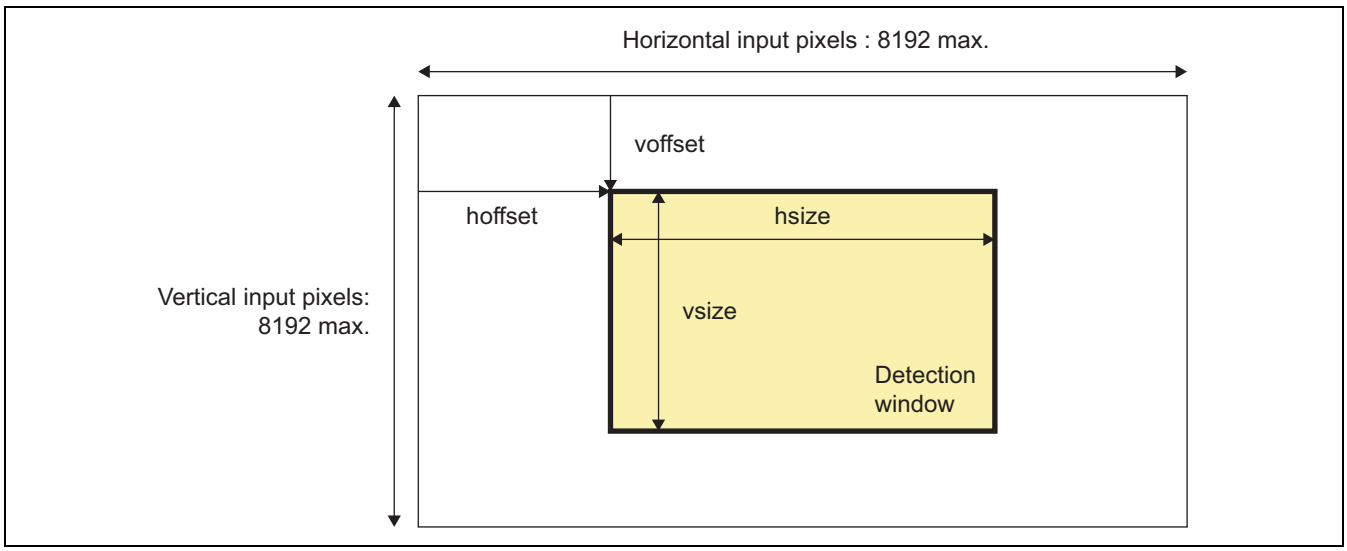


Figure 25.48 Histogram Detection Window of HGT

25.2.18.2 HGT Detection Window Size Register (VI6_HGT_SIZE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	HSIZE[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	VSIZE[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HSIZE[13:0]	H'0000	R/W	Horizontal Size of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 25.48). In these bits, specify the value of horizontal offset (hsize shown in Figure 25.48) in pixel units. A value from 1 to 8,192 can be specified.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VSIZE[13:0]	H'0000	R/W	Vertical Size of Histogram Detection Window The HGT creates a histogram for the detection window in the input image (Figure 25.48). In these bits, specify the value of vertical offset (vsize shown in Figure 25.48) in pixel units. A value from 1 to 8,192 can be specified.

25.2.18.3 HGT Mode Register (VI6_HGT_MODE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	HRATIO[1:0]		VRATIO[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

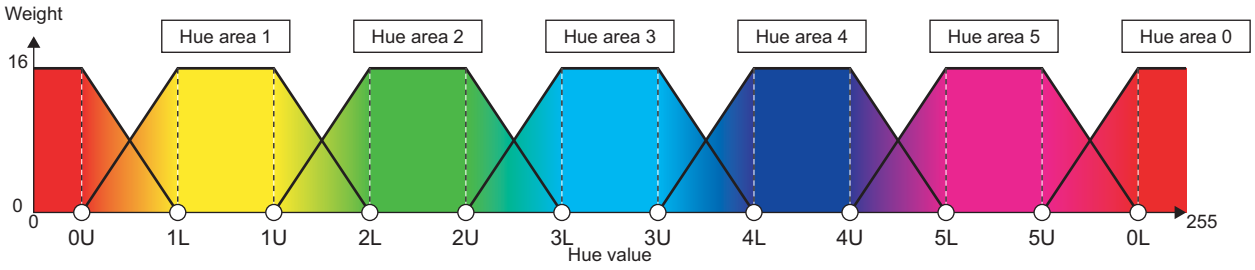
Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3, 2	HRATIO[1:0]	00	R/W	Horizontal Pixel Skipping Mode for Histogram Detection 00: No skipping for horizontal pixels. 01: Horizontal 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created. 10: Horizontal 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created. The first pixel in the horizontal direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.
1, 0	VRATIO[1:0]	00	R/W	Vertical Pixel Skipping Mode for Histogram Detection 00: No skipping for vertical pixels. 01: Vertical 1/2 skipping. One pixel is discarded from every two pixels before a histogram is created. 10: Vertical 1/4 skipping. Three pixels are discarded from every four pixels before a histogram is created. The first pixel in the vertical direction is not discarded but subsequent pixels are discarded (regardless of the histogram detection window). Among the pixels that have not been discarded, only the pixels within the detection window are used to create a histogram.

25.2.18.4 HGT Hue Area Register (VI6_HGT_HUE_AREA_n: n = 0 to 5)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	HUE_LOWER_n[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HUE_UPPER_n[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	HUE_LOWER_n [7:0]	H'00	R/W	Lower Boundary Value for Hue Area – n The HGT creates a two-dimensional histogram of H (hue) and S (saturation) components. Division of hue areas and overlapping of adjacent hue areas can be specified through these bits. In these bits, specify the value of n L (hue_lower n) shown in Figure 25.49. A value from 0 to 255 can be specified. The specified value should satisfy the restrictions shown in Figure 25.49.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	HUE_UPPER_n [7:0]	H'00	R/W	Upper Boundary Value for Hue Area – n The HGT creates a two-dimensional histogram of H (hue) and S (saturation) components. Division of hue areas and overlapping of adjacent hue areas can be specified through these bits. In these bits, specify the value of n U (hue_upper n) shown in Figure 25.49. A value from 0 to 255 can be specified. The specified value should satisfy the restrictions shown in Figure 25.49.



Restrictions: 0U ≤ 1L ≤ 1U ≤ 2L ≤ 2U ≤ 3L ≤ 3U ≤ 4L ≤ 4U ≤ 5L ≤ 5U, 0L ≤ 0U, or 5U ≤ 0L

- Values are rounded down in the diagonal-line sections.
- When overlapped areas are not specified, the boundary value is included in the lower-value

0L = HUE_LOWER_0 register setting	0U = HUE_UPPER_0 register setting
1L = HUE_LOWER_1 register setting	1U = HUE_UPPER_1 register setting
2L = HUE_LOWER_2 register setting	2U = HUE_UPPER_2 register setting
3L = HUE_LOWER_3 register setting	3U = HUE_UPPER_3 register setting
4L = HUE_LOWER_4 register setting	4U = HUE_UPPER_4 register setting
5L = HUE_LOWER_5 register setting	5U = HUE_UPPER_5 register setting

Figure 25.49 Weighting Histogram Using Hue

25.2.18.5 HGT LB Detection Threshold Register (VI6_HGT_LB_TH)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	BLACK_TH[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	BLACK_TH[7:0]	H'00	R/W	Threshold for Black Level Determination in Letter Box Detection In letter box detection, when all pixels of the input image data have the value equal to or smaller than the value specified in these bits, the data is determined as black. Note that the letter box detection is not affected by the histogram detection window illustrated in Figure 25.48 A value from 0 to 255 can be specified.

25.2.18.6 HGT Horizontal Position Register for LB Detection Zone-n (VI6_HGT_LBn_H: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	HPOS0[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	HPOS1[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	HPOS0[13:0]	H'0000	R/W	Horizontal Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of hpos0 of the detection zone-n (Figure 25.50) in pixel units. A value from 0 to 8,191 can be specified. HPOS0 ≤ HPOS1 should be satisfied. These bits are valid for Zone-0 and 1. For Zone-2 and 3, these bits are reserved.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	HPOS1[13:0]	H'0000	R/W	Horizontal End Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of hpos1 of the detection zone-n (Figure 25.50) in pixel units. A value from 0 to 8,191 can be specified. HPOS0 ≤ HPOS1 should be satisfied.

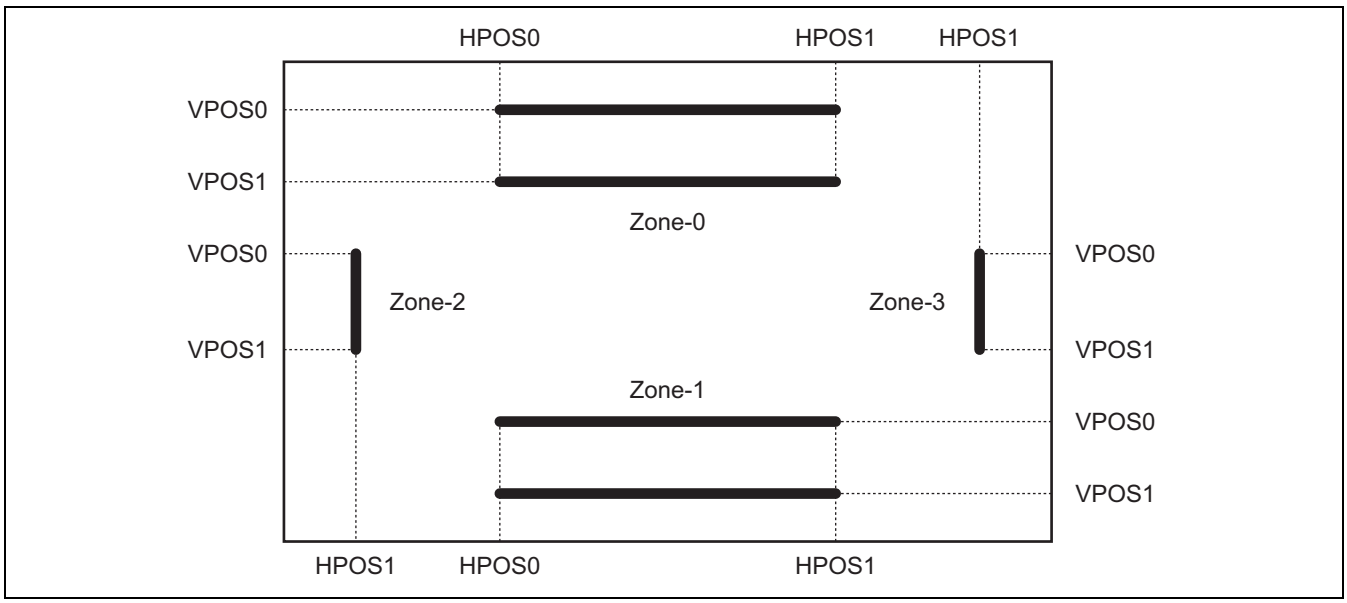


Figure 25.50 Letter Box Detection Position Settings for HGT

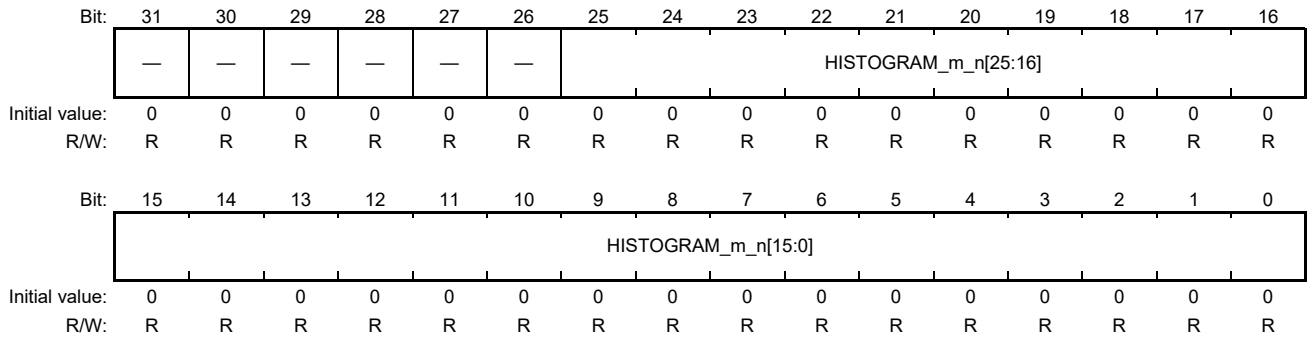
25.2.18.7 HGT Vertical Position Register for LB Detection Zone-n (VI6_HGT_LBn_V: n = 0, 1, 2, 3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	VPOS0[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	VPOS1[13:0]													
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

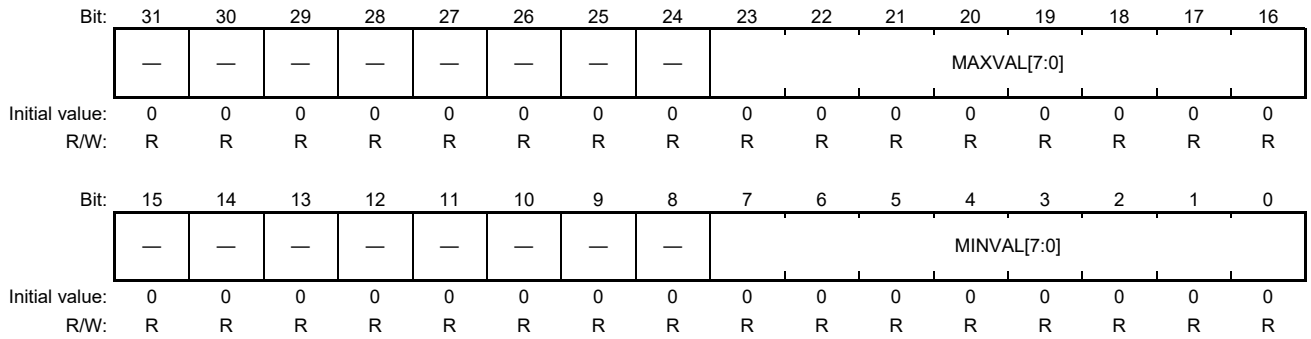
Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 16	VPOS0[13:0]	H'0000	R/W	Vertical Start Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of vpos0 of the detection zone-n (Figure 25.50) in pixel units. A value from 0 to 8,191 can be specified. VPOS0 ≤ VPOS1 should be satisfied.
15, 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13 to 0	VPOS1[13:0]	H'0000	R/W	Vertical Position for Letter Box Detection Zone-n When all pixels on a line (shown in Figure 25.50) in the input image have the value equal to or smaller than the threshold value, the HGT determines that there is a letter box. In these bits, specify the value of vpos1 of the detection zone-n (Figure 25.50) in pixel units. A value from 0 to 8,191 can be specified. VPOS0 ≤ VPOS1 should be satisfied.

25.2.18.8 HGT Histogram Register (VI6_HGT_HISTO_m_n: m = 0 to 5, n = 0 to 31)



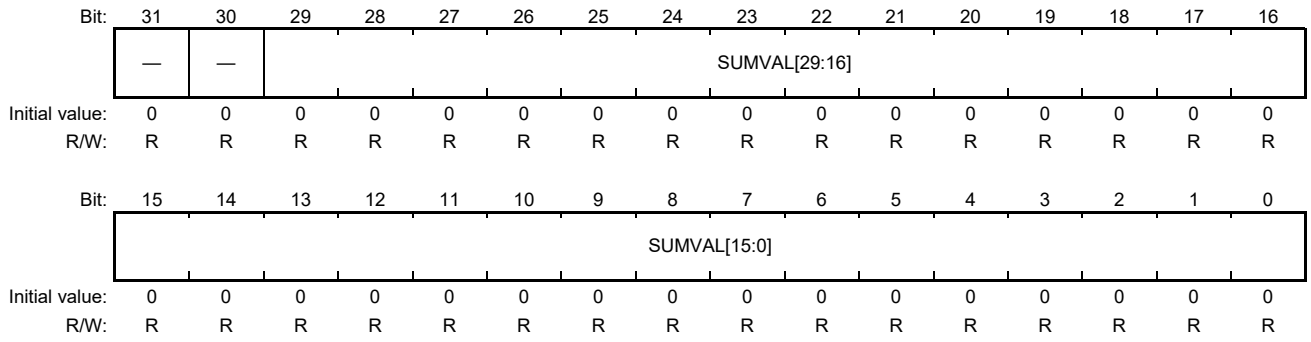
Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25 to 0	HISTOGRAM_m_n [25:0]	H'000 0000	R	Weighted Frequency of Hue Area-m and Saturation Area-n From these bits, the count of weighting for the pixels whose H component value is in hue area m (Figure 25.49) and whose S component value (val) satisfies the following condition within the histogram detection window (Figure 25.48) is read (after pixel skipping is applied when skipping mode is selected). $8 \times n \leq val < 8 \times (n + 1)$ The weight is determined by the H component value as shown in Figure 25.49 and the maximum weight is 16. Counting starts after the HGT is activated. To read the histogram, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.

25.2.18.9 HGT Max/Min Value Register (VI6_HGT_MAXMIN)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 16	MAXVAL[7:0]	H'00	R	Maximum Value of S Components From these bits, the maximum value of the S components of the pixels within the histogram detection window (Figure 25.48) is read (after pixel skipping is applied when skipping mode is selected). Maximum value detection starts after the HGT is activated. To read the maximum value, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 0	MINVAL[7:0]	H'00	R	Minimum Value of S Components From these bits, the minimum value of the S components of the pixels within the histogram detection window (Figure 25.48) is read (after pixel skipping is applied when skipping mode is selected). Minimum value detection starts after the HGT is activated. To read the minimum value, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.

25.2.18.10 HGT Sum Register (VI6_HGT_SUM)



Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29 to 0	SUMVAL[29:0]	H'0000 0000	R	Sum of V Components From these bits, the sum of the V components of the pixels within the histogram detection window (Figure 25.48) is read (after pixel skipping is applied when skipping mode is selected). Accumulation starts after the HGT is activated. To read the sum, read these bits after the HGT has completed processing of one screen of data and before the HGT is activated again.

25.2.18.11 HGT LB Detection Result Register (VI6_HGT_LB_DET)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	LTRBOX1	LTRBOX2	SIDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	LTRBOX1	0	R	Letter Box Detection Result #1 of Zone-0/1 for V Component This bit is set to 1 when none of the V components of the pixels on the lines of zone-0/VPOS0 and zone-1/VPOS1 (two lines in total) in Figure 25.50 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGT has completed processing of one screen of data and before the HGT is activated again. The value read during processing is not guaranteed to be correct.
1	LTRBOX2	0	R	Letter Box Detection Result #2 of Zone-0/1 for V Component This bit is set to 1 when none of the V components of the pixels on the four lines of zone-0 and 1 in Figure 25.50 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGT has completed processing of one screen of data and before the HGT is activated again. The value read during processing is not guaranteed to be correct.
0	SIDE	0	R	Letter Box Detection Result of Zone-2/3 for V Component This bit is set to 1 when none of the V components of the pixels on the two lines of zone-2 and 3 in Figure 25.50 exceeds the threshold (BLACK_TH). If any pixel is greater than the threshold, this bit is set to 0. Read this bit after the HGT has completed processing of one screen of data and before the HGT is activated again. The value read during processing is not guaranteed to be correct.

25.2.18.12 HGT Parameter Register Reset (VI6_HGT_REGRST)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RCLEA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	RCLEA	0	W	Register Reset Writing 1 to this bit resets all read-only registers (sections 25.2.18.8 to 25.2.18.11) to their initial values. This register is write-only and is always read as 0. Note that R/W registers (sections 25.2.18.1 to 25.2.18.7) are not affected by write access to this register.

25.2.19 LIF Control Registers

25.2.19.1 LIF Control Register (VI6_LIF_CTRL)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	OBTH[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	CFMT	—	—	REQSEL	LIF_EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	OBTH[10:0]	H'000	R/W	Buffer Threshold for Start Ready Notification to Display Module When outputting data to the external module, the VSP stores data in the buffer in the LIF. When the amount of data stored in the buffer reaches the value specified in these bits, the VSP notifies the external display module of the start of a frame through an interrupt source (VI6_DISP_IRQ_STA.DST: see section 25.2.5.8). A value from 1 to 1,536 can be specified. Note: The OBTH value should satisfy the following conditions. • The value should not be larger than the VI6_LIF_CSBTH.HBTH bit setting. • When the horizontal and vertical sizes of the image input to the LIF are hlif_in, and vlif_in, OBTH should be specified so that the following is satisfied. $(<h_{lif\_in}+1>/2)\times v_{lif\_in}-4\geq OBTH$ The LIF input image size (hlif_in, and vlif_in) is the same as the WPF0 output image size. Recommendation value of OBTH is 128.
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	CFMT	0	R/W	Chroma Format This bit selects the output format from the LIF module to the display module. When RGB format is used, this bit shall be set to 0. 0: YCbCr444 or RGB Format 1: Reserved Note: ARBG8888 or RGB888 can be used for DU input format.
3, 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	REQSEL	0	R/W	External Display Module Selection This bit should always be set to 1. 0: Prohibited. 1: DU is selected as the destination external display module.
0	LIF_EN	0	R/W	Enable/Disable of Data Output to External Display Module Enables or disables data output from the LIF to DU. 0: Data output to the DU is disabled. 1: Data output to the DU is enabled.

25.2.19.2 LIF Clock Stop Buffer Control Register (VI6_LIF_CSBTH)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	HBTH[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	LBTH[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	HBTH[10:0]	H'000	R/W	Buffer Threshold for Clock Stop in Dynamic Clock Control When the remaining data amount in the buffer in the LIF reaches the value specified in these bits while data is output from the LIF to the external display module, the VSP clock is stopped. A value from 2 to 1,536 can be specified. The specified value should satisfy HBTH > LBTH. Recommendation value of HBTH is 1536.
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	LBTH[10:0]	H'000	R/W	Buffer Threshold for Clock Start in Dynamic Clock Control When the remaining data amount in the buffer in the LIF decreases to the value specified in these bits while data is output from the LIF to the external display module and the clock is stopped through the setting in the HBTH bits, the VSP clock supply is restarted. A value from 1 to 1,535 can be specified. The specified value should satisfy LBTH < HBTH. Recommendation value of LBTH is 1520.

25.2.20 Security Control Registers

25.2.20.1 Secure Access Control Register 0 (VI6_SECURE_CTRL0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SCCH3	SCCH2	SCCH1	SCCH0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SCWPF3	SCWPF2	SCWPF1	SCWPF0	—	—	—	SCRPF4	SCRPF3	SCRPF2	SCRPF1	SCRPF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Each bit is used for specifying the secure attribute of the corresponding registers. If a bit is set to 1 (secure), the corresponding registers can be written only by the secure CPU access.

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27	SCCH3	0	R/W	Secure Attribute for Display List 3 Registers 0: Non-secure 1: Secure
26	SCCH2	0	R/W	Secure Attribute for Display List 2 Registers 0: Non-secure 1: Secure
25	SCCH1	0	R/W	Secure Attribute for Display List 1 Registers 0: Non-secure 1: Secure
24	SCCH0	0	R/W	Secure Attribute for Display List 0 Registers 0: Non-secure 1: Secure
23 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	SCWPF3	0	R/W	Secure Attribute for WPF3 Registers 0: Non-secure 1: Secure
10	SCWPF2	0	R/W	Secure Attribute for WPF2 Registers 0: Non-secure 1: Secure
9	SCWPF1	0	R/W	Secure Attribute for WPF1 Registers 0: Non-secure 1: Secure
8	SCWPF0	0	R/W	Secure Attribute for WPF0 Registers 0: Non-secure 1: Secure

Bit	Bit Name	Initial Value	R/W	Description
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	SCRPF4	0	R/W	Secure Attribute for RPF4 Registers 0: Non-secure 1: Secure
3	SCRPF3	0	R/W	Secure Attribute for RPF3 Registers 0: Non-secure 1: Secure
2	SCRPF2	0	R/W	Secure Attribute for RPF2 Registers 0: Non-secure 1: Secure
1	SCRPF1	0	R/W	Secure Attribute for RPF1 Registers 0: Non-secure 1: Secure
0	SCRPF0	0	R/W	Secure Attribute for RPF0 Registers 0: Non-secure 1: Secure

25.2.20.2 Secure Access Control Register 1 (VI6_SECURE_CTRL1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SCLIF	SCHGT	SCHGO	—	SCBRU	SCHSI	SCHST	SCCLU	SCLUT	—	—	SCUDS2	SCUDS1	SCUDS0	SCSRU
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W

Each bit is used for specifying the secure attribute of the corresponding registers. If a bit is set to 1 (secure), the corresponding registers can be read or written only by the secure CPU access.

Bit	Bit Name	Initial Value	R/W	Description
31 to 15	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
14	SCLIF	0	R/W	Secure Attribute for LIF Registers 0: Non-secure 1: Secure
13	SCHGT	0	R/W	Secure Attribute for HGT Registers 0: Non-secure 1: Secure
12	SCHGO	0	R/W	Secure Attribute for HGO Registers 0: Non-secure 1: Secure
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	SCBRU	0	R/W	Secure Attribute for BRU Registers 0: Non-secure 1: Secure
9	SCHSI	0	R/W	Secure Attribute for HSI Registers 0: Non-secure 1: Secure
8	SCHST	0	R/W	Secure Attribute for HST Registers 0: Non-secure 1: Secure
7	SCCLU	0	R/W	Secure Attribute for CLU Registers 0: Non-secure 1: Secure
6	SCLUT	0	R/W	Secure Attribute for LUT Registers 0: Non-secure 1: Secure
5, 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	SCUDS2	0	R/W	Secure Attribute for UDS2 Registers 0: Non-secure 1: Secure
2	SCUDS1	0	R/W	Secure Attribute for UDS1 Registers 0: Non-secure 1: Secure
1	SCUDS0	0	R/W	Secure Attribute for UDS0 Registers 0: Non-secure 1: Secure
0	SCSRU	0	R/W	Secure Attribute for SRU Registers 0: Non-secure 1: Secure

25.3 Lookup Table Settings

25.3.1 CLUT or LUT

For a single entry to the CLUT space (see Table 25.36) or LUT space (see Table 25.36) of the VSP1, the CLUT or LUT data is set by a write access in the format shown in Figure 25.51.

The entry address of each space is (start address of the space) + (entry number counting from the base point 0 × 4). For example, the address of entry 7 to the LUT space is $VSP_BASE + H'7000 + 7 × 4 (H'FE92_701C (VSPR case)).

Table 25.36 shows the spaces for which entries can be made. Note that if the module that references that space is operating, write accesses to the relevant space are prohibited. For example, while RPF2 is operating, accesses to the entire space of VI6_CLUT2_TBL are prohibited. When a read access is made to the relevant space during operation of the referencing module, undefined values will be read out.

The operating/stopped state of each module in Table 25.36 is the operating state of the WPF to which each module is connected. Determine whether the module is operating or stopped using each WPF operating status bit in the VI6_STATUS register.

Table 25.36 CLUT Space and LUT Space Addresses

Space Name	Space Addresses	Entry Count	Module that References the Space in the Left Column
VI6_CLUT0_TBL	$VSP_BASE + H'4000 to $VSP_BASE + H'43FF	256	RPF0
VI6_CLUT1_TBL	$VSP_BASE + H'4400 to $VSP_BASE + H'47FF	256	RPF1
VI6_CLUT2_TBL	$VSP_BASE + H'4800 to $VSP_BASE + H'4BFF	256	RPF2
VI6_CLUT3_TBL	$VSP_BASE + H'4C00 to $VSP_BASE + H'4FFF	256	RPF3
VI6_CLUT4_TBL	$VSP_BASE + H'5000 to $VSP_BASE + H'53FF	256	RPF4
VI6_LUT_TBL	$VSP_BASE + H'7000 to $VSP_BASE + H'73FF	256	LUT

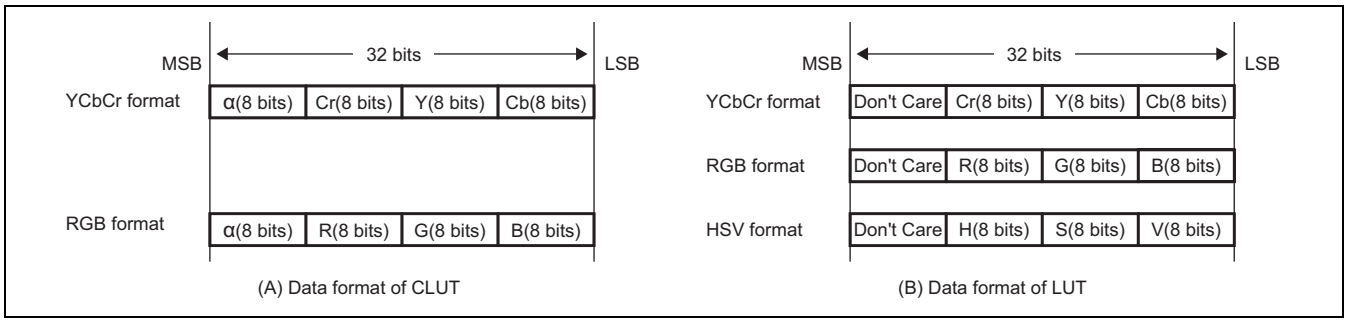


Figure 25.51 VI6_CLUT_TBL and VI6_LUT_TBL Formats

25.3.2 CLU Table

Data is set in the CLU table in the space shown in Table 25.37 through indirect addressing.

Table 25.37 CLU Space Addresses

Space Name	Space Addresses	Module that References the Space in the Left Column
VI6_CLU_TBL	$VSP_BASE + H'7400 to $VSP_BASE + H'7407	CLU

The addresses used in indirect addressing (VI6_CLU_ADDR, VI6_CLU_DATA) are shown in Table 25.38. The CLU table can be accessed by setting the VI6_CLU_ADDR register and then reading from or writing to the VI6_CLU_DATA register. To write-access the CLU table continuously, such as when setting data to the CLU table, perform the following.

(1) Set the first CLU table coordinates in VI6_CLU_ADDR.
(2) Write the first data to be set in VI6_CLU_DATA.
(3) Set the next CLU table coordinates in VI6_CLU_ADDR.
(4) Write the next data to be set in VI6_CLU_DATA.
... Execute these processes in a similar manner.

Accesses to VI6_CLU_ADDR and VI6_CLU_DATA registers are repeated in this way. The location where to access the CLU table to write the VI6_CLU_DATA contents immediately takes effect after a value is set in the VI6_CLU_ADDR register.

To read-access the CLU table continuously, change the write-access operation to the read-access operation in the sequence of processes of (1) to (4) above.

The following describes how to specify VI6_CLU_ADDR.

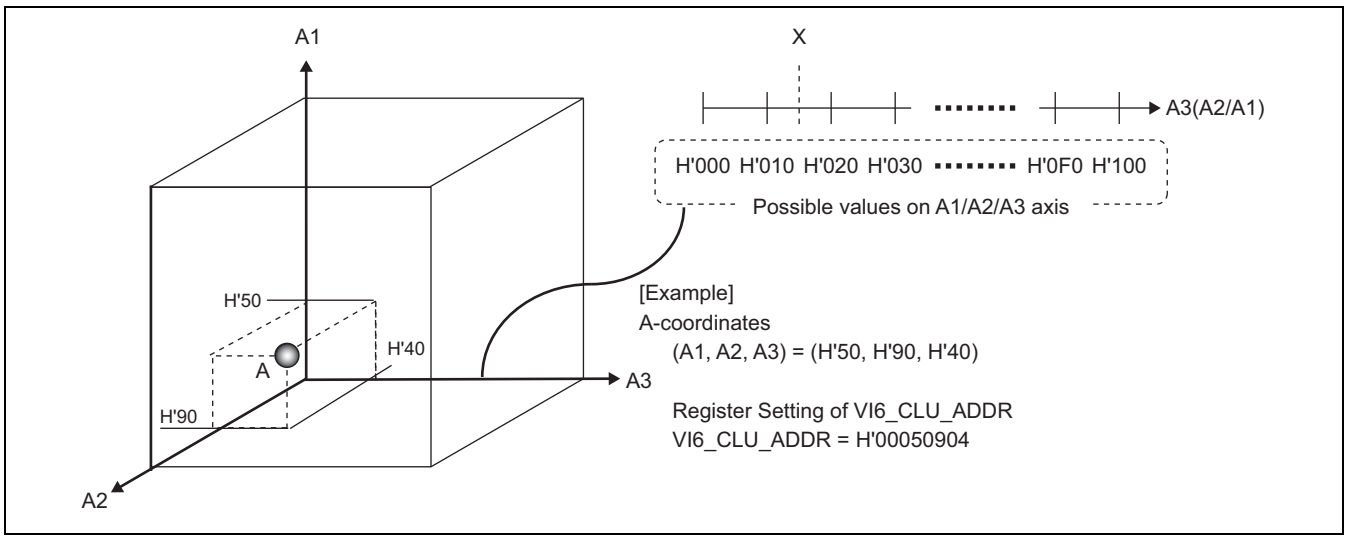


Figure 25.52 VI6_CLU_ADDR Setting

In the CLU table, a table value should be specified for every increase by H'10 along each of the axes and for every intersection between two axes. For a certain axis, as shown in the top right of Figure 25.52, a value to be set in the table corresponds to a scale mark at an interval of H'10. The location of a point between two scale marks (for example, point X in Figure 25.52) is calculated through interpolation by the CLU (refer to section 25.2.13.1). Accordingly, the lower four bits of table settings for each axis has no meaning; only the upper-order five bits of the desired coordinate for each component should be specified in VI6_CLU_ADDR (which should be shifted to the right by four bits) as shown in Figure 25.52.

Table 25.38 Address Spaces Used in Indirect Addressing to CLU Table

Address (Name)	Bit	Initial Value	R/W	Description
$VSP_BASE + H'7400 (VI6_CLU_ADDR)	31 to 24	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
	23 to 16	H'00	R/W	Coordinate Value of First Axis These bits set the coordinate value of the first axis on the three-dimensional space coordinates of the CLU table. A value from 0 to 16 can be specified.
	15 to 8	H'00	R/W	Coordinate Value of Second Axis These bits set the coordinate value of the second axis on the three-dimensional space coordinates of the CLU table. A value from 0 to 16 can be specified.
	7 to 0	H'00	R/W	Coordinate Value of Third Axis These bits set the coordinate value of the third axis on the three-dimensional space coordinates of the CLU table. A value from 0 to 16 can be specified when the CLU is in 3D mode. In 2D mode, these bits must be set to 0.
$VSP_BASE + H'7404 (VI6_CLU_DATA)	31 to 24	Undefined	R	Reserved These bits are always read as 0. The write value should always be 0.
	23 to 16	Undefined	R/W	Component Value of First Axis These bits set the component value of the first axis on the three-dimensional space coordinates of the CLU table, which is defined by the VI6_CLU_ADDR register. A value from 0 to 255 can be specified when the CLU is in 3D mode. In 2D mode, these bits must be set to 0.
$VSP_BASE + H'7404 (VI6_CLU_DATA)	15 to 8	Undefined	R/W	Component Value of Second Axis These bits set the component value of the second axis on the three-dimensional space coordinates of the CLU table, which is defined by the VI6_CLU_ADDR register. A value from 0 to 255 can be specified.
	7 to 0	Undefined	R/W	Component Value of Third Axis These bits set the component value of the third axis on the three-dimensional space coordinates of the CLU table, which is defined by the VI6_CLU_ADDR register. A value from 0 to 255 can be specified when the CLU is in 3D mode. In 2D mode, these bits must be set to 0.

25.4 Operation Linked with Display Unit (DU)

25.4.1 Starting LCD Display

Use the following procedure to display images on the LCD by operating the VSP1 and DU together.

To display images on the LCD by inputting VSYNC to the DU:

(1) Activate the VSP1.
(2) After the VSP1 starts operation, wait until a VI6_DISP_IRQ_STA.DST interrupt source is generated.
(3) After a VI6_DISP_IRQ_STA.DST interrupt source is generated, activate the DU.

To display images on the LCD with VSYNC being output from the DU:

(1) Activate the VSP.
(2) After that, activate the DU.

25.4.2 Stopping LCD Display

To stop the image display on the LCD while the VSP1 and DU work together to display images, stop the DU first by a software reset or the like (refer to section 24, Display Unit (DU) for the software reset of the DU). After checking that the DU has stopped, apply software reset to the VSP1. After both the DU and VSP1 software reset processes are complete, the LCD display stop process ends.

25.4.3 Entire Operation Flow

The VSP1 operation is linked with the DU operation. As the DU operates in real-time, the VSP1 also operates in real-time. However, the VSP1 only provides one plane of registers. Accordingly, modifying registers between frames should be done within the short blanking period between the end of one-frame display (VI6_WPFn_IRQ_STA.FRE interrupt) and the start of the next frame display (VSYNC). To do this, use the display list function of the VSP1 (see section 25.1.8 (3)) to implement two virtual register planes and ensure the one-frame time for modifying registers by software (see section 25.4.4). When using the display list function, make the current-frame settings in a register plane and store the next-frame settings as a display list in external memory such as SDRAM. In this way, the next-frame settings can be modified in the display list in external memory until the end of the current frame processing.

The timing chart of this procedure is shown in Figure 25.53

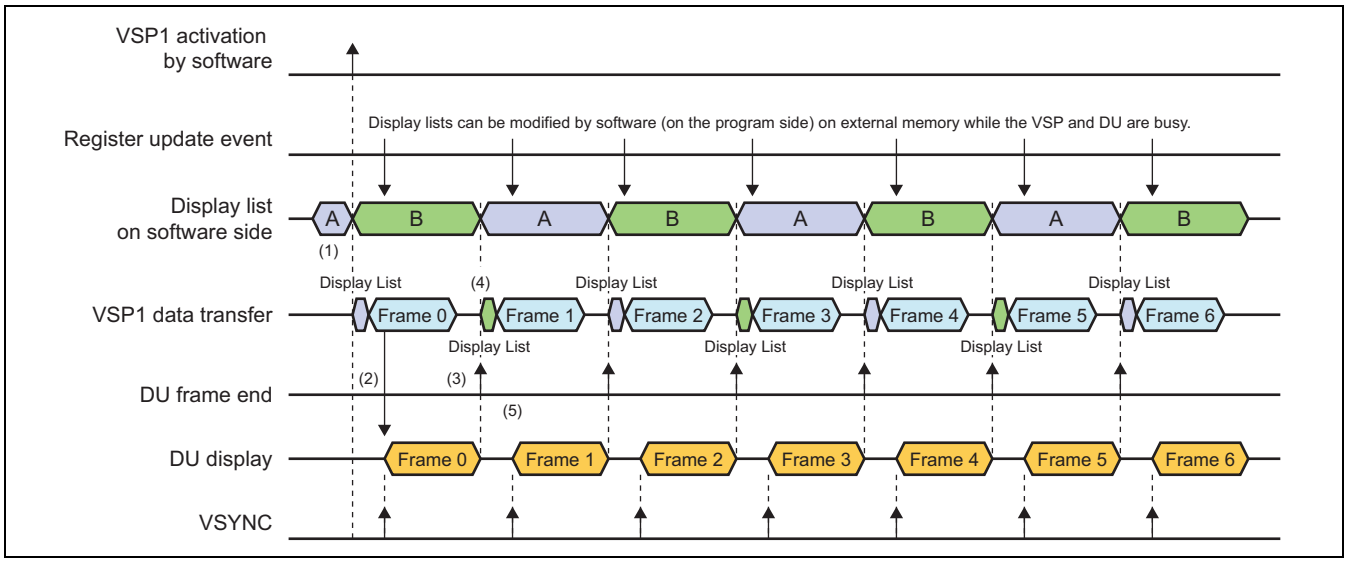


Figure 25.53 Timing when VSP1 Operation is linked with DU

(1) The VSP1 is activated by software, and then the VSP1 downloads a display list.
(2) The VSP1 informs the ready state to the DU, and then the DU starts the display process.
(3) The DU generates a frame end interrupt.
(4) The VSP updates its register settings by downloading the next display list. After that, the VSP reads the next frame data.
(5) The DU generates VSYNC for the next frame and starts transfer of display data.

Figure 25.53 shows the detailed timing of frame switching. The number of VSP1 operating clock cycles necessary for each timing is shown as a reference value in Figure 25.54 where it is assumed that the bus transfer is at the logically fastest speed and the size of the display list to be downloaded is the worst case (downloading of data for all registers and tables in the VSP1).

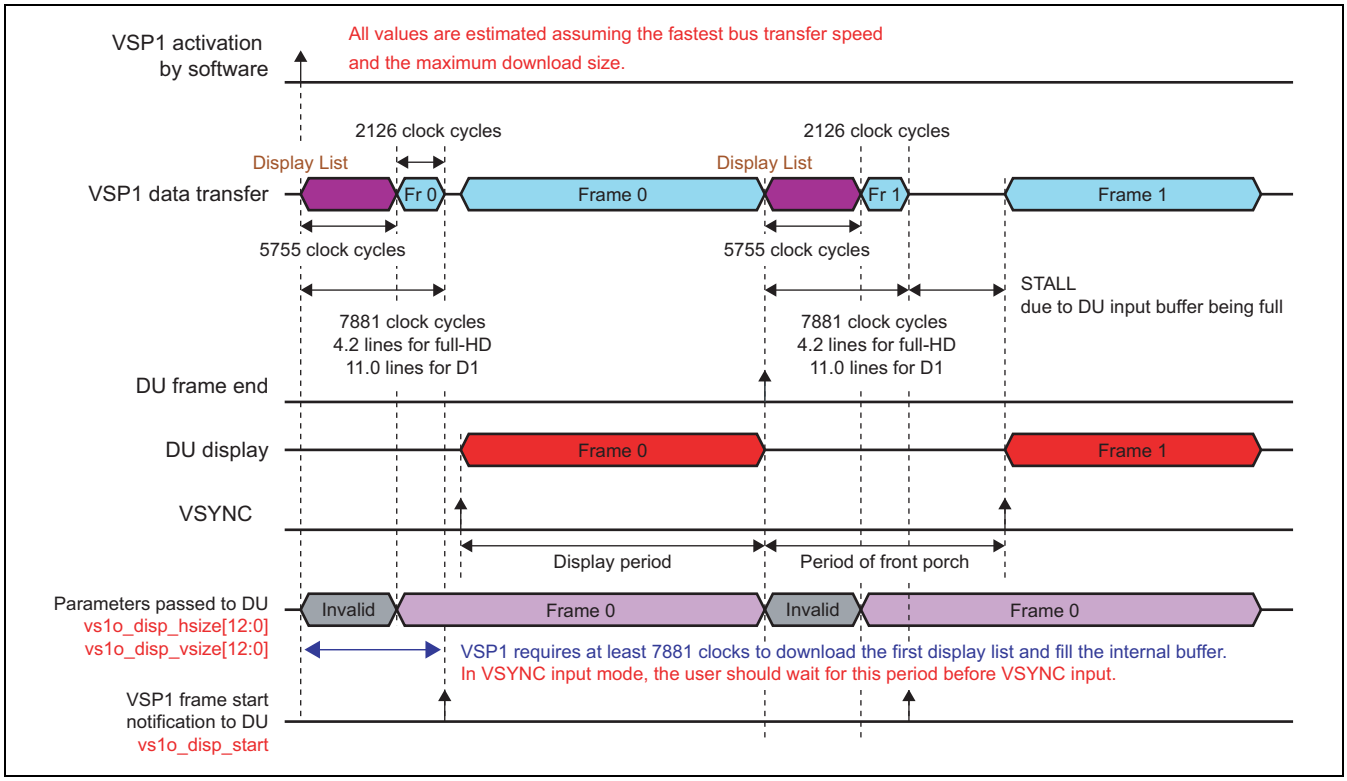
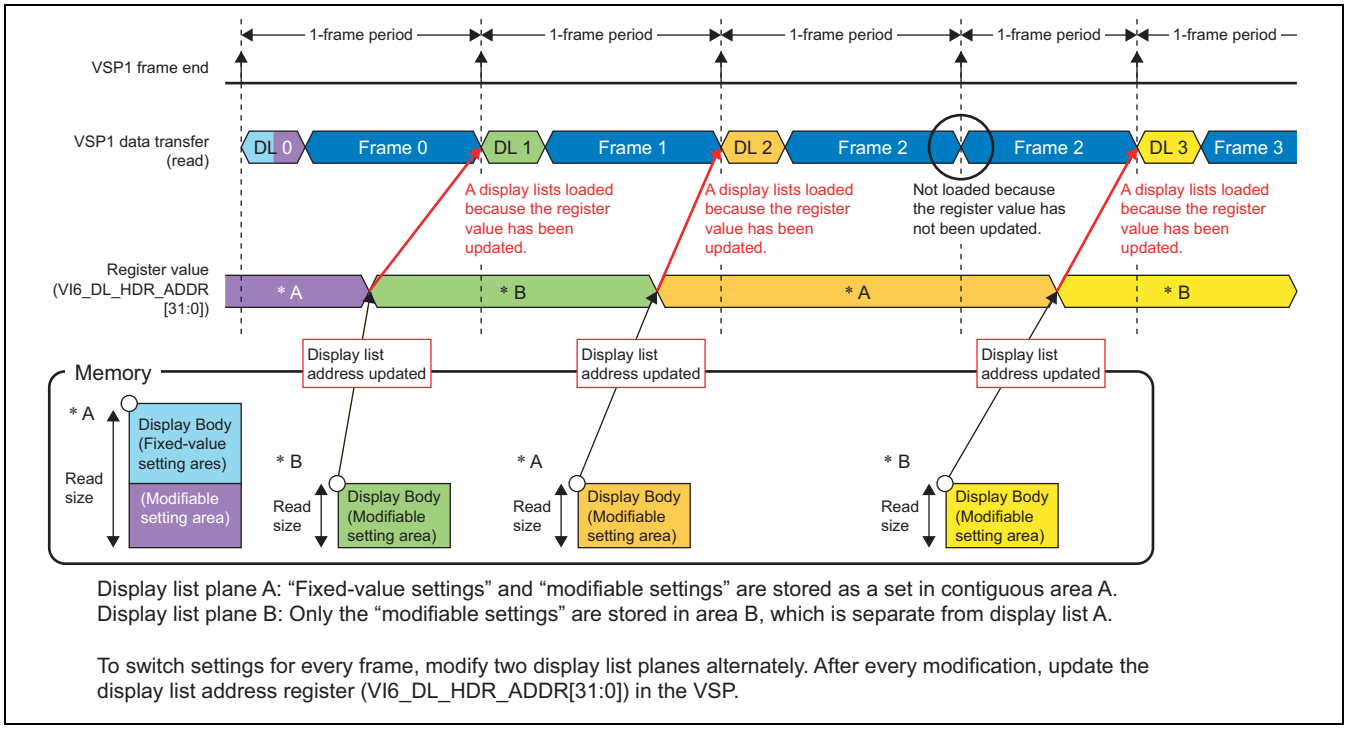


Figure 25.54 Detailed Timing of Frame Switching

25.4.4 Controlling Two Register Planes Using Display Lists

Figure 25.55 shows the control of two register planes using header-less display lists (see section 25.1.8 (3)) and its timing. In the description hereafter, the use of header-less display lists is always assumed and they are simply called display lists.



Display list plane A: “Fixed-value settings” and “modifiable settings” are stored as a set in contiguous area A.
Display list plane B: Only the “modifiable settings” are stored in area B, which is separate from display list A.

To switch settings for every frame, modify two display list planes alternately. After every modification, update the display list address register (VI6_DL_HDR_ADDR[31:0]) in the VSP.

Figure 25.55 Controlling Two Register Planes Using a Display List

The VSP1 downloads a display list immediately after activation. In the start frame, download the display list that contains all necessary settings. From the next frame on, only the necessary register or table values should be specified in a display list.

Only when the destination address (VI6_DL_HDR_ADDR0; see section 25.2.6.2) or the display body size (VI6_DL_BODY_SIZE0; see section 25.2.6.5) has been written to, the VSP1 downloads a new display list at the start of the next frame. When the update flag of VI6_DL_BODY_SIZE0.UPD0 is set to 0, the register settings acquired from the display list previously downloaded are retained and used for the next operation without downloading a new display list.

25.5 Assignment in Memory Space

Make sure that VSP1 memory space shall be mapped to Non-Cache region.

26. Image Extraction Direct Memory Access Controller (2D-DMAC)

This LSI has an image extraction direct memory access controller (2D-DMAC). This module reads the image data in the frame buffer memory, performs image extraction/shift/simple magnification and format conversion, and then rewrites the processed image data to the frame buffer memory.

26.1 Features

- Image extraction

  2D-DMAC extracts an image in the rectangular area from a point (Sx, Sy) shifting from the source image data origin to a point in the frame memory, and then writes the extracted image data to another frame memory. Extraction of data is possible in two-pixel units for YCbCr formats and in one-pixel units for RGB formats. This function is available for image clipping and image motion compensation.
- Image rotation/inversion

  Vertical/horizontal inversion and the 90°/270° rotation can be performed.
- Simple enlargement

  When writing a destination image, it can simply be enlarged twice in the X and Y directions.
- Format conversion

  RGB formats can be converted to each other.

  YCbCr formats (YCbCr4:2:0 and YCbCr4:2:2) can be converted to each other.

  No format conversion is possible between RGB and YCbCr.

  The format conversion method is equivalent to that of VSP.
- Channels

  Settings for eight channels are enabled. For the YCbCr formats, settings for one channel for each Y plane and C plane are enabled. Therefore, concurrent processing is possible for up to four planes (YCbCr formats) or up to eight planes (RGB formats).

  Provided with an outstanding buffer for each channel, even if data transfer of a channel is blocked, 2D-DMAC can continue operation of other channels. Transition of processing between channels is performed upon completion of each line processing.
- Interrupt

  Each channel has interrupt request signals that can be output at the time of data transfer half end and data transfer end respectively.

Figure 26.1 shows a block diagram of 2D-DMAC and Figure 26.2 shows a flow for the pixel processing block.

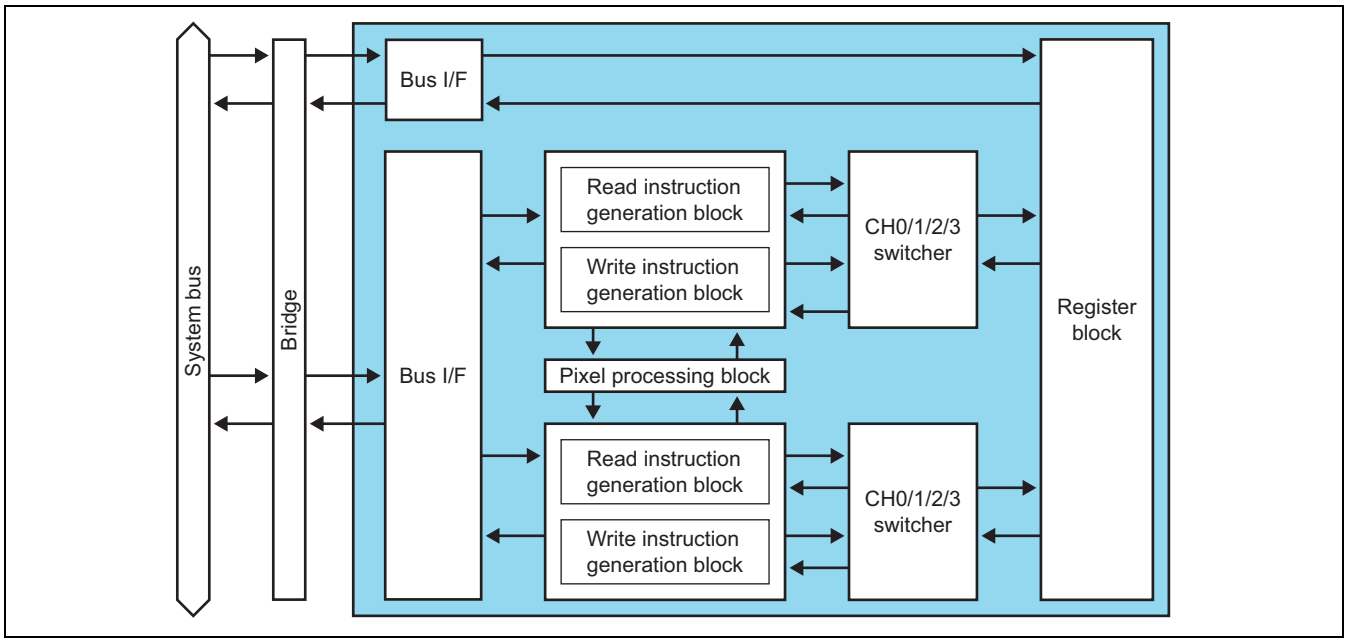


Figure 26.1 Block Diagram of 2D-DMAC

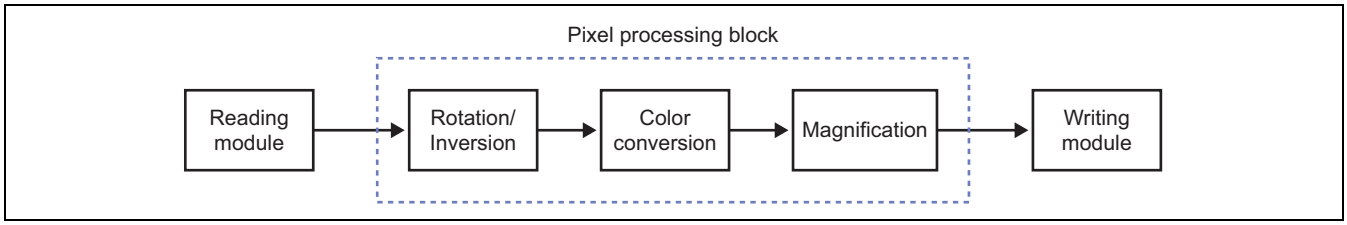


Figure 26.2 Block Flow of Pixel Block

26.2 Register Descriptions

Table 26.1 lists the registers used in 2D-DMAC. Table 26.2 shows the register status in each processing mode.

Table 26.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
Transaction control register	CHTCTRL	R/W	H'FEA0 0008	32
Interrupt status clear register	CHSTCLR	R/W	H'FEA0 0010	32
CH0 control register	CH0CTRL	R/W	H'FEA0 0020	32
CH1 control register	CH1CTRL	R/W	H'FEA0 0024	32
CH2 control register	CH2CTRL	R/W	H'FEA0 0028	32
CH3 control register	CH3CTRL	R/W	H'FEA0 002C	32
CH4 control register	CH4CTRL	R/W	H'FEA0 0120	32
CH5 control register	CH5CTRL	R/W	H'FEA0 0124	32
CH6 control register	CH6CTRL	R/W	H'FEA0 0128	32
CH7 control register	CH7CTRL	R/W	H'FEA0 012C	32
CH0 input/output swap register	CH0SWAP	R/W	H'FEA0 0030	32
CH1 input/output swap register	CH1SWAP	R/W	H'FEA0 0034	32
CH2 input/output swap register	CH2SWAP	R/W	H'FEA0 0038	32
CH3 input/output swap register	CH3SWAP	R/W	H'FEA0 003C	32
CH4 input/output swap register	CH4SWAP	R/W	H'FEA0 0130	32
CH5 input/output swap register	CH5SWAP	R/W	H'FEA0 0134	32
CH6 input/output swap register	CH6SWAP	R/W	H'FEA0 0138	32
CH7 input/output swap register	CH7SWAP	R/W	H'FEA0 013C	32
CH0 source address register	CH0SAR	R/W	H'FEA0 0080	32
CH0 destination address register	CH0DAR	R/W	H'FEA0 0084	32
CH0 destination pixel register	CH0DPXL	R/W	H'FEA0 0088	32
CH0 source format register	CH0SFMT	R/W	H'FEA0 008C	32
CH0 destination format register	CH0DFMT	R/W	H'FEA0 0090	32
CH0 source line address register	CH0SARE	R	H'FEA0 0094	32
CH0 destination line address register	CH0DARE	R	H'FEA0 0098	32
CH0 destination pixel processing Register	CH0DPXLE	R	H'FEA0 009C	32
CH1****	CH1****	—	H'FEA0 00A0 to H'FEA0 00BC	32
CH2****	CH2****	—	H'FEA0 00C0 to H'FEA0 00DC	32
CH3****	CH3****	—	H'FEA0 00E0 to H'FEA0 00FC	32
CH4****	CH4****	—	H'FEA0 0180 to H'FEA0 019C	32
CH5****	CH5****	—	H'FEA0 01A0 to H'FEA0 01BC	32
CH6****	CH6****	—	H'FEA0 01C0 to H'FEA0 01DC	32
CH7****	CH7****	—	H'FEA0 01E0 to H'FEA0 01FC	32

Table 26.2 Register Status in Each Processing Mode

Abbreviation	Power-on Reset	Module Standby
CHSTCLR	Initialized	Retained
CHnCTRL	Initialized	Retained
CHnSWAP	Initialized	Retained
CHnSAR	Initialized	Retained
CHnDAR	Initialized	Retained
CHnDPXL	Initialized	Retained
CHnSFMT	Initialized	Retained
CHnDFMT	Initialized	Retained
CHnSARE	Initialized	Retained
CHnDARE	Initialized	Retained
CHnDPXLE	Initialized	Retained

Note: n = 0 to 7

26.2.1 Transaction Control Register (CHTCTRL)

CHTCTRL register is a 32-bit readable/writable register that controls bus transaction among all channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	OUT	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
5	OUT	0	R/W	Transaction control When operating 2D-DMAC, this bit should always be 1.
4 to 0	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.

26.2.2 Control Registers (CHnCTRL)

CHnCTRL (n = 0 to 7) is a 32-bit readable/writable register that controls transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HMRR	VMRR	ROTL	ROTR	—	MX	—	MY	HIE	HE	TIE	TE	LINK[1] / —	LINK[0] / —	STP	DMAEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	HMRR	0	R/W	Horizontal Inversion (symmetric to the vertical axis) The source image inverted horizontally is output. See Table 26.5 for details on the relations between this bit and inversion/rotation. 0: Horizontal inversion is not performed. 1: Inverted horizontally source image is output.
14	VMRR	0	R/W	Vertical Inversion (symmetric to the horizontal axis) The source image inverted vertically is output. See Table 26.5 for details on the relations between this bit and inversion/rotation. 0: Vertical inversion is not performed. 1: Inverted vertically source image is output.
13	ROTL	0	R/W	270° Rotation (clockwise) The source image rotated 270° is output. When this bit is 1, set the ROTR bit to 0. See Table 26.5 for details on the relations between this bit and inversion/rotation. 0: 270° rotation is not performed. 1: Rotated 270° source image is output.
12	ROTR	0	R/W	90° Rotation (clockwise) The source image rotated 90° is output. When this bit is 1, set the ROTR bit to 0. See Table 26.5 for details on the relations between this bit and inversion/rotation. 0: 90° rotation is not performed. 1: Rotated 90° source image is output.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
10	MX	0	R/W	Magnify X Direction 0: No magnification 1: Outputs with double magnification in the X direction. When ROTR or ROTL is 1, set this bit to 0.
9	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	MY	0	R/W	Magnify Y Direction 0: No magnification 1: Outputs with double magnification in the Y direction. When ROTR or ROTL is 1, set this bit to 0.
7	HIE	0	R/W	Half End Interrupt Enable Specifies whether to output the half end flag as an interrupt request. 0: A half end interrupt is disabled. 1: A half end interrupt is enabled.
6	HE	0	R/W	Half End Indicates that data transfer for half the setting lines has been completed. This bit is set to 1 when the DVPXLE bit in CHnDPXLE becomes half (a value of 1-bit right shift) of the DVPXL bit value in CHnDPXL that was set before starting transfer. If CHnCTRL.ROTR = 1 or CHnCTRL.ROTL = 1, this bit is set to 1 when the DHPXLE bit in CHnDPXLE becomes half of the DHPXL bit value in CHnDPXL that was set before starting transfer. Only clearing to 0 after reading 1 is enabled. Clearing by the CHSTCLR register is also enabled.
5	TIE	0	R/W	Transfer End Interrupt Enable Specifies whether to output the transfer end flag as an interrupt request. 0: A transfer end interrupt is disabled. 1: A transfer end interrupt is enabled.
4	TE	0	R/W	Transfer End This bit is set to 1 when the DVPXL bit in CHxDPXL that was set by the DVPXLE bit in CHxDPXLE before starting transfer and the entire DMA transfer are completed. When this bit is set to 1, the DMAEN bit is automatically cleared. Only clearing to 0 after reading 1 is enabled. Clearing by the CHSTCLR register is also enabled.
3, 2	LINK[1:0] (n = 0, 2, 4, 6) — (n = 1, 3, 5, 7)	00	R/W (n = 0, 2, 4, 6) R (n = 1, 3, 5, 7)	(n = 0, 2, 4, 6) Link Transfer Mode This mode enables alternate block line transfers between a master channel (CHn) and a slave channel (CHn+1). When these bits are set to 10, specify the DVPXL bit in CH(n+1)DPXL equal to half of the DVPXL in CHnDPXL. When these bits are set to 11, specify the DVPXL bit in CH(n+1)DPXL equal to the DVPXL in CHnDPXL. In this mode, start the transfer of the master channel before that of the slave channel. 00: Link transfer mode is disabled. 01: Setting prohibited. 10: A block line transfer of a slave channel is performed every two block line transfers of a master channel. 11: Alternate transfers are performed. (n = 1, 3, 5, 6) Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	STP	0	R/W	Transfer Stop Stops DMA transfer temporarily. When this bit is set to 1, DMA transfer is suspended upon completion of the line that is being transferred, and the DMAEN bit is cleared to 0. At this time, this bit is also cleared. To restart DMA transfer after that, set the DMAEN bit to 1. To reset the operation of a channel, rewrite data to the SAR, DAR, and DPXL registers of the channel. [Writing] 0: NOP 1: Stops DMA transfer temporarily. [Reading] 0: Transfer is in progress or suspended. 1: Pending until the line being transferred is completed
0	DMAEN	0	R/W	DMA Transfer Enable Enables DMA transfer. Only writing 1 is enabled. This bit shows 1 during transfer, and is automatically cleared when a DMA transfer is completed. Writing 0 to this bit is disabled. A DMA transfer can be suspended by setting the STP bit to 1. [Writing] 0: NOP 1: Performs DMA transfer. [Reading] 0: No DMA transfer is in progress. 1: A DMA transfer is in progress.

26.2.3 Input/Output Swap Register (CHnSWAP)

CHnSWAP (n = 0 to 7) controls 64-bit data swapping in the data input/output section of 2D-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	OLS	OWS	OBS	—	ILS	IWS	IBS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	OLS	0	R/W	Output Longword Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in longword units. 0: Output longword swap is not performed. 1: Output longword swap is performed.
5	OWS	0	R/W	Output Word Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in word units. 0: Output word swap is not performed. 1: Output word swap is performed.
4	OBS	0	R/W	Output Byte Swap Setting In the output section of 2D-DMAC, 64 bits of data are swapped with 16-bit groups in byte units. 0: Output byte swap is not performed. 1: Output byte swap is performed.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2	ILS	0	R/W	Input Longword Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in longword units. 0: Input longword swap is not performed. 1: Input longword swap is performed.
1	IWS	0	R/W	Input Word Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 32 bits of the MSB and 32 bits of the LSB in word units. 0: Input word swap is not performed. 1: Input word swap is performed.
0	IBS	0	R/W	Input Byte Swap Setting In the input section of 2D-DMAC, 64 bits of data are swapped with 16-bit groups in byte units. 0: Input byte swap is not performed. 1: Input byte swap is performed.

When the system is operated in little-endian mode, this register should be used to select the swapping method conforming to the input/output format. The data relationships available when swapping methods are set are shown in Figure 26.3, Figure 26.4, and Figure 26.5.

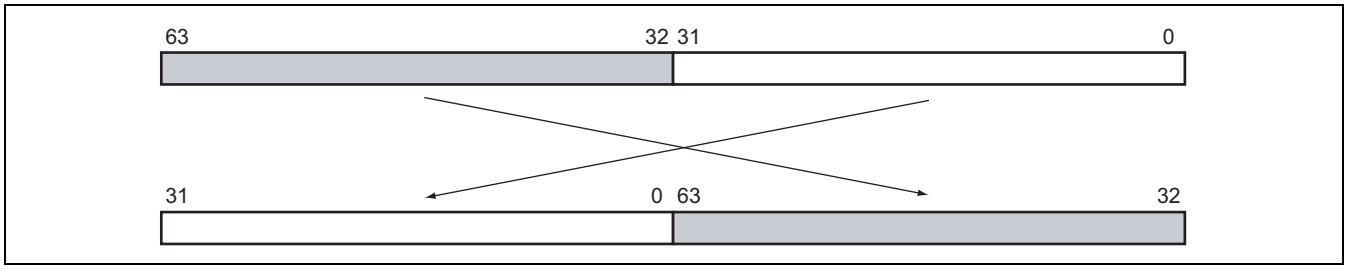


Figure 26.3 Data Relationship Before and After Longword Swapping

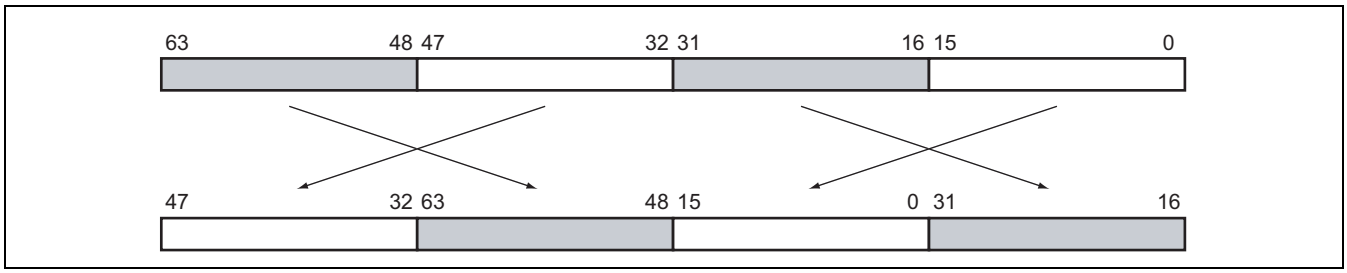


Figure 26.4 Data Relationship Before and After Word Swapping

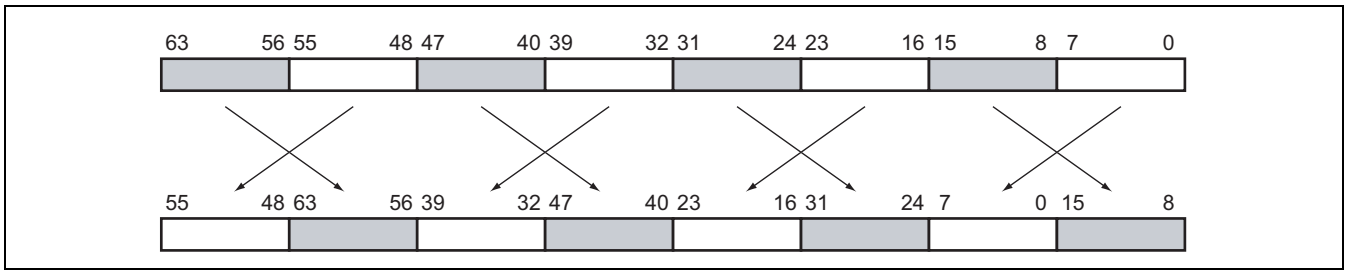


Figure 26.5 Data Relationship Before and After Byte Swapping

26.2.4 Source Format Registers (CHnSFMT)

CHnSFMT (n = 0 to 7) is a 32-bit readable/writable register for setting the source image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HWTH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MD[1:0]		PKF[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

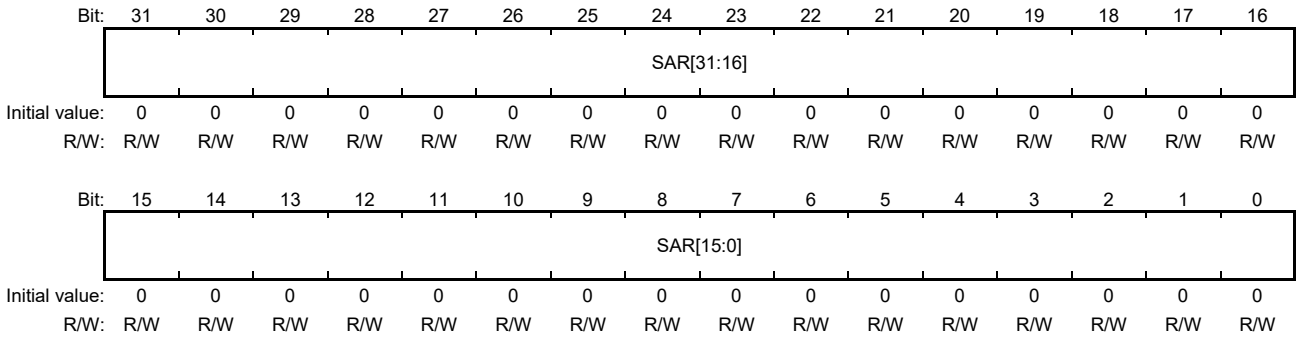
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HWTH[15:0]	H'0000	R/W	Source Image Horizontal Byte Size Specify the one-line width of the source image in units of bytes. This value should be a multiple of the pack size. When ROTR or ROTL is 1, set these bits to 16n.
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	MD[1:0]	00	R/W	Source Image Format 00: RGB data 01: Y data 10: CbCr data (YCbCr4:2:0) 11: CbCr data (YCbCr4:2:2)
4 to 0	PKF[4:0]	00000	R/W	Source Image RGB Data Packed Format Specify the packed format for source image data in the RGB format. These bits are available only when MD = 00. Table 26.3 shows the packed RGB formats.

Table 26.3 Packed RGB Formats

PKF[4:0]	Format	Bit Rate [bpp]	Phase	Bit field																																	
				31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
B'00000	ARGB8888	24	—	a	a	a	a	a	a	a	a	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0
B'00001	RGBA8888	24	—	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	a	a	a	a	a	a	a	a
B'00010	RGB888	24	0	R0	R0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0	B0	B0	R1	R1	R1	R1	R1	R1	R1	R1
			1	G1	G1	G1	G1	G1	G1	G1	G1	B1	B1	B1	B1	B1	B1	B1	B1	R2	R2	R2	R2	R2	R2	R2	R2	G2	G2	G2	G2	G2	G2	G2	G2
			2	B2	B2	B2	B2	B2	B2	B2	B2	R3	R3	R3	R3	R3	R3	R3	R3	G3	G3	G3	G3	G3	G3	G3	G3	B3	B3	B3	B3	B3	B3	B3	B3
B'00011	RGB565	16	—																	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0
B'00100	RGB332	8	—																									R0	R0	R0	G0	G0	G0	B0	B0
B'00111	pRGB14-666	18	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0	B0
B'01000	pRGB4-444	12	—																	0	0	0	0	R0	R0	R0	R0	G0	G0	G0	G0	B0	B0	B0	B0
B'01001	RGB666	18	0	0	0	R0	R0	R0	R0	R0	R0	0	0	G0	G0	G0	G0	G0	G0	0	0	B0	B0	B0	B0	B0	B0	0	0	R1	R1	R1	R1	R1	R1
			1	0	0	G1	G1	G1	G1	G1	G1	0	0	B1	B1	B1	B1	B1	B1	0	0	R2	R2	R2	R2	R2	R2	0	0	G2	G2	G2	G2	G2	G2
			2	0	0	B2	B2	B2	B2	B2	B2	0	0	R3	R3	R3	R3	R3	R3	0	0	G3	G3	G3	G3	G3	G3	0	0	B3	B3	B3	B3	B3	B3
B'01010	BGR666	18	0	0	0	B0	B0	B0	B0	B0	B0	0	0	G0	G0	G0	G0	G0	G0	0	0	R0	R0	R0	R0	R0	R0	0	0	B1	B1	B1	B1	B1	B1
			1	0	0	G1	G1	G1	G1	G1	G1	0	0	R1	R1	R1	R1	R1	R1	0	0	B2	B2	B2	B2	B2	B2	0	0	G2	G2	G2	G2	G2	G2
			2	0	0	R2	R2	R2	R2	R2	R2	0	0	B3	B3	B3	B3	B3	B3	0	0	G3	G3	G3	G3	G3	G3	0	0	R3	R3	R3	R3	R3	R3
B'01011	BGR888	24	0	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0	B1	B1	B1	B1	B1	B1	B1	B1
			1	G1	G1	G1	G1	G1	G1	G1	G1	R1	R1	R1	R1	R1	R1	R1	R1	B2	B2	B2	B2	B2	B2	B2	B2	G2	G2	G2	G2	G2	G2	G2	G2
			2	R2	R2	R2	R2	R2	R2	R2	R2	B3	B3	B3	B3	B3	B3	B3	B3	G3	G3	G3	G3	G3	G3	G3	G3	R3	R3	R3	R3	R3	R3	R3	R3
B'01100	ABGR888	24	—	a	a	a	a	a	a	a	a	B0	B0	B0	B0	B0	B0	B0	B0	G0	G0	G0	G0	G0	G0	G0	G0	R0	R0	R0	R0	R0	R0	R0	R0
B'01101	RGB565	16	—	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	R0	R0	R0	R0	R0	G0	G0	G0	G0	G0	G0	B0	B0	B0	B0	B0

26.2.5 Source Address Registers (CHnSAR)

CHnSAR (n = 0 to 7) is a 32-bit readable/writable register for setting the transfer start address of the source image.



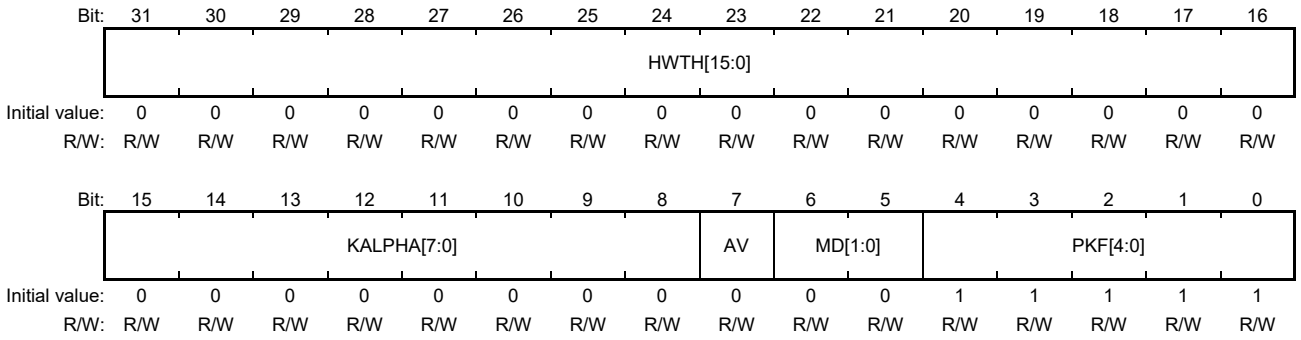
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR[31:0]	H'00000000	R/W	Source Image Extraction Start Address Specify the address of the extraction start pixel in the source image data.

When the source image fills CHnSAR ≠ 16n and cutting out effective pixel bytes number ≤ 16-byte, line finality access = address where line terminal address is rounded up to 16n + 16-byte.

Address where source image final pixel address of cutting out object is rounded up to 16n + 16, secure it as an input image area.

26.2.6 Destination Format Registers (CHnDFMT)

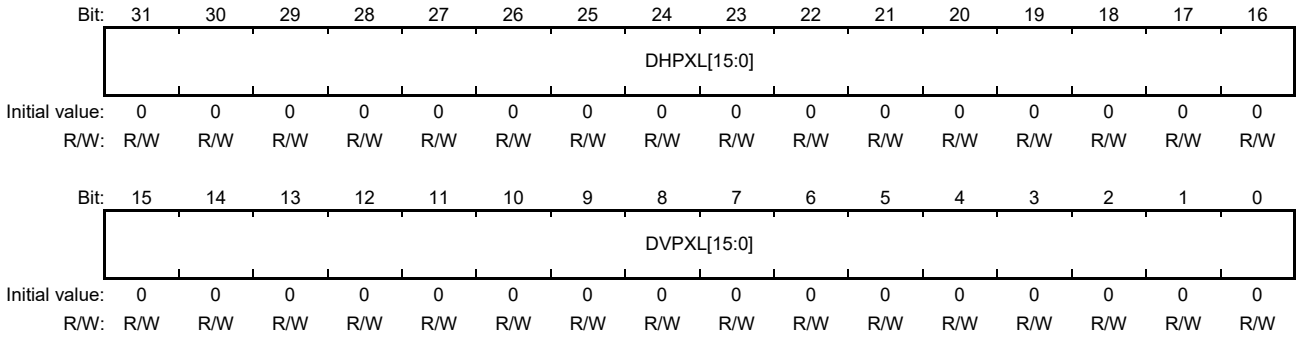
CHnDFMT (n = 0 to 7) is a 32-bit readable/writable register for setting a destination image format and so on.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	HWTH[15:0]	H'0000	R/W	Destination Image Horizontal Byte Size Specify the one-line width of the destination image in units of bytes. Set a multiple of 16. When CTRL.MX is 1, set a value after magnification.
15 to 8	KALPHA[7:0]	H'00	R/W	Alpha Value Specify an alpha value used for output if the source image is in a format without alpha or the AV bit is set to 0.
7	AV	0	R/W	Alpha Enable 0: Disables the alpha value when the source image is in a format with alpha. When the output is in a format with alpha, the KALPHA value is output. 1: Enables the alpha value when the source image is in a format with alpha, and outputs the alpha value when the output is in a format with alpha.
6, 5	MD[1:0]	00	R/W	Destination Image Format 00: RGB data 01: Y data 10: CbCr data (YCbCr4:2:0) 11: CbCr data (YCbCr4:2:2)
4 to 0	PKF[4:0]	11111	R/W	Destination Image RGB Data Packed Format Specify the packed format for destination image data in the RGB format. These bits are available only when MD = 00. Table 26.3 shows the packed RGB formats.

26.2.7 Destination Pixel Registers (CHnDPXL)

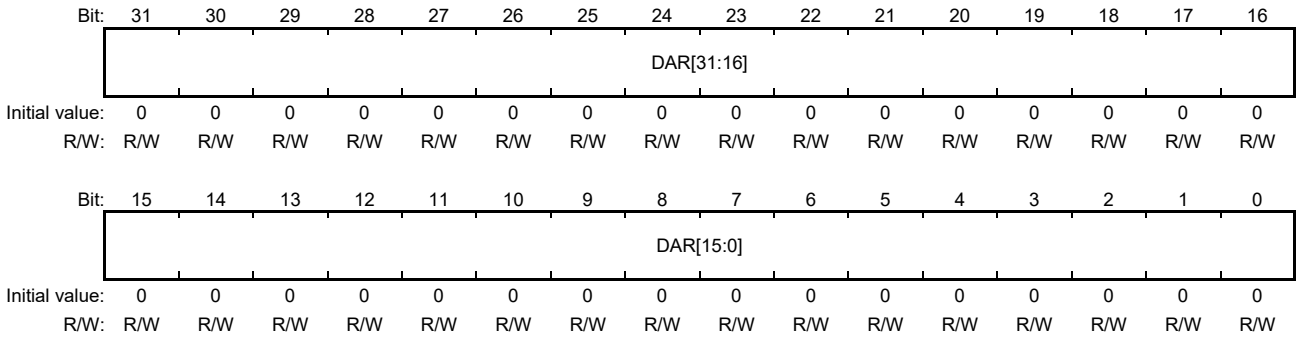
CHnDPXL (n = 0 to 7) is a 32-bit readable/writable register for setting the horizontal pixel size and vertical pixel size of the destination image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DHPXL[15:0]	H'0000	R/W	Destination Image Horizontal Pixel Size Specify the horizontal pixel size of the destination image. When the MX bit in CTRL is 1, set a value before magnification. For the CbCr plane in YCbCr4:2:2 or YCbCr4:2:0, set a value of half of the number of pixels. The minimum pixel size will be 1; set 1 or a larger value.
15 to 0	DVPXL[15:0]	H'0000	R/W	Destination Image Vertical Pixel Size Specify the vertical pixel size of the destination image. When the MY bit in CTRL is 1, set a value before magnification. For the CbCr plane in YCbCr4:2:0, set a value of half of the number of lines. The minimum pixel size will be 1; set 1 or a larger value.

26.2.8 Destination Address Registers (CHnDAR)

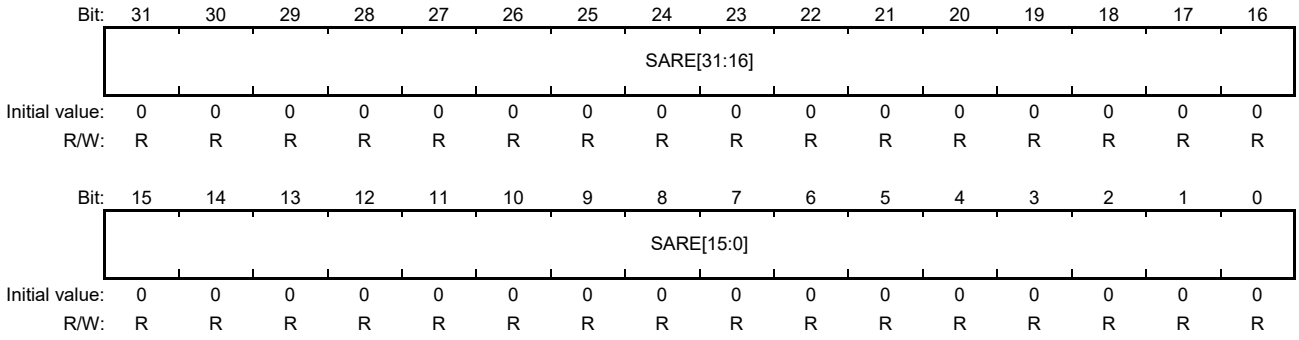
CHnDAR (n = 0 to 7) is a 32-bit readable/writable register for setting the transfer start address of the destination image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR[31:0]	H'00000000	R/W	Specify the start address of the destination image. Only a multiple of 16 can be set. The specified address point is to be changed according to the settings to the VMRR, HMRR, ROTR, ROTL, and MY bits. For details, see section 26.3.2, Image Rotation/Inversion.

26.2.9 Source Line Address Registers (CHnSARE)

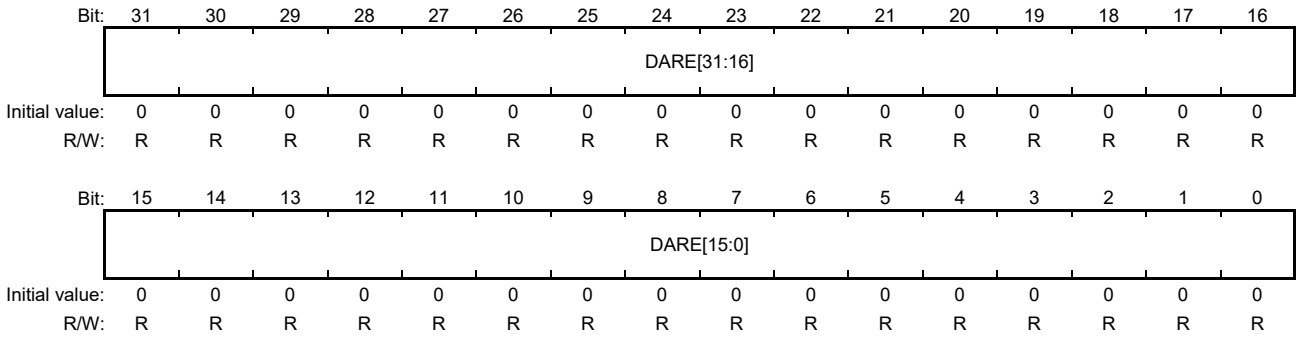
CHnSARE (n = 0 to 7) is a 32-bit read-only register that shows the start address of the line in processing of the source image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SARE [31:0]	H'00000000	R	This read-only register used for internal processing shows the start address of the line in processing of the source image.

26.2.10 Destination Line Address Registers (CHnDARE)

CHnDARE (n = 0 to 7) is a 32-bit read-only register that shows the start address of the line in processing of the destination image.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DARE [31:0]	H'00000000	R	This read-only register used for internal processing shows the start address of the line in processing of the destination image.

26.2.11 Destination Pixel Processing Registers (CHnDPXLE)

CHnDPXLE (n = 0 to 7) is a 32-bit read-only register that shows the number of unprocessed lines of the destination image.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DHPXLE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DVPXLE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	DHPXLE[15:0]	H'0000	R	This read-only register used for internal processing shows the number of unprocessed horizontal lines of the destination image.
15 to 0	DVPXLE[15:0]	H'0000	R	This read-only register used for internal processing shows the number of unprocessed vertical lines of the destination image.

26.2.12 Interrupt Status Clear Register (CHSTCLR)

CHSTCLR is a register that indicates the status of HE and TE bits in each channel. By writing 1 in a bit in CHSTCLR, HE or TE bit in the corresponding channel is to be cleared.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHnHE[7:0]								CHnTE[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	CHnHE[7:0]	H'00	R/W	Indicates the status of the HE bit in CHnCTRL (n = 0 to 7). Writing 1 in this bit, the HE bit in corresponding channel is to be cleared. [Writing] 0: NOP 1: HE bit is cleared. [Reading] 0: 0 is set in the HE bit. 1: 1 is set in the HE bit.
7 to 0	CHnTE[7:0]	H'00	R/W	Indicates the status of the TE bit in CHnCTRL (n = 0 to 7). Writing 1 in this bit, the TE bit in corresponding channel is to be cleared. [Writing] 0: NOP 1: TE bit is cleared. [Reading] 0: 0 is set in the TE bit. 1: 1 is set in the TE bit.

26.3 Operation

This module can extract image data of required size from the source image and store it as a destination image, and also can convert the format, rotation/inversion, and magnify the image at that time.

26.3.1 Image Extraction

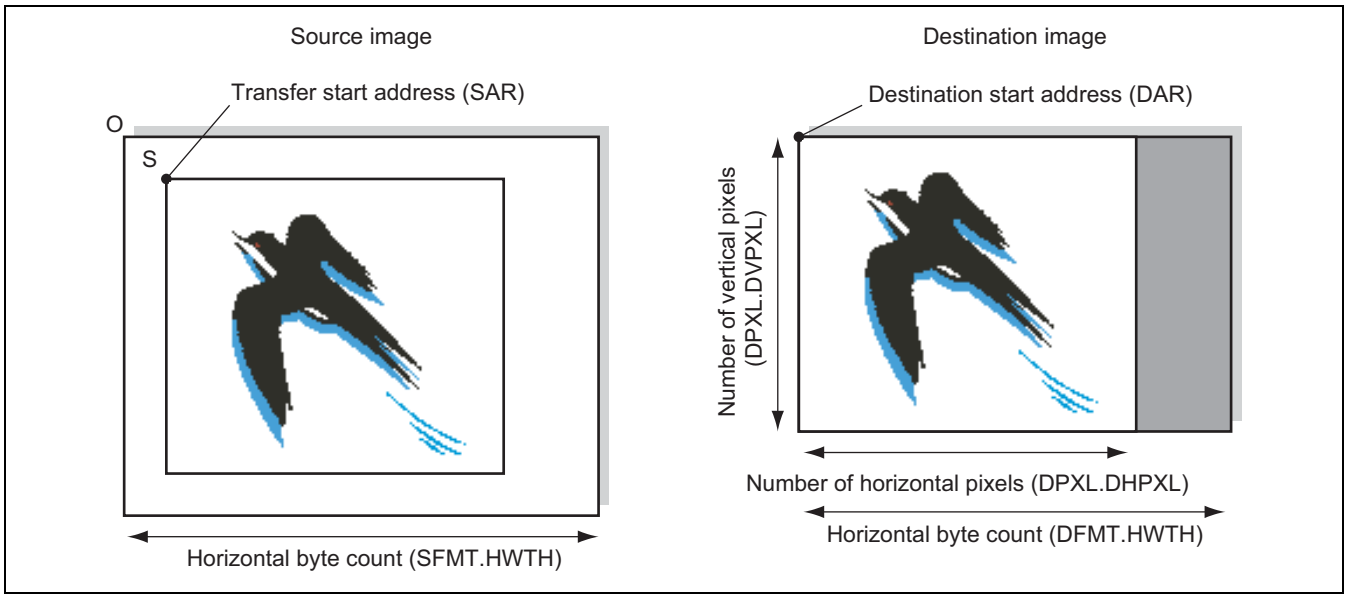


Figure 26.6 Schematic Diagram of Image Extraction

Figure 26.6 shows a schematic diagram of image extraction.

The image format conforms to the YCbCr4:2:0, YCbCr4:2:2, and RGB formats. Extraction of data is possible in two-pixel units for YCbCr formats and in one-pixel units for RGB formats. However, since the Y data and C data are independently stored in the memory in the YCbCr format, set them in different channels respectively.

For source images, the address of extraction start coordinates S and the horizontal byte size must be set in respective registers. Set the start address of the extraction start pixel in SAR. If the X coordinate of extraction start coordinates S (SAR) is an odd number with origin O in the YCbCr format, a deviation is generated between Y data and C data in the horizontal direction. Furthermore, in the YCbCr4:2:0 format, if the Y coordinate of extraction start coordinates S is an odd number with origin O, a deviation is generated between Y data and C data in the vertical direction. For each case, extract image data from the even pixel coordinates where truncation is made.

For destination images, destination start address, numbers of horizontal and vertical pixels, and the horizontal byte size must be set. Set an integer multiple of 16 (≥ DHPXL in DPXL x bytes per pixel) for the horizontal byte size (HWTH in DFMT). Discard the gray area in Figure 26.6 as invalid data. For YCbCr formats, set an even number for the number of Y data horizontal pixels. In addition, for the YCbCr4:2:0 format, the number of vertical pixels must also be set to an even number.

Table 26.4 lists these restrictions.

Table 26.4 Restrictions for Each Format

Format	Item	Restrictions
Common	Destination image horizontal byte size (CHnDFMT.HWTH)	Set an integer multiple of 16.
Y data (YCbCr4:2:2)	Source image horizontal extraction start position (CHnSAR.SAR)	In a case that the X-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, a deviation is generated between Y data and C data in the horizontal direction.
	Destination image horizontal pixel size (CHnDPXL.DHPXL)	In a case that the horizontal pixel size is odd number of the destination image, the invalid data might be generated right side in the image.
Y data (YCbCr4:2:0)	Source image horizontal extraction start position (CHnSAR.SAR)	In a case that the X-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, a deviation is generated between Y data and C data in the horizontal direction.
	Source image vertical extraction start position (CHnSAR.SAR)	In a case that the Y-coordinate of starting coordinate-S (SAR) relative to the coordinate origin 0 of source image is odd number, the vertical throw between Y and CbCr is to be generated.
	Destination image horizontal pixel size (CHnDPXL.DHPXL)	In a case that the horizontal pixel size is odd number of the destination image, the invalid data might be generated right side in the image.
	Destination image vertical pixel size (CHnDPXL.DVPXL)	In a case that the vertical pixel size is odd number of the destination image, the invalid data might be generated bottom in the image.

26.3.2 Image Rotation/Inversion

Table 26.5 The Combination of the Bits, VMRR, HMRR, ROTL, and ROTR and the Rotation/Inversion

VMRR bit	HMRR bit	ROTL bit	ROTR bit	DAR specified point	Rotation/Inversion Performance
0	0	0	0	A	Rotation/Inversion is not performed
0	0	0	1	C	Clockwise 90 degrees rotation
0	0	1	0	B	Clockwise 270 degrees rotation
0	1	0	1	A	After rotating clockwise 90 degrees, inverse horizontally (After rotating clockwise 270 degrees, inverse vertically)
1	0	1	0		
1	0	0	1	D	After rotating clockwise 90 degrees, inverse vertically (After rotating clockwise 270 degrees, inverse horizontally)
0	1	1	0		
0	1	0	0	C	Inversing horizontally
1	0	0	0	B	Inversing vertically
1	1	0	0	D	180 degrees rotation
Others				—	Setting prohibited

The rotation/inversion performance in 90 degrees units can be executed arbitrarily effects of combination of the bits, VMRR, HMRR, ROTR, and ROTL as shown in Table 26.5. Figure 26.7 shows the relations between the source image and the destination image in operating with rotation/inversion performance and Figure 26.8 shows only with inversion performance.

During the rotation/ inversion operating, the address specified point setting in CHnDAR is to be changed according to the setting of the bits, VMRR, HMRR, ROTR, and ROTL. See Figure 26.9 for details on the specified address point corresponding to the processing respectively.

Lists the formulas for the address settings as follows.

offset_add Address at the left above end of the destination image.
dest_hwidth Horizontal byte size of the destination image (CHnDFMT.DHWTH)
dest_vpxl Vertical pixel size of the destination image (CHnDPXL.DVPXL)

A DAR = offset_add
B DAR = offset_add + (dest_hwidth × (dest_vpxl − 1))
C DAR = offset_add + dest_hwidth
D DAR = offset_add + (dest_hwidth × dest_vpxl)

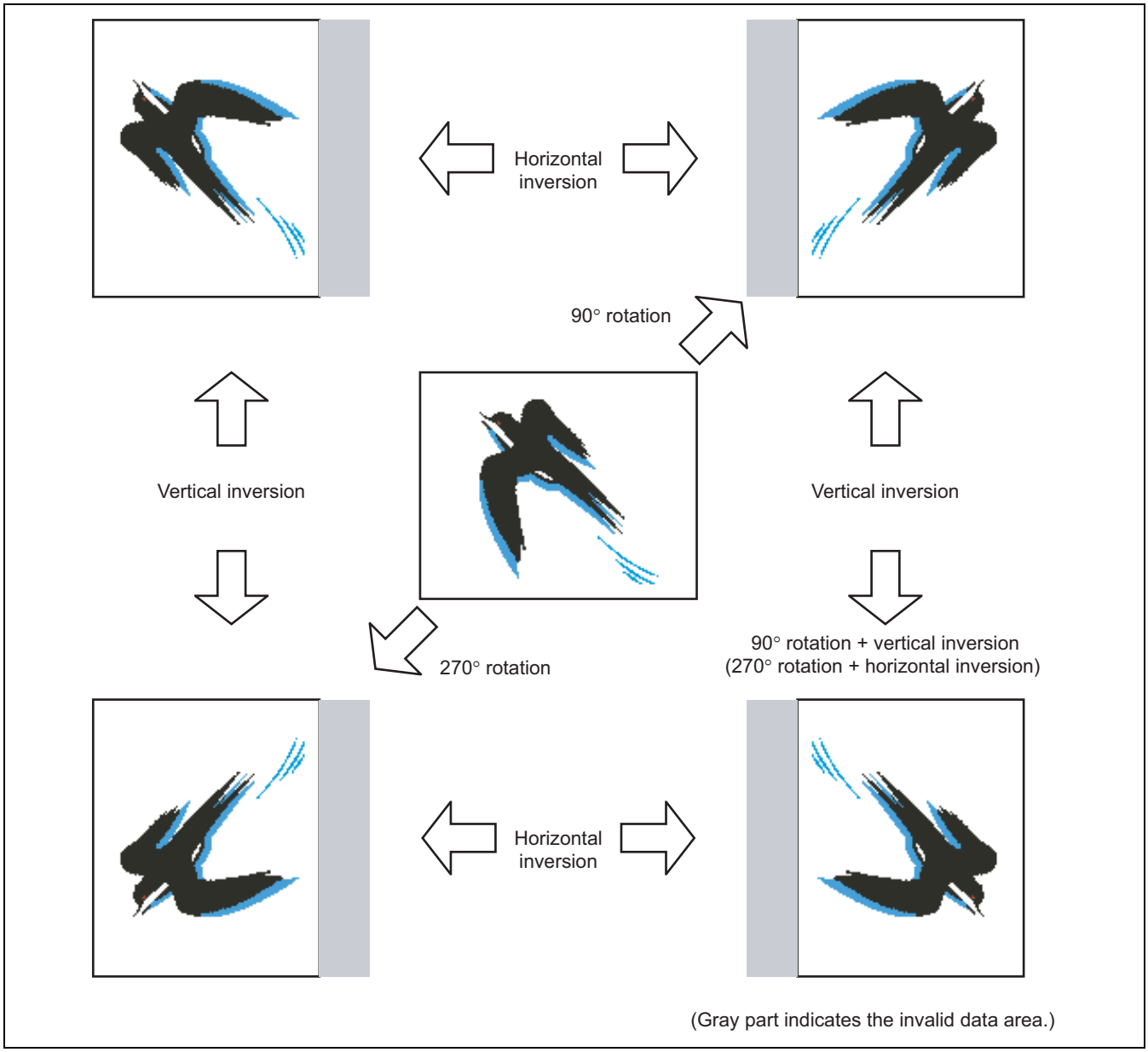


Figure 26.7 Relations between the Source Image and the Destination Image in Operating with Rotation/Inversion Performance

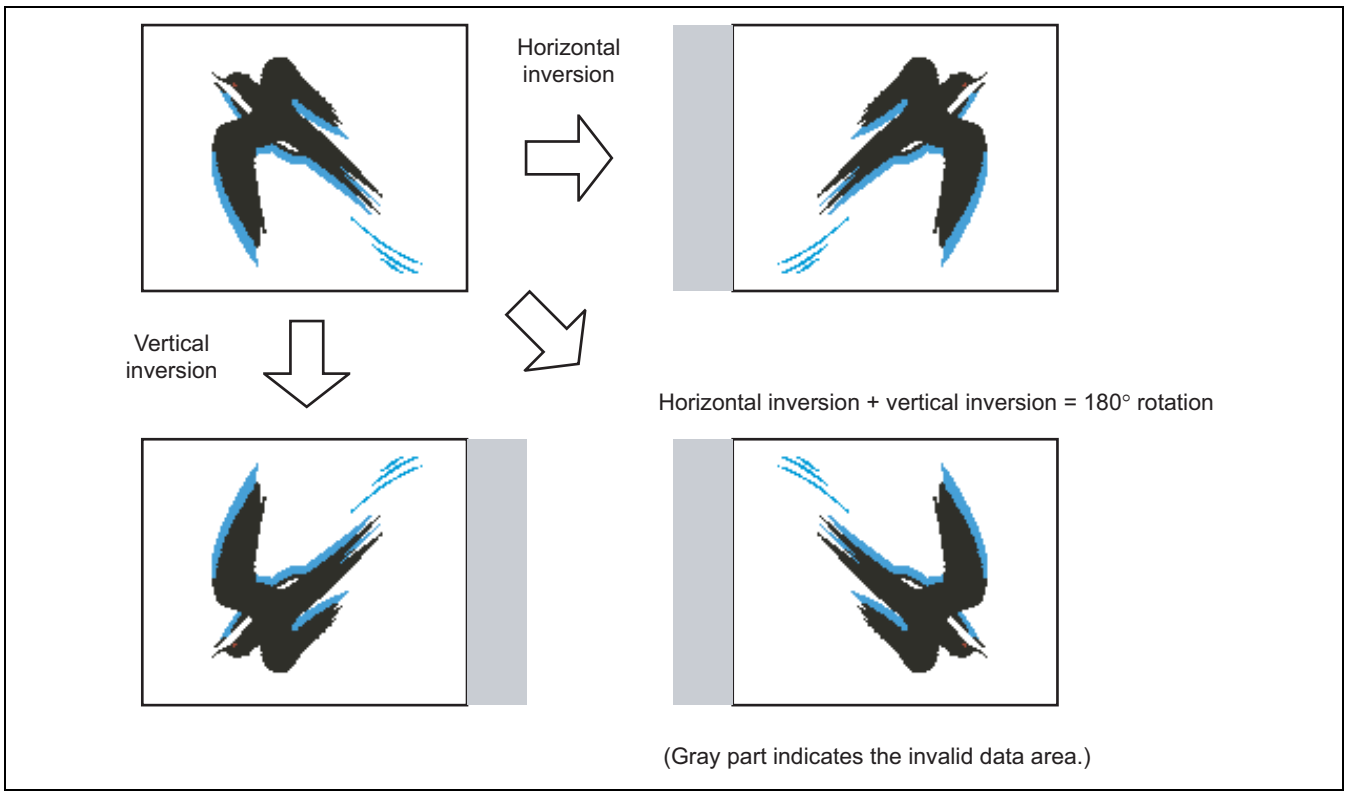


Figure 26.8 Relations between the Source Image and the Destination Image in Operating with Inversion Performance

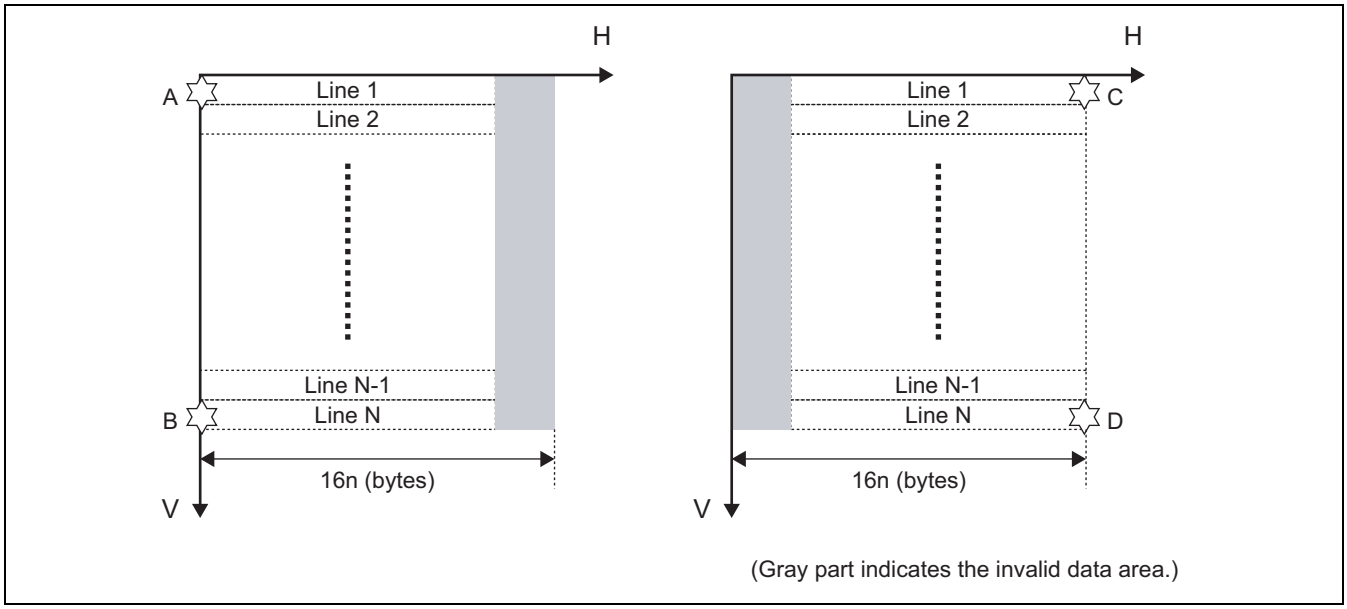


Figure 26.9 The specified Address point of CHnDAR

26.3.3 Format Conversion

Conversions are possible between RGB formats and between YCbCr formats (YCbCr4:2:0 and YCbCr4:2:2). For available RGB formats, see Table 26.3. However, no format conversion is possible between RGB and YCbCr.

26.3.4 Simple Magnification

Setting the MX and MY bits in CTRL allows enlarged output in the X and Y directions respectively.

Simple magnification method is used for the magnification processing where the pixels in the source image are copied in the X and Y directions and are then output.

Figure 26.10 is a schematic diagram of simple magnification of pixels.

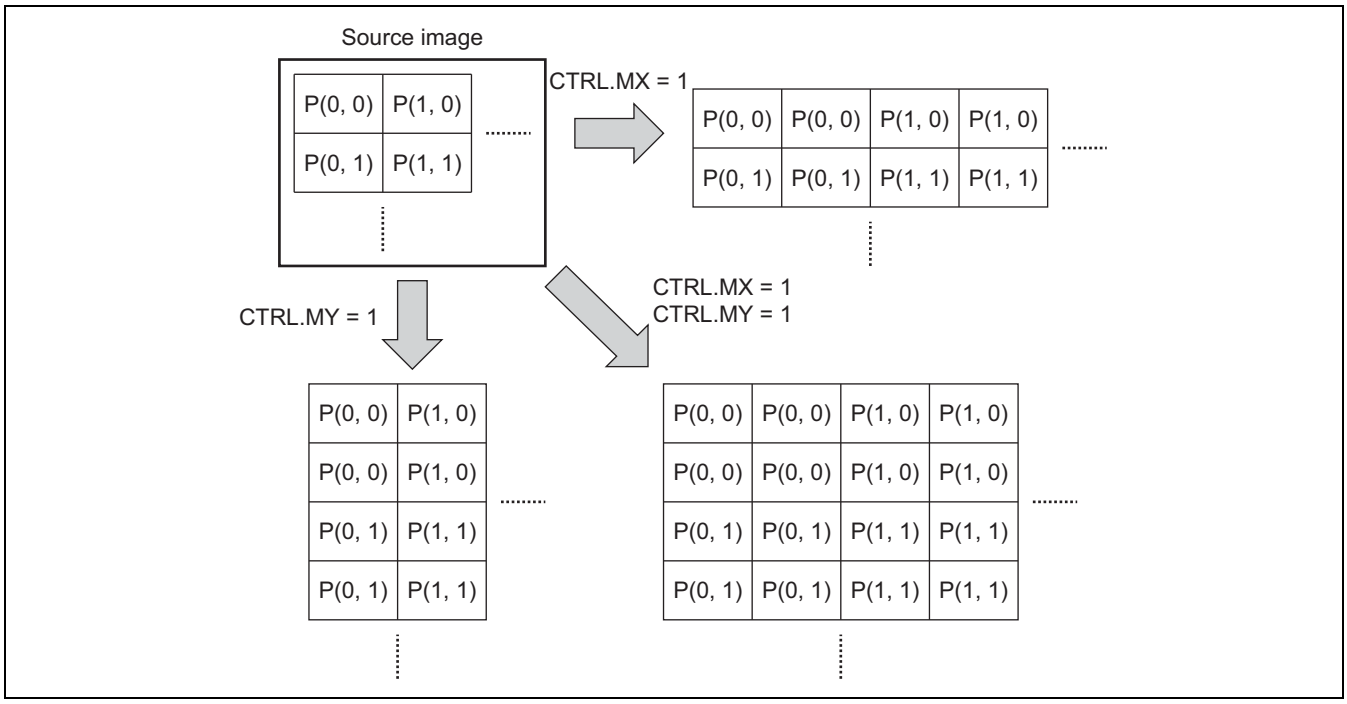


Figure 26.10 Enlarged Output of Pixels

26.4 Transfer Flow

Figure 26.11 shows a flowchart of DMAC transfer using 2D-DMAC.

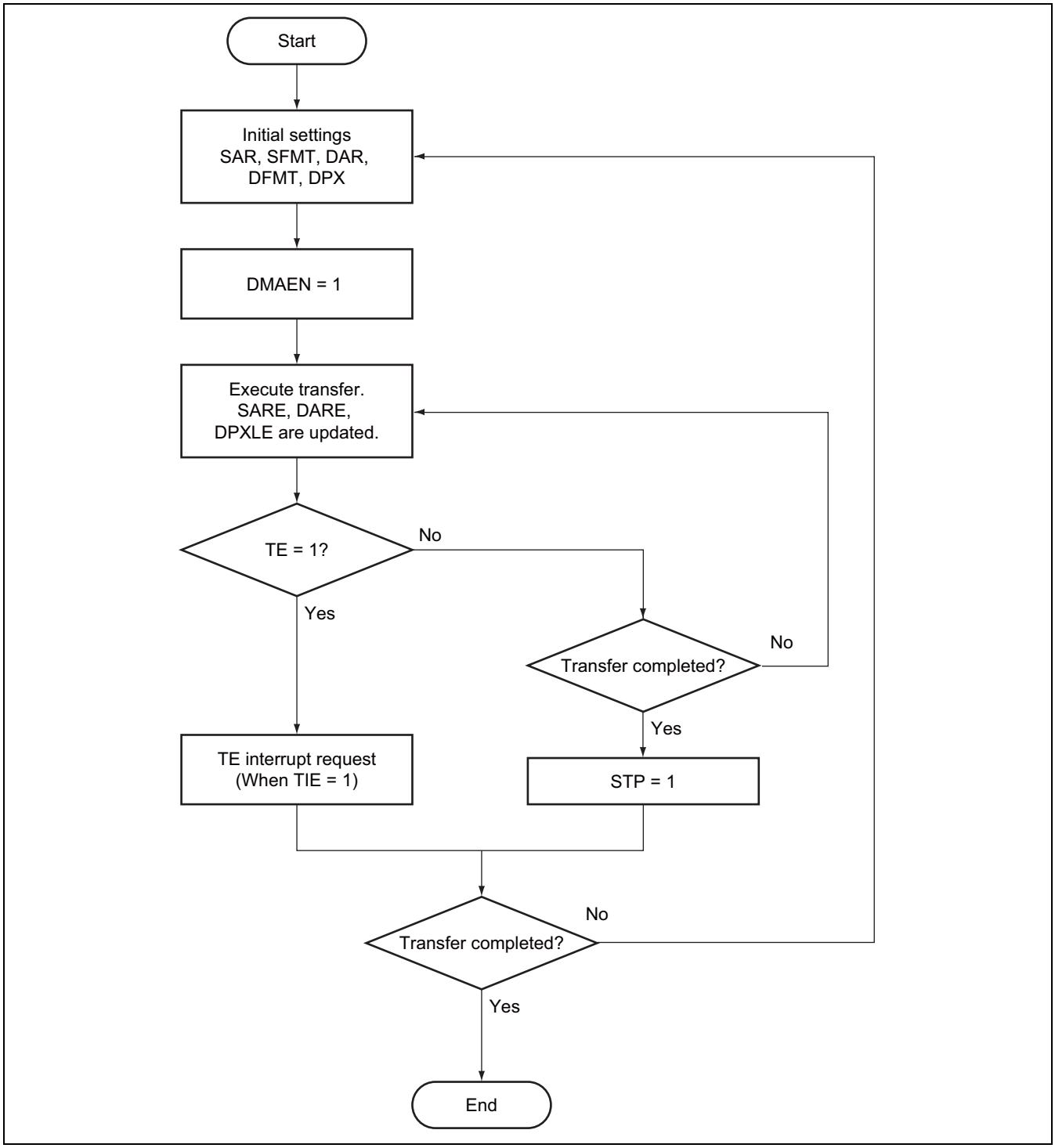


Figure 26.11 Flowchart of DMAC Transfer Using 2D-DMAC

26.5 Handling Interrupts from the 2D-DMAC

The 2D-DMAC module issues an interrupt (TEI = 1) when it completes data output without receiving a confirmation of completion of the data transaction with external memory. This raises the possibility of unexpected (out-of-date) data being read from external memory when a request for access from any module reaches external memory ahead of the 2D-DMAC's interrupt request. This behavior will only appear if the module is accessing 2D-DMAC output data for the part of the bottom line in the right corner (e.g. the CPU is reading image data for 180-degree image rotation.). Avoiding this behavior requires either of the procedures described below.

1. Dummy transaction

   After detecting the TE interruption, set up a dummy transfer with the below conditions:

   Stride size of source image: 2048 bytes

   Output image size: W: 128, H: 32

   Image format: ARGB8888 (PKF = B'00000)

   No image rotation and scaling

   The TE interrupt in response to the dummy transfer guarantees the completion of data output for the target transaction to external memory.

2. Insertion of a wait period

   After detecting the TE interrupt, insert 20 μs of waiting to guarantee completion of the data transaction with external memory.

27. Audio

27.1 Overview

This section describes the data path between audio modules, list of routings, and transfer flow.

27.1.1 Data Paths between Audio Modules

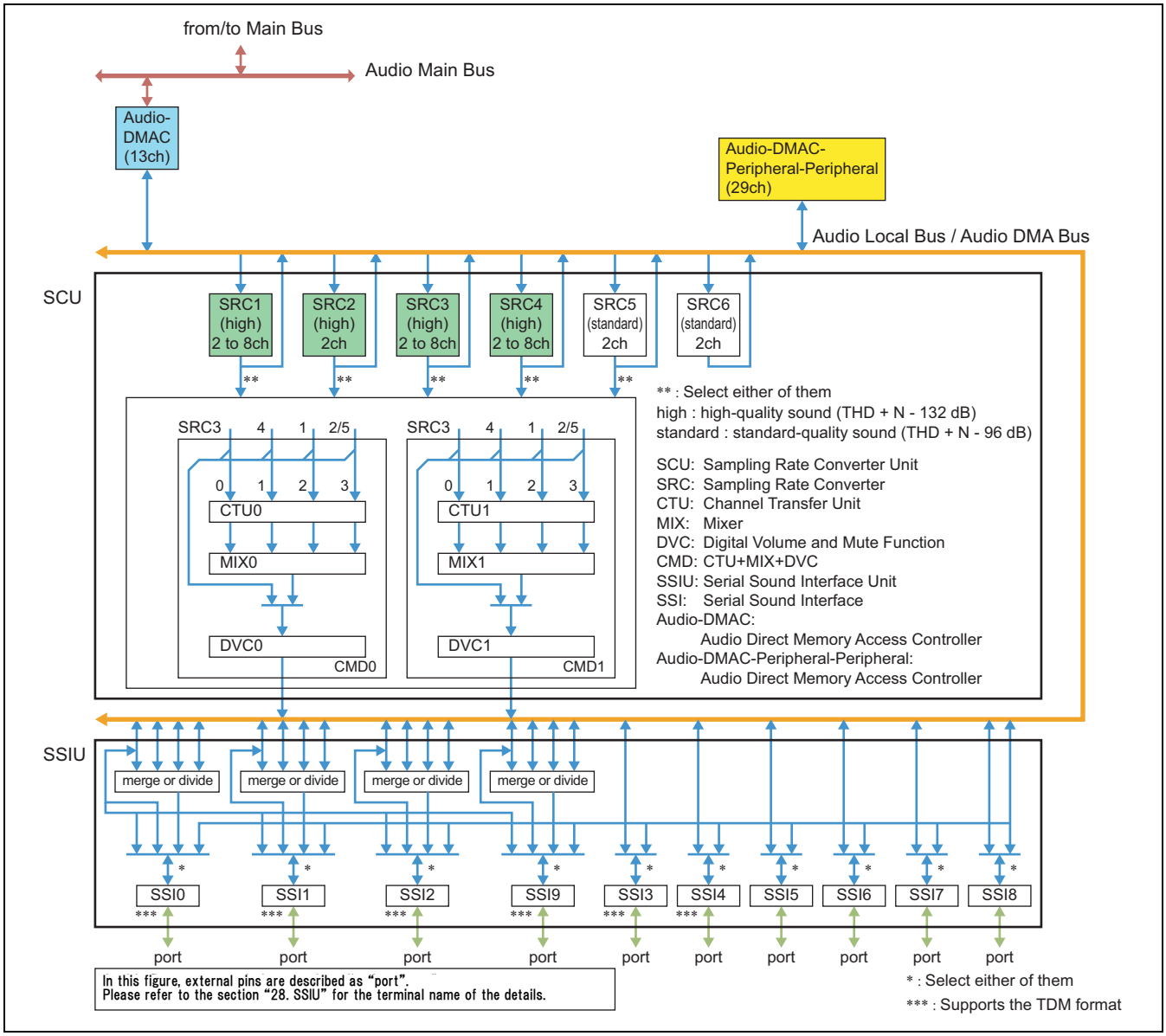


Figure 27.1 Data Paths between Audio Modules List of Routings

Data transmission paths in the Audio module are shown in Figure 27.2.

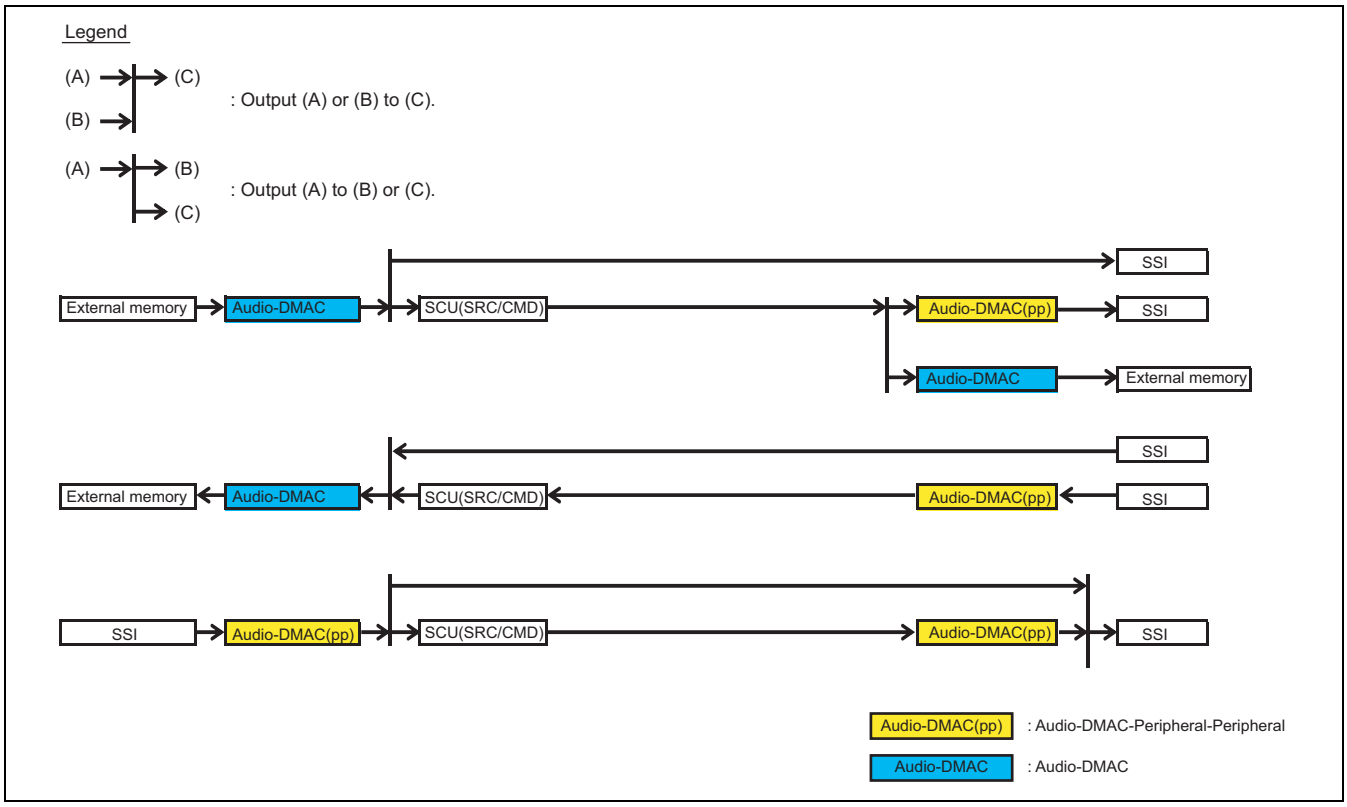


Figure 27.2 List of Routings

27.1.2 Audio-DMAC

The Audio-DMAC is used by data transfer between the external memory and audio modules. The setting values of DMASAR and DMADAR of the Audio-DMAC are shown in Table 27.1.

Table 27.1 Setting Values of DMASAR and DMADAR of Audio-DMAC

Name of Register	DMASAR/DMADAR	
SSI0-0_BUSIF	H'EC10	0000
SSI0-1_BUSIF		0400
SSI0-2_BUSIF		0800
SSI0-3_BUSIF		0C00
SSI1-0_BUSIF		1000
SSI1-1_BUSIF		1400
SSI1-2_BUSIF		1800
SSI1-3_BUSIF		1C00
SSI2-0_BUSIF		2000
SSI2-1_BUSIF		2400
SSI2-2_BUSIF		2800
SSI2-3_BUSIF		2C00
SSI3_BUSIF		3000
SSI4_BUSIF		4000
SSI5_BUSIF		5000
SSI6_BUSIF		6000
SSI7_BUSIF		7000
SSI8_BUSIF		8000
SSI9-0_BUSIF		9000
SSI9-1_BUSIF		9400
SSI9-2_BUSIF		9800
SSI9-3_BUSIF		9C00
SSITDR0*2	H'EC24	1008
SSIRDR0*1		100C
SSITDR1*2		1048
SSIRDR1*1		104C
SSITDR2*2		1088
SSIRDR2*1		108C
SSITDR3*2		10C8
SSIRDR3*1		10CC
SSITDR4*2		1108
SSIRDR4*1		110C
SSITDR5*2		1148
SSIRDR5*1		114C

Name of Register	DMASAR/DMADAR	
SSITDR6*2	H'EC24	1188
SSIRDR6*1		118C
SSITDR7*2		11C8
SSIRDR7*1		11CC
SSITDR8*2		1208
SSIRDR8*1		120C
SSITDR9*2		1248
SSIRDR9*1		124C
SRC1in_BUSIF*2	H'EC00	0400
SRC2in_BUSIF*2		0800
SRC3in_BUSIF*2		0C00
SRC4in_BUSIF*2		1000
SRC5in_BUSIF*2		1400
SRC6in_BUSIF*2		1800
SRC1out_BUSIF*1		4400
SRC2out_BUSIF*1		4800
SRC3out_BUSIF*1		4C00
SRC4out_BUSIF*1		5000
SRC5out_BUSIF*1		5400
SRC6out_BUSIF*1		5800
CMD0out_BUSIF*1		8000
CMD1out_BUSIF*1		8400

Notes: 1. Used only by DMASAR.
2. Used only by DMADAR.

27.1.3 Data Format on Audio Local Bus

Figure 27.3 shows the data formats handled in the audio local bus. When writing or reading data through the Audio-DMAC, align data to match the appropriate data format from those in Figure 27.3.

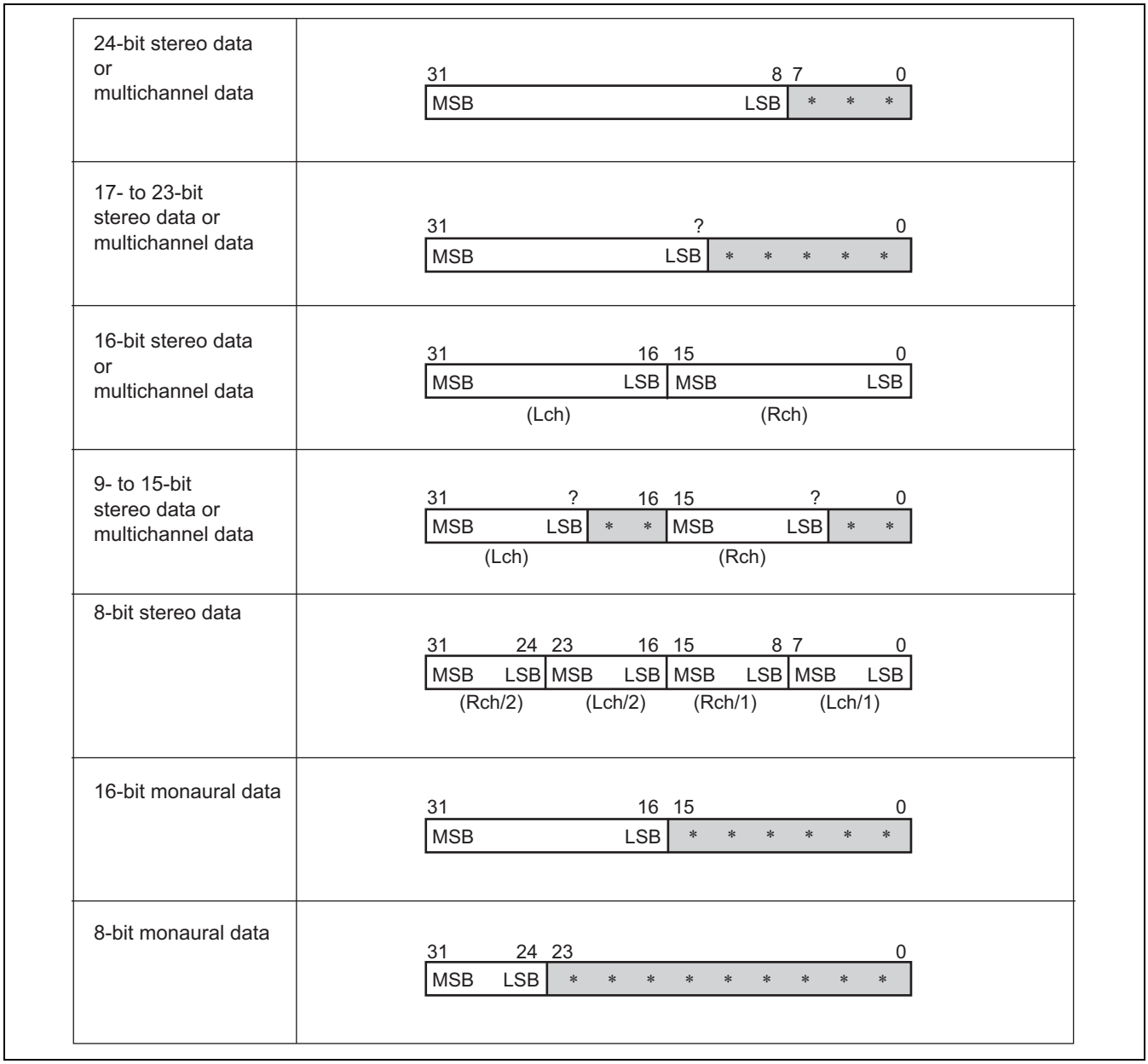


Figure 27.3 Data Format

Notes: 1. Write 0 to the * bits in the figure when writing data. When reading data, ignore the values read from these bits.
2. In the 8-bit stereo data format, (Lch/1) and (Rch/1) indicate the data pair to be processed first and (Lch/2) and (Rch/2) indicate the next data pair to be processed.
3. Only the MSB-first data formats can be used.
4. In Data Format of "16-bit stereo data or multichannel data" and "9- to 15-bitstereo data or multichannel data", set SSIU.SSI_MODE0.ind_word_swap*(* = 0-9) in the setup of independent SSI transmission (SSIU.SSI_MODE0.ind*(* = 0-9) = 1).

27.1.4 Rearranging the Order of Data

For the audio modules (SSI and SCU), rearranging the order of data is possible in the channel unit. Places of data in each data format are defined as in Tables 27.2 to 27.4.

Table 27.2 Definition of Data Places in Each Data Format (1)

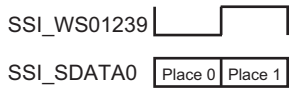
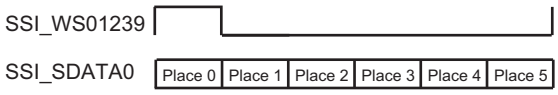
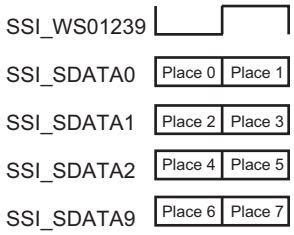
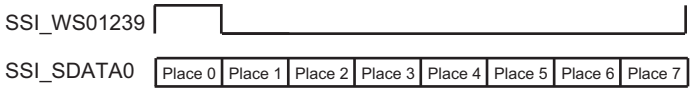
SSI · Stereo (2 channels)	
SSI · Stereo x 3 (6 channels)	
SSI · TDM (6 channels)	
SSI · Stereo x 4 (8 channels)	
SSI · TDM (8 channels)	

Table 27.3 Definition of Data Places in Each Data Format (2)

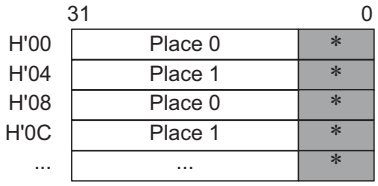
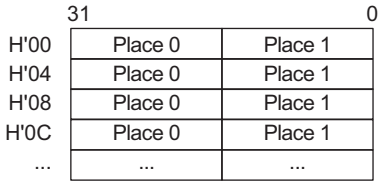
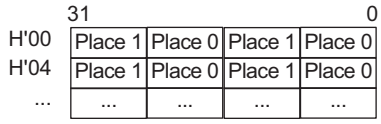
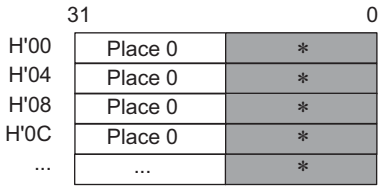
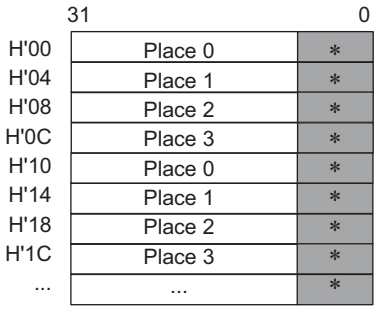
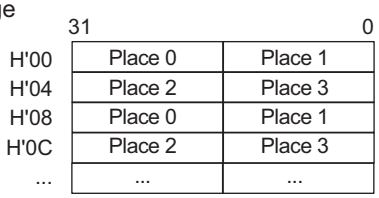
BUSIF · Stereo (2 channels) · 24 bits	External memory image 
BUSIF · Stereo (2 channels) · 16 bits	External memory image 
BUSIF · Stereo (2 channels) · 8 bits	External memory image 
BUSIF · Monaural (1 channel) · 8/16 bits	External memory image 
BUSIF · Multichannel (4 channels) · 24 bits	External memory image 
BUSIF · Multichannel (4 channels) · 16 bits	External memory image 

Table 27.4 Definition of Data Places in Each Data Format (3)

BUSIF · Multichannel (6 channels) · 24 bits	External memory image 31 0 H'00 Place 0 * H'04 Place 1 * H'08 Place 2 * H'0C Place 3 * H'10 Place 4 * H'14 Place 5 * H'18 Place 0 * H'1C Place 1 * ... ... *
BUSIF · Multichannel (6 channels) · 16 bits	External memory image 31 0 H'00 Place 0 Place 1 H'04 Place 2 Place 3 H'08 Place 4 Place 5 H'0C Place 0 Place 1 ... ...
BUSIF · Multichannel (8 channels) · 24 bits	External memory image 31 0 H'00 Place 0 * H'04 Place 1 * H'08 Place 2 * H'0C Place 3 * H'10 Place 4 * H'14 Place 5 * H'18 Place 6 * H'1C Place 7 * H'20 Place 0 * ... ... *
BUSIF · Multichannel (8 channels) · 16 bits	External memory image 31 0 H'00 Place 0 Place 1 H'04 Place 2 Place 3 H'08 Place 4 Place 5 H'0C Place 6 Place 7 H'10 Place 0 Place 1 ... ...

27.1.5 Transfer Flow

When data transfer is performed between the audio modules, which are used in a set of audio routing, use the Audio-DMAC and Audio-DMAC-Peripheral-Peripheral to perform settings in accord with the transfer flow shown in Figure 27.4.

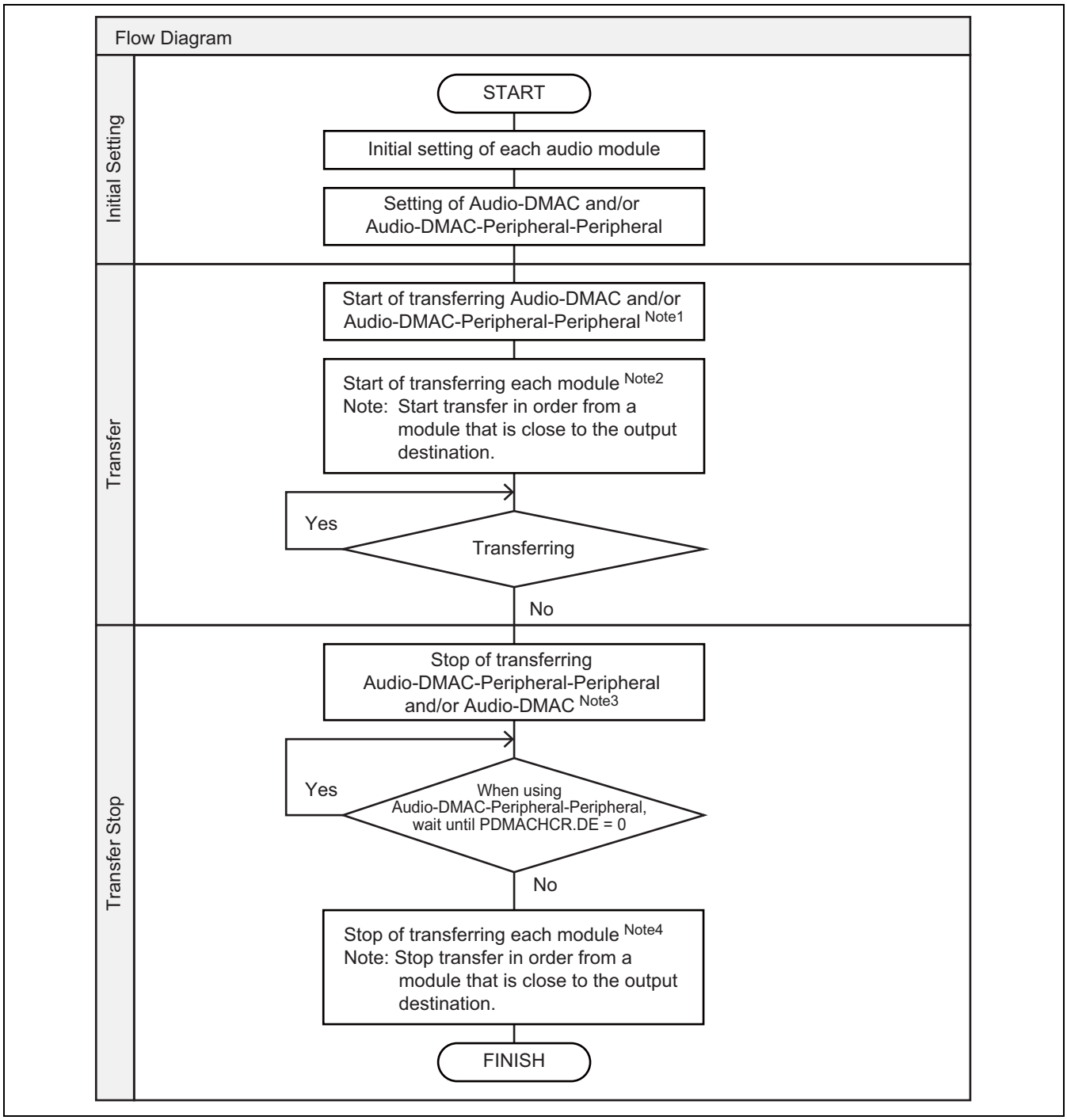


Figure 27.4 Transfer Flow

Notes: 1. For Audio-DMAC, set DMACHCR.DE.
For Audio-DMAC-Peripheral-Peripheral, set PDMACHCR.DE.
Set up registers except the above in "setting of Audio-DMAC and/or Audio-DMAC-Peripheral-Peripheral."

2. For SSI (except for the case when TDM split mode, SSI independent transfer, SSI0, SSI1, SSI2, or SSI9, and SSI3 or SSI4 are used at the same time), when transmitting (from SSI to the external device), set

SSIq/r_CONTROL.start after setting SSICR.en/dmen). When receiving (from the external device to SSI), set SSICR.en/dmen after setting SSIq/r_CONTROL.start.

For SSI (In the case of TDM split mode) regardless of transmission and reception, set SSIq/r_CONTROL.start after setting SSICR.en/dmen.

For SSI (In the case of SSI independent transfer), set SSICR.en/dmen.

For SSI (When using SSI0, SSI1, SSI2, or SSI9 and SSI3 or SSI4 at the same time), when transmitting (from SSI to the external device) set SSIq/r_CONTROL.start after setting SSI_CONTROL. When receiving (from the external device to SSI), set SSI_CONTROL after setting SSIq/r_CONTROL.start. (Set SSICR.dmen at the time of the initial setting.)

For SCU, Set SRCm_CONTROL and CMDn_CONTROL.

Set up registers except the above in “initial setting of each audio module”.

3. For Audio-DMAC-Peripheral-Peripheral, clear PDMACHCR.DE. (mandatory)
   For Audio-DMAC, clear DMACHCR.DE. Clear processing of Audio-DMAC can be cleared anywhere in a TransferStop sequence.
4. For SSI (except for the case when TDM split mode, SSI independent transfer, SSI0, SSI1, SSI2, or SSI9, and SSI3 or SSI4 are used at the same time), when transmitting (from SSI to the external device), clear SSIq/r_CONTROL.start after clearing SSICR.en/dmen. When receiving (from the external device to SSI), clear SSICR.en/dmen after clearing SSIq/r_CONTROL.start.

   For SSI (In the case of TDM split mode), regardless of transmission and reception, clear all SSIq/r_CONTROL.start of the relevant channels to clear SSICR.en/dmen.

   For SSI (In the case of SSI independent transfer), clear SSICR.en/dmen.

   For SSI (When using SSI0, SSI1, SSI2, or SSI9 and SSI3 or SSI4 at the same time), when transmitting (from SSI to the external device) clear SSIq/r_CONTROL.start after clearing SSICR.dmen of each module and SSI_CONTROL. When receiving (from the external device to SSI), clear SSICR.dmen of each module and SSI_CONTROL after clearing SSIq/r_CONTROL.start.

   For SCU, clear SRCm_CONTROL and CMDn_CONTROL.

27.1.6 Module Standby Function

For the register settings to make a transition to or from module standby mode, refer to section 7A, Module Standby and Software Reset.

(1) Transition to Module Standby Mode

To make a transition to module standby mode by the module standby function, refer to the following transition procedure for each module.

(a) SSIU/SSI

1. Check the following registers' settings.
   [SSIU]
   — All bits in the SSIq control register (SSIq_CONTROL) (q = 0-0, 1-0, 2-0, or 9-0) are cleared to 0 (data transfer stopped).
   — All bits in the SSIr control register (SSIr_CONTROL) (r = 3 to 8) are cleared to 0 (data transfer stopped).
   — All bits in the SSIq interrupt enable register (SSIq_INT_ENABLE_MAIN) (q = 0-0, 1-0, 2-0, or 9-0) are cleared to 0 (interrupt disabled).
   — All bits in the SSIr interrupt enable register (SSIr_INT_ENABLE_MAIN) (r = 3 to 8) are cleared to 0 (interrupt disabled).
   — All bits in the SSI control register (SSI_CONTROL) are cleared to 0 (data transfer stopped)

   [SSI]
   — The DMEN and EN bits in the control register (SSICRn) (n = 0 to 9) are cleared to 0 (disabled).
   — The IDST bit in the status register (SSISRn) (n = 0 to 9) is set to 1.
   — The CONT bit in the WS mode register (SSIWSRn) (n = 0 to 9) is cleared to 0 (disabled).

2. Set the MSTP1005 to MSTP1015 bits in the module stop control register (SMSTPCR10)

Note: The above bits should be set while the module operation has been completed and is placed in the idle state in which the module cannot be activated by external pins or other modules.

(b) SCU

1. Check the following registers' settings.
   — All bits in the SRCm control register (SRCm_CONTROL) (m = 1 to 6) are cleared to 0 (data transfer stopped).
   — All bits in the CMDn control register (CMDn_CONTROL) (n = 0, 1) are cleared to 0 (data transfer stopped).
   — All bits in the SRCm interrupt enable register 0 (SRCm_INT_ENABLE0) (m = 1 to 5) are cleared to 0 (interrupt disabled).
   — All bits in the SRCn interrupt enable register 0 (SRCn_INT_ENABLE0) (n = 6) are cleared to 0 (interrupt disabled).
2. Set the MSTP1017 to MSTP1021 and MSTP1025 to MSTP1030 bits in the module stop control register (SMSTPCR10)

Note: The above bits should be set while the module operation has been completed and is placed in the idle state in which the module cannot be activated by external pins or other modules.

(2) Releasing and Restarting from Module Standby Mode

After the transition to module standby mode, modules can be released from module standby mode by a power-on reset or the appropriate procedure from the list below.

(a) SSIU/SSI

1. Supply the clock signal to the ADG and SSIU/SSI modules.
2. Clear the MSTP1005 to MSTP1015 bits in the module stop control register (SMSTPCR10).

(b) SCU

1. Clear the MSTP1017 to MSTP1021 and MSTP1025 to MSTP1030 bits in the module stop control register (SMSTPCR10).

27.2 Usage Notes

27.2.1 Notes on Route Switching and Setting Changes

When switching the transfer route, stop the current transfer, specify the new transfer route, and then start transfer. Also, when changing the quantization bit count or the formats, once stop transfer, and then start transfer again after resetting. If this procedure is not followed, correct operation is not guaranteed.

27.2.2 Use of SSI3 and SSI4

Table 27.5 shows the combinations of SSI3 and SSI4 usage and register settings.

Table 27.5 Combinations of SSI3 and SSI4 Usage and Register Settings

	SSI_MODE1 Register Settings		Bit Used to Control Start or Stop Operation
	ssi34_sync	ssi4_pin	
Operating SSI3 and SSI4 independently	0	00	SSICRn.EN (n = 3 and 4)
Operating SSI4 with the SCK and WS signals of SSI3 being shared by both SSI3 and SSI4	0	01 or 10	SSICRn.EN (n = 3 and 4)
Synchronizing serial data of SSI3 and SSI4	1	01 or 10	SSI_CONTROL.ssi34

27.2.3 Notes on CMD Block Usage

When a single sound source is split into two routes, CMD0 and CMD1, and output to SSI3 and SSI4, use the settings for "Synchronizing serial data of SSI3 and SSI4" in Table 27.5, Combinations of SSI3 and SSI4 Usage and Register Settings. The quantization bit count and sampling frequency settings should be the same between SSI3 and SSI4. Note that only the stereo format can be specified for SSI3 and SSI4. For example, it is not possible to output TDM-format data from SSI3 and stereo-format data from SSI4. The reverse combination is not possible either (stereo-format data from SSI3 or TDM-format data from SSI4).

When a single sound source is split into two routes, CMD0 and CMD1, transfer to different types of destination is impossible. For example, outputting CMD0 to SSI and CMD1 to External memory is not allowed.

27.2.4 Note when SSI0, SSI1, and SSI2, or SSI0, SSI1, SSI2, and SSI9 are Used for Single-Source Audio Data

When SSI0, SSI1, and SSI2, or SSI0, SSI1, SSI2, and SSI9 are used for single-source audio data, specifying eight-bit quantization and six- or eight-channel operation at the same time is not possible.

27.2.5 Note on Transfer

When an underflow or an overflow occurs in any audio module, stop the transfer.

27.2.6 Note on Usage of the SCU Module

Before starting data transfer, the SCU module needs certain “input data timing” and “output data timing”. When “input data timing” and “output data timing” are not inputted before the transmission start, it does not operate correctly.

In addition, if the SSI module operates in master mode, and if the WS signal is used as “input/output timing signal for the SRC”, set SSIWSRn.CONT to 1.

(The WS signal inputted into the ADG module is the same signal as the SSI_WS terminal.)

28. Serial Sound Interface Unit (SSIU)

28.1 Overview

The SSIU, incorporating ten SSI modules, allows independent operation of SSI modules, operation of multiple SSI modules sharing the same serial clock, and connection or split of multichannel data.

Refer to section 28A to understand single SSI module in detail.

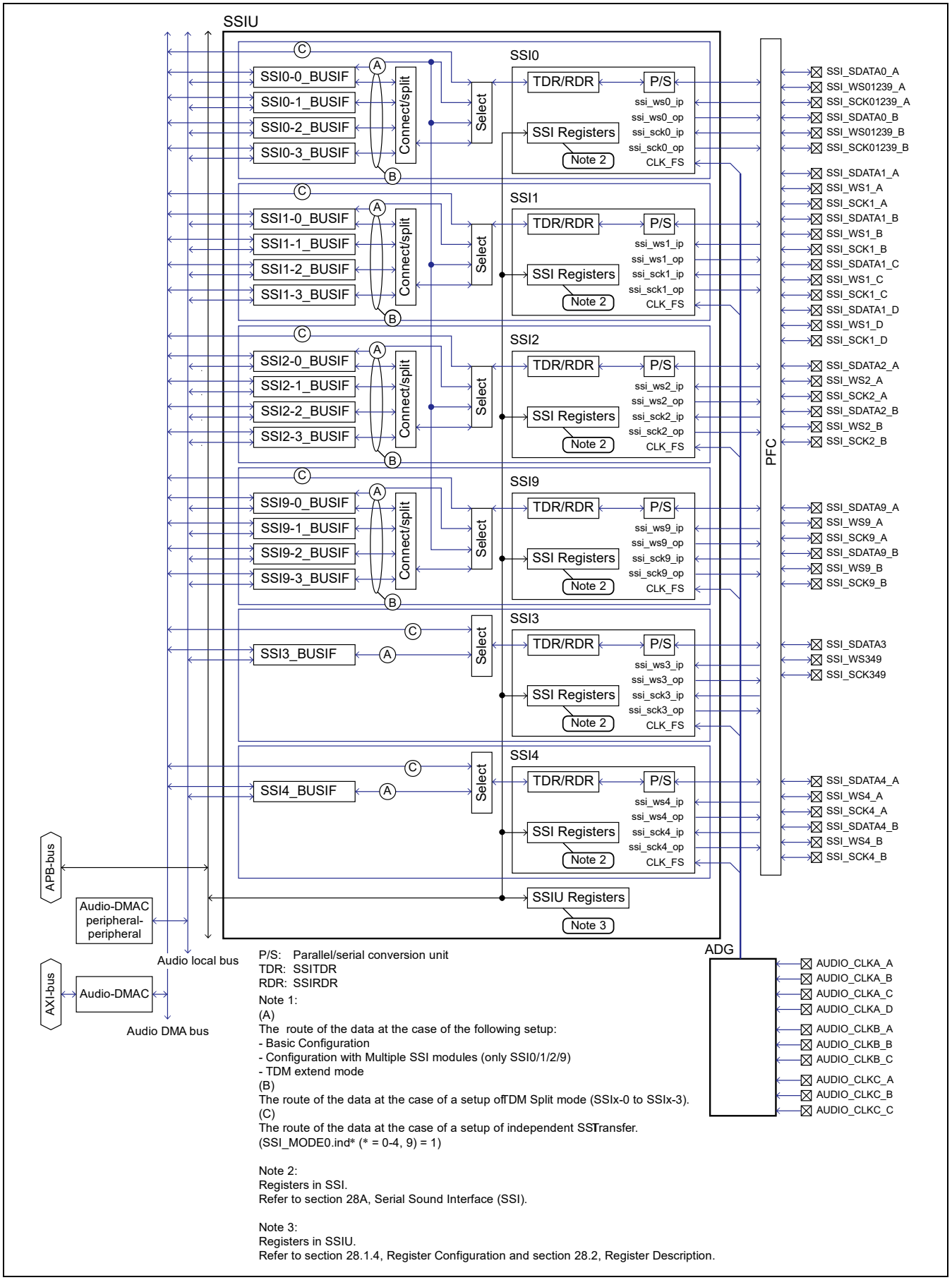
Note: Configure the system so that connected external devices can operate on the same clock source.

28.1.1 Features

- Incorporates ten SSI modules.
- Supports 6 channels/1 sound source with three SSI modules (SSI0, SSI1, and SSI2).
- Supports 8 channels/1 sound source with four SSI modules (SSI0, SSI1, SSI2, and SSI9).
- Operation of multiple modules on the same serial clock (SSI0/SSI1/SSI2/SSI3/SSI9, SSI3/SSI4/SSI9, or SSI7/SSI8).
- TDM format (Basic Configuration) corresponds to 4-, 6-, or 8-channel data.
- Handles 8-channel data on the serial bus and 6-channel data in the RZ/G1C (TDM extend mode).
- Handles 6-channel data on the serial bus and 8-channel data in the RZ/G1C (TDM extend mode).
- Connects monaural or stereo data to output TDM format data (TDM split mode).
- Splits TDM format input data into monaural or stereo data (TDM split mode).
- The frequency range of SCK signal is from 297.3 kHz to 12.5 MHz at master mode, and from 297.3 kHz to 15.1 MHz at slave mode.

28.1.2 Block Diagram

Figures 28.1 and 28.2 show the SSIU block diagrams.



P/S: Parallel/serial conversion unit
TDR: SSITDR
RDR: SSIRDR

Note 1:
(A)
The route of the data at the case of the following setup:
- Basic Configuration
- Configuration with Multiple SSI modules (only SSI0/1/2/9)
- TDM extend mode
(B)
The route of the data at the case of a setup of TDM Split mode (SSIx-0 to SSIx-3).
(C)
The route of the data at the case of a setup of independent SSI transfer.
(SSI_MODE0.ind* (* = 0-4, 9) = 1)

Note 2:
Registers in SSI.
Refer to section 28A, Serial Sound Interface (SSI).

Note 3:
Registers in SSIU.
Refer to section 28.1.4, Register Configuration and section 28.2, Register Description.

Figure 28.1 Block Diagram of SSIU (SSI0, SSI1, SSI2, SSI3, SSI4, and SSI9)

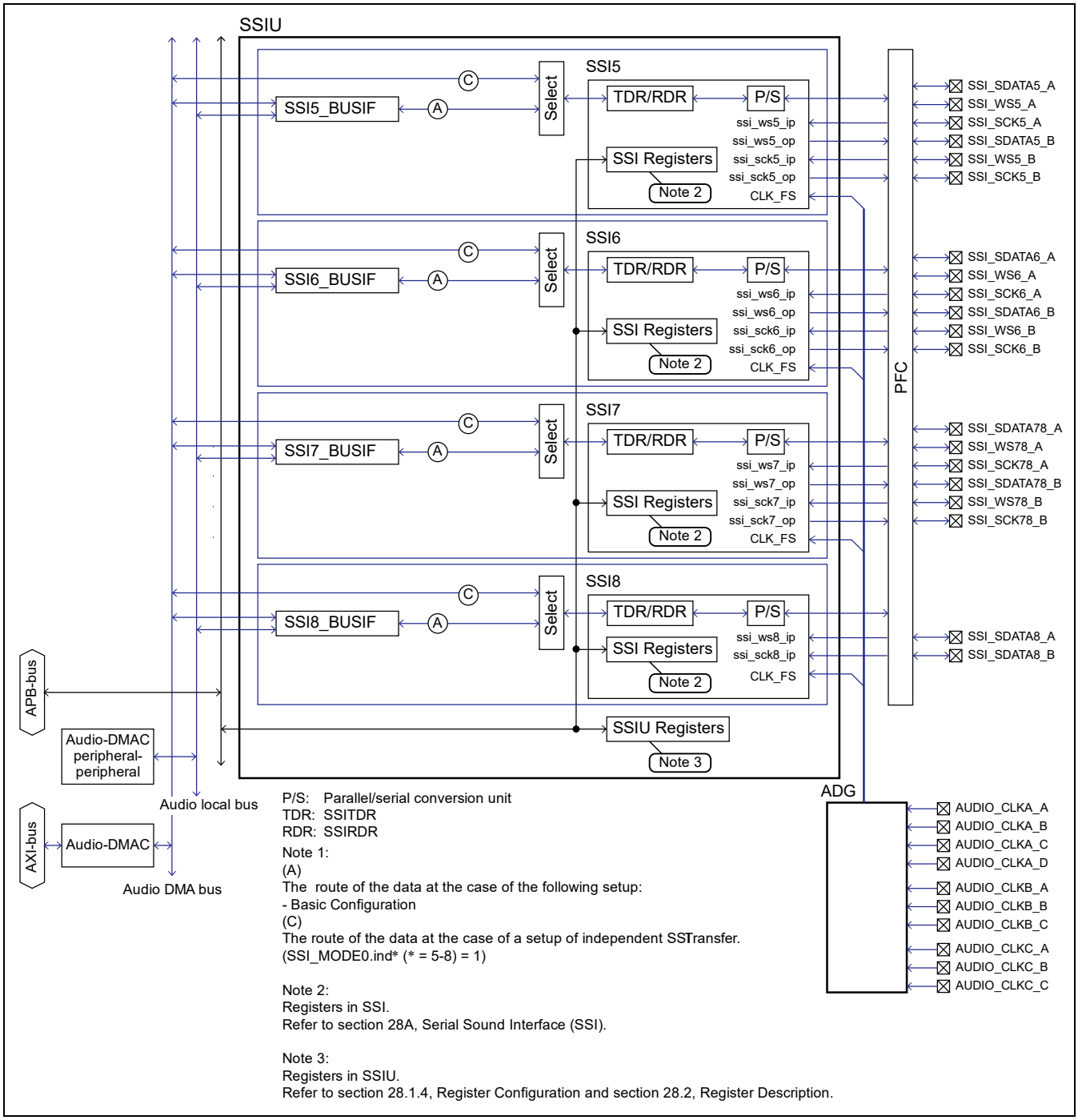


Figure 28.2 Block Diagram of SSIU (SSI5, SSI6, SSI7, and SSI8)

28.1.3 Input/Output Pins

Table 28.1 shows the pin configuration.

Table 28.1 Pin Configuration

Name	Pin Name	I/O	Function
Serial clock pin for SSI0, SSI1, SSI2, SSI3 and SSI9 (Group A)	SSI_SCK0129_A (SSI_SCK01239_A)	I/O	Serial clock (SSI0 only or combination of SSI0, SSI1, SSI2, SSI3, and SSI9) (Group A)
Serial clock pin for SSI0, SSI1, SSI2, SSI3 and SSI9 (Group B)	SSI_SCK0129_B (SSI_SCK01239_B)	I/O	Serial clock (SSI0 only or combination of SSI0, SSI1, SSI2, SSI3, and SSI9) (Group B)
Word select pin for SSI0, SSI1, SSI2, SSI3 and SSI9 (Group A)	SSI_WS0129_A (SSI_WS01239_A)	I/O	Word select (SSI0 only or combination of SSI0, SSI1, SSI2, SSI3, and SSI9) (Group A)
Word select pin for SSI0, SSI1, SSI2, SSI3 and SSI9 (Group B)	SSI_WS0129_B (SSI_WS01239_B)	I/O	Word select (SSI0 only or combination of SSI0, SSI1, SSI2, SSI3, and SSI9) (Group B)
Serial data pin for SSI0 (Group A)	SSI_SDATA0_A	I/O	Serial data (Group A)
Serial data pin for SSI0 (Group B)	SSI_SDATA0_B	I/O	Serial data (Group B)
Serial clock pin for SSI1 (Group A)	SSI_SCK1_A	I/O	Serial clock (Group A)
Serial clock pin for SSI1 (Group B)	SSI_SCK1_B	I/O	Serial clock (Group B)
Serial clock pin for SSI1 (Group C)	SSI_SCK1_C	I/O	Serial clock (Group C)
Serial clock pin for SSI1 (Group D)	SSI_SCK1_D	I/O	Serial clock (Group D)
Word select pin for SSI1 (Group A)	SSI_WS1_A	I/O	Word select (Group A)
Word select pin for SSI1 (Group B)	SSI_WS1_B	I/O	Word select (Group B)
Word select pin for SSI1 (Group C)	SSI_WS1_C	I/O	Word select (Group C)
Word select pin for SSI1 (Group D)	SSI_WS1_D	I/O	Word select (Group D)
Serial data pin for SSI1 (Group A)	SSI_SDATA1_A	I/O	Serial data (Group A)
Serial data pin for SSI1 (Group B)	SSI_SDATA1_B	I/O	Serial data (Group B)
Serial data pin for SSI1 (Group C)	SSI_SDATA1_C	I/O	Serial data (Group C)
Serial data pin for SSI1 (Group D)	SSI_SDATA1_D	I/O	Serial data (Group D)
Serial clock pin for SSI2 (Group A)	SSI_SCK2_A	I/O	Serial clock (Group A)
Serial clock pin for SSI2 (Group B)	SSI_SCK2_B	I/O	Serial clock (Group B)
Word select pin for SSI2 (Group A)	SSI_WS2_A	I/O	Word select (Group A)
Word select pin for SSI2 (Group B)	SSI_WS2_B	I/O	Word select (Group B)
Serial data pin for SSI2 (Group A)	SSI_SDATA2_A	I/O	Serial data (Group A)
Serial data pin for SSI2 (Group B)	SSI_SDATA2_B	I/O	Serial data (Group B)
Serial clock pin for SSI3, SSI4 and SSI9	SSI_SCK34 (SSI_SCK349)	I/O	Serial clock (SSI3 only, common to SSI3 and SSI4, or combination of SSI3, SSI4, and SSI9)
Word select pin for SSI3, SSI4 and SSI9	SSI_WS34 (SSI_WS349)	I/O	Word select (SSI3 only, common to SSI3 and SSI4, or combination of SSI3, SSI4, and SSI9)
Serial data pin for SSI3	SSI_SDATA3	I/O	Serial data
Serial clock pin for SSI4 (Group A)	SSI_SCK4_A	I/O	Serial clock (Group A)
Serial clock pin for SSI4 (Group B)	SSI_SCK4_B	I/O	Serial clock (Group B)
Word select pin for SSI4 (Group A)	SSI_WS4_A	I/O	Word select (Group A)
Word select pin for SSI4 (Group B)	SSI_WS4_B	I/O	Word select (Group B)
Serial data pin for SSI4 (Group A)	SSI_SDATA4_A	I/O	Serial data (Group A)
Serial data pin for SSI4 (Group B)	SSI_SDATA4_B	I/O	Serial data (Group B)
Serial clock pin for SSI5 (Group A)	SSI_SCK5_A	I/O	Serial clock (Group A)
Serial clock pin for SSI5 (Group B)	SSI_SCK5_B	I/O	Serial clock (Group B)

Name	Pin Name	I/O	Function
Word select pin for SSI5 (Group A)	SSI_WS5_A	I/O	Word select (Group A)
Word select pin for SSI5 (Group B)	SSI_WS5_B	I/O	Word select (Group B)
Serial data pin for SSI5 (Group A)	SSI_SDATA5_A	I/O	Serial data (Group A)
Serial data pin for SSI5 (Group B)	SSI_SDATA5_B	I/O	Serial data (Group B)
Serial clock pin for SSI6 (Group A)	SSI_SCK6_A	I/O	Serial clock (Group A)
Serial clock pin for SSI6 (Group B)	SSI_SCK6_B	I/O	Serial clock (Group B)
Word select pin for SSI6 (Group A)	SSI_WS6_A	I/O	Word select (Group A)
Word select pin for SSI6 (Group B)	SSI_WS6_B	I/O	Word select (Group B)
Serial data pin for SSI6 (Group A)	SSI_SDATA6_A	I/O	Serial data (Group A)
Serial data pin for SSI6 (Group B)	SSI_SDATA6_B	I/O	Serial data (Group B)
Serial clock pin for SSI7 and SSI8 (Group A)	SSI_SCK78_A	I/O	Serial clock (common to SSI7 and SSI8) (Group A)
Serial clock pin for SSI7 and SSI8 (Group B)	SSI_SCK78_B	I/O	Serial clock (common to SSI7 and SSI8 (Group B))
Word select pin for SSI7 and SSI8 (Group A)	SSI_WS78_A	I/O	Word select (common to SSI7 and SSI8) (Group A)
Word select pin for SSI7 and SSI8 (Group B)	SSI_WS78_B	I/O	Word select (common to SSI7 and SSI8 (Group B))
Serial data pin for SSI7 (Group A)	SSI_SDATA7_A	I/O	Serial data (Group A)
Serial data pin for SSI7 (Group B)	SSI_SDATA7_B	I/O	Serial data (Group B)
Serial data pin for SSI8 (Group A)	SSI_SDATA8_A	I/O	Serial data (Group A)
Serial data pin for SSI8 (Group B)	SSI_SDATA8_B	I/O	Serial data (Group B)
Serial clock pin for SSI9 (Group A)	SSI_SCK9_A	I/O	Serial clock (Group A)
Serial clock pin for SSI9 (Group B)	SSI_SCK9_B	I/O	Serial clock (Group B)
Word select pin for SSI9 (Group A)	SSI_WS9_A	I/O	Word select (Group A)
Word select pin for SSI9 (Group B)	SSI_WS9_B	I/O	Word select (Group B)
Serial data pin for SSI9 (Group A)	SSI_SDATA9_A	I/O	Serial data (Group A)
Serial data pin for SSI9 (Group B)	SSI_SDATA9_B	I/O	Serial data (Group B)

Note: Although each SSI is multiplexed on multiple LSI pins, the combinations of pins in use must be from the same group. For Example, the use of combinations such as SSI_SCK1_A, SSI_WS1_B, and SSI_SDATA1_C is prohibited. Refer to section 5, Pin Function Controller (PFC) for details.

28.1.4 Register Configuration

Table 28.2 shows the register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register as a longword (32 bits). Operation cannot be guaranteed if the register is not accessed as a longword.

Table 28.2 Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
SSI0_0 BUSIF Mode Register	SSI0-0_BUSIF_MODE	R/W	H'EC54 0000	H'0000 0001	32
SSI0_0 BUSIF Audio Information Register	SSI0-0_BUSIF_ADINR	R/W	H'EC54 0004	H'0000 0000	32
SSI0_0 BUSIF Data Align Register	SSI0-0_BUSIF_DALIGN	R/W	H'EC54 0008	H'7654 3210	32
SSI0_0 Mode Register	SSI0-0_MODE	R/W	H'EC54 000C	H'0000 0000	32
SSI0_0 Control Register	SSI0-0_CONTROL	R/W	H'EC54 0010	H'0000 0000	32
SSI0_0 Status Register	SSI0-0_STATUS	R	H'EC54 0014	H'0000 0000	32
SSI0_0 Interrupt Enable Register	SSI0-0_INT_ENABLE_MAIN	R/W	H'EC54 0018	H'0000 0000	32
SSI0_1 BUSIF Mode Register	SSI0-1_BUSIF_MODE	R/W	H'EC54 0020	H'0000 0001	32
SSI0_1 BUSIF Audio Information Register	SSI0-1_BUSIF_ADINR	R/W	H'EC54 0024	H'0000 0000	32
SSI0_1 BUSIF Data Align Register	SSI0-1_BUSIF_DALIGN	R/W	H'EC54 0028	H'0000 0010	32
SSI0_2 BUSIF Mode Register	SSI0-2_BUSIF_MODE	R/W	H'EC54 0040	H'0000 0001	32
SSI0_2 BUSIF Audio Information Register	SSI0-2_BUSIF_ADINR	R/W	H'EC54 0044	H'0000 0000	32
SSI0_2 BUSIF Data Align Register	SSI0-2_BUSIF_DALIGN	R/W	H'EC54 0048	H'0000 0010	32
SSI0_3 BUSIF Mode Register	SSI0-3_BUSIF_MODE	R/W	H'EC54 0060	H'0000 0001	32
SSI0_3 BUSIF Audio Information Register	SSI0-3_BUSIF_ADINR	R/W	H'EC54 0064	H'0000 0000	32
SSI0_3 BUSIF Data Align Register	SSI0-3_BUSIF_DALIGN	R/W	H'EC54 0068	H'0000 0010	32
SSI1_0 BUSIF Mode Register	SSI1-0_BUSIF_MODE	R/W	H'EC54 0080	H'0000 0001	32
SSI1_0 BUSIF Audio Information Register	SSI1-0_BUSIF_ADINR	R/W	H'EC54 0084	H'0000 0000	32
SSI1_0 BUSIF Data Align Register	SSI1-0_BUSIF_DALIGN	R/W	H'EC54 0088	H'7654 3210	32
SSI1_0 Mode Register	SSI1-0_MODE	R/W	H'EC54 008C	H'0000 0000	32
SSI1_0 Control Register	SSI1-0_CONTROL	R/W	H'EC54 0090	H'0000 0000	32
SSI1_0 Status Register	SSI1-0_STATUS	R	H'EC54 0094	H'0000 0000	32
SSI1_0 Interrupt Enable Register	SSI1-0_INT_ENABLE_MAIN	R/W	H'EC54 0098	H'0000 0000	32
SSI1_1 BUSIF Mode Register	SSI1-1_BUSIF_MODE	R/W	H'EC54 00A0	H'0000 0001	32
SSI1_1 BUSIF Audio Information Register	SSI1-1_BUSIF_ADINR	R/W	H'EC54 00A4	H'0000 0000	32
SSI1_1 BUSIF Data Align Register	SSI1-1_BUSIF_DALIGN	R/W	H'EC54 00A8	H'0000 0010	32
SSI1_2 BUSIF Mode Register	SSI1-2_BUSIF_MODE	R/W	H'EC54 00C0	H'0000 0001	32
SSI1_2 BUSIF Audio Information Register	SSI1-2_BUSIF_ADINR	R/W	H'EC54 00C4	H'0000 0000	32
SSI1_2 BUSIF Data Align Register	SSI1-2_BUSIF_DALIGN	R/W	H'EC54 00C8	H'0000 0010	32
SSI1_3 BUSIF Mode Register	SSI1-3_BUSIF_MODE	R/W	H'EC54 00E0	H'0000 0001	32
SSI1_3 BUSIF Audio Information Register	SSI1-3_BUSIF_ADINR	R/W	H'EC54 00E4	H'0000 0000	32
SSI1_3 BUSIF Data Align Register	SSI1-3_BUSIF_DALIGN	R/W	H'EC54 00E8	H'0000 0010	32
SSI2_0 BUSIF Mode Register	SSI2-0_BUSIF_MODE	R/W	H'EC54 0100	H'0000 0001	32
SSI2_0 BUSIF Audio Information Register	SSI2-0_BUSIF_ADINR	R/W	H'EC54 0104	H'0000 0000	32
SSI2_0 BUSIF Data Align Register	SSI2-0_BUSIF_DALIGN	R/W	H'EC54 0108	H'7654 3210	32
SSI2_0 Mode Register	SSI2-0_MODE	R/W	H'EC54 010C	H'0000 0000	32
SSI2_0 Control Register	SSI2-0_CONTROL	R/W	H'EC54 0110	H'0000 0000	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
SSI2_0 Status Register	SSI2-0_STATUS	R	H'EC54 0114	H'0000 0000	32
SSI2_0 Interrupt Enable Register	SSI2-0_INT_ENABLE_MAIN	R/W	H'EC54 0118	H'0000 0000	32
SSI2_1 BUSIF Mode Register	SSI2-1_BUSIF_MODE	R/W	H'EC54 0120	H'0000 0001	32
SSI2_1 BUSIF Audio Information Register	SSI2-1_BUSIF_ADINR	R/W	H'EC54 0124	H'0000 0000	32
SSI2_1 BUSIF Data Align Register	SSI2-1_BUSIF_DALIGN	R/W	H'EC54 0128	H'0000 0010	32
SSI2_2 BUSIF Mode Register	SSI2-2_BUSIF_MODE	R/W	H'EC54 0140	H'0000 0001	32
SSI2_2 BUSIF Audio Information Register	SSI2-2_BUSIF_ADINR	R/W	H'EC54 0144	H'0000 0000	32
SSI2_2 BUSIF Data Align Register	SSI2-2_BUSIF_DALIGN	R/W	H'EC54 0148	H'0000 0010	32
SSI2_3 BUSIF Mode Register	SSI2-3_BUSIF_MODE	R/W	H'EC54 0160	H'0000 0001	32
SSI2_3 BUSIF Audio Information Register	SSI2-3_BUSIF_ADINR	R/W	H'EC54 0164	H'0000 0000	32
SSI2_3 BUSIF Data Align Register	SSI2-3_BUSIF_DALIGN	R/W	H'EC54 0168	H'0000 0010	32
SSI3 BUSIF Mode Register	SSI3_BUSIF_MODE	R/W	H'EC54 0180	H'0000 0001	32
SSI3 BUSIF Audio Information Register	SSI3_BUSIF_ADINR	R/W	H'EC54 0184	H'0000 0000	32
SSI3 BUSIF Data Align Register	SSI3_BUSIF_DALIGN	R/W	H'EC54 0188	H'7654 3210	32
SSI3 Mode Register	SSI3_MODE	R/W	H'EC54 018C	H'0000 0000	32
SSI3 Control Register	SSI3_CONTROL	R/W	H'EC54 0190	H'0000 0000	32
SSI3 Status Register	SSI3_STATUS	R	H'EC54 0194	H'0000 0000	32
SSI3 Interrupt Enable Register	SSI3_INT_ENABLE_MAIN	R/W	H'EC54 0198	Undefined	32
SSI4 BUSIF Mode Register	SSI4_BUSIF_MODE	R/W	H'EC54 0200	H'0000 0001	32
SSI4 BUSIF Audio Information Register	SSI4_BUSIF_ADINR	R/W	H'EC54 0204	H'0000 0000	32
SSI4 BUSIF Data Align Register	SSI4_BUSIF_DALIGN	R/W	H'EC54 0208	H'7654 3210	32
SSI4 Mode Register	SSI4_MODE	R/W	H'EC54 020C	H'0000 0000	32
SSI4 Control Register	SSI4_CONTROL	R/W	H'EC54 0210	H'0000 0000	32
SSI4 Status Register	SSI4_STATUS	R	H'EC54 0214	H'0000 0000	32
SSI4 Interrupt Enable Register	SSI4_INT_ENABLE_MAIN	R/W	H'EC54 0218	Undefined	32
SSI5 BUSIF Mode Register	SSI5_BUSIF_MODE	R/W	H'EC54 0280	H'0000 0001	32
SSI5 BUSIF Audio Information Register	SSI5_BUSIF_ADINR	R/W	H'EC54 0284	H'0000 0000	32
SSI5 BUSIF Data Align Register	SSI5_BUSIF_DALIGN	R/W	H'EC54 0288	H'7654 3210	32
SSI5 Control Register	SSI5_CONTROL	R/W	H'EC54 0290	H'0000 0000	32
SSI5 Status Register	SSI5_STATUS	R	H'EC54 0294	H'0000 0000	32
SSI5 Interrupt Enable Register	SSI5_INT_ENABLE_MAIN	R/W	H'EC54 0298	Undefined	32
SSI6 BUSIF Mode Register	SSI6_BUSIF_MODE	R/W	H'EC54 0300	H'0000 0001	32
SSI6 BUSIF Audio Information Register	SSI6_BUSIF_ADINR	R/W	H'EC54 0304	H'0000 0000	32
SSI6 BUSIF Data Align Register	SSI6_BUSIF_DALIGN	R/W	H'EC54 0308	H'7654 3210	32
SSI6 Control Register	SSI6_CONTROL	R/W	H'EC54 0310	H'0000 0000	32
SSI6 Status Register	SSI6_STATUS	R	H'EC54 0314	H'0000 0000	32
SSI6 Interrupt Enable Register	SSI6_INT_ENABLE_MAIN	R/W	H'EC54 0318	Undefined	32
SSI7 BUSIF Mode Register	SSI7_BUSIF_MODE	R/W	H'EC54 0380	H'0000 0001	32
SSI7 BUSIF Audio Information Register	SSI7_BUSIF_ADINR	R/W	H'EC54 0384	H'0000 0000	32
SSI7 BUSIF Data Align Register	SSI7_BUSIF_DALIGN	R/W	H'EC54 0388	H'7654 3210	32
SSI7 Control Register	SSI7_CONTROL	R/W	H'EC54 0390	H'0000 0000	32
SSI7 Status Register	SSI7_STATUS	R	H'EC54 0394	H'0000 0000	32
SSI7 Interrupt Enable Register	SSI7_INT_ENABLE_MAIN	R/W	H'EC54 0398	Undefined	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
SSI8 BUSIF Mode Register	SSI8_BUSIF_MODE	R/W	H'EC54 0400	H'0000 0001	32
SSI8 BUSIF Audio Information Register	SSI8_BUSIF_ADINR	R/W	H'EC54 0404	H'0000 0000	32
SSI8 BUSIF Data Align Register	SSI8_BUSIF_DALIGN	R/W	H'EC54 0408	H'7654 3210	32
SSI8 Control Register	SSI8_CONTROL	R/W	H'EC54 0410	H'0000 0000	32
SSI8 Status Register	SSI8_STATUS	R	H'EC54 0414	H'0000 0000	32
SSI8 Interrupt Enable Register	SSI8_INT_ENABLE_MAIN	R/W	H'EC54 0418	Undefined	32
SSI9_0 BUSIF Mode Register	SSI9-0_BUSIF_MODE	R/W	H'EC54 0480	H'0000 0001	32
SSI9_0 BUSIF Audio Information Register	SSI9-0_BUSIF_ADINR	R/W	H'EC54 0484	H'0000 0000	32
SSI9_0 BUSIF Data Align Register	SSI9-0_BUSIF_DALIGN	R/W	H'EC54 0488	H'7654 3210	32
SSI9_0 Mode Register	SSI9-0_MODE	R/W	H'EC54 048C	H'0000 0000	32
SSI9_0 Control Register	SSI9-0_CONTROL	R/W	H'EC54 0490	H'0000 0000	32
SSI9_0 Status Register	SSI9-0_STATUS	R	H'EC54 0494	H'0000 0000	32
SSI9_0 Interrupt Enable Register	SSI9-0_INT_ENABLE_MAIN	R/W	H'EC54 0498	H'0000 0000	32
SSI9_1 BUSIF Mode Register	SSI9-1_BUSIF_MODE	R/W	H'EC54 04A0	H'0000 0001	32
SSI9_1 BUSIF Audio Information Register	SSI9-1_BUSIF_ADINR	R/W	H'EC54 04A4	H'0000 0000	32
SSI9_1 BUSIF Data Align Register	SSI9-1_BUSIF_DALIGN	R/W	H'EC54 04A8	H'0000 0010	32
SSI9_2 BUSIF Mode Register	SSI9-2_BUSIF_MODE	R/W	H'EC54 04C0	H'0000 0001	32
SSI9_2 BUSIF Audio Information Register	SSI9-2_BUSIF_ADINR	R/W	H'EC54 04C4	H'0000 0000	32
SSI9_2 BUSIF Data Align Register	SSI9-2_BUSIF_DALIGN	R/W	H'EC54 04C8	H'0000 0010	32
SSI9_3 BUSIF Mode Register	SSI9-3_BUSIF_MODE	R/W	H'EC54 04E0	H'0000 0001	32
SSI9_3 BUSIF Audio Information Register	SSI9-3_BUSIF_ADINR	R/W	H'EC54 04E4	H'0000 0000	32
SSI9_3 BUSIF Data Align Register	SSI9-3_BUSIF_DALIGN	R/W	H'EC54 04E8	H'0000 0010	32
SSI Mode Register 0	SSI_MODE0	R/W	H'EC54 0800	H'0000 0000	32
SSI Mode Register 1	SSI_MODE1	R/W	H'EC54 0804	H'0000 0000	32
SSI Mode Register 2	SSI_MODE2	R/W	H'EC54 0808	H'0000 0000	32
SSI Mode Register 3	SSI_MODE3	R/W	H'EC54 080C	H'0000 0000	32
SSI Control Register	SSI_CONTROL	R/W	H'EC54 0810	H'0000 0000	32
SSI System Status Register 0	SSI_SYSTEM_STATUS0	R/WC1	H'EC54 0840	H'0000 0000	32
SSI System Status Register 1	SSI_SYSTEM_STATUS1	R/WC1	H'EC54 0844	H'0000 0000	32
SSI System Status Register 2	SSI_SYSTEM_STATUS2	R/WC1	H'EC54 0848	H'0000 0000	32
SSI System Status Register 3	SSI_SYSTEM_STATUS3	R/WC1	H'EC54 084C	H'0000 0000	32
SSI System Interrupt Enable Register 0	SSI_SYSTEM_INT_ENABLE0	R/W	H'EC54 0850	H'0000 0000	32
SSI System Interrupt Enable Register 1	SSI_SYSTEM_INT_ENABLE1	R/W	H'EC54 0854	H'0000 0000	32
SSI System Interrupt Enable Register 2	SSI_SYSTEM_INT_ENABLE2	R/W	H'EC54 0858	H'0000 0000	32
SSI System Interrupt Enable Register 3	SSI_SYSTEM_INT_ENABLE3	R/W	H'EC54 085C	H'0000 0000	32
SSI0-0_BUSIF Data Register	SSI0-0_BUSIF	R/W	H'EC10 0000/ H'EC40 0000*	H'0000 0000	32
SSI0-1_BUSIF Data Register	SSI0-1_BUSIF	R/W	H'EC10 0400/ H'EC40 0400*	H'0000 0000	32
SSI0-2_BUSIF Data Register	SSI0-2_BUSIF	R/W	H'EC10 0800/ H'EC40 0800*	H'0000 0000	32
SSI0-3_BUSIF Data Register	SSI0-3_BUSIF	R/W	H'EC10 0C00/ H'EC40 0C00*	H'0000 0000	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
SSI1-0_BUSIF Data Register	SSI1-0_BUSIF	R/W	H'EC10 1000/ H'EC40 1000*	H'0000 0000	32
SSI1-1_BUSIF Data Register	SSI1-1_BUSIF	R/W	H'EC10 1400/ H'EC40 1400*	H'0000 0000	32
SSI1-2_BUSIF Data Register	SSI1-2_BUSIF	R/W	H'EC10 1800/ H'EC40 1800*	H'0000 0000	32
SSI1-3_BUSIF Data Register	SSI1-3_BUSIF	R/W	H'EC10 1C00/ H'EC40 1C00*	H'0000 0000	32
SSI2-0_BUSIF Data Register	SSI2-0_BUSIF	R/W	H'EC10 2000/ H'EC40 2000*	H'0000 0000	32
SSI2-1_BUSIF Data Register	SSI2-1_BUSIF	R/W	H'EC10 2400/ H'EC40 2400*	H'0000 0000	32
SSI2-2_BUSIF Data Register	SSI2-2_BUSIF	R/W	H'EC10 2800/ H'EC40 2800*	H'0000 0000	32
SSI2-3_BUSIF Data Register	SSI2-3_BUSIF	R/W	H'EC10 2C00/ H'EC40 2C00*	H'0000 0000	32
SSI3_BUSIF Data Register	SSI3_BUSIF	R/W	H'EC10 3000/ H'EC40 3000*	H'0000 0000	32
SSI4_BUSIF Data Register	SSI4_BUSIF	R/W	H'EC10 4000/ H'EC40 4000*	H'0000 0000	32
SSI5_BUSIF Data Register	SSI5_BUSIF	R/W	H'EC10 5000/ H'EC40 5000*	H'0000 0000	32
SSI6_BUSIF Data Register	SSI6_BUSIF	R/W	H'EC10 6000/ H'EC40 6000*	H'0000 0000	32
SSI7_BUSIF Data Register	SSI7_BUSIF	R/W	H'EC10 7000/ H'EC40 7000*	H'0000 0000	32
SSI8_BUSIF Data Register	SSI8_BUSIF	R/W	H'EC10 8000/ H'EC40 8000*	H'0000 0000	32
SSI9-0_BUSIF Data Register	SSI9-0_BUSIF	R/W	H'EC10 9000/ H'EC40 9000*	H'0000 0000	32
SSI9-1_BUSIF Data Register	SSI9-1_BUSIF	R/W	H'EC10 9400/ H'EC40 9400*	H'0000 0000	32
SSI9-2_BUSIF Data Register	SSI9-2_BUSIF	R/W	H'EC10 9800/ H'EC40 9800*	H'0000 0000	32
SSI9-3_BUSIF Data Register	SSI9-3_BUSIF	R/W	H'EC10 9C00/ H'EC40 9C00*	H'0000 0000	32

Note: * Address H'EC10 XXXX is used for data transfer with the Audio-DMAC. Address H'EC40 XXXX is used for data transfer with the Audio-DMAC-Peripheral-Peripheral.

28.2 Register Description

Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in longword units.

28.2.1 SSIn BUSIF Mode Register (SSIn_BUSIF_MODE)

Note: n = 0-0 to 0-3, 1-0 to 1-3, 2-0 to 2-3, 3 to 8, or 9-0 to 9-3

Function: SSIn_BUSIF_MODE determines the initial settings of the bus interface.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	sft_dir	sft_num			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	word_swap	—	—	—	—	—	—	—	dma
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	sft_dir	0	R/W	ssi***n***_busif_shift_dir Selects the bit-shift direction for valid bit position adjustment in the SSI***n***_BUSIF input and output data. 0: Shift to left. 1: Shift to right.
19 to 16	sft_num	0000	R/W	ssi***n***_busif_shift_num Selects the bit-shift count for valid bit position adjustment in the SSI***n***_BUSIF input and output data. 0000: 0 bit 0001: 1 bit 0010: 2 bits 0011: 3 bits 0100: 4 bits 0101: 5 bits 0110: 6 bits 0111: 7 bits 1000: 8 bits 1001: 9 bits 1010: 10 bits 1011: 11 bits 1100: 12 bits 1101: 13 bits 1110: 14 bits 1111: 15 bits
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	word_swap	0	R/W	word_swap_en Swaps the word order in SSI***n***_BUSIF. 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	dma	1	R/W	ssi***n***_dma Selects the access type for SSI***n***_BUSIF. 0: PIO access (setting prohibited) 1: DMA access Be sure to specify the DMA access.

28.2.2 SSIm BUSIF Audio Information Register (SSIm_BUSIF_ADINR)

Note: m = 0-0, 1-0, 2-0, 3 to 8, or 9-0

Function: SSIm_BUSIF_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	OTBL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number. 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved

28.2.3 SSIp BUSIF Audio Information Register (SSIp_BUSIF_ADINR)

Note: p = 0-1 to 0-3, 1-1 to 1-3, 2-1 to 2-3, or 9-1 to 9-3

Function: SSIp_BUSIF_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	OTBL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number. 0000: 0 (none) 0001: 1 channel 0010: 2 channels 0011 to 1111: Reserved

28.2.4 SSIm BUSIF Data Align Register (SSIm_BUSIF_DALIGN)

Note: m = 0-0, 1-0, 2-0, 3 to 8, or 9-0

Function: SSIm_BUSIF_DALIGN determines the initial settings of the SSIm route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	place7			—	place6			—	place5			—	place4		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	place3			—	place2			—	place1			—	place0		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	place7	111	R/W	Changes the stream data order. These bits are used for the 8-channel setting. For the 6- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 7 on the output side. 000: Data at input-side place 0 is sent to output-side place 7. 001: Data at input-side place 1 is sent to output-side place 7. 010: Data at input-side place 2 is sent to output-side place 7. 011: Data at input-side place 3 is sent to output-side place 7. 100: Data at input-side place 4 is sent to output-side place 7. 101: Data at input-side place 5 is sent to output-side place 7. 110: Data at input-side place 6 is sent to output-side place 7. 111: Data at input-side place 7 is sent to output-side place 7.
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26 to 24	place6	110	R/W	Changes the stream data order. These bits are used for the 8-channel setting. For the 6- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 6 on the output side. 000: Data at input-side place 0 is sent to output-side place 6. 001: Data at input-side place 1 is sent to output-side place 6. 010: Data at input-side place 2 is sent to output-side place 6. 011: Data at input-side place 3 is sent to output-side place 6. 100: Data at input-side place 4 is sent to output-side place 6. 101: Data at input-side place 5 is sent to output-side place 6. 110: Data at input-side place 6 is sent to output-side place 6. 111: Data at input-side place 7 is sent to output-side place 6.
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
22 to 20	place5	101	R/W	Changes the stream data order. These bits are used for the 6- or more channel setting. For the 4- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 5 on the output side. 000: Data at input-side place 0 is sent to output-side place 5. 001: Data at input-side place 1 is sent to output-side place 5. 010: Data at input-side place 2 is sent to output-side place 5. 011: Data at input-side place 3 is sent to output-side place 5. 100: Data at input-side place 4 is sent to output-side place 5. 101: Data at input-side place 5 is sent to output-side place 5. 110: Data at input-side place 6 is sent to output-side place 5. 111: Data at input-side place 7 is sent to output-side place 5.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	place4	100	R/W	Changes the stream data order. These bits are used for the 6- or more channel setting. For the 4- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 4 on the output side. 000: Data at input-side place 0 is sent to output-side place 4. 001: Data at input-side place 1 is sent to output-side place 4. 010: Data at input-side place 2 is sent to output-side place 4. 011: Data at input-side place 3 is sent to output-side place 4. 100: Data at input-side place 4 is sent to output-side place 4. 101: Data at input-side place 5 is sent to output-side place 4. 110: Data at input-side place 6 is sent to output-side place 4. 111: Data at input-side place 7 is sent to output-side place 4.
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	place3	011	R/W	Changes the stream data order. These bits are used for the 4- or more channel setting. For the 2- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 3 on the output side. 000: Data at input-side place 0 is sent to output-side place 3. 001: Data at input-side place 1 is sent to output-side place 3. 010: Data at input-side place 2 is sent to output-side place 3. 011: Data at input-side place 3 is sent to output-side place 3. 100: Data at input-side place 4 is sent to output-side place 3. 101: Data at input-side place 5 is sent to output-side place 3. 110: Data at input-side place 6 is sent to output-side place 3. 111: Data at input-side place 7 is sent to output-side place 3.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	place2	010	R/W	Changes the stream data order. These bits are used for the 4- or more channel setting. For the 2- or less channel setting or TDM split mode setting (tdm_split = 1), the initial value should not be changed. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 2 on the output side. 000: Data at input-side place 0 is sent to output-side place 2. 001: Data at input-side place 1 is sent to output-side place 2. 010: Data at input-side place 2 is sent to output-side place 2. 011: Data at input-side place 3 is sent to output-side place 2. 100: Data at input-side place 4 is sent to output-side place 2. 101: Data at input-side place 5 is sent to output-side place 2. 110: Data at input-side place 6 is sent to output-side place 2. 111: Data at input-side place 7 is sent to output-side place 2.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	place1	001	R/W	Changes the stream data order. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 1 on the output side. • When TDM split mode is used (tdm_split = 1) 000: Data at input-side place 0 is sent to output-side place 1. 001: Data at input-side place 1 is sent to output-side place 1. Other settings are prohibited. • When TDM split mode is not used (tdm_split = 0) 000: Data at input-side place 0 is sent to output-side place 1. 001: Data at input-side place 1 is sent to output-side place 1. 010: Data at input-side place 2 is sent to output-side place 1. 011: Data at input-side place 3 is sent to output-side place 1. 100: Data at input-side place 4 is sent to output-side place 1. 101: Data at input-side place 5 is sent to output-side place 1. 110: Data at input-side place 6 is sent to output-side place 1. 111: Data at input-side place 7 is sent to output-side place 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	place0	000	R/W	Changes the stream data order. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 0 on the output side. • When TDM split mode is used (tdm_split = 1) 000: Data at input-side place 0 is sent to output-side place 0. 001: Data at input-side place 1 is sent to output-side place 0. Other settings are prohibited. • When TDM split mode is not used (tdm_split = 0) 000: Data at input-side place 0 is sent to output-side place 0. 001: Data at input-side place 1 is sent to output-side place 0. 010: Data at input-side place 2 is sent to output-side place 0. 011: Data at input-side place 3 is sent to output-side place 0. 100: Data at input-side place 4 is sent to output-side place 0. 101: Data at input-side place 5 is sent to output-side place 0. 110: Data at input-side place 6 is sent to output-side place 0. 111: Data at input-side place 7 is sent to output-side place 0.

28.2.5 SSIp BUSIF Data Align Register (SSIp_BUSIF_DALIGN)

Note: p = 0-1 to 0-3, 1-1 to 1-3, 2-1 to 2-3, or 9-1 to 9-3

Function: SSIp_BUSIF_DALIGN determines the initial settings of the SSIp route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	place1	—	—	—	place0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	place1	1	R/W	Changes the stream data order. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 1 on the output side. 0: Data at input-side place 0 is sent to output-side place 1. 1: Data at input-side place 1 is sent to output-side place 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	place0	0	R/W	Changes the stream data order. The data order is changed between the SSI and bus interface. Selects the input-side data to be output to place 0 on the output side. 0: Data at input-side place 0 is sent to output-side place 0. 1: Data at input-side place 1 is sent to output-side place 0.

28.2.6 SSIq Mode Register (SSIq_MODE)

Note: q = 0-0, 1-0, 2-0, or 9-0

Function: SSIq_MODE determines the initial settings of the SSIq route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	fs_mode	—	—	—	—	tdm_split	—	—	—	—	—	—	—	tdm_ext
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	fs_mode	0	R/W	ssi***i***_fs_mode (***i*** = 0, 1, 2, or 9) Selects fs to be used with TDM split mode for ssi***i***. 0: ssi***i*** TDM split mode is used with 256 fs (stereo x 4). 1: ssi***i*** TDM split mode is used with 128 fs (monaural x 4).
12 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	tdm_split	0	R/W	ssi***i***_tdm_split (***i*** = 0, 1, 2, or 9) Selects whether or not TDM split mode is used for ssi***i***. 0: TDM split mode is not used for ssi***i*** (only ssi***i*** -0_BUSIF is used). 1: TDM split mode is used for ssi***i*** (ssi***i*** -1_BUSIF to ssi***i***-3_BUSIF are also used).
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	tdm_ext	0	R/W	ssi***i***_tdm_ext (***i*** = 0, 1, 2, or 9) Selects whether or not TDM extend mode is used for ssi***i***. 0: ssi***i*** TDM extend mode is not used. 1: ssi***i*** TDM extend mode is used.

Note: Bit 0 (tdm_ext) and bit 8 (tdm_split) cannot be set to 1 at the same time.

28.2.7 SSIr Mode Register (SSIr_MODE)

Note: r = 3 or 4

Function: SSIr_MODE determines the initial settings of the SSIr route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	tdm_ext
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	tdm_ext	0	R/W	ssi*r*_tdm_ext Selects whether or not TDM extend mode is used for ssi*r*. 0: ssi*r* TDM extend mode is not used. 1: ssi*r* TDM extend mode is used.

28.2.8 SSIq Control Register (SSIq_CONTROL)

Note: q = 0-0, 1-0, 2-0, or 9-0

Function: SSIq_CONTROL controls the start and stop of data transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	start_3	—	—	—	start_2	—	—	—	start_1	—	—	—	start_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	start_3	0	R/W	SSI***i-3***_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSI***i-3***. 0: Transfer is stopped. 1: Transfer is started.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	start_2	0	R/W	SSI***i-2***_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSI***i-2***. 0: Transfer is stopped. 1: Transfer is started.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	start_1	0	R/W	SSI***i-1***_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSI***i-1***. 0: Transfer is stopped. 1: Transfer is started.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	start_0	0	R/W	SSI***i-0***_start_flag (i = 0 to 2, 9) Starts or stops data transfer through SSI***i-0***. 0: Transfer is stopped. 1: Transfer is started.

Note: If only SSI***i-0*** is used and TDM split mode is not used, SSI***i-1***_start flag to SSI***i-3***_start flag should be set to 0 (transfer stopped).

28.2.9 SSIr Control Register (SSIr_CONTROL)

Note: r = 3 to 8

Function: SSIr_CONTROL controls the start and stop of data transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	start
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	start	0	R/W	SSI*r*_start_flag Starts or stops data transfer through SSI*r*. 0: Transfer is stopped. 1: Transfer is started.

28.2.10 SSIq Status Register (SSIq_STATUS)

Note: q = 0-0, 1-0, 2-0, 9-0

Function: SSIq_STATUS indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSIq interrupt enable register, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST	DTST	UIRQ	OIRQ	IIRQ	DIRQ	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	uf_3	uf_2	uf_1	uf_0	of_3	of_2	of_1	of_0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST	0	R	SSI***i***_FCST (i = 0 to 2, 9) Indicates the state of SSIFSR***i***_FCST. 0: — 1: The WS signal has stopped.
28	DTST	0	R	SSI***i***_DTST (i = 0 to 2, 9) Indicates the state of SSIFSR***i***_DTST. 0: — 1: The frequency switching has been detected.
27	UIRQ	0	R	SSI***i***_UIRQ (i = 0 to 2, 9) Indicates the state of SSISR***i***_UIRQ. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSICR***i***.UIEN = 0.
26	OIRQ	0	R	SSI***i***_OIRQ (i = 0 to 2, 9) Indicates the state of SSISR***i***_OIRQ. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSICR***i***.OIEN = 0.
25	IIRQ	0	R	SSI***i***_IIRQ (i = 0 to 2, 9) Indicates the state of SSISR***i***_IIRQ. 0: — 1: Idle state Note: Not indicated by the interrupt signal when SSICR***i***.IIEN = 0.

Bit	Bit Name	Initial Value	R/W	Description
24	DIRQ	0	R	SSI*i*_DIRQ (i = 0 to 2, 9) Indicates the state of SSISR*i*_DIRQ. 0: — 1: When SSICR*i*.TRMD is 0, DIRQ = 1 indicates that there are unread data in SSIRDR. When SSICR*i*.TRMD is 1, DIRQ = 1 indicates that data can be written to SSITDR. Note: Not indicated by the interrupt signal when SSICR*i*.DIEN = 0.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	uf_3	0	R	buf_under_flow*i*-3 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.uf*i*-3. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf*i*-3_ie = 0.
14	uf_2	0	R	buf_under_flow*i*-2 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.uf*i*-2. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf*i*-2_ie = 0.
13	uf_1	0	R	buf_under_flow*i*-1 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.uf*i*-1. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf*i*-1_ie = 0.
12	uf_0	0	R	buf_under_flow*i*-0 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.uf*i*-0. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.uf*i*-0_ie = 0.
11	of_3	0	R	buf_over_flow*i*-3 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.of*i*-3. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of*i*-3_ie = 0.
10	of_2	0	R	buf_over_flow*i*-2 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.of*i*-2. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of*i*-2_ie = 0.

Bit	Bit Name	Initial Value	R/W	Description
9	of_1	0	R	buf_over_flow*i*-1 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.of*i*-1. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of*i*-1_ie = 0.
8	of_0	0	R	buf_over_flow*i*-0 (i = 0 to 2, 9) Indicates the state of SSI_SYSTEM_STATUS2/3.of*i*-0. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSI_SYSTEM_INT_ENABLE2/3.of*i*-0_ie = 0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.11 SSIr Status Register (SSIr_STATUS)

Note: r = 3 to 8

Function: SSIr_STATUS indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSIr interrupt enable register, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST	DTST	UIRQ	OIRQ	IIRQ	DIRQ	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST	0	R	SSI***i***_FCST (i = 3 to 8) Indicates the state of SSIFSR***i***_FCST. 0: — 1: The WS signal has stopped.
28	DTST	0	R	SSI***i***_DTST (i = 3 to 8) Indicates the state of SSIFSR***i***_DTST. 0: — 1: The frequency switching has been detected.
27	UIRQ	0	R	SSI***i***_UIRQ (i = 3 to 8) Indicates the state of SSISR***i***_UIRQ. 0: — 1: An underflow has occurred. Note: Not indicated by the interrupt signal when SSICR***i***.UIEN = 0.
26	OIRQ	0	R	SSI***i***_OIRQ (i = 3 to 8) Indicates the state of SSISR***i***_OIRQ. 0: — 1: An overflow has occurred. Note: Not indicated by the interrupt signal when SSICR***i***.OIEN = 0.
25	IIRQ	0	R	SSI***i***_IIRQ (i = 3 to 8) Indicates the state of SSISR***i***_IIRQ. 0: — 1: Idle state Note: Not indicated by the interrupt signal when SSICR***i***.IIEN = 0.

Bit	Bit Name	Initial Value	R/W	Description
24	DIRQ	0	R	SSI*i*_DIRQ (i = 3 to 8) Indicates the state of SSISR*i*_DIRQ. 0: — 1: When SSICR*i*.TRMD is 0, DIRQ = 1 indicates that there are unread data in SSIRDR. When SSICR*i*.TRMD is 1, DIRQ = 1 indicates that data can be written to SSITDR. Note: Not indicated by the interrupt signal when SSICR*i*.DIEN = 0.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.12 SSIq Interrupt Enable Register (SSIq_INT_ENABLE_MAIN)

Note: q = 0-0, 1-0, 2-0, or 9-0

Function: SSIq_INT_ENABLE_MAIN enables or disables output of interrupts corresponding to the states indicated in the SSIq status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST_ie	DTST_ie	UIRQ_ie	OIRQ_ie	IIRQ_ie	DIRQ_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	uf_3_ie	uf_2_ie	uf_1_ie	uf_0_ie	of_3_ie	of_2_ie	of_1_ie	of_0_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST_ie	0	R/W	SSI*i*_FCST_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	DTST_ie	0	R/W	SSI*i*_DTST_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27	UIRQ_ie	0	R/W	SSI*i*_UIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
26	OIRQ_ie	0	R/W	SSI*i*_OIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
25	IIRQ_ie	0	R/W	SSI*i*_IIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
24	DIRQ_ie	0	R/W	SSI*i*_DIRQ_int_enable (i = 0 to 2,9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	uf_3_ie	0	R/W	buf_under_flow*i*-3_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	uf_2_ie	0	R/W	buf_under_flow*i*-2_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
13	uf_1_ie	0	R/W	buf_under_flow*i*-1_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	uf_0_ie	0	R/W	buf_under_flow*i*-0_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	of_3_ie	0	R/W	buf_over_flow*i*-3_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	of_2_ie	0	R/W	buf_over_flow*i*-2_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	of_1_ie	0	R/W	buf_ over_flow*i*-1_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	of_0_ie	0	R/W	buf_over_flow*i*-0_int_enable (i = 0 to 2, 9) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.13 SSIr Interrupt Enable Register (SSIr_INT_ENABLE_MAIN)

Note: r = 3 to 8

Function: SSIr_INT_ENABLE_MAIN enables or disables output of interrupts corresponding to the states indicated in the SSIr status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	FCST_ie	DTST_ie	UIRQ_ie	OIRQ_ie	IIRQ_ie	DIRQ_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	—	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	FCST_ie	0	R/W	SSI*i*_FCST_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	DTST_ie	0	R/W	SSI*i*_DTST_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27	UIRQ_ie	0	R/W	SSI*i*_UIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
26	OIRQ_ie	0	R/W	SSI*i*_OIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
25	IIRQ_ie	0	R/W	SSI*i*_IIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
24	DIRQ_ie	0	R/W	SSI*i*_DIRQ_int_enable (i = 3 to 8) 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	—	R	Reserved The read value is undefined. The write value should always be 0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.14 SSI Mode Register 0 (SSI_MODE0)

Function: SSI_MODE0 specifies the independent SSI transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	ind_word_swap9	ind_word_swap8	ind_word_swap7	ind_word_swap6	ind_word_swap5	ind_word_swap4	ind_word_swap3	ind_word_swap2	ind_word_swap1	ind_word_swap0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ind9	ind8	ind7	ind6	ind5	ind4	ind3	ind2	ind1	ind0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	ind_word_swap9	0	R/W	ind_word_swap_en9 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
24	ind_word_swap8	0	R/W	ind_word_swap_en8 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
23	ind_word_swap7	0	R/W	ind_word_swap_en7 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
22	ind_word_swap6	0	R/W	ind_word_swap_en6 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
21	ind_word_swap5	0	R/W	ind_word_swap_en5 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
20	ind_word_swap4	0	R/W	ind_word_swap_en4 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.

Bit	Bit Name	Initial Value	R/W	Description
19	ind_word_swap3	0	R/W	ind_word_swap_en3 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
18	ind_word_swap2	0	R/W	ind_word_swap_en2 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
17	ind_word_swap1	0	R/W	ind_word_swap_en1 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
16	ind_word_swap0	0	R/W	ind_word_swap_en0 Swaps the word order (only for access to SSITDR or SSIRDR). 0: Word order is not swapped. 1: Word order is swapped. Note: Select this function only when the data length is 16 bits.
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ind9	0	R/W	Independent SSI9 transfer setting 0: Independent SSI9 transfer is not performed. 1: Independent SSI9 transfer is performed.
8	ind8	0	R/W	Independent SSI8 transfer setting 0: Independent SSI8 transfer is not performed. 1: Independent SSI8 transfer is performed.
7	ind7	0	R/W	Independent SSI7 transfer setting 0: Independent SSI7 transfer is not performed. 1: Independent SSI7 transfer is performed.
6	ind6	0	R/W	Independent SSI6 transfer setting 0: Independent SSI6 transfer is not performed. 1: Independent SSI6 transfer is performed.
5	ind5	0	R/W	Independent SSI5 transfer setting 0: Independent SSI5 transfer is not performed. 1: Independent SSI5 transfer is performed.
4	ind4	0	R/W	Independent SSI transfer setting 0: Independent SSI transfer is not performed. 1: Independent SSI transfer is performed. These bits correspond to the SSI modules as follows. SSI3 = ssi_ind3 SSI4 = ssi_ind4
3	ind3	0	R/W	
2	ind2	0	R/W	Independent SSI2 transfer setting 0: Independent SSI2 transfer is not performed. 1: Independent SSI2 transfer is performed.

Bit	Bit Name	Initial Value	R/W	Description
1	ind1	0	R/W	Independent SSI1 transfer setting 0: Independent SSI1 transfer is not performed. 1: Independent SSI1 transfer is performed.
0	ind0	0	R/W	Independent SSI0 transfer setting 0: Independent SSI0 transfer is not performed. 1: Independent SSI0 transfer is performed.

28.2.15 SSI Mode Register 1 (SSI_MODE1)

Function: SSI_MODE1 specifies the SSI pin modes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	ssi34_sync	—	—	ssi4_pin	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ssi012_3mod	ssi2_pin		ssi1_pin	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	ssi34_sync	0	R/W	ssi34_sync_mode Selects whether to synchronize SSI3 and SSI4. 0: SSI3 and SSI4 are not synchronized. 1: SSI3 and SSI4 are synchronized. This bit can be set to 1 only when the ssi4_pin_mode bits are set to 01 or 10.
19, 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	ssi4_pin	00	R/W	ssi4_pin_mode Select the connections of the SSI_SCK4 and SSI_WS4 pins. 00: SSI3 and SSI4 use their own pins independently. 01: The SSI3 pins are used in common by SSI3 and SSI4. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI3 are used. 10: The SSI3 pins are used in common by SSI3 and SSI4. SSI3 works as the master and SSI4 works as a slave. The SSI_WS and SSI_SCK pins of SSI3 are used. 11: Setting prohibited
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	ssi012_3mod	0	R/W	ssi012_3module_mode Selects whether to use three modules (SSI0, SSI1, and SSI2) together as six channels. 0: SSI0, SSI1, and SSI2 are not used as six channels. 1: SSI0, SSI1, and SSI2 are used as six channels. This bit should be cleared to 0 when the ssi1_pin_mode or ssi2_pin_mode bits are set to 00. It can be set to 1 only when the ssi1_pin_mode and ssi2_pin_mode bits are set to 01 or when the ssi1_pin_mode and ssi2_pin_mode bits are set to 10. Either ssi012_3module_mode or ssi0129_4module_mode must be set to 1.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	ssi2_pin	00	R/W	ssi2_pin_mode Select the connections of the SSI_SCK2 and SSI_WS2 pins. 00: SSI0 and SSI2 use their own pins independently. 01: The SSI0 pins are used in common by SSI0 and SSI2. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used. 10: The SSI0 pins are used in common by SSI0 and SSI2. SSI0 works as the master and SSI2 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used. 11: Setting prohibited
1, 0	ssi1_pin	00	R/W	ssi1_pin_mode Select the connections of the SSI_SCK1 and SSI_WS1 pins. 00: SSI0 and SSI1 use their own pins independently. 01: The SSI0 pins are used in common by SSI0 and SSI1. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used. 10: The SSI0 pins are used in common by SSI0 and SSI1. SSI0 works as the master and SSI1 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used. 11: Setting prohibited

28.2.16 SSI Mode Register 2 (SSI_MODE2)

Function: SSI_MODE2 specifies the SSI pin modes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ssi0129_4mod	—	ssi9_pin		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	ssi0129_4mod	0	R/W	ssi0129_4module_mode Selects whether to use four modules (SSI0, SSI1, SSI2, and SSI9) together as eight channels. 0: SSI0, SSI1, SSI2, and SSI9 are not used as eight channels. 1: SSI0, SSI1, SSI2, and SSI9 are used as eight channels. This bit should be cleared to 0 when the ssi1_pin_mode or ssi2_pin_mode bits are set to 00, or when ssi9_pin_mode bits are set to 000. It can be set to 1 only when the ssi1_pin_mode and ssi2_pin_mode bits are set to 01 and the ssi9_pin_mode bits are set to 001, or when the ssi1_pin_mode and ssi2_pin_mode bits are set to 10 and the ssi9_pin_mode bits are set to 010. Either ssi0129_4module_mode or ssi012_3module_mode must be set to 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	ssi9_pin	000	R/W	ssi9_pin_mode Selects the connections of the SSI_SCK9 and SSI_WS9 pins. 000: SSI0 and SSI9 use their own pins independently. 001: The SSI0 pins are used in common by SSI0 and SSI9. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used. 010: The SSI0 pins are used in common by SSI0 and SSI9. SSI0 works as the master and SSI9 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used. 011: Setting prohibited 100: Setting prohibited 101: The SSI3 pins are used in common by SSI3 and SSI9. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI3 are used. 110: The SSI3 pins are used in common by SSI3 and SSI9. SSI3 works as the master and SSI9 works as a slave. The SSI_WS and SSI_SCK pins of SSI3 are used. 111: Setting prohibited

28.2.17 SSI Mode Register 3 (SSI_MODE3)

Function: SSI_MODE3 specifies the SSI pin modes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ssi3_pin	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	ssi3_pin	00	R/W	ssi3_pin_mode Select the connections of the SSI_SCK3 and SSI_WS3 pins. 00: SSI0 and SSI3 use their own pins independently. 01: The SSI0 pins are used in common by SSI0 and SSI3. Both modules work as slaves. The SSI_WS and SSI_SCK pins of SSI0 are used. 10: The SSI0 pins are used in common by SSI0 and SSI3. SSI0 works as the master and SSI3 works as a slave. The SSI_WS and SSI_SCK pins of SSI0 are used. 11: Setting prohibited When setting these bits to use the pins in common by SSI0 and SSI3, ssi4_pin_mode should be 00 and ssi9_pin_mode should be 000, 001, or 010 (selection of the SSI3 pins is prohibited).

28.2.18 SSI Control Register (SSI_CONTROL)

Function: SSI_CONTROL controls the startup of the SSI modules when multiple SSI modules are used at the same time.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	ssi34	—	—	—	ssi0129
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	ssi34	0	R/W	ssi34_enable Starts or stops data transfer through two SSI modules (SSI3 and SSI4) at the same time. 0: Transfer through SSI3 and SSI4 is stopped. 1: Transfer through SSI3 and SSI4 is started.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ssi0129	0	R/W	ssi0129_enable • When ssi012_3module_mode is 1 Starts or stops data transfer through three SSI modules (SSI0, SSI1, and SSI2) at the same time. 0: Transfer through SSI0, SSI1, and SSI2 is stopped. 1: Transfer through SSI0, SSI1, and SSI2 is started. • When ssi0129_4module_mode is 1 Starts or stops data transfer through four SSI modules (SSI0, SSI1, SSI2, and SSI9) at the same time. 0: Transfer through SSI0, SSI1, SSI2, and SSI9 is stopped. 1: Transfer through SSI0, SSI1, SSI2, and SSI9 is started.

Note: This function should be used only when data is transferred through multiple SSI modules in synchronization. When using each SSI module independently, use the EN bit of SSICRn (n = 0 to 4 and 9) for the SSI module to control the transfer.

28.2.19 SSI SYSTEM Status Register 0 (SSI_SYSTEM_STATUS0)

Function: SSI_SYSTEM_STATUS0 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI_SYSTEM interrupt enable register 0, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	of2-3	of2-2	of2-1	of2-0	of1-3	of1-2	of1-1	of1-0	of0-3	of0-2	of0-1	of0-0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	of2-3	0	R/WC1	buf_over_flow2-3 Indicates the state of the SSI2-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
10	of2-2	0	R/WC1	buf_over_flow2-2 Indicates the state of the SSI2-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
9	of2-1	0	R/WC1	buf_over_flow2-1 Indicates the state of the SSI2-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
8	of2-0	0	R/WC1	buf_over_flow2-0 Indicates the state of the SSI2-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
7	of1-3	0	R/WC1	buf_over_flow1-3 Indicates the state of the SSI1-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
6	of1-2	0	R/WC1	buf_over_flow1-2 Indicates the state of the SSI1-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
5	of1-1	0	R/WC1	buf_over_flow1-1 Indicates the state of the SSI1-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
4	of1-0	0	R/WC1	buf_over_flow1-0 Indicates the state of the SSI1-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
3	of0-3	0	R/WC1	buf_over_flow0-3 Indicates the state of the SSI0-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
2	of0-2	0	R/WC1	buf_over_flow0-2 Indicates the state of the SSI0-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
1	of0-1	0	R/WC1	buf_over_flow0-1 Indicates the state of the SSI0-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
0	of0-0	0	R/WC1	buf_over_flow0-0 Indicates the state of the SSI0-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.

28.2.20 SSI SYSTEM Status Register 1 (SSI_SYSTEM_STATUS1)

Function: SSI_SYSTEM_STATUS1 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI_SYSTEM interrupt enable register 1, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	of9-3	of9-2	of9-1	of9-0	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	of9-3	0	R/WC1	buf_over_flow9-3 Indicates the state of the SSI9-3_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
6	of9-2	0	R/WC1	buf_over_flow9-2 Indicates the state of the SSI9-2_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
5	of9-1	0	R/WC1	buf_over_flow9-1 Indicates the state of the SSI9-1_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
4	of9-0	0	R/WC1	buf_over_flow9-0 Indicates the state of the SSI9-0_BUSIF buffer. 0: Normal operation 1: An overflow has occurred.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.21 SSI SYSTEM Status Register 2 (SSI_SYSTEM_STATUS2)

Function: SSI_SYSTEM_STATUS2 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI_SYSTEM interrupt enable register 2, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	uf2-3	uf2-2	uf2-1	uf2-0	uf1-3	uf1-2	uf1-1	uf1-0	uf0-3	uf0-2	uf0-1	uf0-0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	uf2-3	0	R/WC1	buf_under_flow2-3 Indicates the state of the SSI2-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
10	uf2-2	0	R/WC1	buf_under_flow2-2 Indicates the state of the SSI2-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
9	uf2-1	0	R/WC1	buf_under_flow2-1 Indicates the state of the SSI2-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
8	uf2-0	0	R/WC1	buf_under_flow2-0 Indicates the state of the SSI2-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
7	uf1-3	0	R/WC1	buf_under_flow1-3 Indicates the state of the SSI1-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
6	uf1-2	0	R/WC1	buf_under_flow1-2 Indicates the state of the SSI1-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
5	uf1-1	0	R/WC1	buf_under_flow1-1 Indicates the state of the SSI1-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
4	uf1-0	0	R/WC1	buf_under_flow1-0 Indicates the state of the SSI1-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
3	uf0-3	0	R/WC1	buf_under_flow0-3 Indicates the state of the SSI0-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
2	uf0-2	0	R/WC1	buf_under_flow0-2 Indicates the state of the SSI0-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
1	uf0-1	0	R/WC1	buf_under_flow0-1 Indicates the state of the SSI0-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
0	uf0-0	0	R/WC1	buf_under_flow0-0 Indicates the state of the SSI0-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.

28.2.22 SSI SYSTEM Status Register 3 (SSI_SYSTEM_STATUS3)

Function: SSI_SYSTEM_STATUS3 indicates the internal buffer state. When a bit in this register is set, its status is indicated by the corresponding interrupt signal. However, when the interrupt output is masked by the SSI_SYSTEM interrupt enable register 3, the interrupt signal is not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	uf9-3	uf9-2	uf9-1	uf9-0	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	uf9-3	0	R/WC1	buf_under_flow9-3 Indicates the state of the SSI9-3_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
6	uf9-2	0	R/WC1	buf_under_flow9-2 Indicates the state of the SSI9-2_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
5	uf9-1	0	R/WC1	buf_under_flow9-1 Indicates the state of the SSI9-1_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
4	uf9-0	0	R/WC1	buf_under_flow9-0 Indicates the state of the SSI9-0_BUSIF buffer. 0: Normal operation 1: An underflow has occurred.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.23 SSI SYSTEM Interrupt Enable Register 0 (SSI_SYSTEM_INT_ENABLE0)

Function: SSI_SYSTEM_INT_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	of2-3_ie	of2-2_ie	of2-1_ie	of2-0_ie	of1-3_ie	of1-2_ie	of1-1_ie	of1-0_ie	of0-3_ie	of0-2_ie	of0-1_ie	of0-0_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	of2-3_ie	0	R/W	buf_over_flow2-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	of2-2_ie	0	R/W	buf_over_flow2-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	of2-1_ie	0	R/W	buf_over_flow2-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	of2-0_ie	0	R/W	buf_over_flow2-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	of1-3_ie	0	R/W	buf_over_flow1-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	of1-2_ie	0	R/W	buf_over_flow1-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of1-1_ie	0	R/W	buf_over_flow1-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of1-0_ie	0	R/W	buf_over_flow1-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	of0-3_ie	0	R/W	buf_over_flow0-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	of0-2_ie	0	R/W	buf_over_flow0-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
1	of0-1_ie	0	R/W	buf_over_flow0-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	of0-0_ie	0	R/W	buf_over_flow0-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

28.2.24 SSI SYSTEM Interrupt Enable Register 1 (SSI_SYSTEM_INT_ENABLE1)

Function: SSI_SYSTEM_INT_ENABLE1 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	of9-3_ie	of9-2_ie	of9-1_ie	of9-0_ie	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	of9-3_ie	0	R/W	buf_over_flow9-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	of9-2_ie	0	R/W	buf_over_flow9-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of9-1_ie	0	R/W	buf_over_flow9-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of9-0_ie	0	R/W	buf_over_flow9-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.25 SSI SYSTEM Interrupt Enable Register 2 (SSI_SYSTEM_INT_ENABLE2)

Function: SSI_SYSTEM_INT_ENABLE2 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	uf2-3_ie	uf2-2_ie	uf2-1_ie	uf2-0_ie	uf1-3_ie	uf1-2_ie	uf1-1_ie	uf1-0_ie	uf0-3_ie	uf0-2_ie	uf0-1_ie	uf0-0_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	uf2-3_ie	0	R/W	buf_under_flow2-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	uf2-2_ie	0	R/W	buf_under_flow2-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	uf2-1_ie	0	R/W	buf_under_flow2-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	uf2-0_ie	0	R/W	buf_under_flow2-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	uf1-3_ie	0	R/W	buf_under_flow1-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	uf1-2_ie	0	R/W	buf_under_flow1-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf1-1_ie	0	R/W	buf_under_flow1-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf1-0_ie	0	R/W	buf_under_flow1-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	uf0-3_ie	0	R/W	buf_under_flow0-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	uf0-2_ie	0	R/W	buf_under_flow0-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
1	uf0-1_ie	0	R/W	buf_under_flow0-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	uf0-0_ie	0	R/W	buf_under_flow0-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

28.2.26 SSI SYSTEM Interrupt Enable Register 3 (SSI_SYSTEM_INT_ENABLE3)

Function: SSI_SYSTEM_INT_ENABLE3 enables or disables output of interrupts corresponding to the states indicated in the SSI SYSTEM status register 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

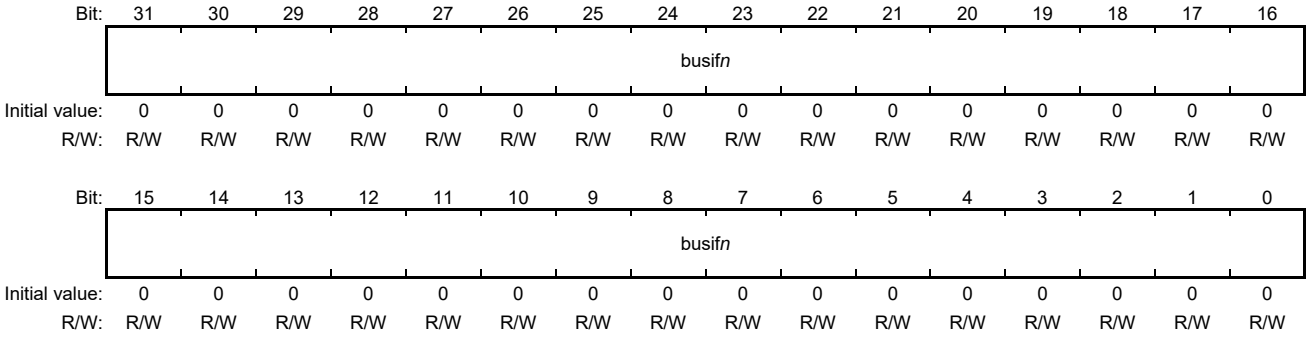
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	uf9-3_ie	uf9-2_ie	uf9-1_ie	uf9-0_ie	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	uf9-3_ie	0	R/W	buf_under_flow9-3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
6	uf9-2_ie	0	R/W	buf_under_flow9-2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf9-1_ie	0	R/W	buf_under_flow9-1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf9-0_ie	0	R/W	buf_under_flow9-0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

28.2.27 SSIn_BUSIF Data Registers (SSIn_BUSIF)

Note: n = 0-0 to 0-3, 1-0 to 1-3, 2-0 to 2-3, 3 to 8, or 9-0 to 9-3

Function: SSIn_BUSIF is a window register in which data is stored during data transfer via SSIn_BUSIF. These registers are used for both transmission and reception.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	busif***n***	H'00000000	R/W	These bits are used to hold the data during data transfer via SSIn_BUSIFn. This register is used for both transmission and reception. This register can only be written to during transmission and only be read from during reception.

28.3 Operation

28.3.1 Module Specifications

Table 28.3 shows the correspondences between the modules and functions.

Table 28.3 Function Correspondences

			Format		
		External Interface	**Basic Configuration**	**TDM Extend Mode**	**TDM Split Mode**
1	SSI0 SSI1 SSI2 SSI9	I2S	Supported	Not supported	Not supported
2	SSI0 SSI1 SSI2 SSI9	TDM	Supported	Supported	Supported
3	SSI0 SSI1 SSI2	I2S × 3 (multichannel)	Supported	Not supported	Not supported
4	SSI0 SSI1 SSI2 SSI9	I2S × 4 (multichannel)	Supported	Not supported	Not supported
5	SSI3 SSI4	I2S	Supported	Not supported	Not supported
6	SSI3 SSI4	TDM	Supported	Supported	Not supported
7	SSI5 SSI6 SSI7 SSI8	I2S	Supported	Not supported	Not supported
8	SSI5 SSI6 SSI7 SSI8	TDM	Not supported	Not supported	Not supported

28.3.2 Basic Configuration

Data transfer is performed between the SSIU and other audio modules or external memories via BUSIF connected to the audio local bus and the audio DMA bus. Figure 28.3 shows the data transfer of SSI0. As shown in Figure 28.3, SSI0_1_BUSIF, SSI0_2_BUSIF, and SSI0_3_BUSIF are not used. This basic configuration is also applied to SSI1, SSI2, and SSI9. Figure 28.4 shows the data transfer of SSI3, which is also applied to SSI4 to SSI8.

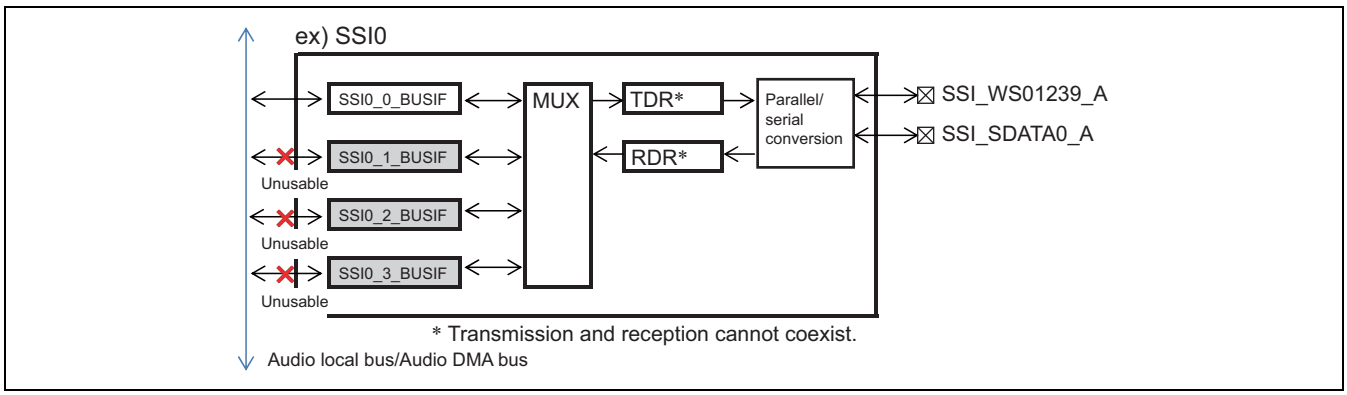


Figure 28.3 Basic Configuration (SSI0)

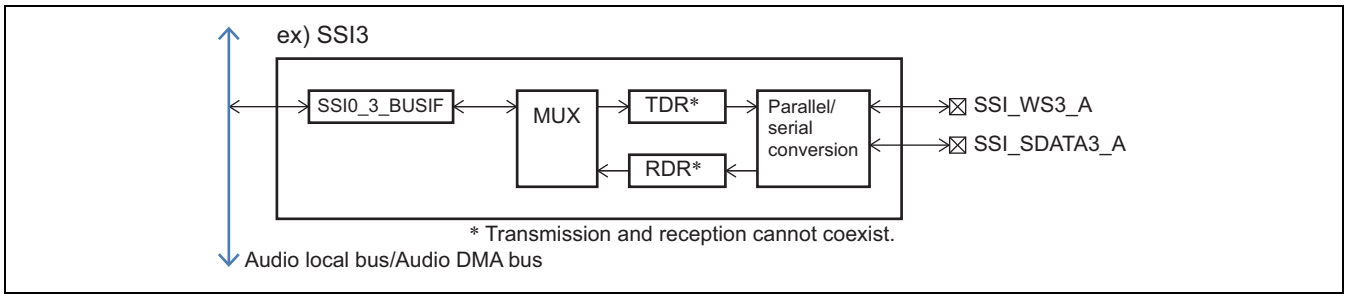


Figure 28.4 Basic Configuration (SSI3)

28.3.3 Configuration with Multiple SSI Modules

Multichannel data transfer can be performed by using multiple SSI modules. The available combination of modules is SSI0, SSI1, and SSI2 or SSI0, SSI1, SSI2, and SSI9.

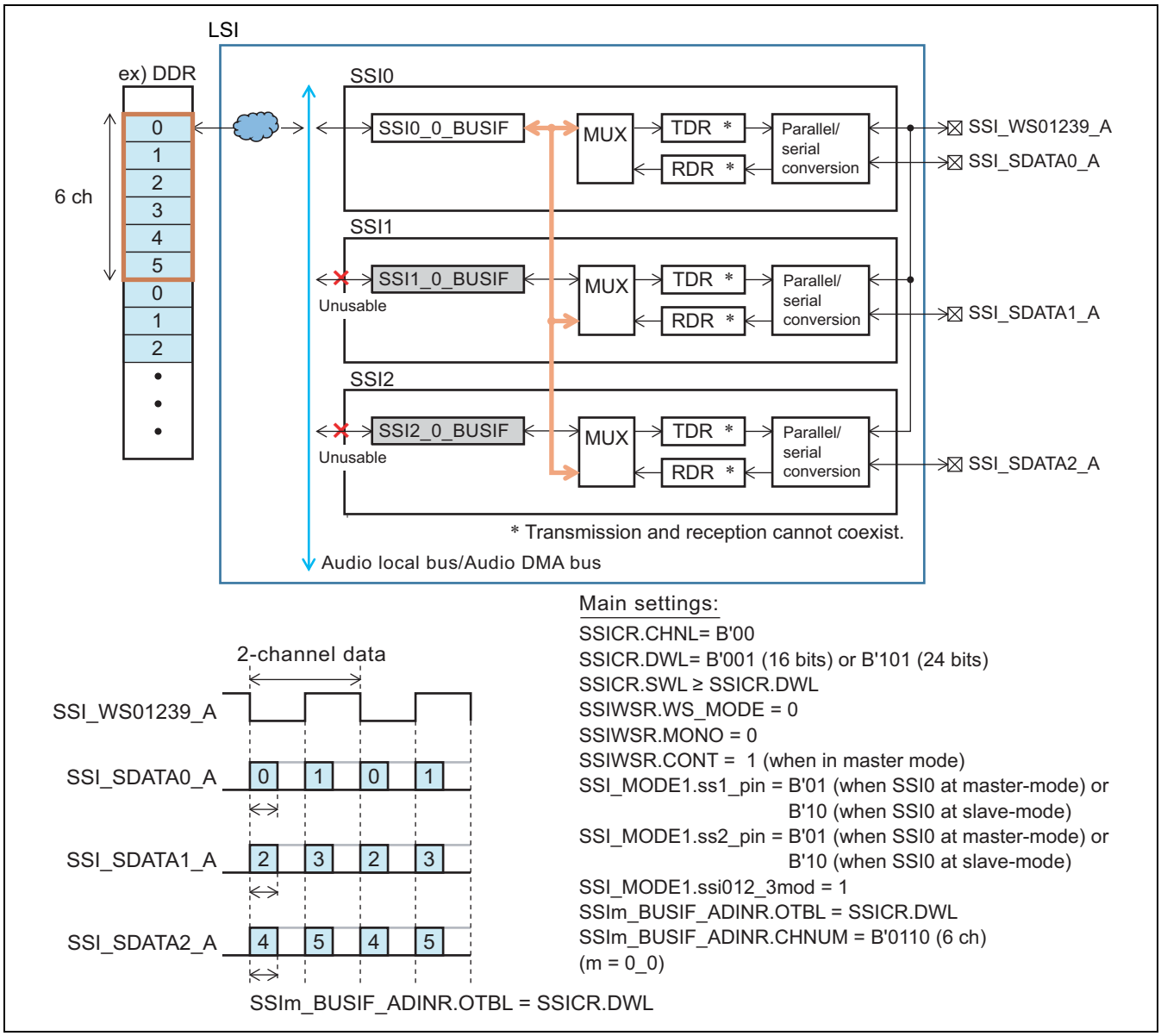


Figure 28.5 Multichannel Data Transfer (Using SSI0, SSI1 and SSI2)

Note: When the above configuration is used, SSI0_1_BUSIF, SSI0_2_BUSIF, SSI0_3_BUSIF, all the BUSIFs of SSI1and SSI2 cannot be used.

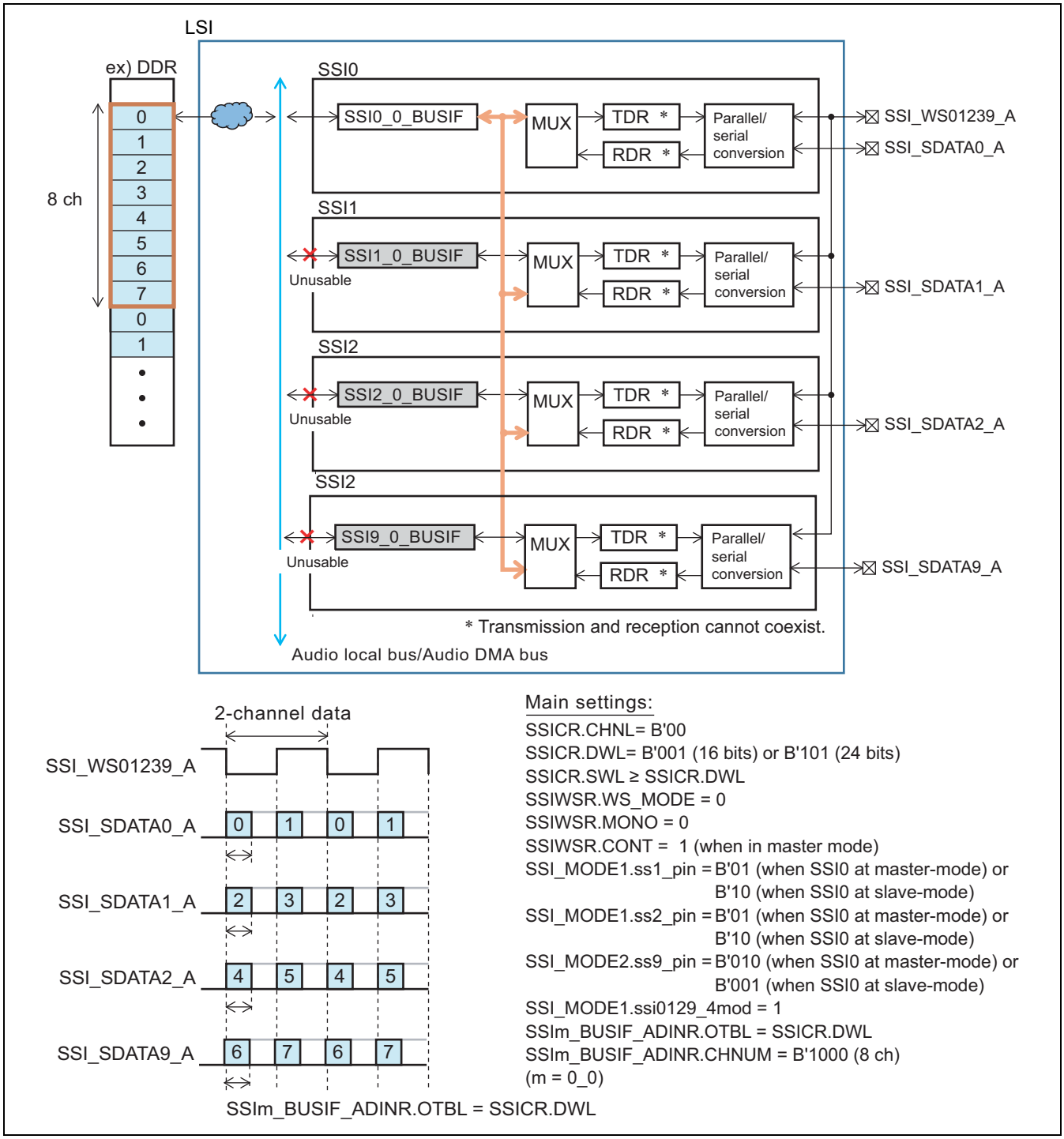


Figure 28.6 Multichannel Data Transfer (Using SSI0, SSI1, SSI2 and SSI9)

Note: When the above configuration is used, SSI0_1_BUSIF, SSI0_2_BUSIF, SSI0_3_BUSIF, all the BUSIFs of SSI1, SSI2, and SSI9 cannot be used.

28.3.4 TDM Format Extension Function (TDM Extend Mode)

The TDM format extension function allows operation with 8-channel data in the serial bus and 6-channel data inside the RZ/G1C, or operation with 6-channel data in the serial bus and 8-channel data inside the RZ/G1C. This function is supported by SSI0, SSI1, SSI2, SSI3, SSI4, and SSI9.

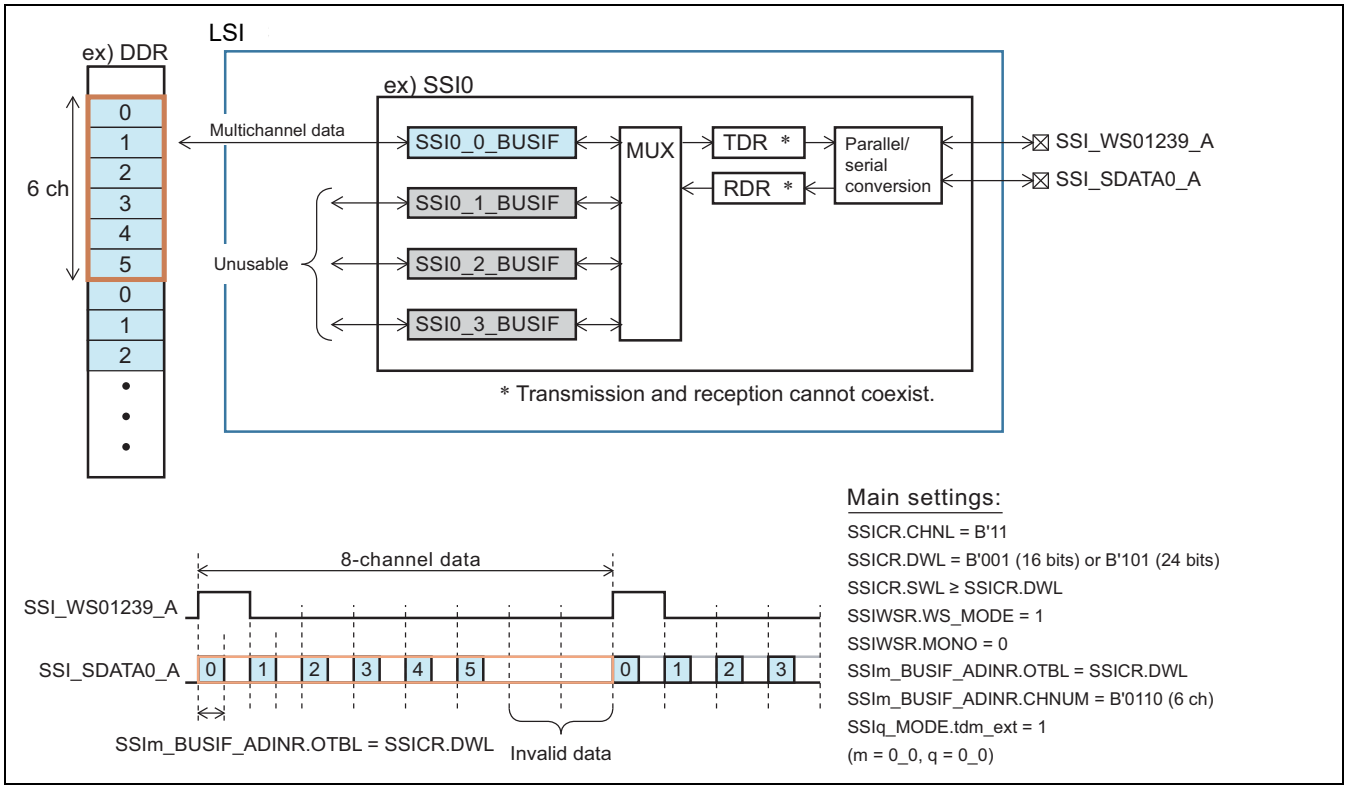


Figure 28.7 TDM Extend Mode Operation with 8-channel Data in Serial Bus and 6-channel Data Inside the RZ/G1C (SSI0)

Note: When the above configuration is used, SSI0_1_BUSIF, SSI0_2_BUSIF, and SSI0_3_BUSIF cannot be used.

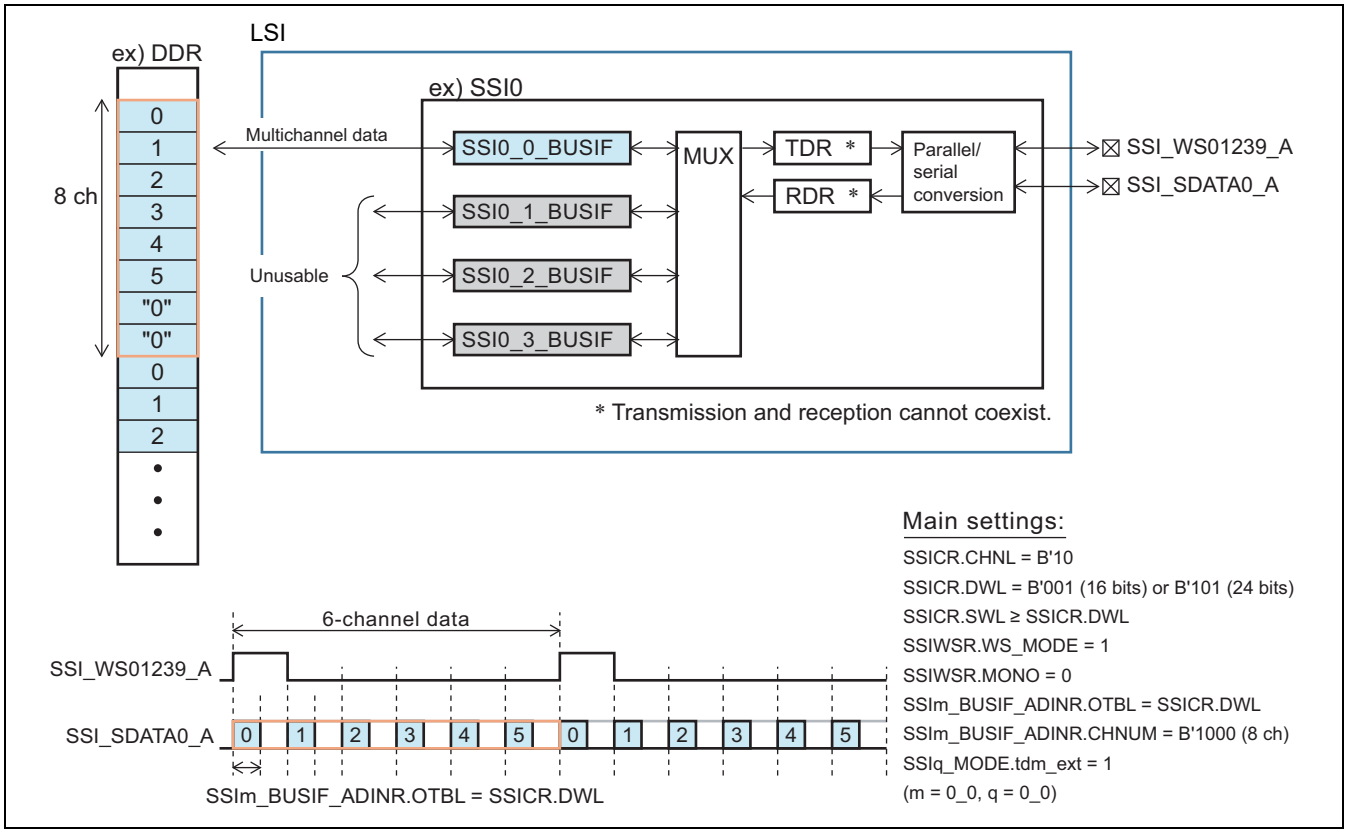


Figure 28.8 TDM Extend Mode Operation with 6-channel Data in Serial Bus and 8-channel Data Inside the RZ/G1C (SSI0)

Note: When the above configuration is used, SSI0_1_BUSIF, SSI0_2_BUSIF, and SSI0_3_BUSIF cannot be used.

28.3.5 TDM Format Split Function (TDM Split Mode)

The TDM format split function (TDM split mode) allows connecting four independent monaural or stereo data inside the RZ/G1C and outputting the data in the TDM format, and splitting TDM format input data into four independent monaural or stereo data and distributing the data inside the RZ/G1C. This function is supported by SSI0, SSI1, SSI2, and SSI9.

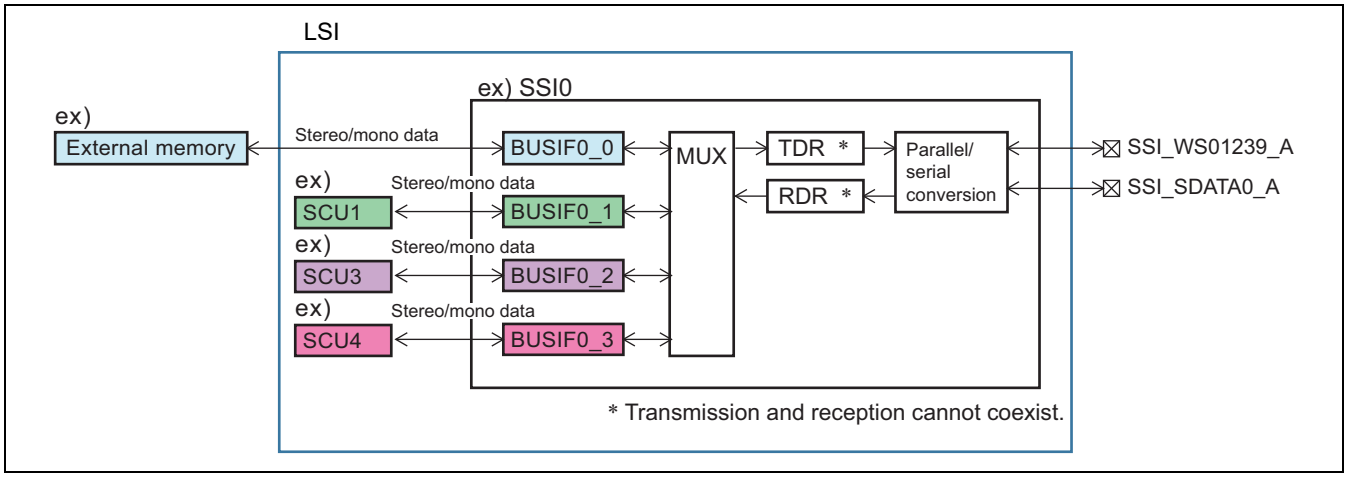


Figure 28.9 TDM Split Mode

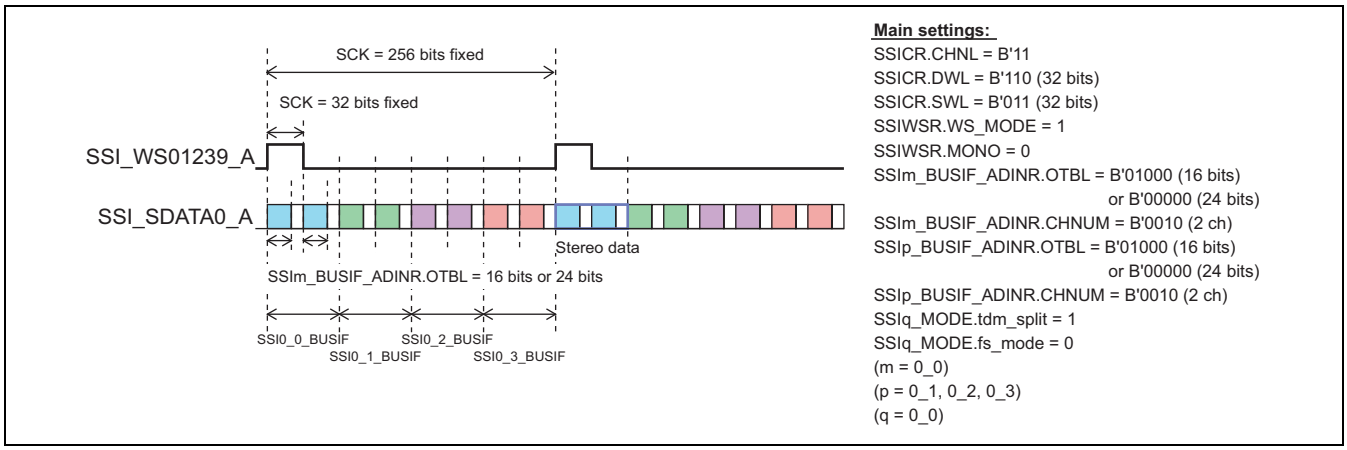


Figure 28.10 TDM Split Mode (Stereo × 4)

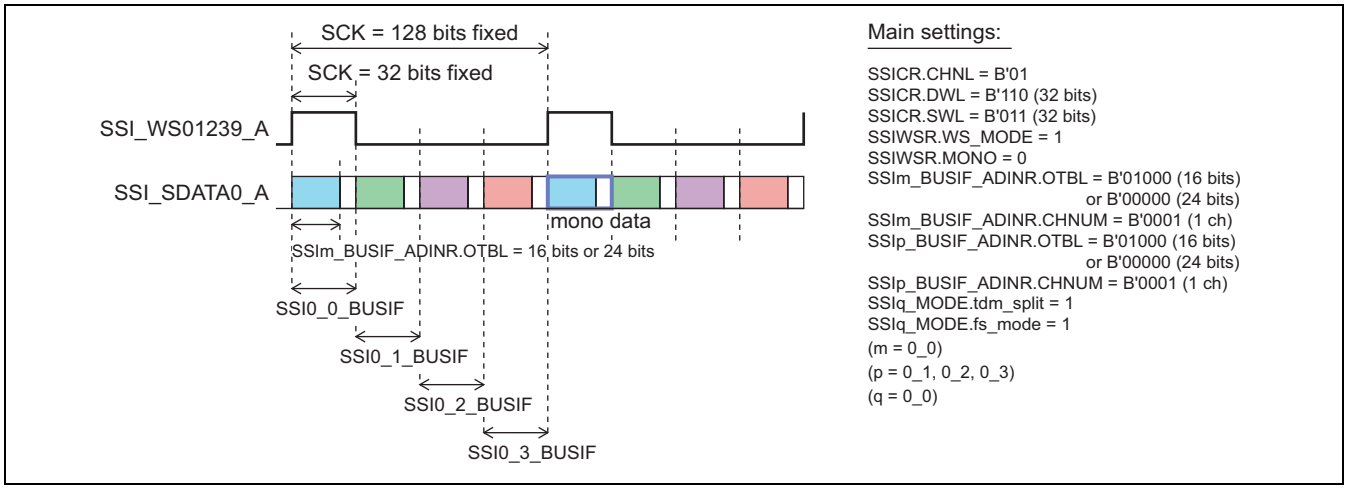


Figure 28.11 TDM Split Mode (Monaural × 4)

Notes: 1. The SWL and DWL bits in SSICR should be fixed at 32-bit setting.
2. Transmission and reception cannot coexist.
3. Data input to BUSIFn 0 to 3 (n = 0, 1, 2, 9) should be operated synchronously with the SSI sampling frequency (WS signal cycle).

28.3.6 SSI Pin Connections

Multiple SSI modules (in combinations of SSI0, SSI1, SSI2, SSI3, and SSI9, SSI3, SSI4, and SSI9, and SSI7 and SSI8) can operate in synchronization with sharing of the same SSI_SCK and SSI_WS signals. Figures 28.12 to 28.17 show how to connect the pins for each combination of SSIs.

In the case of the combination of SSI0, SSI1, SSI2, SSI3, and SSI9, SSI0 as the master should start transfer first thus allowing output on SSI_WS01239_A and SSI_SCK01239_A, after which SSI1, SSI2, SSI3, and SSI9 as the slaves should be used. If the master-side transfer is stopped by setting the CONT bit in SSIWSR to 0, the slave-side SSI1, SSI2, SSI3, and SSI9 should be stopped because output through SSI_WS01239_A is not possible. This also applies to the master and slaves in the combination of SSI3, SSI4, and SSI9, and to the master and slave in the combination of SSI7 and SSI8. All of the multiple SSI modules have to belong to same group (Group A or Group B).

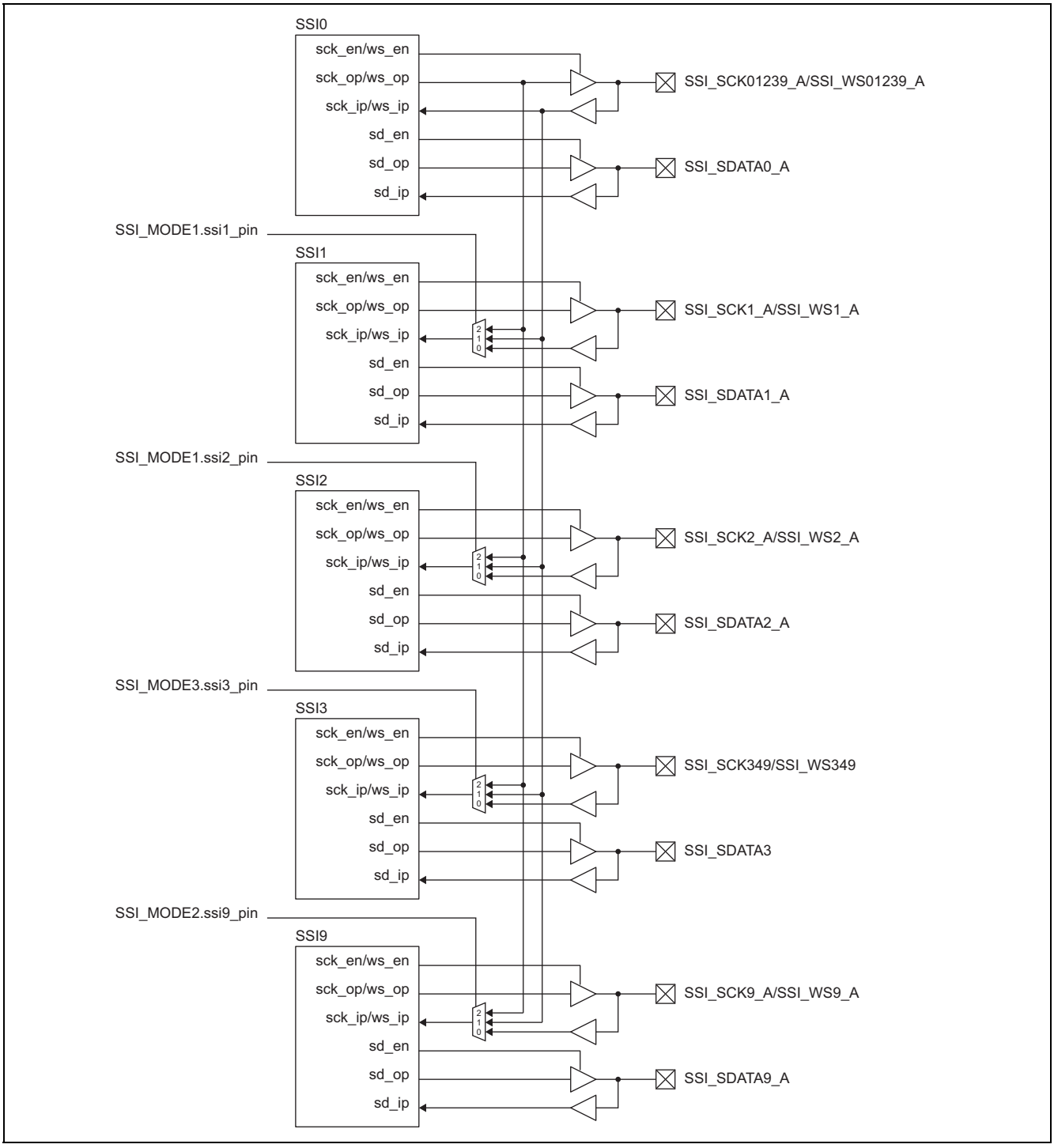


Figure 28.12 Pin Connections for Combination of SSI0, SSI1, SSI2, SSI3, and SSI9 (Group A)

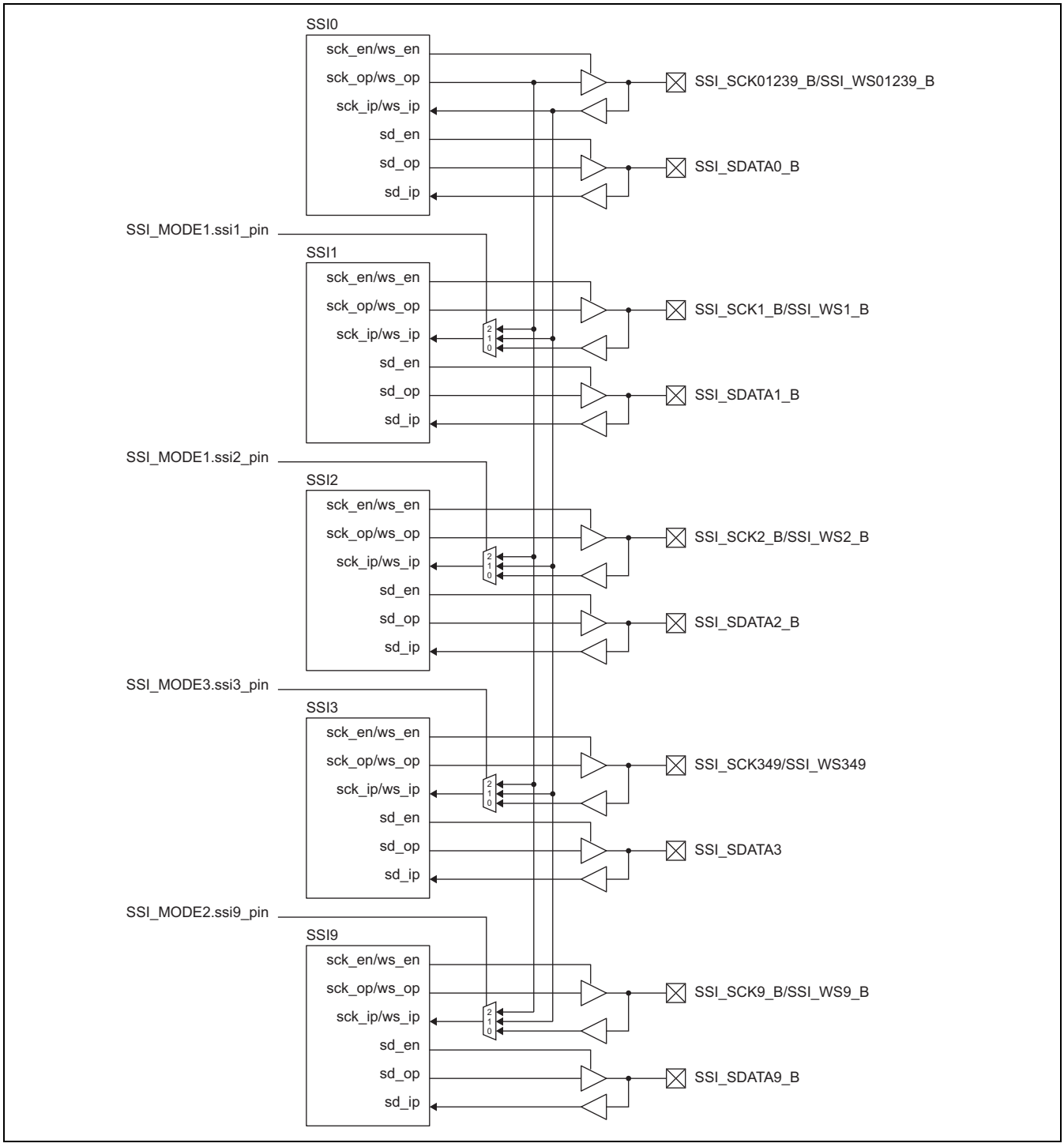


Figure 28.13 Pin Connections for Combination of SSI0, SSI1, SSI2, SSI3, and SSI9 (Group B)

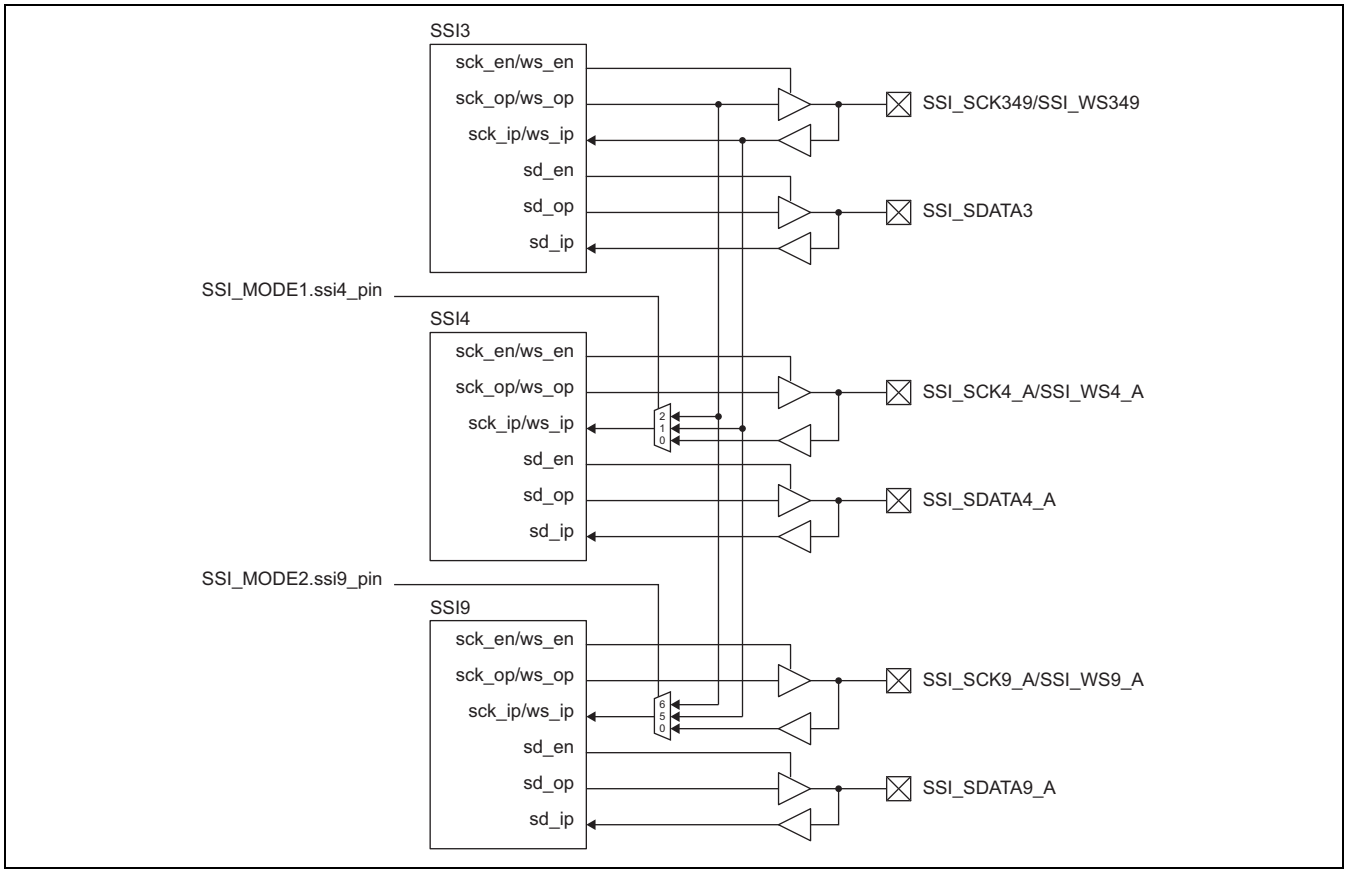


Figure 28.14 Pin Connections for Combination of SSI3, SSI4, and SSI9 (Group A)

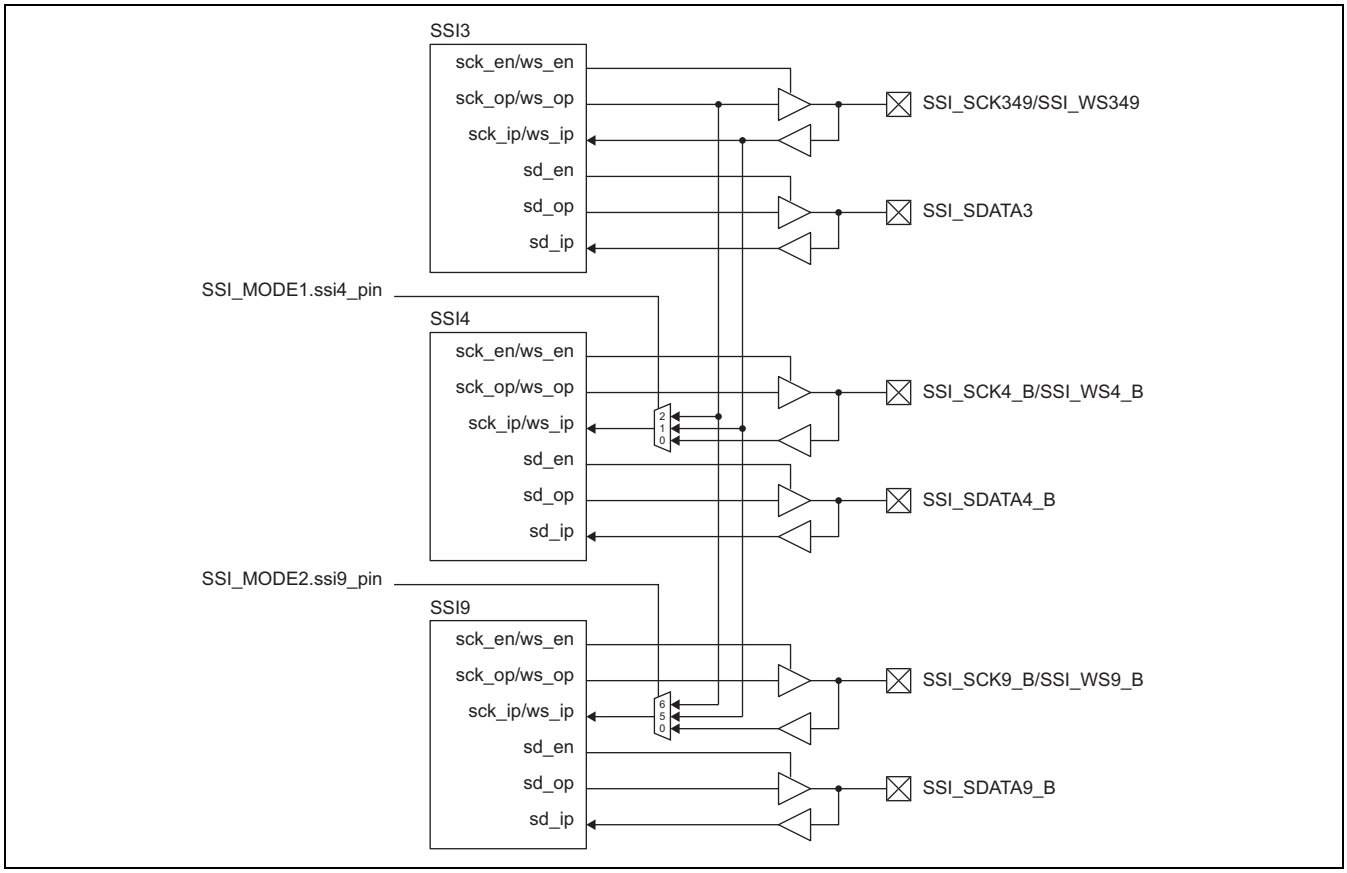


Figure 28.15 Pin Connections for Combination of SSI3, SSI4, and SSI9 (Group B)

Note: The above configuration in Figures 28.14 and 28.15 is prohibited if SSI0 SCK/WS is selected for SSI3 as shown in Figures 28.12 and 28.13.

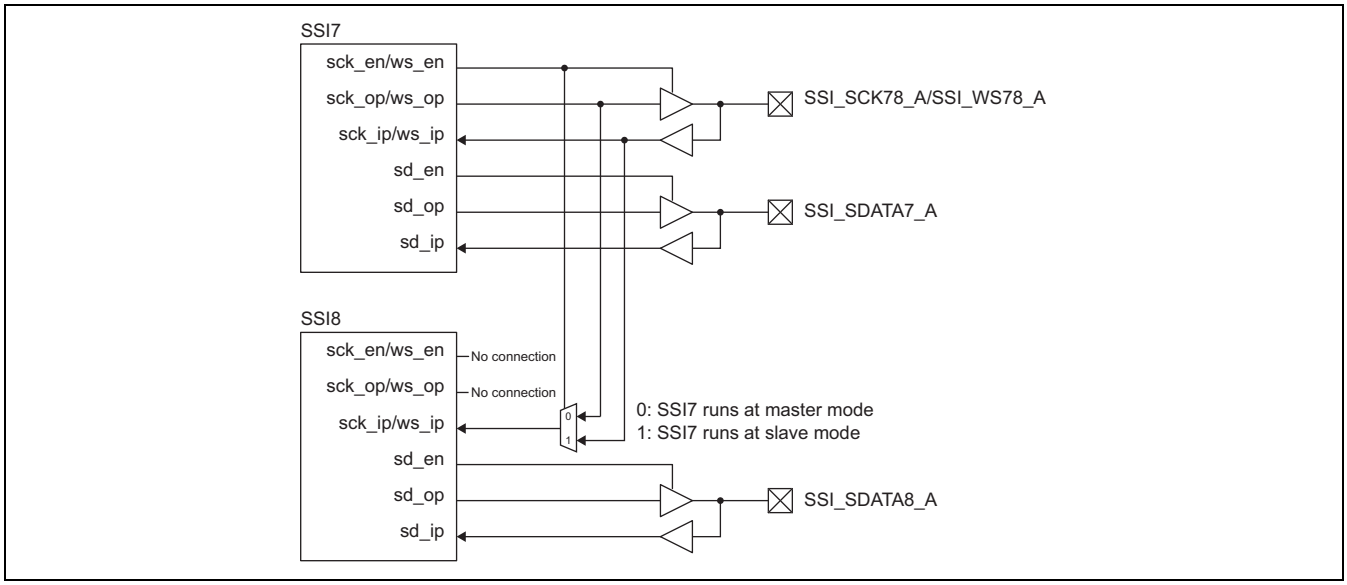


Figure 28.16 Pin Connections for Combination of SSI7 and SSI8 (Group A)

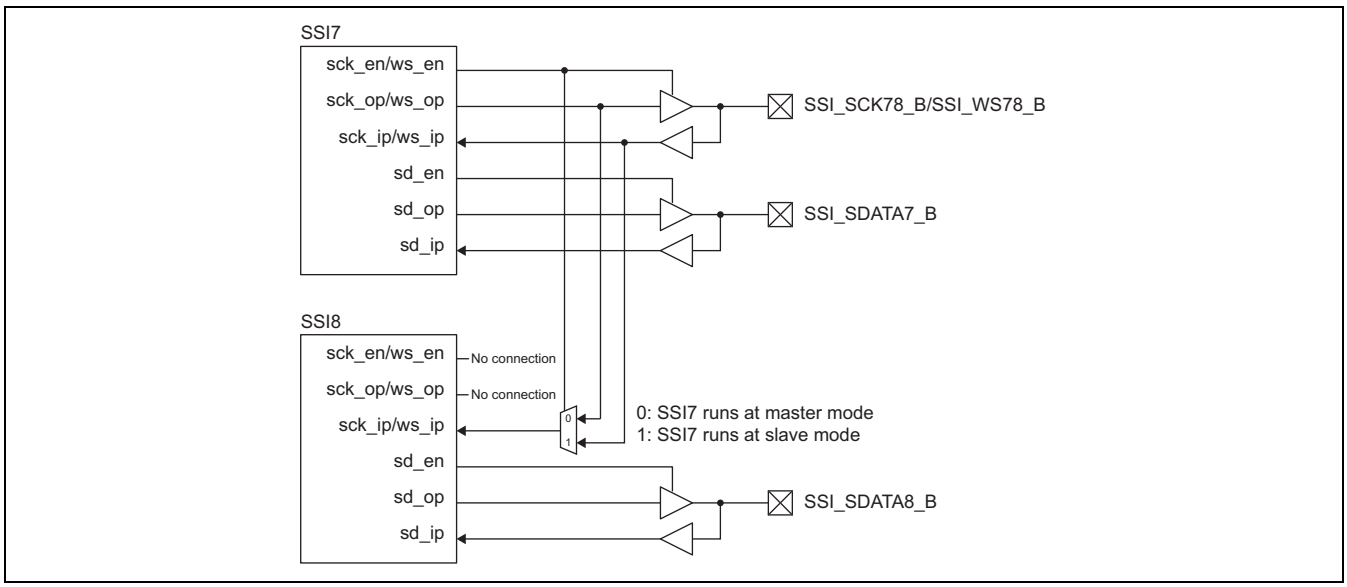


Figure 28.17 Pin Connections for Combination of SSI7 and SSI8 (Group B)

28.3.7 Procedure of SSIU Transfer

Figures 28.18 to 28.21 show the operation flow.

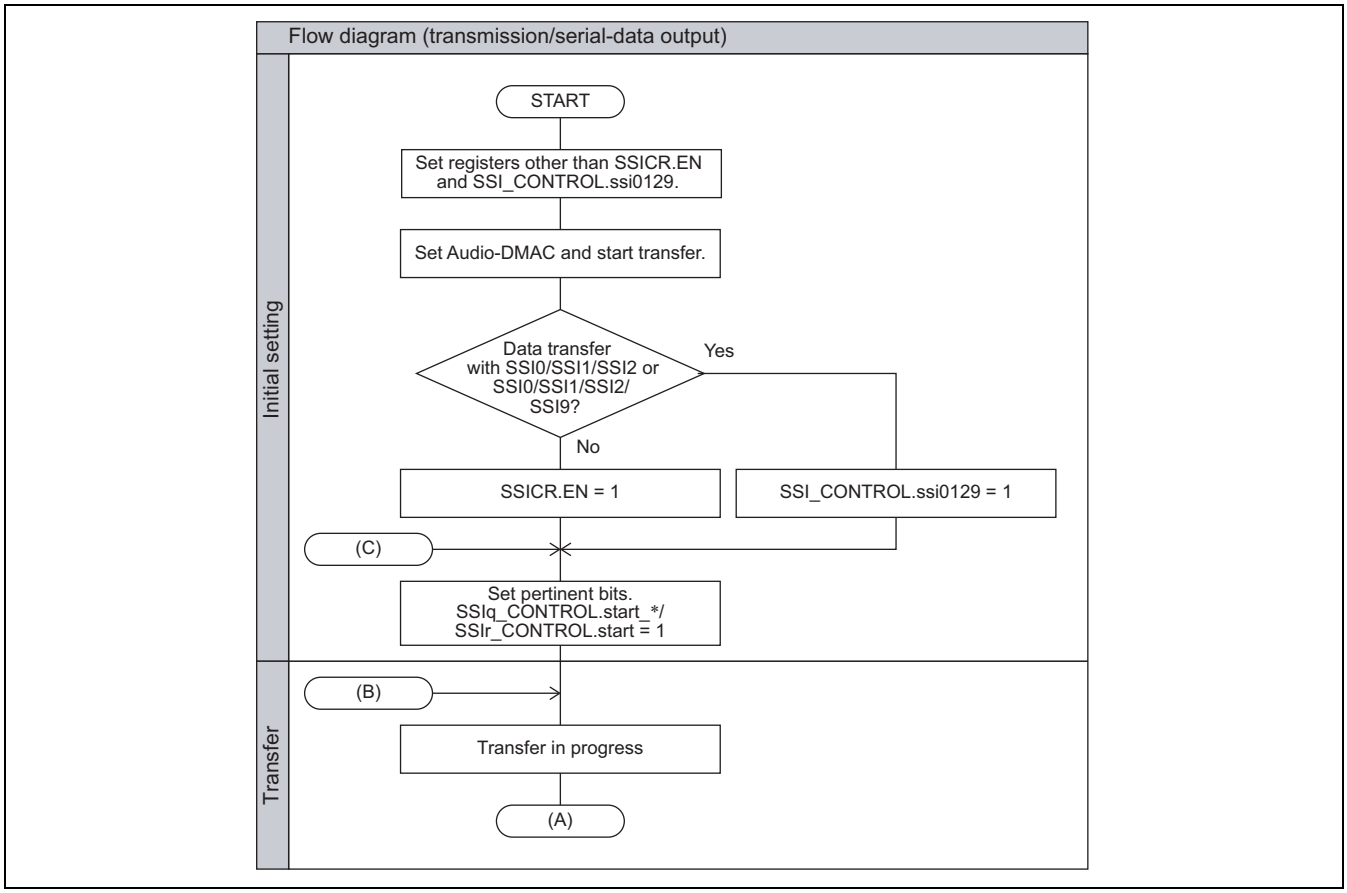


Figure 28.18 Transmission (1)

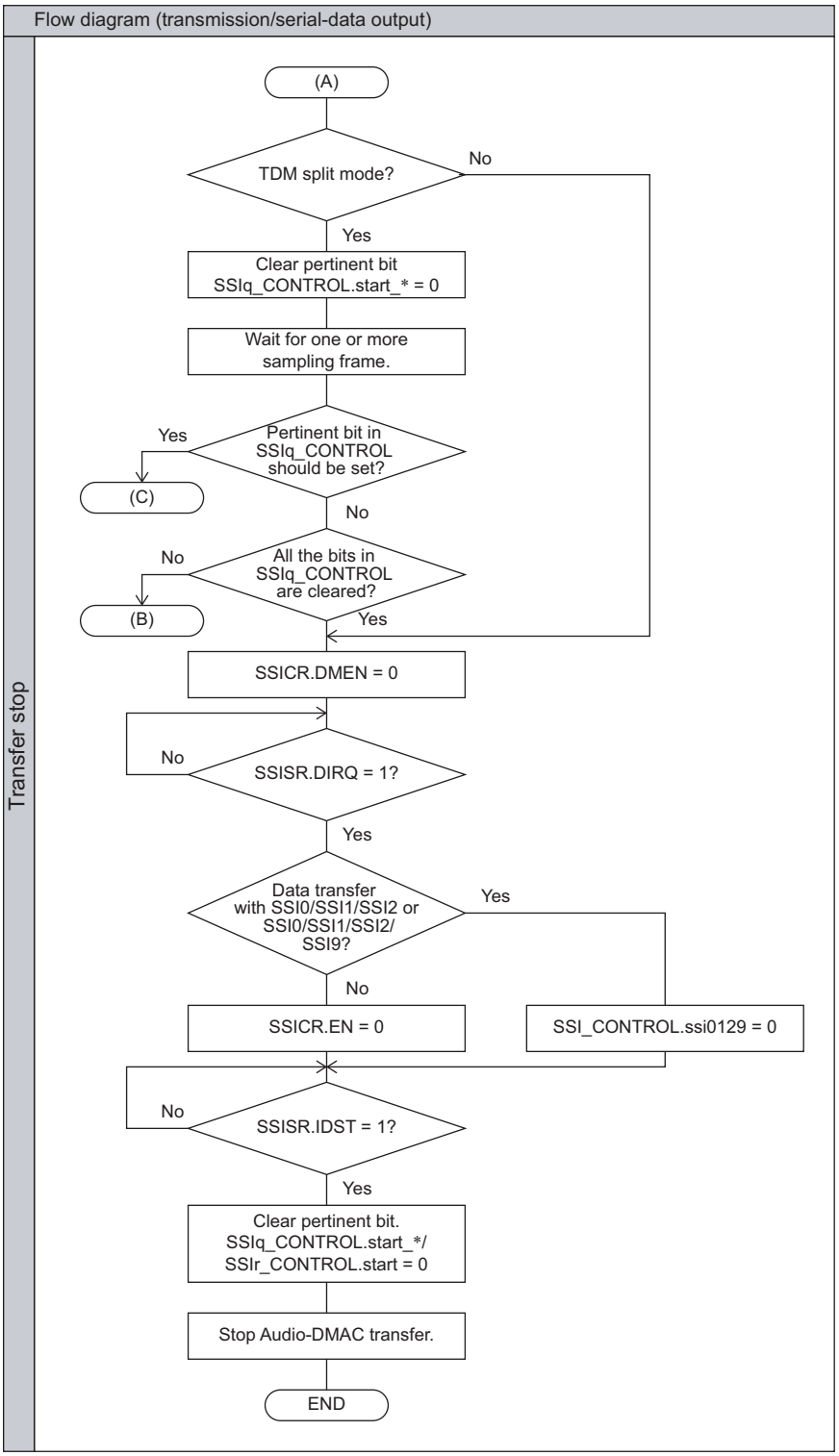


Figure 28.19 Transmission (2)

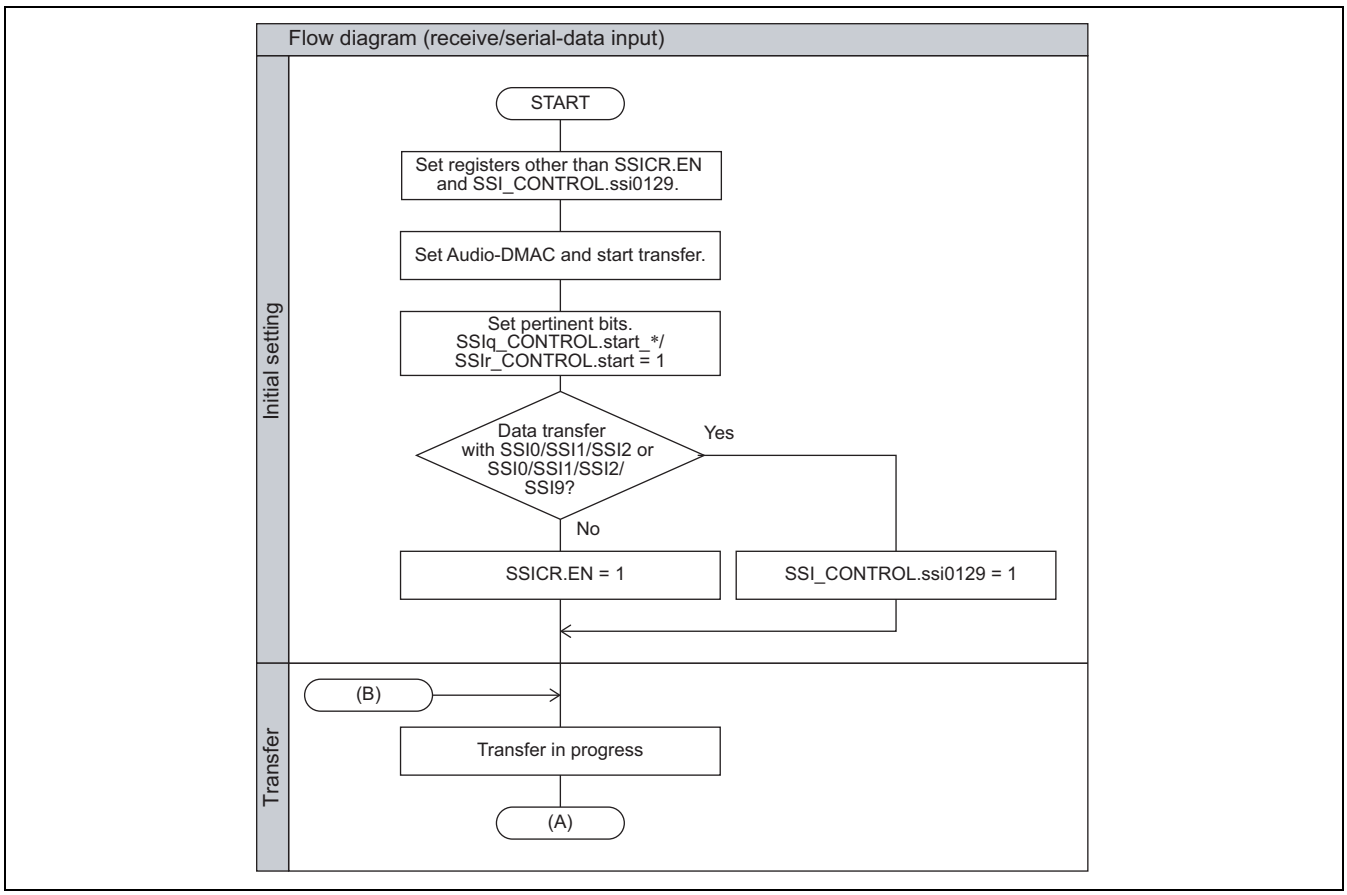


Figure 28.20 Reception (1)

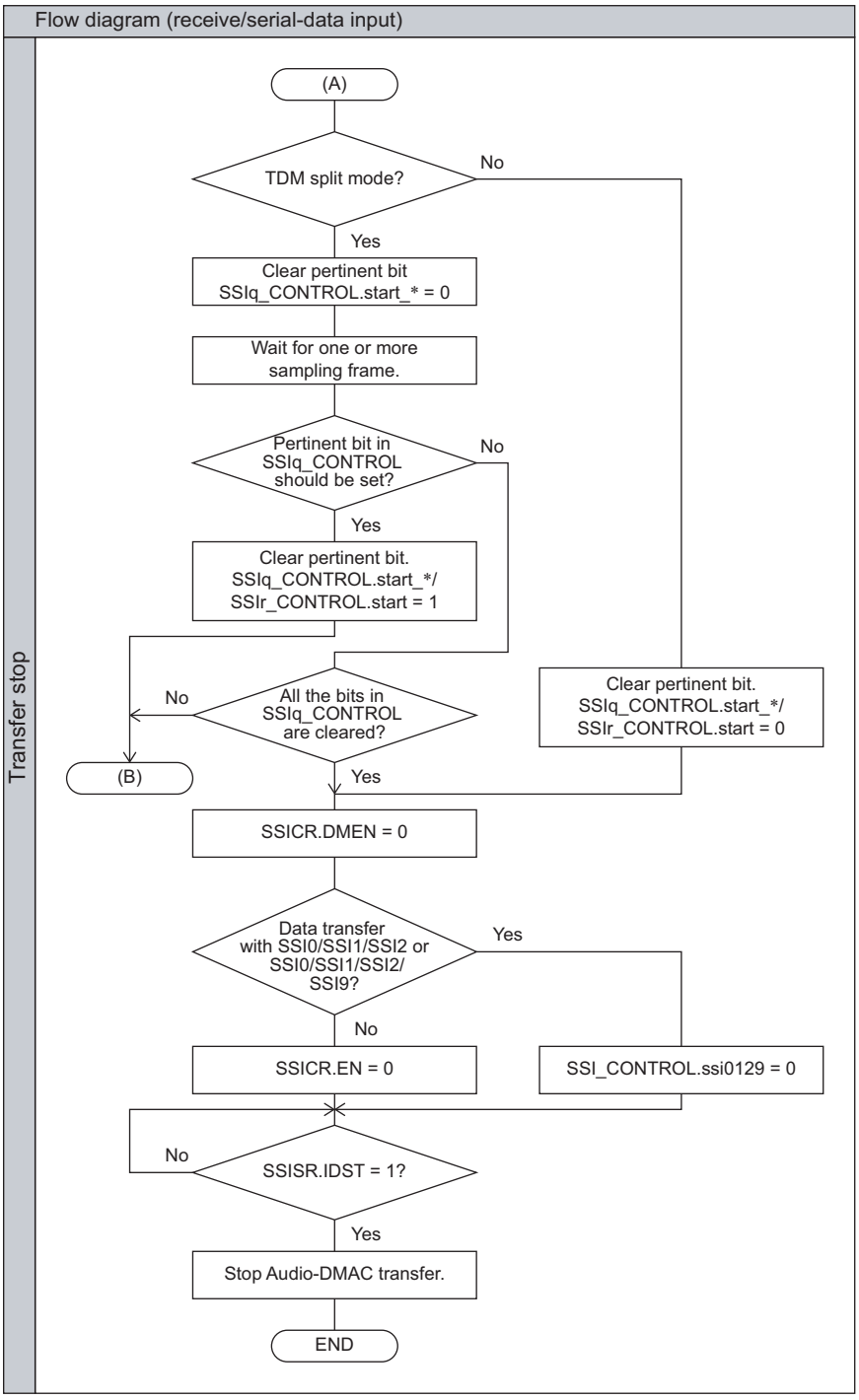


Figure 28.21 Reception (2)

28.3.8 Interrupts of SSI Setting

SSI can output interrupt signals when one of several events happen. Figure 28.22 illustrates how SSI generates interrupt signals and Table 28.4 and Table 28.5 indicate combinations of relevant registers for each SSI to generate interrupt signals (refer to explanations of relevant registers (Section 28.2) and SSI (Section 28A))

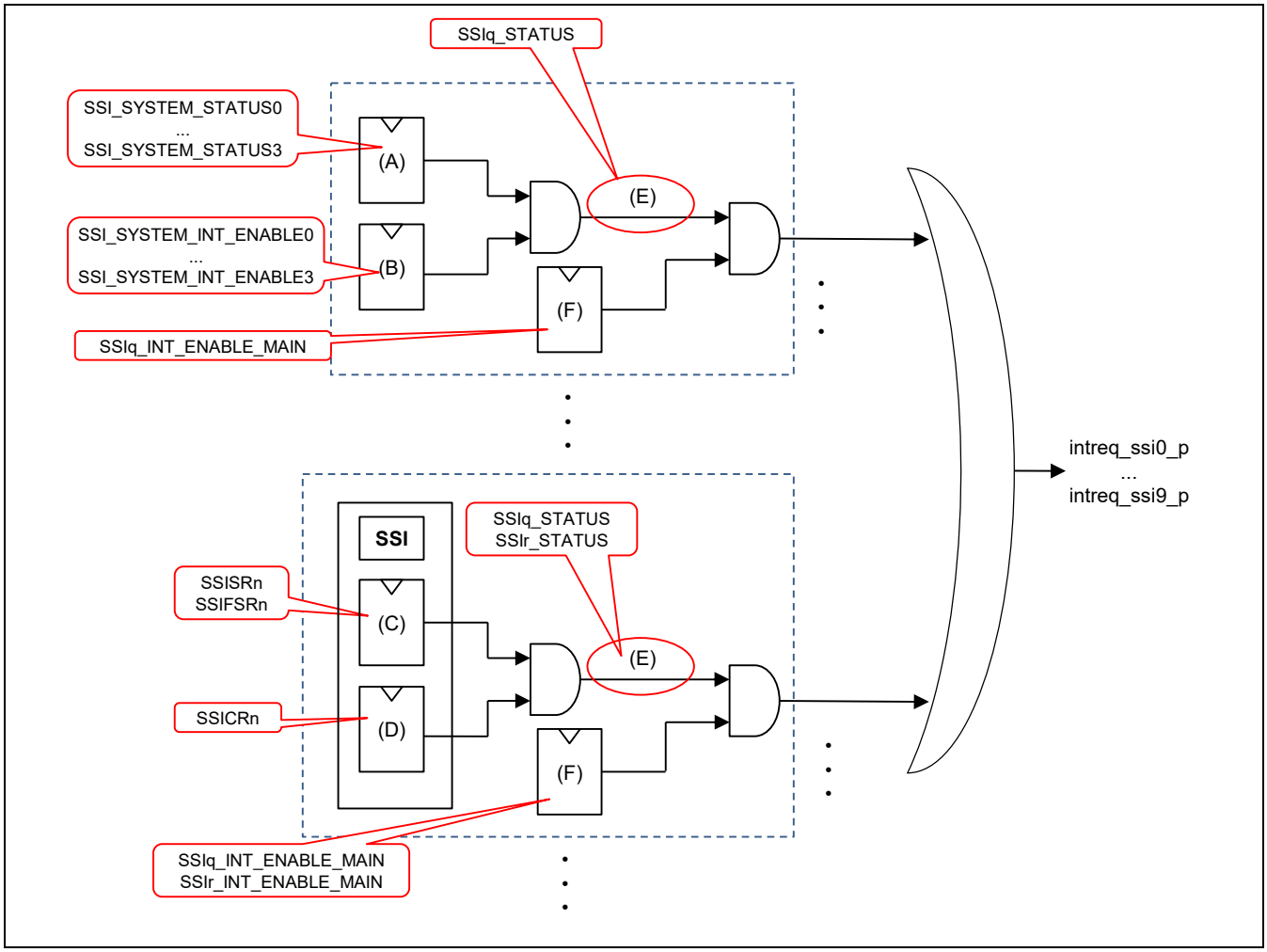


Figure 28.22 Mechanism of generating interrupt signals

Table 28.4 Combinations of relevant registers for each SSI (1)

		(A)	(B)	(E)	(F)
SSI	**BUSIF**	**Register Name (Interrupt Factor)**	**Register Name (Interrupt Enable)**	**Register Name (Interrupt Factor)**	**Register Name (Interrupt Enable)**
SSI0	BUSIF0-0 … BUSIF0-3	SSI_SYSTEM_STATUS0	SSI_SYSTEM_INT_ENABLE0	SSI0-0_STATUS	SSI0-0_INT_ENABLE_MAIN
		SSI_SYSTEM_STATUS2	SSI_SYSTEM_INT_ENABLE2	SSI0-0_STATUS	SSI0-0_INT_ENABLE_MAIN
SSI1	BUSIF1-0 … BUSIF1-3	SSI_SYSTEM_STATUS0	SSI_SYSTEM_INT_ENABLE0	SSI1-0_STATUS	SSI1-0_INT_ENABLE_MAIN
		SSI_SYSTEM_STATUS2	SSI_SYSTEM_INT_ENABLE2	SSI1-0_STATUS	SSI1-0_INT_ENABLE_MAIN
SSI2	BUSIF2-0 … BUSIF2-3	SSI_SYSTEM_STATUS0	SSI_SYSTEM_INT_ENABLE0	SSI2-0_STATUS	SSI2-0_INT_ENABLE_MAIN
		SSI_SYSTEM_STATUS2	SSI_SYSTEM_INT_ENABLE2	SSI2-0_STATUS	SSI2-0_INT_ENABLE_MAIN
SSI9	BUSIF9-0 … BUSIF9-3	SSI_SYSTEM_STATUS1	SSI_SYSTEM_INT_ENABLE1	SSI9-0_STATUS	SSI9-0_INT_ENABLE_MAIN
		SSI_SYSTEM_STATUS3	SSI_SYSTEM_INT_ENABLE3	SSI9-0_STATUS	SSI9-0_INT_ENABLE_MAIN

Table 28.5 Combinations of relevant registers for each SSI (2)

	(C)	(D)	(E)	(F)
SSI	**Register Name (Interrupt Factor)**	**Register Name (Interrupt Enable)**	**Register Name (Interrupt Factor)**	**Register Name (Interrupt Enable)**
SSI0	SSISR0	SSICR0	SSI0-0_STATUS	SSI0-0_INT_ENABLE_MAIN
	SSIFSR0	SSICR0	SSI0-0_STATUS	SSI0-0_INT_ENABLE_MAIN
SSI1	SSISR1	SSICR1	SSI1-0_STATUS	SSI1-0_INT_ENABLE_MAIN
	SSIFSR1	SSICR1	SSI1-0_STATUS	SSI1-0_INT_ENABLE_MAIN
SSI2	SSISR2	SSICR2	SSI2-0_STATUS	SSI2-0_INT_ENABLE_MAIN
	SSIFSR2	SSICR2	SSI2-0_STATUS	SSI2-0_INT_ENABLE_MAIN
SSI3	SSISR3	SSICR3	SSI3_STATUS	SSI3_INT_ENABLE_MAIN
	SSIFSR3	SSICR3	SSI3_STATUS	SSI3_INT_ENABLE_MAIN
SSI4	SSISR4	SSICR4	SSI4_STATUS	SSI4_INT_ENABLE_MAIN
	SSIFSR4	SSICR4	SSI4_STATUS	SSI4_INT_ENABLE_MAIN
SSI5	SSISR5	SSICR5	SSI5_STATUS	SSI5_INT_ENABLE_MAIN
	SSIFSR5	SSICR5	SSI5_STATUS	SSI5_INT_ENABLE_MAIN
SSI6	SSISR6	SSICR6	SSI6_STATUS	SSI6_INT_ENABLE_MAIN
	SSIFSR6	SSICR6	SSI6_STATUS	SSI6_INT_ENABLE_MAIN
SSI7	SSISR7	SSICR7	SSI7_STATUS	SSI7_INT_ENABLE_MAIN
	SSIFSR7	SSICR7	SSI7_STATUS	SSI7_INT_ENABLE_MAIN
SSI8	SSISR8	SSICR8	SSI8_STATUS	SSI8_INT_ENABLE_MAIN
	SSIFSR8	SSICR8	SSI8_STATUS	SSI8_INT_ENABLE_MAIN
SSI9	SSISR9	SSICR9	SSI9-0_STATUS	SSI9-0_INT_ENABLE_MAIN
	SSIFSR9	SSICR9	SSI9-0_STATUS	SSI9-0_INT_ENABLE_MAIN

28.4 Usage Note

28.4.1 Note on Transfer

If an underflow or overflow occurs, stop the transfer and restart it.

Do not stop serial clock (SCK) and word select (WS) signals during data transfer. Confirm that SSISR.IDST = 1 before stopping SCK and WS signals.

28A. Serial Sound Interface (SSI)

28A.1 Overview

The serial sound interface (hereinafter referred to as the "SSI") is a transceiver module designed to send or receive audio data interfacing with a variety of devices offering I2S format. It also supports multi-channel mode in addition to other common formats.

28A.1.1 Features

The SSI has the following features:

- Number of channels: Maximum of four (when a multichannel format is specified)
- The SSI module can serve as both a transmitter and a receiver.
- Asynchronous transfer takes place between the data buffer and the shift register.
- Only the MSB first data alignment is supported.
- A value as the dividing ratio for the clock used by the serial bus interface is selectable.
- Controlling of data transmission or reception with DMAC or interrupt requests is possible.
- TDM format is supported.
- The frequency range of SCK signal is from 297.3 kHz to 12.5MHz at master mode, and from 297.3 kHz to 15.1 MHz at slave mode.
- The WS continue function by which operation can be performed without stopping WS signal is supported.
- Monaural mode (8 bits or 16 bits) is supported.
- In monaural mode, WS signal pulse width can be changed (short or long frame).
- If the sampling clock frequency is switched during transfer, it will be notified of the CPU with interrupts (a function to detect switching frequency).

28A.1.2 Block Diagram

Figure 28A.1 shows a block diagram of a single SSI module.

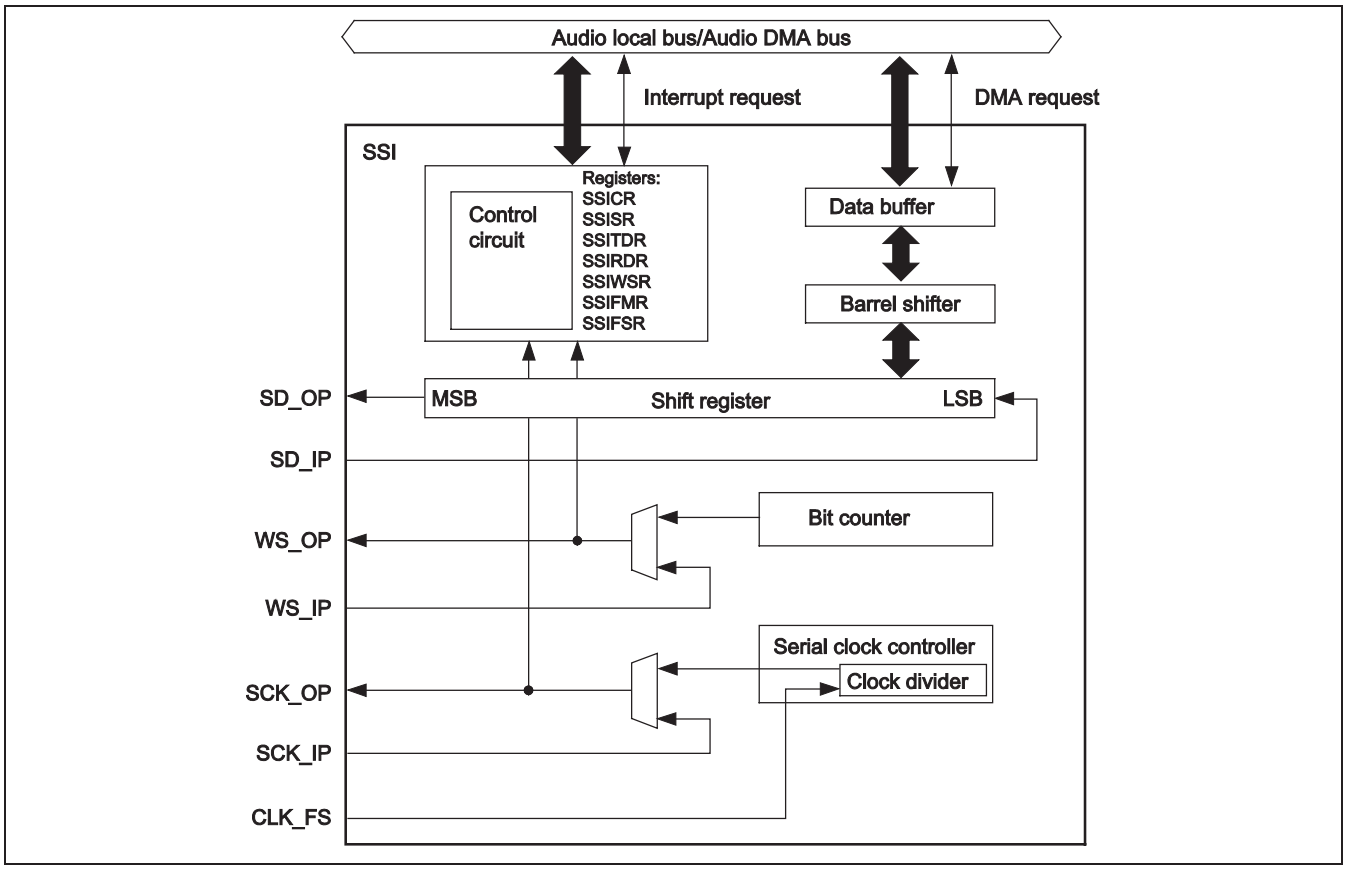


Figure 28A.1 Block Diagram of SSI

28A.1.3 Input/Output Pins

No external pins

28A.1.4 Register Configuration

The SSI has the following registers. Note that the module numbers are basically omitted from the register names in the text.

Table 28A.1 Register Configurations

Module	Register Name	Abbreviation	R/W	Address	Access Size
0	Control Register 0	SSICR0	R/W	H'EC54 1000	32
	Status Register 0	SSISR0	R/W*1	H'EC54 1004	32
	Transmit Data Register 0	SSITDR0	R/W	H'EC54 1008/ H'EC24 1008*3	32
	Receive Data Register 0	SSIRDR0	R	H'EC54 100C/ H'EC24 100C*3	32
	WS Mode Register 0	SSIWSR0	R/W	H'EC54 1020	32
	FS Mode Register 0	SSIFMR0	R/W	H'EC54 1024	32
	FS Status Register 0	SSIFSR0	R/W*2	H'EC54 1028	32
1	Control Register 1	SSICR1	R/W	H'EC54 1040	32
	Status Register 1	SSISR1	R/W*1	H'EC54 1044	32
	Transmit Data Register 1	SSITDR1	R/W	H'EC54 1048/ H'EC24 1048*3	32
	Receive Data Register 1	SSIRDR1	R	H'EC54 104C/ H'EC24 104C*3	32
	WS Mode Register 1	SSIWSR1	R/W	H'EC54 1060	32
	FS Mode Register 1	SSIFMR1	R/W	H'EC54 1064	32
	FS Status Register 1	SSIFSR1	R/W*2	H'EC54 1068	32
2	Control Register 2	SSICR2	R/W	H'EC54 1080	32
	Status Register 2	SSISR2	R/W*1	H'EC54 1084	32
	Transmit Data Register 2	SSITDR2	R/W	H'EC54 1088/ H'EC24 1088*3	32
	Receive Data Register 2	SSIRDR2	R	H'EC54 108C/ H'EC24 108C*3	32
	WS Mode Register 2	SSIWSR2	R/W	H'EC54 10A0	32
	FS Mode Register 2	SSIFMR2	R/W	H'EC54 10A4	32
	FS Status Register 2	SSIFSR2	R/W*2	H'EC54 10A8	32
3	Control Register 3	SSICR3	R/W	H'EC54 10C0	32
	Status Register 3	SSISR3	R/W*1	H'EC54 10C4	32
	Transmit Data Register 3	SSITDR3	R/W	H'EC54 10C8/ H'EC24 10C8*3	32
	Receive Data Register 3	SSIRDR3	R	H'EC54 10CC/ H'EC24 10CC*3	32
	WS Mode Register 3	SSIWSR3	R/W	H'EC54 10E0	32
	FS Mode Register 3	SSIFMR3	R/W	H'EC54 10E4	32
	FS Status Register 3	SSIFSR3	R/W*2	H'EC54 10E8	32

Module	Register Name	Abbreviation	R/W	Address	Access Size
4	Control Register 4	SSICR4	R/W	H'EC54 1100	32
	Status Register 4	SSISR4	R/W*1	H'EC54 1104	32
	Transmit Data Register 4	SSITDR4	R/W	H'EC54 1108/ H'EC24 1108*3	32
	Receive Data Register 4	SSIRDR4	R	H'EC54 110C/ H'EC24 110C*3	32
	WS Mode Register 4	SSIWSR4	R/W	H'EC54 1120	32
	FS Mode Register 4	SSIFMR4	R/W	H'EC54 1124	32
	FS Status Register 4	SSIFSR4	R/W*2	H'EC54 1128	32
5	Control Register 5	SSICR5	R/W	H'EC54 1140	32
	Status Register 5	SSISR5	R/W*1	H'EC54 1144	32
	Transmit Data Register 5	SSITDR5	R/W	H'EC54 1148/ H'EC24 1148*3	32
	Receive Data Register 5	SSIRDR5	R	H'EC54 114C/ H'EC24 114C*3	32
	WS Mode Register 5	SSIWSR5	R/W	H'EC54 1160	32
	FS Mode Register 5	SSIFMR5	R/W	H'EC54 1164	32
	FS Status Register 5	SSIFSR5	R/W*2	H'EC54 1168	32
6	Control Register 6	SSICR6	R/W	H'EC54 1180	32
	Status Register 6	SSISR6	R/W*1	H'EC54 1184	32
	Transmit Data Register 6	SSITDR6	R/W	H'EC54 1188/ H'EC24 1188*3	32
	Receive Data Register 6	SSIRDR6	R	H'EC54 118C/ H'EC24 118C*3	32
	WS Mode Register 6	SSIWSR6	R/W	H'EC54 11A0	32
	FS Mode Register 6	SSIFMR6	R/W	H'EC54 11A4	32
	FS Status Register 6	SSIFSR6	R/W*2	H'EC54 11A8	32
7	Control Register 7	SSICR7	R/W	H'EC54 11C0	32
	Status Register 7	SSISR7	R/W*1	H'EC54 11C4	32
	Transmit Data Register 7	SSITDR7	R/W	H'EC54 11C8/ H'EC24 11C8*3	32
	Receive Data Register 7	SSIRDR7	R	H'EC54 11CC/ H'EC24 11CC*3	32
	WS Mode Register 7	SSIWSR7	R/W	H'EC54 11E0	32
	FS Mode Register 7	SSIFMR7	R/W	H'EC54 11E4	32
	FS Status Register 7	SSIFSR7	R/W*2	H'EC54 11E8	32
8	Control Register 8	SSICR8	R/W	H'EC54 1200	32
	Status Register 8	SSISR8	R/W*1	H'EC54 1204	32
	Transmit Data Register 8	SSITDR8	R/W	H'EC54 1208/ H'EC24 1208*3	32
	Receive Data Register 8	SSIRDR8	R	H'EC54 120C/ H'EC24 120C*3	32
	WS Mode Register 8	SSIWSR8	R/W	H'EC54 1220	32
	FS Mode Register 8	SSIFMR8	R/W	H'EC54 1224	32
	FS Status Register 8	SSIFSR8	R/W*2	H'EC54 1228	32
9	Control Register 9	SSICR9	R/W	H'EC54 1240	32
	Status Register 9	SSISR9	R/W*1	H'EC54 1244	32
	Transmit Data Register 9	SSITDR9	R/W	H'EC54 1248/ H'EC24 1248*3	32
	Receive Data Register 9	SSIRDR9	R	H'EC54 124C/ H'EC24 124C*3	32
	WS Mode Register 9	SSIWSR9	R/W	H'EC54 1260	32
	FS Mode Register 9	SSIFMR9	R/W	H'EC54 1264	32
	FS Status Register 9	SSIFSR9	R/W*2	H'EC54 1268	32

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted.
Values read from addresses other than those listed above are undefined.

1. For this register, bits 26 and 27 are readable/writable bits, although the others are read-only bits. For details, refer to section 28A.2.2 Status Register (SSISRn) (n = 0 to 9).
2. For this register, bits 14 and 15 are readable/writable bits, although the others are read-only bits. For details, refer to section 28A.2.7 FS Status Register (SSIFSRn) (n = 0 to 9).
3. H'EC54 1XXX and H'EC24 1XXX are used with PIO access and Audio-DMAC, respectively.

28A.2 Register Description

[Legend for Register Descriptions]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R: Read-only. The write value should always be 0.

28A.2.1 Control Register (SSICRn) (n = 0 to 9)

SSICR is a readable/writable 32-bit register that controls the IRQ, selects the polarity status, and sets operating mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FORCE	—	FIEN	DMEN	UIEN	OIEN	IIEN	DIEN	CHNL[1:0]		DWL[2:0]			SWL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCKD	SWSD	SCKP	SWSP	SPDP	SDTA	PDTA	DEL	—	CKDV[2:0]			MUEN	—	TRMD	EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	FORCE	0	R/W	Fixed The bit should always be set to 1.
30	—	0	R	Reserved The read value is 0. The write value should always be 0.
29	FIEN	0	R/W	Frequency Switching Detection Interrupt Enable 0: Frequency switching detection interrupt is disabled. 1: Frequency switching detection interrupt is enabled.
28	DMEN	0	R/W	DMA Enable Enables or disables the DMA request. 0: DMA request is disabled. 1: DMA request is enabled.
27	UIEN	0	R/W	Underflow Interrupt Enable 0: Underflow interrupt is disabled. 1: Underflow Interrupt is enabled.
26	OIEN	0	R/W	Overflow Interrupt Enable 0: Overflow interrupt is disabled. 1: Overflow interrupt is enabled.
25	IIEN	0	R/W	Idle Mode Interrupt Enable 0: Idle mode interrupt is disabled. 1: Idle mode interrupt is enabled.

Bit	Bit Name	Initial Value	R/W	Description
24	DIEN	0	R/W	Data Interrupt Enable 0: Data interrupt is disabled. 1: Data interrupt is enabled.
23, 22	CHNL[1:0]	00	R/W	Channels These bits set the number of channels in each system word. When the stereo format or multi-channel format is used (WS_MODE = 0, MONO = 0, and WIDTH = B'00000 in the WS Mode Register): 00: A system word has one channel. 01: A system word has two channels. 10: A system word has three channels. 11: A system word has four channels. When the TDM format is used (WS_MODE = 1, MONO = 0, and WIDTH = B'00000 in the WS Mode Register): 00: Setting prohibited* 01: A TDM frame consists of four system words. 10: A TDM frame consists of six system words. 11: A TDM frame consists of eight system words. When the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS Mode Register): 00: A monaural frame consists of one system word. 01: Setting prohibited 10: Setting prohibited 11: Setting prohibited
21 to 19	DWL[2:0]	000	R/W	Data Word Length These bits set the number of bits in a data word. When the stereo format or multi-channel format (WS_MODE = 0, MONO = 0, and WIDTH = B'00000 in the WS Mode Register) or TDM format (WS_MODE = 1, MONO = 0, and WIDTH = B'00000 in the WS Mode Register) is used: 000: 8 bits 001: 16 bits 010: 18 bits 011: 20 bits 100: 22 bits 101: 24 bits 110: 32 bits 111: Setting prohibited When the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS Mode Register): 000: 8 bits 001: 16 bits Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
18 to 16	SWL[2:0]	000	R/W	System Word Length These bits set the number of bits in a system word. When the stereo format or multi-channel format (WS_MODE = 0, MONO = 0, and WIDTH = B'00000 in the WS Mode Register) or TDM format (WS_MODE = 1, MONO = 0, and WIDTH = B'00000 in the WS Mode Register) is used: 000: 8 bits 001: 16 bits 010: 24 bits 011: 32 bits 100: 48 bits 101: 64 bits 110: 128 bits 111: 256 bits When the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS Mode Register): 000: 16 bits 001: 32 bits 010: 48 bits 011: 64 bits 100: 96 bits 101: 128 bits 110: 256 bits 111: 512 bits
15	SCKD	0	R/W	Serial Bit Clock Direction 0: Serial bit clock is input, slave mode. 1: Serial bit clock is output, master mode. Note: (SCKD, SWSD) = (0, 0) or (1, 1) can be set to SSI0 to SSI7 and SSI9. To SSI8, only (SCKD, SWSD) = (0, 0) can be set. Other settings are prohibited.
14	SWSD	0	R/W	Serial WS Direction 0: Serial word select is input, slave mode. 1: Serial word select is output, master mode. Note: (SCKD, SWSD) = (0, 0) or (1, 1) can be set to SSI0 to SSI7 and SSI9. To SSI8, only (SCKD, SWSD) = (0, 0) can be set. Other settings are prohibited.

Bit	Bit Name	Initial Value	R/W	Description
13	SCKP	0	R/W	Serial Bit Clock Polarity 0: SSI_WS and SSI_SDATA change at the SSI_SCK falling edge (sampled at the SCK rising edge). 1: SSI_WS and SSI_SDATA change at the SSI_SCK rising edge (sampled at the SCK falling edge).

	SCKP = 0	SCKP = 1
SSI_SDATA input sampling timing at the time of reception (TRMD = 0)	SSI_SCK rising edge	SSI_SCK falling edge
SSI_SDATA output change timing at the time of transmission (TRMD = 1)	SSI_SCK falling edge	SSI_SCK rising edge
SSI_WS input sampling timing at the time of slave mode (SWSD = 0)	SSI_SCK rising edge	SSI_SCK falling edge
SSI_WS output change timing at the time of master mode (SWSD = 1)	SSI_SCK falling edge	SSI_SCK rising edge

Bit	Bit Name	Initial Value	R/W	Description
12	SWSP	0	R/W	Serial WS Polarity The value of this bit must not be changed when the SSI module enable (EN) bit in this register is set to 1. • When the stereo format or multi-channel format is used (WS_MODE = 0, MONO = 0, and WIDTH = B'00000 in the WS Mode Register): 0: SSI_WS is low for 1st channel, high for 2nd channel. 1: SSI_WS is high for 1st channel, low for 2nd channel. • When the TDM format is used (WS_MODE = 1, MONO = 0, and WIDTH = B'00000 in the WS Mode Register): 0: The SYNC pulse is high over the period of system word 1, and low otherwise. 1: The SYNC pulse is low for over the period of system word 1, and high otherwise. • When the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS Mode Register): 0: WS pulse is high over the period specified with the WIDTH bits in the WS Mode Register, and low otherwise. 1: WS pulse is low over the period specified with the WIDTH bits in the WS Mode Register, and high otherwise.
11	SPDP	0	R/W	Serial Padding Polarity 0: Padding bits are low. 1: Padding bits are high. Padding bits are low when MUEN = 1. (The mute function takes priority.)
10	SDTA	0	R/W	Serial Data Alignment This bit should be set to 0 when the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS Mode Register). 0: Transmitting and receiving in the order of serial data and padding bits. 1: Transmitting and receiving in the order of padding bits and serial data.

Bit	Bit Name	Initial Value	R/W	Description
9	PDTA	0	R/W	Parallel Data Alignment When the length of data word is 32, 16 or 8 bits, this configuration field has no meaning. This bit should be set to 0 when the monaural format is used (WS_MODE = 1, MONO = 1, and WIDTH = B'00001 to B'11111 in the WS Mode Register). This bit applies to SSIRDR in receive mode and SSITDR in transmit mode. 0: Parallel data (SSITDR, SSIRDR) is left-aligned. 1: Parallel data (SSITDR, SSIRDR) is right-aligned. DWL = 000 (with a data word length of 8 bits), the PDTA setting is ignored. All data bits in SSIRDR or SSITDR are used on the audio serial bus. Four data words are transmitted or received at each 32-bit access. The first data word is derived from bits 7 to 0, the second from bits 15 to 8, the third from bits 23 to 16 and the last data word is derived from bits 31 to 24. DWL = 001 (with a data word length of 16 bits), the PDTA setting is ignored. All data bits in SSIRDR or SSITDR are used on the audio serial bus. Two data words are transmitted or received at each 32-bit access. The first data word is derived from bits 15 to 0 and the second data word is derived from bits 31 to 16. DWL = 010, 011, 100, 101 (with a data word length of 18, 20, 22 or 24 bits), PDTA = 0 (left-aligned) The data bits used in SSIRDR or SSITDR are the following: Bits 31 down to (32 minus the number of bits in the data word length specified by DWL). That is, if DWL = 011, the data word length is 20 bits; therefore, bits 31 to 12 in either SSIRDR or SSITDR are used. All other bits are ignored or reserved. DWL = 010, 011, 100, 101 (with a data word length of 18, 20, 22 or 24 bits), PDTA = 1 (right-aligned) The data bits used in SSIRDR or SSITDR are the following: Bits (the number of bits in the data word length specified by DWL minus 1) to 0 i.e. if DWL = 011, then DWL = 20 and bits 19 to 0 are used in either SSIRDR or SSITDR. All other bits are ignored or reserved. DWL = 110 (with a data word length of 32 bits), the PDTA setting is ignored. All data bits in SSIRDR or SSITDR are used on the audio serial bus.
8	DEL	0	R/W	Serial Data Delay 0: One clock cycle delay between SSI_WS and SSI_SDATA 1: No delay between SSI_WS and SSI_SDATA
7	—	0	R	Reserved The read value is 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	CKDV[2:0]	000	R/W	Serial Oversampling Clock Division Ratio Set the ratio between oversampling clock, CLK_FS, and the serial bit clock. These bits are ignored if SCKD = 0. The serial bit clock is used in the shift register and is provided on the SSI_SCK module pin. 000: Serial bit clock frequency = oversampling clock frequency/1 001: Serial bit clock frequency = oversampling clock frequency/2 010: Serial bit clock frequency = oversampling clock frequency/4 011: Serial bit clock frequency = oversampling clock frequency/8 100: Serial bit clock frequency = oversampling clock frequency/16 101: Serial bit clock frequency = oversampling clock frequency/6 110: Serial bit clock frequency = oversampling clock frequency/12 111: Setting prohibited CKDV = 000 is invalid when WS_MODE = 1 or CONT = 1 in the WS Mode Register.
3	MUEN	0	R/W	Serial Data Output Disable 0: Module is not muted. 1: Module is muted. Note: This bit can be used to stop output (low output) or to enable output. However, the operation is not synchronized with the change of SSI_WS.
2	—	0	R	Reserved The read value is 0. The write value should always be 0.
1	TRMD	0	R/W	Transmit/Receive Mode Select 0: Module is in receive mode. 1: Module is in transmit mode.
0	EN	0	R/W	SSI Module Enable 0: Module is disabled. 1: Module is enabled.

28A.2.2 Status Register (SSISRn) (n = 0 to 9)

SSISR consists of status flags indicating the operational status of the SSI module and bits indicating the current channel numbers and word numbers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	DMRQ	UIRQ	OIRQ	IIRQ	DIRQ	—	—	—	—	—	—	—	—
Initial value:	—	—	—	0	0	0	—	0	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R/WC0	R/WC0	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNO[1:0]		SWNO	IDST
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	0	0	1	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	Undefined	R	Reserved The read value is not guaranteed. The write value should always be 0.
28	DMRQ	0	R	DMA Request Status Flag This status flag allows the CPU to recognize the value of the DMA request pin on the SSI module. • TRMD = 0 (receive mode) If DMRQ = 1, the SSIRDR has unread data. If SSIRDR is read, DMRQ = 0 until there is new unread data. • TRMD = 1 (transmit mode) If DMRQ = 1, SSITDR requires data to be written to continue the transmission to the audio serial bus. Once data is written to SSITDR, DMRQ = 0 until it requires further transmit data.
27	UIRQ	0	R/WC0	Underflow Error Interrupt Status Flag This status flag indicates that data was supplied at a lower rate than was required. In either case, this bit is set to 1 regardless of the value of the UIEN bit and can be cleared by writing 0 to this bit. If UIRQ = 1 and UIEN = 1, an interrupt occurs. • TRMD = 0 (receive mode) If UIRQ = 1, SSIRDR was read before there was new unread data indicated by the DMRQ or DIRQ bit. This can lead to the same received data being stored twice by the host leading to potential corruption of multi-channel data. • TRMD = 1 (transmit mode) If UIRQ = 1, SSITDR did not have data written to it before it was required for transmission. This will lead to the same data being transmitted once more and a potential corruption of multi-channel data. This is more serious error than a receive mode underflow as the output SSI data results in error. Note: When underflow error occurs, the current data in the data buffer of this module is transmitted until the next data is filled.

Bit	Bit Name	Initial Value	R/W	Description
26	OIRQ	0	R/WC0	Overflow Error Interrupt Status Flag This status flag indicates that data was supplied at a higher rate than was required. In either case this bit is set to 1 regardless of the value of the OIEN bit and can be cleared by writing 0 to this bit. If OIRQ = 1 and OIEN = 1, an interrupt occurs. • TRMD = 0 (receive mode) If OIRQ = 1, SSIRDR was not read before there was new unread data written to it. This will lead to the loss of a data and a potential corruption of multi-channel data. Note: When overflow error occurs, the current data in the data buffer of this module is overwritten by the next incoming data from the SSI interface. • TRMD = 1 (transmit mode) If OIRQ = 1, SSITDR had data written to it before it was transferred to the shift register. This will lead to the loss of a data and a potential corruption of multi-channel data.
25	IIRQ	Undefined	R	Idle Mode Interrupt Status Flag This interrupt status flag indicates whether the SSI module is in idle state. This bit is set regardless of the value of the IIEN bit to allow polling. “Idle state” refers to the state where the serial bus has been stopped after activation of the SSI. The interrupt can be masked by clearing IIEN, but cannot be cleared by writing to this bit. If IIRQ = 1 and IIEN = 1, an interrupt occurs. 0: The SSI module is not in idle state. 1: The SSI module is in idle state.
24	DIRQ	0	R	Data Interrupt Status Flag This status flag indicates that the module has data to be read or requires data to be written. In either case this bit is set to 1 regardless of the value of the DIEN bit to allow polling. The interrupt can be masked by clearing DIEN, but cannot be cleared by writing to this bit. If DIRQ = 1 and DIEN = 1, an interrupt occurs. • TRMD = 0 (receive mode) 0: No unread data in SSIRDR 1: Unread data in SSIRDR • TRMD = 1 (transmit mode) 0: Transmit buffer is full. 1: Transmit buffer is empty and requires data to be written to SSITDR.
23 to 4	—	—	R	Reserved The read value is not guaranteed. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	CHNO[1:0]	00	R	Channel Number These bits indicate the current channel number. However, if the length of data words is 8 or 16 bits, the value of these bits is meaningless. 00: 1st channel 01: 2nd channel 10: 3rd channel 11: 4th channel • TRMD = 0 (receive mode) CHNO indicates which channel the data in SSIRDR currently represents. This value will change as the data in SSIRDR is updated from the shift register. • TRMD = 1 (transmit mode) CHNO indicates which channel is required to be written to SSITDR. This value will change as the data is copied to the shift register, regardless of whether the data is written to SSITDR. These bits cannot be used when WS_MODE = 1 or CONT = 1 in the WS Mode Register.
1	SWNO	1	R	System Word Number This status bit indicates the current word number. However, if the length of data words is 8 or 16 bits, the value of this bit is meaningless. • TRMD = 0 (receive mode) SWNO indicates which system word the data in SSIRDR currently represents. This value will change as the data in SSIRDR is updated from the shift register, regardless of whether SSIRDR has been read. • TRMD = 1 (transmit mode) SWNO indicates which system word is required to be written to SSITDR. This value will change as the data is copied to the shift register, regardless of whether the data is written to SSITDR. This bit cannot be used when WS_MODE = 1 or CONT = 1 in the WS Mode Register.
0	IDST	Undefined	R	Idle Mode Status Flag This status flag indicates that the serial bus activity has stopped. This bit is cleared if EN = 1 and the serial bus are currently active. This bit is automatically set to 1 under the following conditions. • SSI = Master transmitter (SWSD = 1 and TRMD = 1) This bit is set to 1 when the EN bit is cleared and data written in SSITDR has been output from the serial data input/output pin (SSI_SDATA). • SSI = Master receiver (SWSD = 1 and TRMD = 0) This bit is set to 1 when the EN bit is cleared and transfer of the current system word is completed. • SSI = Slave transmitter/receiver (SWSD = 0) This bit is set to 1 when the EN bit is cleared and transfer of the current system word is completed. Note: If an external device stops the serial bus clock before transfer of the current system word is completed, this bit is not set.

28A.2.3 Transmit Data Register (SSITDRn) (n = 0 to 9)

SSITDR is a 32-bit register that holds data to be transmitted.

Data written to this register is transferred to the shift register upon transmission request. If the data word length is less than 32 bits, the alignment is determined by the setting of the PDTA control bit in SSICR. The data in the buffer can be accessed by reading this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SSITDR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSITDR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SSITDR[31:0]	All 0	R/W	Transmit Data Data transmitted from SSI.

28A.2.4 Receive Data Register (SSIRDRn) (n = 0 to 9)

SSIRDR is a 32-bit register that stores receive messages.

Data in this register is transferred from the shift register each time data word is received. If the data word length is less than 32 bits, the alignment is determined by the setting of the PDTA control bit in SSICR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SSIRDR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SSRDR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SSIRDR[31:0]	All 0	R	Receive Data Data received from external pins.

28A.2.5 WS Mode Register (SSIWSRn) (n = 0 to 9)

SSIWSR is a 32-bit readable/writable register that sets the TDM format, monaural format, and WS continue function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	WIDTH[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CONT	—	—	—	—	—	—	MONO	WS_ MODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
20 to 16	WIDTH[4:0]	00000	R/W	SYNC Pulse Width Change • When the TDM format is used (WS_MODE = 1 and MONO = 0 in this register): 00000: TDM format Other than 00000: Setting prohibited • When the monaural format is used (WS_MODE = 1 and MONO = 1 in this register): 00000: Setting prohibited 00001: Pulse width is equivalent to one cycle of SCK. 00010: Pulse width is equivalent to two cycles of SCK. ... 11111: Pulse width is equivalent to 31 cycles of SCK. Note that the set value of the system word length bits (SWL) in SSICR should be greater than that of the SYNC pulse width bits (WIDTH) when the monaural format is used.
15 to 9	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
8	CONT	0	R/W	WS Continue Function 0: WS continue function is disabled. 1: WS continue function is enabled. Note: This bit can only be set in master mode (SSICR.SCKD = 1, SSICR.SWSD = 1).
7 to 2	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
1	MONO	0	R/W	TDM Format/Monaural Format Selects the TDM format or monaural format. When the normal stereo format, multi-channel format, this bit should be 0. 0: TDM format 1: Monaural format
0	WS_MODE	0	R/W	WS Mode 0: Stereo format, multi-channel format 1: TDM format, monaural format

28A.2.6 FS Mode Register (SSIFMRn) (n = 0 to 9)

SSIFMR is used to set the frequency switching detection function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	DTCT[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	CTDV[1:0]		—	—	—	FSEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
21 to 16	DTCT[5:0]	000000	R/W	Frequency Switching Detection Range Set 000100: Set the value in the range as 5.
15 to 6	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
5, 4	CTDV[1:0]	00	R/W	Bus Clock Division Ratio Sets the bus clock division ratio used for the frequency switching detection function. 11: Set the switching detection clock frequency = bus clock frequency/8.
3 to 1	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
0	FSEN	0	R/W	Frequency Switching Detection Function Enable 0: The frequency switching detection function is disabled. 1: The frequency switching detection function is enabled. Note: This bit must be enabled after the desired settings have been made for SWSP in SSICR and WS_MODE in SSIWSR.

28A.2.7 FS Status Register (SSIFSRn) (n = 0 to 9)

SSIFSR is used to read the frequency switching detection status and information on the frequency counter.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FCST	DTST	—	—	FCNT[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/WC0	R/WC0	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The read value is 0. The write value should always be 0.
15	FCST	0	R/WC0	WS Stopped Status Flag In the frequency switching detection function, this status flag reflects the state that the WS signal is stopped. When FCST = 1, this bit indicates that the WS signal has stopped (the state is detected only when FSEN in SSIFMR = 1). Write 0 if this bit is cleared to 0.
14	DTST	0	R/WC0	Frequency Switching Detection Status Flag In the frequency switching detection function, this status flag reflects the state that frequency switching has been detected. When DTST = 1, this bit indicates that the switching has been detected (the state is detected only when FSEN in SSIFMR = 1). Write 0 if this bit is cleared to 0.
13, 12	—	0	R	Reserved The read value is 0. The write value should always be 0.
11 to 0	FCNT[11:0]	H'000	R	Frequency Count Monitor When the frequency switching detection function is enabled, the count value between WS signal edges is reflected according to the setting of the operating mode and the serial WS polarity (SWSP in SSICR). This value is updated when the frequency is switched and the WS signal has been detected.

28A.3 Operation

28A.3.1 Bus Format

The SSI module can operate as a transmitter or a receiver and can be configured into many serial bus formats in either mode.

The bus format can be selected from one of the four major modes shown in Table 28A.2.

Table 28A.2 Bus Format for SSI Module

	SSICR																	SSIWSR		
	TRMD	SCKD	SWSD	EN	MUEN	DIEN	IIEN	OIEN	UIEN	DEL	PDTA	SDTA	SPDP	SWSP	SCKP	SWL[2:0]	DWL[2:0]	CHNL[1:0]	WS_MODE	MONO	CONT
Slave receiver	0	0	0	Control bits						Configuration bits									WS mode bits		
Slave transmitter	1	0	0																		
Master receiver	0	1	1																		
Master transmitter	1	1	1																		

(1) Slave receiver

This mode allows the module to receive serial data from another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of the SSI module, operation is not guaranteed.

(2) Slave transmitter

This mode allows the module to transmit serial data to another device. The clock and word select signal used for the serial data stream is also supplied from an external device. If these signals do not conform to the format specified in the configuration fields of the SSI module, operation is not guaranteed.

(3) Master receiver

This mode allows the module to receive serial data from another device. The clock and word select signals are internally derived from the CLK_FS input clock. The format of these signals is defined in the configuration fields of the SSI module. If the incoming data does not follow the configured format, operation is not guaranteed.

(4) Master transmitter

This mode allows the module to transmit serial data to another device. The clock and word select signals are internally derived from the CLK_FS input clock. The format of these signals is defined in the configuration fields of the SSI module.

(5) Setting for each format

Table 28A.3 shows the setting for each format:

Table 28A.3 Setting for Each Format

	SSICR	SSIWSR		
Format	**CHNL[1:0]**	**WS_MODE**	**MONO**	**WIDTH[4:0]**
Stereo format	B'00	0	0	B'00000
Multi-channel format	B'01/B'10/B'11	0	0	B'00000
Monaural format	B'00	1	1	B'00001 to B'11111
TDM format	B'00/B'01/B'10/B'11 *	1	0	B'00000

(6) Configuration bits (related to word length)

There are many configurations the SSI module supports, but only some of the combinations are shown below for the I2S, left-aligned, and right-aligned formats.

Figure 28A.2 and Figure 28A.3 demonstrate the supported I2S format both with and without padding. Padding occurs when the data word length is smaller than the system word length.

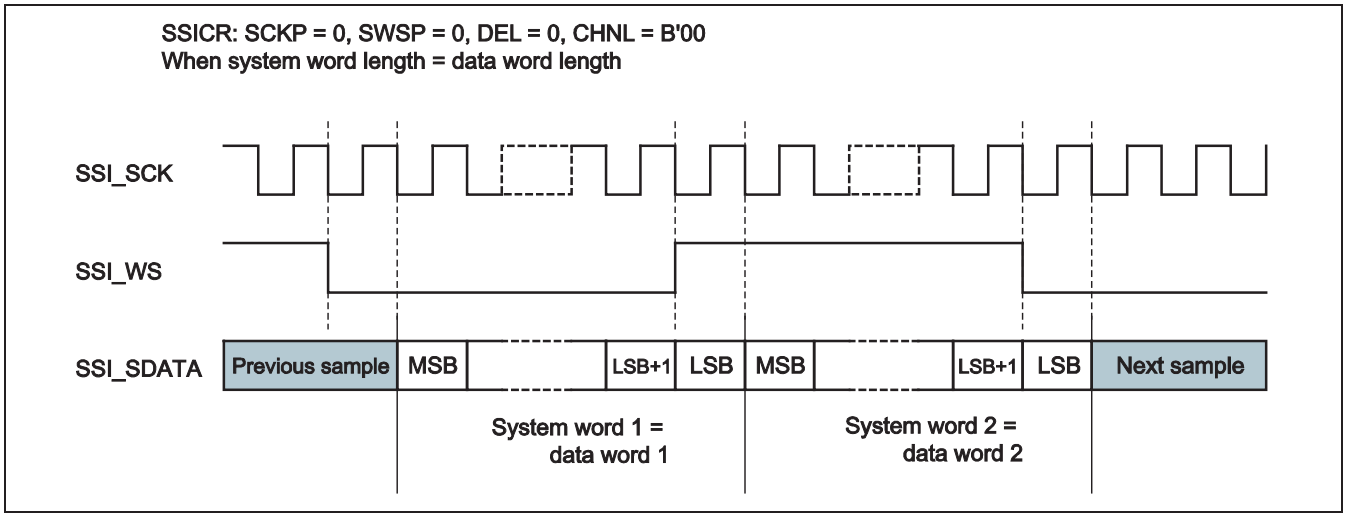


Figure 28A.2 I2S Format (without Padding)

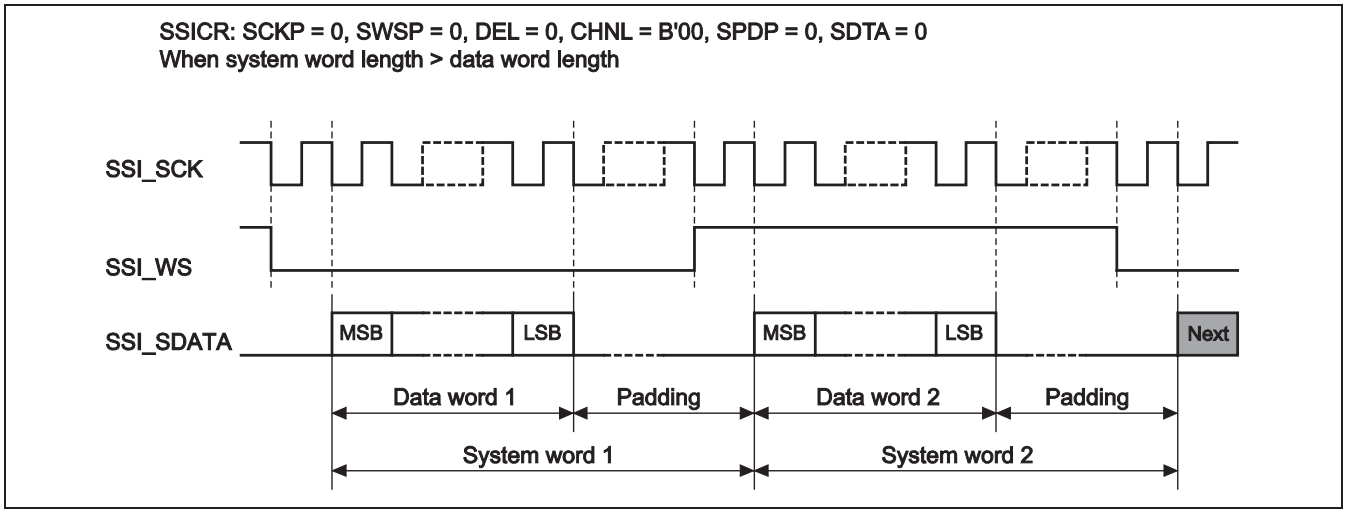


Figure 28A.3 I2S Format (with Padding)

Figure 28A.4 shows the left-aligned format and Figure 28A.5 shows the right-aligned format. Padding is assumed in both cases, but may not be present in a final implementation if the system word length equals the data word length.

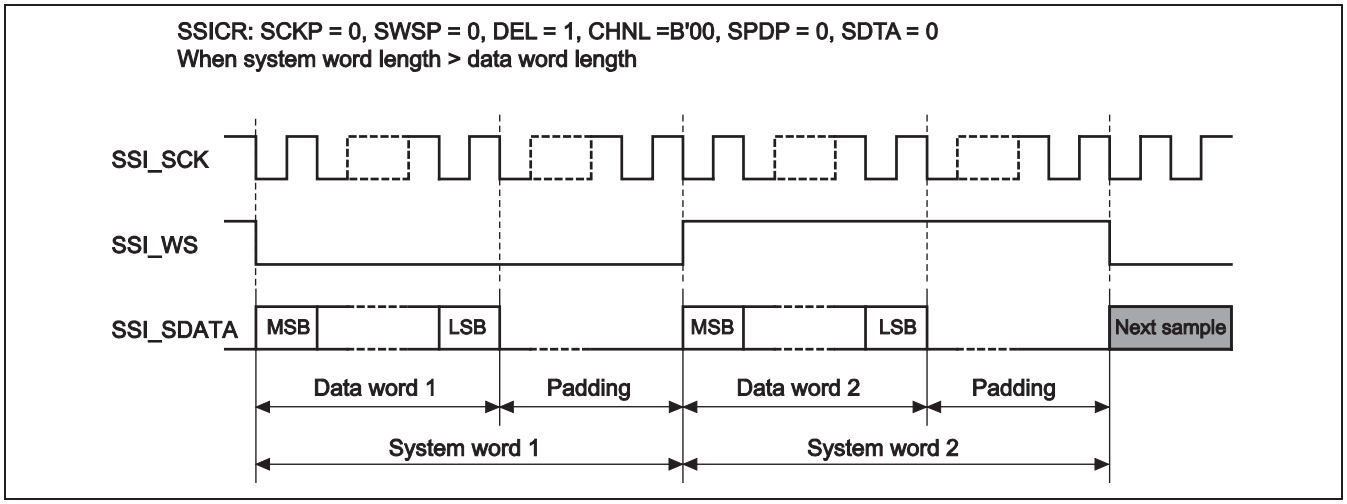


Figure 28A.4 Left-Aligned Format
(Transmitting and Receiving in the Order of Serial Data and Padding Bits)

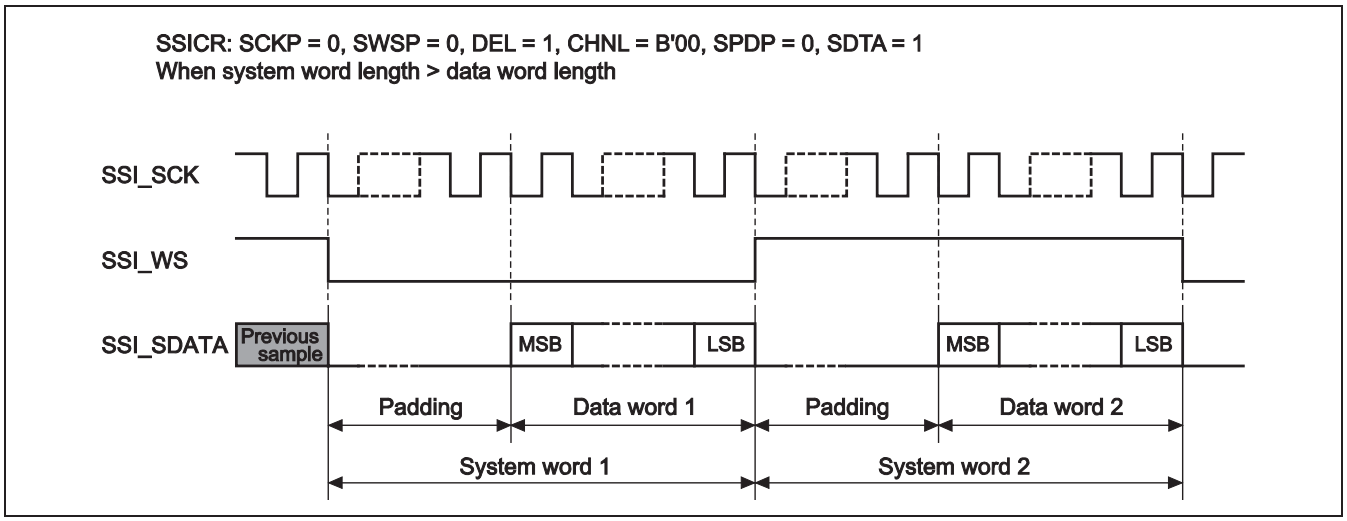


Figure 28A.5 Right-Aligned Format
(Transmitting and Receiving in the Order of Padding Bits and Serial Data)

(7) Multi-channel formats

Some devices extend the definition of the I2S format and allow more than two channels to be transferred within two system words.

The SSI module supports the transfer of two, three, and four channels by using the CHNL, SWL and DWL bits only when the system word length (SWL) is greater than or equal to the data word length (DWL) multiplied by channels (CHNL).

Table 28A.4 shows the number of padding bits for each of the valid setting. If setting is not valid, "—" is indicated instead of a number.

Table 28A.4 The Number of Padding Bits for Each Valid Setting

Padding Bits Per System Word			DWL[2:0]	B'000	B'001	B'010	B'011	B'100	B'101	B'110
CHNL [1:0]	Decoded Channels per System Word	SWL [2:0]	Decoded Word Length	8	16	18	20	22	24	32
B'00	1	B'000	8	0	—	—	—	—	—	—
		B'001	16	8	0	—	—	—	—	—
		B'010	24	16	8	6	4	2	0	—
		B'011	32	24	16	14	12	10	8	0
		B'100	48	40	32	30	28	26	24	16
		B'101	64	56	48	46	44	42	40	32
		B'110	128	120	112	110	108	106	104	96
		B'111	256	248	240	238	236	234	232	224
B'01	2	B'000	8	—	—	—	—	—	—	—
		B'001	16	0	—	—	—	—	—	—
		B'010	24	8	—	—	—	—	—	—
		B'011	32	16	0	—	—	—	—	—
		B'100	48	32	16	12	8	4	0	—
		B'101	64	48	32	28	24	20	16	0
		B'110	128	112	96	92	88	84	80	64
		B'111	256	240	224	220	216	212	208	192
B'10	3	B'000	8	—	—	—	—	—	—	—
		B'001	16	—	—	—	—	—	—	—
		B'010	24	0	—	—	—	—	—	—
		B'011	32	8	—	—	—	—	—	—
		B'100	48	24	0	—	—	—	—	—
		B'101	64	40	16	10	4	—	—	—
		B'110	128	104	80	74	68	62	56	32
		B'111	256	232	208	202	196	190	184	160

Padding Bits Per System Word		DWL[2:0]	B'000	B'001	B'010	B'011	B'100	B'101	B'110
CHNL [1:0]	Decoded Channels per System Word	SWL [2:0]	Decoded Word Length	8	16	18	20	22	24	32
B'11	4	B'000	8	—	—	—	—	—	—	—
		B'001	16	—	—	—	—	—	—	—
		B'010	24	—	—	—	—	—	—	—
		B'011	32	0	—	—	—	—	—	—
		B'100	48	16	—	—	—	—	—	—
		B'101	64	32	0	—	—	—	—	—
		B'110	128	96	64	56	48	40	32	0
		B'111	256	224	192	184	176	168	160	128

When the SSI module acts as a transmitter, each word written to SSITDR is transmitted to the serial audio bus in the order they are written. When the SSI module acts as a receiver, each word received by the serial audio bus is read in the order received from SSIRDR.

Figure 28A.6 to Figure 28A.8 show how two, three and four channels are transferred to the serial audio bus. Note that there are no padding bits in the first example, the second example is left-aligned and the third is right-aligned. This selection is arbitrary and is just for demonstration purposes only.

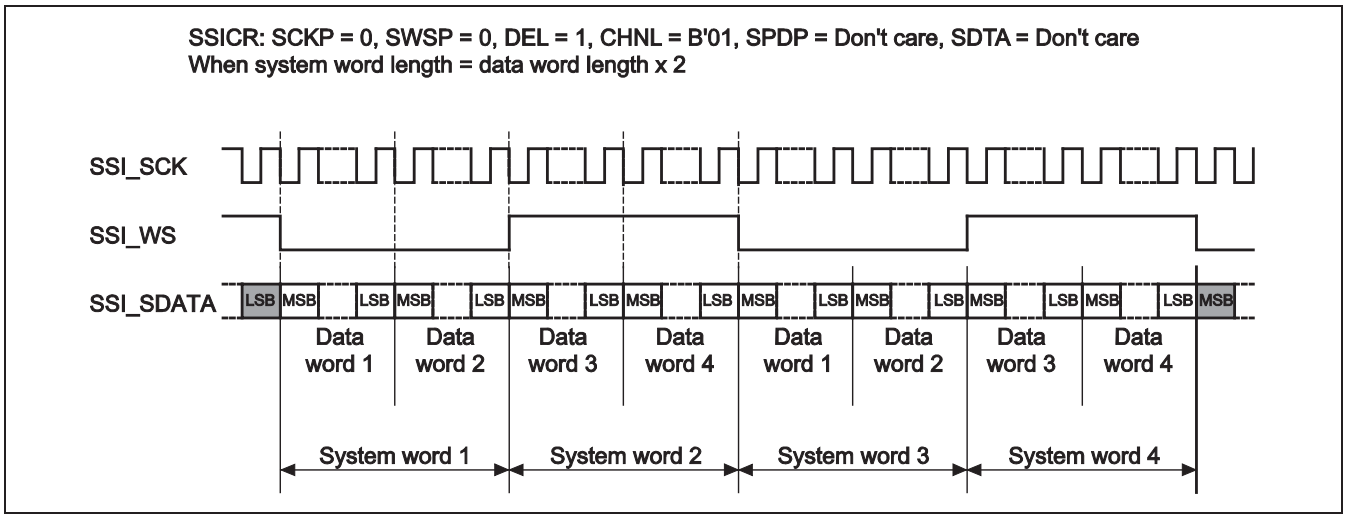


Figure 28A.6 Multi-Channel Format (Two Channels without Padding)

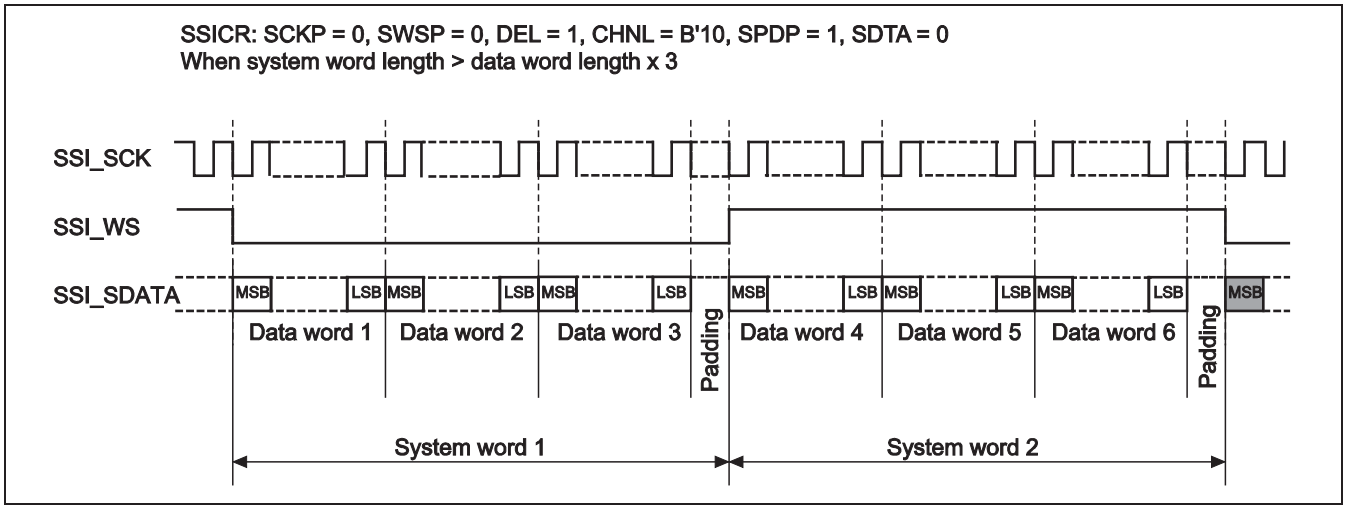


Figure 28A.7 Multi-Channel Format (Three Channels with High Padding)

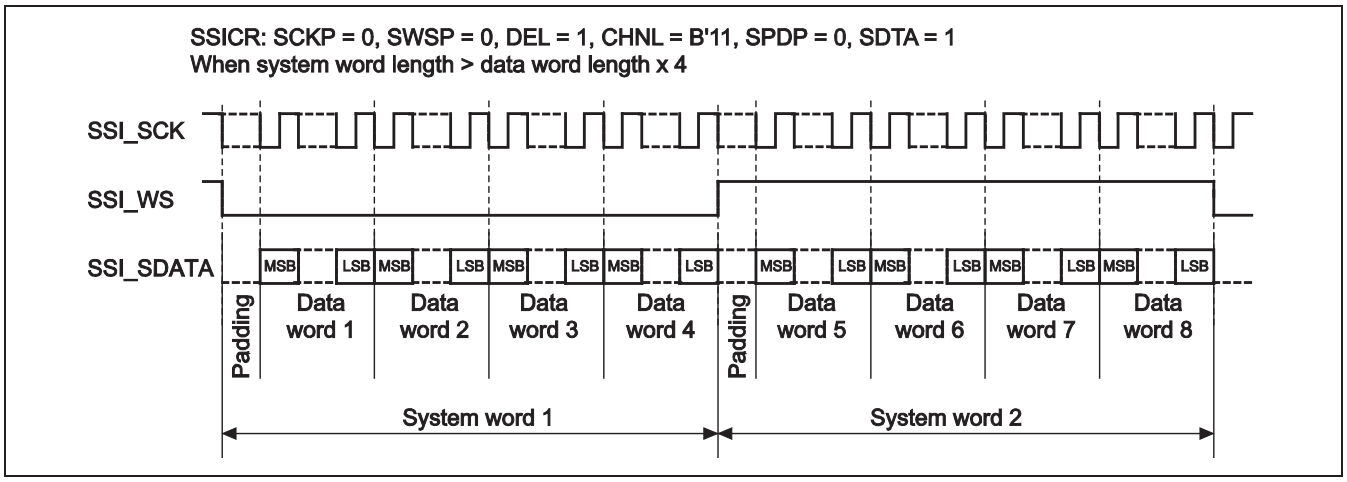


Figure 28A.8 Multi-Channel Format (Four Channels; Transmitting and Receiving in the Order of Padding Bits and Serial Data; with Padding)

(8) TDM formats

The TDM format is used for connecting the SSI with a multi-channel device which supports TDM. The TDM format is set by using the WS_MODE and MONO bits in SSIWSR. When the SWSP bit in SSICR is 0 with the TDM format, SSI_WS is driven high over the period of system word 1, and pulled low otherwise. When the SWSP bit is 1, SSI_WS is pulled low over the period of system word 1, and driven high otherwise. The pulses generated on the SSI_WS signal are referred to as SYNC pulses.

Figure 28A.9 and Figure 28A.10 show the TDM formats without padding and with padding.

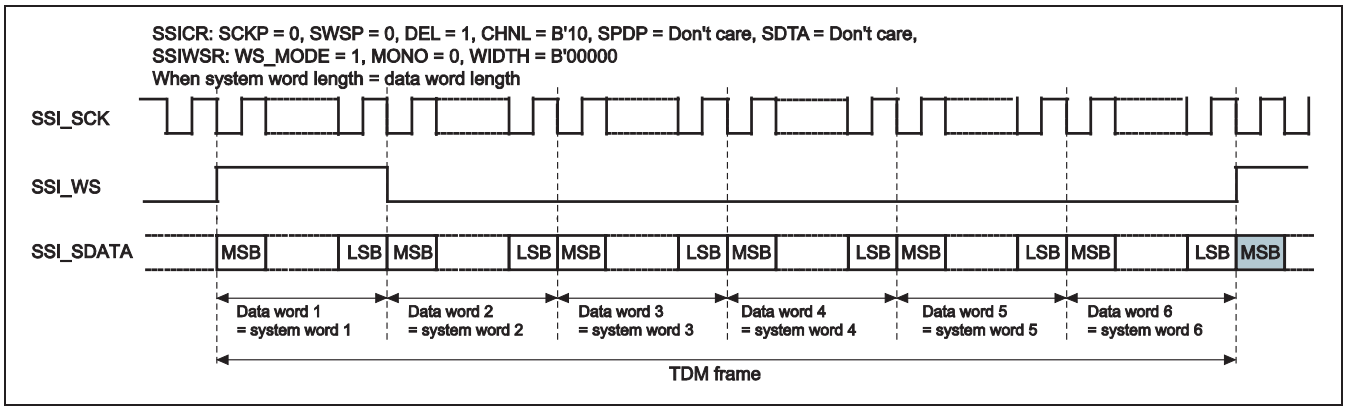


Figure 28A.9 TDM Format (Six System Words, without Padding)

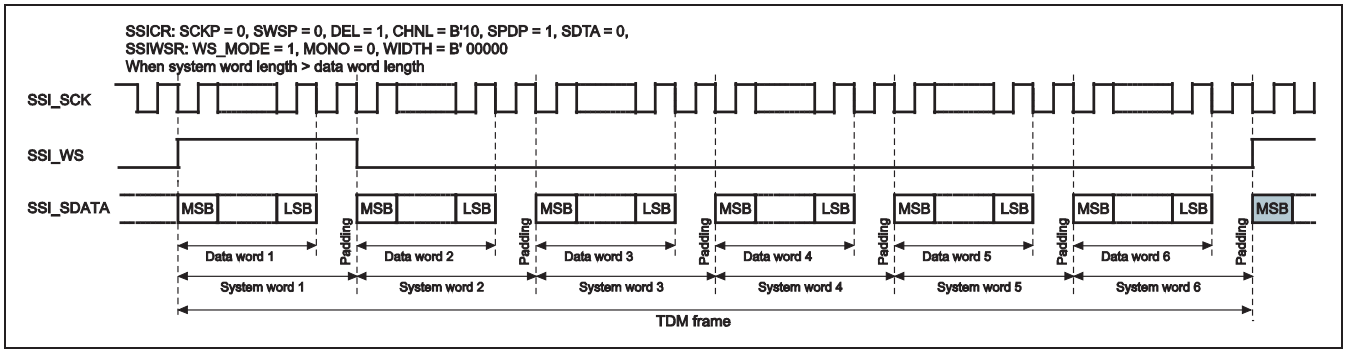


Figure 28A.10 TDM Format (Six System Words, with Padding)

The following describes operation in each mode:

(a) Master transmitter

By a transfer start trigger (setting the EN bit in the control register to 1), a transfer of system word 1 begins synchronously with the SYNC pulses.

By a transfer stop trigger (setting the EN bit in the control register to 0), a transfer is stopped at the end of the currently-transferred system word and the SDATA signal is output according to the SPDP setting in SSICR (when SPDP = 0, a low-level signal is output).

If transmit data is not ready in the SSI module during transmission, an underflow will occur. When an underflow occurs, data to be output for the SYNC pulses cannot be determined. Therefore, stop and reconfigure the transfer.

(b) Master receiver

By a transfer start trigger (setting the EN bit in the control register to 1), a reception of system word 1 data begins at the point where the SSI module recognizes a SYNC pulse.

By a transfer stop trigger (setting the EN bit in the control register to 0), a reception is stopped at the end of the currently-transferred system word.

The receive data register should not be read when it does not have data. If read, an underflow will occur. When an underflow occurs, stop and reconfigure the transfer.

The receive data should not be written to before read. If written to, an overflow will occur. When an overflow occurs, stop and reconfigure the transfer.

(c) Slave transmitter

By a transfer start trigger (setting the EN bit in the control register to 1), a transfer of system word 1 begins synchronously with the SYNC pulses.

By a transfer stop trigger (setting the EN bit in the control register to 0), a transfer is stopped at the end of the currently-transferred system word and the SDATA signal is output according to the SPDP setting in SSICR (when SPDP = 0, a low-level signal is output).

If transmit data is not ready in the SSI module during transmission, an underflow will occur. When an underflow occurs, data to be output for SYNC pulses cannot be determined. Therefore, stop and re-set the transfer.

Transfers cannot be performed if the SCK signal and SYNC pulses are not provided to the SSI module during transfer.

(d) Slave receiver

By a transfer start trigger (setting the EN bit in the control register to 1), a reception of system word 1 data begins at the point where the SSI module recognizes a SYNC pulse.

By a transfer stop trigger (setting the EN bit in the control register to 0), a reception is stopped at the end of the currently-transferred system word.

The receive data should not be read when it does not have data. If read, an underflow will occur. When an underflow occurs, stop and reconfigure the transfer.

The receive data register should not be written to before read. If written to, an overflow will occur. When an overflow occurs, stop and reconfigure the transfer.

Transfer cannot proceed if the SCK signal and SYNC pulses are not being provided to the SSI module during transfer.

(9) Monaural format

The monaural format is set by using the WS_MODE and MONO bits in SSIWSR. The available data lengths are 8 bits and 16 bits. When the SWSP bit in SSICR is 0 and the monaural format is selected, SSI_WS is driven high over the period from bit 1 to bit 31, and pulled low otherwise. When the SWSP bit is 1, SSI_WS is pulled low over the period from bit 1 to bit 31, and driven high otherwise. The pulses generated as the SSI_WS signal are referred to as SYNC pulses. The width of the SYNC pulses can be set to a value in bits between 1 and 31 by using the WIDTH bits in SSIWSR. The setting must be smaller than the system word length (SSICR.SWL). In the monaural format, the system word length is equal to one monaural frame period.

Figure 28A.11 shows the left-aligned monaural format and Figure 28A.12 shows the monaural format with a delay of one bit-period.

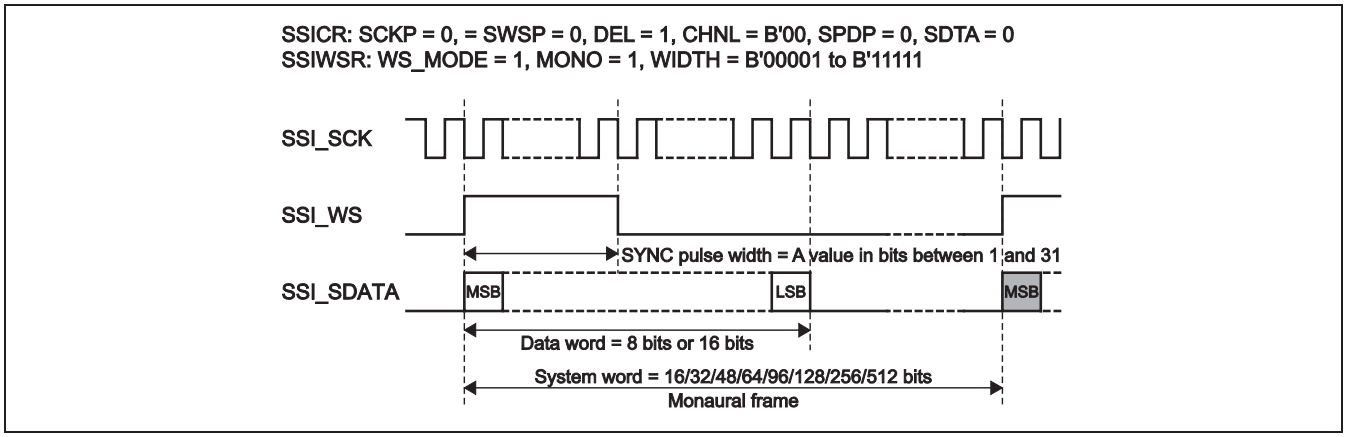


Figure 28A.11 Monaural Format (Left-Aligned)

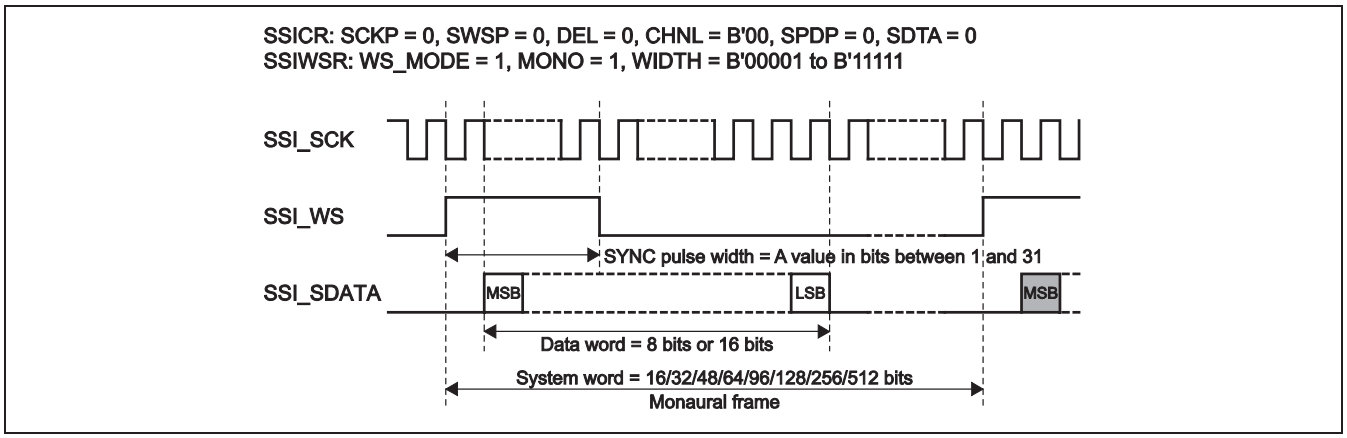


Figure 28A.12 Monaural Format (with 1-bit Delay)

(10) Configuration bits

Several more configuration bits are shown below. These bits are not mutually exclusive, but some combinations may not be useful for any other device.

These configuration bits are described below with reference to Figure 28A.13, Basic Sample Format.

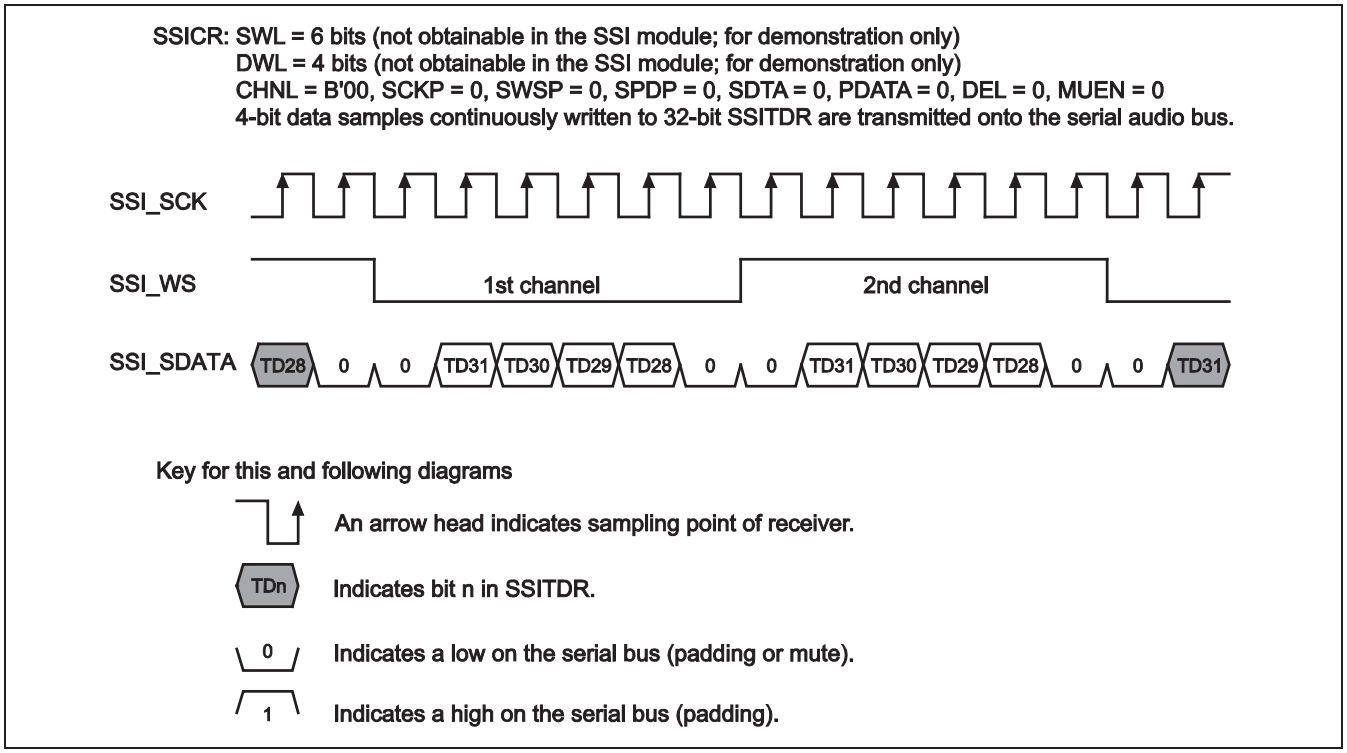


Figure 28A.13 Basic Sample Format (Transmit Mode with Example System/Data Word Length)

Figure 28A.13 uses a system word length of 6 bits and a data word length of 4 bits. These settings are not possible with the SSI module but are used only for clarification of the other configuration bits.

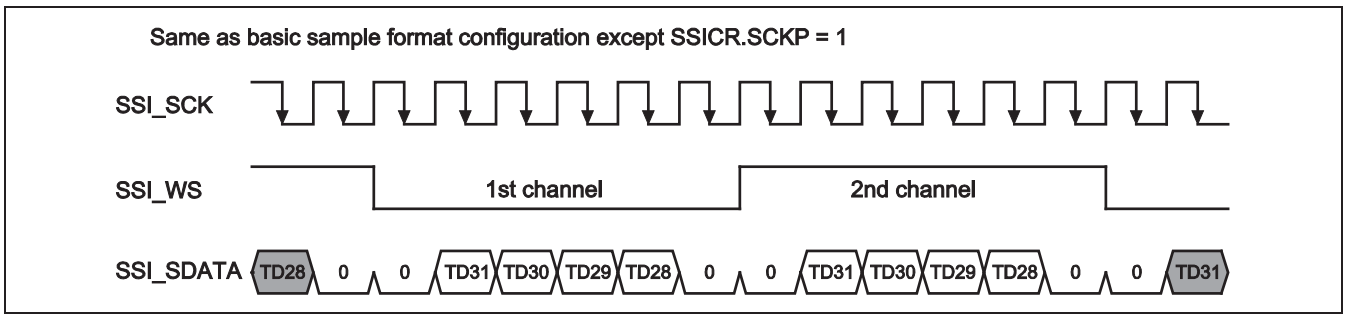


Figure 28A.14 Inverted Clock

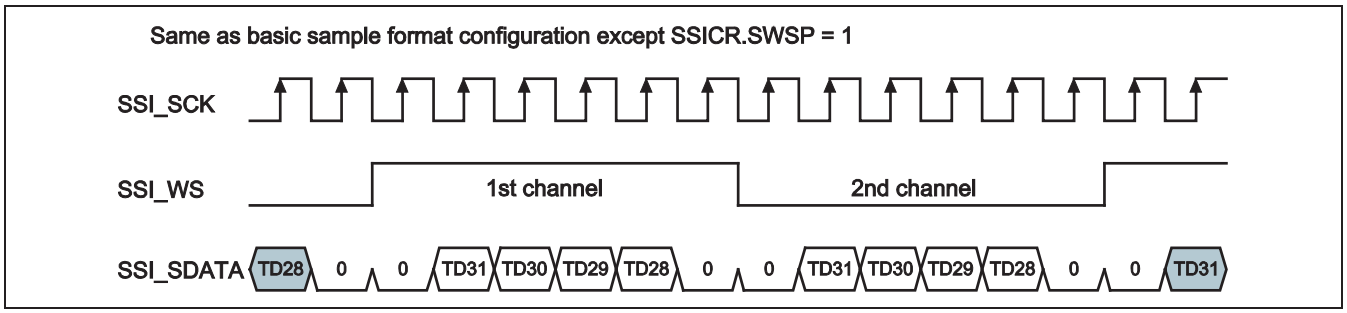


Figure 28A.15 Inverted Word Select

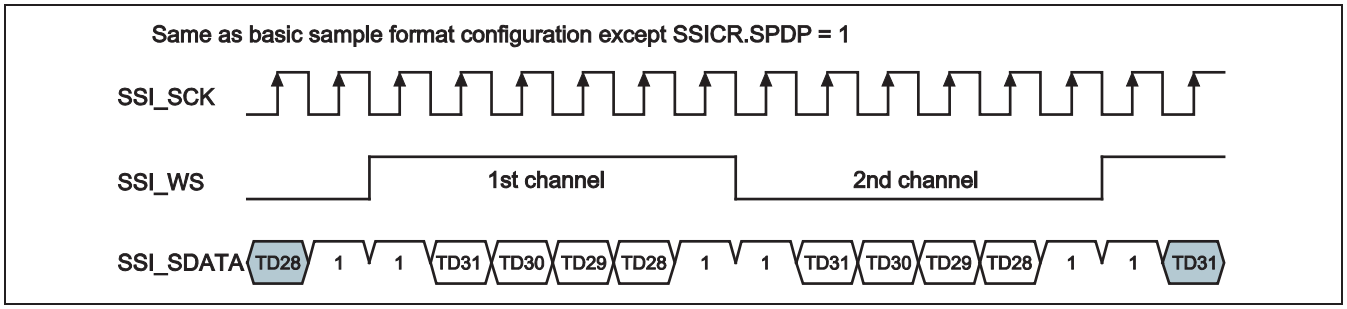


Figure 28A.16 Inverted Padding Polarity

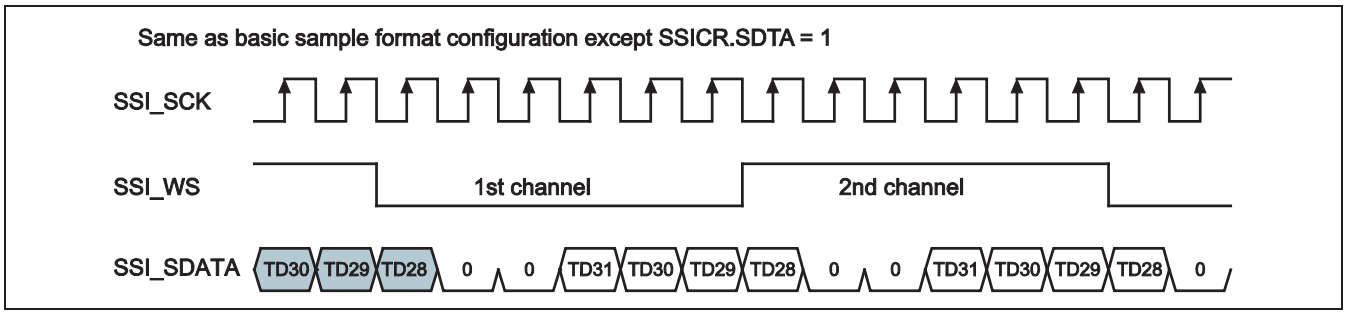


Figure 28A.17 Transmitting and Receiving in the Order of Padding Bits and Serial Data; with Delay

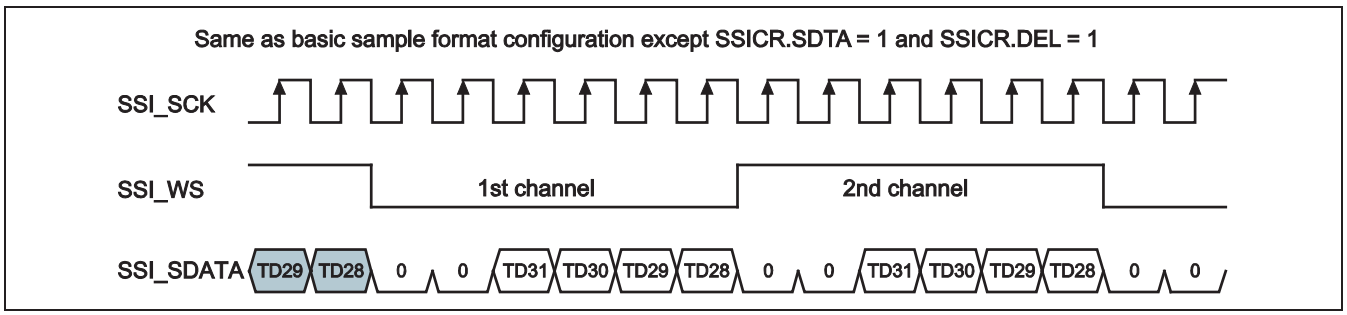


Figure 28A.18 Transmitting and Receiving in the Order of Padding Bits and Serial Data; without Delay

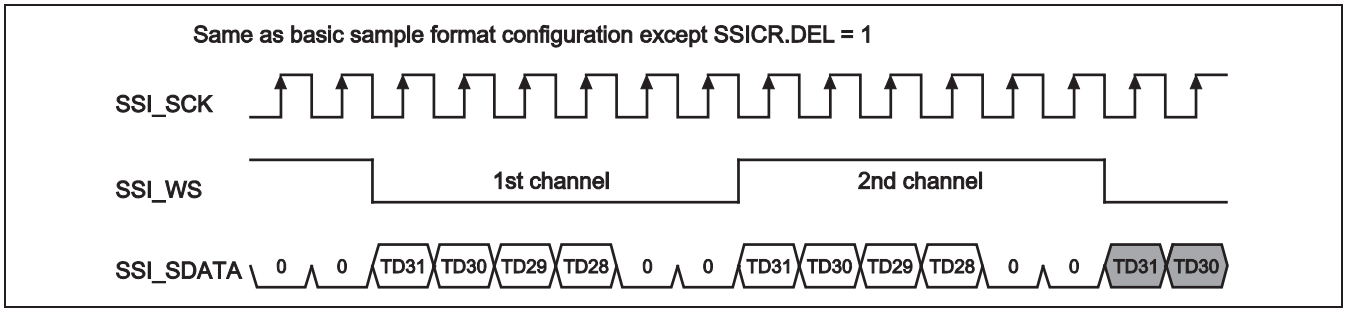


Figure 28A.19 Transmitting and Receiving in the Order of Serial Data and Padding Bits; without Delay

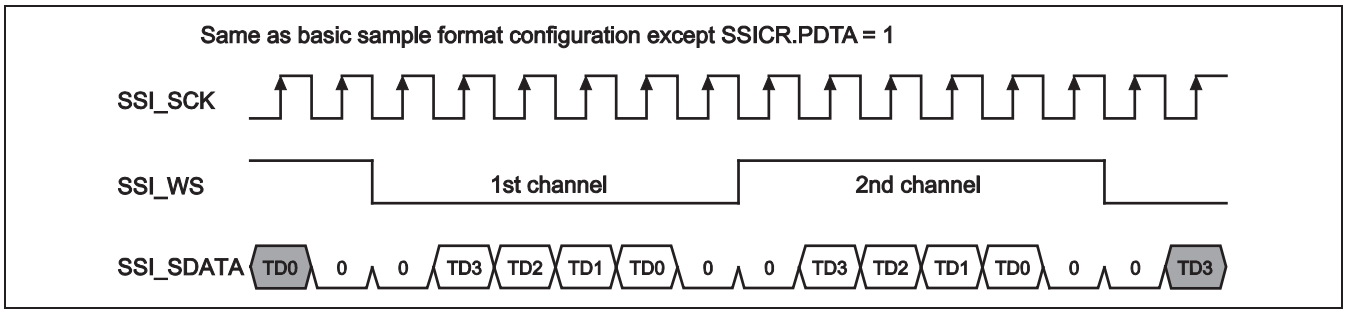


Figure 28A.20 Parallel Right-Aligned with Delay

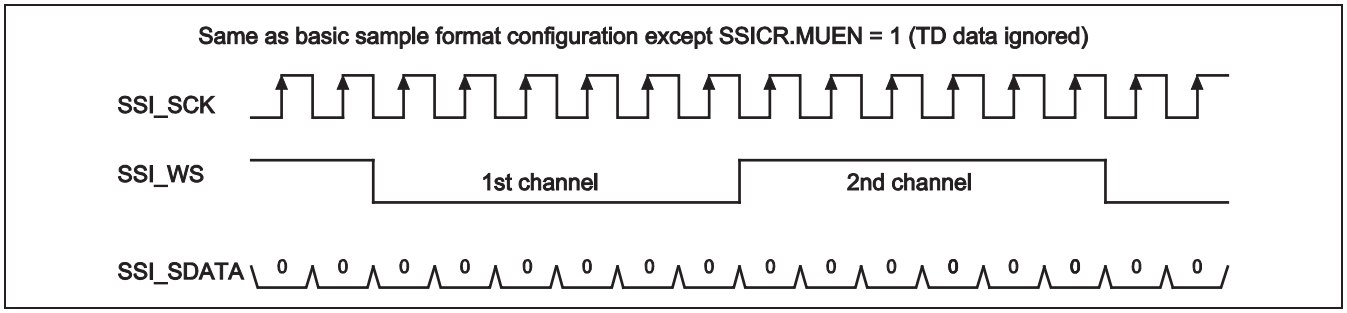


Figure 28A.21 Mute Enabled

(11) WS continue function

The WS continue function is used to output SSI_WS signal continuously regardless of whether data transfer is enabled or disabled. The WS continue function can be set by using the CONT bit in SSIWSR. This function can be combined with master mode only. When this function is enabled, the SSI_WS signal continues to operate even if the EN bit in SSICR is cleared to 0 (stopping a transfer). When this function is disabled, the SSI_WS signal operates synchronously with the EN bit.

Figure 28A.22 and Figure 28A.23 show operations when the WS continue function is enabled and disabled, respectively.

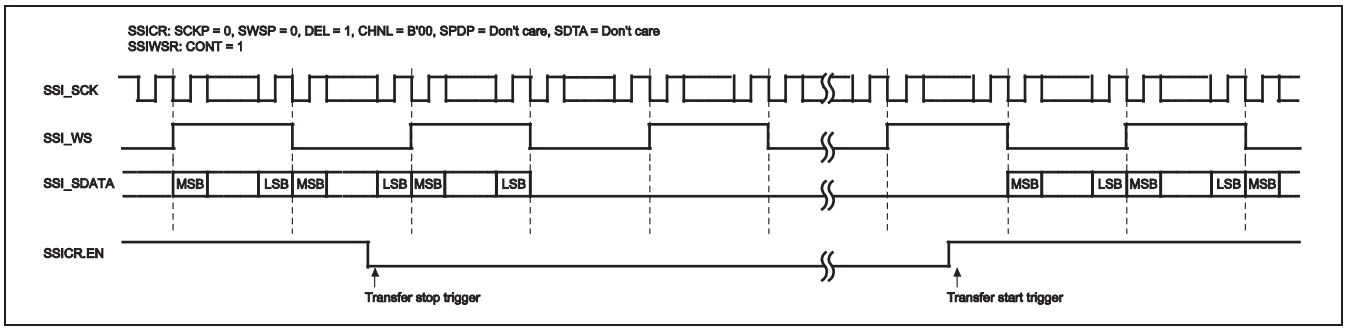


Figure 28A.22 WS Continue Function Operation (When the Function is Enabled)

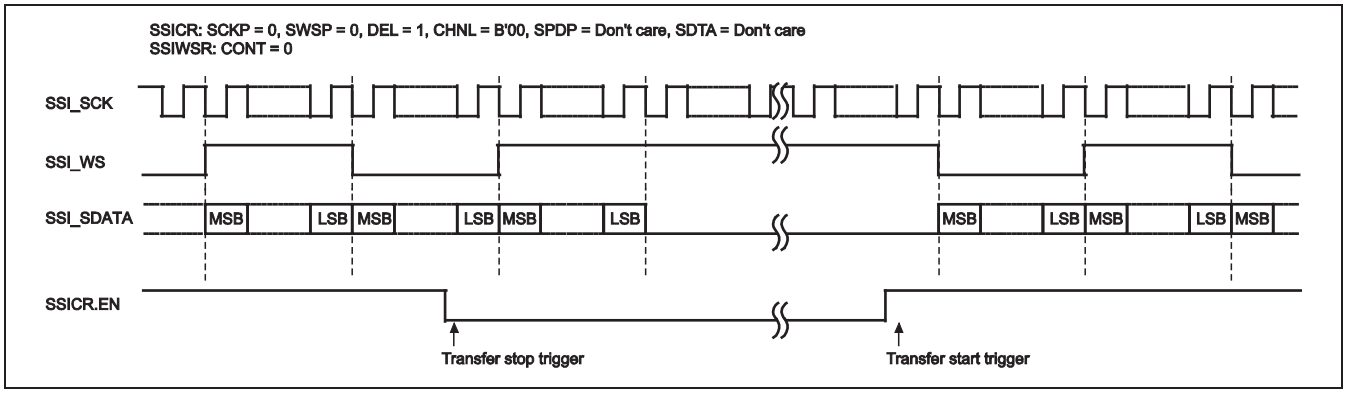


Figure 28A.23 WS Continue Function Operation (When the Function is Disabled)

(12) Bit alignment in transferred data

Figure 28A.24 to Figure 28A.36 show the bit alignment in transmit or receive data. Only the MSB first alignment is available. The waveforms in Figure 28A.24 to Figure 28A.36 are setting examples without delay (SSICR.DEL is set to 1, the number of bits specified with SSICR.DWL is the same as that specified with SSICR.SWL).

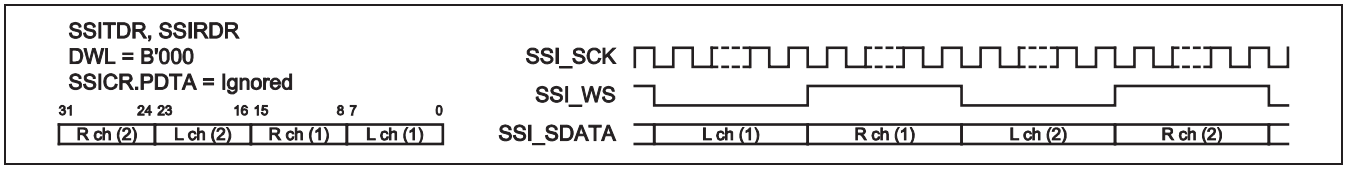


Figure 28A.24 Bit Alignment in 8-Bit Stereo Format

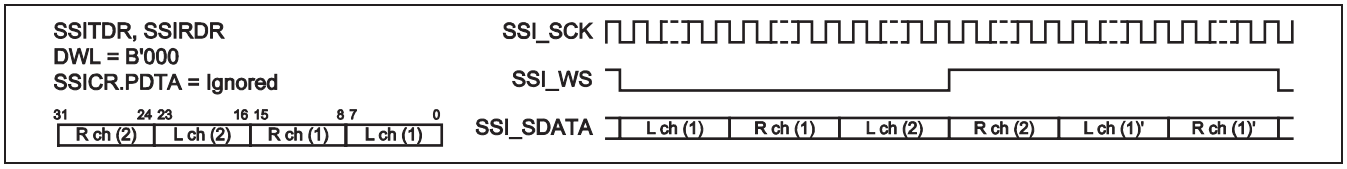


Figure 28A.25 Bit Alignment in 8-Bit Multi-Channel Format (Three Channels)

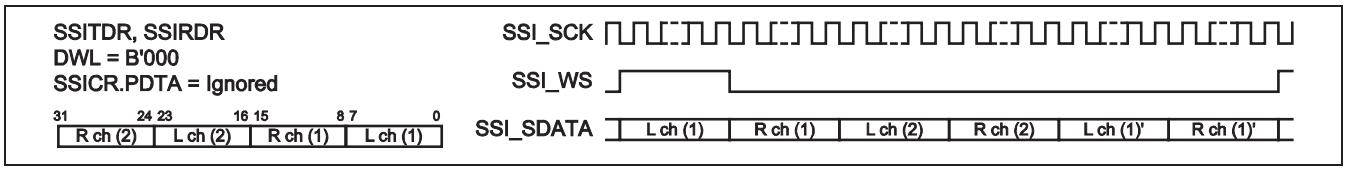


Figure 28A.26 Bit Alignment in 8-Bit TDM Format (Six System Words)

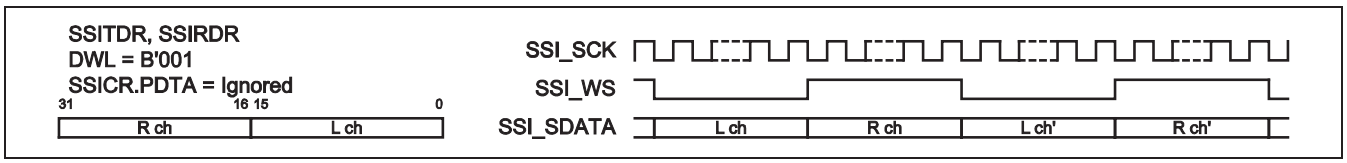


Figure 28A.27 Bit Alignment in 16-Bit Stereo Format

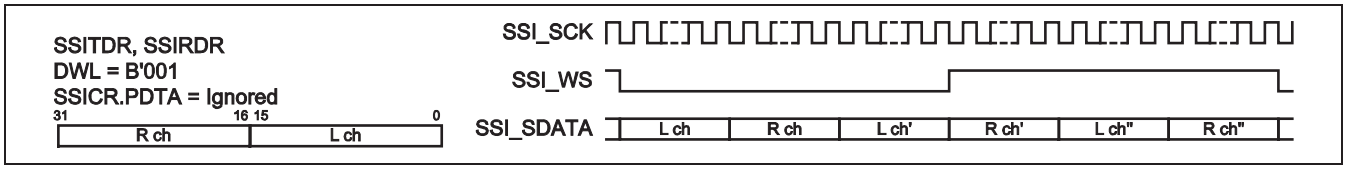


Figure 28A.28 Bit Alignment in 16-Bit Multi-Channel Format (Three Channels)

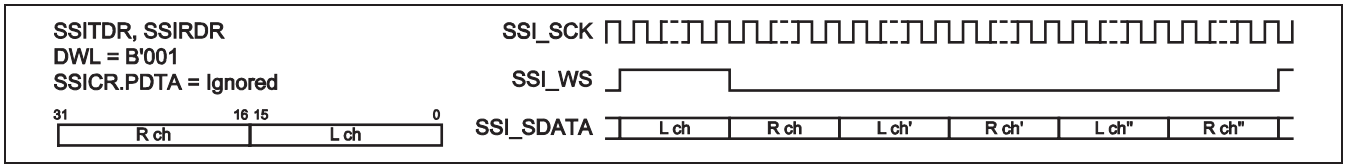


Figure 28A.29 Bit Alignment in 16-Bit TDM Format (Six System Words)

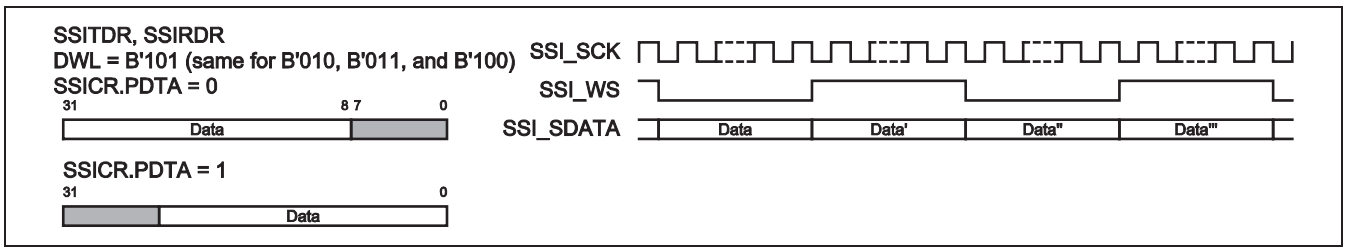


Figure 28A.30 Bit Alignment in 18-/20-/22-/24-Bit Stereo Format

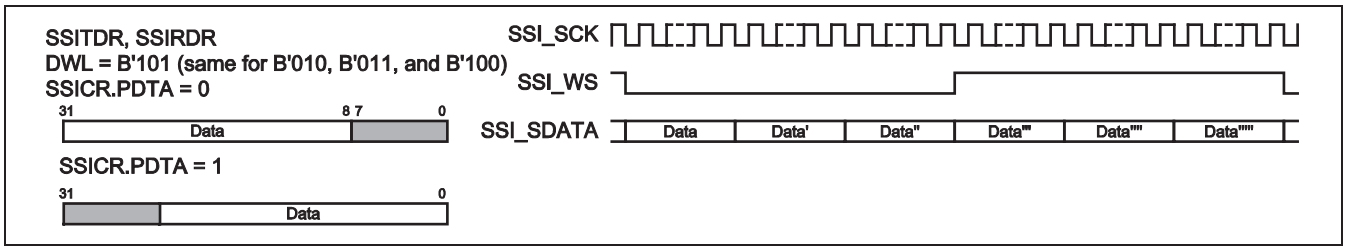


Figure 28A.31 Bit Alignment in 18-/20-/22-/24-Bit Multi-Channel Format (Three Channels)

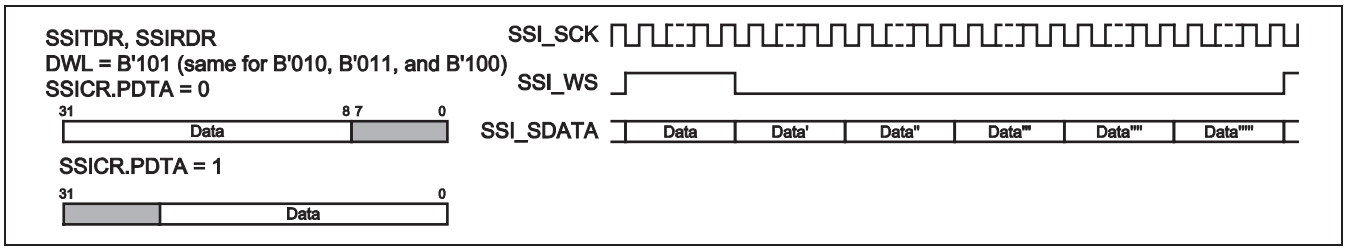


Figure 28A.32 Bit Alignment in 18-/20-/22-/24-Bit TDM Format (Six System Words)

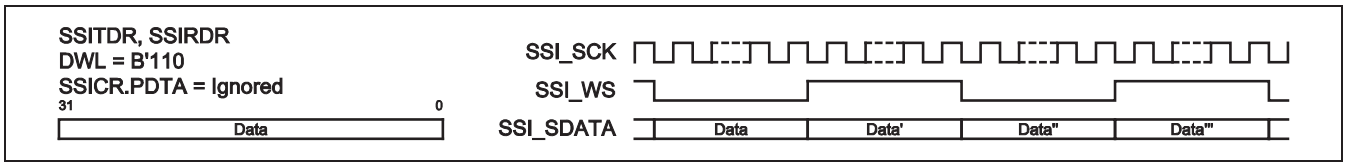


Figure 28A.33 Bit Alignment in 32-Bit Stereo Format

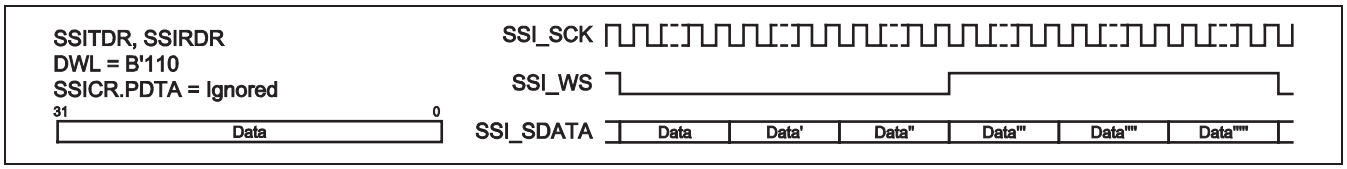


Figure 28A.34 Bit Alignment in 32-Bit Multi-Channel Format (Three Channels)

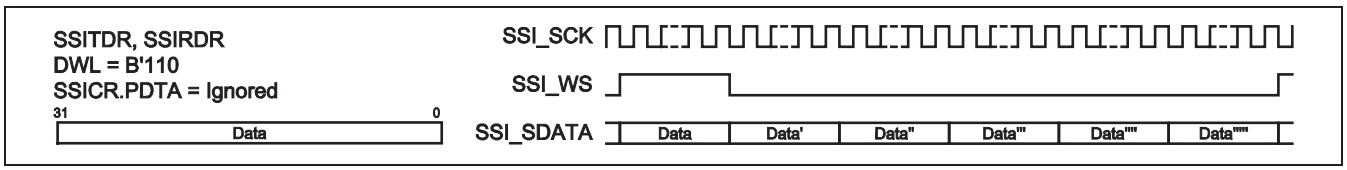


Figure 28A.35 Bit Alignment in 32-Bit TDM Format (Six System Words)

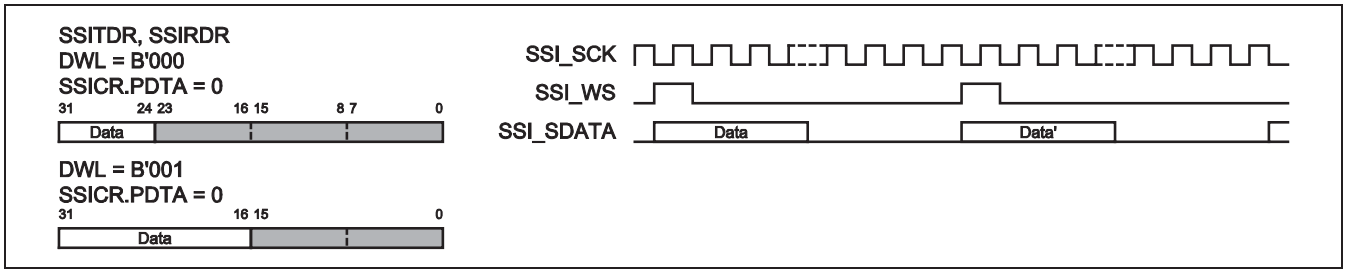


Figure 28A.36 Bit Alignment in 8-/16-Bit Monaural Format

28A.3.2 Operating Modes

There are three modes of operation: configuration, module enabled and module disabled. Figure 28A.37 shows how the module enters each of these modes.

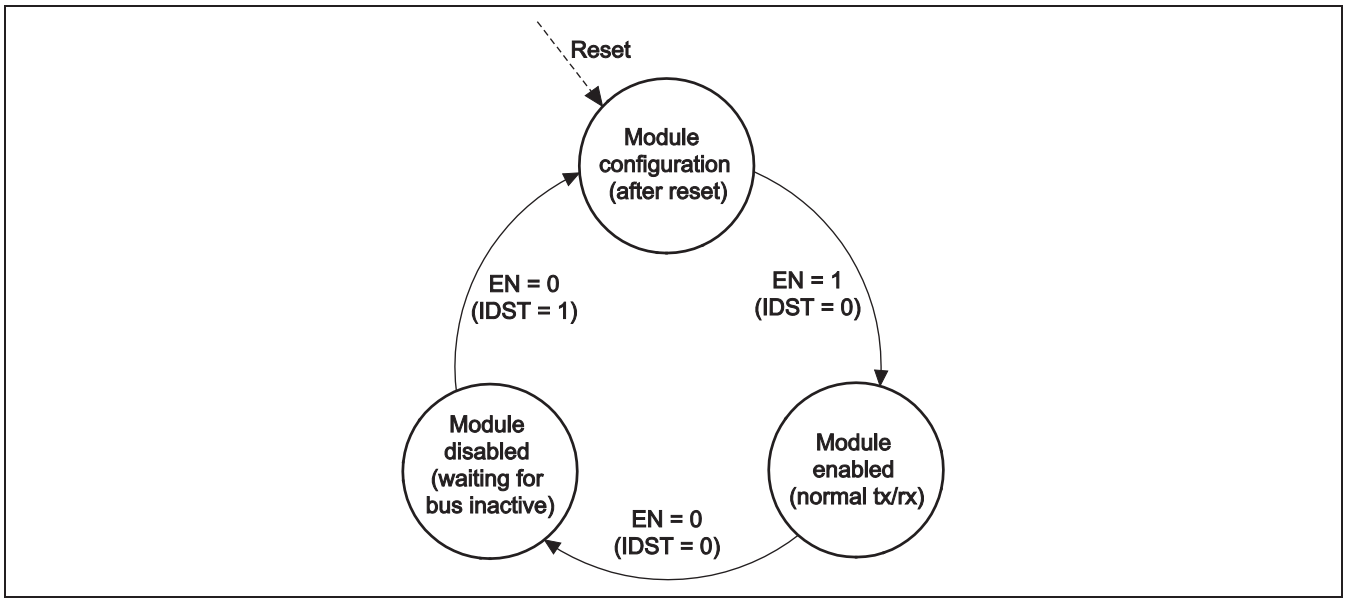


Figure 28A.37 Operating Modes

(1) Configuration mode

This mode is entered after the module is released from reset. All required configuration fields in the control register should be defined in this mode, before the SSI module is enabled by setting the EN bit.

Setting the EN bit causes the module to enter the module enabled mode.

(2) Module enabled mode

Operation of the module in this mode is dependent on the operating mode selected. For details, refer to Section 28A.3.3 Transmit Operation and Section 28A.3.4, Receive Operation, below.

28A.3.3 Transmit Operation

Transmission can be controlled either by DMA or interrupt.

DMA control is preferred to reduce the processor load. In DMA control mode, the processor will only receive interrupts if there is an underflow or overflow of data or the DMAC has finished its transfer.

The alternative method is using the interrupts that the SSI module generates to supply data as required. This mode has a higher interrupt load as the module is only double buffered and will require data to be written at least every system word period.

When disabling the module, the SSI clock* must remain present until the SSI module is in idle state, indicated by the SSISR.IIRQ bit.

Figure 28A.38 shows the transmit operation in DMA control mode, and Figure 28A.39 shows the transmit operation in interrupt control mode.

Note: * Input clock from the SSI_SCK pin when SCKD = 0.
Input clock from the CLK_FS pin when SCKD = 1.

Use the flowcharts in Figure 28A.38 and Figure 28A.39 when bits ind9 to ind0, which are covered in the description of SSI Mode Register 0 (SSI_MODE0) in Section 28, Serial Sound Interface Unit (SSIU), are set to 1 (independent SSI transfer).

(1) Transmission using DMA controller

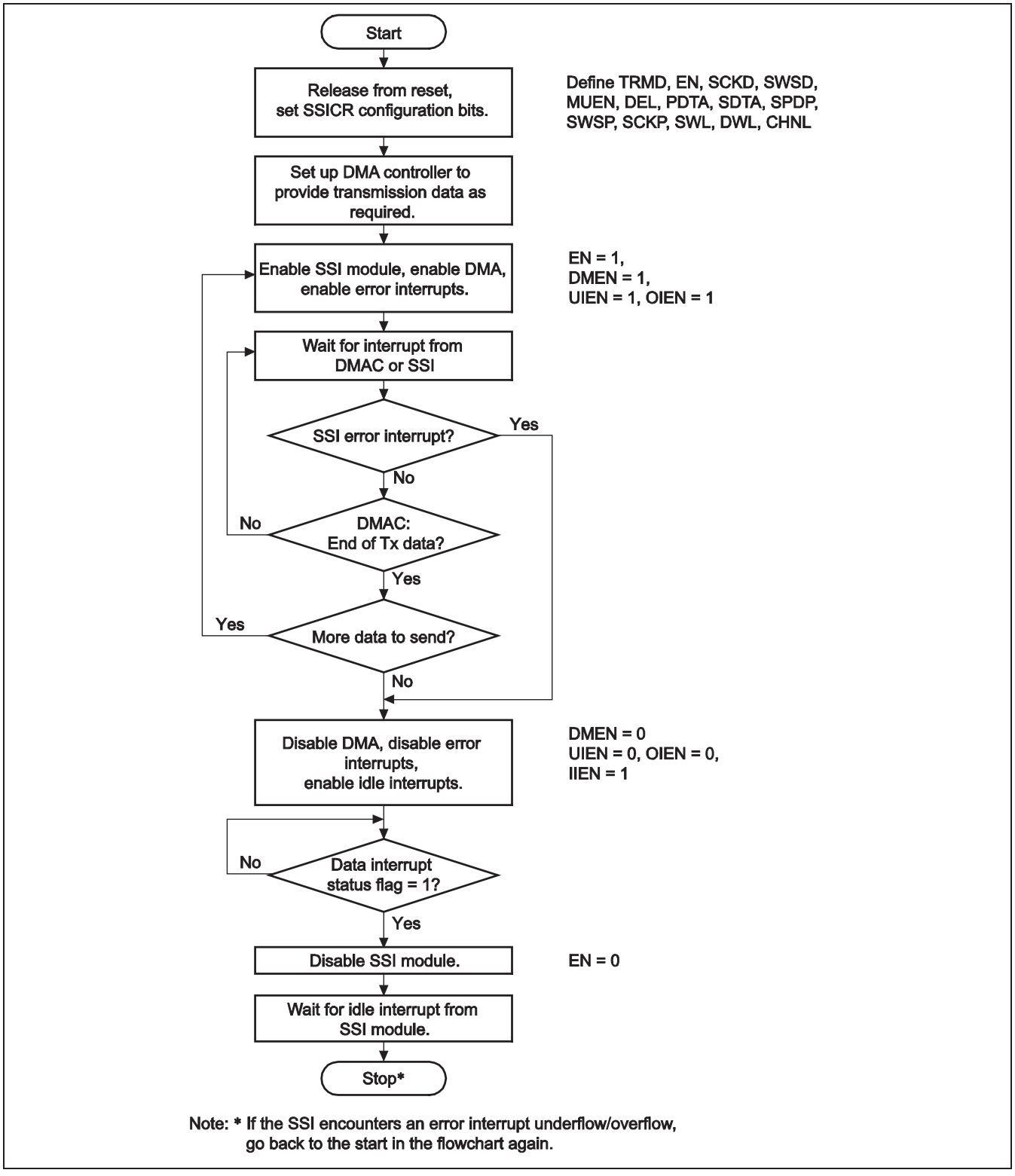


Figure 28A.38 Transmission Using DMA Controller

(2) Transmission using interrupt data flow control

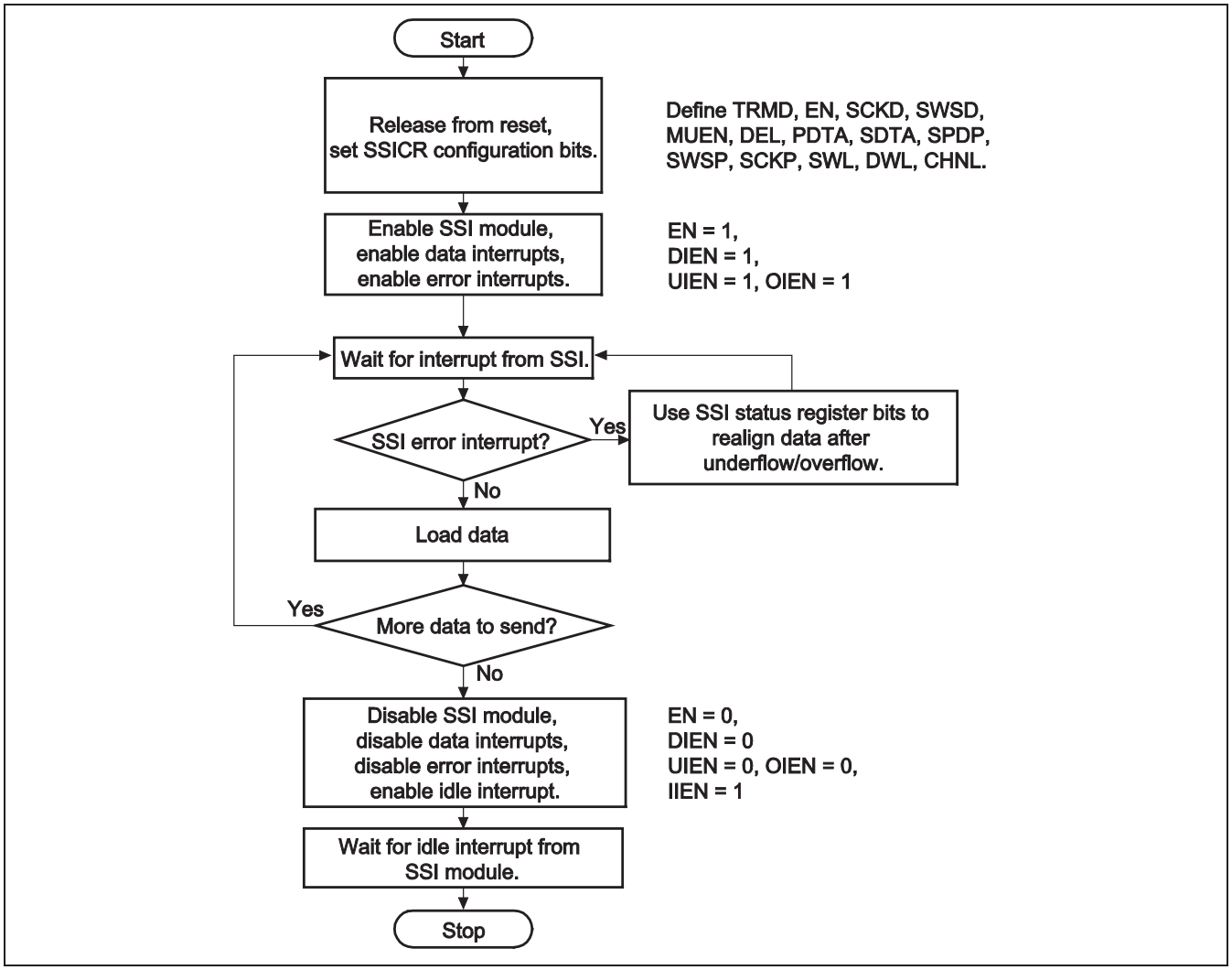


Figure 28A.39 Transmission Using Interrupt Data Flow Control

28A.3.4 Receive Operation

Like transmission, reception can be controlled either by DMA or interrupt.

Figure 28A.40 and Figure 28A.41 show the flow of operation.

When disabling the SSI module, the SSI clock* must be kept supplied until the SSISR.IIRQ bit is in idle state.

Note: * Input clock from the SSI_SCK pin when SCKD = 0.
Input clock from the CLK_FS pin when SCKD = 1.

Use the flowcharts in Figure 28A.40 and Figure 28A.41 when bits ind9 to ind0, which are covered in the description of SSI Mode Register 0 (SSI_MODE0) in Section 28, Serial Sound Interface Unit (SSIU), are set to 1 (independent SSI transfer).

(1) Reception using DMA controller

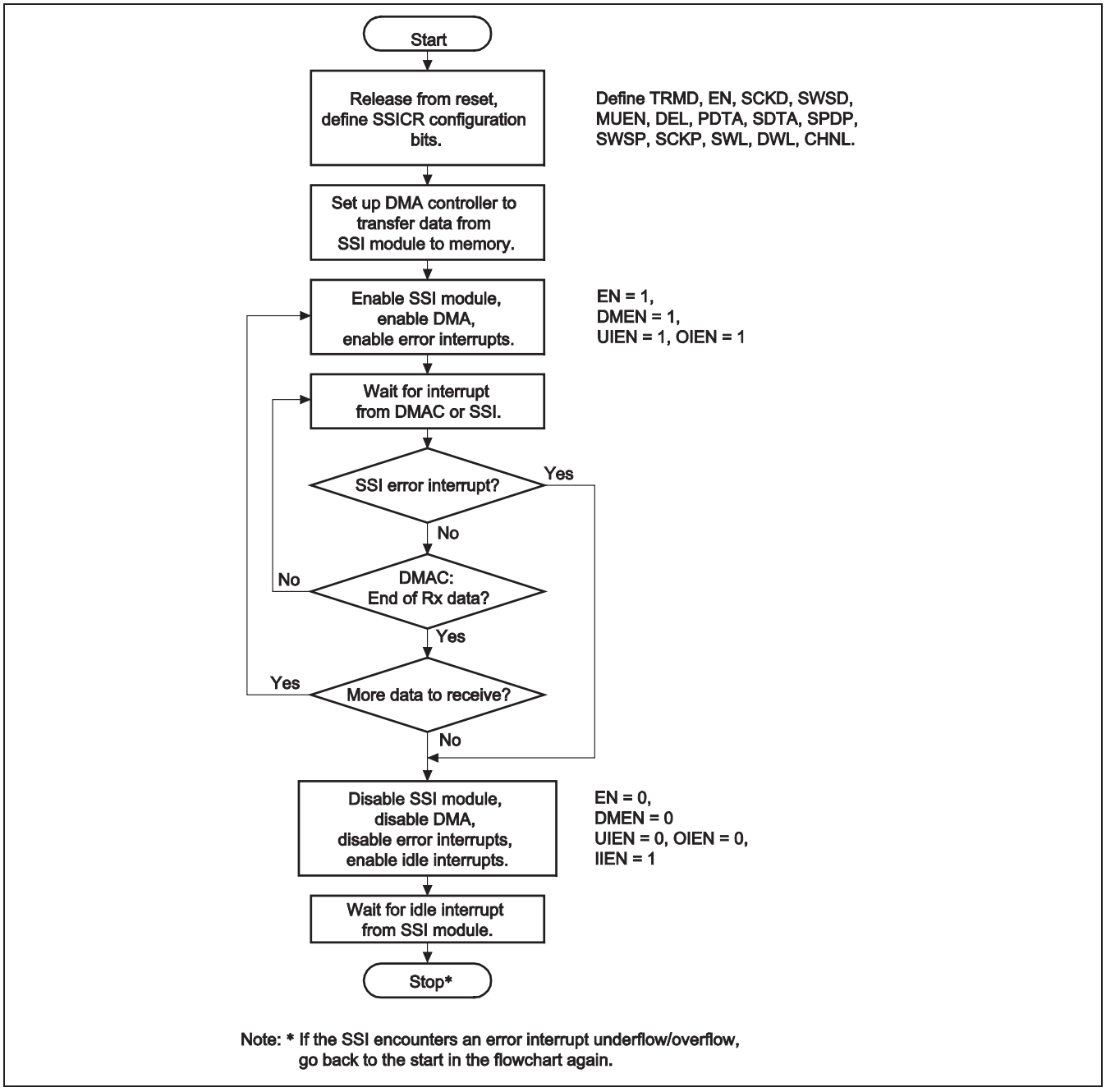


Figure 28A.40 Reception Using DMA Controller

(2) Reception using interrupt data flow control

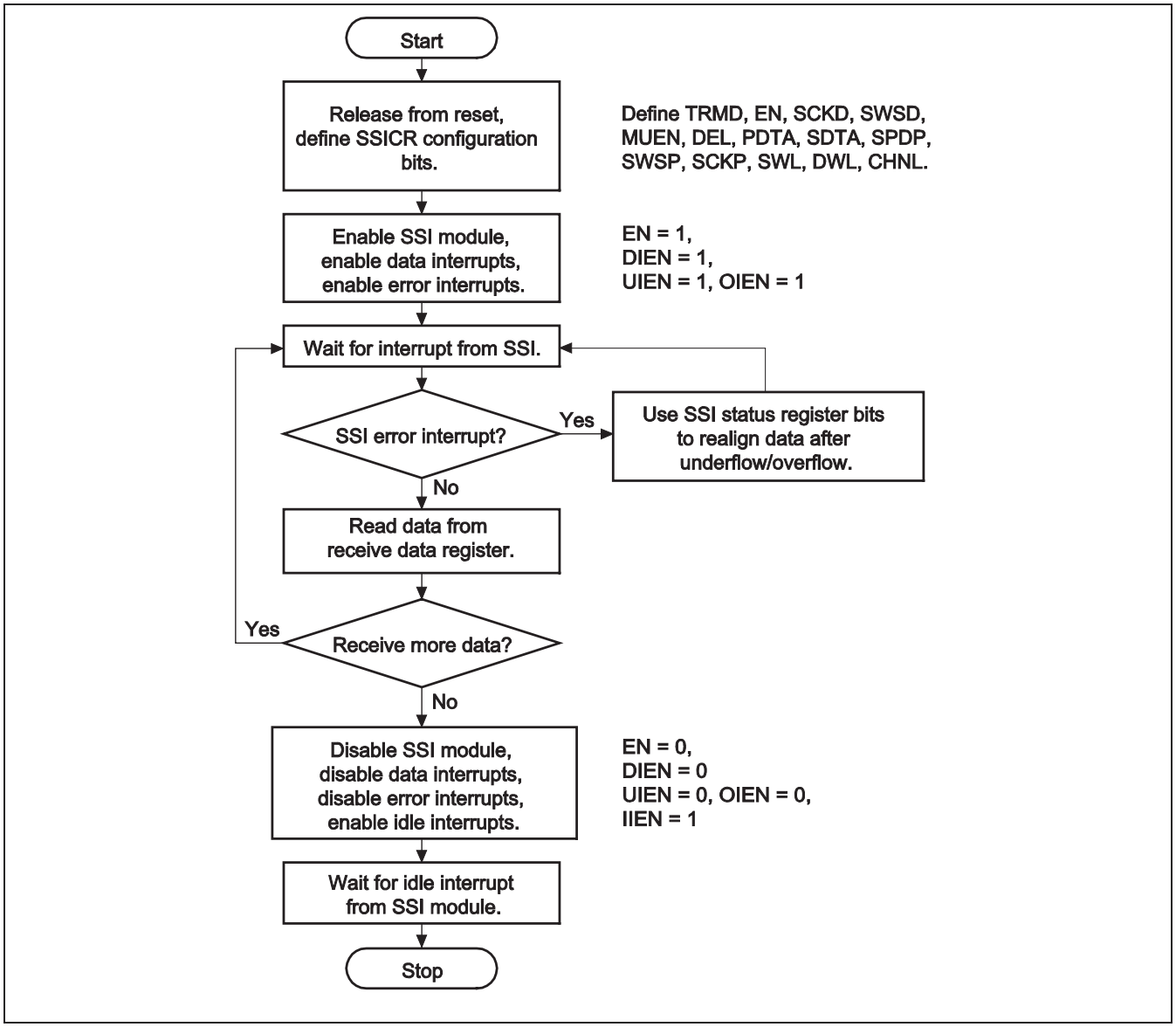


Figure 28A.41 Reception Using Interrupt Data Flow Control

28A.3.5 Serial Bit Clock Control

This function is used to control and select which clock is used for the serial bus interface.

If the serial clock direction is set to input (SSICR.SCKD = 0), the SSI module is in clock slave mode and the shift register uses the bit clock that was input to the SSI_SCK pin.

If the serial clock direction is set to output (SSICR.SCKD = 1), the SSI module is in clock master mode, and the shift register uses the bit clock that is input from the CLK_FS pin or the bit clock that is obtained by dividing the input from the CLK_FS pin. In the latter case, the clock input from the CLK_FS pin is divided by the ratio in the serial oversampling clock divide ratio (CKDV) in SSICR and used as the bit clock in the shift register.

In either case, the SSI_SCK pin output is the same as the bit clock.

28A.4 Usage Notes

28A.4.1 Limitations from Overflow during Receive DMA Operation

If an overflow occurs while the receive DMA is in operation, the module should be restarted. The receive buffer in the SSI consists of 32-bit registers that share the L and R channels. Therefore, data to be received at the L channel may sometimes be received at the R channel if an overflow occurs, for example, under the following condition: the control register (SSICR) has a 32-bit setting for both data word length (DWL2 to DWL0) and system word length (SWL2 to SWL).

If an overflow is confirmed with the overflow error interrupt or overflow error status flag (SSISR. OIRQ), write 0 to the EN and DMEN bits in SSICR to disable DMA in the SSI module, thus stopping the operation (In this case, the controller setting should also be stopped). After this, write 0 to the OIRQ bit in SSISR to clear the overflow status, set DMA again and restart the transfer.

28A.4.2 Limitations on Combinations of Modes Related to Common Pins to SSI7 and SSI8

Table 28A.5 shows the available combinations of operating modes for SSI7 and SSI8. Operating modes can be set with the control registers for the SSI7 and SSI8 (SSICR).

Table 28A.5 Usable Operating Mode Combinations for SSI7 and SSI8

	Operating Mode		Operating Mode of External Device		
No.	SSI7	SSI8	SSI7 Side	SSI8 Side	Function
1	Slave	Slave	Master	Slave	SSI7 and SSI8 operate synchronously with SSI_WS78_A/B and SSI_SCK78_A/B input.
			Slave	Master	
			Slave	Slave	
2	Master	Slave	Slave	Slave	SSI8 and an external device operate synchronously with WS and SCK of SSI7.
3	Slave	Master	—	—	Setting prohibited
4	Master	Master	—	—	Setting prohibited

There are the following limitations on the operating mode combinations shown in Table 28A.5.

For No. 1, SSI_WS78_A/B and SSI_SCK78_A/B should be input before either of SSI7 or SSI8 starts data transfer.

For No. 2, the SSI7 as the master should start transfer first thus allowing SSI_WS78_A/B and SSI_SCK78_A/B to be output, and then the SSI8 as the slave should be used. If the master-side transfer is stopped with the CONT bit in SSIWSR being 0, the slave-side SSI8 should be stopped because SSI_WS78_A/B is not output.

28A.4.3 Limitations on Slave Mode Operation

When this LSI is used in slave mode, in ending a data transfer process, data transfer on this LSI should be stopped (SSICR.EN = 0) before the input word selection signal (SSI_WS) is stopped.

In slave mode, data transfer is stopped by clearing the EN bit in SSICR (setting to stop transfer) and detecting the falling edge of the word selection signal (SSI_WS). If the input word selection signal is stopped first, the falling edge of the word selection signal cannot be detected and data transfer cannot be ended successfully.

28A.4.4 Limitations on Changes to Settings

The SSI_SCK and SSI_WS signals are not guaranteed immediately after changes of the WS mode bit in the WS Mode Register (SSIWSR) and configuration bits in the control register (SSICR). Settings must not be changed dynamically if this would affect any connected device.

28A.4.5 Stopping or Resuming Transmission

Follow the procedure below to stop or resume transmission.

Stopping transmission:

1. Set the DMEN bit in SSICR to 0 for stopping transmission.
2. Wait for SSISR.DIRQ = 1 by using polling or interrupts.
3. Set the EN bit in SSICR to 0 to stop transmission.
4. Check that SSISR.IDST is 1.

Resuming transmission:

Set DMEN and EN bits in SSICR to 1 for resuming transmission (The DMEN bit should be set to 1 at the same time of or before the EN bit).

29. Audio Clock Generator (ADG)

29.1 Overview

The audio clock generator (ADG) selects and supplies the necessary clock for the SSI or SCU module. It also divides the frequency of the selected clock and sends it outside the chip.

29.1.1 Features

- Selects the clock signal from the AUDIO_CLKA, AUDIO_CLKB or AUDIO_CLKC pin or the internal clock and supplies it to the SSI or SCU module.
- The frequency of the clock signals from the AUDIO_CLKA, AUDIO_CLKB or AUDIO_CLKC pins and the internal clock can be divided before use.
- The divided clock can be output through the AUDIO_CLKOUT pin.

29.1.2 Block Diagram

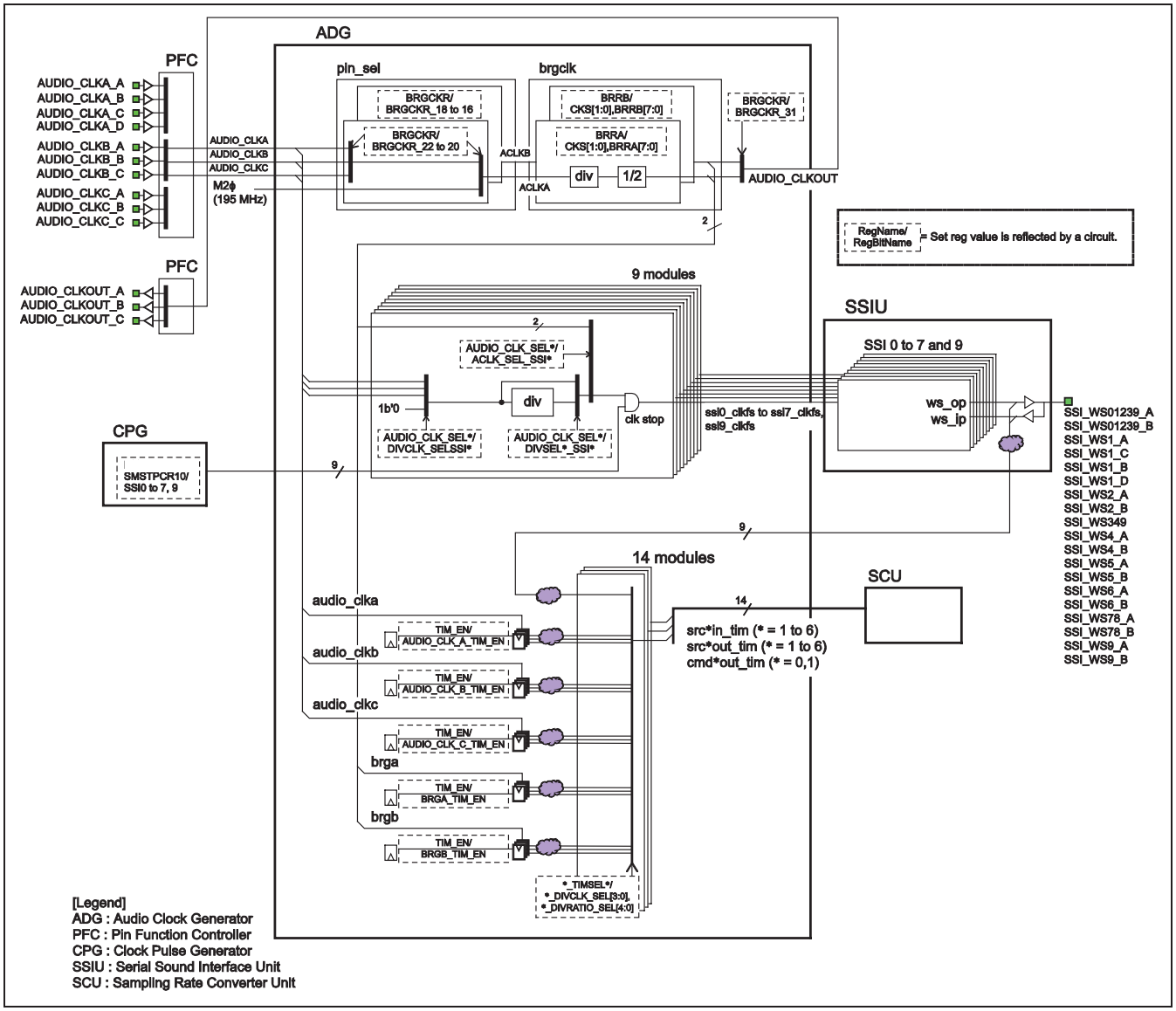


Figure 29.1 Block Diagram

29.1.3 Input/Output Pins

Table 29.1 Pin Configuration

Pin Name	I/O	Function
AUDIO_CLKA_A	Input	AUDIO CLOCK A
AUDIO_CLKA_B	Input	AUDIO CLOCK A
AUDIO_CLKA_C	Input	AUDIO CLOCK A
AUDIO_CLKA_D	Input	AUDIO CLOCK A
AUDIO_CLKB_A	Input	AUDIO CLOCK B
AUDIO_CLKB_B	Input	AUDIO CLOCK B
AUDIO_CLKB_C	Input	AUDIO CLOCK B
AUDIO_CLKC_A	Input	AUDIO CLOCK C
AUDIO_CLKC_B	Input	AUDIO CLOCK C
AUDIO_CLKC_C	Input	AUDIO CLOCK C
AUDIO_CLKOUT_A	Output	AUDIO CLOCK OUT
AUDIO_CLKOUT_B	Output	AUDIO CLOCK OUT
AUDIO_CLKOUT_C	Output	AUDIO CLOCK OUT

29.1.4 Register Configuration

Table 29.2 shows the register configuration. The base address is H'EC5A_0000. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

Table 29.2 Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access size
BRGA Baud Rate Setting Register	BRRA	R/W	H'000	H'0000 00FF	32
BRGB Baud Rate Setting Register	BRRB	R/W	H'004	H'0000 00FF	32
BRG Clock Select Register	BRGCKR	R/W	H'008	H'2300 0000	32
Audio Clock Select Register 0	AUDIO_CLK_SEL0	R/W	H'00C	H'0000 0000	32
Audio Clock Select Register 1	AUDIO_CLK_SEL1	R/W	H'010	H'0000 0000	32
Audio Clock Select Register 2	AUDIO_CLK_SEL2	R/W	H'014	H'0000 0000	32
Timing Signal Enable Register	TIM_EN	R/W	H'030	H'0000 0000	32
SRC Input Timing Select Register 0	SRCIN_TIMSEL0	R/W	H'034	H'0000 0000	32
SRC Input Timing Select Register 1	SRCIN_TIMSEL1	R/W	H'038	H'0000 0000	32
SRC Input Timing Select Register 2	SRCIN_TIMSEL2	R/W	H'03C	H'0000 0000	32
SRC Input Timing Select Register 3	SRCIN_TIMSEL3	R/W	H'040	H'0000 0000	32
SRC Input Timing Select Register 4	SRCIN_TIMSEL4	R/W	H'044	H'0000 0000	32
SRC Output Timing Select Register 0	SRCOUT_TIMSEL0	R/W	H'048	H'0000 0000	32
SRC Output Timing Select Register 1	SRCOUT_TIMSEL1	R/W	H'04C	H'0000 0000	32
SRC Output Timing Select Register 2	SRCOUT_TIMSEL2	R/W	H'050	H'0000 0000	32
SRC Output Timing Select Register 3	SRCOUT_TIMSEL3	R/W	H'054	H'0000 0000	32
SRC Output Timing Select Register 4	SRCOUT_TIMSEL4	R/W	H'058	H'0000 0000	32
CMD Output Timing Select Register	CMDOUT_TIMSEL	R/W	H'05C	H'0000 0000	32

Note: * Some restrictions apply.

29.2 Register Descriptions

[Legend for Register Description]

Initial value: Register value after a reset.

—: Undefined value

R/W: Bit or field is readable and writable. The written value can be read.

All registers are accessed in longword units.

29.2.1 BRGA Baud Rate Setting Register (BRRA)

Function: BRRA is a 32-bit readable/writable register that specifies the baud rate for ACLK_A (see Table 29.3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CKS[1:0]		BRRA[7:0]							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
9, 8	CKS[1:0]	B'00	R/W	These bits specify the clock source for the on-chip baud rate generator. 00: ACLK_A 01: ACLK_A/4 10: ACLK_A/16 11: ACLK_A/64
7 to 0	BRRA[7:0]	H'FF	R/W	These bits specify the division ratio. For details, see Table 29.3.

Table 29.3 Division Ratio for BRGA

BRGA Operating Clock (CKS[1], CKS[0])	Division Ratio BRRA (N = 0 to 255)	Calculating Formula
ACLK_A	1/2, 1/4, 1/6, ..., 1/512	1 / (2(N + 1))
ACLK_A/4	1/8, 1/16, 1/24, ..., 1/2048	1 / (8(N + 1))
ACLK_A/16	1/32, 1/64, 1/96, ..., 1/8192	1 / (32(N + 1))
ACLK_A/64	1/128, 1/256, 1/384, ..., 1/32768	1 / (128(N + 1))

Note: Use the output of BRGA in less than 25 MHz.

29.2.2 BRGB Baud Rate Setting Register (BRRB)

Function: BRRB is a 32-bit readable/writable register that specifies the baud rate for ACLK_B (see Table 29.4).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CKS[1:0]		BRRB[7:0]							
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
9, 8	CKS[1:0]	B'00	R/W	These bits specify the clock source for the on-chip baud rate generator. 00: ACLK_B 01: ACLK_B/4 10: ACLK_B/16 11: ACLK_B/64
7 to 0	BRRB[7:0]	H'FF	R/W	These bits specify the division ratio. For details, see Table 29.4.

Table 29.4 Division Ratio for BRGB

BRGB Operating Clock (CKS[1], CKS[0])	Division Ratio BRRB (N = 0 to 255)	Calculating Formula
ACLK_B	1/2, 1/4, 1/6, ..., 1/512	1 / (2(N + 1))
ACLK_B/4	1/8, 1/16, 1/24, ..., 1/2048	1 / (8(N + 1))
ACLK_B/16	1/32, 1/64, 1/96, ..., 1/8192	1 / (32(N + 1))
ACLK_B/64	1/128, 1/256, 1/384, ..., 1/32768	1 / (128(N + 1))

Note: Use the output of BRGB in less than 25 MHz.

29.2.3 BRG Clock Select Register (BRGCKR)

Function: BRGCKR selects the clocks input to and output from the ADG.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BRGCKR_31	—	—	—	—	—	—	—	—	BRGCKR_22	BRGCKR_21	BRGCKR_20	—	BRGCKR_18	BRGCKR_17	BRGCKR_16
Initial value:	0	0	1	0	0	0	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	BRGCKR_31	B'0	R/W	This bit selects the clock signal output to the AUDIO_CLKOUT_A, AUDIO_CLKOUT_B or AUDIO_CLKOUT_C external pin. 0: BRGA output clock 1: BRGB output clock
30 to 23	—	H'46	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
22 21 20	BRGCKR_22 BRGCKR_21 BRGCKR_20	B'0 B'0 B'0	R/W	These bits select the clock signal input to the BRGA. 000: AUDIO_CLKA 001: AUDIO_CLKB 01x: M2ϕ (195 MHz) 100: AUDIO_CLKC 101: Fixed at 0 11x: Fixed at 0 x = Don't care
19	—	B'0	R	Reserved The initial value is always read from this bit. The write value should always be the initial value.
18 17 16	BRGCKR_18 BRGCKR_17 BRGCKR_16	B'0 B'0 B'0	R/W	These bits select the clock signal input to the BRGB. 000: AUDIO_CLKA 001: AUDIO_CLKB 01x: M2ϕ (195 MHz) 100: AUDIO_CLKC 101: Fixed at 0 11x: Fixed at 0 x = Don't care
15 to 0	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.

29.2.4 Audio Clock Select Register 0 (AUDIO_CLK_SEL0)

Function: AUDIO_CLK_SEL0 selects the clocks for the SSIU (for SSI0 to SSI3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIVSEL_SSI3 [1:0]		ACLK_SEL _SSI3[1:0]		DIVSEL 2_SSI3	DIVCLK_SEL_SSI3 [2:0]			DIVSEL_SSI2 [1:0]		ACLK_SEL _SSI2[1:0]		DIVSEL 2_SSI2	DIVCLK_SEL_SSI2 [2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVSEL_SSI1 [1:0]		ACLK_SEL _SSI1[1:0]		DIVSEL 2_SSI1	DIVCLK_SEL_SSI1 [2:0]			DIVSEL_SSI0 [1:0]		ACLK_SEL _SSI0[1:0]		DIVSEL 2_SSI0	DIVCLK_SEL_SSI0 [2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	DIVSEL_SSI3[1:0]	B'00	R/W	SSI3 Frequency Divider Select
27	DIVSEL2_SSI3	B'0	R/W	[27], [31:30]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
29, 28	ACLK_SEL_SSI3[1:0]	B'00	R/W	SSI3 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
26 to 24	DIVCLK_SEL_SSI3 [2:0]	B'000	R/W	SSI3 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting prohibited
23, 22	DIVSEL_SSI2[1:0]	B'00	R/W	SSI2 Frequency Divider Select
19	DIVSEL2_SSI2	B'0	R/W	[19], [23:22]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0

Bit	Bit Name	Initial Value	R/W	Description
21, 20	ACLK_SEL_SSI2[1:0]	B'00	R/W	SSI2 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
18 to 16	DIVCLK_SEL_SSI2 [2:0]	B'000	R/W	SSI2 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
15, 14	DIVSEL_SSI1[1:0]	B'00	R/W	SSI1 Frequency Divider Select
11	DIVSEL2_SSI1	B'0	R/W	[11], [15:14]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
13, 12	ACLK_SEL_SSI1[1:0]	B'00	R/W	SSI1 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
10 to 8	DIVCLK_SEL_SSI1 [2:0]	B'000	R/W	SSI1 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
7, 6	DIVSEL_SSI0[1:0]	B'00	R/W	SSI0 Frequency Divider Select
3	DIVSEL2_SSI0	B'0	R/W	[3], [7:6]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
5, 4	ACLK_SEL_SSI0[1:0]	B'00	R/W	SSI0 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	DIVCLK_SEL_SSI0 [2:0]	B'000	R/W	SSI0 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited

29.2.5 Audio Clock Select Register 1 (AUDIO_CLK_SEL1)

Function: AUDIO_CLK_SEL1 selects the clocks for the SSIU (for SSI4 to SSI7).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIVSEL_SSI7 [1:0]		ACLK_SEL _SSI7[1:0]		DIVSEL 2_SSI7	DIVCLK_SEL_SSI7 [2:0]			DIVSEL_SSI6 [1:0]		ACLK_SEL _SSI6[1:0]		DIVSEL 2_SSI6	DIVCLK_SEL_SSI6 [1:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVSEL_SSI5 [1:0]		ACLK_SEL _SSI5[1:0]		DIVSEL 2_SSI5	DIVCLK_SEL_SSI5 [2:0]			DIVSEL_SSI4 [1:0]		ACLK_SEL _SSI4[1:0]		DIVSEL 2_SSI4	DIVCLK_SEL_SSI4 [1:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	DIVSEL_SSI7[1:0]	B'00	R/W	SSI7 Frequency Divider Select
27	DIVSEL2_SSI7	B'0	R/W	[27], [31:30]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
29, 28	ACLK_SEL_SSI7[1:0]	B'00	R/W	SSI7 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
26 to 24	DIVCLK_SEL_SSI7 [2:0]	B'000	R/W	SSI7 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
23, 22	DIVSEL_SSI6[1:0]	B'00	R/W	SSI6 Frequency Divider Select
19	DIVSEL2_SSI6	B'0	R/W	[19], [23:22]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0

Bit	Bit Name	Initial Value	R/W	Description
21, 20	ACLK_SEL_SSI6[1:0]	B'00	R/W	SSI6 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
18 to 16	DIVCLK_SEL_SSI6 [2:0]	B'000	R/W	SSI6 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
15, 14	DIVSEL_SSI5[1:0]	B'00	R/W	SSI5 Frequency Divider Select
11	DIVSEL2_SSI5	B'0	R/W	[11], [15:14]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
13, 12	ACLK_SEL_SSI5[1:0]	B'00	R/W	SSI5 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
10 to 8	DIVCLK_SEL_SSI5 [2:0]	B'000	R/W	SSI5 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
7, 6	DIVSEL_SSI4[1:0]	B'00	R/W	SSI4 Frequency Divider Select
3	DIVSEL2_SSI4	B'0	R/W	[3], [7:6]: 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
5, 4	ACLK_SEL_SSI4[1:0]	B'00	R/W	SSI4 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	DIVCLK_SEL_SSI4 [2:0]	B'000	R/W	SSI4 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited

29.2.6 Audio Clock Select Register 2 (AUDIO_CLK_SEL2)

Function: AUDIO_CLK_SEL2 selects the clocks for the SSIU (for SSI9).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DIVSEL_SSI9 [1:0]		ACLK_SEL _SSI9[1:0]		DIVSEL 2_SSI9	DIVCLK_SEL_SSI9 [2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.
15, 14 11	DIVSEL_SSI9[1:0] DIVSEL2_SSI9	B'00 B'0	R/W R/W	SSI9 Frequency Divider Select [11], [15:14] 000: Not divided 001: Divided by 2 010: Divided by 4 011: Divided by 8 100: Divided by 16 101: Divided by 32 110, 111: Fixed at 0
13, 12	ACLK_SEL_SSI9[1:0]	B'00	R/W	SSI9 Clock Select 00: DIVCLK 01: BRGA output clock 10: BRGB output clock 11: Setting prohibited
10 to 8	DIVCLK_SEL_SSI9[2:0]	B'000	R/W	SSI9 Clock Select 000: Fixed at 0 001: AUDIO_CLKA 010: AUDIO_CLKB 011: AUDIO_CLKC Others: Setting Prohibited
7 to 0	—	All 0	R	Reserved The initial value is always read from these bits. The write value should always be the initial value.

29.2.7 Timing Signal Enable Register (TIM_EN)

Function: TIM_EN is enabling of the Timing Signal supplied to SCU.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BRGB_TIM_EN	BRGA_TIM_EN	AUDIO_CLKC_TIM_EN	AUDIO_CLKB_TIM_EN	AUDIO_CLKA_TIM_EN	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved The initial value is always read from this bit. The write value should always be the initial value.
5	BRGB_TIM_EN	B'0	R/W	This bit is enabling of the Timing Signal generated from the BRGB frequency divider. 0: Disables timing signal. 1: Enables timing signal.
4	BRGA_TIM_EN	B'0	R/W	This bit is enabling of the Timing Signal generated from the BRGA frequency divider. 0: Disables timing signal. 1: Enables timing signal.
3	AUDIO_CLKC_TIM_EN	B'0	R/W	This bit is enabling of the Timing Signal generated from the AUDIO_CLKC frequency divider. 0: Disables timing signal. 1: Enables timing signal.
2	AUDIO_CLKB_TIM_EN	B'0	R/W	This bit is enabling of the Timing Signal generated from the AUDIO_CLKB frequency divider. 0: Disables timing signal. 1: Enables timing signal.
1	AUDIO_CLKA_TIM_EN	B'0	R/W	This bit is enabling of the Timing Signal generated from the AUDIO_CLKA frequency divider. 0: Disables timing signal. 1: Enables timing signal.
0	—	B'0	R/W	Reserved The write value should always be the initial value.

29.2.8 SRC Input Timing Select Register 0 (SRCIN_TIMSEL0)

Function: SRCIN_TIMSEL0 selects the input timing signals for SRC1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SRC1_IN_DIVCLK_SEL[3:0]				—	—	—	SRC1_IN_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC1_IN_DIVCLK_SEL [3:0]	B'0000	R/W	SRC1 Input Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC1_IN_DIVRATIO_SEL [4:0]	B'00000	R/W	SRC1 Input Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC1_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 0	—	All 0	R/W	Reserved The write value should always be the initial value.

29.2.9 SRC Input Timing Select Register 1 (SRCIN_TIMSEL1)

Function: SRCIN_TIMSEL1 selects the input timing signals for SRC2 and SRC3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SRC3_IN_DIVCLK_SEL[3:0]				—	—	—	SRC3_IN_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SRC2_IN_DIVCLK_SEL[3:0]				—	—	—	SRC2_IN_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC3_IN_DIVCLK_SEL [3:0]	B'0000	R/W	SRC3 Input Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

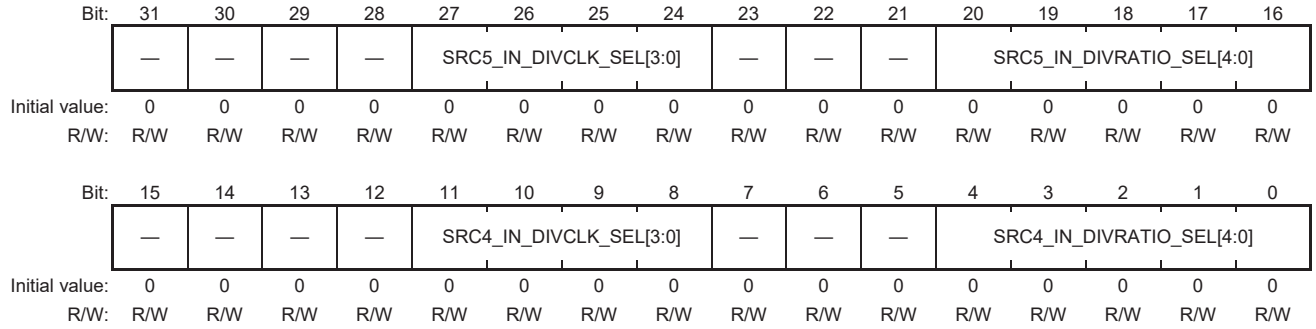
Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC3_IN_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC3 Input Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC3_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC2_IN_DIVCLK_SEL [3:0]	B'0000	R/W	SRC2 Input Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC2_IN_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC2 Input Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC2_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.2.10 SRC Input Timing Select Register 2 (SRCIN_TIMSEL2)

Function: SRCIN_TIMSEL2 selects the input timing signals for SRC4 and SRC5.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC5_IN_DIVCLK_SEL [3:0]	B'0000	R/W	SRC5 Input Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC5_IN_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC5 Input Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC5_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC4_IN_DIVCLK_SEL [3:0]	B'0000	R/W	SRC4 Input Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC4_IN_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC4 Input Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC4_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.2.11 SRC Input Timing Select Register 3 (SRCIN_TIMSEL3)

Function: SRCIN_TIMSEL3 selects the input timing signals for SRC6.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SRC6_IN_DIVCLK_SEL[3:0]				—	—	—	SRC6_IN_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.
11 to 8	SRC6_IN_DIVCLK_SEL [3:0]	B'0000	R/W	SRC6 Input Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC6_IN_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC6 Input Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC6_IN_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.2.12 SRC Output Timing Select Register 0 (SRCOUT_TIMSEL0)

Function: SRCOUT_TIMSEL0 selects the output timing signals for SRC1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	SRC1_OUT_DIVCLK_SEL[3:0]				—	—	—	SRC1_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

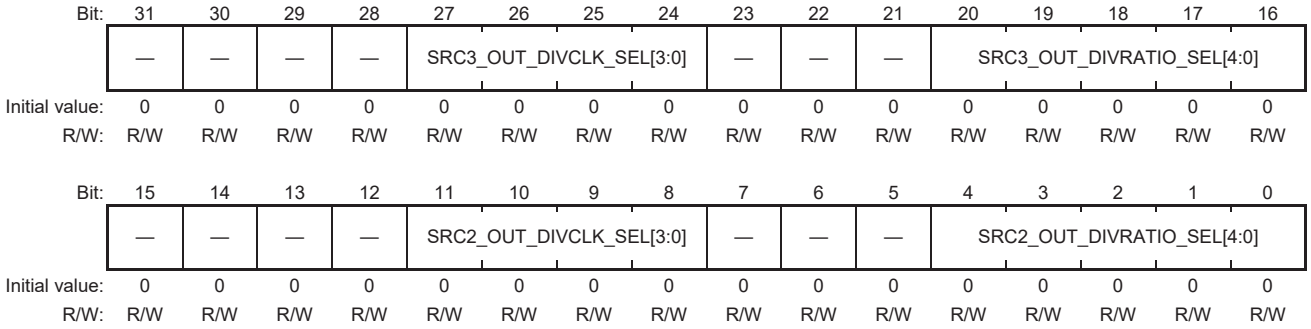
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC1_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	SRC1 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC1_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC1 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC1_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 0	—	All 0	R/W	Reserved The write value should always be the initial value.

29.2.13 SRC Output Timing Select Register 1 (SRCOUT_TIMSEL1)

Function: SRCOUT_TIMSEL1 selects the output timing signals for SRC2 and SRC3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC3_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	SRC3 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

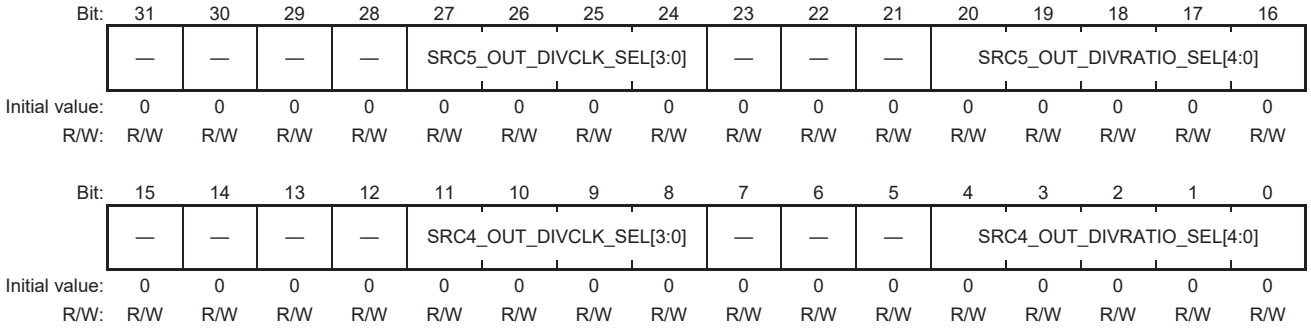
Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC3_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC3 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC3_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC2_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	SRC2 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC2_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC2 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC2_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.2.14 SRC Output Timing Select Register 2 (SRCOUT_TIMSEL2)

Function: SRCOUT_TIMSEL2 selects the output timing signals for SRC4 and SRC5.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	SRC5_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	SRC5 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	SRC5_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC5 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC5_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SRC4_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	SRC4 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC4_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC4 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC4_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.2.15 SRC Output Timing Select Register 3 (SRCOUT_TIMSEL3)

Function: SRCOUT_TIMSEL3 selects the output timing signals for SRC6.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	SRC6_OUT_DIVCLK_SEL[3:0]				—	—	—	SRC6_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.
11 to 8	SRC6_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	SRC6 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	SRC6_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	SRC6 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using SRC6_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.2.16 CMD Output Timing Select Register (CMDOUT_TIMSEL)

Function: CMDOUT_TIMSEL selects the output timing signals for CMD0 and CMD1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	CMD1_OUT_DIVCLK_SEL[3:0]				—	—	—	CMD1_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	CMD0_OUT_DIVCLK_SEL[3:0]				—	—	—	CMD0_OUT_DIVRATIO_SEL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved The write value should always be the initial value.
27 to 24	CMD1_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	CMD1 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
23 to 21	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
20 to 16	CMD1_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	CMD1 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using CMD1_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited
15 to 12	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	CMD0_OUT_DIVCLK_SEL [3:0]	B'0000	R/W	CMD0 Output Timing Signal Select 0000: Divided AUDIO_CLKA 0001: Divided AUDIO_CLKB 0010: Divided AUDIO_CLKC 0011: Divided BRGA 0100: Divided BRGB 0101: Setting prohibited 0110: ssi_ws0 0111: ssi_ws1 1000: ssi_ws2 1001: ssi_ws3 1010: ssi_ws4 1011: ssi_ws5 1100: ssi_ws6 1101: ssi_ws7 1110: ssi_ws9 1111: Setting prohibited
7 to 5	—	All 0	R/W	Reserved The write value should always be the initial value.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	CMD0_OUT_DIVRATIO_SEL[4:0]	B'00000	R/W	CMD0 Output Timing Signal Frequency Division Ratio Select These bits select the frequency division ratio for the clock signal selected using CMD0_OUT_DIVCLK_SEL[3:0]. Note that ssi_ws signals cannot be divided. 0_0000: Divided by 2 0_0001: Divided by 4 0_0010: Divided by 6 0_0011: Divided by 8 0_0100: Divided by 12 0_0101: Divided by 16 0_0110: Divided by 24 0_0111: Divided by 32 0_1000: Divided by 48 0_1001: Divided by 64 0_1010: Divided by 96 0_1011: Divided by 128 0_1100: Divided by 192 0_1101: Divided by 256 0_1110: Divided by 384 0_1111: Divided by 512 1_0000: Divided by 768 1_0001: Divided by 1024 1_0010: Divided by 1536 1_0011: Divided by 2048 1_0100: Divided by 3072 1_0101: Divided by 4096 1_0110: Divided by 6144 1_0111: Divided by 8192 1_1000: Divided by 12288 1_1001: Divided by 16384 1_1010: Divided by 24576 1_1011: Divided by 32768 1_1100: Divided by 49152 1_1101: Divided by 98304 Others: Setting prohibited

29.3 Operation

The following sections give examples of setting the ADG registers.

(1) Supplying SSI3 with Audio Clock

The following procedure can be used to divide the internal clock (195-MHz) by d'18 and supply the resulting BRGB clock (10.833-MHz) to SSI3. (If the procedure is applied before starting SSI3, steps 1 to 5 can be executed in any order.)

1. Set BRRB so that the frequency division ratio should be d'18.
2. Select internal clock (M2ϕ) as the clock to be input to BRGB using BRGCKR.
3. Select the BRGB output clock as SSI3 clock using AUDIO_CLK_SEL0.
4. Release the ADG from the module standby state using SMSTPCR1 of the CPG module.
5. Release SSI3 from the module standby state using SMSTPCR10 of the CPG module.

Table 29.5 Setting Example 1

Register Name	Address	Setting Value	Description
BRRB	H'EC5A 0004	H'0000 0008	Divided by d'18
BRGCKR	H'EC5A 0008	H'2302 0000	Selects M2ϕ as the clock to be input to BRGB.
AUDIO_CLK_SEL0	H'EC5A 000C	H'2000 0000	Selects the BRGB output clock as the clock to be output to SSI3.
SMSTPCR1	H'E615 0134	Set bit 6 to 0.	Releases the ADG from the module standby state.
SMSTPCR10	H'E615 0998	Set bits 12 to 0.	Releases the SSI3 from the module standby state.

29.4 Usage Notes

There is no attention of the usage.

30. Sampling Rate Converter Unit (SCU)

30.1 Overview

The SCU has six SRC modules (four for high-sound-quality type; two for general-sound-quality type) that are useful for synchronization of asynchronous data, which is necessary for data transfer with external memory or external devices. It also provides the functions to change the number of channels, perform mixing, and control the volume.

Note: When the SRCs are not in use, configure the system with the same clock sources for AUDIO CLOCK that is input to ADG, and INIC or devices for I2S that are connected to external modules, and all thus operate at the same sampling frequency.

30.1.1 Features

(1) Sampling Rate Converter (SRC)

- Asynchronous sampling rate conversion is available
- Supports resolutions up to 24 bits
- High-sound-quality type (THD + N* is -132 dB) and general-sound-quality type (THD + N* is -96 dB)
- Automatically generates antialiasing filter coefficients
- Three modules support one, two, four, six, or eight channels, and three modules support one or two channels.

Note: * Total harmonic distortion plus noise

(2) Channel Transfer Unit (CTU)

- Downmixing and splitter functions
  - Conversion of eight input channels into two output channels
  - Conversion of six input channels into two output channels
  - Conversion of two input channels into four sets of two output channels
  - Conversion of one input channel into eight sets of one output channel
  - No conversion

(3) Mixer (MIX)

- Mixing (adds) two to four sources into one
- Ratio for adding sources is selectable
- Ratio is dynamically changeable
- Mixing with volume ramp is available (ramp period is selectable)

(4) Digital Volume and Mute Function (DVC)

- Volume control function including digital volume, volume ramp, and zero-crossing mute
- The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute or -120 to 18 dB)
- The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment
- The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2
- The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

The CTU, MIX, and DVC functional blocks are collectively called "CMD".

30.1.2 Block Diagram

Figure 30.1 shows the SCU block diagram.

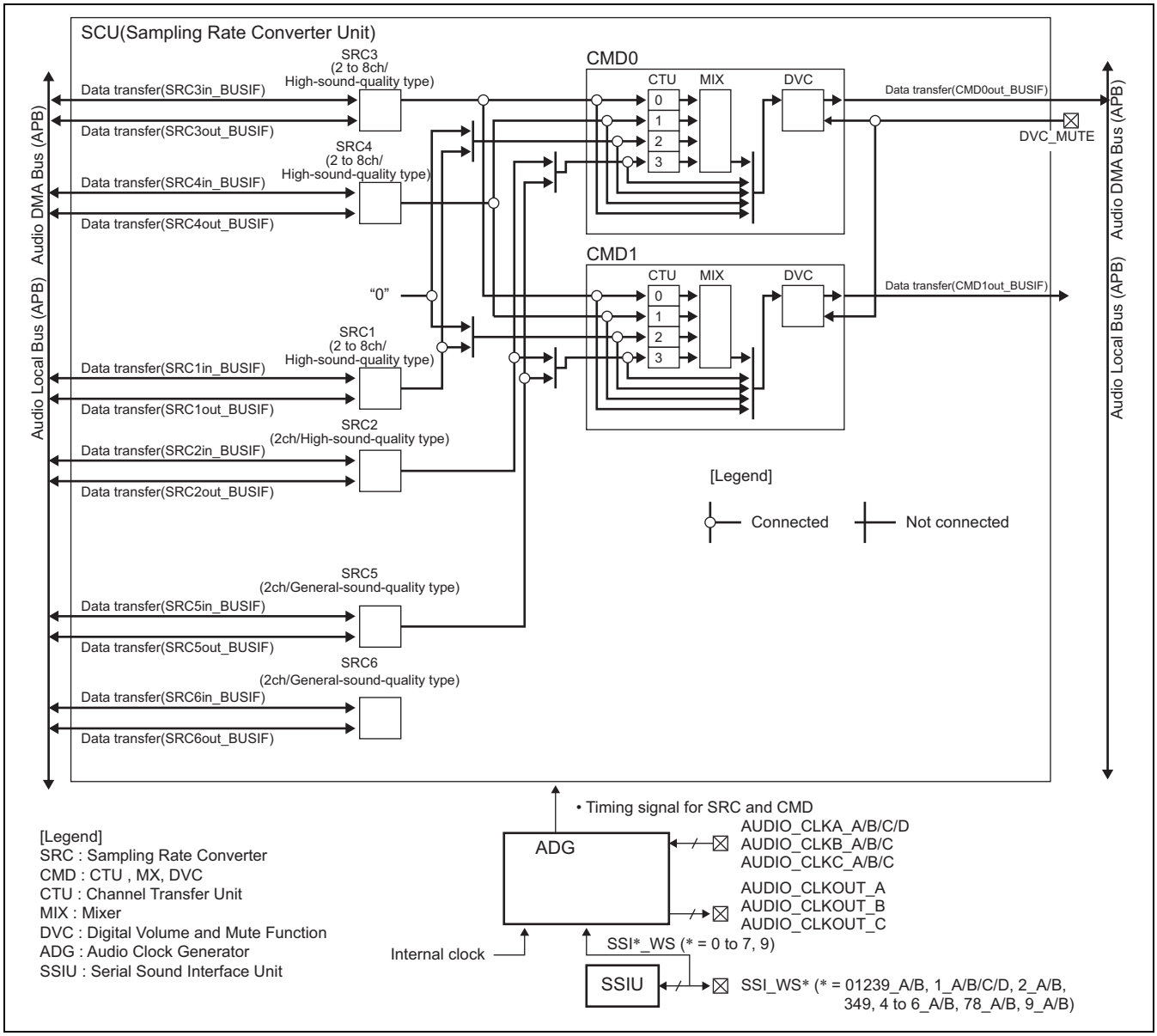


Figure 30.1 Block Diagram of SCU

30.1.3 Input/Output Pins

Table 30.1 shows the pin configuration.

Table 30.1 Pin Configuration

Name	Pin Name	I/O	Function
DVC_MUTE pin	DVC_MUTE	Input	DVCEN

30.1.4 Register Configuration

Table 30.2 shows the register configuration. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined. Access the register as a longword (32 bits). Operation cannot be guaranteed if the register is not accessed as a longword.

Table 30.2 Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
SRC1in_BUSIF_MODE Register	SRC1in_BUSIF_MODE	R/W	H'EC50 0020	H'0000 0001	32
SRC1out_BUSIF_MODE Register	SRC1out_BUSIF_MODE	R/W	H'EC50 0024	H'0000 0001	32
SRC1_BUSIF_ DALIGN Register	SRC1_BUSIF_DALIGN	R/W	H'EC50 0028	H'7654 3210	32
SRC1_MODE Register	SRC1_MODE	R/W	H'EC50 002C	H'0000 0000	32
SRC1 Control Register	SRC1_CONTROL	R/W	H'EC50 0030	H'0000 0000	32
SRC1 Status Register	SRC1_STATUS	R	H'EC50 0034	H'0000 0000	32
SRC1 Interrupt Enable Register 0	SRC1_INT_ENABLE0	R/W	H'EC50 0038	H'0000 0000	32
SRC2in_BUSIF_MODE Register	SRC2in_BUSIF_MODE	R/W	H'EC50 0040	H'0000 0001	32
SRC2out_BUSIF_MODE Register	SRC2out_BUSIF_MODE	R/W	H'EC50 0044	H'0000 0001	32
SRC2_BUSIF_ DALIGN Register	SRC2_BUSIF_DALIGN	R/W	H'EC50 0048	H'0000 0010	32
SRC2_MODE Register	SRC2_MODE	R/W	H'EC50 004C	H'0000 0000	32
SRC2 Control Register	SRC2_CONTROL	R/W	H'EC50 0050	H'0000 0000	32
SRC2 Status Register	SRC2_STATUS	R	H'EC50 0054	H'0000 0000	32
SRC2 Interrupt Enable Register 0	SRC2_INT_ENABLE0	R/W	H'EC50 0058	H'0000 0000	32
SRC3in_BUSIF_MODE Register	SRC3in_BUSIF_MODE	R/W	H'EC50 0060	H'0000 0001	32
SRC3out_BUSIF_MODE Register	SRC3out_BUSIF_MODE	R/W	H'EC50 0064	H'0000 0001	32
SRC3_BUSIF_DALIGN Register	SRC3_BUSIF_DALIGN	R/W	H'EC50 0068	H'7654 3210	32
SRC3_MODE Register	SRC3_MODE	R/W	H'EC50 006C	H'0000 0000	32
SRC3 Control Register	SRC3_CONTROL	R/W	H'EC50 0070	H'0000 0000	32
SRC3 Status Register	SRC3_STATUS	R	H'EC50 0074	H'0000 0000	32
SRC3 Interrupt enable Register 0	SRC3_INT_ENABLE0	R/W	H'EC50 0078	H'0000 0000	32
SRC4in_BUSIF_MODE Register	SRC4in_BUSIF_MODE	R/W	H'EC50 0080	H'0000 0001	32
SRC4out_BUSIF_MODE Register	SRC4out_BUSIF_MODE	R/W	H'EC50 0084	H'0000 0001	32
SRC4_BUSIF_ DALIGN Register	SRC4_BUSIF_DALIGN	R/W	H'EC50 0088	H'7654 3210	32
SRC4_MODE Register	SRC4_MODE	R/W	H'EC50 008C	H'0000 0000	32
SRC4 Control Register	SRC4_CONTROL	R/W	H'EC50 0090	H'0000 0000	32
SRC4 Status Register	SRC4_STATUS	R	H'EC50 0094	H'0000 0000	32
SRC4 Interrupt Enable Register 0	SRC4_INT_ENABLE0	R/W	H'EC50 0098	H'0000 0000	32
SRC5in_BUSIF_MODE Register	SRC5in_BUSIF_MODE	R/W	H'EC50 00A0	H'0000 0001	32
SRC5out_BUSIF_MODE Register	SRC5out_BUSIF_MODE	R/W	H'EC50 00A4	H'0000 0001	32
SRC5_BUSIF_ DALIGN Register	SRC5_BUSIF_DALIGN	R/W	H'EC50 00A8	H'0000 0010	32
SRC5_MODE Register	SRC5_MODE	R/W	H'EC50 00AC	H'0000 0000	32
SRC5 Control Register	SRC5_CONTROL	R/W	H'EC50 00B0	H'0000 0000	32
SRC5 Status Register	SRC5_STATUS	R	H'EC50 00B4	H'0000 0000	32
SRC5 Interrupt Enable Register 0	SRC5_INT_ENABLE0	R/W	H'EC50 00B8	H'0000 0000	32
SRC6in_BUSIF_MODE Register	SRC6in_BUSIF_MODE	R/W	H'EC50 00C0	H'0000 0001	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
SRC6out_BUSIF_MODE Register	SRC6out_BUSIF_MODE	R/W	H'EC50 00C4	H'0000 0001	32
SRC6_BUSIF_DALIGN Register	SRC6_BUSIF_DALIGN	R/W	H'EC50 00C8	H'0000 0010	32
SRC6_MODE Register	SRC6_MODE	R/W	H'EC50 00CC	H'0000 0000	32
SRC6 Control Register	SRC6_CONTROL	R/W	H'EC50 00D0	H'0000 0000	32
SRC6 Status Register	SRC6_STATUS	R	H'EC50 00D4	H'0000 0000	32
SRC6 Interrupt Enable Register 0	SRC6_INT_ENABLE0	R/W	H'EC50 00D8	H'0000 0000	32
CMD0out_BUSIF_MODE Register	CMD0out_BUSIF_MODE	R/W	H'EC50 0184	H'0000 0001	32
CMD0_BUSIF_DALIGN Register	CMD0_BUSIF_DALIGN	R/W	H'EC50 0188	H'7654 3210	32
CMD0_ROUTE_SELECT Register	CMD0_ROUTE_SELECT	R/W	H'EC50 018C	H'0000 0000	32
CMD0 Control Register	CMD0_CONTROL	R/W	H'EC50 0190	H'0000 0000	32
CMD1out_BUSIF_MODE Register	CMD1out_BUSIF_MODE	R/W	H'EC50 01A4	H'0000 0001	32
CMD1_BUSIF_DALIGN Register	CMD1_BUSIF_DALIGN	R/W	H'EC50 01A8	H'7654 3210	32
CMD1_ROUTE_SELECT Register	CMD1_ROUTE_SELECT	R/W	H'EC50 01AC	H'0000 0000	32
CMD1 Control Register	CMD1_CONTROL	R/W	H'EC50 01B0	H'0000 0000	32
SCU SYSTEM Status Register 0	SCU_SYSTEM_STATUS0	R/WC1	H'EC5001C8	H'0000 0000	32
SCU SYSTEM interrupt enable Register 0	SCU_SYSTEM_INT_ENABLE 0	R/W	H'EC5001CC	H'0000 0000	32
SCU SYSTEM Status Register 1	SCU_SYSTEM_STATUS1	R/WC1	H'EC5001D0	H'0000 0000	32
SCU SYSTEM Interrupt Enable Register 1	SCU_SYSTEM_INT_ENABLE 1	R/W	H'EC5001D4	H'0000 0000	32
SRC Registers	—	—	SRC1_BASE: H'EC50 0240	—	—
			SRC2_BASE: H'EC50 0280	—	—
			SRC3_BASE: H'EC50 02C0	—	—
			SRC4_BASE: H'EC50 0300	—	—
			SRC5_BASE: H'EC50 0340	—	—
			SRC6_BASE: H'EC50 0380	—	—
SRCm Software Reset Register	SRCm_SWRSR	R/W	SRCm_BASE + H'00	H'0000 0001	32
SRCm SRC Initialization Register	SRCm_SRCIR	R/W	SRCm_BASE + H'04	H'0000 0001	32
SRCm Audio Information Register	SRCm_ADINR	R/W	SRCm_BASE + H'14	H'0000 0000	32
SRCm IFS Control Register	SRCm_IFSCR	R/W	SRCm_BASE + H'1C	H'0000 0000	32
SRCm IFS Value Setting Register	SRCm_IFSVR	R/W	SRCm_BASE + H'20	H'0000 0000	32
SRCm SRC Control Register	SRCm_SRCCR	R/W	SRCm_BASE + H'24	H'0000 0000**	32
SRCm Buffer Size DATA RAM Setting Register	SRCm_BSDSR	R/W	SRCm_BASE + H'2C	H'0000 0000	32
SRCm Buffer Size IJEC RAM Setting Register	SRCm_BSISR	R/W	SRCm_BASE + H'38	H'0000 0000	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
CTU Registers	—	—	CTU00_BASE: H'EC50 0500 CTU01_BASE: H'EC50 0600 CTU02_BASE: H'EC50 0700 CTU03_BASE: H'EC50 0800 CTU10_BASE: H'EC50 0900 CTU11_BASE: H'EC50 0A00 CTU12_BASE: H'EC50 0B00 CTU13_BASE: H'EC50 0C00	—	—
CTUn Software Reset Register	CTUn_SWRSR	R/W	CTUn_BASE + H'00	H'0000 0001	32
CTUn CTU Initialization Register	CTUn_CTUIR	R/W	CTUn_BASE + H'04	H'0000 0001	32
CTUn Audio Information Register	CTUn_ADINR	R/W	CTUn_BASE + H'08	H'0000 0000	32
CTUn CTU Pass Mode Register	CTUn_CPMDR	R/W	CTUn_BASE + H'10	H'0000 0000	32
CTUn Scale Mode Register	CTUn_SCMDR	R/W	CTUn_BASE + H'14	H'0000 0000	32
CTUn Scale Value e00 Register	CTUn_SV00R	R/W	CTUn_BASE + H'18	H'0000 0000	32
CTUn Scale Value e01 Register	CTUn_SV01R	R/W	CTUn_BASE + H'1C	H'0000 0000	32
CTUn Scale Value e02 Register	CTUn_SV02R	R/W	CTUn_BASE + H'20	H'0000 0000	32
CTUn Scale Value e03 Register	CTUn_SV03R	R/W	CTUn_BASE + H'24	H'0000 0000	32
CTUn Scale Value e04 Register	CTUn_SV04R	R/W	CTUn_BASE + H'28	H'0000 0000	32
CTUn Scale Value e05 Register	CTUn_SV05R	R/W	CTUn_BASE + H'2C	H'0000 0000	32
CTUn Scale Value e06 Register	CTUn_SV06R	R/W	CTUn_BASE + H'30	H'0000 0000	32
CTUn Scale Value e07 Register	CTUn_SV07R	R/W	CTUn_BASE + H'34	H'0000 0000	32
CTUn Scale Value e10 Register	CTUn_SV10R	R/W	CTUn_BASE + H'38	H'0000 0000	32
CTUn Scale Value e11 Register	CTUn_SV11R	R/W	CTUn_BASE + H'3C	H'0000 0000	32
CTUn Scale Value e12 Register	CTUn_SV12R	R/W	CTUn_BASE + H'40	H'0000 0000	32
CTUn Scale Value e13 Register	CTUn_SV13R	R/W	CTUn_BASE + H'44	H'0000 0000	32
CTUn Scale Value e14 Register	CTUn_SV14R	R/W	CTUn_BASE + H'48	H'0000 0000	32
CTUn Scale Value e15 Register	CTUn_SV15R	R/W	CTUn_BASE + H'4C	H'0000 0000	32
CTUn Scale Value e16 Register	CTUn_SV16R	R/W	CTUn_BASE + H'50	H'0000 0000	32
CTUn Scale Value e17 Register	CTUn_SV17R	R/W	CTUn_BASE + H'54	H'0000 0000	32
CTUn Scale Value e20 Register	CTUn_SV20R	R/W	CTUn_BASE + H'58	H'0000 0000	32
CTUn Scale Value e21 Register	CTUn_SV21R	R/W	CTUn_BASE + H'5C	H'0000 0000	32
CTUn Scale Value e22 Register	CTUn_SV22R	R/W	CTUn_BASE + H'60	H'0000 0000	32
CTUn Scale Value e23 Register	CTUn_SV23R	R/W	CTUn_BASE + H'64	H'0000 0000	32
CTUn Scale Value e24 Register	CTUn_SV24R	R/W	CTUn_BASE + H'68	H'0000 0000	32
CTUn Scale Value e25 Register	CTUn_SV25R	R/W	CTUn_BASE + H'6C	H'0000 0000	32
CTUn Scale Value e26 Register	CTUn_SV26R	R/W	CTUn_BASE + H'70	H'0000 0000	32
CTUn Scale Value e27 Register	CTUn_SV27R	R/W	CTUn_BASE + H'74	H'0000 0000	32
CTUn Scale Value e30 Register	CTUn_SV30R	R/W	CTUn_BASE + H'78	H'0000 0000	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
CTUn Scale Value e31 Register	CTUn_SV31R	R/W	CTUn_BASE + H'7C	H'0000 0000	32
CTUn Scale Value e32 Register	CTUn_SV32R	R/W	CTUn_BASE + H'80	H'0000 0000	32
CTUn Scale Value e33 Register	CTUn_SV33R	R/W	CTUn_BASE + H'84	H'0000 0000	32
CTUn Scale Value e34 Register	CTUn_SV34R	R/W	CTUn_BASE + H'88	H'0000 0000	32
CTUn Scale Value e35 Register	CTUn_SV35R	R/W	CTUn_BASE + H'8C	H'0000 0000	32
CTUn Scale Value e36 Register	CTUn_SV36R	R/W	CTUn_BASE + H'90	H'0000 0000	32
CTUn Scale Value e37 Register	CTUn_SV37R	R/W	CTUn_BASE + H'94	H'0000 0000	32
MIX Registers	—	—	MIX0_BASE: H'EC50 0D00 MIX1_BASE: H'EC50 0D40	—	—
MIXp Software Reset Register	MIXp_SWRSR	R/W	MIXp_BASE + H'00	H'0000 0001	32
MIXp MIX Initialization Register	MIXp_MIXIR	R/W	MIXp_BASE + H'04	H'0000 0001	32
MIXp Audio Information Register	MIXp_ADINR	R/W	MIXp_BASE + H'08	H'0000 0000	32
MIXp MIX Mode Register	MIXp_MIXMR	R/W	MIXp_BASE + H'10	H'0000 0000	32
MIXp MIX Volume Period Register	MIXp_MVPDR	R/W	MIXp_BASE + H'14	H'0000 0000	32
MIXp MIX Decibel A Register	MIXp_MDBAR	R/W	MIXp_BASE + H'18	H'0000 0000	32
MIXp MIX Decibel B Register	MIXp_MDBBR	R/W	MIXp_BASE + H'1C	H'0000 0000	32
MIXp MIX Decibel C Register	MIXp_MDBCR	R/W	MIXp_BASE + H'20	H'0000 0000	32
MIXp MIX Decibel D Register	MIXp_MDBDR	R/W	MIXp_BASE + H'24	H'0000 0000	32
MIXp MIX Decibel Enable Register	MIXp_MDBER	R/W	MIXp_BASE + H'28	H'0000 0000	32
MIXp MIX Status Register	MIXp_MIXSR	R	MIXp_BASE + H'2C	H'0000 0000	32
DVC Registers	—	—	DVC0_BASE: H'EC50 0E00 DVC1_BASE: H'EC50 0F00	—	—
DVCp Software Reset Register	DVCp_SWRSR	R/W	DVCp_BASE + H'00	H'0000 0001	32
DVCp DVU Initialization Register	DVCp_DVUIR	R/W	DVCp_BASE + H'04	H'0000 0001	32
DVCp Audio Information Register	DVCp_ADINR	R/W	DVCp_BASE + H'08	H'0000 0000	32
DVCp DVU Control Register	DVCp_DVUCR	R/W	DVCp_BASE + H'10	H'0000 0000	32
DVCp Zero Cross Mute Control Register	DVCp_ZCMCR	R/W	DVCp_BASE + H'14	H'0000 0000	32
DVCp Volume Ramp Control Register	DVCp_VRCTR	R/W	DVCp_BASE + H'18	H'0000 0000	32
DVCp Volume Ramp Period Register	DVCp_VRPDR	R/W	DVCp_BASE + H'1C	H'0000 0000	32
DVCp Volume Ramp Decibel Register	DVCp_VRDBR	R/W	DVCp_BASE + H'20	H'0000 0000	32
DVCp Volume Ramp Wait Time Register	DVCp_VRWTR	R/W	DVCp_BASE + H'24	H'0000 0000	32
DVCp Volume Value Setting 0 Register	DVCp_VOL0R	R/W	DVCp_BASE + H'28	H'0000 0000	32
DVCp Volume Value Setting 1 Register	DVCp_VOL1R	R/W	DVCp_BASE + H'2C	H'0000 0000	32
DVCp Volume Value Setting 2 Register	DVCp_VOL2R	R/W	DVCp_BASE + H'30	H'0000 0000	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
DVCp Volume Value Setting 3 Register	DVCp_VOL3R	R/W	DVCp_BASE + H'34	H'0000 0000	32
DVCp Volume Value Setting 4 Register	DVCp_VOL4R	R/W	DVCp_BASE + H'38	H'0000 0000	32
DVCp Volume Value Setting 5 Register	DVCp_VOL5R	R/W	DVCp_BASE + H'3C	H'0000 0000	32
DVCp Volume Value Setting 6 Register	DVCp_VOL6R	R/W	DVCp_BASE + H'40	H'0000 0000	32
DVCp Volume Value Setting 7 Register	DVCp_VOL7R	R/W	DVCp_BASE + H'44	H'0000 0000	32
DVCp DVU Enable Register	DVCp_DVUER	R/W	DVCp_BASE + H'48	H'0000 0000	32
DVCp DVU Status Register	DVCp_DVUSR	R	DVCp_BASE + H'4C	H'0000 0008	32
DVCp Interrupt Enable Register	DVCp_DVIER	R/W	DVCp_BASE + H'50	H'0000 0000	32
SRC1 in Write Data Register	SRC1in_BUSIF	-/W	H'EC00 0400/ H'EC30 0400*	H'0000 0000	32
SRC2 in Write Data Register	SRC2in_BUSIF	-/W	H'EC00 0800/ H'EC30 0800*	H'0000 0000	32
SRC3 in Write Data Register	SRC3in_BUSIF	-/W	H'EC00 0C00/ H'EC30 0C00*	H'0000 0000	32
SRC4 in Write Data Register	SRC4in_BUSIF	-/W	H'EC00 1000/ H'EC30 1000*	H'0000 0000	32
SRC5 in Write Data Register	SRC5in_BUSIF	-/W	H'EC00 1400/ H'EC30 1400*	H'0000 0000	32
SRC6 in Write Data Register	SRC6in_BUSIF	-/W	H'EC00 1800/ H'EC30 1800*	H'0000 0000	32
SRC1 out Read Data Register	SRC1out_BUSIF	R	H'EC00 4400/ H'EC30 4400*	H'0000 0000	32
SRC2 out Read Data Register	SRC2out_BUSIF	R	H'EC00 4800/ H'EC30 4800*	H'0000 0000	32
SRC3 out Read Data Register	SRC3out_BUSIF	R	H'EC00 4C00/ H'EC30 4C00*	H'0000 0000	32
SRC4 out Read Data Register	SRC4out_BUSIF	R	H'EC00 5000/ H'EC30 5000*	H'0000 0000	32
SRC5 out Read Data Register	SRC5out_BUSIF	R	H'EC00 5400/ H'EC30 5400*	H'0000 0000	32
SRC 6out Read Data Register	SRC6out_BUSIF	R	H'EC00 5800/ H'EC30 5800*	H'0000 0000	32
CMD0 out Read Data Register	CMD0out_BUSIF	R	H'EC00 8000/ H'EC30 8000*	H'0000 0000	32
CMD1 out Read Data Register	CMD1out_BUSIF	R	H'EC00 8400/ H'EC30 8400*	H'0000 0000	32

Notes: m = 1 to 6; n = 00, 01, 02, 03, 10, 11, 12, or 13; p = 0 or 1

* H'EC00 XXXX is the address for transferring by Audio-DMAC. H'EC30 XXXX is the address for transferring by Audio-DMAC-Peripheral-Peripheral.

** This register is just what to show the initial value here, but, set a value according to section 30.2.23 by all means when you use it.

30.2 Register Description

Legend for Register Description

Initial value: Register value after a reset. H'xxxx represents a hexadecimal number. Others are represented in binary numbers.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be 0.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

W: Write-only. Reading this bit is prohibited. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

All access to registers is made in longword units.

30.2.1 SRCm(in/out)_BUSIF_MODE Register (SRCm(in/out)_BUSIF_MODE)

Note: m = 1 to 6

Function: SRCm (in/out)_BUSIF_MODE sets the initial setting for the bus interface.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	sft_dir	sft_num			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	dma
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	sft_dir	0	R/W	src*m*(in/out)_busif_shift_dir Selects the bit-shift direction for position adjustment of the valid SRC*m*(in/out)_BUSIF input and output data. 0: Shift to left. 1: Shift to right.
19 to 16	sft_num	0000	R/W	src*m*(in/out)_busif _shift_num Selects the bit-shift count for position adjustment of the valid SRC*m*(in/out)_BUSIF input and output data. 0000: 0 bit 0001: 1 bit 0010: 2 bits 0011: 3 bits 0100: 4 bits 0101: 5 bits 0110: 6 bits 0111: 7 bits 1000: 8 bits 1001: 9 bits 1010: 10 bits 1011: 11 bits 1100: 12 bits 1101: 13 bits 1110: 14 bits 1111: 15 bits
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	dma	1	R/W	src*m*(in/out)_busif _dma Selects the access type for SRC*m*(in/out)_BUSIF. 0: PIO access (setting prohibited) 1: DMA access Be sure to specify the DMA access.

30.2.2 SRCm_BUSIF_DALIGN Register (SRCm_BUSIF_DALIGN)

Note: m = 1, 3, or 4

Function: SRCm_BUSIF_DALIGN determines the initial settings of the SRCm route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	place7			—	place6			—	place5			—	place4		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	place3			—	place2			—	place1			—	place0		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	place7	111	R/W	Changes the stream data order. These bits are used for the 8-channel setting. **For the 6- or less-channel setting, the initial value should not be changed.** The data order is changed before input to the SRC. Selects the input-side data to be output to place 7 on the output side. 000: Data at input-side place 0 is sent to output-side place 7. 001: Data at input-side place 1 is sent to output-side place 7. 010: Data at input-side place 2 is sent to output-side place 7. 011: Data at input-side place 3 is sent to output-side place 7. 100: Data at input-side place 4 is sent to output-side place 7. 101: Data at input-side place 5 is sent to output-side place 7. 110: Data at input-side place 6 is sent to output-side place 7. 111: Data at input-side place 7 is sent to output-side place 7.
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26 to 24	place6	110	R/W	Changes the stream data order. These bits are used for the 8-channel setting. **For the 6- or less-channel setting, the initial value should not be changed.** The data order is changed before input to the SRC. Selects the input-side data to be output to place 6 on the output side. 000: Data at input-side place 0 is sent to output-side place 6. 001: Data at input-side place 1 is sent to output-side place 6. 010: Data at input-side place 2 is sent to output-side place 6. 011: Data at input-side place 3 is sent to output-side place 6. 100: Data at input-side place 4 is sent to output-side place 6. 101: Data at input-side place 5 is sent to output-side place 6. 110: Data at input-side place 6 is sent to output-side place 6. 111: Data at input-side place 7 is sent to output-side place 6.
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
22 to 20	place5	101	R/W	Changes the stream data order. These bits are used for the 6- or more-channel setting. **For the 4- or less-channel setting, the initial value should not be changed.** The data order is changed before input to the SRC. Selects the input-side data to be output to place 5 on the output side. 000: Data at input-side place 0 is sent to output-side place 5. 001: Data at input-side place 1 is sent to output-side place 5. 010: Data at input-side place 2 is sent to output-side place 5. 011: Data at input-side place 3 is sent to output-side place 5. 100: Data at input-side place 4 is sent to output-side place 5. 101: Data at input-side place 5 is sent to output-side place 5. 110: Data at input-side place 6 is sent to output-side place 5. 111: Data at input-side place 7 is sent to output-side place 5.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	place4	100	R/W	Changes the stream data order. These bits are used for the 6- or more-channel setting. **For the 4- or less-channel setting, the initial value should not be changed.** The data order is changed before input to the SRC. Selects the input-side data to be output to place 4 on the output side. 000: Data at input-side place 0 is sent to output-side place 4. 001: Data at input-side place 1 is sent to output-side place 4. 010: Data at input-side place 2 is sent to output-side place 4. 011: Data at input-side place 3 is sent to output-side place 4. 100: Data at input-side place 4 is sent to output-side place 4. 101: Data at input-side place 5 is sent to output-side place 4. 110: Data at input-side place 6 is sent to output-side place 4. 111: Data at input-side place 7 is sent to output-side place 4.
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	place3	011	R/W	Changes the stream data order. These bits are used for the 4- or more-channel setting. **For the 2- or less-channel setting, the initial value should not be changed.** The data order is changed before input to the SRC. Selects the input-side data to be output to place 3 on the output side. 000: Data at input-side place 0 is sent to output-side place 3. 001: Data at input-side place 1 is sent to output-side place 3. 010: Data at input-side place 2 is sent to output-side place 3. 011: Data at input-side place 3 is sent to output-side place 3. 100: Data at input-side place 4 is sent to output-side place 3. 101: Data at input-side place 5 is sent to output-side place 3. 110: Data at input-side place 6 is sent to output-side place 3. 111: Data at input-side place 7 is sent to output-side place 3.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	place2	010	R/W	Changes the stream data order. These bits are used for the 4- or more-channel setting. **For the 2- or less-channel setting, the initial value should not be changed.** The data order is changed before input to the SRC. Selects the input-side data to be output to place 2 on the output side. 000: Data at input-side place 0 is sent to output-side place 2. 001: Data at input-side place 1 is sent to output-side place 2. 010: Data at input-side place 2 is sent to output-side place 2. 011: Data at input-side place 3 is sent to output-side place 2. 100: Data at input-side place 4 is sent to output-side place 2. 101: Data at input-side place 5 is sent to output-side place 2. 110: Data at input-side place 6 is sent to output-side place 2. 111: Data at input-side place 7 is sent to output-side place 2.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	place1	001	R/W	Changes the stream data order. The data order is changed before input to the SRC. Selects the input-side data to be output to place 1 on the output side. 000: Data at input-side place 0 is sent to output-side place 1. 001: Data at input-side place 1 is sent to output-side place 1. 010: Data at input-side place 2 is sent to output-side place 1. 011: Data at input-side place 3 is sent to output-side place 1. 100: Data at input-side place 4 is sent to output-side place 1. 101: Data at input-side place 5 is sent to output-side place 1. 110: Data at input-side place 6 is sent to output-side place 1. 111: Data at input-side place 7 is sent to output-side place 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	place0	000	R/W	Changes the stream data order. The data order is changed before input to the SRC. Selects the input-side data to be output to place 0 on the output side. 000: Data at input-side place 0 is sent to output-side place 0. 001: Data at input-side place 1 is sent to output-side place 0. 010: Data at input-side place 2 is sent to output-side place 0. 011: Data at input-side place 3 is sent to output-side place 0. 100: Data at input-side place 4 is sent to output-side place 0. 101: Data at input-side place 5 is sent to output-side place 0. 110: Data at input-side place 6 is sent to output-side place 0. 111: Data at input-side place 7 is sent to output-side place 0.

30.2.3 SRCn_BUSIF_DALIGN Register (SRCn_BUSIF_DALIGN)

Note: n = 2, 5, or 6

Function: SRCn_BUSIF_DALIGN determines the initial settings of the SRCn route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	place1	—	—	—	place0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	place1	1	R/W	Changes the stream data order. The data order is changed before input to the SRC. Selects the input-side data to be output to place 1 on the output side. 0: Data at input-side place 0 is sent to output-side place 1. 1: Data at input-side place 1 is sent to output-side place 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	place0	0	R/W	Changes the stream data order. The data order is changed before input to the SRC. Selects the input-side data to be output to place 0 on the output side. 0: Data at input-side place 0 is sent to output-side place 0. 1: Data at input-side place 1 is sent to output-side place 0.

30.2.4 SRCm_MODE Register (SRCm_MODE)

Note: m = 1 to 6

Function: SRCm_MODE determines the initial settings of the SRCm route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	sync_out	sync_in	—	—	—	—	—	—	—	uf_data
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	src
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	sync_out	0	R/W	src*m*out_sync Selects how to treat data in the SRC output buffer. 0: Asynchronous SRC 1: Synchronous SRC
24	sync_in	0	R/W	src*m*in_sync Selects how to treat data in the SRC input buffer. 0: Asynchronous SRC 1: Synchronous SRC
23 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	uf_data	0	R/W	src*m*_uf_data_sel Selects how to treat data when an underflow occurs in the SRC input buffer. 0: Data before the underflow occurs is output. 1: All 0s are output.
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	src	0	R/W	src*m*_src Selects whether to use SRC*m*. 0: SRC*m* is not used. 1: SRC*m* is used.

Notes: 1. Set one of sync_in and sync_out bits, when SRC*m* is used in synchronous mode by setting SRCMD bit in SRCm_SRCCR register.
2. If sync_out is set in synchronous mode, data should directly transmit to memory. (Data should not transmit throughout CMD.)

30.2.5 SRCm Control Register (SRCm_CONTROL)

Note: m = 1 to 6

Function: SRCm_CONTROL starts or stops transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	start_ out	—	—	—	start_ in
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	start_out	0	R/W	SRC*m*out_start_flag Starts or stops transfer via SRC*m*. 0: Stops transfer. 1: Starts transfer.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	start_in	0	R/W	SRC*m*in_start_flag Starts or stops transfer via SRC*m*. 0: Stops transfer. 1: Starts transfer.

When CMD is used with route SRC1, SRC2, SRC3, SRC4, or SRC5, SRC*m*out_start_flag should be set to 0 to stop transfer. When CMD is not used with route SRC1, SRC2, SRC3, SRC4, or SRC5, SRC*m*in_start_flag and SRC*m*out_start_flag should be set simultaneously.

When CMD is used and the sync_in bit in the SRCm_MODE register is set for synchronous mode, SRC*m*out_start_flag should be set to 1 to start transfer. However, in this case, use of the output data SRCm out_BUSIF is prohibited and ignore the value of over_flow_srcout in the SRCm_STATUS register.

30.2.6 SRCm Status Register (SRCm_STATUS)

Note: m = 1 to 5

Function: SRCm_STATUS indicates the state of each SRC. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SRC*m* interrupt enable register, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	dvc1	—	—	—	dvc0	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_srco	of_srco	—	—	of_srci	uf_srci	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	dvc1	0	R	dvc1 Indicates the state of the DVC1_DVUSR register collectively. The state information is used only for the interrupt signal that is enabled by DVC1_DVIER.
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	dvc0	0	R	dvc0 Indicates the state of the DVC0_DVUSR register collectively. The state information is used only for the interrupt signal that is enabled by DVC0_DVIER.
23 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_srco	0	R	under_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
12	of_srco	0	R	over_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_srci	0	R	over_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.

Bit	Bit Name	Initial Value	R/W	Description
8	uf_srci	0	R	under_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.7 SRCn Status Register (SRCn_STATUS)

Note: n = 6

Function: SRCn_STATUS indicates the state of each SRC. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SRCn interrupt enable register, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_srco	of_srco	—	—	of_srci	uf_srci	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_srco	0	R	under_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
12	of_srco	0	R	over_flow_srcout Indicates the state of the output buffer of SRCout in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_srci	0	R	over_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS1 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE1.
8	uf_srci	0	R	under_flow_srcin Indicates the state of the output buffer of SRCin in the SCU_SYSTEM_STATUS0 register. The state information is used when the interrupt signal is enabled by SCU_SYSTEM_INT_ENABLE0.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.8 SRCm Interrupt Enable Register 0 (SRCm_INT_ENABLE0)

Note: m = 1 to 5

Function: SRCm_INT_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SRCm status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	dvc1_ie	—	—	—	dvc0_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_srco_ie	of_srco_ie	—	—	of_srci_ie	uf_srci_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28	dvc1_ie	0	R/W	dvc1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	dvc0_ie	0	R/W	dvc0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_srco_ie	0	R/W	under_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	of_srco_ie	0	R/W	over_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_srci_ie	0	R/W	over_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	uf_srci_ie	0	R/W	under_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.9 SRCn Interrupt Enable Register 0 (SRCn_INT_ENABLE0)

Note: n = 6

Function: SRCn_INT_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SRCn status register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	uf_srco_ie	of_srco_ie	—	—	of_srci_ie	uf_srci_ie	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
13	uf_srco_ie	0	R/W	under_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	of_srco_ie	0	R/W	over_flow_srcout_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	of_srci_ie	0	R/W	over_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	uf_srci_ie	0	R/W	under_flow_srcin_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.10 CMDn out_BUSIF_MODE Register (CMDn out_BUSIF_MODE)

Note: n = 0, 1

Function: CMDn out_BUSIF_MODE sets the initial setting for the bus interface

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	sft_dir	sft_num			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	dma
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	sft_dir	0	R/W	cmd*n*out_busif_shift_dir Selects the bit-shift direction for position adjustment of the valid CMD*n*out_BUSIF input and output data. 0: Shift to left. 1: Shift to right.
19 to 16	sft_num	0000	R/W	cmd*n*out_busif_shift_num Selects the bit-shift count for position adjustment of the valid CMD*n*out_BUSIF input and output data. 0000: 0 bit 0001: 1 bit 0010: 2 bits 0011: 3 bits 0100: 4 bits 0101: 5 bits 0110: 6 bits 0111: 7 bits 1000: 8 bits 1001: 9 bits 1010: 10 bits 1011: 11 bits 1100: 12 bits 1101: 13 bits 1110: 14 bits 1111: 15 bits
15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	dma	1	R/W	CMDnout_busif _dma Selects the access type for CMDnout_BUSIF. 0: PIO access (setting prohibited) 1: DMA access Be sure to specify the DMA access.

30.2.11 CMDn_BUSIF_DALIGN Register (CMDn_BUSIF_DALIGN)

Note: n = 0, 1

Function: CMDn_BUSIF_DALIGN determines the initial settings of the CMDn route.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	place7			—	place6			—	place5			—	place4		
Initial value:	0	1	1	1	0	1	1	0	0	1	0	1	0	1	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	place3			—	place2			—	place1			—	place0		
Initial value:	0	0	1	1	0	0	1	0	0	0	0	1	0	0	0	0
R/W:	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 28	place7	111	R/W	Changes the stream data order. These bits are used for the 8-channel setting. **For the 6- or less-channel setting, the initial value should not be changed.** The data order is changed after output from the CMD. Selects the input-side data to be output to place 7 on the output side. 000: Data at input-side place 0 is sent to output-side place 7. 001: Data at input-side place 1 is sent to output-side place 7. 010: Data at input-side place 2 is sent to output-side place 7. 011: Data at input-side place 3 is sent to output-side place 7. 100: Data at input-side place 4 is sent to output-side place 7. 101: Data at input-side place 5 is sent to output-side place 7. 110: Data at input-side place 6 is sent to output-side place 7. 111: Data at input-side place 7 is sent to output-side place 7.
27	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
26 to 24	place6	110	R/W	Changes the stream data order. These bits are used for the 8-channel setting. **For the 6- or less-channel setting, the initial value should not be changed.** The data order is changed after output from the CMD. Selects the input-side data to be output to place 6 on the output side. 000: Data at input-side place 0 is sent to output-side place 6. 001: Data at input-side place 1 is sent to output-side place 6. 010: Data at input-side place 2 is sent to output-side place 6. 011: Data at input-side place 3 is sent to output-side place 6. 100: Data at input-side place 4 is sent to output-side place 6. 101: Data at input-side place 5 is sent to output-side place 6. 110: Data at input-side place 6 is sent to output-side place 6. 111: Data at input-side place 7 is sent to output-side place 6.
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
22 to 20	place5	101	R/W	Changes the stream data order. These bits are used for the 6- or more-channel setting. **For the 4- or less-channel setting, the initial value should not be changed.** The data order is changed after output from the CMD. Selects the input-side data to be output to place 5 on the output side. 000: Data at input-side place 0 is sent to output-side place 5. 001: Data at input-side place 1 is sent to output-side place 5. 010: Data at input-side place 2 is sent to output-side place 5. 011: Data at input-side place 3 is sent to output-side place 5. 100: Data at input-side place 4 is sent to output-side place 5. 101: Data at input-side place 5 is sent to output-side place 5. 110: Data at input-side place 6 is sent to output-side place 5. 111: Data at input-side place 7 is sent to output-side place 5.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	place4	100	R/W	Changes the stream data order. These bits are used for the 6- or more-channel setting. **For the 4- or less-channel setting, the initial value should not be changed.** The data order is changed after output from the CMD. Selects the input-side data to be output to place 4 on the output side. 000: Data at input-side place 0 is sent to output-side place 4. 001: Data at input-side place 1 is sent to output-side place 4. 010: Data at input-side place 2 is sent to output-side place 4. 011: Data at input-side place 3 is sent to output-side place 4. 100: Data at input-side place 4 is sent to output-side place 4. 101: Data at input-side place 5 is sent to output-side place 4. 110: Data at input-side place 6 is sent to output-side place 4. 111: Data at input-side place 7 is sent to output-side place 4.
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 12	place3	011	R/W	Changes the stream data order. These bits are used for the 4- or more-channel setting. **For the 2- or less-channel setting, the initial value should not be changed.** The data order is changed after output from the CMD. Selects the input-side data to be output to place 3 on the output side. 000: Data at input-side place 0 is sent to output-side place 3. 001: Data at input-side place 1 is sent to output-side place 3. 010: Data at input-side place 2 is sent to output-side place 3. 011: Data at input-side place 3 is sent to output-side place 3. 100: Data at input-side place 4 is sent to output-side place 3. 101: Data at input-side place 5 is sent to output-side place 3. 110: Data at input-side place 6 is sent to output-side place 3. 111: Data at input-side place 7 is sent to output-side place 3.
11	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10 to 8	place2	010	R/W	Changes the stream data order. These bits are used for the 4- or more-channel setting. **For the 2- or less-channel setting, the initial value should not be changed.** The data order is changed after output from the CMD. Selects the input-side data to be output to place 2 on the output side. 000: Data at input-side place 0 is sent to output-side place 2. 001: Data at input-side place 1 is sent to output-side place 2. 010: Data at input-side place 2 is sent to output-side place 2. 011: Data at input-side place 3 is sent to output-side place 2. 100: Data at input-side place 4 is sent to output-side place 2. 101: Data at input-side place 5 is sent to output-side place 2. 110: Data at input-side place 6 is sent to output-side place 2. 111: Data at input-side place 7 is sent to output-side place 2.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 4	place1	001	R/W	Changes the stream data order. The data order is changed after output from the CMD. Selects the input-side data to be output to place 1 on the output side. 000: Data at input-side place 0 is sent to output-side place 1. 001: Data at input-side place 1 is sent to output-side place 1. 010: Data at input-side place 2 is sent to output-side place 1. 011: Data at input-side place 3 is sent to output-side place 1. 100: Data at input-side place 4 is sent to output-side place 1. 101: Data at input-side place 5 is sent to output-side place 1. 110: Data at input-side place 6 is sent to output-side place 1. 111: Data at input-side place 7 is sent to output-side place 1.
3	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
2 to 0	place0	000	R/W	Changes the stream data order. The data order is changed after output from the CMD. Selects the input-side data to be output to place 0 on the output side. 000: Data at input-side place 0 is sent to output-side place 0. 001: Data at input-side place 1 is sent to output-side place 0. 010: Data at input-side place 2 is sent to output-side place 0. 011: Data at input-side place 3 is sent to output-side place 0. 100: Data at input-side place 4 is sent to output-side place 0. 101: Data at input-side place 5 is sent to output-side place 0. 110: Data at input-side place 6 is sent to output-side place 0. 111: Data at input-side place 7 is sent to output-side place 0.

30.2.12 CMDn_ROUTE_SELECT Register (CMDn_ROUTE_SELECT)

Note: n = 0, 1

Function: CMDn_ROUTE_SELECT selects the sound route for each CMD (CTU, MIX, and DVC). Refer to Figures 30.1 and 30.11 for the sound routes.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	cmd_case		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	cmdin_ctu3	—	—	—	—	—	—	—	cmdin_ctu2
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 19	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
18 to 16	cmd_case	000	R/W	cmd*n*_case_sel Selects the route in CMD*n*. 000: Input audio data0 to 3 → CTU → MIX → DVC route is used. 001: Input audio data0 (from SRC3) → DVC route is used. 010: Input audio data1 (from SRC4) → DVC route is used. 011: Input audio data2 (from SRC1) → DVC route is used. 100: Input audio data3 (from SRC2 or SRC5) → DVC route is used. Others: Setting prohibited.
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	cmdin_ctu3	0	R/W	cmd*n*in_ctu3_sel Selects SRC for Input audio data3 of CMD*n*. 0: SRC2 route is used. 1: SRC5 route is used.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	cmdin_ctu2	0	R/W	cmd*n*in_ctu2_sel Selects SRC for Input audio data2 of CMD*n*. 0: No operation 1: SRC1 route is used.

30.2.13 CMDn Control Register (CMDn_CONTROL)

Note: n = 0, 1

Function: CMDn_CONTROL starts or stops transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	start_ out	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	start_out	0	R/W	CMD*n*out_start_flag Starts or stops transfer via CMD*n*. 0: Stops transfer. 1: Starts transfer.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.14 SCU_SYSTEM Status Register 0 (SCU_SYSTEM_STATUS0)

Function: SCU_SYSTEM_STATUS0 indicates the internal buffer state. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SYSTEM interrupt enable register 0, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	of_cmd1o	of_cmd0o	—	—	—	—	—	of_src6o	of_src5o	of_src4o	of_src3o	of_src2o	of_src1o	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/WC1	R/WC1	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	uf_src6i	uf_src5i	uf_src4i	uf_src3i	uf_src2i	uf_src1i	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	of_cmd1o	0	R/WC1	over_flow_cmd1out Indicates the state of the CMD1out output buffer. 0: Normal operation 1: An overflow has occurred.
28	of_cmd0o	0	R/WC1	over_flow_cmd0out Indicates the state of the CMD0out output buffer. 0: Normal operation 1: An overflow has occurred.
27 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	of_src6o	0	R/WC1	over_flow_src6out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An overflow has occurred.
21	of_src5o	0	R/WC1	over_flow_src5out Indicates the state of the SRC5out output buffer. 0: Normal operation 1: An overflow has occurred.
20	of_src4o	0	R/WC1	over_flow_src4out Indicates the state of the SRC4out output buffer. 0: Normal operation 1: An overflow has occurred.
19	of_src3o	0	R/WC1	over_flow_src3out Indicates the state of the SRC3out output buffer. 0: Normal operation 1: An overflow has occurred.

Bit	Bit Name	Initial Value	R/W	Description
18	of_src2o	0	R/WC1	over_flow_src2out Indicates the state of the SRC2out output buffer. 0: Normal operation 1: An overflow has occurred.
17	of_src1o	0	R/WC1	over_flow_src1out Indicates the state of the SRC1out output buffer. 0: Normal operation 1: An overflow has occurred.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	uf_src6i	0	R/WC1	under_flow_src6in Indicates the state of the SRC6in input buffer. 0: Normal operation 1: An underflow has occurred.
5	uf_src5i	0	R/WC1	under_flow_src5in Indicates the state of the SRC5in input buffer. 0: Normal operation 1: An underflow has occurred.
4	uf_src4i	0	R/WC1	under_flow_src4in Indicates the state of the SRC4in input buffer. 0: Normal operation 1: An underflow has occurred.
3	uf_src3i	0	R/WC1	under_flow_src3in Indicates the state of the SRC3in input buffer. 0: Normal operation 1: An underflow has occurred.
2	uf_src2i	0	R/WC1	under_flow_src2in Indicates the state of the SRC2in input buffer. 0: Normal operation 1: An underflow has occurred.
1	uf_src1i	0	R/WC1	under_flow_src1in Indicates the state of the SRC1in input buffer. 0: Normal operation 1: An underflow has occurred.
0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.15 SCU_SYSTEM Interrupt Enable Register 0 (SCU_SYSTEM_INT_ENABLE0)

Function: SCU_SYSTEM_INT_ENABLE0 enables or disables output of interrupts corresponding to the states indicated in the SCU_SYSTEM status register 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	of_cmd1o_ie	of_cmd0o_ie	—	—	—	—	—	of_src6o_ie	of_src5o_ie	of_src4o_ie	of_src3o_ie	of_src2o_ie	of_src1o_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	uf_src6i_ie	uf_src5i_ie	uf_src4i_ie	uf_src3i_ie	uf_src2i_ie	uf_src1i_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	of_cmd1o_ie	0	R/W	over_flow_cmd1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
28	of_cmd0o_ie	0	R/W	over_flow_cmd0out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
27 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	of_src6o_ie	0	R/W	over_flow_src6out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	of_src5o_ie	0	R/W	over_flow_src5out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	of_src4o_ie	0	R/W	over_flow_src4out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	of_src3o_ie	0	R/W	over_flow_src3out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	of_src2o_ie	0	R/W	over_flow_src2out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
17	of_src1o_ie	0	R/W	over_flow_src1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	uf_src6i_ie	0	R/W	under_flow_src6in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	uf_src5i_ie	0	R/W	under_flow_src5in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	uf_src4i_ie	0	R/W	under_flow_src4in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	uf_src3i_ie	0	R/W	under_flow_src3in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	uf_src2i_ie	0	R/W	under_flow_src2in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	uf_src1i_ie	0	R/W	under_flow_src1in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

30.2.16 SCU_SYSTEM Status Register 1 (SCU_SYSTEM_STATUS1)

Function: SCU_SYSTEM_STATUS1 indicates the internal buffer state in synchronous mode. When a register bit is set, the corresponding interrupt signal is output. However, if interrupt outputs are masked by the SYSTEM interrupt enable register 1, interrupt signals are not output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	uf_src6o	uf_src5o	uf_src4o	uf_src3o	uf_src2o	uf_src1o	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	of_src6i	of_src5i	of_src4i	of_src3i	of_src2i	of_src1i	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R/WC1	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	uf_src6o	0	R/WC1	under_flow_src6out Indicates the state of the SRC6out output buffer. 0: Normal operation 1: An underflow has occurred.
21	uf_src5o	0	R/WC1	under_flow_src5out Indicates the state of the SRC5out output buffer. 0: Normal operation 1: An underflow has occurred.
20	uf_src4o	0	R/WC1	under_flow_src4out Indicates the state of the SRC4out output buffer. 0: Normal operation 1: An underflow has occurred.
19	uf_src3o	0	R/WC1	under_flow_src3out Indicates the state of the SRC3out output buffer. 0: Normal operation 1: An underflow has occurred.
18	uf_src2o	0	R/WC1	under_flow_src2out Indicates the state of the SRC2out output buffer. 0: Normal operation 1: An underflow has occurred.
17	uf_src1o	0	R/WC1	under_flow_src1out Indicates the state of the SRC1out output buffer. 0: Normal operation 1: An underflow has occurred.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
6	of_src6i	0	R/WC1	over_flow_src6in Indicates the state of the SRC6in input buffer. 0: Normal operation 1: An overflow has occurred.
5	of_src5i	0	R/WC1	over_flow_src5in Indicates the state of the SRC5in input buffer. 0: Normal operation 1: An overflow has occurred.
4	of_src4i	0	R/WC1	over_flow_src4in Indicates the state of the SRC4in input buffer. 0: Normal operation 1: An overflow has occurred.
3	of_src3i	0	R/WC1	over_flow_src3in Indicates the state of the SRC3in input buffer. 0: Normal operation 1: An overflow has occurred.
2	of_src2i	0	R/WC1	over_flow_src2in Indicates the state of the SRC2in input buffer. 0: Normal operation 1: An overflow has occurred.
1	of_src1i	0	R/WC1	over_flow_src1in Indicates the state of the SRC1in input buffer. 0: Normal operation 1: An overflow has occurred.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

30.2.17 SCU_SYSTEM Interrupt Enable Register 1 (SCU_SYSTEM_INT_ENABLE1)

Function: SCU_SYSTEM_INT_ENABLE1 enables or disables output of interrupts corresponding to the states indicated in the SCU_SYSTEM status register 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	uf_src6o_ie	uf_src5o_ie	uf_src4o_ie	uf_src3o_ie	uf_src2o_ie	uf_src1o_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	of_src6i_ie	of_src5i_ie	of_src4i_ie	of_src3i_ie	of_src2i_ie	of_src1i_ie	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	uf_src6o_ie	0	R/W	under_flow_src6out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	uf_src5o_ie	0	R/W	under_flow_src5out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	uf_src4o_ie	0	R/W	under_flow_src4out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	uf_src3o_ie	0	R/W	under_flow_src3out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	uf_src2o_ie	0	R/W	under_flow_src2out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
17	uf_src1o_ie	0	R/W	under_flow_src1out_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	of_src6i_ie	0	R/W	over_flow_src6in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	of_src5i_ie	0	R/W	over_flow_src5in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	of_src4i_ie	0	R/W	over_flow_src4in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
3	of_src3i_ie	0	R/W	over_flow_src3in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	of_src2i_ie	0	R/W	over_flow_src2in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	of_src1i_ie	0	R/W	over_flow_src1in_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

30.2.18 SRCm Software Reset Register (SRCm_SWRSR)

Note: m = 1 to 6

Function: SRCm_SWRSR is a 32-bit readable/writable register that controls operation/reset of the SRC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the SRC internal circuits are put in the reset state. SRCm_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the SRC 1: SRC enters the operating state

30.2.19 SRCm SRC Initialization Register (SRCm_SRCIR)

Note: m = 1 to 6

Function: SRCm_SRCIR is a 32-bit readable/writable register that initializes the operation of the SRC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the SRC processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

30.2.20 SRCm Audio Information Register (SRCm_ADINR)

Note: m = 1 to 6

Function: SRCm_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	OTBL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number (For m = 1, 3, or 4) These bits set the channel number. 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved Channel Number (For m = 2, 5, or 6) These bits set the channel number. 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011 to 1111: Reserved

30.2.21 SRCm IFS Control Register (SRCm_IFSCR)

Note: m = 1 to 6

Function: SRCm_IFSCR is a 32-bit readable/writable register that controls INTIFS value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INTIFS EN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INTIFSEN	0	R/W	INTIFS Value Setting Enable This bit controls the INTIFS bit of SRCm_IFSVR register. This bit is effective only in asynchronous SRC Mode (bit SRCMD in SRCm_SRCCR register is 0) 0: Disables INTIFS bit of SRCm_IFSVR register 1: Enables INTIFS bit of SRCm_IFSVR register Basically, this bit should be set to 1.

30.2.22 SRCm IFS Value Setting Register (SRCm_IFSVR)

Note: m = 1 to 6

Function: SRCm_IFSVR is a 32-bit readable/writable register that sets the value of INTIFS. The INTIFS is the initial value of FSI of sampling rate conversion function. SRC detects input sampling rate and output sampling rate automatically. By doing this, it calculates the FSI value so that the below formula is satisfied.

Fin/Fout ≈ FSI/FSO

The INTIFS value is used for the initial value of FSI. If this setting is disabled (INTIFSEN bit of SRCm_IFSCR register is 0), SRC will use FSO for initial value of FSI.

INTIFS = Fin × FSO/Fout

Note: Fin: Input sampling frequency
Fout: Output sampling frequency
FSI: Input sampling rate
FSO: Output sampling rate (Fixed value: 2^{22} = H'040 0000)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	INTIFS[27:16]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	INTIFS[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
27 to 0	INTIFS[27:0]	H'000 0000	R/W	Initial Value of FSI These bits set initial value of FSI. These bits should be set the ratio of input and output sampling-rate within the range of the restriction decided from channel number. Example: Fin = 32 kHz Fout = 44.1 kHz FSI = 2^{22} × 32000 / 44100 = 3043485 = H'02E709D For the setting value examples, see Table 30.8.

Note: When SRCm is used in synchronous mode (SRCMD bit in SRCm_SRCCR register is 1), INTIFS can change without SRC initialization. On the operating state, INTIFS can change within 1%.
However, the change of the SRC conversion rate means that it will set jitter by manual operation. Evaluate sound quality, and use this function as far as you judged sound quality is no problem.
If on the occasion of the change more than 1%, it should do SRC initialization (cf. section 30.3.5 (1) (d)) after changing INTIFS.

30.2.23 SRCm SRC Control Register (SRCm_SRCCR)

Note: m = 1 to 6

Function: SRCm_SRCCR is a 32-bit readable/writable register that controls the operation of sampling rate converter.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SRCMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	0	R/W	This bit should be set to 1.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	0	R/W	This bit should be set to 1.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	—	0	R/W	This bit should be set to 1.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	—	0	R/W	This bit should be set to 1.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SRCMD	0	R/W	Select SRC Mode 0: Asynchronous SRC 1: Synchronous SRC

Note: Set sync_in or sync_out bit in SRCm_MODE register, when SRCm is used in synchronous mode by setting SRCMD = 1.

30.2.24 SRCm Buffer Size DATA RAM Setting Register (SRCm_BSDSR)

Note: m = 1 to 4

Function: SRCm_BSDSR is a 32-bit readable/writable register that controls the buffer size of DATA RAM. This register should set with SRCm_BSISR register. See Table 30.7 for the combination of settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	BUFDATA[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	BUFDATA [10:0]	H'000	R/W	These bits should be set appropriately according to the following table. Refer to Table 30.7 for the combination of FSO/FSI ratio, channel number, and latency.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

FSO/FSI Ratio	Value
6 – 1/6	H'180
6 – 1/4	H'100
6 – 1/3	H'0C0
6 – 1/2	H'080
6 – 2/3	H'060
6 – 1	H'040

30.2.25 SRCn Buffer Size DATA RAM Setting Register (SRCn_BSDSR)

Note: n = 5 or 6

Function: SRCn_BSDSR is a 32-bit readable/writable register that controls the buffer size of DATA RAM. This register should set with SRCm_BSISR register. See Table 30.7 for the combination of settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	BUFDATA[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 16	BUFDATA [10:0]	H'000	R/W	These bits should be set appropriately according to the following table. Refer to Table 30.7 for the combination of FSO/FSI ratio, channel number, and latency.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

FSO/FSI Ratio	Value
6 – 1/6	H'240
6 – 1/4	H'180
6 – 1/3	H'120
6 – 1/2	H'0C0
6 – 2/3	H'090
6 – 1	H'060

30.2.26 SRCm Buffer Size IJEC RAM Setting Register (SRCm_BSISR)

Note: m = 1 to 6

Function: SRCm_BSISR is a 32-bit readable/writable register that controls the precision value and buffer size of IJEC RAM. This register should set with SRCm_BSDSR/SRCn_BSDSR register. See Table 30.7 for the combination of settings.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	IJECPREC[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	IJECSIZE[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 16	IJECPREC[5:0]	H'00	R/W	These bits should be set to H'10.
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	IJECSIZE[8:0]	H'000	R/W	These bits should be set appropriately according to the following table. Refer to Table 30.7 for the combination of FSO/FSI ratio, channel number, and latency.

FSO/FSI Ratio	Value
6 – 1/6	H'60
6 – 1/4	H'40
6 – 1/3	H'30
6 – 1/2	H'20
6 – 2/3	H'20
6 – 1	H'20

30.2.27 CTUn Software Reset Register (CTUn_SWRSR)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SWRSR is a 32-bit readable/writable register that controls operation/reset of the CTU internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the CTU internal circuits are put in the reset state. CTUn_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the CTU 1: Operating state

30.2.28 CTUn CTU Initialization Register (CTUn_CTUIR)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_CTUIR is a 32-bit readable/writable register that initializes the operation of the CTU internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the CTU processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

30.2.29 CTUn Audio Information Register (CTUn_ADINR)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_ADINR is a 32-bit readable/writable register that selects channel number.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved

30.2.30 CTUn CTU Pass Mode Register (CTUn_CPMDR)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_CPMDR is a 32-bit readable/writable register that controls the pass of channel data for each output.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SELOT0[3:0]				SELOT1[3:0]				SELOT2[3:0]				SELOT3[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SELOT4[3:0]				SELOT5[3:0]				SELOT6[3:0]				SELOT7[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	SELOT0[3:0]	0000	R/W	Select output data for channel 0 These bits select the output data for channel 0. 0000: Connect input data of channel 0 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3
27 to 24	SELOT1[3:0]	0000	R/W	Select output data for channel 1 These bits select the output data for channel 1. 0000: Connect input data of channel 1 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3

Bit	Bit Name	Initial Value	R/W	Description
23 to 20	SELOT2[3:0]	0000	R/W	Select output data for channel 2 These bits select the output data for channel 2. 0000: Connect input data of channel 2 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3
19 to 16	SELOT3[3:0]	0000	R/W	Select output data for channel 3 These bits select the output data for channel 3. 0000: Connect input data of channel 3 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3
15 to 12	SELOT4[3:0]	0000	R/W	Select output data for channel 4 These bits select the output data for channel 4. 0000: Connect input data of channel 4 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	SELOT5[3:0]	0000	R/W	Select output data for channel 5 These bits select the output data for channel 5. 0000: Connect input data of channel 5 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3
7 to 4	SELOT6[3:0]	0000	R/W	Select output data for channel 6 These bits select the output data for channel 6. 0000: Connect input data of channel 6 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3
3 to 0	SELOT7[3:0]	0000	R/W	Select output data for channel 7 These bits select the output data for channel 7. 0000: Connect input data of channel 7 0001: Connect input data of channel 0 0010: Connect input data of channel 1 0011: Connect input data of channel 2 0100: Connect input data of channel 3 0101: Connect input data of channel 4 0110: Connect input data of channel 5 0111: Connect input data of channel 6 1000: Connect input data of channel 7 1001: Connect calculated data by scale values of matrix row 0 1010: Connect calculated data by scale values of matrix row 1 1011: Connect calculated data by scale values of matrix row 2 1100: Connect calculated data by scale values of matrix row 3

30.2.31 CTUn Scale Mode Register (CTUn_SCMDR)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SCMDR is a 32-bit readable/writable register that selects the number of rows calculated by matrix.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	SCMD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	SCMD[2:0]	000	R/W	The number of rows calculated by matrix These bits select the number of rows calculated by matrix by the scale values. 000: No operation 001: Calculate matrix row 0 by scale values. 010: Calculate matrix row 0 and 1 by scale values. 011: Calculate matrix row 0 and 1 and 2 by scale values. 100: Calculate matrix row 0 and 1 and 2 and 3 by scale values.

30.2.32 CTUn Scale Value e00 Register (CTUn_SV00R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV00R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE00[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE00[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE00[23:0]	H'00 0000	R/W	Scale Value e00 for Input Channel 0 of Matrix Row 0 These bits set the scale value for input data of channel 0 of matrix row 0. SVE00[23]: Sign bit SVE00[22]: Integer bit SVE00[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.33 CTUn Scale Value e01 Register (CTUn_SV01R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV01R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE01[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE01[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE01[23:0]	H'00 0000	R/W	Scale Value e01 for Input Channel 1 of Matrix Row 0 These bits set the scale value for input data of channel 1 of matrix row 0. SVE01[23]: Sign bit SVE01[22]: Integer bit SVE01[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.34 CTUn Scale Value e02 Register (CTUn_SV02R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV02R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE02[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE02[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE02[23:0]	H'00 0000	R/W	Scale Value e02 for Input Channel 2 of Matrix Row 0 These bits set the scale value for input data of channel 2 of matrix row 0. SVE02[23]: Sign bit SVE02[22]: Integer bit SVE02[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.35 CTUn Scale Value e03 Register (CTUn_SV03R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV03R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE03[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE03[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE03[23:0]	H'00 0000	R/W	Scale Value e03 for Input Channel 3 of Matrix Row 0 These bits set the scale value for input data of channel 3 of matrix row 0. SVE03[23]: Sign bit SVE03[22]: Integer bit SVE03[21:0]: Decimal bits

plus			minus		
Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.36 CTUn Scale Value e04 Register (CTUn_SV04R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV04R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE04[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE04[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE04[23:0]	H'00 0000	R/W	Scale Value e04 for Input Channel 4 of Matrix Row 0 These bits set the scale value for input data of channel 4 of matrix row 0. SVE04[23]: Sign bit SVE04[22]: Integer bit SVE04[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.37 CTUn Scale Value e05 Register (CTUn_SV05R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV05R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE05[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE05[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE05[23:0]	H'00 0000	R/W	Scale Value e05 for Input Channel 5 of Matrix Row 0 These bits set the scale value for input data of channel 5 of matrix row 0. SVE05[23]: Sign bit SVE05[22]: Integer bit SVE05[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.38 CTUn Scale Value e06 Register (CTUn_SV06R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV06R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE06[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE06[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE06[23:0]	H'00 0000	R/W	Scale Value e06 for Input Channel 6 of Matrix Row 0 These bits set the scale value for input data of channel 6 of matrix row 0. SVE06[23]: Sign bit SVE06[22]: Integer bit SVE06[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.39 CTUn Scale Value e07 Register (CTUn_SV07R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV07R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE07[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE07[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE07[23:0]	H'00 0000	R/W	Scale Value e07 for Input Channel 7 of Matrix Row 0 These bits set the scale value for input data of channel 7 of matrix row 0. SVE07[23]: Sign bit SVE07[22]: Integer bit SVE07[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.40 CTUn Scale Value e10 Register (CTUn_SV10R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV10R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE10[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE10[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE10[23:0]	H'00 0000	R/W	Scale Value e10 for Input Channel 0 of Matrix Row 1 These bits set the scale value for input data of channel 0 of matrix row 1. SVE10[23]: Sign bit SVE10[22]: Integer bit SVE10[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.41 CTUn Scale Value e11 Register (CTUn_SV11R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV11R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE11[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE11[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

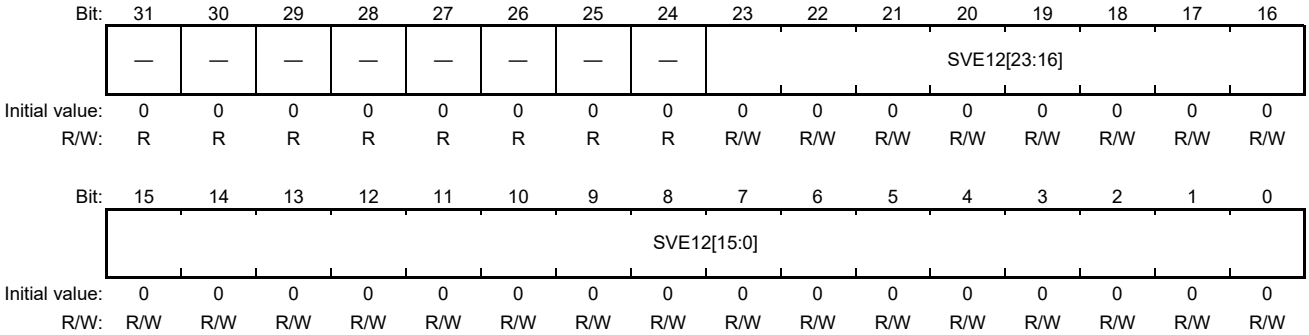
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE11[23:0]	H'00 0000	R/W	Scale Value e11 for Input Channel 1 of Matrix Row 1 These bits set the scale value for input data of channel 1 of matrix row 1. SVE11[23]: Sign bit SVE11[22]: Integer bit SVE11[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.42 CTUn Scale Value e12 Register (CTUn_SV12R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV12R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 1.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE12[23:0]	H'00 0000	R/W	Scale Value e12 for Input Channel 2 of Matrix Row 1 These bits set the scale value for input data of channel 2 of matrix row 1. SVE12[23]: Sign bit SVE12[22]: Integer bit SVE12[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.43 CTUn Scale Value e13 Register (CTUn_SV13R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV13R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE13[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE13[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE13[23:0]	H'00 0000	R/W	Scale Value e13 for Input Channel 3 of Matrix Row 1 These bits set the scale value for input data of channel 3 of matrix row 1. SVE13[23]: Sign bit SVE13[22]: Integer bit SVE13[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.44 CTUn Scale Value e14 Register (CTUn_SV14R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV14R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE14[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE14[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE14[23:0]	H'00 0000	R/W	Scale Value e14 for Input Channel 4 of Matrix Row 1 These bits set the scale value for input data of channel 4 of matrix row 1. SVE14[23]: Sign bit SVE14[22]: Integer bit SVE14[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.45 CTUn Scale Value e15 Register (CTUn_SV15R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV15R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE15[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE15[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE15[23:0]	H'00 0000	R/W	Scale Value e15 for Input Channel 5 of Matrix Row 1 These bits set the scale value for input data of channel 5 of matrix row 1. SVE15[23]: Sign bit SVE15[22]: Integer bit SVE15[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.46 CTUn Scale Value e16 Register (CTUn_SV16R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV16R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE16[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE16[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE16[23:0]	H'00 0000	R/W	Scale Value e16 for Input Channel 6 of Matrix Row 1 These bits set the scale value for input data of channel 6 of matrix row 1. SVE16[23]: Sign bit SVE16[22]: Integer bit SVE16[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.47 CTUn Scale Value e17 Register (CTUn_SV17R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV17R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE17[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE17[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE17[23:0]	H'00 0000	R/W	Scale Value e17 for Input Channel 7 of Matrix Row 1 These bits set the scale value for input data of channel 7 of matrix row 1. SVE17[23]: Sign bit SVE17[22]: Integer bit SVE17[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.48 CTUn Scale Value e20 Register (CTUn_SV20R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV20R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE20[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE20[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE20[23:0]	H'00 0000	R/W	Scale Value e20 for Input Channel 0 of Matrix Row 2 These bits set the scale value for input data of channel 0 of matrix row 2. SVE20[23]: Sign bit SVE20[22]: Integer bit SVE20[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.49 CTUn Scale Value e21 Register (CTUn_SV21R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV21R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE21[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE21[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE21[23:0]	H'00 0000	R/W	Scale Value e21 for Input Channel 1 of Matrix Row 2 These bits set the scale value for input data of channel 1 of matrix row 2. SVE21[23]: Sign bit SVE21[22]: Integer bit SVE21[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.50 CTUn Scale Value e22 Register (CTUn_SV22R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV22R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE22[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE22[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE22[23:0]	H'00 0000	R/W	Scale Value e22 for Input Channel 2 of Matrix Row 2 These bits set the scale value for input data of channel 2 of matrix row 2. SVE22[23]: Sign bit SVE22[22]: Integer bit SVE22[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.51 CTUn Scale Value e23 Register (CTUn_SV23R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV23R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE23[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE23[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE23[23:0]	H'00 0000	R/W	Scale Value e23 for Input Channel 3 of Matrix Row 2 These bits set the scale value for input data of channel 3 of matrix row 2. SVE23[23]: Sign bit SVE23[22]: Integer bit SVE23[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.52 CTUn Scale Value e24 Register (CTUn_SV24R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV24R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE24[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE24[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE24[23:0]	H'00 0000	R/W	Scale Value e24 for Input Channel 4 of Matrix Row 2 These bits set the scale value for input data of channel 4 of matrix row 2. SVE24[23]: Sign bit SVE24[22]: Integer bit SVE24[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.53 CTUn Scale Value e25 Register (CTUn_SV25R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV25R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE25[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE25[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE25[23:0]	H'00 0000	R/W	Scale Value e25 for Input Channel 5 of Matrix Row 2 These bits set the scale value for input data of channel 5 of matrix row 2. SVE25[23]: Sign bit SVE25[22]: Integer bit SVE25[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.54 CTUn Scale Value e26 Register (CTUn_SV26R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV26R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE26[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE26[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE26[23:0]	H'00 0000	R/W	Scale Value e26 for Input Channel 6 of Matrix Row 2 These bits set the scale value for input data of channel 6 of matrix row 2. SVE26[23]: Sign bit SVE26[22]: Integer bit SVE26[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.55 CTUn Scale Value e27 Register (CTUn_SV27R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV27R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 2.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE27[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE27[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE27[23:0]	H'00 0000	R/W	Scale Value e27 for Input Channel 7 of Matrix Row 2 These bits set the scale value for input data of channel 7 of matrix row 2. SVE27[23]: Sign bit SVE27[22]: Integer bit SVE27[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.56 CTUn Scale Value e30 Register (CTUn_SV30R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV30R is a 32-bit readable/writable register that sets the scale value for channel 0 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE30[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE30[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE30[23:0]	H'00 0000	R/W	Scale Value e30 for Input Channel 0 of Matrix Row 3 These bits set the scale value for input data of channel 0 of matrix row 3. SVE30[23]: Sign bit SVE30[22]: Integer bit SVE30[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.57 CTUn Scale Value e31 Register (CTUn_SV31R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV31R is a 32-bit readable/writable register that sets the scale value for channel 1 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE31[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE31[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE31[23:0]	H'00 0000	R/W	Scale Value e31 for Input Channel 1 of Matrix Row 3 These bits set the scale value for input data of channel 1 of matrix row 3. SVE31[23]: Sign bit SVE31[22]: Integer bit SVE31[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.58 CTUn Scale Value e32 Register (CTUn_SV32R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV32R is a 32-bit readable/writable register that sets the scale value for channel 2 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE32[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE32[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE32[23:0]	H'00 0000	R/W	Scale Value e32 for Input Channel 2 of Matrix Row 3 These bits set the scale value for input data of channel 2 of matrix row 3. SVE32[23]: Sign bit SVE32[22]: Integer bit SVE32[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.59 CTUn Scale Value e33 Register (CTUn_SV33R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV33R is a 32-bit readable/writable register that sets the scale value for channel 3 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE33[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE33[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE33[23:0]	H'00 0000	R/W	Scale Value e33 for Input Channel 3 of Matrix Row 3 These bits set the scale value for input data of channel 3 of matrix row 3. SVE33[23]: Sign bit SVE33[22]: Integer bit SVE33[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.60 CTUn Scale Value e34 Register (CTUn_SV34R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV34R is a 32-bit readable/writable register that sets the scale value for channel 4 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE34[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE34[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

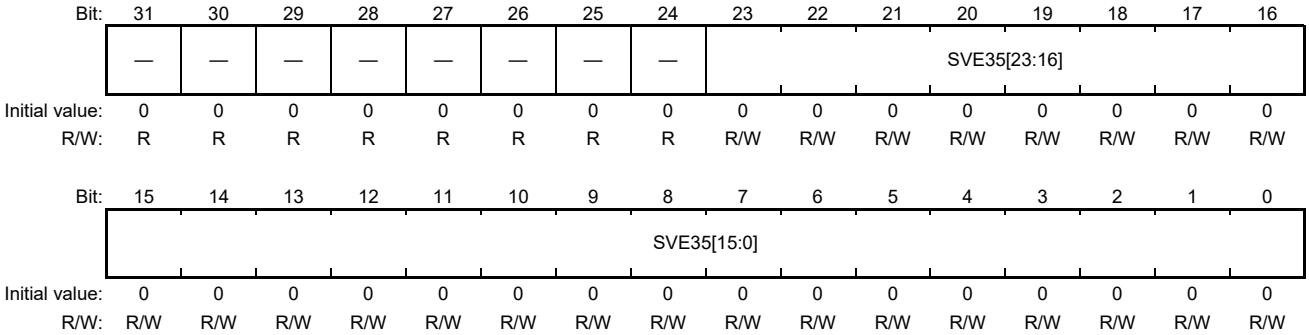
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE34[23:0]	H'00 0000	R/W	Scale Value e34 for Input Channel 4 of Matrix Row 3 These bits set the scale value for input data of channel 4 of matrix row 3. SVE34[23]: Sign bit SVE34[22]: Integer bit SVE34[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.61 CTUn Scale Value e35 Register (CTUn_SV35R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV35R is a 32-bit readable/writable register that sets the scale value for channel 5 of matrix row 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE35[23:0]	H'00 0000	R/W	Scale Value e35 for Input Channel 5 of Matrix Row 3 These bits set the scale value for input data of channel 5 of matrix row 3. SVE35[23]: Sign bit SVE35[22]: Integer bit SVE35[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.62 CTUn Scale Value e36 Register (CTUn_SV36R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV36R is a 32-bit readable/writable register that sets the scale value for channel 6 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE36[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE36[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE36[23:0]	H'00 0000	R/W	Scale Value e36 for Input Channel 6 of Matrix Row 3 These bits set the scale value for input data of channel 6 of matrix row 3. SVE36[23]: Sign bit SVE36[22]: Integer bit SVE36[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.63 CTUn Scale Value e37 Register (CTUn_SV37R)

Note: n = 00, 01, 02, 03, 10, 11, 12, or 13

Function: CTUn_SV37R is a 32-bit readable/writable register that sets the scale value for channel 7 of matrix row 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	SVE37[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SVE37[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	SVE37[23:0]	H'00 0000	R/W	Scale Value e37 for Input Channel 7 of Matrix Row 3 These bits set the scale value for input data of channel 7 of matrix row 3. SVE37[23]: Sign bit SVE37[22]: Integer bit SVE37[21:0]: Decimal bits

plus			minus		
Value	**[time]**	**[dB]**	**Value**	**[time]**	**[dB]**
H'7F FFFF	2	6	H'80 0000	2	6
.....	.....	.....	.....	.....	.....
H'40 0000	1	0	H'C0 0000	1	0
.....	.....	.....	.....	.....	.....
H'00 0001	2.38×10^{-7}	-132	.....	.....	.....
H'00 0000	0 (Mute)	-∞	H'FF FFFF	2.38×10^{-7}	-132

30.2.64 MIXp Software Reset Register (MIXp_SWRSR)

Note: p = 0 or 1

Function: MIXp_SWRSR is a 32-bit readable/writable register that controls operation/reset of the MIX internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the MIX internal circuits are put in the reset state. MIXp_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the MIX 1: Operating state

30.2.65 MIXp MIX Initialization Register (MIXp_MIXIR)

Note: p = 0 or 1

Function: MIXp_MIXIR is a 32-bit readable/writable register that initializes the operation of the MIX internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the MIX processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

30.2.66 MIXp Audio Information Register (MIXp_ADINR)

Note: p = 0 or 1

Function: MIXp_ADINR is a 32-bit readable/writable register that selects channel number.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved

30.2.67 MIXp MIX Mode Register (MIXp_MIXMR)

Note: p = 0 or 1

Function: MIXp_MIXMR is a 32-bit readable/writable register that controls the mix mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MIX MODE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MIXMODE	0	R/W	MIX Mode This bit controls the mix mode. 0: Selects volume step mixer 1: Selects volume ramp mixer

30.2.68 MIXp MIX Volume Period Register (MIXp_MVPDR)

Note: p = 0 or 1

Function: MIXp_MVPDR is a 32-bit readable/writable register that sets the value of the change of the volume a sample.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MXPDUP[3:0]				—	—	—	—	MXPDDW[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	MXPDUP[3:0]	0000	R/W	MIX Period for Volume Up These bits set the decibel value that changed by one sample for volume up. And when MIXMODE bit of MIXp_MIXMR register is 1, this setting can be used. 0000: 128 dB / 1 sample 0001: 64 dB / 1 sample 0010: 32 dB / 1 sample 0011: 16 dB / 1 sample 0100: 8 dB / 1 sample 0101: 4 dB / 1 sample 0110: 2 dB / 1 sample 0111: 1 dB / 1 sample 1000: 0.5 dB / 1 sample 1001: 0.25 dB / 1 sample 1010: 0.125 dB / 1 sample 1011 to 1111: Reserved
7 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	MXPDDW[3:0]	0000	R/W	MIX Period for Volume Down These bits set the decibel value that changed by one sample for volume down. And when MIXMODE bit of MIXp_MIXMR register is 1, this setting can be used. 0000: -128 dB / 1 sample 0001: -64 dB / 1 sample 0010: -32 dB / 1 sample 0011: -16 dB / 1 sample 0100: -8 dB / 1 sample 0101: -4 dB / 1 sample 0110: -2 dB / 1 sample 0111: -1 dB / 1 sample 1000: -0.5 dB / 1 sample 1001: -0.25 dB / 1 sample 1010: -0.125 dB / 1 sample 1011 to 1111: Reserved

30.2.69 MIXp MIX Decibel A Register (MIXp_MDBAR)

Note: p = 0 or 1

Function: MIXp_MDBAR is a 32-bit readable/writable register that sets the decibel (gain level) of system A.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MIXDBA[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBA[9:0]	H'000	R/W	dB of System A These bits control the decibel (gain level) of system A. The value can select 1024 points from 0 dB to -∞ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	……	……	……
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	……	……
.....	.....	.....	H'3FE	4.1×10^{-7}	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	-∞

The relation between the setting value and the decibel is shown in Tables 30.9, 30.10, 30.11 and 30.12.

30.2.70 MIXp MIX Decibel B Register (MIXp_MDBBR)

Note: p = 0 or 1

Function: MIXp_MDBBR is a 32-bit readable/writable register that sets the decibel (gain level) of system B.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MIXDBB[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBB[9:0]	H'000	R/W	dB of System B These bits control the decibel (gain level) of system B. The value can select 1024 points from 0 dB to -∞ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	……	……	……
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	……	……
.....	.....	.....	H'3FE	4.1×10^{-7}	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	-∞

The relation between the setting value and the decibel is shown in Tables 30.9, 30.10, 30.11 and 30.12.

30.2.71 MIXp MIX Decibel C Register (MIXp_MDBCR)

Note: p = 0 or 1

Function: MIXp_MDBCR is a 32-bit readable/writable register that sets the decibel (gain level) of system C.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MIXDBC[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBC[9:0]	H'000	R/W	dB of System C These bits control the decibel (gain level) of system C. The value can select 1024 points from 0 dB to -∞ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	……	……	……
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	……	……
.....	.....	.....	H'3FE	4.1×10^{-7}	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	-∞

The relation between the setting value and the decibel is shown in Tables 30.9, 30.10, 30.11 and 30.12.

30.2.72 MIXp MIX Decibel D Register (MIXp_MDBDR)

Note: p = 0 or 1

Function: MIXp_MDBDR is a 32-bit readable/writable register that sets the decibel (gain level) of system D.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MIXDBD[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	MIXDBD[9:0]	H'000	R/W	dB of System D These bits control the decibel (gain level) of system D. The value can select 1024 points from 0 dB to -∞ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	……	……	……
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	……	……
.....	.....	.....	H'3FE	4.1×10^{-7}	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	-∞

The relation between the setting value and the decibel is shown in Tables 30.9, 30.10, 30.11 and 30.12.

30.2.73 MIXp MIX Decibel Enable Register (MIXp_MDBER)

Note: p = 0 or 1

Function: MIXp_MDBER is a 32-bit readable/writable register that controls the dB value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MIX DBEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	MIXDBEN	0	R/W	MIX dB Enable This bit controls the dB value that sets in MIXp_MDBAR, MIXp_MDBBR, MIXp_MDBCR and MIXp_MDBDR registers. 0: Disables the setting of dB 1: Enables the setting of dB

30.2.74 MIXp MIX Status Register (MIXp_MIXSR)

Note: p = 0 or 1

Function: MIXp_MIXSR is a 32-bit readable register that indicates the status of the volume ramp.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MRPSTS	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	MRPSTS	00	R	MIX Volume Ramp Status These bits indicate the volume ramp status of mix operation. 00: Level of volume ramp is stable 01: Volume ramp down 10: Volume ramp up

30.2.75 DVCp Software Reset Register (DVCp_SWRSR)

Note: p = 0 or 1

Function: DVCp_SWRSR is a 32-bit readable/writable register that controls operation/reset of the DVC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWRST	1	R/W	Software Reset While this bit is 0, the DVC internal circuits are put in the reset state. DVCp_* registers except this register are reset. Therefore, they should be set again after the reset is canceled. 0: Resets the DVC 1: Operating state

30.2.76 DVCp DVU Initialization Register (DVCp_DVUIR)

Note: p = 0 or 1

Function: DVCp_DVUIR is a 32-bit readable/writable register that initializes the operation of the DVC internal circuits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	INIT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	INIT	1	R/W	Initialization of Processing When this bit is set to 1, the DVC processing is initialized. This bit should be cleared to 0 after it was set to 1. 0: Processing State 1: Initialization (sets the initial setting of other registers)

30.2.77 DVCp Audio Information Register (DVCp_ADINR)

Note: p = 0 or 1

Function: DVCp_ADINR is a 32-bit readable/writable register that selects channel number and bit length of output audio data.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	OTBL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	CHNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20 to 16	OTBL[4:0]	00000	R/W	Bit Length of Output Audio Data. These bits set the bit length of output audio data. 00000: 24 bits 00001: Reserved 00010: 22 bits 00011: Reserved 00100: 20 bits 00101: Reserved 00110: 18 bits 00111: Reserved 01000: 16 bits 01001 to 01111: Reserved 10000: 8 bits 10001 to 11111: Reversed
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	CHNUM[3:0]	0000	R/W	Channel Number These bits set the channel number 0000: 0 (None) 0001: 1 channel 0010: 2 channels 0011: Reserved 0100: 4 channels 0101: Reserved 0110: 6 channels 0111: Reserved 1000: 8 channels 1001 to 1111: Reserved

30.2.78 DVCp DVU Control Register (DVCp_DVUCR)

Note: p = 0 or 1

Function: DVCp_DVUCR is a 32-bit readable/writable register that selects the mode of function to operate.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	HWMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	VVMD	—	—	—	VRMD	—	—	—	ZCMD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	HWMD	0	R/W	Enable the DVC_MUTE pin This bit enables DVC_MUTE pin for the setting of DVCEN bit of DVCp_DVUER register. (Set enable only. To set disable, write 0 DVCEN bit) 0: Disables the DVC_MUTE pin 1: Enables the DVC_MUTE pin
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	VVMD	0	R/W	Select Digital Volume Value Mode This bit selects the digital volume value function. 0: Sleep the digital volume value function 1: Use the digital volume value function
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VRMD	0	R/W	Select Volume Ramp Mode This bit selects the volume ramp function. 0: Sleep the volume ramp function 1: Use the volume ramp function
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ZCMD	0	R/W	Select Zero Cross Mute Mode This bit selects the zero cross mute function. 0: Sleep the zero cross mute function 1: Use the zero cross mute function

30.2.79 DVCp Zero Cross Mute Control Register (DVCp_ZCMCR)

Note: p = 0 or 1

Function: DVCp_ZCMCR is a 32-bit readable/writable register that controls the operation of the zero cross mute function for each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ZCEN7	ZCEN6	ZCEN5	ZCEN4	ZCEN3	ZCEN2	ZCEN1	ZCEN0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	ZCEN7	0	R/W	Zero Cross Mute Enable for Channel 7 This bit controls the operation of the zero cross mute function for channel 7. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
6	ZCEN6	0	R/W	Zero Cross Mute Enable for Channel 6 This bit controls the operation of the zero cross mute function for channel 6. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
5	ZCEN5	0	R/W	Zero Cross Mute Enable for Channel 5 This bit controls the operation of the zero cross mute function for channel 5. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
4	ZCEN4	0	R/W	Zero Cross Mute Enable for Channel 4 This bit controls the operation of the zero cross mute function for channel 4. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
3	ZCEN3	0	R/W	Zero Cross Mute Enable for Channel 3 This bit controls the operation of the zero cross mute function for channel 3. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function

Bit	Bit Name	Initial Value	R/W	Description
2	ZCEN2	0	R/W	Zero Cross Mute Enable for Channel 2 This bit controls the operation of the zero cross mute function for channel 2. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
1	ZCEN1	0	R/W	Zero Cross Mute Enable for Channel 1 This bit controls the operation of the zero cross mute function for channel 1. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function
0	ZCEN0	0	R/W	Zero Cross Mute Enable for Channel 0 This bit controls the operation of the zero cross mute function for channel 0. 0: Disables the operation of the zero cross mute function 1: Enables the operation of the zero cross mute function

30.2.80 DVCp Volume Ramp Control Register (DVCp_VRCTR)

Note: p = 0 or 1

Function: DVCp_VRCTR is a 32-bit readable/writable register that controls the operation of the volume ramp function for each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	VREN7	VREN6	VREN5	VREN4	VREN3	VREN2	VREN1	VREN0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	VREN7	0	R/W	Volume Ramp Enable for Channel 7 This bit controls the operation of the volume ramp function for channel 7. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
6	VREN6	0	R/W	Volume Ramp Enable for Channel 6 This bit controls the operation of the volume ramp function for channel 6. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
5	VREN5	0	R/W	Volume Ramp Enable for Channel 5 This bit controls the operation of the volume ramp function for channel 5. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
4	VREN4	0	R/W	Volume Ramp Enable for Channel 4 This bit controls the operation of the volume ramp function for channel 4. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
3	VREN3	0	R/W	Volume Ramp Enable for Channel 3 This bit controls the operation of the volume ramp function for channel 3. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
2	VREN2	0	R/W	Volume Ramp Enable for Channel 2 This bit controls the operation of the volume ramp function for channel 2. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function
1	VREN1	0	R/W	Volume Ramp Enable for Channel 1 This bit controls the operation of the volume ramp function for channel 1. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function

Bit	Bit Name	Initial Value	R/W	Description
0	VREN0	0	R/W	Volume Ramp Enable for Channel 0 This bit controls the operation of the volume ramp function for channel 0. 0: Disables the operation of the volume ramp function 1: Enables the operation of the volume ramp function

Note: All of these bits should be set to 1 when VRMD bit of DVCp_DVUCR register is 1.

30.2.81 DVCp Volume Ramp Period Register (DVCp_VRPDR)

Note: p = 0 or 1

Function: DVCp_VRPDR is a 32-bit readable/writable register that controls.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	VRPDUP[4:0]					—	—	—	VRPDDW[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	VRPDUP[4:0]	00000	R/W	Volume Ramp Period for Volume Up 00000: 1 [sample] (128 dB/1 step) 00001: 2 [sample] (64 dB/1 step) 00010: 4 [sample] (32 dB/1 step) 00011: 8 [sample] (16 dB/1 step) 00100: 16 [sample] (8 dB/1 step) 00101: 32 [sample] (4 dB/1 step) 00110: 64 [sample] (2 dB/1 step) 00111: 128 [sample] (1 dB/1 step) 01000: 256 [sample] (0.5 dB/1 step) 01001: 512 [sample] (0.25 dB/1 step) 01010: 1024 [sample] (0.125 dB/1 step) 01011: 2048 [sample] (0.125 dB/2 steps) 01100: 4096 [sample] (0.125 dB/4 steps) 01101: 8192 [sample] (0.125 dB/8 steps) 01110: 16384 [sample] (0.125 dB/16 steps) 01111: 32768 [sample] (0.125 dB/32 steps) 10000: 65536 [sample] (0.125 dB/64 steps) 10001: 131072 [sample] (0.125 dB/128 steps) 10010: 262144 [sample] (0.125 dB/256 steps) 10011: 524288 [sample] (0.125 dB/512 steps) 10100: 1048576 [sample] (0.125 dB/1024 steps) 10101: 2097152 [sample] (0.125 dB/2048 steps) 10110: 4194304 [sample] (0.125 dB/4096 steps) 10111: 8388608 [sample] (0.125 dB/8192 steps) 11000 to 11111: Reserved
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4 to 0	VRPDDW[4:0]	00000	R/W	Volume Ramp Period for Volume Down 00000: 1 [sample] (-128 dB/1 step) 00001: 2 [sample] (-64 dB/1 step) 00010: 4 [sample] (-32 dB/1 step) 00011: 8 [sample] (-16 dB/1 step) 00100: 16 [sample] (-8 dB/1 step) 00101: 32 [sample] (-4 dB/1 step) 00110: 64 [sample] (-2 dB/1 step) 00111: 128 [sample] (-1 dB/1 step) 01000: 256 [sample] (-0.5 dB/1 step) 01001: 512 [sample] (-0.25 dB/1 step) 01010: 1024 [sample] (-0.125 dB/1 step) 01011: 2048 [sample] (-0.125 dB/2 steps) 01100: 4096 [sample] (-0.125 dB/4 steps) 01101: 8192 [sample] (-0.125 dB/8 steps) 01110: 16384 [sample] (-0.125 dB/16 steps) 01111: 32768 [sample] (-0.125 dB/32 steps) 10000: 65536 [sample] (-0.125 dB/64 steps) 10001: 131072 [sample] (-0.125 dB/128 steps) 10010: 262144 [sample] (-0.125 dB/256 steps) 10011: 524288 [sample] (-0.125 dB/512 steps) 10100: 1048576 [sample] (-0.125 dB/1024 steps) 10101: 2097152 [sample] (-0.125 dB/2048 steps) 10110: 4194304 [sample] (-0.125 dB/4096 steps) 10111: 8388608 [sample] (-0.125 dB/8192 steps) 11000 to 11111: Reserved

30.2.82 DVCp Volume Ramp Decibel Register (DVCp_VRDBR)

Note: p = 0 or 1

Function: DVCp_VRDBR is a 32-bit readable/writable register that sets the decibel (gain level) of volume ramp.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	VRDB[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	VRDB[9:0]	H'000	R/W	dB of Volume Ramp These bits control the decibel (gain level) of volume ramp. The value can select 1024 points from 0 dB to -∞ dB at intervals of 0.125 dB.

Value	[time]	[dB]	Value	[time]	[dB]
H'000	1	0	……	……	……
.....	.....	.....	H'091	0.125	-18.125
H'031	0.5	-6.125	.....	……	……
.....	.....	.....	H'3FE	4.1×10^{-7}	-127.75
H'061	0.25	-12.125	H'3FF	0 (Mute)	-∞

The relation between the setting value and the decibel is shown in Tables 30.9, 30.10, 30.11 and 30.12.

30.2.83 DVCp Volume Ramp Wait Time Register (DVCp_VRWTR)

Note: p = 0 or 1

Function: DVCp_VRWTR is a 32-bit readable/writable register that sets the standby time to start the operation of the volume ramp function.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VRWT[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VRWT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VRWT[23:0]	H'00 0000	R/W	Volume Ramp Wait Time These bits set the standby time to adjust the start timing of operation of the volume ramp function when the setting of DVCp_VRDBR register is changed. If the internal counter of the DVC logic reached to the value of these bits, the volume ramp function starts to operate to change the volume to target volume of DVCp_VRDBR register.

30.2.84 DVCp Volume Value Setting 0 Register (DVCp_VOL0R)

Note: p = 0 or 1

Function: DVCp_VOL0R is a 32-bit readable/writable register that sets digital volume value for channel 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VOLVAL0[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VOLVAL0[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL0 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 0 These bits set the digital volume of channel 0. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL0[23]: Sign bit (The write value should be 0.) VOLVAL0[22:20]: Integer bits VOLVAL0[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.85 DVCp Volume Value Setting 1 Register (DVCp_VOL1R)

Note: p = 0 or 1

Function: DVCp_VOL1R is a 32-bit readable/writable register that sets digital volume value for channel 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VOLVAL1[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VOLVAL1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

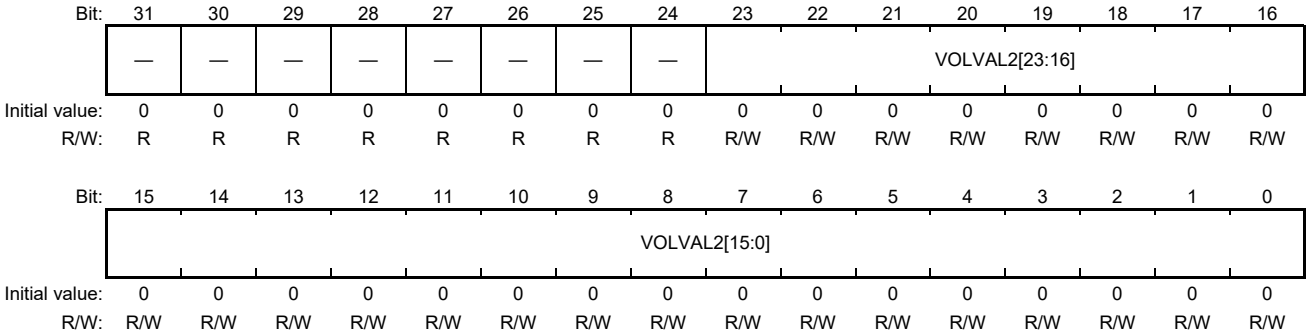
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL1 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 1 These bits set the digital volume of channel 1. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL1[23]: Sign bit (The write value should be 0.) VOLVAL1[22:20]: Integer bits VOLVAL1[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.86 DVCp Volume Value Setting 2 Register (DVCp_VOL2R)

Note: p = 0 or 1

Function: DVCp_VOL2R is a 32-bit readable/writable register that sets digital volume value for channel 2.



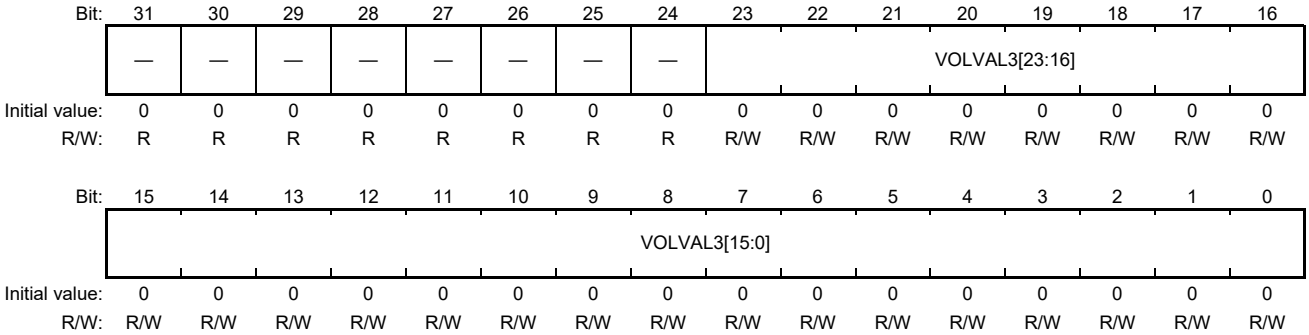
Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL2 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 2 These bits set the digital volume of channel 2. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL2[23]: Sign bit (The write value should be 0.) VOLVAL2[22:20]: Integer bits VOLVAL2[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.87 DVCp Volume Value Setting 3 Register (DVCp_VOL3R)

Note: p = 0 or 1

Function: DVCp_VOL3R is a 32-bit readable/writable register that sets digital volume value for channel 3.



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL3 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 3 These bits set the digital volume of channel 3. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL3[23]: Sign bit (The write value should be 0.) VOLVAL3[22:20]: Integer bits VOLVAL3[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.88 DVCp Volume Value Setting 4 Register (DVCp_VOL4R)

Note: p = 0 or 1

Function: DVCp_VOL4R is a 32-bit readable/writable register that sets digital volume value for channel 4.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VOLVAL4[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VOLVAL4[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL4 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 4 These bits set the digital volume of channel 4. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL4[23]: Sign bit (The write value should be 0.) VOLVAL4[22:20]: Integer bits VOLVAL4[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.89 DVCp Volume Value Setting 5 Register (DVCp_VOL5R)

Note: p = 0 or 1

Function: DVCp_VOL5R is a 32-bit readable/writable register that sets digital volume value for channel 5.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VOLVAL5[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VOLVAL5[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL5 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 5 These bits set the digital volume of channel 5. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL5[23]: Sign bit (The write value should be 0.) VOLVAL5[22:20]: Integer bits VOLVAL5[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.90 DVCp Volume Value Setting 6 Register (DVCp_VOL6R)

Note: p = 0 or 1

Function: DVCp_VOL6R is a 32-bit readable/writable register that sets digital volume value for channel 6.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VOLVAL6[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VOLVAL6[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL6 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 6 These bits set the digital volume of channel 6. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL6[23]: Sign bit (The write value should be 0.) VOLVAL6[22:20]: Integer bits VOLVAL6[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.91 DVCp Volume Value Setting 7 Register (DVCp_VOL7R)

Note: p = 0 or 1

Function: DVCp_VOL7R is a 32-bit readable/writable register that sets digital volume value for channel 7.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	VOLVAL7[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VOLVAL7[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	VOLVAL7 [23:0]	H'00 0000	R/W	Digital Volume Value for Channel 7 These bits set the digital volume of channel 7. The maximum value is 8-time (18 dB) and the minimum value is 0 (-∞ dB). VOLVAL7[23]: Sign bit (The write value should be 0.) VOLVAL7[22:20]: Integer bits VOLVAL7[19:0]: Decimal bits

Value	[time]	[dB]	Value	[time]	[dB]
H'7F FFFF	8	18	H'08 0000	0.5	-6
…	…	…	…	…	…
H'10 0000	1	0	H'00 0001	9.5×10^{-7}	-120
…	…	…	H'00 0000	0	-∞

30.2.92 DVCp DVU Enable Register (DVCp_DVUER)

Note: p = 0 or 1

Function: DVCp_DVUER is a 32-bit readable/writable register that controls the setting of DVC registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DVCEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DVCEN	0	R/W	DVC Register Setting Enable This bit controls the setting of DVC registers (DVCp_ZCMCR, DVCp_VRCTR, DVCp_VRPDR, DVCp_VRDBR, DVCp_VOL0R, DVCp_VOL1R, DVCp_VOL2R, DVCp_VOL3R, DVCp_VOL4R, DVCp_VOL5R, DVCp_VOL6R, DVCp_VOL7R). 0: Disables the setting of dvc registers to DVC logic 1: Enables the setting of dvc registers to DVC logic

30.2.93 DVCp DVU Status Register (DVCp_DVUSR)

Note: p = 0, 1

Function: DVCp_DVUSR is a 32-bit readable register that indicates the status of the zero cross mute and the volume ramp. This register is used for debug.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ALLZSTS	ZSTS7	ZSTS6	ZSTS5	ZSTS4	ZSTS3	ZSTS2	ZSTS1	ZSTS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VRSTS_LEVEL	VRSTS_MUTE	VRSTS[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	ALLZSTS	0	R	All-Channel Zero Cross Mute Status 0: Not all-channel zero cross mute state 1: All-channel zero cross mute state Note: The state is determined only based on the channels for which the zero cross mute function is set.
23	ZSTS7	0	R	Zero Cross Mute Status of Channel 7 This bit indicates the zero cross mute status of channel 7. 0: Not mute status 1: Mute status
22	ZSTS6	0	R	Zero Cross Mute Status of Channel 6 This bit indicates the zero cross mute status of channel 6. 0: Not mute status 1: Mute status
21	ZSTS5	0	R	Zero Cross Mute Status of Channel 5 This bit indicates the zero cross mute status of channel 5. 0: Not mute status 1: Mute status
20	ZSTS4	0	R	Zero Cross Mute Status of Channel 4 This bit indicates the zero cross mute status of channel 4. 0: Not mute status 1: Mute status
19	ZSTS3	0	R	Zero Cross Mute Status of Channel 3 This bit indicates the zero cross mute status of channel 3. 0: Not mute status 1: Mute status
18	ZSTS2	0	R	Zero Cross Mute Status of Channel 2 This bit indicates the zero cross mute status of channel 2. 0: Not mute status 1: Mute status

Bit	Bit Name	Initial Value	R/W	Description
17	ZSTS1	0	R	Zero Cross Mute Status of Channel 1 This bit indicates the zero cross mute status of channel 1. 0: Not mute status 1: Mute status
16	ZSTS0	0	R	Zero Cross Mute Status of Channel 0 This bit indicates the zero cross mute status of channel 0. 0: Not mute status 1: Mute status
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VRSTS_LEVEL	0	R	Volume Ramp Level Status 0: The volume ramp level is not the level specified by the DVCp_VRDBR register. (VRSTS is not 011.) 1: The volume ramp level is the level specified by the DVCp_VRDBR register. (VRSTS is 011.)
3	VRSTS_MUTE	1	R	Volume Ramp Mute Status 0: Not mute status 1: Mute status
2 to 0	VRSTS[2:0]	000	R	Volume Ramp Status These bits indicate the volume ramp status. 000: Mute status 001: Volume ramp down 010: Volume ramp up 011: The volume ramp level is not the level specified by the DVCp_VRDBR register. 100: Volume of input data is maintained (Volume is 1-time) 101~111: Reserved bits

30.2.94 DVCp Interrupt Enable Register (DVCp_DVIER)

Note: p = 0, 1

Function: DVCp_DVIER enables or disables output of interrupts corresponding to the states indicated in the DVCp_DVUSR register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	ALLZSTS_ie	ZSTS7_ie	ZSTS6_ie	ZSTS5_ie	ZSTS4_ie	ZSTS3_ie	ZSTS2_ie	ZSTS1_ie	ZSTS0_ie
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	VRSTS_LEVEL_ie	VRSTS_MUTE_ie	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	ALLZSTS_ie	0	R/W	allzsts_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
23	ZSTS7_ie	0	R/W	zsts7_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
22	ZSTS6_ie	0	R/W	zsts6_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
21	ZSTS5_ie	0	R/W	zsts5_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
20	ZSTS4_ie	0	R/W	zsts4_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
19	ZSTS3_ie	0	R/W	zsts3_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
18	ZSTS2_ie	0	R/W	zsts2_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
17	ZSTS1_ie	0	R/W	zsts1_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
16	ZSTS0_ie	0	R/W	zsts0_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
15 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	VRSTS_LEVEL_ie	0	R/W	vrsts_level_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	VRSTS_MUTE_ie	0	R/W	vrsts_mute_int_enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

30.2.95 SRCm in Write Data Register (SRCm in_BUSIF)

Note: m = 1 to 6

Function: SRCm in_BUSIF are window registers in which data is stored during data transfer via SRCm in_BUSIF. These registers are used for transmission.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SRC*m* in_BUSIF															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

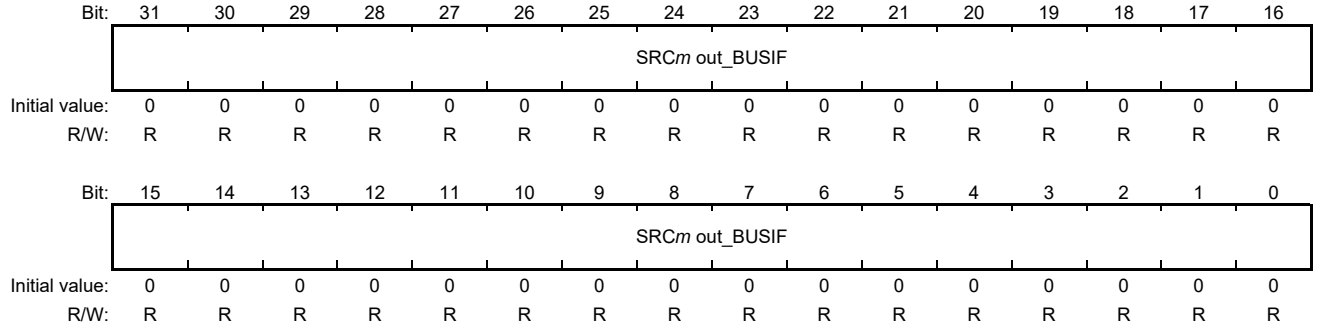
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRC*m* in_BUSIF															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W	-/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRC*m* in_BUSIF	All 0	-/W	These bits are a window register in which data is stored during data transfer via SRC*m*in_BUSIF. This register is used for transmission.

30.2.96 SRCm out Read Data Register (SRCm out_BUSIF)

Note: m = 1 to 6

Function: SRCm out_BUSIF are window registers in which data is stored during data transfer via SRCm out_BUSIF. These registers are used for reception.

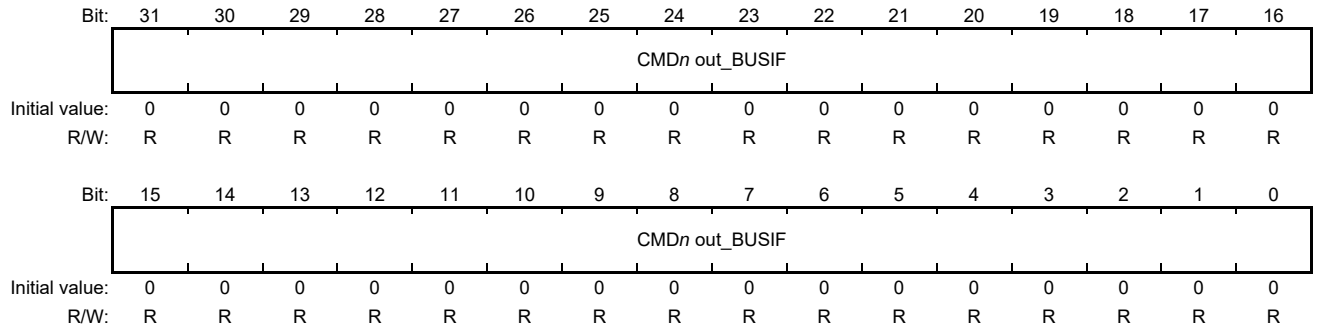


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SRC*m* out_BUSIF	All 0	R	These bits are a window register in which data is stored during data transfer via SRC*m*out_BUSIF. This register is used for reception.

30.2.97 CMDn out Read Data Register (CMDn out_BUSIF)

Note: n = 0 or 1

Function: CMDn out_BUSIF are window registers in which data is stored during data transfer via CMDn out_BUSIF. These registers are used for reception.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CMD*n* out_BUSIF	All 0	R	These bits are a window register in which data is stored during data transfer via CMD*n*out_BUSIF. This register is used for reception.

30.3 Operation

30.3.1 Procedure for Initializing the SCU

Figures 30.2 and 30.3 show the procedure for initializing the SCU. For details on the register settings, refer to section 30.2, Register Description.

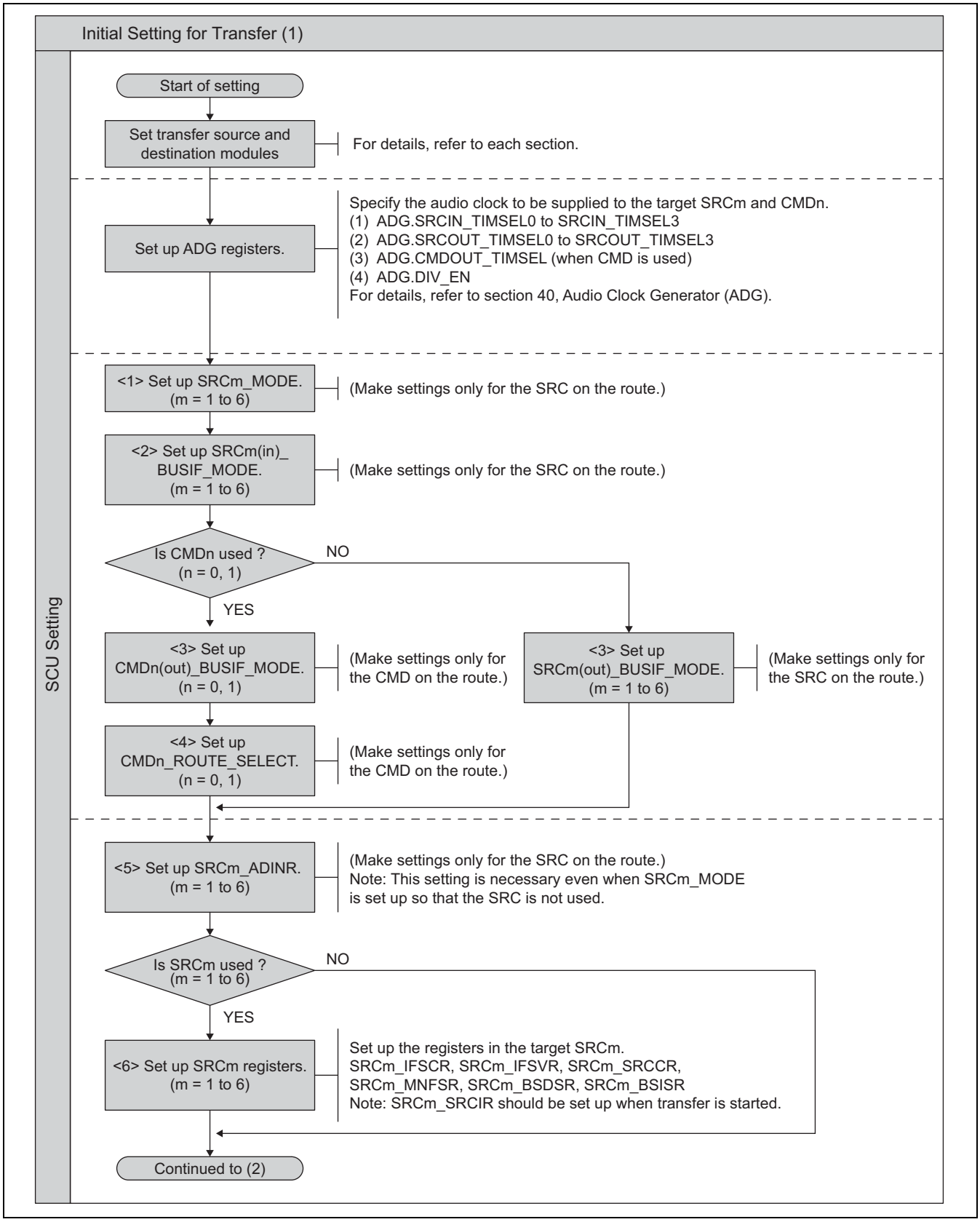


Figure 30.2 Procedure for Initializing the SCU (1)

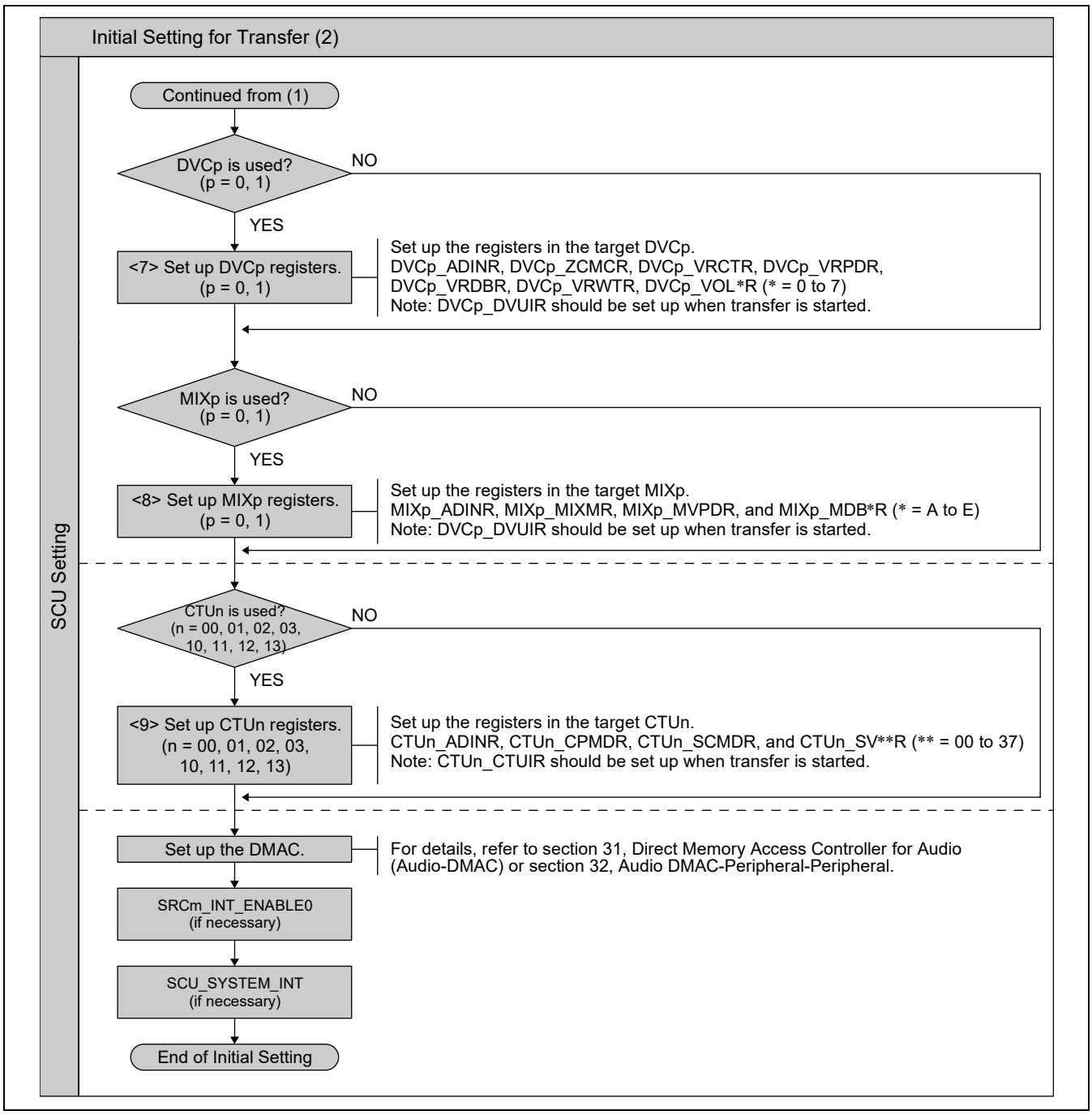


Figure 30.3 Procedure for Initializing the SCU (2)

30.3.2 Procedure for Starting and Stopping Transfer by the SCU

Figure 30.4 shows the procedure for starting and stopping the transfer by the SCU. For details on the register settings, refer to section 30.2, Register Description.

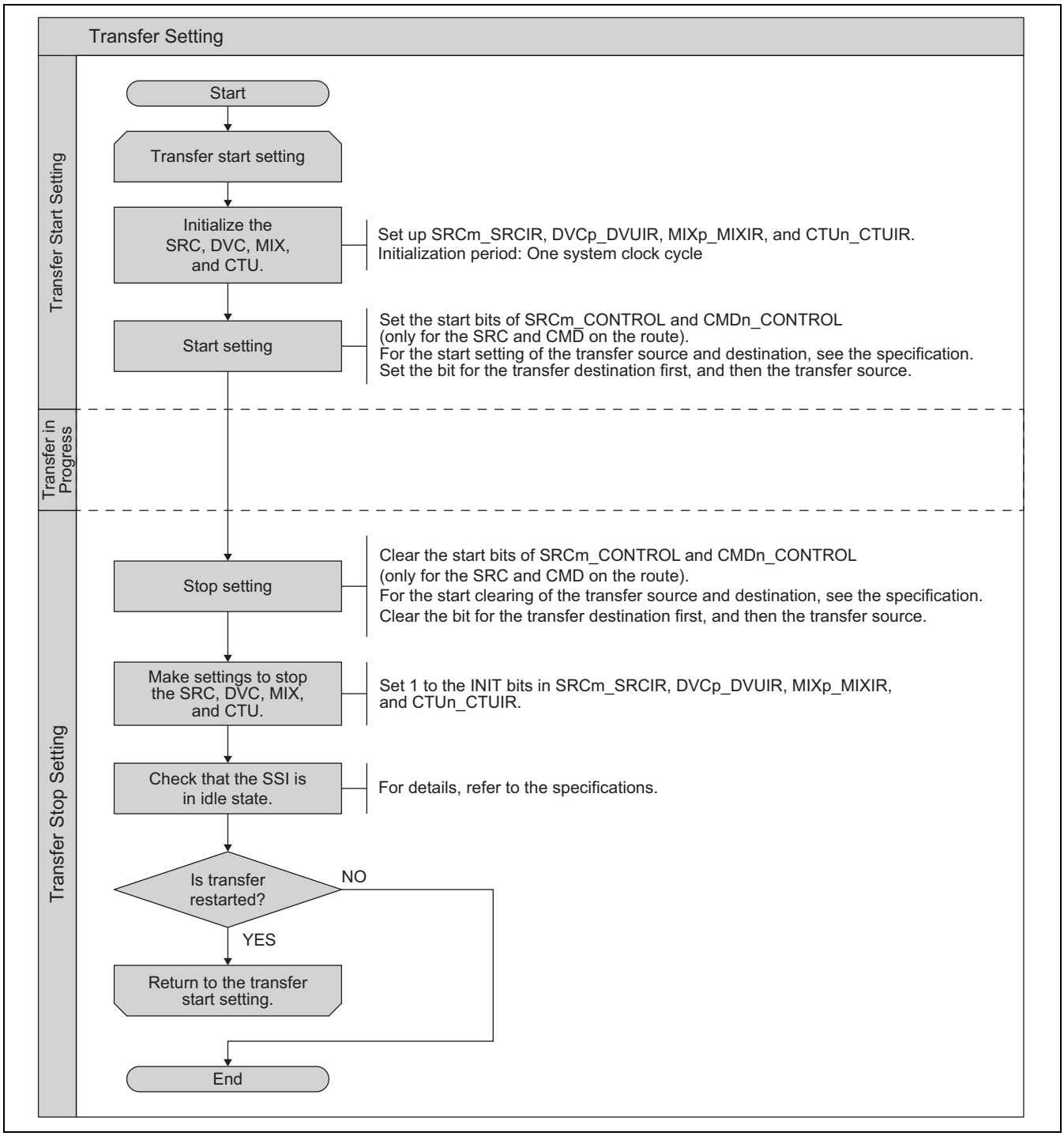
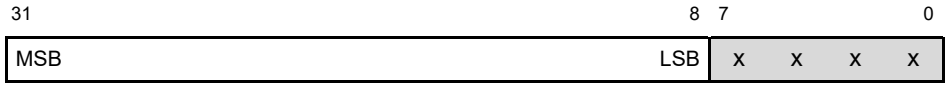
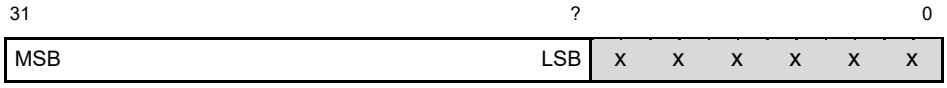
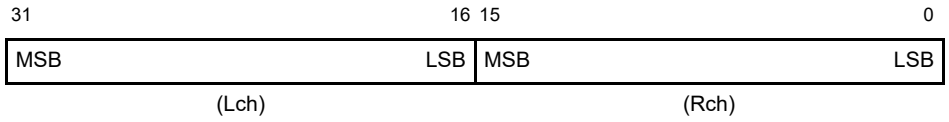
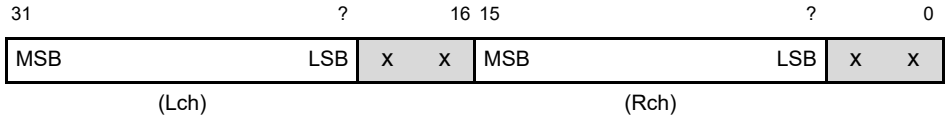
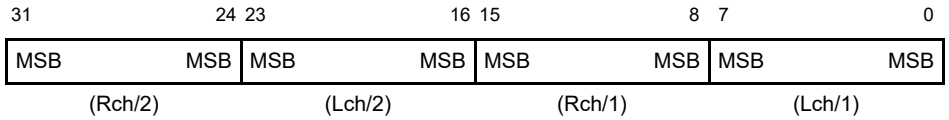
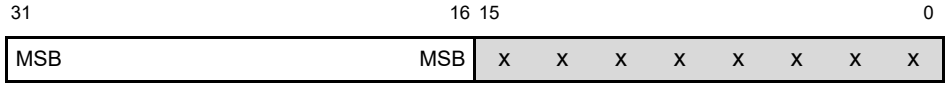
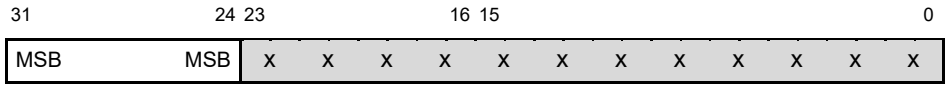


Figure 30.4 Procedure for Starting and Stopping Transfer by the SCU

30.3.3 Data Format for Data Transfer BUSIF

Table 30.3 shows the data formats handled in the SCU. When writing or reading data through the data transfer BUSIF (SRCm in_BUSIF, SRCm out_BUSIF, or CMDn out_BUSIF), align data to match the appropriate data format from those in Table 30.3. Data alignment can be changed through the SRCm(in/out)_BUSIF_MODE, SRCm_MODE register or CMDnout_BUSIF_MODE register (see section 30.2.4, SRCm_MODE Register (SRCm_MODE) or section 30.2.10, CMDn out_BUSIF_MODE Register (CMDn out_BUSIF_MODE)).

Table 30.3 Data Formats Handled in the SCU

24-bit stereo data, multichannel data	
17- to 23-bit stereo data, multichannel data	
16-bit stereo data, multichannel data	
9- to 15-bit stereo data, multichannel data	
8-bit stereo data	
16-bit monaural data	
8-bit monaural data	

Notes: 1. Write 0 to the "x" bits in the table when writing data through the data transfer SRCm in_BUSIF. When reading data through the SRCm out_BUSIF or CMDn out_BUSIF, ignore the values read from these bits.
2. In the 8-bit stereo data format, (Lch/1) and (Rch/1) indicate the data pair to be processed first and (Lch/2) and (Rch/2) indicate the next data pair to be processed.
3. Only the MSB-first data formats can be used in the SRU.

30.3.4 Changing Data Order in Channel Units

The data order can be changed in channel units in the SCU immediately before input to the SRC and immediately after output from the CMD. Tables 30.4 and 30.5 show the data places in each data format. Use SRCm_BUSIF_DALIGN or SRCn_BUSIF_DALIGN to change the order before input to the SRC (see section 30.2.2, SRCm_BUSIF_DALIGN Register (SRCm_BUSIF_DALIGN) or section 30.2.3, SRCn_BUSIF_DALIGN Register (SRCn_BUSIF_DALIGN). Use CMDn_BUSIF_DALIGN to change the order immediately after output from the CMD (see section 30.2.11, CMDn_BUSIF_DALIGN Register (CMDn_BUSIF_DALIGN)). Tables 30.4 and 30.5 show the data places when these registers are set to the initial values.

Table 30.4 Data Places in Each Data Format (1)

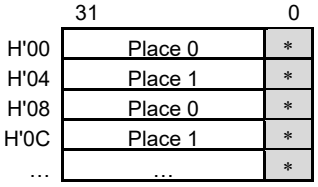
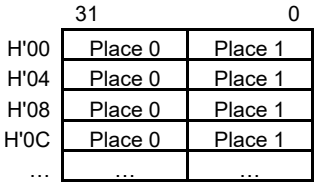
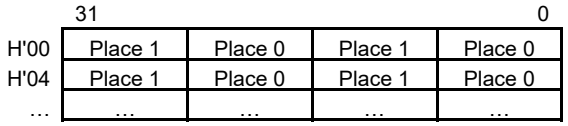
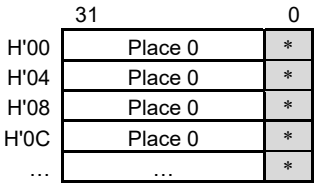
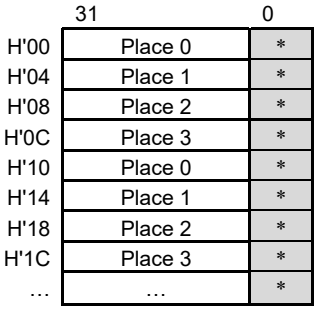
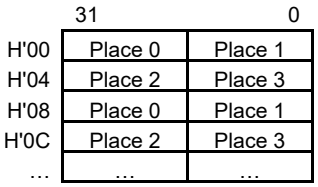
BUSIF · Stereo (2 channels) · 24 bits	External memory image 
BUSIF · Stereo (2 channels) · 16 bits	External memory image 
BUSIF · Stereo (2 channels) · 8 bits	External memory image 
BUSIF · Monaural (1 channel) · 8/16 bits	External memory image 
BUSIF · Multichannel (4 channels) · 24 bits	External memory image 
BUSIF · Multichannel (4 channels) · 16 bits	External memory image 

Table 30.5 Data Places in Each Data Format (2)

BUSIF · Multichannel (6 channels) · 24 bits	External memory image 31 0 H'00 Place 0 * H'04 Place 1 * H'08 Place 2 * H'0C Place 3 * H'10 Place 4 * H'14 Place 5 * H'18 Place 0 * H'1C Place 1 * … … …
BUSIF · Multichannel (6 channels) · 16 bits	External memory image 31 0 H'00 Place 0 Place 1 H'04 Place 2 Place 3 H'08 Place 4 Place 5 H'0C Place 0 Place 1 … … …
BUSIF · Multichannel (8 channels) · 24 bits	External memory image 31 0 H'00 Place 0 * H'04 Place 1 * H'08 Place 2 * H'0C Place 3 * H'10 Place 4 * H'14 Place 5 * H'18 Place 6 * H'1C Place 7 * H'20 Place 0 * … … *
BUSIF · Multichannel (8 channels) · 16 bits	External memory image 31 0 H'00 Place 0 Place 1 H'04 Place 2 Place 3 H'08 Place 4 Place 5 H'0C Place 6 Place 7 H'10 Place 0 Place 1 … … …

30.3.5 SRC Block

The SRC is a block for implementing the sampling rate conversion function, which can convert asynchronous sampling rates.

- Asynchronous sampling rate conversion is available
- Supports resolutions up to 24 bits
- High-sound-quality type (THD+N is -132 dB) and general-sound-quality type (THD+N is -96 dB)
- Automatically generates antialiasing filter coefficients
- Three modules support one, two, four, six, or eight channels, and six three modules support one or two channels.

Figure 30.5 shows the SRC block diagram.

The "Input audio data" in the figure indicates the data before SRC processing is applied. The "Output audio data" indicates the data after SRC processing is applied.

The "Input data timing" is a signal to show the sampling period for the input audio data. The "Output data timing" is a signal to show the sampling period for the output audio data. When CMD is used in the route, the output data timing signal is the same signal as the output data timing signal used in the CMD.

In synchronous mode specified by setting the SRCMD bit in the SRCm_SRCCR register, when the sync_in bit in the SRCm_MODE register is set to 1, the SRCm doesn't need the input data timing signal, and when the sync_out bit in the SRCm_MODE register is set to 1, the SRCm doesn't need the output data timing signal.

Before using the SRC function, be sure to specify the sampling rate through the SRCm IFS value setting register (see section 30.2.22, SRCm IFS Value Setting Register (SRCm_IFSVR).

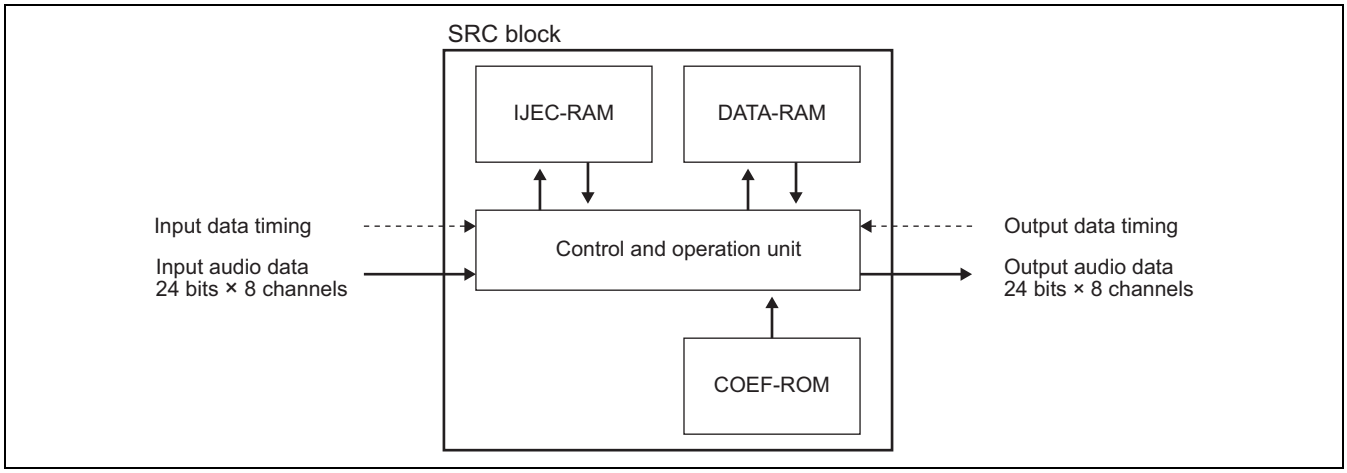


Figure 30.5 SRC Block Diagram

Table 30.6 shows the SRC functions.

Table 30.6 SRC Functions

Item		Performance			
Type of SRC		Asynchronous/ Synchronous SRC			
Channel number		1 or 2	4	6	8
Sampling rate of input source	SRC1, SRC3, SRC4	8k to 192k [Hz]	8k to 192k [Hz]	8k to 128k [Hz]	8k to 96k [Hz]
	SRC2	8k to 192k [Hz]	—	—	—
	SRC5, SRC6	8k to 192k [Hz]	—	—	—
Sampling rate of output source	SRC1, SRC3, SRC4	8k to 192k [Hz]	8k to 192k [Hz]	8k to 128k [Hz]	8k to 96k [Hz]
	SRC2	8k to 192k [Hz]	—	—	—
	SRC5, SRC6	8k to 192k [Hz]	—	—	—
Ratio of input and output sampling rates (FSO/FSI ratio)	SRC1, SRC3, SRC4	6 to 1/6 [times]	6 to 1/4 [times]	6 to 1/2 [times]	6 to 1/2 [times]
	SRC2	6 to 1/6 [times]	—	—	—
	SRC5, SRC6	6 to 1/6 [times]	—	—	—
Sound quality (THD+N)	SRC1 to SRC4	-132 dB (for high-quality type)			
	SRC5, SRC6	-96 dB (for general-quality type)			

Table 30.7 shows the IJEC RAM and DATA RAM buffer size settings and the latencies.

Latency is different by setting of channel number.

Select the combination of settings BUFDATA[10:0] bits in SRCm_BSDSR/ SRCn_BSDSR register and IJECSIZE[8:0] bits in SRCm_BSISR register from Table 30.7. Operation cannot be guaranteed if the register is not set as specified combination.

Output delay depends on FSO/FSI ratio and it is calculated from following formula.

Output delay [sample] = (Processing delay) × (FSO/FSI ratio) + (Logic delay)

Table 30.7 Combination of Register Setting Related to FSO/FSI Ratio and Channel, Latency

Item	Setting Range FSO/FSI Ratio	Channel Number	Register Setting IJEC SIZE [8:0]	Register Setting BUF DATA [10:0]	Processing Delay [sample]	Latency (Example case calculated by formula, Logic delay = 3) 6	4	3	2	1	2/3	1/2	1/3	1/4	1/6	Note
SRC1 SRC3 SRC4	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*
	6 to 1/4	1 to 4	H'40	H'100	161	969	647	486	325	164	110	84	57	43		
	6 to 1/3	1 to 4	H'30	H'0C0	121	729	487	366	245	124	84	64	43			
	6 to 1/2	1 to 8	H'20	H'080	81	489	327	246	165	84	57	44				
	6 to 2/3	1 to 8	H'20	H'060	65	393	263	198	133	68	46					
	6 to 1	1 to 8	H'20	H'040	49	297	199	150	101	52						
SRC2	6 to 1/6	1 to 2	H'60	H'180	241	1449	967	726	485	244	164	124	83	63	43	*
	6 to 1/4	1 to 2	H'40	H'100	161	969	647	486	325	164	110	84	57	43		
	6 to 1/3	1 to 2	H'30	H'0C0	121	729	487	366	245	124	84	64	43			
	6 to 1/2	1 to 2	H'20	H'080	81	489	327	246	165	84	57	44				
	6 to 2/3	1 to 2	H'20	H'060	65	393	263	198	133	68	46					
	6 to 1	1 to 2	H'20	H'040	49	297	199	150	101	52						
SRC5 to SRC6	6 to 1/6	1 to 2	H'60	H'240	337	2025	1351	1014	677	340	228	172	115	87	59	*
	6 to 1/4	1 to 2	H'40	H'180	225	1353	903	678	453	228	153	116	78	59		
	6 to 1/3	1 to 2	H'30	H'120	169	1017	679	510	341	172	116	88	59			
	6 to 1/2	1 to 2	H'20	H'0C0	113	681	455	342	229	116	78	60				
	6 to 2/3	1 to 2	H'20	H'090	89	537	359	270	181	92	62					
	6 to 1	1 to 2	H'20	H'060	65	393	263	198	133	68						

Note: Set up “*” case by common setting, if there are no problem for the latency.

Table 30.8 shows the INTIFS setting examples in the SRC block.

Table 30.8 INTIFS Values in SRCm_IFSVR Register for Some Specific Cases

INTIFS[27:0]

Input sampling rate [kHz]	Output sampling rate [kHz]						
	8	16	32	44.1	48	96	192
8	H'040 0000	H'020 0000	H'010 0000	H'00B 9C27	H'00A AAAA	—	—
11.025	H'058 3333	H'02C 1999	H'016 0CCC	H'010 0000	H'00E B333	—	—
12	H'060 0000	H'030 0000	H'018 0000	H'011 6A3B	H'010 0000	—	—
16	H'080 0000	H'040 0000	H'020 0000	H'017 384E	H'015 5555	H'00A AAAA	—
22.05	H'0B0 6666	H'058 3333	H'02C 1999	H'020 0000	H'01D 6666	H'00E B333	—
24	H'0C0 0000	H'060 0000	H'030 0000	H'022 D476	H'020 0000	H'010 0000	—
32	H'100 0000	H'080 0000	H'040 0000	H'02E 709D	H'02A AAAA	H'015 5555	H'00A AAAA
44.1	H'160 CCCC	H'0B0 6666	H'058 3333	H'040 0000	H'03A CCCC	H'01D 6666	H'00E B333
48	H'180 0000	H'0C0 0000	H'060 0000	H'045 A8EC	H'040 0000	H'020 0000	H'010 0000
64	—	H'100 0000	H'080 0000	H'05C E13B	H'055 5555	H'02A AAAA	H'015 5555
88.2	—	H'160 CCCC	H'0B0 6666	H'080 0000	H'075 9999	H'03A CCCC	H'01D 6666
96	—	H'180 0000	H'0C0 0000	H'08B 51D9	H'080 0000	H'040 0000	H'020 0000
176.4	—	H'2C1 9999	H'160 CCCC	H'100 0000	H'0EB 3333	H'075 9999	H'03A CCCC
192	—	—	H'180 0000	H'116 A3B3	H'100 0000	H'080 0000	H'040 0000

(1) Register Setting Procedure

The following describes the SRC register setting procedures. The register should be used according to the following procedures.

(a) SRC Processing Procedure

Figure 30.6 shows the processing procedure of SRC.

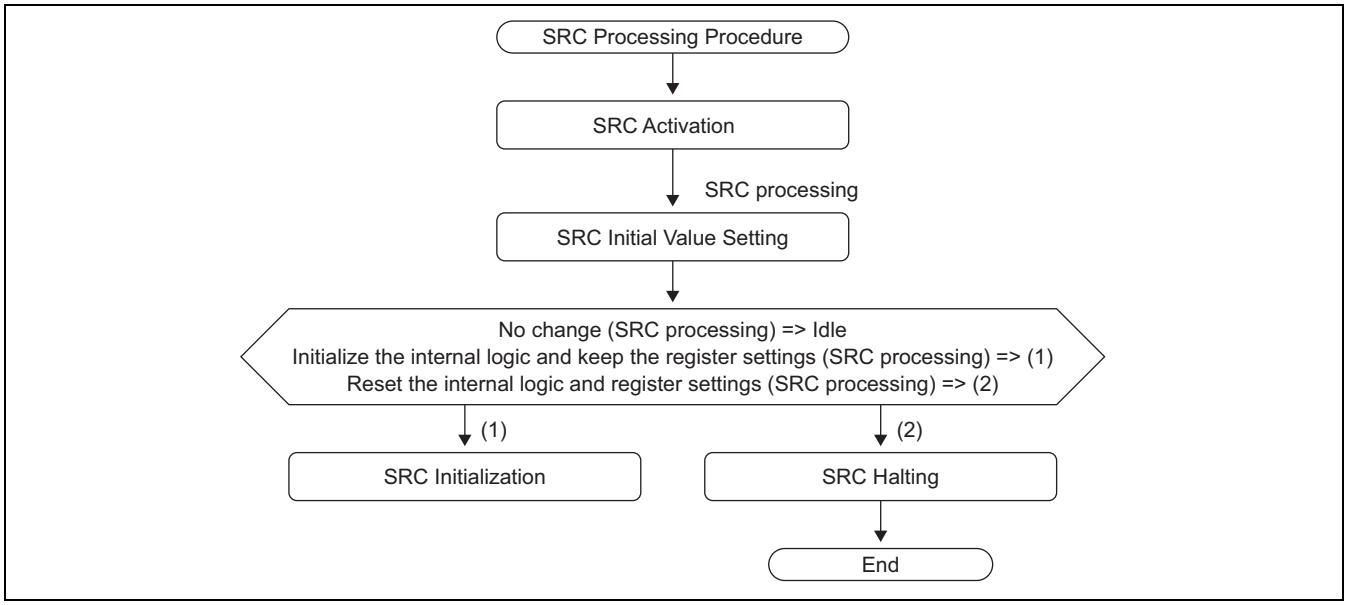


Figure 30.6 SRC Processing Procedure

(b) SRC Activation

Figure 30.7 shows the SRC activation flowchart. When the SRC is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate SRC. When reset the SRC function, all registers are initialized. If the SRC function was initialized by a hardware reset, it doesn't need to initialize the SRC function by software reset.

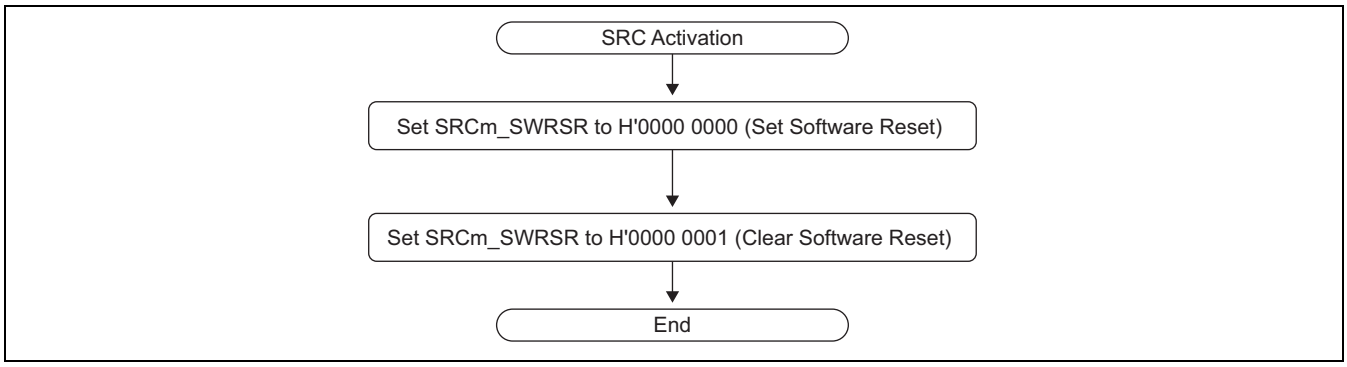


Figure 30.7 SRC Activation Flowchart

(c) SRC Initial Value Setting

Figure 30.8 shows the flowchart of the SRC initial value setting. Before operating SRC function, the initial values should be set.

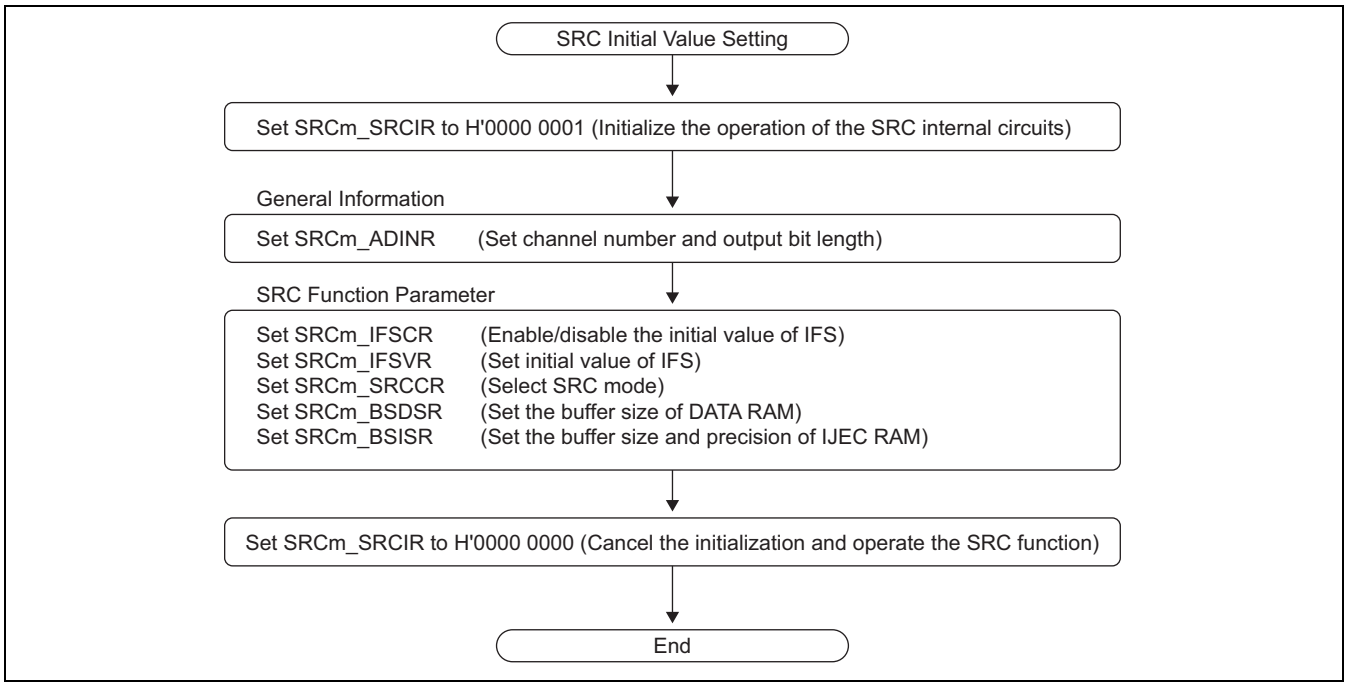


Figure 30.8 SRC Initial Value Setting Flowchart

(d) SRC Initialization

Figure 30.9 shows the SRC initialization flowchart. SRCm_SRCIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP. And also it is necessary to provide the input and output timing signal.

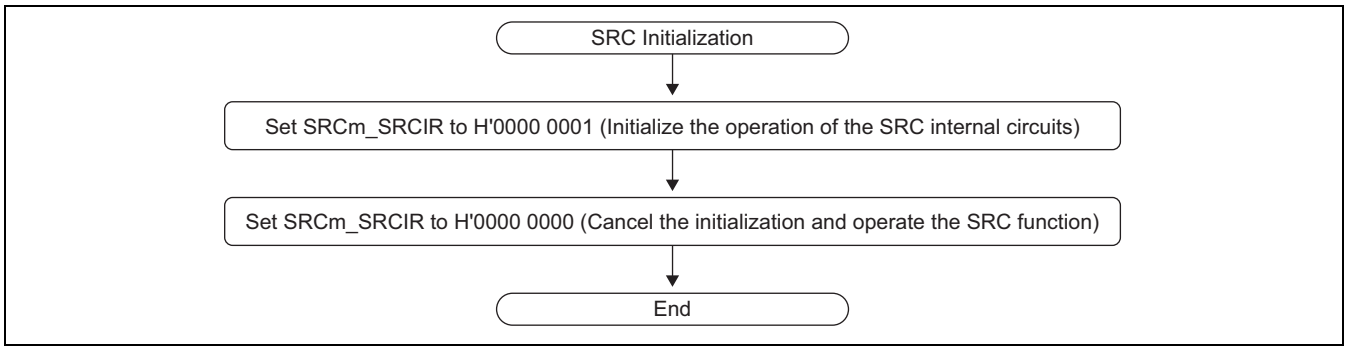


Figure 30.9 SRC Initialization Flowchart

(e) SRC Halting

Figure 30.10 shows the flowchart of SRC halting. When SRC is halting, it should be initialized or reset by software reset or hardware reset. Before initializing or reset the SRC function, it is necessary to confirm the register settings and operation of peripheral IP.

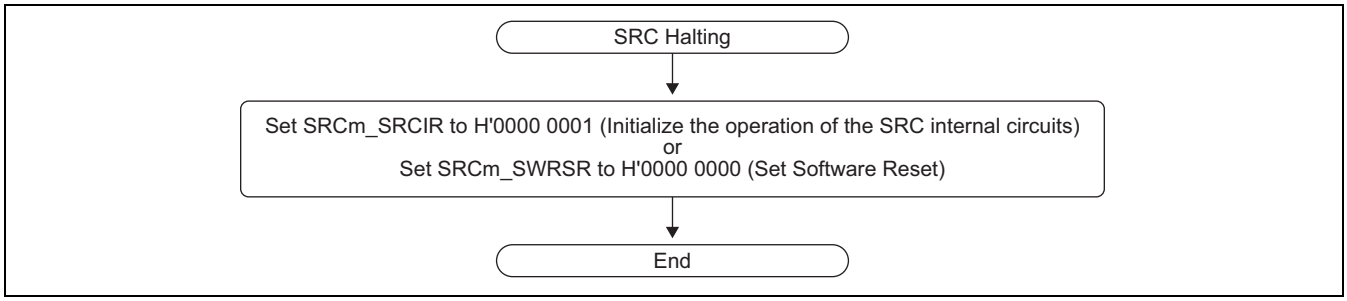


Figure 30.10 SRC Halting Flowchart

30.3.6 CMD Block

The CMD is a block for implementing the channel transfer unit (CTU block), mixing (MIX block), and digital volume and mute (DVC block) functions. Figure 30.11 shows the CMD block diagram.

The "Input audio data 0" to "Input audio data 3" in the figure indicate the data before the CMD function is applied. The "Output audio data" indicates the data after the CMD function is applied.

The "Output data timing" is a signal to show the sampling period for the output audio data. In addition, give the same signals to CMD output timing signal and output data timing signal used in the SRC.

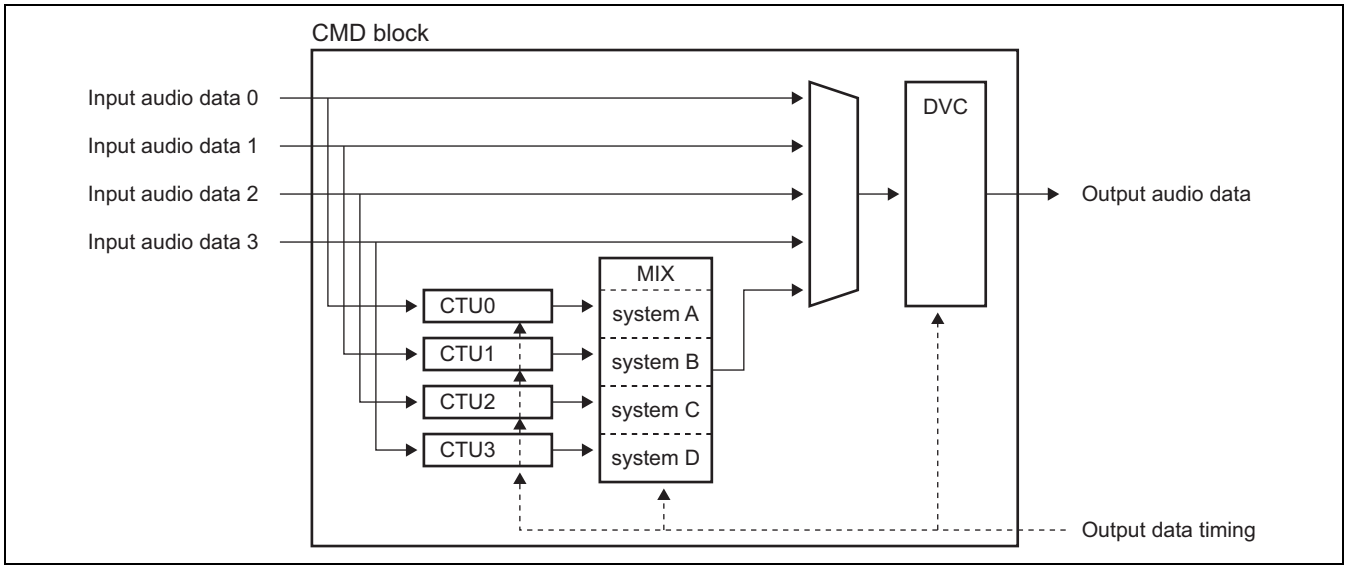


Figure 30.11 CMD Block Diagram

30.3.7 Functional Blocks in CMD

(1) CTU Block

The CTU is a block for implementing channel transfer unit functions such as downmixing and splitter functions.

- Conversion of eight input channels into two output channels
- Conversion of six input channels into two output channels
- Conversion of two input channels into four sets of two output channels
- Conversion of one input channel into eight sets of one output channel
- No conversion

The settings of the Scale Value e00 to Scale Value e37 registers are calculated by using the following formula (signed bits are excluded):

Setting (decimal) = $10^{X} \times 4194304$
X = (value in dB) / 20

(a) Register Setting Procedure

The following describes the CTU register setting procedures. The register should be used according to the following procedures.

- CTU Processing Procedure
  Figure 30.12 shows the processing procedure of CTU.

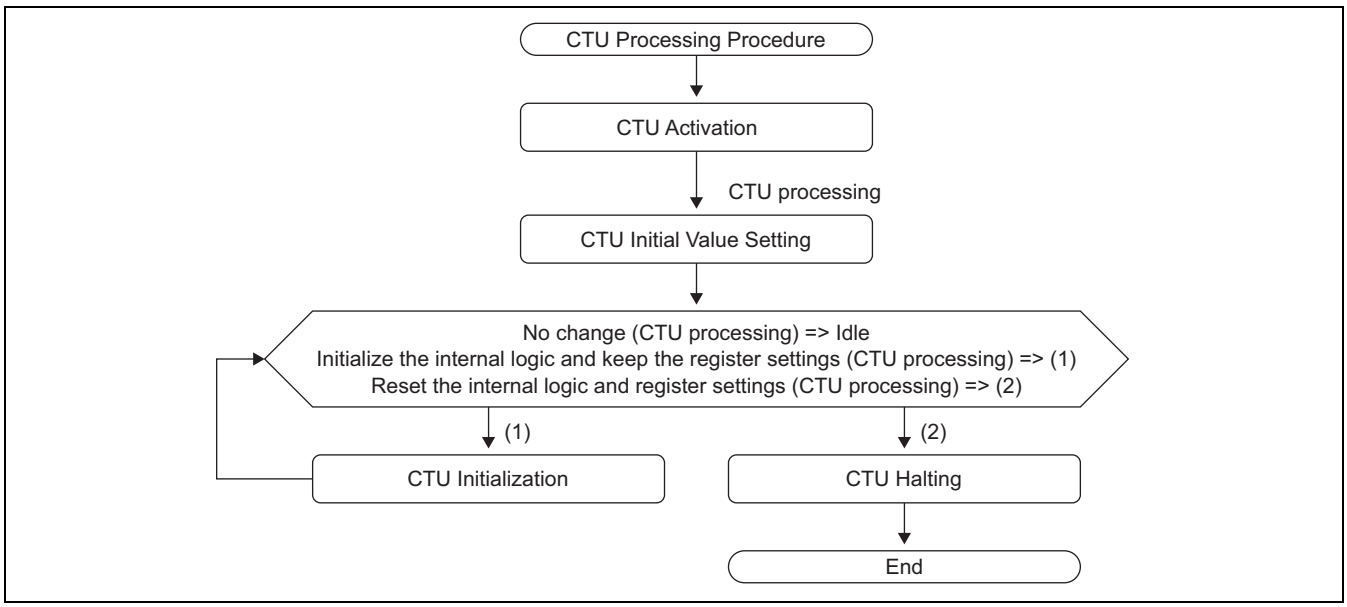


Figure 30.12 CTU Processing Procedure

- CTU Activation
  Figure 30.13 shows the CTU activation flowchart. When the CTU is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate CTU. When reset the CTU function, all registers are initialized. If the CTU function was initialized by a hardware reset, it doesn't need to initialize the CTU function by software reset.

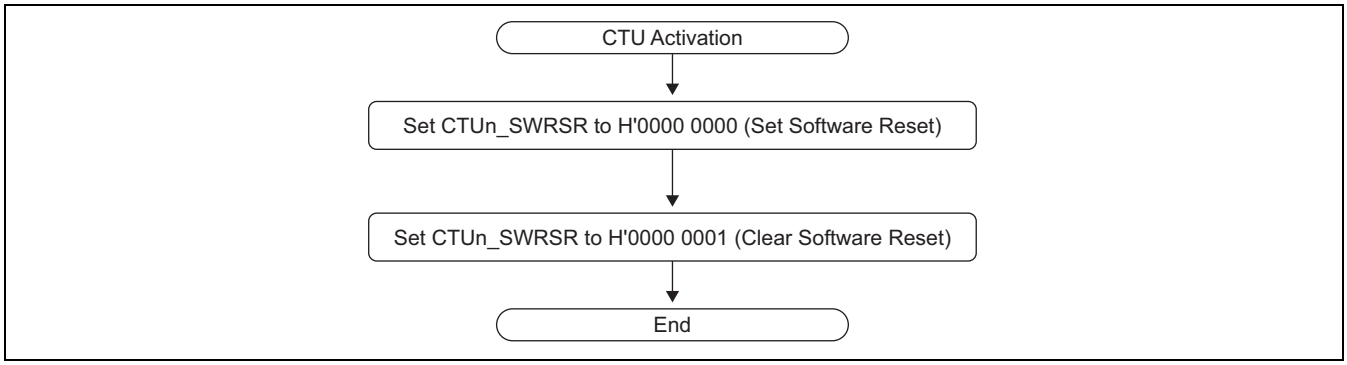


Figure 30.13 CTU Activation Flowchart

- CTU Initial Value Setting

  Figure 30.14 shows the flowchart of the CTU initial value setting. Before operating CTU function, the initial values should be set. After set the register setting and cancel the initialization, CTU module starts the operation.

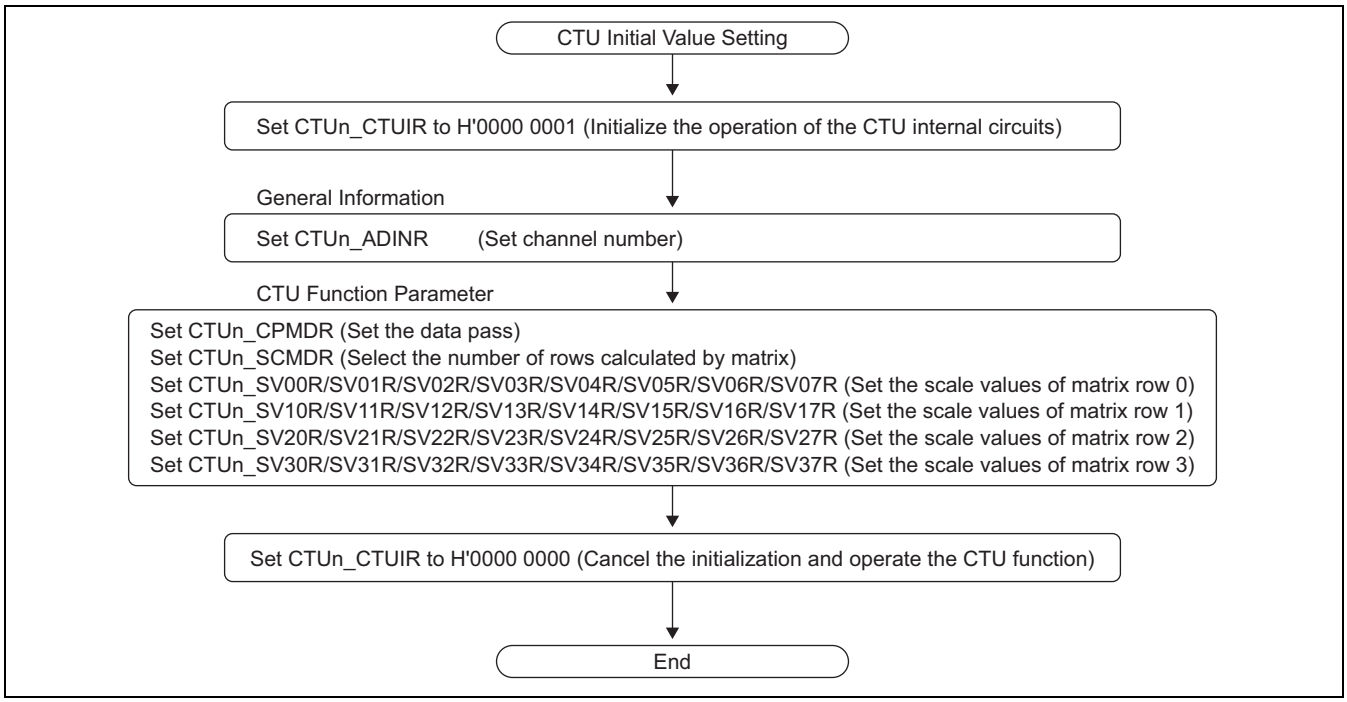


Figure 30.14 CTU Initial Value Setting Flowchart

- CTU Initialization

  Figure 30.15 shows the CTU initialization flowchart. CTUn_CTUIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP.

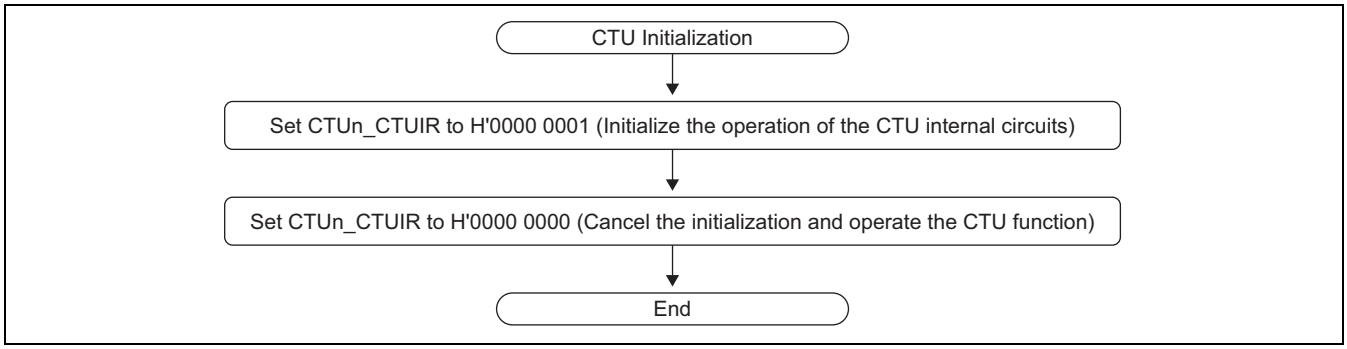


Figure 30.15 CTU Initialization Flowchart

- CTU Halting

  Figure 30.16 shows the flowchart of CTU halting. When CTU is halting, it should be initialized or reset by software reset or hardware reset. Before initializing or reset the CTU function, it is necessary to confirm the register settings and operation of peripheral IP.

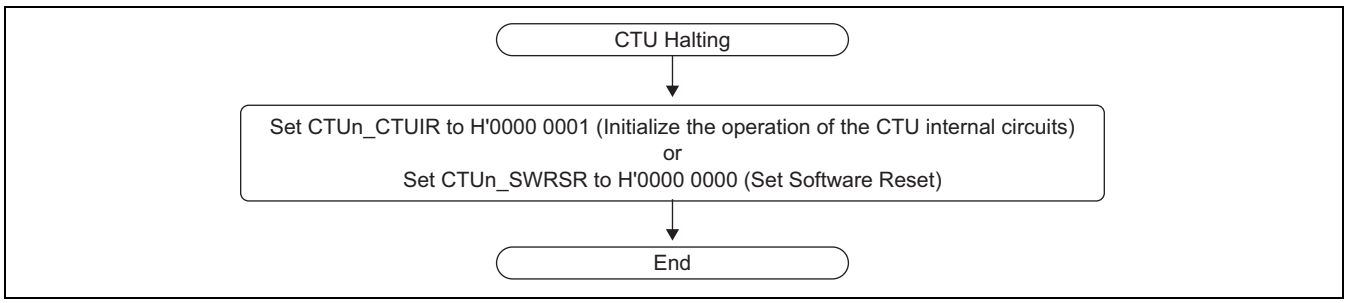


Figure 30.16 CTU Halting Flowchart

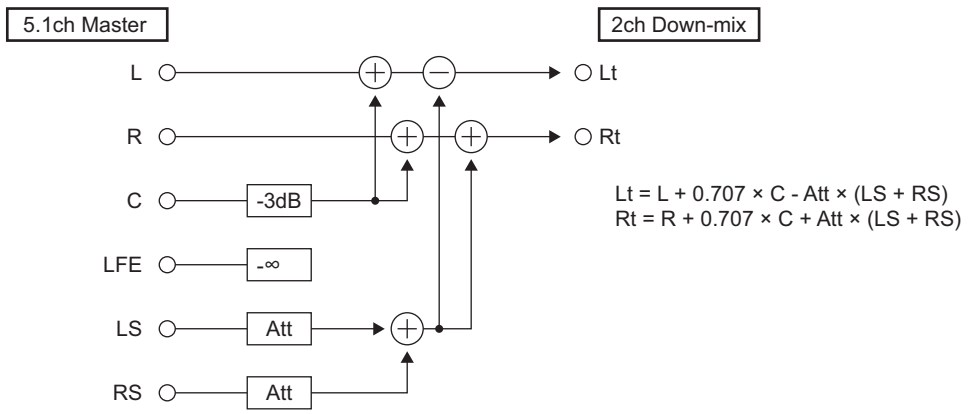
- CTU – Example

  The channel conversion executes the linear transformation (matrix operation) as follows.

$$\begin{pmatrix} y_0 \\ y_1 \\ y_2 \\ y_3 \\ y_4 \\ y_5 \\ y_6 \\ y_7 \end{pmatrix} = \begin{pmatrix} e_{00} & e_{01} & e_{02} & e_{03} & e_{04} & e_{05} & e_{06} & e_{07} \\ e_{10} & e_{11} & e_{12} & e_{13} & e_{14} & e_{15} & e_{16} & e_{17} \\ e_{20} & e_{21} & e_{22} & e_{23} & e_{24} & e_{25} & e_{26} & e_{27} \\ e_{30} & e_{31} & e_{32} & e_{33} & e_{34} & e_{35} & e_{36} & e_{37} \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \\ 0 & 0 & 0 & 0 & 0 & 0 & 0 & 0 \end{pmatrix} \times \begin{pmatrix} x_0 \\ x_1 \\ x_2 \\ x_3 \\ x_4 \\ x_5 \\ x_6 \\ x_7 \end{pmatrix}$$

x_i : Input data of channel i (i = 0 to 7)
y_i: Output data of channel i (i = 0 to 7)
e_j: CTUn_SVjR.SVEj (j = 00, 01, 02, 03, 04, 05, 06, 07,
10, 11, 12, 13, 14, 15, 16, 17,
20, 21, 22, 23, 24, 25, 26, 27,
30, 31, 32, 33, 34, 35, 36, 37)

Figure 30.17 shows 2 channels fold-down.



L(Left) : x0 (Input data of channel 0)
R(Right) : x1 (Input data of channel 1)
C(Center) : x2 (Input data of channel 2)
LFE(Low Frequency Effect) : x3 (Input data of channel 3)
LS(Left Surround) : x4 (Input data of channel 4)
RS(Right Surround) : x5 (Input data of channel 5)

Lt(L total) : y0 (Output data of channel 0)
Rt(R total) : y1 (Output data of channel 1)

CTUn_ADINR.CHNUM[3:0] = B'0110 (6 channel)
(MIXp_ADINR.CHNUM[3:0] = B'0010 (2 channel))
CTUn_CPMDR.SELOT0[3:0] = B'1001 (Connect calculated data by scale values of matrix row 0)
CTUn_CPMDR.SELOT1[3:0] = B'1010 (Connect calculated data by scale values of matrix row 1)
CTUn_CPMDR.SELOT2[3:0] = B'0000 (Connect input data of channel 2)
CTUn_CPMDR.SELOT3[3:0] = B'0000 (Connect input data of channel 3)
CTUn_CPMDR.SELOT4[3:0] = B'0000 (Connect input data of channel 4)
CTUn_CPMDR.SELOT5[3:0] = B'0000 (Connect input data of channel 5)
CTUn_CPMDR.SELOT6[3:0] = B'0000 (Connect input data of channel 6)
CTUn_CPMDR.SELOT7[3:0] = B'0000 (Connect input data of channel 7)
CTUn_SCMDR.SCMD[2:0] = B'010 (Calculate matrix row 0 and 1 by scale values.)

e00 : CTUn_SV00R.SVE00[23:0] = 1 × 2^22 = H'400000
e01 : CTUn_SV01R.SVE01[23:0] = 0 × 2^22 = H'000000
e02 : CTUn_SV02R.SVE02[23:0] = 0.707 × 2^22 = H'2D3F7C
e03 : CTUn_SV03R.SVE03[23:0] = 0 × 2^22 = H'000000
e04 : CTUn_SV04R.SVE04[23:0] = -Att × 2^22 = (bit23(Sign bit) = 1),(bit[22:0] = Att × 2^22)
e05 : CTUn_SV05R.SVE05[23:0] = -Att × 2^22 = (bit23(Sign bit) = 1),(bit[22:0] = Att × 2^22)
e06 : CTUn_SV06R.SVE06[23:0] = 0 × 2^22 = H'000000
e07 : CTUn_SV07R.SVE07[23:0] = 0 × 2^22 = H'000000

e10 : CTUn_SV10R.SVE10[23:0] = 0 × 2^22 = H'000000
e11 : CTUn_SV11R.SVE11[23:0] = 1 × 2^22 = H'400000
e12 : CTUn_SV12R.SVE12[23:0] = 0.707 × 2^22 = H'2D3F7C
e13 : CTUn_SV13R.SVE13[23:0] = 0 × 2^22 = H'000000
e14 : CTUn_SV14R.SVE14[23:0] = Att × 2^22 = (bit23(Sign bit) = 0),(bit[22:0] = Att × 2^22)
e15 : CTUn_SV15R.SVE15[23:0] = Att × 2^22 = (bit23(Sign bit) = 0),(bit[22:0] = Att × 2^22)
e16 : CTUn_SV16R.SVE16[23:0] = 0 × 2^22 = H'000000
e17 : CTUn_SV17R.SVE17[23:0] = 0 × 2^22 = H'000000

Figure 30.17 2 channels fold-down (Lt/Rt Downmix)

(2) MIX Block

The MIX block is for mixing (adding) streams from two to four audio data sources into a single stream.

- Ratio for adding sources is selectable
- Ratio is dynamically changeable
- Mixing with volume ramp is available (ramp period is selectable)

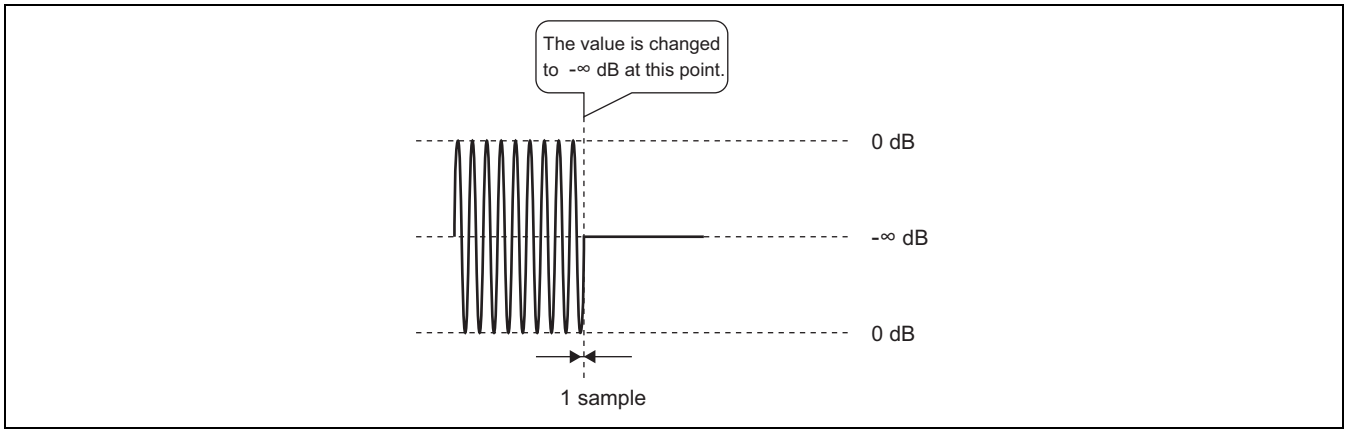


Figure 30.18 Step Processing

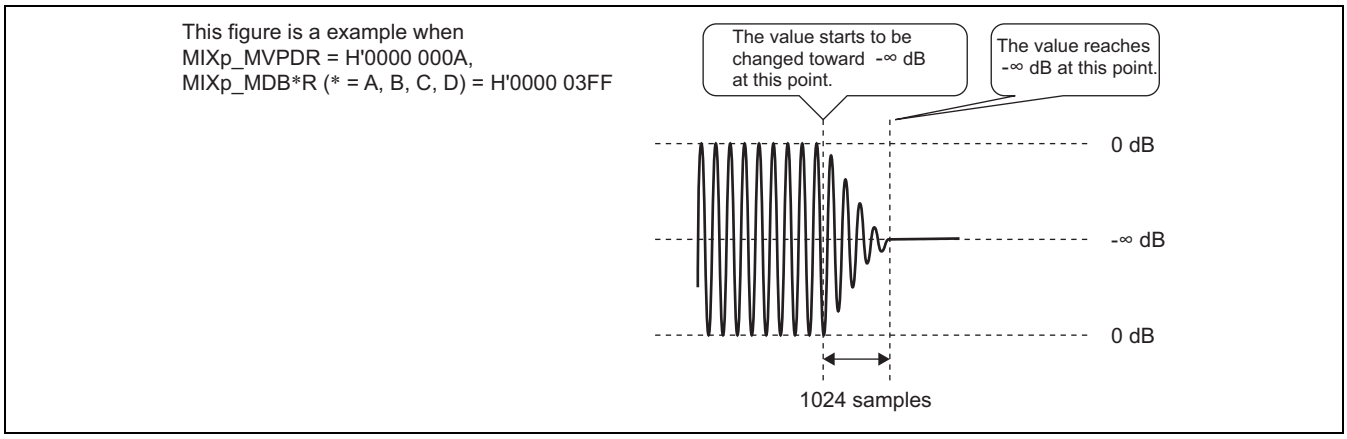


Figure 30.19 Ramp Processing

Tables 30.9 to 30.12 show the settings of the MIX decibel register and the corresponding levels in decibels.

Table 30.9 Settings of MIXp_MDBAR, MIXp_MDBBR, MIXp_MDBCR, and MIXp_MDBDR and Corresponding Values in Decibels (No. 0 to 255)

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
0	000	0	39	027	-4.875	78	04E	-9.75	117	075	-14.625
1	001	-0.125	40	028	-5	79	04F	-9.875	118	076	-14.75
2	002	-0.25	41	029	-5.125	80	050	-10	119	077	-14.875
3	003	-0.375	42	02A	-5.25	81	051	-10.125	120	078	-15
4	004	-0.5	43	02B	-5.375	82	052	-10.25	121	079	-15.125
5	005	-0.625	44	02C	-5.5	83	053	-10.375	122	07A	-15.25
6	006	-0.75	45	02D	-5.625	84	054	-10.5	123	07B	-15.375
7	007	-0.875	46	02E	-5.75	85	055	-10.625	124	07C	-15.5
8	008	-1	47	02F	-5.875	86	056	-10.75	125	07D	-15.625
9	009	-1.125	48	030	-6	87	057	-10.875	126	07E	-15.75
10	00A	-1.25	49	031	-6.125	88	058	-11	127	07F	-15.875
11	00B	-1.375	50	032	-6.25	89	059	-11.125	128	080	-16
12	00C	-1.5	51	033	-6.375	90	05A	-11.25	129	081	-16.125
13	00D	-1.625	52	034	-6.5	91	05B	-11.375	130	082	-16.25
14	00E	-1.75	53	035	-6.625	92	05C	-11.5	131	083	-16.375
15	00F	-1.875	54	036	-6.75	93	05D	-11.625	132	084	-16.5
16	010	-2	55	037	-6.875	94	05E	-11.75	133	085	-16.625
17	011	-2.125	56	038	-7	95	05F	-11.875	134	086	-16.75
18	012	-2.25	57	039	-7.125	96	060	-12	135	087	-16.875
19	013	-2.375	58	03A	-7.25	97	061	-12.125	136	088	-17
20	014	-2.5	59	03B	-7.375	98	062	-12.25	137	089	-17.125
21	015	-2.625	60	03C	-7.5	99	063	-12.375	138	08A	-17.25
22	016	-2.75	61	03D	-7.625	100	064	-12.5	139	08B	-17.375
23	017	-2.875	62	03E	-7.75	101	065	-12.625	140	08C	-17.5
24	018	-3	63	03F	-7.875	102	066	-12.75	141	08D	-17.625
25	019	-3.125	64	040	-8	103	067	-12.875	142	08E	-17.75
26	01A	-3.25	65	041	-8.125	104	068	-13	143	08F	-17.875
27	01B	-3.375	66	042	-8.25	105	069	-13.125	144	090	-18
28	01C	-3.5	67	043	-8.375	106	06A	-13.25	145	091	-18.125
29	01D	-3.625	68	044	-8.5	107	06B	-13.375	146	092	-18.25
30	01E	-3.75	69	045	-8.625	108	06C	-13.5	147	093	-18.375
31	01F	-3.875	70	046	-8.75	109	06D	-13.625	148	094	-18.5
32	020	-4	71	047	-8.875	110	06E	-13.75	149	095	-18.625
33	021	-4.125	72	048	-9	111	06F	-13.875	150	096	-18.75
34	022	-4.25	73	049	-9.125	112	070	-14	151	097	-18.875
35	023	-4.375	74	04A	-9.25	113	071	-14.125	152	098	-19
36	024	-4.5	75	04B	-9.375	114	072	-14.25	153	099	-19.125
37	025	-4.625	76	04C	-9.5	115	073	-14.375	154	09A	-19.25
38	026	-4.75	77	04D	-9.625	116	074	-14.5	155	09B	-19.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
156	09C	-19.5	181	0B5	-22.625	206	0CE	-25.75	231	0E7	-28.875
157	09D	-19.625	182	0B6	-22.75	207	0CF	-25.875	232	0E8	-29
158	09E	-19.75	183	0B7	-22.875	208	0D0	-26	233	0E9	-29.125
159	09F	-19.875	184	0B8	-23	209	0D1	-26.125	234	0EA	-29.25
160	0A0	-20	185	0B9	-23.125	210	0D2	-26.25	235	0EB	-29.375
161	0A1	-20.125	186	0BA	-23.25	211	0D3	-26.375	236	0EC	-29.5
162	0A2	-20.25	187	0BB	-23.375	212	0D4	-26.5	237	0ED	-29.625
163	0A3	-20.375	188	0BC	-23.5	213	0D5	-26.625	238	0EE	-29.75
164	0A4	-20.5	189	0BD	-23.625	214	0D6	-26.75	239	0EF	-29.875
165	0A5	-20.625	190	0BE	-23.75	215	0D7	-26.875	240	0F0	-30
166	0A6	-20.75	191	0BF	-23.875	216	0D8	-27	241	0F1	-30.125
167	0A7	-20.875	192	0C0	-24	217	0D9	-27.125	242	0F2	-30.25
168	0A8	-21	193	0C1	-24.125	218	0DA	-27.25	243	0F3	-30.375
169	0A9	-21.125	194	0C2	-24.25	219	0DB	-27.375	244	0F4	-30.5
170	0AA	-21.25	195	0C3	-24.375	220	0DC	-27.5	245	0F5	-30.625
171	0AB	-21.375	196	0C4	-24.5	221	0DD	-27.625	246	0F6	-30.75
172	0AC	-21.5	197	0C5	-24.625	222	0DE	-27.75	247	0F7	-30.875
173	0AD	-21.625	198	0C6	-24.75	223	0DF	-27.875	248	0F8	-31
174	0AE	-21.75	199	0C7	-24.875	224	0E0	-28	249	0F9	-31.125
175	0AF	-21.875	200	0C8	-25	225	0E1	-28.125	250	0FA	-31.25
176	0B0	-22	201	0C9	-25.125	226	0E2	-28.25	251	0FB	-31.375
177	0B1	-22.125	202	0CA	-25.25	227	0E3	-28.375	252	0FC	-31.5
178	0B2	-22.25	203	0CB	-25.375	228	0E4	-28.5	253	0FD	-31.625
179	0B3	-22.375	204	0CC	-25.5	229	0E5	-28.625	254	0FE	-31.75
180	0B4	-22.5	205	0CD	-25.625	230	0E6	-28.75	255	0FF	-31.875

Table 30.10 Settings of MIXp_MDBAR, MIXp_MDBBR, MIXp_MDBCR, and MIXp_MDBDR and Corresponding Values in Decibels (No. 256 to 511)

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
256	100	-32	297	129	-37.125	338	152	-42.25	379	17B	-47.375
257	101	-32.125	298	12A	-37.25	339	153	-42.375	380	17C	-47.5
258	102	-32.25	299	12B	-37.375	340	154	-42.5	381	17D	-47.625
259	103	-32.375	300	12C	-37.5	341	155	-42.625	382	17E	-47.75
260	104	-32.5	301	12D	-37.625	342	156	-42.75	383	17F	-47.875
261	105	-32.625	302	12E	-37.75	343	157	-42.875	384	180	-48
262	106	-32.75	303	12F	-37.875	344	158	-43	385	181	-48.125
263	107	-32.875	304	130	-38	345	159	-43.125	386	182	-48.25
264	108	-33	305	131	-38.125	346	15A	-43.25	387	183	-48.375
265	109	-33.125	306	132	-38.25	347	15B	-43.375	388	184	-48.5
266	10A	-33.25	307	133	-38.375	348	15C	-43.5	389	185	-48.625
267	10B	-33.375	308	134	-38.5	349	15D	-43.625	390	186	-48.75
268	10C	-33.5	309	135	-38.625	350	15E	-43.75	391	187	-48.875
269	10D	-33.625	310	136	-38.75	351	15F	-43.875	392	188	-49
270	10E	-33.75	311	137	-38.875	352	160	-44	393	189	-49.125
271	10F	-33.875	312	138	-39	353	161	-44.125	394	18A	-49.25
272	110	-34	313	139	-39.125	354	162	-44.25	395	18B	-49.375
273	111	-34.125	314	13A	-39.25	355	163	-44.375	396	18C	-49.5
274	112	-34.25	315	13B	-39.375	356	164	-44.5	397	18D	-49.625
275	113	-34.375	316	13C	-39.5	357	165	-44.625	398	18E	-49.75
276	114	-34.5	317	13D	-39.625	358	166	-44.75	399	18F	-49.875
277	115	-34.625	318	13E	-39.75	359	167	-44.875	400	190	-50
278	116	-34.75	319	13F	-39.875	360	168	-45	401	191	-50.125
279	117	-34.875	320	140	-40	361	169	-45.125	402	192	-50.25
280	118	-35	321	141	-40.125	362	16A	-45.25	403	193	-50.375
281	119	-35.125	322	142	-40.25	363	16B	-45.375	404	194	-50.5
282	11A	-35.25	323	143	-40.375	364	16C	-45.5	405	195	-50.625
283	11B	-35.375	324	144	-40.5	365	16D	-45.625	406	196	-50.75
284	11C	-35.5	325	145	-40.625	366	16E	-45.75	407	197	-50.875
285	11D	-35.625	326	146	-40.75	367	16F	-45.875	408	198	-51
286	11E	-35.75	327	147	-40.875	368	170	-46	409	199	-51.125
287	11F	-35.875	328	148	-41	369	171	-46.125	410	19A	-51.25
288	120	-36	329	149	-41.125	370	172	-46.25	411	19B	-51.375
289	121	-36.125	330	14A	-41.25	371	173	-46.375	412	19C	-51.5
290	122	-36.25	331	14B	-41.375	372	174	-46.5	413	19D	-51.625
291	123	-36.375	332	14C	-41.5	373	175	-46.625	414	19E	-51.75
292	124	-36.5	333	14D	-41.625	374	176	-46.75	415	19F	-51.875
293	125	-36.625	334	14E	-41.75	375	177	-46.875	416	1A0	-52
294	126	-36.75	335	14F	-41.875	376	178	-47	417	1A1	-52.125
295	127	-36.875	336	150	-42	377	179	-47.125	418	1A2	-52.25
296	128	-37	337	151	-42.125	378	17A	-47.25	419	1A3	-52.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
420	1A4	-52.5	443	1BB	-55.375	466	1D2	-58.25	489	1E9	-61.125
421	1A5	-52.625	444	1BC	-55.5	467	1D3	-58.375	490	1EA	-61.25
422	1A6	-52.75	445	1BD	-55.625	468	1D4	-58.5	491	1EB	-61.375
423	1A7	-52.875	446	1BE	-55.75	469	1D5	-58.625	492	1EC	-61.5
424	1A8	-53	447	1BF	-55.875	470	1D6	-58.75	493	1ED	-61.625
425	1A9	-53.125	448	1C0	-56	471	1D7	-58.875	494	1EE	-61.75
426	1AA	-53.25	449	1C1	-56.125	472	1D8	-59	495	1EF	-61.875
427	1AB	-53.375	450	1C2	-56.25	473	1D9	-59.125	496	1F0	-62
428	1AC	-53.5	451	1C3	-56.375	474	1DA	-59.25	497	1F1	-62.125
429	1AD	-53.625	452	1C4	-56.5	475	1DB	-59.375	498	1F2	-62.25
430	1AE	-53.75	453	1C5	-56.625	476	1DC	-59.5	499	1F3	-62.375
431	1AF	-53.875	454	1C6	-56.75	477	1DD	-59.625	500	1F4	-62.5
432	1B0	-54	455	1C7	-56.875	478	1DE	-59.75	501	1F5	-62.625
433	1B1	-54.125	456	1C8	-57	479	1DF	-59.875	502	1F6	-62.75
434	1B2	-54.25	457	1C9	-57.125	480	1E0	-60	503	1F7	-62.875
435	1B3	-54.375	458	1CA	-57.25	481	1E1	-60.125	504	1F8	-63
436	1B4	-54.5	459	1CB	-57.375	482	1E2	-60.25	505	1F9	-63.125
437	1B5	-54.625	460	1CC	-57.5	483	1E3	-60.375	506	1FA	-63.25
438	1B6	-54.75	461	1CD	-57.625	484	1E4	-60.5	507	1FB	-63.375
439	1B7	-54.875	462	1CE	-57.75	485	1E5	-60.625	508	1FC	-63.5
440	1B8	-55	463	1CF	-57.875	486	1E6	-60.75	509	1FD	-63.625
441	1B9	-55.125	464	1D0	-58	487	1E7	-60.875	510	1FE	-63.75
442	1BA	-55.25	465	1D1	-58.125	488	1E8	-61	511	1FF	-63.875

Table 30.11 Settings of MIXp_MDBAR, MIXp_MDBBR, MIXp_MDBCR, and MIXp_MDBDR and Corresponding Values in Decibels (No. 512 to 767)

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
512	200	-64	553	229	-69.125	594	252	-74.25	635	27B	-79.375
513	201	-64.125	554	22A	-69.25	595	253	-74.375	636	27C	-79.5
514	202	-64.25	555	22B	-69.375	596	254	-74.5	637	27D	-79.625
515	203	-64.375	556	22C	-69.5	597	255	-74.625	638	27E	-79.75
516	204	-64.5	557	22D	-69.625	598	256	-74.75	639	27F	-79.875
517	205	-64.625	558	22E	-69.75	599	257	-74.875	640	280	-80
518	206	-64.75	559	22F	-69.875	600	258	-75	641	281	-80.125
519	207	-64.875	560	230	-70	601	259	-75.125	642	282	-80.25
520	208	-65	561	231	-70.125	602	25A	-75.25	643	283	-80.375
521	209	-65.125	562	232	-70.25	603	25B	-75.375	644	284	-80.5
522	20A	-65.25	563	233	-70.375	604	25C	-75.5	645	285	-80.625
523	20B	-65.375	564	234	-70.5	605	25D	-75.625	646	286	-80.75
524	20C	-65.5	565	235	-70.625	606	25E	-75.75	647	287	-80.875
525	20D	-65.625	566	236	-70.75	607	25F	-75.875	648	288	-81
526	20E	-65.75	567	237	-70.875	608	260	-76	649	289	-81.125
527	20F	-65.875	568	238	-71	609	261	-76.125	650	28A	-81.25
528	210	-66	569	239	-71.125	610	262	-76.25	651	28B	-81.375
529	211	-66.125	570	23A	-71.25	611	263	-76.375	652	28C	-81.5
530	212	-66.25	571	23B	-71.375	612	264	-76.5	653	28D	-81.625
531	213	-66.375	572	23C	-71.5	613	265	-76.625	654	28E	-81.75
532	214	-66.5	573	23D	-71.625	614	266	-76.75	655	28F	-81.875
533	215	-66.625	574	23E	-71.75	615	267	-76.875	656	290	-82
534	216	-66.75	575	23F	-71.875	616	268	-77	657	291	-82.125
535	217	-66.875	576	240	-72	617	269	-77.125	658	292	-82.25
536	218	-67	577	241	-72.125	618	26A	-77.25	659	293	-82.375
537	219	-67.125	578	242	-72.25	619	26B	-77.375	660	294	-82.5
538	21A	-67.25	579	243	-72.375	620	26C	-77.5	661	295	-82.625
539	21B	-67.375	580	244	-72.5	621	26D	-77.625	662	296	-82.75
540	21C	-67.5	581	245	-72.625	622	26E	-77.75	663	297	-82.875
541	21D	-67.625	582	246	-72.75	623	26F	-77.875	664	298	-83
542	21E	-67.75	583	247	-72.875	624	270	-78	665	299	-83.125
543	21F	-67.875	584	248	-73	625	271	-78.125	666	29A	-83.25
544	220	-68	585	249	-73.125	626	272	-78.25	667	29B	-83.375
545	221	-68.125	586	24A	-73.25	627	273	-78.375	668	29C	-83.5
546	222	-68.25	587	24B	-73.375	628	274	-78.5	669	29D	-83.625
547	223	-68.375	588	24C	-73.5	629	275	-78.625	670	29E	-83.75
548	224	-68.5	589	24D	-73.625	630	276	-78.75	671	29F	-83.875
549	225	-68.625	590	24E	-73.75	631	277	-78.875	672	2A0	-84
550	226	-68.75	591	24F	-73.875	632	278	-79	673	2A1	-84.125
551	227	-68.875	592	250	-74	633	279	-79.125	674	2A2	-84.25
552	228	-69	593	251	-74.125	634	27A	-79.25	675	2A3	-84.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
676	2A4	-84.5	699	2BB	-87.375	722	2D2	-90.25	745	2E9	-93.125
677	2A5	-84.625	700	2BC	-87.5	723	2D3	-90.375	746	2EA	-93.25
678	2A6	-84.75	701	2BD	-87.625	724	2D4	-90.5	747	2EB	-93.375
679	2A7	-84.875	702	2BE	-87.75	725	2D5	-90.625	748	2EC	-93.5
680	2A8	-85	703	2BF	-87.875	726	2D6	-90.75	749	2ED	-93.625
681	2A9	-85.125	704	2C0	-88	727	2D7	-90.875	750	2EE	-93.75
682	2AA	-85.25	705	2C1	-88.125	728	2D8	-91	751	2EF	-93.875
683	2AB	-85.375	706	2C2	-88.25	729	2D9	-91.125	752	2F0	-94
684	2AC	-85.5	707	2C3	-88.375	730	2DA	-91.25	753	2F1	-94.125
685	2AD	-85.625	708	2C4	-88.5	731	2DB	-91.375	754	2F2	-94.25
686	2AE	-85.75	709	2C5	-88.625	732	2DC	-91.5	755	2F3	-94.375
687	2AF	-85.875	710	2C6	-88.75	733	2DD	-91.625	756	2F4	-94.5
688	2B0	-86	711	2C7	-88.875	734	2DE	-91.75	757	2F5	-94.625
689	2B1	-86.125	712	2C8	-89	735	2DF	-91.875	758	2F6	-94.75
690	2B2	-86.25	713	2C9	-89.125	736	2E0	-92	759	2F7	-94.875
691	2B3	-86.375	714	2CA	-89.25	737	2E1	-92.125	760	2F8	-95
692	2B4	-86.5	715	2CB	-89.375	738	2E2	-92.25	761	2F9	-95.125
693	2B5	-86.625	716	2CC	-89.5	739	2E3	-92.375	762	2FA	-95.25
694	2B6	-86.75	717	2CD	-89.625	740	2E4	-92.5	763	2FB	-95.375
695	2B7	-86.875	718	2CE	-89.75	741	2E5	-92.625	764	2FC	-95.5
696	2B8	-87	719	2CF	-89.875	742	2E6	-92.75	765	2FD	-95.625
697	2B9	-87.125	720	2D0	-90	743	2E7	-92.875	766	2FE	-95.75
698	2BA	-87.25	721	2D1	-90.125	744	2E8	-93	767	2FF	-95.875

Table 30.12 Settings of MIXp_MDBAR, MIXp_MDBBR, MIXp_MDBCR, and MIXp_MDBDR and Corresponding Values in Decibels (No. 768 to 1023)

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
768	300	-96	809	329	-101.125	850	352	-106.25	891	37B	-111.375
769	301	-96.125	810	32A	-101.25	851	353	-106.375	892	37C	-111.5
770	302	-96.25	811	32B	-101.375	852	354	-106.5	893	37D	-111.625
771	303	-96.375	812	32C	-101.5	853	355	-106.625	894	37E	-111.75
772	304	-96.5	813	32D	-101.625	854	356	-106.75	895	37F	-111.875
773	305	-96.625	814	32E	-101.75	855	357	-106.875	896	380	-112
774	306	-96.75	815	32F	-101.875	856	358	-107	897	381	-112.125
775	307	-96.875	816	330	-102	857	359	-107.125	898	382	-112.25
776	308	-97	817	331	-102.125	858	35A	-107.25	899	383	-112.375
777	309	-97.125	818	332	-102.25	859	35B	-107.375	900	384	-112.5
778	30A	-97.25	819	333	-102.375	860	35C	-107.5	901	385	-112.625
779	30B	-97.375	820	334	-102.5	861	35D	-107.625	902	386	-112.75
780	30C	-97.5	821	335	-102.625	862	35E	-107.75	903	387	-112.875
781	30D	-97.625	822	336	-102.75	863	35F	-107.875	904	388	-113
782	30E	-97.75	823	337	-102.875	864	360	-108	905	389	-113.125
783	30F	-97.875	824	338	-103	865	361	-108.125	906	38A	-113.25
784	310	-98	825	339	-103.125	866	362	-108.25	907	38B	-113.375
785	311	-98.125	826	33A	-103.25	867	363	-108.375	908	38C	-113.5
786	312	-98.25	827	33B	-103.375	868	364	-108.5	909	38D	-113.625
787	313	-98.375	828	33C	-103.5	869	365	-108.625	910	38E	-113.75
788	314	-98.5	829	33D	-103.625	870	366	-108.75	911	38F	-113.875
789	315	-98.625	830	33E	-103.75	871	367	-108.875	912	390	-114
790	316	-98.75	831	33F	-103.875	872	368	-109	913	391	-114.125
791	317	-98.875	832	340	-104	873	369	-109.125	914	392	-114.25
792	318	-99	833	341	-104.125	874	36A	-109.25	915	393	-114.375
793	319	-99.125	834	342	-104.25	875	36B	-109.375	916	394	-114.5
794	31A	-99.25	835	343	-104.375	876	36C	-109.5	917	395	-114.625
795	31B	-99.375	836	344	-104.5	877	36D	-109.625	918	396	-114.75
796	31C	-99.5	837	345	-104.625	878	36E	-109.75	919	397	-114.875
797	31D	-99.625	838	346	-104.75	879	36F	-109.875	920	398	-115
798	31E	-99.75	839	347	-104.875	880	370	-110	921	399	-115.125
799	31F	-99.875	840	348	-105	881	371	-110.125	922	39A	-115.25
800	320	-100	841	349	-105.125	882	372	-110.25	923	39B	-115.375
801	321	-100.125	842	34A	-105.25	883	373	-110.375	924	39C	-115.5
802	322	-100.25	843	34B	-105.375	884	374	-110.5	925	39D	-115.625
803	323	-100.375	844	34C	-105.5	885	375	-110.625	926	39E	-115.75
804	324	-100.5	845	34D	-105.625	886	376	-110.75	927	39F	-115.875
805	325	-100.625	846	34E	-105.75	887	377	-110.875	928	3A0	-116
806	326	-100.75	847	34F	-105.875	888	378	-111	929	3A1	-116.125
807	327	-100.875	848	350	-106	889	379	-111.125	930	3A2	-116.25
808	328	-101	849	351	-106.125	890	37A	-111.25	931	3A3	-116.375

No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB	No	Value (HEX)	dB
932	3A4	-116.5	955	3BB	-119.375	978	3D2	-122.25	1001	3E9	-125.125
933	3A5	-116.625	956	3BC	-119.5	979	3D3	-122.375	1002	3EA	-125.25
934	3A6	-116.75	957	3BD	-119.625	980	3D4	-122.5	1003	3EB	-125.375
935	3A7	-116.875	958	3BE	-119.75	981	3D5	-122.625	1004	3EC	-125.5
936	3A8	-117	959	3BF	-119.875	982	3D6	-122.75	1005	3ED	-125.625
937	3A9	-117.125	960	3C0	-120	983	3D7	-122.875	1006	3EE	-125.75
938	3AA	-117.25	961	3C1	-120.125	984	3D8	-123	1007	3EF	-125.875
939	3AB	-117.375	962	3C2	-120.25	985	3D9	-123.125	1008	3F0	-126
940	3AC	-117.5	963	3C3	-120.375	986	3DA	-123.25	1009	3F1	-126.125
941	3AD	-117.625	964	3C4	-120.5	987	3DB	-123.375	1010	3F2	-126.25
942	3AE	-117.75	965	3C5	-120.625	988	3DC	-123.5	1011	3F3	-126.375
943	3AF	-117.875	966	3C6	-120.75	989	3DD	-123.625	1012	3F4	-126.5
944	3B0	-118	967	3C7	-120.875	990	3DE	-123.75	1013	3F5	-126.625
945	3B1	-118.125	968	3C8	-121	991	3DF	-123.875	1014	3F6	-126.75
946	3B2	-118.25	969	3C9	-121.125	992	3E0	-124	1015	3F7	-126.875
947	3B3	-118.375	970	3CA	-121.25	993	3E1	-124.125	1016	3F8	-127
948	3B4	-118.5	971	3CB	-121.375	994	3E2	-124.25	1017	3F9	-127.125
949	3B5	-118.625	972	3CC	-121.5	995	3E3	-124.375	1018	3FA	-127.25
950	3B6	-118.75	973	3CD	-121.625	996	3E4	-124.5	1019	3FB	-127.375
951	3B7	-118.875	974	3CE	-121.75	997	3E5	-124.625	1020	3FC	-127.5
952	3B8	-119	975	3CF	-121.875	998	3E6	-124.75	1021	3FD	-127.625
953	3B9	-119.125	976	3D0	-122	999	3E7	-124.875	1022	3FE	-127.75
954	3BA	-119.25	977	3D1	-122.125	1000	3E8	-125	1023	3FF	-∞

(a) Register Setting Procedure

The following describes the MIX register setting procedures. The register should be used according to the following procedures.

- MIX Processing Procedure
  Figure 30.20 shows the processing procedure of MIX.

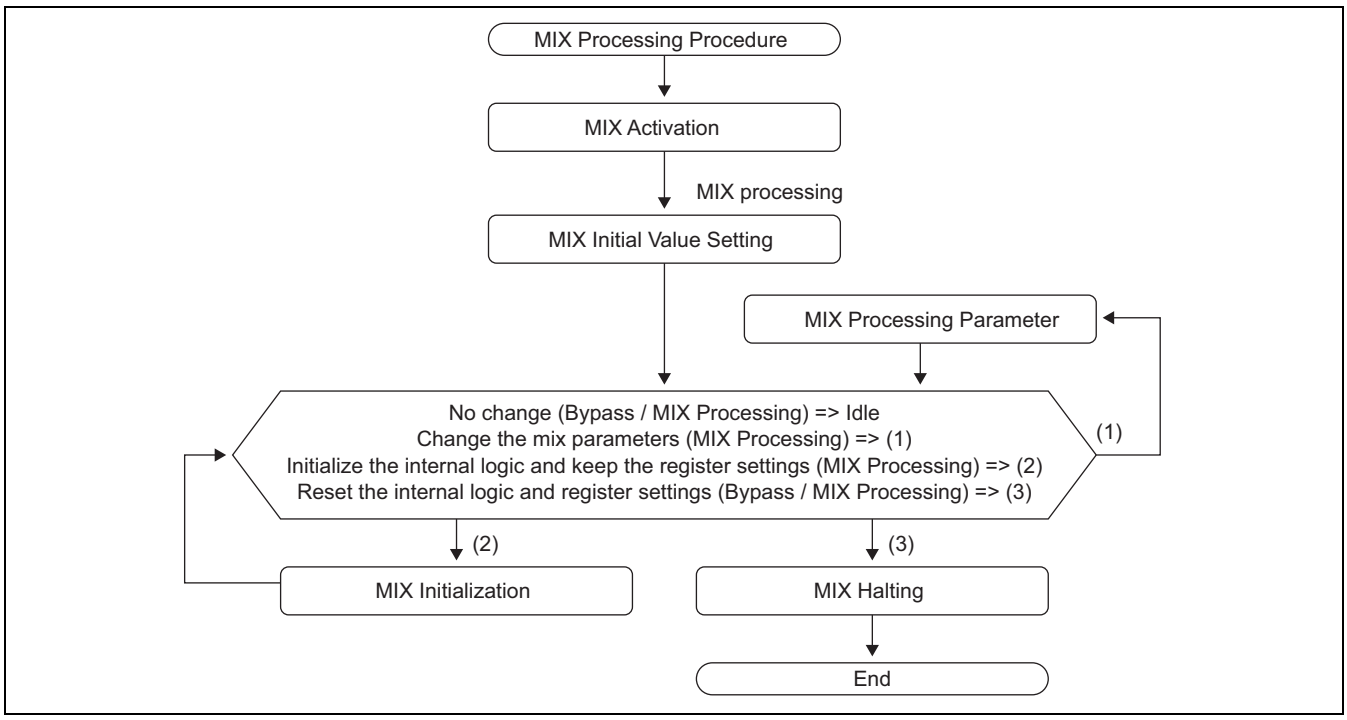


Figure 30.20 MIX Processing Procedure

- MIX Activation
  Figure 30.21 shows the MIX activation flowchart. When the MIX is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate MIX. When reset the MIX function, all registers are initialized. If the MIX function was initialized by a hardware reset, it doesn't need to initialize the MIX function by software reset.

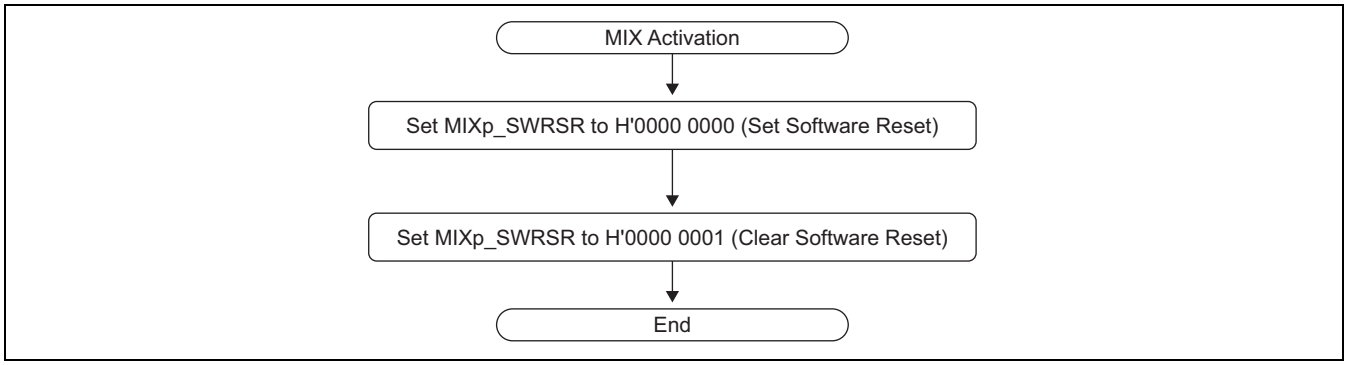


Figure 30.21 MIX Activation Flowchart

- MIX Initial Value Setting

  Figure 30.22 shows the flowchart of the MIX initial value setting. Before operating MIX function, the initial values should be set. After set the register setting and cancel the initialization, MIX module changes the volume of each system by volume step to the dB value of MIXp_MDBAR and MIXp_MDBBR and MIXp_MDBCR and MIXp_MDBDR regardless of MIXp_MIXMR setting.

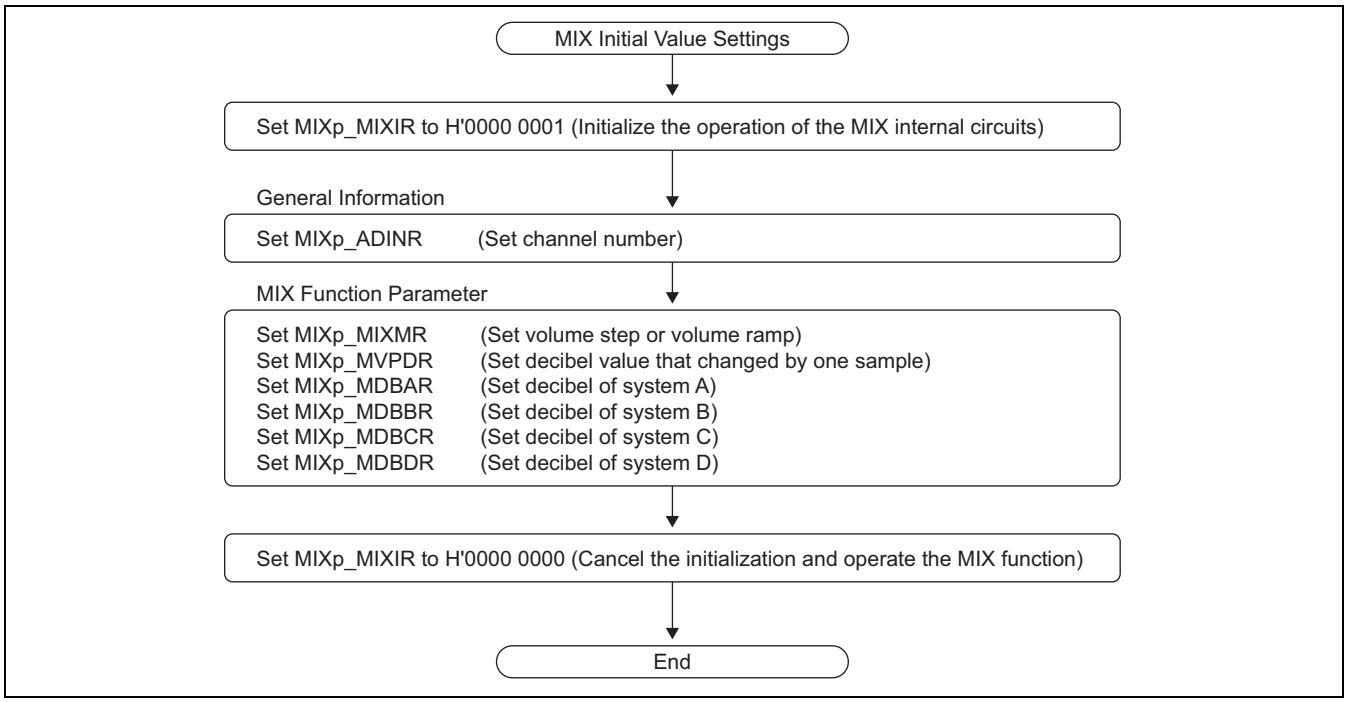


Figure 30.22 MIX Initial Value Setting Flowchart

- MIX Processing Parameter

  Figure 30.23 shows the MIX processing parameter flowchart. Before change the parameter of decibel for each system, the setting of the MIXp_MDBER should be disables. After that set the decibels of MIXp_MDBAR and MIXp_MDBBR and MIXp_MDBCR and MIXp_MDBDR and enables the MIXp_MDBER for reflect the decibel setting to the MIX processing.

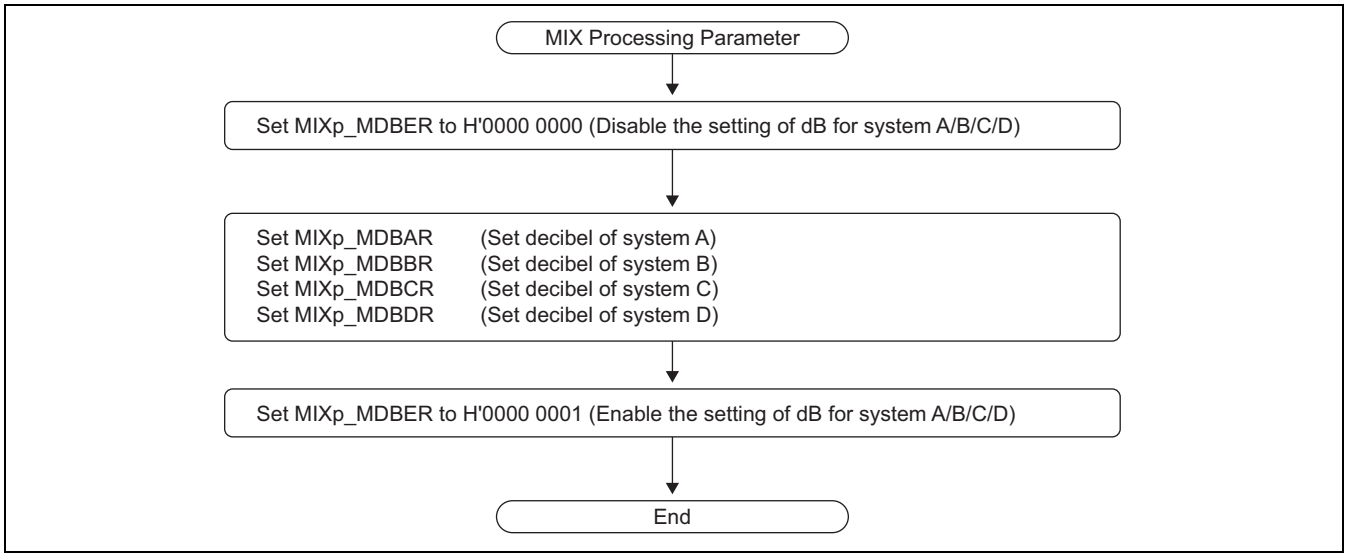


Figure 30.23 MIX Processing Parameter Flowchart

- MIX Initialization

  Figure 30.24 shows the MIX initialization flowchart. MIXp_MIXIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP.

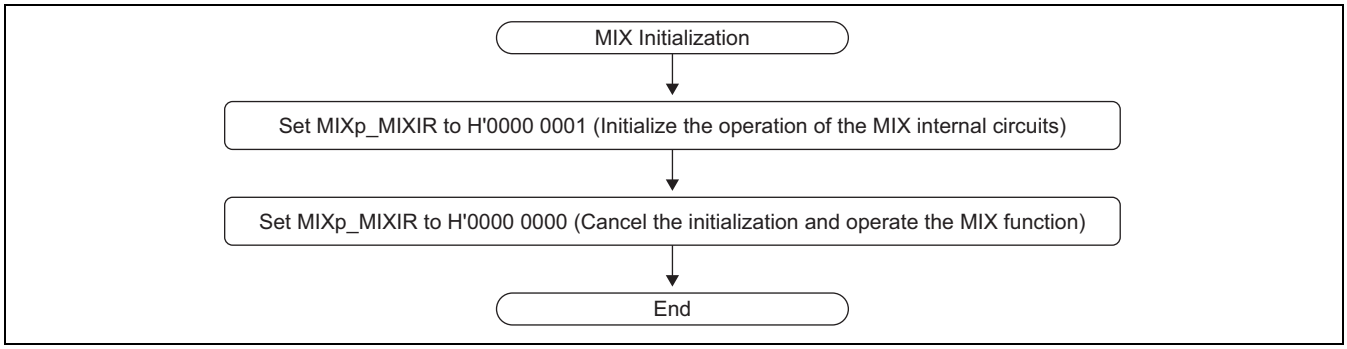


Figure 30.24 MIX Initialization Flowchart

- MIX Halting

  Figure 30.25 shows the flowchart of MIX halting. When MIX is halting, it should be initialized or reset by software reset or hardware reset. Before initializing or reset the MIX function, it is necessary to confirm the register settings and operation of peripheral IP.

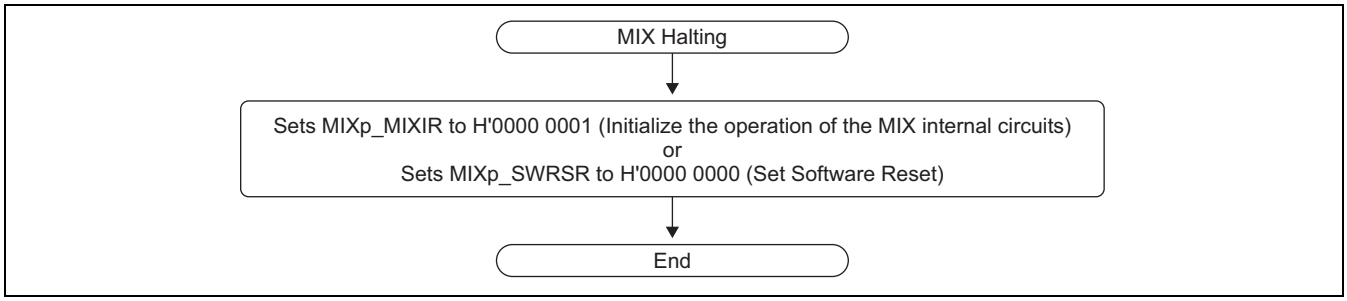


Figure 30.25 MIX Halting Flowchart

(3) DVC Block

The DVC is a block for implementing the volume and mute functions.

- Volume control function including digital volume, volume ramp, and zero-crossing mute
- The digital volume function is specified by a 24-bit fixed-point value within the range from 0 to 8 times (mute or -120 to 18 dB)
- The volume ramp function can be used for soft mute, fade-in, fade-out, or desired volume adjustment
- The volume ramp period can be changed within the sampling range from the 0th to 23rd power of 2
- The zero-crossing mute function silences the sound at the zero-crossing point of the audio data

Table 30.13 shows the DVC functions.

Table 30.13 DVC Functions

Item	Performance
Digital volume	Range: -120 dB to 18 dB (9.5×10^{-7} times to 8 times)
Volume ramp	Volume ramp is used for many kinds of operation (soft mute, fade-in, fade-out, and volume adjustment by ramp) Ramp period: 2^0/fso to 2^{23}/fso Examples: (1/fso: -128 dB/1 step) (2/fso: -64 dB/1 step) (4/fso: -32 dB/1 step) : (128/fso: -1 dB/1 step) (256/fso: -0.5 dB/1 step) (512/fso: -0.25 dB/1 step) (1024/fso: -0.125 dB/1 step) (2048/fso: -0.125 dB/2 steps) (4096/fso: -0.125 dB/4 steps) : (8388608/fso: -0.125 dB/8192 steps)
Zero-crossing mute	Mute the signal at zero-crossing point

The settings and corresponding values for the volume ramp are the same as those listed in Tables 30.9 to 30.12.

The settings and corresponding values for the digital volume are calculated by using the following formula:

Setting (decimal) = $10^X \times 1048576$
X = (value in dB) / 20

(a) Register Setting Procedure

The following describes the DVC register setting procedures. The register should be used according to the following procedures.

- DVC Processing Procedure
  Figure 30.26 shows the processing procedure of DVC.

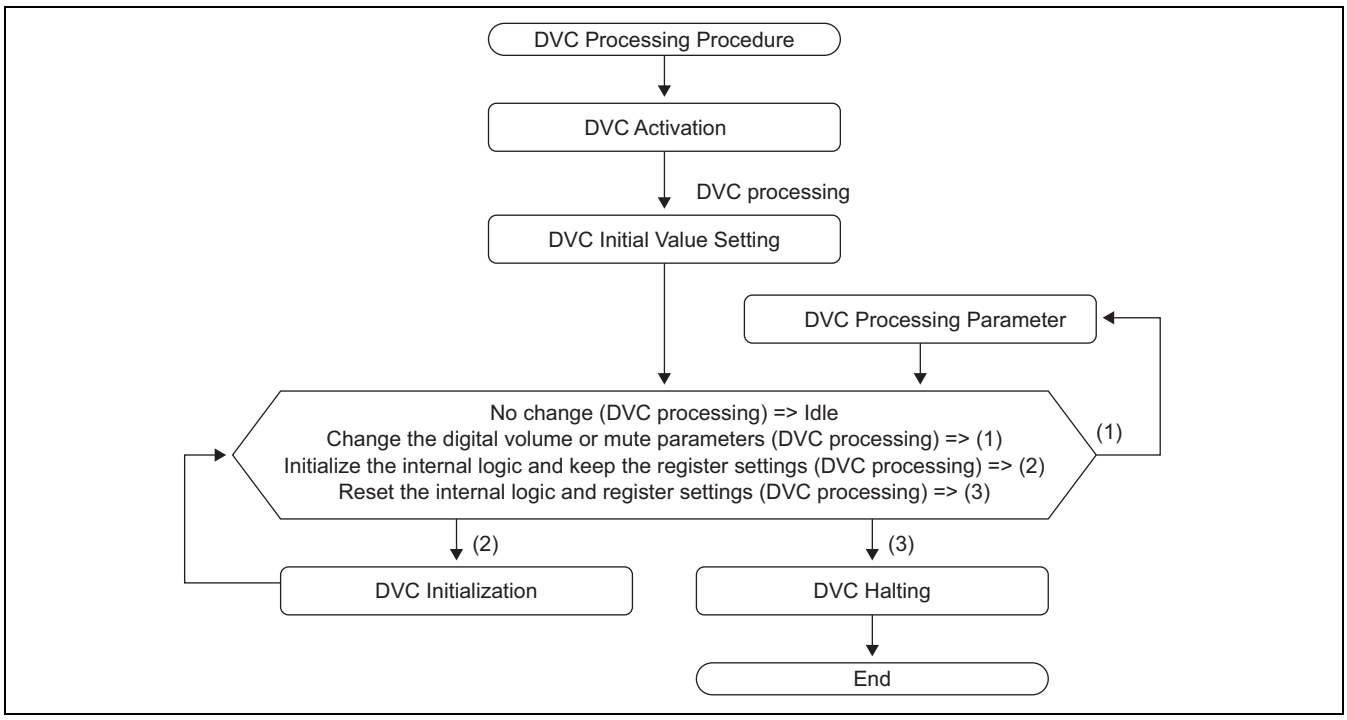


Figure 30.26 DVC Processing Procedure

- DVC Activation
  Figure 30.27 shows the DVC activation flowchart. When the DVC is activated, a software reset should be set to initialize logic and register setting. Then, the software reset should be cleared and ready to operate DVC. When reset the DVC function, all registers are initialized. If the DVC function was initialized by a hardware reset, it doesn't need to initialize the DVC function by software reset.

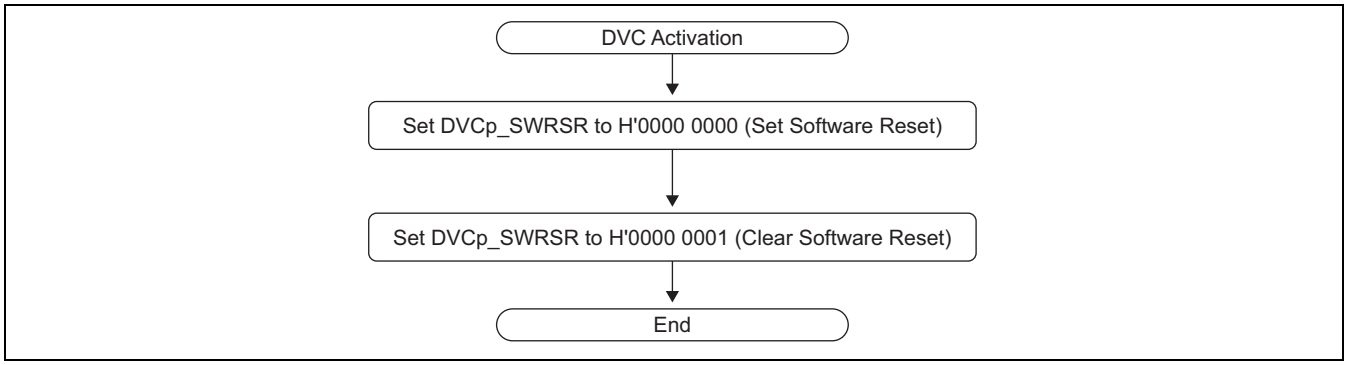


Figure 30.27 DVC Activation Flowchart

- DVC Initial Value Setting

  Figure 30.28 shows the flowchart of the DVC initial value setting. Before operating DVC function, the initial values should be set.

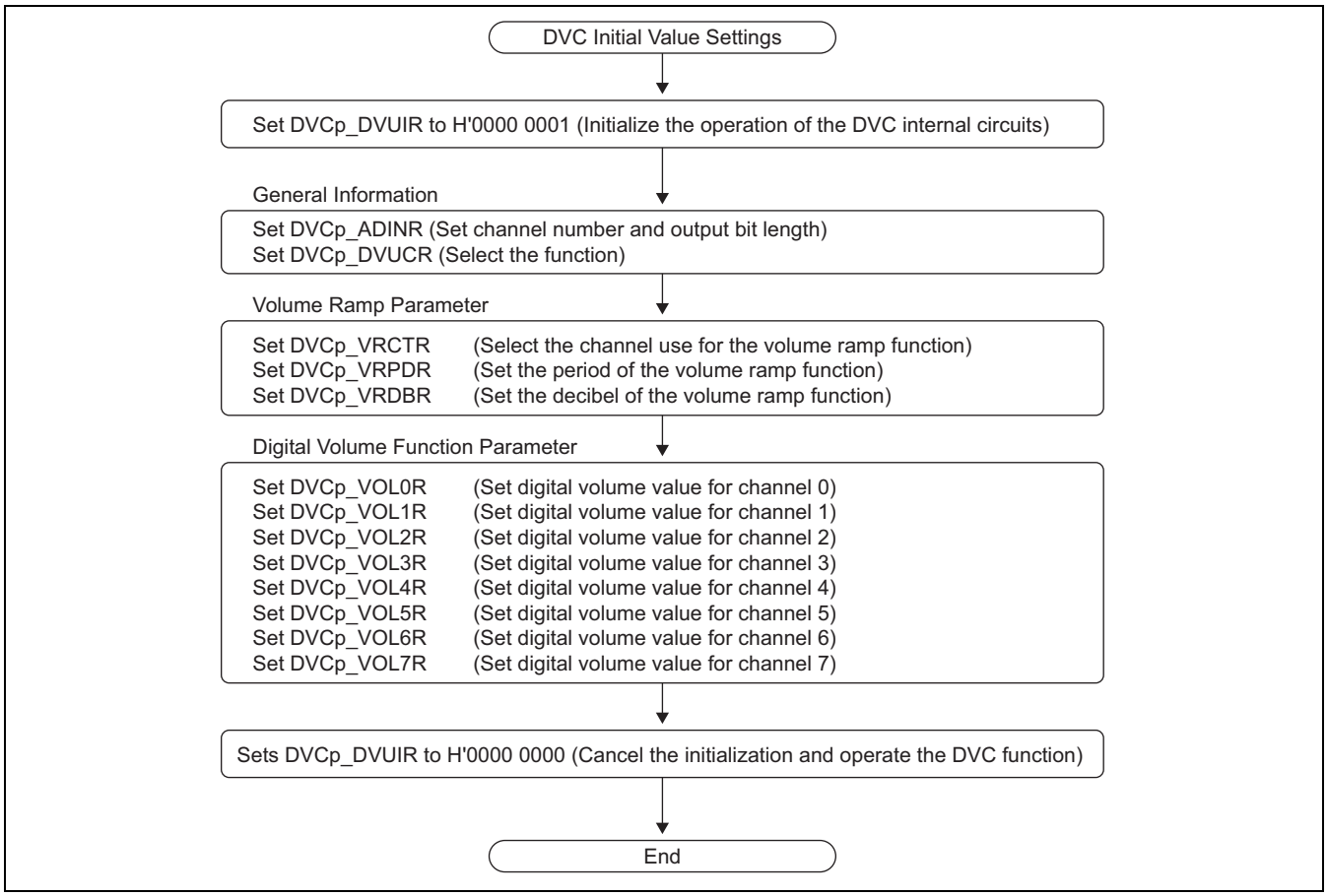


Figure 30.28 DVC Initial Value Setting Flowchart

- DVC Processing Parameter

  Figure 30.29 shows the DVC processing parameter flowchart. When DVC is processing, user can control the zero cross mute and the volume ramp and the digital volume value or by changing the setting value of registers. Before change the parameter of each function, the setting of DVCp_DVUER should be disables. After that set the setting of each function and enables the DVCp_DVUER for reflect the register setting to the DVC processing.

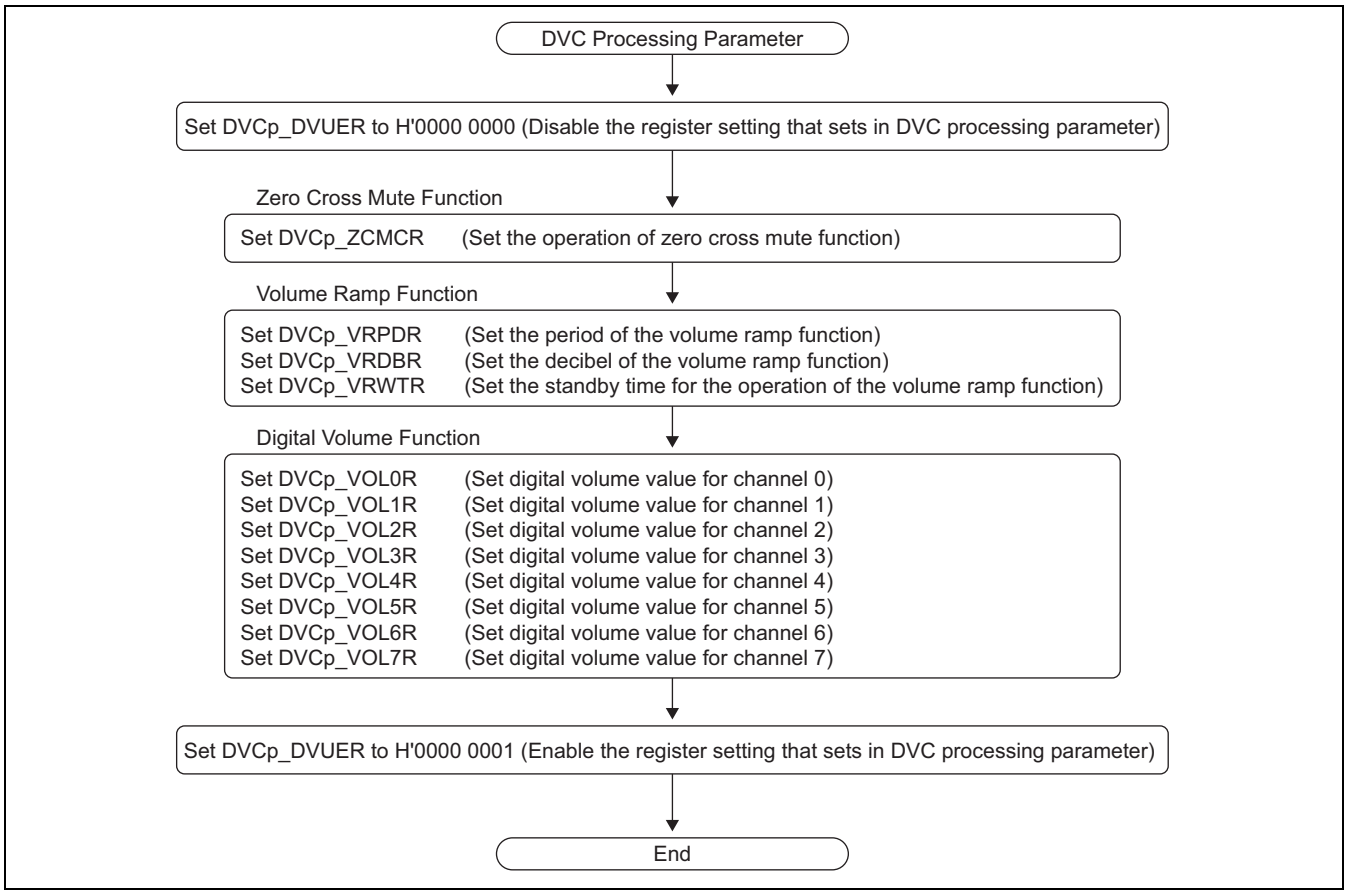


Figure 30.29 DVC Processing Parameter Flowchart

- DVC Initialization

  Figure 30.30 shows the flowchart of DVC Initialization. DVCp_DVUIR register doesn't initialize the register settings and these values are maintained. Before cancel the initialization, it is necessary to set or check the register settings of peripheral IP.

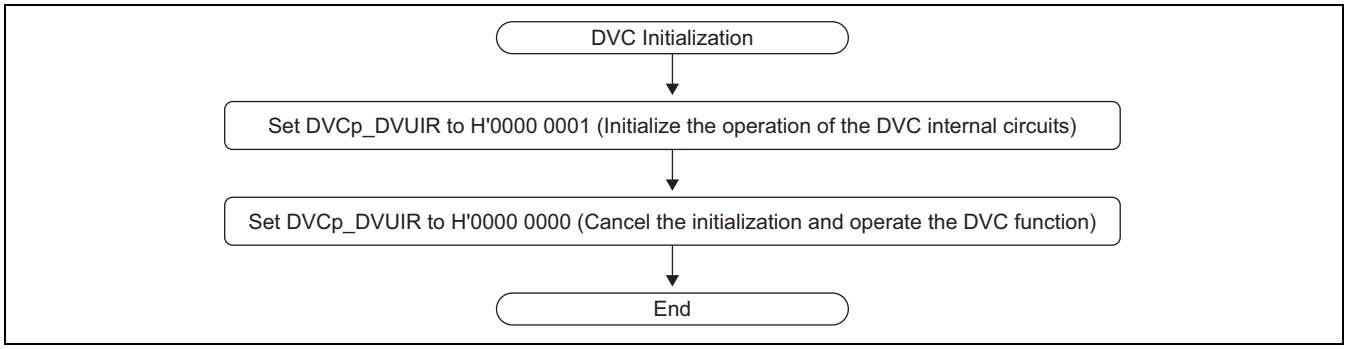


Figure 30.30 DVC Initialization Flowchart

- DVC Halting

  Figure 30.31 shows the flowchart of DVC halting. When DVC is halting, it should be initialized or reset by software reset or hardware reset. Before initializing or reset the DVC function, it is necessary to confirm the register settings and operation of peripheral IP.

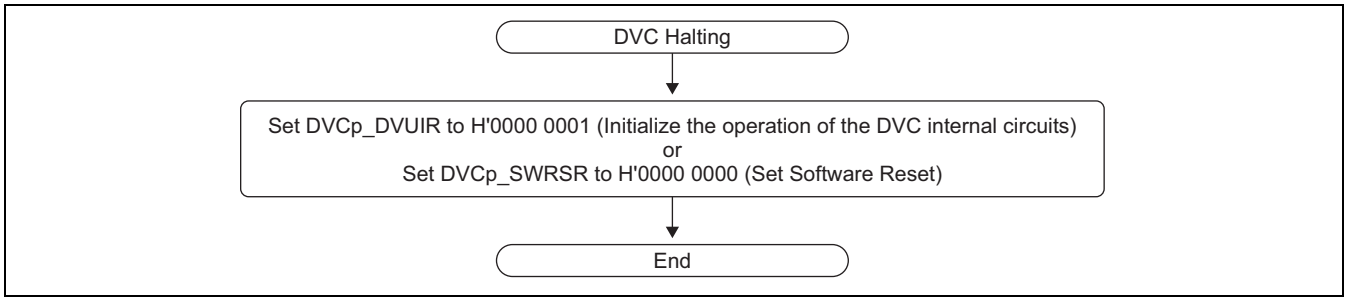


Figure 30.31 DVC Halting Flowchart

30.3.8 Input Data Timing and Output Data Timing

When using the SRC or CMD, the input data timing and output data timing should be specified. For details of the settings, refer to section 29, Audio Clock Generator (ADG).

30.4 Usage Notes

There is no attention of the usage.

31. Direct Memory Access Controller for Audio (Audio-DMAC)

This LSI includes a direct memory access controller for audio (audio-DMAC). The audio-DMAC can be used in place of the CPU to handle high-speed data transfer to and from an external memory, the on-chip memory, memory-mapped external devices, or on-chip peripheral modules.

31.1 Features

- 13 channels are available.
  Support: 13 channels (channels 0 to 12)
- 4-Gbyte physical address space
- Transfer data length: Byte, word (2 bytes), longword (4 bytes), 8 bytes, 16 bytes, 32 bytes, and 64 bytes
- Maximum number of transfer times: 16,777,215
- Address mode: Dual address mode
- Transfer requests:
  Requests from on-chip peripheral modules or auto requests can be selected. The following modules can issue on-chip peripheral module requests.
  SSI0 to SSI9, SCU1 to SCU6
- Selectable bus modes:
  Normal speed mode or slow mode can be selected for each channel.
- Either fixed priority or round-robin arbitration can be selected for use in arbitration among the transfer channels.
- Interrupt request:
  The audio-DMAC can be set up to generate an interrupt request for the CPU upon completion of transfer under the control of one stage of the descriptor memory, at the end of the data transfer, in response to an MMU error, and in response to an address error.
- Descriptor memory function:
  Up to 128 sets of the settings for the source address register, destination address register, and transfer count register are available (if use of the descriptor memory is only enabled for one channel) for use in setting up consecutive DMA transfers (the memory can hold register values for up to 256 stages of transfer when the external memory is selected). An infinite repeat mode is also available.

Figure 31.1 shows the block diagram of the audio-DMAC.

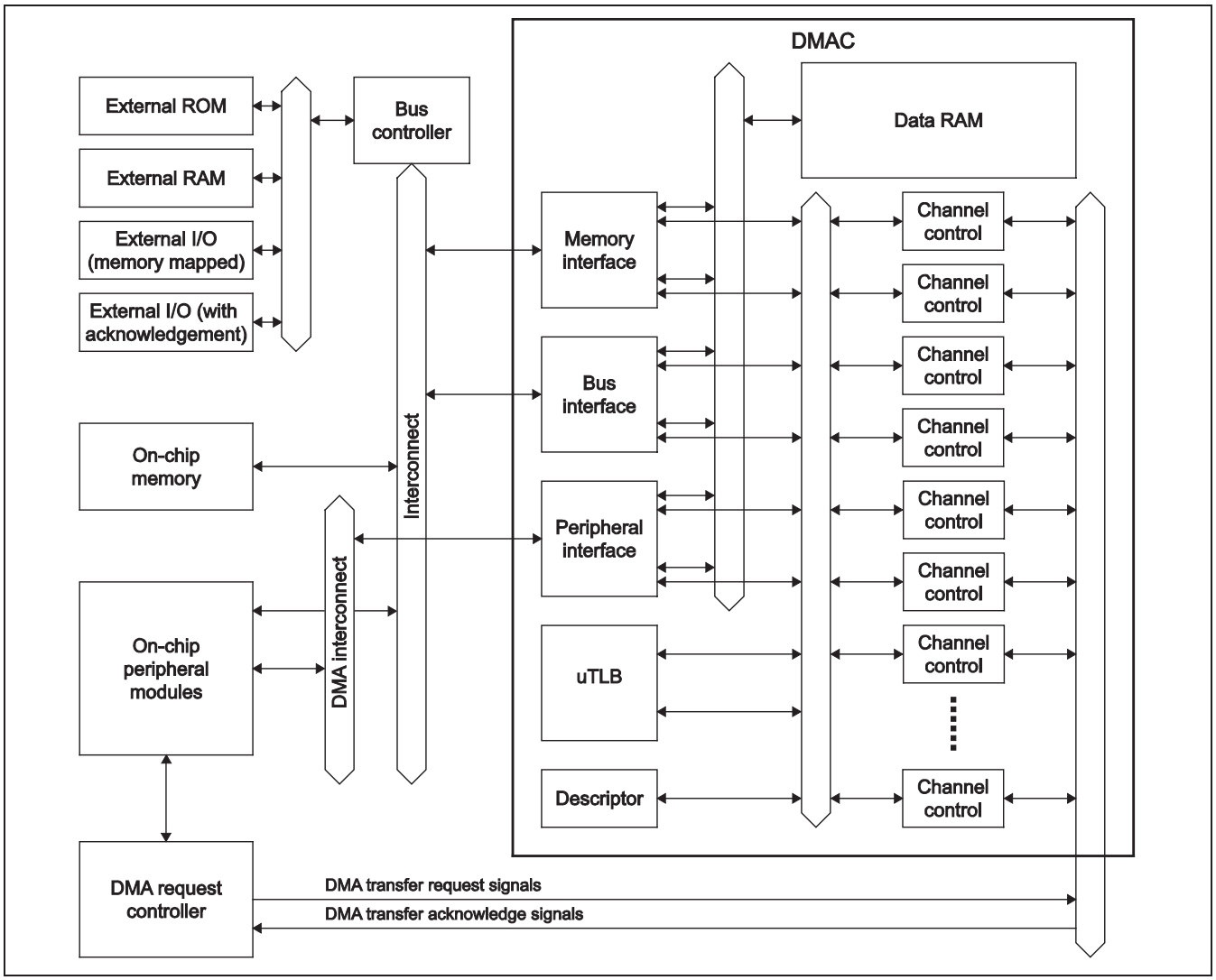


Figure 31.1 Block Diagram of the Audio-DMAC

31.2 Input/Output Pins

There are no external pins relevant to the audio-DMAC.

31.3 Register Descriptions

Table 31.1 lists the registers of the audio-DMAC. Table 31.2 shows the register states of the audio-DMAC in each operating mode.

Table 31.1 Register Configuration of the Audio-DMAC

Name	Abbreviation	R/W	Address	Access Size
DMA interrupt status register	DMAISTA	R	H'EC70 0020	32
DMA secure control register	DMASEC	R/W	H'EC70 0030	32
DMA operation register	DMAOR	R/W	H'EC70 0060	16
DMA channel clear register	DMACHCLR	W	H'EC70 0080	32
DPRAM secure control register	DMADPSEC	R/W	H'EC70 00A0	32
DMA source address register_0	DMASAR_0	R/W	H'EC70 8000 H'EC70 8020*	32
DMA destination address register_0	DMADAR_0	R/W	H'EC70 8004 H'EC70 8024*	32
DMA transfer count register_0	DMATCR_0	R/W	H'EC70 8008	32
DMA transfer size register_0	DMATSR_0	R/W	H'EC70 8028*	32
DMA channel control register_0	DMACHCR_0	R/W	H'EC70 800C H'EC70 802C*	32
DMA transfer count register B_0	DMATCRB_0	R/W	H'EC70 8018	32
DMA transfer size register B_0	DMATSRB_0	R/W	H'EC70 8038	32
DMA channel control register B_0	DMACHCRB_0	R/W	H'EC70 801C	32
DMA extended resource selector_0	DMARS_0	R/W	H'EC70 8040	16
DMA buffer control register_0	DMABUFCR_0	R/W	H'EC70 8048	32
DMA descriptor base address register_0	DMADPBASE_0	R/W	H'EC70 8050	32
DMA descriptor control register_0	DMADPCR_0	R/W	H'EC70 8054	32
DMA fixed source address register_0	DMAFIXSAR_0	R/W	H'EC70 8010	32
DMA fixed destination address register_0	DMAFIXDAR_0	R/W	H'EC70 8014	32
DMA fixed descriptor base address register_0	DMAFIXDP BASE_0	R/W	H'EC70 8060	32
DMA source address register_1	DMASAR_1	R/W	H'EC70 8080 H'EC70 80A0*	32
DMA destination address register_1	DMADAR_1	R/W	H'EC70 8084 H'EC70 80A4*	32
DMA transfer count register_1	DMATCR_1	R/W	H'EC70 8088	32
DMA transfer size register_1	DMATSR_1	R/W	H'EC70 80A8*	32
DMA channel control register_1	DMACHCR_1	R/W	H'EC70 808C H'EC70 80AC*	32
DMA transfer count register B_1	DMATCRB_1	R/W	H'EC70 8098	32
DMA transfer size register B_1	DMATSRB_1	R/W	H'EC70 80B8*	32
DMA channel control register B_1	DMACHCRB_1	R/W	H'EC70 809C	32
DMA extended resource selector_1	DMARS_1	R/W	H'EC70 80C0	16
DMA buffer control register_1	DMABUFCR_1	R/W	H'EC70 80C8	32

Name	Abbreviation	R/W	Address	Access Size
DMA descriptor base address register_1	DMADPBASE_1	R/W	H'EC70 80D0	32
DMA descriptor control register_1	DMADPCR_1	R/W	H'EC70 80D4	32
DMA fixed descriptor base address register_1	DMAFIXDPBASE_1	R/W	H'EC70 80E0	32
DMA fixed source address register_1	DMAFIXSAR_1	R/W	H'EC70 8090	32
DMA fixed destination address register_1	DMAFIXDAR_1	R/W	H'EC70 8094	32
DMA source address register_2	DMASAR_2	R/W	H'EC70 8100 H'EC70 8120*	32
DMA destination address register_2	DMADAR_2	R/W	H'EC70 8104 H'EC70 8124*	32
DMA transfer count register_2	DMATCR_2	R/W	H'EC70 8108	32
DMA transfer size register_2	DMATSR_2	R/W	H'EC70 8128*	32
DMA channel control register_2	DMACHCR_2	R/W	H'EC70 810C H'EC70 812C*	32
DMA transfer count register B_2	DMATCRB_2	R/W	H'EC70 8118	32
DMA transfer size register B_2	DMATSRB_2	R/W	H'EC70 8138*	32
DMA channel control register B_2	DMACHCRB_2	R/W	H'EC70 811C	32
DMA extended resource selector_2	DMARS_2	R/W	H'EC70 8140	16
DMA buffer control register_2	DMABUFCR_2	R/W	H'EC70 8148	32
DMA descriptor base address register_2	DMADPBASE_2	R/W	H'EC70 8150	32
DMA descriptor control register_2	DMADPCR_2	R/W	H'EC70 8154	32
DMA fixed source address register_2	DMAFIXSAR_2	R/W	H'EC70 8110	32
DMA fixed destination address register_2	DMAFIXDAR_2	R/W	H'EC70 8114	32
DMA fixed descriptor base address register_2	DMAFIXDPBASE_2	R/W	H'EC70 8160	32
DMA source address register_3	DMASAR_3	R/W	H'EC70 8180 H'EC70 81A0*	32
DMA destination address register_3	DMADAR_3	R/W	H'EC70 8184 H'EC70 81A4*	32
DMA transfer count register_3	DMATCR_3	R/W	H'EC70 8188	32
DMA transfer size register_3	DMATSR_3	R/W	H'EC70 81A8*	32
DMA channel control register_3	DMACHCR_3	R/W	H'EC70 818C H'EC70 81AC*	32
DMA transfer count register B_3	DMATCRB_3	R/W	H'EC70 8198	32
DMA transfer size register B_3	DMATSRB_3	R/W	H'EC70 81B8*	32
DMA channel control register B_3	DMACHCRB_3	R/W	H'EC70 819C	32
DMA extended resource selector_3	DMARS_3	R/W	H'EC70 81C0	16
DMA buffer control register_3	DMABUFCR_3	R/W	H'EC70 81C8	32
DMA descriptor base address register_3	DMADPBASE_3	R/W	H'EC70 81D0	32
DMA descriptor control register_3	DMADPCR_3	R/W	H'EC70 81D4	32
DMA fixed source address register_3	DMAFIXSAR_3	R/W	H'EC70 8190	32
DMA fixed destination address register_3	DMAFIXDAR_3	R/W	H'EC70 8194	32
DMA fixed descriptor base address register_3	DMAFIXDPBASE_3	R/W	H'EC70 81E0	32
DMA source address register_4	DMASAR_4	R/W	H'EC70 8200 H'EC70 8220*	32

Name	Abbreviation	R/W	Address	Access Size
DMA destination address register_4	DMADAR_4	R/W	H'EC70 8204 H'EC70 8224*	32
DMA transfer count register_4	DMATCR_4	R/W	H'EC70 8208	32
DMA transfer size register_4	DMATSR_4	R/W	H'EC70 8228*	32
DMA channel control register_4	DMACHCR_4	R/W	H'EC70 820C H'EC70 822C*	32
DMA transfer count register B_4	DMATCRB_4	R/W	H'EC70 8218	32
DMA transfer size register B_4	DMATSRB_4	R/W	H'EC70 8238*	32
DMA channel control register B_4	DMACHCRB_4	R/W	H'EC70 821C	32
DMA extended resource selector_4	DMARS_4	R/W	H'EC70 8240	16
DMA buffer control register_4	DMABUFCR_4	R/W	H'EC70 8248	32
DMA descriptor base address register_4	DMADPBASE_4	R/W	H'EC70 8250	32
DMA descriptor control register_4	DMADPCR_4	R/W	H'EC70 8254	32
DMA fixed source address register_4	DMAFIXSAR_4	R/W	H'EC70 8210	32
DMA fixed destination address register_4	DMAFIXDAR_4	R/W	H'EC70 8214	32
DMA fixed descriptor base address register_4	DMAFIXDPBASE_4	R/W	H'EC70 8260	32
DMA source address register_5	DMASAR_5	R/W	H'EC70 8280 H'EC70 82A0*	32
DMA destination address register_5	DMADAR_5	R/W	H'EC70 8284 H'EC70 82A4*	32
DMA transfer count register_5	DMATCR_5	R/W	H'EC70 8288	32
DMA transfer size register_5	DMATSR_5	R/W	H'EC70 82A8*	32
DMA channel control register_5	DMACHCR_5	R/W	H'EC70 828C H'EC70 82AC*	32
DMA transfer count register B_5	DMATCRB_5	R/W	H'EC70 8298	32
DMA transfer size register B_5	DMATSRB_5	R/W	H'EC70 82B8*	32
DMA channel control register B_5	DMACHCRB_5	R/W	H'EC70 829C	32
DMA extended resource selector_5	DMARS_5	R/W	H'EC70 82C0	16
DMA buffer control register_5	DMABUFCR_5	R/W	H'EC70 82C8	32
DMA descriptor base address register_5	DMADPBASE_5	R/W	H'EC70 82D0	32
DMA descriptor control register_5	DMADPCR_5	R/W	H'EC70 82D4	32
DMA fixed source address register_5	DMAFIXSAR_5	R/W	H'EC70 8290	32
DMA fixed destination address register_5	DMAFIXDAR_5	R/W	H'EC70 8294	32
DMA fixed descriptor base address register_5	DMAFIXDPBASE_5	R/W	H'EC70 82E0	32
DMA source address register_6	DMASAR_6	R/W	H'EC70 8300 H'EC70 8320*	32
DMA destination address register_6	DMADAR_6	R/W	H'EC70 8304 H'EC70 8324*	32
DMA transfer count register_6	DMATCR_6	R/W	H'EC70 8308	32
DMA transfer size register_6	DMATSR_6	R/W	H'EC70 8328*	32
DMA channel control register_6	DMACHCR_6	R/W	H'EC70 830C H'EC70 832C*	32
DMA transfer count register B_6	DMATCRB_6	R/W	H'EC70 8318	32

Name	Abbreviation	R/W	Address	Access Size
DMA transfer size register B_6	DMATSRB_6	R/W	H'EC70 8338*	32
DMA channel control register B_6	DMACHCRB_6	R/W	H'EC70 831C	32
DMA extended resource selector_6	DMARS_6	R/W	H'EC70 8340	16
DMA buffer control register_6	DMABUFCR_6	R/W	H'EC70 8348	32
DMA descriptor base address register_6	DMADPBASE_6	R/W	H'EC70 8350	32
DMA descriptor control register_6	DMADPCR_6	R/W	H'EC70 8354	32
DMA fixed source address register_6	DMAFIXSAR_6	R/W	H'EC70 8310	32
DMA fixed destination address register_6	DMAFIXDAR_6	R/W	H'EC70 8314	32
DMA fixed descriptor base address register_6	DMAFIXDPBASE_6	R/W	H'EC70 8360	32
DMA source address register_7	DMASAR_7	R/W	H'EC70 8380 H'EC70 83A0*	32
DMA destination address register_7	DMADAR_7	R/W	H'EC70 8384 H'EC70 83A4*	32
DMA transfer count register_7	DMATCR_7	R/W	H'EC70 8388	32
DMA transfer size register_7	DMATSR_7	R/W	H'EC70 83A8*	32
DMA channel control register_7	DMACHCR_7	R/W	H'EC70 838C H'EC70 83AC*	32
DMA transfer count register B_7	DMATCRB_7	R/W	H'EC70 8398	32
DMA transfer size register B_7	DMATSRB_7	R/W	H'EC70 83B8*	32
DMA channel control register B_7	DMACHCRB_7	R/W	H'EC70 839C	32
DMA extended resource selector_7	DMARS_7	R/W	H'EC70 83C0	16
DMA buffer control register_7	DMABUFCR_7	R/W	H'EC70 83C8	32
DMA descriptor base address register_7	DMADPBASE_7	R/W	H'EC70 83D0	32
DMA descriptor control register_7	DMADPCR_7	R/W	H'EC70 83D4	32
DMA fixed source address register_7	DMAFIXSAR_7	R/W	H'EC70 8390	32
DMA fixed destination address register_7	DMAFIXDAR_7	R/W	H'EC70 8394	32
DMA fixed descriptor base address register_7	DMAFIXDPBASE_7	R/W	H'EC70 83E0	32
DMA source address register_8	DMASAR_8	R/W	H'EC70 8400 H'EC70 8420*	32
DMA destination address register_8	DMADAR_8	R/W	H'EC70 8404 H'EC70 8424*	32
DMA transfer count register_8	DMATCR_8	R/W	H'EC70 8408	32
DMA transfer size register_8	DMATSR_8	R/W	H'EC70 8428*	32
DMA channel control register_8	DMACHCR_8	R/W	H'EC70 840C H'EC70 842C*	32
DMA transfer count register B_8	DMATCRB_8	R/W	H'EC70 8418	32
DMA transfer size register B_8	DMATSRB_8	R/W	H'EC70 8438*	32
DMA channel control register B_8	DMACHCRB_8	R/W	H'EC70 841C	32
DMA extended resource selector_8	DMARS_8	R/W	H'EC70 8440	16
DMA buffer control register_8	DMABUFCR_8	R/W	H'EC70 8448	32
DMA descriptor base address register_8	DMADPBASE_8	R/W	H'EC70 8450	32
DMA descriptor control register_8	DMADPCR_8	R/W	H'EC70 8454	32
DMA fixed source address register_8	DMAFIXSAR_8	R/W	H'EC70 8410	32

Name	Abbreviation	R/W	Address	Access Size
DMA fixed destination address register_8	DMAFIXDAR_8	R/W	H'EC70 8414	32
DMA fixed descriptor base address register_8	DMAFIXDPBASE_8	R/W	H'EC70 8460	32
DMA source address register_9	DMASAR_9	R/W	H'EC70 8480 H'EC70 84A0*	32
DMA destination address register_9	DMADAR_9	R/W	H'EC70 8484 H'EC70 84A4*	32
DMA transfer count register_9	DMATCR_9	R/W	H'EC70 8488	32
DMA transfer size register_9	DMATSR_9	R/W	H'EC70 84A8*	32
DMA channel control register_9	DMACHCR_9	R/W	H'EC70 848C H'EC70 84AC*	32
DMA transfer count register B_9	DMATCRB_9	R/W	H'EC70 8498	32
DMA transfer size register B_9	DMATSRB_9	R/W	H'EC70 84B8*	32
DMA channel control register B_9	DMACHCRB_9	R/W	H'EC70 849C	32
DMA extended resource selector_9	DMARS_9	R/W	H'EC70 84C0	16
DMA buffer control register_9	DMABUFCR_9	R/W	H'EC70 84C8	32
DMA descriptor base address register_9	DMADPBASE_9	R/W	H'EC70 84D0	32
DMA descriptor control register_9	DMADPCR_9	R/W	H'EC70 84D4	32
DMA fixed source address register_9	DMAFIXSAR_9	R/W	H'EC70 8490	32
DMA fixed destination address register_9	DMAFIXDAR_9	R/W	H'EC70 8494	32
DMA fixed descriptor base address register_9	DMAFIXDPBASE_9	R/W	H'EC70 84E0	32
DMA source address register_10	DMASAR_10	R/W	H'EC70 8500 H'EC70 8520*	32
DMA destination address register_10	DMADAR_10	R/W	H'EC70 8504 H'EC70 8524*	32
DMA transfer count register_10	DMATCR_10	R/W	H'EC70 8508	32
DMA transfer size register_10	DMATSR_10	R/W	H'EC70 8528*	32
DMA channel control register_10	DMACHCR_10	R/W	H'EC70 850C H'EC70 852C*	32
DMA transfer count register B_10	DMATCRB_10	R/W	H'EC70 8518	32
DMA transfer size register B_10	DMATSRB_10	R/W	H'EC70 8538*	32
DMA channel control register B_10	DMACHCRB_10	R/W	H'EC70 851C	32
DMA extended resource selector_10	DMARS_10	R/W	H'EC70 8540	16
DMA buffer control register_10	DMABUFCR_10	R/W	H'EC70 8548	32
DMA descriptor base address register_10	DMADPBASE_10	R/W	H'EC70 8550	32
DMA descriptor control register_10	DMADPCR_10	R/W	H'EC70 8554	32
DMA fixed source address register_10	DMAFIXSAR_10	R/W	H'EC70 8510	32
DMA fixed destination address register_10	DMAFIXDAR_10	R/W	H'EC70 8514	32
DMA fixed descriptor base address register_10	DMAFIXDPBASE_10	R/W	H'EC70 8560	32
DMA source address register_11	DMASAR_11	R/W	H'EC70 8580 H'EC70 85A0*	32
DMA destination address register_11	DMADAR_11	R/W	H'EC70 8584 H'EC70 85A4*	32
DMA transfer count register_11	DMATCR_11	R/W	H'EC70 8588	32

Name	Abbreviation	R/W	Address	Access Size
DMA transfer size register_11	DMATSR_11	R/W	H'EC70 85A8*	32
DMA channel control register_11	DMACHCR_11	R/W	H'EC70 858C H'EC70 85AC*	32
DMA transfer count register B_11	DMATCRB_11	R/W	H'EC70 8598	32
DMA transfer size register B_11	DMATSRB_11	R/W	H'EC70 85B8*	32
DMA channel control register B_11	DMACHCRB_11	R/W	H'EC70 859C	32
DMA extended resource selector_11	DMARS_11	R/W	H'EC70 85C0	16
DMA buffer control register_11	DMABUFCR_11	R/W	H'EC70 85C8	32
DMA descriptor base address register_11	DMADPBASE_11	R/W	H'EC70 85D0	32
DMA descriptor control register_11	DMADPCR_11	R/W	H'EC70 85D4	32
DMA fixed source address register_11	DMAFIXSAR_11	R/W	H'EC70 8590	32
DMA fixed destination address register_11	DMAFIXDAR_11	R/W	H'EC70 8594	32
DMA fixed descriptor base address register_11	DMAFIXDPBASE_11	R/W	H'EC70 85E0	32
DMA source address register_12	DMASAR_12	R/W	H'EC70 8600 H'EC70 8620*	32
DMA destination address register_12	DMADAR_12	R/W	H'EC70 8604 H'EC70 8624*	32
DMA transfer count register_12	DMATCR_12	R/W	H'EC70 8608	32
DMA transfer size register_12	DMATSR_12	R/W	H'EC70 8628*	32
DMA channel control register_12	DMACHCR_12	R/W	H'EC70 860C H'EC70 862C*	32
DMA transfer count register B_12	DMATCRB_12	R/W	H'EC70 8618	32
DMA transfer size register B_12	DMATSRB_12	R/W	H'EC70 8638*	32
DMA channel control register B_12	DMACHCRB_12	R/W	H'EC70 861C	32
DMA extended resource selector_12	DMARS_12	R/W	H'EC70 8640	16
DMA buffer control register_12	DMABUFCR_12	R/W	H'EC70 8648	32
DMA descriptor base address register_12	DMADPBASE_12	R/W	H'EC70 8650	32
DMA descriptor control register_12	DMADPCR_12	R/W	H'EC70 8654	32
DMA fixed source address register_12	DMAFIXSAR_12	R/W	H'EC70 8610	32
DMA fixed destination address register_12	DMAFIXDAR_12	R/W	H'EC70 8614	32
DMA fixed descriptor base address register_12	DMAFIXDPBASE_12	R/W	H'EC70 8660	32
Descriptor memory	DescriptorMEM	R/W	H'EC70 A000 to H'EC70 A7FC	32

Note: * This address is used in total size transmission (see section 31.4.6, Total Size Transmission).

Table 31.2 States of Audio-DMAC Registers in each Operating Mode

Abbreviation	Power-On Reset	Module Standby
DMAISTA	Initialized	Retained
DMASEC	Initialized	Retained
DMAOR	Initialized	Retained
DMACHCLR	Initialized	Retained
DMADPSEC	Initialized	Retained
DMASAR_0 to DMASAR_12	Initialized	Retained
DMADAR_0 to DMADAR_12	Initialized	Retained
DMATCR_0 to DMATCR_12	Initialized	Retained
DMATSR_0 to DMATSR_12	Initialized	Retained
DMACHCR_0 to DMACHCR_12	Initialized	Retained
DMATCRB_0 DMATCRB_12	Initialized	Retained
DMATSRB_0 to DMATSRB_12	Initialized	Retained
DMACHCRB_0 to DMACHCRB_12	Initialized	Retained
DMABUFCR_0 to DMABUFCR_12	Initialized	Retained
DMARS_0 to DMARS_12	Initialized	Retained
DMADPBASE_0 to DMADPBASE_12	Initialized	Retained
DMADPCR_0 to DMADPCR_12	Initialized	Retained
DMAFIXSAR_0 to DMAFIXSAR_12	Initialized	Retained
DMAFIXDAR_0 to DMAFIXDAR_12	Initialized	Retained
DMAFIXDPBASE_0 to DMAFIXDPBASE_12	Initialized	Retained
DescriptorMEM	Undefined	Retained

31.3.1 DMA Interrupt Status Register (DMAISTA)

DMAISTA is a 32-bit readable register that indicates the states of the interrupt signals for each of the lower-numbered channels.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	I12	I11	I10	I9	I8	I7	I6	I5	I4	I3	I2	I1	I0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	I12	0	R	Interrupt State in Channel 12 0: An interrupt is not present. 1: An interrupt is present.
11	I11	0	R	Interrupt State in Channel 11 0: An interrupt is not present. 1: An interrupt is present.
10	I10	0	R	Interrupt State in Channel 10 0: An interrupt is not present. 1: An interrupt is present.
9	I9	0	R	Interrupt State in Channel 9 0: An interrupt is not present. 1: An interrupt is present.
8	I8	0	R	Interrupt State in Channel 8 0: An interrupt is not present. 1: An interrupt is present.

Bit	Bit Name	Initial Value	R/W	Descriptions
7	I7	0	R	Interrupt State in Channel 7 0: An interrupt is not present. 1: An interrupt is present.
6	I6	0	R	Interrupt State in Channel 6 0: An interrupt is not present. 1: An interrupt is present.
5	I5	0	R	Interrupt State in Channel 5 0: An interrupt is not present. 1: An interrupt is present.
4	I4	0	R	Interrupt State in Channel 4 0: An interrupt is not present. 1: An interrupt is present.
3	I3	0	R	Interrupt State in Channel 3 0: An interrupt is not present. 1: An interrupt is present.
2	I2	0	R	Interrupt State in Channel 2 0: An interrupt is not present. 1: An interrupt is present.
1	I1	0	R	Interrupt State in Channel 1 0: An interrupt is not present. 1: An interrupt is present.
0	I0	0	R	Interrupt State in Channel 0 0: An interrupt is not present. 1: An interrupt is present.

31.3.2 DMA Secure Control Register (DMASEC)

DMASEC is a 32-bit readable/writeable register that controls the security attribute of each channels. Only the initiator in the secure mode can change the setting of this register.

Only secure access is allowed to registers of channels with the secure mode setting. The following registers are protected by the secure mode.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	S12	S11	S10	S9	S8	S7	S6	S5	S4	S3	S2	S1	S0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	S12	0	R/W	Secure Mode Setting for Channel 12 0: Non-secure mode 1: Secure mode
11	S11	0	R/W	Secure Mode Setting for Channel 11 0: Non-secure mode 1: Secure mode
10	S10	0	R/W	Secure Mode Setting for Channel 10 0: Non-secure mode 1: Secure mode
9	S9	0	R/W	Secure Mode Setting for Channel 9 0: Non-secure mode 1: Secure mode
8	S8	0	R/W	Secure Mode Setting for Channel 8 0: Non-secure mode 1: Secure mode
7	S7	0	R/W	Secure Mode Setting for Channel 7 0: Non-secure mode 1: Secure mode
6	S6	0	R/W	Secure Mode Setting for Channel 6 0: Non-secure mode 1: Secure mode

Bit	Bit Name	Initial Value	R/W	Descriptions
5	S5	0	R/W	Secure Mode Setting for Channel 5 0: Non-secure mode 1: Secure mode
4	S4	0	R/W	Secure Mode Setting for Channel 4 0: Non-secure mode 1: Secure mode
3	S3	0	R/W	Secure Mode Setting for Channel 3 0: Non-secure mode 1: Secure mode
2	S2	0	R/W	Secure Mode Setting for Channel 2 0: Non-secure mode 1: Secure mode
1	S1	0	R/W	Secure Mode Setting for Channel 1 0: Non-secure mode 1: Secure mode
0	S0	0	R/W	Secure Mode Setting for Channel 0 0: Non-secure mode 1: Secure mode

31.3.3 DMA Operation Register (DMAOR)

DMAOR is a 16-bit readable/writable register that enables DMA transfer on all channels and specifies the method used to determine the priority levels for all DMA channels. This register also indicates address errors.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PR[1:0]		—	—	—	—	—	AE	—	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R/(W)*	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	PR[1:0]	00	R/W	Priority Mode Select the method for setting the order of priority of channels when transfer requests for multiple channels arrive simultaneously. 00: Fixed CH0 > CH1 > ... > CH11 > CH12 11: Round-robin priority Other than above: Setting prohibited
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	AE	0	R/(W)*	Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the AE bit, write 0 to the AE bit after reading 1 from it or clear the CAE bit for each channel for which it is set. Clearing the AE bit clears the channel address error bits for all channels. 0: An audio-DMAC address error interrupt is not present. [Clearing condition] (*) Writing CAE = 0 after reading CAE = 1 1: An audio-DMAC address error interrupt being generated during DMA transfer.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfer on all channels. If the DME bit and the DE bit in DMACHCR are both set to 1, DMA transfer is enabled. At this time all AE bits in DMAOR must have the value 0. For DMA transfer on a channel to then proceed, the TE bit in DMACHCR for the channel must also have the value 0. Clearing this bit during transfer aborts transfer on all channels. 0: Disables DMA transfers on all channels 1: Enables DMA transfers on all channels

31.3.4 DMA Channel Clear Register (DMACHCLR)

DMACHCLR is a 32-bit writable register that initializes each of channels.

When a bit of this register is set, the state of the corresponding channel is completely initialized.
This includes initialization of the following registers.

DMASAR, DMADAR, DMATCR, DMATSR, DMACHCR, DMATCRB, DMATSRB, DMACHCRB, DMARS, DMABUFCR, DMADPBASE, DMADPCR, DMAFIXSAR, DMAFIXDAR, and DMAFIXDPBASE

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CLR[12:0]												
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 0	CLR[12:0]	All 0	W	Writing to a bit leads to clearing of all registers for the corresponding channel. CLR[0] 0: Ignored 1: All registers for channel 0 are cleared. CLR[1] 0: Ignored 1: All registers for channel 1 are cleared. CLR[2] 0: Ignored 1: All registers for channel 2 are cleared. ... CLR[12] 0: Ignored 1: All registers for channel 12 are cleared. When writing to this register, confirm that the DE bit is set to 0.

31.3.5 DPRAM Secure Control Register (DMADPSEC)

DMADPSEC is a 32-bit readable/writeable register that controls the security attribute of the descriptor memory. Only the initiator in the secure mode can change the setting of this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SEC	—	—	—	—	—	—	SA[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SM[8:0]								
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SEC	0	R/W	Security Attribute Setting for Descriptor Memory Specifies the security attribute of the address space used for the descriptor memory. 0: Non-secure 1: Secure
30 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	SA[8:0]	H'000	R/W	Security Attribute Setting for Base Address of Descriptor Memory Specify the base address of the descriptor memory to be assigned the security attribute. H'000: H'A000 H'001: H'A004 ... H'1FF: H'A7FC
15 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8 to 0	SM[8:0]	H'000	R/W	Security Attribute Setting for Base Address Mask of Descriptor Memory Specify the security attribute base address mask of the descriptor memory. The range of memory to be assigned the security attribute is specified by this register. See Figure 31.4.

31.3.6 DMA Source Address Registers 0 to 12 (DMASAR_0 to DMASAR_12)

DMASAR is a 32-bit readable/writable register that specifies the source address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next source address.

When the address mode is incrementation, sources in memory only have byte boundaries. For details, refer to Table 31.3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.7 DMA Destination Address Registers 0 to 12 (DMADAR_0 to DMADAR_12)

DMADAR is 32-bit readable/writable register that specify the destination address of a DMA transfer. While a DMA transfer is in progress, this register indicates the next destination address.

When the address mode is incrementation, destinations in memory only have byte boundaries. For details, refer to Table 31.3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DAR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DAR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Table 31.3 SAR/DAR Address Restriction

Resource Selection	Address Mode	Restriction
Auto request	Incrementation	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/DAR, Reception/SAR	All	Boundary corresponding to the DMA transfer size
On-chip peripheral module request Transmission/SAR, Reception/DAR	Incrementation	No restriction (byte boundaries)
	Others	Boundary corresponding to the DMA transfer size

31.3.8 DMA Transfer Count Registers 0 to 12 (DMATCR_0 to DMATCR_12)

DMATCR is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001 and 16,777,215 (the maximum) when the setting is H'00FFFFFF. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in reading.

The eight higher-order bits of DMATCR are always read as 0, and the write value should always be 0.

The value of this register should be set before DMA transfer starting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCR[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.9 DMA Transfer Count Registers B_0 to 12 (DMATCRB_0 to DMATCRB_12)

DMATCRB is a 32-bit readable/writable register that specifies the number of rounds of DMA transfer. The number of rounds of DMA transfer is 1 when the setting is H'00000001 and 16,777,215 (the maximum) when the setting is H'00FFFFFF. During a DMA transfer, this register indicates the remaining number of rounds of transfer.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, the read transfer counter and write transfer counter have different values. This register indicates the counter value used in writing.

The eight higher-order bits of DMATCRB are always read as 0, and the write value should always be 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	TCR[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TCR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.10 DMA Transfer Size Registers 0 to 12 (DMATSR_0 to DMATSR_12)

DMATSR is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967295 bytes when the setting is H'FFFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the read transfer size.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.11 DMA Transfer Size Registers B_0 to 12 (DMATSRB_0 to DMATSRB_12)

DMATSRB is a 32-bit readable/writable register that specifies a total amount of memory to be transferred. The total size of DMA transfer is 1 byte when the setting is H'00000001, 4,294,967295 bytes when the setting is H'FFFFFFFF, and 4,294,967,296 bytes (the maximum) when the setting is H'00000000. During a DMA transfer, this register indicates the remaining amount of memory to be transferred. This register is used in total size transmission.

The audio-DMAC includes independent data buffers for reading and writing. Therefore, reading and writing will have different transfer sizes. This register indicates the value of the write transfer size.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSR[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSR[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.12 DMA Channel Control Registers 0 to 12 (DMACHCR_0 to DMACHCR_12)

DMACHCR is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CAE	CAIE	DPM[1:0]		RPT[2:0]			—	—	DPB	TS[3:2]		DSE	DSIE	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/(W)*	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/(W)*	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DM[1:0]		SM[1:0]		RS[3:0]				—	—	—	TS[1:0]		IE	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/(W)*	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	CAE	0	R/(W)*	Channel Address Error Flag Indicates that an address error interrupt occurred during DMA transfer. This bit is set under the following conditions: The value set in DMASAR or DMADAR does not fall on a boundary corresponding to the transfer size. The source or destination for transfer is in an invalid space. The source or destination for transfer is in module stop mode. If this bit is set, DMA transfer through the channel is not possible even if the DE bit is set to 1. To clear the CAE bit, write 0 to the CAE bit after reading 1 from it or clear the AE bit in DMAOR. Clearing the CAE bit clears the channel address error bits for all channels. 0: An audio-DMAC address error interrupt is not present. (*) [Clearing condition] Writing CAE = 0 after reading CAE = 1 1: An audio-DMAC address error interrupt being generated during DMA transfer.
30	CAIE	0	R/W	Channel Address Error Interrupt Enable Enables or disables the generation of interrupt requests for the CPU when address errors occur. When the CAIE bit is set to 1, if the CAE bit is also set, an interrupt (DEI 0 to 25) from the corresponding channel will be generated for the CPU in response to address errors. Note: An address error interrupt (DADERR) is also asserted simultaneously. See section 11, Interrupt Controller for AP-System Core (INTC-SYS) for more details. 0: Interrupt requests are disabled. 1: Interrupt requests are enabled.
29, 28	DPM[1:0]	00	R/W	Operating Mode of Descriptor Memory Enable or disable the descriptor memory and specify its operating mode. 00: Disabled (normal use) 01: Enabled (normal mode) 10: Enabled (repeat mode) 11: Enabled (read-out interrupt mode, infinite repeat mode)

Bit	Bit Name	Initial Value	R/W	Descriptions
27 to 25	RPT[2:0]	000	R/W	Descriptor Setting Update Specify the parameters to be updated from the descriptor memory. RPT[2]: Enables or disables updating of the source address register RPT[1]: Enables or disables updating of the destination address register RPT[0]: Enables or disables updating of the transfer count register 0: Disabled 1: Enabled
24, 23	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
22	DPB	0	R/W	Descriptor Start Specifies configuration to be loaded when transfer under control of the descriptor memory begins. This bit is cleared after the descriptor memory is read. 0: Processing starts with the values in DMASAR, DMADAR, and DMATCR. 1: Processing starts after the first set of descriptors is read out.
21, 20	TS[3:2]	00	R/W	DMA Transfer Size In combination with TS[1:0], these bits specify the DMA transfer size. When the transfer source or transfer destination is a register of an on-chip peripheral module for which a transfer size is specified, be sure to select the specified transfer size. For the transfer source or destination address specified by DMASAR or DMADAR, an appropriate boundary address should be set according to the transfer data size. Transfer size must be specified to satisfy both source and destination access sizes. For example, the MSIOF must be accessed by 4-byte (TS [3:0] = B'0010) unit only except for SITSCR. TS[3:2] + TS[1:0] (“+” here indicates concatenation, not addition) 0000: Transfer is in byte units. 0001: Transfer is in word (2-byte) units. 0010: Transfer is in longword (4-byte) units. 0011: Transfer is in 16-byte units. 0100: Transfer is in 32-byte units. 0101: Transfer is in 64-byte units. 0111: Transfer is in 8-byte units. Other than above: Setting prohibited
19	DSE	0	R/(W)*	Descriptor Stage End When the DSIE bit is set to 1 and the descriptor memory is enabled, the DSE bit is set to 1 on completion of the DMA transfer. This bit is not set when the DPM bit is set to 0 (descriptors are disabled). (*) To clear the DSE bit, start by reading it as 1, and then write 0 to the bit. 0: DMA transfer is still running or has been aborted. 1: Transfer under the control of one stage of the descriptor memory has been completed.

Bit	Bit Name	Initial Value	R/W	Descriptions
18	DSIE	0	R/W	Descriptor Stage End Interrupt Enable Specifies whether an interrupt request is generated for the CPU on completion of transfer under the control of one stage of the descriptor memory. When this bit is set to 1, an interrupt (DEI) is generated for the CPU whenever the DSE is set to 1. 0: Interrupt requests are disabled. 1: Interrupt requests are enabled.
17, 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15, 14	DM[1:0]	00	R/W	Destination Address Mode Specify whether the DMA destination address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment. 00: Destination address is fixed. 01: Destination addresses are incremented. + 1 when transfer is in byte units. + 2 when transfer is in word units. + 4 when transfer is in longword units. + 8 when transfer is in 8-byte units. + 16 when transfer is in 16-byte units. + 32 when transfer is in 32-byte units. + 64 when transfer is in 64-byte units. 10: Destination addresses are decremented. – 1 when transfer is in byte units. – 2 when transfer is in word units. – 4 when transfer is in longword units. Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units. 11: Setting Prohibited
13, 12	SM[1:0]	00	R/W	Source Address Mode Specify whether the DMA source address is incremented, fixed, or decremented. The unit of transfer (transfer size) determines the size of the increment. 00: Source address is fixed. 01: Source addresses are incremented. + 1 when transfer is in byte units. + 2 when transfer is in word units. + 4 when transfer is in longword units. + 8 when transfer is in 8-byte units. + 16 when transfer is in 16-byte units. + 32 when transfer is in 32-byte units. + 64 when transfer is in 64-byte units. 10: Source addresses are decremented. – 1 when transfer is in byte units. – 2 when transfer is in word units. – 4 when transfer is in longword units. Setting prohibited when transfer is in 8-, 16-, 32-, or 64-byte units. 11: Setting Prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
11 to 8	RS[3:0]	0000	R/W	Resource Selection Specify the source of transfer requests. Only change the transfer request source while the DMA enable bit (DE) is set to 0. 0100: Auto request 1000: Source is selected by the DMA extended resource selector. Other than above: Settings prohibited
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4, 3	TS[1:0]	00	R/W	DMA Transfer Size See the description of TS[3:2] (bits 21 and 20).
2	IE	0	R/W	Interrupt Enable Specifies whether or not an interrupt request is generated for the CPU on completion of DMA transfer. When this bit is set to 1, an interrupt request (DEI) for the CPU is generated whenever the TE bit is set to 1. 0: Interrupt request is disabled. 1: Interrupt request is enabled.
1	TE	0	R/(W)*	Transfer End Flag When the descriptor memory is not in use, the TE bit is set to 1 when DMATCR and DMATSR become 0 on completion of the DMA transfer. When the descriptor memory is in use, the TE bit is set to 1 on completion of all transfers set up in the descriptor memory. The TE bit is not set to 1 in the following cases. • DMA transfer ends due to a DMA address error before DMATCR and DMATSR become 0. • DMA transfer is aborted by clearing the DE and DME bits in DMAOR. To clear the TE bit, start by reading it as 1, and then write 0 to it. When the TE bit is set to 1, transfer is not possible even if the DE bit is set to 1. 0: DMA transfer is in progress or was aborted (*) [Clearing condition] Writing of 0 after reading of 1 1: DMA transfer ended on the specified count (TCR = 0 and TSR = 0)
0	DE	0	R/W	DMA Enable Enables or disables DMA transfer. In the auto request mode, a DMA transfer is started by setting the DE and DME bits in DMAOR to 1. At this time, the setting of both the AE and TE bits in DMAOR must be 0. In a peripheral module request, a DMA transfer starts if the transfer request is generated by the selected device or on-chip peripheral module after setting the DE and DME bits to 1. In this case too, the settings of both the TE and AE bits must be 0. Clearing the DE bit to 0 aborts all DMA transfer. Note: Ensure that the setting of the DE bit is actually 0 after clearing it. 0: DMA transfer is disabled. 1: DMA transfer is enabled.

Note: * Writing 0 is possible to clear the flag.

31.3.13 DMA Channel Control Register B_0 to 12 (DMACHCRB_0 to DMACHCRB_12)

DMACHCRB is a 32-bit readable/writable register that controls the DMA transfer mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DCNT[7:0]								DPTR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRST	—	—	—	—	—	—	DTS	SLM[3:0]				PRI[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DCNT[7:0]	H'00	R/W	Number of Stages of Descriptor Memory Specify the number of stages of the descriptor memory as DCNT + 1. When the descriptor memory is enabled, a transfer end (TE) interrupt is only generated for the CPU on completion of transfer under control of the specified number of stages.
23 to 16	DPTR[7:0]	H'00	R	Descriptor Pointer This bit indicates the pointer to the next descriptor to be read. It is cleared to 0 when the last descriptor of the number of stages specified by DCNT[7:0] is read. It is also cleared to 0 when 1 is written to DRST.
15	DRST	0	W	Descriptor Reset Resets the descriptor pointer. Before the descriptor memory is used, the pointer must be reset by writing 1 to this bit. This bit is always read as 0.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	DTS	0	R/W	Total Size Transmission under Descriptor Control This bit is only effective when total size transmission is selected. 0: The TCR fields of the descriptors are used as transfer count settings. 1: The TCR fields of the descriptors are used as total size settings.
7 to 4	SLM[3:0]	0000	R/W	DMA Transfer Low-Speed Mode Specify the number of cycles of the clock (ZSϕ) for the DMA transfer. One round of DMA transfer is executed in the number of cycles of the clock specified by this bit. 0000: Normal mode 1000: On round in 256 cycles of the clock. 1001: On round in 512 cycles of the clock. 1010: On round in 1024 cycles of the clock. : 1111: On round in 32768 cycles of the clock. Other than above: Setting prohibited

Bit	Bit Name	Initial Value	R/W	Descriptions
3 to 0	PRI[3:0]	0000	R/W	Channel Request Priority Setting These bits set the priority of requests for transfer on the given channel. 1111: Highest priority : 0111 to 0000: Lowest priority

31.3.14 DMA Buffer Control Registers 0 to 12 (DMABUFCR_0 to DMABUFCR_12)

DMABUFCR is a 32-bit readable/writable register that controls the upper limit on buffer size in and burst unit for the SDRAM.

Use this register when the upper limit on buffering requires control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	MBU[8:0]								
Initial value:	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ULB[9:0]									
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24 to 16	MBU[8:0]	H'080	R/W	Maximum Burst Unit for SDRAM This register is only effective for SDRAM access, and everything other than that is under control of the transfer size (unit). Settings bigger than UBL are prohibited. Power-of-two settings are recommended. Maximum value is 256 (bytes).
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9 to 0	ULB[9:0]	H'100	R/W	Upper Limit on Buffer Size This register controls the upper limit value for buffering. Power-of-two settings are recommended. Maximum value is 512 (bytes).

31.3.15 DMA Extended Resource Selectors 0 to 12 (DMARS_0 to DMARS_12)

DMARS is a 16-bit readable/writable register that specifies the on-chip peripheral module to be the source of the DMA transfer request for the given channel. DMARS_0 specifies the source for channel 0, DMARS_1 specifies the source for channel 1 and so on.

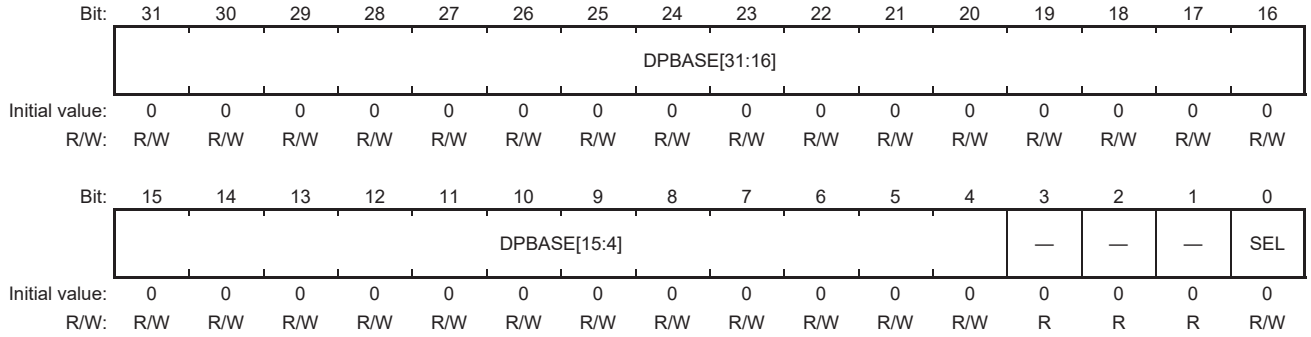
When bits MID and RID are set to a value other than the values listed in Table 31.4, the operation of this LSI is not guaranteed. Transfer requests from the source selected in DMARS are only valid when the resource selection bits (RS[3:0]) in DMACHCR have been set to B'1000. Otherwise, even if DMARS has been set, requests from the corresponding transfer request source are not accepted.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MID[5:0]						RID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 8	—	—	R	Reserved These bits are always read as 0. The write value should always be 0.
7 to 2	MID[5:0]	000000	R/W	DMA Request Source Adoption ID5 to ID0 (MID) See Table 31.4.
1, 0	RID[1:0]	00	R/W	DMA Request Source Adoption ID1 and ID0 (RID) See Table 31.4.

31.3.16 DMA Descriptor Base Address Registers 0 to 12 (DMADPBASE_0 to DMADPBASE_12)

DMADPBASE specifies the base address of the descriptor memory. The address range of the descriptor memory is specified by setting this register.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 4	DPBASE[31:4]	All 0	R/W	Base Address of Descriptor Memory Place each stage of the descriptor memory on a 16-byte boundary. Setting example: When Built-in memory is used, [Audio-DMAC]: H'EC70 A00 to H'EC70 A7F When External memory is used, Other memory area on a 16-byte boundary
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SEL	0	R/W	Descriptor Memory Selection Selects the memory to be used as descriptor memory. 0: Setting Prohibited 1: Built-in memory or External memory is used.

31.3.17 DMA Descriptor Control Registers 0 to 12 (DMADPCR_0 to DMADPCR_12)

DMADPCR is a 32-bit readable/writable register that controls the timing with which interrupts are output in read-out interrupt mode (descriptor mode 3).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DIPT[7:0]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	DIPT[7:0]	H'00	R/W	Descriptor Read-out Interrupt Pointer The number of stages for which descriptor read-out interrupts are generated in descriptor mode 3. DIPT + 1 specifies the number of descriptor stages.
23 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

31.3.18 DMA Fixed Source Address Registers 0 to 12 (DMAFIXSAR_0 to DMAFIXSAR_12)

DMAFIXSAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit source address for a DMA transfer.

This register is not incremented by carrying when DMASAR overflows.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SAR[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.19 DMA Fixed Destination Address Registers 0 to 12 (DMAFIXDAR_0 to DMAFIXDAR_12)

DMAFIXDAR is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit destination address for a DMA transfer.

This register is not incremented by carrying when DMADAR overflows.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DAR[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.20 DMA Fixed Descriptor Base Address Registers 0 to 12 (DMAFIXDPBASE_0 to DMAFIXDPBASE_12)

DMAFIXDPBASE is a 32-bit readable/writable register that specifies the most significant 8 bits of the 40-bit descriptor base address for a DMA transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	DPBASE[39:32]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

31.3.21 Descriptor Memory (DescriptorMEM)

See section 31.4.4, Descriptor Memory for the descriptor memory.

31.4 Operation

When there is a DMA transfer request, the DMAC starts the transfer according to the predetermined channel priority; when the transfer end conditions are satisfied, it ends the transfer. Transfers can be requested in two modes: auto request and on-chip peripheral module request. The bus mode can be selected from normal speed mode and slow speed mode).

31.4.1 DMA Transfer Requests

Most commonly, DMA transfer requests are generated by either the source or destination for transfer, but they can also be generated by on-chip peripheral modules that are neither the source nor the destination. Transfers can be requested in two modes: auto request, and on-chip peripheral module request. The request mode is selected for each channel by DMARS.

(1) Auto-Request Mode

When there is no transfer request signal from an external source, as in a memory-to-memory transfer or a transfer between memory and an on-chip peripheral module unable to request a transfer, auto-request mode allows the audio-DMAC to automatically generate a transfer request signal internally. When the DE bit in DMACHCR and the DME bit in DMAOR are set to 1 for the target channel, the transfer begins so long as the CAE bit in DMACHCR is 0.

(2) On-Chip Peripheral Module Request Mode

In this mode, a transfer is performed at the transfer request signal of an on-chip peripheral module. The source (on-chip peripheral module) of the DMA transfer request is specified by DMARS.

When this mode is selected, if the DMA transfer is enabled (DE = 1, DME = 1, TE = 0, CAE = 0), a transfer is performed upon the input of a transfer request signal.

When a transmit data empty transfer request of the SCIF is set as the transfer request, the transfer destination must be the SCIF's transmit data register. Likewise, when receive data full transfer request of the SCIF is set as the transfer request, the transfer source must be the SCIF's receive data register. These conditions also apply to the other on-chip peripheral modules.

The number of the receive FIFO triggers can be set as a transfer request depending on an on-chip peripheral module. Data needs to be read after the DMA transfer is ended, because data may be left in the receive FIFO when the receive FIFO trigger condition is not satisfied.

Table 31.4 Selecting On-Chip Peripheral Module Request Modes

DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination
H'87	SCU1	Transmit	Arbitrary	
H'89	SCU2	Transmit	Arbitrary	
H'8B	SCU3	Transmit	Arbitrary	
H'8D	SCU4	Transmit	Arbitrary	
H'8F	SCU5	Transmit	Arbitrary	
H'91	SCU6	Transmit	Arbitrary	
H'BC	SCUCMD0	Receive		Arbitrary
H'BE	SCUCMD1	Receive		Arbitrary
H'9C	SCUOUT1	Receive		Arbitrary
H'9E	SCUOUT2	Receive		Arbitrary
H'A0	SCUOUT3	Receive		Arbitrary
H'B0	SCUOUT4	Receive		Arbitrary
H'B2	SCUOUT5	Receive		Arbitrary
H'B4	SCUOUT6	Receive		Arbitrary
H'15	SSI0_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip00
H'16	SSI0_0 receiver	RXI (Receive data request)	ssip00	Arbitrary
H'35	SSI0_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip01
H'36	SSI0_1 receiver	RXI (Receive data request)	ssip01	Arbitrary
H'37	SSI0_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip02
H'38	SSI0_2 receiver	RXI (Receive data request)	ssip02	Arbitrary
H'47	SSI0_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip03
H'48	SSI0_3 receiver	RXI (Receive data request)	ssip03	Arbitrary
H'49	SSI1_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip10
H'4A	SSI1_0 receiver	RXI (Receive data request)	ssip10	Arbitrary
H'4B	SSI1_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip11
H'4C	SSI1_1 receiver	RXI (Receive data request)	ssip11	Arbitrary
H'57	SSI1_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip12
H'58	SSI1_2 receiver	RXI (Receive data request)	ssip12	Arbitrary
H'59	SSI1_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip13
H'5A	SSI1_3 receiver	RXI (Receive data request)	ssip13	Arbitrary
H'63	SSI2_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip20
H'64	SSI2_0 receiver	RXI (Receive data request)	ssip20	Arbitrary
H'67	SSI2_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip21
H'68	SSI2_1 receiver	RXI (Receive data request)	ssip21	Arbitrary
H'6B	SSI2_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip22
H'6C	SSI2_2 receiver	RXI (Receive data request)	ssip22	Arbitrary
H'6D	SSI2_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip23
H'6E	SSI2_3 receiver	RXI (Receive data request)	ssip23	Arbitrary
H'6F	SSI3 transmitter	TXI (Transmit data request)	Arbitrary	ssip3
H'70	SSI3 receiver	RXI (Receive data request)	ssip3	Arbitrary
H'71	SSI4 transmitter	TXI (Transmit data request)	Arbitrary	ssip4

DMARS MID + RID	DMA Transfer Request Source	DMA Transfer Request Signal	Source	Destination
H'72	SSI4 receiver	RXI (Receive data request)	ssip4	Arbitrary
H'73	SSI5 transmitter	TXI (Transmit data request)	Arbitrary	ssip5
H'74	SSI5 receiver	RXI (Receive data request)	ssip5	Arbitrary
H'75	SSI6 transmitter	TXI (Transmit data request)	Arbitrary	ssip6
H'76	SSI6 receiver	RXI (Receive data request)	ssip6	Arbitrary
H'79	SSI7 transmitter	TXI (Transmit data request)	Arbitrary	ssip7
H'7A	SSI7 receiver	RXI (Receive data request)	ssip7	Arbitrary
H'7B	SSI8 transmitter	TXI (Transmit data request)	Arbitrary	ssip8
H'7C	SSI8 receiver	RXI (Receive data request)	ssip8	Arbitrary
H'7D	SSI9_0 transmitter	TXI (Transmit data request)	Arbitrary	ssip90
H'7E	SSI9_0 receiver	RXI (Receive data request)	ssip90	Arbitrary
H'7F	SSI9_1 transmitter	TXI (Transmit data request)	Arbitrary	ssip91
H'80	SSI9_1 receiver	RXI (Receive data request)	ssip91	Arbitrary
H'81	SSI9_2 transmitter	TXI (Transmit data request)	Arbitrary	ssip92
H'82	SSI9_2 receiver	RXI (Receive data request)	ssip92	Arbitrary
H'83	SSI9_3 transmitter	TXI (Transmit data request)	Arbitrary	ssip93
H'84	SSI9_3 receiver	RXI (Receive data request)	ssip93	Arbitrary
H'01	SSIND0 transmitter	TXI (Transmit data request)	Arbitrary	ssindd0
H'02	SSIND0 receiver	RXI (Receive data request)	ssindd0	Arbitrary
H'03	SSIND1 transmitter	TXI (Transmit data request)	Arbitrary	ssindd1
H'04	SSIND1 receiver	RXI (Receive data request)	ssindd1	Arbitrary
H'05	SSIND2 transmitter	TXI (Transmit data request)	Arbitrary	ssindd2
H'06	SSIND2 receiver	RXI (Receive data request)	ssindd2	Arbitrary
H'07	SSIND3 transmitter	TXI (Transmit data request)	Arbitrary	ssindd3
H'08	SSIND3 receiver	RXI (Receive data request)	ssindd3	Arbitrary
H'09	SSIND4 transmitter	TXI (Transmit data request)	Arbitrary	ssindd4
H'0A	SSIND4 receiver	RXI (Receive data request)	ssindd4	Arbitrary
H'0B	SSIND5 transmitter	TXI (Transmit data request)	Arbitrary	ssindd5
H'0C	SSIND5 receiver	RXI (Receive data request)	ssindd5	Arbitrary
H'0D	SSIND6 transmitter	TXI (Transmit data request)	Arbitrary	ssindd6
H'0E	SSIND6 receiver	RXI (Receive data request)	ssindd6	Arbitrary
H'0F	SSIND7 transmitter	TXI (Transmit data request)	Arbitrary	ssindd7
H'10	SSIND7 receiver	RXI (Receive data request)	ssindd7	Arbitrary
H'11	SSIND8 transmitter	TXI (Transmit data request)	Arbitrary	ssindd8
H'12	SSIND8 receiver	RXI (Receive data request)	ssindd8	Arbitrary
H'13	SSIND9 transmitter	TXI (Transmit data request)	Arbitrary	ssindd9
H'14	SSIND9 receiver	RXI (Receive data request)	ssindd9	Arbitrary

Table 31.5 Data Length of DMA Transfer for Each of the On-Chip Peripheral Modules

Module	1 Byte	2 Bytes	4 Bytes	8 Bytes	16 Bytes	32 Bytes
SCU1/SCU2/SCU3/ SCU4/SCU5/SCU6			✓			
SCUCMD0/SCUCMD1			✓			
SCUOUT1/SCUOUT2/ SCUOUT3/SCUOUT4/ SCUOUT5/SCUOUT6			✓			
SSI0_0/SSI0_1/SSI0_2/ SSI0_3/SSI1_0/SSI1_1/ SSI1_2/SSI1_3/SSI2_0/ SSI2_1/SSI2_2/SSI2_3/ SSI3/SSI4/SSI5/SSI6/ SSI7/SSI8/SSI9_0/ SSI9_1/SSI9_2/SSI9_3			✓			
SSIND0/1/2/3/4/5/6/7/8/9			✓			

31.4.2 Channel Priority

When the audio-DMAC receives simultaneous transfer requests on two or more channels, it transfers data according to a predetermined priority. Two modes (fixed mode and round-robin mode) are selected by the PR[1:0] bits in DMAOR.

(a) Fixed Mode

In this mode, the priority levels among the channels remain fixed.

CH0 > CH1 > ... > CH11 > CH12

(b) Round-Robin Mode

In round-robin mode, each time data of one transfer unit (byte, word, longword, 8-byte or 16-byte units) is transferred on one channel, the priority is rotated. The channel on which the transfer was just finished rotates to the bottom of the priority. The priority of round-robin mode is CH0 > CH1 > ... >CH11 > CH12 immediately after reset.

31.4.3 Slow Speed Mode

In the low-speed mode, a single round of DMA transfer is performed every time the number of clock cycles specified by the SLM bits in DMACHCRB elapse. This mode can be selected per DMA channel. Transfer on other channels can proceed after each round of transfer for a channel in the low-speed mode is completed.

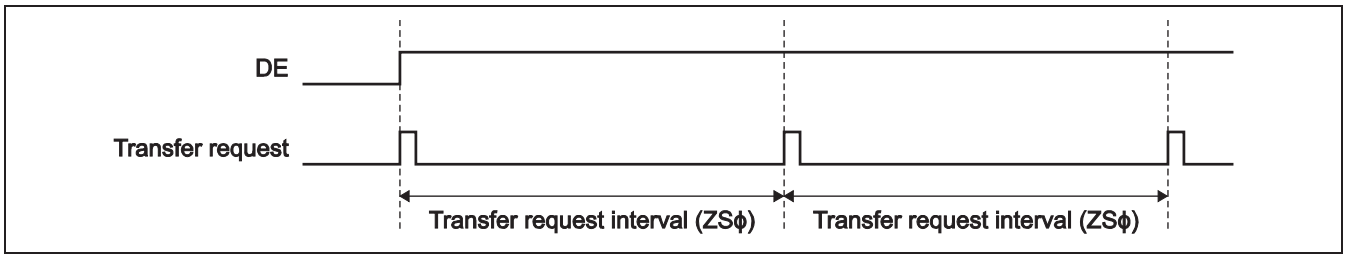


Figure 31.2 Slow Speed Mode

31.4.4 Descriptor Memory

The descriptor memory function is selected by setting the DPM[1:0] bits in DMACHCR to B'01, B'10, or B'11. When DMATCR is set to 0 and the DMA transfer is completed, the next set of settings is read, and if only a single channel is enabled, the contents defined by up to 128 stages of descriptor memory can be consecutively transferred when the built-in descriptor memory is used. External memory can also be used as the descriptor memory. In that case, the contents defined by up to 256 stages of descriptor memory can be transferred.

The following initial settings are required to use the descriptor memory.

- Set the base address of the descriptor memory for the DMA transfer in DMADPBASE.
- Set the DRST bit in DMACHCRB to reset the descriptor memory.
- Set the number of stages of the descriptor memory in the DCNT bits of DMACHCRB.

The descriptor memory is shared between all channels. Ensure that the areas of descriptor memory for use by each of the channels do not overlap. It is necessary to arrange each stage of the descriptor memory on a 16-byte boundary.

There are two methods to activate the descriptor memory as follows.

- Specify the first DMA transfer settings in DMASAR, DMADAR, and DMATCR, and specify the subsequent settings in the descriptor memory. Then, set the DPB bit in DMACHCR to 0 to activate the descriptor memory. In this case, after completion of the transfer specified in DMASAR, DMADAR, and DMATCR, transfer continues after new settings are read from the descriptor memory. Note, however, that, when the operating mode of the descriptor memory is set to the repeat mode, the values specified in DMASAR, DMADAR, and DMATCR are not read, and the transfer starts and is repeated from the head of the descriptor memory.
- Write the DMA transfer settings to the descriptor memory, and write 1 to the DPB bit in DMACHCR to activate the descriptor memory. In this case, the DMA transfer starts from the first settings in the descriptor memory.

There are three operating modes of the descriptor memory, which can be selected by setting the DPM bits in DMACHCR.

For details on these operating modes, see the descriptions of each operating mode in this section.

(1) Configuration of Descriptor Memory

Figure 31.3 shows the configuration of the built-in descriptor memory.

The capacity of the built-in descriptor memory is 16 bytes per stage × 128 stages.

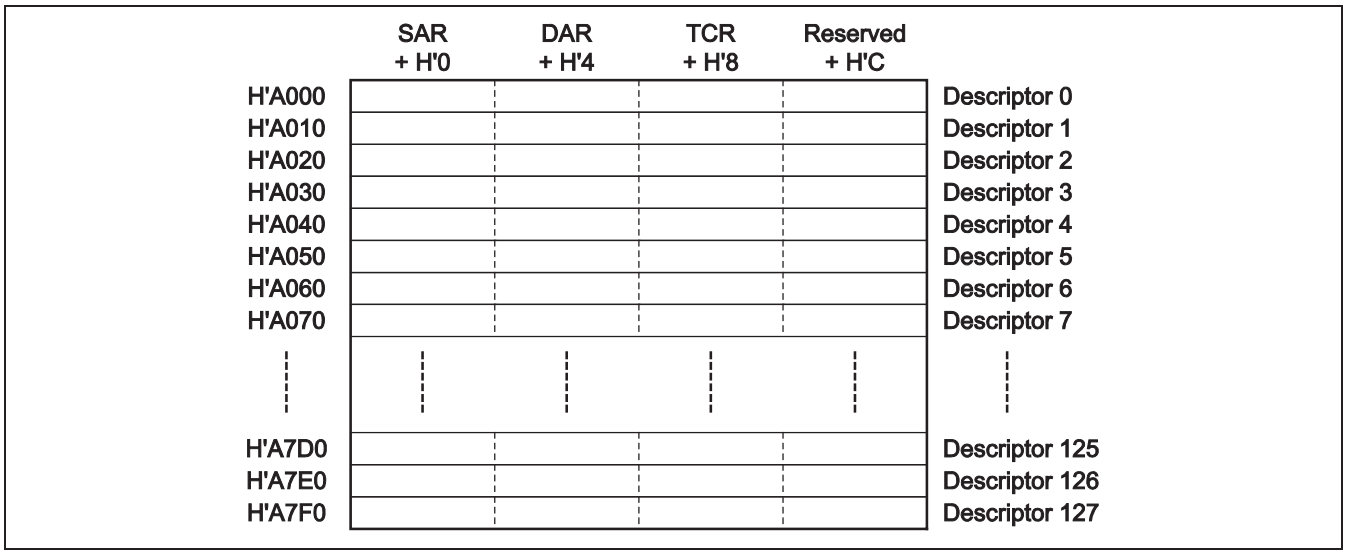


Figure 31.3 Configuration of Built-in Descriptor Memory

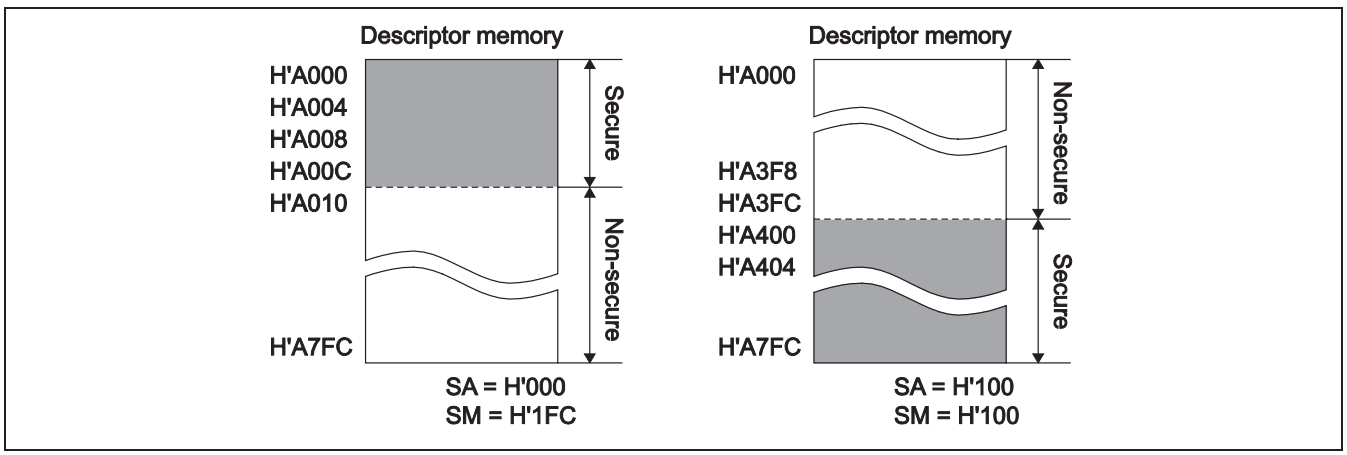


Figure 31.4 Example of DMADPSEC Setting

(2) Flow of Updating from Descriptor Memory

The RPT bits in DMACHCR can be used to specify which registers are to be updated from the descriptor memory.

The DPTR bits in DMACHCRB are incremented when updating from the descriptor memory is completed. If the DPTR value matches the DCNT value, the DPTR value is reset to 0.

This flow is automatically processed by hardware.

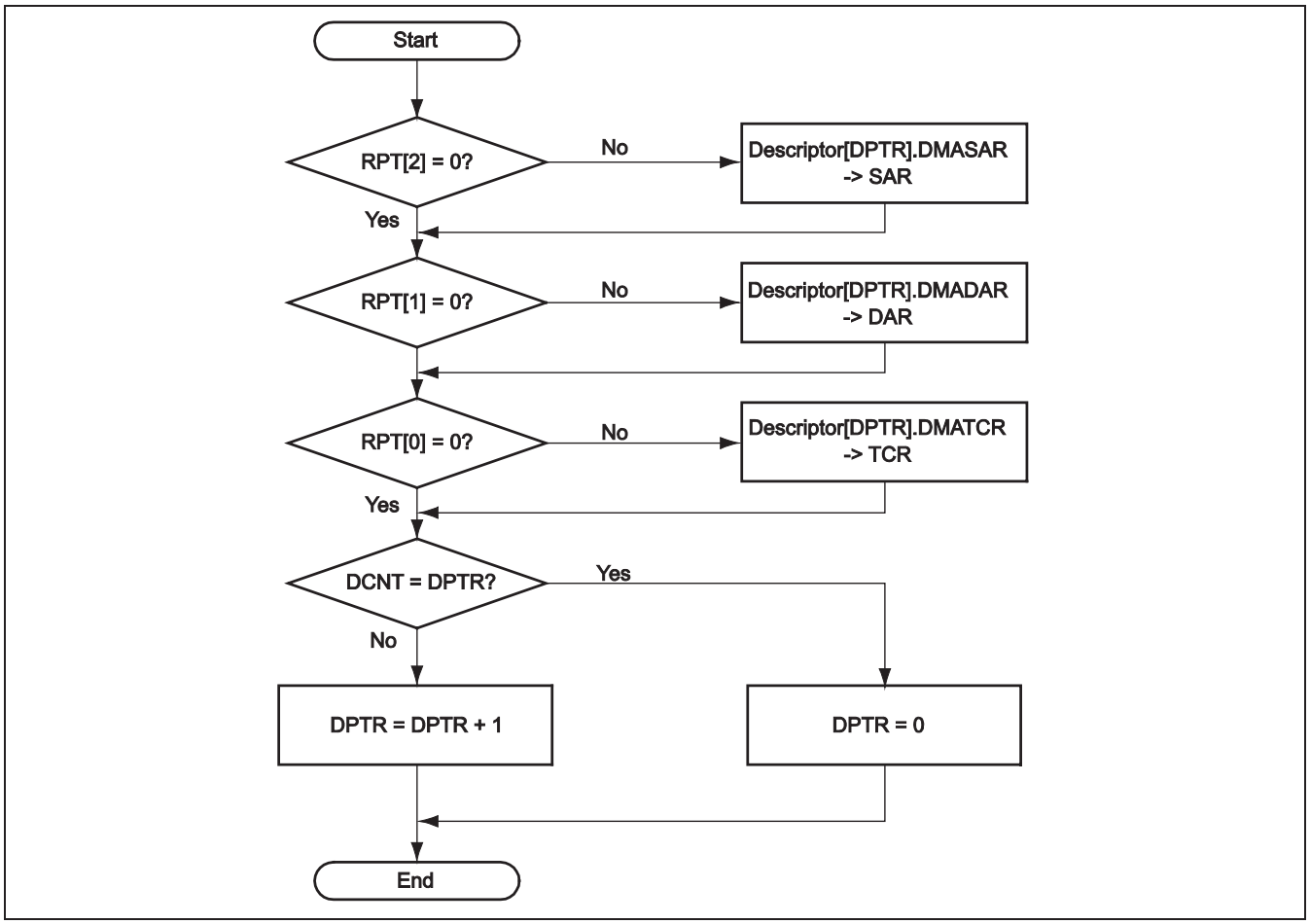


Figure 31.5 Flow of Updating from Descriptor Memory

(3) Operating Mode 1 of Descriptor Memory

Set the DPM bits in DMACHCR to B'01 to select operating mode 1 (normal mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, the DMA transfer is complete when the TE bit in DMACHCR is set to 1 after transfer under control of the number of stages of the descriptor memory specified in the DCNT bits in DMACHCRB.

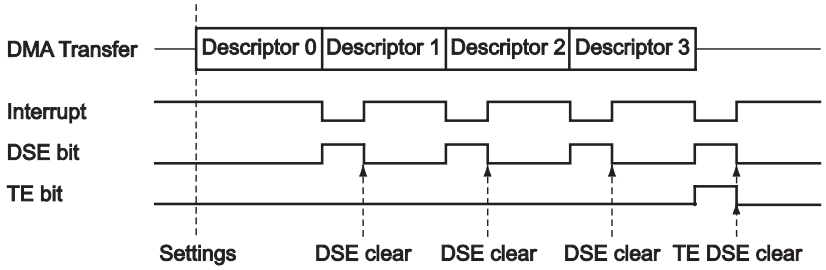
When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

Figure 31.6 is an example of transfer when operating mode 1 is selected and the TE and DSE bits are set to 1.

Figure 31.7 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 1 is selected and the TE and DSE bits are set to 1.

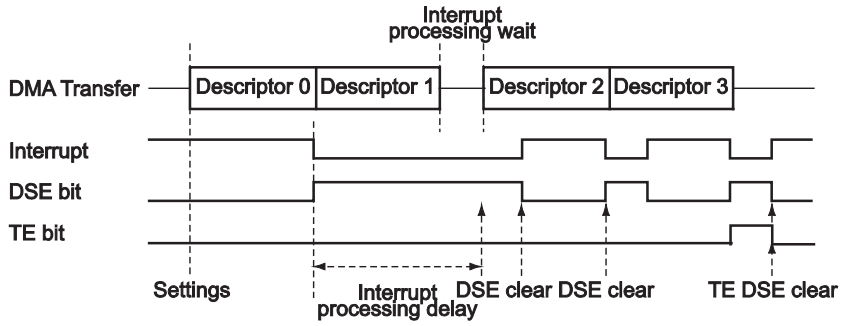
Figure 31.8 is an example of transfer when operating mode 1 is selected and the TE bit is set to 1.

In each example, there are four descriptor stages.



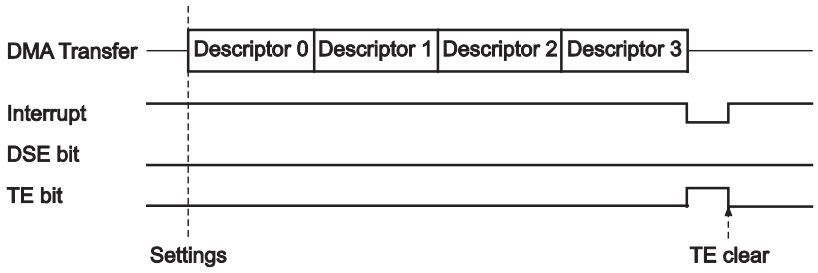
Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 31.6 Operating Mode 1 (Example 1)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 31.7 Operating Mode 1 (Example 2)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'1).

Figure 31.8 Operating Mode 1 (Example 3)

(4) Operating Mode 2 of Descriptor Memory

Set the DPM bits in DMACHCR to B'10 to select operating mode 2 (repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. If a first DSE interrupt has not been processed when a further DSE interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the DSE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

When the DSIE bit in DMACHCR is set to 0, after transfer under control of all stages of the descriptor memory is complete, the TE bit in DMACHCR is set to 1 and a TE interrupt is generated. If a TE interrupt has not been processed when a further interrupt is generated, the contents of the next stage of the descriptor memory are not read and the DMA transfer is aborted. Clearing the TE bit only causes clearing of the first interrupt and reading of the next stage of the descriptor memory.

To end operation in mode 2, change the mode to mode 1 by using the TE interrupt processing. When the mode is changed to mode 1, the DMA transfer is completed when the next TE interrupt is generated.

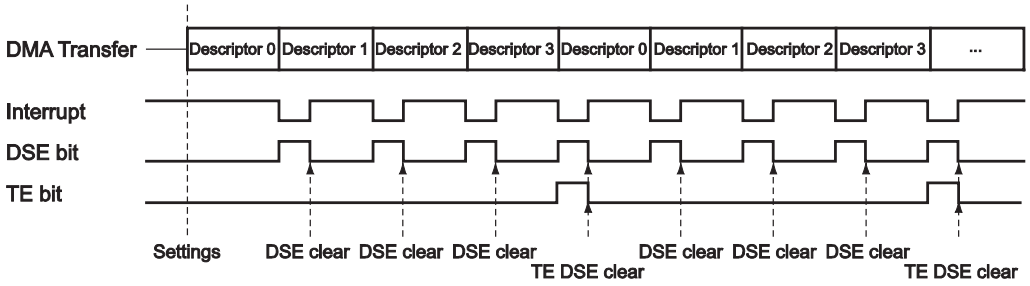
Figure 31.9 is an example of transfer when operating mode 2 is selected and the TE and DSE bits are set to 1.

Figure 31.10 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE and DSE bits are set to 1.

Figure 31.11 is an example of transfer when operating mode 2 is selected and the TE bit is set to 1.

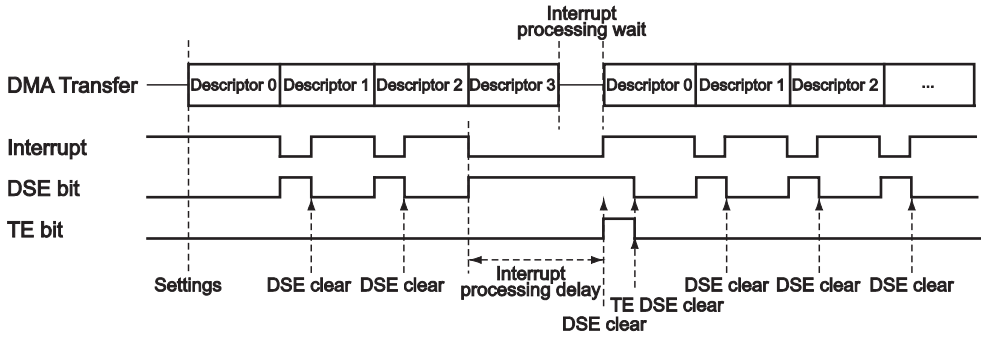
Figure 31.12 is an example of transfer when there is a delay in processing of the DSE interrupt when operating mode 2 is selected and the TE is set to 1.

In each example, there are four descriptor stages.



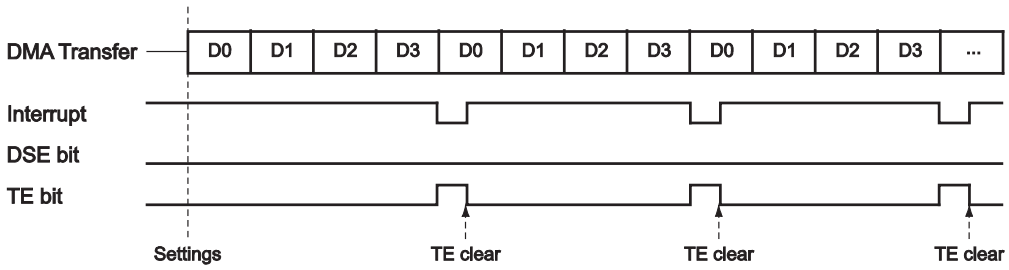
Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'01, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 31.9 Operating Mode 2 (Example 1)



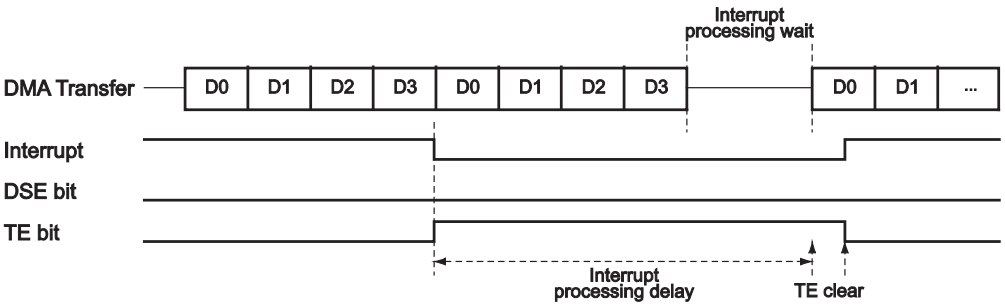
Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'1).

Figure 31.10 Operating Mode 2 (Example 2)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'1).

Figure 31.11 Operating Mode 2 (Example 3)



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'1).

Figure 31.12 Operating Mode 2 (Example 4)

(5) Operating Mode 3 of Descriptor Memory

Set the DPM bits in DMACHCR to B'11 to select operating mode 3 (infinite repeat mode). This mode allows consecutive transfer under control of the descriptor memory.

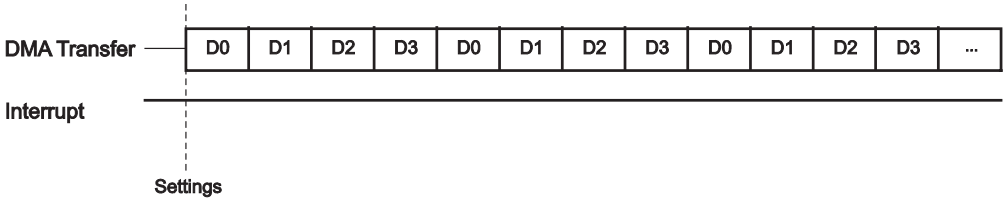
In this mode, after transfer under control of the number of stages of descriptor memory specified in the DCNT bits in DMACHCRB, the TE bit in DMACHCR is set to 1. This operation is then repeated from the head of the descriptor memory.

When the DSIE bit in DMACHCR is set to 1, a DSE interrupt is generated every time transfer under the control of one stage of descriptor memory is complete. Even if a first DSE interrupt has not been processed when a further DSE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of DSE interrupts that have been generated, the DSE bit can be cleared by writing to it once. Similarly, even if a first TE interrupt has not been processed when a further TE interrupt is generated, the DMA transfer is not aborted. Regardless of the number of TE interrupts that have been generated, the TE bit can be cleared by writing to it once.

Figure 31.13 is an example of transfer when infinite repeat mode is selected.

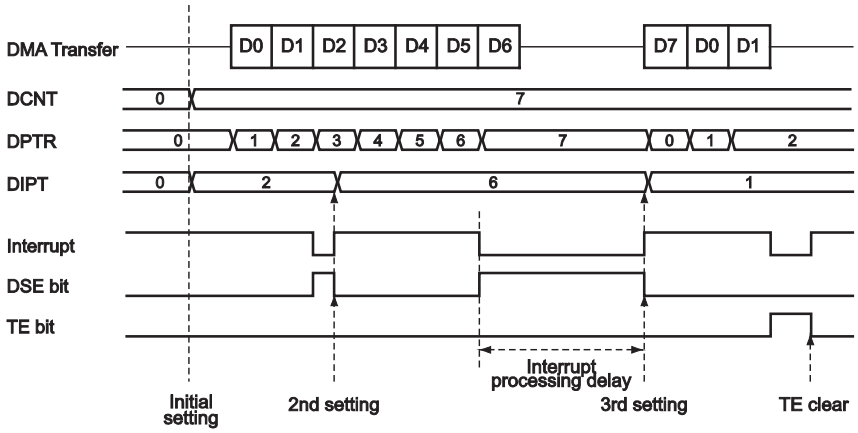
Figure 31.14 is an example of transfer when read-out interrupt mode is selected.

In each example, there are four descriptor stages.



Settings: 1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMACHCRB register (DCNT = 3).
3. Set the DMACHCR register (DPM = B'11, DRST = B'1, DB = B'1, DSIE = B'0, IE = B'0).

Figure 31.13 Operating Mode 3 (Infinite Repeat Mode)



Initial setting:
1. Set the DMACHCRB register (DCNT = 7).
2. The descriptor has three setting (DMASAR, DMADAR, DMATCR) stages.
3. Set the DMADPCR register (DIPT = 2).
4. Set the DMACHCR register (DPM = B'11, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'0).

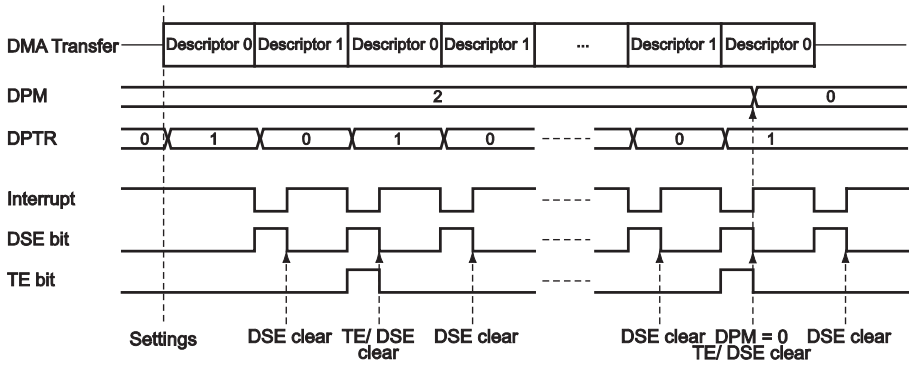
2nd setting:
1. The descriptor has four setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMADPCR register (DIPT = 6).
   (3 stages + 4 stages -1) mod 8 = 6
3. Clear DSE.

3rd setting: (Transfer end)
1. The descriptor has three setting (DMASAR, DMADAR, DMATCR) stages.
2. Set the DMADPCR register (DIPT =1).
   (3 stages + 4 stages + 3 stages -1) mod 8 = 1
3. Clear the DSE bit and set the DMACHCR register (DPM = B'11, DB = B'0, DSIE = B'0, IE = B'1).

Figure 31.14 Operating Mode 3 (Read-Out Interrupt Mode)

(6) Using the Descriptor Memory for Double Buffering

To use the descriptor memory for double buffering, set the number of stages of descriptor memory to 2, set the buffer configuration to the descriptor memory, and activate the memory in operating mode 2. The DSE interrupt is used in double buffering. To end the use of double buffering, disable the descriptor operating mode, which stops the transfer on completion of the transfer currently in progress.



Settings: 1. The descriptor has two setting (buffer A, buffer B) stages.
2. Set the DMACHCRB register (DCNT = 1).
3. Set the DMACHCR register (DPM = B'10, DRST = B'1, DB = B'1, DSIE = B'1, IE = B'0).

Figure 31.15 Using the Descriptor Memory for Double Buffering

31.4.5 Transmission Flow

Set the transfer conditions as required in the following registers:

DMA source address register (DMASAR), DMA destination address register (DMADAR), DMA transfer count register (DMATCR), DMA Channel control register (DMACHCR), DMA operation register (DMAOR) and DMA extended resource selector (DMARS)

The DMAC then transmits data in the following order.

- A transfer request is generated and the controller checks whether the transfer is allowed (DE = 1, DME = 1, TE = 0, DSE = 0, CAE = 0). When a channel is in the auto request mode, the transfer starts automatically.
- The controller checks whether updating from the descriptor memory is required.
  Updating from the descriptor memory proceeds when the DPB bit in DMACHCR is set to 1 or the descriptor memory is enabled, if DMATCR is set to 0.
  For updating by using the descriptor memory, see section 31.4.4, Descriptor Memory.
- Check whether address translation by the IPMMU is required.
  Address translation by the IPMMU proceeds if the address exceeds the effective size for address translation when the DE bit in DMACHCR is enabled and updating of transfer settings from the descriptor memory is executed.
- Each time a transfer request is generated, the amount of data for a single round of transfer (specified by the TS[3:0] bits) is transmitted. The value in DMATCR is decremented by 1 every time the DMA transfer is completed.
- When the specified number of rounds of transfer are completed (the value in DMATCR is set to 0), the transfer ends normally. A TE interrupt is generated for the CPU upon the end of the transfer if the IE bit in DMACHCR is set to 1. If the descriptor memory is enabled, the processing differs with the mode of the descriptor memory. For more details, see section 31.4.4, Descriptor Memory.
- Transfer is aborted when the DMAC encounters an address error. Transfer is also aborted when the DE bit in DMACHCR or the DME bit in DMAOR is set to 0.

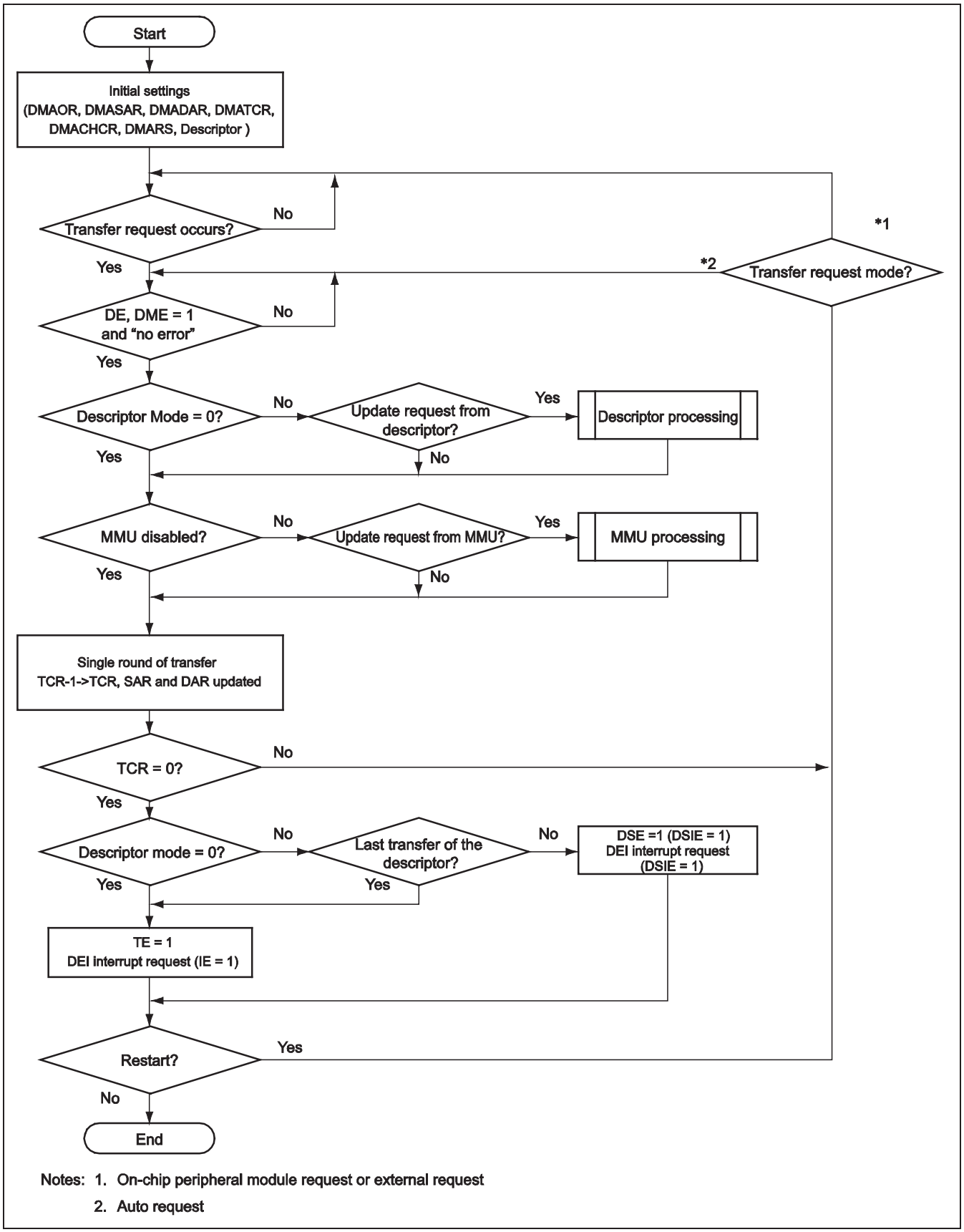


Figure 31.16 Transmission Flow

31.4.6 Total Size Transmission

The amount of data for total size transmission can be set in DMATSR (in bytes), and this setting is effective regardless of the size specified in the TS bits in DMACHCR. Thereby, the desired size can be transmitted in a single round of DMA transfer.

To use this function, make the settings for total size transmission in DMASAR, DMADAR, DMATSR, DMATSRB and DMACHCR.

Total size is set in the TCR (TSR) field of descriptors and 1 is set in DMACHCRB.DTS when total size transmission and descriptors are in use.

31.5 Usage Notes

Pay attention to the following notes when using the audio-DMAC.

(1) DMA Transfer for Peripheral Modules

When executing DMA transfer for an on-chip peripheral module, set addresses on the appropriate boundary (in terms of the amount of data for each round of transfer) for the transfer source and destination addresses. Otherwise, an address error may occur.

(2) Module Stop

While the audio-DMAC is operating, the module stop register (MSTPCR5) should not be set to stop the audio-DMAC. If the audio-DMAC is stopped in this way, results of the transfer that was in progress cannot be guaranteed.

(3) Address Error

When a DMA address error is generated, reset the registers of the channel on which the error has occurred and then start transfer anew.

(4) Aborting DMA Transfer

To abort a DMA transfer, disable the interrupt signal and set the DE bit in the DMA channel control register (DMACHCR) to 0 to disable the DMA transfer. If the TE and DSE bits are set when DMA transfer is aborted, these bits should be initialized. There is a possibility that TE and DSE will not be set with synchronized timing after transmission, so it's necessary to recognize the following three possibilities and take measures accordingly.

1. The DSE and TE bits are set to 1 before initialization of DMACHCR, but after the interrupt was disabled.
   The TE and DSE bits are initialized within the DMA transfer initialization sequence.
2. The DSE and TE bits are set to1 and the controller fails to abort the transfer, after the interrupt was disabled.
   When the DE bit has become 0 after DMA transfer initialization, check the TE and DSE bits. If the TE or DSE bit is 1, go through the DMA transfer initialization process.
3. The TE and DSE bits are not cleared to 0 but the transfer is aborted, after the interrupt is disabled.
   The TE or DSE bits are not set because data for transfer still remain after transfer is aborted.

Note: Initialization of DMA transfer during execution of the last transfer leads to a delay in setting of the TE and DSE bits, so include a dummy read.

Figure 31.17 shows an example of processing to abort DMA transfer.

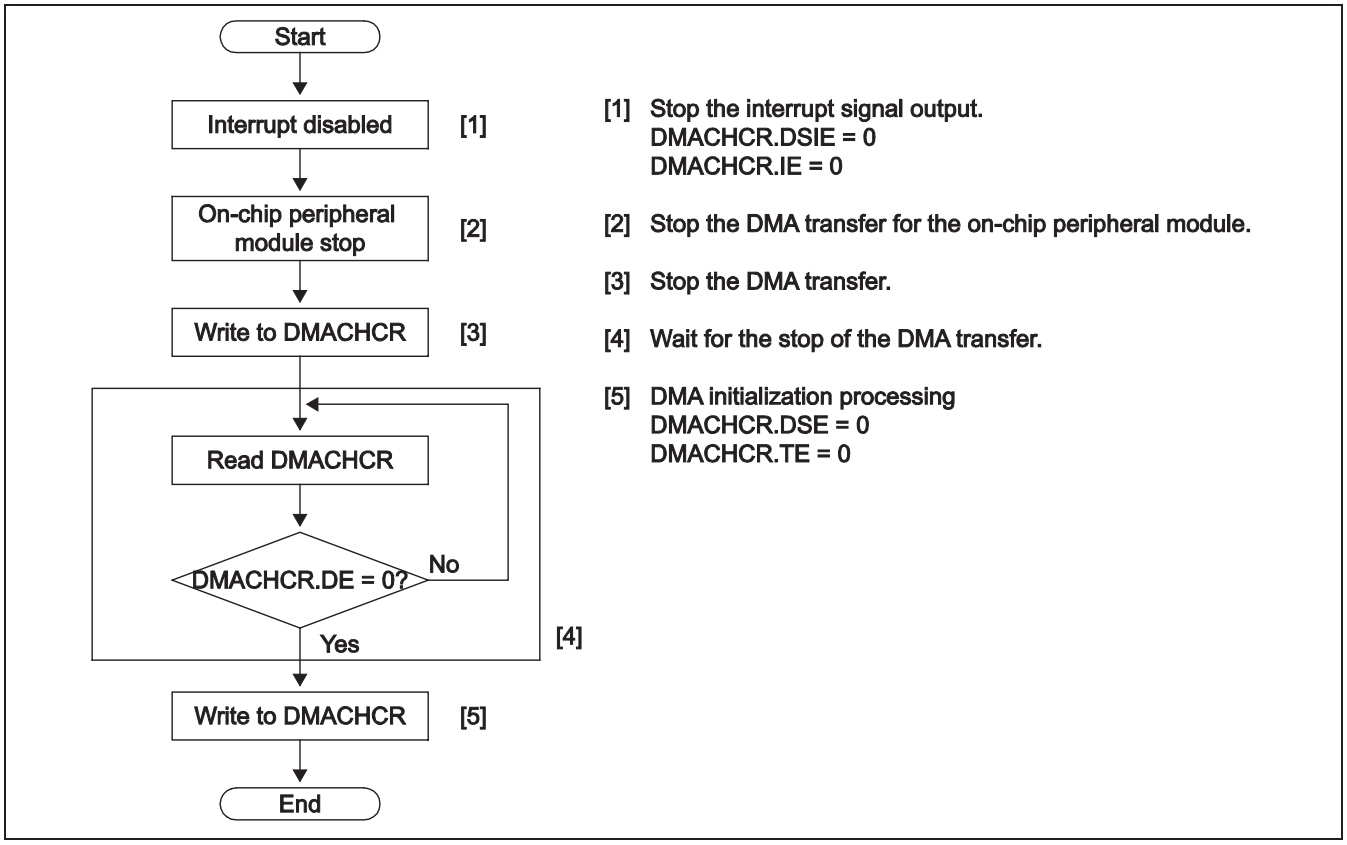


Figure 31.17 Example of Processing to Abort DMA Transfer

32. Audio-DMAC-Peripheral-Peripheral (Audio-DMACpp)

32.1 Overview

The Audio DMAC-Peripheral-Peripheral module controls data transfer between the audio modules connected to the audio local bus.

32.1.1 Features

- Number of channels: 29 channels
- Data transfer size: Longword (4 bytes)
- Addressing mode: Dual addressing; fixed access size
- Transfer count: Not programmable
- Interrupt processing: None

32.1.2 Block Diagram

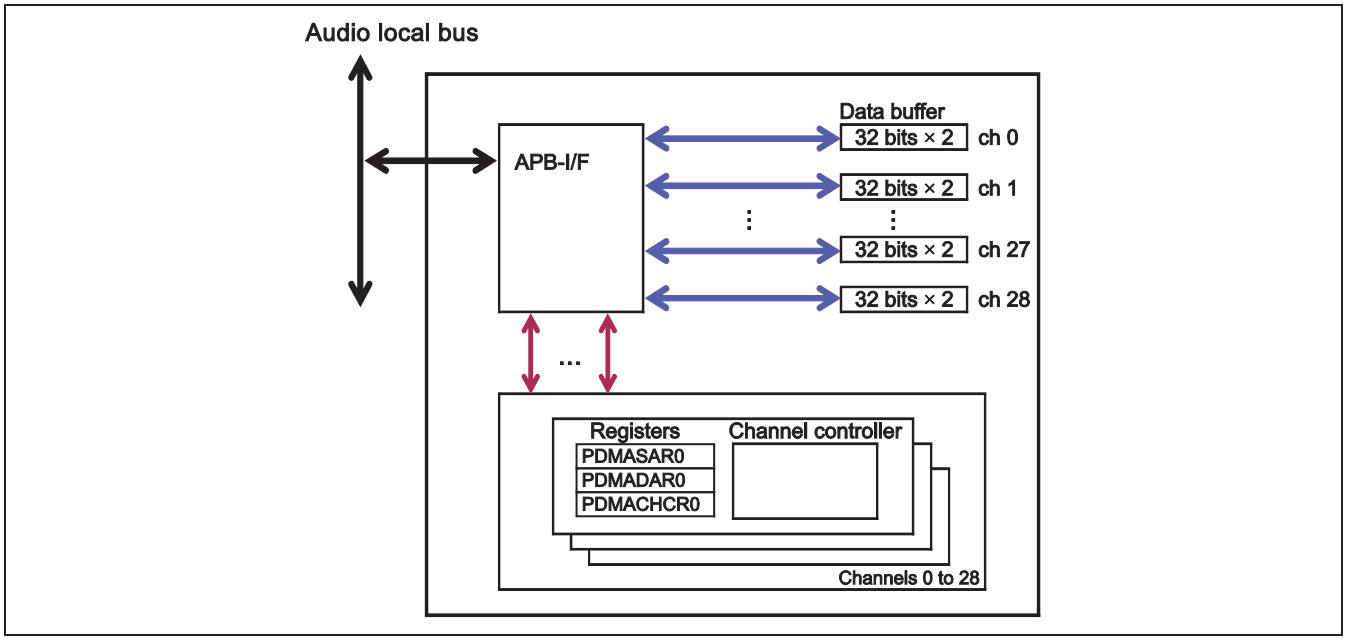


Figure 32.1 Block Diagram

32.1.3 Input/Output Pins

No external pins are provided.

32.1.4 Register Configuration

Table 32.1 List of Registers

Register Name	Abbreviation	R/W	Address	Initial Value	Access Size
PDMA Source Address n Register	PDMASARn	R/W	H'EC74 0020 + H'10 × [n]	H'0000 0000	32
PDMA Destination Address n Register	PDMADARn	R/W	H'EC74 0024 + H'10 × [n]	H'0000 0000	32
PDMA Channel Control n Register	PDMACHCRn	R/W	H'EC74 002C + H'10 × [n]	H'0000 0000	32

Notes: 1. n indicates the DMAC channel number (n = 0 to 28).
2. Access the listed registers from the CPU in longword (32-bit) units; byte or word access is prohibited.
3. Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

32.2 Register Description

[Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

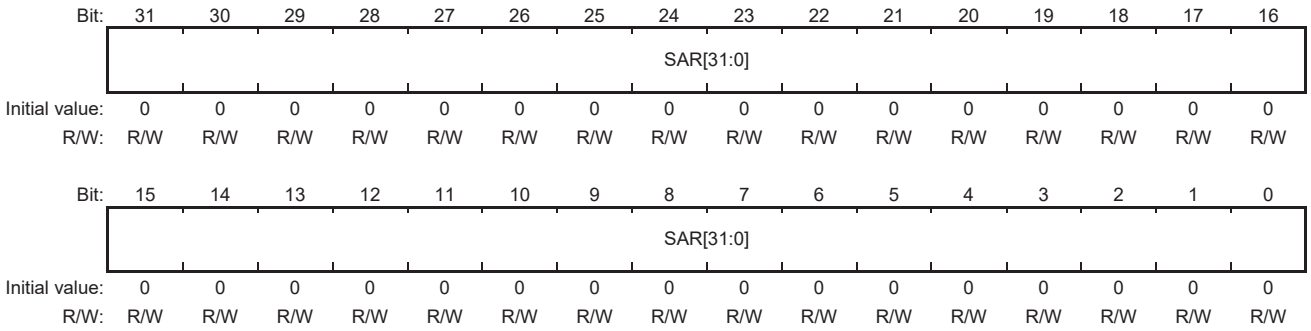
R/WC1: Readable/writable. Writing 1 initializes the bit, and writing 0 is ignored.

R: Read-only. The write value should always be 0.

—/W: Write-only. The read value is undefined.

32.2.1 PDMA Source Address n Register (PDMASARn)

Function: Sets the DMA transfer source address.

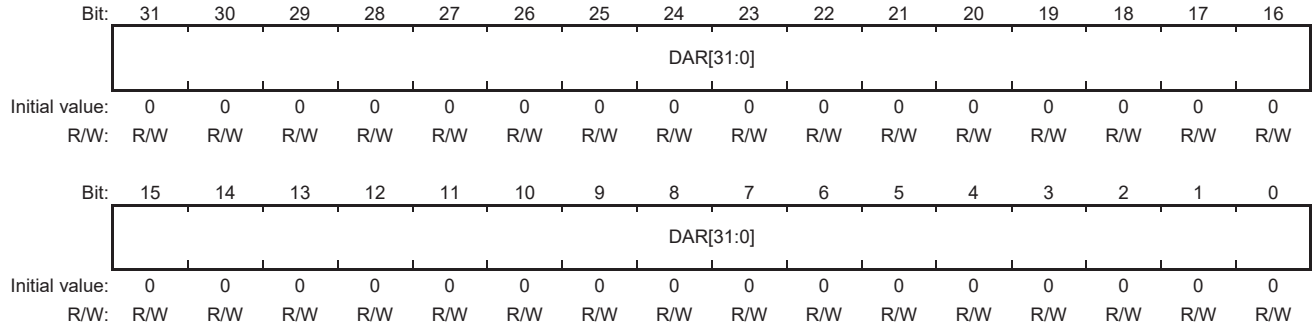


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR	All 0	R/W	Sets the DMA transfer source address.

Note: It's prohibited to set same source address in other channels including.

32.2.2 PDMA Destination Address n Register (PDMADARn)

Function: Sets the DMA transfer destination address.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR	All 0	R/W	Sets the DMA transfer destination address.

Note: It's prohibited to set same source address in other channels including.

32.2.3 PDMA Channel Control n Register (PDMACHCRn)

Function: Selects the request sources of DMA transfer source and destination, and also starts or stops DMA.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	SRS[6:0]							—	DRS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30 to 24	SRS	H'00	R/W	Transfer Source Request Source Select (setting H'00 to H'38 and the values with — are prohibited)

Set Value (H'xx)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
Transfer Source Request Source	SSI00	SSI01	SSI02	SSI03	SSI10	SSI11	SSI12	SSI13	SSI20	SSI21	SSI22	SSI23	SSI3	SSI4	SSI5	SSI6	SSI7	SSI8	SSI90	SSI91	SSI92	SSI93
Set Value (H'xx)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Transfer Source Request Source	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Set Value (H'xx)	—	—	—	—	—	—	—	—	—	2E	2F	30	31	32	33	—	—	—	37	38	—	—
Transfer Source Request Source	—	—	—	—	—	—	—	—	—	SCU_SRCO1	SCU_SRCO2	SCU_SRCO3	SCU_SRCO4	SCU_SRCO5	SCU_SRCO6	—	—	—	SCU_CMD0	SCU_CMD1	—	—

23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
22 to 16	DRS	H'00	R/W	Transfer Destination Request Source Select (setting H'00 to H'33 and the values with — are prohibited)

Set Value (H'xx)	00	01	02	03	04	05	06	07	08	09	0A	0B	0C	0D	0E	0F	10	11	12	13	14	15
Transfer Destination Request Source	SSI00	SSI01	SSI02	SSI03	SSI10	SSI11	SSI12	SSI13	SSI20	SSI21	SSI22	SSI23	SSI3	SSI4	SSI5	SSI6	SSI7	SSI8	SSI90	SSI91	SSI92	SSI93
Set Value (H'xx)	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Transfer Destination Request Source	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Set Value (H'xx)	—	—	—	—	—	—	—	—	—	2E	2F	30	31	32	33	—	—	—	—	—	—	—
Transfer Destination Request Source	—	—	—	—	—	—	—	—	—	SCU_SRCI1	SCU_SRCI2	SCU_SRCI3	SCU_SRCI4	SCU_SRCI5	SCU_SRCI6	—	—	—	—	—	—	—

15 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	DE	0	R/W	DMA Enable To enable DMA transfer function, set this bit to 1. Clearing this bit to 0 stops transfer. Note: Even if 0 is written to this bit while it is 1, 1 is read out until the transfer is completed.

Note: It's prohibited to set same source address in other channels including.

32.3 Operation

32.3.1 PDMASARn and PDMADARn Register Settings

Table 32.2 PDMASARn and PDMADARn Register Settings

Request Source	PDMASARn or PDMADARn	
SSI00	H'EC40	0000
SSI01		0400
SSI02		0800
SSI03		0C00
SSI10		1000
SSI11		1400
SSI12		1800
SSI13		1C00
SSI20		2000
SSI21		2400
SSI22		2800
SSI23		2C00
SSI3		3000
SSI4		4000
SSI5		5000
SSI6		6000
SSI7		7000
SSI8		8000
SSI90		9000
SSI91		9400
SSI92		9800
SSI93		9C00
SCU_SRCI1**	H'EC30	0400
SCU_SRCI2**		0800
SCU_SRCI3**		0C00
SCU_SRCI4**		1000
SCU_SRCI5**		1400
SCU_SRCI6**		1800
SCU_SRCO1*		4400
SCU_SRCO2*		4800
SCU_SRCO3*		4C00
SCU_SRCO4*		5000
SCU_SRCO5*		5400
SCU_SRCO6*		5800
SCU_CMD0*		8000
SCU_CMD1*		8400

Notes: * Only PDMASARn is used.
** Only PDMADARn is used.

32.3.2 Setting Flow

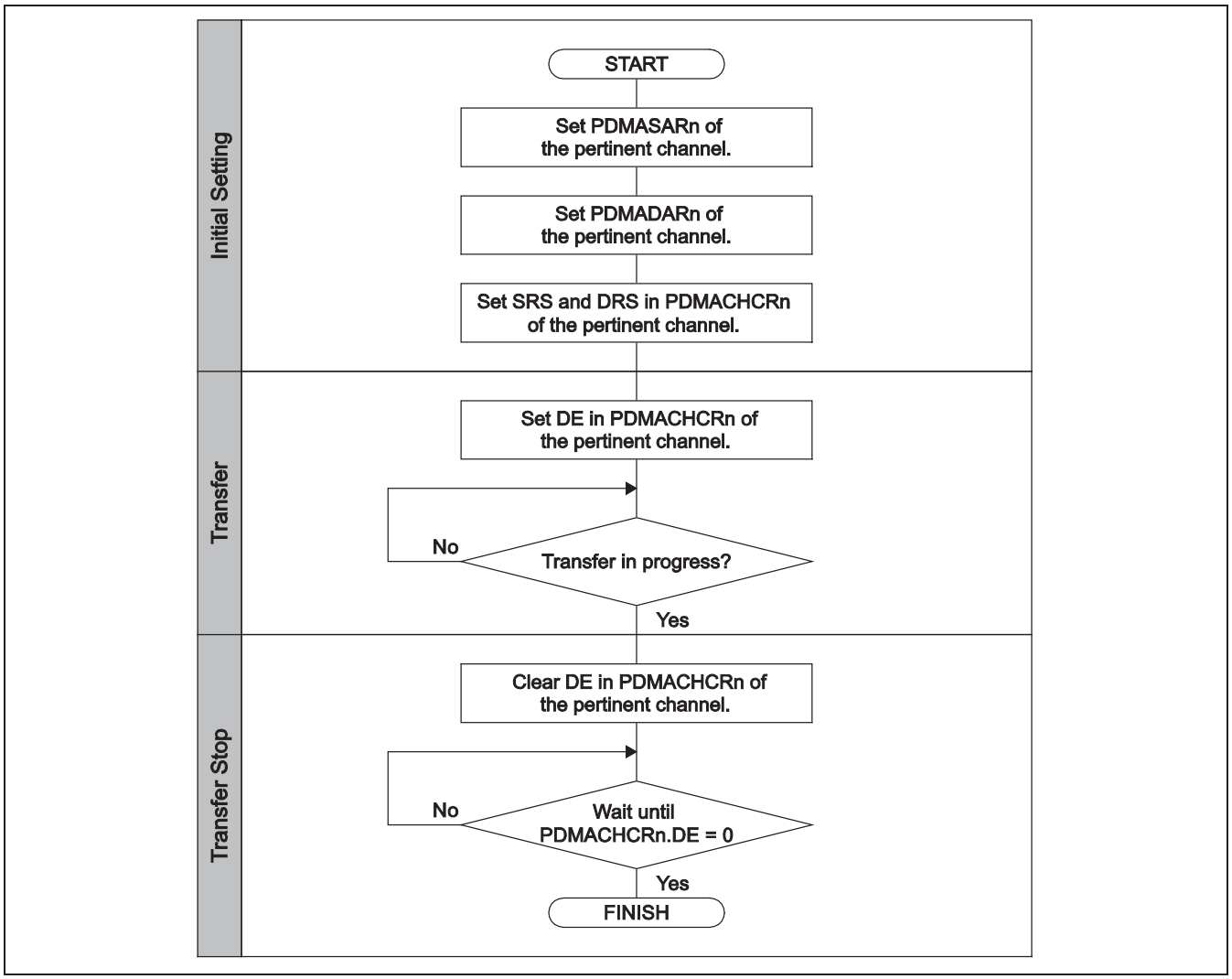


Figure 32.2 Setting Flow

32.4 Usage Notes

There is no attention of the usage.

33. Ethernet MAC Controller (Ether)

33.1 Overview

The Ether is a control unit which incorporates a function core conforming to the IEEE802.3u MAC (media access control) layer standard.

33.1.1 Features

- IEEE802.3u MAC (Ether) function
- Transmits and receives data frames
- Supports transfer at 10 and 100 Mbps
- Conforms to IEEE802.3u
- Reduced media independent interface (RMII)
- Magic packet detection
- Flow control conforming to IEEE802.3x or back pressure system
- On-chip DMA controller

Figure 33.1 shows a block diagram of the Ether. Table 33.1 lists the functions of each block.

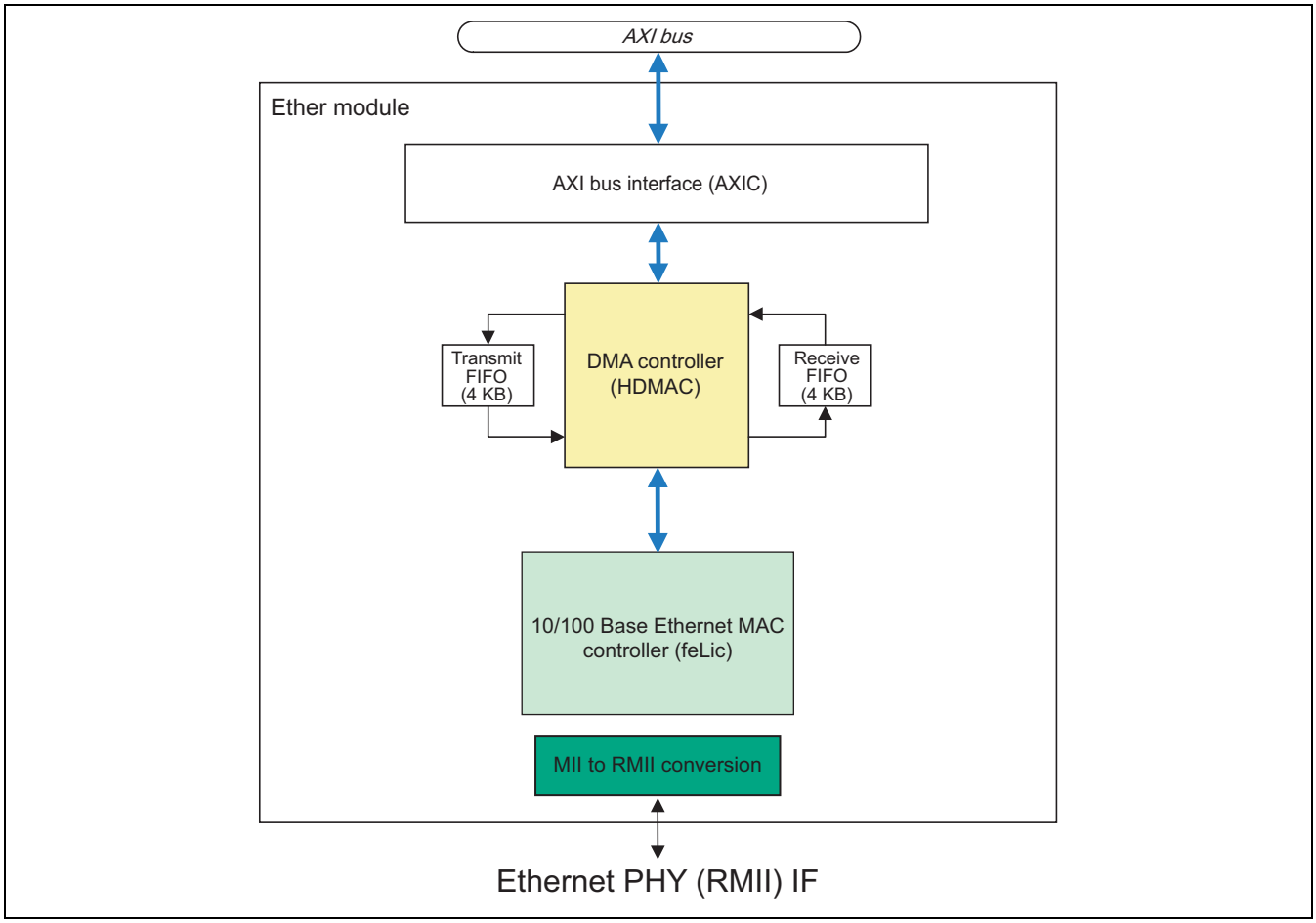


Figure 33.1 Block Diagram of Ether

Table 33.1 Functions of Each Block

Block	Function
AXI bus interface (AXIC)	• Controls AXI bus interface.
DMA controller (HDMAC)	• DMA transfer of data transmitted from and received in the 10/100 Base Ethernet MAC controller between the transmit/receive buffer on memory and internal FIFOs • For details, see section 33.8, HDMAC Function Specifications.
10/100 Base Ethernet MAC controller (feLic)	• Conforms to the IEEE802.3u MAC layer standard. • Transmits and receives data frames. • Supports transfer at 10/100 Mbps. • Magic packet detection • Flow control conforming to IEEE802.3x or back pressure system • For details, see section 33.9, feLic Function Specifications.
MII to RMII conversion	• MII to RMII interface conversion
Transmit/receive FIFO (TFIFO/RFIFO)	• Transmit/receive FIFO for DMA controller • Transmit FIFO depth: 4 Kbytes • Receive FIFO depth: 4 Kbytes

33.2 Input/Output Pins

Table 33.2 lists the external pin functions.

Table 33.2 External Pin Function

Pin Name	I/O	Function
ETH_REF_CLK	Input	Reference input clock
ETH_TXD0 ETH_TXD1	Output	Transmit data
ETH_TX_EN	Output	Transmit data enable
ETH_CRS_DV	Input	Carrier sense
ETH_RX_ER	Input	Receive error
ETH_RXD0 ETH_RXD1	Input	Receive data
ETH_MDC	Output	Management data clock
ETH_MDIO	I/O	Management data
ETH_LINK	Input	PHY output LINK signal
ETH_MAGIC	Output	Magic packet detection

33.3 Endian

The Ether has a 32-bit interface. Figure 33.2 shows data arrangement. The Ether allows endian conversion for DMA data through the setting of the CXR0 register of the HDMAC.

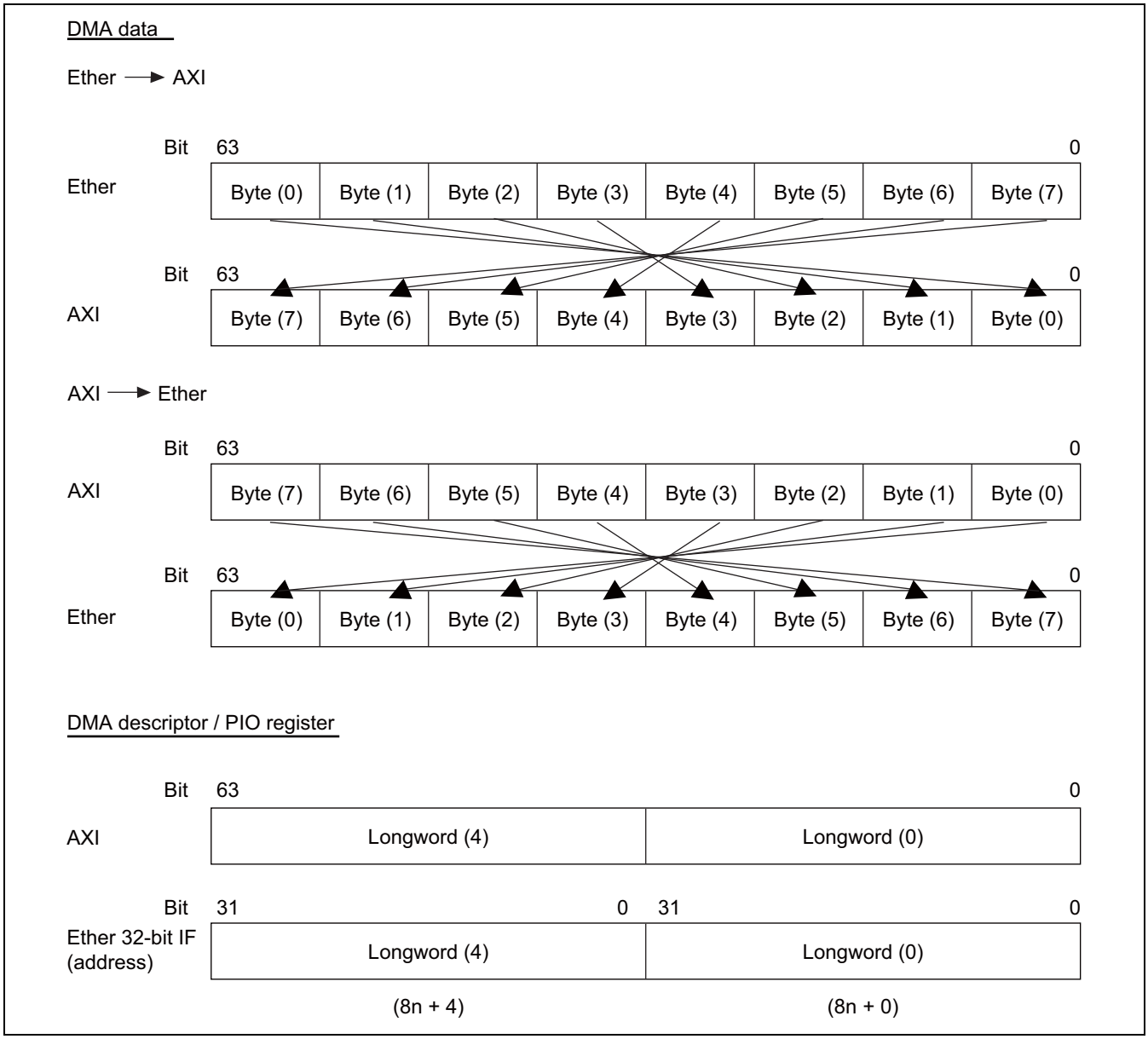


Figure 33.2 Data Arrangement

33.4 Register Descriptions

(1) Notes on Register Access

To access the registers, the following restrictions and notes should be obeyed.

1. For the register bits not defined implicitly in this specifications document, the write value should always be 0, and the read value should always be handled as undefined.
2. Even when there are no restrictions on writing to each register, the undefined bits should be written to as described in the above restriction.
3. Each register is a 32-bit long and should be accessed in 32-bit units. Accordingly, any register cannot be partially read from or written to.

(2) Register Configuration

Table 33.3 shows the configuration of HDMAC registers. Table 33.4 shows the configuration of feLic registers.

Table 33.3 HDMAC Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
HDMAC operating mode setting register	CXR0	R/W*	H'EE70 0200	H'0000 0000	32
Transmit activation register	CXR1	R/W*	H'EE70 0208	H'0000 0000	32
Receive activation register	CXR2	R/W	H'EE70 0210	H'0000 0000	32
Transmit descriptor start address setting register	CXR3	R/W*	H'EE70 0218	H'0000 0000	32
Receive descriptor start address setting register	CXR4	R/W*	H'EE70 0220	H'0000 0000	32
Status register	CXR5	R/W	H'EE70 0228	H'0000 0000	32
Interrupt mask setting register	CXR6	R/W	H'EE70 0230	H'0000 0000	32
Error mask setting register	CXR7	R/W	H'EE70 0238	H'0000 0000	32
Discarded frame counter register	CXR8	R/W	H'EE70 0240	H'0000 0000	32
Transmit FIFO threshold setting register	CXR9	R/W*	H'EE70 0248	H'0000 0000	32
External FIFO depth setting register	CXR10	R/W*	H'EE70 0250	H'0000 0000	32
Receive activation reset method setting register	CXR11	R/W*	H'EE70 0258	H'0000 0000	32
Transmit FIFO underflow counter register	CXR13	R/W	H'EE70 0264	H'0000 0000	32
Receive FIFO overflow counter register	CXR14	R/W	H'EE70 0268	H'0000 0000	32
RMII mode register	CXR15	R/W	H'EE70 026C	H'0000 0000	32
Receive FIFO busy transmit threshold setting register	CXR16	R/W	H'EE70 0270	H'0007 0007	32
Transmit interrupt mode setting register	CXR18	R/W	H'EE70 027C	H'0000 0000	32

Note: * There are restrictions on write access.

Table 33.4 feLic Register Configuration

Name	Abbreviation	R/W	Address	Initial Value	Access Size
feLic operating mode setting register	CXR20	R/W*	H'EE70 0300	H'0000 0000	32
Long frame length check value setting register	CXR2A	R/W*	H'EE70 0308	H'0000 0000	32
Status register	CXR21	R/W	H'EE70 0310	H'0000 0000	32
interrupt mask setting register	CXR22	R/W	H'EE70 0318	H'0000 0000	32
MII control register	CXR23	R/W	H'EE70 0320	H'0000 000x	32
PHY status register	CXR2B	R	H'EE70 0328	H'0000 000x	32
Random number generating counter upper limit setting register	CXR30	R/W	H'EE70 0340	H'0000 0000	32
IPG counter setting register	CXR70	R/W*	H'EE70 0350	H'0000 0014	32
Automatic PAUSE parameter setting register	CXR71	R/W	H'EE70 0354	H'0000 0000	32
Manual PAUSE parameter setting register	CXR72	W	H'EE70 0358	H'0000 0000	32
Receive PAUSE frame counter register	CXR80	R	H'EE70 0360	H'0000 0000	32
PAUSE frame retransmit count setting register	CXR81	R/W*	H'EE70 0364	H'0000 0000	32
PAUSE frame retransmit counter register	CXR82	R	H'EE70 0368	H'0000 0000	32
MAC address high register	CXR24	R/W*	H'EE70 03C0	H'0000 0000	32
MAC address low register	CXR25	R/W*	H'EE70 03C8	H'0000 0000	32
TINT1 count register	CXR40	R/W	H'EE70 03D0	H'0000 0000	32
TINT2 count register	CXR41	R/W	H'EE70 03D4	H'0000 0000	32
TINT3 count register	CXR42	R/W	H'EE70 03D8	H'0000 0000	32
TINT4 count register	CXR43	R/W	H'EE70 03DC	H'0000 0000	32
RINT1 count register	CXR50	R/W	H'EE70 03E4	H'0000 0000	32
RINT2 count register	CXR51	R/W	H'EE70 03E8	H'0000 0000	32
RINT3 count register	CXR52	R/W	H'EE70 03EC	H'0000 0000	32
RINT4 count register	CXR53	R/W	H'EE70 03F0	H'0000 0000	32
RINT5 count register	CXR54	R/W	H'EE70 03F4	H'0000 0000	32
RINT8 count register	CXR55	R/W	H'EE70 03F8	H'0000 0000	32

Note: * There are restrictions on write access.

33.4.1 HDMAC Operating Mode Setting Register (CXR0)

CXR0 is used for specifying the operating mode of the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	DE	DL1	DL0	—	—	—	SWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 7	—	All 0	R	Reserved
6	DE	0	R/W	DMA Data Endian Conversion 0: Does not perform endian conversion for DMA data. 1: Performs endian conversion for DMA data. Endian conversion for descriptors and registers is not performed. Note: Be sure to set this bit to 1 before operating the Ethernet MAC controller (Ether).
5, 4	DL1 and DL0	00	R/W	Transmit/Receive Descriptor Length Setting Descriptor length 00: 16 bytes 01: 32 bytes 10: 64 bytes 11: Reserved
3 to 1	—	All 0	R	Reserved
0	SWR	0	R/W	HDMAC/feLic Software Reset Writing 1 resets the HDMAC/feLic module except for CXR3, CXR4, CXR8, CXR13 and CXR14. Note: Registers should not be accessed until 64 clock cycles have elapsed after the SWR bit is set to 1. When writing to registers (except for the SWR bit), the transmitting and receiving function should be disabled.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.2 Transmit Activation Register (CXR1)

CXR1 initiates transmission by the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	TRNS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	TRNS	0	R/W	Transmit Activation If 1 is written to this bit, the HDMAC accesses the transmit descriptor ring and transmits frames for all the valid descriptors. This bit is automatically cleared when transmission of all the valid frames has been completed, or the transmit descriptor depletion occurs. Note: Writing 0 is disabled.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.3 Receive Activation Register (CXR2)

CXR2 initiates reception by the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	R
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

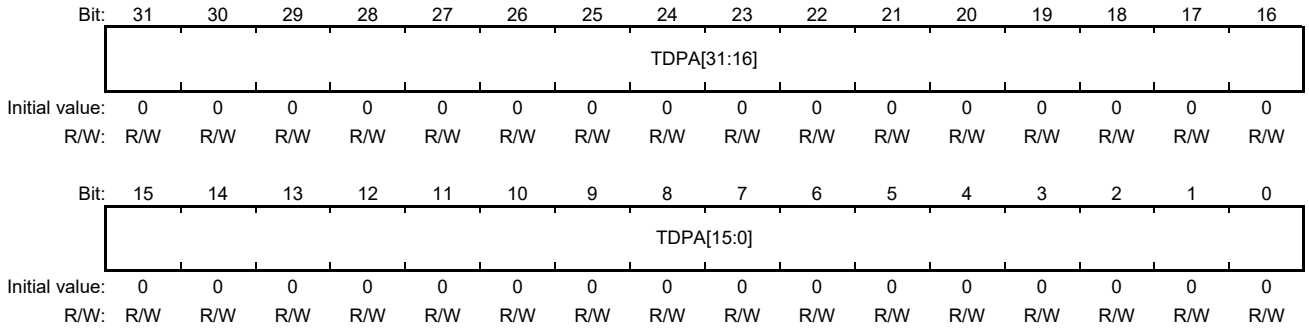
Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	R	0	R/W	Receive Ready If 1 is written to this bit, the HDMAC accesses the receive descriptor ring and enters the receive wait state. For operation of this bit after completion of reception, which depends on the CXR11 settings, see section 33.4.12, Receive Activation Reset Method Setting Register (CXR11). If 0 is written to this bit, the HDMAC completes reception of the frame being processed, and then disables the receiving function. This bit is reset to 0 when the RACT bit of the fetched descriptor is 0 (when the receive descriptor depletion occurs).

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.4 Transmit Descriptor Start Address Setting Register (CXR3)

CXR3 specifies the start address of the transmit descriptor ring. The start address of the descriptor ring should be aligned to the boundary consistent with the descriptor length specified by the DL bits in CXR0.

Writing to CXR3 should be performed before transmission is started. Writing to CXR3 after transmission has been started is prohibited and operation according to the written value cannot be guaranteed.

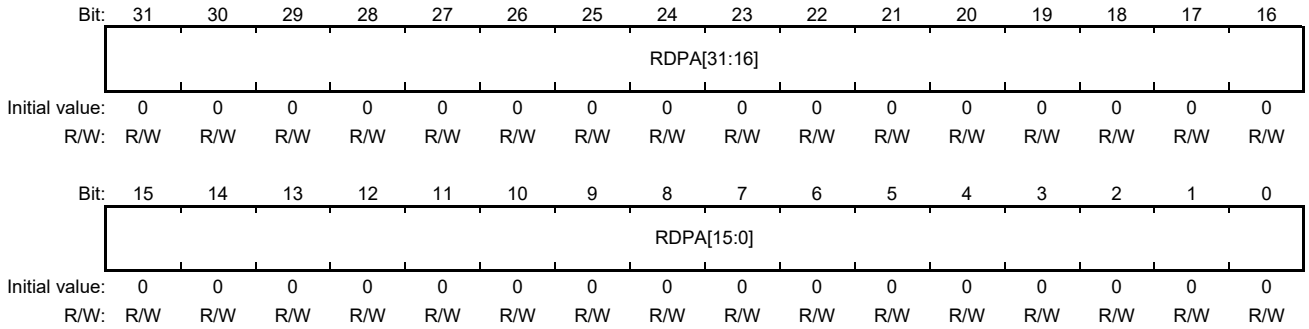


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TDPA [31:0]	All 0	R/W	Transmit Descriptor Start Address Bits 3 to 0 should be set to 0 for alignment of the descriptor. Note: A value other than 0 must not be set to bits 3 to 0. Writing is prohibited after transmission has been started.

33.4.5 Receive Descriptor Start Address Setting Register (CXR4)

CXR4 specifies the start address of the receive descriptor ring. The start address of the descriptor ring should be aligned to the boundary consistent with the descriptor length specified by the DL bits in CXR0.

Writing to CXR4 should be performed before reception is started. Writing to CXR4 after reception has been started is prohibited and operation according to the written value cannot be guaranteed.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	RDPA [31:0]	All 0	R/W	Receive Descriptor Start Address Bits 3 to 0 should be set to 0 for alignment of the descriptor. Note: A value other than 0 must not be set to bits 3 to 0. Writing is prohibited after transmission has been started.

33.4.6 Status Register (CXR5)

CXR5 is a register that indicates HDMAC interrupt sources.

The status sources are output to the INTC module by a signal of each source.

Each bit is cleared by writing 1 to the corresponding bit. The MINT bit is set to 0 by clearing CXR21. Generation of interrupts can be masked by the corresponding bits in CXR6.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TWB	BINT	AINT	LKON	TABT	RABT	RFRMER	BER	MINT	FTC	TDE	TFE	FRC	RDE	RFE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT8	TINT7	TINT6	TINT5	TINT4	TINT3	TINT2	TINT1	RINT8	RINT7	RINT6	RINT5	RINT4	RINT3	RINT2	RINT1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value*2	R/W	Description
31	—	0	R	Reserved
30	TWB	0	R/W*1	Indicates that write-back to the transmit descriptor whose TWBI bit is set has been performed. The interrupt can be generated every frame by so setting CXR18. <Interrupt source>
29	BINT	0	R/W*1	Reserved This bit should always be set to 0.
28	AINT	0	R/W*1	Reserved This bit should always be set to 0.
27	LKON	0	R/W*1	Reserved This bit should always be set to 0.
26	TABT	0	R/W*1	Transmit Abort Detect <Interrupt source>
25	RABT	0	R/W*1	Receive Abort Detect <Interrupt source>
24	RFRMER	0	R/W*1	Receive Frame Count Overflow Occurrence <Interrupt source>
23	BER	0	R/W*1	Indicates that a DMA error is input.
22	MINT	0	R	M Port Interrupt Occurrence <Interrupt source> Indicates that an interrupt signal from the feLic is asserted.
21	FTC	0	R/W*1	Frame Transmit Completion <Interrupt source> Indicates that transmission of all the frames specified by the transmit descriptor has been completed. This bit is not set for each frame.
20	TDE	0	R/W*1	Reserved This bit should always be set to 0.
19	TFE	0	R/W*1	Transmit FIFO Underflow Error Occurrence <Interrupt source> Indicates that the transmit FIFO becomes empty during frame transmission.

Bit	Bit Name	Initial Value*2	R/W	Description
18	FRC	0	R/W*1	Frame Receive Completion <Interrupt source> Indicates that the receive descriptor is updated by frame reception. This bit is set when reception of one frame has been completed regardless of the setting of the RR bit in CXR11.
17	RDE	0	R/W*1	Receive Descriptor Depletion <Interrupt source> Indicates that the fetched receive descriptor is invalid. Occurrence of this source resets the R bit in CXR2 to 0.
16	RFE	0	R/W*1	Receive FIFO Overflow Error Occurrence <Interrupt source>
15 to 8	TINT8 to TINT1	All 0	R/W*1	Transmit Port Interrupt
7 to 0	RINT8 to RINT1	All 0	R/W*1	Receive Port Interrupt

Notes: 1. These bits are cleared by writing 1 to the corresponding bits. Writing 0 has no meaning.
2. This register is initialized by an HDMAC/feLic software reset.

33.4.7 Interrupt Mask Setting Register (CXR6)

CXR6 is a register that masks the interrupts indicated by CXR5.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	TWB	BINT	AINT	LKON	TABT	RABT	RFRMER	BER	MINT	FTC	TDE	TFE	FRC	RDE	RFE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT8	TINT7	TINT6	TINT5	TINT4	TINT3	TINT2	TINT1	RINT8	RINT7	RINT6	RINT5	RINT4	RINT3	RINT2	RINT1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31	—	0	R	Reserved
30	TWB	0	R/W	Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR5. 1: Enables an interrupt indicated by the corresponding bit in CXR5. Note: Bits 29 to 27 should always be set to 0.
29	BINT	0	R/W	
28	AINT	0	R/W	
27	LKON	0	R/W	
26	TABT	0	R/W	
25	RABT	0	R/W	
24	RFRMER	0	R/W	
23	BER	0	R/W	
22	MINT	0	R/W	
21	FTC	0	R/W	
20	TDE	0	R/W	
19	TFE	0	R/W	
18	FRC	0	R/W	
17	RDE	0	R/W	
16	RFE	0	R/W	
15 to 8	TINT8 to TINT1	All 0	R/W	
7 to 0	RINT8 to RINT0	All 0	R/W	

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.8 Error Mask Setting Register (CXR7)

CXR7 is a register that specifies whether or not to allow the status of the descriptor information (indicated by the RFS7 bit in RD0) to be reflected in the RFE bit in the receive descriptor 0 (RD0) as a summary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

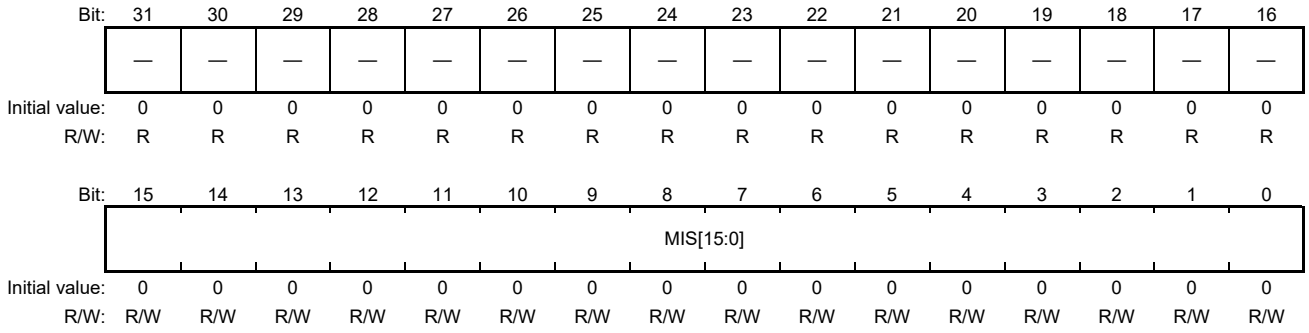
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RINT8	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 8	—	All 0	R	Reserved
7	RINT8	All 0	R/W	Receive Descriptor Error Flag (RFE) Mask 0: Allows RINT8 (RFS7 bit in RD0) to be reflected in RFE. 1: Does not allow RINT8 (RFS7 bit in RD0) to be reflected in RFE.
6 to 0	—	All 0	R	Reserved

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.9 Discarded Frame Counter Register (CXR8)

CXR8 is a register that indicates the number of discarded frames.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	MIS[15:0]	H'0000	R/W	Discarded Frame Counter These bits indicate the number of frames which are discarded because the receive descriptor is disabled, for example. The counter stops counting when all bits are set to 1 (H'FFFF). Note: Writing any data clears these bits.

33.4.10 Transmit FIFO Threshold Setting Register (CXR9)

CXR9 is a register that specifies the threshold for the transmit FIFO.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	FO[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R	R	R	R	R	R/W	R	R	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 11	—	All 0	R	Reserved
10 to 0	FO[10:0]	H'000	R/W	Transmit FIFO Threshold Setting Threshold H'000: Store and forward H'001: 4 bytes H'002: 8 bytes : : H'0FE: 1016 bytes H'0FF: 1020 bytes H'100: 1024 bytes : : H'1FE: 1040 bytes H'1FF: 2044 bytes H'200: 2048 bytes : : H'3FE: 4088 bytes H'3FF: 4092 bytes H'400 to H'7FF: Setting prohibited Reading (transmission) is started when one frame data has been written to the FIFO or when data in the FIFO exceeds the above setting. Using on the initial value (store and forward) is recommended to prevent from occurring underflow error on sending. Note: Writing is disabled when the TRNS bit in CXR1 = 1.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.11 External FIFO Depth Setting Register (CXR10)

CXR10 is a register that specifies the depth of the transmit and receive FIFOs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	TA[4:0]					—	—	—	RA[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 13	—	All 0	R	Reserved
12 to 8	TA[4:0]	H'00	R/W	Transmit FIFO Depth Setting Depth H'00: 256 bytes H'01: 512 bytes H'02: 768 bytes H'03: 1024 bytes : : H'07: 2048 bytes : : H'0F: 4096 bytes H'10 to H'1F: Setting prohibited Note: Writing to bits 12 to 8 is disabled when the TRNS bit in CXR1 = 1.
7 to 5	—	All 0	R	Reserved
4 to 0	RA[4:0]	H'00	R/W	Receive FIFO Depth Setting Depth H'00: 256 bytes H'01: 512 bytes H'02: 768 bytes H'03: 1024 bytes : : H'07: 2048 bytes : : H'0F: 4096 bytes H'10 to H'1F: Setting prohibited Note: Writing to bits 4 to 0 is disabled when the R bit in CXR2 = 1.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.12 Receive Activation Reset Method Setting Register (CXR11)

CXR11 is a register that specifies a method for resetting the receive ready bit (R bit in CXR2).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RNR	RR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 2	—	All 0	R	Reserved
1	RNR	0	R/W	Reserved This bit should always be set to 0.
0	RR	0	R/W	Receive Ready Reset 0: (initial value) Automatically clears the receive ready bit (R bit in CXR2) by hardware. The receive ready bit (R bit in CXR2) is automatically cleared by receiving one frame, thus disabling reception of the following frames. In this mode, interrupt control for each frame is possible. 1: Normal operating mode Resets the receive ready bit (R bit in CXR2 by software. After 1 is written to the receive ready bit (R bit in CXR2), the HDMAC automatically fetches the receive descriptor and receives frames until 0 is written to the receive ready bit (R bit in CXR2). Continuous reception of multiple frames is possible. Note that the receive ready bit (R bit in CXR2) is reset to 0 when the RACT bit in the fetched descriptor is 0. Note: Writing to this bit is disabled when the R bit in CXR2 = 1.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.13 Transmit FIFO Underflow Counter Register (CXR13)

CXR13 is a register that indicates the number of times the transmit FIFO underflow occurs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TFUF[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	TFUF[15:0]	H'0000	R/W	Transmit FIFO Underflow Counter The counter stops counting when all bits are set to 1 (H'FFFF). Note: Writing any data clears these bits.

33.4.14 Receive FIFO Overflow Counter Register (CXR14)

CXR14 is a register that indicates the number of times the receive FIFO overflow occurs.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFOF[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	RFOF[15:0]	H'0000	R/W	Receive FIFO Overflow Counter The counter stops counting when all bits are set to 1 (H'FFFF). Note: Writing any data clears these bits.

33.4.15 RMII Mode Register (CXR15)

CXR15 sets the RMII mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RMII
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	RMII	0	R/W	RMII Mode Specification 0: (initial value) 1: RMII mode Be sure to set this bit to 1 before operating the Ethernet MAC controller (Ether).

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.16 Receive FIFO Busy Transmit Threshold Setting Register (CXR16)

CXR16 is a register that specifies the threshold value for sending the receive FIFO busy to the feLic based on the number of frames and number of data bytes stored in the receive FIFO.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFF[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	RFD[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 19	—	All 0	R	Reserved
18 to 16	RFF[2:0]	100	R/W	Busy Transmit Threshold based on the Number of Receive Frames Setting Threshold 000: Transmits the busy when two frames have been stored. 001: Transmits the busy when four frames have been stored. 010: Transmits the busy when six frames have been stored. : 110: Transmits the busy when 14 frames have been stored. 111: Transmits the busy when 16 frames have been stored.
15 to 3	—	All 0	R	Reserved
2 to 0	RFD[2:0]	100	R/W	Busy Transmit Threshold based on the Amount of Data in the Receive FIFO Setting Threshold 000: Transmits the busy when 224 (256 – 32) bytes have been stored. 001: Transmits the busy when 480 (512 – 32) bytes have been stored. 010: Transmits the busy when 736 (768 – 32) bytes have been stored. 011: Transmits the busy when 992 (1024 – 32) bytes have been stored. : 110: Transmits the busy when 1760 (1792 – 32) bytes have been stored. 111: See the following note. Note: The set value to these bits should be smaller than the set value to the RA bits in CXR10. If the former and latter values are equal, the busy will be sent out when (receive FIFO depth – 64 bytes) have been stored in the receive FIFO, not when (receive FIFO depth – 32 bytes) have been stored. For example, when the RA bits in CXR10 and RFD bits in CXR16 are both 7, the busy will be sent out when 1984 (= 2048 – 64) bytes have been stored in the receive FIFO.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.17 Transmit Interrupt Mode Setting Register (CXR18)

CXR18 is used for setting transmit interrupt operating mode for the HDMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	TIM	—	—	—	TIS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 5	—	All 0	R	Reserved
4	TIM	0	R/W	Transmit Interrupt Mode 0: Mode in which the interrupt is issued each time a frame has been transmitted. 1: Mode in which the interrupt is issued when write-back to the descriptor whose TWBI bit is set has been completed.
3 to 1	—	All 0	R	Reserved
0	TIS	0	R/W	Interrupt Mode Enable 0: TIM setting is disabled. 1: TIM setting is enabled.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.18 feLic Operating Mode Setting Register (CXR20)

CXR20 is a register that specifies the operating mode of the feLic. Some mode bits in this register should not be modified while the transmitting and receiving functions are enabled.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	TPC	ZPF	PFR	RXF	TXF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CER	—	—	MPM	—	—	RPE	TPE	—	ILB	OLB	DPM	PRM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R/W	R	R	R/W	R/W	R	R/W*1	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value*2	R/W	Description
31 to 21	—	All 0	R	Reserved
20	TPC	0	R/W	PAUSE Frame Transmission 0: Transmission of a PAUSE frame is enabled even during a PAUSE period. 1: Transmission of a PAUSE frame is disabled during PAUSE period.
19	ZPF	0	R/W	PAUSE Frame Enable with TIME = 0 0: Control of a PAUSE frame whose TIME parameter value is 0 is disabled. 1: Control of a PAUSE frame whose TIME parameter value is 0 is enabled.
18	PFR	0	R/W	PAUSE Frame Receive Mode 0: PAUSE frame is not transferred to the upper module. 1: PAUSE frame is transferred to the upper module.
17	RXF	0	R/W	Operating Mode for Reception Flow Control 0: Reception flow control is disabled. 1: Reception flow control is enabled.
16	TXF	0	R/W	Operating Mode for Transmission Flow Control 0: Transmission flow control is disabled. 1: Transmission flow control is enabled.
15 to 13	—	All 0	R	Reserved
12	CER	0	R/W	CRC Error Frame Receive Mode 0: Normal mode (an error frame is regarded as an error). 1: Mode in which the received frame with a CRC error is not regarded as an error.
11, 10	—	All 0	R	Reserved
9	MPM	0	R/W	Magic Packet Detection Enable 0: Magic packet detection is disabled. 1: Magic packet detection is enabled.
8, 7	—	All 0	R	Reserved

Bit	Bit Name	Initial Value*2	R/W	Description
6	RPE	0	R/W	Reception Enable 0: Receiving function is disabled after completion of current frame reception. 1: Frame receiving function is enabled and receive data is transferred to the HDMAC.
5	TPE	0	R/W	Transmission Enable 0: Transmitting function is disabled after completion of current frame transmission. 1: A frame transmit request from the HDMAC is enabled.
4	—	0	R	Reserved
3	ILB	0	R/W*1	feLic Loopback Mode 0: The feLic enters normal mode. 1: The feLic enters loopback mode.
2	OLB	0	R/W*1	10-Base T or 100-Base TX Transfer Setting (Transfer at 10 or 100 Mbps) 0: Transfer is 10-base T (i.e. at 10 Mbps). 1: Transfer is 100-base TX (i.e. at 100 Mbps).
1	DPM	0	R/W*1	Duplex Mode 0: The feLic enters half-duplex mode. Note that feLic loopback mode should not be specified during this mode. 1: The feLic enters full-duplex mode.
0	PRM	0	R/W*1	Promiscuous Mode 0: The feLic enters normal mode. (When the MPM bit is set, the feLic operates in normal mode regardless of the status of this bit.) 1: The feLic enters promiscuous mode.

Notes: 1. Bits 3 to 0 should not be modified while the transmitting and receiving functions are enabled.
2. This register is initialized by an HDMAC/feLic software reset.

33.4.19 Long Frame Length Check Value Setting Register (CXR2A)

CXR2A is a register that specifies the upper limit of the receive frame length used for checking the length.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	FLUL[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 12	—	All 0	R	Reserved
11 to 0	FLUL[11:0]	H'000	R/W	Frame Length Upper Limit The specified value is used as the frame length check value. When the received frame length value exceeds this value, it is regarded as RINT4 (frame length error). (See below.) Setting Check Value H'000 to H'5EE: 1518 bytes H'5EF: 1519 bytes : : H'7FF: 2047 bytes H'800 to H'FFF: 2048 bytes Note: The CXR20 register should not be modified while the receiving function is enabled.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.20 Status Register (CXR21)

CXR21 is a register that indicates the feLic status.

The status sources are output to the INTC module by a signal of each source.

Each bit is cleared by writing 1 to the corresponding bit. Generation of interrupts can be masked by the corresponding bits in CXR22.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BCR	PRO	—	LNK	MPR	FCD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W*1	R/W*1	R	R/W*1	R/W*1	R/W*1

Bit	Bit Name	Initial Value*2	R/W	Description
31 to 6	—	All 0	R	Reserved
5	BCR	0	R/W*1	Reserved This bit should always be set to 0.
4	PRO	0	R/W*1	PAUSE Frame Retransmit Retry Over <Interrupt Source> Indicates that the PAUSE frame retransmission count has reached the upper limit of retransmission set in the CXR81 register.
3	—	0	R	Reserved
2	LNK	0	R/W*1	LINK Signal Change Interrupt <Interrupt Source> Indicates that the LINK signal output from the PHY has changed from high to low or low to high.
1	MPR	0	R/W*1	Magic Packet Receive Interrupt <Interrupt Source> Indicates that a magic packet has been received. (This bit is cleared by writing 1 to the bit; however, the MAGIC signal is not cleared because it is an external output signal.)
0	FCD	0	R/W*1	Illegal Carrier Detection Interrupt <Interrupt Source> Indicates that an illegal carrier is detected on the line.

Notes: 1. These bits are cleared by writing 1 to the corresponding bits. Writing 0 has no meaning.
2. This register is initialized by an HDMAC/feLic software reset.

33.4.21 Interrupt Mask Setting Register (CXR22)

CXR22 is a register that masks the interrupts indicated by CXR21.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	BCRE	PROE	—	LNKE	MPRE	FCDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 6	—	All 0	R	Reserved
5	BCRE	0	R/W	Reserved This bit should always be set to 0.
4	PROE	0	R/W	PAUSE Frame Retransmit Retry Over Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.
3	—	0	R	Reserved
2	LKNE	0	R/W	LINK Signal Change Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.
1	MPRE	0	R/W	Magic Packet Receive Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.
0	FCDE	0	R/W	Illegal Carrier Detection Interrupt Enable 0: Disables an interrupt indicated by the corresponding bit in CXR21. 1: Enables an interrupt indicated by the corresponding bit in CXR21.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.22 MII Control Register (CXR23)

CXR23 is a register that controls the MII interface to access the PHY register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 4	—	All 0	R	Reserved
3	MDI	—	R	MII Management Data In Read data from MII
2	MDO	0	R/W	MII Management Data Out Write data to MII
1	MMD	0	R/W	MII Management Mode 1: Data is written to MII. 0: Data is read from MII.
0	MDC	0	R/W	MII Management Clock Clock for MII

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.23 PHY Status Register (CXR2B)

CXR2B is a register that can monitor the PHY status signal.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

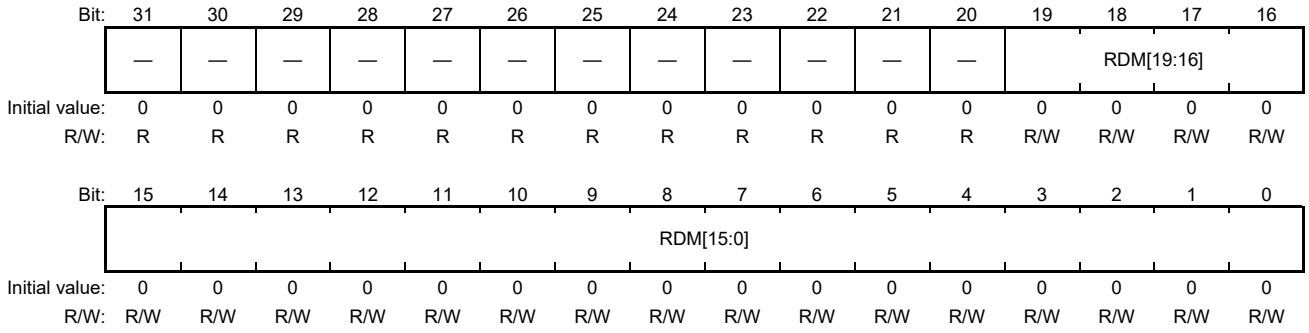
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LINK
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 1	—	All 0	R	Reserved
0	LINK	—	R	The status of the PHY output LINK signal can be monitored. See the specifications of the PHY to be connected.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.24 Random Number Generating Counter Upper Limit Setting Register (CXR30)

CXR30 is a register that can set the upper limit of the counter used for the random number generator.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 20	—	All 0	R	Reserved
19 to 0	RDM[19:0]	H'00000	R/W	Upper limit of the Counter used for the Random Number Generator H'00000: Setting for normal operation H'00001 to H'FFFFE: Counter upper limit Note: Since the operation of the feLic random number generator depends on the value set to this register, take care when setting a value other than 0.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.25 IPG Counter Setting Register (CXR70)

CXR70 is a register that specifies the IPG (inter packet gap) value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	IPG[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 5	—	All 0	R	Reserved
4 to 0	IPG[4:0]	H'14	R/W	These bits set the IPG value in 40 ns units. Setting IPG value H'00 to H'06: 400 ns H'07: 440 ns : H'13: 920 ns H'14: 960 ns (default) : H'1F: 1440 ns Note: The CXR20 register should not be modified while the transmitting and receiving functions are enabled.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.26 Automatic PAUSE Parameter Setting Register (CXR71)

CXR71 is used to set the TIME parameter value of an automatic PAUSE frame. When an automatic PAUSE frame is transmitted, the value set in this register is used as the TIME parameter of the PAUSE frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	APAUSE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	APAUSE[15:0]	H'0000	R/W	TIME Parameter Value of an Automatic PAUSE Frame One bit is equivalent to 512 bit-time.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.27 Manual PAUSE Parameter Setting Register (CXR72)

CXR72 is used to set the TIME parameter value of a manual PAUSE frame. When a manual PAUSE frame is transmitted, the value set in this register is used as the TIME parameter of the PAUSE frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MPAUSE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	W	Reserved These bits should always be set to 0.
15 to 0	MPAUSE[15:0]	H'0000	W	TIME Parameter Value of an Manual PAUSE Frame One bit is equivalent to 512 bit-time.

Note: This register can't be read.
* This register is initialized by an HDMAC/feLic software reset.

33.4.28 Receive PAUSE Frame Counter Register (CXR80)

CXR80 is used to the counter of received the PAUSE frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RPAUSE[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	RPAUSE[7:0]	H'00	R	Received PAUSE frame Counter

Note: Writing to this register has no meaning.

* This register is initialized by an HDMAC/feLic software reset.

33.4.29 PAUSE Frame Retransmit Count Setting Register (CXR81)

CXR81 is used to set the upper limit of the automatic PAUSE frame retransmission count. For details of this register, see section 33.9.2 (6), Flow Control Conforming to IEEE802.3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXPAUSE[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*1	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	TXPAUSE[15:0]	H'0000	R/W	Upper Limit of PAUSE Frame Retransmission Setting Retransmit count H'0000: Unlimited*2 H'0001: 1 : : H'FFFF: 65535 Note: The CXR20 register should not be modified while the transmitting function is enabled.

Notes: 1. This register is initialized by an HDMAC/feLic software reset.
2. When using in unlimited setting, the time parameter MPAUSE of CXR71 should be set other than zero.

33.4.30 PAUSE Frame Retransmit Counter Register (CXR82)

CXR82 is used to the counter of retransmitting of the PAUSE frame. For details of this register, see section 33.9.2 (6), Flow Control Conforming to IEEE802.3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TXP[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	TXP[15:0]	H'0000	R	PAUSE Frame Retransmit Counter

Note: Writing to this register has no meaning.
* This register is initialized by an HDMAC/feLic software reset.

33.4.31 MAC Address High Register (CXR24)

CXR24 is used to set the upper 32 bits of the universal MAC address.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MACH[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACH[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	MACH[31:0]	H'00000000	R/W	MAC Address Upper 32 Bits Note: These bits should not be written to while the transmission enable and reception enable bits in CXR20 are set.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.32 MAC Address Low Register (CXR25)

CXR25 is used to set the lower 16 bits of the universal MAC address.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MACL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 16	—	All 0	R	Reserved
15 to 0	MACL[15:0]	H'0000	R/W	MAC Address Lower 16 Bits Note: These bits should not be written to while the transmission enable and reception enable bits in CXR20 are set.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.33 TINT1 Count Register (CXR40)

CXR40 is a register with which the TINT1 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TINT1C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT1C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT1C[31:0]	H'00000000	R/W	TINT1 (Transmit Timeout) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.34 TINT2 Count Register (CXR41)

CXR41 is a register with which the TINT2 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TINT2C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT2C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT2C[31:0]	H'00000000	R/W	TINT2 (Collision Detection during Frame Transmission) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.35 TINT3 Count Register (CXR42)

CXR42 is a register with which the TINT3 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TINT3C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT3C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT3C[31:0]	H'00000000	R/W	TINT3 (Carrier Loss during Frame Transmission) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.36 TINT4 Count Register (CXR43)

CXR43 is a register with which the TINT4 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TINT4C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TINT4C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	TINT4C[31:0]	H'00000000	R/W	TINT4 (Carrier not Detected) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.37 RINT1 Count Register (CXR50)

CXR50 is a register with which the RINT1 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RINT1C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RINT1C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT1C[31:0]	H'00000000	R/W	RINT1 (CRC Error) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.38 RINT2 Count Register (CXR51)

CXR51 is a register with which the RINT2 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RINT2C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RINT2C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT2C[31:0]	H'00000000	R/W	RINT2 (Frame Receive Error) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.39 RINT3 Count Register (CXR52)

CXR52 is a register with which the RINT3 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RINT3C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RINT3C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT3C[31:0]	H'00000000	R/W	RINT3 (Frame Length Error: less than 64 bytes) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.40 RINT4 Count Register (CXR53)

CXR53 is a register with which the RINT4 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RINT4C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RINT4C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT4C[31:0]	H'00000000	R/W	RINT4 (Frame Length Error: 1518 bytes or more) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.41 RINT5 Count Register (CXR54)

CXR54 is a register with which the RINT5 source signal count value can be read and refer to.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RINT5C[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

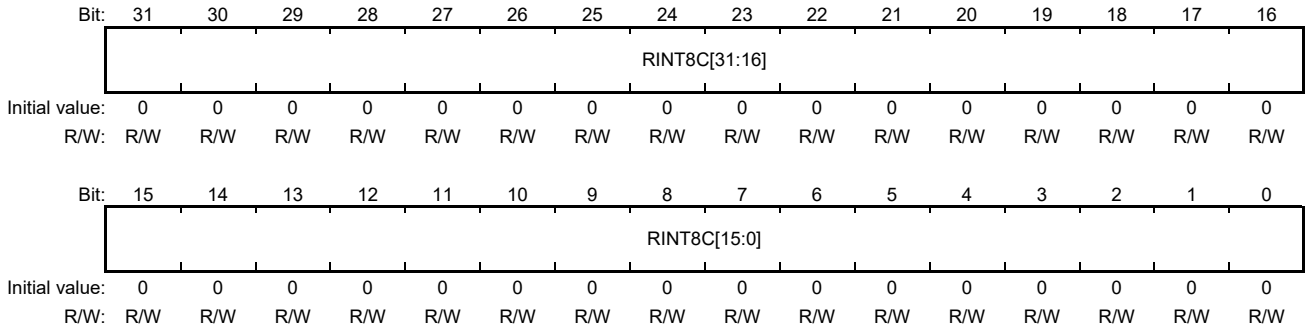
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RINT5C[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT5C[31:0]	H'00000000	R/W	RINT5 (Fractional Number Bit Error) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.4.42 RINT8 Count Register (CXR55)

CXR55 is a register with which the RINT8 source signal count value can be read and refer to.



Bit	Bit Name	Initial Value*	R/W	Description
31 to 0	RINT8C[31:0]	H'00000000	R/W	RINT8 (Multicast Frame Reception) Counter This counter is not automatically updated after incremented to H'FFFFFFFF. To update the counter continuously and restart increment from H'00000000, write-access to the counter and clear it. Note: Cleared by write access.

Note: * This register is initialized by an HDMAC/feLic software reset.

33.5 Data Format

33.5.1 Ethernet Packet

(1) Transmit Packet

Figure 33.3 shows the data format of a transmit packet. Table 33.5 shows the field definition of a transmit packet.

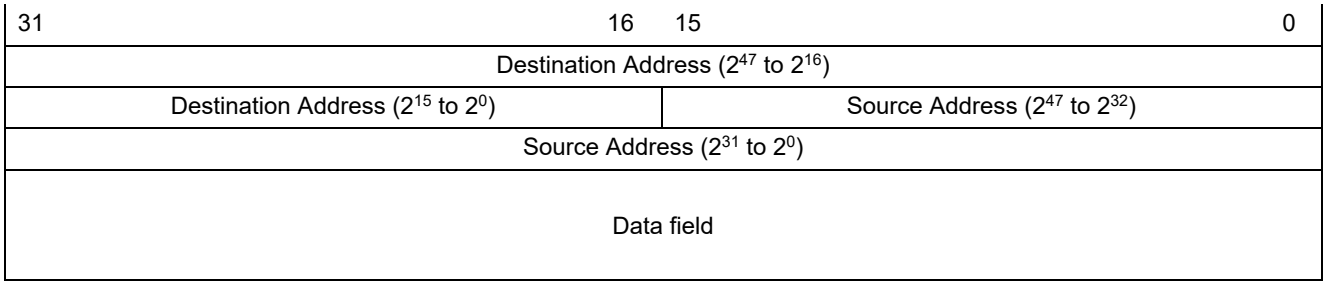


Figure 33.3 Data Format of a Transmit Packet

Table 33.5 Field Definition of a Transmit Packet

Field	Definition
Destination Address	See IEEE Std 802.3.
Source Address	See IEEE Std 802.3.
Data field	See IEEE Std 802.3.

(2) Receive Packet

Figure 33.4 shows the data format of a receive packet. Table 33.6 shows the field definition of a receive packet.

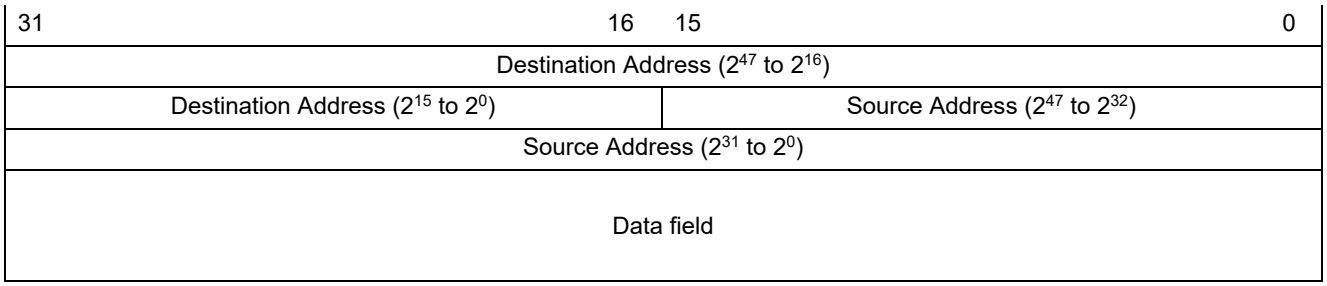


Figure 33.4 Data Format of a Receive Packet

Table 33.6 Field Definition of a Receive Packet

Field	Definition
Destination Address	See IEEE Std 802.3.
Source Address	See IEEE Std 802.3.
Data field	See IEEE Std 802.3.

33.6 Software Control Flow

33.6.1 Ether Software Control Flow

(1) Example of Ethernet Transmission and Reception Procedure

Figure 33.5 shows an example of initialization procedure for Ethernet transmission and reception. Figure 33.6 shows an example of Ethernet transmission and reception procedure.

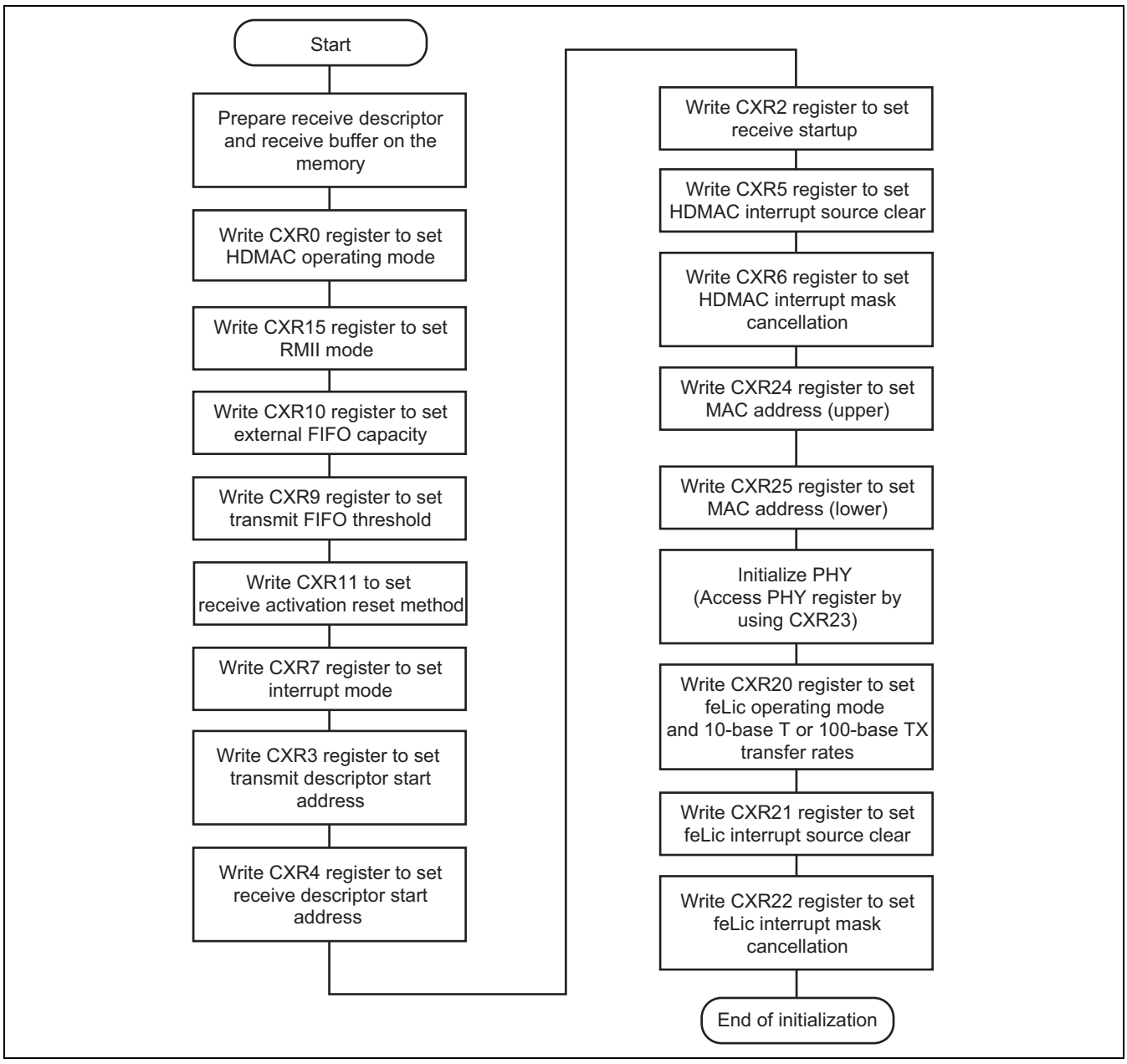


Figure 33.5 Initialization Procedure for Ethernet Transmission and Reception

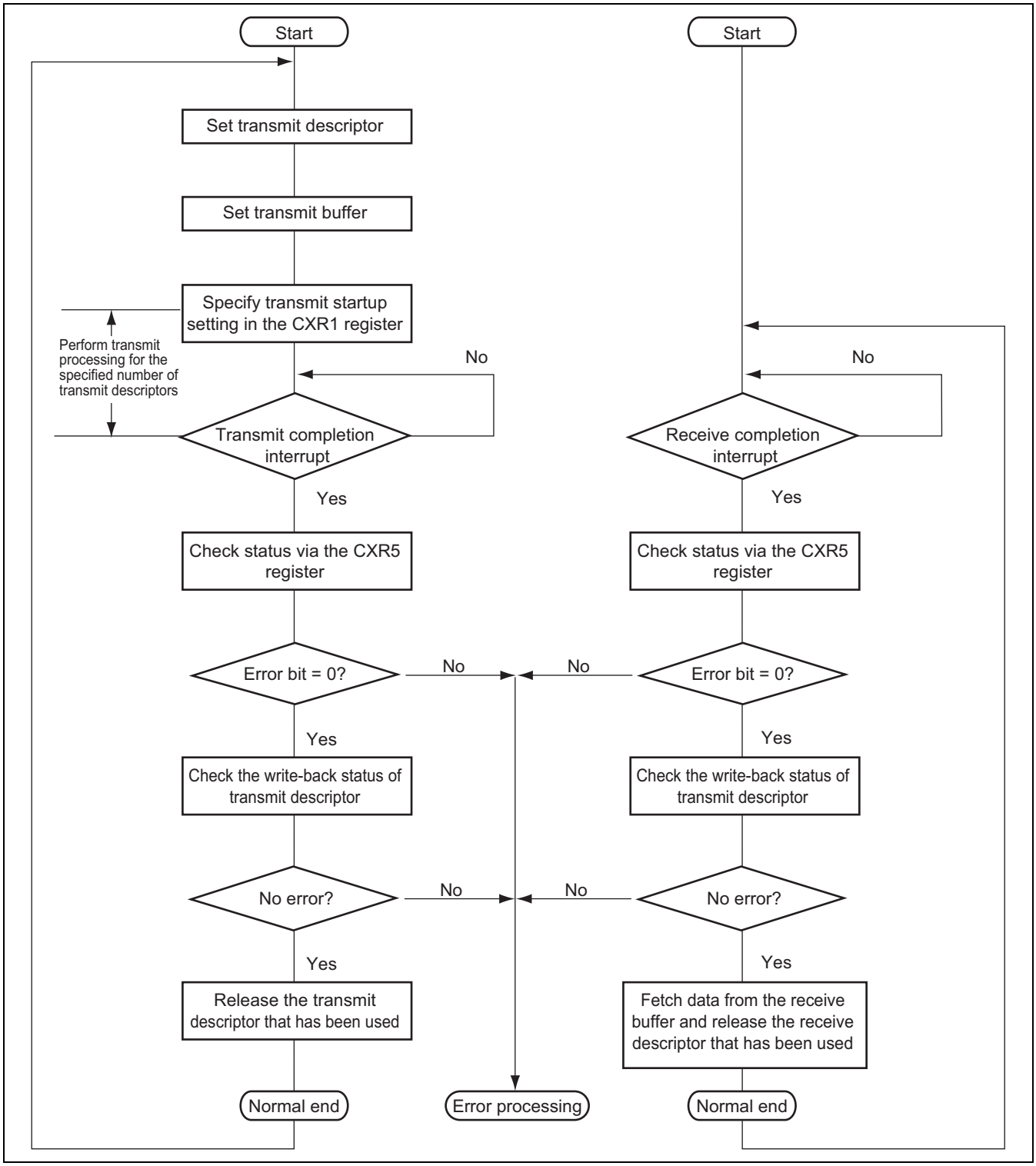


Figure 33.6 Ethernet Transmission and Reception Procedure

(2) Example of PHY Register Accessing Procedure

The PHY register is accessed by using the CXR23 register. This access should be performed using the MII management frame format as shown in Figure 33.7. Figure 33.8 shows an example of 1-bit data writing procedure to achieve the MII management frame. Figure 33.9 shows an example of bus releasing procedure. Figure 33.10 shows an example of 1-bit data reading procedure. Figure 33.11 shows an example of single bus releasing procedure.

Access Type	MII Management Frame							
Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Number of Bits	32	2	2	5	5	2	16	
Read	1..1	01	10	AAAAA	RRRRR	Z0	D....D	
Write	1..1	01	01	AAAAA	RRRRR	10	D....D	X

Legend:

PRE: 32 consecutive 1s

ST: Write B'01 to indicate the start of a frame

OP: Write a code to indicate an access type

PHYAD: Write B'00001 if a PHY-LSI address is 1 (write sequentially from MSB). The values of these bits change according to the PHY-LSI address.

REGAD: Write B'00001 when a register address is 1 (write sequentially from MSB). The value of these bits change according to the PHY-LSI address.

TA: Data transmit source switch time on the MII interface.
(a) Write B'10 during write
(b) Release bus (indicated as Z0) during read

DATA: 16-bit data. Written to or read sequentially from MSB.
(a) Write 16-bit data during write
(b) Read 16-bit data during read

IDLE: Wait time until next MII management format is input
(a) Release a single bus (indicated as X) during write
(b) Control not required because a bus has been released using the TA bits during read

Figure 33.7 MII Management Frame Format

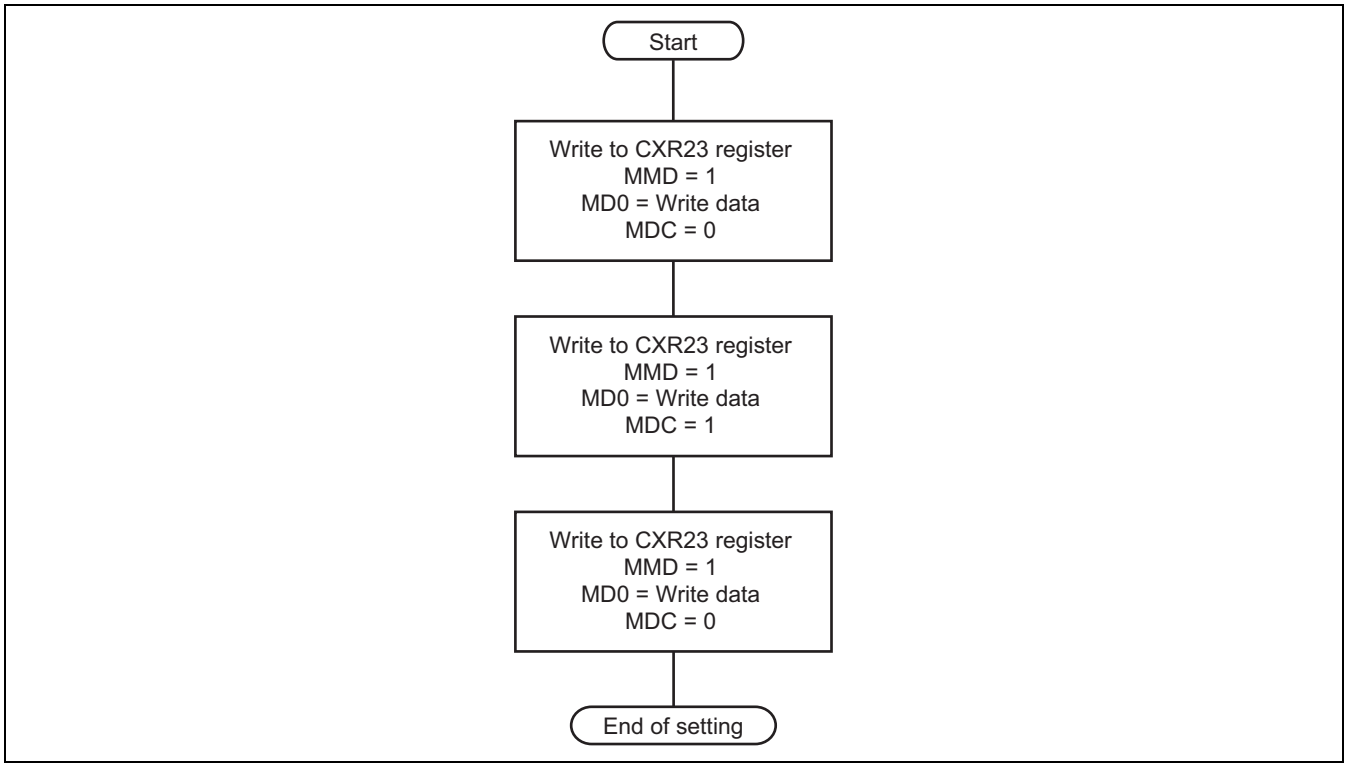


Figure 33.8 1-Bit Data Writing Procedure

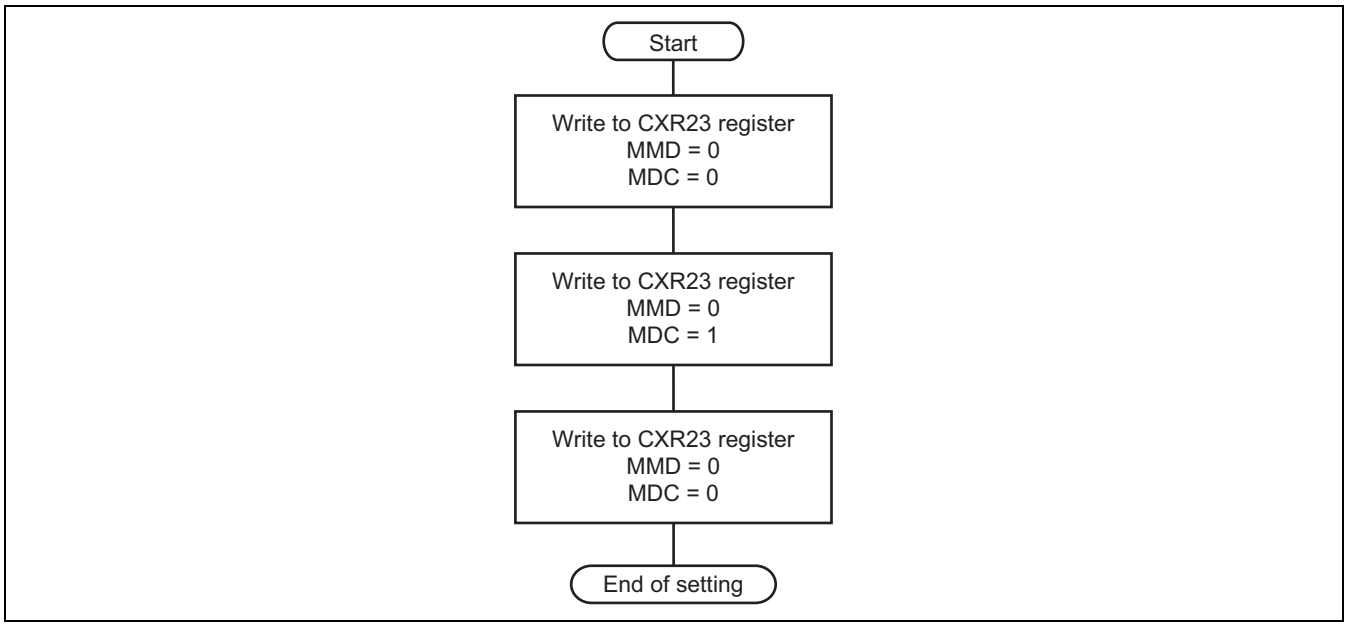


Figure 33.9 Bus Releasing Procedure

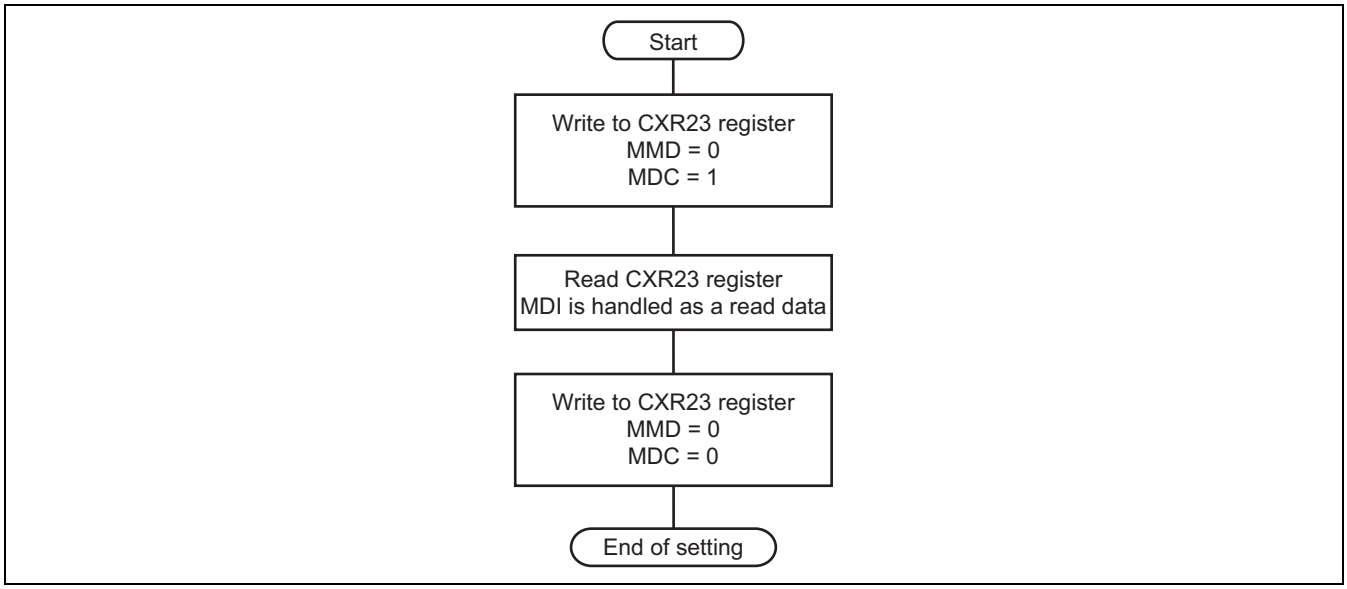


Figure 33.10 1-Bit Data Reading Procedure

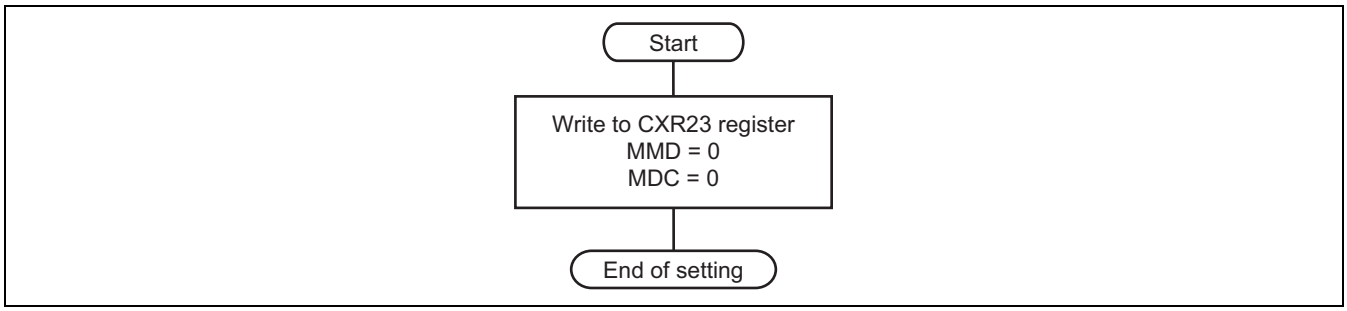


Figure 33.11 Single Bus Releasing Procedure

(3) Example of the Procedure for Setting 10-Base T or 100-Base TX Transfer Rates

An example of the procedure for setting 10-base T and 100-base TX transfer rates is given below. Follow this procedure when setting the transfer rate.

This section describes the procedure during operation. For the initial settings, follow the flow in subsection (1), Example of Ethernet Transmission and Reception Procedure, above.

1. Detecting the PHY chip link being down
   Use the CXR2B or CXR21 register to detect the PHY chip link being down.
2. On finding the linking from the PHY chip down
   On detecting the link from the PHY chip being down, proceed with processing for that situation in accord with the PHY chip specification.
3. Transfer Rate Settings
   Make settings on the feLic side as required by the state of the PHY chip. Use the OLB bit in the CXR20 register to set the transfer rate.

33.7 Notes

33.7.1 Software Reset

The ether can be software-reset by setting the SWR bit in the CXR0 register of the HDMAC to 1. If software reset is applied during DMA transfer, the current DMA transfer can be completed but the data transferred by DMA transfer cannot be guaranteed.

33.7.2 Standby

If the ether is requested to enter the standby state, the ether first completes the current AXI bus operation, and then enters the standby state. After returning from the standby state, the ether should be reset and initialized.

33.7.3 Input Signal on the ETH_RX_ER Pin

If an error signal received from PHY is not at the active level for more than one cycle of the RMII reference clock at 50 MHz, the signal is not detected as an error signal.

33.8 HDMAC Function Specifications

33.8.1 Operation

(1) Basic Operation

Figure 33.12 shows an image of control between this logic core (HDMAC) and device driver (software).

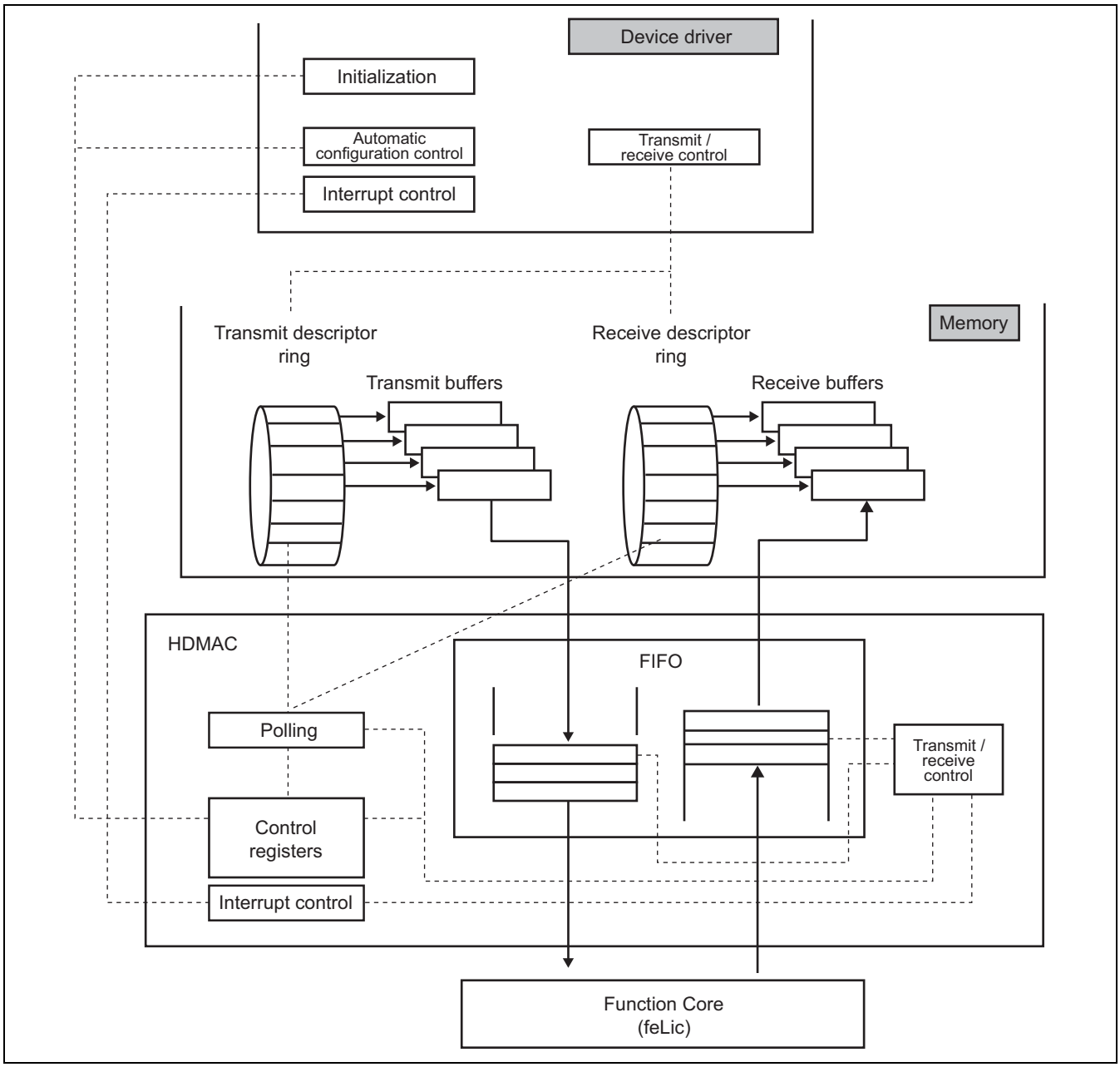


Figure 33.12 Image of Control between Device Driver and HDMAC

The device driver should create the transmit and receive descriptor rings and their corresponding transmit and receive buffers on the memory.

During transmission, this logic core fetches the transmit descriptor to obtain the transmit buffer address and the number of transmit bytes, and transmits data from the transmit buffer to the function core via the transmit FIFO. During reception, this logic core fetches the receive descriptor to obtain the receive buffer address and buffer size, and stores data received from the function core in the receive buffer via the receive FIFO.

(2) Descriptor Rings

There is no restriction on the number of descriptors. It is recommended, however, that multiple descriptors are provided.

This logic core uses the descriptor from the start descriptor to the last descriptor sequentially. If it reaches the last descriptor, it returns to use the start descriptor.

The start descriptor address is specified by the start address setting registers (CXR3 and CXR4). The last descriptor is specified by the descriptor ring end bits (TDL, RDL) = 1 in the descriptor. The descriptor boundary is specified by the descriptor length bits (DL) in the operating mode setting register (CXR0).

There is no restriction on the number of receive descriptors in terms of a ring configuration. Note that if only one receive descriptor is used, a receive descriptor depletion occurs when one frame has been received. (For details, refer to section 33.8.1 (8) (g), Receive Descriptor Depletion.)

For details on the descriptor description format, refer to section 33.8.2, Transmit Descriptors, and section 33.8.3, Receive Descriptors.

(3) Multiple Frames and Multiple Buffers

Multiple frames and multiple buffers enable consecutive frame transmission and reception.

In the receiver, a frame can be divided and stored in multiple buffers separately by specifying the frame in multiple descriptors.

In the transmitter, a frame is specified by a descriptor.

During transmission, after having transmitted data (frame) specified by a transmit descriptor, this logic core fetches the next descriptor. This logic core then determines that there is data (frame) to be transmitted next if the TACT bit in the fetched transmit descriptor is 1 and transmits the data (frame). If the TACT bit in the fetched transmit descriptor is 0, this logic core completes the transmit operation.

Note that bits 29 and 28 in the transmit descriptor TD0 should be set to 11. Otherwise, correct operation cannot be guaranteed.

During reception, after having received a frame, this logic core fetches the next receive descriptor. This logic core determines that the reception is ready if the RACT bit in the fetched receive descriptor is 1 and stores the received frame. If the RACT bit in the fetched receive descriptor is 0, this logic core determines that the receive descriptors have been depleted and completes the receive operation.

If this logic core receives a frame longer than the buffer length specified in the receive descriptor, it stores the frame up to the specified buffer length and then fetches the next receive descriptor. If this logic core further receives a frame longer than the buffer length specified in the fetched receive descriptor, it stores the frame up to the specified buffer length and then fetches the following descriptor. If this logic core receives a frame whose frame length is within the buffer size specified by the fetched receive descriptor, it stores the last byte of the frame and writes back the number of bytes so far stored in the receive buffer to the receive frame length (RFL) in the receive descriptor. The logic core then fetches the next descriptor to prepare for the next frame reception.

Note that correct operation cannot be guaranteed if the receive buffer length is specified as 0 in the receive descriptor.

(4) DMA Operation

(a) Burst Operation

This logic core accesses the descriptors and buffers in longword units via DMA transfer.

During descriptor (16 bytes as standard) fetch, 16-byte DMA transfer is performed per bus acquisition.

During transmit descriptor write back, 4-byte DMA transfer is performed per bus acquisition.

During receive descriptor write back, 8-byte DMA transfer is performed per bus acquisition.

During buffer data transfer, a maximum of 32-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 17 to 32 bytes, 32-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 9 to 16 bytes, 16-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 5 to 8 bytes, 8-byte DMA transfer is performed per bus acquisition.

If the remaining data in a frame to be transferred is 1 to 4 bytes, 4-byte DMA transfer is performed per bus acquisition.

(b) DMA Operation Error Report

If a DMA error is detected during DMA operation, the BER bit in the status register (CXR5) is set to 1 to generate an interrupt. After interrupt, DMA operation should be restarted by a reset (system reset or software reset).

(5) Transmit and Receive Buffers

A transmit buffer address and transmit buffer length to be specified by a transmit descriptor can be set in byte units. However, if 1 to 16 bytes is specified as the transmit buffer length, the transmit buffer address should be aligned on a 32-byte boundary. Note that correct operation cannot be guaranteed if 0 byte is specified as the transfer buffer length.

A receive buffer address to be specified by a receive descriptor should be aligned on a 32-byte boundary to prevent the DMA burst operation from being performed beyond SDRAM boundary.

In addition, if the number of data bytes remaining in a frame to be transferred cannot be divided by DMA burst bytes (32 bytes), the receive buffer length to be specified by the receive descriptor should be specified on a 32-byte boundary since extra data is transmitted.

For example, if the number of last data bytes remaining in a receive frame is 17 bytes, invalid data is written in the 18th to 32nd bytes in the corresponding address of the receive buffer since 32-byte DMA burst transfer is performed.

(6) Endian

Endian conversion can be used for the data arrangement in the transmit and receive buffers according to the DE bit setting in the operating mode setting register (CXR0).

Note that only the endian of the data in the transmit and receive buffers can be changed. Endian of descriptors and registers cannot be changed.

Note: Be sure to set DE bit to 1 before operating the Ethernet MAC controller (Ether).

(7) Transmit Operation

(a) Normal Transmit Operation

This logic core starts the transmit processing when 1 is written to the TRNS bit in the transmit activation register (CXR1).

This logic core fetches a descriptor next to the previous descriptor from the transmit descriptor ring.

If the TACT bit in the fetched transmit descriptor is 1, data in the transmit buffer is read out and written in the transmit FIFO sequentially according to the specified transmit buffer address and the number of bytes.

If the TACT bit in the fetched transmit descriptor is 0, the TRNS bit in the transmit activation register (CXR1) is cleared to 0 and transmit processing is completed without any operation.

When data of the buffer length indicated by the descriptor has been transmitted to the function core via the transmit FIFO (normally completed or aborted), the transmit descriptor is written back to, and the next descriptor is fetched.

While the TACT bit in the fetched transmit descriptor is 1, the transmit descriptor fetch and DMA transfer are performed continuously.

If the TACT bit in the fetched transmit descriptor is 0, the FTC bit in the status register (CXR5) is set to 1 to indicate the completion of transmission thus requesting an interrupt to the CPU, and simultaneously the TRNS bit in the transmit activation register (CXR1) is cleared to 0 to stop transmit processing.

If data in the transmit FIFO exceeds the threshold (changes according to the register setting), if data of a frame has been stored, or if the transmit FIFO becomes full, the function core is activated and data in the transmit FIFO is transmitted to the function core synchronously with the RDY signal in the function core.

When a transmit completion signal or abort signal is input from the function core, the above transmit operation is ended.

(b) Continuous Frame Transmit Operation

Multiple frames can be specified in a transmit descriptor.

This logic core clears the TACT bit in the transmit descriptor to 0 when data transmission indicated in the transmit descriptor has been completed, and fetches the next transmit descriptor. While the TACT bit in the fetched descriptor is 1, the frame transmission is performed continuously. When the TACT bit in the transmit descriptor is 0, the FTC bit in the status register (CXR5) is set to 1 to indicate the transmission completion thus requesting an interrupt to the CPU, and the TRNS bit in the transmit activation register (CXR1) is cleared to 0 to stop transmit processing.

Generation of a transmit completion interrupt (the FTC bit in CXR1 is set to 1) informs the CPU that all the specified frames have been transmitted.

(c) Transmit Abort

If this logic core receives an abort signal (ATABT) from the function core during frame transmission, it aborts data transmission of the corresponding frame from transmit FIFO to the function core.

When the transmission is aborted, this logic core clears the TACT bit in the transmit descriptor to 0, sets bit 8 in the transmit frame status (TFS) to 1.

The following operations are the same as (1) Normal Transmit Operation or (2) Continuous Frame Transmit Operation described above.

When detected the TACT bit in the fetched transmit descriptor is 0, the FTC bit in the status register (CXR5) is set to 1 to indicate the transmission completion, and TABT bit is also set to 1 to indicate the transmission abort to requesting an interrupt to the CPU.

(d) Transmit FIFO Underflow

This logic core does not transmit data to the function core until data in the transmit FIFO exceeds the specified threshold (changes according to the register setting), data of a frame is stored in the transmit FIFO, or the transmit FIFO becomes full to prevent the transmit FIFO from underflow.

An underflow will occur if the transmit FIFO becomes empty (there is no data to be transmitted) because the bus mastership cannot be obtained.

In this case, the TFE bit in the status register (CXR5) is set to 1 to indicate transmit FIFO underflow and an interrupt is requested to the CPU.

The frame where an underflow occurred is transmitted to the function core in the same way as the normal frame. After the frame transmission, the TACT bit in the transmit descriptor is cleared to 0 and transmit frame status (TFS) is set to 1. The following operations are the same as (1) Normal Transmit Operation or (2) Continuous Frame Transmit Operation described above.

(e) Transmit Frame Retry

If this logic core receives an ATRTRY signal from the function core after having transmitted the last byte of a frame to the function core, this logic core fetches the start descriptor of the current frame again, and re-transmits the data of the current frame from the start to last bytes to the transmit FIFO.

(8) Receive Operation

(a) Normal Receive Operation

This logic core starts receive processing when 1 is written to the R bit in the receive activation register (CXR2).

This logic core fetches the receive descriptor (Nth receive descriptor) next to the previous receive descriptor ((N – 1)th receive descriptor) from the receive descriptor ring, and enters the receive wait state.

In the receive wait state, if the receive FIFO contains data of 32 bytes or more or the last byte, data is transferred from the receive FIFO to the receive buffer.

When the receive buffer specified by the receive descriptor becomes full, this logic core writes 0 to the RACT bit in the receive descriptor and fetches the (N + 1)th receive descriptor. If the RACT bit in the (N + 1)th receive descriptor is 1, this logic core enters the receive wait state again.

If the last byte of a frame has been transferred, this logic core writes 0 and 1 in the RACT bit and the RFP[0] bit in the receive descriptor, respectively, sets the FRC bit in the status register (CXR5) to 1 to indicate the completion of frame reception, requests an interrupt to the CPU, and finally fetches the (N + 2)th receive descriptor.

If the RACT bit in the (N + 2)th receive descriptor is 1, this logic core enters the receive wait state. Contrarily, if the RACT bit in the (N + 2)th receive descriptor is 0, a receive descriptor depletion occurs. (For details, refer to section 33.8.1 (8) (g), Receive Descriptor Depletion.)

(b) Continuous Frame Receive Operation

As described in (1) Normal Receive Operation, when a frame has been received and the last byte of the frame has been transferred, this logic core writes 0 and 1 in the RACT bit and RFP[0] bit in the Nth receive descriptor, respectively, sets the FRC bit in the status register (CXR5) to 1 to indicate the completion of frame reception, generates an interrupt to the CPU, fetches the (N + 1)th receive descriptor, and enters the receive wait state.

When the last byte in the (N + 1)th receive descriptor has been transferred, this logic core writes 0 and 1 in the RACT bit and RFP[0] bit in the (N + 1)th receive descriptor, respectively, sets the FRC bit in the status register (CXR5) to 1 to indicate the completion of frame reception, generates an interrupt to the CPU, fetches the (N + 2)th receive descriptor, and enters the receive wait state.

This logic core then receives frames continuously until the RACT bit in the fetched descriptor is cleared to 0 (a receive descriptor depletion occurs).

(c) Receive Operation of Multiple Frames and Multiple Buffers

If the byte count of the received Mth frame is greater than the buffer length specified by the Nth receive descriptor, this logic core transfers data of the specified receive buffer length and then writes 0s in the RACT bit and RFP[0] bit in the Nth receive descriptor and fetches the (N + 1)th receive descriptor.

With the (N + 1)th receive descriptor, this logic core performs the data transfer of the same frame (Mth frame). If the byte count of the received Mth frame is greater than the buffer length specified by the (N + 1)th receive descriptor, this logic core transfers data of the specified receive buffer length and writes 0s in the RACT bit and RFP[0] bit in the (N + 1)th receive descriptor and fetches the (N + 2)th receive descriptor as described above. Contrarily, if the byte count of the received Mth frame is smaller than the buffer length specified by the (N + 1)th receive descriptor, this logic core, after having transferred the last byte, writes 0 and 1 in the RACT bit and RFP[0] bit in the (N + 1)th receive descriptor, sets the FRC bit in the status register (CRX5) to 1 to indicate the completion of frame reception, generates an interrupt to the CPU, fetches the (N + 2)th receive descriptor, and enters the receive wait state, as described in (1) Normal Receive Operation.

(d) Receive Abort

If this logic core receives a receive abort (ARABT) signal from the function core during frame reception, it aborts reception of the corresponding frame data from the function core.

This logic core transfers data stored in the receive FIFO before receive abortion to the receive buffer. When the last byte has been transferred, this logic core clears the RACT bit in the receive descriptor to 0, sets bit 8 of receive frame status in the receive descriptor to 1, sets the FRC and RABT bits in the status register (CRX5) to 1s to indicate the frame transmission completion and receive abort detection, respectively, and finally generates an interrupt to the CPU.

If this logic core receives an ARABT signal from the function core while the number of data bytes of the stored frame in the receive FIFO is less than 16 bytes, this logic core deletes the corresponding frame.

(e) Receive FIFO Overflow

If the receive FIFO becomes full because the bus mastership cannot be obtained, an overflow error occurs because the next data cannot be stored in the receive FIFO.

If an overflow error occurs, the receive FIFO terminates the data reception and sets the RFE bit in the status register (CXR5) to 1 to indicate the receive FIFO overflow, and generates an interrupt to the CPU. When the transfer of the byte immediately before the overflow has been completed, this logic core writes 0 and 1 to the RACT bit and bit 9 of receive frame status (RFS) in the receive descriptor, respectively, sets the FRC and RFE bits in the status register (CXR5) to 1s to indicate the frame reception completion and receive FIFO overflow, respectively, and finally generates an interrupt to the CPU.

While the receive FIFO is full, the next frame is received but discarded. Simultaneously, the discarded frame counter register (CXR8) is incremented.

If the receive FIFO becomes not full after data has been transferred from the receive FIFO to the receive buffer, this logic core restarts the reception from the start byte of the next receive frame.

The number of frames that can be simultaneously stored in the receive FIFO is limited to 16 frames due to the frame management restriction. Accordingly, this logic core cannot receive a frame if 16 frames have been stored in the receive FIFO. If this logic core receives the start data of the 17th frame, it sets the RFRMER bit in the status register (CXR5) to 1 to indicate the receive frame count overflow, and generates an interrupt to the CPU.

This logic core receives the next frame but discards it, and simultaneously increments the discarded frame counter register (CXR8).

If a space of 1 frame or more is produced in the receive FIFO after data has been transferred from the receive FIFO to the receive buffer, this logic core restarts the reception from the start byte of the next receive frame.

(f) Flow Control Support

This function core provides an ARBSY signal to inform the function core of the receive FIFO status. It can output the ARBSY signal based on the data amount stored in the receive FIFO according to the setting of the receive FIFO busy transmit threshold setting register (CXR16).

Accordingly, the flow can be controlled by sending "BUSY" to the function core before the receive FIFO overflows.

The BUSY status can be cancelled when the data byte count or the frame count in the receive FIFO become (the byte count value causing a transition to the BUSY state − 32 bytes) or smaller and (the frame count value causing a transition to the BUSY state − 1 frame) or smaller, respectively.

(g) Receive Descriptor Depletion

When this logic core has transferred data of the Mth frame to the receive buffer specified by the Nth receive descriptor, it fetches the (N + 1)th receive descriptor to prepare for the reception of the (M + 1)th frame.

If the RACT bit of the fetched descriptor ((N + 1)th descriptor) is 0, this logic core regards it as receive descriptor depletion, sets the RDE bit in the status register (CXR5) to 1 to indicate the receive descriptor depletion, and generates an interrupt to the CPU.

Simultaneously, this logic core clears the R bit in the receive activation register (CXR2) to 0 and terminates the receive processing. In this case, data transfer from the function core to the receive FIFO continues.

In this situation, the CPU should clear the interrupt source and reset the receive descriptor correctly.

If the valid receive descriptor is set before a receive FIFO overflow occurs, a frame reception can be continued without data loss.

33.8.2 Transmit Descriptors

Figure 33.13 shows a transmit descriptor format.

If 1 to 16 bytes is specified as the transmit buffer length, the transmit buffer address should be aligned on a 32-byte boundary. Note that correct operation cannot be guaranteed if 0 byte is specified as the transfer buffer length.

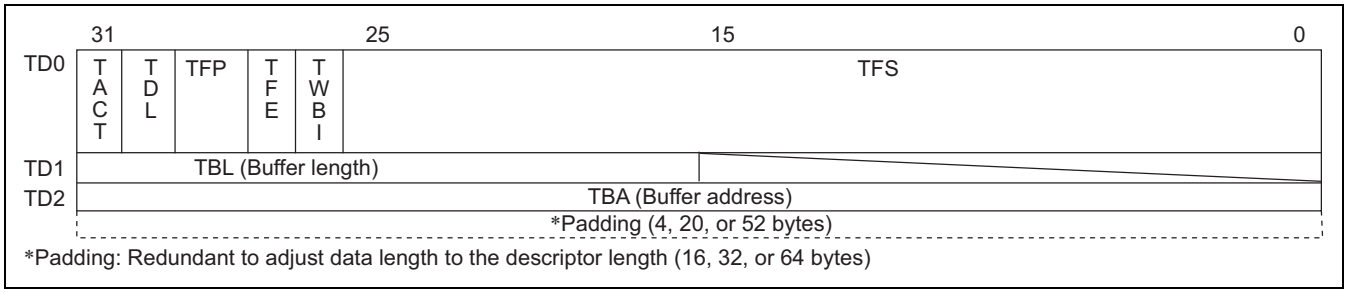


Figure 33.13 Transmit Descriptor Format

(1) Transmit Descriptor 0 (TD0)

Table 33.7 shows a definition of transmit descriptor 0. (A bit to be written back to is underlined.)

Table 33.7 Definition of Transmit Descriptor 0

Bit	Bit Name	Initial Value	R/W	Definition
31	TACT	Undefined	R/W	Descriptor Valid Indicates that the corresponding descriptor is valid. This bit is set to 1 by a driver, and reset (cleared to 0) by this logic core when a frame transmission has been completed or a frame transmission has been aborted for some reason.
30	TDL	Undefined	R/W	Descriptor Ring End Set to 1 to indicate that the corresponding descriptor is an end of the transmit descriptor ring.
29, 28	TFP	Undefined	R/W	Position in a Frame 11: Indicate that the information in this descriptor includes one whole frame. This field should be set to 11.
27	TFE	Undefined	R/W	Transmit Frame Error Set to 1 to indicate that an error occurs in TFS.
26	TWBI	Undefined	R/W	Write-Back Completion Interrupt Request (Enabled according to CXR18 settings) 0: nop 1: Requests an interrupt after a write-back to this descriptor has been completed.
25 to 0	TFS	Undefined	R/W	Transmit Frame Status Bit 8: Set to 1 to indicate that the underflow occurs shown as an abort signal is set to 1 during transmission of the frame, (TFE set source). Bits 7 to 0: Set to 1 to indicate that a corresponding bit among TINT8 to TINT1 is set to 1.

(2) Transmit Descriptor 1 (TD1)

Table 33.8 shows a definition of transmit descriptor 1.

Table 33.8 Definition of Transmit Descriptor 1

Bit	Bit Name	Initial Value	R/W	Definition
31 to 16	TBL	Undefined	R/W	Buffer length: Indicates the valid byte count in the target transmit buffer.
15 to 0	—	Undefined	R/W	Reserved

(3) Transmit Descriptor 2 (TD2)

Table 33.9 shows a definition of transmit descriptor 2.

Table 33.9 Definition of Transmit Descriptor 2

Bit	Bit Name	Initial Value	R/W	Definition
31 to 0	TBA	Undefined	R/W	Buffer address: Indicates the start address of the transmit buffer.

33.8.3 Receive Descriptors

Figure 33.14 shows a receive descriptor format.

A receive buffer address specified by a receive descriptor should be aligned on a 32-byte boundary. Note that correct operation cannot be guaranteed if 0 byte is specified as the receive buffer length (RBL).

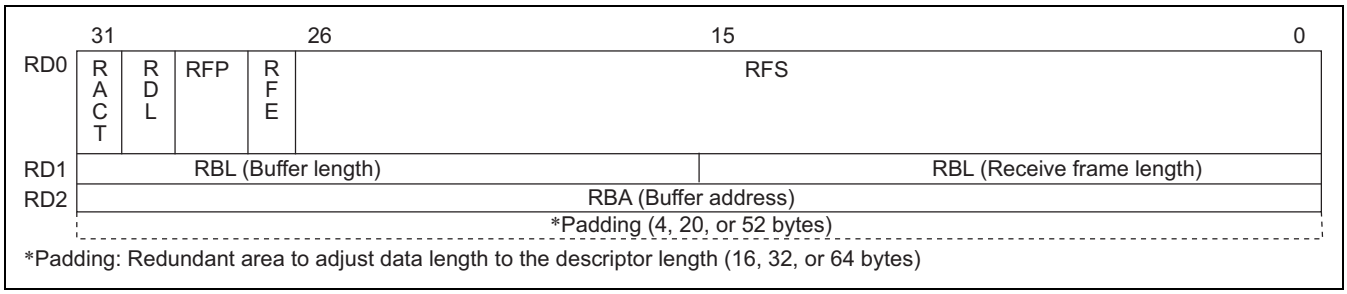


Figure 33.14 Receive Descriptor Format

(1) Receive Descriptor 0 (RD0)

Table 33.10 shows a definition of receive descriptor 0. (A bit to be written back to is underlined.)

Table 33.10 Definition of Receive Descriptor 0

Bit	Bit Name	Initial Value	R/W	Definition
31	RACT	Undefined	R/W	Descriptor Valid Indicates that the corresponding descriptor is valid. This bit is set to 1 by a driver, and reset (cleared to 0) by this logic core when a frame transmission has been completed or the receive buffers have become full.
30	RDL	Undefined	R/W	Descriptor Ring End Set to 1 to indicate that the corresponding descriptor is an end of the receive descriptor ring.
29, 28	RFP	Undefined	R/W	Position in a Frame 10: Indicate that the information in this descriptor includes the start of a frame. 11: Indicate that the information in this descriptor includes one whole frame. 01: indicate that the information in this descriptor includes the end of a frame. 00: Indicate that the information in this descriptor is other than above.
27	RFE	Undefined	R/W	Receive Frame Error Set to 1 to indicate that an error occurs in RFS.
26 to 0	RFS	Undefined	R/W	Receive Frame Status Bit 9: Set to 1 to indicate that an aborted frame is written back due to a receive FIFO overflow (FRE setting source). Bit 8: Set to 1 to indicate that an abort signal is set to 1 during frame reception (RFE set source). Bits 7 to 0: Set to 1 to indicate that a corresponding bit among RINT8 to TINT1 is set to 1 (RFE setting sources specified by CXR7).

(2) Receive Descriptor 1 (RD1)

Table 33.11 shows a definition of receive descriptor 1. (A bit to be written back to is underlined.)

Table 33.11 Definition of Receive Descriptor 1

Bit	Bit Name	Initial Value	R/W	Definition
31 to 16	RBL	Undefined	R/W	Buffer length Indicate the byte count in the target receive buffer. The buffer length should be specified by 32 bytes x n.
15 to 0	RFL	Undefined	R/W	Receive Frame Length Indicate the receive frame length (bytes) stores in the receive buffer. This receive frame length does not include the number of bytes for padding specified in the CXRS5. This receive frame length is written back in the receive descriptor that includes the last of a frame.

(3) Receive Descriptor 1 (RD2)

Table 33.12 shows a definition of receive descriptor 2.

Table 33.12 Definition of Receive Descriptor 2

Bit	Bit Name	Initial Value	R/W	Definition
31 to 0	RBA	Undefined	R/W	Buffer Address These bits indicate the start address of a receive buffer. The buffer address should be aligned on a 32-byte boundary.

33.8.4 Error Detection and Report

The error sources are classified into two types: those detected by the HDMAC and those detected and reported by the feLic.

Each error is described below. If an error is detected, the detected error is indicated in the status register (CXR5) and an interrupt signal is output.

(1) Error Sources Detected by the HDMAC

(a) Descriptor Depletion

If no descriptor whose descriptor valid bit is set can be detected during frame reception, a receive descriptor depletion error occurs and the R bit in the receive activation register (CXR2) is reset to complete the receive processing.

(b) External FIFO Underflow/Overflow

If a transmit FIFO becomes empty during frame transmission, an underflow error occurs because there is no data to be transmitted.

If a receive FIFO becomes full during frame reception, an overflow error occurs because the next receive data cannot be stored in the receive FIFO.

If an underflow error in a transmit FIFO or an overflow error in a receive FIFO is detected, it is indicated in the status register (CXR5).

(2) Error Sources Detected and Reported by the Function Core (feLic)

(a) Transmit Interrupt

Interrupt sources detected by the function core (feLic) during frame transmission are reported to the transmit descriptor of the corresponding frame and status register (CXR5) as TINT1 to TINT8, or transmit abort detect (TABT).

(b) Receive Interrupt

Interrupt sources detected by the function core (feLic) during frame reception are reported to the receive descriptor of the corresponding frame and status register (CXR5) as RINT1 to RINT8, and receive abort detect (RABT).

(c) MPORT Interrupt (MINT)

If an error is detected other than during transmission or reception, it is reported as an MPORT interrupt.

For details on TINT, RINT, and MINT bits, see the Function Core Function Specifications.

(3) Error Log Information

This logic core provides the following log collection registers.

1. Discarded frame counter register (CXR8)
2. Transmit FIFO underflow counter register (CXR13)
3. Receive FIFO overflow counter register (CXR14)

33.8.5 Firmware/Software Interface

(1) Interrupts

Interrupts sources in this logic module are as follows.

1. RINT1 to RINT8
2. TINT1 to TINT8
3. Receive FIFO overflow
4. Receive descriptor depletion
5. Frame receive completion
6. Transmit FIFO underflow
7. Transmit descriptor depletion (not used)
8. Frame transmit completion
9. M port interrupt
10. DMA error
11. Receive frame count overflow
12. Receive abort detection
13. Transmit abort detection
14. External EXIN signal assertion detection (not used)
15. Transmit descriptor write-back

The above interrupt sources are indicated in the status register (CXR5). An interrupt source (other than M port interrupt signal (MINT) bit) can be reset by writing 1 to the corresponding bit in the CXR5 register. An M port interrupt signal (MINT) can be reset by resetting the corresponding source in the function core. The above interrupt sources can be separately masked by setting the interrupt mask register (CXR6).

33.9 feLic Function Specifications

33.9.1 Configuration

Figure 33.15 shows a block diagram of feLic.

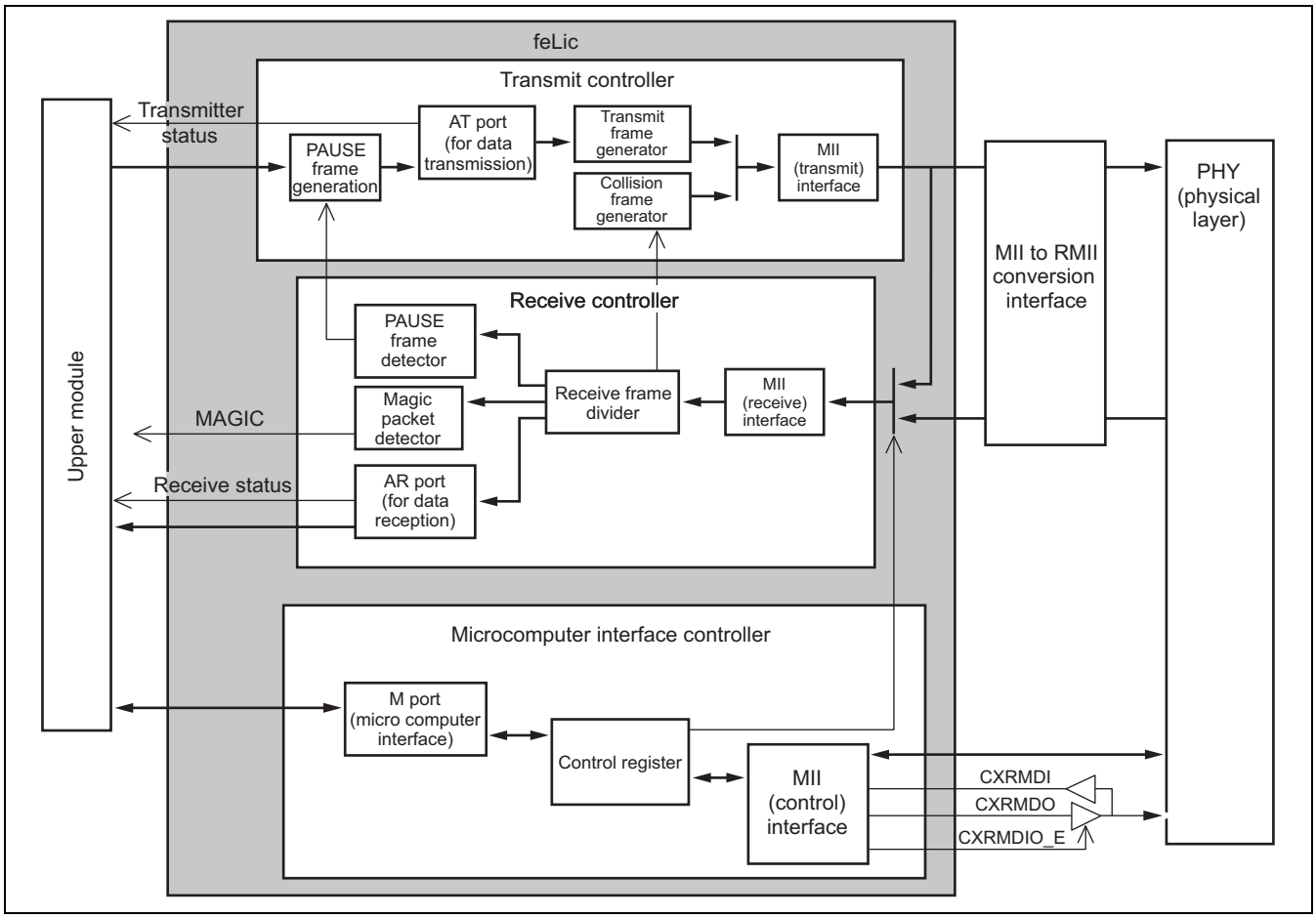


Figure 33.15 feLic Block Diagram

33.9.2 feLic Function

(1) Transmit Controller

The transmit controller assembles data received from AT port into the IEEE802.3 format frames, and transmits them via the MII interface.

The main functions of the transmit controller are listed below.

1. Assembles data received from the AT port into the IEEE802.3 format frames and transmits them.
2. Performs CRC calculation and adds it to the frame.
3. Retransmits frames (up to 15 times) when a collision occurs.
4. Provides the MII interface function conforming to the IEEE802.3u.
5. Performs serial and parallel conversion according to the PHY chip speed.
6. Provides transmit frame data padding function.
7. Generates a PAUSE frame.

(2) Receive Controller

Upon receiving a frame via the MII interface, the receive controller checks the frame address to see if the address matches the self-node; it also checks CRC and the frame length of the data and transfers the data to the AR port.

The main functions of the receive controller are listed below.

1. Checks the format of the received frame header.
2. Checks the CRC and frame length of the received frame data.
3. Transfers frames addressed to itself, multicast frames, and broadcast frames to the AR port.
4. Provides the MII interface function conforming to the IEEE802.3u.
5. Performs serial and parallel conversion according to the PHY chip speed.
6. Monitors a magic packet.
7. Analyzes a PAUSE frame.

(3) Microcomputer Interface Controller

The microcomputer interface controller incorporates a function to interface to the upper microprocessor. The data width of the M port is 32 bits. The M port operates synchronously with the external clock. The upper microprocessor controls the registers in this microcomputer interface controller block and the registers in PHY via the MII interface.

The main functions of the microcomputer interface controller are listed below.

1. Controls the operation of transmitter and receiver.
2. Accesses the PHY registers via the serial bus.

(4) Magic Packet Monitor Function

The receive controller monitors the magic packet and report the magic packet detection to an external device in magic packet monitor mode. This function becomes effective by the MPM bit in the CXR20 register. When the magic packet is detected, "ETH_MAGIC" signal that is an output is asserted and the CXR21 register is updated. Their detecting functions are explained as follows.

(a) Assertion by the ETH_MAGIC signal

ETH_MAGIC signal that is an output signal of the feLic is asserted synchronizing with the rising edge of the received clock from PHY. Detection of the magic packet can be informed to external circuits by using this signal. The ETH_MAGIC signal is negated by the hardware reset and the software reset of the HDMAC/feLic using CXR0 register.

(b) Assertion by the CXR21 register

Updating CXR21 can assert as software interruption. The detecting information is cleared by writing a 1 to the corresponding bit. Note that if a magic packet is received again, CXR21 register is not updated while the ETH_MAGIC signal is asserting. Set the feLic again after clearing by the procedure described (1).

(5) Transmit and Receive Status Statistical Function

The interrupt source signals (TINT/RINT) to be output to the upper modules can be counted and referenced as statistical information by accessing a register via the M port.

The interrupt source signal counting starts after reset (includes a soft reset by CXR0 register) and the count value can be cleared only by a write access.

(6) Flow Control Conforming to IEEE802.3

As the flow control during full-duplex operation, the flow control conforming to IEEE802.3x is supported. Transmission of a PAUSE frame used in flow control is performed in the following methods. These methods can be used by mutually combining.

(a) Automatic PAUSE Frame Transmission

A PAUSE frame is transmitted automatically by asserting the ARBSY signal. Note that as the Timer value included in the PAUSE frame, the value set in the automatic PAUSE parameter setting register (see CXR71) is used. If the ARBSY signal is not negated when the time indicated by the Timer value has passed after transmitting a PAUSE frame, a PAUSE frame is transmitted again. The number of PAUSE frame re-transmissions (upper limit) can be specified from 1 to 65535 times by setting the PAUSE frame retransmit count setting register (CXR81). If the number of PAUSE frame re-transmissions reaches the upper limit, the following PAUSE frame re-transmissions will not be performed.

Transmission can be restarted when ARBSY signal is negated once and then asserted again thus resetting the PAUSE frame re-transmission counter (CXR82). In addition, it is possible not to set the upper limit of the re-transmissions (unlimited).

(b) Manual PAUSE Frame Transmission

This method can send the PAUSE frame by calling of software. Set the Timer value to the CXR72 register to sending the PAUSE frame. It is sent just one time (one frame) in this method.

(c) PAUSE Timer Value

For the PAUSE frame whose Timer value is 0, it is possible to enable or disable the PAUSE frame control.

- During transmission
  When control of a PAUSE frame whose Timer value is 0 is enabled, a PAUSE frame with Timer value 0 is transmitted if the ARBSY signal is negated before the time indicated by the Timer value has passed.
  When control of a PAUSE frame whose Timer value is 0 is disabled, the next frame will not be transmitted until the time indicated by the Timer value has passed.
- During reception
  When control of a PAUSE frame whose Timer value is 0 is enabled, a PAUSE frame is set in the receive wait counter even if the time indicated by Timer value is 0. (The receive wait state is cancelled.)
  When control of a PAUSE frame whose Timer value is 0 is disabled, the PAUSE frame is discarded if the time indicated by Timer value is 0.

(d) PAUSE Frame Reception

When a PAUSE frame is received, this logic function suspends transmission of the next frame until the time indicated by the Timer value has passed. However, transmission of the frame being transmitted continues. A number of the PAUSE frame receiving is counted to CXR80.

(7) Back-Pressure Flow Control

As the flow control during half-duplex operation, the back-pressure flow control is supported. This method generates a pseudo collision (transmits a collision frame) to stop the frame reception if the remaining space in the FIFO is not sufficient when the frame is received. This method does not refer to the DA.

33.9.3 Detailed Description of Transmit and Receive Controllers

(1) Transmit Controller

The transmit controller assembles the transmit data from the AT port into the frames based on the appropriate format and transmits them via the MII interface. Here, an error may occur according to the status of the communication lines. If an error of TINT1 to RINT8 occurs, the transmission is aborted and the error source is reported to the upper block using the abort signal (ARABT). If the transmission is completed normally, it is reported via the transmit completion signal (ATCOMP).

The conditions of generating each error source and operation are described below.

- TINT1: Transmit timeout
  When a collision occurs (the COL signal assertion) during frame transmission, the transmission is retried after the back-off time has passed. A transmit timeout is generated if a collision occurs again during the 15th transmission retry.
- TINT2: Collision detection during frame transmission
  Generated if a delay collision described in the IEEE802.3 standard occurs.
  Description in the standard: It is regarded as a delay collision if a collision occurs after the collision window at 512-bit time from the transmission start.
- TINT3: Carrier loss during frame transmission
  Generated when a carrier is lost (the CRS signal is negated) during frame transmission.
- TINT4: Carrier not detected
  Generated when a carrier is not detected (the CRS signal is not asserted) during preamble field transmission.
- TINT5: Not assigned
- TINT6: Not assigned
- TINT7: Not assigned
- TINT8: Not assigned

If any transmit error described above occurs, the feLic enters the wait state for the next frame transmission request and starts the next frame transmission when the next frame transmission is requested.

(2) Receive Controller

The receive controller transfers a frame received via the MII interface to the AR port. Here, an error may occur according to the status of the communication lines. If an error of RINT1 to RINT4 occurs, the reception is aborted and the error source is reported to the upper block using the abort signal (ARABT). RINT5 indicates that a fractional number bit error has occurred. Note, however, that a frame with an RINT5 error but with no CRC error can be received normally. A frame with RINT8 can also be received normally. RINT8 is an error source allowing normal frame reception and is reported by using the receive completion signal (ARCOMP) when the frame destination address is a multicast address.

The conditions of generating each error source and operation are described below.

- RINT1: CRC error
  Generated when an error is detected in the FCS field in the receive frame.
- RINT2: Frame receive error
  Reported when the RX_ER signal in the MII interface is asserted during frame reception. For details on the RX_ER signal assertion, see the Data Book of the PHY to be connected.
- RINT3: Frame length error
  Reported when the receive frame length is less than 64 bytes.
- RINT4: Frame length error
  Reported when the receive frame length exceeds the value specified in the CXR2A register. An excess of data field over the specified frame length is discarded in the feLic and will not be transferred to the upper block.

- RINT5: Fractional number bit error

  Reported when the received frame length is not the multiple of an octet. In this case, the last 1 to 4 octets in the data field will not be transferred to the upper block.
- RINT6: Not assigned
- RINT7: Not assigned
- RINT8: Multicast frame reception

  Reported when the frame destination address is a multicast address. This error source is reported with a receive completion signal only when other error source is not generated.

If any receive error described above occurs, the feLic enters the wait state for the next frame reception and starts the next frame reception when the next frame is received.

33.10 MII-RMII Interface Conversion

This LSI supports an RMII interface. The RMII signals are generated by converting the MII signals in the MII-RMII conversion circuit.

(1) Clock

ETH_REFCLK (50 MHz) from the RMII interface is divided and ET_TX-CLK/ET_RX-CLK (25 MHz or 2.5 MHz) is output.

(2) Reception

Waveforms received from the RMII interface are converted to MII waveforms and output (10 Mbps or 100 Mbps). Illegal carrier detection signal received from the RMII interface is converted to MII signal and output. ETH_RX_ER signal received from the RMII interface is converted to MII interface signal and output.

Note: Illegal carrier detection is not generated from preamble detection to reception completion.

(3) Transmission

Transmit waveforms from the MII interface is converted to the RMII interface waveforms and output (10 Mbps or 100 Mbps). The collision signal, ET_COL, is generated by AND operation of the ET_CRS and ET_TX-EN signals.

(4) Full-Duplex/Half-Duplex Selection

In full-duplex transfer mode, the assertion of the COL is suppressed. Figure 33.16 shows a schematic of the conversion circuit.

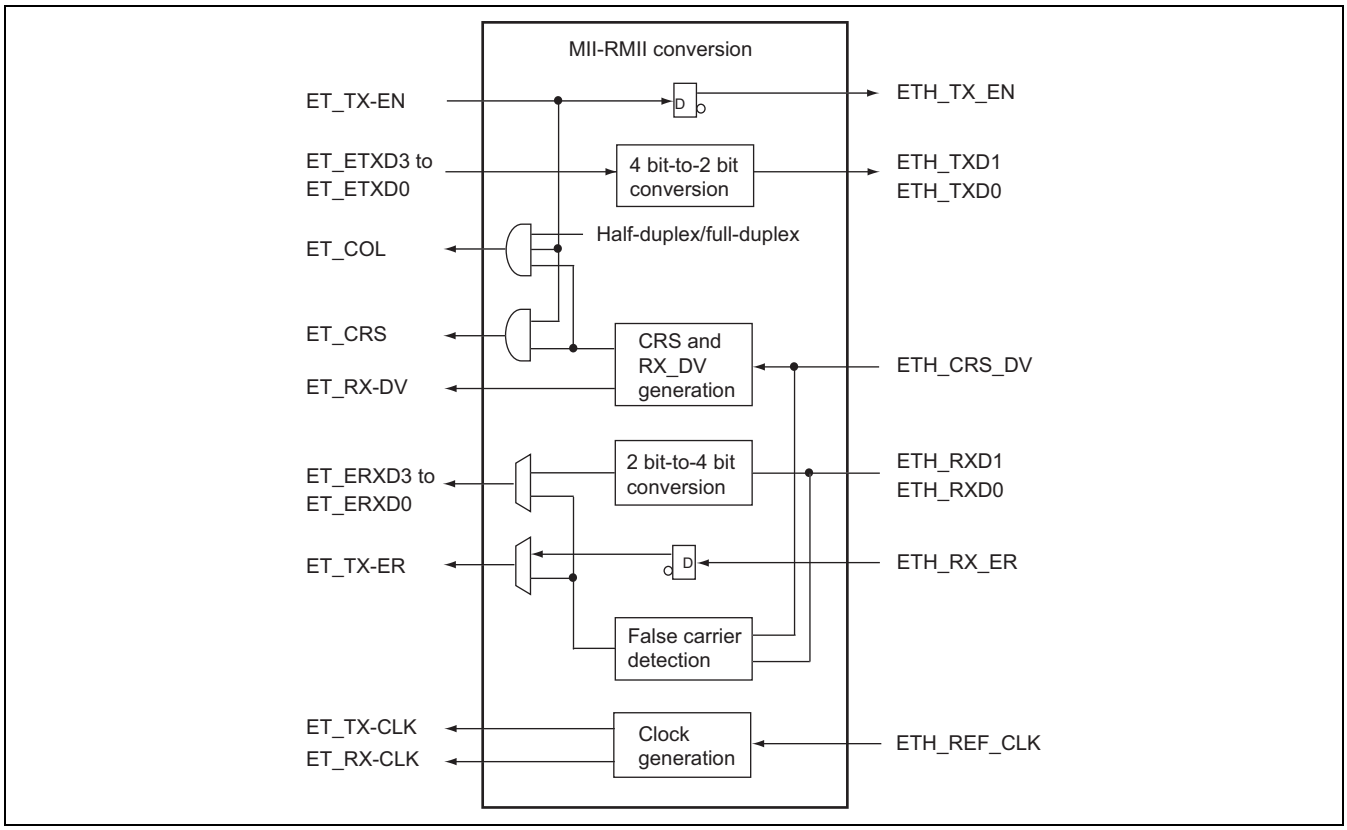


Figure 33.16 MII-RMII Conversion Circuit

33A. EthernetAVB

33A.1 Overview

The EthernetAVB includes an Ethernet controller (E-MAC) that conforms to the definition of the MAC (Media Access Control) layer for Ethernet in the IEEE 802.3 standard.

When connected with a physical-layer LSI chip (PHY-LSI) that complies with the standard, the E-MAC is able to transmit and receive Ethernet (IEEE 802.3) frames. The E-MAC has a single MAC layer interface.

The EthernetAVB has a dedicated direct memory access controller (AVB-DMAC) for transferring transmitted Ethernet frames to and received Ethernet frames from respective storage areas in the User RAM(URAM) at high speed.

The AVB-DMAC is compliant with the following three standards formulated for IEEE 802.1BA: the IEEE 802.1AS timing and synchronization protocol, the IEEE 802.1Qav real-time transfer, and the IEEE 802.1Qat stream reservation protocol.

In this section, URAM refers to the local RAM and external memory.

Descriptors are recommended to be located at addresses H'00 EE0E 8000 to H'00 EE0E BFFF.

33A.1.1 Features

Table 33A.1 lists the specifications of the EthernetAVB module.

Table 33A.1 Specifications (Functions)

Item	Description
Protocol	Flow control conforming with the IEEE 802.3x standard
Data transmission and reception	Transmission and reception of Ethernet (IEEE 802.3) frames
Transfer speed	Supports transfer at 100 and 1000 Mbps
Mode	Full-duplex mode
Interface	Supports the IEEE 802.3 standard MII (Media Independent Interface) and GMII (Gigabit Media Independent Interface)
Summary of the EthernetAVB function	An intelligent frame separation DMAC (AVB-DMAC) conforming with the following standards stipulated for IEEE 802.1BA: IEEE 802.1AS (time synchronization protocol) IEEE 802.1Qav (real-time transfer) IEEE 1722 (AVTP presentation timestamp) IEEE 802.1Qat is supported by software. Descriptor management system Identification and sorting of frame data, and extraction and gathering of valid data Controllable interrupt frequency (reducing the load on the CPU)
Magic Packet™	Detection of Magic Packets™* and output of a detected signal

Note: * Magic Packet™ is a trademark of Advanced Micro Devices, Inc.

33A.1.2 Block Diagram

Figure 33A.1 is a block diagram of the EthernetAVB.

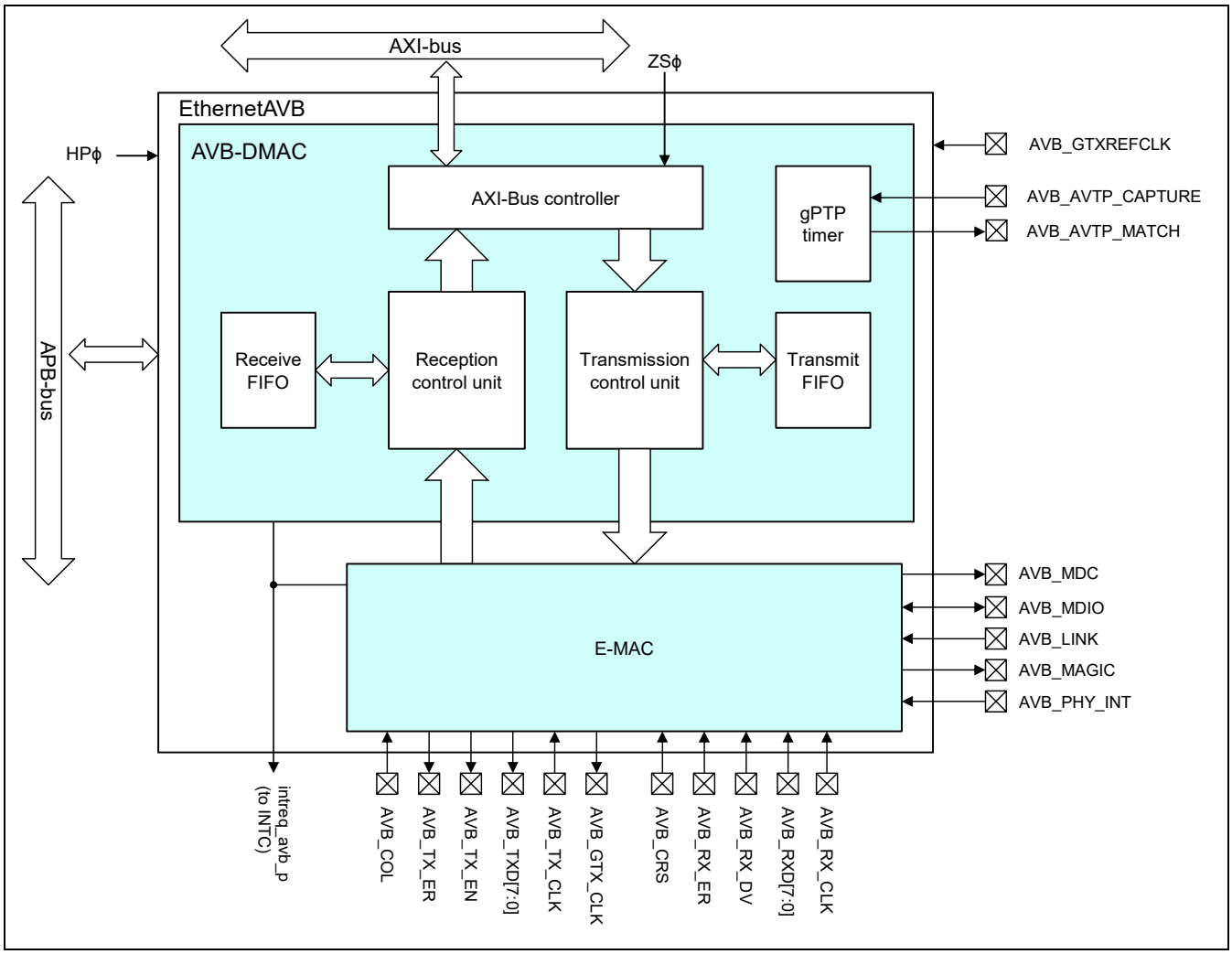


Figure 33A.1 Block Diagram of EthernetAVB

Table 33A.2 Clock Specification

Name	Function
ZSϕ	AXI bus clock
HPϕ	High speed Peripheral clock

33A.1.3 Input/Output Pins

Table 33A.3 lists the pins for use by EthernetAVB.

Table 33A.3 Pin Configuration

Name	I/O	Function
AVB_TXD[7:0]	O	Transmit data signal
AVB_TX_EN	O	Transmit data enable signal
AVB_RXD[7:0]	I	Receive data signal
AVB_RX_DV	I	Receive data enable signal
AVB_TX_CLK	I	Transmit clock signal
AVB_RX_CLK	I	Receive clock signal
AVB_TX_ER	O	Transmit error signal
AVB_RX_ER	I	Reception error signal
AVB_GTX_CLK	O	GMII transmit clock signal
AVB_GTXREFCLK	I	GMII reference clock signal
AVB_MDC	O	Management information transfer clock signal
AVB_MDIO	I/O	Management information transmit/receive data
AVB_CRS	I	Carrier detection signal
AVB_COL	I	Collision detection signal
AVB_LINK	I	Link status signal
AVB_MAGIC	O	Magic packet signal
AVB_PHY_INT	I	PHY interrupt signal
AVB_AVTP_CAPTURE	I	AVTP capture signal
AVB_AVTP_MATCH	O	AVTP match signal

33A.1.4 Register Configuration

Table 33A.4 and Table 33A.5 lists the EthernetAVB related registers and their configurations.

Table 33A.4 Configurations of AVB-DMAC-related Registers

Name	Abbreviation	R/W	Address	Initial Value	Access Size
AVB-DMAC mode register	CCC	R/W	H'E680 0000	H'0000 0000	32
Descriptor base address table register	DBAT	R/W	H'E680 0004	H'0000 0000	32
Descriptor base address load request register	DLR	R/W	H'E680 0008	H'003F FFFF	32
AVB-DMAC status register	CSR	R	H'E680 000C	H'0000 0001	32
Current descriptor address register q (q = 0 to 21)	CDARq	R	H'E680 0010 + q × 4	H'0000 0000	32
Error status register	ESR	R	H'E680 0088	H'0000 0000	32
Receive configuration register	RCR	R/W	H'E680 0090	H'1800 0000	32
Receive queue configuration register i (i = 0 to 4)	RQCi	R/W	H'E680 0094 + i × 4	H'0000 0000	32
Receive padding configuration register	RPC	R/W	H'E680 00B0	H'0000 0100	32
Reception Truncation Configuration register	RTC	R/W	H'E680 00B4	H'0FFC 0FFC	32
Unread frame counter warning level register	UFCW	R/W	H'E680 00BC	H'0000 0000	32
Unread frame counter stop level register	UFCS	R/W	H'E680 00C0	H'0000 0000	32
Unread frame counter register i (i = 0 to 4)	UFCVi	R	H'E680 00C4 + i × 4	H'0000 0000	32
Unread frame counter decrement register i (i = 0 to 4)	UFCDi	R/W	H'E680 00E0 + i × 4	H'0000 0000	32
Separation filter offset register	SFO	R/W	H'E680 00FC	H'0000 0000	32
Separation filter pattern register i (i = 0 to 31)	SFPi	R/W	H'E680 0100 + i × 4	H'0000 0000	32
Separation Filter Value register i (i = 0 to 1)	SFVi	R/W	H'E680 01B8 + i × 4	H'0000 0000	32
Separation filter mask register i (i = 0, 1)	SFMi	R/W	H'E680 01C0 + i × 4	H'0000 0000	32
Separation Filter Load register	SFL	R/W	H'E680 01C8	H'0000 001F	32
Current Incremental Address Register r (r = 0 to 17)	CIARr	R	H'E680 0200 + i × 4	H'0000 0000	32
Last Incremental Address Register r (r = 0 to 17)	LIARr	R	H'E680 0280 + i × 4	H'0000 0000	32
Transmit configuration register	TGC	R/W	H'E680 0300	H'0022 2200	32
Transmit configuration control register	TCCR	R/W	H'E680 0304	H'0000 0000	32
Transmit status register	TSR	R	H'E680 0308	H'0000 0000	32
E-MAC status FIFO Access register	MFA	R	H'E680 030C	H'0000 0000	32
Time stamp FIFO access register 0	TFA0	R	H'E680 0310	H'0000 0000	32
Time stamp FIFO access register 1	TFA1	R	H'E680 0314	H'0000 0000	32
Time stamp FIFO access register 2	TFA2	R	H'E680 0318	H'0000 0000	32
Version and Release Register	VRR	R	H'E680 031C	H'0000 E300	32
CBS increment value register c (c = 0, 1)	CIVRc	R/W	H'E680 0320 + c × 4	H'0000 0001	32
CBS decrement value register c (c = 0, 1)	CDVRc	R/W	H'E680 0328 + c × 4	H'FFFF FFFF	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
CBS upper limit register c (c = 0, 1)	CULc	R/W	H'E680 0330 + c × 4	H'7FFF FFFF	32
CBS lower limit register c (c = 0, 1)	CLLc	R/W	H'E680 0338 + c × 4	H'8000 0001	32
Descriptor interrupt control register	DIC	R/W	H'E680 0350	H'0000 0000	32
Descriptor interrupt status register	DIS	R/W	H'E680 0354	H'0000 0000	32
Error interrupt control register	EIC	R/W	H'E680 0358	H'0000 0000	32
Error interrupt status register	EIS	R/W	H'E680 035C	H'0000 0000	32
Receive interrupt control register 0	RIC0	R/W	H'E680 0360	H'0000 0000	32
Receive interrupt status register 0	RIS0	R/W	H'E680 0364	H'0000 0000	32
Receive interrupt control register 1	RIC1	R/W	H'E680 0368	H'0000 0000	32
Receive interrupt status register 1	RIS1	R/W	H'E680 036C	H'0000 0000	32
Receive interrupt control register 2	RIC2	R/W	H'E680 0370	H'0000 0000	32
Receive interrupt status register 2	RIS2	R/W	H'E680 0374	H'0000 0000	32
Transmit interrupt control register	TIC	R/W	H'E680 0378	H'0000 0000	32
Transmit interrupt status register	TIS	R/W	H'E680 037C	H'0000 0000	32
Interrupt summary status register	ISS	R	H'E680 0380	H'0000 0000	32
Common Interrupt Enable register	CIE	R/W	H'E680 0384	H'0000 0000	32
Reception Interrupt Control register 3	RIC3	R/W	H'E680 0388	H'0000 0000	32
Reception Interrupt Status register 3	RIS3	R/W	H'E680 038C	H'0000 0000	32
gPTP configuration control register	GCCR	R/W	H'E680 0390	H'0000 002C	32
gPTP maximum transit time register	GMTT	R/W	H'E680 0394	H'0000 0000	32
gPTP presentation time comparison register	GPTC	R/W	H'E680 0398	H'0000 0000	32
gPTP timer increment register	GTI	R/W	H'E680 039C	H'0000 0001	32
gPTP timer offset register i (i = 0 to 2)	GTOi	R/W	H'E680 03A0 + i × 4	H'0000 0000	32
gPTP interrupt control register	GIC	R/W	H'E680 03AC	H'0000 0000	32
gPTP interrupt status register	GIS	R/W	H'E680 03B0	H'0000 0000	32
gPTP Captured Presentation Time register	GCPT	R	H'E680 03B4	H'0000 0000	32
gPTP timer capture register i (i = 0 to 2)	GCTi	R/W	H'E680 03B8 + i × 4	H'0000 0000	32
gPTP Status Register	GSR	R	H'E680 03C4	H'0000 0000	32
gPTP Interrupt Enable register	GIE	R/W	H'E680 03CC	H'0000 0000	32
gPTP Interrupt Disable register	GID	R/W	H'E680 03D0	H'0000 0000	32
gPTP Interrupt Line selection register	GIL	R/W	H'E680 03D4	H'0000 0000	32
gPTP Presentation Time Fifo register i (i = 0 to 3)	GPTFi	R/W	H'E680 03E0 + i × 4	H'0000 0000	32
Descriptor Interrupt Line selection register	DIL	R/W	H'E680 0440	H'0000 0000	32
Error Interrupt Line selection register	EIL	R/W	H'E680 0444	H'0000 0000	32
Transmission Interrupt Line selection register	TIL	R/W	H'E680 0448	H'0000 0000	32
Descriptor Interrupt Enable register	DIE	R/W	H'E680 0450	H'0000 0000	32
Descriptor Interrupt Disable register	DID	R/W	H'E680 0454	H'0000 0000	32
Error Interrupt Enable register	EIE	R/W	H'E680 0458	H'0000 0000	32
Error Interrupt Disable register	EID	R/W	H'E680 045C	H'0000 0000	32

Name	Abbreviation	R/W	Address	Initial Value	Access Size
Reception Interrupt Enable register 0	RIE0	R/W	H'E680 0460	H'0000 0000	32
Reception Interrupt Disable register 0	RID0	R/W	H'E680 0464	H'0000 0000	32
Reception Interrupt Enable register 1	RIE1	R/W	H'E680 0468	H'0000 0000	32
Reception Interrupt Disable register 1	RID1	R/W	H'E680 046C	H'0000 0000	32
Reception Interrupt Enable register 2	RIE2	R/W	H'E680 0470	H'0000 0000	32
Reception Interrupt Disable register 2	RID2	R/W	H'E680 0474	H'0000 0000	32
Transmission Interrupt Enable register	TIE	R/W	H'E680 0478	H'0000 0000	32
Transmission Interrupt Disable register	TID	R/W	H'E680 047C	H'0000 0000	32
Reception Interrupt Enable register 3	RIE3	R/W	H'E680 0488	H'0000 0000	32
Reception Interrupt Disable register 3	RID3	R/W	H'E680 048C	H'0000 0000	32

Table 33A.5 Configuration of E-MAC-related Registers

Name	Abbreviation	R/W	Address	Initial Value	Access Size
E-MAC mode register	ECMR	R/W	H'E680 0500	H'0000 0000	32
Receive frame length register	RFLR	R/W	H'E680 0508	H'0000 0000	32
E-MAC status register	ECSR	R/W	H'E680 0510	H'0000 0000	32
E-MAC interrupt permission register	ECSIPR	R/W	H'E680 0518	H'0000 0000	32
PHY interface register	PIR	R/W	H'E680 0520	H'0000 000X	32
PHY Status Register	PSR	R	H'E680 0528	H'0000 0000	32
PHY_INT Polarity Register	PIPR	R/W	H'E680 052C	H'0000 0000	32
Automatic PAUSE frame register	APR	R/W	H'E680 0554	H'0000 0000	32
Manual PAUSE frame register	MPR	R/W	H'E680 0558	H'0000 0000	32
PAUSE frame transmit counter	PFTCR	R	H'E680 055C	H'0000 0000	32
PAUSE frame receive counter	PFRCR	R	H'E680 0560	H'0000 0000	32
Automatic PAUSE frame retransmit count register	TPAUSER	R/W	H'E680 0564	H'0000 0000	32
PAUSE frame transmit times counter	PFTTCR	R	H'E680 0568	H'0000 0000	32
E-MAC Mode Register 2	GECMR	R/W	H'E680 05B0	H'0000 0000	32
E-MAC address high register	MAHR	R/W	H'E680 05C0	H'0000 0000	32
E-MAC address low register	MALR	R/W	H'E680 05C8	H'0000 0000	32
Transmit retry over counter register	TROCR	R/W	H'E680 0700	H'0000 0000	32
CRC error frame receive counter register	CEFCR	R/W	H'E680 0740	H'0000 0000	32
Frame receive error counter register	FRECR	R/W	H'E680 0748	H'0000 0000	32
Too-short frame receive counter register	TSFRCR	R/W	H'E680 0750	H'0000 0000	32
Too-long frame receive counter register	TLFRCR	R/W	H'E680 0758	H'0000 0000	32
Residual-bit frame receive counter register	RFCR	R/W	H'E680 0760	H'0000 0000	32
Multicast address frame receive counter register	MAFCR	R/W	H'E680 0778	H'0000 0000	32

33A.2 Register Description

33A.2.1 AVB-DMAC Mode Register (CCC)

The CCC register specifies the operating mode of the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	FCE	LBME	—	—	—	—	—	—	CSEL[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DTSR	GAC	—	—	—	—	—	OPC[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
25	FCE	0	R/W	Flow Control Enable This bit enables the flow control support of E-MAC. When flow control is enabled, the E-MAC gets informed about the Rx-FIFO level (Rx-FIFO fill level reached RCR.RFCL). 0: Flow control disabled 1: Flow control enabled
24	LBME	0	R/W	Loopback Mode Enable This bit enables loopback mode. In loopback mode, the transmission lines are internally connected to the reception lines. When loopback mode is to be used, the Ethernet transmission clock must be supplied to the RGMII interface. A received clock signal is not required. Writing to this bit is only possible when the current operating mode is configuration mode. 0: Normal operation 1: Loopback mode is enabled. Note: Data for transmission are still output normally. To eliminate effects on external modules, pin control should be applied to block the output of data.
23 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17, 16	CSEL[1:0]	00	R/W	gPTP Clock Select These bits select the clock source for the gPTP timer. Writing to these bits is only possible when the current operating mode is configuration mode and CCC.GAC is 0. Writing to these bits is only possible when the current operating mode is Reset mode when writing CCC.GAC to 1 and CCC.OPC to B'01 by same write access. 00: gPTP is disabled 01: High-speed peripheral bus clockOther: Setting prohibited
15 to 9	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	DTSR	0	R/W	Data Transmission Suspend Request This bit can suspend access to the URAM. The access is suspended on completion of the transfer of the AXI transaction currently being transferred. This function disables access to the URAM without affecting normal operation of the AVB-DMAC. Use this bit when exclusive control over the contents of the URAM is necessary, for example, in checking its integrity. Note that the transmission and reception queues are not processed while access is suspended. Change neither the AVB-DMAC settings nor the mode while access is suspended. 0: Normal operation 1: Requests suspension
7	GAC	0	R/W	Gptp Active in Config This bit enables the gPTP support of EthernetAVB in CONFIG mode. Function of gPTP support in OPERATION and STANDBY is not influenced by this bit. When gPTP support is active in CONFIG, CCC.CSEL defines the timer clock source. The CPU can only write 1 to this bit if CSR.OPS is RESET when writing CCC.OPC to B'01 by same write access. 0: Normal operation 1: gPTP support active in CONFIG mode
6 to 2	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
1, 0	OPC[1:0]	00	R/W	Operating Mode Configuration These bits specify the operating mode. For the operating modes, see section 33A.3.1.1 Operating Modes. Writing to these bits is possible in any of the operating modes, but should not be done after the application system has issued a Power Off request. When CCC.GAC is 1 CPU should not write B'11 to these bits. [Changing condition] These bits are set to B'00 when RESET mode is entered due to 'enter power off' request. 00: Reset mode 01: Configuration mode 10: Operation mode 11: standby mode

33A.2.2 Descriptor Base Address Table Register (DBAT)

The DBAT register specifies the base address of the descriptor table in the URAM. For the structure of this table, see section 33A.3.3 Descriptors. Writing to this bit is only possible when the current operating mode is configuration mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TA[31:0]	H'0000 0000	R/W	Descriptor Base Table Address Base address of the descriptor table in the URAM Note: The setting of this bit must be a multiple of four (i.e. bit 0 and bit 1 must be set to 0).

33A.2.3 Descriptor Base Address Load Request Register (DLR)

The DLR register is used to issue a request to load the values from the current descriptor address register q (CDARq) for each queue to the descriptor base address table register (DBAT).

Setting a bit to 1 issues a request for loading the descriptor base address for the queue q. If transfer is currently in progress, loading is executed on completion of transfer for the current frame. Completion of loading leads to automatic setting of the corresponding bit to 0.

For the transmission queues, base address load requests are executed even while fetching is in progress (the transmit start request bit in the transmit configuration control register (TCCR.TSRQt) is 1). Therefore, be sure to check that fetching is not in progress before issuing a request.

Writing to a bit of this register is only possible when the current operating mode is operation mode. Only 1 can be written to this bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	LBA21	LBA20	LBA19	LBA18	LBA17	LBA16
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LBA15	LBA14	LBA13	LBA12	LBA11	LBA10	LBA9	LBA8	LBA7	LBA6	LBA5	LBA4	LBA3	LBA2	LBA1	LBA0
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21	LBA21	1	R/W	Base Address Load Request (Rx17: Stream 15) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
20	LBA20	1	R/W	Base Address Load Request (Rx16: Stream 14) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
19	LBA19	1	R/W	Base Address Load Request (Rx15: Stream 13) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
18	LBA18	1	R/W	Base Address Load Request (Rx14: Stream 12) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.

Bit	Bit Name	Initial Value	R/W	Description
17	LBA17	1	R/W	Base Address Load Request (Rx13: Stream 11) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
16	LBA16	1	R/W	Base Address Load Request (Rx12: Stream 10) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
15	LBA15	1	R/W	Base Address Load Request (Rx11: Stream 9) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
14	LBA14	1	R/W	Base Address Load Request (Rx10: Stream 8) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
13	LBA13	1	R/W	Base Address Load Request (Rx9: Stream 7) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
12	LBA12	1	R/W	Base Address Load Request (Rx8: Stream 6) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
11	LBA11	1	R/W	Base Address Load Request (Rx7: Stream 5) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
10	LBA10	1	R/W	Base Address Load Request (Rx6: Stream 4) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
9	LBA9	1	R/W	Base Address Load Request (Rx5: Stream 3) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
8	LBA8	1	R/W	Base Address Load Request (Rx4: Stream 2) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.

Bit	Bit Name	Initial Value	R/W	Description
7	LBA7	1	R/W	Base Address Load Request (Rx3: Stream 1) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
6	LBA6	1	R/W	Base Address Load Request (Rx2: Stream 0) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
5	LBA5	1	R/W	Base Address Load Request (Rx1: Network Control) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
4	LBA4	1	R/W	Base Address Load Request (Rx0: Best Effort) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
3	LBA3	1	R/W	Base Address Load Request (Tx3: Stream Class A) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
2	LBA2	1	R/W	Base Address Load Request (Tx2: Stream Class B) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
1	LBA1	1	R/W	Base Address Load Request (Tx1: Network Control) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.
0	LBA0	1	R/W	Base Address Load Request (Tx0: Best Effort) 0: No load request is issued. 1: When written: A request for loading the corresponding base address is issued. When read: The given base address is being loaded.

33A.2.4 AVB-DMAC Status Register (CSR)

The CSR register is used to indicate the operating mode in which the AVB-DMAC is running and the individual communications states.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TDUO	RPO	TPO3	TPO2	TPO1	TPO0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	DTS	—	—	—	—	OPS[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are read as 0.
21	TDUO	0	R	Transmission Descriptor Update On-going This bit indicates that there is pending descriptor update for one or more transmit queues. When this bit is 1, there are descriptors of already or currently processed transmit storage elements not updated in URAM. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when all transmit queue related storage elements processed. This bit is set to 1 when descriptor related status update procedure starts (descriptor update and register flagging). 0: No pending descriptor update 1: Pending descriptor update in URAM
20	RPO	0	R	Receive Process Status This bit indicates whether a reception queue contains an unread received frame. This bit being set to 1 indicates that a received frame is yet to be stored in the URAM. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Received frames in the reception FIFO all being stored in the URAM. 1: Reception is in progress. [Setting condition] — A received frame being stored in the reception FIFO (but not yet in the URAM).

Bit	Bit Name	Initial Value	R/W	Description
19	TPO3	0	R	Transmit Process Status 3 (Stream Class A) This bit indicates whether a class A stream is being transmitted. This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ3 is 0. 1: Transmission is in progress. [Setting condition] — Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ3)).
18	TPO2	0	R	Transmit Process Status 2 (Stream Class B) This bit indicates whether a class B stream is being transmitted. This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ2 is 0. 1: Transmission is in progress. [Setting condition] — Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ2)).
17	TPO1	0	R	Transmit Process Status 1 (Network Control) This bit indicates whether a network control is being transmitted. This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ1 is 0. 1: Transmission is in progress. [Setting condition] — Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ1)).

Bit	Bit Name	Initial Value	R/W	Description
16	TPO0	0	R	Transmit Process Status 0 (Best Effort) This bit indicates whether a best effort is being transmitted. This bit being set to 1 indicates that the AVB-DMAC is fetching data for transmission from the URAM, or the E-MAC is transmitting data. 0: Normal operation [Clearing conditions] — The current operating mode is not operation mode. — Completion of transfer of all frames for transmission from the transmission FIFO and TCCR.TSRQ0 is 0. 1: Transmission is in progress. [Setting condition] — Transmission being started (by writing 1 to the transmit start request bit in the transmit configuration control register (TCCR.TSRQ0)).
15 to 9	—	All 0	R	Reserved These bits are read as 0.
8	DTS	0	R	Data Transmission Suspended Status This bit indicates whether access to the URAM is enabled. 0: Normal operation [Clearing conditions] — The data transmission suspend request bit in the AVB-DMAC mode register (CCC.DTSR) being 0. 1: Transmission is in progress. [Setting condition] — Access to the URAM not proceeding while the data transmission suspend request bit (CCC.DTSR) in the AVB-DMAC mode register (CCC) is 1 (if the URAM is being accessed, this bit is set to 1 on completion of access).
7 to 4	—	All 0	R	Reserved These bits are read as 0.
3 to 0	OPS[3:0]	0001	R	Operating Mode Status These bits indicate the current operating mode. For the operating modes, see section 33A.3.1.1 Operating Modes. 0001: Reset mode 0010: Configuration mode 0100: Operation mode 1000: standby mode Other settings are reserved.

33A.2.5 Current Descriptor Address Register q (CDARq) (q = 0 to 21)

The CDARq register indicates the current descriptor address.

CDAR0 to CDAR3 indicate the addresses of the current descriptors for the corresponding transmission queues while CDAR4 to CDAR21 indicate the addresses of the current descriptors for the corresponding reception queues.

If the operating mode is changed to operation mode, the contents of the register for the queue to be used are set in the descriptor base address table register (DBAT).

Also, when the descriptor base address load request register (DLR) issues a load request, the contents of the descriptor base address table register (DBAT) are set in to the corresponding CDAR registers.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CDA[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CDA[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDA[31:0]	H'0000 0000	R	Current Descriptor Address The address of the current descriptors for the transmission queues. Conditions for updating: • These bits are set to 0 when the operating mode is not operation mode. This register is updated in response to processing of the descriptor for a queue.

33A.2.6 Error Status Register (ESR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	EIL	ET[3:0]				—	—	—	EQN[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved These bits are read as 0.
12	EIL	0	R	Error Information Lost This bit indicates that error information detect by EthernetAVB is lost, because the previous reported error has not been processed by CPU. [Changing conditions] — This bit is set to 0 when leaving operation mode. — This bit is set to 0 when CPU writes 0 to EIS.QEF. — This bit is set to 1 when the set condition of EIS.QEF is fulfilled while EIS.QEF is 1. 0: No loss of error information 1: Lost of error information detected

Bit	Bit Name	Initial Value	R/W	Description
11 to 8	ET[3:0]	0000	R	Error Type These bits indicate details about the transfer stage which was handled when EthernetAVB has detected an error. When the fault is related to the read descriptor (ESR.ET = B'0000 or B'0010), CPU needs to correct the faulty descriptor before the related queue can continue processing. Because the queue halts at the faulty descriptor CDARq.CDA (q = ESR.EQN) is identifying the faulty descriptor directly. When the fault is related to descriptor writing (ESR.ET = B'0001), CPU needs to recognize the not-updated or incorrectly updated descriptor in queue ESR.EQN. The write problem is not influencing how EthernetAVB processes the descriptor chain. When the fault is related to the Tx-buffer (ESR.ET = B'0011), CPU needs to clean-up the Tx-buffer to correct the buffer control structures. All other errors are transient in nature and may be corrected by continuation of hardware or software operation; so there is no strong demand on CPU interaction. Refer to section 33A.3.2.2 Checking Integrity for details of error handling. The CPU should only evaluate these bits when the EIS.QEF bit is 1. [Changing condition] — These bits are updated when the set condition of the EIS.QEF bit is fulfilled and the EIS.QEF bit is 0. 0000: Read descriptor from URAM 0001: Write descriptor to URAM 0010: Interpret data descriptor 0011: Tx-buffer is corrupted 0100: Read data from URAM 0101: Write data or timestamp to URAM 0110: Reading from Rx-FIFO 0111: Rx-FIFO is corrupted 1000: Frame size error during reception detected 1001: Frame size error during transmission detected 1010: Tx-buffer overflow 1011: AVTP FIFO error
7 to 5	—	All 0	R	Reserved These bits are read as 0.
4 to 0	EQN[4:0]	00000	R	Error Queue Number These bits indicate the queue number which was handled when EthernetAVB has detected an error. A fault reported for ESR.EQN = 0 to 3 is related to transmit queue t (t = 0 to 3). From ESR.EQN = 4, the fault is related to receive queue r (r = ESR.EQN – 4). The CPU should only evaluate these bits when the EIS.QEF bit is 1. The CPU should not evaluate these bits when the ESR.ET bit is B'0011, B'0111 or B'1011. [Changing condition] — These bits are updated when the set condition of the EIS.QEF bit is fulfilled and the EIS.QEF bit is 0.

33A.2.7 Receive Configuration Register (RCR)

The RCR register is used to make settings related to reception for the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	RFCL[12:0]												
Initial value:	0	0	0	1	1	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	ETS2	ETS0	ESF[1:0]		ENCF	EFFS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 29	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
28 to 16	RFCL[12:0]	H'1800	R/W	Receive FIFO Caution Level These bits set the caution level for the reception FIFO and are used to maintain the priority order of the storage of received data and the fetching of data for transmission. If the reception FIFO contains less data than this level, processing of both transmission and reception queues becomes pending. If the reception FIFO contains more data than this level, only data in the reception queue are transferred, and processing of the transmission queue becomes pending. Writing to this bit is only possible when the current operating mode is configuration mode. Recommended value: H'1800 Notes: • The setting of this bit must be a multiple of four (i.e. set RFCL[1:0] = B'00). • In the case of this LSI chip, set these bits to H'1800.
15 to 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5	ETS2	0	R/W	Time Stamp Enable (Stream) Enables the inclusion of time-stamp information in reception queues 2 to 17. Writing to this bit is only possible when the current operating mode is configuration mode. 0: Time stamping is disabled. 1: Time stamping is enabled. Recommended value: 0
4	ETS0	0	R/W	Time Stamp Enable (Best Effort) Enables the inclusion of time-stamp information in reception queue 0. Writing to this bit is only possible when the current operating mode is configuration mode. 0: Time stamping is disabled. 1: Time stamping is enabled. Recommended value: 0

Bit	Bit Name	Initial Value	R/W	Description
3, 2	ESF[1:0]	00	R/W	Stream Filtering Select Settings for reception queues 2 to 17. These bits select separation filtering for reception queues 2 to 17. The queue-dependent separation filter can be used in combination with the identification of AVB stream frames. When the value is B'00, filtering is disabled and frames from streams are processed in reception queue 0 (best effort). When the value is B'01, the separation filter is enabled for both AVB stream frames and non-AVB stream frames; frames from non-matching streams are processed in reception queue 0 (best effort). When the value is B'10, the separation filter is enabled for AVB stream frames; frames from non-matching streams are discarded. When the value is B'11, the separation filter is enabled for AVB stream frames; frames from non-matching streams are processed in reception queue 0 (best effort). For separation filtering, see section 33A.3.4.1(1) Separation Filtering. Writing to this bit is only possible when the current operating mode is configuration mode. 00: Filtering is disabled. Frames are processed in queue 0 (best effort). 01: The filter for both AVB stream frames and non-AVB stream frames is enabled; non-matching frames from the stream are processed in queue 0 (best effort). 10: The filter for separating AVB stream frames from non-AVB stream frames is enabled; non-matching frames are discarded. 11: The filter for separating AVB stream frames from non-AVB stream frames is enabled; non-matching frames from a stream are processed in queue 0 (best effort). Recommended value: B'10 or B'11
1	ENCF	0	R/W	Network Control Filtering Enable Setting for reception queue 1 (network control) Enables the AVB network control frame for reception queue 1. When reception queue 1 is disabled, a received frame is stored in reception queue 0 (best effort). Writing to this bit is only possible when the current operating mode is configuration mode. 0: Network control is disabled. 1: Network control is enabled.
0	EFFS	0	R/W	Error Frame Enable Enables or disables the reception of frames that have been classified as error frames by the E-MAC. Received error frames are stored in reception queue 0 (best effort). An indicator of error detection by the E-MAC during reception is stored in the descriptor (DESCR.MS). Writing to this bit is only possible when the current operating mode is configuration mode. 0: Error frames are disabled. 1: Error frames are enabled. Recommended value: 0

33A.2.8 Receive Queue Configuration Register i (RQCi) (i = 0 to 4)

The RQC0 register is used to set up reception queues 0 to 3.

The RQC1 register is used to set up reception queues 4 to 7.

The RQC2 register is used to set up reception queues 8 to 11.

The RQC3 register is used to set up reception queues 12 to 15.

The RQC4 register is used to set up reception queues 16 to 17.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	PIA3	UFCC3[1:0]		TSEL3[1:0]		RSM3[1:0]		—	PIA2	UFCC2[1:0]		TSEL2[1:0]		RSM2[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PIA2	UFCC1[1:0]		TSEL1[1:0]		RSM1[1:0]		—	PIA0	UFCC0[1:0]		TSEL0[1:0]		RSM0[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.
30	PIA3	0	R/W	Packed Incremental data Area (Receive Queue 3+i×4) This bit defines how addresses inside the incremental data area of queue 3+i×4 are handled. When this bit is 0, frame data in incremental data area starts always at a 32 bit address. Depending on received frame length there are up to 3 undefined bytes between two frames in URAM. When this bit is 1, there will no gaps generated between two frames in incremental data area. The CPU can only write to this bit if CSR.OPS is CONFIG. 0: Frame data starts always 32 bit aligned 1: No gaps between frame data in incremental data area
29, 28	UFCC3[1:0]	00	R/W	Unread Frame Counter Configuration (Receive Queue 3+i×4) These bits set the unread frame counter used in reception queue 3+i×4. With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter. Set the pattern number 3 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit. When the value is B'00, the stop function is disabled. Writing to the bits is only possible when the current operating mode is configuration mode.

Bit	Bit Name	Initial Value	R/W	Description
27, 26	TSEL3	00	R/W	Truncation SELection (Receive Queue 3+i×4) This bit defines a maximum number of bytes for storing frames in receive queue 3+i×4. Frames longer than the selected maximum are truncated. EthernetAVB provides 2 common configurations for the maximum frame length. This bit selects one of the configurations j defined by RTCi.MFLj. 00: Maximum frame length defined by RTC0.MFL0 01: Maximum frame length defined by RTC0.MFL1 Other configurations are Invalid The CPU can only write to these bits if CSR.OPS is CONFIG.
25, 24	RSM3[1:0]	00	R/W	Receive Synchronous Mode (Receive Queue 3+i×4) These bits set receive synchronous mode. Set B'00 in this bit. For receive synchronous mode, see section 33A.3.4.3(3) Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode. 00: Mode with write-back 01: Keep DT mode (no update of DT field at descriptor write back) 10: No write-back (no descriptor write back) 11: Invalid
23	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.
22	PIA2	0	R/W	Packed Incremental data Area (Receive Queue 2+i×4) This bit defines how addresses inside the incremental data area of queue 2+i×4 are handled. When this bit is 0, frame data in incremental data area starts always at a 32 bit address. Depending on received frame length there are up to 3 undefined bytes between two frames in URAM. When this bit is 1, there will no gaps generated between two frames in incremental data area. The CPU can only write to this bit if CSR.OPS is CONFIG. 0: Frame data starts always 32 bit aligned 1: No gaps between frame data in incremental data area
21, 20	UFCC2[1:0]	00	R/W	Unread Frame Counter Configuration (Receive Queue 2+i×4) These bits set the unread frame counter used in reception queue 2+i×4. With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter. Set the pattern number 2 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit. When the value is B'00, the stop function is disabled. Writing to the bits is only possible when the current operating mode is configuration mode.

Bit	Bit Name	Initial Value	R/W	Description
19, 18	TSEL2	00	R/W	Truncation SELection (Receive Queue 2+i×4) This bit defines a maximum number of bytes for storing frames in receive queue 2+i×4. Frames longer than the selected maximum are truncated. EthernetAVB provides 2 common configurations for the maximum frame length. This bit selects one of the configurations j defined by RTCi.MFLj. 00: Maximum frame length defined by RTC0.MFL0 01: Maximum frame length defined by RTC0.MFL1 Other configurations are Invalid The CPU can only write to these bits if CSR.OPS is CONFIG.
17, 16	RSM2[1:0]	00	R/W	Receive Synchronous Mode (Receive Queue 2+i×4) These bits set receive synchronous mode. Set B'00 in this bit. For receive synchronous mode, see section 33A.3.4.3(3) Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode. 00: Mode with write-back 01: Keep DT mode (no update of DT field at descriptor write back) 10: No write-back (no descriptor write back) 11: Invalid
15	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.
14	PIA1	0	R/W	Packed Incremental data Area (Receive Queue 1+i×4) This bit defines how addresses inside the incremental data area of queue 1+i×4 are handled. When this bit is 0, frame data in incremental data area starts always at a 32 bit address. Depending on received frame length there are up to 3 undefined bytes between two frames in URAM. When this bit is 1, there will no gaps generated between two frames in incremental data area. The CPU can only write to this bit if CSR.OPS is CONFIG. 0: Frame data starts always 32 bit aligned 1: No gaps between frame data in incremental data area
13, 12	UFCC1[1:0]	00	R/W	Unread Frame Counter Configuration (Receive Queue 1+i×4) These bits set the unread frame counter used in reception queue 1+i×4. With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter. Set the pattern number 1 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit. When the value is B'00, the stop function is disabled. Writing to the bits is only possible when the current operating mode is configuration mode.

Bit	Bit Name	Initial Value	R/W	Description
11, 10	TSEL1	00	R/W	Truncation SELection (Receive Queue 1+i×4) This bit defines a maximum number of bytes for storing frames in receive queue 1+i×4. Frames longer than the selected maximum are truncated. EthernetAVB provides 2 common configurations for the maximum frame length. This bit selects one of the configurations j defined by RTCi.MFLj. 00: Maximum frame length defined by RTC0.MFL0 01: Maximum frame length defined by RTC0.MFL1 Other configurations are Invalid The CPU can only write to these bits if CSR.OPS is CONFIG.
9, 8	RSM1[1:0]	00	R/W	Receive Synchronous Mode (Receive Queue 1+i×4) These bits set receive synchronous mode. Set B'00 in this bit. For receive synchronous mode, see section 33A.3.4.3(3) Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode. 00: Mode with write-back 01: Keep DT mode (no update of DT field at descriptor write back) 10: No write-back (no descriptor write back) 11: Invalid
7	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.
6	PIA0	0	R/W	Packed Incremental data Area (Receive Queue 0+i×4) This bit defines how addresses inside the incremental data area of queue 0+i×4 are handled. When this bit is 0, frame data in incremental data area starts always at a 32 bit address. Depending on received frame length there are up to 3 undefined bytes between two frames in URAM. When this bit is 1, there will no gaps generated between two frames in incremental data area. The CPU can only write to this bit if CSR.OPS is CONFIG. 0: Frame data starts always 32 bit aligned 1: No gaps between frame data in incremental data area
5, 4	UFCC0[1:0]	00	R/W	Unread Frame Counter Configuration (Receive Queue 0+i×4) These bits set the unread frame counter used in reception queue 0+i×4. With the AVB-DMAC, four patterns of settings are available for the unread frame counter. Use the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) to set the warning level and stop level of the unread frame counter. Set the pattern number 0 set in the unread frame counter warning level configuration register (UFCW) and unread frame counter stop level configuration register (UFCS) in this bit. When the value is B'00, the stop function is disabled. Writing to the bits is only possible when the current operating mode is configuration mode.

Bit	Bit Name	Initial Value	R/W	Description
3, 2	TSEL0	00	R/W	Truncation SELection (Receive Queue 0+i×4) This bit defines a maximum number of bytes for storing frames in receive queue 0+i×4. Frames longer than the selected maximum are truncated. EthernetAVB provides 2 common configurations for the maximum frame length. This bit selects one of the configurations j defined by RTCi.MFLj. 00: Maximum frame length defined by RTC0.MFL0 01: Maximum frame length defined by RTC0.MFL1 Other configurations are Invalid The CPU can only write to these bits if CSR.OPS is CONFIG.
1, 0	RSM0[1:0]	00	R/W	Receive Synchronous Mode (Receive Queue 0+i×4) These bits set receive synchronous mode. Set B'00 in this bit. For receive synchronous mode, see section 33A.3.4.3(3) Mode with Write-Back. Writing to the bits is only possible when the current operating mode is configuration mode. 00: Mode with write-back 01: Keep DT mode (no update of DT field at descriptor write back) 10: No write-back (no descriptor write back) 11: Invalid

33A.2.9 Receive Padding Configuration Register (RPC)

The RPC register is used to set padding for received frames.

Note: Padding can be used to extend frame lengths, but frame lengths should not exceed 4 Kbytes.

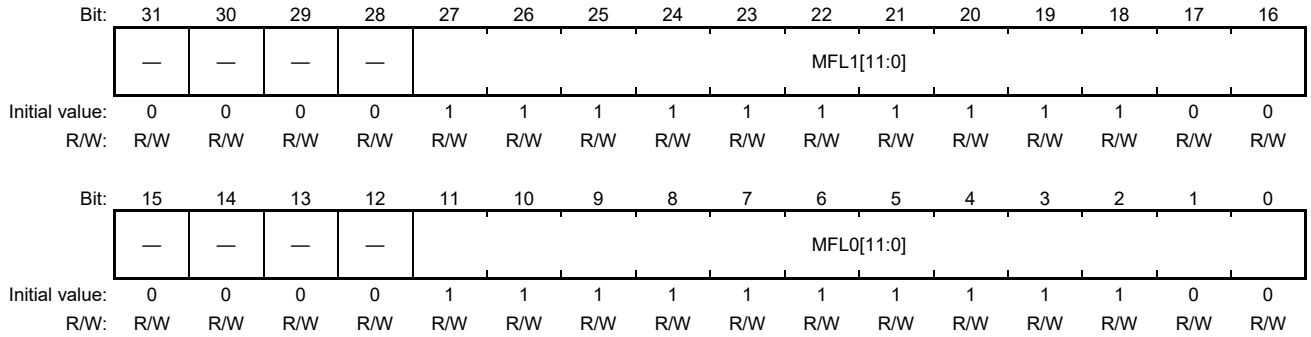
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	DCNT[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	PCNT[2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
23 to 16	DCNT[7:0]	H'00	R/W	Stored Data Counter These bits specify the amount of the frame data (1 to 255) to be stored following the padding. Counting by one indicates one word (4 bytes). For example, when these bits are set to 47, the amount of data is 47 words (= 188 bytes). When these bits are 0, all received data have been stored following the initial padding. Writing to the bits is only possible when the current operating mode is configuration mode. For details on padding, see section 33A.3.4.3(2) Incremental Data Areas.
15 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10 to 8	PCNT[2:0]	001	R/W	Stored Padding Counter These bits specify the amount of padding to be appended to the URAM. Counting by one indicates one word (4 bytes). For example, when these bits are set to 1, the amount of padding is one word (= 4 bytes). Writing to the bits is only possible when the current operating mode is configuration mode. For details on padding, see section 33A.3.4.3(2) Incremental Data Areas. The CPU should not write 0 to these bits.
7 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

33A.2.10 Reception Truncation Configuration register (RTC)

The RTC register is used to set Maximum Number of bytes stored per received frame.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
27 to 16	MFL1[11:0]	H'FFC	R/W	Maximum Frame Length 1 These bits define the maximum frame length (64 to 4092 bytes) stored to URAM. For each receive queue one parameter 1 used for truncation is selected. When a frame received by E-MAC is truncated, CPU gets informed by EIS.QEF and frame size error (ESR.ET is B'1000). Additionally the DESCR.TI in the updated descriptor is set to 1. The CPU can only write to these bits if CSR.OPS is CONFIG. The CPU should only write values which are a multiple of 4 to these bits. The CPU should not write values less than 64 to these bits. The CPU should not write values less then SFO.FBP + 8 to these bits when RCR.ESF is not equal to B'00.
15 to 12	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
11 to 0	MFL0[11:0]	H'FFC	R/W	Maximum Frame Length 0 These bits define the maximum frame length (64 to 4092 bytes) stored to URAM. For each receive queue one parameter 0 used for truncation is selected. When a frame received by E-MAC is truncated, CPU gets informed by EIS.QEF and frame size error (ESR.ET is B'1000). Additionally the DESCR.TI in the updated descriptor is set to 1. The CPU can only write to these bits if CSR.OPS is CONFIG. The CPU should only write values which are a multiple of 4 to these bits. The CPU should not write values less than 64 to these bits. The CPU should not write values less then SFO.FBP + 8 to these bits when RCR.ESF is not equal to B'00.

33A.2.11 Unread frame counter warning level register (UFCW)

The UFCW register sets the warning levels for the number of unread frames.

One of the four warning levels from 0 to 3 can be set for each reception queue. When these bits are set to 0, the stop function is disabled. The level to be used is specified by the receive queue configuration register i (RQCi) (i = 0 to 4).

Writing to the bits is only possible when the current operating mode is configuration mode.

The CPU should not write 63 to these bits.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	WL3[5:0]						—	—	WL2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	WL1[5:0]						—	—	WL0[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29 to 24	WL3[5:0]	000000	R/W	Warning Level 3 Unread frame count warning level 3
23, 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21 to 16	WL2[5:0]	000000	R/W	Warning Level 2 Unread frame count warning level 2
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13 to 8	WL1[5:0]	000000	R/W	Warning Level 1 Unread frame count warning level 1
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	WL0[5:0]	000000	R/W	Warning Level 0 Unread frame count warning level 0

33A.2.12 Unread frame counter stop level register (UFCS)

The UFCS register sets the stop levels for unread frames.

One of the four stop levels from 0 to 3 can be set for each reception queue. When these bits are set to 0, the stop function is disabled. The level to be used is specified by the receive queue configuration register i (RQCi) (i = 0 to 4).

Writing to the bits is only possible when the current operating mode is configuration mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	SL3[5:0]						—	—	SL2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	SL1[5:0]						—	—	SL0[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29 to 24	SL3[5:0]	000000	R/W	Stop Level 3 Unread frame count stop level 3
23, 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21 to 16	SL2[5:0]	000000	R/W	Stop Level 2 Unread frame count stop level 2
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13 to 8	SL1[5:0]	000000	R/W	Stop Level 1 Unread frame count stop level 1
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	SL0[5:0]	000000	R/W	Stop Level 0 Unread frame count stop level 0 The CPU can only write 0

33A.2.13 Unread Frame Counter Register i (UFCVi) (i = 0 to 4)

The UFCV0 register indicates the number of unread frames in reception queues 0 to 3.

The UFCV1 register indicates the number of unread frames in reception queues 4 to 7.

The UFCV2 register indicates the number of unread frames in reception queues 8 to 11.

The UFCV3 register indicates the number of unread frames in reception queues 12 to 15.

The UFCV4 register indicates the number of unread frames in reception queues 16 and 17.

For a description of how to use unread frames, refer to section 33A.3.4.4, Unread Frame Counters.

Conditions for updating:

The bits are set to 0 when the operating mode is not operation mode and when the descriptor base address load request register (DLR) issues a base address load request.

The number is incremented when data received in reception queue r are stored normally. The maximum increment is H'3F. If the value exceeds H'3F, incrementation will not proceed.)

The number is decremented by the value written to the unread frame counter decrement register i (UFCDi).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	CV3[5:0]						—	—	CV2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CV1[5:0]						—	—	CV0[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R	Reserved These bits are read as 0.
29 to 24	CV3[5:0]	000000	R	Unread Frame Count 3+4×i Number of unread frames in reception queue 3+4×i
23, 22	—	All 0	R	Reserved These bits are read as 0.
21 to 16	CV2[5:0]	000000	R	Unread Frame Count 2+4×i Number of unread frames in reception queue 2+4×i
15, 14	—	All 0	R	Reserved These bits are read as 0.
13 to 8	CV1[5:0]	000000	R	Unread Frame Count 1+4×i Number of unread frames in reception queue 1+4×i
7, 6	—	All 0	R	Reserved These bits are read as 0.
5 to 0	CV0[5:0]	000000	R	Unread Frame Count 0+4×i Number of unread frames in reception queue 0+4×i

33A.2.14 Unread Frame Counter Decrement Register i (UFCDi) (i = 0 to 4)

The UFCD0 register is used to decrement unread counters in reception queues 0 to 3.

The UFCD1 register is used to decrement unread counters in reception queues 4 to 7.

The UFCD2 register is used to decrement unread counters in reception queues 8 to 11.

The UFCD3 register is used to decrement unread counters in reception queues 12 to 15.

The UFCD4 register is used to decrement unread counters in reception queues 16 and 17.

Write H'3F to these bits to reset the unread counters in reception queue r (r = 0 to 17). These bits are always read as 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	DV3[5:0]						—	—	DV2[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	DV1[5:0]						—	—	DV0[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31, 30	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
29 to 24	DV3[5:0]	000000	R/W	Unread Frame Decrement Value 3+4×i Unread frame decrement value for reception queue 3+4×i
23, 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21 to 16	DV2[5:0]	000000	R/W	Unread Frame Decrement Value 2+4×i Unread frame decrement value for reception queue 2+4×i
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13 to 8	DV1[5:0]	000000	R/W	Unread Frame Decrement Value 1+4×i Unread frame decrement value for reception queue 1+4×i
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	DV0[5:0]	000000	R/W	Unread Frame Decrement Value 0+4×i Unread frame decrement value for reception queue 0+4×i

33A.2.15 Separation Filter Offset Register (SFO)

The SFO register sets an offset into frames for use by the separation filter.

Note: Received frames having fewer bytes than the setting of these bits + 8 bytes are judged to be non-matching by the separation filter. In this case, the data will either be sorted into a reception queue or discarded in accord with the setting of the separation filtering select bits in the receive configuration register (RCR.ESF).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	FBP[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
5 to 0	FBP[5:0]	000000	R/W	First Byte Position These bits set the position in Ethernet frames of the first byte of the bytes to be used by the separation filter. When these bits are 0, the separation filter starts from the start of each Ethernet frame (first byte of the destination address). For bytes in Ethernet frames, see Figure 33A.2 Operating Mode of AVB-DMAC, in section 33A.3.1.1 Operating Modes. Writing to the bits is only possible when the current operating mode is configuration mode. [Changing condition] These bits are updated to the value of SFVi.LV[5:0] when SFL.LC changes from 30 (Load SFO.FBP) to 31 while CSR.OPS is OPERATION. For separation filtering, see section 33A.3.4.1(1) Separation Filtering.

33A.2.16 Separation Filter Pattern Register i (SFPi) (i = 0 to 31)

A pair of SFPi registers set the pattern for the separation filters to be used by the corresponding reception queues 2 to 17 (for streams 0 to 15).

Each queue shares a 64-bit setting; reception queue 2 (for stream 0) uses SFP0 and SFP1, reception queue 17 (for stream 15) uses SFP30 and SFP31, and so on.

The separation filter passes a frame when, after masking by the mask value set in the separation filter mask register (SFMi), data from received frames match the value defined in these bits.

SFPi.FP[7:0] (where i is an even number) are used for the byte of Ethernet frame data specified by the separation filter offset register, while SFPi.FP[63:56] (where i is the corresponding odd number) are used for the byte at the address specified by the separation filter offset register (SFO) + 7.

Writing to the bits is only possible when the current operating mode is configuration mode.

[Changing condition]

These bits are updated to the value of SFVi.LV[63:0] when SFL.LC changes from s (Load SFPi.FPs) to 31 while CSR.OPS is OPERATION.

For separation filtering, see section 33A.3.4.1(1) Separation Filtering.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FP[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FP[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FP[31:0]	H'0000 0000	R/W	Separation Filter Pattern These bits set the pattern of the separation filter. The 64-bit filter pattern is set for each queue.

33A.2.17 Separation Filter Value register i (SFVi) (i = 0 to 1)

These bits define the 64 bit value to be loaded for separation filtering.

When loading the first by position (SFO.FBP), SFVi.LV[63:6] are ignored.

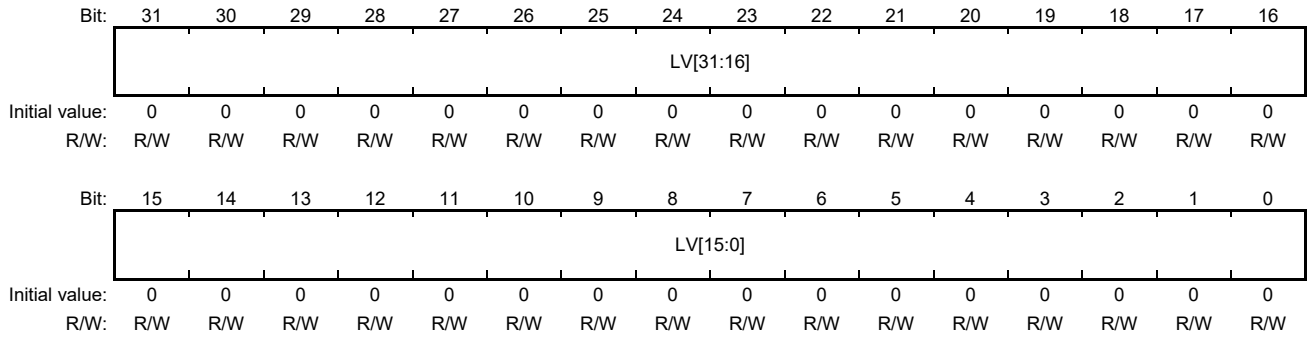
The CPU can only write to these bits if CSR.OPS is OPERATION.

The CPU can only write to these bits if SFL.LC is 31.

[Changing condition]

These bits are set to 0 when leaving OPERATION mode.

For separation filtering, see section 33A.3.4.1(1) Separation Filtering.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LV[31:0]	H'0000 0000	R/W	Separation Filter Value These bits set the Load value of the separation filter.

33A.2.18 Separation Filter Mask Register i (SFMi) (i = 0 or 1)

A pair of SFMi registers sets the mask value for the separation filter used by the corresponding reception queue 2 to 17 (stream 0 to 15).

SFM0.CFM[7:0] are used for bytes of Ethernet frame data specified by the separation filter offset register, while SFM1.CFM[63:56] are used for the separation filter offset register (SFO) + 7.

Frame data at the positions of mask bits that are set to 0 are masked; that is, they do not affect pattern-matching by the separation filter.

Writing to the bits is only possible when the current operating mode is configuration mode.

[Changing condition]

These bits are updated to the value of SFVi.LV[63:0] when SFL.LC changes from 29 (Load SFMi.CFM) to 31 while CSR.OPS is OPERATION.

For separation filtering, see section 33A.3.4.1(1) Separation Filtering.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CFM[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CFM[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CFM[31:0]	H'0000 0000	R/W	Separation Filter Mask These bits set the mask value for the separation filter.

33A.2.19 Separation Filter Load register (SFL)

The SFL register is used to separation filter load.

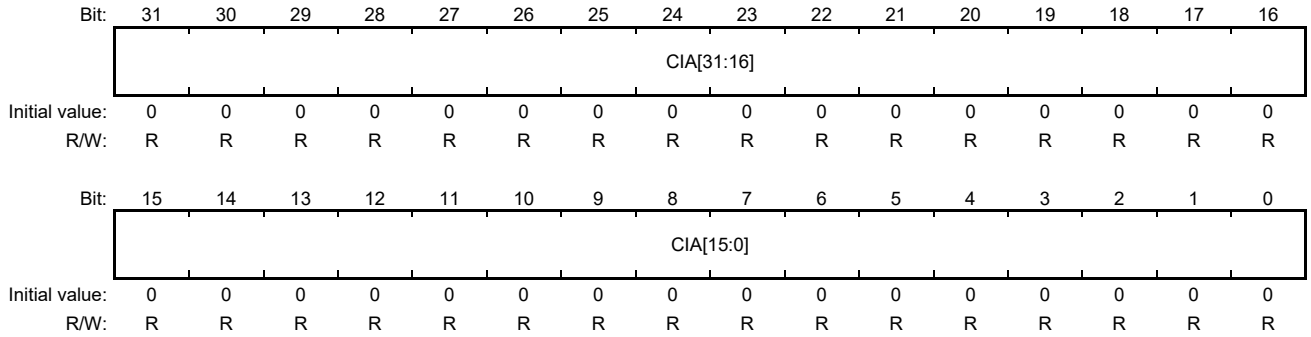
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	LC[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
4 to 0	LC[4:0]	H'1F	R/W	Load Command These bits control update of separation filter configuration in OPERATION mode. By writing 30 to these bits CPU triggers an update of First Byte Position (SFO.FBP) value. By writing 29 to these bits CPU triggers an update of Common Filter Mask (SFMi.CFM) value. By writing number between 0 and 15 to these bits CPU triggers an update of Filter Pattern s (SFPi.FPs) value. The number written to SFL.LC defines the index s of the updated Filter Pattern. The CPU can only write to these bits if CSR.OPS is OPERATION. The CPU can only write to these bits if SFL.LC is 31. [Changing condition] These bits are set to 31 when leaving OPERATION mode. These bits are set to 31 when the requested update has been processed. 0-15: Load of SFPi.FPs with s = SFL.LC 16-28: Invalid 29: Load of SFMi.CFM 30: Load of SFO.FBP 31: No pending load request

33A.2.20 Current Incremental Address Register r (CIARr) (r = 0 to 17)

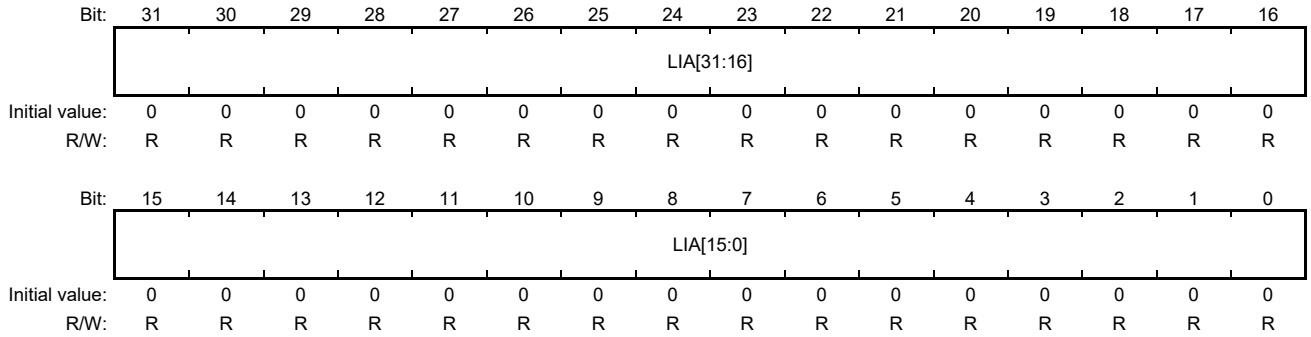
The CIARr register is used to check queue address.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CIA[31:0]	H'0000 0000	R	Current incremental address used by receive queue These bits indicate the incremental address of receive queue r, where currently frame data is stored or where frame data will be stored when queue r gets active. Refer to section 33A.3.4.3(2) Incremental Data Areas. [Changing condition] These bits are set to 0 when leaving OPERATION mode. These bits are updated to next address in incremental data area when processing a FEMPTY_IS or FEMPTY_IC descriptor.

33A.2.21 Last Incremental Address Register r (LIARr) (r = 0 to 17)

The LIARr register is used to check queue address.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LIA[31:0]	H'0000 0000	R	Last incremental address used by receive queue These bits indicate the current incremental address of receive queue r (CIARr.CIA) before its address was updated due to processing a FEMPTY_IS descriptor. So it describes the first not used address inside the incremental data area of receive queue r. Refer to section 33A.3.4.3(2) Incremental Data Areas. [Changing condition] These bits are set to 0 when leaving OPERATION mode. These bits are set to CIARr.CIA when processing a FEMPTY_IS descriptor.

33A.2.22 Transmit Configuration Register (TGC)

The TGC register is used to make settings related to transmission for the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TBD3[1:0]		—	—	TBD2[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TBD1[1:0]		—	—	TBD0[1:0]		—	—	TQP	ECBS	TSM3	TSM2	TSM1	TSM0
Initial value:	0	0	1	0	0	0	1	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
21, 20	TBD3[1:0]	10	R/W	Transmit FIFO Size (Stream Class A) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 3 (for stream class A). Writing to these bits is only possible when the current operating mode is configuration mode. Set these bits to B'10.
19, 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17, 16	TBD2[1:0]	10	R/W	Transmit FIFO Size (Stream Class B) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 2 (for stream class B). Writing to these bits is only possible when the current operating mode is configuration mode. Set these bits to B'10.
15, 14	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
13, 12	TBD1[1:0]	10	R/W	Transmit FIFO Size (Network Control) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 1 (for network control). Writing to these bits is only possible when the current operating mode is configuration mode.
11, 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9, 8	TBD0[1:0]	10	R/W	Transmit FIFO Size (Best Effort) These bits set the sizes of the transmission FIFO buffers for use with each of the transmission queue 0 (for best effort). Writing to these bits is only possible when the current operating mode is configuration mode.
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
5	TQP	0	R/W	Transmission Queues Priority This bit defines how EtherAVB-IF prioritises between transmit queues when scheduling transmission. For fetching always the queue with highest priority is selected, for transmission the queue with highest priority where data is available in Tx-Buffer. Transmission priority of queue 2 and 3 can be influenced by the credit based shaping algorithm. The priority of the transmit queues is given from high to low. 0: Default priority: Q3(CBS), Q2(CBS), Q1, Q0 1: Alternate priority: Q1, Q3(CBS), Q2(CBS), Q0 For the credit-based shaping (CBS) algorithm, see section 33A.3.6 CBS (Credit-Based Shaping). Writing to the bits is only possible when the current operating mode is configuration mode.
4	ECBS	0	R/W	Enable Credit Based Shaping This bit defines if CBS algorithm is used for transmit queue 2 and 3 to prioritise between transmit queues when scheduling transmission. When CBS is enabled, the shaping bases on queue specific configuration in CIVRc, CDVRc, CULc and CLLc. 0: CBS globally disabled 1: CBS enabled based on queue specific configuration For the credit-based shaping (CBS) algorithm, see section 33A.3.6 CBS (Credit-Based Shaping). Writing to the bits is only possible when the current operating mode is configuration mode.
3	TSM3	0	R/W	Transmit Synchronous Mode (Stream Class A) Set these bits to 0. 0: With write-back 1: Setting prohibited
2	TSM2	0	R/W	Transmit Synchronous Mode (Stream Class B) Set these bits to 0. 0: With write-back 1: Setting prohibited
1	TSM1	0	R/W	Transmit Synchronous Mode (Network Control) Set these bits to 0. 0: With write-back 1: Setting prohibited
0	TSM0	0	R/W	Transmit Synchronous Mode (Best Effort) Set these bits to 0. 0: With write-back 1: Setting prohibited

33A.2.23 Transmit Configuration Control Register (TCCR)

The TCCR register controls transmission by the AVB-DMAC and is used to make related settings.

Conditions for updating:

The bit is set to 0 when the operating mode is not operation mode, when a descriptor of type EEMPTY, FEMPTY or LEMPTY (no usable data) is processed, when an EOS descriptor is processed, and when a descriptor with defective data is processed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	MFR	MFEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TFR	TFEN	—	—	—	—	TSRQ3	TSRQ2	TSRQ1	TSRQ0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	MFR	0	R/W	E-MAC status FIFO Release This bit releases the oldest entry of the E-MAC status FIFO. When 1 is written to this bit, EthernetAVB gets informed that CPU has processed the oldest E-MAC status FIFO entry as visible in MFA register. The oldest entry is removed from E-MAC status FIFO. This bit is always read as 0. 0: No request to E-MAC status FIFO 1: Release oldest entry of E-MAC status FIFO
16	MFEN	0	R/W	E-MAC status FIFO ENable This bit enables the storage of transmission status information (the MAC flags for frame transmission) in the E-MAC status FIFO. Additionally CPU can control the status storage for each frame provided for transmission using DESCR.MSR. When this bit is set to 0 all pending FIFO entries are removed. 0: Disabled 1: Enabled
15 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	TFR	0	R/W	Time Stamp FIFO Release This bit releases the oldest entry in the time-stamp FIFO. For a description of how to use the time-stamp FIFO, see section 33A.3.5.4 Time Stamping in Transmission. 0: (Not operating) 1: Releases the oldest entry in the time-stamp FIFO.

Bit	Bit Name	Initial Value	R/W	Description
8	TFEN	0	R/W	Time Stamp FIFO Enable This bit enables storage in the time-stamp FIFO. When it is set, time-stamp information is stored for descriptors with DESCR.TSR set to 1 (for DESCR.TSR, see section 33A.3.5.2(2) Configuration of Transmission Frame Data Descriptors. When 0 is set in this bit, no entries are made in the time-stamp FIFO. For a description of how to use the time-stamp FIFO, see section 33A.3.5.4 Time Stamping in Transmission. 0: Recording of transmission time stamps in the time-stamp FIFO is disabled. 1: Recording of transmission time stamps in the time-stamp FIFO is enabled.
7 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	TSRQ3	0	R/W	Transmit Start Request (Queue 3 (Stream Class A)) This bit issues a request to start transmission for transmission queue 3. When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO. Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission. For the scheduling of transmission queues, see section 33A.3.5.1 Transmission Modes. Writing to this bit is only possible when the current operating mode is operation mode. Only 1 can be written to the bit. Writing 0 to the bit has no effect. 0: Transmission queue is empty or stopped. 1: When written: A transmission start request is issued. When read: Fetching of data for transmission is pending.
2	TSRQ2	0	R/W	Transmit Start Request (Queue 2 (Stream Class B)) This bit issues a request to start transmission for transmission queue 2. When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO. Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission. For the scheduling of transmission queues, see section 33A.3.5.1 Transmission Modes. Writing to this bit is only possible when the current operating mode is operation mode. Only 1 can be written to the bit. Writing 0 to the bit has no effect. 0: Transmission queue is empty or stopped. 1: When written: A transmission start request is issued. When read: Fetching of data for transmission is pending.

Bit	Bit Name	Initial Value	R/W	Description
1	TSRQ1	0	R/W	Transmit Start Request (Queue 1 (Network Control)) This bit issues a request to start transmission for transmission queue 1. When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO. Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission. For the scheduling of transmission queues, see section 33A.3.5.1 Transmission Modes. Writing to this bit is only possible when the current operating mode is operation mode. Only 1 can be written to the bit. Writing 0 to the bit has no effect. 0: Transmission queue is empty or stopped. 1: When written: A transmission start request is issued. When read: Fetching of data for transmission is pending.
0	TSRQ0	0	R/W	Transmit Start Request (Queue 0 (Best Effort)) This bit issues a request to start transmission for transmission queue 0. When read, this bit being set to 1 indicates that transmission queue t has a frame that has not yet been fetched to the transmission FIFO. Frame transmission by the E-MAC is processed independently from fetching to the transmission FIFO. The timing of transmission from a queue depends on the priority order of transmission. For the scheduling of transmission queues, see section 33A.3.5.1 Transmission Modes. Writing to this bit is only possible when the current operating mode is operation mode. Only 1 can be written to the bit. Writing 0 to the bit has no effect. 0: Transmission queue is empty or stopped. 1: When written: A transmission start request is issued. When read: Fetching of data for transmission is pending.

33A.2.24 Transmit Status Register (TSR)

The TSR register indicates the state of transmission by the AVB-DMAC.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	MFFL[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

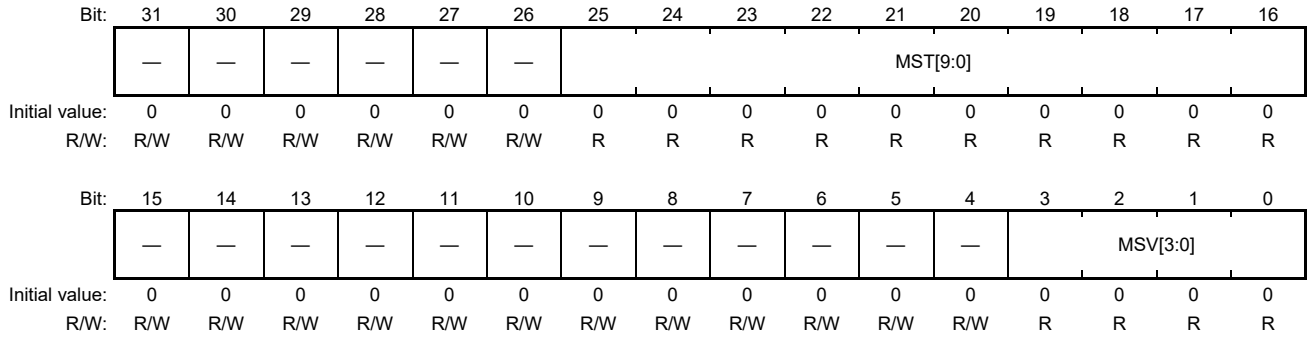
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TFFL[2:0]			—	—	—	—	CCS1[1:0]		CCS0[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 21	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
20 to 16	MFFL[4:0]	H'00	R	Number of entries stored in the E-MAC status FIFO E-MAC status FIFO Fill Level These bits indicate the number of entries available in the MAC status FIFO. If this value is 0, the FIFO is empty. If this value is 16, the FIFO is full. The values 17 to 31 are reserved. [Changing condition] These bits are set to 0 when leaving OPERATION mode. These bits are set to 0 when TCCR.MFEN is 0. This value is incremented when frame with DESCR.MSR has been transmitted by E-MAC, TCCR.MFEN is 1 and TSR.MFFL is not 16. This value is incremented when E-MAC detects an error during transmission, TCCR.MFEN is 1 and TSR.MFFL is not 16. This value is decremented when 1 is written to TCCR.MFR and TSR.MFFL is not 0.
15 to 11	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
10 to 8	TFFL[2:0]	00	R	Time Stamp FIFO Count These bits indicate the number of time stamps in the time-stamp FIFO. The values 0 and 3 indicate that the time-stamp FIFO is empty and full, respectively (values 4 to 7 are reserved). Conditions for updating: • The bits are set to 0 when the operating mode is not operation mode and when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) = 0. • When the time stamp FIFO enable bit (TCCR.TFEN) is 1 and these bits are not 3, the value of these bits is incremented after a frame with DESCR.TSR set has been transmitted by the E-MAC (for DESCR.TSR, see section 33A.3.5.2(2) Configuration of Transmission Frame Data Descriptors. • The value of these bits is decremented if it is not 0 when 1 is written to the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR).

Bit	Bit Name	Initial Value	R/W	Description
7 to 4	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
3, 2	CCS1[1:0]	00	R	CBS Counter Status 1 (Class A) These bits indicate the CBS (credit-based shaping) state of stream data transmission queue 1. If the calculated credit value is outside the range specified by CBS upper limit register c (CULc) and CBS lower limit register c (CLLc), it falls outside the range for CBS. Conditions for updating: • The bits are set to B'00 when the operating mode is not operation mode. The bits are set to B'00 when the CBS is inside the condition limits. • The bits are set to B'01 if the credit value calculated by the CBS is lower than the value in CBS lower limit register c (CLLc). • The bits are set to B'10 if the credit value calculated by the CBS is higher than the value in CBS upper limit register c (CULc). 00: The current credit value is within the limit. 01: The current credit value is less than or equal to the lower limit. 10: The current credit value is greater than or equal to the upper limit. 11: (Reserved)
1, 0	CCS0[1:0]	00	R	CBS Counter Status 0 (Class B) These bits indicate the CBS (credit-based shaping) state of stream data transmission queue 0. If the calculated credit value is outside the range specified by CBS upper limit register c (CULc) and CBS lower limit register c (CLLc), it falls outside the range for CBS. Conditions for updating: • The bits are set to B'00 when the operating mode is not operation mode. The bits are set to B'00 when the CBS is inside the condition limits. • The bits are set to B'01 if the credit value calculated by the CBS is lower than the value in CBS lower limit register c (CLLc). • The bits are set to B'10 if the credit value calculated by the CBS is higher than the value in CBS upper limit register c (CULc). 00: The current credit value is within the limit. 01: The current credit value is less than or equal to the lower limit. 10: The current credit value is greater than or equal to the upper limit. 11: (Reserved)

33A.2.25 E-MAC status FIFO Access register (MFA)

The MFA register indicates the state of MAC.



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	MST[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R

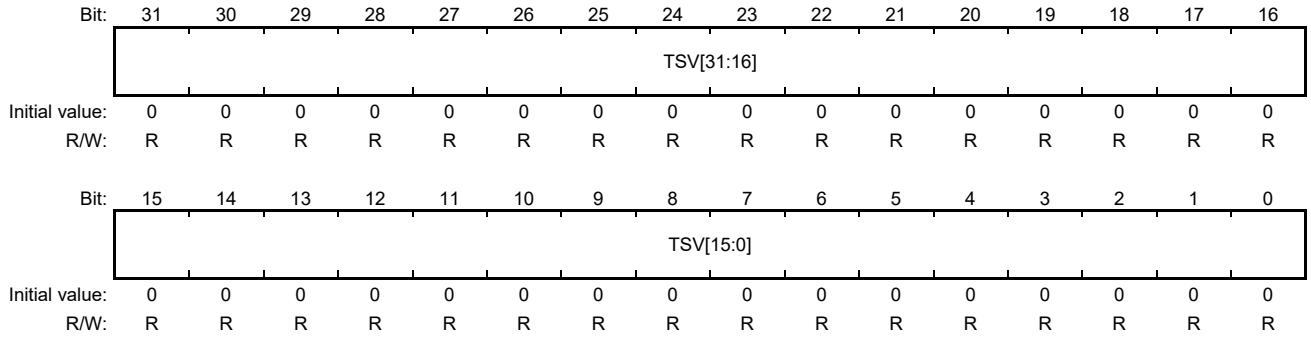
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MSV[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
25 to 16	MST[9:0]	H'000	R	Tag number from descriptor identifying the frame E-MAC status relation E-MAC Status Tag These bits represent the DESCR.TAG bits from the descriptor defining the data for frame transmission. The tag is used to get the relation between the frame inside a transmit queue and the E-MAC status available in the FIFO (MFA.MSV). The CPU should not read these bits when TSR.MFFL is 0. [Changing condition] These bits are updated when the first entry is stored in FIFO (TSR.MFFL changes from 0 to 1). These bits are updated when the oldest entry is released (writing 1 to TCCR.MFR). These bits are updated when the FIFO is overwritten (a frame with DESCR.MSR in descriptor has been transmitted by MAC, TCCR.MFEN is 1 and TSR.MFFL is 16). These bits are updated when the FIFO is overwritten (E-MAC detects an error during transmission and TSR.MFFL is 16). Note for verification: These bits are set to 0 when leaving OPERATION mode.
15 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	MSV[3:0]	H'0	R	E-MAC Status Value These bits represent the E-MAC status bits as stored in the oldest E-MAC status FIFO entry. MSV[3] Reserved MSV[2] Carrier lost during frame transmission MSV[1] Delay collision MSV[0] Transmission time out The CPU should not read these bits when TSR.MFFL is 0. [Changing condition] These bits are updated when the first entry is stored in FIFO (TSR.MFFL changes from 0 to 1). These bits are updated when the oldest entry is released (writing 1 to TCCR.MFR). These bits are updated when the FIFO overwritten (a frame with DESCR.MSR in descriptor has been transmitted by E-MAC, TCCR.MFEN is 1 and TSR.MFFL is 16). These bits are updated when the FIFO is overwritten (E-MAC detects an error during transmission and TSR.MFFL is 16). Note for verification: These bits are set to 0 when leaving OPERATION mode.

33A.2.26 Time Stamp FIFO Access Register 0 (TFA0)

TFA0 indicates the nano seconds portion of the timestamp value.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSV[31:0]	H'0000 0000	R	Time Stamp Value These 80 bits consist of TFA0.TSV[31:0], TFA1.TSV[63:32], and TFA2.TSV[79:64], which together indicate the oldest time stamp value stored in the time-stamp FIFO. Once the time-stamp FIFO is full, no further time-stamp values are stored. Conditions for updating: • The bits are set to H'0000 0000 when the operating mode is not operation mode. • The register is updated whenever a value is stored in the time-stamp FIFO (when the time-stamp FIFO count bit in the transmit status register (TSR.TFFL) changes from 0 to 1). • The register is updated when the oldest entry is released (when the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR) is set to 1).

33A.2.27 Time Stamp FIFO Access Register 1 (TFA1)

The TFA1 register indicates the lower seconds portion of the timestamp value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSV[63:48]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSV[47:32]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TSV[63:32]	H'0000 0000	R	Time Stamp Value For details, see section 33A.2.26 Time Stamp FIFO Access Register 0 (TFA0).

33A.2.28 Time Stamp FIFO Access Register 2 (TFA2)

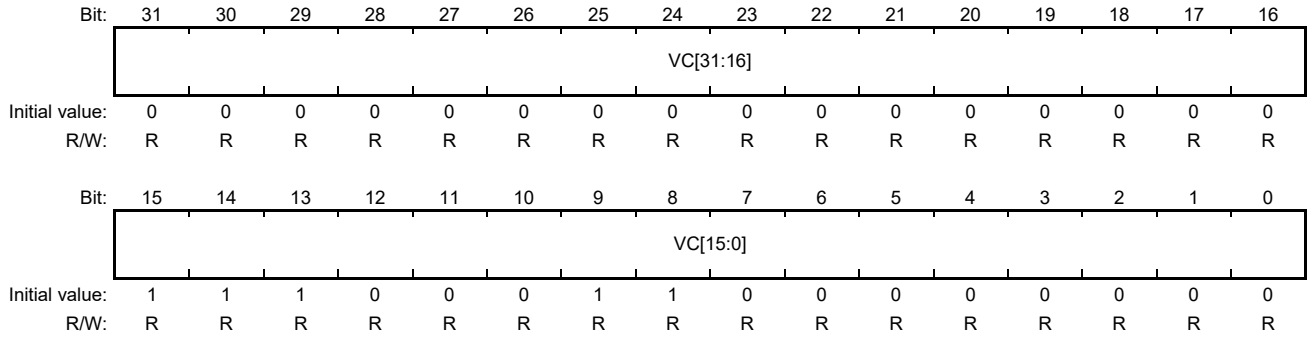
The TFA2 register indicates the timestamp tag and the higher seconds portion of the timestamp value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	TST[9:0]									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSV[79:64]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved These bits are read as 0.
25 to 16	TST[9:0]	H'000	R	Time Stamp Tag These bits indicate the contents of the DESCR.TAG bit within the descriptor for frame transmission. These values are used to check the correlation between frames within the transmission queue and the time-stamp values (accessible through time stamp FIFO access register i (TFAi)) which can be placed in the FIFO. For the tagging of frames in transmission, see section 33A.3.5.4 Time Stamping in Transmission. Conditions for updating: • The bits are set to H'000 when the operating mode is not operation mode. • Updated when a value is stored in the time-stamp FIFO (when the value of the time stamp FIFO count bit in the transmit status register (TSR.TFFL) changes from 0 to 1). • Updated when the oldest entry has been released (1 is set in the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR)).
15 to 0	TSV[79:64]	H'0000	R	Time Stamp Value For details, see section 33A.2.26 Time Stamp FIFO Access Register 0 (TFA0).

33A.2.29 Version and Release Register (VRR)

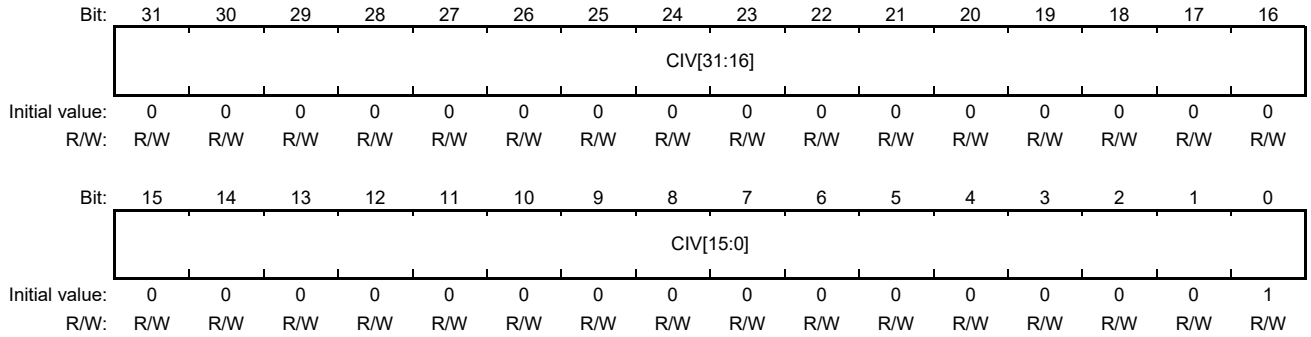


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	VC[31:0]	H'0000 E300	R	Version Code These bits identify the version of used EthernetAVB. H'0000 E300: RAVBES3

33A.2.30 CBS Increment Value Register c (CIVRc) (c = 0 or 1)

The CIVR0 register sets the increment in the CBS algorithm for transmission queue 2 (for stream class B).

The CIVR1 register sets the increment in the CBS algorithm for transmission queue 3 (for stream class A).

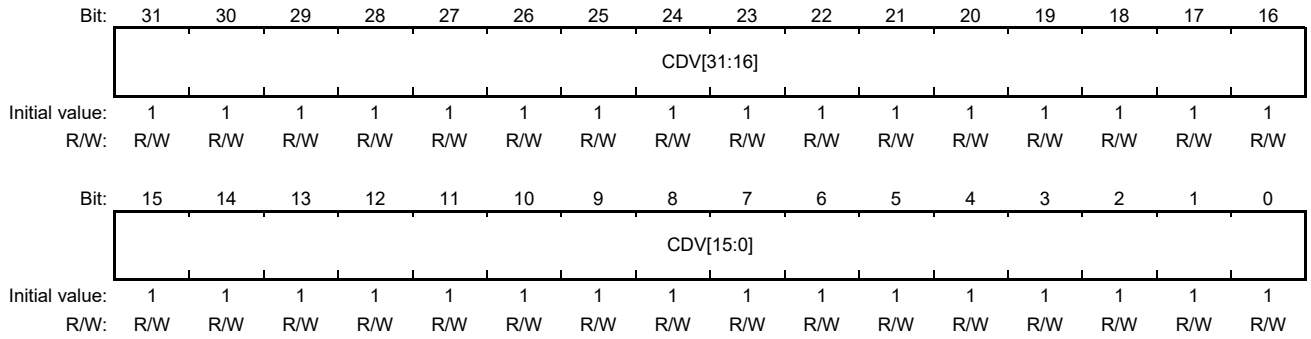


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CIV[31:0]	H'0000 0001	R/W	CBS Increment Value CBS increment value (1 to H'FFFF) These bits define the increment value related to idleSlope for the CBS algorithm. Set a value in the range from H'0000 0001 to H'0000 FFFF. The value to be written to these bits depends on the Ethernet bit rate and HPϕ (high-speed peripheral clock). For details, see section 33A.3.6 CBS (Credit-Based Shaping).

33A.2.31 CBS Decrement Value Register c (CDVRc) (c = 0 or 1)

The CDVR0 register sets the decrement in the CBS algorithm for transmission queue 2 (for stream class B).

The CDVR1 register sets the decrement in the CBS algorithm for transmission queue 3 (for stream class A).

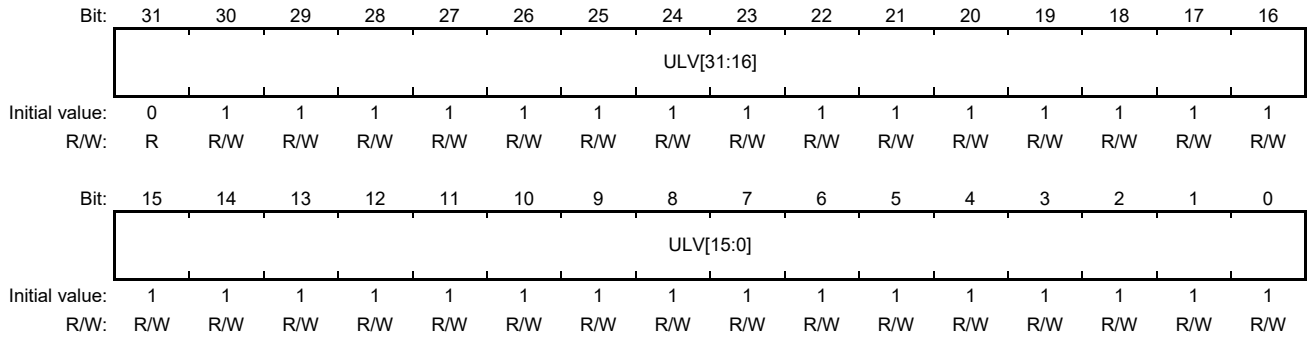


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CDV[31:0]	H'FFFF FFFF	R/W	CBS Decrement Value Setting value: -1 to -65536 (H'FFFF FFFF to H'FFFF 0000) These bits set the decrement for the CBS algorithm. These bits define the decrement value related to sendSlope for CBS algorithm. The value to be written to these bits depends on the Ethernet bit rate and HPϕ (high-speed peripheral clock). For details, see section 33A.3.6 CBS (Credit-Based Shaping).

33A.2.32 CBS Upper Limit Register c (CULc) (c = 0 or 1)

The CUL0 register sets the upper limit for credit values calculated by using the CBS algorithm for transmission queue 2 (for stream class B).

The CUL1 register sets the upper limit for credit values calculated by using the CBS algorithm for transmission queue 3 (for stream class A).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	ULV[31:0]	H'7FFF FFFF	R/W	CBS Upper Limit These bits set the upper limit for credit values calculated by using the CBS algorithm. The setting is a limiting value for error detection and does not normally affect operation of the algorithm. Write a positive value to these bits. For details, see section 33A.3.6 CBS (Credit-Based Shaping). Note: The write value to the bit 31 should always be 0.

33A.2.33 CBS Lower Limit Register c (CLLc) (c = 0 or 1)

The CUL0 register sets the lower limit for credit values calculated by using the CBS algorithm for transmission queue 2 (for stream class B).

The CUL1 register sets the lower limit for credit values calculated by using the CBS algorithm for transmission queue 3 (for stream class A).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LLV[31:16]															
Initial value:	1	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LLV[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	LLV[31:0]	H'8000 0001	R/W	CBS Lower Limit These bits set the lower limit for credit values calculated by using the CBS algorithm. The setting is a limiting value for error detection and does not normally affect operation of the algorithm. Write a negative value to these bits. For details, see section 33A.3.6 CBS (Credit-Based Shaping). Note: The write value to the bit 31 should always be 1.

33A.2.34 Descriptor Interrupt Control Register (DIC)

The DIC register is used to control descriptor interrupts 1 to 15.

When an interrupt source flag is set (a bit from DPF1 to DPF15 bits in the descriptor interrupt status register (DIS) = 1) while the interrupt is enabled, the interrupt is issued.

[Changing condition]

This bit is set to 0 when writing 1 to DID.DPDi.

This bit is set to 1 when writing 1 to DIE.DPSi.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPE15	DPE14	DPE13	DPE12	DPE11	DPE10	DPE9	DPE8	DPE7	DPE6	DPE5	DPE4	DPE3	DPE2	DPE1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPE15	0	R/W	Descriptor Interrupt Enable 15 0: Disabled 1: Enabled
14	DPE14	0	R/W	Descriptor Interrupt Enable 14 0: Disabled 1: Enabled
13	DPE13	0	R/W	Descriptor Interrupt Enable 13 0: Disabled 1: Enabled
12	DPE12	0	R/W	Descriptor Interrupt Enable 12 0: Disabled 1: Enabled
11	DPE11	0	R/W	Descriptor Interrupt Enable 11 0: Disabled 1: Enabled
10	DPE10	0	R/W	Descriptor Interrupt Enable 10 0: Disabled 1: Enabled
9	DPE9	0	R/W	Descriptor Interrupt Enable 9 0: Disabled 1: Enabled
8	DPE8	0	R/W	Descriptor Interrupt Enable 8 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
7	DPE7	0	R/W	Descriptor Interrupt Enable 7 0: Disabled 1: Enabled
6	DPE6	0	R/W	Descriptor Interrupt Enable 6 0: Disabled 1: Enabled
5	DPE5	0	R/W	Descriptor Interrupt Enable 5 0: Disabled 1: Enabled
4	DPE4	0	R/W	Descriptor Interrupt Enable 4 0: Disabled 1: Enabled
3	DPE3	0	R/W	Descriptor Interrupt Enable 3 0: Disabled 1: Enabled
2	DPE2	0	R/W	Descriptor Interrupt Enable 2 0: Disabled 1: Enabled
1	DPE1	0	R/W	Descriptor Interrupt Enable 1 0: Disabled 1: Enabled
0	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.

33A.2.35 Descriptor Interrupt Status Register (DIS)

The DIS register indicates the state of descriptor interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPF15	DPF14	DPF13	DPF12	DPF11	DPF10	DPF9	DPF8	DPF7	DPF6	DPF5	DPF4	DPF3	DPF2	DPF1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPF15	0	R/W	Descriptor Interrupt Status15 0: The interrupt is not pending. 1: The interrupt is pending.
14	DPF14	0	R/W	Descriptor Interrupt Status14 0: The interrupt is not pending. 1: The interrupt is pending.
13	DPF13	0	R/W	Descriptor Interrupt Status13 0: The interrupt is not pending. 1: The interrupt is pending.
12	DPF12	0	R/W	Descriptor Interrupt Status12 0: The interrupt is not pending. 1: The interrupt is pending.
11	DPF11	0	R/W	Descriptor Interrupt Status11 0: The interrupt is not pending. 1: The interrupt is pending.
10	DPF10	0	R/W	Descriptor Interrupt Status10 0: The interrupt is not pending. 1: The interrupt is pending.
9	DPF9	0	R/W	Descriptor Interrupt Status9 0: The interrupt is not pending. 1: The interrupt is pending.
8	DPF8	0	R/W	Descriptor Interrupt Status8 0: The interrupt is not pending. 1: The interrupt is pending.
7	DPF7	0	R/W	Descriptor Interrupt Status7 0: The interrupt is not pending. 1: The interrupt is pending.
6	DPF6	0	R/W	Descriptor Interrupt Status6 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
5	DPF5	0	R/W	Descriptor Interrupt Status5 0: The interrupt is not pending. 1: The interrupt is pending.
4	DPF4	0	R/W	Descriptor Interrupt Status4 0: The interrupt is not pending. 1: The interrupt is pending.
3	DPF3	0	R/W	Descriptor Interrupt Status3 0: The interrupt is not pending. 1: The interrupt is pending.
2	DPF2	0	R/W	Descriptor Interrupt Status2 0: The interrupt is not pending. 1: The interrupt is pending.
1	DPF1	0	R/W	Descriptor Interrupt Status1 0: The interrupt is not pending. 1: The interrupt is pending.
0	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.

DPF1 to DPF15 Descriptor Interrupt Status Bits:

When DESCR.DIE is 1 to 15, the corresponding bit indicates completion of the processing of a descriptor within the reception or transmission queue.

When DESCR.DIE is 0, the descriptor interrupt is not generated.

When DESCR.DIE is B'0001, in addition a queue specific descriptor interrupt is generated.

Only 0 can be written to these bits.

[Conditions for Changing]

— A bit is set to 0 when the operating mode is not operation mode.
— A bit is set to 1 when a descriptor with DESCR.DIE set to the corresponding number from 1 to 15 is processed.

33A.2.36 Error Interrupt Control Register (EIC)

The EIC register controls the AVB-DMAC-related error interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TBFE	MFFE	TFFE	CULE1	CULE0	CLLE1	CLLE0	SEE	QEE	MTEE	MREE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10	TBFE	0	R/W	Tx-Buffer Full interrupt Enable While this bit is 1 an interrupt will be generated when EIS.TBFF is 1. [Changing condition] This bit is set to 0 when writing 1 to EID.TBFD. This bit is set to 1 when writing 1 to EIE.TBFS. 0: Disabled 1: Enabled
9	MFFE	0	R/W	MAC status FIFO Full interrupt Enable While this bit is 1 an interrupt will be generated when EIS.MFFF is 1. [Changing condition] This bit is set to 0 when writing 1 to EID.MFFD. This bit is set to 1 when writing 1 to EIE.MFFS. 0: Disabled 1: Enabled
8	TFFE	0	R/W	Time Stamp FIFO Full-Error Interrupt Enable When the time stamp FIFO is full (TFFF in the error interrupt status register (EIS) = 1) and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to EID.TFFD. This bit is set to 1 when writing 1 to EIE.TFFS. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
7	CULE1	0	R/W	CBS Upper Limit Error Interrupt Enable (Class A) When the Class A CBS reaches its upper limit (CULF1 in the error interrupt status register (EIS) = 1), the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to EID.CULD1. This bit is set to 1 when writing 1 to EIE.CULS1. 0: Disabled 1: Enabled
6	CULE0	0	R/W	CBS Upper Limit Error Interrupt Enable (Class B) When the Class B CBS reaches its upper limit (CULF0 in the error interrupt status register (EIS) = 1), the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to EID.CULD0. This bit is set to 1 when writing 1 to EIE.CULS0. 0: Disabled 1: Enabled
5	CLLE1	0	R/W	CBS Lower Limit Error Interrupt Enable (Class A) When the Class A CBS reaches its lower limit (CLLF1 in the error interrupt status register (EIS) = 1), the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to EID.CLLD1. This bit is set to 1 when writing 1 to EIE.CLLS1. 0: Disabled 1: Enabled
4	CLLE0	0	R/W	CBS Lower Limit Error Interrupt Enable (Class B) When the Class B CBS reaches its lower limit (CLLF0 in the error interrupt status register (EIS) = 1), the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to EID.CLLD0. This bit is set to 1 when writing 1 to EIE.CLLS0. 0: Disabled 1: Enabled
3	SEE	0	R/W	Separation Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.SEF bit is 1. [Changing condition] This bit is set to 0 when writing 1 to EID.SED. This bit is set to 1 when writing 1 to EIE.SES. 0: Disabled 1: Enabled
2	QEE	0	R/W	Queue Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.QEF bit is 1. [Changing condition] This bit is set to 0 when writing 1 to EID.QED. This bit is set to 1 when writing 1 to EIE.QES. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
1	MTEE	0	R/W	E-MAC Transmission Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.MTEF bit is 1. [Changing condition] This bit is set to 0 when writing 1 to EID.MTED. This bit is set to 1 when writing 1 to EIE.MTES. 0: Disabled 1: Enabled
0	MREE	0	R/W	E-MAC Reception Error Interrupt Enable While this bit is 1, an interrupt will be generated when the EIS.MREF bit is 1. [Changing condition] This bit is set to 0 when writing 1 to EID.MRED. This bit is set to 1 when writing 1 to EIE.MRES. 0: Disabled 1: Enabled

33A.2.37 Error Interrupt Status Register (EIS)

The EIS register indicates the states of AVB-DMAC-related error interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	QFS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TBFF	MFFF	TFFF	CULF1	CULF0	CLLF1	CLLF0	SEF	QEF	MTEF	MREF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 17	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
16	QFS	0	R/W	Queue Full Error Interrupt Status With the interrupts enabled, this bit indicates that a queue is full (the receive queue r full interrupt status bit (QFFr) or the receive FIFO full interrupt status bit (RFFF) in receive interrupt status register 2 (RIS2) = 1). [Conditions for Changing] — If the receive queue r full interrupt status bit (RIS2.QFFr) and/or the receive queue r full interrupt enable bit in the - receive interrupt control register 2 (RIC2.QFEr) are updated, this bit is also updated. — If the receive FIFO full interrupt status bit (RIS2.RFFF) and/or the receive FIFO full interrupt enable bit (RIC2.RFFE) are updated, this bit is also updated. 0: The interrupt is not pending. 1: The interrupt is pending.
15 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10	TBFF	0	R/W	Tx-Buffer Full Flag This bit indicates that fetching transmit data was delayed because the Tx-Buffer has no sufficient storage available to store fetched frame. It depends on configuration of TGC.TBDt (refer to section 33A.3.5.1) if a full Tx-Buffer is expected during normal operation. No frame gets lost but transmission priority may be influenced. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when frame data has been fetched from URAM but there is no storage available in Tx-Buffer. 0: No interrupt pending 1: Tx-Buffer full condition detected

Bit	Bit Name	Initial Value	R/W	Description
9	MFFF	0	R/W	E-MAC status FIFO Full Flag This bit indicates that a transmission E-MAC status is overwritten because the E-MAC status FIFO is full (overwrite condition). The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a frame with DESCR.MSR has been transmitted by E-MAC, TCCR.MFEN is 1 and TSR.MFFL is 16. This bit is set to 1 when E-MAC detects an error during transmission and TSR.MFFL is 16. 0: No interrupt pending 1: E-MAC status FIFO full, oldest E-MAC status lost
8	TFFF	0	R/W	Time Stamp FIFO Full Error Interrupt Status This bit indicates that a new transmission time stamp has been discarded due to the time-stamp FIFO being full (i.e. has reached the overflow state). Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when a frame with DESCR.TSR set is transmitted while the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is set to 1 and the time stamp FIFO count bit in the transmit status register (TSR.TFFL) is set to 3. 0: The interrupt is not pending. 1: The interrupt is pending.
7	CULF1	0	R/W	CBS Upper Limit Error Interrupt Status (Class A) This bit indicates that CBS counter 1 has exceeded the set upper limit (CUL1.ULV in the CBS upper limit register c (CULc)). Only 0 can be written to the bit. [Conditions for Changing] — This bit is set to 0 when the operating mode is not operation mode. — This bit is set to 1 when the value of the CBS counter status 1 (Class A) bits in the transmit status register (TSR.CCS1) change from B'00 (indicating a value within the range between the limits) to B'10 (indicating a value over the upper limit). 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
6	CULF0	0	R/W	CBS Upper Limit Error Interrupt Status (Class B) This bit indicates that CBS counter 0 has exceeded the set upper limit (CUL0.ULV in the CBS upper limit register c (CULc)). Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when the value of the CBS counter status 0 (Class B) bit in the transmit status register changes from B'00 (indicating a value within the range between the limits) to B'10 (indicating a value over the upper limit). 0: The interrupt is not pending. 1: The interrupt is pending.
5	CLLF1	0	R/W	CBS Lower Limit Error Interrupt Status (Class A) This bit indicates that CBS counter 1 has fallen below the set lower limit (CLL1.LLV in CBS lower limit register c (CLLc)). Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when the value of the CBS counter status 1 (Class A) bit in the transmit status register (TSR.CCS1) changes from B'00 (indicating a value within the range between the limits) to B'01 (indicating a value less than the lower limit). 0: The interrupt is not pending. 1: The interrupt is pending.
4	CLLF0	0	R/W	CBS Lower Limit Error Interrupt Status (Class B) This bit indicates that CBS counter 0 has fallen below the set lower limit (CLL0.LLV in the CBS lower limit register c (CLLc)). Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when the value of the CBS counter status 0 (Class B) bit in the transmit status register (TSR.CCS0) changes from B'00 (indicating a value within the range between the limits) to B'01 (indicating a value less than the lower limit). 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
3	SEF	0	R/W	Separation Error Flag This bit indicates that a received frame was discarded because it has not matched any configurated separation filter for AVB stream data frames. The CPU can only write 0 to this bit. [Conditions for Changing] — This bit is set to 0 when leaving operation mode. — This bit is set to 1 when a valid AVB stream data frame was received by E-MAC but discarded because the RCR.ESF bits are B'10 and no separation filter has matched. 0: No interrupt pending. 1: AVB stream data frame has discarded.
2	QEF	0	R/W	Queue Error Flag This bit indicates that an error has been detected while processing reception or transmit queue or while processing AVTP FIFO entries. Details about the detected error is indicated by ESR. Section 33A.3.2.2 gives an overview of detail error conditions and the required interaction. The CPU can only write 0 to this bit. [Conditions for Changing] — This bit is set to 0 when leaving operating mode. — This bit is set to 1 when an error condition is detected. 0: No interrupt pending. 1: Interrupt pending.
1	MTEF	0	R/W	E-MAC Transmission Error Flag This bit indicates that the E-MAC has detected a fault during transmission. For detail, the E-MAC registers have to be checked. The CPU can only write 0 to this bit. [Conditions for Changing] — This bit is set to 0 when leaving operating mode. — This bit is set to 1 when E-MAC detects an error during frame transmission. 0: No interrupt pending. 1: E-MAC has reported an error during transmission.

Bit	Bit Name	Initial Value	R/W	Description
0	MREF	0	R/W	E-MAC Reception Error Flag This bit indicates that the E-MAC has detected a fault during reception. For detail, the E-MAC registers have to be checked. Note: When the storage of faulty received frames (RCR.EFFS) is enabled, the E-MAC error code (DESCR.MSC) is stored in the descriptor. By evaluating this information, CPU can identify corrupted frames in URAM. The CPU can only write 0 to this bit. [Conditions for Changing] — This bit is set to 0 when leaving operating mode. — This bit is set to 1 when E-MAC detects an error during frame reception. 0: No interrupt pending. 1: E-MAC has reported an error during reception.

33A.2.38 Receive Interrupt Control Register 0 (RIC0)

The RIC0 register controls the AVB-DMAC receive interrupts.

When an interrupt source flag is set (a bit from among the receive interrupt status bits in the receive interrupt status register (RIS0.FRF0 to 17) = 1) while the interrupt is enabled, the interrupt is issued.

[Changing condition]

This bit is set to 0 when writing 1 to RID0.FRDr.

This bit is set to 1 when writing 1 to RIE0.FRSr.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRE17	FRE16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRE15	FRE14	FRE13	FRE12	FRE11	FRE10	FRE9	FRE8	FRE7	FRE6	FRE5	FRE4	FRE3	FRE2	FRE1	FRE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	FRE17	0	R/W	Receive Frame Enable 17 (Stream) 0: Disabled 1: Enabled
16	FRE16	0	R/W	Receive Frame Enable 16 (Stream) 0: Disabled 1: Enabled
15	FRE15	0	R/W	Receive Frame Enable 15 (Stream) 0: Disabled 1: Enabled
14	FRE14	0	R/W	Receive Frame Enable 14 (Stream) 0: Disabled 1: Enabled
13	FRE13	0	R/W	Receive Frame Enable 13 (Stream) 0: Disabled 1: Enabled
12	FRE12	0	R/W	Receive Frame Enable 12 (Stream) 0: Disabled 1: Enabled
11	FRE11	0	R/W	Receive Frame Enable 11 (Stream) 0: Disabled 1: Enabled
10	FRE10	0	R/W	Receive Frame Enable 10 (Stream) 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
9	FRE9	0	R/W	Receive Frame Enable 9 (Stream) 0: Disabled 1: Enabled
8	FRE8	0	R/W	Receive Frame Enable 8 (Stream) 0: Disabled 1: Enabled
7	FRE7	0	R/W	Receive Frame Enable 7 (Stream) 0: Disabled 1: Enabled
6	FRE6	0	R/W	Receive Frame Enable 6 (Stream) 0: Disabled 1: Enabled
5	FRE5	0	R/W	Receive Frame Enable 5 (Stream) 0: Disabled 1: Enabled
4	FRE4	0	R/W	Receive Frame Enable 4 (Stream) 0: Disabled 1: Enabled
3	FRE3	0	R/W	Receive Frame Enable 3 (Stream) 0: Disabled 1: Enabled
2	FRE2	0	R/W	Receive Frame Enable 2 (Stream) 0: Disabled 1: Enabled
1	FRE1	0	R/W	Receive Frame Enable 1 (Network Control) 0: Disabled 1: Enabled
0	FRE0	0	R/W	Receive Frame Enable 0 (Best Effort) 0: Disabled 1: Enabled

33A.2.39 Receive Interrupt Status Register 0 (RIS0)

The RIS0 register indicates the states of the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRF17	FRF16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRF15	FRF14	FRF13	FRF12	FRF11	FRF10	FRF9	FRF8	FRF7	FRF6	FRF5	FRF4	FRF3	FRF2	FRF1	FRF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	FRF17	0	R/W	Receive Frame Interrupt Status 17 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
16	FRF16	0	R/W	Receive Frame Interrupt Status 16 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
15	FRF15	0	R/W	Receive Frame Interrupt Status 15 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
14	FRF14	0	R/W	Receive Frame Interrupt Status 14 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
13	FRF13	0	R/W	Receive Frame Interrupt Status 13 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
12	FRF12	0	R/W	Receive Frame Interrupt Status 12 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
11	FRF11	0	R/W	Receive Frame Interrupt Status 11 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
10	FRF10	0	R/W	Receive Frame Interrupt Status 10 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
9	FRF9	0	R/W	Receive Frame Interrupt Status 9 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
8	FRF8	0	R/W	Receive Frame Interrupt Status 8 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
7	FRF7	0	R/W	Receive Frame Interrupt Status 7 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
6	FRF6	0	R/W	Receive Frame Interrupt Status 6 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
5	FRF5	0	R/W	Receive Frame Interrupt Status 5 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
4	FRF4	0	R/W	Receive Frame Interrupt Status 4 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
3	FRF3	0	R/W	Receive Frame Interrupt Status 3 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
2	FRF2	0	R/W	Receive Frame Interrupt Status 2 (Stream) 0: The interrupt is not pending. 1: The interrupt is pending.
1	FRF1	0	R/W	Receive Frame Interrupt Status 1 (Network Control) 0: The interrupt is not pending. 1: The interrupt is pending.
0	FRF0	0	R/W	Receive Frame Interrupt Status 0 (Best Effort) 0: The interrupt is not pending. 1: The interrupt is pending.

FRF0 to FRF17 Receive Frame Interrupt Status Bits 0 to 17:

Each bit indicates that a corresponding frame has been stored normally in reception queues 0 to 17 and that data are ready for CPU processing.

Only 0 can be written to the bit.

[Conditions for Changing]

- A bit is set to 0 when the operating mode is not operation mode.
- A bit is set to 0 when a value is written to the unread frame counter decrement register i (UFCDi) (i = 0 to 4), and this decrements the value of unread frame counter register i (UFCVi) (i = 0 to 4) to 0.
- When a frame is stored normally in a reception queue, the corresponding bit is set to 1.

33A.2.40 Receive Interrupt Control Register 1 (RIC1)

The RIC1 register controls the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFWE	—	—	—	—	—	—	—	—	—	—	—	—	—	RWE17	RWE16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RWE15	RWE14	RWE13	RWE12	RWE11	RWE10	RWE9	RWE8	RWE7	RWE6	RWE5	RWE4	RWE3	RWE2	RWE1	RWE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFWE	0	R/W	Receive FIFO Warning Interrupt Enable If the reception FIFO reaches the caution level (the value set in the receive FIFO caution level bits in the receive configuration register (RCR.RFCL)) with the corresponding interrupt enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID1.RFWD. This bit is set to 1 when writing 1 to RIE1.RFWS. 0: Disabled 1: Enabled
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RWE17	0	R/W	Reception Warning interrupt Enable 17 While this bit is 1 an interrupt will be generated when RIS1.RWF17 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD17. This bit is set to 1 when writing 1 to RIE1.RWS17. 0: Disabled 1: Enabled
16	RWE16	0	R/W	Reception Warning interrupt Enable 16 While this bit is 1 an interrupt will be generated when RIS1.RWF16 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD16. This bit is set to 1 when writing 1 to RIE1.RWS16. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
15	RWE15	0	R/W	Reception Warning interrupt Enable 15 While this bit is 1 an interrupt will be generated when RIS1.RWF15 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD15. This bit is set to 1 when writing 1 to RIE1.RWS15. 0: Disabled 1: Enabled
14	RWE14	0	R/W	Reception Warning interrupt Enable 14 While this bit is 1 an interrupt will be generated when RIS1.RWF14 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD14. This bit is set to 1 when writing 1 to RIE1.RWS14. 0: Disabled 1: Enabled
13	RWE13	0	R/W	Reception Warning interrupt Enable 13 While this bit is 1 an interrupt will be generated when RIS1.RWF13 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD13. This bit is set to 1 when writing 1 to RIE1.RWS13. 0: Disabled 1: Enabled
12	RWE12	0	R/W	Reception Warning interrupt Enable 17 While this bit is 1 an interrupt will be generated when RIS1.RWF12 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD12. This bit is set to 1 when writing 1 to RIE1.RWS12. 0: Disabled 1: Enabled
11	RWE11	0	R/W	Reception Warning interrupt Enable 11 While this bit is 1 an interrupt will be generated when RIS1.RWF11 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD11. This bit is set to 1 when writing 1 to RIE1.RWS11. 0: Disabled 1: Enabled
10	RWE10	0	R/W	Reception Warning interrupt Enable 10 While this bit is 1 an interrupt will be generated when RIS1.RWF10 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD10. This bit is set to 1 when writing 1 to RIE1.RWS10. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
9	RWE9	0	R/W	Reception Warning interrupt Enable 9 While this bit is 1 an interrupt will be generated when RIS1.RWF9 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD9. This bit is set to 1 when writing 1 to RIE1.RWS9. 0: Disabled 1: Enabled
8	RWE8	0	R/W	Reception Warning interrupt Enable 8 While this bit is 1 an interrupt will be generated when RIS1.RWF8 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD18. This bit is set to 1 when writing 1 to RIE1.RWS18. 0: Disabled 1: Enabled
7	RWE7	0	R/W	Reception Warning interrupt Enable 7 While this bit is 1 an interrupt will be generated when RIS1.RWF7 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD7. This bit is set to 1 when writing 1 to RIE1.RWS7. 0: Disabled 1: Enabled
6	RWE6	0	R/W	Reception Warning interrupt Enable 6 While this bit is 1 an interrupt will be generated when RIS1.RWF6 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD6. This bit is set to 1 when writing 1 to RIE1.RWS6. 0: Disabled 1: Enabled
5	RWE5	0	R/W	Reception Warning interrupt Enable 5 While this bit is 1 an interrupt will be generated when RIS1.RWF5 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD5. This bit is set to 1 when writing 1 to RIE1.RWS5. 0: Disabled 1: Enabled
4	RWE4	0	R/W	Reception Warning interrupt Enable 4 While this bit is 1 an interrupt will be generated when RIS1.RWF4 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD4. This bit is set to 1 when writing 1 to RIE1.RWS4. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
3	RWE3	0	R/W	Reception Warning interrupt Enable 3 While this bit is 1 an interrupt will be generated when RIS1.RWF3 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD3. This bit is set to 1 when writing 1 to RIE1.RWS3. 0: Disabled 1: Enabled
2	RWE2	0	R/W	Reception Warning interrupt Enable 2 While this bit is 1 an interrupt will be generated when RIS1.RWF2 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD2. This bit is set to 1 when writing 1 to RIE1.RWS2. 0: Disabled 1: Enabled
1	RWE1	0	R/W	Reception Warning interrupt Enable 1 While this bit is 1 an interrupt will be generated when RIS1.RWF1 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD1. This bit is set to 1 when writing 1 to RIE1.RWS1. 0: Disabled 1: Enabled
0	RWE0	0	R/W	Reception Warning interrupt Enable 0 While this bit is 1 an interrupt will be generated when RIS1.RWF0 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID1.RWD0. This bit is set to 1 when writing 1 to RIE1.RWS0. 0: Disabled 1: Enabled

33A.2.41 Receive Interrupt Status Register 1 (RIS1)

The RIS1 register indicates the states of the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFWF	—	—	—	—	—	—	—	—	—	—	—	—	—	RWF17	RWF16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RWF15	RWF14	RWF13	RWF12	RWF11	RWF10	RWF9	RWF8	RWF7	RWF6	RWF5	RWF4	RWF3	RWF2	RWF1	RWF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFWF	0	R/W	Receive FIFO Warning Interrupt Status This bit indicates that the reception FIFO has exceeded the set caution level (the value set in the receive FIFO caution level bits in the receive configuration register (RCR.RFCL)). Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when the reception FIFO exceeded the set caution level (the value set in the receive FIFO caution level bits in the receive configuration register (RCR.RFCL)). 0: The interrupt is not pending. 1: The interrupt is pending.
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RWF17	0	R/W	Reception Warning Flag 17 This bit indicates that the unread frame counter of receive queue 17 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA21 is 1). This bit is set to 0 when CPU writes to UFCD4.DV1 and UFCV4.CV1 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV4.CV1 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

Bit	Bit Name	Initial Value	R/W	Description
16	RWF16	0	R/W	Reception Warning Flag 16 This bit indicates that the unread frame counter of receive queue 16 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA20 is 1). This bit is set to 0 when CPU writes to UFCD4.DV0 and UFCV4.CV0 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV4.CV0 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
15	RWF15	0	R/W	Reception Warning Flag 15 This bit indicates that the unread frame counter of receive queue 15 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA19 is 1). This bit is set to 0 when CPU writes to UFCD3.DV3 and UFCV3.CV3 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV3.CV3 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
14	RWF14	0	R/W	Reception Warning Flag 14 This bit indicates that the unread frame counter of receive queue 14 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA18 is 1). This bit is set to 0 when CPU writes to UFCD3.DV2 and UFCV3.CV2 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV3.CV2 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

Bit	Bit Name	Initial Value	R/W	Description
13	RWF13	0	R/W	Reception Warning Flag 13 This bit indicates that the unread frame counter of receive queue 13 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA17 is 1). This bit is set to 0 when CPU writes to UFCD3.DV1 and UFCV3.CV1 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV3.CV1 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
12	RWF12	0	R/W	Reception Warning Flag 12 This bit indicates that the unread frame counter of receive queue 12 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA16 is 1). This bit is set to 0 when CPU writes to UFCD3.DV0 and UFCV3.CV0 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV3.CV0 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
11	RWF11	0	R/W	Reception Warning Flag 11 This bit indicates that the unread frame counter of receive queue 11 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA15 is 1). This bit is set to 0 when CPU writes to UFCD2.DV3 and UFCV2.CV3 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV2.CV3 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

Bit	Bit Name	Initial Value	R/W	Description
10	RWF10	0	R/W	Reception Warning Flag 10 This bit indicates that the unread frame counter of receive queue 10 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA14 is 1). This bit is set to 0 when CPU writes to UFCD2.DV2 and UFCV2.CV2 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV2.CV2 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
9	RWF9	0	R/W	Reception Warning Flag 9 This bit indicates that the unread frame counter of receive queue 9 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA13 is 1). This bit is set to 0 when CPU writes to UFCD2.DV1 and UFCV2.CV1 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV2.CV1 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
8	RWF8	0	R/W	Reception Warning Flag 8 This bit indicates that the unread frame counter of receive queue 8 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA12 is 1). This bit is set to 0 when CPU writes to UFCD2.DV0 and UFCV2.CV0 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV2.CV0 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

Bit	Bit Name	Initial Value	R/W	Description
7	RWF7	0	R/W	Reception Warning Flag 7 This bit indicates that the unread frame counter of receive queue 7 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA11 is 1). This bit is set to 0 when CPU writes to UFCD1.DV3 and UFCV1.CV3 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV1.CV3 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
6	RWF6	0	R/W	Reception Warning Flag 6 This bit indicates that the unread frame counter of receive queue 6 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA10 is 1). This bit is set to 0 when CPU writes to UFCD1.DV2 and UFCV1.CV2 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV1.CV2 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
5	RWF5	0	R/W	Reception Warning Flag 5 This bit indicates that the unread frame counter of receive queue 5 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA9 is 1). This bit is set to 0 when CPU writes to UFCD1.DV1 and UFCV1.CV1 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV1.CV1 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

Bit	Bit Name	Initial Value	R/W	Description
4	RWF4	0	R/W	Reception Warning Flag 4 This bit indicates that the unread frame counter of receive queue 4 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA8 is 1). This bit is set to 0 when CPU writes to UFCD1.DV0 and UFCV1.CV0 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV1.CV0 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
3	RWF3	0	R/W	Reception Warning Flag 3 This bit indicates that the unread frame counter of receive queue 3 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA7 is 1). This bit is set to 0 when CPU writes to UFCD0.DV3 and UFCV0.CV3 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV0.CV3 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
2	RWF2	0	R/W	Reception Warning Flag 2 This bit indicates that the unread frame counter of receive queue 2 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA6 is 1). This bit is set to 0 when CPU writes to UFCD0.DV2 and UFCV0.CV2 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV0.CV2 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

Bit	Bit Name	Initial Value	R/W	Description
1	RWF1	0	R/W	Reception Warning Flag 1 This bit indicates that the unread frame counter of receive queue 1 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA5 is 1). This bit is set to 0 when CPU writes to UFCD0.DV1 and UFCV0.CV1 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV0.CV1 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached
0	RWF0	0	R/W	Reception Warning Flag 0 This bit indicates that the unread frame counter of receive queue 0 has reached the configured warning level. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when CPU request a reload of the base address (DLR.LBA4 is 1). This bit is set to 0 when CPU writes to UFCD0.DV0 and UFCV0.CV0 is decremented to a value less than the selected warning level UFCW.WLj. This bit is set to 1 when a frame is stored in queue r and the unread frame counter value r is incremented to the selected warning level j (UFCV0.CV0 + 1 == UFCW.WLj). 0: No interrupt pending 1: Unread frame counter warning level reached

33A.2.42 Receive Interrupt Control Register 2 (RIC2)

The RIC2 register controls the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFFE	—	—	—	—	—	—	—	—	—	—	—	—	—	QFE17	QFE16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QFE15	QFE14	QFE13	QFE12	QFE11	QFE10	QFE9	QFE8	QFE7	QFE6	QFE5	QFE4	QFE3	QFE2	QFE1	QFE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFFE	0	R/W	Receive FIFO Full Interrupt Enable When the reception FIFO is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.RFFD. This bit is set to 1 when writing 1 to RIE2.RFFS. 0: Disabled 1: Enabled
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	QFE17	0	R/W	Receive Queue 17 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD17. This bit is set to 1 when writing 1 to RIE2.QFS17. 0: Disabled 1: Enabled
16	QFE16	0	R/W	Receive Queue 16 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD16. This bit is set to 1 when writing 1 to RIE2.QFS16. 0: Disabled 1: Enabled
15	QFE15	0	R/W	Receive Queue 15 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD15. This bit is set to 1 when writing 1 to RIE2.QFS15. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
14	QFE14	0	R/W	Receive Queue 14 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD14. This bit is set to 1 when writing 1 to RIE2.QFS14. 0: Disabled 1: Enabled
13	QFE13	0	R/W	Receive Queue 13 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD13. This bit is set to 1 when writing 1 to RIE2.QFS13. 0: Disabled 1: Enabled
12	QFE12	0	R/W	Receive Queue 12 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD12. This bit is set to 1 when writing 1 to RIE2.QFS12. 0: Disabled 1: Enabled
11	QFE11	0	R/W	Receive Queue 11 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD11. This bit is set to 1 when writing 1 to RIE2.QFS11. 0: Disabled 1: Enabled
10	QFE10	0	R/W	Receive Queue 10 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD10. This bit is set to 1 when writing 1 to RIE2.QFS10. 0: Disabled 1: Enabled
9	QFE9	0	R/W	Receive Queue 9 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD9. This bit is set to 1 when writing 1 to RIE2.QFS9. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
8	QFE8	0	R/W	Receive Queue 8 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD8. This bit is set to 1 when writing 1 to RIE2.QFS8. 0: Disabled 1: Enabled
7	QFE7	0	R/W	Receive Queue 7 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD7. This bit is set to 1 when writing 1 to RIE2.QFS7. 0: Disabled 1: Enabled
6	QFE6	0	R/W	Receive Queue 6 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD6. This bit is set to 1 when writing 1 to RIE2.QFS6. 0: Disabled 1: Enabled
5	QFE5	0	R/W	Receive Queue 5 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD5. This bit is set to 1 when writing 1 to RIE2.QFS5. 0: Disabled 1: Enabled
4	QFE4	0	R/W	Receive Queue 4 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD4. This bit is set to 1 when writing 1 to RIE2.QFS4. 0: Disabled 1: Enabled
3	QFE3	0	R/W	Receive Queue 3 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD3. This bit is set to 1 when writing 1 to RIE2.QFS3. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
2	QFE2	0	R/W	Receive Queue 2 (Stream) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD2. This bit is set to 1 when writing 1 to RIE2.QFS2. 0: Disabled 1: Enabled
1	QFE1	0	R/W	Receive Queue 1 (Network Control) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD1. This bit is set to 1 when writing 1 to RIE2.QFS1. 0: Disabled 1: Enabled
0	QFE0	0	R/W	Receive Queue 0 (Best Effort) Full Interrupt Enable When a reception queue is full and the interrupt is enabled, the interrupt is issued. [Changing condition] This bit is set to 0 when writing 1 to RID2.QFD0. This bit is set to 1 when writing 1 to RIE2.QFS0. 0: Disabled 1: Enabled

33A.2.43 Receive Interrupt Status Register 2 (RIS2)

The RIS2 register indicates the states of the AVB-DMAC receive interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFFF	—	—	—	—	—	—	—	—	—	—	—	—	—	QFF17	QFF16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QFF15	QFF14	QFF13	QFF12	QFF11	QFF10	QFF9	QFF8	QFF7	QFF6	QFF5	QFF4	QFF3	QFF2	QFF1	QFF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFFF	0	R/W	Receive FIFO Full Interrupt Status This bit indicates that a frame was received but storing it was not possible due to the reception FIFO being full. When receiving a frame is not possible, the frame will be discarded. Other information regarding discarded frames is not retained. Even if the frame is discarded, this bit may also be set to 1 if the E-MAC determines that the frame is an error frame Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when frame data provided by the E-MAC cannot be stored in the reception FIFO. 0: The interrupt is not pending. 1: The interrupt is pending
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	QFF17	0	R/W	Receive Queue 17 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
16	QFF16	0	R/W	Receive Queue 16 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
15	QFF15	0	R/W	Receive Queue 15 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
14	QFF14	0	R/W	Receive Queue 14 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
13	QFF13	0	R/W	Receive Queue 13 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
12	QFF12	0	R/W	Receive Queue 12 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
11	QFF11	0	R/W	Receive Queue 11 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
10	QFF10	0	R/W	Receive Queue 10 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
9	QFF9	0	R/W	Receive Queue 9 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
8	QFF8	0	R/W	Receive Queue 8 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
7	QFF7	0	R/W	Receive Queue 7 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
6	QFF6	0	R/W	Receive Queue 6 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
5	QFF5	0	R/W	Receive Queue 5 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
4	QFF4	0	R/W	Receive Queue 4 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
3	QFF3	0	R/W	Receive Queue 3 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
2	QFF2	0	R/W	Receive Queue 2 (Stream) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
1	QFF1	0	R/W	Receive Queue 1 (Network Control) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.
0	QFF0	0	R/W	Receive Queue 0 (Best Effort) Full Interrupt Status 0: The interrupt is not pending. 1: The interrupt is pending.

QFF0 to 17 Receive 0 to 17 Full Interrupt Status Bits:

These bits indicate that reception queue r did not have space for storing a received frame.

A reception queue is treated as full when it has no descriptors (descriptor type (DESCR.DT) = FEMPTY, FEMPTY_IS, FEMPTY_IC, or FEMPTY_ND) available or reaches the set level for stopping.

Note: If no FEMPTY descriptors or no empty space for descriptors remains in the queue during storing of a divided frame (see section 33A.3.4.3(1) Storing Frame Data in the Descriptor Data Area, for storing a frame as a divided frame), an error frame is stored in the queue. Such error frames are treated as descriptor sequence errors.

[Conditions for Changing]

- A bit is set to 0 when the operating mode is not operation mode.
- A bit is set to 1 when reception queue r has no space available for storage.
- A bit is set to 1 when a SW defined stop point (EOS descriptor) reached within a split frame.
- A bit is set to 1 when the unread frame counter (unread frame counter register i (UFCVi) (i = 0 to 4)) reaches the set level for stopping.

33A.2.44 Transmit Interrupt Control Register (TIC)

The TIC register controls the AVB-DMAC transmit interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TDPE3	TDPE2	TDPE1	TDPE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MFWE	MFUE	TFWE	TFUE	—	—	—	—	FTE3	FTE2	FTE1	FTE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
19	TDPE3	0	R/W	Transmit Descriptor Processed interrupt Enable 3 While this bit is 1 an interrupt will be generated when TIS.TDPF3 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.TDPD3. This bit is set to 1 when writing 1 to TIE.TDPS3. 0: Disabled 1: Enabled
18	TDPE2	0	R/W	Transmit Descriptor Processed interrupt Enable 2 While this bit is 1 an interrupt will be generated when TIS.TDPF2 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.TDPD2. This bit is set to 1 when writing 1 to TIE.TDPS2. 0: Disabled 1: Enabled
17	TDPE1	0	R/W	Transmit Descriptor Processed interrupt Enable 1 While this bit is 1 an interrupt will be generated when TIS.TDPF1 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.TDPD1. This bit is set to 1 when writing 1 to TIE.TDPS1. 0: Disabled 1: Enabled
16	TDPE0	0	R/W	Transmit Descriptor Processed interrupt Enable 0 While this bit is 1 an interrupt will be generated when TIS.TDPF0 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.TDPD0. This bit is set to 1 when writing 1 to TIE.TDPS0. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
11	MFWE	0	R/W	MAC status FIFO Warning interrupt Enable While this bit is 1 an interrupt will be generated when TIS.MFWF is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.MFWD. This bit is set to 1 when writing 1 to TIE.MFWS. 0: Disabled 1: Enabled
10	MFUE	0	R/W	MAC status FIFO Updated interrupt Enable While this bit is 1 an interrupt will be generated when TIS.MFUF is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.MFUD. This bit is set to 1 when writing 1 to TIE.MFUS. 0: Disabled 1: Enabled
9	TFWE	0	R/W	Time Stamp FIFO Warning Interrupt Enable When the time-stamp FIFO reaches the warning level while the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
8	TFUE	0	R/W	Time Stamp FIFO Update Interrupt Enable When the time-stamp FIFO is updated while the interrupt is enabled, the interrupt is issued. 0: Disabled 1: Enabled
7 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	FTE3	0	R/W	Frame Transmitted interrupt Enable 3 While this bit is 1 an interrupt will be generated when TIS.FTF3 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.FTD3. This bit is set to 1 when writing 1 to TIE.FTS3. 0: Disabled 1: Enabled
2	FTE2	0	R/W	Frame Transmitted interrupt Enable 2 While this bit is 1 an interrupt will be generated when TIS.FTF2 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.FTD2. This bit is set to 1 when writing 1 to TIE.FTS2. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
1	FTE1	0	R/W	Frame Transmitted interrupt Enable 1 While this bit is 1 an interrupt will be generated when TIS.FTF1 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.FTD1. This bit is set to 1 when writing 1 to TIE.FTS1. 0: Disabled 1: Enabled
0	FTE0	0	R/W	Frame Transmitted interrupt Enable 0 While this bit is 1 an interrupt will be generated when TIS.FTF0 is 1. [Changing condition] This bit is set to 0 when writing 1 to TID.FTD0. This bit is set to 1 when writing 1 to TIE.FTS0. 0: Disabled 1: Enabled

33A.2.45 Transmit Interrupt Status Register (TIS)

The TIS register indicates the states of the AVB-DMAC transmit interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TDPF3	TDPF2	TDPF1	TDPF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MFWF	MFUF	TFWF	TFUF	—	—	—	—	FTF3	FTF2	FTF1	FTF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
19	TDPF3	0	R/W	Transmit Descriptor Processed Flag 3 This bit indicates that a descriptor in transmit queue 3 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in transmit queue 3 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
18	TDPF2	0	R/W	Transmit Descriptor Processed Flag 2 This bit indicates that a descriptor in transmit queue 2 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in transmit queue 2 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending

Bit	Bit Name	Initial Value	R/W	Description
17	TDPF1	0	R/W	Transmit Descriptor Processed Flag 1 This bit indicates that a descriptor in transmit queue 1 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in transmit queue 1 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
16	TDPF0	0	R/W	Transmit Descriptor Processed Flag 0 This bit indicates that a descriptor in transmit queue 0 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in transmit queue 0 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
15 to 12	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
11	MFWF	0	R/W	E-MAC status FIFO Warning Flag This bit indicates that the warning level of the E-MAC status FIFO (12 out of 16 entries) has been reached. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when TCCR.MFEN is 0. This bit is set to 0 when writing 1 to TCCR.MFR. This bit is set to 1 when a frame with DESCR.MSR has been transmitted by E-MAC and the E-MAC Status FIFO contains already 11 entries (TSR.MFFL is 11). This bit is set to 1 when E-MAC detects an error during transmission and the E-MAC Status FIFO contains already 11 entries (TSR.MFFL is 11). 0: No interrupt pending 1: Tx Status FIFO warning level has been reached

Bit	Bit Name	Initial Value	R/W	Description
10	MFUF	0	R/W	E-MAC status FIFO Updated Flag This bit indicates that the E-MAC status FIFO has been updated after the E-MAC has transmitted a frame. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 0 when TCCR.MFEN is 0. This bit is set to 0 when writing 1 to TCCR.MFR. This bit is set to 1 when a frame with DESCR.MSR has been transmitted by E-MAC and TCCR.MFEN is 1. This bit is set to 1 when E-MAC detects an error during transmission and TCCR.MFEN is 1. 0: No interrupt pending 1: Tx Status FIFO has been updated
9	TFWF	0	R/W	Time Stamp FIFO Warning Interrupt Status This bit indicates that the transmission time-stamp FIFO has reached the warning level. Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode and when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0. — The bit is set to 1 after a frame including DESCR.TSR set has been transmitted and one entry has already been stored in the time-stamp FIFO. 0: The interrupt is not pending. 1: The time-stamp FIFO has reached the warning level.
8	TFUF	0	R/W	Time Stamp FIFO Update Interrupt Status This bit indicates that the transmission time-stamp FIFO has been updated. Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode, when the time stamp FIFO enable bit in the transmit configuration control register (TCCR.TFEN) is 0, and when 1 is written to the time stamp FIFO release bit in the transmit configuration control register (TCCR.TFR). — The bit is set to 1 when the time stamp FIFO enable bit (TCCR.TFEN) is 1 after a frame including DESCR.TSR set has been transmitted. 0: The interrupt is not pending. 1: The time-stamp FIFO has been updated.
7 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
3	FTF3	0	R/W	Frame Transmitted Flag 3 This bit indicates that from transmit queue a frame is transmitted by E-MAC. Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (DIS.DPFi) refers to the end of processing storage element. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a frame from transmit queue 3 has been transmitted by the E-MAC. 0: No interrupt pending 1: Frame transmitted by E-MAC
2	FTF2	0	R/W	Frame Transmitted Flag 2 This bit indicates that from transmit queue a frame is transmitted by E-MAC. Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (DIS.DPFi) refers to the end of processing storage element. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a frame from transmit queue 2 has been transmitted by the E-MAC. 0: No interrupt pending 1: Frame transmitted by E-MAC
1	FTF1	0	R/W	Frame Transmitted Flag 1 This bit indicates that from transmit queue a frame is transmitted by E-MAC. Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (DIS.DPFi) refers to the end of processing storage element. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a frame from transmit queue 1 has been transmitted by the E-MAC. 0: No interrupt pending 1: Frame transmitted by E-MAC

Bit	Bit Name	Initial Value	R/W	Description
0	FTF0	0	R/W	Frame Transmitted Flag 0 This bit indicates that from transmit queue a frame is transmitted by E-MAC. Note: This interrupt flag refers to the end of frame transmission by E-MAC whereas the descriptor interrupt (DIS.DPFi) refers to the end of processing storage element. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a frame from transmit queue 0 has been transmitted by the E-MAC. 0: No interrupt pending 1: Frame transmitted by E-MAC

33A.2.46 Interrupt Summary Status Register (ISS)

The ISS register gives a summary of the states of AVB-DMAC-related interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DPM15	DPM14	DPM13	DPM12	DPM11	DPM10	DPM9	DPM8	DPM7	DPM6	DPM5	DPM4	DPM3	DPM2	DPM1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	CGIM	RFWM	MFWM	MFUM	TFWM	TFUM	MM	EM	—	—	—	FTM	RWM	FRM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	DPM15	0	R	Descriptor Interrupt 15 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE15) and descriptor interrupt status flag (DIS.DPF15) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
30	DPM14	0	R	Descriptor Interrupt 14 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE14) and descriptor interrupt status flag (DIS.DPF14) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
29	DPM13	0	R	Descriptor Interrupt 13 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE13) and descriptor interrupt status flag (DIS.DPF13) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
28	DPM12	0	R	Descriptor Interrupt 12 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE12) and descriptor interrupt status flag (DIS.DPF12) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
27	DPM11	0	R	Descriptor Interrupt 11 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE11) and descriptor interrupt status flag (DIS.DPF11) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
26	DPM10	0	R	Descriptor Interrupt 10 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE10) and descriptor interrupt status flag (DIS.DPF10) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
25	DPM9	0	R	Descriptor Interrupt 9 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE9) and descriptor interrupt status flag (DIS.DPF9) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
24	DPM8	0	R	Descriptor Interrupt 8 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE8) and descriptor interrupt status flag (DIS.DPF8) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
23	DPM7	0	R	Descriptor Interrupt 7 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE7) and descriptor interrupt status flag (DIS.DPF7) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
22	DPM6	0	R	Descriptor Interrupt 6 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE6) and descriptor interrupt status flag (DIS.DPF6) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
21	DPM5	0	R	Descriptor Interrupt 5 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE5) and descriptor interrupt status flag (DIS.DPF5) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
20	DPM4	0	R	Descriptor Interrupt 4 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE4) and descriptor interrupt status flag (DIS.DPF4) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
19	DPM3	0	R	Descriptor Interrupt 3 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE3) and descriptor interrupt status flag (DIS.DPF3) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
18	DPM2	0	R	Descriptor Interrupt 2 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE2) and descriptor interrupt status flag (DIS.DPF2) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
17	DPM1	0	R	Descriptor Interrupt 1 Mirror This bit is set to 1 when the given descriptor interrupt enable bit (DIC.DPE1) and descriptor interrupt status flag (DIS.DPF1) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
16 to 14	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
13	CGIM	0	R	gPTP Interrupt Mirror This bit is set to 1 when either interrupt-related bit in the two gPTP-related interrupt registers (GIC and GIS) is 1. 0: The interrupt is not pending. 1: The interrupt is pending.
12	RFWM	0	R	Receive FIFO Warning Interrupt Mirror This bit is set to 1 when the receive FIFO warning interrupt enable bit (RIC1.RFWE) and receive FIFO warning interrupt status flag (RIS1.RFWF) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
11	MFWM	0	R	E-MAC status FIFO Warning Mirror This bit indicates that TIS.MFWF is 1 and TIC.MFWE is 1. [Changing condition] This bit is updated when TIS.MFWF or TIC.MFWE changes. 0: No interrupt pending 1: E-MAC status FIFO warning interrupt pending
10	MFUM	0	R	E-MAC status FIFO Updated Mirror This bit indicates that TIS.MFUF is 1 and TIC.MFUE is 1. [Changing condition] This bit is updated when TIS.MFUF or TIC.MFUE changes. 0: No interrupt pending 1: E-MAC status FIFO updated interrupt pending
9	TFWM	0	R	Time Stamp FIFO Warning Interrupt Mirror This bit is set to 1 when the time stamp FIFO warning interrupt enable bit (TIC.TFWE) and time stamp FIFO warning interrupt status flag (TIS.TFWF) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
8	TFUM	0	R	Time Stamp FIFO Update Mirror This bit is set to 1 when the time stamp FIFO update interrupt enable bit (TIC.TFUE) and time stamp FIFO update interrupt status flag (TIS.TFUF) are both 1. 0: The interrupt is not pending. 1: The interrupt is pending.
7	MM	0	R	E-MAC Interrupt Mirror This bit is set to 1 when an E-MAC interrupt is issued. 0: The interrupt is not pending. 1: The interrupt is pending.

Bit	Bit Name	Initial Value	R/W	Description
6	EM	0	R	Error Interrupt Mirror This bit is set to 1 when an error interrupt is issued (both of a bit in EIS and corresponding to the bit in EIC are 1). 0: The interrupt is not pending. 1: The interrupt is pending.
5 to 3	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
2	FTM	0	R	Frame Transmitted Mirror [Changing condition] This bit is set when any matching pair of TIC.FTEt enable and TIS.FTFt flag are both 1. This bit is set when any matching pair of TIC.TDPEt enable and TIS.TDPFt flag are both 1. 0: No interrupt pending 1: Frame transmitted interrupt pending
1	RWM	0	R	Reception Warning Mirror [Changing condition] This bit is set when any matching pair of RIC1.RWEr enable and RIS1.RWFr flag are both 1. 0: No interrupt pending 1: Frame transmitted interrupt pending
0	FRM	0	R	Frame Received Mirror [Changing condition] This bit is set when any matching pair of RIC0.FREr enable and RIS0.FRFr flag are both 1. This bit is set when any matching pair of RIC3.RDPEr enable and RIS3.RDPFr flag are both 1. 0: No interrupt pending 1: Frame received interrupt pending

33A.2.47 Common Interrupt Enable register (CIE)

The CIE register is used to control the Common Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	RFFL	RFWL	CL0M	RQFM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	CTIE	—	—	—	—	—	—	—	CRIE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
19	RFFL	0	R/W	Rx-FIFO Full interrupt Line select This bit selects the interrupt line of notification flagged by RIS2.RFFF. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
18	RFWL	0	R/W	Rx-FIFO Warning interrupt Line select This bit selects the interrupt line of notification flagged by RIS1.RFWF. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
17	CL0M	0	R/W	Common Line 0 Mode This bit controls if all data related interrupts using a common interrupt line or if queue specific interrupt lines for data related interrupts are used. The selected mode has no influence to internal flagging in EthernetAVB register (e.g. ISS). To prevent interrupt notifications on different lines, it is recommended to set all CIE.CTIE, CIE.CRIE, and DIL.DPLi (i=2 to 15) to 0 when this bit is 1. 0: Use common interrupt line 0 1: Use queue specific interrupt line 0
16	RQFM	0	R/W	Reception Queue Full Mode This bit controls if queue full notification is mapped to error interrupt line or to queue data interrupt line. The selected mode has no influence to internal flagging in EthernetAVB register (e.g. ISS). 0: Use for error interrupt line 1: Use for queue specific interrupt line
15 to 9	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
8	CTIE	0	R/W	Common Transmit Interrupt Enable This bit controls transmit related interrupt line outputs of EthernetAVB. It has no influence to internal flagging in EthernetAVB register (e.g. ISS). These lines are controlled by this bit: line0_Tx[3:0] -- individual transmit queue interrupts Transmission interrupts mapped on other lines are not influenced. 0: Disabled 1: Enabled
7 to 1	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
0	CRIE	0	R/W	Common Receive Interrupt enable This bit controls receive related interrupt line outputs of EthernetAVB. It has no influence to internal flagging in EthernetAVB register (e.g. ISS). These lines are controlled by this bit: line0_Rx[17:0] -- individual receive queue interrupts Receive interrupts mapped on other lines are not influenced. 0: Disabled 1: Enabled

33A.2.48 Reception Interrupt Control register 3 (RIC3)

The RIC3 register controls the AVB-DMAC receive descriptor interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDPE17	RDPE16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDPE15	RDPE14	RDPE13	RDPE12	RDPE11	RDPE10	RDPE9	RDPE8	RDPE7	RDPE6	RDPE5	RDPE4	RDPE3	RDPE2	RDPE1	RDPE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RDPE17	0	R/W	Receive Descriptor Processed interrupt Enable 17 While this bit is 1 an interrupt will be generated when RIS3.RDPF17 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD17. This bit is set to 1 when writing 1 to RIE3.RDPS17. 0: Disabled 1: Enabled
16	RDPE16	0	R/W	Receive Descriptor Processed interrupt Enable 16 While this bit is 1 an interrupt will be generated when RIS3.RDPF16 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD16. This bit is set to 1 when writing 1 to RIE3.RDPS16. 0: Disabled 1: Enabled
15	RDPE15	0	R/W	Receive Descriptor Processed interrupt Enable 15 While this bit is 1 an interrupt will be generated when RIS3.RDPF15 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD15. This bit is set to 1 when writing 1 to RIE3.RDPS15. 0: Disabled 1: Enabled
14	RDPE14	0	R/W	Receive Descriptor Processed interrupt Enable 14 While this bit is 1 an interrupt will be generated when RIS3.RDPF14 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD14. This bit is set to 1 when writing 1 to RIE3.RDPS14. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
13	RDPE13	0	R/W	Receive Descriptor Processed interrupt Enable 13 While this bit is 1 an interrupt will be generated when RIS3.RDPF13 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD13. This bit is set to 1 when writing 1 to RIE3.RDPS13. 0: Disabled 1: Enabled
12	RDPE12	0	R/W	Receive Descriptor Processed interrupt Enable 12 While this bit is 1 an interrupt will be generated when RIS3.RDPF12 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD12. This bit is set to 1 when writing 1 to RIE3.RDPS12. 0: Disabled 1: Enabled
11	RDPE11	0	R/W	Receive Descriptor Processed interrupt Enable 11 While this bit is 1 an interrupt will be generated when RIS3.RDPF11 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD11. This bit is set to 1 when writing 1 to RIE3.RDPS11. 0: Disabled 1: Enabled
10	RDPE10	0	R/W	Receive Descriptor Processed interrupt Enable 10 While this bit is 1 an interrupt will be generated when RIS3.RDPF10 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD10. This bit is set to 1 when writing 1 to RIE3.RDPS10. 0: Disabled 1: Enabled
9	RDPE9	0	R/W	Receive Descriptor Processed interrupt Enable 9 While this bit is 1 an interrupt will be generated when RIS3.RDPF9 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD9. This bit is set to 1 when writing 1 to RIE3.RDPS9. 0: Disabled 1: Enabled
8	RDPE8	0	R/W	Receive Descriptor Processed interrupt Enable 8 While this bit is 1 an interrupt will be generated when RIS3.RDPF8 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD8. This bit is set to 1 when writing 1 to RIE3.RDPS8. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
7	RDPE7	0	R/W	Receive Descriptor Processed interrupt Enable 7 While this bit is 1 an interrupt will be generated when RIS3.RDPF7 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD7. This bit is set to 1 when writing 1 to RIE3.RDPS7. 0: Disabled 1: Enabled
6	RDPE6	0	R/W	Receive Descriptor Processed interrupt Enable 6 While this bit is 1 an interrupt will be generated when RIS3.RDPF6 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD6. This bit is set to 1 when writing 1 to RIE3.RDPS6. 0 Disabled 1 Enabled
5	RDPE5	0	R/W	Receive Descriptor Processed interrupt Enable 5 While this bit is 1 an interrupt will be generated when RIS3.RDPF5 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD5. This bit is set to 1 when writing 1 to RIE3.RDPS5. 0: Disabled 1: Enabled
4	RDPE4	0	R/W	Receive Descriptor Processed interrupt Enable 4 While this bit is 1 an interrupt will be generated when RIS3.RDPF4 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD4. This bit is set to 1 when writing 1 to RIE3.RDPS4. 0: Disabled 1: Enabled
3	RDPE3	0	R/W	Receive Descriptor Processed interrupt Enable 3 While this bit is 1 an interrupt will be generated when RIS3.RDPF3 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD3. This bit is set to 1 when writing 1 to RIE3.RDPS3. 0: Disabled 1: Enabled
2	RDPE2	0	R/W	Receive Descriptor Processed interrupt Enable 2 While this bit is 1 an interrupt will be generated when RIS3.RDPF2 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD2. This bit is set to 1 when writing 1 to RIE3.RDPS2. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
1	RDPE1	0	R/W	Receive Descriptor Processed interrupt Enable 1 While this bit is 1 an interrupt will be generated when RIS3.RDPF1 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD1. This bit is set to 1 when writing 1 to RIE3.RDPS1. 0: Disabled 1: Enabled
0	RDPE0	0	R/W	Receive Descriptor Processed interrupt Enable 0 While this bit is 1 an interrupt will be generated when RIS3.RDPF0 is 1. [Changing condition] This bit is set to 0 when writing 1 to RID3.RDPD0. This bit is set to 1 when writing 1 to RIE3.RDPS0. 0: Disabled 1: Enabled

33A.2.49 Reception Interrupt Status register 3 (RIS3)

The RIS3 register indicates the states of the AVB-DMAC receive descriptor interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDPF17	RDPF16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDPF15	RDPF14	RDPF13	RDPF12	RDPF11	RDPF10	RDPF9	RDPF8	RDPF7	RDPF6	RDPF5	RDPF4	RDPF3	RDPF2	RDPF1	RDPF0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RDPF17	0	R/W	Receive Descriptor Processed Flag 17 This bit indicates that a descriptor in reception queue 17 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 17 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
16	RDPF16	0	R/W	Receive Descriptor Processed Flag 16 This bit indicates that a descriptor in reception queue 16 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 16 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending

Bit	Bit Name	Initial Value	R/W	Description
15	RDPF15	0	R/W	Receive Descriptor Processed Flag 15 This bit indicates that a descriptor in reception queue 15 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 15 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
14	RDPF14	0	R/W	Receive Descriptor Processed Flag 14 This bit indicates that a descriptor in reception queue 14 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 14 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
13	RDPF13	0	R/W	Receive Descriptor Processed Flag 13 This bit indicates that a descriptor in reception queue 13 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 13 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
12	RDPF12	0	R/W	Receive Descriptor Processed Flag 12 This bit indicates that a descriptor in reception queue 12 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 12 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending

Bit	Bit Name	Initial Value	R/W	Description
11	RDPF11	0	R/W	Receive Descriptor Processed Flag 11 This bit indicates that a descriptor in reception queue 11 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 11 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
10	RDPF10	0	R/W	Receive Descriptor Processed Flag 10 This bit indicates that a descriptor in reception queue 10 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 10 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
9	RDPF9	0	R/W	Receive Descriptor Processed Flag 9 This bit indicates that a descriptor in reception queue 9 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 9 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
8	RDPF8	0	R/W	Receive Descriptor Processed Flag 8 This bit indicates that a descriptor in reception queue 8 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 8 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending

Bit	Bit Name	Initial Value	R/W	Description
7	RDPF7	0	R/W	Receive Descriptor Processed Flag 7 This bit indicates that a descriptor in reception queue 7 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 7 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
6	RDPF6	0	R/W	Receive Descriptor Processed Flag 6 This bit indicates that a descriptor in reception queue 6 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 6 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
5	RDPF5	0	R/W	Receive Descriptor Processed Flag 5 This bit indicates that a descriptor in reception queue 5 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 5 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
4	RDPF4	0	R/W	Receive Descriptor Processed Flag 4 This bit indicates that a descriptor in reception queue 4 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 4 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending

Bit	Bit Name	Initial Value	R/W	Description
3	RDPF3	0	R/W	Receive Descriptor Processed Flag 3 This bit indicates that a descriptor in reception queue 3 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 3 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
2	RDPF2	0	R/W	Receive Descriptor Processed Flag 2 This bit indicates that a descriptor in reception queue 2 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 2 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
1	RDPF1	0	R/W	Receive Descriptor Processed Flag 1 This bit indicates that a descriptor in reception queue 1 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 1 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending
0	RDPF0	0	R/W	Receive Descriptor Processed Flag 0 This bit indicates that a descriptor in reception queue 0 has been processed where DESCR.DIE is B'0001. Note: The descriptor with DESCR.DIE is 1, which sets this bit, sets in addition the universal descriptor interrupt DIS.DPF1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode. This bit is set to 1 when a descriptor in reception queue 0 has been processed where DESCR.DIE is 1. 0: No interrupt pending 1: Descriptor interrupt pending

33A.2.50 gPTP Configuration Control Register (GCCR)

The GCCR register is used to set and control the gPTP (generalized precision time protocol).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	LI[2:0]			SPC	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TCSS[1:0]		—	—	LMTT	LPTC	LTI	LTO	TCR[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	1	1	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

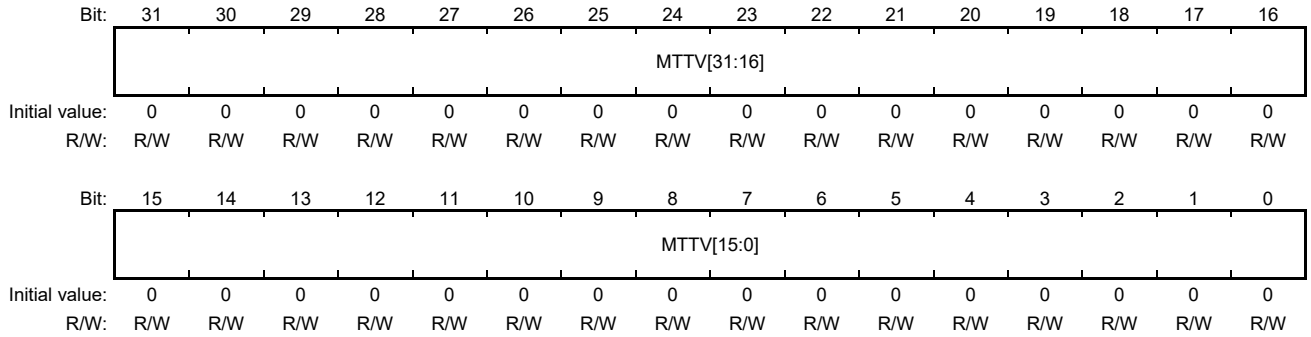
Bit	Bit Name	Initial Value	R/W	Description
31 to 23	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
22 to 20	LI[2:0]	000	R/W	Index number of compare unit to be loaded Load Index These bits define the target unit to be updated by GCCR.LPTC. The CPU can only write to these bits if GCCR.LPTC is 0.
19	SPC	0	R/W	Start Periodic Comparison This bit defines if the absolute comparison value or the periodicity value is updated to the value of GPTC.PTCV on GCCR.LPTC request. Periodic comparison starts when updating the periodic comparison value; periodic comparison stops when updating the absolute comparison value. The CPU can only write to these bits if GCCR.LPTC is 0. 0: Absolute comparison value updated by GCCR.LPTC request 1: Periodic comparison value updated by GCCR.LPTC request
18 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9, 8	TCSS[1:0]	00	R/W	Timer Capture Source Select These bits select the source used for updating the captured timer register (gPTP timer capture register (GCTi.CTV)). These bits should still be controlled when timer control is not being requested (GCCR.TCR = 0). 00: gPTP timer value 01: Adjusted gPTP timer value 10: AVTP presentation time 11: Setting prohibited
7, 6	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
5	LMTT	1	R/W	Maximum Transit Time Configuration Request This bit issues requests for configuring the gPTP maximum transit time configuration register (GMTT). Only 1 can be written to the bit. [Conditions for Changing] — The bit is set to 1 when the operating mode is not operation mode. — The bit is set to 0 when the value of the gPTP maximum transit time configuration register (GMTT) is loaded. 0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.
4	LPTC	0	R/W	Presentation Time Compare Value Configuration Request This bit issues requests for configuring the gPTP presentation time comparison register (GPTC). Only 1 can be written to the bit. The CPU cannot write to this bit if CSR.OPS is CONFIG and CCC.GAC is 0. The CPU should not write 1 to this bit when AVTP FIFO of selected compare unit is in use. [Conditions for Changing] — The bit is set to 1 when the operating mode is not operation mode and CCC.GAC is 0. — The bit is set to 0 when the value of the gPTP presentation time comparison register (GPTC) is loaded. 0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.
3	LTI	1	R/W	Timer Increment Value Configuration Request This bit issues requests for configuring the gPTP timer increment configuration register (GTI). Only 1 can be written to the bit. [Conditions for Changing] — The bit is set to 1 when the operating mode is not operation mode and CCC.GAC is 0. — The bit is set to 0 when the value of the gPTP timer increment configuration register (GTI) is loaded. 0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.

Bit	Bit Name	Initial Value	R/W	Description
2	LTO	1	R/W	Timer Offset Value Configuration Request This bit issues requests for configuring gPTP timer offset configuration register i (GTOi). Only 1 can be written to the bit. [Conditions for Changing] — The bit is set to 1 when the operating mode is not operation mode and CCC.GAC is 0. — The bit is set to 0 when the value of gPTP timer offset configuration register i (GTOi) is loaded. 0: Setting completed 1: When written: Issue a configuration request. When read: Completion of settings is pending.
1, 0	TCR[1:0]	00	R/W	Timer Control Request These bits issue requests for controlling the gPTP timer. The source selection (GCCR.TCSS) can be done by same write access. Writing to the bits is only possible when the current operating mode is operation mode, or if CSR.OPS is CONFIG and CCC.GAC is 1. Do not write to the bit when the gPTP timer clock select bit in the AVB-DMAC mode register is B'00. Write to these bits while GCCR.TCR is B'00 or B'10. The CPU should not write other values than B'11 to these bits if GCCR.TCR is B'10. The CPU should only use continuous capture (B'10) for AVTP presentation time value (GCCR.TCSS is B'10). [Conditions for Changing] — The bits are set to B'00 when the operating mode is not operation mode and CCC.GAC is 0. — The bits are also set to B'00 on completion of the requested processing. 00: Timer control is not requested. 01: gPTP/AVTP presentation time reset 10: Continuous capture of AVTP to GCTt.CTV 11: Captures the value set in the TCSS bit.

33A.2.51 gPTP Maximum Transit Time Configuration Register (GMTT)

The GMTT register sets the maximum time for transitions of the gPTP timer.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MTTV[31:0]	H'0000 0000	R/W	Maximum Transit Time These bits set the maximum transition time for use in calculating AVTP presentation time. Write the desired setting to the bits, then issue the configuration request by setting the maximum transit time configuration request bit in the gPTP configuration control register (GCCR.LMTT) to 1.

Note: Do not write a value to these bits when the operating mode is operation mode or CCC.GAC is 1 and the maximum transit time configuration request bit (GCCR.LMTT) is 1.

33A.2.52 gPTP Presentation Time Comparison Register (GPTC)

The GPTC register sets a value for comparison with presentation times in the gPTP timer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PTCV[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

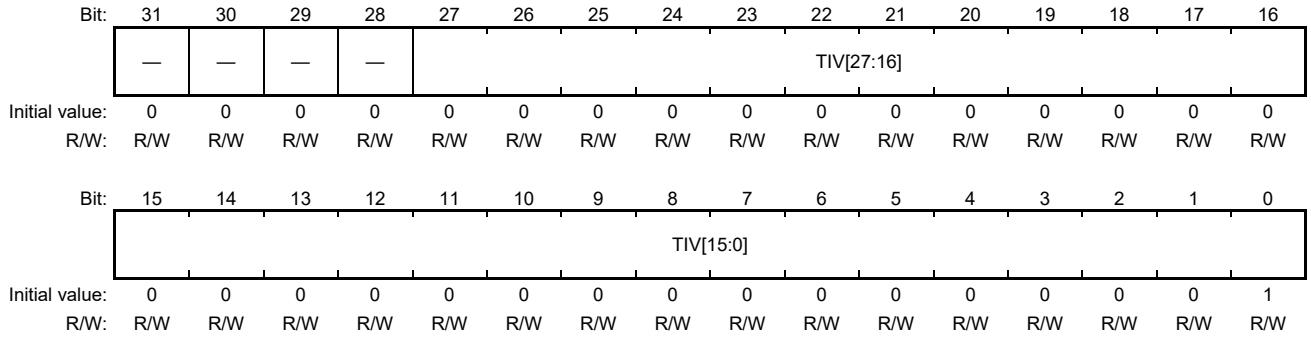
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PTCV[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PTCV[31:0]	H'0000 0000	R/W	Presentation Time Comparison Value These bits set a value for comparison with AVTP timer values to which a maximum transit time is not appended. Write the desired setting to the bits, then issue the configuration request by setting the presentation time comparison value configuration request bit in the gPTP configuration control register (GCCR.LPTC) to 1.

Note: Do not write a value to these bits when the presentation time comparison value configuration request bit (GCCR.LPTC) is 1.
The CPU should only write values in range of 0 to 3FFF_FFFFh to these bits when they are defining the period value of AVTP comparison unit (controlled by GCCR.SPC).

33A.2.53 gPTP Timer Increment Configuration Register (GTI)

The GTI register sets the increment for the gPTP timer.



Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
27 to 0	TIV[27:0]	H'000 0001	R/W	gPTP Timer Increment Value When the gPTP clock select bits in the AVB-DMAC mode register (CCC.CSEL) are selecting a clock signal, these bits set the value by which the timer is incremented each time a cycle of that clock signal elapses. Write the desired setting to the bits, then issue the configuration request by setting the timer increment value configuration request bit in the gPTP configuration control register (GCCR.LTI) to 1.

Note: Do not write a value to these bits when the operating mode is operation mode or CCC.GAC is 1 and the timer increment value configuration request bit (GCCR.LTI) is 1.

Do not write 0 to the bits.

Keep comparison value in the following range

$x \leq comparison\_value \leq 2^{32} - x$

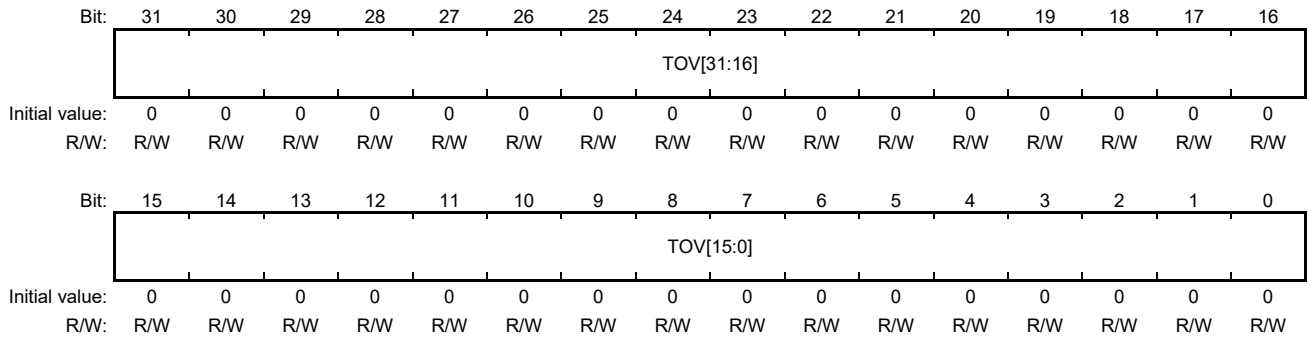
, where x is amount of nanoseconds of the configured increment value in GTI.TIV

The CPU should not program increment values less than H'0010 0000

33A.2.54 gPTP timer offset register i (GTOi) (i = 0 to 2)

The GTOi register sets an offset value for the gPTP timer.

The offset value is added to the combination of bits 0 to 31 in GTO0, 32 to 63 in GTO1, and 64 to 79 in GTO2, which together make up the gPTP timer.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	TOV[31:0]	H'0000 0000	R/W	Timer Offset Value This is an 80-bit value consisting of the settings in GTO0.TOV[31:0], GTO1.TOV[63:32], and GTO2.TOV[79:64], and is used to set an offset for adding to the value of the gPTP timer. Write the desired setting to the bits, then issue the configuration request by setting the timer offset value configuration request bit in the gPTP configuration control register (GCCR.LTO) to 1.

Note: Do not write a value to these bits when the operating mode is operation mode or CCC.GAC is 1 and the timer offset value configuration request bit (GCCR.LTO) is 1. Write H'0000 to GTO2.TOV[95:80].
Set a value in the range from 0 to 10^9-1 (H'0000 0000 to H'3B9A C9FF) in GTOi.TOV[31:0].

33A.2.55 gPTP Interrupt Control Register (GIC)

The GCI register is used to control gPTP-related interrupts.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PTME7	PTME6	PTME5	PTME4	PTME3	PTME2	PTME1	PTME0	PTOE	PTCE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	PTME7	0	R/W	Presentation Time Matched interrupt Enable 7 While this bit is 1 an interrupt will be generated when GIS.PTMF7 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD7. This bit is set to 1 when writing 1 to GIE.PTMS7. 0: Disabled 1: Enabled
8	PTME6	0	R/W	Presentation Time Matched interrupt Enable 6 While this bit is 1 an interrupt will be generated when GIS.PTMF6 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD6. This bit is set to 1 when writing 1 to GIE.PTMS6. 0: Disabled 1: Enabled
7	PTME5	0	R/W	Presentation Time Matched interrupt Enable 5 While this bit is 1 an interrupt will be generated when GIS.PTMF5 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD5. This bit is set to 1 when writing 1 to GIE.PTMS5. 0: Disabled 1: Enabled
6	PTME4	0	R/W	Presentation Time Matched interrupt Enable 4 While this bit is 1 an interrupt will be generated when GIS.PTMF4 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD4. This bit is set to 1 when writing 1 to GIE.PTMS4. 0: Disabled 1: Enabled

Bit	Bit Name	Initial Value	R/W	Description
5	PTME3	0	R/W	Presentation Time Matched interrupt Enable 3 While this bit is 1 an interrupt will be generated when GIS.PTMF3 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD3. This bit is set to 1 when writing 1 to GIE.PTMS3. 0: Disabled 1: Enabled
4	PTME2	0	R/W	Presentation Time Matched interrupt Enable 2 While this bit is 1 an interrupt will be generated when GIS.PTMF2 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD2. This bit is set to 1 when writing 1 to GIE.PTMS2. 0: Disabled 1: Enabled
3	PTME1	0	R/W	Presentation Time Matched interrupt Enable 1 While this bit is 1 an interrupt will be generated when GIS.PTMF1 is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD1. This bit is set to 1 when writing 1 to GIE.PTMS1. 0: Disabled 1: Enabled
2	PTME0	0	R/W	Presentation Time Match Interrupt Enable 0 When this bit is 1, setting of the presentation time match interrupt flag in the gPTP interrupt status register (GIS.PTMF) to 1 leads to generation of that interrupt. [Changing condition] This bit is set to 0 when writing 1 to GID.PTMD0. This bit is set to 1 when writing 1 to GIE.PTMS0. 0: Disabled 1: Enabled
1	PTOE	0	R/W	Presentation Time Overrun interrupt Enable While this bit is 1 an interrupt will be generated when GIS.PTOF is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTOD. This bit is set to 1 when writing 1 to GIE.PTOS. 0: Disabled 1: Enabled
0	PTCE	0	R/W	Presentation Time Captured interrupt Enable While this bit is 1 an interrupt will be generated when GIS.PTCF is 1. [Changing condition] This bit is set to 0 when writing 1 to GID.PTCD. This bit is set to 1 when writing 1 to GIE.PTCS. 0: Disabled 1: Enabled

33A.2.56 gPTP interrupt status register (GIS)

The GIC register indicates the state of the gPTP-related interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PTMF7	PTMF6	PTMF5	PTMF4	PTMF3	PTMF2	PTMF1	PTMF0	PTOF	PTCF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	PTMF7	0	R/W	Presentation Time Matched Flag 7 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 7. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 7. 0: No interrupt pending 1: Presentation time exceeded
8	PTMF6	0	R/W	Presentation Time Matched Flag 6 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 6. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 6. 0: No interrupt pending 1: Presentation time exceeded
7	PTMF5	0	R/W	Presentation Time Matched Flag 5 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 5. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 5. 0: No interrupt pending 1: Presentation time exceeded

Bit	Bit Name	Initial Value	R/W	Description
6	PTMF4	0	R/W	Presentation Time Matched Flag 4 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 4. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 4. 0: No interrupt pending 1: Presentation time exceeded
5	PTMF3	0	R/W	Presentation Time Matched Flag 3 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 3. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 3. 0: No interrupt pending 1: Presentation time exceeded
4	PTMF2	0	R/W	Presentation Time Matched Flag 2 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 2. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 2. 0: No interrupt pending 1: Presentation time exceeded
3	PTMF1	0	R/W	Presentation Time Matched Flag 1 This bit indicates that the AVTP timer value has matched the configured comparison value of AVTP comparator 1. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when the AVTP timer value reaches or exceeds the comparison value of AVTP comparator 1. 0: No interrupt pending 1: Presentation time exceeded

Bit	Bit Name	Initial Value	R/W	Description
2	PTMF0	0	R/W	Presentation Time Match Interrupt Flag 0 This bit indicates that the value of the AVTP timer exceeds the value of the gPTP presentation time comparison register (GPTC). Only 0 can be written to the bit. [Conditions for Changing] — The bit is set to 0 when the operating mode is not operation mode. — The bit is set to 1 when the AVTP timer value is greater than or equal to the value of the gPTP presentation time comparison register (GPTC). 0: The interrupt is not pending. 1: The interrupt is pending.
1	PTOF	0	R/W	Presentation Time Overrun Flag This bit indicates that an external capture event (rising edge of avb_pt_capture[0] signal) has occurred before the last captured value was processed by CPU. The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when EthernetAVB gets an external capture trigger while GIS.PTCF is 1. 0: No interrupt pending 1: Presentation time overrun
0	PTCF	0	R/W	Presentation Time Capture Flag This bit indicates that the AVTP presentation time has been captured based on external capture event (rising edge of avb_pt_capture[0] signal). The CPU can only write 0 to this bit. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 1 when EthernetAVB gets an external capture trigger. 0: No interrupt pending 1: Presentation time captured

33A.2.57 gPTP Captured Presentation Time register (GCPT)

The GCPT registers that captured presentation the gPTP timer value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CPTV[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CPTV[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CPTV[31:0]	H'0000 0000	R	Captured Presentation Time Value These bits represent the captured AVTP presentation time (with Max Transit Time added) due to HW trigger. The CPU should not read these bits when GIS.PTCF is 0. [Changing condition] These bits are updated with the current AVTP presentation time when an external capture trigger (avb_pt_capture[0]) occurs and GIS.PTCF is 0. Note for verification: These bits are set to 0 when leaving OPERATION mode and CCC.GAC is 0.

33A.2.58 gPTP Timer Capture Register i (GCTi) (i = 0 to 2)

The GCTi registers form an 80-bit register that captures the gPTP timer value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CTV[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CTV[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	CTV[31:0]	H'0000 0000	R/W	gPTP Timer Capture Value These 80 bits consist of GCT0.CTV[31:0], GCT1.CTV[63:32 and GCT2.CTV[79:64], which together indicate captured timer values. When B'00 (value of the gPTP timer) or B'01 (adjusted gPTP timer value) is selected by the timer capture source select bits in the gPTP configuration control register, the corresponding 80-bit values are stored in these bits. When B'10 (AVTP presentation time) is selected by the timer capture source select bit, the corresponding 32-bit values are stored in these bits. In case of continuous update (GCCR.TCR is B'10) CPU should only use 32 bit read access to get consistent value. Actual writing of the timer value specified by the timer capture source select bits (GCCR.TCSS) proceeds when B'11 (timer capture request) is written to the timer control request bits in the gPTP configuration control register (GCCR.TCR). Do not read the value while the value of the timer control request bits (GCCR.TCR) is B'11, because this indicates that storage is still in progress. Note for verification: These bits are set to 0 when leaving OPERATION mode and CCC.GAC is 0.

33A.2.59 gPTP Status Register (GSR)

The GSR register indicates the state of the gPTP.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	AFU3	AFU2	AFU1	AFU0	AFFL3[3:0]				AFFL2[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	AFFL1[3:0]				AFFL0[3:0]				PCM7	PCM6	PCM5	PCM4	PCM3	PCM2	PCM1	PCM0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
27	AFU3	0	R	Avtp Fifo Update 3 This bit indicates an ongoing update of the AVTP-FIFO of compare unit 3. When this bit is 0, the AVTP-FIFO is able to process adding new values. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when AVTP compare value is added to the AVTP-FIFO. This bit is set to 1 when CPU writes a new value to GPTF3.PTFV and GSR.AFFL3 is not 15. 0: No update of AVTP FIFO pending 1: Update of AVTP FIFO with value from GPTF3.PTFV is ongoing
26	AFU2	0	R	Avtp Fifo Update 2 This bit indicates an ongoing update of the AVTP-FIFO of compare unit 2. When this bit is 0, the AVTP-FIFO is able to process adding new values. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when AVTP compare value is added to the AVTP-FIFO. This bit is set to 1 when CPU writes a new value to GPTF2.PTFV and GSR.AFFL2 is not 15. 0: No update of AVTP FIFO pending 1: Update of AVTP FIFO with value from GPTF2.PTFV is ongoing

Bit	Bit Name	Initial Value	R/W	Description
25	AFU1	0	R	Avtp Fifo Update 1 This bit indicates an ongoing update of the AVTP-FIFO of compare unit 1. When this bit is 0, the AVTP-FIFO is able to process adding new values. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when AVTP compare value is added to the AVTP-FIFO. This bit is set to 1 when CPU writes a new value to GPTF1.PTFV and GSR.AFFL1 is not 15. 0: No update of AVTP FIFO pending 1: Update of AVTP FIFO with value from GPTF1.PTFV is ongoing
24	AFU0	0	R	Avtp Fifo Update 0 This bit indicates an ongoing update of the AVTP-FIFO of compare unit 0. When this bit is 0, the AVTP-FIFO is able to process adding new values. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when AVTP compare value is added to the AVTP-FIFO. This bit is set to 1 when CPU writes a new value to GPTF0.PTFV and GSR.AFFL0 is not 15. 0: No update of AVTP FIFO pending 1: Update of AVTP FIFO with value from GPTF0.PTFV is ongoing
23 to 20	AFFL3[3:0]	H'0	R	FIFO fill level of AVTP compare unit 3 These bits indicate the number of AVTP timestamps pending in AVTP-FIFO of compare unit 3. The timestamps are provided by CPU and taken by compare unit when no comparison on AVTP comparator 3 is active. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This value is incremented when a new value is added to AVTP-FIFO (GSR.AFU3 changes to 0). This value is decremented when a timestamp value from FIFO has been loaded to the AVTP comparator.
19 to 16	AFFL2[3:0]	H'0	R	FIFO fill level of AVTP compare unit 2 These bits indicate the number of AVTP timestamps pending in AVTP-FIFO of compare unit 2. The timestamps are provided by CPU and taken by compare unit when no comparison on AVTP comparator 2 is active. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This value is incremented when a new value is added to AVTP-FIFO (GSR.AFU2 changes to 0). This value is decremented when a timestamp value from FIFO has been loaded to the AVTP comparator.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	AFFL1[3:0]	H'0	R	FIFO fill level of AVTP compare unit 1 These bits indicate the number of AVTP timestamps pending in AVTP-FIFO of compare unit 1. The timestamps are provided by CPU and taken by compare unit when no comparison on AVTP comparator 1 is active. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This value is incremented when a new value is added to AVTP-FIFO (GSR.AFU1 changes to 0). This value is decremented when a timestamp value from FIFO has been loaded to the AVTP comparator.
11 to 8	AFFL0[3:0]	H'0	R	FIFO fill level of AVTP compare unit 0 These bits indicate the number of AVTP timestamps pending in AVTP-FIFO of compare unit 0. The timestamps are provided by CPU and taken by compare unit when no comparison on AVTP comparator 0 is active. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This value is incremented when a new value is added to AVTP-FIFO (GSR.AFU0 changes to 0). This value is decremented when a timestamp value from FIFO has been loaded to the AVTP comparator.
7	PCM7	0	R	Periodic Comparison Mode 7 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 7. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison
6	PCM6	0	R	Periodic Comparison Mode 6 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 6. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison

Bit	Bit Name	Initial Value	R/W	Description
5	PCM5	0	R	Periodic Comparison Mode 5 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 5. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison
4	PCM4	0	R	Periodic Comparison Mode 4 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 4. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison
3	PCM3	0	R	Periodic Comparison Mode 3 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 3. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison
2	PCM2	0	R	Periodic Comparison Mode 2 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 2. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison

Bit	Bit Name	Initial Value	R/W	Description
1	PCM1	0	R	Periodic Comparison Mode 1 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 1. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison
0	PCM0	0	R	Periodic Comparison Mode 0 This bit indicates if single shot or periodic comparison mode is active on AVTP comparator unit 0. [Changing condition] This bit is set to 0 when leaving OPERATION mode and CCC.GAC is 0. This bit is set to 0 when the last match has happened after CPU has requested entering single shot mode. This bit is set to 1 when loading a period value for the AVTP comparator. 0: Single shot comparison 1: Periodic comparison

33A.2.60 gPTP Interrupt Enable register (GIE)

The GIE register is used to control the gPTP Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PTMS7	PTMS6	PTMS5	PTMS4	PTMS3	PTMS2	PTMS1	PTMS0	PTOS	PTCS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	PTMS7	0	R/W	Presentation Time Matched interrupt Set 7 This bit supports interrupt enable. It controls set of GIC.PTME7. This bit is always read as 0. 0: No change of GIC.PTME7 1: Set GIC.PTME7 to 1
8	PTMS6	0	R/W	Presentation Time Matched interrupt Set 6 This bit supports interrupt enable. It controls set of GIC.PTME6. This bit is always read as 0. 0: No change of GIC.PTME6 1: Set GIC.PTME6 to 1
7	PTMS5	0	R/W	Presentation Time Matched interrupt Set 5 This bit supports interrupt enable. It controls set of GIC.PTME5. This bit is always read as 0. 0: No change of GIC.PTME5 1: Set GIC.PTME5 to 1
6	PTMS4	0	R/W	Presentation Time Matched interrupt Set 4 This bit supports interrupt enable. It controls set of GIC.PTME4. This bit is always read as 0. 0: No change of GIC.PTME4 1: Set GIC.PTME4 to 1
5	PTMS3	0	R/W	Presentation Time Matched interrupt Set 3 This bit supports interrupt enable. It controls set of GIC.PTME3. This bit is always read as 0. 0: No change of GIC.PTME3 1: Set GIC.PTME3 to 1
4	PTMS2	0	R/W	Presentation Time Matched interrupt Set 2 This bit supports interrupt enable. It controls set of GIC.PTME2. This bit is always read as 0. 0: No change of GIC.PTME2 1: Set GIC.PTME2 to 1

Bit	Bit Name	Initial Value	R/W	Description
3	PTMS1	0	R/W	Presentation Time Matched interrupt Set 1 This bit supports interrupt enable. It controls set of GIC.PTME1. This bit is always read as 0. 0: No change of GIC.PTME1 1: Set GIC.PTME1 to 1
2	PTMS0	0	R/W	Presentation Time Matched interrupt Set 0 This bit supports interrupt enable. It controls set of GIC.PTME0. This bit is always read as 0. 0: No change of GIC.PTME0 1: Set GIC.PTME0 to 1
1	PTOS	0	R/W	Presentation Time Overrun interrupt Set This bit supports interrupt enable. It controls set of GIC.PTOE. This bit is always read as 0. 0: No change of GIC.PTOE 1: Set GIC.PTOE to 1
0	PTCS	0	R/W	Presentation Time Captured interrupt Set This bit supports interrupt enable. It controls set of GIC.PTCE. This bit is always read as 0. 0: No change of GIC.PTCE 1: Set GIC.PTCE to 1

33A.2.61 gPTP Interrupt Disable register (GID)

The GID register is used to control the gPTP Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PTMD7	PTMD6	PTMD5	PTMD4	PTMD3	PTMD2	PTMD1	PTMD0	PTOD	PTCD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	PTMD7	0	R/W	Presentation Time Matched interrupt Disable 7 This bit supports interrupt enable. It controls set of GIC.PTME7. This bit is always read as 0. 0: No change of GIC.PTME7 1: Set GIC.PTME7 to 0
8	PTMD6	0	R/W	Presentation Time Matched interrupt Disable 6 This bit supports interrupt enable. It controls set of GIC.PTME6. This bit is always read as 0. 0: No change of GIC.PTME6 1: Set GIC.PTME6 to 0
7	PTMD5	0	R/W	Presentation Time Matched interrupt Disable 5 This bit supports interrupt enable. It controls set of GIC.PTME5. This bit is always read as 0. 0: No change of GIC.PTME5 1: Set GIC.PTME5 to 0
6	PTMD4	0	R/W	Presentation Time Matched interrupt Disable 4 This bit supports interrupt enable. It controls set of GIC.PTME4. This bit is always read as 0. 0: No change of GIC.PTME4 1: Set GIC.PTME4 to 0
5	PTMD3	0	R/W	Presentation Time Matched interrupt Disable 3 This bit supports interrupt enable. It controls set of GIC.PTME3. This bit is always read as 0. 0: No change of GIC.PTME3 1: Set GIC.PTME3 to 0
4	PTMD2	0	R/W	Presentation Time Matched interrupt Disable 2 This bit supports interrupt enable. It controls set of GIC.PTME2. This bit is always read as 0. 0: No change of GIC.PTME2 1: Set GIC.PTME2 to 0

Bit	Bit Name	Initial Value	R/W	Description
3	PTMD1	0	R/W	Presentation Time Matched interrupt Disable 1 This bit supports interrupt enable. It controls set of GIC.PTME1. This bit is always read as 0. 0: No change of GIC.PTME1 1: Set GIC.PTME1 to 0
2	PTMD0	0	R/W	Presentation Time Matched interrupt Disable 0 This bit supports interrupt enable. It controls set of GIC.PTME0. This bit is always read as 0. 0: No change of GIC.PTME0 1: Set GIC.PTME0 to 0
1	PTOD	0	R/W	Presentation Time Overrun interrupt Disable This bit supports interrupt enable. It controls set of GIC.PTOE. This bit is always read as 0. 0: No change of GIC.PTOE 1: Set GIC.PTOE to 0
0	PTCD	0	R/W	Presentation Time Captured interrupt Disable This bit supports interrupt enable. It controls set of GIC.PTCE. This bit is always read as 0. 0: No change of GIC.PTCE 1: Set GIC.PTCE to 0

33A.2.62 gPTP Interrupt Line select register (GIL)

The GIL register is used to control the gPTP Interrupt line.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

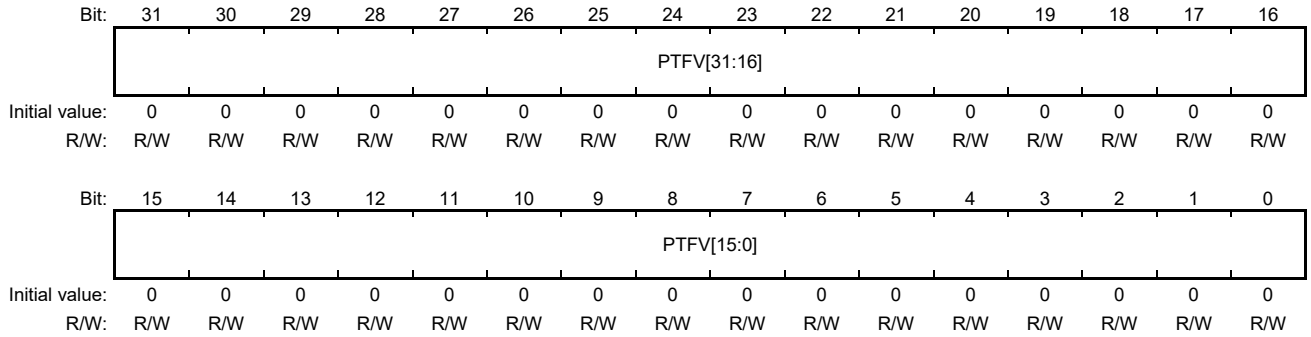
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PTML7	PTML6	PTML5	PTML4	PTML3	PTMI2	PTML1	PTML0	PTOL	PTCL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	PTML7	0	R/W	Presentation Time Matched interrupt Line select 7 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
8	PTML6	0	R/W	Presentation Time Matched interrupt Line select 6 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
7	PTML5	0	R/W	Presentation Time Matched interrupt Line select 5 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
6	PTML4	0	R/W	Presentation Time Matched interrupt Line select 4 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
5	PTML3	0	R/W	Presentation Time Matched interrupt Line select 3 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
4	PTML2	0	R/W	Presentation Time Matched interrupt Line select 2 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification

Bit	Bit Name	Initial Value	R/W	Description
3	PTML1	0	R/W	Presentation Time Matched interrupt Line select 1 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
2	PTML0	0	R/W	Presentation Time Matched interrupt Line select 0 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
1	PTOL	0	R/W	Presentation Time Overrun interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
0	PTCL	0	R/W	Presentation Time Captured interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification

33A.2.63 gPTP Presentation Time Fifo register i (GPTFi) (i = 0 to 3)

The GPTFi register is used to control the gPTP FIFO.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	PTFV[31:0]	H'0000 0000	R/W	Presentation Time Fifo Value These bits define a value to be compared with the AVTP timer value (without Max Transit Time added). When writing to this register the value is added to AVTP-FIFO of comparator unit i. These bits are always read as 0. The CPU cannot write to these bits if CSR.OPS is CONFIG and CCC.GAC is 0. The CPU should not write to these bits when GSR.PCMi is 1. The CPU should not write to these bits when GSR.AFUi is 1. The CPU should not write to these bits when GSR.AFFLi is 15.

33A.2.64 Descriptor Interrupt Line selection register (DIL)

The DIL register is used to control the Descriptor Interrupt line.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPL15	DPL14	DPL13	DPL12	DPL11	DPL10	DPL9	DPL8	DPL7	DPL6	DPL5	DPL4	DPL3	DPL2	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPL15	0	R/W	Descriptor Processed interrupt Line select 15 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
14	DPL14	0	R/W	Descriptor Processed interrupt Line select 14 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
13	DPL13	0	R/W	Descriptor Processed interrupt Line select 13 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
12	DPL12	0	R/W	Descriptor Processed interrupt Line select 12 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
11	DPL11	0	R/W	Descriptor Processed interrupt Line select 11 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
10	DPL10	0	R/W	Descriptor Processed interrupt Line select 10 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification

Bit	Bit Name	Initial Value	R/W	Description
9	DPL9	0	R/W	Descriptor Processed interrupt Line select 9 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
8	DPL8	0	R/W	Descriptor Processed interrupt Line select 8 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
7	DPL7	0	R/W	Descriptor Processed interrupt Line select 7 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
6	DPL6	0	R/W	Descriptor Processed interrupt Line select 6 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
5	DPL5	0	R/W	Descriptor Processed interrupt Line select 5 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
4	DPL4	0	R/W	Descriptor Processed interrupt Line select 4 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
3	DPL3	0	R/W	Descriptor Processed interrupt Line select 3 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
2	DPL2	0	R/W	Descriptor Processed interrupt Line select 2 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
1, 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

33A.2.65 Error Interrupt Line selection register (EIL)

The EIL register is used to control the Error Interrupt line.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TBFL	MFFL	TFFL	CULL1	CULL0	CLLL1	CLLL0	SEL	QEL	MTEL	MREL
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10	TBFL	0	R/W	Tx-Buffer Full interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
9	MFFL	0	R/W	E-MAC status FIFO Full interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
8	TFFL	0	R/W	Timestamp FIFO Full interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
7	CULL1	0	R/W	CBS Upper Limit reached interrupt Line select 1 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
6	CULL0	0	R/W	CBS Upper Limit reached interrupt Line select 0 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
5	CLLL1	0	R/W	CBS Lower Limit reached interrupt Line select 1 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification

Bit	Bit Name	Initial Value	R/W	Description
4	CLLL0	0	R/W	CBS Lower Limit reached interrupt Line select 0 This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
3	SEL	0	R/W	Separation Error interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
2	QEL	0	R/W	Queue Error interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
1	MTEL	0	R/W	E-MAC Transmission Error interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
0	MREL	0	R/W	E-MAC Reception Error interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification

33A.2.66 Transmission Interrupt Line select register (TIL)

The TIL register is used to control the Transmission Interrupt line.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MFWL	MFUL	TFWL	TFUL	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 12	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
11	MFWL	0	R/W	E-MAC status FIFO Warning interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
10	MFUL	0	R/W	E-MAC status FIFO Updated interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
9	TFWL	0	R/W	Timestamp FIFO Warning interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
8	TFUL	0	R/W	Timestamp FIFO Updated interrupt Line select This bit selects the interrupt line used for this notification. It is recommended to disable interrupt before change the line. 0: Interrupt line A used for this notification 1: Interrupt line B used for this notification
7 to 0	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.

33A.2.67 Descriptor Interrupt Enable register (DIE)

The DIE register is used to control the Descriptor Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPS15	DPS14	DPS13	DPS12	DPS11	DPS10	DPS9	DPS8	DPS7	DPS6	DPS5	DPS4	DPS3	DPS2	DPS1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPS15	0	R/W	Descriptor Processed interrupt Set 15 This bit supports interrupt enable. It controls set of DIC.DPE15. This bit is always read as 0. 0: No change of DIC.DPE15 1: Set DIC.DPE15 to 1
14	DPS14	0	R/W	Descriptor Processed interrupt Set 14 This bit supports interrupt enable. It controls set of DIC.DPE14. This bit is always read as 0. 0: No change of DIC.DPE14 1: Set DIC.DPE14 to 1
13	DPS13	0	R/W	Descriptor Processed interrupt Set 13 This bit supports interrupt enable. It controls set of DIC.DPE13. This bit is always read as 0. 0: No change of DIC.DPE13 1: Set DIC.DPE13 to 1
12	DPS12	0	R/W	Descriptor Processed interrupt Set 12 This bit supports interrupt enable. It controls set of DIC.DPE12. This bit is always read as 0. 0: No change of DIC.DPE12 1: Set DIC.DPE12 to 1
11	DPS11	0	R/W	Descriptor Processed interrupt Set 11 This bit supports interrupt enable. It controls set of DIC.DPE11. This bit is always read as 0. 0: No change of DIC.DPE11 1: Set DIC.DPE11 to 1
10	DPS10	0	R/W	Descriptor Processed interrupt Set 10 This bit supports interrupt enable. It controls set of DIC.DPE10. This bit is always read as 0. 0: No change of DIC.DPE10 1: Set DIC.DPE10 to 1

Bit	Bit Name	Initial Value	R/W	Description
9	DPS9	0	R/W	Descriptor Processed interrupt Set 9 This bit supports interrupt enable. It controls set of DIC.DPE9. This bit is always read as 0. 0: No change of DIC.DPE9 1: Set DIC.DPE9 to 1
8	DPS8	0	R/W	Descriptor Processed interrupt Set 8 This bit supports interrupt enable. It controls set of DIC.DPE8. This bit is always read as 0. 0: No change of DIC.DPE8 1: Set DIC.DPE8 to 1
7	DPS7	0	R/W	Descriptor Processed interrupt Set 7 This bit supports interrupt enable. It controls set of DIC.DPE7. This bit is always read as 0. 0: No change of DIC.DPE7 1: Set DIC.DPE7 to 1
6	DPS6	0	R/W	Descriptor Processed interrupt Set 6 This bit supports interrupt enable. It controls set of DIC.DPE6. This bit is always read as 0. 0: No change of DIC.DPE6 1: Set DIC.DPE6 to 1
5	DPS5	0	R/W	Descriptor Processed interrupt Set 5 This bit supports interrupt enable. It controls set of DIC.DPE5. This bit is always read as 0. 0: No change of DIC.DPE5 1: Set DIC.DPE5 to 1
4	DPS4	0	R/W	Descriptor Processed interrupt Set 4 This bit supports interrupt enable. It controls set of DIC.DPE4. This bit is always read as 0. 0: No change of DIC.DPE4 1: Set DIC.DPE4 to 1
3	DPS3	0	R/W	Descriptor Processed interrupt Set 3 This bit supports interrupt enable. It controls set of DIC.DPE3. This bit is always read as 0. 0: No change of DIC.DPE3 1: Set DIC.DPE3 to 1
2	DPS2	0	R/W	Descriptor Processed interrupt Set 2 This bit supports interrupt enable. It controls set of DIC.DPE2. This bit is always read as 0. 0: No change of DIC.DPE2 1: Set DIC.DPEi to 1
1	DPS1	0	R/W	Descriptor Processed interrupt Set 1 This bit supports interrupt enable. It controls set of DIC.DPE1. This bit is always read as 0. 0: No change of DIC.DPE1 1: Set DIC.DPE1 to 1
0	—	0	R/W	Reserved These bits are read as 0. The write value should be 0.

33A.2.68 Descriptor Interrupt Disable register (DID)

The DID register is used to control the Descriptor Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DPD15	DPD14	DPD13	DPD12	DPD11	DPD10	DPD9	DPD8	DPD7	DPD6	DPD5	DPD4	DPD3	DPD2	DPD1	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15	DPD15	0	R/W	Descriptor Processed interrupt Disable 15 This bit supports interrupt enable. It controls set of DIC.DPE15. This bit is always read as 0. 0: No change of DIC.DPE15 1: Set DIC.DPE15 to 0
14	DPD14	0	R/W	Descriptor Processed interrupt Disable 14 This bit supports interrupt enable. It controls set of DIC.DPE14. This bit is always read as 0. 0: No change of DIC.DPE14 1: Set DIC.DPE14 to 0
13	DPD13	0	R/W	Descriptor Processed interrupt Disable 13 This bit supports interrupt enable. It controls set of DIC.DPE13. This bit is always read as 0. 0: No change of DIC.DPE13 1: Set DIC.DPE13 to 0
12	DPD12	0	R/W	Descriptor Processed interrupt Disable 12 This bit supports interrupt enable. It controls set of DIC.DPE12. This bit is always read as 0. 0: No change of DIC.DPE12 1: Set DIC.DPE12 to 0
11	DPD11	0	R/W	Descriptor Processed interrupt Disable 11 This bit supports interrupt enable. It controls set of DIC.DPE11. This bit is always read as 0. 0: No change of DIC.DPE11 1: Set DIC.DPE11 to 0
10	DPD10	0	R/W	Descriptor Processed interrupt Disable 10 This bit supports interrupt enable. It controls set of DIC.DPE10. This bit is always read as 0. 0: No change of DIC.DPE10 1: Set DIC.DPE10 to 0

Bit	Bit Name	Initial Value	R/W	Description
9	DPD9	0	R/W	Descriptor Processed interrupt Disable 9 This bit supports interrupt enable. It controls set of DIC.DPE9. This bit is always read as 0. 0: No change of DIC.DPE9 1: Set DIC.DPE9 to 0
8	DPD8	0	R/W	Descriptor Processed interrupt Disable 8 This bit supports interrupt enable. It controls set of DIC.DPE8. This bit is always read as 0. 0: No change of DIC.DPE8 1: Set DIC.DPE8 to 0
7	DPD7	0	R/W	Descriptor Processed interrupt Disable 7 This bit supports interrupt enable. It controls set of DIC.DPE7. This bit is always read as 0. 0: No change of DIC.DPE7 1: Set DIC.DPE7 to 0
6	DPD6	0	R/W	Descriptor Processed interrupt Disable 6 This bit supports interrupt enable. It controls set of DIC.DPE6. This bit is always read as 0. 0: No change of DIC.DPE6 1: Set DIC.DPE6 to 0
5	DPD5	0	R/W	Descriptor Processed interrupt Disable 5 This bit supports interrupt enable. It controls set of DIC.DPE5. This bit is always read as 0. 0: No change of DIC.DPE5 1: Set DIC.DPE5 to 0
4	DPD4	0	R/W	Descriptor Processed interrupt Disable 4 This bit supports interrupt enable. It controls set of DIC.DPE4. This bit is always read as 0. 0: No change of DIC.DPE4 1: Set DIC.DPE4 to 0
3	DPD3	0	R/W	Descriptor Processed interrupt Disable 3 This bit supports interrupt enable. It controls set of DIC.DPE3. This bit is always read as 0. 0: No change of DIC.DPE3 1: Set DIC.DPE3 to 0
2	DPD2	0	R/W	Descriptor Processed interrupt Disable 2 This bit supports interrupt enable. It controls set of DIC.DPE2. This bit is always read as 0. 0: No change of DIC.DPE2 1: Set DIC.DPE2 to 0
1	DPD1	0	R/W	Descriptor Processed interrupt Disable 1 This bit supports interrupt enable. It controls set of DIC.DPE1. This bit is always read as 0. 0: No change of DIC.DPE1 1: Set DIC.DPE1 to 0
0	—	0	R/W	Reserved This bit is read as 0. The write value should be 0.

33A.2.69 Error Interrupt Enable register (EIE)

The EIE register is used to control the Error Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TBFS	MFFS	TFFS	CULS 1	CULS 0	CLLS1	CLLS0	SES	QES	MTES	MRES
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10	TBFS	0	R/W	Tx-Buffer Full interrupt Set This bit supports interrupt enable. It controls set of EIC.TBFE. This bit is always read as 0. 0: No change of EIC.TBFE 1: Set EIC.TBFE to 1
9	MFFS	0	R/W	E-MAC status FIFO Full interrupt Set This bit supports interrupt enable. It controls set of EIC.MFFE. This bit is always read as 0. 0: No change of EIC.MFFE 1: Set EIC.MFFE to 1
8	TFFS	0	R/W	Timestamp FIFO Full interrupt Set This bit supports interrupt enable. It controls set of EIC.TFFE. This bit is always read as 0. 0: No change of EIC.TFFE 1: Set EIC.TFFE to 1
7	CULS1	0	R/W	CBS Upper Limit reached interrupt Set 1 This bit supports interrupt enable. It controls set of EIC.CULE1. This bit is always read as 0. 0: No change of EIC.CULE1 1: Set EIC.CULE1 to 1
6	CULS0	0	R/W	CBS Upper Limit reached interrupt Set 0 This bit supports interrupt enable. It controls set of EIC.CULE0. This bit is always read as 0. 0: No change of EIC.CULE0 1: Set EIC.CULE0 to 1
5	CLLS1	0	R/W	CBS Lower Limit reached interrupt Set 1 This bit supports interrupt enable. It controls set of EIC.CLLE1. This bit is always read as 0. 0: No change of EIC.CLLE1 1: Set EIC.CLLE1 to 1

Bit	Bit Name	Initial Value	R/W	Description
4	CLLS0	0	R/W	CBS Lower Limit reached interrupt Set 0 This bit supports interrupt enable. It controls set of EIC.CLLE0. This bit is always read as 0. 0: No change of EIC.CLLE0 1: Set EIC.CLLE0 to 1
3	SES	0	R/W	Separation Error interrupt Set This bit supports interrupt enable. It controls set of EIC.SEE. This bit is always read as 0. 0: No change of EIC.SEE 1: Set EIC.QEE to 1
2	QES	0	R/W	Queue Error interrupt Set This bit supports interrupt enable. It controls set of EIC.QEE. This bit is always read as 0. 0: No change of EIC.QEE 1: Set EIC.QEE to 1
1	MTES	0	R/W	E-MAC Transmission Error interrupt Set This bit supports interrupt enable. It controls set of EIC.MTEE. This bit is always read as 0. 0: No change of EIC.MTEE 1: Set EIC.MTEE to 1
0	MRES	0	R/W	E-MAC Reception Error interrupt Set This bit supports interrupt enable. It controls set of EIC.MREE. This bit is always read as 0. 0: No change of EIC.MREE 1: Set EIC.MREE to 1

33A.2.70 Error Interrupt Disable register (EID)

The EID register is used to control the Error Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	TBFD	MFFD	TFFD	CULD 1	CULD 0	CLLD1	CLLD0	SED	QED	MTED	MRED
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 11	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
10	TBFD	0	R/W	Tx-Buffer Full interrupt Disable This bit supports interrupt enable. It controls set of EIC.TBFE. This bit is always read as 0. 0: No change of EIC.TBFE 1: Set EIC.TBFE to 0
9	MFFD	0	R/W	E-MAC status FIFO Full interrupt Disable This bit supports interrupt enable. It controls set of EIC.MFFE. This bit is always read as 0. 0: No change of EIC.MFFE 1: Set EIC.MFFE to 0
8	TFFD	0	R/W	Timestamp FIFO Full interrupt Disable This bit supports interrupt enable. It controls set of EIC.TFFE. This bit is always read as 0. 0: No change of EIC.TFFE 1: Set EIC.TFFE to 0
7	CULD1	0	R/W	CBS Upper Limit reached interrupt Disable 1 This bit supports interrupt enable. It controls set of EIC.CULE1. This bit is always read as 0. 0: No change of EIC.CULE1 1: Set EIC.CULE1 to 0
6	CULD0	0	R/W	CBS Upper Limit reached interrupt Disable 0 This bit supports interrupt enable. It controls set of EIC.CULE0. This bit is always read as 0. 0: No change of EIC.CULE0 1: Set EIC.CULE0 to 0
5	CLLD1	0	R/W	CBS Lower Limit reached interrupt Disable 1 This bit supports interrupt enable. It controls set of EIC.CLLE1. This bit is always read as 0. 0: No change of EIC.CLLE1 1: Set EIC.CLLE1 to 0

Bit	Bit Name	Initial Value	R/W	Description
4	CLLD0	0	R/W	CBS Lower Limit reached interrupt Disable 0 This bit supports interrupt enable. It controls set of EIC.CLLE0. This bit is always read as 0. 0: No change of EIC.CLLE0 1: Set EIC.CLLE0 to 0
3	SED	0	R/W	Separation Error interrupt Disable This bit supports interrupt enable. It controls set of EIC.SEE. This bit is always read as 0. 0: No change of EIC.SEE 1: Set EIC.SEE to 0
2	QED	0	R/W	Queue Error interrupt Disable This bit supports interrupt enable. It controls set of EIC.QEE. This bit is always read as 0. 0: No change of EIC.QEE 1: Set EIC.QEE to 0
1	MTED	0	R/W	E-MAC Transmission Error interrupt Disable This bit supports interrupt enable. It controls set of EIC.MTEE. This bit is always read as 0. 0: No change of EIC.MTEE 1: Set EIC.MTEE to 0
0	MRED	0	R/W	E-MAC Reception Error interrupt Disable This bit supports interrupt enable. It controls set of EIC.MREE. This bit is always read as 0. 0: No change of EIC.MREE 1: Set EIC.MREE to 0

33A.2.71 Reception Interrupt Enable register 0 (RIE0)

The RIE0 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRS17	FRS16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRS15	FRS14	FRS13	FRS12	FRS11	FRS10	FRS9	FRS8	FRS7	FRS6	FRS5	FRS4	FRS3	FRS2	FRS1	FRS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	FRS17	0	R/W	Frame Received interrupt Set 17 This bit supports interrupt enable. It controls set of RIC0.FRE17. This bit is always read as 0. 0: No change of RIC0.FRE17 1: Set RIC0.FRE17 to 1
16	FRS16	0	R/W	Frame Received interrupt Set 16 This bit supports interrupt enable. It controls set of RIC0.FRE16. This bit is always read as 0. 0: No change of RIC0.FRE16 1: Set RIC0.FRE16 to 1
15	FRS15	0	R/W	Frame Received interrupt Set 15 This bit supports interrupt enable. It controls set of RIC0.FRE15. This bit is always read as 0. 0: No change of RIC0.FRE15 1: Set RIC0.FRE15 to 1
14	FRS14	0	R/W	Frame Received interrupt Set 14 This bit supports interrupt enable. It controls set of RIC0.FRE14. This bit is always read as 0. 0: No change of RIC0.FRE14 1: Set RIC0.FRE14 to 1
13	FRS13	0	R/W	Frame Received interrupt Set 13 This bit supports interrupt enable. It controls set of RIC0.FRE13. This bit is always read as 0. 0: No change of RIC0.FRE13 1: Set RIC0.FRE13 to 1
12	FRS12	0	R/W	Frame Received interrupt Set 12 This bit supports interrupt enable. It controls set of RIC0.FRE12. This bit is always read as 0. 0: No change of RIC0.FRE12 1: Set RIC0.FRE12 to 1

Bit	Bit Name	Initial Value	R/W	Description
11	FRS11	0	R/W	Frame Received interrupt Set 11 This bit supports interrupt enable. It controls set of RIC0.FRE11. This bit is always read as 0. 0: No change of RIC0.FRE11 1: Set RIC0.FRE11 to 1
10	FRS10	0	R/W	Frame Received interrupt Set 10 This bit supports interrupt enable. It controls set of RIC0.FRE10. This bit is always read as 0. 0: No change of RIC0.FRE10 1: Set RIC0.FRE10 to 1
9	FRS9	0	R/W	Frame Received interrupt Set 9 This bit supports interrupt enable. It controls set of RIC0.FRE9. This bit is always read as 0. 0: No change of RIC0.FRE9 1: Set RIC0.FRE9 to 1
8	FRS8	0	R/W	Frame Received interrupt Set 8 This bit supports interrupt enable. It controls set of RIC0.FRE8. This bit is always read as 0. 0: No change of RIC0.FRE8 1: Set RIC0.FRE8 to 1
7	FRS7	0	R/W	Frame Received interrupt Set 7 This bit supports interrupt enable. It controls set of RIC0.FRE7. This bit is always read as 0. 0: No change of RIC0.FRE7 1: Set RIC0.FRE7 to 1
6	FRS6	0	R/W	Frame Received interrupt Set 6 This bit supports interrupt enable. It controls set of RIC0.FRE6. This bit is always read as 0. 0: No change of RIC0.FRE6 1: Set RIC0.FRE6 to 1
5	FRS5	0	R/W	Frame Received interrupt Set 5 This bit supports interrupt enable. It controls set of RIC0.FRE5. This bit is always read as 0. 0: No change of RIC0.FRE5 1: Set RIC0.FRE5 to 1
4	FRS4	0	R/W	Frame Received interrupt Set 4 This bit supports interrupt enable. It controls set of RIC0.FRE4. This bit is always read as 0. 0: No change of RIC0.FRE4 1: Set RIC0.FRE4 to 1
3	FRS3	0	R/W	Frame Received interrupt Set 3 This bit supports interrupt enable. It controls set of RIC0.FRE3. This bit is always read as 0. 0: No change of RIC0.FRE3 1: Set RIC0.FRE3 to 1

Bit	Bit Name	Initial Value	R/W	Description
2	FRS2	0	R/W	Frame Received interrupt Set 2 This bit supports interrupt enable. It controls set of RIC0.FRE2. This bit is always read as 0. 0: No change of RIC0.FRE2 1: Set RIC0.FRE2 to 1
1	FRS1	0	R/W	Frame Received interrupt Set 1 This bit supports interrupt enable. It controls set of RIC0.FRE1. This bit is always read as 0. 0: No change of RIC0.FRE1 1: Set RIC0.FRE1 to 1
0	FRS0	0	R/W	Frame Received interrupt Set 0 This bit supports interrupt enable. It controls set of RIC0.FRE0. This bit is always read as 0. 0: No change of RIC0.FRE0 1: Set RIC0.FRE0 to 1

33A.2.72 Reception Interrupt Disable register 0 (RID0)

The RID0 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	FRD17	FRD16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FRD15	FRD14	FRD13	FRD12	FRD11	FRD10	FRD9	FRD8	FRD7	FRD6	FRD5	FRD4	FRD3	FRD2	FRD1	FRD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	FRD17	0	R/W	Frame Received interrupt Disable 17 This bit supports interrupt enable. It controls set of RIC0.FRE17. This bit is always read as 0. 0: No change of RIC0.FRE17 1: Set RIC0.FRE17 to 0
16	FRD16	0	R/W	Frame Received interrupt Disable 16 This bit supports interrupt enable. It controls set of RIC0.FRE16. This bit is always read as 0. 0: No change of RIC0.FRE16 1: Set RIC0.FRE16 to 0
15	FRD15	0	R/W	Frame Received interrupt Disable 15 This bit supports interrupt enable. It controls set of RIC0.FRE15. This bit is always read as 0. 0: No change of RIC0.FRE15 1: Set RIC0.FRE15 to 0
14	FRD14	0	R/W	Frame Received interrupt Disable 14 This bit supports interrupt enable. It controls set of RIC0.FRE14. This bit is always read as 0. 0: No change of RIC0.FRE14 1: Set RIC0.FRE14 to 0
13	FRD13	0	R/W	Frame Received interrupt Disable 13 This bit supports interrupt enable. It controls set of RIC0.FRE13. This bit is always read as 0. 0: No change of RIC0.FRE13 1: Set RIC0.FRE13 to 0
12	FRD12	0	R/W	Frame Received interrupt Disable 12 This bit supports interrupt enable. It controls set of RIC0.FRE12. This bit is always read as 0. 0: No change of RIC0.FRE12 1: Set RIC0.FRE12 to 0

Bit	Bit Name	Initial Value	R/W	Description
11	FRD11	0	R/W	Frame Received interrupt Disable 11 This bit supports interrupt enable. It controls set of RIC0.FRE11. This bit is always read as 0. 0: No change of RIC0.FRE11 1: Set RIC0.FRE11 to 0
10	FRD10	0	R/W	Frame Received interrupt Disable 10 This bit supports interrupt enable. It controls set of RIC0.FRE10. This bit is always read as 0. 0: No change of RIC0.FRE10 1: Set RIC0.FRE10 to 0
9	FRD9	0	R/W	Frame Received interrupt Disable 9 This bit supports interrupt enable. It controls set of RIC0.FRE9. This bit is always read as 0. 0: No change of RIC0.FRE9 1: Set RIC0.FRE9 to 0
8	FRD8	0	R/W	Frame Received interrupt Disable 8 This bit supports interrupt enable. It controls set of RIC0.FRE8. This bit is always read as 0. 0: No change of RIC0.FRE8 1: Set RIC0.FRE8 to 0
7	FRD7	0	R/W	Frame Received interrupt Disable 7 This bit supports interrupt enable. It controls set of RIC0.FRE7. This bit is always read as 0. 0: No change of RIC0.FRE7 1: Set RIC0.FRE7 to 0
6	FRD6	0	R/W	Frame Received interrupt Disable 6 This bit supports interrupt enable. It controls set of RIC0.FRE6. This bit is always read as 0. 0: No change of RIC0.FRE6 1: Set RIC0.FRE6 to 0
5	FRD5	0	R/W	Frame Received interrupt Disable 5 This bit supports interrupt enable. It controls set of RIC0.FRE5. This bit is always read as 0. 0: No change of RIC0.FRE5 1: Set RIC0.FRE5 to 0
4	FRD4	0	R/W	Frame Received interrupt Disable 4 This bit supports interrupt enable. It controls set of RIC0.FRE4. This bit is always read as 0. 0: No change of RIC0.FRE4 1: Set RIC0.FRE4 to 0
3	FRD3	0	R/W	Frame Received interrupt Disable 3 This bit supports interrupt enable. It controls set of RIC0.FRE3. This bit is always read as 0. 0: No change of RIC0.FRE3 1: Set RIC0.FRE3 to 0

Bit	Bit Name	Initial Value	R/W	Description
2	FRD2	0	R/W	Frame Received interrupt Disable 2 This bit supports interrupt enable. It controls set of RIC0.FRE2. This bit is always read as 0. 0: No change of RIC0.FRE2 1: Set RIC0.FRE2 to 0
1	FRD1	0	R/W	Frame Received interrupt Disable 1 This bit supports interrupt enable. It controls set of RIC0.FRE1. This bit is always read as 0. 0: No change of RIC0.FRE1 1: Set RIC0.FRE1 to 0
0	FRD0	0	R/W	Frame Received interrupt Disable 0 This bit supports interrupt enable. It controls set of RIC0.FRE0. This bit is always read as 0. 0: No change of RIC0.FRE0 1: Set RIC0.FRE0 to 0

33A.2.73 Reception Interrupt Enable register 1 (RIE1)

The RIE1 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFWS	—	—	—	—	—	—	—	—	—	—	—	—	—	RWS17	RWS16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RWS15	RWS14	RWS13	RWS12	RWS11	RWS10	RWS9	RWS8	RWS7	RWS6	RWS5	RWS4	RWS3	RWS2	RWS1	RWS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFWS	0	R/W	Rx-FIFO Warning interrupt Set This bit supports interrupt enable. It controls set of RIC1.RFWE. This bit is always read as 0. 0: No change of RIC1.RFWE 1: Set RIC1.RFWE to 1
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RWS17	0	R/W	Reception Warning interrupt Set 17 This bit supports interrupt enable. It controls set of RIC1.RWE17. This bit is always read as 0. 0: No change of RIC1.RWE17 1: Set RIC1.RWE17 to 1
16	RWS16	0	R/W	Reception Warning interrupt Set 16 This bit supports interrupt enable. It controls set of RIC1.RWE16. This bit is always read as 0. 0: No change of RIC1.RWE16 1: Set RIC1.RWE16 to 1
15	RWS15	0	R/W	Reception Warning interrupt Set 15 This bit supports interrupt enable. It controls set of RIC1.RWE15. This bit is always read as 0. 0: No change of RIC1.RWE15 1: Set RIC1.RWE15 to 1
14	RWS14	0	R/W	Reception Warning interrupt Set 14 This bit supports interrupt enable. It controls set of RIC1.RWE14. This bit is always read as 0. 0: No change of RIC1.RWE14 1: Set RIC1.RWE14 to 1
13	RWS13	0	R/W	Reception Warning interrupt Set 13 This bit supports interrupt enable. It controls set of RIC1.RWE13. This bit is always read as 0. 0: No change of RIC1.RWE13 1: Set RIC1.RWE13 to 1

Bit	Bit Name	Initial Value	R/W	Description
12	RWS12	0	R/W	Reception Warning interrupt Set 12 This bit supports interrupt enable. It controls set of RIC1.RWE12. This bit is always read as 0. 0: No change of RIC1.RWE12 1: Set RIC1.RWE12 to 1
11	RWS11	0	R/W	Reception Warning interrupt Set 11 This bit supports interrupt enable. It controls set of RIC1.RWE11. This bit is always read as 0. 0: No change of RIC1.RWE11 1: Set RIC1.RWE11 to 1
10	RWS10	0	R/W	Reception Warning interrupt Set 10 This bit supports interrupt enable. It controls set of RIC1.RWE10. This bit is always read as 0. 0: No change of RIC1.RWE10 1: Set RIC1.RWE10 to 1
9	RWS9	0	R/W	Reception Warning interrupt Set 9 This bit supports interrupt enable. It controls set of RIC1.RWE9. This bit is always read as 0. 0: No change of RIC1.RWE9 1: Set RIC1.RWE9 to 1
8	RWS8	0	R/W	Reception Warning interrupt Set 8 This bit supports interrupt enable. It controls set of RIC1.RWE8. This bit is always read as 0. 0: No change of RIC1.RWE8 1: Set RIC1.RWE8 to 1
7	RWS7	0	R/W	Reception Warning interrupt Set 7 This bit supports interrupt enable. It controls set of RIC1.RWE7. This bit is always read as 0. 0: No change of RIC1.RWE7 1: Set RIC1.RWE7 to 1
6	RWS6	0	R/W	Reception Warning interrupt Set 6 This bit supports interrupt enable. It controls set of RIC1.RWE6. This bit is always read as 0. 0: No change of RIC1.RWE6 1: Set RIC1.RWE6 to 1
5	RWS5	0	R/W	Reception Warning interrupt Set 5 This bit supports interrupt enable. It controls set of RIC1.RWE5. This bit is always read as 0. 0: No change of RIC1.RWE5 1: Set RIC1.RWE5 to 1
4	RWS4	0	R/W	Reception Warning interrupt Set 4 This bit supports interrupt enable. It controls set of RIC1.RWE4. This bit is always read as 0. 0: No change of RIC1.RWE4 1: Set RIC1.RWE4 to 1

Bit	Bit Name	Initial Value	R/W	Description
3	RWS3	0	R/W	Reception Warning interrupt Set 3 This bit supports interrupt enable. It controls set of RIC1.RWE3. This bit is always read as 0. 0: No change of RIC1.RWE3 1: Set RIC1.RWE3 to 1
2	RWS2	0	R/W	Reception Warning interrupt Set 2 This bit supports interrupt enable. It controls set of RIC1.RWE2. This bit is always read as 0. 0: No change of RIC1.RWE2 1: Set RIC1.RWE2 to 1
1	RWS1	0	R/W	Reception Warning interrupt Set 1 This bit supports interrupt enable. It controls set of RIC1.RWE1. This bit is always read as 0. 0: No change of RIC1.RWE1 1: Set RIC1.RWE1 to 1
0	RWS0	0	R/W	Reception Warning interrupt Set 0 This bit supports interrupt enable. It controls set of RIC1.RWE0. This bit is always read as 0. 0: No change of RIC1.RWE0 1: Set RIC1.RWE0 to 1

33A.2.74 Reception Interrupt Disable register 1 (RID1)

The RID1 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFWD	—	—	—	—	—	—	—	—	—	—	—	—	—	RWD17	RWD16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RWD15	RWD14	RWD13	RWD12	RWD11	RWD10	RWD9	RWD8	RWD7	RWD6	RWD5	RWD4	RWD3	RWD2	RWD1	RWD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFWD	0	R/W	Rx-FIFO Warning interrupt Disable This bit supports interrupt enable. It controls set of RIC1.RFWE. This bit is always read as 0. 0: No change of RIC1.RFWE 1: Set RIC1.RFWE to 0
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RWD17	0	R/W	Reception Warning interrupt Disable 17 This bit supports interrupt enable. It controls set of RIC1.RWE17. This bit is always read as 0. 0: No change of RIC1.RWE17 1: Set RIC1.RWE17 to 0
16	RWD16	0	R/W	Reception Warning interrupt Disable 16 This bit supports interrupt enable. It controls set of RIC1.RWE16. This bit is always read as 0. 0: No change of RIC1.RWE16 1: Set RIC1.RWE16 to 0
15	RWD15	0	R/W	Reception Warning interrupt Disable 15 This bit supports interrupt enable. It controls set of RIC1.RWE15. This bit is always read as 0. 0: No change of RIC1.RWE15 1: Set RIC1.RWE15 to 0
14	RWD14	0	R/W	Reception Warning interrupt Disable 14 This bit supports interrupt enable. It controls set of RIC1.RWE14. This bit is always read as 0. 0: No change of RIC1.RWE14 1: Set RIC1.RWE14 to 0
13	RWD13	0	R/W	Reception Warning interrupt Disable 13 This bit supports interrupt enable. It controls set of RIC1.RWE13. This bit is always read as 0. 0: No change of RIC1.RWE13 1: Set RIC1.RWE13 to 0

Bit	Bit Name	Initial Value	R/W	Description
12	RWD12	0	R/W	Reception Warning interrupt Disable 12 This bit supports interrupt enable. It controls set of RIC1.RWE12. This bit is always read as 0. 0: No change of RIC1.RWE12 1: Set RIC1.RWE12 to 0
11	RWD11	0	R/W	Reception Warning interrupt Disable 11 This bit supports interrupt enable. It controls set of RIC1.RWE11. This bit is always read as 0. 0: No change of RIC1.RWE11 1: Set RIC1.RWE11 to 0
10	RWD10	0	R/W	Reception Warning interrupt Disable 10 This bit supports interrupt enable. It controls set of RIC1.RWE10. This bit is always read as 0. 0: No change of RIC1.RWE10 1: Set RIC1.RWE10 to 0
9	RWD9	0	R/W	Reception Warning interrupt Disable 9 This bit supports interrupt enable. It controls set of RIC1.RWE9. This bit is always read as 0. 0: No change of RIC1.RWE9 1: Set RIC1.RWE9 to 0
8	RWD8	0	R/W	Reception Warning interrupt Disable 8 This bit supports interrupt enable. It controls set of RIC1.RWE8. This bit is always read as 0. 0: No change of RIC1.RWE8 1: Set RIC1.RWE8 to 0
7	RWD7	0	R/W	Reception Warning interrupt Disable 7 This bit supports interrupt enable. It controls set of RIC1.RWE7. This bit is always read as 0. 0: No change of RIC1.RWE7 1: Set RIC1.RWE7 to 0
6	RWD6	0	R/W	Reception Warning interrupt Disable 6 This bit supports interrupt enable. It controls set of RIC1.RWE6. This bit is always read as 0. 0: No change of RIC1.RWE6 1: Set RIC1.RWE6 to 0
5	RWD5	0	R/W	Reception Warning interrupt Disable 5 This bit supports interrupt enable. It controls set of RIC1.RWE5. This bit is always read as 0. 0: No change of RIC1.RWE5 1: Set RIC1.RWE5 to 0
4	RWD4	0	R/W	Reception Warning interrupt Disable 4 This bit supports interrupt enable. It controls set of RIC1.RWE4. This bit is always read as 0. 0: No change of RIC1.RWE4 1: Set RIC1.RWE4 to 0

Bit	Bit Name	Initial Value	R/W	Description
3	RWD3	0	R/W	Reception Warning interrupt Disable 3 This bit supports interrupt enable. It controls set of RIC1.RWE3. This bit is always read as 0. 0: No change of RIC1.RWE3 1: Set RIC1.RWE3 to 0
2	RWD2	0	R/W	Reception Warning interrupt Disable 2 This bit supports interrupt enable. It controls set of RIC1.RWE2. This bit is always read as 0. 0: No change of RIC1.RWE2 1: Set RIC1.RWE2 to 0
1	RWD1	0	R/W	Reception Warning interrupt Disable 1 This bit supports interrupt enable. It controls set of RIC1.RWE1. This bit is always read as 0. 0: No change of RIC1.RWE1 1: Set RIC1.RWE1 to 0
0	RWD0	0	R/W	Reception Warning interrupt Disable 0 This bit supports interrupt enable. It controls set of RIC1.RWE0. This bit is always read as 0. 0: No change of RIC1.RWE0 1: Set RIC1.RWE0 to 0

33A.2.75 Reception Interrupt Enable register 2 (RIE2)

The RIE2 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFFS	—	—	—	—	—	—	—	—	—	—	—	—	—	QFS17	QFS16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QFS15	QFS14	QFS13	QFS12	QFS11	QFS10	QFS9	QFS8	QFS7	QFS6	QFS5	QFS4	QFS3	QFS2	QFS1	QFS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFFS	0	R/W	Rx-FIFO Full interrupt Set This bit supports interrupt enable. It controls set of RIC2.RFFE. This bit is always read as 0. 0: No change of RIC2.RFFE 1: Set RIC2.RFFE to 1
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	QFS17	0	R/W	Queue Full interrupt Set 17 This bit supports interrupt enable. It controls set of RIC2.QFE17. This bit is always read as 0. 0: No change of RIC2.QFE17 1: Set RIC2.QFE17 to 1
16	QFS16	0	R/W	Queue Full interrupt Set 16 This bit supports interrupt enable. It controls set of RIC2.QFE16. This bit is always read as 0. 0: No change of RIC2.QFE16 1: Set RIC2.QFE16 to 1
15	QFS15	0	R/W	Queue Full interrupt Set 15 This bit supports interrupt enable. It controls set of RIC2.QFE15. This bit is always read as 0. 0: No change of RIC2.QFE15 1: Set RIC2.QFE15 to 1
14	QFS14	0	R/W	Queue Full interrupt Set 14 This bit supports interrupt enable. It controls set of RIC2.QFE14. This bit is always read as 0. 0: No change of RIC2.QFE14 1: Set RIC2.QFE14 to 1
13	QFS13	0	R/W	Queue Full interrupt Set 13 This bit supports interrupt enable. It controls set of RIC2.QFE13. This bit is always read as 0. 0: No change of RIC2.QFE13 1: Set RIC2.QFE13 to 1

Bit	Bit Name	Initial Value	R/W	Description
12	QFS12	0	R/W	Queue Full interrupt Set 12 This bit supports interrupt enable. It controls set of RIC2.QFE12. This bit is always read as 0. 0: No change of RIC2.QFE12 1: Set RIC2.QFE12 to 1
11	QFS11	0	R/W	Queue Full interrupt Set 11 This bit supports interrupt enable. It controls set of RIC2.QFE11. This bit is always read as 0. 0: No change of RIC2.QFE11 1: Set RIC2.QFE11 to 1
10	QFS10	0	R/W	Queue Full interrupt Set 10 This bit supports interrupt enable. It controls set of RIC2.QFE10. This bit is always read as 0. 0: No change of RIC2.QFE10 1: Set RIC2.QFE10 to 1
9	QFS9	0	R/W	Queue Full interrupt Set 9 This bit supports interrupt enable. It controls set of RIC2.QFE9. This bit is always read as 0. 0: No change of RIC2.QFE9 1: Set RIC2.QFE9 to 1
8	QFS8	0	R/W	Queue Full interrupt Set 8 This bit supports interrupt enable. It controls set of RIC2.QFE8. This bit is always read as 0. 0: No change of RIC2.QFE8 1: Set RIC2.QFE8 to 1
7	QFS7	0	R/W	Queue Full interrupt Set 7 This bit supports interrupt enable. It controls set of RIC2.QFE7. This bit is always read as 0. 0: No change of RIC2.QFE7 1: Set RIC2.QFE7 to 1
6	QFS6	0	R/W	Queue Full interrupt Set 6 This bit supports interrupt enable. It controls set of RIC2.QFE6. This bit is always read as 0. 0: No change of RIC2.QFE6 1: Set RIC2.QFE6 to 1
5	QFS5	0	R/W	Queue Full interrupt Set 5 This bit supports interrupt enable. It controls set of RIC2.QFE5. This bit is always read as 0. 0: No change of RIC2.QFE5 1: Set RIC2.QFE5 to 1
4	QFS4	0	R/W	Queue Full interrupt Set 4 This bit supports interrupt enable. It controls set of RIC2.QFE4. This bit is always read as 0. 0: No change of RIC2.QFE4 1: Set RIC2.QFE4 to 1

Bit	Bit Name	Initial Value	R/W	Description
3	QFS3	0	R/W	Queue Full interrupt Set 3 This bit supports interrupt enable. It controls set of RIC2.QFE3. This bit is always read as 0. 0: No change of RIC2.QFE3 1: Set RIC2.QFE3 to 1
2	QFS2	0	R/W	Queue Full interrupt Set 2 This bit supports interrupt enable. It controls set of RIC2.QFE2. This bit is always read as 0. 0: No change of RIC2.QFE2 1: Set RIC2.QFE2 to 1
1	QFS1	0	R/W	Queue Full interrupt Set 1 This bit supports interrupt enable. It controls set of RIC2.QFE1. This bit is always read as 0. 0: No change of RIC2.QFE1 1: Set RIC2.QFE1 to 1
0	QFS0	0	R/W	Queue Full interrupt Set 0 This bit supports interrupt enable. It controls set of RIC2.QFE0. This bit is always read as 0. 0: No change of RIC2.QFE0 1: Set RIC2.QFE0 to 1

33A.2.76 Reception Interrupt Disable register 2 (RID2)

The RID2 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	RFFD	—	—	—	—	—	—	—	—	—	—	—	—	—	QFD17	QFD16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	QFD15	QFD14	QFD13	QFD12	QFD11	QFD10	QFD9	QFD8	QFD7	QFD6	QFD5	QFD4	QFD3	QFD2	QFD1	QFD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	RFFD	0	R/W	Rx-FIFO Full interrupt Disable This bit supports interrupt enable. It controls set of RIC2.RFFE. This bit is always read as 0. 0: No change of RIC2.RFFE 1: Set RIC2.RFFE to 0
30 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	QFD17	0	R/W	Queue Full interrupt Disable 17 This bit supports interrupt enable. It controls set of RIC2.QFE17. This bit is always read as 0. 0: No change of RIC2.QFE17 1: Set RIC2.QFE17 to 0
16	QFD16	0	R/W	Queue Full interrupt Disable 16 This bit supports interrupt enable. It controls set of RIC2.QFE16. This bit is always read as 0. 0: No change of RIC2.QFE16 1: Set RIC2.QFE16 to 0
15	QFD15	0	R/W	Queue Full interrupt Disable 15 This bit supports interrupt enable. It controls set of RIC2.QFE15. This bit is always read as 0. 0: No change of RIC2.QFE15 1: Set RIC2.QFE15 to 0
14	QFD14	0	R/W	Queue Full interrupt Disable 14 This bit supports interrupt enable. It controls set of RIC2.QFE14. This bit is always read as 0. 0: No change of RIC2.QFE14 1: Set RIC2.QFE14 to 0
13	QFD13	0	R/W	Queue Full interrupt Disable 13 This bit supports interrupt enable. It controls set of RIC2.QFE13. This bit is always read as 0. 0: No change of RIC2.QFE13 1: Set RIC2.QFE13 to 0

Bit	Bit Name	Initial Value	R/W	Description
12	QFD12	0	R/W	Queue Full interrupt Disable 12 This bit supports interrupt enable. It controls set of RIC2.QFE12. This bit is always read as 0. 0: No change of RIC2.QFE12 1: Set RIC2.QFE12 to 0
11	QFD11	0	R/W	Queue Full interrupt Disable 11 This bit supports interrupt enable. It controls set of RIC2.QFE11. This bit is always read as 0. 0: No change of RIC2.QFE11 1: Set RIC2.QFE11 to 0
10	QFD10	0	R/W	Queue Full interrupt Disable 10 This bit supports interrupt enable. It controls set of RIC2.QFE10. This bit is always read as 0. 0: No change of RIC2.QFE10 1: Set RIC2.QFE10 to 0
9	QFD9	0	R/W	Queue Full interrupt Disable 9 This bit supports interrupt enable. It controls set of RIC2.QFE9. This bit is always read as 0. 0: No change of RIC2.QFE9 1: Set RIC2.QFE9 to 0
8	QFD8	0	R/W	Queue Full interrupt Disable 8 This bit supports interrupt enable. It controls set of RIC2.QFE8. This bit is always read as 0. 0: No change of RIC2.QFE8 1: Set RIC2.QFE8 to 0
7	QFD7	0	R/W	Queue Full interrupt Disable 7 This bit supports interrupt enable. It controls set of RIC2.QFE7. This bit is always read as 0. 0: No change of RIC2.QFE7 1: Set RIC2.QFE7 to 0
6	QFD6	0	R/W	Queue Full interrupt Disable 6 This bit supports interrupt enable. It controls set of RIC2.QFE6. This bit is always read as 0. 0: No change of RIC2.QFE6 1: Set RIC2.QFE6 to 0
5	QFD5	0	R/W	Queue Full interrupt Disable 5 This bit supports interrupt enable. It controls set of RIC2.QFE5. This bit is always read as 0. 0: No change of RIC2.QFE5 1: Set RIC2.QFE5 to 0
4	QFD4	0	R/W	Queue Full interrupt Disable 4 This bit supports interrupt enable. It controls set of RIC2.QFE4. This bit is always read as 0. 0: No change of RIC2.QFE4 1: Set RIC2.QFE4 to 0

Bit	Bit Name	Initial Value	R/W	Description
3	QFD3	0	R/W	Queue Full interrupt Disable 3 This bit supports interrupt enable. It controls set of RIC2.QFE3. This bit is always read as 0. 0: No change of RIC2.QFE3 1: Set RIC2.QFE3 to 0
2	QFD2	0	R/W	Queue Full interrupt Disable 2 This bit supports interrupt enable. It controls set of RIC2.QFE2. This bit is always read as 0. 0: No change of RIC2.QFE2 1: Set RIC2.QFE2 to 0
1	QFD1	0	R/W	Queue Full interrupt Disable 1 This bit supports interrupt enable. It controls set of RIC2.QFE1. This bit is always read as 0. 0: No change of RIC2.QFE1 1: Set RIC2.QFE1 to 0
0	QFD0	0	R/W	Queue Full interrupt Disable 0 This bit supports interrupt enable. It controls set of RIC2.QFE0. This bit is always read as 0. 0: No change of RIC2.QFE0 1: Set RIC2.QFE0 to 0

33A.2.77 Transmission Interrupt Enable register (TIE)

The TIE register is used to control the Transmission Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TDPS3	TDPS2	TDPS1	TDPS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MFWS	MFUS	TFWS	TFUS	—	—	—	—	FTS3	FTS2	FTS1	FTS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
19	TDPS3	0	R/W	Transmit Descriptor Processed interrupt Set 3 This bit supports interrupt enable. It controls set of TIC.TDPE3. This bit is always read as 0. 0: No change of TIC.TDPE3 1: Set TIC.TDPE3 to 1
18	TDPS2	0	R/W	Transmit Descriptor Processed interrupt Set 2 This bit supports interrupt enable. It controls set of TIC.TDPE2. This bit is always read as 0. 0: No change of TIC.TDPE2 1: Set TIC.TDPE2 to 1
17	TDPS1	0	R/W	Transmit Descriptor Processed interrupt Set 1 This bit supports interrupt enable. It controls set of TIC.TDPE1. This bit is always read as 0. 0: No change of TIC.TDPE1 1: Set TIC.TDPE1 to 1
16	TDPS0	0	R/W	Transmit Descriptor Processed interrupt Set 0 This bit supports interrupt enable. It controls set of TIC.TDPE0. This bit is always read as 0. 0: No change of TIC.TDPE0 1: Set TIC.TDPE0 to 1
15 to 12	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
11	MFWS	0	R/W	E-MAC status FIFO Warning interrupt Set This bit supports interrupt enable. It controls set of TIC.MFWE. This bit is always read as 0. 0: No change of TIC.MFWE 1: Set TIC.MFWE to 1

Bit	Bit Name	Initial Value	R/W	Description
10	MFUS	0	R/W	E-MAC status FIFO Updated interrupt Set This bit supports interrupt enable. It controls set of TIC.MFUE. This bit is always read as 0. 0: No change of TIC.MFUE 1: Set TIC.MFUE to 1
9	TFWS	0	R/W	Timestamp FIFO Warning interrupt Set This bit supports interrupt enable. It controls set of TIC.TFWE. This bit is always read as 0. 0: No change of TIC.TFWE 1: Set TIC.TFWE to 1
8	TFUS	0	R/W	Timestamp FIFO Updated interrupt Set This bit supports interrupt enable. It controls set of TIC.TFUE. This bit is always read as 0. 0: No change of TIC.TFUE 1: Set TIC.TFUE to 1
7 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	FTS3	0	R/W	Frame Transmitted interrupt Set 3 This bit supports interrupt enable. It controls set of TIC.FTE3. This bit is always read as 0. 0: No change of TIC.FTE3 1: Set TIC.FTE3 to 1
2	FTS2	0	R/W	Frame Transmitted interrupt Set 2 This bit supports interrupt enable. It controls set of TIC.FTE2. This bit is always read as 0. 0: No change of TIC.FTE2 1: Set TIC.FTE2 to 1
1	FTS1	0	R/W	Frame Transmitted interrupt Set 1 This bit supports interrupt enable. It controls set of TIC.FTE1. This bit is always read as 0. 0: No change of TIC.FTE1 1: Set TIC.FTE1 to 1
0	FTS0	0	R/W	Frame Transmitted interrupt Set 0 This bit supports interrupt enable. It controls set of TIC.FTE0. This bit is always read as 0. 0: No change of TIC.FTE0 1: Set TIC.FTE0 to 1

33A.2.78 Transmission Interrupt Disable register (TID)

The TID register is used to control the Transmission Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TDPD3	TDPD2	TDPD1	TDPD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	MFWD	MFUD	TFWD	TFUD	—	—	—	—	FTD3	FTD2	FTD1	FTD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
19	TDPD3	All 0	R/W	Transmit Descriptor Processed interrupt Disable 3 This bit supports interrupt enable. It controls set of TIC.TDPE3. This bit is always read as 0. 0: No change of TIC.TDPE3 1: Set TIC.TDPE3 to 0
18	TDPD2	All 0	R/W	Transmit Descriptor Processed interrupt Disable 2 This bit supports interrupt enable. It controls set of TIC.TDPE2. This bit is always read as 0. 0: No change of TIC.TDPE2 1: Set TIC.TDPE2 to 0
17	TDPD1	All 0	R/W	Transmit Descriptor Processed interrupt Disable 1 This bit supports interrupt enable. It controls set of TIC.TDPE1. This bit is always read as 0. 0: No change of TIC.TDPE1 1: Set TIC.TDPE1 to 0
16	TDPD0	All 0	R/W	Transmit Descriptor Processed interrupt Disable 0 This bit supports interrupt enable. It controls set of TIC.TDPE0. This bit is always read as 0. 0: No change of TIC.TDPE0 1: Set TIC.TDPE0 to 0
15 to 12	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
11	MFWD	0	R/W	E-MAC status FIFO Warning interrupt Disable This bit supports interrupt enable. It controls set of TIC.MFWE. This bit is always read as 0. 0: No change of TIC.MFWE 1: Set TIC.MFWE to 0

Bit	Bit Name	Initial Value	R/W	Description
10	MFUD	0	R/W	E-MAC status FIFO Updated interrupt Disable This bit supports interrupt enable. It controls set of TIC.MFUE. This bit is always read as 0. 0: No change of TIC.MFUE 1: Set TIC.MFUE to 0
9	TFWD	0	R/W	Timestamp FIFO Warning interrupt Disable This bit supports interrupt enable. It controls set of TIC.TFWE. This bit is always read as 0. 0: No change of TIC.TFWE 1: Set TIC.TFWE to 0
8	TFUD	0	R/W	Timestamp FIFO Updated interrupt Disable This bit supports interrupt enable. It controls set of TIC.TFUE. This bit is always read as 0. 0: No change of TIC.TFUE 1: Set TIC.TFUE to 0
7 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	FTD3	0	R/W	Frame Transmitted interrupt Disable 3 This bit supports interrupt enable. It controls set of TIC.FTE3. This bit is always read as 0. 0: No change of TIC.FTE3 1: Set TIC.FTE3 to 0
2	FTD2	0	R/W	Frame Transmitted interrupt Disable 2 This bit supports interrupt enable. It controls set of TIC.FTE2. This bit is always read as 0. 0: No change of TIC.FTE2 1: Set TIC.FTE2 to 0
1	FTD1	0	R/W	Frame Transmitted interrupt Disable 1 This bit supports interrupt enable. It controls set of TIC.FTE1. This bit is always read as 0. 0: No change of TIC.FTE1 1: Set TIC.FTE1 to 0
0	FTD0	0	R/W	Frame Transmitted interrupt Disable 0 This bit supports interrupt enable. It controls set of TIC.FTE0. This bit is always read as 0. 0: No change of TIC.FTE0 1: Set TIC.FTE0 to 0

33A.2.79 Reception Interrupt Enable register 3 (RIE3)

The RIE3 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDPS17	RDPS16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDPS15	RDPS14	RDPS13	RDPS12	RDPS11	RDPS10	RDPS9	RDPS8	RDPS7	RDPS6	RDPS5	RDPS4	RDPS3	RDPS2	RDPS1	RDPS0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RDPS17	0	R/W	Receive Descriptor Processed interrupt Set 17 This bit supports interrupt enable. It controls set of RIC3.RDPE17. This bit is always read as 0. 0: No change of RIC3.RDPE17 1: Set RIC3.RDPE17 to 1
16	RDPS16	0	R/W	Receive Descriptor Processed interrupt Set 16 This bit supports interrupt enable. It controls set of RIC3.RDPE16. This bit is always read as 0. 0: No change of RIC3.RDPE16 1: Set RIC3.RDPE16 to 1
15	RDPS15	0	R/W	Receive Descriptor Processed interrupt Set 15 This bit supports interrupt enable. It controls set of RIC3.RDPE15. This bit is always read as 0. 0: No change of RIC3.RDPE15 1: Set RIC3.RDPE15 to 1
14	RDPS14	0	R/W	Receive Descriptor Processed interrupt Set 14 This bit supports interrupt enable. It controls set of RIC3.RDPE14. This bit is always read as 0. 0: No change of RIC3.RDPE14 1: Set RIC3.RDPE14 to 1
13	RDPS13	0	R/W	Receive Descriptor Processed interrupt Set 13 This bit supports interrupt enable. It controls set of RIC3.RDPE13. This bit is always read as 0. 0: No change of RIC3.RDPE13 1: Set RIC3.RDPE13 to 1
12	RDPS12	0	R/W	Receive Descriptor Processed interrupt Set 12 This bit supports interrupt enable. It controls set of RIC3.RDPE12. This bit is always read as 0. 0: No change of RIC3.RDPE12 1: Set RIC3.RDPE12 to 1

Bit	Bit Name	Initial Value	R/W	Description
11	RDPS11	0	R/W	Receive Descriptor Processed interrupt Set 11 This bit supports interrupt enable. It controls set of RIC3.RDPE11. This bit is always read as 0. 0: No change of RIC3.RDPE11 1: Set RIC3.RDPE11 to 1
10	RDPS10	0	R/W	Receive Descriptor Processed interrupt Set 10 This bit supports interrupt enable. It controls set of RIC3.RDPE10. This bit is always read as 0. 0: No change of RIC3.RDPE10 1: Set RIC3.RDPE10 to 1
9	RDPS9	0	R/W	Receive Descriptor Processed interrupt Set 9 This bit supports interrupt enable. It controls set of RIC3.RDPE9. This bit is always read as 0. 0: No change of RIC3.RDPE9 1: Set RIC3.RDPE9 to 1
8	RDPS8	0	R/W	Receive Descriptor Processed interrupt Set 8 This bit supports interrupt enable. It controls set of RIC3.RDPE8. This bit is always read as 0. 0: No change of RIC3.RDPE8 1: Set RIC3.RDPE8 to 1
7	RDPS7	0	R/W	Receive Descriptor Processed interrupt Set 7 This bit supports interrupt enable. It controls set of RIC3.RDPE7. This bit is always read as 0. 0: No change of RIC3.RDPE7 1: Set RIC3.RDPE7 to 1
6	RDPS6	0	R/W	Receive Descriptor Processed interrupt Set 6 This bit supports interrupt enable. It controls set of RIC3.RDPE6. This bit is always read as 0. 0: No change of RIC3.RDPE6 1: Set RIC3.RDPE6 to 1
5	RDPS5	0	R/W	Receive Descriptor Processed interrupt Set 5 This bit supports interrupt enable. It controls set of RIC3.RDPE5. This bit is always read as 0. 0: No change of RIC3.RDPE5 1: Set RIC3.RDPE5 to 1
4	RDPS4	0	R/W	Receive Descriptor Processed interrupt Set 4 This bit supports interrupt enable. It controls set of RIC3.RDPE4. This bit is always read as 0. 0: No change of RIC3.RDPE4 1: Set RIC3.RDPE4 to 1
3	RDPS3	0	R/W	Receive Descriptor Processed interrupt Set 3 This bit supports interrupt enable. It controls set of RIC3.RDPE3. This bit is always read as 0. 0: No change of RIC3.RDPE3 1: Set RIC3.RDPE3 to 1

Bit	Bit Name	Initial Value	R/W	Description
2	RDPS2	0	R/W	Receive Descriptor Processed interrupt Set 2 This bit supports interrupt enable. It controls set of RIC3.RDPE2. This bit is always read as 0. 0: No change of RIC3.RDPE2 1: Set RIC3.RDPE2 to 1
1	RDPS1	0	R/W	Receive Descriptor Processed interrupt Set 1 This bit supports interrupt enable. It controls set of RIC3.RDPE1. This bit is always read as 0. 0: No change of RIC3.RDPE1 1: Set RIC3.RDPE1 to 1
0	RDPS0	0	R/W	Receive Descriptor Processed interrupt Set 0 This bit supports interrupt enable. It controls set of RIC3.RDPE0. This bit is always read as 0. 0: No change of RIC3.RDPE0 1: Set RIC3.RDPE0 to 1

33A.2.80 Reception Interrupt Disable register 3 (RID3)

The RID3 register is used to control the Reception Interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RDPD17	RDPD16
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDPD15	RDPD14	RDPD13	RDPD12	RDPD11	RDPD10	RDPD9	RDPD8	RDPD7	RDPD6	RDPD5	RDPD4	RDPD3	RDPD2	RDPD1	RDPD0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17	RDPD17	0	R/W	Receive Descriptor Processed interrupt Disable 17 This bit supports interrupt enable. It controls set of RIC3.RDPE17. This bit is always read as 0. 0: No change of RIC3.RDPE17 1: Set RIC3.RDPE17 to 0
16	RDPD16	0	R/W	Receive Descriptor Processed interrupt Disable 16 This bit supports interrupt enable. It controls set of RIC3.RDPE16. This bit is always read as 0. 0: No change of RIC3.RDPE16 1: Set RIC3.RDPE16 to 0
15	RDPD15	0	R/W	Receive Descriptor Processed interrupt Disable 15 This bit supports interrupt enable. It controls set of RIC3.RDPE15. This bit is always read as 0. 0: No change of RIC3.RDPE15 1: Set RIC3.RDPE15 to 0
14	RDPD14	0	R/W	Receive Descriptor Processed interrupt Disable 14 This bit supports interrupt enable. It controls set of RIC3.RDPE14. This bit is always read as 0. 0: No change of RIC3.RDPE14 1: Set RIC3.RDPE14 to 0
13	RDPD13	0	R/W	Receive Descriptor Processed interrupt Disable 13 This bit supports interrupt enable. It controls set of RIC3.RDPE13. This bit is always read as 0. 0: No change of RIC3.RDPE13 1: Set RIC3.RDPE13 to 0
12	RDPD12	0	R/W	Receive Descriptor Processed interrupt Disable 12 This bit supports interrupt enable. It controls set of RIC3.RDPE12. This bit is always read as 0. 0: No change of RIC3.RDPE12 1: Set RIC3.RDPE12 to 0

Bit	Bit Name	Initial Value	R/W	Description
11	RDPD11	0	R/W	Receive Descriptor Processed interrupt Disable 11 This bit supports interrupt enable. It controls set of RIC3.RDPE11. This bit is always read as 0. 0: No change of RIC3.RDPE11 1: Set RIC3.RDPE11 to 0
10	RDPD10	0	R/W	Receive Descriptor Processed interrupt Disable 10 This bit supports interrupt enable. It controls set of RIC3.RDPE10. This bit is always read as 0. 0: No change of RIC3.RDPE10 1: Set RIC3.RDPE10 to 0
9	RDPD9	0	R/W	Receive Descriptor Processed interrupt Disable 9 This bit supports interrupt enable. It controls set of RIC3.RDPE9. This bit is always read as 0. 0: No change of RIC3.RDPE9 1: Set RIC3.RDPE9 to 0
8	RDPD8	0	R/W	Receive Descriptor Processed interrupt Disable 8 This bit supports interrupt enable. It controls set of RIC3.RDPE8. This bit is always read as 0. 0: No change of RIC3.RDPE8 1: Set RIC3.RDPE8 to 0
7	RDPD7	0	R/W	Receive Descriptor Processed interrupt Disable 7 This bit supports interrupt enable. It controls set of RIC3.RDPE7. This bit is always read as 0. 0: No change of RIC3.RDPE7 1: Set RIC3.RDPE7 to 0
6	RDPD6	0	R/W	Receive Descriptor Processed interrupt Disable 6 This bit supports interrupt enable. It controls set of RIC3.RDPE6. This bit is always read as 0. 0: No change of RIC3.RDPE6 1: Set RIC3.RDPE6 to 0
5	RDPD5	0	R/W	Receive Descriptor Processed interrupt Disable 5 This bit supports interrupt enable. It controls set of RIC3.RDPE5. This bit is always read as 0. 0: No change of RIC3.RDPE5 1: Set RIC3.RDPE5 to 0
4	RDPD4	0	R/W	Receive Descriptor Processed interrupt Disable 4 This bit supports interrupt enable. It controls set of RIC3.RDPE4. This bit is always read as 0. 0: No change of RIC3.RDPE4 1: Set RIC3.RDPE4 to 0
3	RDPD3	0	R/W	Receive Descriptor Processed interrupt Disable 3 This bit supports interrupt enable. It controls set of RIC3.RDPE3. This bit is always read as 0. 0: No change of RIC3.RDPE3 1: Set RIC3.RDPE3 to 0

Bit	Bit Name	Initial Value	R/W	Description
2	RDPD2	0	R/W	Receive Descriptor Processed interrupt Disable 2 This bit supports interrupt enable. It controls set of RIC3.RDPE2. This bit is always read as 0. 0: No change of RIC3.RDPE2 1: Set RIC3.RDPE2 to 0
1	RDPD1	0	R/W	Receive Descriptor Processed interrupt Disable 1 This bit supports interrupt enable. It controls set of RIC3.RDPE1. This bit is always read as 0. 0: No change of RIC3.RDPE1 1: Set RIC3.RDPE1 to 0
0	RDPD0	0	R/W	Receive Descriptor Processed interrupt Disable 0 This bit supports interrupt enable. It controls set of RIC3.RDPE0. This bit is always read as 0. 0: No change of RIC3.RDPE0 1: Set RIC3.RDPE0 to 0

33A.2.81 E-MAC Mode Register (ECMR)

ECMR is used to specify the operating mode of the E-MAC. The settings in this register are normally made in the initialization process following a reset.

The operating mode settings must not be changed while transmission or reception is enabled (i.e. while the RE or TE bit in this register is 1).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	TRCCM	—	—	RCSC	—	DPAD	RZPF	TZPF	PFR	RXF	TXF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	MPDE	—	—	RE	TE	—	—	—	DM	PRM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
26	TRCCM	0	R/W	Counter Clear Mode This bit sets the method for clearing the counter register. Refer to the descriptions of the counter registers. 0: Writing to a counter register leads to the register being cleared to 0. 1: Reading from a counter register leads to the register being cleared to 0.
25, 24	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
23	RCSC	0	R/W	Checksum Calculation Setting this bit to 1 enables automatic calculation of checksums for data in received frames. Only the data field of an Ethernet frame without a VLAN field is in the scope of checksum calculation. Specifically, the checksum is calculated from the data field, which follows the length/type field and is followed by the CRC field. Calculation only involves 16-bit addition; it does not involve bit inversion. 0: Checksums are not automatically calculated. 1: Checksums are automatically calculated.
22	—	0	R/W	Reserved This bit is read as 0. The write value should be 0.
21	DPAD	0	R/W	Data Padding This bit specifies padding or non-padding of data when less than 60 bytes are to be transmitted. When this bit is set to 1, data are transmitted without padding; when it is set to 0, data are padded to make up 60-byte units for transmission. 0: Padding to make up 60 bytes is inserted in data for transmission when fewer than 60 bytes are to be transmitted. 1: Padding is not inserted in data for transmission when fewer than 60 bytes are to be transmitted and the data are transmitted without being changed.

Bit	Bit Name	Initial Value	R/W	Description
20	RZPF	0	R/W	PAUSE Frame Reception with Time = 0 When the RZPF bit is set to 0, received PAUSE frames with the Timer value 0 are discarded. When the RZPF bit is set to 1, release from the transmission wait state follows reception of a PAUSE frame with the Timer value 0. 0: Reception of PAUSE frames with the TIME parameter value 0 is disabled. 1: Reception of PAUSE frames with the TIME parameter value 0 is enabled.
19	TZPF	0	R/W	Transmit Zero PAUSE Frame When setting CCC.FCE=1, and Rx FIFO become Warning Level. 0: Not transmit the PAUSE frame of TIME parameter value 0. 1: Transmit the PAUSE frame of TIME parameter value 0.
18	PFR	0	R/W	PAUSE Frame Receive Mode This bit specifies whether PAUSE frames are transferred to the AVB-DMAC. 0: PAUSE frames are not transferred to the AVB-DMAC. 1: PAUSE frames are transferred to the AVB-DMAC.
17	RXF	0	R/W	Operating Mode for Flow Control in Reception When the RXF bit is set to 1 and a PAUSE frame is received, a next frame to be transmitted is not transmitted until the time indicated by the Timer value in the PAUSE frame has elapsed. However, the transmission of a current frame is continued. The number of received PAUSE frames is also counted. For details, see section 33A.2.91 PAUSE Frame Receive Counter (PFRCR). Setting this bit to 0 disables PAUSE frame detection. 0: Detection of PAUSE frames is disabled. 1: Flow control for the receiving port is enabled.
16	TXF	0	R/W	Transmit Flow control mode 0: Flow control for the transmitting port is disabled. 1: Flow control for the transmitting port is enabled.
15 to 10	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
9	MPDE	0	R/W	Magic Packet™ Detection Enable The MPDE bit enables or disables Magic Packet™ detection by hardware to allow activation via the Ethernet connection. 0: Magic Packet™ detection is not enabled. 1: Magic Packet™ detection is enabled.
8, 7	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
6	RE	0	R/W	Reception Enable If this bit is switched from reception being enabled (RE = 1) to reception being disabled (RE = 0) while a frame is being received, reception will continue until reception of the frame is completed. 0: Reception is disabled. 1: Reception is enabled.

Bit	Bit Name	Initial Value	R/W	Description
5	TE	0	R/W	Transmission Enable If this bit is switched from transmission being enabled (TE = 1) to transmission being disabled (TE = 0) while a frame is being transmitted, transmission will continue until transmission of that frame is completed. 0: Transmission is disabled. 1: Transmission is enabled.
4 to 2	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
1	DM	0	R/W	Duplex Mode This bit should always be set to 1. The value after reset is 0. 0: Value after reset 1: Full-duplex operation This bit should always be set to 1.
0	PRM	0	R/W	Promiscuous Mode Setting the PRM bit enables all Ethernet frames to be received. All Ethernet frames mean all receivable frames, irrespective of differences of destination address (exclude PAUSE frame). 0: Normal operation 1: Promiscuous mode operation

33A.2.82 Receive Frame Length Register (RFLR)

The RFLR register specifies the maximum length (in bytes) of frames that can be received by this LSI. Settings in this register must not be changed while reception is enabled (while the RE bit in the E-MAC mode register (EMCR) is 1).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	RFL[17:16]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
17 to 0	RFL[17:0]	H'0 0000	R/W	Receive Frame Length Frame data described here refers to all fields from the destination address up to the CRC data. Frame contents from the destination address up to the data are actually transferred to memory. CRC data are not included in the transfer. When more data than the specified number of bytes are received, the portion of data that exceeds the specified value and more 8 byte length is discarded. CAUTION: The prepared descriptor data size is just the specified value (RFLR.RFL). Therefore descriptor data size must be more than RFLR.RFL + 8 if you will receive such the long frame. H'0 0000 to H'0 05EE: 1,518 bytes H'0 05EF: 1,519 bytes H'0 05F0: 1,520 bytes : : H'0 07FF: 2,047 bytes H'0 0800: 2,048 bytes : : H'0 1000: 4,096 bytes : : H'1 0000: 65,535 bytes : : H'2 0000 to H'3 FFFF: 131,072 bytes

33A.2.83 E-MAC Status Register (ECSR)

The ECSR register indicates the state of the E-MAC. The CPU can be notified of the state. For bits associated with interrupts, the interrupt can be enabled or disabled by the corresponding bit in the E-MAC Interrupt Permission Register (ECSIPR) described in section 33A.2.84.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PFRI	PHYI	LCHNG	MPD	ICD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
4	PFRI	0	R/W	PAUSE Frame Retry Interrupt This bit indicate that reached to the number of PAUSE frame retransmission for register PFTTLR setting. Procedure for 0-clear to this bit is follows. 0: Read the PFTTCR register to clear the PFTTCR register. 1: Write to this bit 1.
3	PHYI	0	R/W	PHY interrupt terminal state bit This bit indicates the state of input to the PHY interrupt pin (AVB_PHY_INT) from the PHY-LSI. 0: PHY interrupt terminal (AVB_PHY_INT) is not asserted. 1: PHY interrupt terminal (AVB_PHY_INT) is asserted.
2	LCHNG	0	R/W	Link signal change bit This bit indicates a transition of the link status signal (AVB_LINK) input from the PHY-LSI from high to low or low to high. However, signal changes may also be detected at times when the link status signal (AVB_LINK) function is selected. To check the current link state, refer to the link status pin state bit in the PHY status register (PSR.LMON). 0: The change of Link status signal (AVB_LINK) is not detected. 1: The change of Link status signal (AVB_LINK) is detected.
1	MPD	0	R/W	Magic Packet™ Detection This bit indicates that a Magic Packet™ has been detected on the line. Writing 1 to this bit clears it to 0. 0: A Magic Packet™ has not been detected. 1: A Magic Packet™ has been detected.

Bit	Bit Name	Initial Value	R/W	Description
0	ICD	0	R/W	Illegal Carrier Detection This bit indicates that the PHY-LSI has detected an illegal carrier on the line. If a change in the signal input from the PHY-LSI occurs in a period shorter than the software recognition period, the correct information may not be obtained. Refer to the timing specification for the PHY-LSI used. Writing 1 to this bit clears it to 0. 0: PHY-LSI has not detected an illegal carrier on the line. 1: PHY-LSI has detected an illegal carrier on the line.

33A.2.84 E-MAC Interrupt Permission Register (ECSIPR)

The ECSIPR register enables or disables the states indicated by the ECSR register as interrupt sources. Each effective bit disables or enables interrupts corresponding to the bits in ECSR.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PFRIM	PHYIM	LINKIM	MPDIP	ICDIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
4	PFRIM	0	R/W	PAUSE Frame Retry Interrupt Mask Setting this bit to 1 selects interrupt generation on setting of the PAUSE Frame Retry Interrupt bit (ECSR. PFRI) in the E-MAC status register to 1. 0: Interrupts on setting of the PFRI bit is disabled. 1: Interrupts on setting of the PFRI bit is enabled.
3	PHYIM	0	R/W	PHY Interrupt Mask Setting this bit to 1 selects interrupt generation on setting of the PHY interrupt terminal state bit (ECSR. PHYI) in the E-MAC status register to 1. 0: Interrupts on setting of the PHYI bit is disabled. 1: Interrupts on setting of the PHYI bit is enabled.
2	LINKIM	0	R/W	LINK Interrupt Mask Setting this bit to 1 selects interrupt generation on setting of the Link signal change bit (ECSR. LCHNG) in the E-MAC status register to 1. 0: Interrupts on setting of the LCHNG bit is disabled. 1: Interrupts on setting of the LCHNG bit is enabled.
1	MPDIP	0	R/W	Magic Packet™ Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the Magic Packet™ detection bit (ECSR.MPD) in the E-MAC status register to 1. 0: Interrupts on setting of the MPD bit is disabled. 1: Interrupts on setting of the MPD bit is enabled.
0	ICDIP	0	R/W	Illegal Carrier Detect Interrupt Enable Setting this bit to 1 selects interrupt generation on setting of the illegal carrier detection bit (ECSR.ICD) in the E-MAC status register to 1. 0: Interrupts on setting of the ICD bit is disabled. 1: Interrupt on setting of the ICD bit is enabled.

33A.2.85 PHY Interface Register (PIR)

The PIR register provides a means of access to the PHY-LSI internal registers via the MII.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MDI	MDO	MMD	MDC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	—	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
3	MDI	—	R/W	MII Management Data-In This bit indicates the level of the AVB_MDIO pin.
2	MDO	0	R/W	MII Management Data-Out This bit holds data for output from the AVB_MDIO pin. The AVB_MDIO pin outputs data when the MMD bit is set to 1 (to specify writing as the direction). Data are not output while the MMD bit is set to 0 (to specify reading as the direction).
1	MMD	0	R/W	MII Management Mode This bit specifies the direction for data through MDIO (reading or writing). 0: Read direction is specified. 1: Write direction is specified.
0	MDC	0	R/W	MII Management Data Clock Values set in this bit are output on the AVB_MDC pin to supply the MII with the management data clock. For the method of access to the MII registers, see section 33A.3.13 Connection to PHY-LSI.

33A.2.86 PHY Status Register (PSR)

The PSR register is a read-only register that can read interface signals from the PHY-LSI.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LMON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are read as 0.
0	LMON	0	R	Link Status Pin State The Link state can be read by connecting the Link signal output from the PHY-LSI to the link status pin (AVB_LNK) pin. For the active sense, refer to the specifications of the PHY-LSI to be connected. 0: The link status signal (AVB_LNK) is at the low level. 1: The link status signal (AVB_LNK) is at the high level.

33A.2.87 PHY_INT Polarity Register (PIPR)

The PIPR register is used to set the active sense of the AVB_PHY-INT pin.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

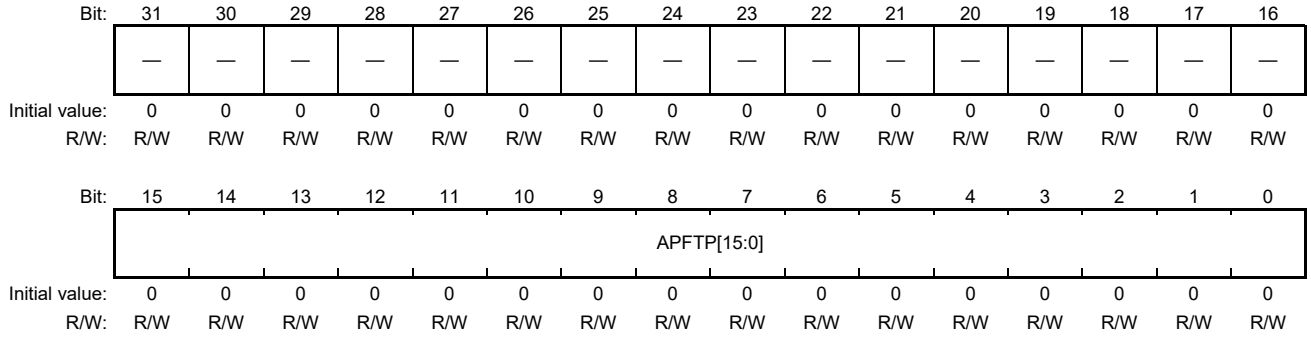
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PHYIP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
0	PHYIP	0	R/W	PHY Interrupt Input Pin Polarity This bit sets the active sense of the PHY interrupt pin (AVB_PHY-INT). For the active sense, refer to the specifications of the PHY-LSI to be connected. 0: PHY interrupt pin (AVB_PHY-INT) is active low (the low level triggers the interrupt state) 1: PHY interrupt pin (AVB_PHY-INT) is active high (the high level triggers the interrupt state)

33A.2.88 Automatic PAUSE frame register (APR)

The APR register is used to set the value for the TIME parameter of auto generated PAUSE frames.

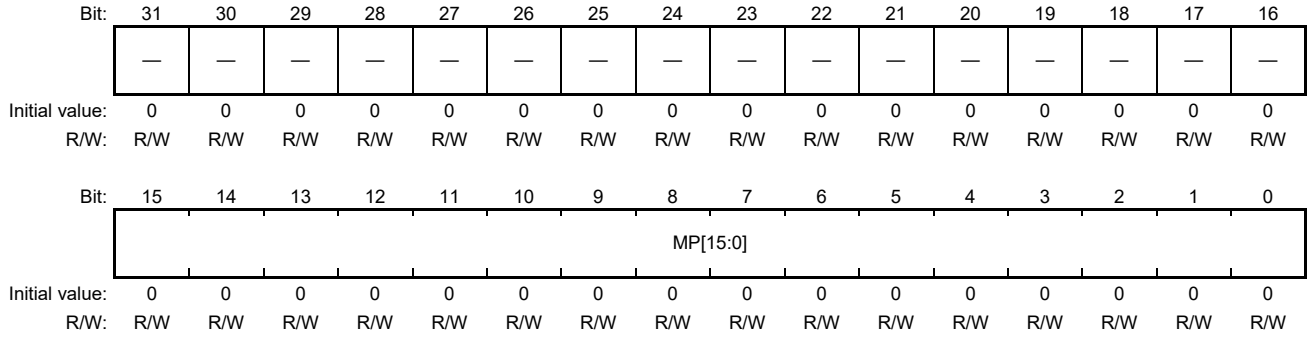
When ECMR.TXF = B'1, the value shouldn't set all 0 in this register.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	APFTP[15:0]	H'0000	R/W	Auto Pause Frame Time Parameter When a PAUSE frame is auto transmitted, the value set in this register is used as its TIME parameter. H'0000: — H'0001: 1 × 512 bit time H'0002: 2 × 512 bit time : : H'FFFF: 65535 × 512 bit time A bit time changes relative to the transfer speed as follows. 1000 Mbps:1 bit time = 1 ns 100 Mbps: 1 bit time = 10 ns

33A.2.89 Manual PAUSE Frame Register (MPR)

The MPR register is used to set the value for the TIME parameter of manually generated PAUSE frames. When a PAUSE frame is manually transmitted, the value set in this register is used as its TIME parameter.



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MP[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	MP[15:0]	H'0000	R/W	Manual PAUSE These bits set the value of the TIME parameter in manually generated PAUSE frames. The unit for the setting is 512 bit time. These bits set the TIME parameter value of a manual PAUSE frame. H'0000: — H'0001: 1 × 512 bit time H'0002: 2 × 512 bit time : : H'FFFF: 65535 × 512 bit time A bit time changes relative to the transfer speed as follows. 1000 Mbps: 1 bit time = 1 ns 100 Mbps: 1 bit time = 10 ns

33A.2.90 PAUSE Frame Transmit Counter (PFTCR)

The PFTCR register is a counter that indicates the number of times PAUSE frames have been transmitted.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PFTXC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
15 to 0	PFTXC[15:0]	H'0000	R	PAUSE Frame Transmit Counter Counter for counting the number of transmitted PAUSE frames The bits are cleared to 0 when they are read. If counting up and clearing of the counter coincide, clearing the counter takes priority.

33A.2.91 PAUSE Frame Receive Counter (PFRCR)

The RFRCR register is a counter that indicates the number of times PAUSE frames have been received.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PFRXC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are read as 0. The write value should be 0.
15 to 0	PFRXC[15:0]	H'0000	R	PAUSE Frame Receive Counter These bits indicate the number of PAUSE frames that have been received when flow control in reception is enabled (the RXF bit in ECMR = 1). The bits are cleared to 0 when they are read. If counting up and clearing the counter coincide, clearing the counter takes priority.

33A.2.92 Automatic PAUSE frame retransmit count register (TPAUSER)

The TPAUSER register is used to set the value for upper limit number of auto generated PAUSE frames.

The setting in this register must not be changed while transmission is enabled.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PFRTULMT[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	PFRTULMT [15:0]	H'0000	R/W	Pause Frame Retry Upper LiMiT These bit's set the value for upper limit time of auto generated PAUSE frames while Receive FIFO caution. H'0000: unlimited H'0001: 1 time H'0002: 2 times : : H'FFFF: 65535 times

33A.2.93 PAUSE frame transmit times counter (PFTTCR)

The PFTTCR register is a counter that indicates the number of times auto PAUSE frames have been transmit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PFRTC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	PFRTC[15:0]	H'0000	R	Pause Frame Retry Counter These bits indicate the number of auto PAUSE frames that have been transmit while Receive FIFO caution. The bits are cleared to 0 when they are read and Receive FIFO caution start.

33A.2.94 E-MAC Mode Register 2 (GECMR)

The GECMR register specifies the operating mode for the E-MAC.

The setting in the GECMR register must not be changed while transmission or reception is enabled.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

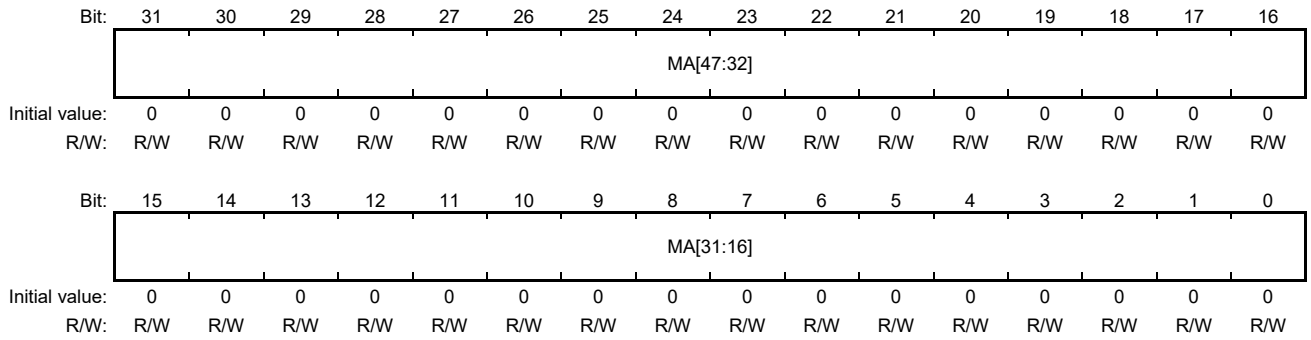
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SPEED
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
0	SPEED	0	R/W	Transfer Speed Setting This bit sets the transfer rate. 0: Transfer is at 100 Mbps. 1: Transfer is at 1000 Mbps.

33A.2.95 E-MAC Address High Register (MAHR)

The MAHR register specifies the 32 higher-order bits of the 48-bit E-MAC address. The settings in this register are normally made in the initialization process after a reset.

The settings in this register must not be changed while transmission or reception is enabled.

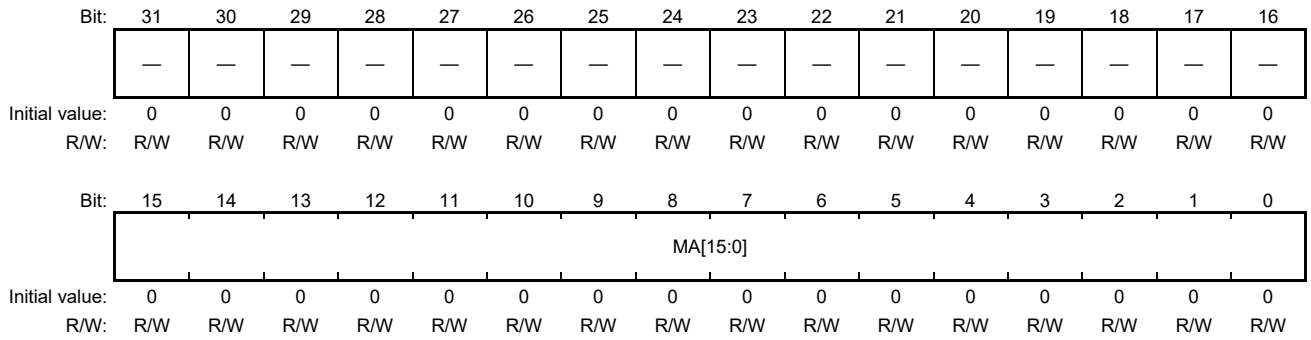


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	MA[47:16]	H'0000 0000	R/W	E-MAC Address Bits 47 to 16 These bits are used to set the 32 higher-order bits of the E-MAC address. For example, if the E-MAC address is 01-23-45-67-89-AB (hexadecimal), set H'0123 4567 in the MAHR register.

33A.2.96 E-MAC Address Low Register (MALR)

The MALR register specifies the 16 lower-order bits of the 48-bit E-MAC address. The settings in this register are normally made in the initialization process after a reset.

The settings in this register must not be changed while transmission or reception is enabled.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	MA[15:0]	H'0000	R/W	E-MAC Address Bits 15 to 0 These bits are used to set the 16 lower-order bits of the E-MAC address. For example, if the E-MAC address is 01-23-45-67-89-AB (hexadecimal), set H'89AB in the MALR register.

33A.2.97 Transmit retry over counter register (TROCR)

The TROCR register is a counter that indicates the number of times frames with time-out were transmit. Counting up stops when the value in this register reaches H'0000 FFFF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FTTOC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	FTTOC [15:0]	H'0000	R/W	Frame transmit time-out counter These bits indicate the number of transmit frames having time-out. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.2.98 CRC Error Frame Receive Counter Register (CEFCR)

The CEFCR register is a counter that indicates the number of times frames with CRC errors were received. Counting up stops when the value in this register reaches H'0000 FFFF.

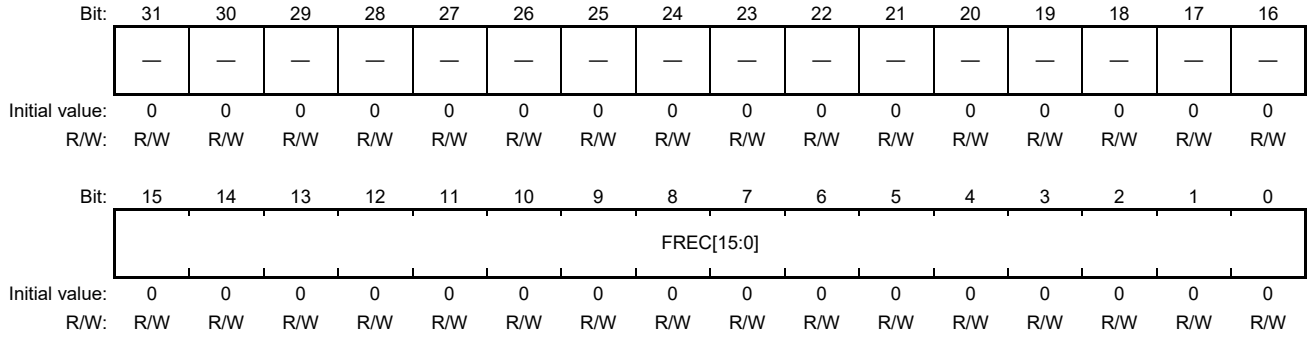
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CEFC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	CEFC[15:0]	H'0000	R/W	CRC Error Frame Counter These bits indicate the number of received frames having CRC errors. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.2.99 Frame Receive Error Counter Register (FRECR)

The FRECR register is a counter that indicates the number of frames for which receive errors were generated by input on the AVB_RX_ER pin from the PHY-LSI. Counting up stops when the value in this register reaches H'0000 FFFF.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	FREC[15:0]	H'0000	R/W	Frame Receive Error Counter These bits indicate the number of errors during frame reception. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.2.100 Too-Short Frame Receive Counter Register (TSFRCR)

The TSFRCR register is a counter that indicates the number of received frames that were fewer than 64 bytes in length. Counting stops when the value in this register reaches H'0000 FFFF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSFRC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	TSFRC[15:0]	H'0000	R/W	Too-Short Frame Receive Counter These bits indicate the number of received frames that were fewer than 64 bytes in length. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.2.101 Too-Long Frame Receive Counter Register (TLFRCR)

The TLFRCR register is a counter that indicates the number of received frames that were longer than the value specified in the receive frame length register (RFLR). Counting up stops when the value in the TLFRCR register reaches H'0000 FFFF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TLFC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	TLFC[15:0]	H'0000	R/W	Too-Long Frame Receive Counter These bits indicate the number of received frames that were longer than the value in RFLR. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.2.102 Residual-Bit Frame Receive Counter Register (RFCR)

The RFCR register is a counter that indicates the number of received frames containing “residual bits” (trailing bits not making up an 8-bit unit). Counting up stops when the value in this register reaches H'0000 FFFF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	RFC[15:0]	H'0000	R/W	Residual-Bit Frame Receive Counter These bits indicate the number of received frames containing residual bits. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.2.103 Multicast Address Frame Receive Counter Register (MAFCR)

The MAFCR register is a counter that indicates the number of received frames for which a multicast address was specified. Counting up stops when the value in this register reaches H'0000 FFFF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MAFC[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R/W	Reserved These bits are read as 0. The write value should be 0.
15 to 0	MAFC[15:0]	H'0000	R/W	Multicast Address Frame Counter These bits indicate the number of multicast frames that have been received. The bits are cleared to 0 when they are read while the counter clear mode bit (TRCCM) in the E-MAC mode register is set to 1. When TRCCM = 0, they are cleared to 0 by the writing of any value to this register.

33A.3 Operation

The EthernetAVB consists of the following functional units:

- DMA transfer controller (AVB-DMAC): Handles DMA transfer between the data storage areas for reception and transmission in the URAM and the reception and transmission FIFO buffers
- MAC controller (E-MAC): Handles transfer between the reception and transmission FIFO buffers and the RGMII

Using its direct memory access (DMA) function, the AVB-DMAC handles DMA transfer of frame data between the destinations for storing Ethernet frame data for transmission and reception in the URAM and the FIFO buffers for reception and transmission. Data cannot be directly read from or written to the FIFO buffers.

To handle DMA transfer, the AVB-DMAC requires information that includes the addresses for storage of data for transmission and received data. These data are referred to as descriptors. The AVB-DMAC reads data for transmission from the storage area for data to be transmitted according to the information in descriptors and writes received data to the storage area for received data accompanied by information in descriptors. The descriptors are placed in the URAM. Arranging multiple descriptors in descriptor lists allows the continuous reception or transmission of multiple Ethernet frames.

The E-MAC supports a RGMII, which provides an interface format for the externally connected PHY-LSI. The E-MAC constructs Ethernet frames from data written to the transmission FIFO and transmits these frames to the RGMII. It also performs CRC checking of Ethernet frames received from the RGMII and writes the frames to the reception FIFO.

33A.3.1 AVB-DMAC Operating Modes

Figure 33A.2 illustrates the operating modes of the AVB-DMAC.

Transitions of AVB-DMAC operating mode are under the control of the items listed below.

- CPU operating mode (hardware reset and power-down mode)
- Configuration of the operating mode configuration bits (CCC.OPC) in the AVB-DMAC mode register

The current operating mode can be confirmed by reading the operating mode status bits in the AVB-DMAC status register (CSR.OPS).

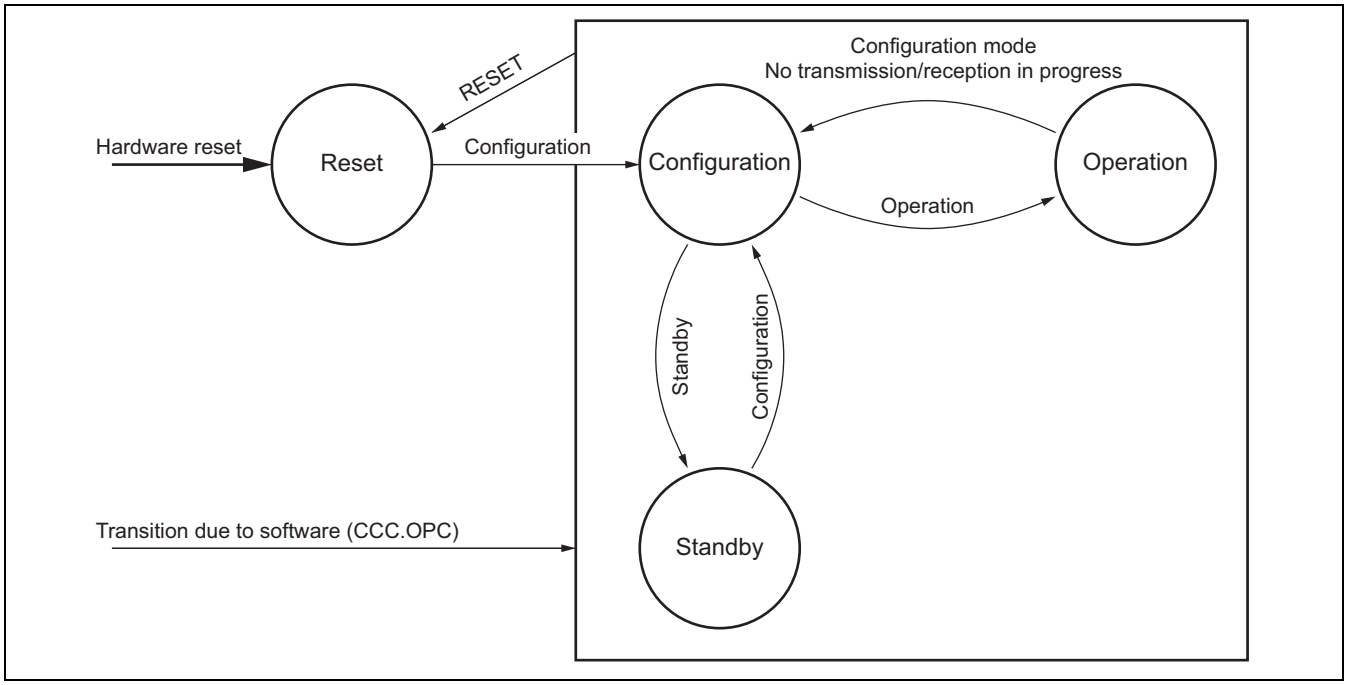


Figure 33A.2 Operating Mode of AVB-DMAC

33A.3.1.1 Operating Modes

(1) Reset mode

After a hardware reset, the AVB-DMAC enters reset mode.
In reset mode, only the AVB-DMAC operating mode control function is controllable and other functions are all stopped. This mode is designed for reduced power when the Ethernet function is not necessary.

(2) Configuration mode

In configuration mode, various settings for the AVB-DMAC can be made.
The operation of most functions is stopped and all status registers are initialized to their reset values. The E-MAC functions in this mode.
By CCC.GAC it is possible to enable gPTP support already in CONFIG mode.

(3) Operation mode

In operation mode, all functions of the AVB-DMAC can operate. Ethernet communications can only proceed in this mode.

(4) Standby mode

In standby mode, the E-MAC can only be used to control the operating mode. Other functions cannot be used.
When CCC.GAC is 1 CPU should not enter STANDBY mode.

33A.3.1.2 How to Set the Operating Mode

Set the operating mode configuration bits in the AVB-DMAC mode register (CCC.OPC) to select the operating mode. Furthermore, the current operating mode can be checked by reading the operating mode status bits in the AVB-DMAC status register (CSR.OPS).

Transitions other than from operation mode to configuration mode are made after the value is written to the operating mode configuration bits (CCC.OPC) (Figure 33A.3).

For transitions from operation mode to configuration mode, follow the procedure in Figure 33A.4 because any transmission and reception in progress will be executed before the transition to configuration mode.

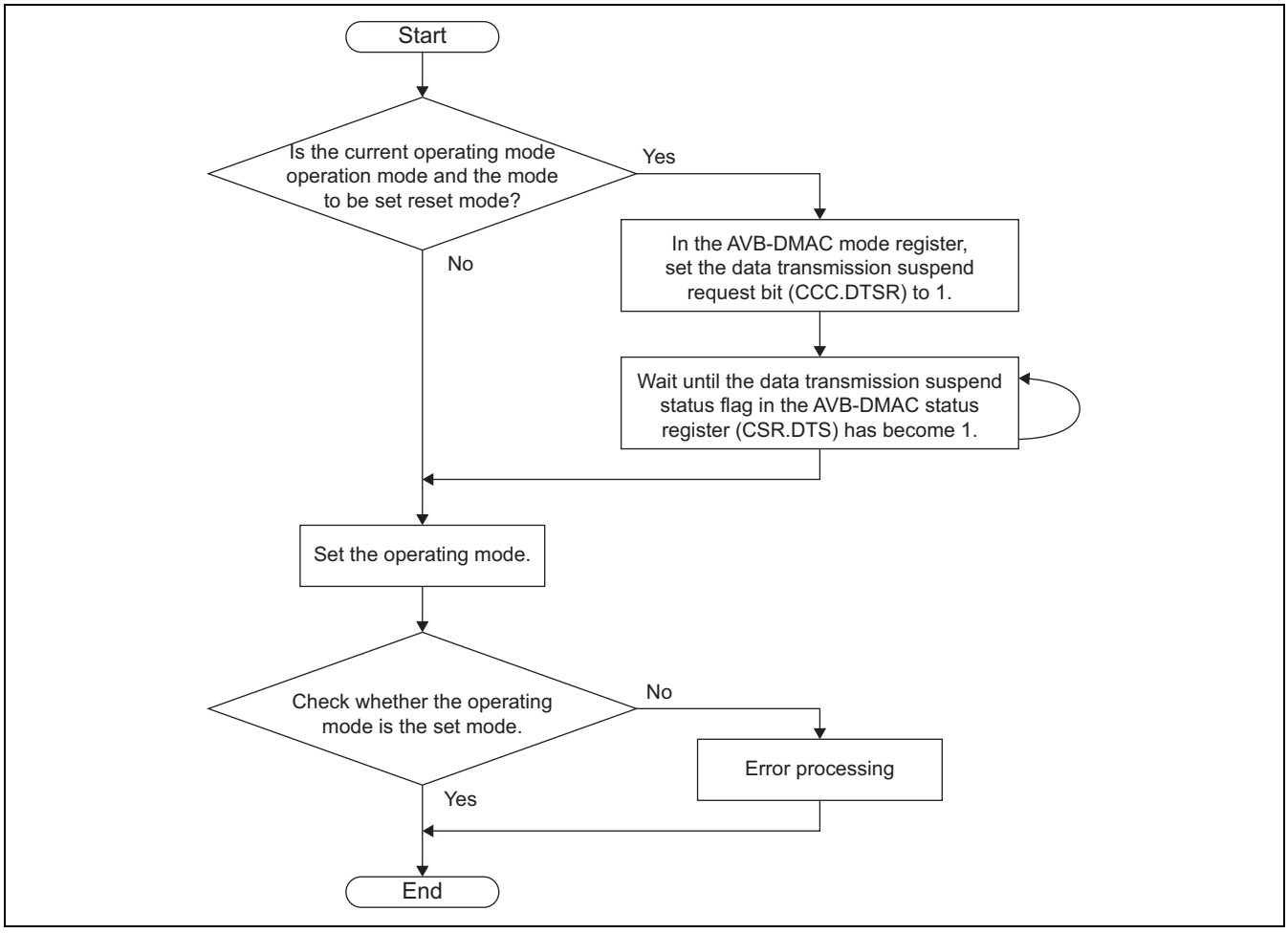


Figure 33A.3 Flow for Transitions of Operating Mode (Other than from Operation Mode to Configuration Mode)

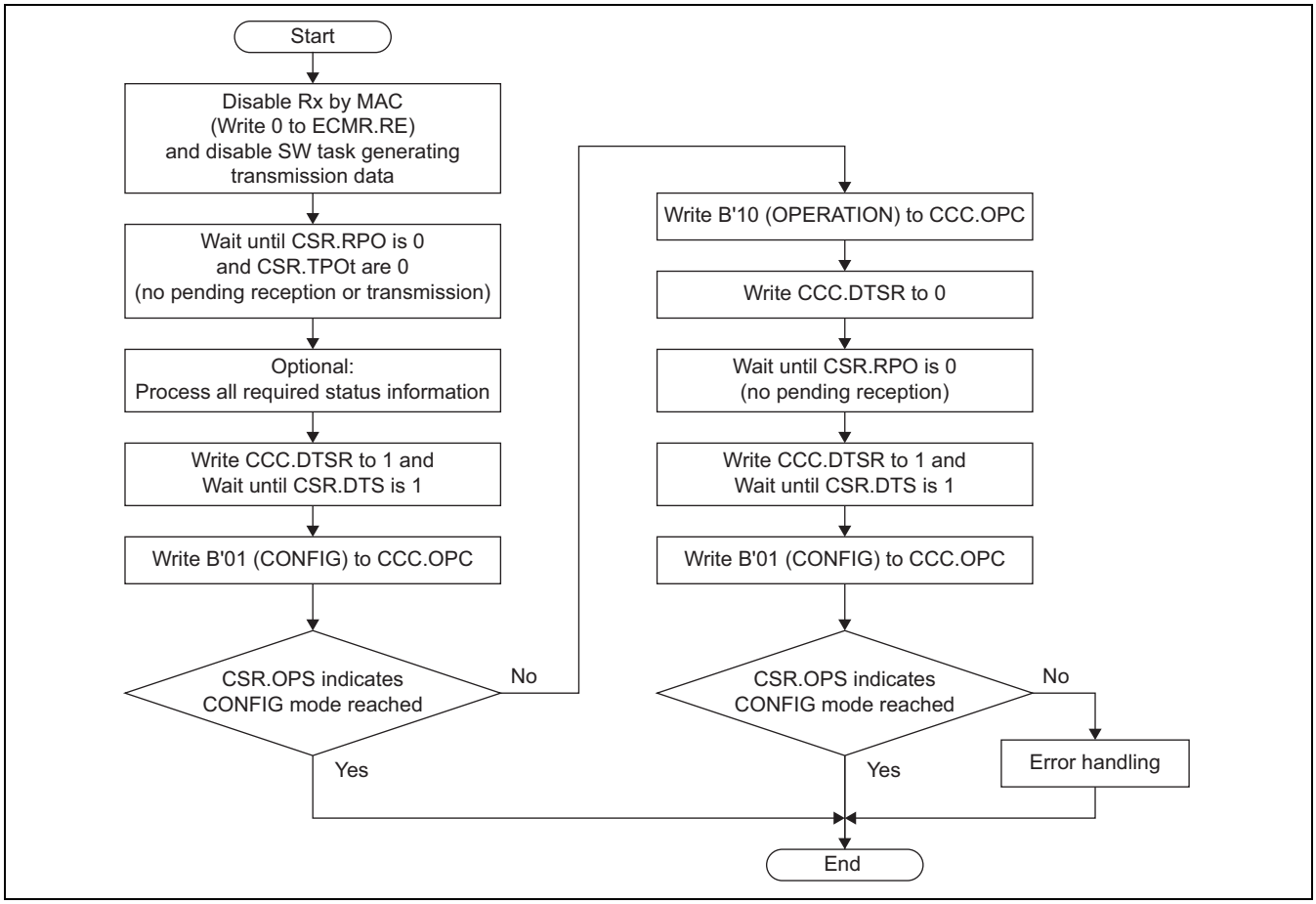


Figure 33A.4 Flow for Transitions of Operating Mode (from Operation Mode to Configuration Mode)

In the transition from operation mode to configuration mode, the AVB-DMAC executes the following operations before the transition is completed. Read the operating mode status bits in the AVB-DMAC status register (CSR.OPS) to check that the transition to configuration mode has been completed.

- If the transfer of a frame between the reception FIFO and URAM is in progress, this is completed (other received frames remaining in the FIFO and any frames that are subsequently received by the E-MAC are discarded).
- If the transfer of a frame is in progress between the transmission FIFO and URAM, this is completed (frames for transmission remaining in the URAM will not be transmitted).
- All frames for transmission in the transmission FIFO are transferred to the E-MAC.

The CPU should not disable URAM transfers by CCC.DTSR nor prevent transmission by MAC when requesting transition from OPERATION to CONFIG, else EthernetAVB cannot perform requested mode change.

Notes: When the operating mode shifts to configuration mode, all status registers are cleared.
We recommend following the procedure below in the case of this transition.

1. Disable reception.
2. Since reception actually stopping after being disabled requires time, wait for an interval equivalent to that for reception of a maximum length packet.
3. Stop the software task that is generating data for transmission.
4. Wait until the receive process status bit (CSR.RPO) and the transmit process status bits (CSR.TPO0 to 3) in the AVB-DMAC status register are set to 0.
5. Capture all of the required status information.

6. Set the operating mode configuration bits in the AVB-DMAC mode register (CCC.OPC) to initiate the transition to configuration mode.

33A.3.1.3 Leave RESET mode with additional configuration

When writing B'01 (CONFIG) to CCC.OPC while EthernetAVB is in RESET mode, it is possible to configure availability of gPTP support within CONFIG mode

To enable gPTP support in CONFIG mode use a 32 bit write access when setting CCC.OPC to B'01. This write should also set CCC.GAC to 1 and CCC.CSEL to intended configuration.

33A.3.1.4 Operating Mode Transitions Due to Hardware

The following hardware factors can also initiate transitions of the AVB-DMAC operating mode.

(1) Hardware reset

Resetting of the LSI chip leads to resetting of the entire EthernetAVB module. The operating mode shifts to reset mode.

(2) Transition during power-off by module standby

This transition is triggered by module standby of CPG during the power-off sequence.

The AVB-DMAC completes the bus master access in progress, and then shifts to reset mode. At this time, the operating mode configuration bits in the AVB-DMAC mode register (CCC.OPC) are set to B'00.

33A.3.2 Common Control for Transmission and Reception

33A.3.2.1 Initialization Procedure

Figure 33A.5 shows the overall initialization procedure in outline.

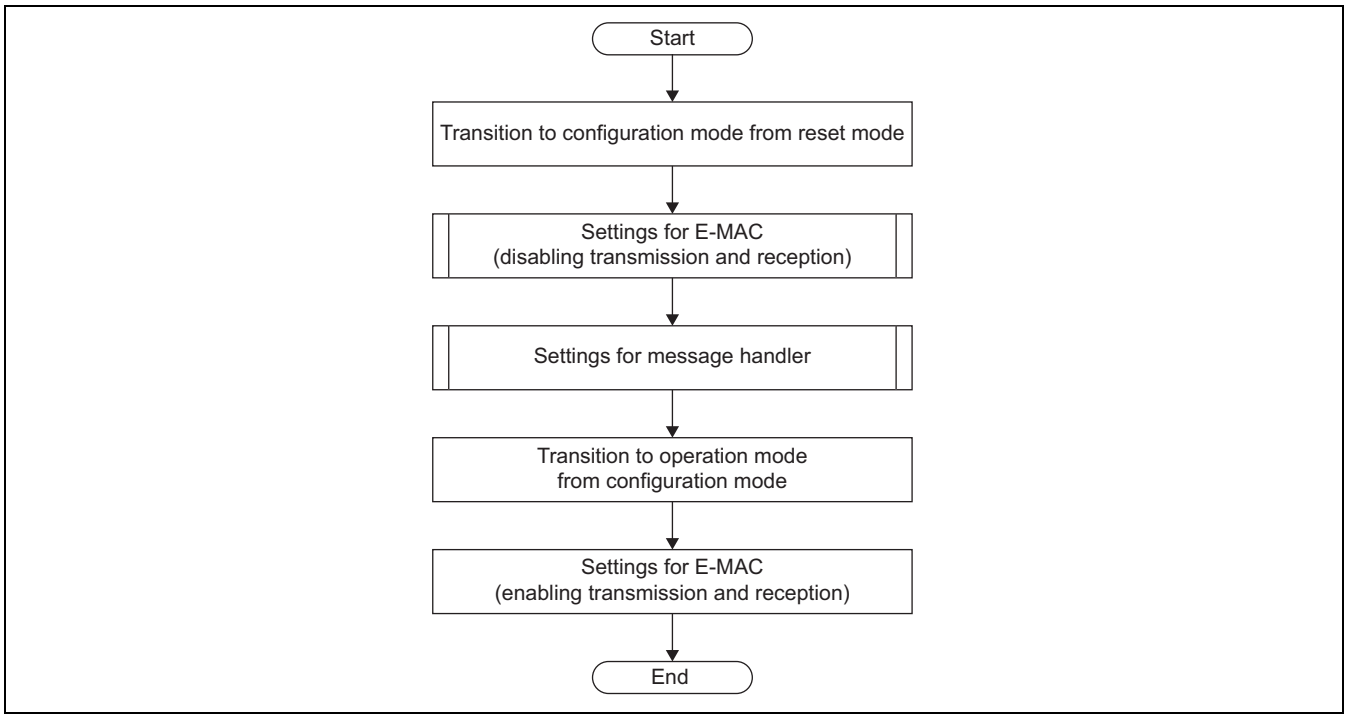


Figure 33A.5 Outline of the Initialization Procedure

(1) Initializing the Receiver Section

Before starting reception, follow the procedure below.

Keep the operating mode to configuration mode, and do not enable reception until the settings for the AVB-DMAC are completed.

- Set the operating mode to configuration mode.
- Set AVB filtering for network control frames and AVB stream frames to suit the specifications of the product the chip will be used in.
- Create a descriptor chain for each queue to be used.
- Set the base address for table address in the descriptor base address table register (DBAT).
- Specify the maximum frame length with the receive frame length upper limit register (RFLR).
- Specify whether padding is to be used with the receive padding configuration register (RPC).
- Set the unread frame counter for each queue with unread frame counter registers (UFCVs) 0 to 4.

(2) Initializing the Transmitter Section

Figure 33A.6 illustrates initialization of the transmitter section.

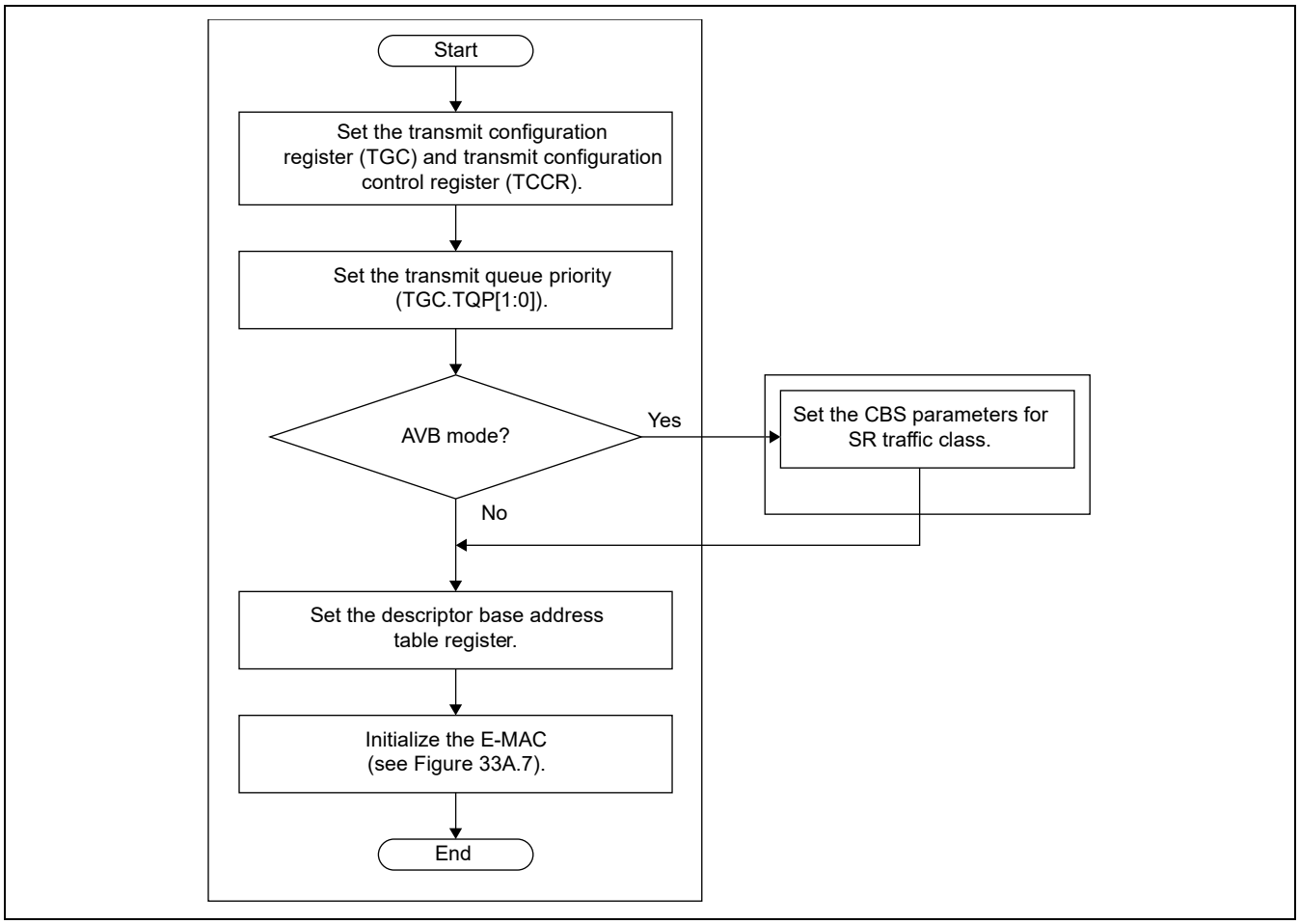


Figure 33A.6 Procedure for Initializing the Transmitter Section

(3) Initializing the E-MAC Section

Figure 33A.7 illustrates initialization of the E-MAC section.

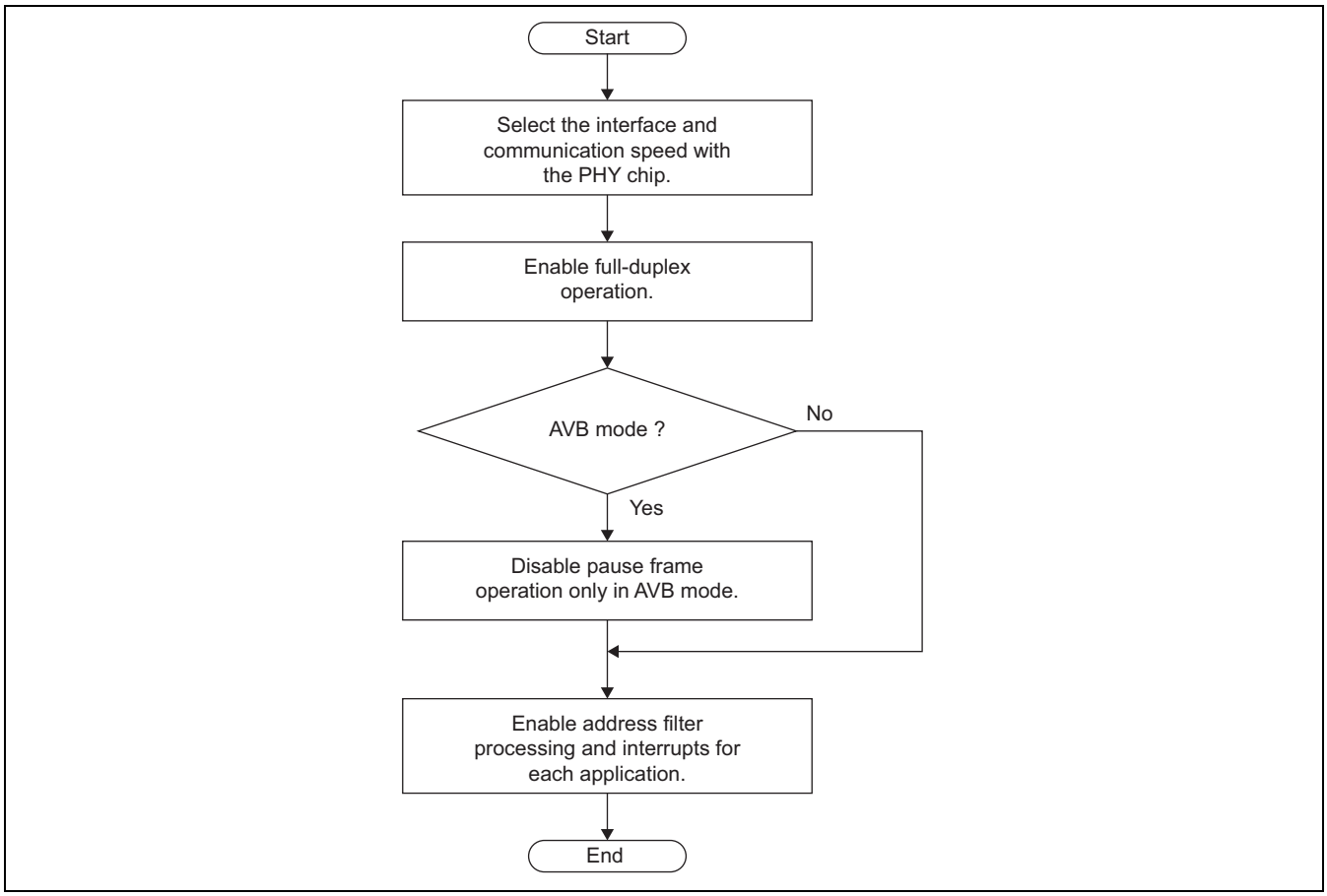


Figure 33A.7 Procedure for Initializing the E-MAC Section

(4) Initialization of the Application Unit

Figure 33A.8 illustrates initialization of the application unit.

For a description of how to set up the descriptors and the CBS traffic shaping parameters, see section 33A.3.3 Descriptors, and section 33A.3.6 CBS (Credit-Based Shaping).

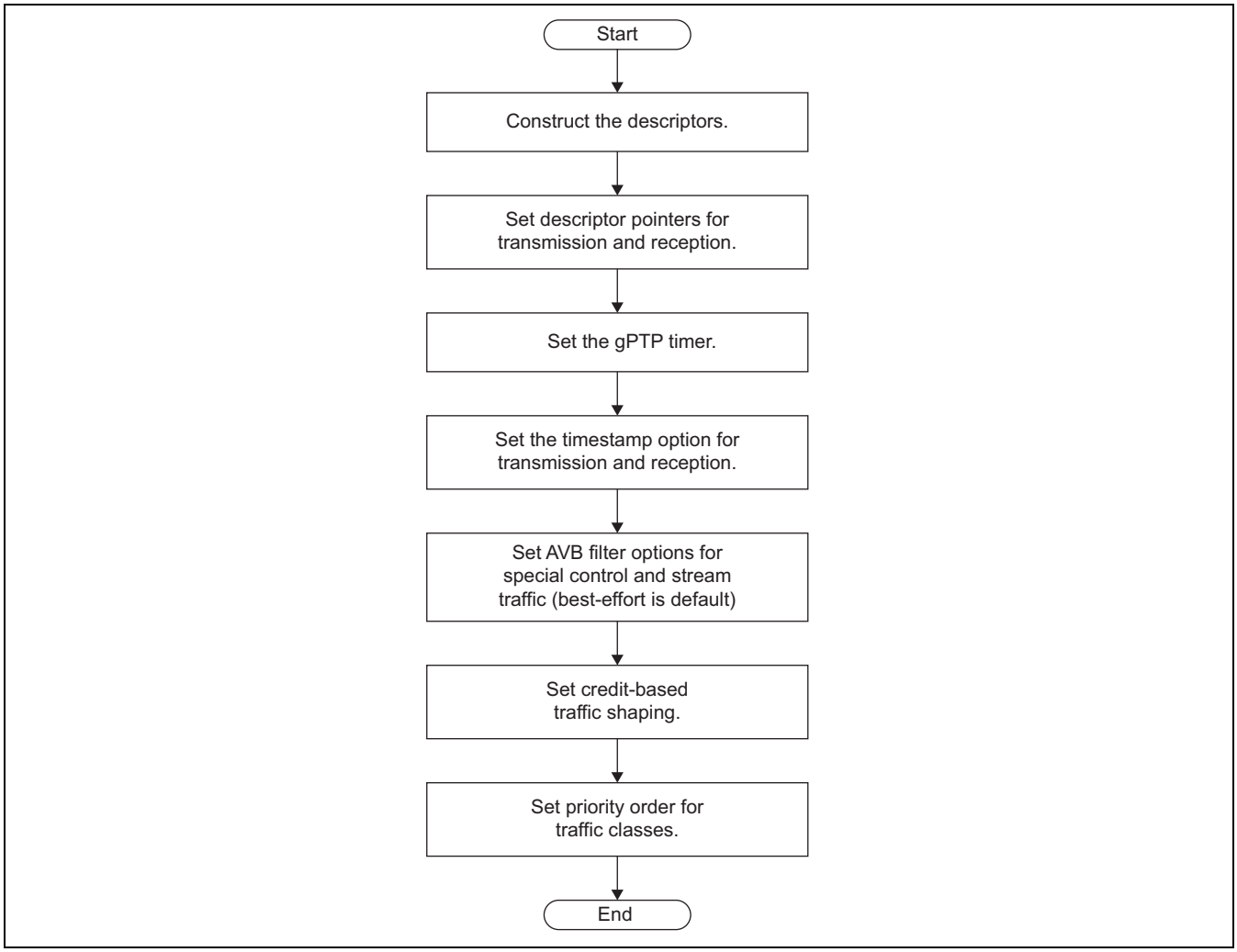


Figure 33A.8 Initializing the Sections for Use by the Application

(5) Relationship between Transmission Queue Numbers and Traffic Classes

In fetching, the relationships between the transmission queues and traffic classes are fixed, so the priority specified by the transmit queue priority bits in the transmit configuration register (TGC.TQP) has no effect.

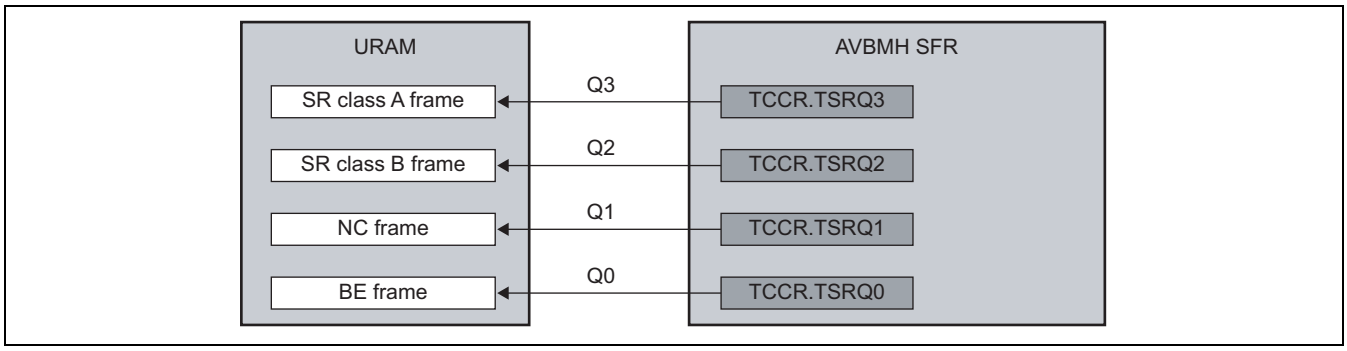


Figure 33A.9 Class Associations of Queues for the Scheduler

In fetching, the credit values for stream classes A and B are not taken into account. Behavior depends on the setting of the transfer FIFO size configuration bits in the transfer configuration registers (TGC.TBDt) and on the frame size that can be fetched to the transmission FIFO.

When the transmit queue priority bits in the transmit configuration register (TGC.TQP) are B'00 or B'01, the priority order is Q3 → Q 2 → Q1 → Q0.

When the transmit queue priority bits in the transmit configuration register (TGC.TQP) are B'11, the priority order is Q1 → Q3 → Q2 → Q0.

33A.3.2.2 Checking Integrity

The AVB-DMAC is capable of detecting and identifying errors produced in the processing of Ethernet frames and in the transfer of frame data for transmission and reception.

(1) Concept of Integrity Checking in Reception

The aim of integrity checking in reception is preventing the storage of error frames in the URAM. If an error frame is stored in the URAM, software can get information to identify the frame as an error frame.

Note: If a special descriptor chain is to be used for separation of received headers from the associated data, an error that breaks the sequence may lead to storage space for synchronization running out. In such cases, software interaction or re-synchronization via the EOS descriptor is required.

(2) Concept of Integrity Checking in Transmission

The purpose of integrity checking in transmission is to prevent the transmission of broken frames.

Since transmission of a frame by the E-MAC can neither be stopped nor disabled once it has started, this check involves intensive monitoring for problems that can arise during fetching.

(3) Items for Monitoring in Both Reception and Transmission

(a) Errors in access to the URAM for reading of descriptors

The same descriptor may be processed again because the current descriptor address (CDARq.CDA) was not changed. If this problem occurs in a divided frame, the sequence may be broken.

In reception

— The received frame will be lost.
— The same problem will occur for the next frame of data received for the same queue.

In transmission

— The transmit start request bit in the transmit configuration control register (TCCR.TSRQt) is set to 0.
— The frame will be lost from the transmission FIFO.

Errors in access to read descriptors from the URAM are detected from the response signal of the AXI-Bus. EthernetAVB flags only one access error per descriptor read.

(b) Illegal configuration of a descriptor by an application

The same descriptor may be processed again because the current descriptor address (CDARq.CDA) was not changed. If this problem occurs in a divided frame, the sequence may be broken.

In reception

— The received frame will be lost.
— The same problem will occur for the next frame of data received for the same queue.

In transmission

— The transmit start request bit in the transmit configuration control register (TCCR.TSRQt) is set to 0.
— The frame will be lost from the transmission FIFO.

(c) Errors in access to the URAM for writing of descriptors

As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start request bit in the transmit configuration control register (TCCR.TSRQt) are updated.

As DESCR.DT was not updated, hardware and software synchronization may have been destroyed.

Errors in access to write descriptors to the URAM are detected from the response signal of the AXI-Bus.

(4) Items for Monitoring in Reception

(a) Errors in access to the URAM for writing of data or time stamps

— As in the case where no error occurs, the current descriptor address (CDARq.CDA) is updated.
— DESCR.EI is set to indicate incorrect contents.
— This problem occurring in a divided frame may break the descriptor sequence, making the queue unusable.

Errors in access to write data or descriptors to the URAM are detected from the response signal of the AXI-Bus.

EthernetAVB flags each access error individually, even they are related to same frame.

(b) Error of the Reception FIFO

— Received frames are all invalidated.
— All frames stored as received frames are discarded. At this time, the number of frames and queue information cannot be captured.

If the reception FIFO RAM faults, AVB-DMAC detects the fault as error of the reception FIFO.

(c) Queue Synchronisation Fault of the Reception

EthernetAVB will not continue splitting frame across EOS descriptor. A queue synchronisation fault is detected when read descriptor with DESCR.DT = EOS at position where FMID, or FEND should be written

— RIS2.QFFr is set 1
— CDARq.CDA is updated as in fault free operation.
— Neither CIARr.CIA nor LIARr.LIA is changed.
— Neither UFCVi.CVr nor RIS0.FRFr is changed.
— Received frame is lost. There is an incomplete frame (no FEND) in descriptor chain.

Note: Reading descriptor may be one or more storage elements ahead in descriptor chain.

(5) Items for Monitoring in Transmission

(a) Errors in Access for Reading Data from the URAM

— Data that have already been fetched are discarded from the transmission FIFO.
— When an error of this type occurs during processing of an FSINGLE or FEND descriptor:
As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start bit in the transmit configuration control register (TCCR.TSRQt) are updated. Fetching resumes after the error frame.
— When an error of this type occurs during processing of an FSTART or FMID descriptor:
The current descriptor address (CDARq.CDA) is not updated.
The transmit start bit in the transmit configuration control register (TCCR.TSRQt) is set to 0.

Errors in access to read data from the URAM are detected from the response signal of the AXI-Bus.

(b) Overflow of the Transmission FIFO

— As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start bit in the transmit configuration control register (TCCR.TSRQt) are updated. Fetching resumes after the error frame.
— The frame will be discarded from the FIFO.

(c) Frame size error during transmission

— As in the case where no error occurs, the current descriptor address (CDARq.CDA) and the transmit start bit in the transmit configuration control register (TCCR.TSRQt) are updated. Fetching resumes after the error frame.

A transmit frame size error is detected when the size setting in one or more (in the case of a divided frame) descriptors for frame transmission is 1966 or more bytes. Such frames are cut out and transmitted.

(d) Damaged Data in the Transmission FIFO

— Fetching is not affected by damaged data.
— Since damaged data from the FIFO is only detected during frame transmission, an error frame may be transmitted.

If damaged data in the transmission FIFO is an error due to the transmission FIFO, this is detected by the AVB-DMAC.

(6) Items for Monitoring in gPTP

(a) Access error while reading AVTP timestamps from Tx-Buffer RAM

— AVTP timestamps are invalidated.
— gPTP unit ignores the issue. It uses the value as read for AVTP comparison.

An access error when reading timestamps from Tx-Buffer RAM is flagged to EthernetAVB by external RAM protection logic.

33A.3.3 Descriptors

33A.3.3.1 Data Representation in URAM

The AVB-DMAC transfers data for transmission and received data to and from the application software via the URAM.

The memory in the URAM for use by the AVB-DMAC is configured with control structures referred to as descriptors and associated areas to which the frame data are allocated. Dividing the memory into a control area and data area allows the flexible allocation of frame data to the URAM. This enables sharing of the areas to which frame data are allocated and the use of non-contiguous areas. Frame data can be copied without using the CPU. Arbitration that ensures hardware and software access to the memory area is also available without access to registers of the AVB-DMAC.

Figure 33A.10 shows an example of the memory maps for descriptors and the descriptor data area in the URAM.

A descriptor consists of its type (DESCR.DT), which controls the descriptor functions, a descriptor pointer (DESCR.DPTR) indicating the start address for storage of the frame data in the descriptor area, and the data size field (DESCR.DS), indicating the amount of frame data. Post-processing interrupt generation can be set up for each descriptor. Enabling and disabling of the interrupt is controlled by the descriptor interrupt enable bits (DESCR.DIE).

The descriptor may also hold information related to content. This information does not affect general descriptor functions. It provides information other than the frame data proper, such as on the state of reception.

For details, see section 33A.3.4.2 Setting Up Reception Descriptors, and section 33A.3.5.2 Setting Up Transmission Descriptors.

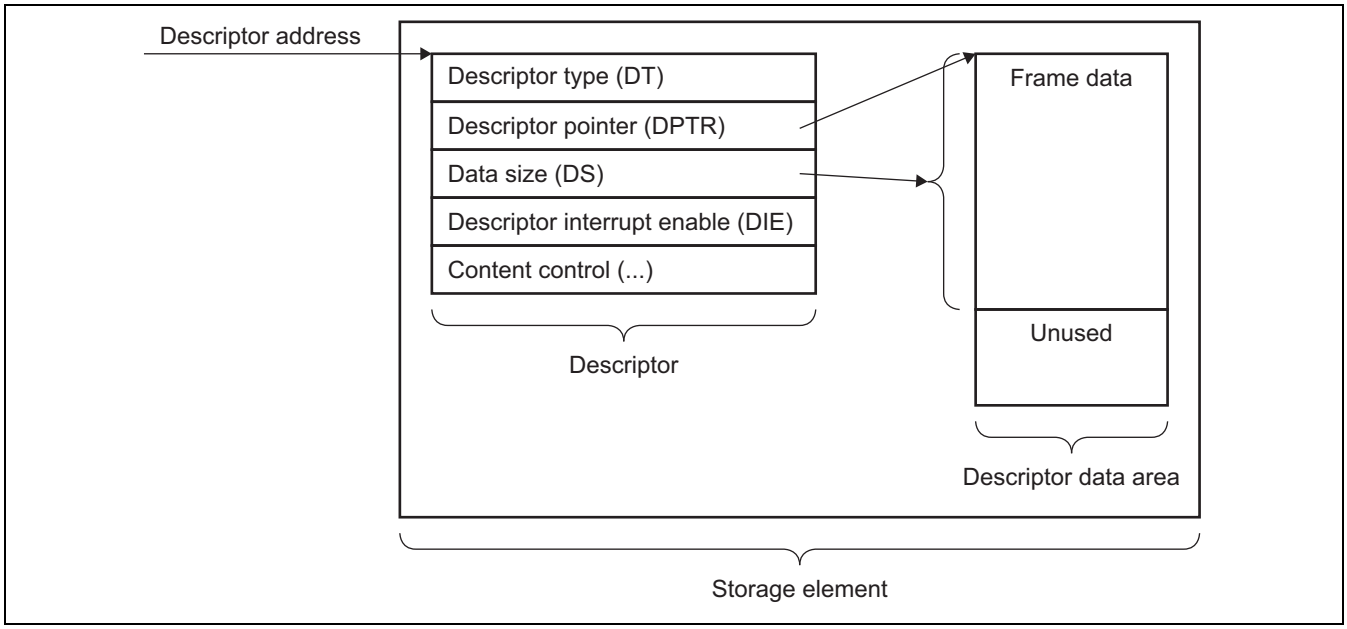


Figure 33A.10 Outline of Storage Element Used for Receive and Transmit Queues

The descriptor must be aligned with a 32-bit boundary in the URAM.

Descriptors are generally configured of 64 bits, but are configured of 160 bits when reception and storage of gPTP time stamps is enabled.

The amount of data in the frame is defined by the data size bits (DESCR.DS). In reception, these bits indicate the upper limit on the size of frames to be received. If the data size is not aligned with a 32-bit boundary, the bytes to the next 32-bit boundary in the data area will be an unused area.

33A.3.3.2 Using Descriptor Chains in Queues

Transmission and reception descriptors in the URAM are grouped into queues. Each queue handles frames so that they are transmitted in order of priority and received separately. A queue is capable of controlling one or more frames. Accordingly, multiple descriptors can be assigned to one queue. A combination of multiple descriptors is referred to as a descriptor chain.

For a descriptor chain, the three general descriptor types listed below are defined. For details on these descriptor types, see section 33A.3.3.6 Descriptor Type.

- Descriptors that define frame data
- Descriptors that control the descriptor chain itself (e.g. LINK, EOS).
- Descriptors that arbitrate access by hardware or software

Figure 33A.11 shows the two basic topologies for descriptor chains. In the simplified examples in the figure, all descriptors allocated to the chain are stored in the array.

- For a linear descriptor chain, the last descriptor in the array is a control descriptor indicating the end of the descriptors (e.g. EEMPTY).
- For a cyclic descriptor chain, the last descriptor in the array is a control descriptor that returns to the first descriptor in the array (e.g. LINK).

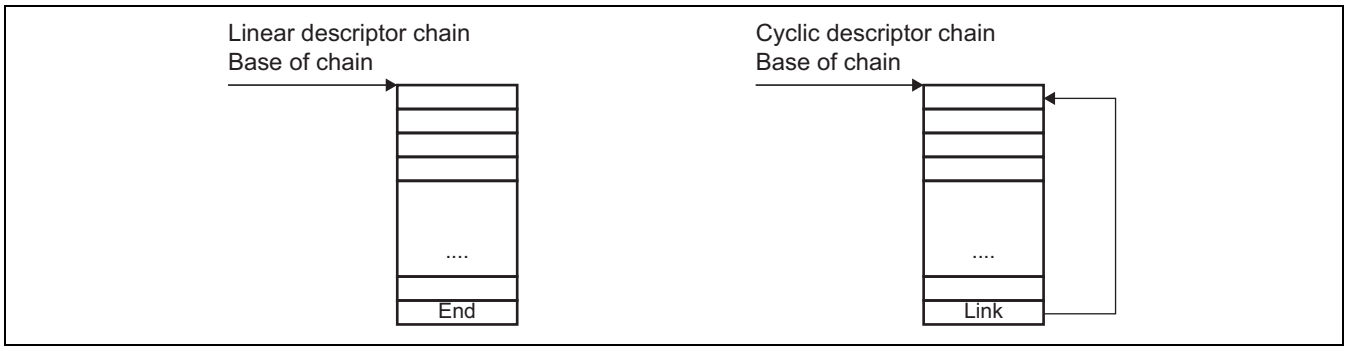


Figure 33A.11 Outline of the Basic Descriptor Chains

The relationship between queues and descriptor chains is defined by the base addresses of chains. A queue is connected to one descriptor chain over one round of processing. There is also a method of switching to a different chain while in operation mode.

There are no restrictions on the number of link descriptors and their locations within the chain. The last descriptor of a designed chain determines the topology.

Which chain structure is to be used or which topology is suitable depends on the application. A description of how to design descriptor chains to suit various applications is given in section 33A.3.4.2 Setting Up Reception Descriptors, and section 33A.3.5.2 Setting Up Transmission Descriptors.

33A.3.3.3 Descriptor Base Address Table

The base address table in the URAM contains the address of the first descriptor of all chains to be handled by the respective queues.

Entries 0 to 3 are used to access transmission queues 0 to 3. Subsequent entries are used to access reception queues. Entry 4 thus corresponds to reception queue 0.

The configuration of entries in the base address table is the same as the configuration of link descriptors. We recommend using the descriptor type (DESCR.DT) LINKFIX. Processing of this link descriptor does not change it, so it does not require updating. The first descriptor of a chain performs hardware and software synchronization. If the application requires hardware and software synchronization for the base addresses, use the descriptor type (DESCR.DT) LINK.

The CPU is only capable of using LINKFIX and LINK as descriptor types (DESCR.DT) of descriptors in the base address table.

Set the location of the base address table in the URAM in the descriptor base address table register (DBAT).

Figure 33A.12 shows an example of a base address table for controlling four transmission and three reception queues. The boxes to the right of the table represent descriptor chains with the desired topologies.

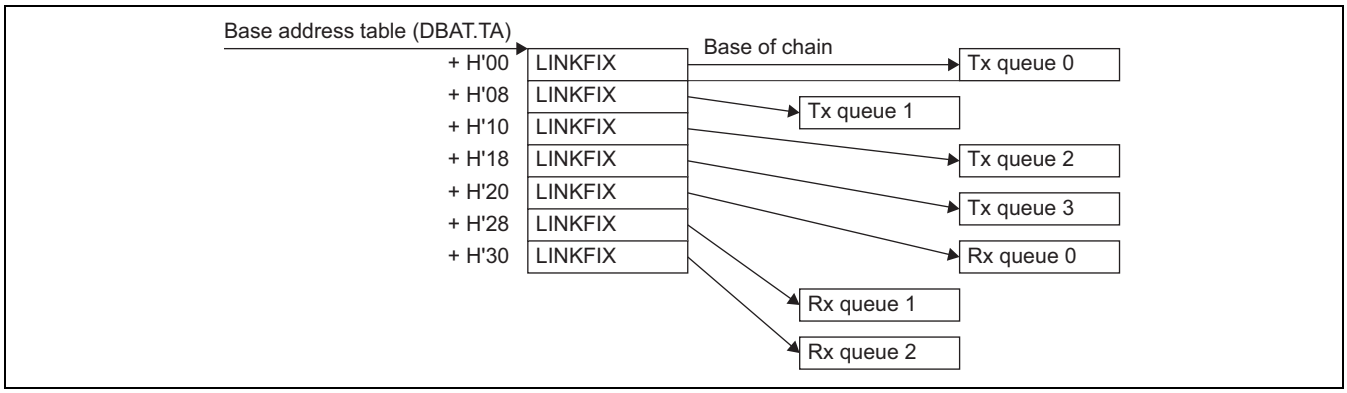


Figure 33A.12 Example of a Base Address Table for Reception and Transmission Queues

Note: The size of the descriptors in the base address table is always eight bytes even if the queue itself includes extended descriptors.

33A.3.3.4 Descriptor Chain Processing

The descriptor that is currently processed or will be processed when the related queue gets active is the current descriptor. The current descriptor address for use by a queue q can be checked in the current descriptor address register q (CDARq).

Current descriptors are stored in registers or in descriptors as described below in the given situations.

- In the descriptor base address table registers for all q queues (DBAT) (DBAT.TA+8*q) when the operating mode shifts to operation mode.
- In the descriptor base address table register (DBAT) (DBAT.TA+8*q) when a base address load request is issued for a queue q by setting the corresponding bit (DLR.LBAq) in the descriptor base address load request register (DLR).
- In DESCR.DPTR for a link descriptor (LINK, LINKFIX) to be processed.
- After a descriptor has been processed, the current descriptor for the same queue is incremented by the size of the descriptors being handled by the queue (8 bytes for normal descriptors and 20 bytes for extended descriptors). The AVB-DMAC updates the descriptor type and informs the CPU that the descriptor has been processed.

33A.3.3.5 Descriptor Interrupts

A descriptor is able to issue a descriptor interrupt on completion of its processing. The setting of the descriptor interrupt enable bits (DESCR.DIE) in each descriptor selects disabling or generation of the descriptor interrupt.

EthernetAVB provides two kinds of descriptor interrupts:

- Queue specific descriptor interrupt (1 per receive/transmit queue)
- Universal descriptor interrupt (15 shared between all receive/transmit queues)

The descriptor interrupt is a common resource that is shared between reception and transmission queues. Software control of the descriptor interrupt provides a flexible method of application-specific flag processing.

Figure 33A.13 illustrates the way in which the AVB-DMAC generates descriptor interrupts (or sets bits in the descriptor interrupt status register (DIS.DPFi)). Processing of a descriptor with the value i in the descriptor interrupt enable bits (DESCR.DIE) leads to the corresponding bit in the descriptor interrupt status register (DIS.DPFi) being set.

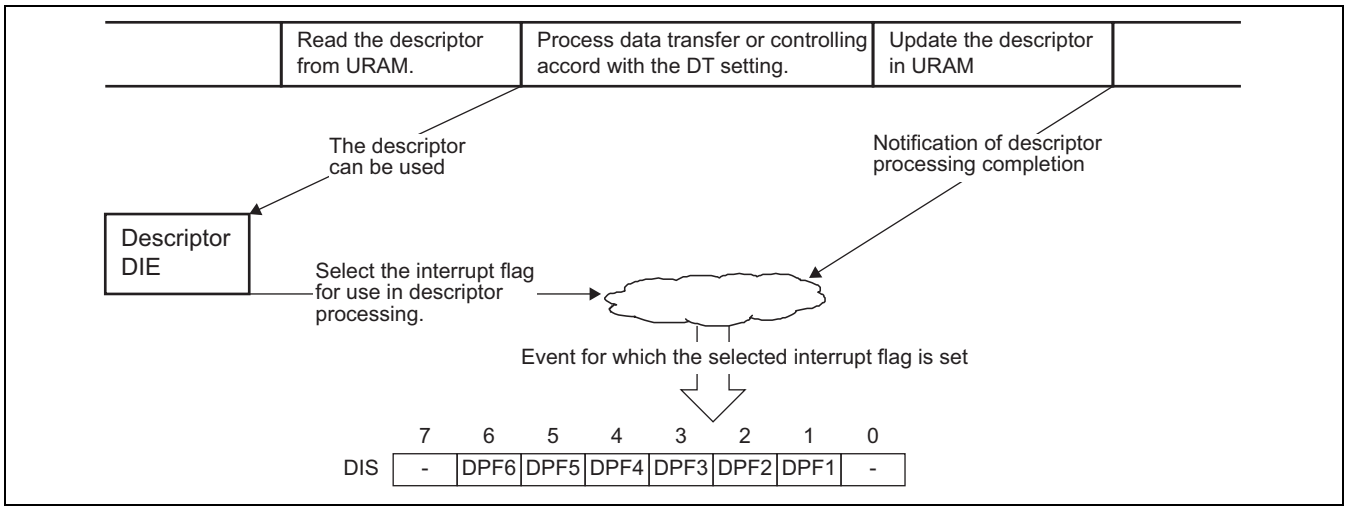


Figure 33A.13 Method of Descriptor Interrupt Generation

33A.3.3.6 Descriptor Type

The descriptor types (indicated by the DESCR.DT bits) supported by the AVB-DMAC fall into the following three categories.

- Definitions of frame data
- Control of descriptor chains
- Hardware and software arbitration

Table 33A.6 is a summary of the descriptor types available for the AVB-DMAC. Entries under “Name” are the names of the descriptor types and the values under “DT” are the corresponding values to be set in the descriptor type field (DESCR.DT). A given descriptor may be handled differently according to whether it is in a transmission or reception queue, so the transmission and reception columns list the scopes of control and processing of the descriptor types.

The abbreviations defined below are used in the transmission and reception columns.

Definition of SW:

— The descriptor is processed by software.
— Software has access to and may modify the descriptor and descriptor data area.
— This descriptor cannot be changed by hardware (AVB-DMAC).

Definition of HW:

— The descriptor is processed by hardware (AVB-DMAC).
— Software must modify neither the descriptor nor the descriptor data area.
— Hardware (AVB-DMAC) processes this descriptor and subsequently changes the descriptor type.

Invalid:

This descriptor type is not used in transfer in the given direction (transmission or reception).

Do not write this value to the descriptor type (DESCR.DT) field for transfer in the given direction.

Hardware does not process these descriptor types in the cases listed as invalid. The current descriptor address (CDARq.CDA) will not be changed when processing of a queue for the given direction arrives at a descriptor with this type setting.

Table 33A.6 Summary of Descriptor Types

Name	DT	Description	Reception	Transmission
Frame data				
FSTART	5	Frame Start The descriptor points to valid data for a frame. The frame starts with the given data and continues with that indicated by the next descriptor.	SW	HW
FMID	4	Frame Middle The descriptor points to valid data for a frame. The frame started with a previous descriptor and continues to the data indicated by the next descriptor.	SW	HW
FEND	6	Frame End The descriptor points to valid data for a frame. The frame continues from the previous descriptor and ends with the data indicated by in this descriptor.	SW	HW
FSINGLE	7	Frame Single The descriptor points to valid data for a complete frame.	SW	HW
Chain control				
LINK	8	Link Defines the next descriptor in the chain.	HW	HW
LINKFIX	9	Fixed Link Same as LINK, but not changed by AVB-DMAC after processing.	SW	SW
EOS	10	End Of Set Control element to split a descriptor chain. The chain stops and waits for user interaction.	HW	HW
HW/SW arbitration				
FEMPTY	12	Frame Empty A descriptor related to frame data but not containing valid data for a frame	HW	SW
FEMPTY_IS	13	Frame Empty Incremental Start A descriptor related to frame data but not containing valid data for a frame. DESCR.DPTR sets the base address of an “incremental data area” in the URAM.	HW	Invalid
FEMPTY_IC	14	Frame Empty Incremental Continue A descriptor related to frame data but not containing valid data for a frame. Data is stored to the incremental data area in the URAM.	HW	Invalid
FEMPTY_ND	15	Frame Empty No Data storage A descriptor related to frame data but not containing valid data for a frame. The descriptor is processed in the same way as FEMPTY but data are not stored in the URAM.	HW	Invalid
LEMPTY	2	Link Empty A link descriptor for processing by the AVB-DMAC	SW	SW
EEMPTY	3	EOS Empty An EOS descriptor for processing by the AVB-DMAC	SW	SW
DT0	0	Reserved	Invalid	Invalid
DT1	1	Reserved	Invalid	Invalid
DT11	11	Reserved	Invalid	Invalid

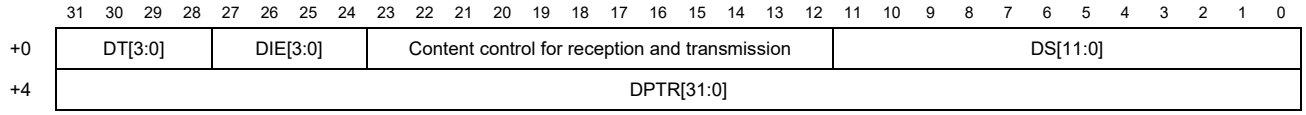
33A.3.3.7 Layout of General Descriptors in the URAM

The AVB-DMAC updates processed descriptors in the URAM. The field to be changed in the descriptor being updated depends upon whether the direction is transmission or reception and the queue mode. Other fields will not be changed. There are no restrictions on the values set in unused descriptor fields (indicated by "—" in the figure).

(1) Frame Data Descriptors

The allocation of bits in the frame data descriptors (FSTART, FMID, FEND, and FSINGLE) is shown below.

- Normal descriptor (usable in both reception and transmission)



- Extended descriptor (usable only in reception)

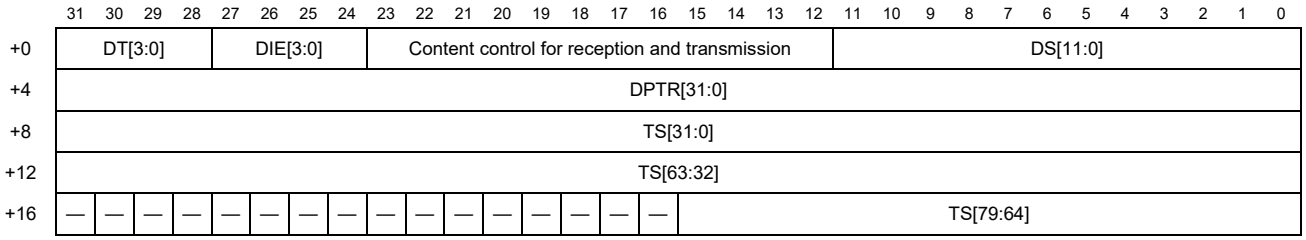


Table 33A.7 Contents of Frame Data Descriptors (DESCR)

Bit Name	Function
DT[3:0]	Descriptor Type 5: FSTART 4: FMID 6: FEND 7: FSINGLE For details, see section 33A.3.4.2, Setting Up Reception Descriptors, and section 33A.3.5.2, Setting Up Transmission Descriptors.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).
—	Content Control For details, see section 33A.3.4.2, Setting Up Reception Descriptors, and section 33A.3.5.2, Setting Up Transmission Descriptors.
DS[11:0]	Data Size Size of the data area/frame data for the descriptor (in bytes)
DPTR[31:0]	Descriptor Pointer Pointer to the data area for the descriptor
TS[79:0]	Time Stamp Time stamp of the received frame (only available in extended descriptors)

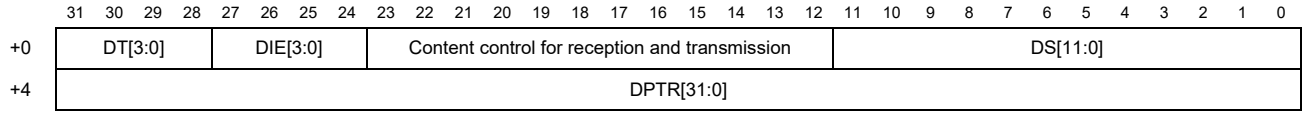
Note: Register an address aligned with a 32-bit boundary as the descriptor pointer (DESCR.DPTR).
Some bits in extended descriptors are reserved (The reserved bits (above DESCR.TS[79:64]) in an extended descriptor are set to H'0000 after the time stamp is stored).

(2) Hardware/Software Arbitration Descriptors (Only for Reception)

The allocation of bits in the descriptors for hardware/software arbitration (FEMPTY, FEMPTY_IS, FEMPTY_IC, and FEMPTY_ND) is shown below.

The allocation of bits in the arbitration descriptors for use in reception is the same as in frame data descriptors.

- Normal descriptor



- Extended descriptor (usable only in reception)

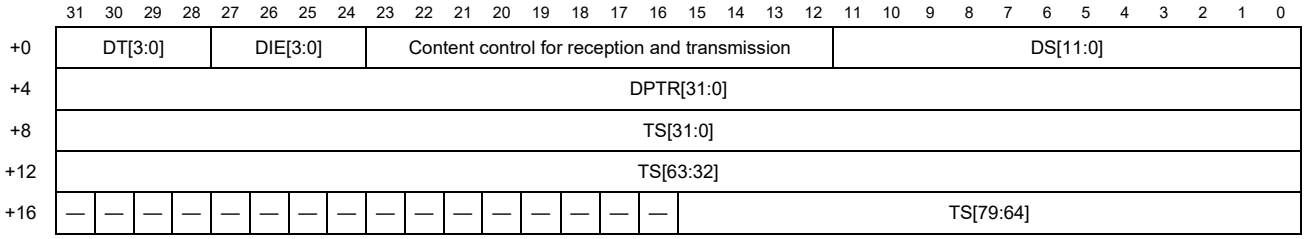


Table 33A.8 Contents of Hardware/Software Arbitration Descriptors (DESCR)

Bit Name	Function
DT[3:0]	Descriptor Type 12: FEMPTY 13: FEMPTY_IS 14: FEMPTY_IC 15: FEMPTY_ND For details, see Table 33A.6 Summary of Descriptor Types.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).
—	Content Control For details, see section 33A.3.4.2, Setting Up Reception Descriptors, and section 33A.3.5.2, Setting Up Transmission Descriptors.
DS[11:0]	Data Size Size of the data area/frame data for the descriptor (in bytes)
DPTR[31:0]	Descriptor Pointer Pointer to the data area for the descriptor
TS[79:0]	Time Stamp Time stamp of the received frame (only available in extended descriptors)

Note: Register an address aligned with a 32-bit boundary as the descriptor pointer (DESCR.DPTR).
When the descriptor is an extended descriptor, it has a 12-byte unused area.

In an FEMPTY descriptor, the descriptor type (DT), descriptor interrupt enable (DIE), data size (DS), and descriptor pointer (DPTR) fields are used.

In an FEMPTY_IS descriptor, the descriptor type (DT), descriptor interrupt enable (DIE), and descriptor pointer (DPTR) fields are used.

In an FEMPTY_IC descriptor, the descriptor type (DT) and descriptor interrupt enable (DIE) are used.

In an FEMPTY_ND descriptor, the descriptor type (DT), descriptor interrupt enable (DIE), and data size (DS) are used.

(3) Link Descriptors

The allocation of bits in the link descriptors (LINK and LINKFIX) is shown below.

- Normal descriptor

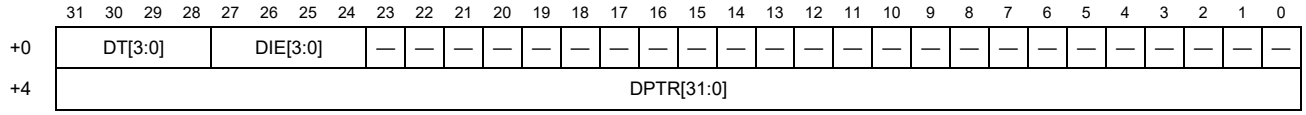


Table 33A.9 Contents of Link Descriptors (DESCR)

Bit Name	Function
DT[3:0]	Descriptor Type 8: LINK 9: LINKFIX For details, see Table 33A.6 Summary of Descriptor Types.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).
DPTR[31:0]	Descriptor Pointer Pointer to the data area for the descriptor Register an address on a 32-bit boundary.

Note: Register an address aligned with a 32-bit boundary as the descriptor pointer (DESCR.DPTR).

(4) Other Descriptors

The allocation of bits in the other descriptors (EOS, FEMPTY (only for transmission), LEMPTY, and EEMPTY) is shown below.

	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
+0	DT[3:0]				DIE[3:0]				—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
+4	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—

Table 33A.10 Contents of Other Descriptors (DESCR)

Bit Name	Function
DT[3:0]	Descriptor Type 10: EOS 12: FEMPTY (only for transmission) 2: LEMPTY 3: EEMPTY For details, see Table 33A.6 Summary of Descriptor Types.
DIE[3:0]	Descriptor Interrupt Enable B'0000: Descriptor interrupt is disabled. B'0001 to B'1111: The corresponding descriptor interrupt is generated (DIS.DPFi).

33A.3.3.8 How to Use Frame Data Descriptors

The descriptor data area size field (DESCR.DS) can specify up to 2048 bytes of Ethernet frame data per data area. Settings higher than 2048 (bytes) cannot be made.

In general, Ethernet frames are not of uniform length. The AVB-DMAC is capable of dividing frame data into multiple descriptors in order to minimize the memory capacity for frame data. This function allows processing of frames that are longer than the limit for descriptor data areas. Division can also be applied to frames on the basis of their data structures.

To handle frames and descriptors, four descriptor types (DESCR.DT) as FSTART, FEND, FMID and FSINGLE are defined.

Figure 33A.14 shows the mapping of frame data by frame data descriptors. The descriptor data areas are allocated to the URAM. For frames that require division into four or more data areas, additional FMID descriptors can be added as required.

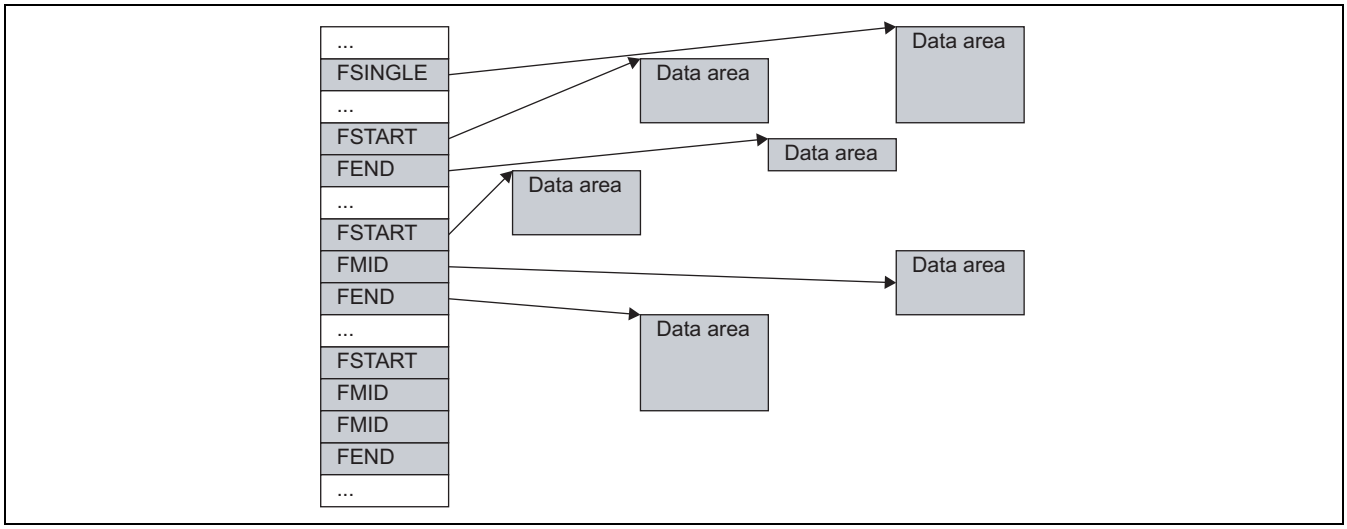


Figure 33A.14 Mapping of Frame Data

For reception, set the descriptor data areas to the maximum size (i.e. give DESCR.DS its maximum value). The AVB-DMAC will store received frame data in the given area. If a received frame has more data than the maximum size, the AVB-DMAC will divide the data up.

For transmission, set the descriptor data area size field to the actual data size. The AVB-DMAC modifies the descriptor type (DESCR.DT) to FEMPTY after processing the relevant descriptor. The data size (DESCR.DS) and descriptor pointer (DESCR.PTR) fields retain their settings.

A descriptor data area including unused space produces an empty space between data areas. In reception, an “incremental data area” can be used to prevent empty spaces. For incremental data areas, see section 33A.3.4.3(2) Incremental Data Areas.

As well as reducing the memory capacity taken up by the descriptor area in the URAM, division into frames can be used to identify different sections of data (e.g. for separating a header and data).

33A.3.3.9 How to Use Chain Control Descriptors

(a) Link Descriptors

The link descriptors can be used to set up cyclic descriptor chains (for details, see section 33A.3.3.2 Using Descriptor Chains in Queues)

After a LINK descriptor is processed, its descriptor type (DESCR.DT) is changed to LEMPTY. The descriptor pointer (DESCR.PTR) retains its setting.

After processing of a LINKFIX descriptor, the descriptor type (DESCR.DT) is not updated. Software can change the descriptor type (DESCR.DT), descriptor interrupt enable (DESCR.DIE), and descriptor pointer (DESCR.DPTR). However, DESCR.DT should not be modified by software. Take care to check the current descriptor address register (CDARq.CDA) before changing the descriptor pointer (DESCR.DPTR).

(b) EOS Descriptor

Use the EOS descriptor to divide a descriptor chain into various segments. The queue can continue even after an EOS descriptor.

In transmission, the response to an EOS descriptor is clearing of the transmit start request bit in the transmit configuration control register (TCCR.TSRQq) to 0.

In reception, the response is generation of a receive queue full interrupt (RIS2.QFFr), although if the frame currently being received is being divided for storage (received data such as those where some storage is in FMID- or FEND-type frames), the data are not completely stored.

33A.3.3.10 How to Use Hardware and Software Arbitration Descriptors

In hardware processing of descriptors, the empty descriptor types (FEMPTY, LEMPTY, and EEMPTY) are used to distinguish various descriptors. For software, they can be used to initiate checking for empty spaces, etc.

(a) FEMPTY, FEMPTY_IS, FEMPTY_IC, and FEMPTY_ND

These descriptor types (DESCR.DT) are used for descriptors that do not contain effective data. Of these, only FEMPTY is used in transmission. The descriptor pointer of a FEMPTYxxx descriptor refers to a descriptor data area.

(b) LEMPTY

This descriptor type (DESCR.DT) is assigned to LINK descriptors after they have been processed. The descriptor pointer (DESCR.DPTR) of an LEMPTY descriptor still points to the linked descriptor.

(c) EEMPTY

This descriptor type (DESCR.DT) is assigned to EOS descriptors after they have been processed. The descriptor pointer (DESCR.DPTR) of an EEMPTY descriptor is not used.

33A.3.3.11 Synchronization between Descriptor Access by Hardware and Software

The allocation of descriptor types (DESCR.DT) to the URAM can be used to set up the primary synchronization between hardware and software. By this, the number of CPU accesses to registers of EthernetAVB can be minimized and performance can be increased.

Basic concepts of synchronization:

- Each descriptor type in the set is exclusively for processing by hardware or software, depending on the direction of transfer (see Table 33A.6 Summary of Descriptor Types).
- Software must not change a descriptor assigned to hardware processing (the hardware does not change descriptors assigned to software processing).

In the case of software processing, the software must process the information in the descriptor and the corresponding frame data before changing the descriptor type. If a descriptor type for hardware is set in DESCR.DT, the software should not change any part of the descriptor or of the corresponding frame data.

33A.3.3.12 Tips for Optimizing Performance in Handling Descriptors

The following items are recommended as ways to ensure the optimal use of data structures in the URAM.

They are not requirements, but using a different approach may increase the load on the system bus within the LSI chip.

- Register descriptors with 64-bit alignment (this does not apply to extended descriptors).
- While in operation mode, use LINKFIX instead of LINK whenever a descriptor need not be changed. Hardware modifies the descriptor type (DESCR.DT) fields of LINK descriptors.
- Frame data is accessed in blocks up to 128 bytes.
- The number of 128 byte borders (addresses H'x xx00 and H'x xx80) and frame data inside should be minimized.
- Design the descriptor chains in ways that minimize parallelism of processing. This helps in dividing the chains into segments allocated to different cache pages, and in arranging the different segments exclusively for access by software or hardware.
- Minimize the number of divided frames. This can reduce the overhead of descriptor handling.

33A.3.4 Control in Reception

The point of the AVB-DMAC is to transfer data between the E-MAC and URAM without intervention by the CPU.

AVB-DMAC needs descriptors that define the amounts of frame data to be stored and the locations. After the E-MAC receives a frame, it stores the received frame data and the conditions of reception as the E-MAC state. If the descriptor is extended, the time stamp is also stored. For a description of how to set up descriptors for use in reception, see section 33A.3.4.2 Setting Up Reception Descriptors.

The AVB-DMAC filters received frames to separate them into various classifications (separation filtering). More specifically, this is done to separate received frames into the various reception queues and to set the priorities of different classes of received frames. For more on separation filtering, see section 33A.3.4.1(1) Separation Filtering.

Figure 33A.15 shows the reception data bus and the selection of queues for use in reception.

Each frame received from the E-MAC is stored in the reception FIFO; in parallel with this, the frame is analyzed to identify its type and the target queue number. After the E-MAC completes reception, the target queue number is generated and stored in the reception FIFO. Appending of a reception flag depends on the storage of one frame among the reception queues in the URAM, and the unread frame counter (UFC) is also associated with frame storage.

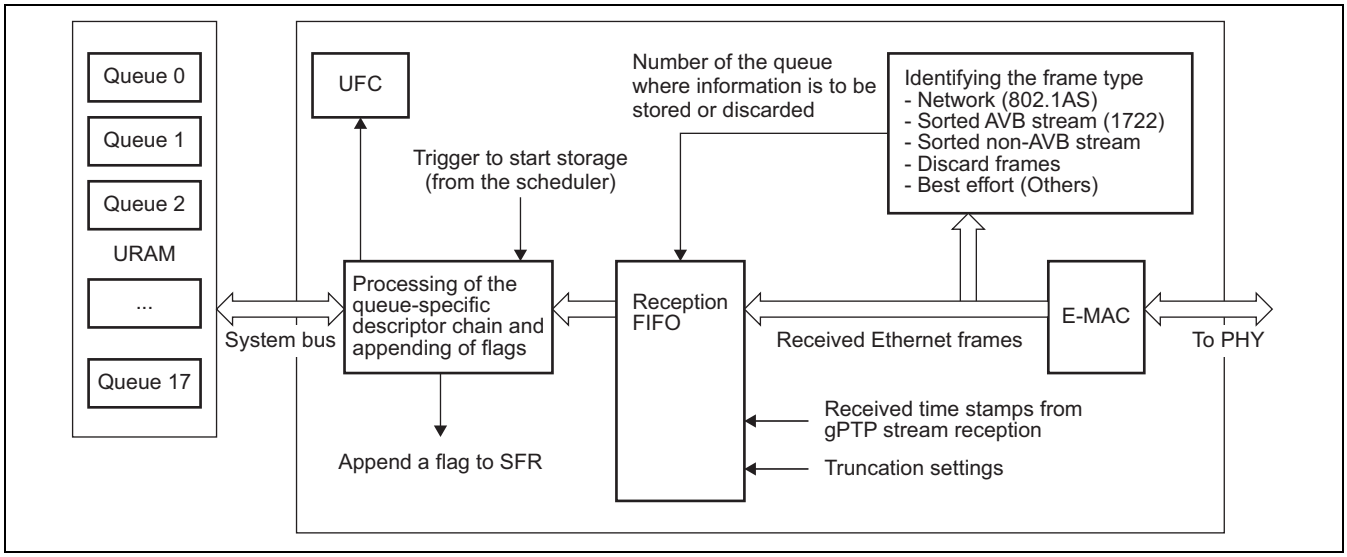


Figure 33A.15 Mechanism of General Reception Queue Selection

33A.3.4.1 Reception Queues

The AVB-DMAC applies its separation filtering mechanism to select the reception queue for storing a received frame. The AVB-DMAC stores all received frames in the URAM.

There are two conditions for the AVB-DMAC to discard a received frame.

- Detection of an error during reception by the E-MAC
  - Whether error frames are discarded or stored in reception queue 0 (best effort) depends on the setting of the error frame enable bit in the receive configuration register (RCR.EFFS). If error frames are to be stored (RCR.EFFS = 1), they are always stored in queue 0 (best effort). In this case, characteristics specific to the queue (e.g. truncation) will vary. If the storage of time stamps for reception queue 0 (best effort) is enabled (the time stamp enable bit in the receive configuration register RCR.ETS0 = 1), time stamps are stored even for error frames.
- Frame fails the separation filter
  - It depends on RCR.ESF if such frame is discarded or stored in receive queue 0 (best effort).

The flowchart in Figure 33A.16 shows how the AVB-DMAC selects the reception queue in accord with the frame type, including judgment by the separation filter. Selection of the queue starts when the E-MAC completes frame reception. The result is storage of the frame in the proper queue or the frame being discarded.

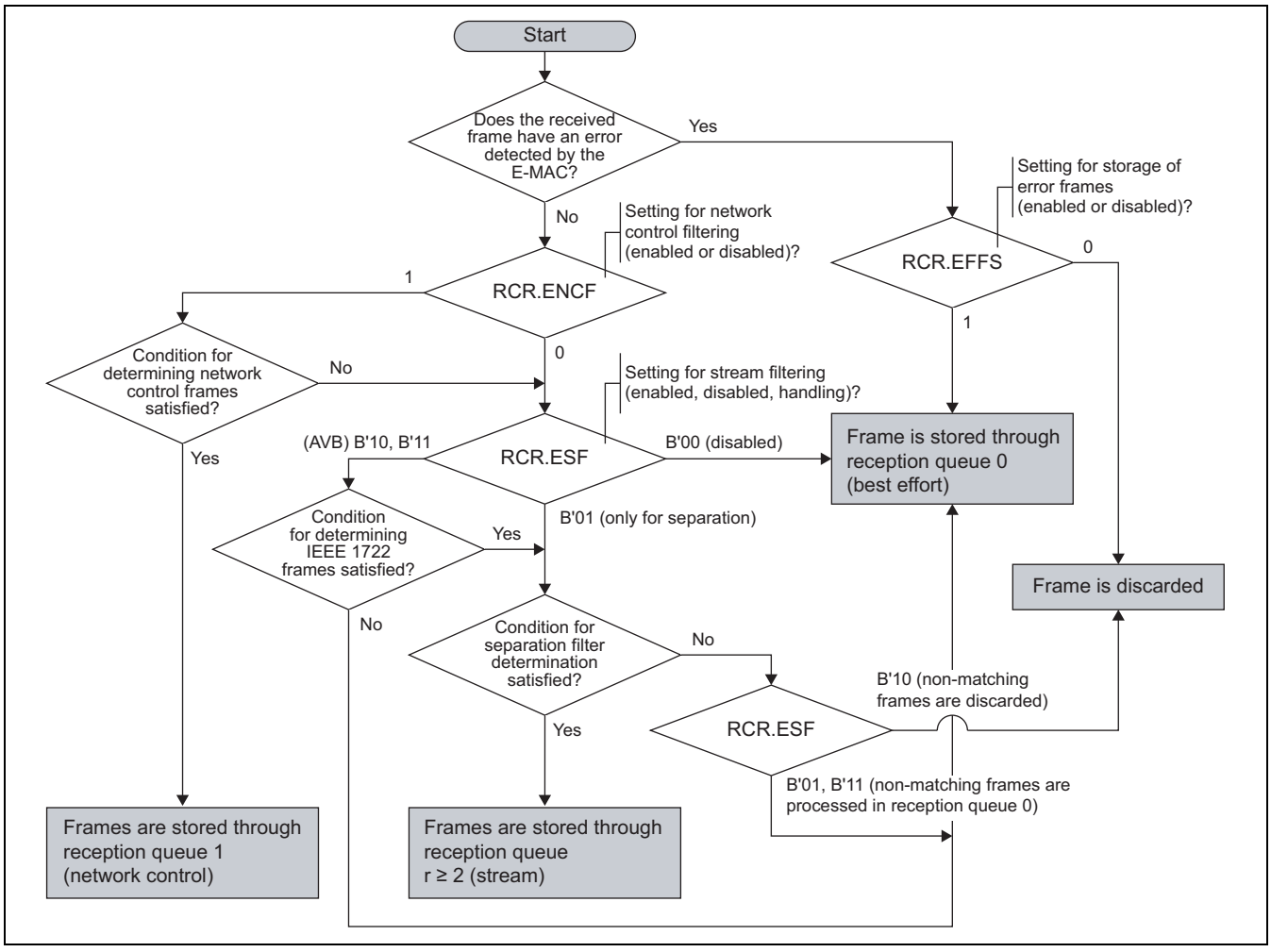


Figure 33A.16 Mechanism of Reception Queue Selection

Notes on the meanings of entries in the flowchart

- “Condition for determining network control frames”

The Ethernet destination address (DA) is 01:80:C2:00:00:0E.
The Ethernet type (ET) is 88:F7.

- “Condition for determining IEEE 1722 frames”

  The Ethernet destination address (DA) is within the range from 91:E0:F0:00:00:00 to 91:E0:F0:00:FE:FF.
  The VLAN tagged TPID (tag protocol identifier) field (VL) is 81:00.
  The Ethernet type (ET) is 22:F0.

- “Condition for separation filter determination”

  See section 33A.3.4.1(1) Separation Filtering.

Figure 33A.17 shows the allocation of bits related to the network and stream types in Ethernet frames. The preambles of Ethernet frames are not taken into account.

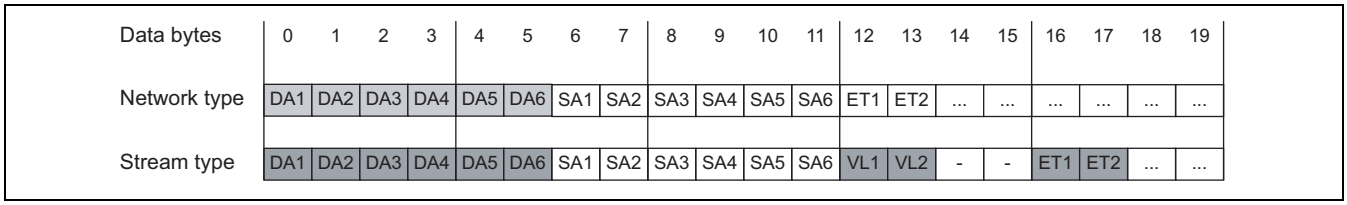


Figure 33A.17 Data Bytes of Ethernet Frames Used in Classification

(1) Separation Filtering

Separation filtering involves the checking of up to 64 bits (eight successive bytes) in received Ethernet frames. The setting for the first byte (i.e. the setting of the separation filter offset configuration register (SFO.FBP)), selects the part of frames to be used in separation filtering. There is also a common filter mask (set in the separation filter mask configuration register (SFMi.CFM)) that can be freely set to reduce the number of bytes used in separation filtering or to mask particular bits.

Examples

To use one byte in separation, set separation filter mask configuration register 0 (SFM0.CFM) to H'0000 00FF and separation filter mask configuration register 1 (SFM1.CFM) to H'0000 0000.

To use seven bytes in separation, set separation filter mask configuration register 0 (SFM0.CFM) to H'FFFF FFFF and separation filter mask configuration register 1 (SFM1.CFM) to H'00FF FFFF.

Note: If bits at some positions are set to 0 in the separation mask, in order to match with the pattern, the bits at the corresponding positions of the pattern must also be set to 0. Only those bits in which the separation filter pattern configuration register (SFPi.FPs) setting is equal to the separation filter mask configuration register (SFMi.CFM) are sorted by matching with received data.

Figure 33A.18 shows separation filtering. The selected data from a received frame (Rx_Frame[63:0]) are masked by the common filter mask. As a result, the selected frame data can be obtained. This value is compared with all filter patterns. The separation filter circuit in the AVB-DMAC selects the filter pattern that matches the queue having the lowest index s or selects a flag to indicate that there is no matching separation pattern.

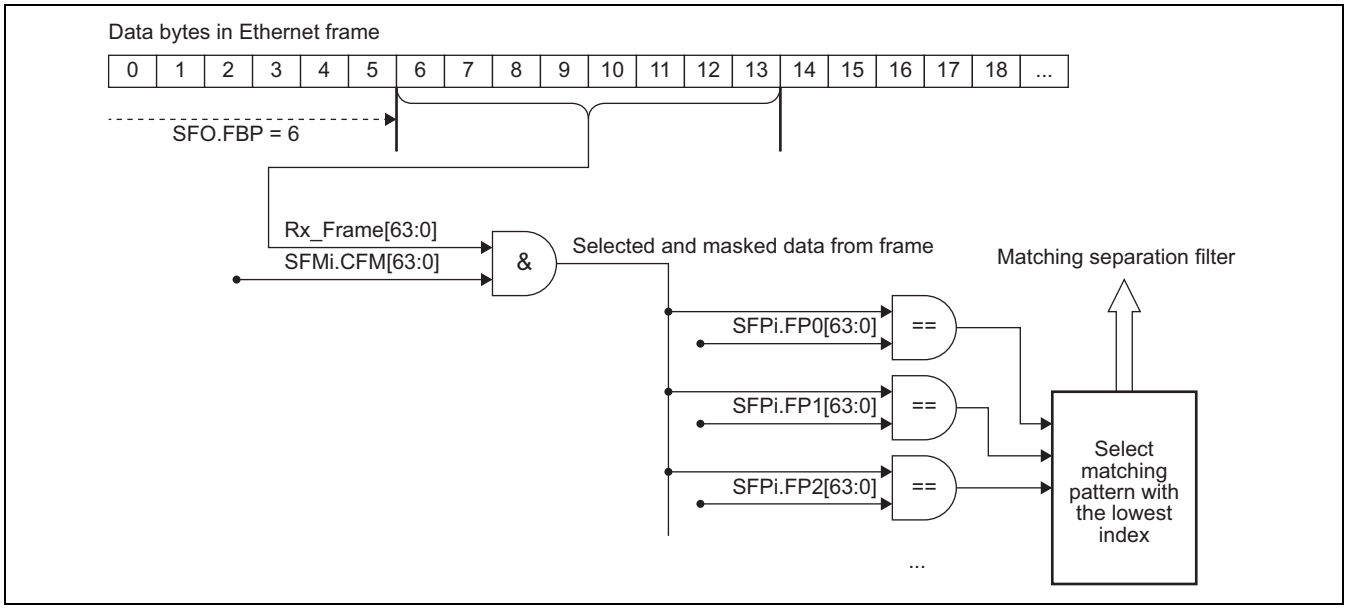


Figure 33A.18 Separation Filtering

(2) Separating Streams

The AVB-DMAC applies separation filtering to sort frames received in streams. An AVB network has a concept of “Talker” and “Listener”. A Talker is an end station that generates one or more streams. A Listener is an end station that has the role of being a sink for at least one stream. The various A/V streams are identified by 8-byte stream IDs.

The number of end stations within an AVB network and their roles differ with the application.

The stream ID is a general pattern of the AVB network for identifying one stream. Figure 33A.19 shows the bit allocation of bits in IEEE1722 Ethernet frames and stream ID fields.

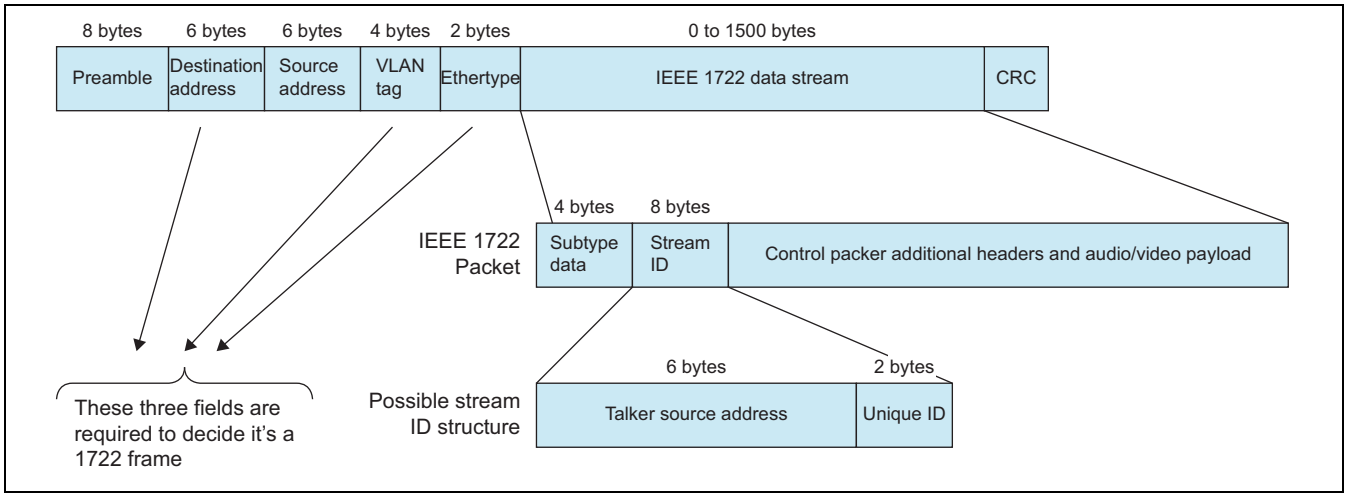


Figure 33A.19 IEEE 1722 Frame Layout and Stream ID

The IEEE 1722 standard stipulates that the stream ID field starts from the 23rd byte (not counting the preamble). Accordingly, set the separation filter offset (SFO.FBP) to 22 in operations on IEEE 1722 streams. Set the separation filter mask (SFMi) and separation filter pattern (SFPi) in accord with the specification of the product in which the chip is being used.

Example: In the example of a stream ID shown in Figure 33A.19, the current application divides the field into the talker source address and the unique stream ID. The unique ID is used to differentiate between multiple streams from the same talker. Based on this, there are two settings for separation filter masking:

- To divide various streams into individual queues, set SFM0.CFM to H'FFFF FFFF and SFM1.CFM to H'FFFF FFFF.
- To divide streams from various talkers into individual queues, set SFM0.CFM to H'FFFF FFFF and SFM1.CFM to H'0000 FFFF. This excludes the unique ID from the filter condition.

(3) Reconfiguration of separation filter during OPERATION

In CONFIG mode the initial separation filter configuration is defined. To prevent inconsistent filter results during OPERATION direct parameter change is not possible; instead update mechanism by SFVi.LV and SFL.LC should be used.

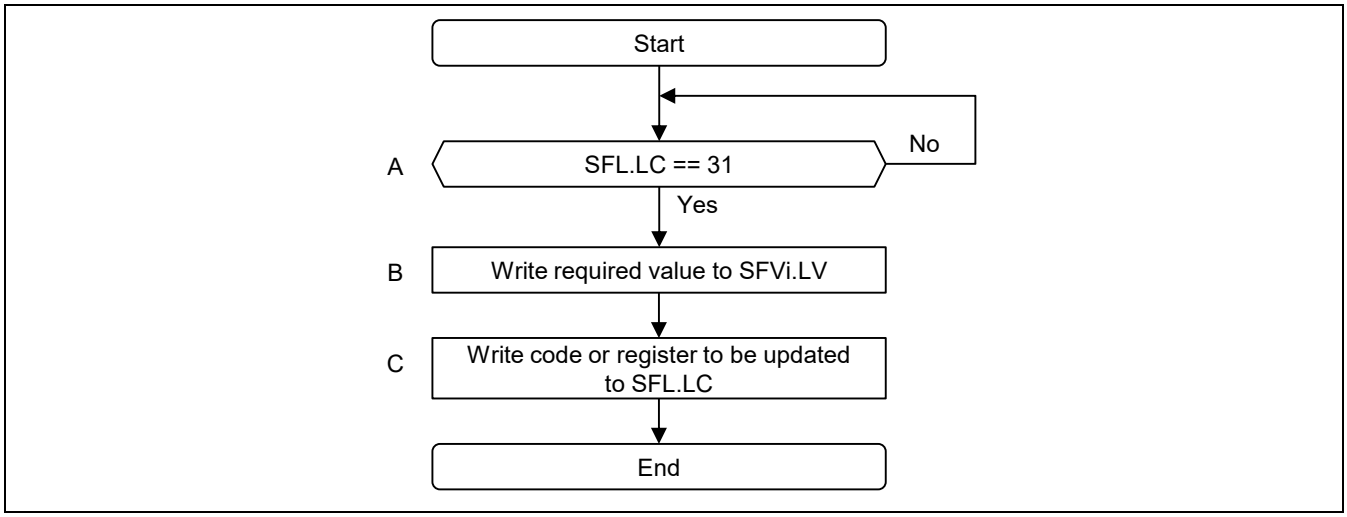


Figure 33A.20 SW flow to update separation filter during OPERATION

When reconfigure separation filter, EthernetAVB guarantees consistent classification for one received frame. If reconfiguration requires a sequence of parameter changes, CPU has to order reconfiguration based on application demand. EthernetAVB updates filter configurations when no frame reception is handled. In worse case the update is delayed by one frame reception. Exact duration depends on PHY speed and frame size. By reading SFL.LC CPU can observe when a previous update has been processed.

Note: Frame classification happens during frame reception and storage into internal Rx-FIFO. There may be frames with old classification pending in Rx-FIFO or under storage to URAM when filter reconfiguration is accepted.

33A.3.4.2 Setting Up Reception Descriptors

For reception, the descriptor mechanism is essentially as described in section 33A.3.3 Descriptors.

This section describes memory operations that are especially required in handling reception queues.

(1) Reception Descriptor Type

The type of a descriptor is defined by the descriptor type (DESCR.DT) field.

Table 33A.11 shows the descriptor types used in reception.

Table 33A.11 Descriptor Types in Reception

Descriptor Type (DESCR.DT)	Operation	Write-back
Frame Start (FSTART)	Condition for data not being stored in a reception queue: The RIS2.QFFr bit indicates that queue r is full and the received frame is not stored. Descriptor processing proceeds again in response to further reception.	Not changed
Frame Middle (FMID)	Same as FSTART	Not changed
Frame End (FEND)	Same as FSTART	Not changed
Frame Single (FSINGLE)	Same as FSTART	Not changed
Link (LINK)	Processing proceeds to the descriptor specified by DESCR.DPTR.	LEMPTY
Fixed Link (LINKFIX)	Same as LINK	Not changed
End Of Set (EOS)	A stop point defined by software has been reached. A descriptor of this type within a divided frame (writing of FMID or FEND) stops the frame being stored and the frame is lost. RIS2.QFFr indicates that the frame has been lost. If this happens at the start of a frame (writing of FSTART or FSINGLE), storing of frames starts from the next descriptor. In either case, processing shifts to the next descriptor in the chain.	EEMPTY
Frame Empty (FEMPTY)	The descriptor can be used to store received data. Up to DESCR.DS bytes are stored in the descriptor data area. For details, see section 33A.3.4.3(1) Storing Frame Data in the Descriptor Data Area.	FSTART, FMID, FEND, or FSINGLE
Frame Empty Incremental Start (FEMPTY_IS)	The descriptor can be used to store received data. All data for the frame are stored in the descriptor data area. DESCR.DPTR indicates the base address of the incremental data area. For details, see section 33A.3.4.3(2) Incremental Data Areas.	FEND or FSINGLE
Frame Empty Incremental Continue (FEMPTY_IC)	The descriptor can be used to store received data. The remaining bytes of frame data are stored in the descriptor data area. DESCR.DPTR is undefined, but is written back at the start position within the incremental data area after processing. For details, see section 33A.3.4.3(2) Incremental Data Areas.	FEND or FSINGLE
Frame Empty No Data storage (FEMPTY_ND)	The descriptor can be used to store received data. Up to DESCR.DS bytes are captured from the reception FIFO but not stored. After processing, DESCR.DS is written back as 0. For details, see section 33A.3.4.3(2) Incremental Data Areas.	FSTART, FMID, FEND or FSINGLE
Link Empty (LEMPTY)	Same as FSTART	Not changed
EOS Empty (EEMPTY)	Same as FSTART	Not changed

(2) Configuration of Reception Frame Data Descriptors

Figure 33A.21 shows the configuration of descriptors for use with reception queues. The reception-specific fields are the same whether the descriptor is normal or extended. The reception-specific fields (DESCR.MSC, DESCR.PS, DESCR.EI, and DESCR.TR) are described in Table 33A.12.

For the other fields and the descriptor types, see section 33A.3.3.6 Descriptor Type.

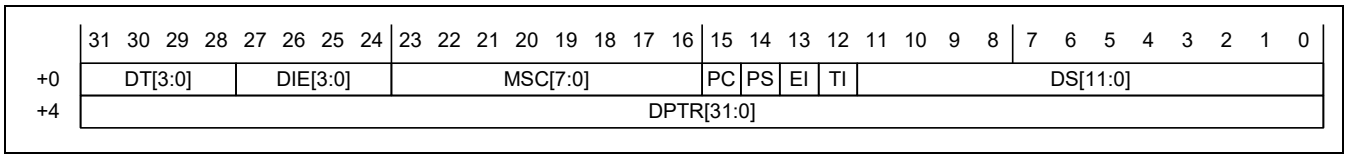


Figure 33A.21 Configuration of Descriptor for a Received Frame

Table 33A.12 Configuration of a Received Descriptor

Bit Name	Function
MSC	E-MAC Status Code These bits indicate errors in reception detected by the E-MAC. In the case of a divided frame, these bits are set to the same value within all descriptors for the frame data. Details of the bits are as follows. MSC[7]: Received frame has a multicast address. MSC[6]: Carrier extend error MSC[5]: Carrier sense error MSC[4]: Received frame has alignment error. MSC[3]: Received frame is too long. MSC[2]: Received frame is too short MSC[1]: Error in frame reception (PHY detects an error) MSC[0]: Received frame has a CRC error.
PC	Payload Crc status This bit informs about result of payload CRC check EthernetAVB does not make any confirmation if a frame contains a payload CRC. CPU need to analyse frame content before evaluating this bit. 0: Payload CRC is not matching 1: Payload CRC is correct
PS	Padding Selection These bits specify whether frame data are to be padded when stored in the incremental data area. Insertion of padding data is in accord with the settings in the RPC register. 0: Padding is not to be inserted. 1: Padding data may be inserted. This depends on the RPC settings.
EI	Error Indication This bit indicates the detection of an error in frame data while a frame was being stored. The bit is set to 1 for a descriptor in which an error has been detected. If the descriptor is for a divided frame, storage of the frame is aborted. 0: No error 1: Error is detected

Bit Name	Function
TI	Truncation Indication This bit indicates whether frame data received from the E-MAC have been truncated before being stored. These bits are set to the same value within all frame data descriptors for a divided frame. 0: Data have not been truncated. 1: Data have been truncated.

Note: The RCR.EFFS bit specifies whether or not frames with errors detected by the E-MAC are to be stored in the URAM. When the storing of error frames is disabled, error codes are not written to DESCR.MSC.

33A.3.4.3 Reception Processing

After initialization, the AVB-DMAC is able to select the proper reception queue and store received frames in the data area in the URAM as indicated by the descriptor. The AVB-DMAC continues to store received data in the URAM as long as space is available for descriptors and data areas.

Received frames are classified and stored in the reception FIFO in accord with the algorithm described in section 33A.3.4.1(1) Separation Filtering.

If the reception FIFO contains even one frame, storing is executed to the reception queue.

If there is even one empty data descriptor in a queue for which reception has started, the storage of frame data starts. Received frames for a queue that is already full (there is no empty frame descriptor or the UFC stop level has been reached) are discarded from the reception FIFO. This ensures that one queue being full does not prevent the storage of data in the other queues.

(1) Storing Frame Data in the Descriptor Data Area

Frame data for storage are assumed to be in either of the two patterns described below.

- The data for an entire frame will fit in the descriptor data area.
  - In this case, the descriptor type (DESCR.DT) is FSINGLE.
- Frame data to be stored in the descriptor data area arrive in divided form.
  - In this case, FSTART is written to the descriptor type (DESCR.DT) bits of the first descriptor of the frame data to arrive and FMID and FEND are written to the type bits of descriptors for subsequent data.

The descriptor type is updated by the AVB-DMAC in the last step of descriptor processing, so software can always access the descriptor assigned to DESCR.DT.

When normal synchronization mode is used, the CPU can write FEMPTYxxx directly to the descriptor type field after processing the stored element. Do not change the descriptor or any part of the descriptor data area after FEMPTYxxx is written to DESCR.DT.

(a) Storing Frame Data for a Whole Single Frame

For a frame with an FSINGLE descriptor, all data for the frame are held at the position defined by DESCR.DPTR. DESCR.DS indicates the length of the received frame.

If DESCR.DS is bigger than the actual size of a received frame, the FSINGLE descriptor is stored in place of the FEMPTY or FEMPTY_ND descriptor after processing.

Also, the FSINGLE descriptor is stored in place of the FEMPTY_IS or FEMPTY_IC descriptor, which always hold the descriptor data area greater than all frame data in Rx-FIFO after processing.

(b) Storing Frame Data as Divided Frames

Divided frames are handled in the same way as a single frame. A frame stored with divided descriptors must be recombined before use. DESCR.EI and DESCR.TS are only valid in the last descriptor of the sequence for a divided frame.

Note: If the data area size setting in DESCR.DS is not a multiple of four, the number of bytes set in DESCR.DS is fetched from the reception FIFO and the remaining bytes are used as the next storage area.
After a received frame is divided into different descriptors, each storage element is handled separately, and the descriptor type is assigned by software after processing. Accordingly, an error frame (FEMPTYxxx instead of FMID or FEND) may exist while a descriptor chain is being processed. In such a case, the CPU must postpone processing of the error frame to the next trigger point.

(c) No Data are Stored

The application specification may lead to some types of received frames being unimportant (for example, when the application only requires stream data from the Ethernet frames). Storing frames in divided form makes separating out the unnecessary parts of Ethernet frames possible.

If part of a divided frame is not required, use the FEMPTY_ND descriptor for that part so that it is not stored in the URAM. Not storing the data negates the need for bandwidth on the data bus, improving the overall performance.

When an FEMPTY_ND descriptor is processed, DESCR.DS is set to 0. This brings the frame data section of the descriptor into agreement with the FEMPTY type. DESCR.DS = 0 is for the unique identification of the descriptor after writing.

(2) Incremental Data Areas

Secure space in the URAM for storing received data. Even when data are placed in the URAM area such that all descriptor data areas of a chain are contiguous, a received frame being shorter than the descriptor data area will lead to an empty space. Figure 33A.22 shows an example of settings and the memory map.

Certain applications require that data areas be contiguous (e.g. when received data are to be processed other than by hardware as the A/V codec module). When the length of received frames differs (e.g. when payloads vary between having one or two A/V packages), the use of a static pointer in the descriptor produces empty spaces in the data area. This may necessitate direct additional processing to remove the empty spaces.

Accordingly, and to reduce the CPU load imposed by copying data, the AVB-DMAC supports an “incremental data area” function.

When incremental data areas are in use, all descriptors use a common data area for storage. One descriptor (FEMPTY_IS) defines the base address of the incremental data area and the next descriptor (FEMPTY_IC) within the descriptor chain holds received data. Figure 33A.23 shows an example of settings and the memory map.

Use of an incremental data area does not reduce the memory space in the individual descriptor data areas.

The hardware and software synchronization strategy and performance are also not changed.

It is also possible to divide a frame up among various descriptors in a way that reflects its structure (e.g. one descriptor for the Ethernet header and one for the data payload).

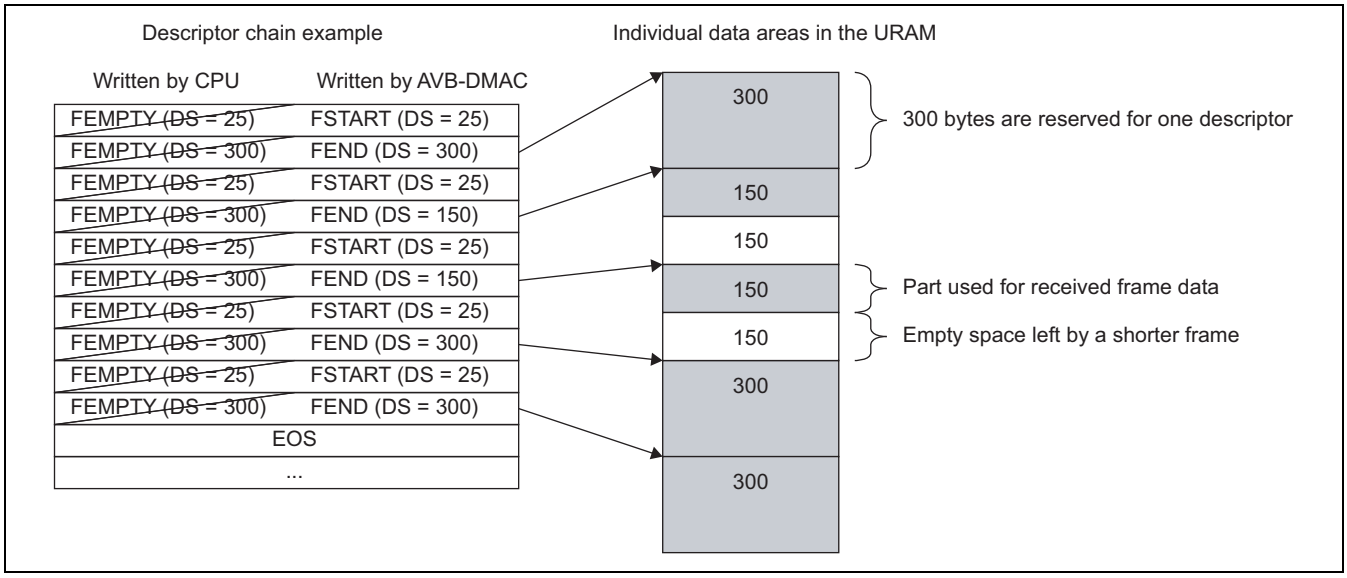


Figure 33A.22 A Reception Queue Using Individual Descriptor Data Areas

Figure 33A.22 and Figure 33A.23 show how control of the data storage areas by a descriptor chain varies according to whether individual or incremental data areas are in use. The chains are configured for storing received frames consisting of a 25-byte header (which is treated as one descriptor; and is outside the scope) and a 150- or 300-byte payload (whether one or two 150-byte payload packages are transmitted with one Ethernet frame depends on the data source).

In Figure 33A.22, the EOS descriptor is added as an example of a re-synchronization point. If the frame source transmits a frame containing more than 325 bytes, the frame will be divided among three descriptors, meaning that synchronization of the header and data sequences is lost. Despite this, however, the frame is not divided across the EOS descriptor, so recovery is automatic without software interaction. The EOS is not required with the incremental descriptors because all data being processed are always stored while an incremental data area is in use.

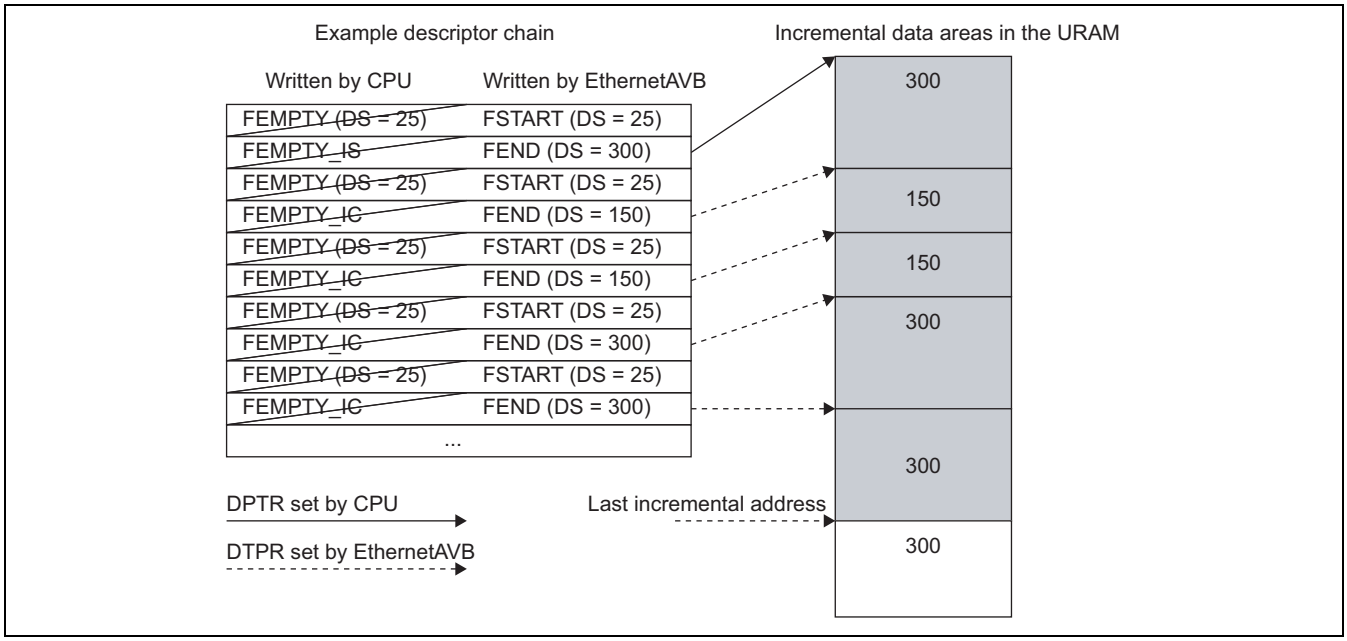


Figure 33A.23 Reception Queue Using a Common Incremental Data Area

As Figure 33A.23 shows, when data are stored in an incremental data area, the descriptor pointers in the FEMPTY_IC descriptors (DESCR.DPTR) are updated. Accordingly, the resulting FEND or FSINGLE descriptor is in the same format as after writing to an FEMPTY descriptor.

Software captures received data from an incremental data area, which has no empty storage areas between frame data. The only empty space is that at the end of the incremental data area. The sizes of incremental data areas and of blocks of data for storage in incremental data areas must be multiples of four bytes. When the amount of data for storage in an incremental data area is not a multiple of four bytes, from one to three bytes of empty space will be produced. DESCR.DS can be read to check for such empty spaces.

CPU cannot restrict directly the amount of received data stored by an incremental descriptor (FEMPTY_IS, FEMPTY_IC) as this is possible for other descriptors (FEMPTY, FEMPTY_ND) by DESCR.DS. Incremental descriptors store always all received data.

(a) Setting Up an Incremental Data Area

A descriptor chain in the incremental data area having N descriptors (one FEMPTY_IS and N-1 FEMPTY_IC) means that the incremental storage area of N times of maximum frame size is needed.

As Figure 33A.23 shows, DESCR.DPTR of an FEMPTY_IS descriptor indicates the base address of the incremental data area. The next FEMPTY_IS descriptor in the chain indicates the processing step where data must be stored in the incremental data area.

(b) Processing an Incremental Data Area Based on Descriptors

Since data processing by the CPU is the same regardless of how the AVB-DMAC stores the data, data stored in an incremental data area do not require any special handling.

(c) Padding

Use padding for received frame data that are not aligned correctly in the specified memory structure. Padding can be set individually for each descriptor. Accordingly, in the reception of divided frames, padding can be restricted to only those frames that require it (e.g. A/V payload data.)

Padding can also be used to optimize system performance in an incremental data area (e.g. to prevent inefficient access by aligning received data with 32-byte boundaries in the incremental data area), as well as to fulfill application-specific requirements for specified memory structures (e.g. formats required by other modules that will be processing the received data).

Padding can only be used in an incremental data area.

The value H'0000 0000 is always used in padding.

Padding is the addition of the number of words (from one to seven 32-bit words) set in the stored padding counter in the receive padding configuration register (RPC.PCNT). This padding is repeatedly inserted in accord with the value in the stored data counter (RPC.DCNT) (from one to 255 32-bit words). When the stored data counter (RPC.DCNT) reaches 0, however, padding is not repeated.

The first word of padding is always inserted at the position specified by DESCR.DPTR. When divided frames are in use, a padding word can be inserted at any byte position, and padding is handled on a 32-bit basis (e.g. an incremental data area where the first descriptor is for a 42-byte header data and the second descriptor holds padded payload data).

The next figure shows a general example of how padding is inserted and an example of setting up padding. A indicates frame data A received by the E-MAC, and B indicates the frame data stored in the descriptor data area (32-bit word units).

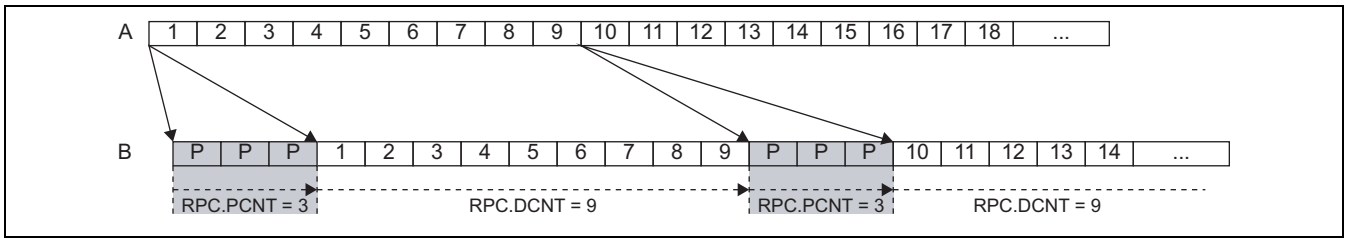


Figure 33A.24 Example of a Padding Setting

Both padding and received frame data are counted in the descriptor size (DESCR.DS).

(3) Mode with Write-Back

Constructing a descriptor chain requires software (see Figure 33A.25).

In the example in the figure, the variable SWdescr (software descriptor pointer) is a structure to identify a descriptor being processed. SWdescr must be initialized after operation mode is entered and a descriptor base address load request (DLR.LBAq) is executed (condition for starting the flow of software operations).

The frame_processing() function processes the stored data. The function can use SWdescr.DT to check whether processing of a frame is completed. How frame data are processed differs with the application, so create functions that handle processing in accord with the specification.

The processing section is common to all modes of reception. The number of frames processed in response to each trigger can be restricted. When multiple frames have to be processed in a batch, waiting for individual trigger boxes must be skipped for these frames.

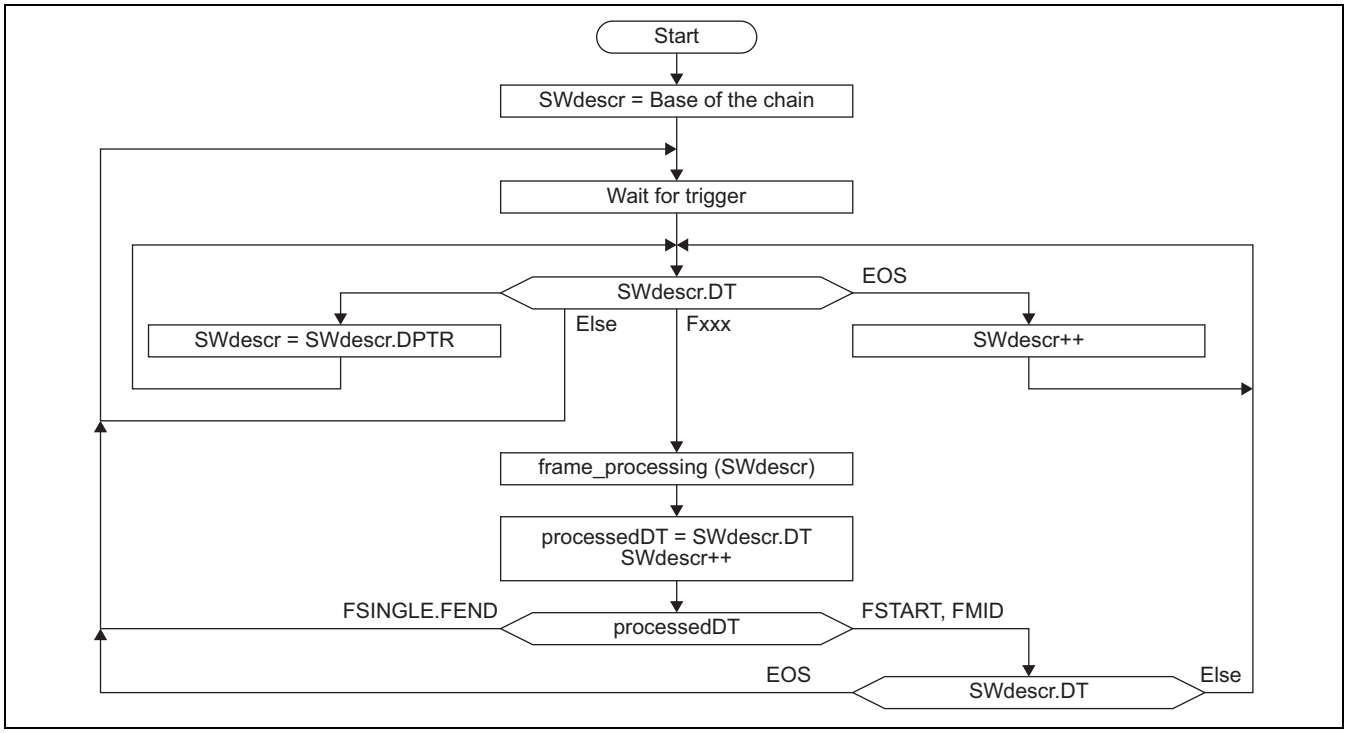


Figure 33A.25 Flow of Reception Descriptor Processing (with Write-Back)

(4) Support for Reception Time Stamps

Capturing reception time stamps is essential for IEEE 802.1AS time synchronization. Other types of received frames may also require that a reception time stamp be appended; this depends on the application. The AVB-DMAC supports reception time stamps based on the gPTP timer by storing time stamps, which have been captured when Start Frame Delimiter (SFD) of a received frame is arrived, in the last frame data descriptor (FEND or FSINGLE). For the gPTP timer, see section 33A.3.7.1 gPTP Timer.

When time stamps are to be stored, use extended descriptors for the entire reception queue. Furthermore, time stamps are always stored for reception queue 1 (network control). Time stamps for reception queue 0 (best effort) and reception queue r ($r \geq 2$; for stream data) can be selected by the time stamp enable bits in the receive configuration register (RCR.ETS0 or RCR.ETS2).

33A.3.4.4 Unread Frame Counters

Each reception queue has an unread frame counter (UFCVi). Use the unread frame counter configuration bits in the receive queue configuration register (RQCi.UFCCr) to select from among the four warning and stop levels for each unread frame counter. The 0 setting disables the stop and warning functions. For how to set this up, see Figure 33A.26.

Operations of the AVB-DMAC (hardware) and CPU (software) drive an unread frame counter (UFC) in the following ways.

- The hardware indicates that it has added a new frame to the descriptor chain for the queue (this increments the counter).
- Software indicates how many frames from the descriptor chain it has processed by writing to the corresponding bits of the unread frame counter decrement register for the queue (this decrements the register by the number written).

The unread frame counter is based on the number of frames stored in the URAM and is only incremented by one even when a received frame is divided into different descriptors. Failure in storing a descriptor chain requires care because this may unread frame counter may fail in synchronization as described in section 33A.3.4.4(1) Unread Frame (UFC) Synchronization Failure.

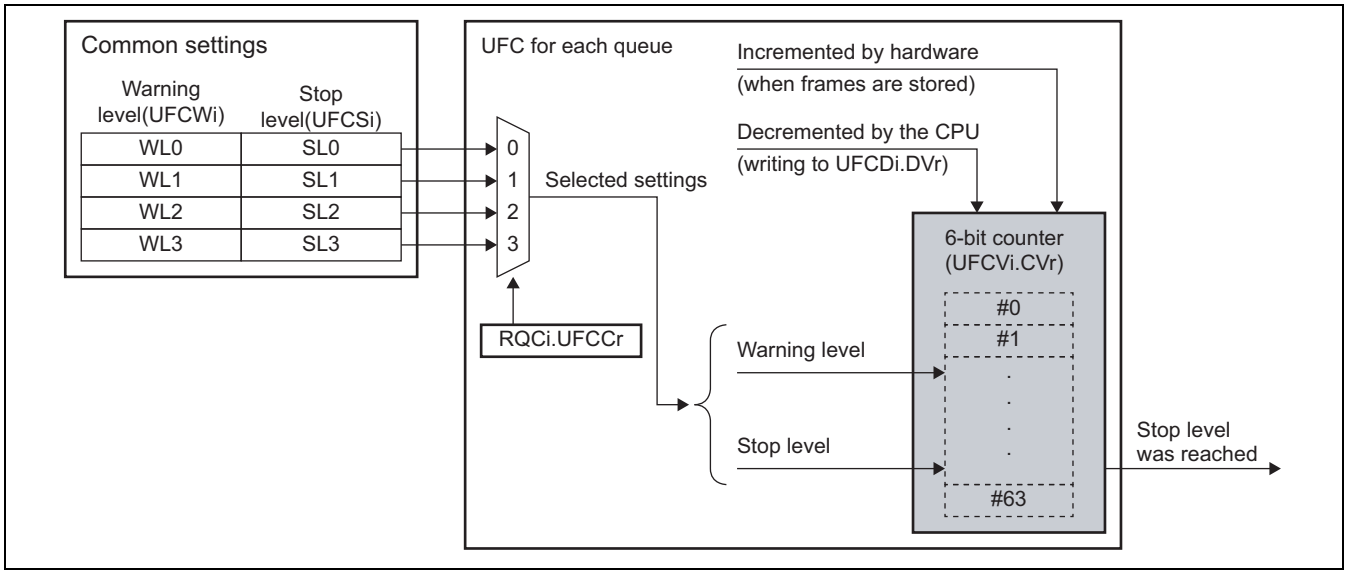


Figure 33A.26 Overview of an Unread Frame Counter

Unless synchronization of hardware and software is lost, the current unread frame counter value (UFCVi.CVr) indicates the number of unread frames in the queue.

The indicator that the stop level has been reached prevents the storage of further received frames in the descriptor chain. Selecting 0 as the stop level disables this function. Otherwise, further received frames for the queue are discarded once its unread frame counter reaches the stop level. Activation of the unread frame counter stop function is indicating by setting of the receive queue full interrupt flag in the receive interrupt status register 2 (RIS2.QFFr).

Set the unread frame counter warning level configuration register (UFCW) and the unread frame counter stop level configuration register (UFCS) for each reception queue that will use the unread frame counter function while the current operating mode is configuration mode.

(1) Unread Frame (UFC) Synchronization Failure

The unread frame counters do not recognize failure to store a frame in the URAM. In other words, the AVB-DMAC increments the counter for a queue each time it captures a frame for that queue from the reception FIFO whether or not it succeeds in storing the frame normally in the descriptor chain.

In general, synchronization of hardware and software fails under the following conditions.

- An unread frame counter reaching its maximum value
  When the value of a counter in an unread frame counter register i (UFCVi) (i = 0 to 4) reaches 63, synchronization for the corresponding queue can fail.
  The CPU can only judge that a failure in synchronization has not occurred when the stop level is set to 63.
- A queue not having enough space for a descriptor
  In this case, the corresponding receive queue full interrupt flag (RIS2.QFFr) in receive interrupt status register 2 (RIS2) is set.
  If an unread frame counter reaches its stop level while synchronization remains normal, the receive queue full interrupt flag (RIS2.QFFr) in the receive interrupt status register 2 (RIS2) is set. Software must respond to this.
- A problem occurring during access to memory

The result of a failure in synchronization is the unread frame counter indicating that the corresponding descriptor chain may contain more available frames than it actually can. To retrieve the correct starting point for operations, use the descriptor base address load request (DLR.LBAq) for the given queue.

33A.3.5 Transmission Control

Areas in the URAM for storing transmission descriptors must also be secured (for descriptors, see section 33A.3.3 Descriptors).

The AVB-DMAC fetches data from the URAM in accord with the procedure the descriptor describes. The descriptor also retains tag information once the frame has been fetched for transmission. The tag information is used to maintain the relationships between status and time stamps for the software and the AVB-DMAC. The status and time stamp information for transmitted frames remains accessible after their transmission is completed.

33A.3.5.1 Transmission Modes

The AVB-DMAC has two modes of transmission.

- AVB transmission mode
  This mode is selected by the priority level setting for the transmission queue in the transmit configuration register (setting of the TGC.TQP[1:0] bits) being B'01 or B'11.
- Non-AVB transmission mode
  This mode is selected by the priority level setting for the transmission queue in the transmit configuration register (setting of the TGC.TQP[1:0] bits) being B'00.

(1) AVB Transmission Mode

AVB transmission supports the control of traffic through the output port to implement various traffic classes.

(a) Support for Traffic Classes and Associated Priority

When transmission is in AVB transmission mode, streams of traffic are transmitted in accord with the part of the AVB specification called Forwarding and Queuing for Time Sensitive Streams (FQTSS; for details on this, see the IEEE 802.1Q standard).

In the AVB specification, at least one queue for a reserving stream under the Stream Reservation Protocol (SR stream) and at least one queue for a non-SR stream are present, and the queues for SR traffic is Highest priority queue.

The AVB-DMAC supports four traffic classes: SR class A, SR class B, network control (NC) traffic (gPTP frames), and best effort (BE) traffic. Allocating a specific queue to network control (NC) frames ensures the control of synchronization.

The AVB-DMAC realizes compliance with the AVB standards by handling queues with the following architecture (in terms of traffic classes).

- Four transmission queues (Q3, Q2, Q1, and Q0) are available.
- Q3 and Q2 are for SR streams (one each for class A and class B).
- Q1 is for low-bandwidth network control (NC) traffic (gPTP frames)
- Q0 is for other types of traffic (MSRPDU*1, MVRPDU*2, best effort (BE), etc.)

Notes: 1. MSRPDU: Multiple Stream Registration Protocol Data Unit
2. MVRPDU: Multiple VLAN Registration Protocol Data Unit

Fetching from queues proceeds in order of priority of the above traffic types. Three systems of priority are available through the setting of the transmit queue priority bits in the transmit configuration register (TGC.TQP[1:0]). In the default priority scheme, which is called AVB mode 1 (selected by TGC.TQP[1:0] = B'01), operation of the AVB-DMAC is fully in accord with the AVB specification. AVB mode 2 (transmit queue priority bits (TGC.TQP[1:0] = B'11) is an alternative priority scheme and varies from the AVB specification. Using this scheme thus requires more care. The other setting is for non-AVB-mode transmission.

Table 33A.13 Default and Alternative Priority Orders in AVB Transmission Mode

Priority Schemes (AVB Mode)	Priority Order of Queues
Default	Q3 (SR class A) > Q2 (SR class B) > Q1 (NC) > Q0 (BE)
Alternative	Q1 (NC) > Q3 (SR class A) > Q2 (SR class B) > Q0 (BE)

(b) Transmission Selecting Algorithm and CBS

The algorithm the AVB-DMAC applies to select frames for transmission is in accord with the specifications under section 8.6.8, Transmission selection, of the IEEE 802.1Q standard. For AVB mode, the CBS (credit-based shaping) algorithm is applied to the class A and class B SR queues (Q3 and Q2). Use of the CBS enables correct handling of the priorities of transmission from the SR queues. For the CBS algorithm, see section 33A.3.6 CBS (Credit-Based Shaping).

When the following conditions both hold, transmission from an SR queue (Q3 or Q2) proceeds at the specified time.

- The queue contains at least one frame ready for transmission.
- The queue has available credit.
- Unless an SR queue satisfies the above conditions, a higher priority queue is not present (not ready for transmission).

A non-SR queue (Q1 or Q0) is selected if the conditions below both hold.

- The queue contains at least one frame ready for transmission.
- As well as the above condition, a higher priority queue is not present (not ready for transmission).

Figure 33A.27 and Figure 33A.28 are flowcharts of selection for transmission in AVB mode 1 (default) and AVB mode 2 (alternative).

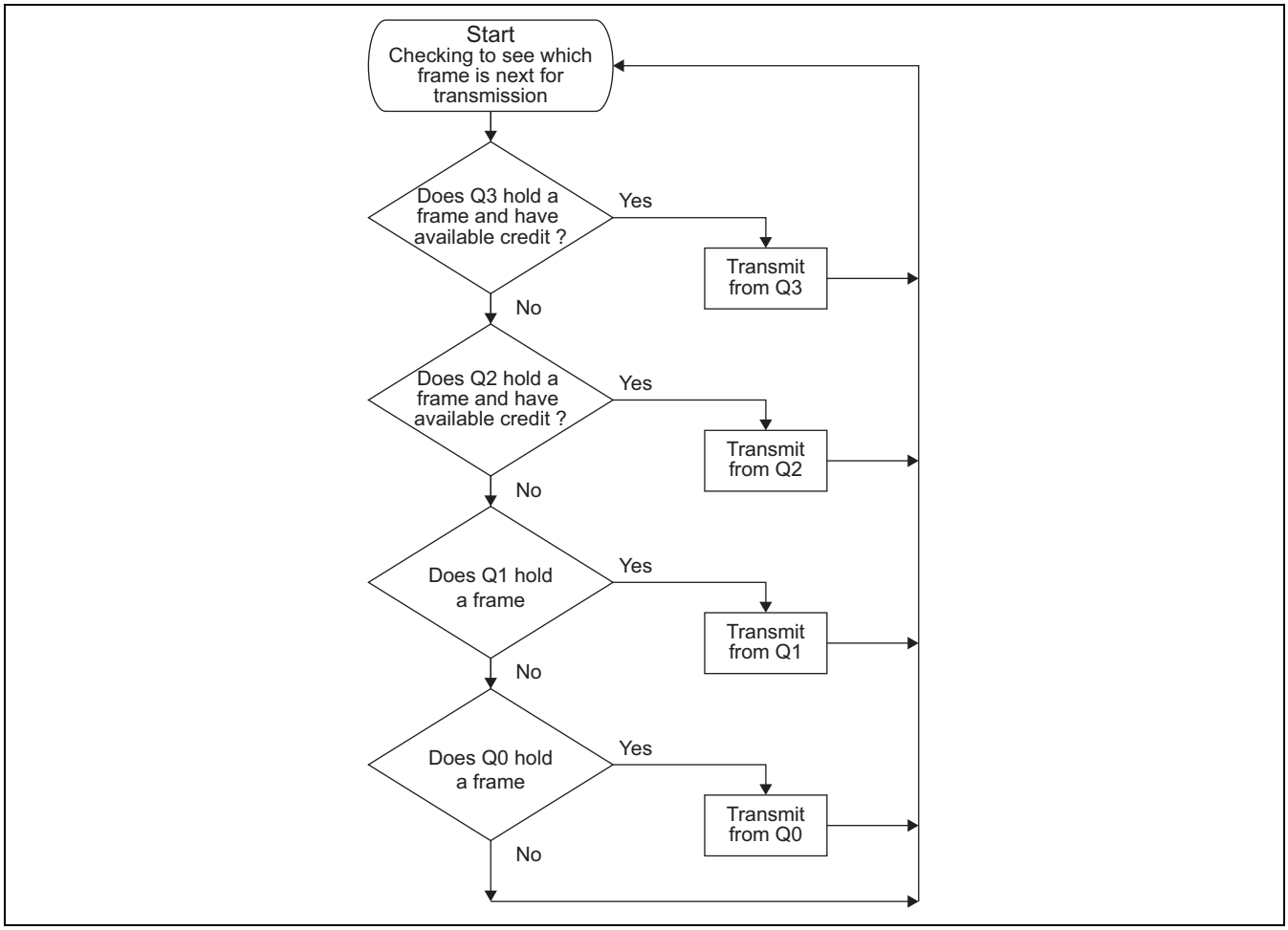


Figure 33A.27 Flow of Selection for Transmission in AVB Mode 1 (Default)

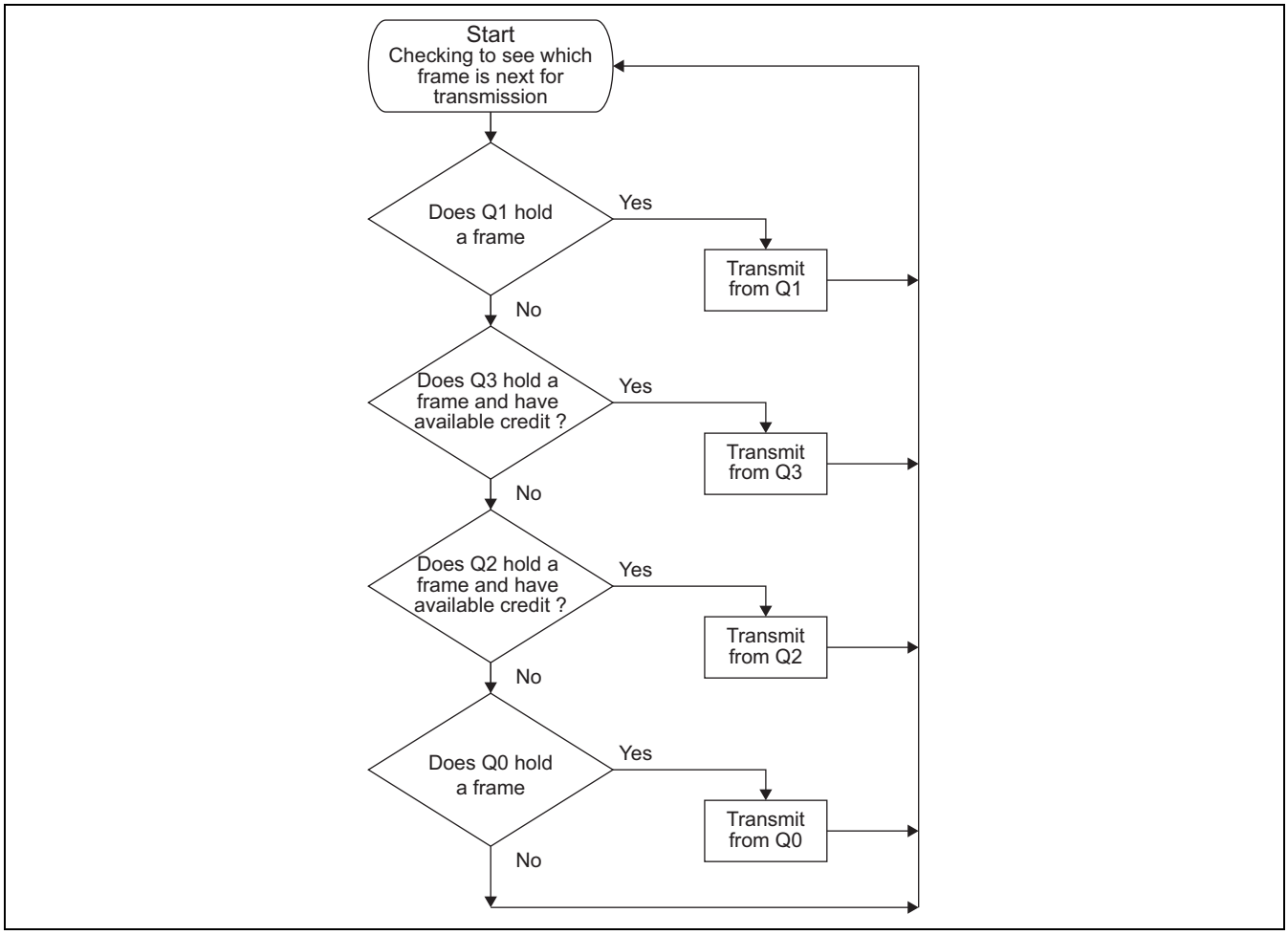


Figure 33A.28 Flow of Selection for Transmission in AVB Mode 2 (Alternative)

(2) Non-AVB Transmission Mode

In non-AVB transmission mode, an absolute priority scheme is used. The SR class is not supported and the CBS algorithm is not used.

In non-AVB transmission mode (when the transmit queue priority bits in the transmit configuration register (TGC.TQP[1:0]) are B'00), data is fetched for transmission in a strict order of priority (Q3 > Q2 > Q1 > Q0).

Figure 33A.29 shows the flow of selection in non-AVB transmission mode.

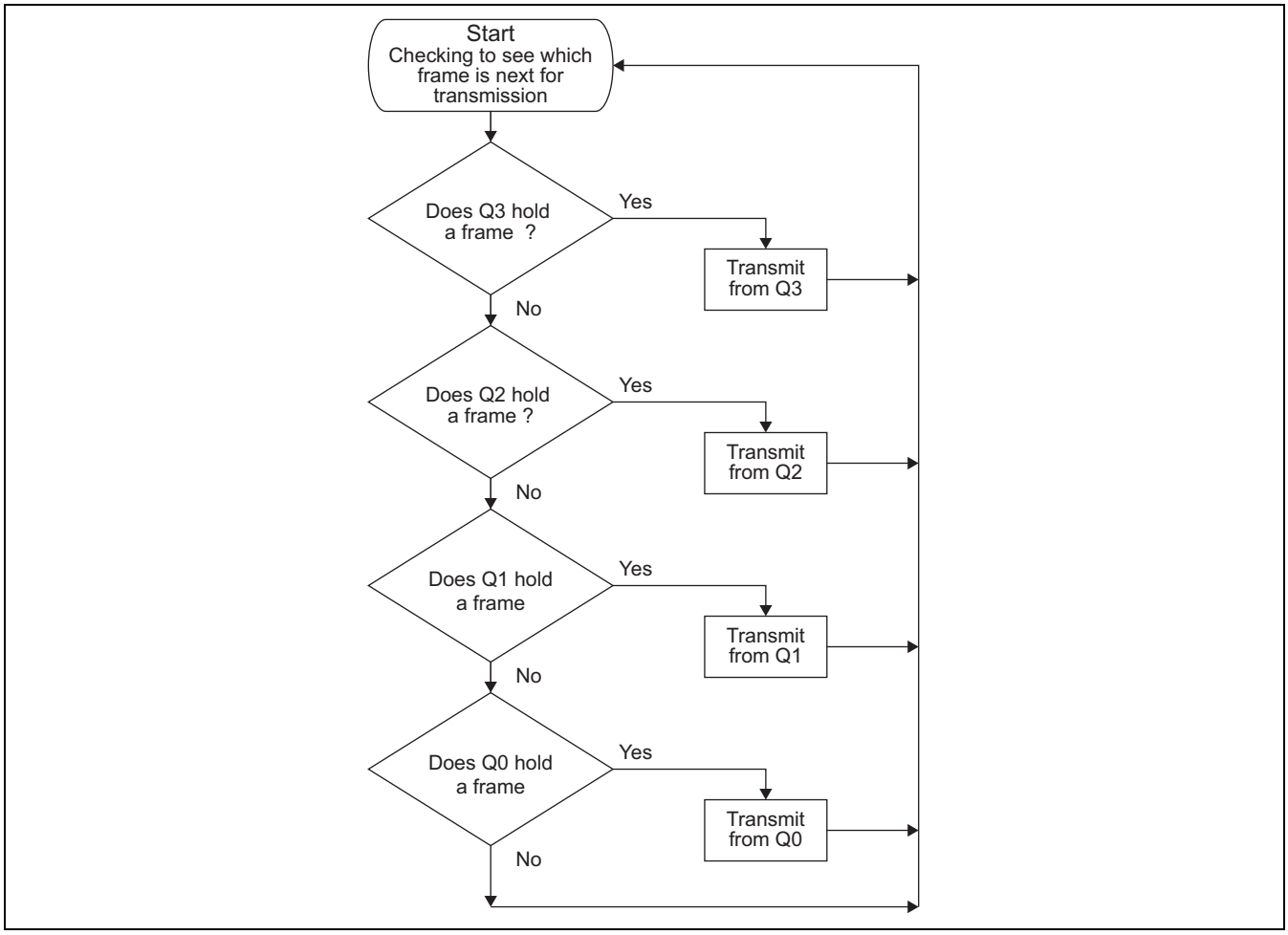


Figure 33A.29 Flow of Selection for Transmission in Non-AVB Mode

(3) Setting the Size of the Transmission FIFO

The transmission FIFO is made up of 122 clusters. Each cluster can hold up to 128 bytes.

The size of the part of the transmission FIFO for use by each of the four transmission queues can be set by the corresponding transmit queue configuration q bits in the transmit control register (TGC.TBDq). The setting of TGC.TBDq is fixed to 2.

General Usage Examples:

Q0: Frames containing up to 1500 bytes → 1500/128 = 11.7 → 12 clusters
Q1: Frames containing up to 1024 bytes → 1024/128 = 8.0 → 8 clusters
Q3: Frames containing up to 1996 bytes → 1996/128 = 15.6 → 16 clusters
Q4: Frames containing up to 1996 bytes → 1996/128 = 15.6 → 16 clusters
When the depth of all transmission queues is 2, only the following number of clusters is required.
$2 \times (12 + 8 + 16 + 16) + 16 = 2 \times 52 + 16 = 120$

In the worst case (each of the transmission queues holds 1996 bytes), $2 \times 64 + 16 = 144$ clusters are required, so the maximum length of transmission frames must be less than 1996 bytes for some queues.

33A.3.5.2 Setting Up Transmission Descriptors

(1) Transmission Descriptor Type

The type of a descriptor is defined by the descriptor type (DESCR.DT) field.

Table 33A.14 shows the descriptor types used in transmission.

Table 33A.14 Descriptor Types in Transmission

Descriptor Type (DESCR.DT)	Operation	Write-back
Frame Start (FSTART)	The AVB-DMAC fetches the first of the data for the divided frame and proceeds to processing of the next descriptor.	FEMPTY
Frame Middle (FMID)	The AVB-DMAC fetches the second or subsequent data for the divided frame and proceeds to processing of the next descriptor.	FEMPTY
Frame End (FEND)	The AVB-DMAC fetches the last of the data for the divided frame. The frame of data that has been fetched to the transmission FIFO is ready for transmission by the E-MAC, and then the AVB-DMAC proceeds to processing of the next descriptor.	FEMPTY
Frame Single (FSINGLE)	The AVB-DMAC fetches the frame of data. The frame of data that has been fetched to the transmission FIFO is ready for transmission by the E-MAC, and then the AVB-DMAC proceeds to processing of the next descriptor.	FEMPTY
Link (LINK)	Processing proceeds to the descriptor specified by DESCR.DPTR.	LEMPTY
Fixed Link (LINKFIX)	Same as LINK	Not changed
End Of Set (EOS)	This is a transmission stop point defined by software This leads to clearing of the transmit start request bit (TCCR.TSRQt), which stops transmission. When the TCCR.TSRQt is again set to 1 (a new transmission start request is issued), processing proceeds to the next descriptor.	EEMPTY
Frame Empty (FEMPTY)	No frame data are ready for transmission This leads to clearing of the transmit start request bit (TCCR.TSRQt), which stops transmission. When the TCCR.TSRQt is again set to 1 (a new transmission start request is issued), processing starts at this descriptor.	Not changed
Link Empty (LEMPTY)	Same as FEMPTY	Not changed
EOS Empty (EEMPTY)	Same as FEMPTY	Not changed

(2) Configuration of Transmission Frame Data Descriptors

Figure 33A.30 shows the configuration of descriptors for use with transmission queues. The transmission-specific fields (DESCR.MSR, DESCR.TSR, and DESCR.TAG) are described in Table 33A.15.

For the other fields and the descriptor types, see section 33A.3.3.6 Descriptor Type.

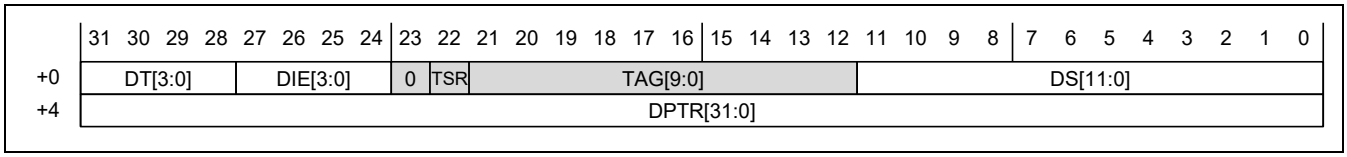


Figure 33A.30 Configuration of Descriptor for a Transmitted Frame

Table 33A.15 Configuration of a Transmission Descriptor

Bit Name	Function
TSR	Time Stamp Store Request This bit specifies whether the transmission time stamp is to be stored within the EthernetAVB module. 0: The time stamp status FIFO within the EthernetAVB module does not retain a transmission time stamp. 1: The time stamp status FIFO within the EthernetAVB module retains a transmission time stamp. This bit is available while the current DESCR.DT is FEND or FSINGLE.
TAG	Frame Tag This TAG field is used to associate each frame data with a time stamp. Frame TAG is not required but is recommended. This bit is available while the current DESCR.DT is FEND or FSINGLE.

For the time stamp FIFO function, see section 33A.3.5.4 Time Stamping in Transmission.

33A.3.5.3 Transmission

(1) Transmitting Frames

Setting the transmit start request bit in the transmit configuration control register (TCCR.TSRQt) starts the transfer of frames from the corresponding transmission queue.

The descriptor in the current descriptor address (CDARq.CDA) for the queue t (with q = t) is read first.

If this descriptor is a descriptor for frame transmission (FSINGLE, etc.), the AVB-DMAC fetches the frame data from the data area indicated by the descriptor, writes FEMPTY back to the descriptor type (DESCR.DT) bits to indicate completion of this processing, then proceeds to processing of the next descriptor.

If the descriptor is not for transmission, processing is as dictated by the given descriptor (for these descriptors, see the descriptions in section 33A.3.3 Descriptors).

If a base address load request is issued for a descriptor chain while it is being processed (by setting 1 in the LBAq bit for transmission queue q that is currently being processed in the descriptor base address load request register, DLR), processing proceeds to the new descriptor chain. Changing the chain does not interrupt frame fetching, but note that frames that have not been fetched from the old chain remain where they are.

Figure 33A.31 shows descriptor processing during transmission.

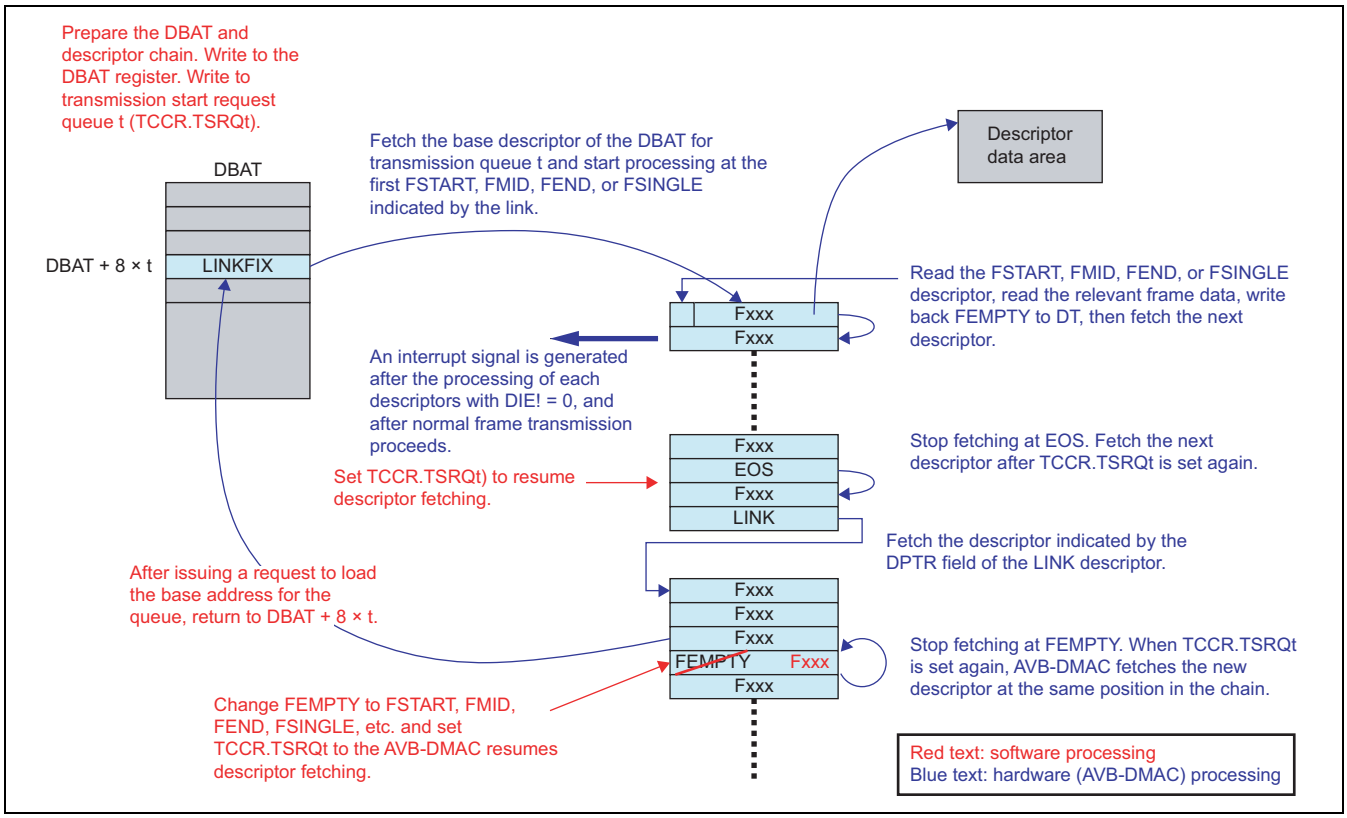


Figure 33A.31 Descriptor Processing During Transmission

(2) Examples of Descriptor Usage

(a) Immediate Frame Transmission

Immediate frame transmission is a pattern in which fetching by the AVB-DMAC starts whenever software adds data to a queue. FEMPTY descriptors are used as stop points to keep the hardware and software in synchronization.

Create descriptor chains that have FEMTPY descriptors at the stop points.

Figure 33A.32 shows the flow for software implementing this pattern. SW should read back written descriptor between changing FEMPTY descriptor before writing to TCCR.TSRQt.

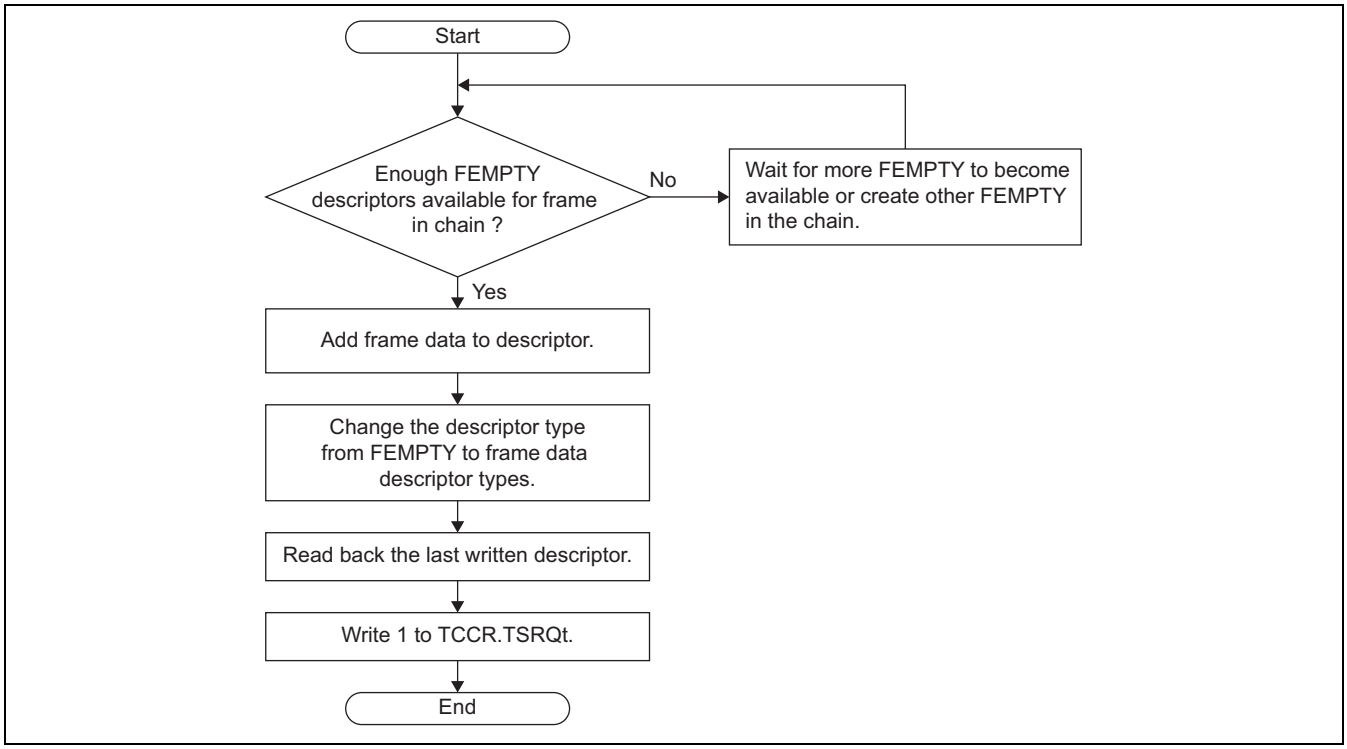


Figure 33A.32 Software Flow for Immediate Frame Transmission

Figure 33A.33 shows software and AVB-DMAC operations for immediate frame transmission.

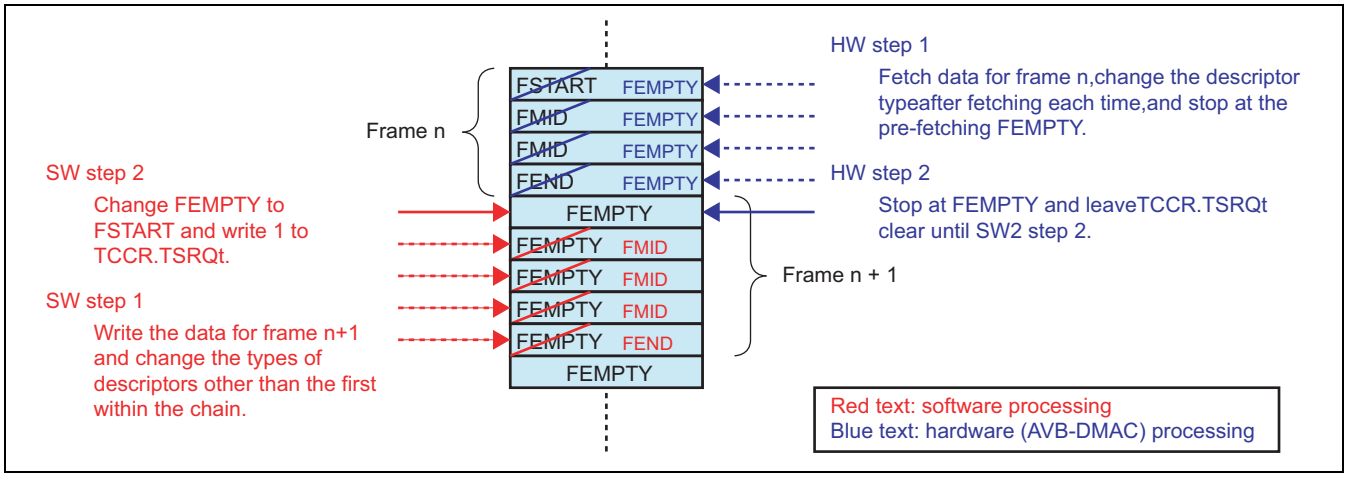


Figure 33A.33 Software and AVB-DMAC Operations for Immediate Frame Transmission

(b) Frame Set Transmission with Changing of the Active Descriptor Chain

This pattern is used when data are transmitted with a delay for software control to secure bandwidth or for other reasons, rather than immediately transmitted. EOS descriptors are used for the stop points. Start by creating a descriptor chain that has a FEMPTY descriptor as its stop point.

Figure 33A.34 shows the software flow in this pattern.

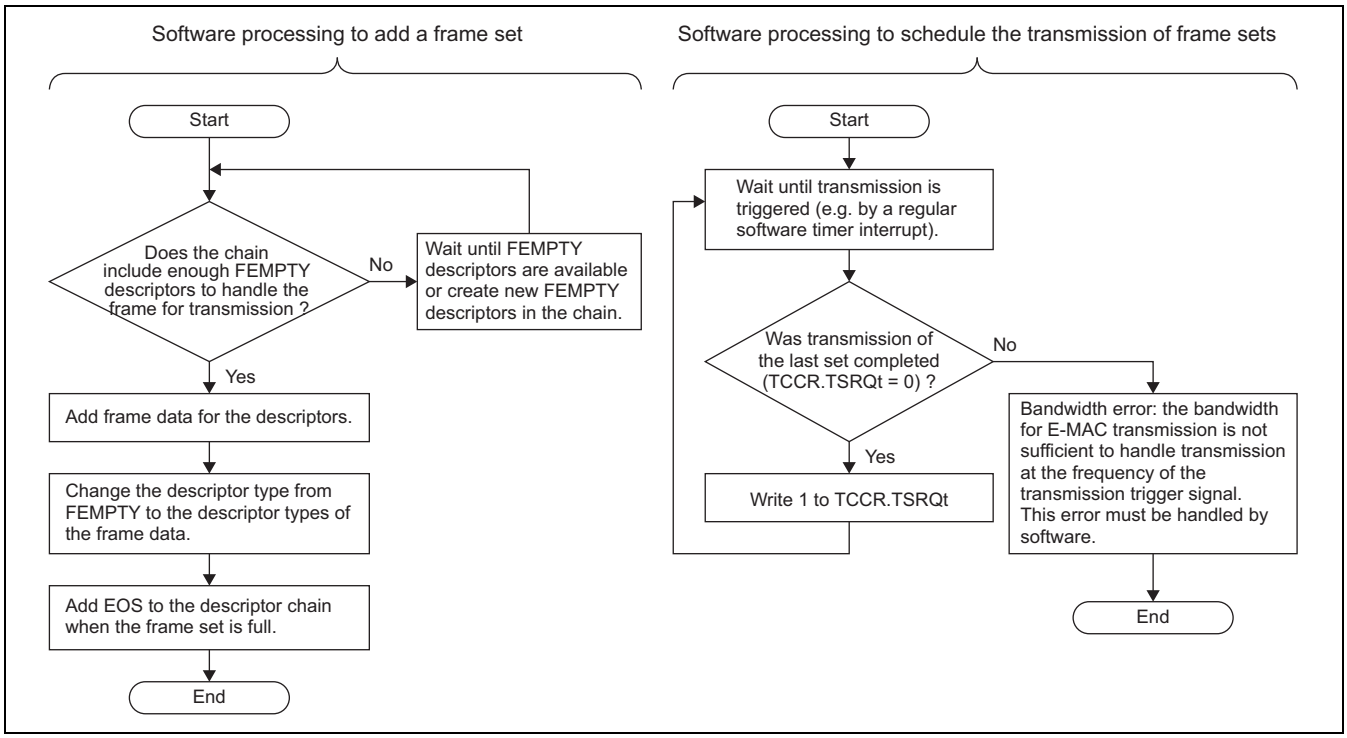


Figure 33A.34 Software Flow for Frame Set Transmission with Changing of the Active Descriptor Chain

Figure 33A.35 shows software and AVB-DMAC operations for frame set transmission.

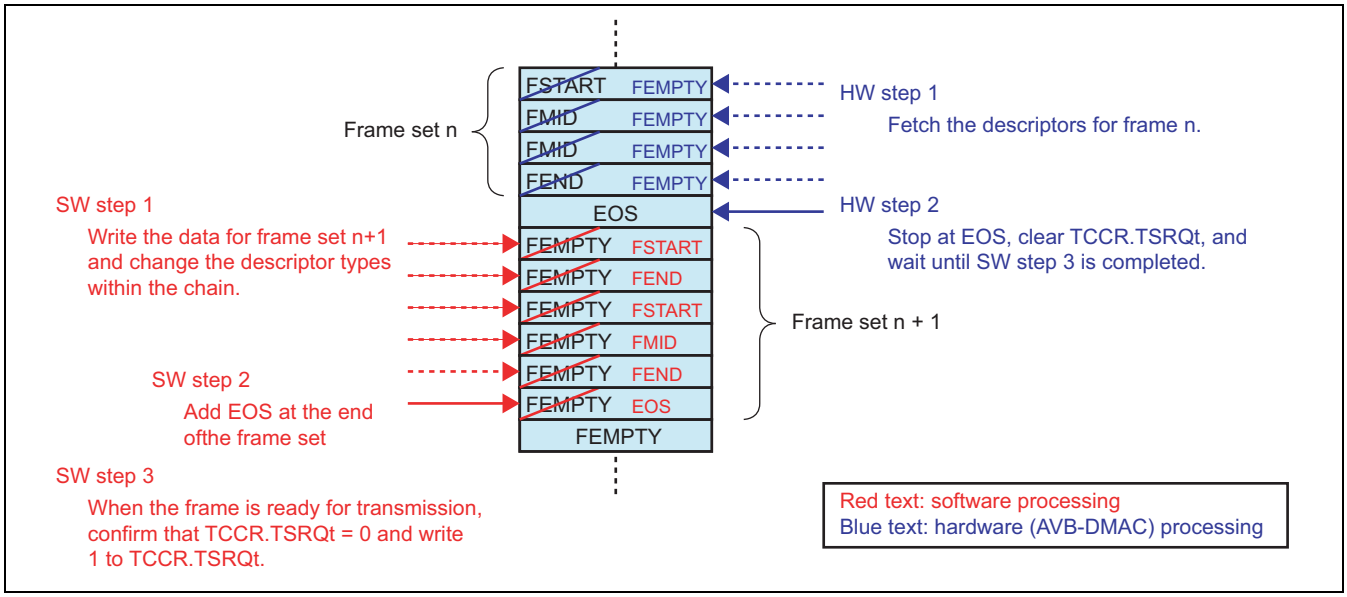


Figure 33A.35 SW and AVB-DMAC Operations for Frame Set Transmission with Changing of the Active Descriptor Chain

(c) Frame Set Transmission Using a Shadow Descriptor Chain

This pattern is used when data are transmitted with a delay for software control to secure bandwidth or for other reasons, rather than immediately transmitted. Two or more descriptor chains are used. The chains are classified as active or shadow chains. EOS descriptors are used for the stop points.

Create descriptor chains that have FEMPTY descriptors at the stop points.

Figure 33A.36 shows the flow for software implementing this pattern.

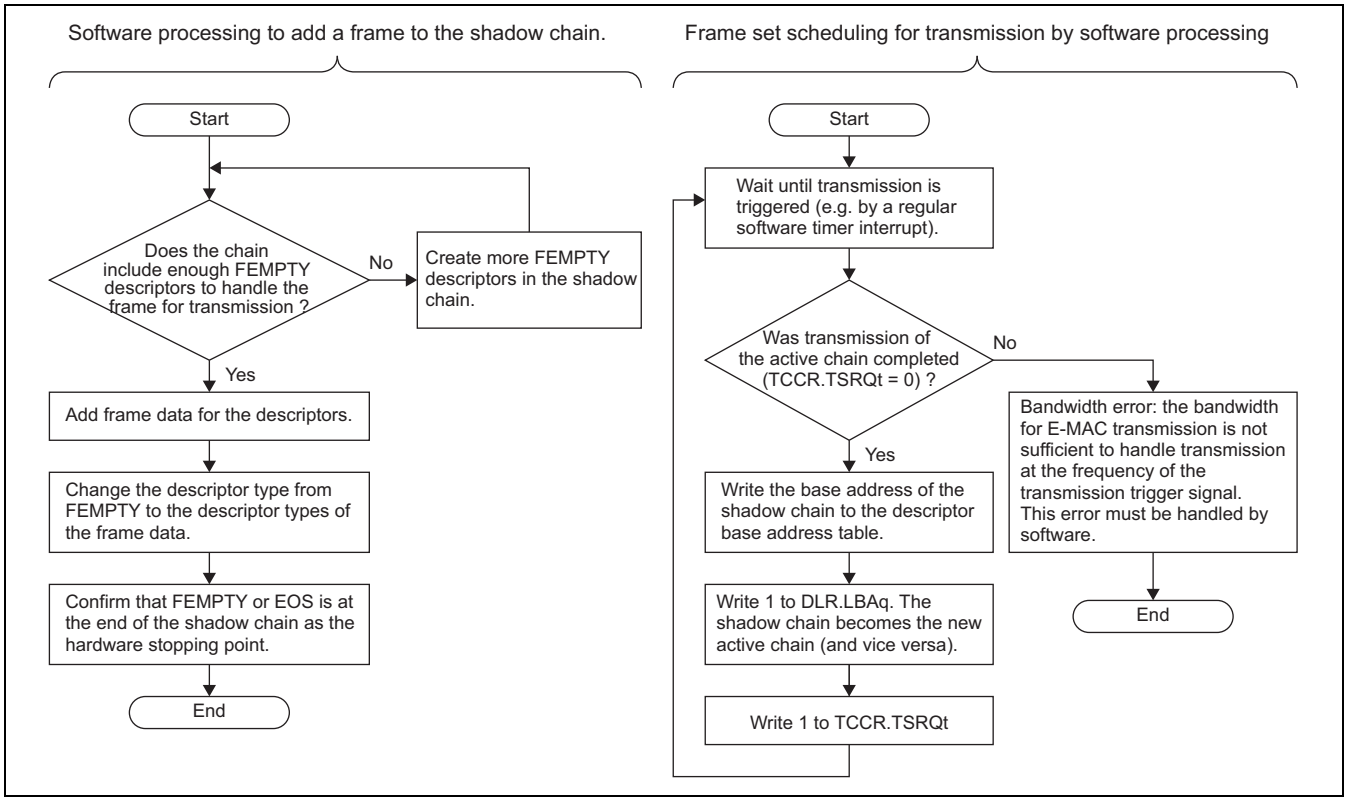


Figure 33A.36 Software Flow for Frame Set Transmission Using the Shadow Descriptor Chain

Figure 33A.37 shows software and AVB-DMAC operations for frame set transmission.

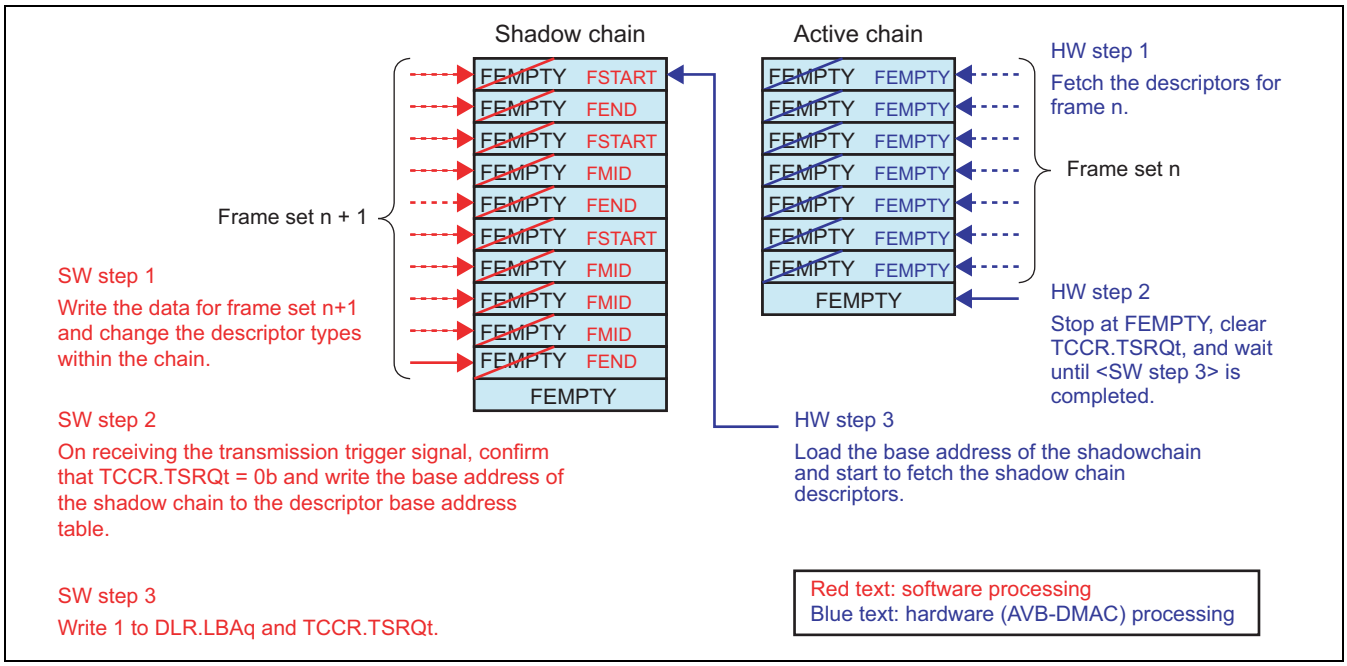


Figure 33A.37 SW and AVB-DMAC Operations for Frame Set Transmission Using the Shadow Descriptor Chain

33A.3.5.4 Time Stamping in Transmission

Transmission time stamps are important in satisfying the requirements for timing and synchronization of the IEEE 802.1AS standard. Reference to this information can also be useful to other applications and in testing. The AVB-DMAC supports the storage of time stamps for transmitted frames. The time-stamp values are based on the gPTP timer and are captured at the same time as sending of the Start of Frame Delimiter (SFD) for transmitted frames.

When the time stamp storage request field (DESCR.TSR) is set to 1, selecting storage of a time stamp, the tag number defined in the tag field (DESCR.TAG) of the last descriptor (FEND or FSINGLE) for the frame being transmitted is stored with the time stamp. This eases identification and association. The time-stamp FIFO is accessible at any time.

Figure 33A.38 shows the mechanism supporting transmission time stamping.

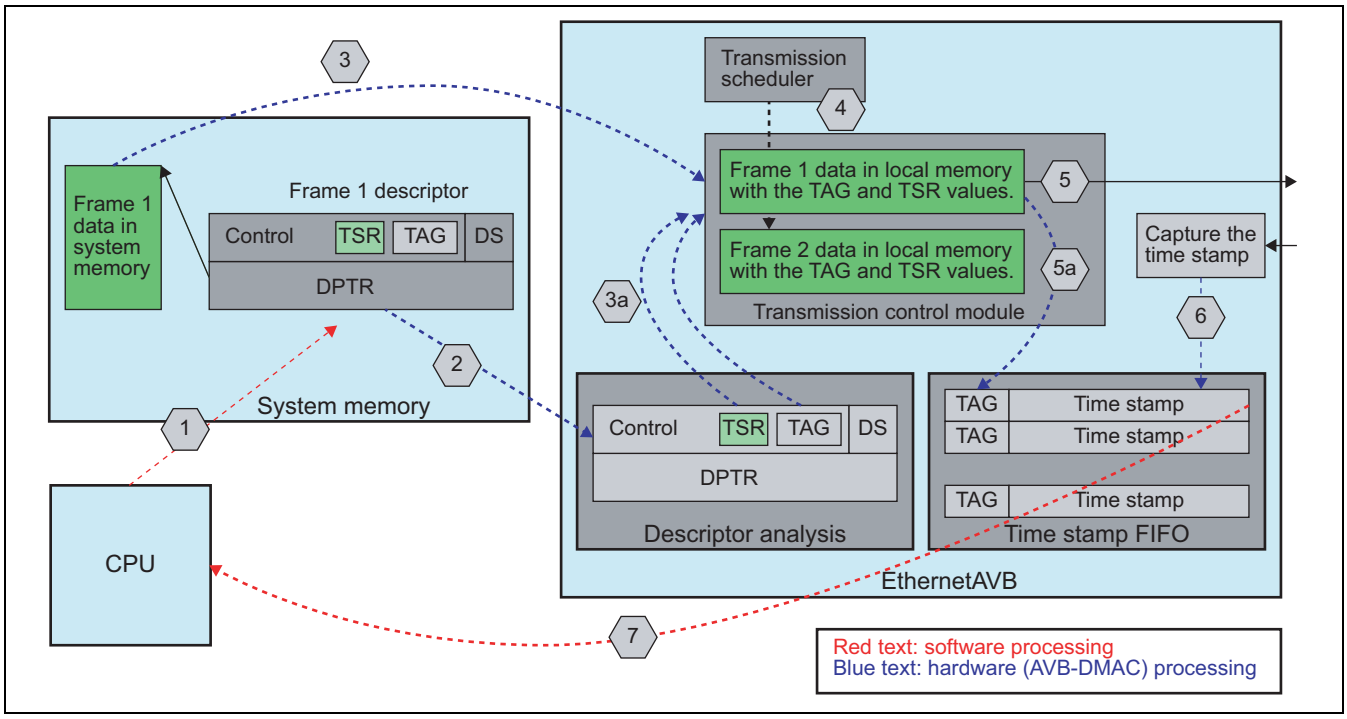


Figure 33A.38 Mechanism to Support Transmission Time Stamps

The method of using this function is described below:

1. Secure space in the URAM for the frame requiring time stamping.
   Write the tag number of the frame to the frame tag field (DESCR.TAG) and set the time stamp storage request field (DESCR.TSR) to 1.
2. The AVB-DMAC fetches and analyzes the descriptor. The time stamp storage request field (DESCR.TSR) is 1, so it recognizes that transmitting this frame also requires storage of the time stamp.
3. The AVB-DMAC fetches the data for frame 1 and temporarily stores the frame in internal memory for scheduling.
   3a: The frame tag field (DESCR.TAG) and time stamp storage request field (DESCR.TSR) are stored with the fetched data.)
4. Under the control of priority settings according to credit-based shaping (CBS) or another scheme, the transmission scheduler decides it is time to transmit frame 1.
5. Transmission of frame 1 starts.
   5a: Frame 1's tag is stored in the time-stamp FIFO.
6. The gPTP time stamp is captured at the start of frame delimiter (SFD) for transmission and stored with the tag in the time-stamp FIFO when the frame is completely transmitted. An interrupt is generated to indicate existence of new timestamp information. For this to happen, the descriptor interrupt control register (DIC) must be set beforehand.
7. The entry can now be read from the time-stamp FIFO.

Use the time-stamp FIFO for the timing and synchronization of frames with IEEE 802.1AS compliance.

Time stamping can also be used with other frames, but take care not to allow the time-stamp FIFO to overflow. When the FIFO is full, further time stamps supplied to it are lost.

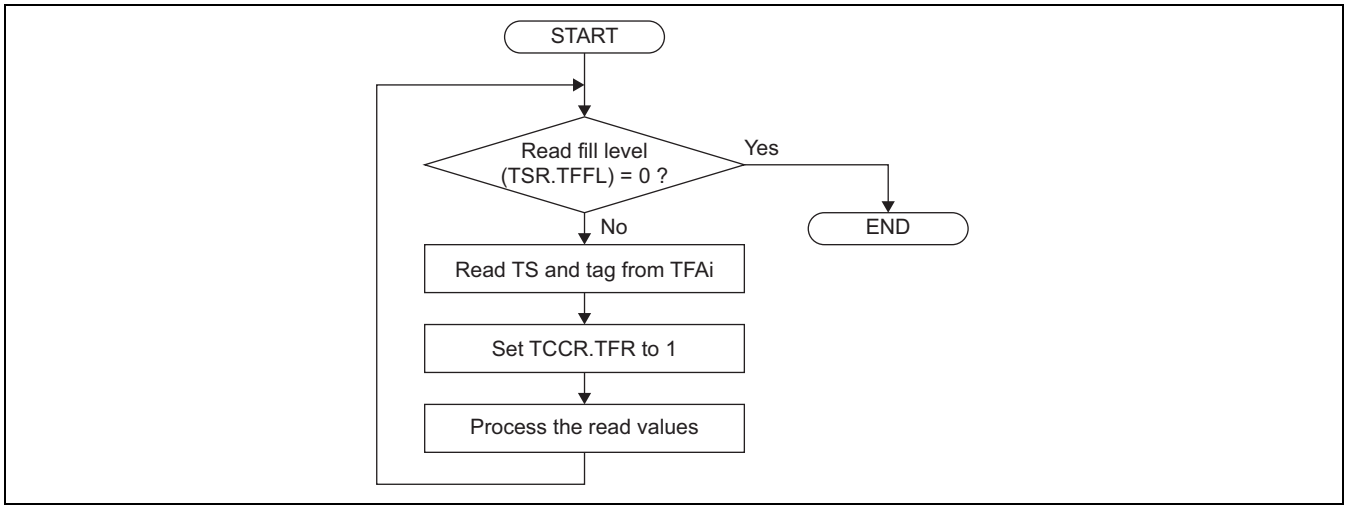


Figure 33A.39 Flow of Transmission Time Stamping

33A.3.5.5 Ending Transmission

Figure 33A.40 shows the procedure for ending transmission.

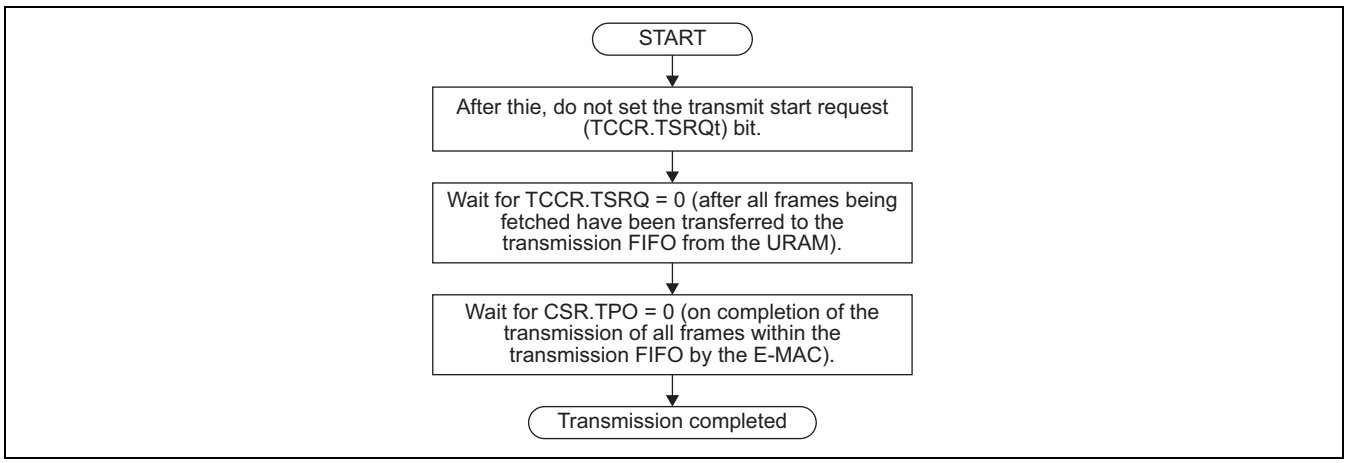


Figure 33A.40 Procedures for Ending Transmission

33A.3.6 CBS (Credit-Based Shaping)

In AVB transmission mode (i.e. when the transmit queue priority field in the transmit configuration register (TGC.TQP) is B'01 or B'11), transmission queues Q3 and Q2 are respectively assigned to class A and class B stream traffic and the CBS (Credit Based Shaping) algorithm is used to select the transmission queues in order to satisfy the Forwarding and Queuing for Time Sensitive Streams (FQTSS) specification (see section 8.6.8 or section 34 in IEEE 802.1Q).

The CBS algorithm is based on the concept of transmission credit for each queue. Credit can be thought of as the degree to which a queue has the “right” to transmit at a given time. Actually, in AVB transmission mode as specified in IEEE 802.1Q, queues that are subject to the CBS algorithm are able to transmit when the following conditions are met.

At least one frame is stored in the queue.

The credit for the queue is 0 or a positive value.

The credit for a transmission queue is incremented while one or more frames from the queue are present in the transmission FIFO but transmission of these frames is not proceeding. This state is indicated by the transmission process status bit for queue t in the AVB-DMAC status register (CSR.TPOt). The credit is decremented while transmission of a frame from the queue is in progress. This mechanism is used to control transmission so that the transmission of frames from the queues for each of the traffic classes does not exceed the specified maximum bandwidths.

IEEE 802.1Q defines the following parameters for queues under the control of the CBS algorithm.

portTransmitRate: Maximum transmission data rate of an external port. The E-MAC determines this parameter.

bandwidthFraction: Maximum fraction of portTransmitRate that can be used for a queue.

idleSlope: Rate of change of credit for a queue when transmission of frames from the queue is not proceeding so the credit value (in bits per second) is increasing. idleSlope is also equal to the maximum fraction of the total bandwidth (portTransmitRate) that is available to the given queue under a specified condition (frames from the queue can be placed in a continuous stream. See Annex L of IEEE 802.Q.
idleSlope = bandwidthFraction × portTransmitRate

sendSlope: Rate of change of credit for a queue while transmission of a frame from the queue is in progress so the credit value is decreasing.
The value of sendSlope is defined as follows:
sendSlope = idleSlope – portTransmitRate

Furthermore, the values below are used to define individual traffic classes (or queues for the classes) under control of the algorithm. See Annex L of IEEE 802.Q.

maxFrameSize: Maximum size of frames (in bits) of the corresponding traffic class that can be transmitted from a port

maxInterferenceSize: Maximum burst size (in bits) by which delays for the corresponding traffic class can be allowed

hiCredit: Maximum credit value (positive number). Can be calculated by using the following equation: hiCredit = maxInterferenceSize × (idleSlope / portTransmitRate)

loCredit: Minimum credit value (negative number). Can be calculated by using the following equation:
loCredit = maxFrameSize × (sendSlope / portTransmitRate)

Figure 33A.41 shows how the CBS algorithm works and the meaning of the above parameters.

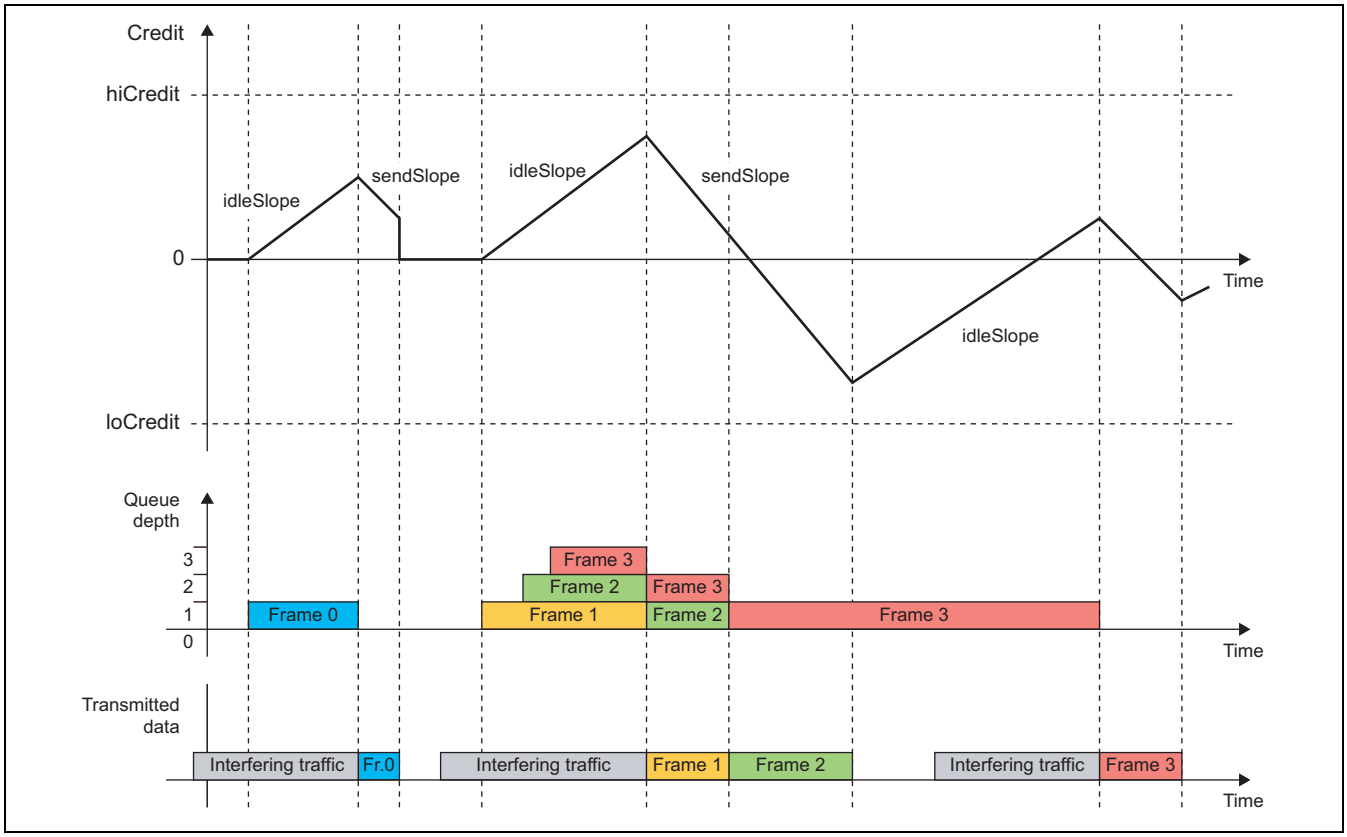


Figure 33A.41 CBS (Credit-Based Shaping) Operation

Figure 33A.42 shows the implementation of CBS in the AVB-DMAC.

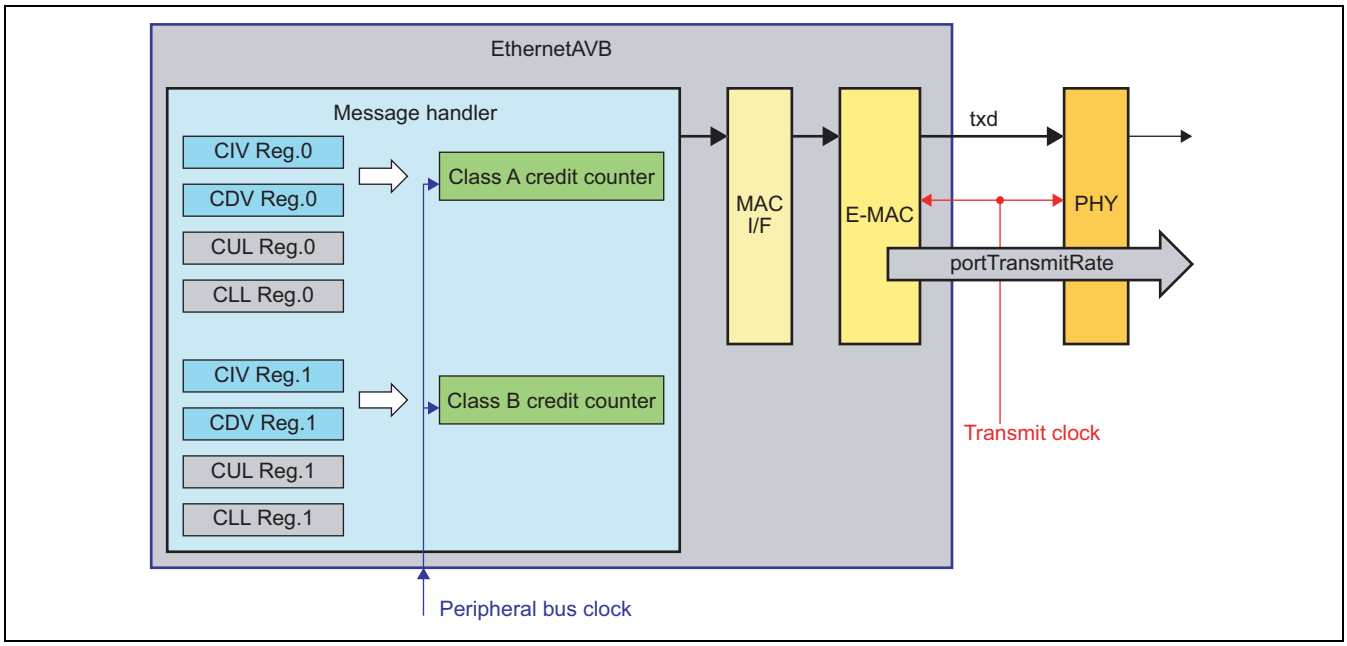


Figure 33A.42 CBS (Credit-Based Shaping) Operation in the AVB-DMAC

The above implementation is based on “credit counters” for the respective traffic classes (SR class A and class B). The following parameters apply for these classes.

CBS increment value (CIV): Signed positive number
The credit is incremented by this amount every high-speed peripheral bus clock cycle while a frame from the queue is pending but transmission has not started (idleSlope).

CBS decrement value (CDV): Signed negative number
The credit is decremented by this amount every high-speed peripheral bus clock cycle while transmission of a frame from the queue is proceeding (sendSlope).

The CBS increment value (CIV) and CBS decrement value (CDV) are defined as follows.

CIV = idleSlope × Mfactor
CDV = sendSlope × Mfactor

Mfactor is a multiplier factor to ensure accuracy for CIV and CDV. CIV and CDV are calculated by using the following equations.

CIV = (portTransmitRate/HPϕ) × bwFraction × Mfactor
CDV = (portTransmitRate/HPϕ) × (bwFraction – 1) × Mfactor

HPϕ is the frequency of the high-speed peripheral bus clock. The credit counters are driven by the high-speed peripheral bus clock, so calculating the slope parameters for CBS requires (1/HPϕ).

Use software to prepare Mfactor for the CBS parameters. All queues for the same class must have the same Mfactor for all CBS parameters. Mfactor for a specified class c can be changed during operation, unless transmission is pending for that class (i.e. the transmit process status bit in the AVB-DMAC status register (CSR.TPOt) = 0). At that time, the credit counter values for class A and class B are 0. Note that the credit value will not match a new incrementation or decrementation parameter if Mfactor is changed while the credit counter value is non-zero. Mfactor is not present in the AVB-DMAC registers.

Set the CIV and CDV parameters in the CBS increment value registers (CIVRc) and the CBS decrement value registers (CDVRc). These are treated as dynamic settings since they should be updated when streams are registered and erased in accord with IEEE 802.1Qat.

The AVB-DMAC also has CBS upper limit registers (CULc) (the upper limit registers for classes A and B) and CBS lower limit registers (CLLc) (the lower limit registers for classes A and B). Set Mfactor to match the credit value and set the upper limit (hiCredit) and the lower limit (loCredit) for each class as defined above.

CUL = hiCredit × Mfactor = maxInterferenceSize × bwFraction × Mfactor
CLL = loCredit × Mfactor = maxFrameSize × (bwFraction – 1) × Mfactor

Example:

Assume that portTransmitRate = 100 Mbps, HPϕ = 130 MHz and bwFraction = 3%. Then idleSlope and sendSlope represented as one bit vs. cycles of the high-speed peripheral bus clock are as follows.

idleSlope = (portTransmitRate/HPϕ) × bwFraction = 100/130 (Mbps/MHz) × 3% = 0.023 bit per high-speed peripheral bus clock cycle
sendSlope = idleSlope – (portTransmitRate / HPϕ) = –0.746 bits per high-speed peripheral bus clock cycle
Let Mfactor be 100, then CIV and CDV parameters are determined as follows.

CIV = idleSlope × Mfactor = 2.3
CDV = sendSlope × Mfactor = –74.6

33A.3.6.1 Restrictions on CIV, CDV and Mfactor

The maximum value (the minimum value for negative numbers) up to which the credit counter will not overflow determines the maximum values of CIV and CDV that can be set in the CBS registers. This maximum credit value is equivalent to the worst case of the hiCredit value, and the maximum values for class A and class B are calculated as follows.

<Conditions>

- Class A maximum value (hiCredit_max_classA)
  classA bwFraction ≅ 100%
  Maintaining the proper relations in the transmission priority order requires waiting for a period equivalent to the maximum frame size.
  hiCredit_max_classA ≅ maxInterferenceSize for class A = Interference due to one max. sized frame = header + max. size payload + CRC (2000 bytes) + preamble (8 bytes) + IFG (12 bytes) + processing_delay (≅ 80 bytes) ≅ 2100 bytes
- Class B maximum value (hiCredit_max_classB)
  classB bwFraction ≅ 100%
  Maintaining the proper relations in the transmission priority order requires waiting for a period equivalent to the maximum size of frames in the class A transmission queue and other transmission queues.
  hiCredit_max_classB ≅ maxInterferenceSize for class B = Interference due to two max-size frames = 2 × hiCredit_max_classA ≅ 4200 bytes

hiCredit_max_classA = 16800

hiCredit_max_classB = 33600

The maximum values that can be selected with Mfactor for the 32-bit signed counter without overflow are:

Mfactor_max_classA = 2^{31}–1 / hiCredit_max_classA ≅ 127826 and
Mfactor_max_classB = 2^{31}–1 / hiCredit_max_classB ≅ 63913.

A high degree of accuracy can be achieved even with a low bandwidth. In class B, bandwidthFraction = 0.05% and the bandwidth error < 0.1%.

The maximum value of CIV is calculated from the following equation.

CIV = idleSlope x Mfactor = (portTransmitRate / HPϕ) × bandwidthFraction × Mfactor

When Mfactor is the maximum value and bandwidthFraction is the maximum value (up to 100%):

CIV_max_classA = (portTransmitRate / HPϕ) × Mfactor_max_classA and
CIV_max_classB = (portTransmitRate / HPϕ) × Mfactor_max_classB.

The maximum values when portTransmitRate = 1000 Mbps and HPϕ = 130 MHz are as follows:

CIV_max_classA ≅ 983277

CIV_max_classB ≅ 491638

These values in the table are the limits of CIV up to which the 32-bit credit counter will not overflow. The CIV parameters are implemented as 16 bits + a sign bit, so a further limit of CIV ≤ 65535 applies to both class A and class B.

33A.3.6.2 Credit Incrementation during Inter-Frame Gaps (IFGs)

The inter-frame gap (IFG) after a frame is transmitted is not treated as part of frame transmission by the CBS credit counter. During an IFG, the credit is incremented for all SR queues that have pending frames or negative credit. Figure 33A.43 illustrates credit operations during IFGs.

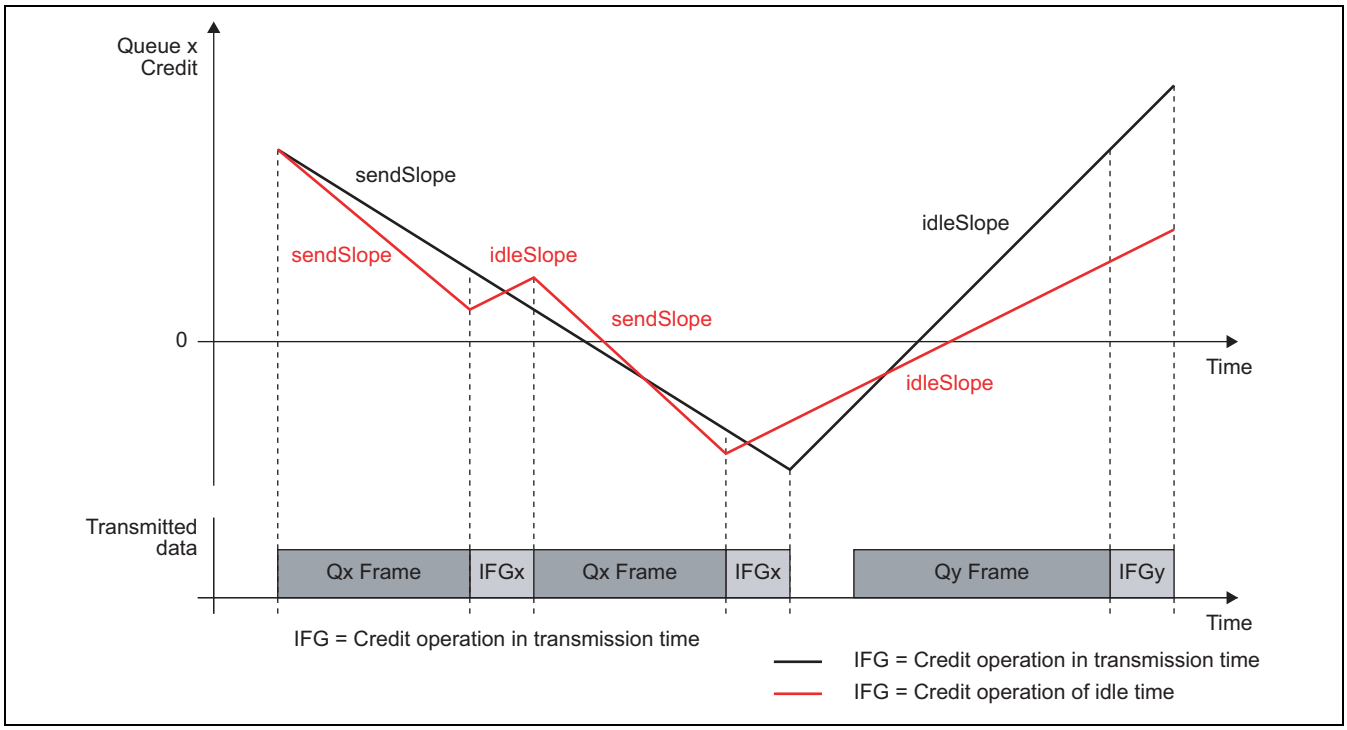


Figure 33A.43 Credit Operations during IFGs

Accordingly, the IFG need not be included in calculation of the bandwidth requirements for the specified SR class when deciding the idleSlope, sendSlope, and CIV and CDV parameters. However, IFG must also be included in the calculation in order to confirm that the total bandwidth allocated to all SR classes does not exceed 100% of portTransmitRate. This is described in *Section 35.2.2.8.4* of *IEEE 802.1Q*.

33A.3.6.3 Example

The case of a class A 48-kHz stereo audio stream among Ethernet frames is described as an example.

After every class A measurement interval (125 µs), 80 octets consisting of two sets of six 32-bit samples plus a 32-octet header are stored as audio data within a frame. The IEEE 802.3 also imposes a 42-octet media-specific framing overhead (an 8-octet preamble, 14-octet IEEE 802.3 header, 4-octet IEEE 802.1Q priority/VID Tag, 4-octet CRC, and 12-octet IFG) are also added. Accordingly, the total frame size is 80 + 42 = 122, and one such frame is transmitted after every class measurement interval.

This represents a total bandwidth of about 7.8 Mbits per second (122 octets × 8 bits per octet × 8000 frames per second) for this class. If the E-MAC is assumed to run at 1 Gbps (portTransmitRate), this is equivalent to the allocation of about 0.78% of the total bandwidth to each class A queue. If other traffic classes are to share the total transmission bandwidth, checking that this 0.78% allocation does not lead to the total allocation of bandwidth being greater than 100% of portTransmitRate is required.

To obtain the CIV and CDV parameters for a given class, the IFG must not be taken into account in calculation of the frame size must not include the IFG. For this case, therefore, we obtain an 80-bit payload + 30-bit overhead = 110-octet measurement interval for the class → the total bandwidth for the class = 7.04 Mbps = 0.704% of portTransmitRate.

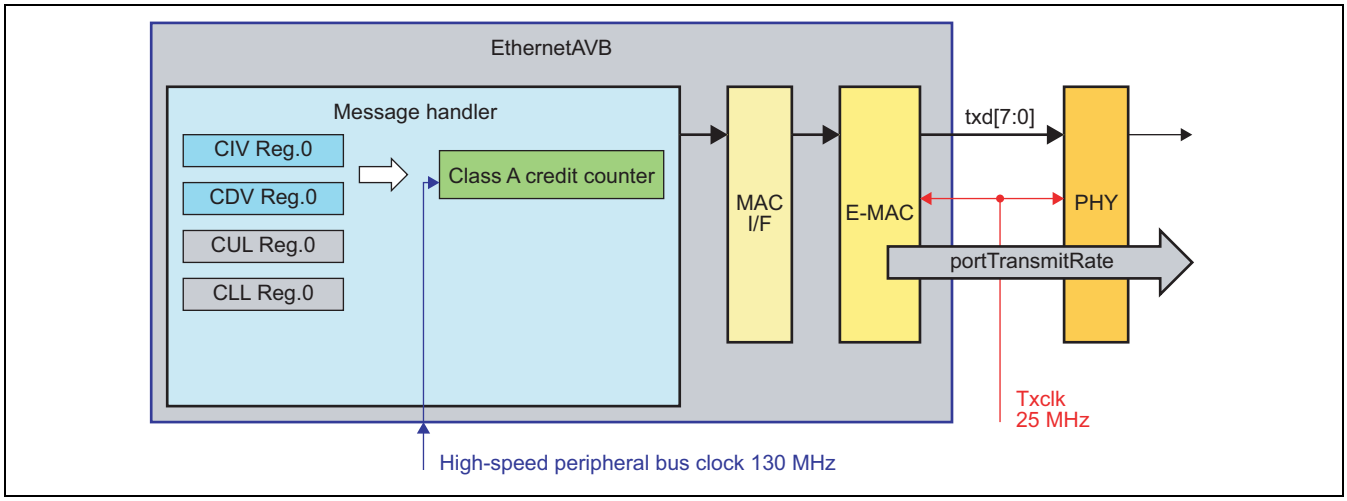


Figure 33A.44 Example of CBS Settings

Given that:

- the E-MAC runs at 100 Mbps, so portTransmitRate = 100 Mbps and
- high-speed peripheral bus clock (operating clock for the credit counter) frequency = 130 MHz, securing a bandwidth of 7.04 Mbits/sec for class A requires configuring the CBS parameters as follows.
  bandwidthFraction = 0.704%
  idleSlope = (portTransmitRate / HPϕ) × bandwidthFraction ≅ 0.0176 bits per high-speed peripheral bus clock cycle
  sendSlope = idleSlope – (portTransmitRate / HPϕ) ≅ –2.4824 bits per high-speed peripheral bus clock cycle

When Mfactor = 100000, the parameters are as follows.

- CIV = idleSlope × Mfactor = 1760 bits per high-speed peripheral bus clock cycle
- CDV = sendSlope × Mfactor = 248240 bits per high-speed peripheral bus clock cycle

These are the final values for setting in the CIVR1 and CDVR1 registers.

33A.3.7 Time Synchronization

33A.3.7.1 gPTP Timer

An 84-bit timer is provided to support the gPTP function. Figure 33A.45 shows the definitions of bits for the timer and in related registers.

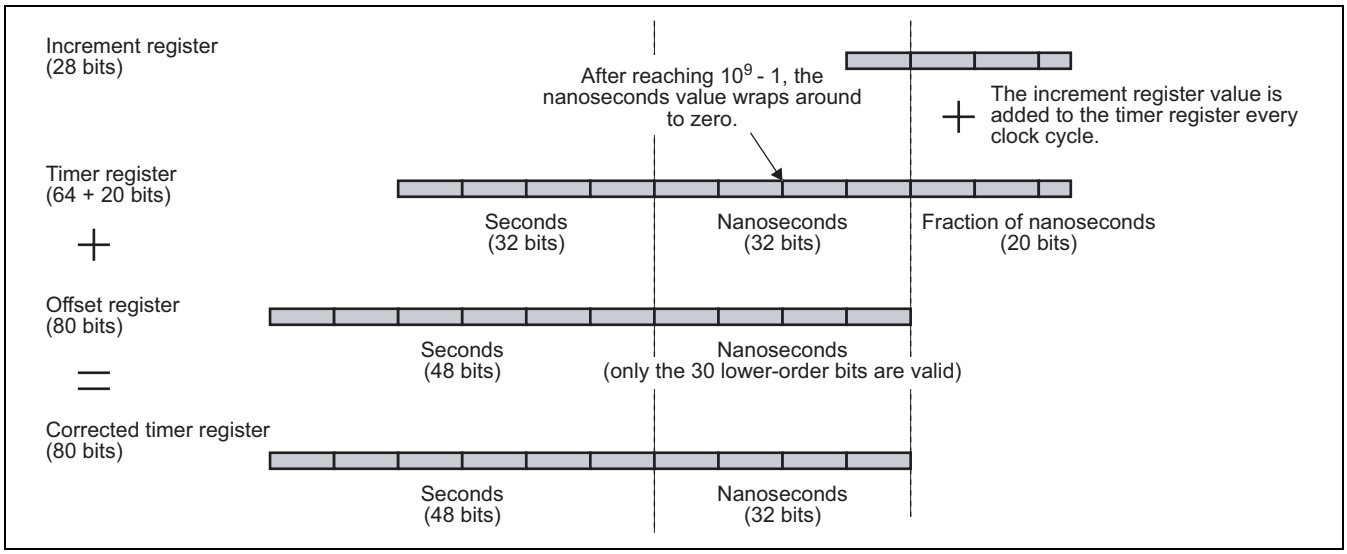


Figure 33A.45 Definitions of gPTP Timer Bits and Related Bits

The higher-order 32 bits indicate seconds. For the next 32 bits, counting by one corresponds to the passage of 1 ns. The lower-order 20 bits are a fractional value (less than 1 ns). Software can only read the 32 higher-order bits, indicating seconds, and the subsequent 32-bits, indicating nanoseconds. The 20 lower-order 20 bits, representing less than 1 ns, are not readable. They are only used within the AVB-DMAC to maintain accuracy in time measurement.

The timer can be reset by setting the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) to B'01. These bits are set to B'00 on completion of normal resetting of the timer.

After the timer starts, the value in the gPTP timer increment register (GTI.TIV) is added to the value of the gPTP timer every clock cycle.

Before setting a value in the gPTP timer increment register (GTI.TIV), set the timer increment value setting request bit in the gPTP configuration control register (GCCR.LTI). If this bit is not set to 1, new values that are written will not be reflected in the register. This bit returns to 0 after the setting is completed.

An offset to the gPTP timer is also available. If this is required, set the value in the gPTP timer offset register (GTO.TOV). Before setting a value in this register, set the timer offset value setting request bit in the gPTP configuration control register (GCCR.LTO). If this bit is not set to 1, new values that are written will not be reflected in the register. This bit returns to 0 after the setting is completed. When adding an offset, take care that it does not exceed 80 bits.

The value of the gPTP timer can be read from the gPTP timer capture register (GCTi.CTV). Set the timer capture source select bits in the gPTP configuration control register (TCCR.TCSS) to select the timer value for capture as the value of the gPTP timer, the corrected value of the gPTP timer (value with the offset added), or the AVTP presentation time. Setting the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) to B'11 initiates the capture. Once normal capture of the timer is complete, the value of the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) returns to B'00.

The timer for gPTP operates as a free-running timer but can be synchronized with the Grandmaster clock.

33A.3.7.2 Free-Running Operation

The IEEE 802.1 AS standard for timing and synchronization does not prescribe the physical adjustment of local clocks to the Grandmaster clock. To avoid negative effects from the correction procedure, we recommend the use of a free-running timer.

As a free-running timer, the timer counts the local time in seconds or nanoseconds. The gPTP timer increment register (GTI.TIV) is set to 1 ns (the setting value = H'0010 0000) and the gPTP timer offset register (GTOi.TOV) is set to 0. The ratio information captured at the time of the gPTP delay measurement and synchronization procedures is used to correct the frequency ratio to that of the Grandmaster clock. The Grandmaster clock can be calculated from the local clock by using the information collected during the gPTP measurement and synchronization procedures.

33A.3.7.3 Synchronization with the Grandmaster Clock

In situations requiring physical synchronization of the local clock with the Grandmaster clock, the fractional nanoseconds value (the 20 lower-order bits of the gPTP timer) is used to make the adjustment. Specifically, the increment value is finely adjusted to correct for deviations of the clock frequency from that of the Grandmaster clock.

Use the timer offset value (in the gPTP timer offset registers, GTOi.TOV) to correct for offsets from the theoretical value (at start-up, etc.). The sum of the timer value and the offset register is the “corrected timer” value.

Note that for the nanoseconds part of the Offset register GTOi.TOV[31:0] should be below 10^9.

The following equation gives a method of calculating the increment (GTI.TIV) from the frequency of the gPTP clock and its deviation from that of the Grandmaster clock. Variable d is the deviation (d = 10^{-6} for 1 ppm).

$$GTI.TIV = round\left(\frac{2^{20}\,GHz}{f_{GPTP}} \times (1 + d)\right)$$

After adjusting for the current deviation of clock frequency, reset the gPTP timer increment register (GTI.TIV).

After calculating the new offset value, reset the gPTP timer offset register (GTOi.TOV).

33A.3.7.4 Continuous AVTP capture

CPU can request a selected timer value by setting bit GCCR.TCR to B'11. GCCR.TCSS determines which of the three values:

- gPTP Timer value,
- Corrected Timer value or
- AVTP Timer value

is captured in GCTi.CTV. GCCR.TCR is set to B'00 after capturing the related timer value. Successful capturing operation can be confirmed by checking GCCR.TCR is B'00.

By setting GCCR.TCR to B'10 continuous AVTP timer value capture is activated. In this mode CPU has always access to current AVTP value by reading GCTi.CTV[31:0].

Flow to enter continuous AVTP capture mode:

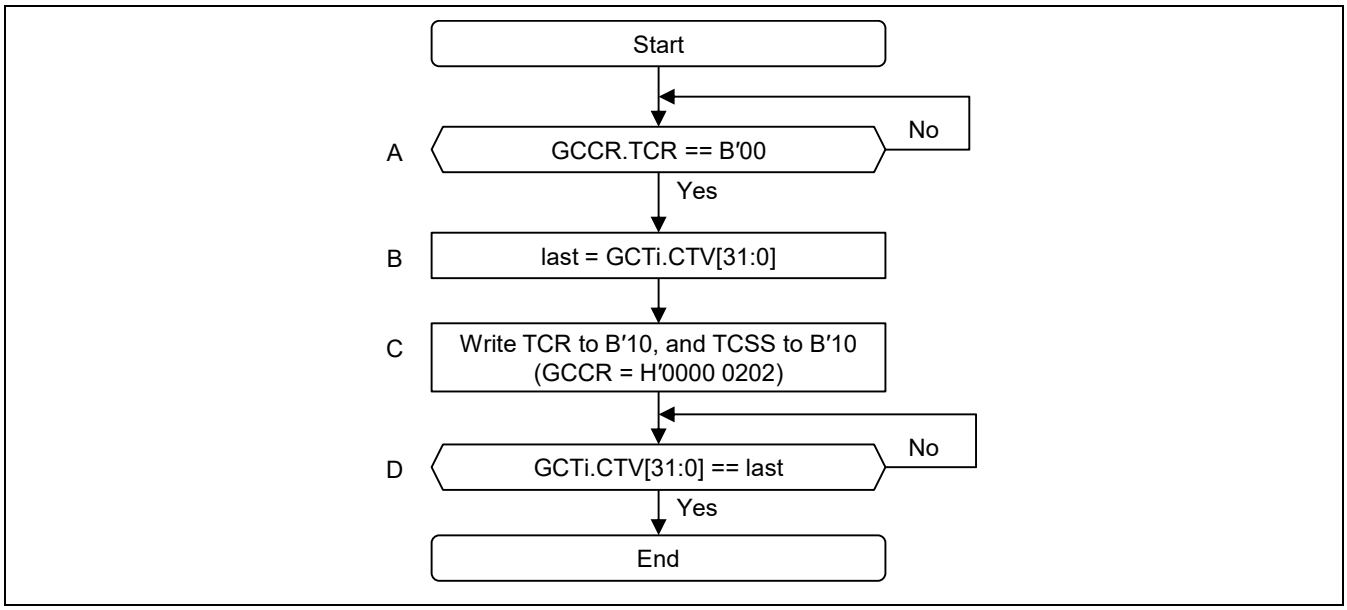


Figure 33A.46 SW flow entering continuous AVTP capture mode

Flow to leave continuous AVTP capture mode:

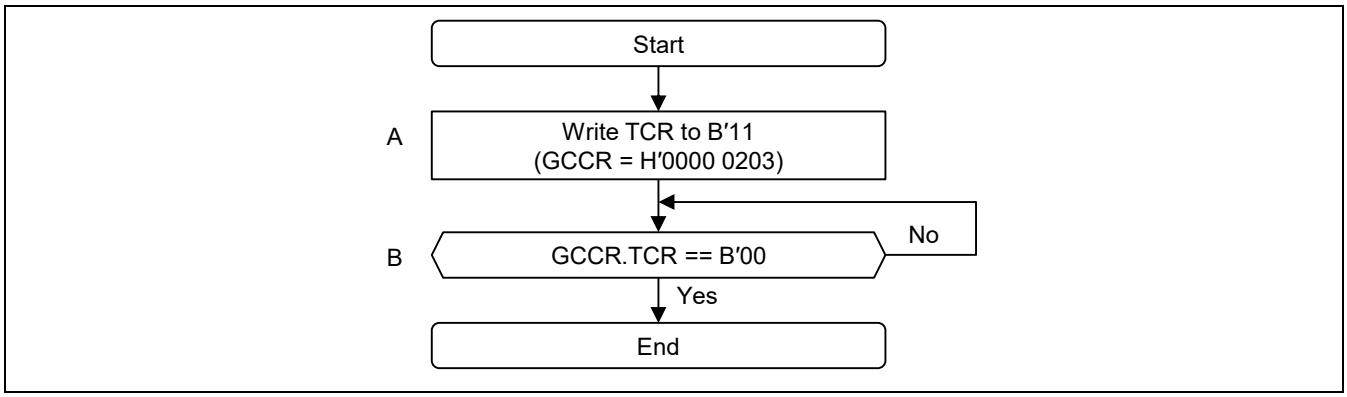


Figure 33A.47 SW flow leaving continuous AVTP capture mode

33A.3.7.5 Support Provided by the gPTP Timer in Transmission and Reception

The timer value described above is used in the time-stamp values captured when start frame delimiters are detected in reception and generated in transmission at PHY interface.

Captured time stamp values for received frames are stored in the corresponding descriptors. Those for transmitted frames are stored with tag information in the time-stamp FIFO. The time stamp values are thus correlated with both transmitted and received frames.

Note that the use of corrected timer values can introduce an error due to the offset correction in the gPTP synchronization procedure.

Due to asynchronous interface between the SFD notification and the timer modules, errors must also be taken into account.

33A.3.8 Support for IEEE 1722

For IEEE 1722, the following two functions are supported.

- Output and capture of values in the IEEE 1722 AVTP (Audio/Video Transport Protocol) presentation time format
- Comparison of IEEE 1722 AVTP presentation time stamps

The 32-bit AVTP time stamp field of IEEE 1722 frames holds the AVTP presentation time when the AVTP time-stamp enable bit in the frame is 1. The AVTP time stamp field is generated from the gPTP timer and is given as seconds (gPTP_seconds) and nanoseconds (gPTP_nanoseconds) according to the following equation.

AVTP time stamp = (gPTP_seconds $\times 10^9$ + gPTP_nanoseconds) modulo 2^{32}

The AVTP presentation time can be read from the gPTP timer capture register (GCTi.CTV). Set the timer capture source select bits in the gPTP configuration control register (GCCR.TCSS) to select the timer value for capture as the AVTP presentation time. Setting the timer control request bits in the gPTP configuration control register (GCCR.TCR[1:0]) to B'11 initiates the capture. The value is obtained by adding the maximum transit time defined in the gPTP maximum transit time register (GMTT.MTTV) to the corrected timer value. The AVTP presentation time wraps around approximately every four seconds.

Note: The AVTP presentation time captured in GCTi.CTV is only valid when the corrected timer value is in synchronization with the Grandmaster clock. That is, the timer increment and timer offset values for the corrected timer value must be adjusted during the synchronization procedure so that the corrected gPTP clock is physically adjusted to match the time kept by the Grandmaster clock.

33A.3.8.1 AVTP capture (HW)

EthernetAVB provides 1 units to capture AVTP based on external events.

Table 33A.16 lists the assignment of the EthernetAVB capture unit.

Table 33A.16 Capture unit assignment

Unit	signal	from	Function
avb_pt_capture[0]	AVB_AVTP_CAPTURE	External	External input

To allow proper detection of the edges of avb_pt_capture[0] signal, a pulse longer than 2 peripheral bus clock cycles should be provided on this input to trigger AVTP capture. Also SW should limit frequency of external capturing signal; period should be at least (6 peripheral bus clock periods + 3 gPTP periods).

There are two variants of capture units in EthernetAVB:

- First one captures AVTP presentation time (including max transit time) and have overflow flagging.
- Second one captures AVTP timer value (without max transit timing) and have prescaler.

The AVTP capture units provides always the first captured value until SW has acknowledged reading of this value.

(1) AVTP presentation time capture unit

EthernetAVB provides one capture unit of this functionality.

When a rising edge is applied to avb_pt_capture[0], AVTP presentation time is captured to GCPT.CPTV and the interrupt flag GIS.PTCF is set to 1.

The captured value includes the configured max transit time value.

Capture of a new AVTP presentation time is suppressed until CPU acknowledges processing of the captured value by setting GIS.PTCF to 0. GIS.PTOF informs about one or more lost capture events.

33A.3.8.2 AVTP compare

EthernetAVB provides 8 independent AVTP compare units. Each unit is able to handle single shot comparison as well as periodic comparison. GSR.PCMi informs about the current mode of unit i. To 4 units (0 to 3) the single shot compare value can provided via AVTP-FIFO to relax timing requirements to application SW.

When the AVTP Presentation Time value has reached or exceeded the configured comparison value the interrupt flag GIS.PTMFi is set to 1. And Comparison unit 0, a pulse of one or four High speed Peripheral clock cycle is applied to AVB_AVTP_MATCH.

The configured max transit time value is not taken in count when comparing.

SW should ensure that configured comparison value is well in future to take into account SW inaccuracy.

SW should ensure that comparison value is not too far in future (more than 2 seconds) with respect to current AVTP timer value to guarantee comparison functionality.

When writing to GCCR, SW can use a 32 bit access if GCCR.TCSS is written to B'11 and all other bits not required for comparison value programming are written to 0.

(1) Single shot compare

An AVTP compare unit used in single shot mode generates exactly one match after CPU programs the comparison value.

CPU should use this flow to program absolute comparison values in single shot mode:

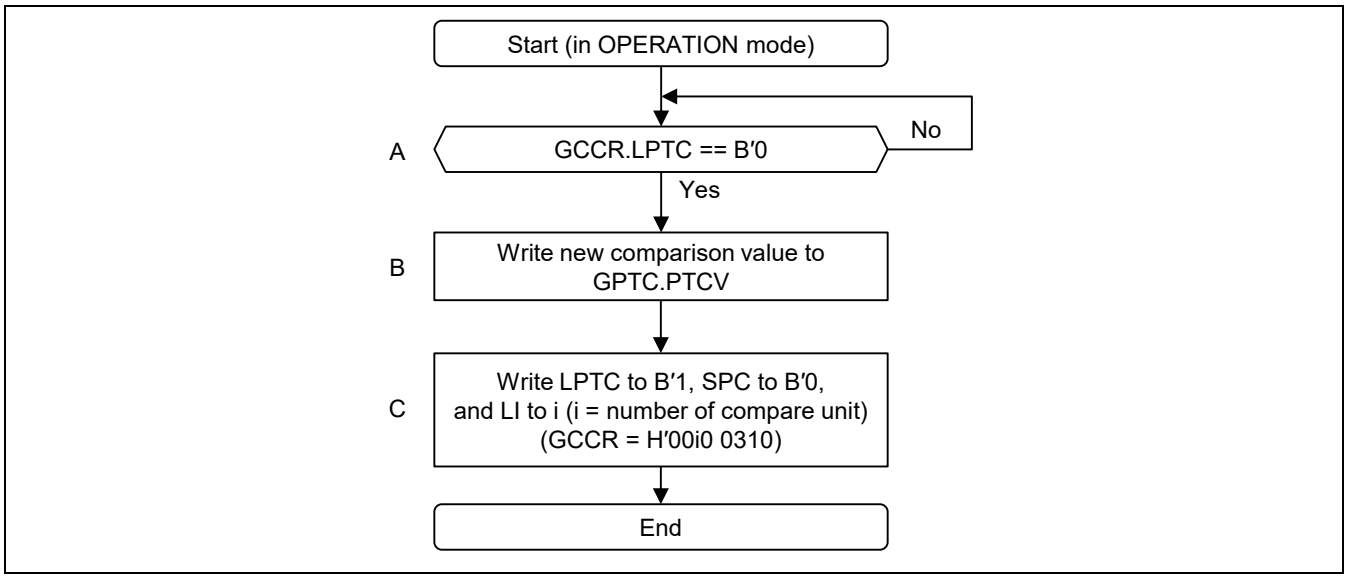


Figure 33A.48 SW flow to program a single shot compare value

(2) Periodic compare

An AVTP compare unit used in periodic compare mode generates matches of configured period until CPU disables periodic mode. Optional it is possible to define the initial phase before repetition starts.

CPU should use this flow to start periodic compare mode or to change period value:

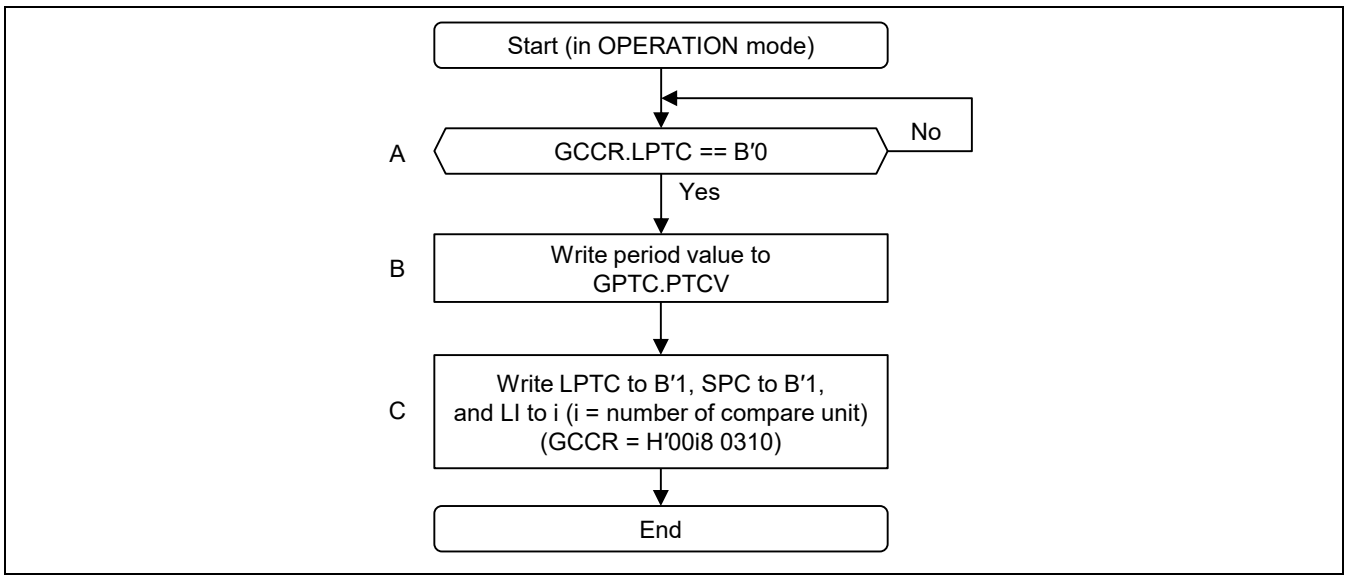


Figure 33A.49 SW flow to program period value (without phase relation)

Some application may require phase relation between periodical match events generated by different units. In this case the next flow can be used to enter periodic compare mode with phase relation. A compare unit will only start a period when there is no pending comparison. If the absolute starting point of all units (box B in flow) is well in future the period of all units start at the same time (e.g. 48 kHz on unit 1 and 96 kHz on unit 2).

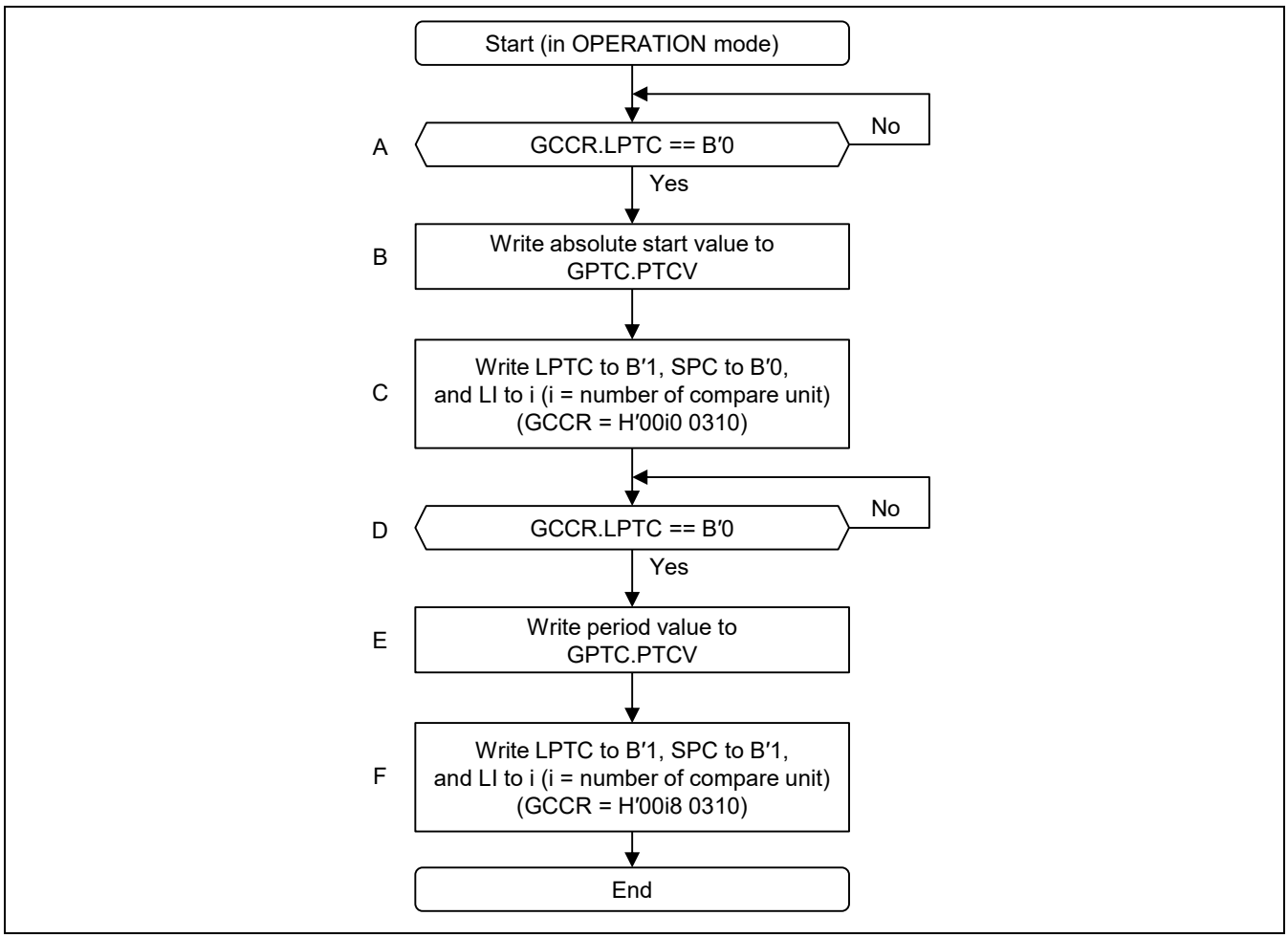


Figure 33A.50 SW flow to program period value (with phase relation)

The periodic mode is left by entering single-shot mode. Do not write new comparison value in GPTC.PTCV for changing mode as shown in flow below, this value will not be used as new comparison value.

CPU should use this flow to leave periodic compare mode:

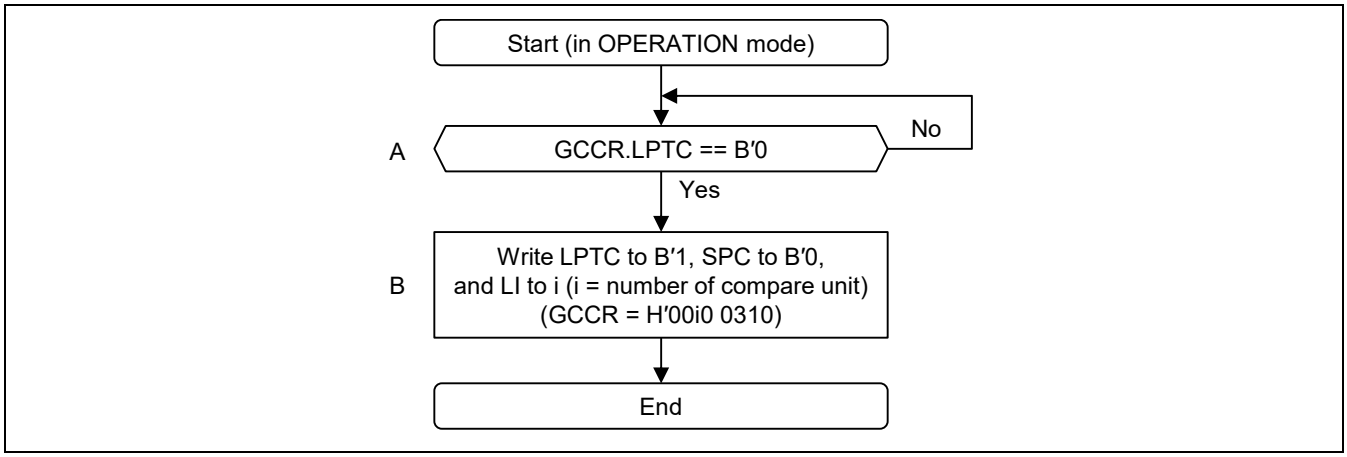


Figure 33A.51 SW flow to end period mode

The last periodical comparison happens after Point B in SW flow. EthernetAVB leaves periodic mode after last periodical comparison happens. This is flagged by GSR.PCMi. Comparison unit can only be reused after GCR.PCMi is 0.

(3) FIFO based single-shot comparison

Some comparison units provide the possibility to use timestamps from a FIFO. To use this possibility CPU writes AVTP timestamp to GPTFi instead of GPTC. By writing to GPTFi the value is added to FIFO, no load is required but CPU needs to check if AVTP-FIFO is able to accept new values.

FIFO usage may reduce CPU load because CPU can program a bunch of timestamps at same time.

When there is no comparison ongoing in AVTP compare unit, the next value from AVTP-FIFO is loaded and comparison starts. If the FIFO is empty no value is loaded and no further match event is generated.

When moving from single-shot comparison to FIFO based single-shot comparison, the 1st FIFO value is immediately loaded independent of an ongoing comparison.

By reading GSR.AFFLi CPU can observe number of pending timestamps.

CPU should use this flow to add timestamps to the AVTP-FIFO of compare unit. If FIFO depth is insufficient, FIFO size should be extended in SW (box E).

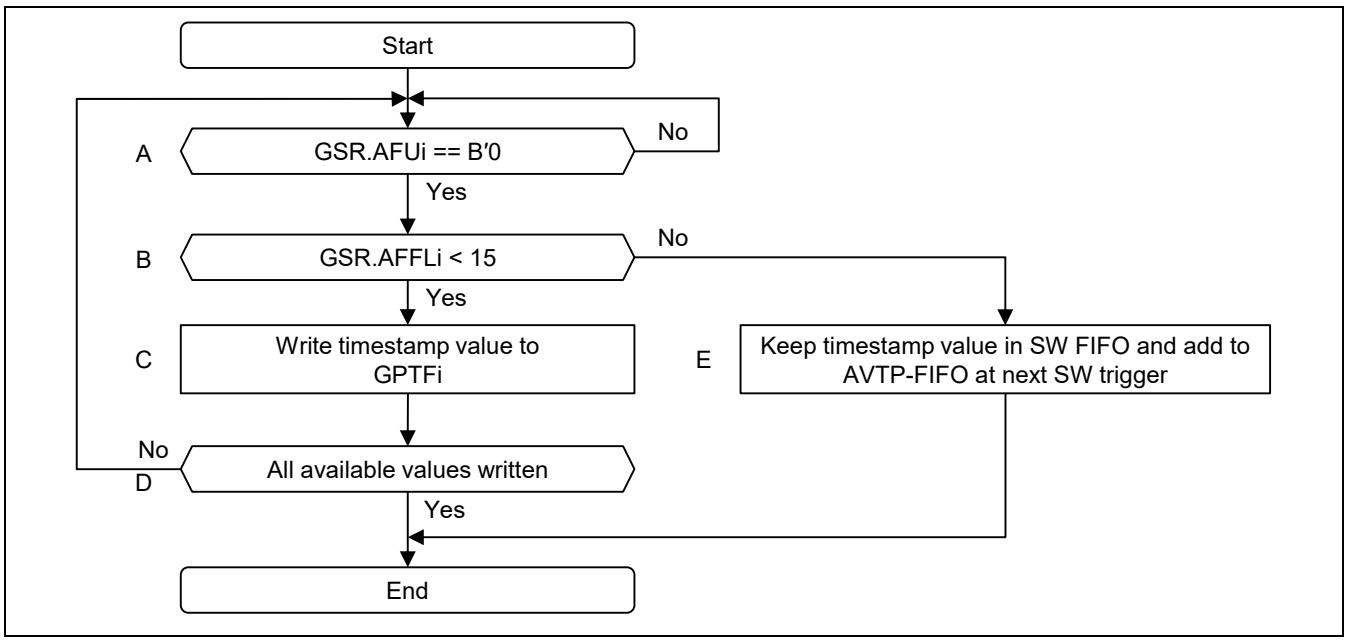


Figure 33A.52 SW flow to add timestamp to AVTP-FIFO

It is recommended to combine box A and B into one access to limit accesses to GSR register.

33A.3.8.3 gPTP timer functionality in CONFIG mode

When CCC.GAC is 1, it is possible to use some gPTP functions in CONFIG mode. Because the frame handling mechanisms are not available in CONFIG mode, usage of gPTP support is restricted. Only basic timer functions of gPTP support can be used:

- gPTP timer is running based on selected clock source (CCC.CSEL),
- Offset and increment value can be configured and adjusted
- SW capture function (timer, corrected timer, AVTP)
- HW capture function (AVTP)
- SW compare function

When AVTP FIFO functionality is used in CONFIG mode, there is no error flagging by ESR.ET = B'1011 available. CPU can use error flagging by external RAM protection directly, there are no other read accesses to RAM by EthernetAVB.

33A.3.9 Flow Control

The EthernetAVB does not support flow control in the specification. Flow control is only effective when transmitting and receiving only normal (non-AVB) packets.

The E-MAC supports flow control for full-duplex operation in compliance with the IEEE 802.3 standards. This flow control is applicable to both reception and transmission. In regard to the transmission of PAUSE frames, flow control operates in the following ways.

(1) PAUSE Frame Transmission

PAUSE frames can also be transmitted in response to software operations. Writing a timer value to the manual PAUSE frame register (MPR) starts the transmission of a PAUSE frame. This only causes the transmission of one PAUSE frame.

(2) PAUSE Frame Reception

After reception of a PAUSE frame, transmission of the next frame does not proceed until the time indicated by the Timer value elapses. However, transmission of a frame currently being transmitted continues. PAUSE frames are only received while the RXF bit in the E-MAC mode register (ECMR) is set to 1. The number of received PAUSE frames is counted.

(3) PAUSE Frames with the Timer Value 0

The setting of the 0-time PAUSE frame enable bit (ECMR.ZPF) enables or disables the reception of PAUSE frames with the TIME parameter value 0.

- When control of PAUSE frames with the TIME parameter value 0 is disabled

  PAUSE frames with the TIME parameter value 0 are not transmitted. Received PAUSE frames with the TIME parameter value 0 are discarded.

33A.3.10 Magic Packet Detection

The E-MAC has a Magic Packet detection function. This function provides a facility for host devices and other sources to start other peripheral devices connected to a LAN. A peripheral device that handles Magic Packets starts itself in response to receiving a Magic Packet.

When a Magic Packet is detected, data from broadcast packets that were previously being received are stored in the FIFO and the E-MAC is notified of the receiving status. To return to normal operation from the associated interrupt processing, the E-MAC and AVB-DMAC must be initialized by using the operating mode configuration bit in the AVB-DMAC mode register (CCC.OPC) to set the operating mode to reset mode.

Magic Packets are received regardless of the destination address. As a result, the AVB_MAGIC pin is only enabled in the case of a match with the destination address specified in the Magic Packet.

The procedure for using the Magic Packet detection function with this LSI chip is as follows.

1. Use the various interrupt enabling and masking registers to disable the output of interrupts from interrupt sources.
2. Set the Magic Packet detection enable bit in the E-MAC mode register (ECMR.MPDE).
3. Set the Magic Packet detection interrupt enable bit in the E-MAC interrupt enable register (ECSIPR.MPDIP) to enable the interrupt.
4. Place the CPU in sleep mode as required.
5. An interrupt is conveyed to the CPU on detection of a Magic Packet.
6. The AVB_MAGIC pin notifies connected devices of Magic Packet detection.

Note: The Magic Packet detection interrupt status can be read in the E-MAC status register (ECSR.MPD). The bit can be cleared by setting the E-MAC status register Magic Packet™ detection bit (ECSR.MPD) to 1.

But EthernetAVB can't detect 2nd or later Magic Packet™ and the AVB_MAGIC pin can be negated though the bit is cleared.

The AVB_MAGIC pin can be negated and EthernetAVB can detect Magic Packet™ again according to below way.

1) Hardware reset — set reset pin in the RZ/G1C to reset signal.
2) Software reset — set mstp/srst register for EthernetAVB to software reset mode.
3) Software reset register in AVB — set AVB DMAC mode register Operating Mode Configuration bits (CCC.OPC) to reset mode.

33A.3.11 Interrupts

The EthernetAVB is capable of generating one interrupt.

The interrupts of EthernetAVB are indicated by individual flags DIS, EIS, RISi, TIS, and GIS. Each interrupt is controllable by the corresponding interrupt enable bit. The status flags are independent from this enable bits.

Additionally grouped interrupt status available in ISS and EIS.QFS. The summary status allows CPU to locate the interrupt source with a minimum number of read accesses to EthernetAVB.

EthernetAVB interrupts are combined to 4 groups of interrupt lines for request an interrupt service by CPU. Interrupt requests in group 0 and 1 are only generated in OPERATION mode. Interrupt requests in group 2 are only generated in OPERATION mode and in CONFIG mode if gPTP support is enabled (CCC.GAC). Interrupt request on line 3 depends on E-MAC configuration and can be generated in CONFIG, OPERATION and STANDBY mode.

Interrupt lines are level output and each line is asserted when at least one of the interrupt status registers bits belonging to the group associated with that line is set to 1, and the corresponding enable bit in the related interrupt control register is also set to 1.

For ISS bits the combined flag/enable is used. The green dots in detailed interrupt figures in detailed interrupt line description illustrates the point where status information for ISS is taken.

33A.3.11.1 Concurrent interrupt enable support

The interrupt enable bits can be directly modified by writing the interrupt control registers (xxC.yyE). If concurrent processes enable/disable interrupts located in same interrupt control register inter-process communication is required. To reduce SW overhead there are dedicated registers available controlling conflict free enable/disable of interrupts.

To enable an interrupt CPU should write 1 to the corresponding bit (xxE.yyS) in the enable register. Because written 0 have no effect, there is no side effect to concurrent processes.

To disable an interrupt CPU should write 1 to the corresponding bit (xxD.yyD) in the disable register. Because written 0 have no effect, there is no side effect to concurrent processes.

The current interrupt enable status is readable in xxC.yyE.

Grouping of interrupts for each interrupt line is as described in following sub-chapters.

33A.3.11.2 Group 0 (Data related interrupts)

This group consists on:

Frame received interrupts RIS0.FRFr (for each received frame stored in URAM)
Receive warning interrupts RIS1.RWFr (when Unread Frame Counter reaches warning level)
Descriptor processed interrupts RIS3.RDPFr (for reception)
Frame transmitted interrupts TIS.FTFt (for completion of frame transmission by E-MAC)
Descriptor processed interrupts TIS.TDPFr (for transmission)
Descriptor processed interrupts DIS.DPFi (for reception and transmission)

By reading ISS, CPU get an overview of all data related interrupts (ISS.FRM, ISS.RWM, ISS.DPMi, ISS.FTM).

Interrupt group 0 consists on these 24 interrupt lines:

Line0_Rx[17:0]
Line0_Tx[3:0]
Line0_DiA
Line0_DiB

(1) Reception interrupts

There are 18 dedicated interrupt lines flagging frame reception. For the queue full flag it is configurable by CIE.RQFM if these notification are part of the queue specific reception interrupt lines or part of the error interrupt lines (group 1).

There is a common interrupt enable (CIE.CRIE) for all reception lines.

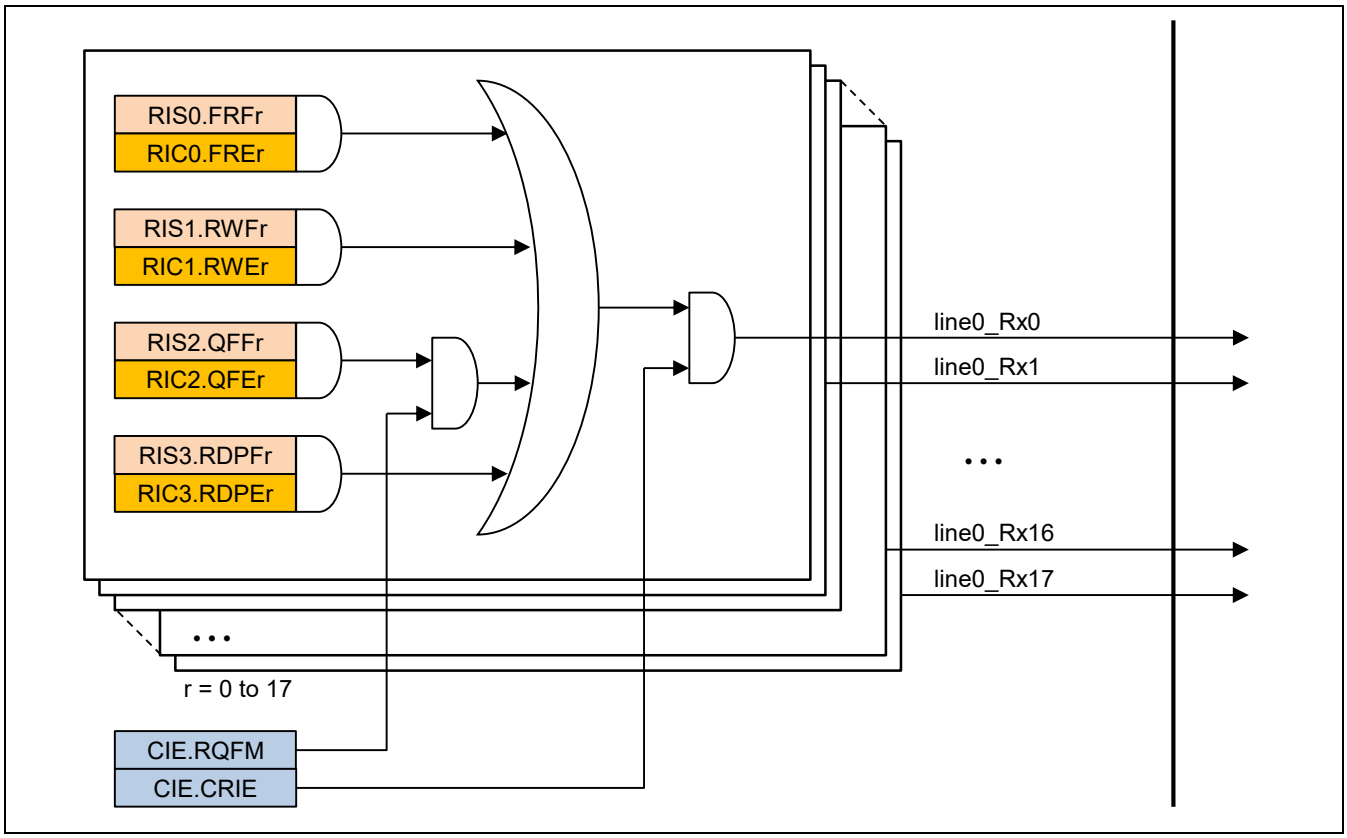


Figure 33A.53 Interrupt group 0, reception interrupt lines

(2) Transmission interrupts

There are 4 dedicated interrupt lines flagging frame transmission.

There is a common interrupt enable (CIE.CTIE) for all reception lines.

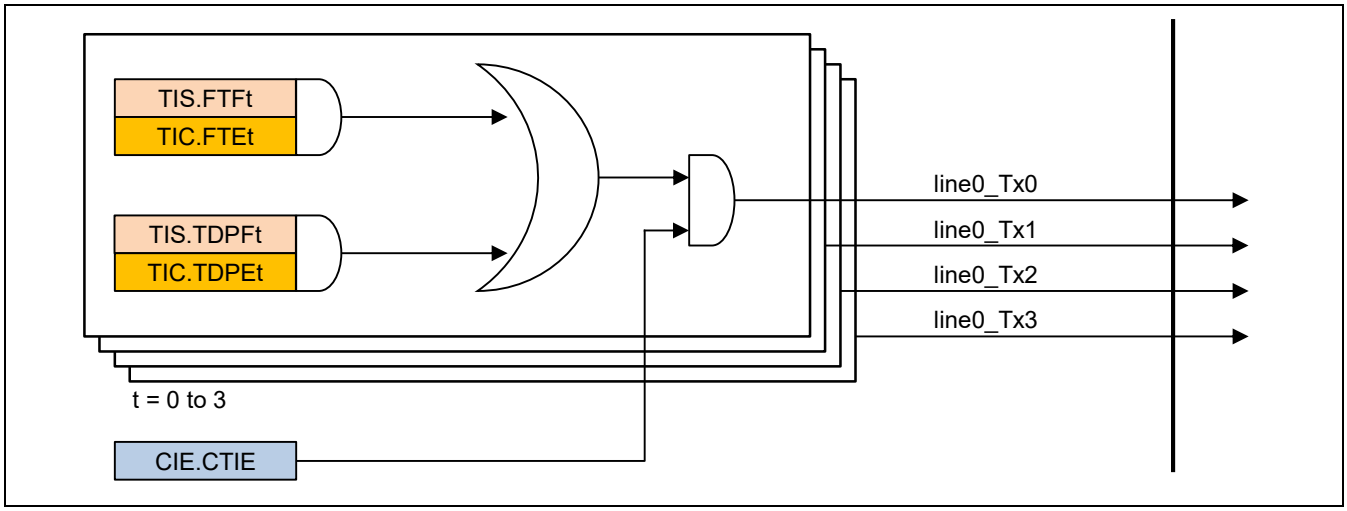


Figure 33A.54 Interrupt group 0, transmission interrupt lines

(3) Descriptor and merged interrupts

There are 2 interrupt lines flagging descriptor interrupts. Line line0_DiA has also the capability to generate a merged data interrupt (controlled by CIE.CL0M).

Descriptor interrupt 1 is not available as common descriptor interrupt; this descriptor interrupt is split into queue specific descriptor interrupts.

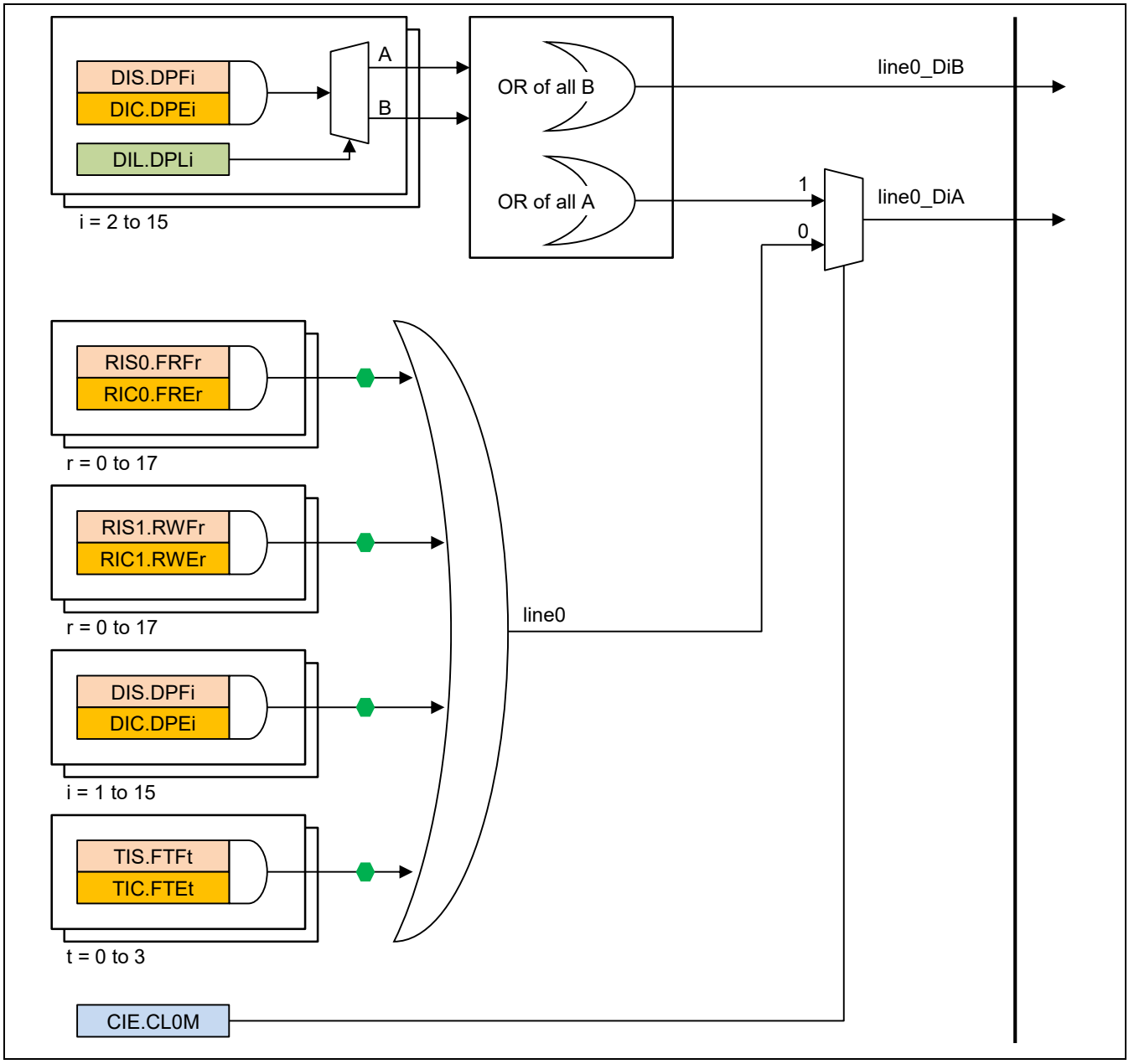


Figure 33A.55 Interrupt group 0, common descriptor and merged interrupt lines

33A.3.11.3 Group 1 (Error related interrupts)

This group consists on:

Tx-Buffer full interrupt EIS.TBFF (when delaying fetching of transmit frame)
Interrupt for E-MAC Status FIFO overwrite (EIS.MFFF)
Interrupt for Timestamp FIFO overrun (EIS.TFFF)
Interrupts for CBS limits (EIS.CULF1, EIS.CULF0, EIS.CLLF1, EIS.CLLF0)
Interrupt for separation filtering error (EIS.SEF)
Interrupt for queue error (error while processing receive or transmit queue) (EIS.QEF)
Interrupt for transmission error detected by E-MAC (EIS.MTEF, EIS.MREF)
Rx-FIFO full interrupt RIS2.RFFF (when Rx-FIFO overflows)
Receive queue full interrupts RIS2.QFFr (when no sufficient space is in receive queue)

By reading EIS, CPU get an overview of all error interrupts. Additionally ISS.EM informs about pending error related interrupt.

Interrupt group 1 consists on these 2 interrupt lines:

Line1_A
Line1_B

For the queue full flag it is configurable by CIE.RQFM if these notification are part of the queue specific reception interrupt lines or part of the error interrupt line line1_A.

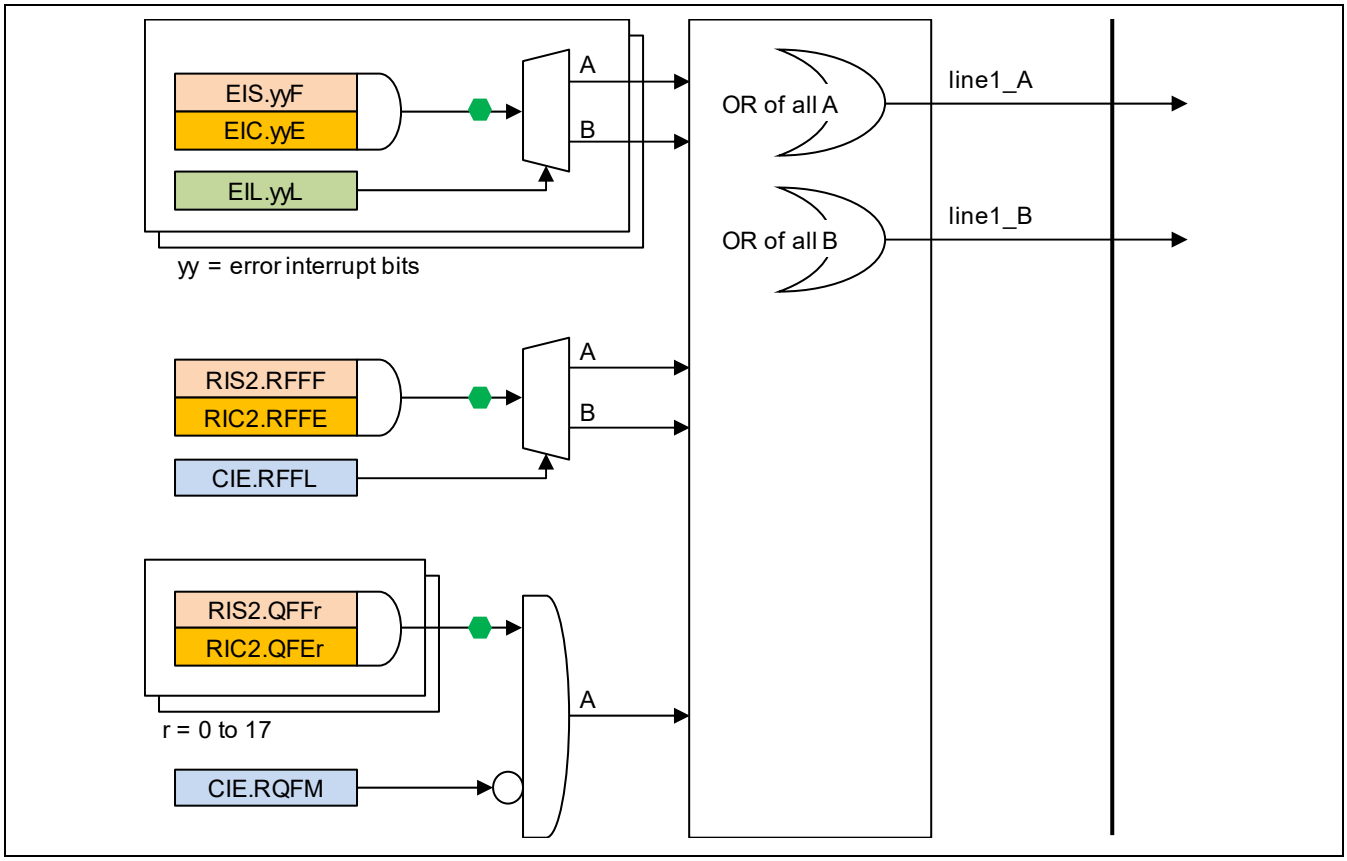


Figure 33A.56 Interrupt group 1, error interrupt lines

The abbreviation **yy** in figure indicates error interrupts: TBF, MFF, TFF, CULFc, CLLFc, SE, QE, MTE, and MRE.

33A.3.11.4 Group 2 (Management related interrupts)

Reception

Rx-FIFO Warning interrupt RIS1.RFWF (Rx-FIFO has reached configured warning level)

Transmission

E-MAC status FIFO warning interrupt TIS.MFWF
E-MAC Status FIFO updated interrupt TIS.MFUF
Timestamp FIFO warning interrupt TIS.TFWF
Timestamp FIFO updated interrupt TIS.TFUF

gPTP

AVTP time captured interrupt GIS.ATCFi
AVTP presentation target matched interrupt GIS.PTMFi
AVTP presentation time overrun interrupt GIS.PTOF (when external trigger before old value is processed)
AVTP presentation time captured interrupt GIS.PTCF

By reading ISS, CPU get an overview of all management related interrupts (ISS.RFWM, ISS.MFWM, ISS.MFUM, ISS.TFWM, ISS.TFUM, ISS.CGIM).

Interrupt group 2 consists on these 2 interrupt lines:

Line2_A
Line2_B

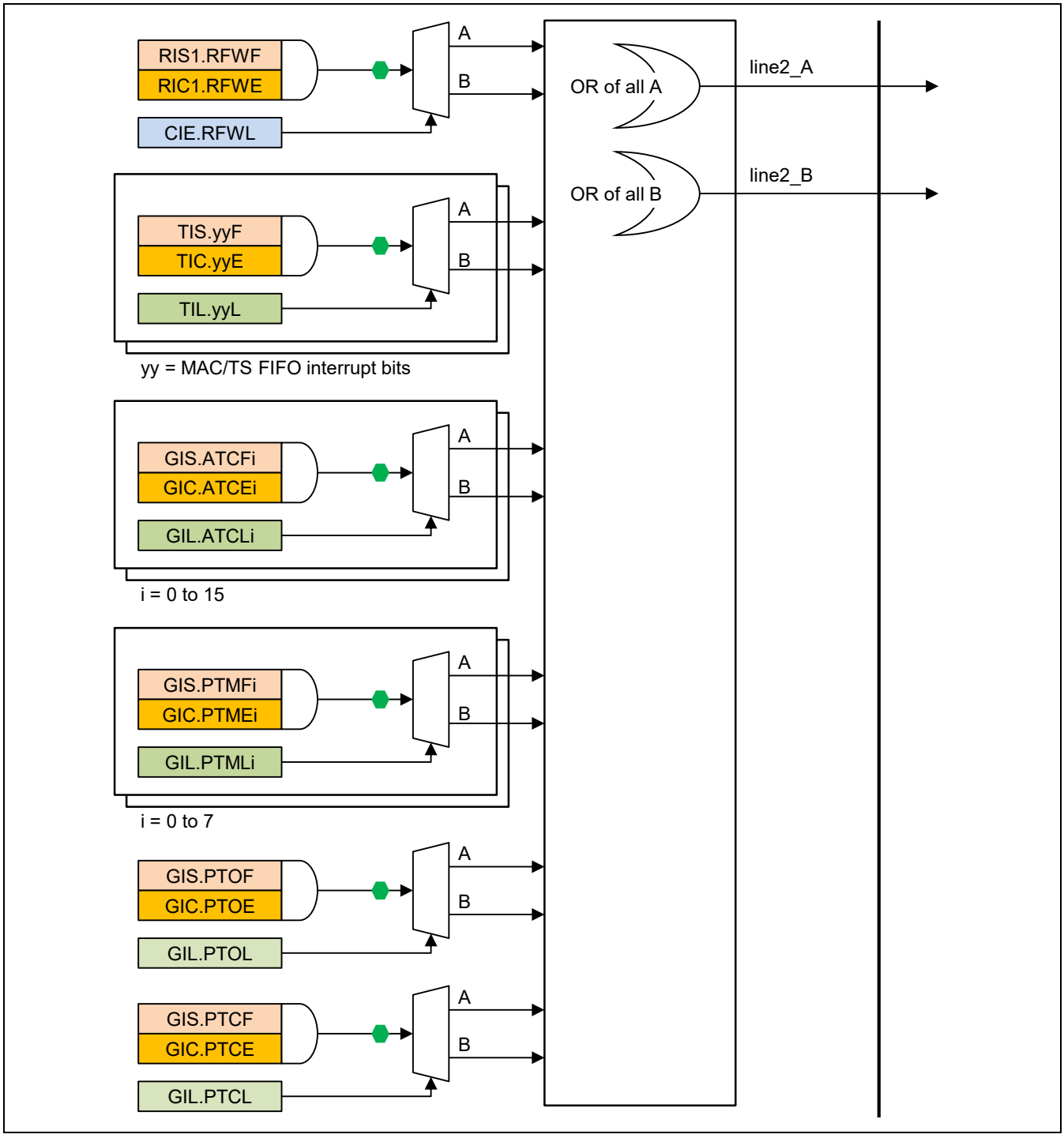


Figure 33A.57 Interrupt group 2, management interrupt lines

The abbreviation **yy** in figure indicates error interrupts: MFW, MFU, TFW, and TFU.

33A.3.11.5 Line 3 (E-MAC interrupt)

The E-MAC interrupt is conveyed when the E-MAC interrupt source is generated.

The general error interrupt state can be checked by reading the E-MAC interrupt summary bit in the interrupt summary status register (ISS.MS).

33A.3.12 Flows of Operations

33A.3.12.1 Flow of E-MAC Initialization

Figure 33A.58 shows the flow of E-MAC initialization (for AVB mode and full-duplex operation).

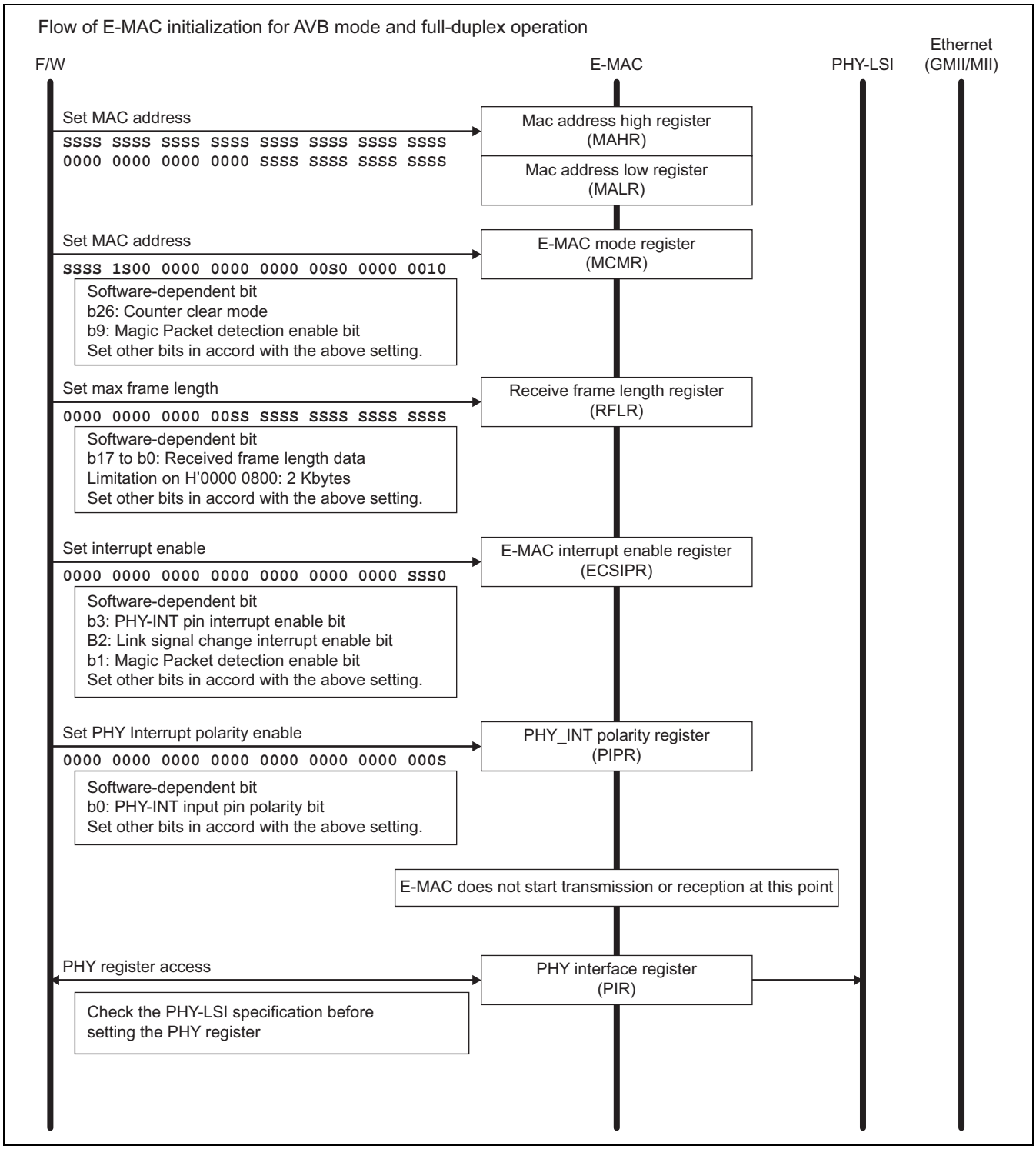


Figure 33A.58 Flow of E-MAC Initialization (for AVB Mode and Full-Duplex Operation)

33A.3.12.2 Flow of AVB-DMAC Initialization

Figure 33A.59 shows the flow of AVB-DMAC initialization (for AVB mode and full-duplex operation).

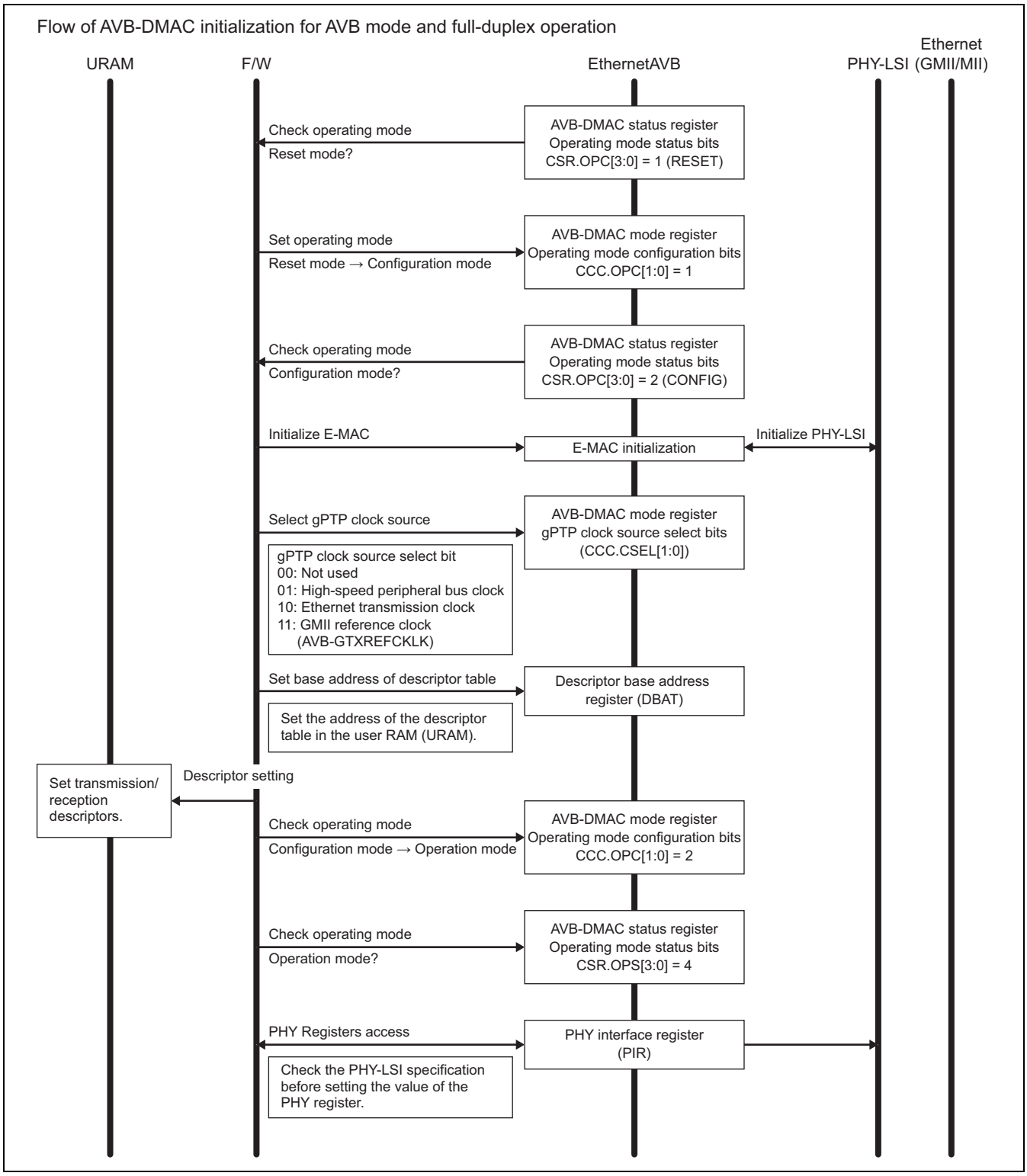


Figure 33A.59 Flow of AVB-DMAC Initialization (for AVB Mode and Full-Duplex Operation)

33A.3.12.3 Flow for the AVB-DMAC in Reception

Figure 33A.60 shows the flow for the AVB-DMAC in reception (in AVB mode and full-duplex operation).

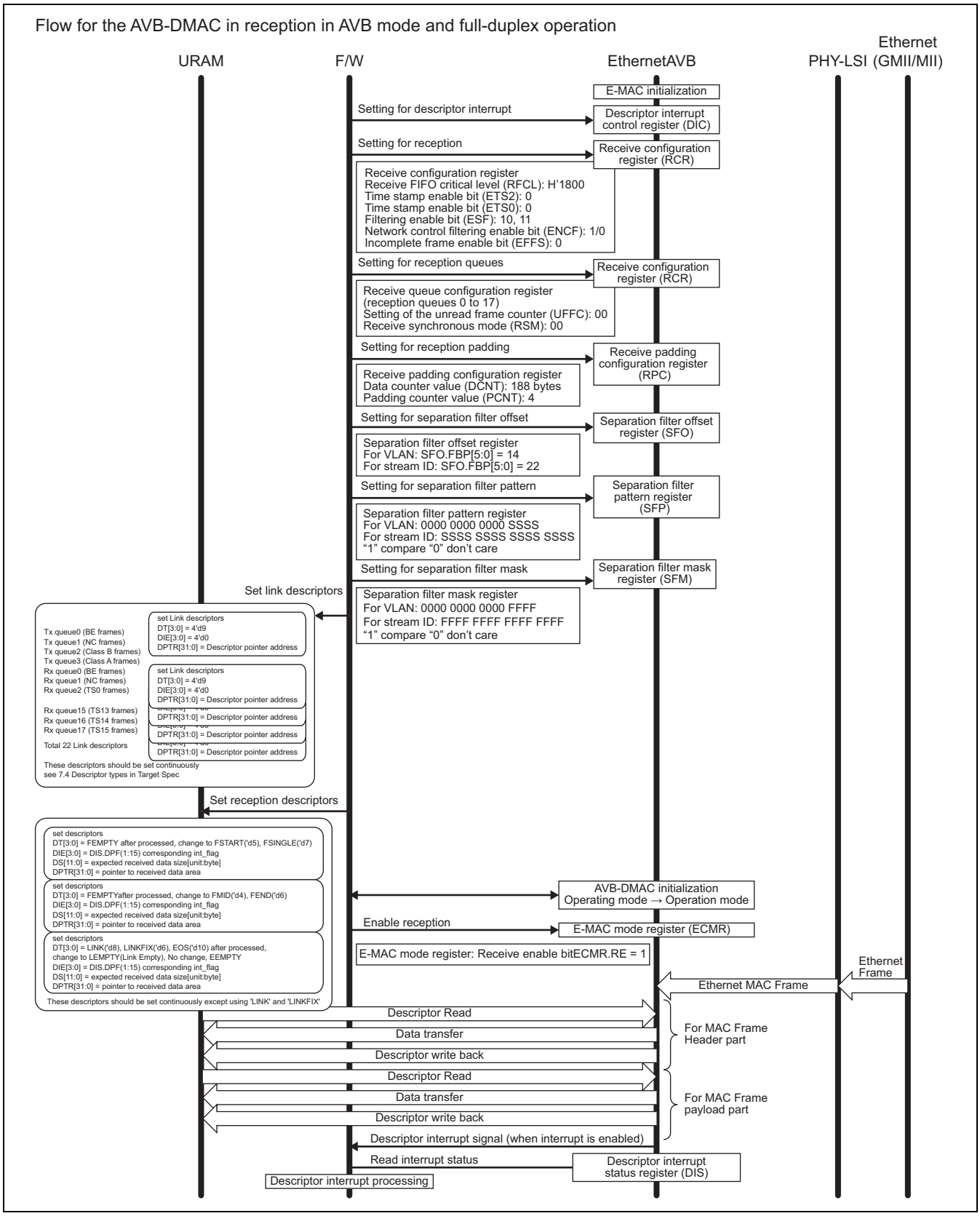


Figure 33A.60 Flow for the AVB-DMAC in Reception (in AVB Mode and Full-Duplex Operation)

33A.3.12.4 Flow for the AVB-DMAC in Transmission

Figure 33A.61 shows the flow for the AVB-DMAC in transmission (in AVB mode and full-duplex operation).

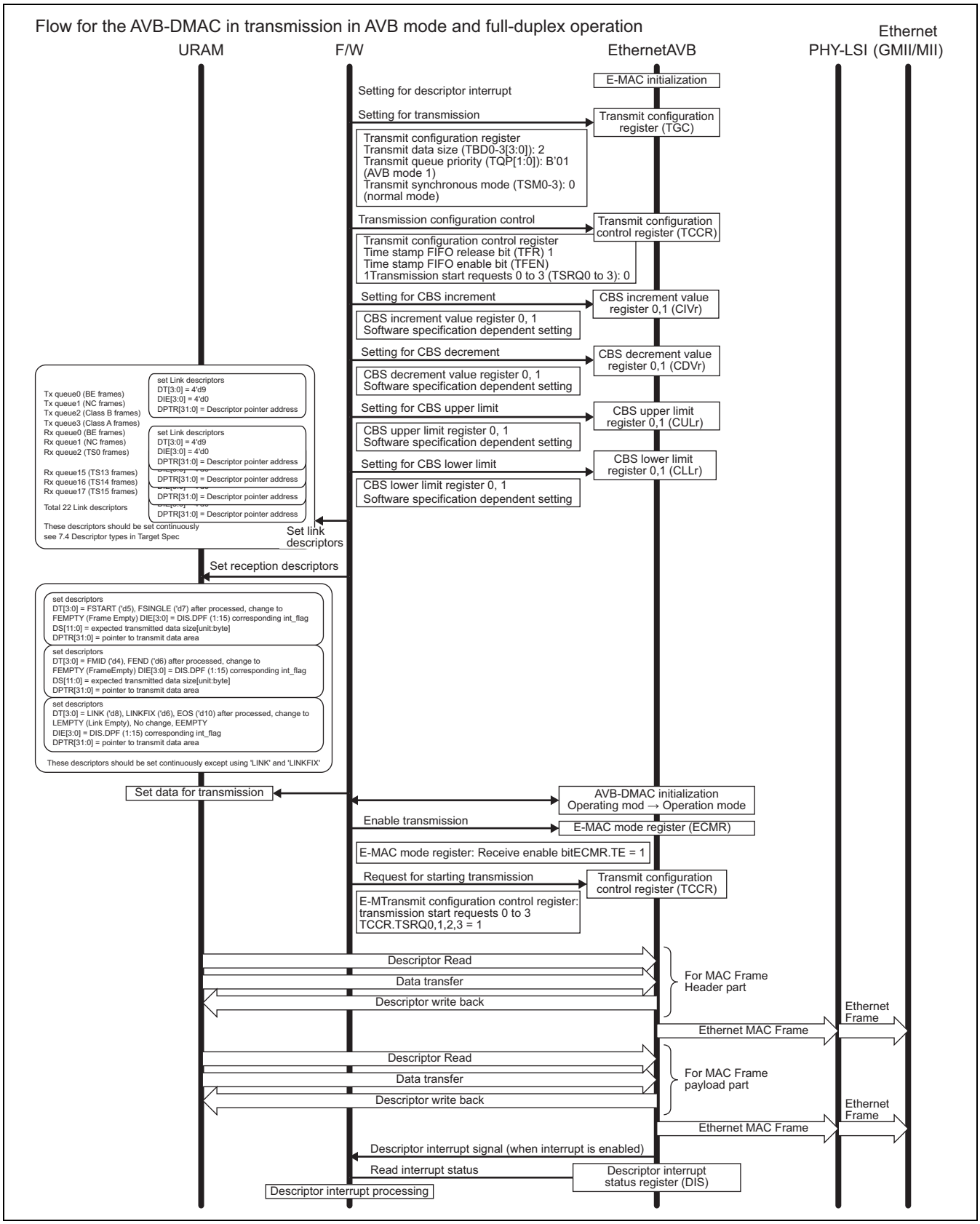


Figure 33A.61 Flow for the AVB-DMAC in Transmission (in AVB Mode and Full-Duplex Operation)

33A.3.12.5 Flow for Stopping AVB-DMAC Operation in Reception

Figure 33A.62 shows the flow for stopping AVB-DMAC operation in reception (normal, common to all modes).

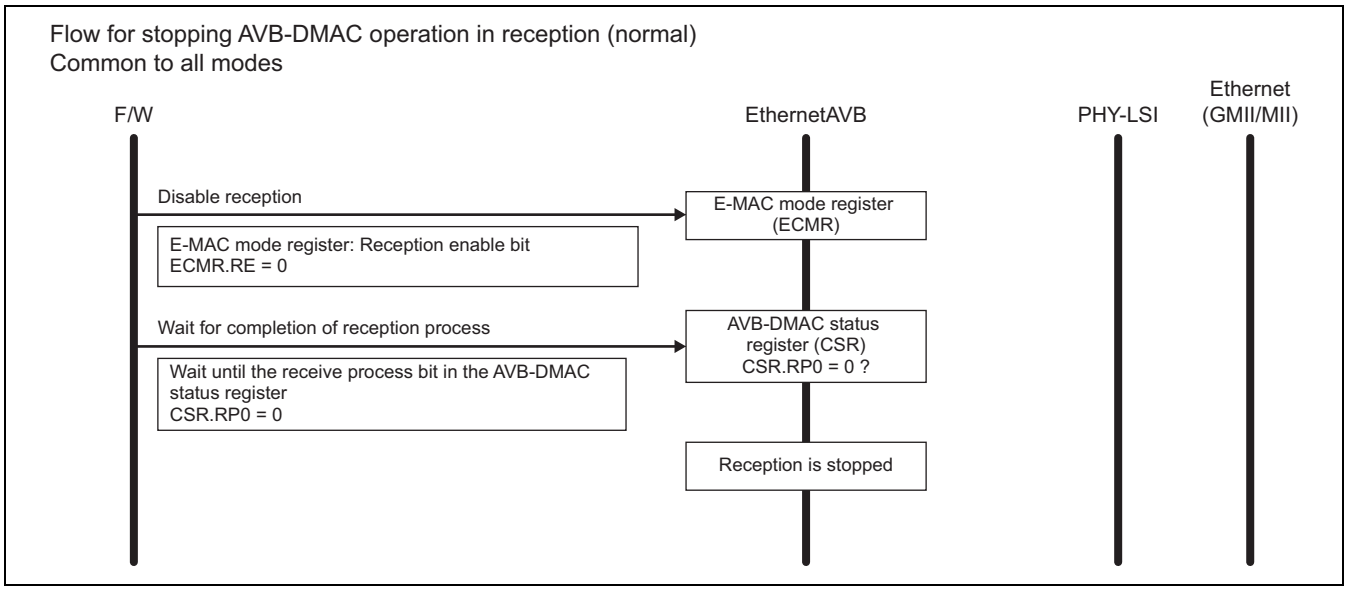


Figure 33A.62 Flow for Stopping AVB-DMAC Operation in Reception (Normal, Common to All Modes)

33A.3.12.6 Flow for Stopping AVB-DMAC Operation in Transmission

Figure 33A.63 shows the flow for stopping AVB-DMAC operation in transmission (normal, common to all modes).

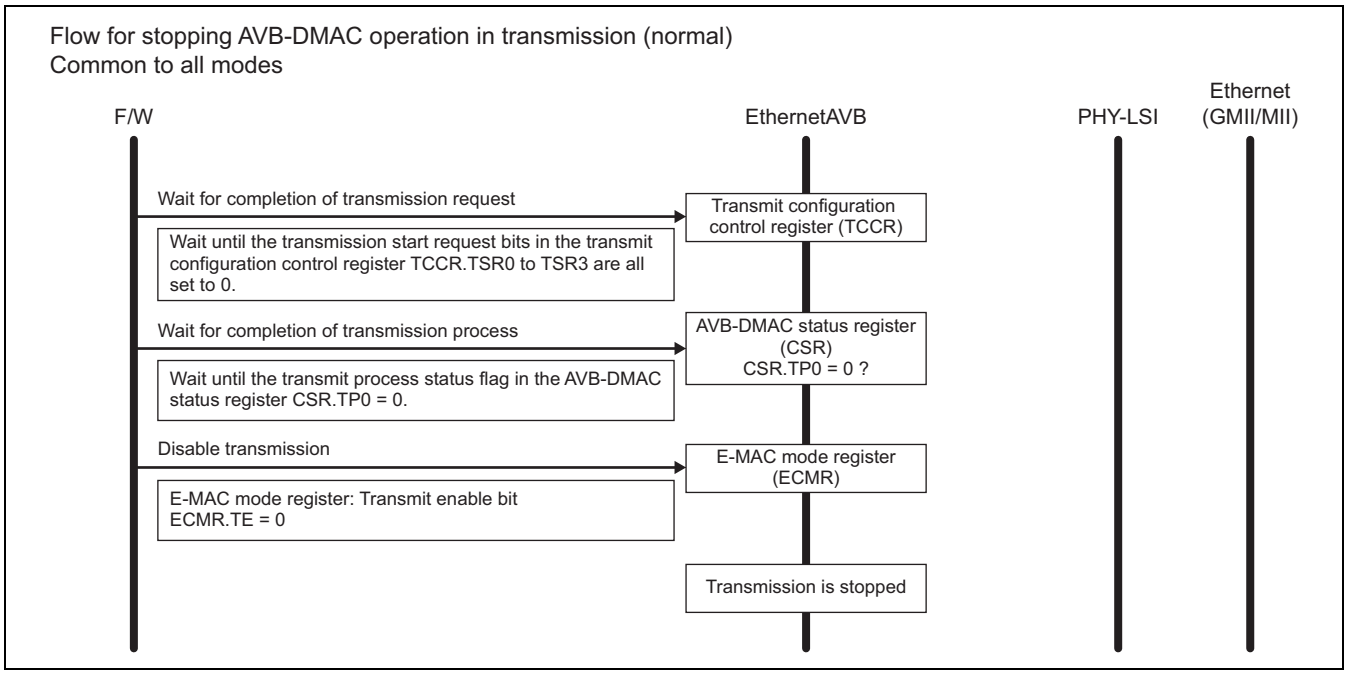


Figure 33A.63 Flow for Stopping AVB-DMAC Operation in Transmission (Normal, Common to All Modes)

33A.3.12.7 Flow for Stopping and Resetting the AVB-DMAC

Figure 33A.64 shows the flow for stopping and resetting the AVB-DMAC (normal, common to all modes).

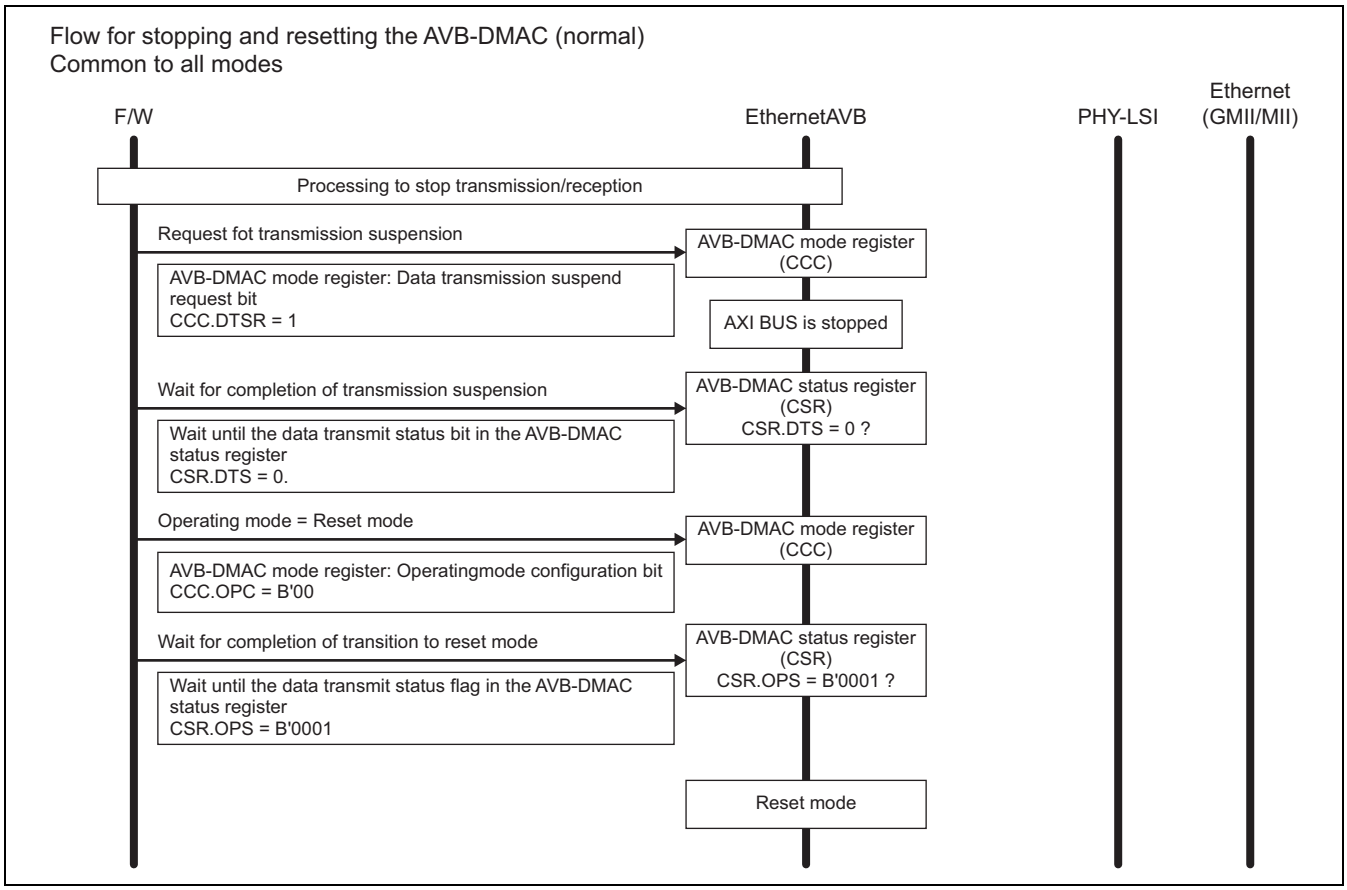


Figure 33A.64 Flow for Stopping and Resetting the AVB-DMAC (Normal, Common to All Modes)

33A.3.12.8 Flow for Emergency Stopping the AVB-DMAC

Figure 33A.65 shows the flow for emergency stopping the AVB-DMAC (normal, common to all modes).

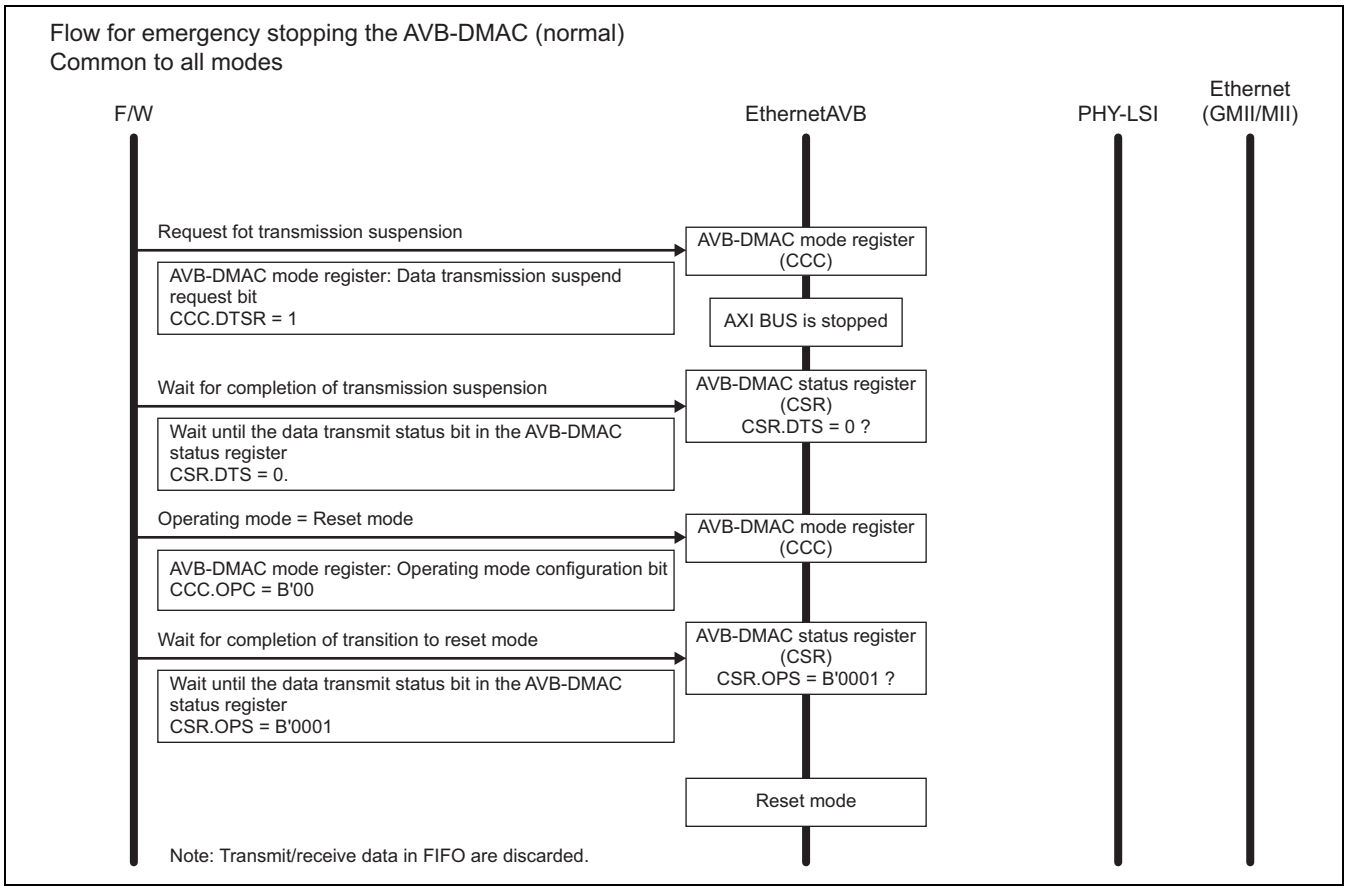


Figure 33A.65 Flow for Emergency Stopping the AVB-DMAC (Normal, Common to All Modes)

33A.3.12.9 Flow of gPTP Initialization

Figure 33A.66 shows the flow of gPTP initialization (normal, common to all modes).

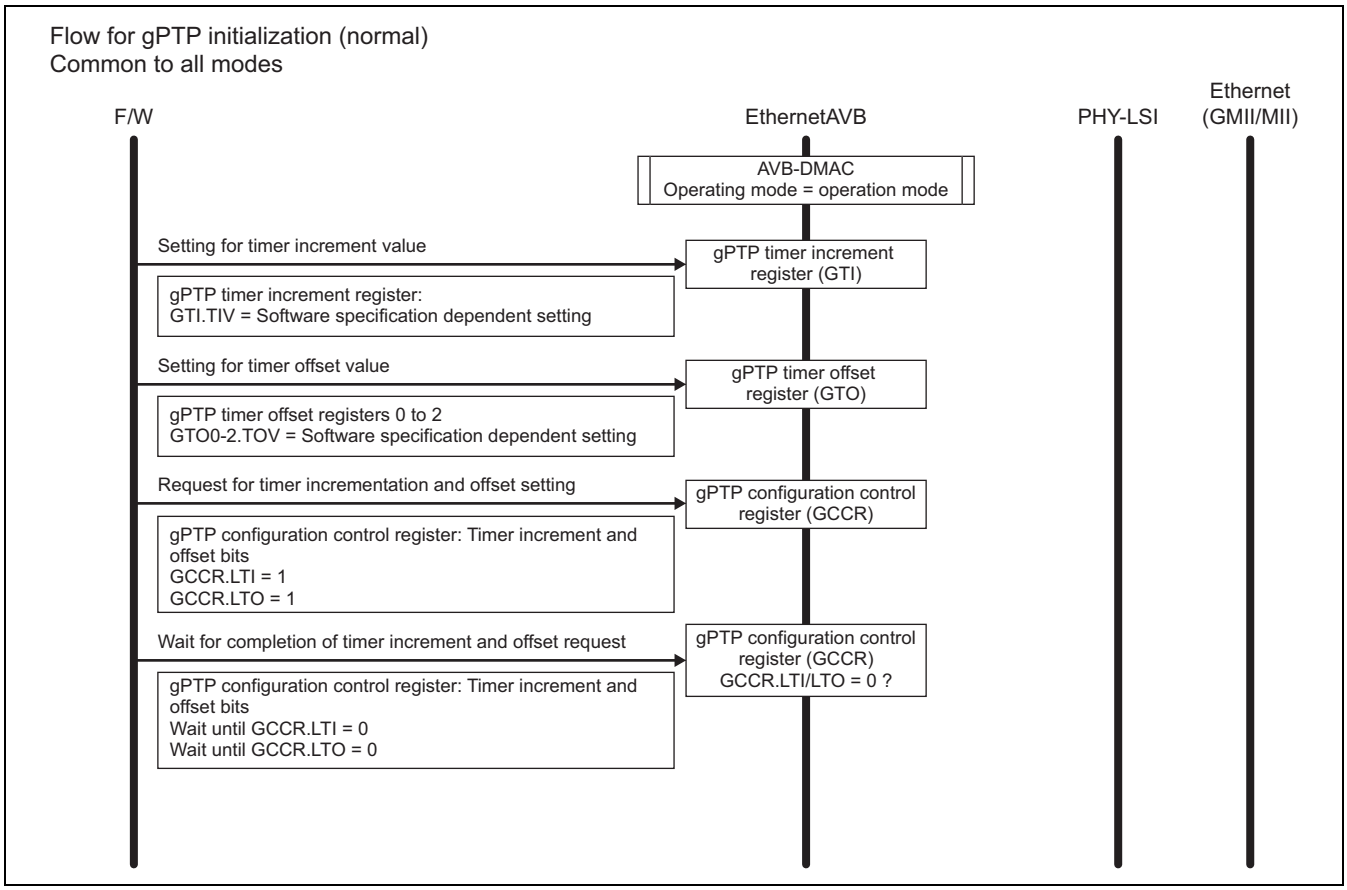


Figure 33A.66 Flow of gPTP Initialization (Normal, Common to All Modes)

33A.3.12.10 Flow of gPTP Time Stamping in Transmission

Figure 33A.67 shows the flow of gPTP time stamping in transmission (normal, common to all modes).

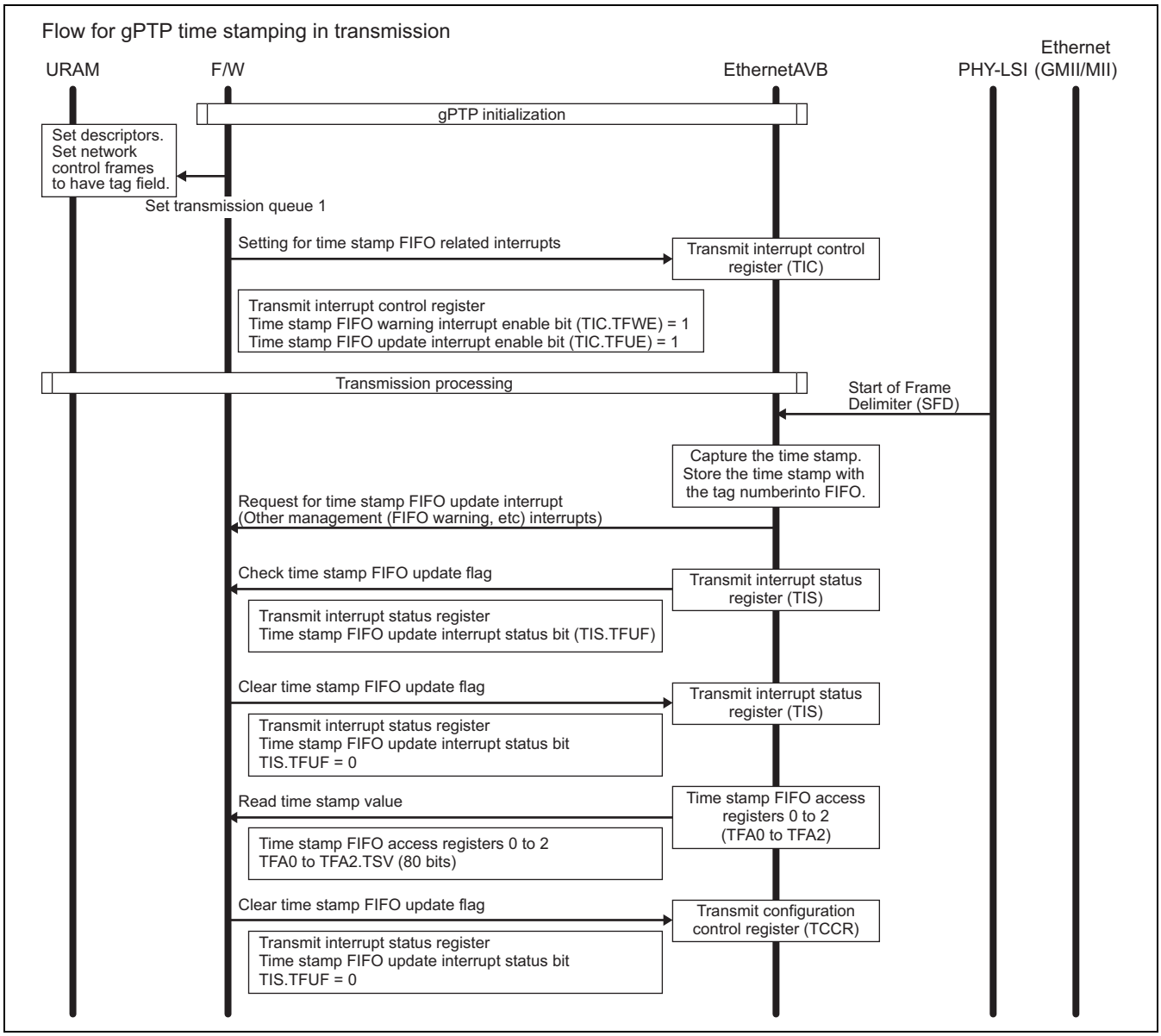


Figure 33A.67 Flow of gPTP Time Stamping in Transmission (Normal, Common to All Modes)

33A.3.12.11 Flow of gPTP Time Stamping and Synchronization in Reception

Figure 33A.68 shows the flow of gPTP time stamping and synchronization in reception (normal, common to all modes).

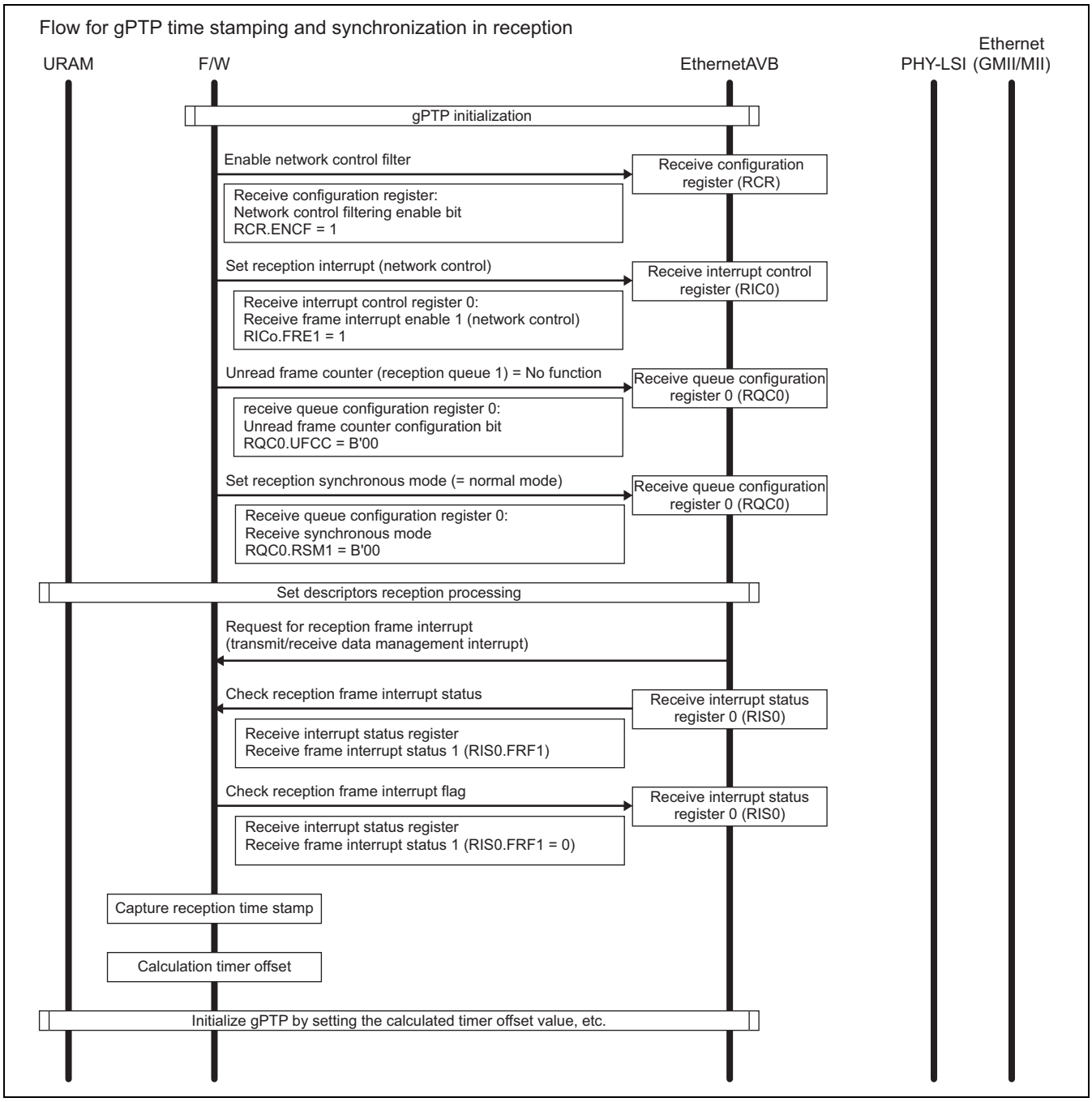


Figure 33A.68 Flow of gPTP Time Stamping and Synchronization in Reception (Normal, Common to All Modes)

33A.3.12.12 Flow of Capturing gPTP Presentation Times

Figure 33A.69 shows the flow of capturing gPTP presentation times (common to all modes).

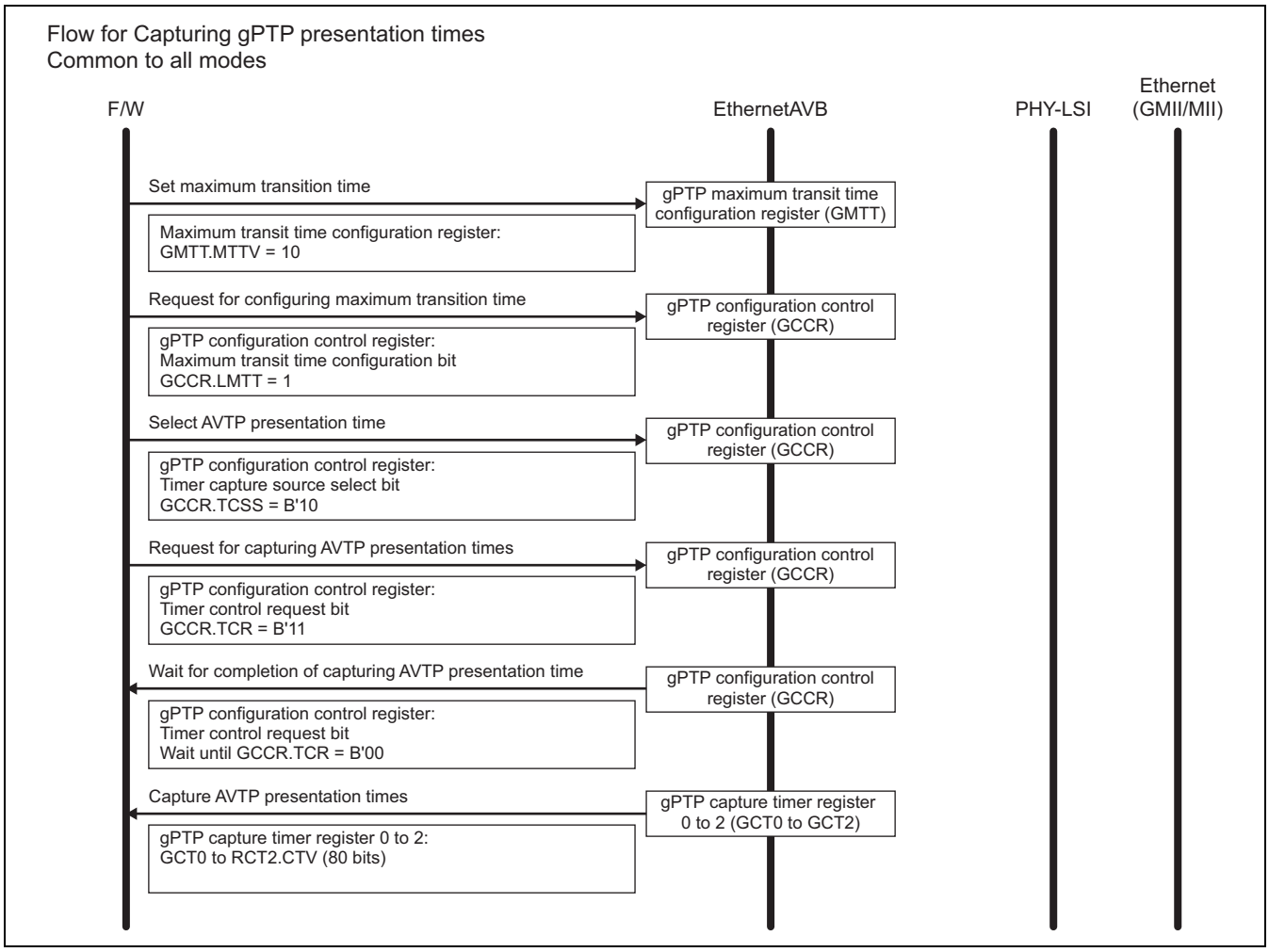


Figure 33A.69 Flow of Capturing gPTP Presentation Times (Common to All Modes)

33A.3.12.13 Flow of AVTP Presentation Time Comparison

Figure 33A.70 shows the flow of AVTP presentation time comparison (common to all modes).

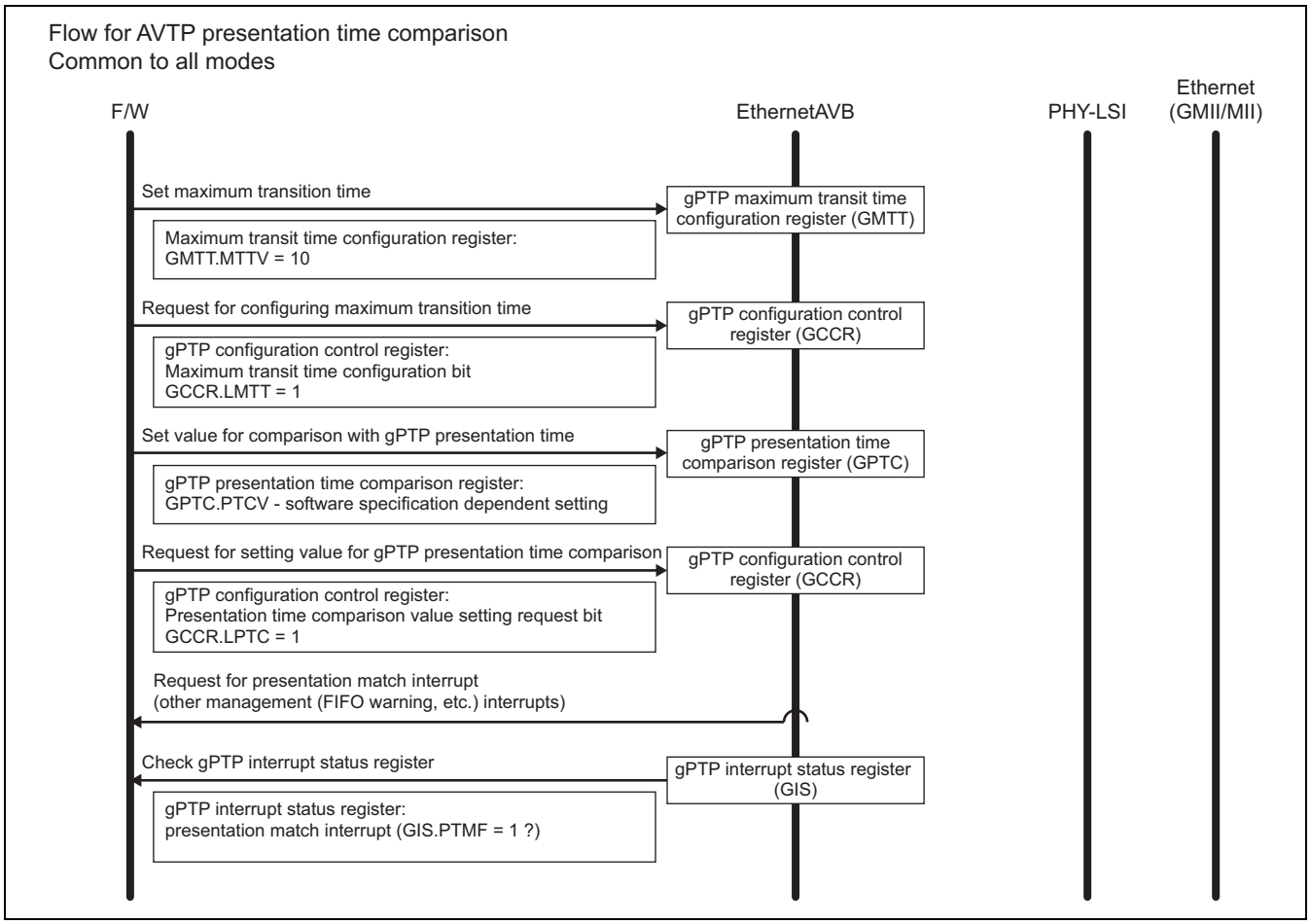


Figure 33A.70 Flow of AVTP Presentation Time Comparison (Common to All Modes)

33A.3.12.14 Flow of Loopback Mode Operation

Figure 33A.71 shows the flow of loopback mode operation.

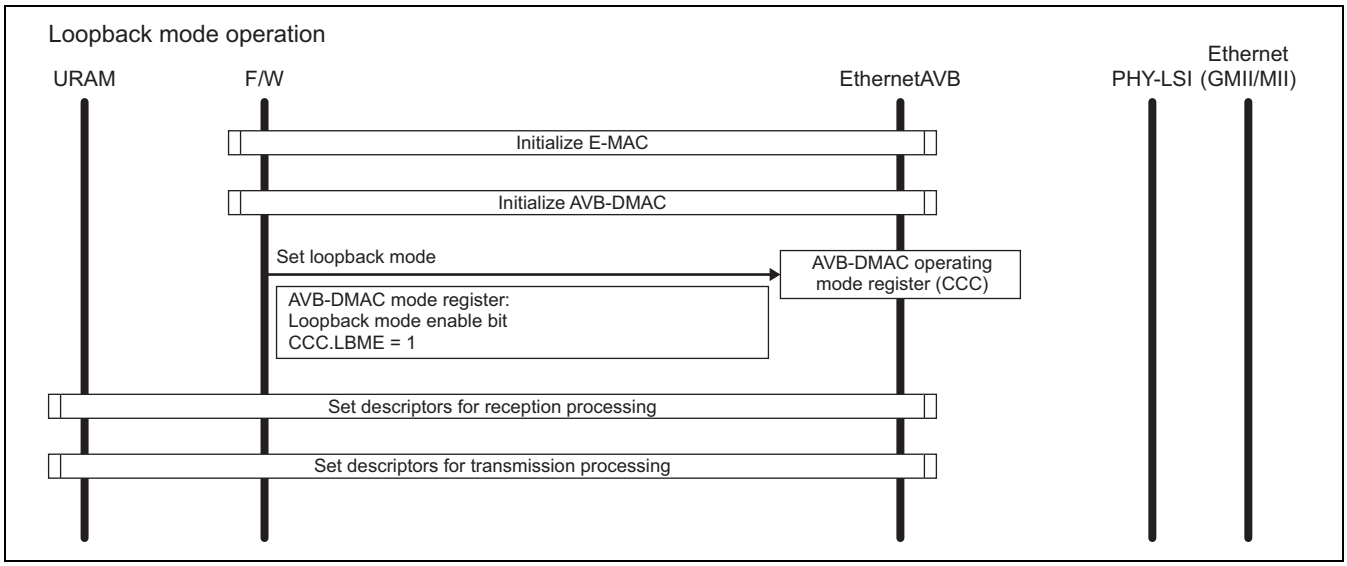


Figure 33A.71 Flow of Loopback Mode Operation

33A.3.13 Connection to PHY-LSI

33A.3.13.1 MII Frame Transmission/Reception Timing

Each MII frame transmission/reception timing is shown in Figure 33A.72 to Figure 33A.77.

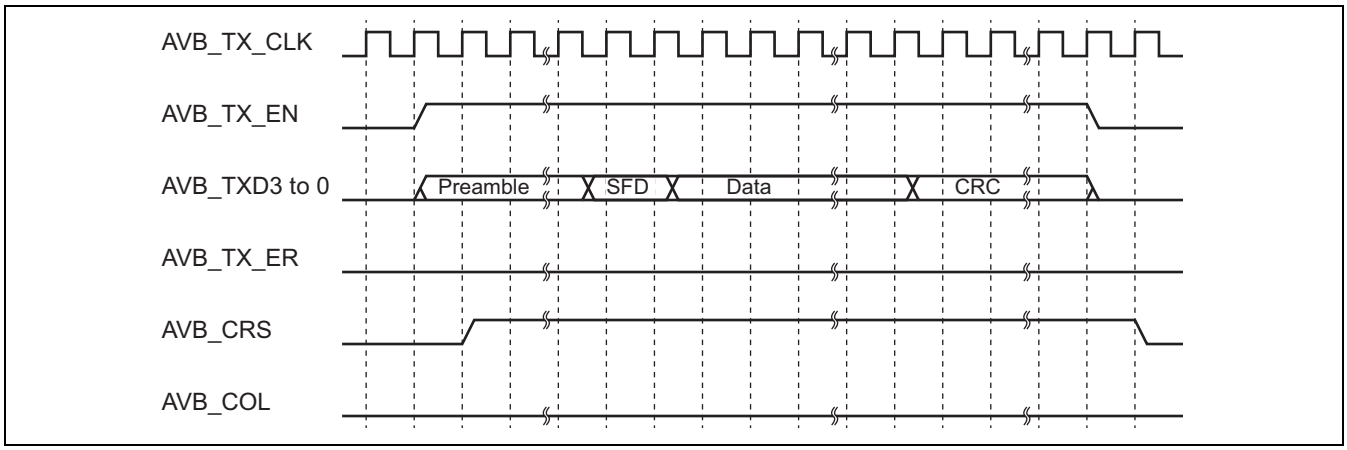


Figure 33A.72 MII Frame Transmit Timing (Normal Transmission)

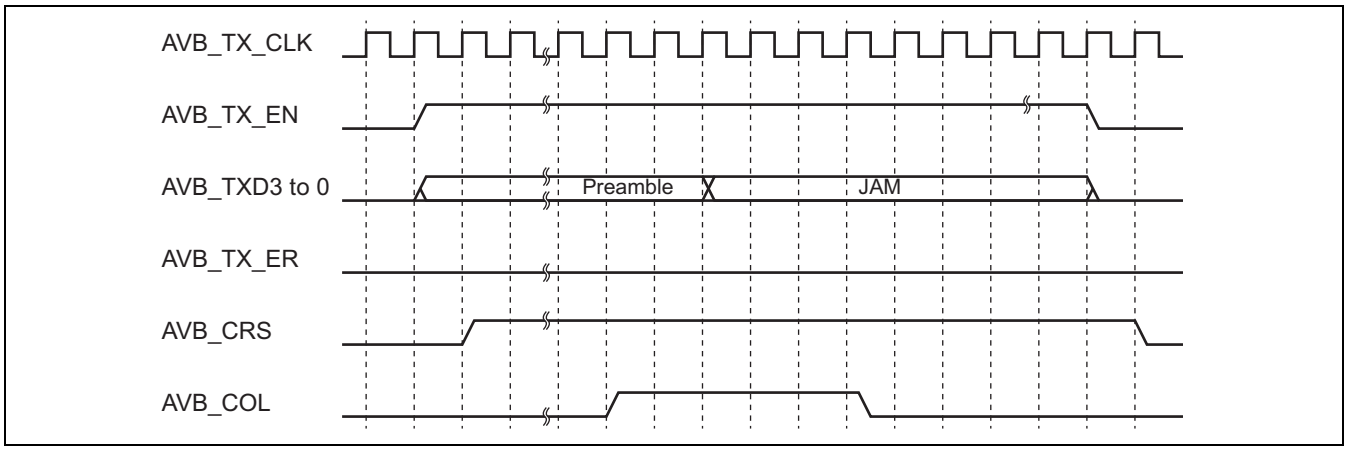


Figure 33A.73 MII Frame Transmit Timing (Collision)

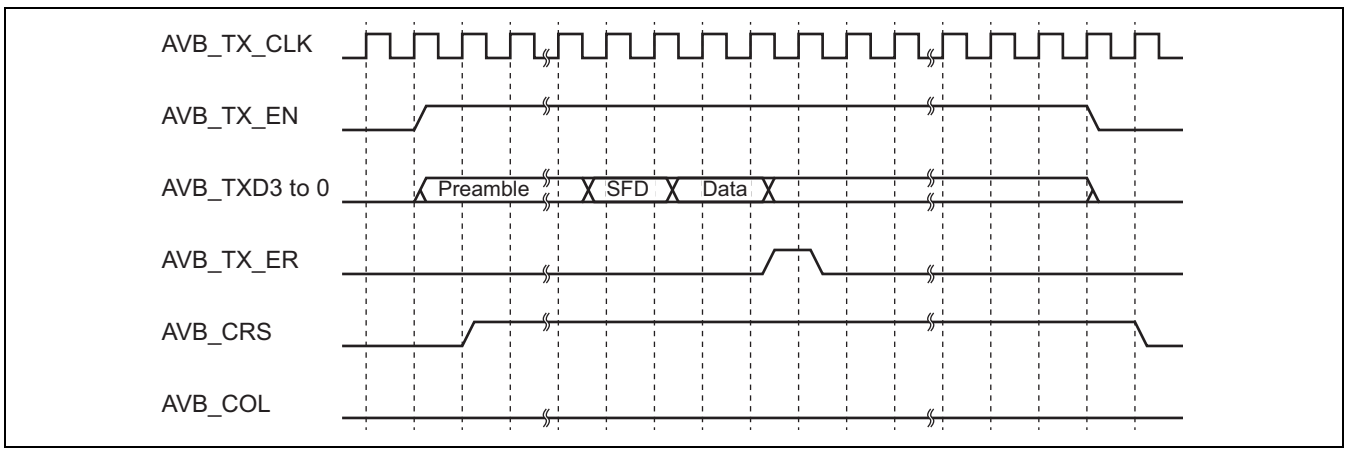


Figure 33A.74 MII Frame Transmit Timing (Transmit Error)

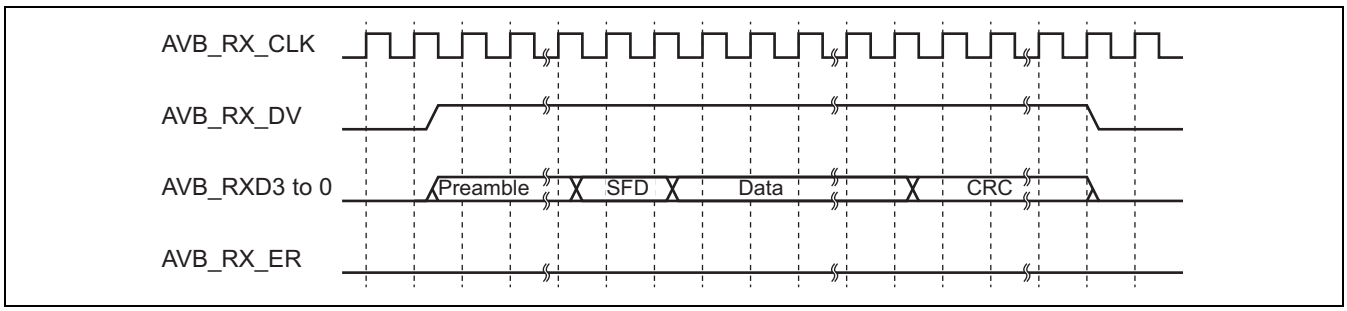


Figure 33A.75 MII Frame Receive Timing (Normal Reception)

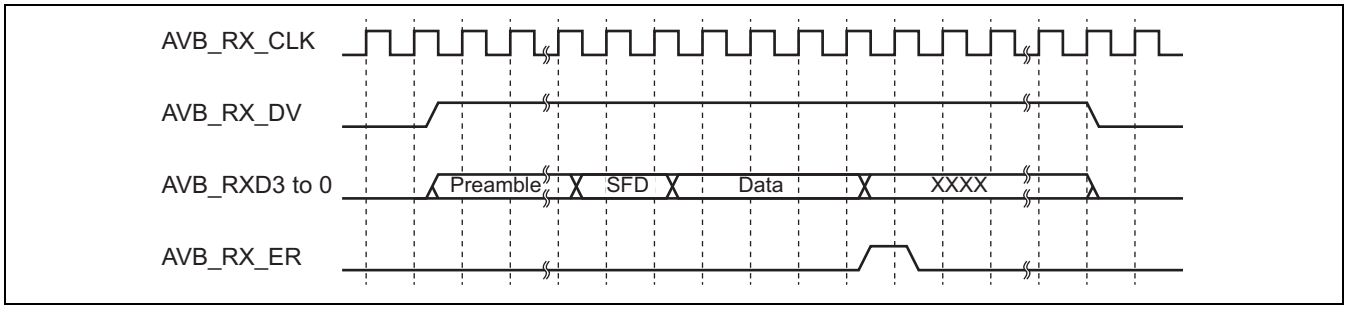


Figure 33A.76 MII Frame Receive Timing (Reception Error (1))

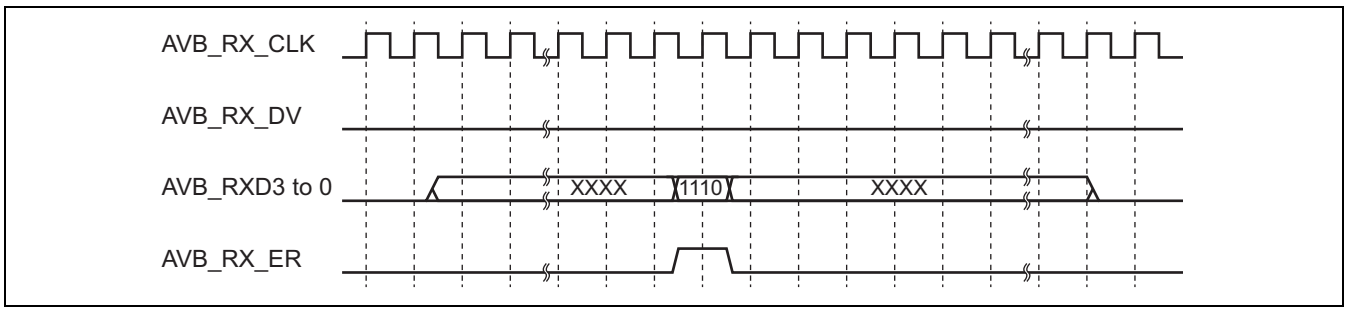


Figure 33A.77 MII Fame Receive Timing (Reception Error (2))

33A.3.13.2 GMII Frame Reception Timing

Each GMII frame transmission/reception timing is shown in Figure 33A.78 to Figure 33A.83.

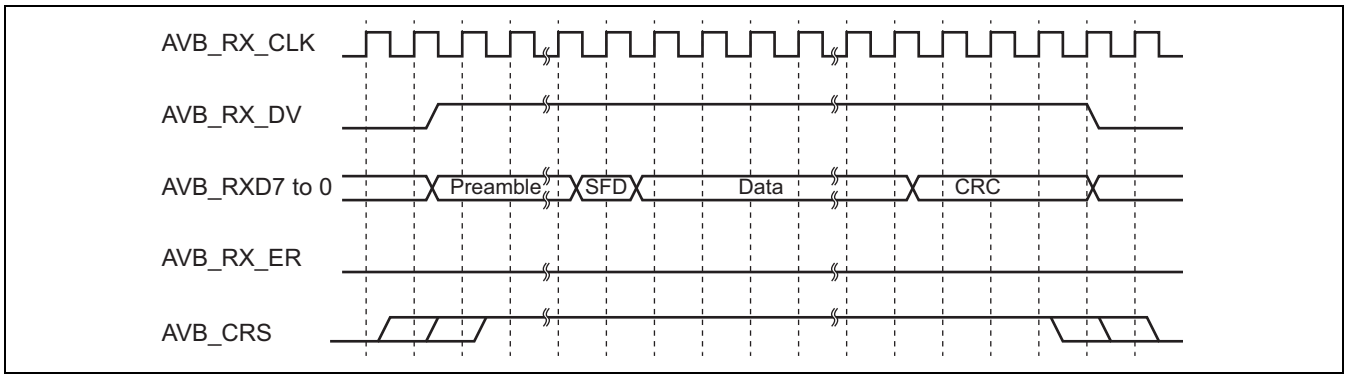


Figure 33A.78 GMII Fame Receive Timing (Normal Reception)

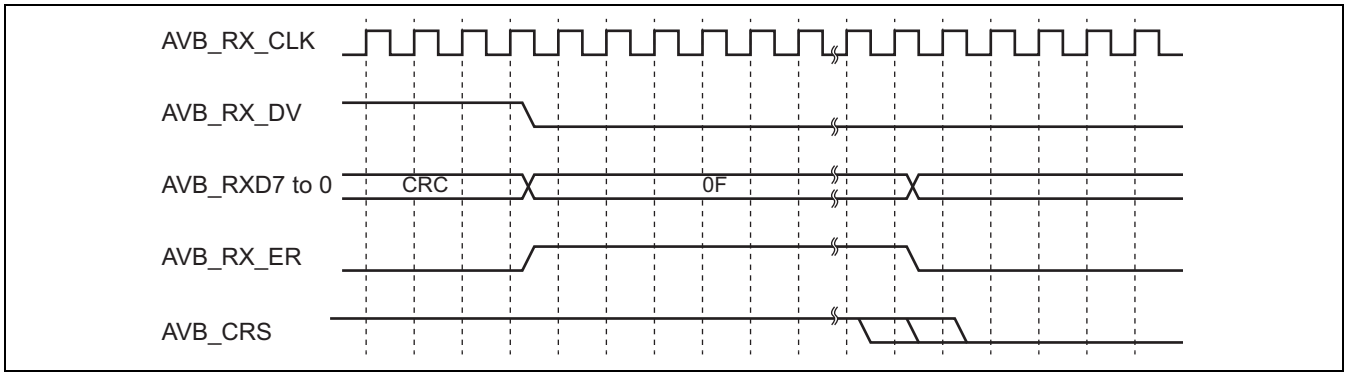


Figure 33A.79 GMII Fame Receive Timing (with Carrier Extension)

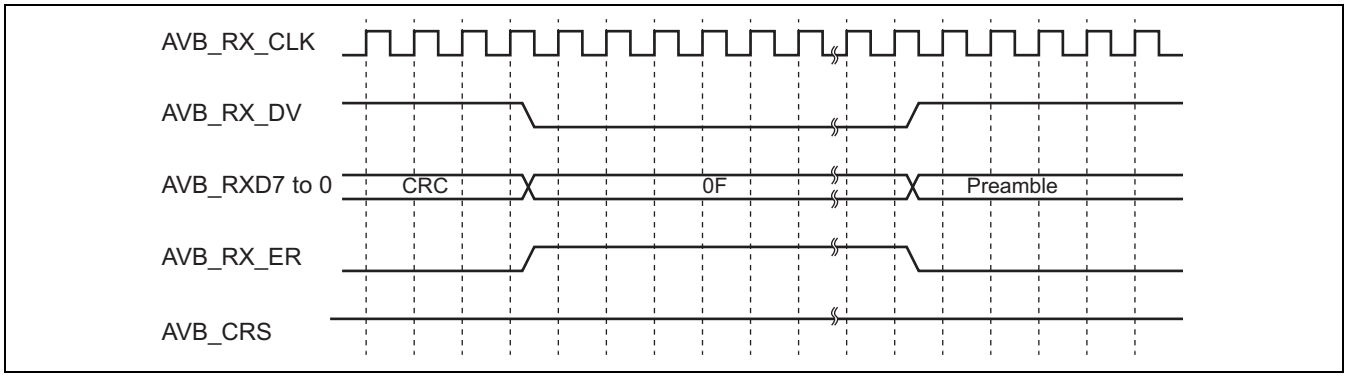


Figure 33A.80 GMII Fame Receive Timing (Burst Reception)

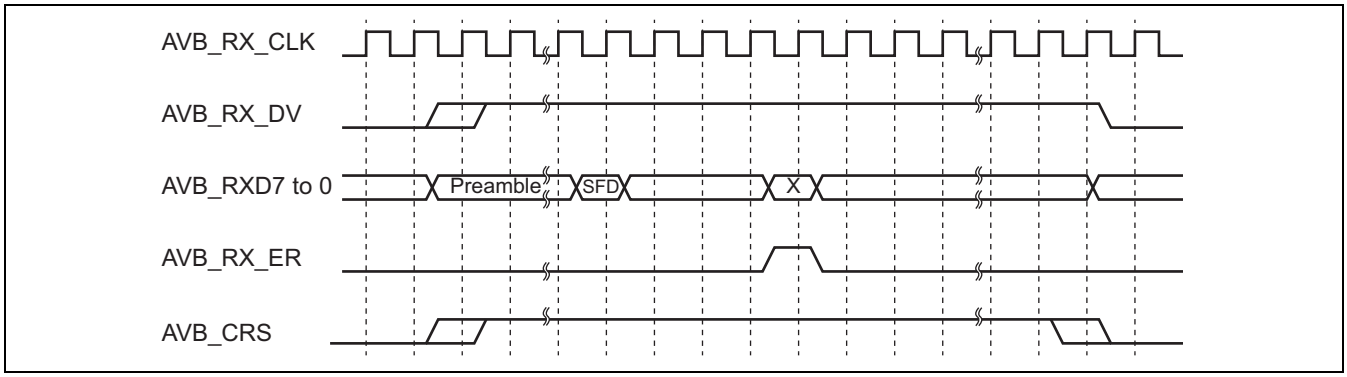


Figure 33A.81 GMII Fame Receive Timing (Reception Error)

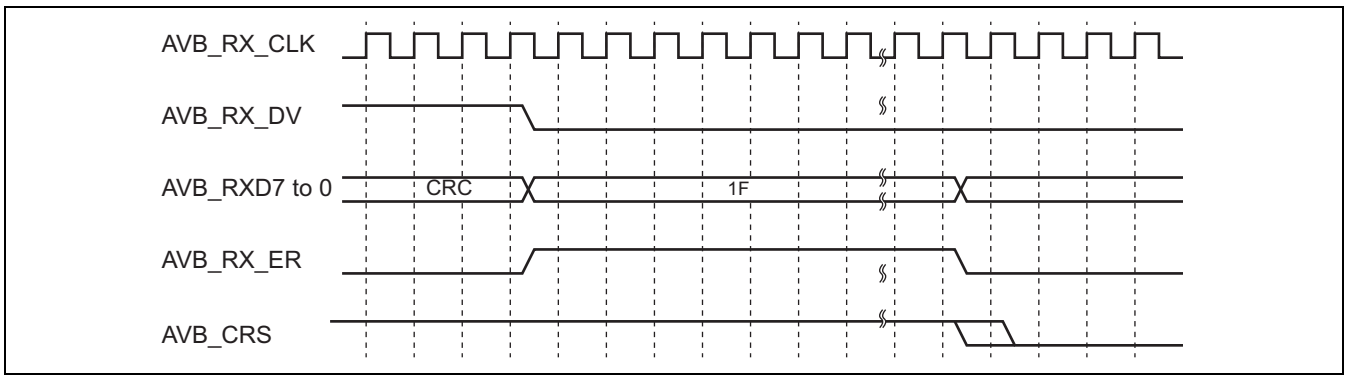


Figure 33A.82 GMII Fame Receive Timing (Error with Carrier Extension)

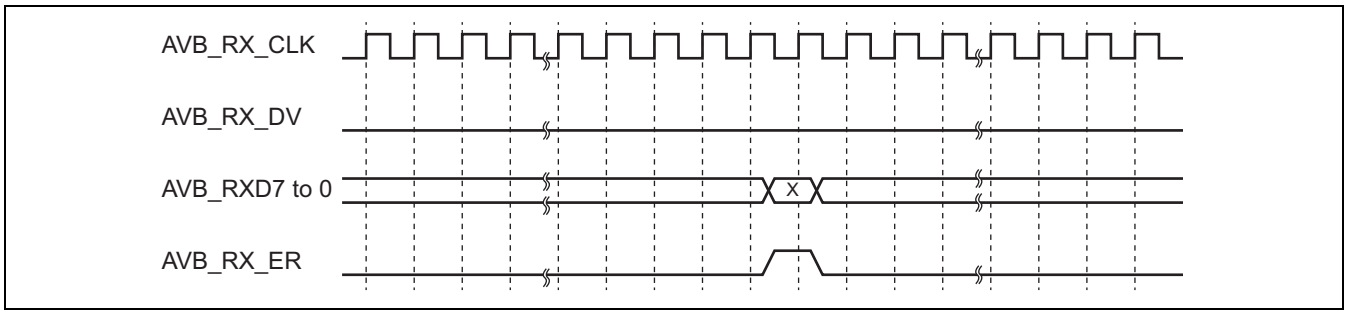


Figure 33A.83 GMII Fame Receive Timing (False Carrier Indication)

33A.3.13.3 Accessing MII Management Registers

MII management registers in the PHY-LSI are accessed via PIR in this LSI. PIR is used as a serial interface conforming to the MII frame format specified in IEEE802.3u.

(1) MII Management Frame Format

Figure 33A.84 shows the format of an MII management frame. To access an MII management register, a management frame is implemented by the program in accordance with the procedures shown in MII Management Register Access Procedure.

Access Type	MII Management Frame							
Item	PRE	ST	OP	PHYAD	REGAD	TA	DATA	IDLE
Number of bits	32	2	2	5	5	2	16	
Read	1..1	01	10	00001	RRRRR	Z0	D...D	
Write	1..1	01	01	00001	RRRRR	10	D...D	X

[Legend]
PRE: 32 consecutive 1 s
ST: Write of B'01 indicating start of frame
OP: Write of code indicating access type
PHYAD: Write of B'00001 if the PHY-LSI address is 1 (sequential write starting with the MSB).
This bit changes depending on the PHY-LSI address.
REGAD: Write of 000q if the register address is 1 (sequential write starting with the MSB).
This bit changes depending on the PHY-LSI register address.
TA: Time for switching data transmission source on MII interface
(a) Write: 10 written
(b) Read: Bus release (notation: Z0) performed
DATA: 16-bit data. Sequential write or read from MSB
(a) Write: 16-bit data write
(b) Read: 16-bit data read
IDLE: Wait time until next MII management format input
(a) Write: Independent bus release (notation: X) performed
(b) Read: Bus already released in TA: control unnecessary

Figure 33A.84 MII Management Frame Format

(2) MII Management Register Access Procedure

The program accesses MII management registers via PIR. Access is implemented by a combination of 1-bit-unit data write, 1-bit-unit data read, bus release, and independent bus release. Figure 33A.85 to Figure 33A.88 show the MII management register timing. The timing will differ depending on the PHY-LSI type.

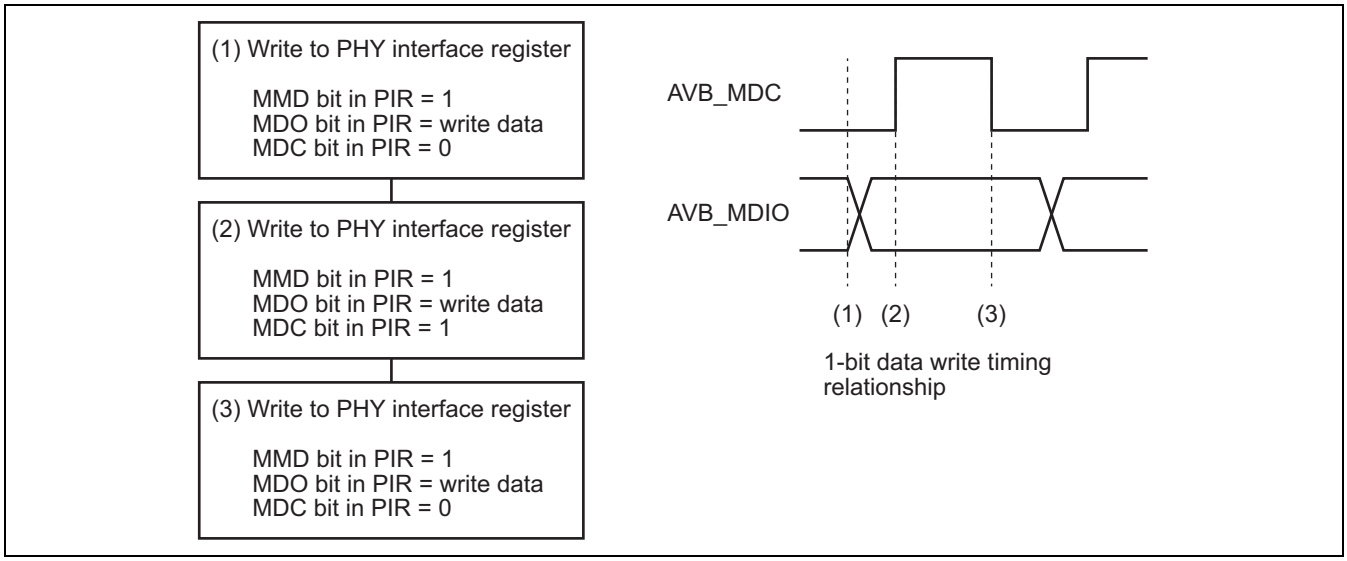


Figure 33A.85 1-Bit Data Write Flowchart

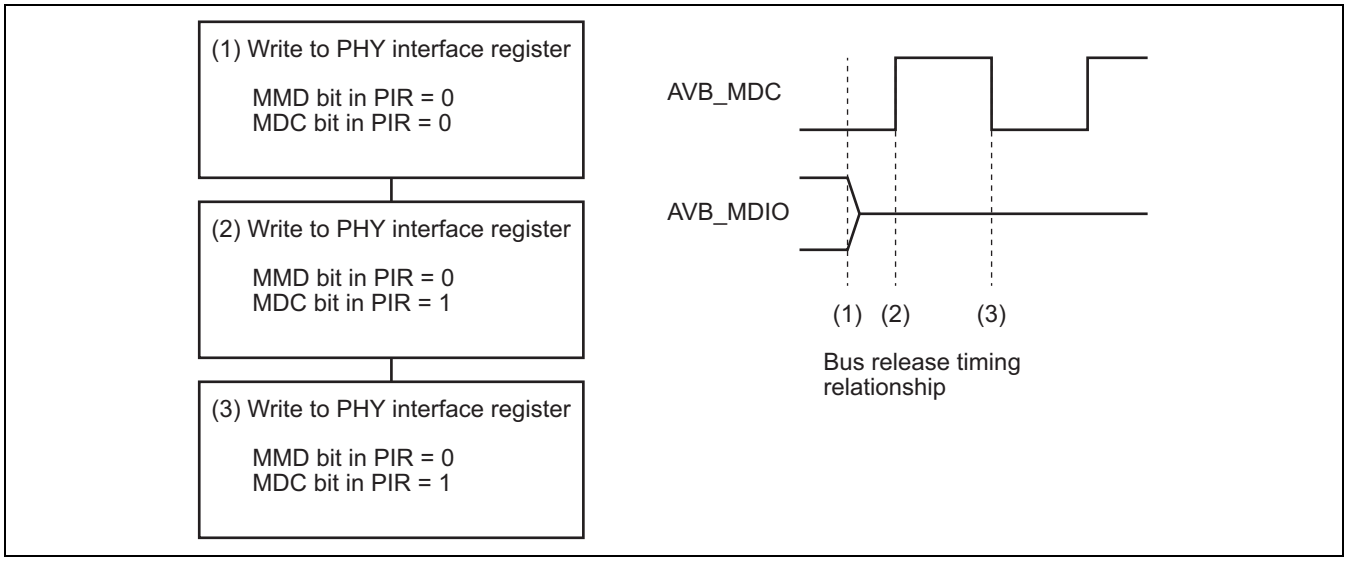


Figure 33A.86 Bus Release Flowchart (TA in Read in Figure 33A.84)

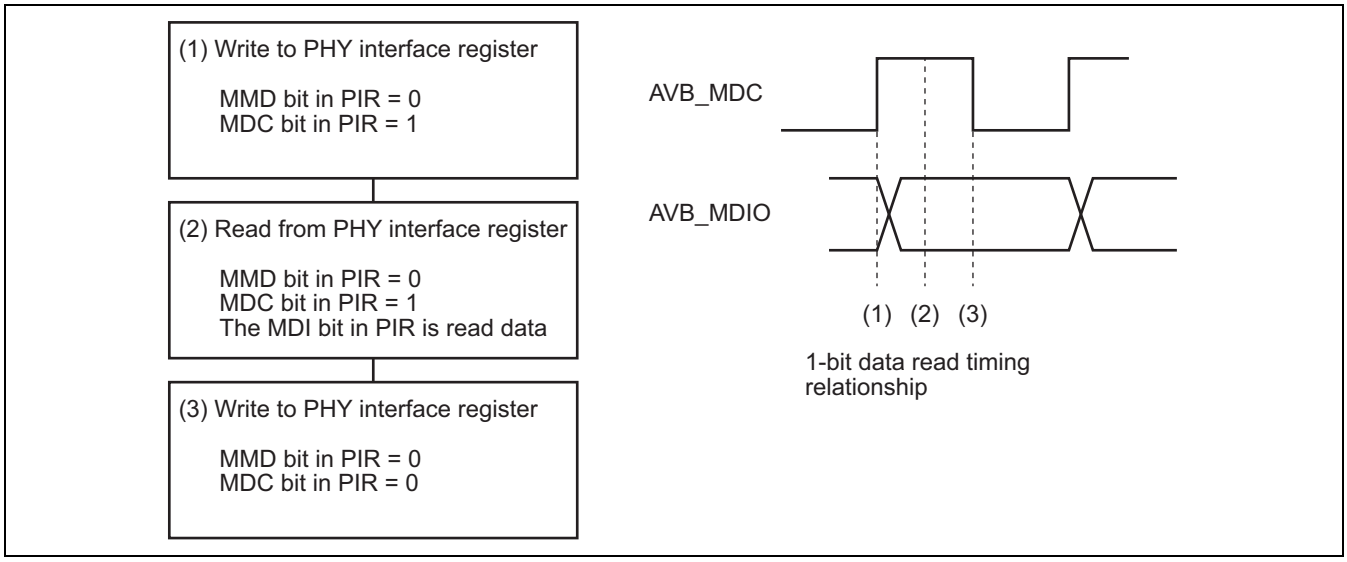


Figure 33A.87 1-Bit Data Read Flowchart

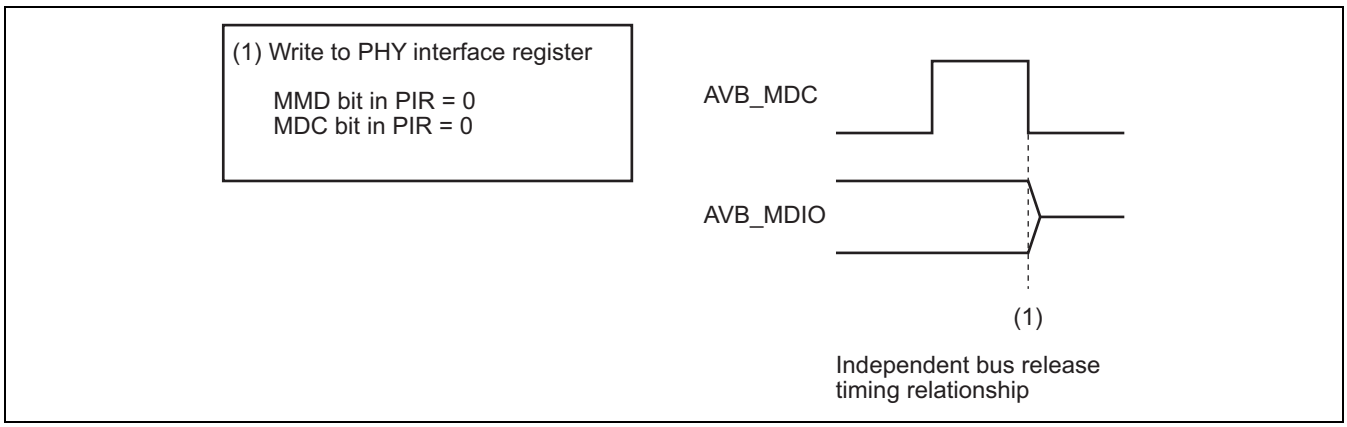


Figure 33A.88 Independent Bus Release Flowchart (IDLE in Write in Figure 33A.84)

33A.4 Usage Notes

33A.4.1 Checksum Calculation of Ethernet Frames

This LSI is capable of calculating the checksum data of the received frames. Only the data fields of the Ethernet frames are subject to checksum calculation. Specifically, a data field follows the length/type field and is followed by the CRC field. Figure 33A.89 shows schematics indicating which parts of the Ethernet frames are calculated. Calculation involves 16-bit addition only; it does not involve bit inversion. Note that when the checksum data is valid, the CRC data (4 bytes) is not transferred as a receive frame, and the checksum data (sum data) is added automatically. Figure 33A.90 shows schematics of Ethernet frames to which the checksum data has been added.

Note: Also for the frames with VLANtag inserted, the 15th byte from the top and the following bytes before the CRC field are subject to calculation.

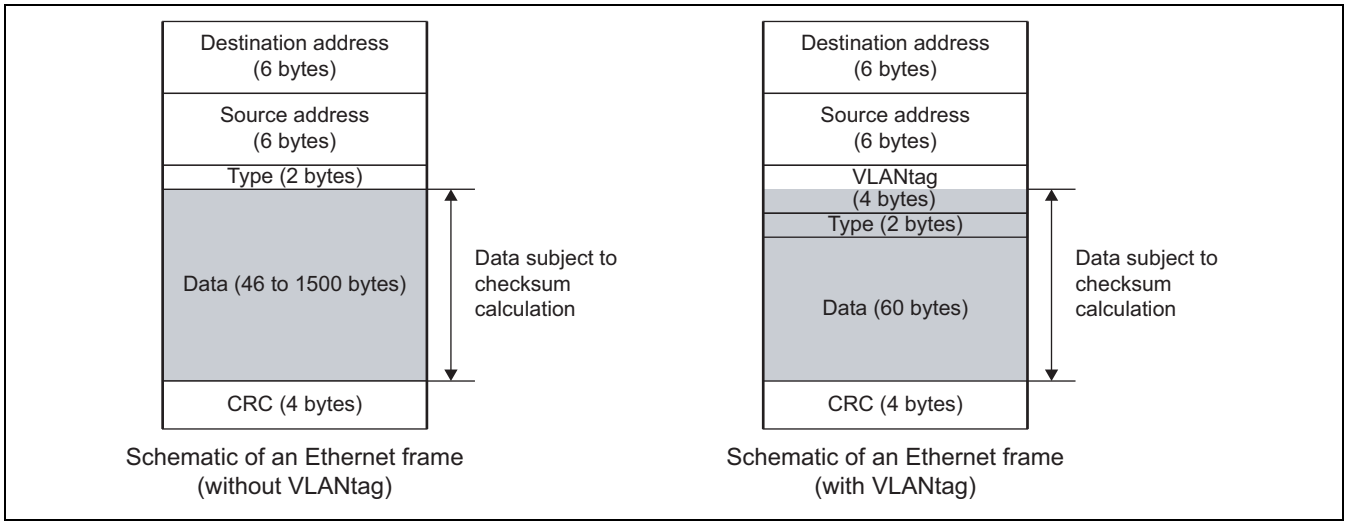


Figure 33A.89 Data Subject to Checksum Calculation

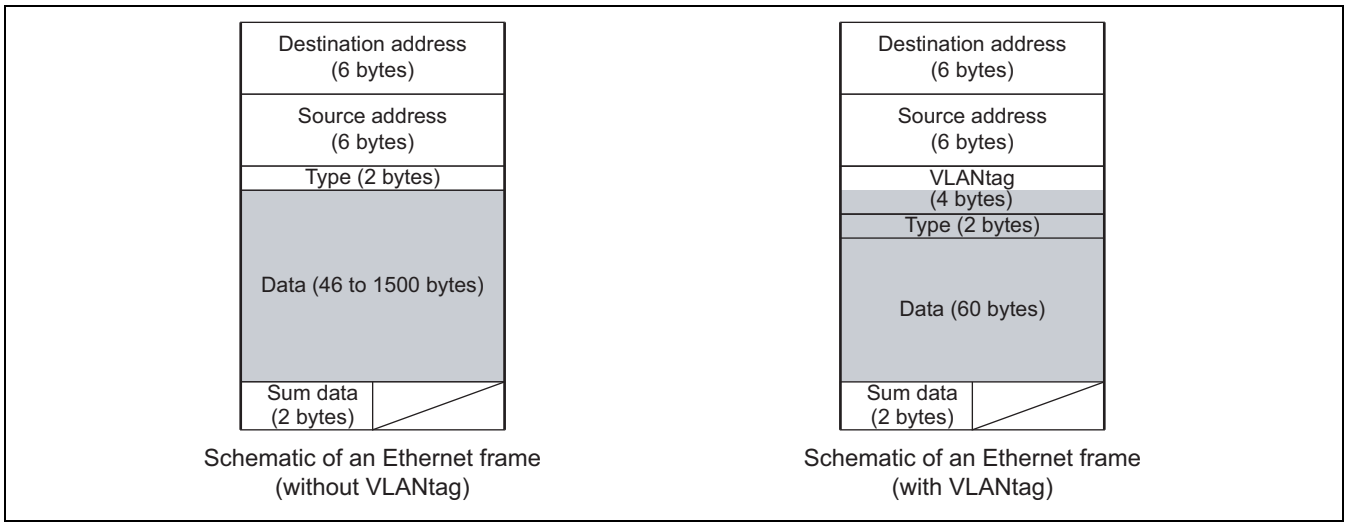


Figure 33A.90 Data after Checksum Data Addition

33A.4.2 Data Transfer Function Stops after Read Access Error

If EthernetAVB gets an access error when reading from work RAM, it may happen that no further work RAM accesses are issued. So transfer of receive/transmit frames is halted. By using the data transfer suspend function SW can observe if data transfer function is available or not.

Perform one of given SW flows which are triggered by this start condition: when AXI read access error has been flagged by EIS.QEF is 1, and ESR.ET is B'0000 or B'0100; additionally when ESR.EIL is 1 (this is an indication that an work RAM read error may be lost).

There are two possible SW flows given. Figure 33A.91 applies always the SW reset, independently if this is required or not. Figure 33A.92 checks in addition if SW reset is required; checking CSR.DTS after wait gives an indication that issue has been occurred.

Note that the wait after write of CCC.DTSR is mandatory to prevent cases where issue has not been occurred.

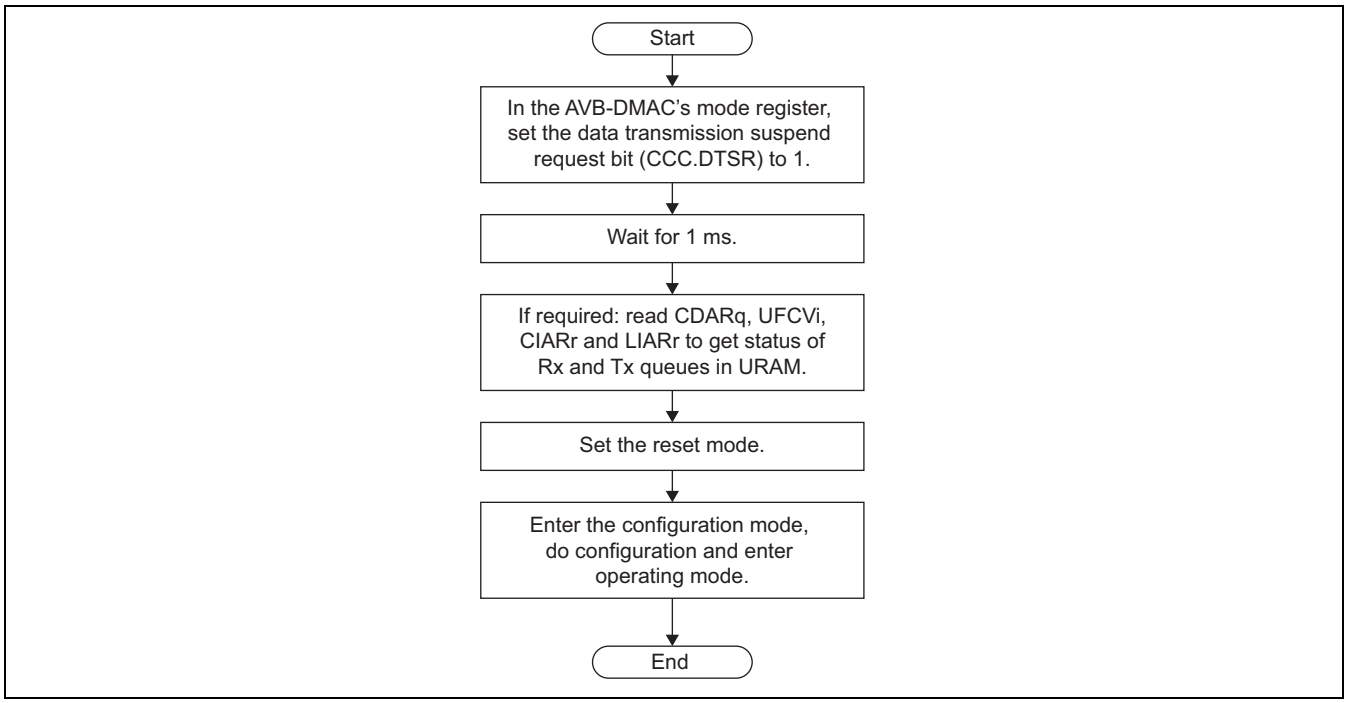


Figure 33A.91 Data Transfer Function Stop Flow1 after Read Access Error

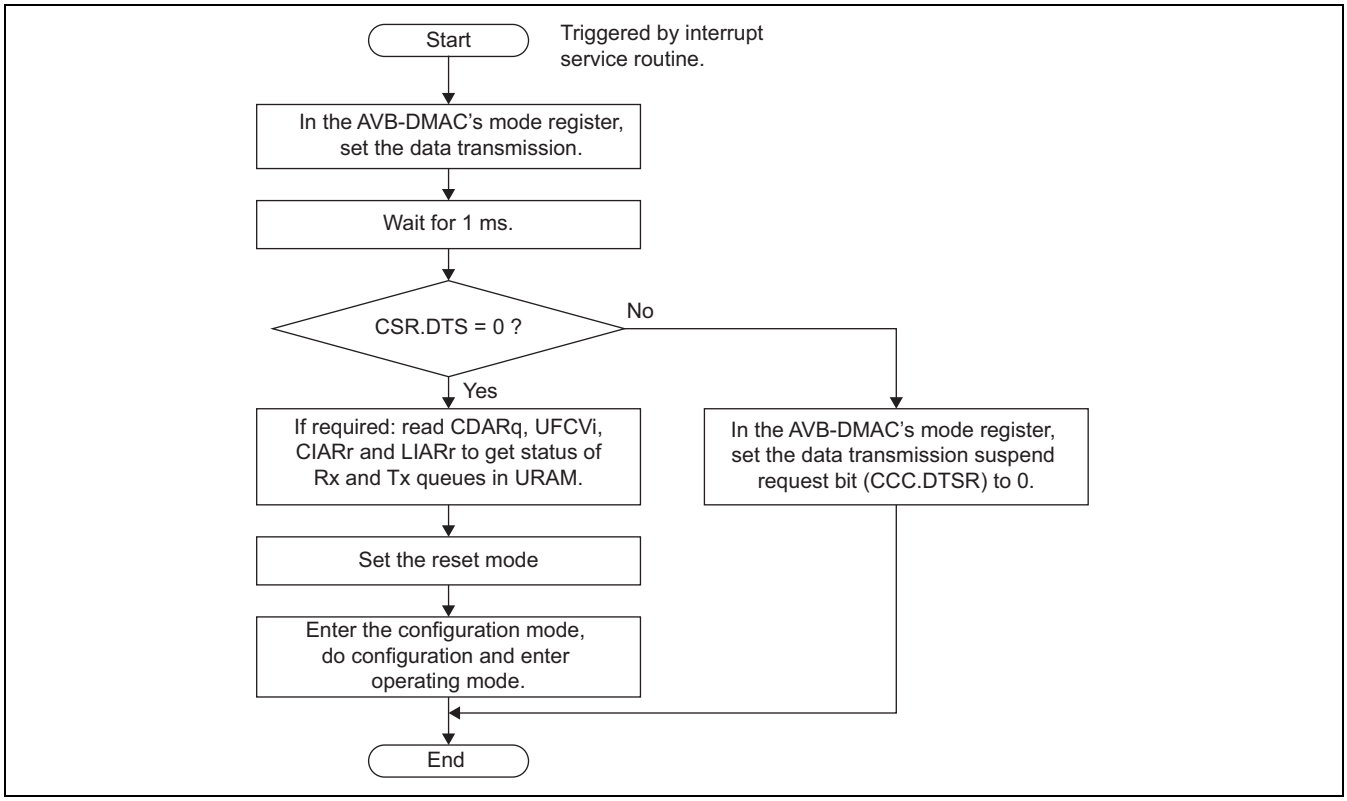


Figure 33A.92 Data Transfer Function Stop Flow2 after Read Access Error

33A.4.3 Power Down Request

If EthernetAVB gets a power down request while writing to work RAM, it may happen that the request is not accepted even if the transfer is completed. Due to this the external power down module cannot complete the power down sequence.

A power down request is acceptable only when EthernetAVB is in RESET state.

33A.4.4 Reception

(1) Reception is Ignored when AVB_RX_ER indicates an error from PHY is Flagged at 1st Data Byte

The issue is limited to reception of frames with physical faults. Flagging of occurrence in SFR is missing. When EthernetAVB is configured to store faulty frames in reception queue 0 (BE) by RCR.EFFS there is no storage.

(2) Unexpected Data are Exported when AVB_RX_ER indicates an error is Flagged at 8th Data Byte

The issue is limited to reception of frames with physical faults.

Flagging of occurrence in SFR is invalid. When EthernetAVB is configured to store faulty frames in reception queue 0 (BE) by RCR.EFFS corrupted data is stored and MAC status code is wrong.

(3) Receive Frame Interrupt and Descriptor Interrupt may be Issued before Completion of Writing Data

When receive frame interrupt and descriptor interrupt are issued, whether writing data is completed by DESCR.DT in a descriptor can be confirmed.

And CDARq register has the descriptor address which EthernetAVB is processing currently or is going to process at the next time.

The descriptors before one indicated by CDARq register are scope for receive frame interrupt and descriptor interrupt scope.

If there is a descriptor which wait for HW processing (ex. FEMPTY), it's delayed. Confirm the descriptor again after waiting for 1ms.

33B. Stream Buffer for EthernetAVB (STBE)

33B.1 Overview

The stream buffer for the EthernetAVB module (hereinafter referred to as STBE) incorporates a 16-Kbyte RAM for the EthernetAVB descriptors.

Using the STBE reduces the number of accesses to the DRAM and provides efficient access.

33B.1.1 Features

- 1-, 2-, 4-, 8-, or 16-byte access is available for transfer.
- Transfer to/from the EthernetAVB is performed via the AXI bus using the following addresses: H'EE0E_8000 to H'EE0E_BFFF (16 Kbytes)

Note: For use of the EthernetAVB descriptors, refer to section 33A, EthernetAVB.

33B.1.2 Block Diagram

Figure 33B.1 shows a block diagram of the STBE.

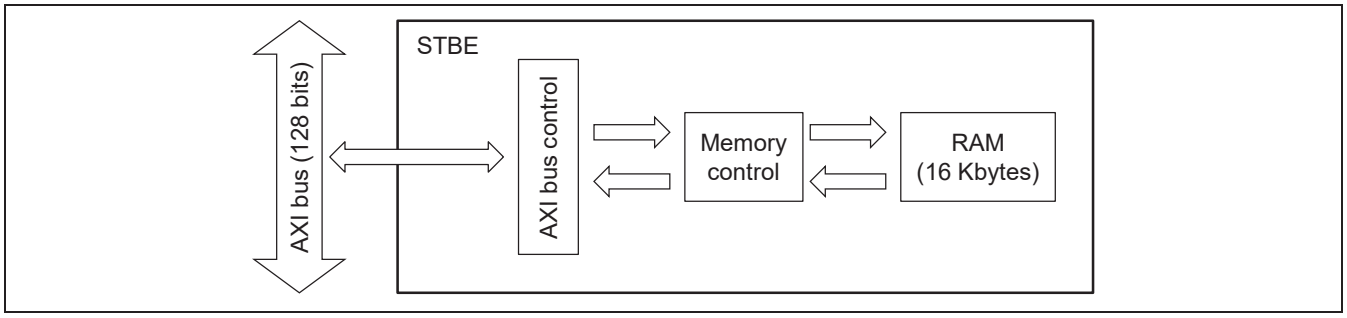


Figure 33B.1 Block Diagram

33B.2 Usage Notes

33B.2.1 Module Standby Mode

This module can be placed on module standby mode.

Ensure that this module is released from the module standby mode before using it.

33B.2.2 Transition to Module Standby Mode

1. Before stopping supply of the clock signal to this module, confirm that this module is not being accessed.
2. Set the relevant module stop control register in the clock pulse generator to stop supply of a clock signal to this module.

Note: Refer to section 7A, Module Standby and Software Reset, for the module stop control register.

33B.2.3 Release of Module Standby Mode and Restarting the STBE

Set the relevant module stop control register in the clock pulse generator to start supply of the clock signal to this module.

Note: Refer to section 7A, Module Standby and Software Reset, for the module stop control register.

34. Controller Area Network Interface (CAN interface)

34.1 Features

This MCU implements two channels (referred to as CAN0 and CAN1) of CAN (Controller Area Net-work) module that complies with the ISO11898-1 Specifications. The CAN module transmits and receives both formats of messages, namely the standard identifier (11 bits) (identifier hereafter referred to as ID) and extended ID (29 bits). Table 34.1 lists the CAN module overview and Figure 34.1 shows the CAN module block diagram. Connect the CAN bus transceiver externally.

Table 34.1 CAN Module Overview

Item	Overview
Protocol	• ISO11898-1 compliant
Bit-rate	• Up to 1 Mbps
Message box	• 64 mailboxes: Two selectable mailbox mode Normal mailbox mode: Of the 64 mailboxes, 32 can be configured for either transmission or reception (and the other 32 are reception-only). FIFO mailbox mode: 24 mailboxes configurable as transmission or reception (and the other 32 are reception-only). 4 stages FIFO for transmission and 4 stages FIFO for reception
Reception	• Data frame and remote frame can be received. • Selectable receiving ID format (only standard ID, only extended ID or both ID) • Programmable one-shot reception function • Selectable overwrite mode (message overwritten) or overrun mode (message discarded) • The reception complete interrupt can be enabled or disabled for each mailbox.
Acceptance filter	• 8 acceptance masks (one mask every 4 mailboxes) • 2 acceptance masks (one mask every 16 mailboxes) • The mask can be enabled or disabled for each mailbox.
Transmission	• Data frame and remote frame can be transmitted. • Selectable transmitting ID format (only standard ID, only extended ID or both ID) • Programmable one-shot transmission function (enable or disable) • Selectable ID priority mode or mailbox number priority mode • Transmission request can be aborted (The completion of abort can be confirmed with a flag.) • The transmission complete interrupt can be enabled or disabled for each mailbox.
Mode transition for bus-off recovery	• Mode transition for the recovery from the bus-off state can be selected: Automatic entry to CAN halt mode at bus-off entry Automatic entry to CAN halt mode at bus-off end Entry to CAN halt mode by a program Transition into error-active state by a program
Error status monitoring	• CAN bus errors (stuff error, form error, ACK error, CRC error, bit error, and ACK delimiter error) can be monitored. • Transition to error states can be detected (error-warning, error-passive, bus-off entry, and bus-off recovery). • The error counters can be read.
Time stamp function	• Time stamp function using a 16-bit counter • The reference clock can be selected from either 1-, 2-, 4- or 8-bit time periods.

Item	Overview
Interrupt sources	• 5 types: Reception complete Transmission complete Receive FIFO Transmit FIFO Error
CAN sleep mode	• Current consumption can be reduced by stopping the CAN clock.
Software support unit	• 3 software support units: Acceptance filter support Mailbox search support (receive mailbox search, transmit mailbox search and message lost search) Channel search support
CAN clock source (fCAN)	• Peripheral clocks (clkp1 or clkp2) or externally input clock is selectable. clkp1 = Pϕ, clkp2 = RCANϕ
Test mode	• 3 test modes available for user evaluation: Listen-only mode Self-test mode 0 (external loop back) Self-test mode 1 (internal loop back)

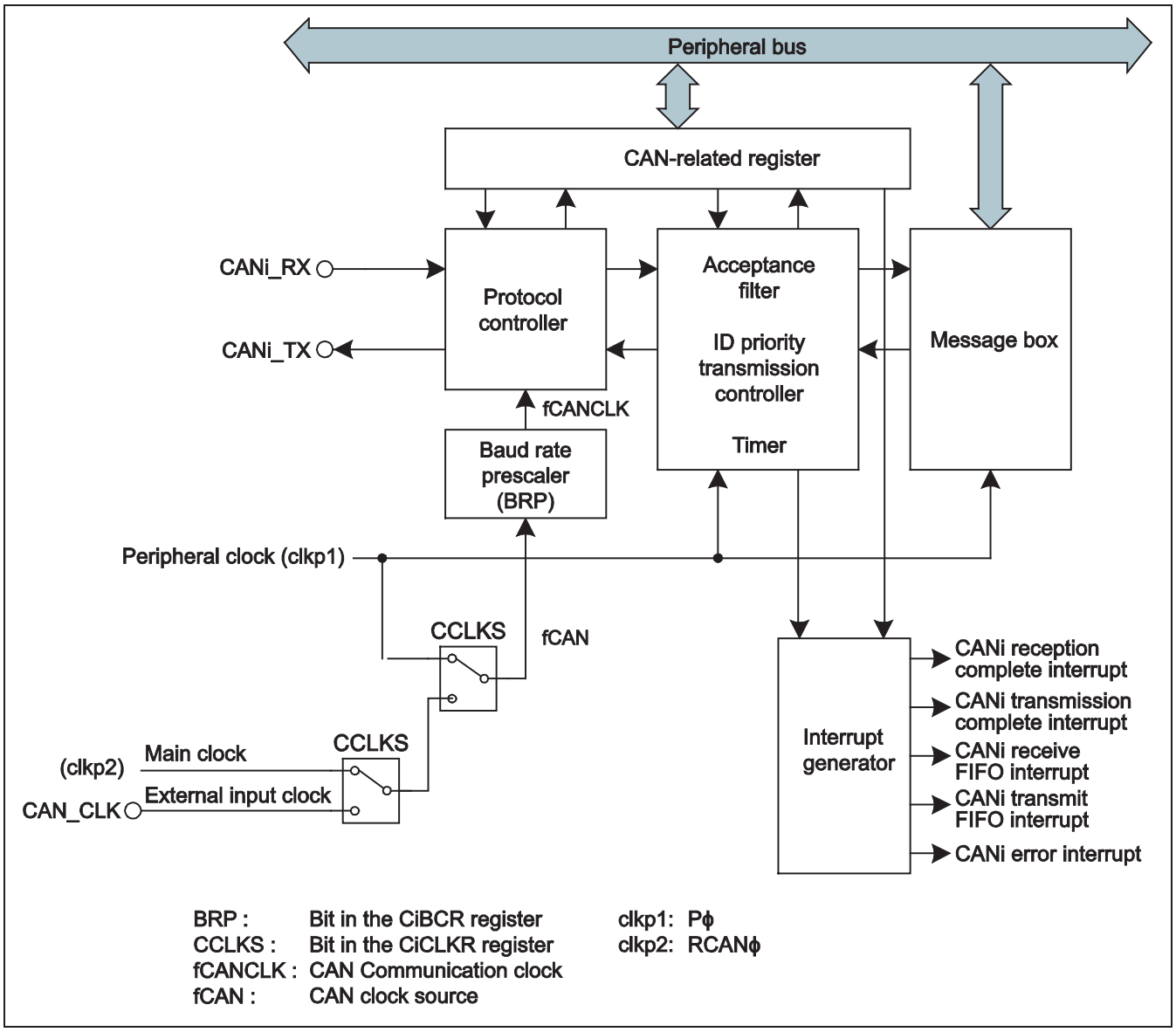


Figure 34.1 Block Diagram of CAN Module (i = 0, 1)

- CANi_RX/CANi_TX (i = 0 and 1):
  CAN input/output pins
- Protocol controller:
  Handles CAN protocol processing such as bus arbitration, bit timing at transmission and reception, stuffing, and error handling, etc.
- Message box:
  Consists of 64 mailboxes which can be configured as either transmit or receive mailboxes. Each mailbox has an individual ID, data length code, a data field (8 bytes), and a time stamp.
- Acceptance filter:
  Perform filtering of received messages. Registers CiMKR0 to CiMKR9 are used for the filtering process.
- Timer:
  Used for the time stamp function. The timer value when storing a message into the mailbox is written as the time stamp value.
- Interrupt generator:
  Generates the following five types of interrupts:
  CANi reception complete interrupt

CANi transmission complete interrupt
CANi receive FIFO interrupt
CANi transmit FIFO interrupt
CANi error interrupt

34.2 Input/Output Pins

Table 34.2 shows the CAN module pin.

Pin switching is required for pins which are multiplexed with other functions. For details, see section 5, Pin Function Controller (PFC).

Table 34.2 Pin Configuration

Pin Name	I/O	Function
CANi_RX	Input	Pins for receiving data
CANi_TX	Output	Pins for transmitting data
CAN_CLK	Input	Input pin used for external clock input.

Legend: i = 0 and 1

34.3 Register Descriptions

Table 34.3 Register Configuration

Register Name	Symbol	R/W	Value after Reset	Address	Access Size
CAN0 Control Register	C0CTLR	R/W	H'0500	H'E6E80840	8, 16
CAN0 Clock Select Register	C0CLKR	R/W	H'00	H'E6E80847	8
CAN0 Bit Configuration Register	C0BCR	R/W	H'00 0000	H'E6E80844	8, 16, 32
CAN0 Mask Register 0	C0MKR0	R/W	Undefined	H'E6E80430	8, 16, 32
CAN0 Mask Register 1	C0MKR1	R/W	Undefined	H'E6E80434	8, 16, 32
CAN0 Mask Register 2	C0MKR2	R/W	Undefined	H'E6E80400	8, 16, 32
CAN0 Mask Register 3	C0MKR3	R/W	Undefined	H'E6E80404	8, 16, 32
CAN0 Mask Register 4	C0MKR4	R/W	Undefined	H'E6E80408	8, 16, 32
CAN0 Mask Register 5	C0MKR5	R/W	Undefined	H'E6E8040C	8, 16, 32
CAN0 Mask Register 6	C0MKR6	R/W	Undefined	H'E6E80410	8, 16, 32
CAN0 Mask Register 7	C0MKR7	R/W	Undefined	H'E6E80414	8, 16, 32
CAN0 Mask Register 8	C0MKR8	R/W	Undefined	H'E6E80418	8, 16, 32
CAN0 Mask Register 9	C0MKR9	R/W	Undefined	H'E6E8041C	8, 16, 32
CAN0 FIFO Received ID Compare Register 0	C0FIDCR0	R/W	Undefined	H'E6E80420	8, 16, 32
CAN0 FIFO Received ID Compare Register 1	C0FIDCR1	R/W	Undefined	H'E6E80424	8, 16, 32
CAN0 Mask Invalid Register 0	C0MKIVLR0	R/W	Undefined	H'E6E80438	8, 16, 32
CAN0 Mask Invalid Register 1	C0MKIVLR1	R/W	Undefined	H'E6E80428	8, 16, 32
CAN0 Mailbox Register 0 to 63	C0MB0 to C0MB63	R/W	Undefined	H'E6E80000 to H'E6E803FF	8, 16, 32
CAN0 Mailbox Interrupt Enable Register 0	C0MIER0	R/W	Undefined	H'E6E8043C	8, 16, 32
CAN0 Mailbox Interrupt Enable Register 1	C0MIER1	R/W	Undefined	H'E6E8042C	8, 16, 32
CAN0 Message Control Register 0 to 63	C0MCTL0 to C0MCTL63	R/W	H'00	H'E6E80800 to H'E6E8083F	8
CAN0 Receive FIFO Control Register	C0RFCR	R/W	H'80	H'E6E80848	8
CAN0 Receive FIFO Pointer Control Register	C0RFPCR	R/W	Undefined	H'E6E80849	8
CAN0 Transmit FIFO Control Register	C0TFCR	R/W	H'80	H'E6E8084A	8
CAN0 Transmit FIFO Pointer Control Register	C0TFPCR	R/W	Undefined	H'E6E8084B	8
CAN0 Status Register	C0STR	R	H'0500	H'E6E80842	8, 16
CAN0 Mailbox Search Mode Register	C0MSMR	R/W	H'00	H'E6E80853	8
CAN0 Mailbox Search Status Register	C0MSSR	R	H'80	H'E6E80852	8
CAN0 Channel Search Support Register	C0CSSR	R/W	Undefined	H'E6E80851	8
CAN0 Acceptance Filter Support Register	C0AFSR	R/W	Undefined	H'E6E80856	8, 16

Register Name	Symbol	R/W	Value after Reset	Address	Access Size
CAN0 Error Interrupt Enable Register	C0EIER	R/W	H'00	H'E6E8084C	8
CAN0 Error Interrupt Factor Judge Register	C0EIFR	R/W	H'00	H'E6E8084D	8
CAN0 Receive Error Count Register	C0RECR	R	H'00	H'E6E8084E	8
CAN0 Transmit Error Count Register	C0TECR	R	H'00	H'E6E8084F	8
CAN0 Error Code Store Register	C0ECSR	R/W	H'00	H'E6E80850	8
CAN0 Time Stamp Register	C0TSR	R	H'0000	H'E6E80854	8, 16
CAN0 Test Control Register	C0TCR	R/W	H'00	H'E6E80858	8
CAN0 Interrupt Enable Register	C0IER	R/W	H'00	H'E6E80860	8
CAN0 Interrupt Status Register	C0ISR	R/W	H'00	H'E6E80861	8
CAN0 Mailbox Search Mask Register	C0MBSMR	R/W	H'00	H'E6E80863	8
CAN0 Parity Error Control Register	C0PECR	R/W	H'00	H'E6E8085C	8
CAN0 Parity Error Address Capture Register	C0PEACR	R	H'0000	H'E6E8085E	16
CAN1 Control Register	C1CTLR	R/W	H'0500	H'E6E88840	8, 16
CAN1 Clock Select Register	C1CLKR	R/W	H'00	H'E6E88847	8
CAN1 Bit Configuration Register	C1BCR	R/W	H'00 0000	H'E6E88844	8, 16, 32
CAN1 Mask Register 0	C1MKR0	R/W	Undefined	H'E6E88430	8, 16, 32
CAN1 Mask Register 1	C1MKR1	R/W	Undefined	H'E6E88434	8, 16, 32
CAN1 Mask Register 2	C1MKR2	R/W	Undefined	H'E6E88400	8, 16, 32
CAN1 Mask Register 3	C1MKR3	R/W	Undefined	H'E6E88404	8, 16, 32
CAN1 Mask Register 4	C1MKR4	R/W	Undefined	H'E6E88408	8, 16, 32
CAN1 Mask Register 5	C1MKR5	R/W	Undefined	H'E6E8840C	8, 16, 32
CAN1 Mask Register 6	C1MKR6	R/W	Undefined	H'E6E88410	8, 16, 32
CAN1 Mask Register 7	C1MKR7	R/W	Undefined	H'E6E88414	8, 16, 32
CAN1 Mask Register 8	C1MKR8	R/W	Undefined	H'E6E88418	8, 16, 32
CAN1 Mask Register 9	C1MKR9	R/W	Undefined	H'E6E8841C	8, 16, 32
CAN1 FIFO Received ID Compare Register 0	C1FIDCR0	R/W	Undefined	H'E6E88420	8, 16, 32
CAN1 FIFO Received ID Compare Register 1	C1FIDCR1	R/W	Undefined	H'E6E88424	8, 16, 32
CAN1 Mask Invalid Register 0	C1MKIVLR0	R/W	Undefined	H'E6E88438	8, 16, 32
CAN1 Mask Invalid Register 1	C1MKIVLR1	R/W	Undefined	H'E6E88428	8, 16, 32
CAN1 Mailbox Register 0 to 63	C1MB0 to C1MB63	R/W	Undefined	H'E6E88000 to H'E6E883FF	8, 16, 32
CAN1 Mailbox Interrupt Enable Register 0	C1MIER0	R/W	Undefined	H'E6E8843C	8, 16, 32
CAN1 Mailbox Interrupt Enable Register 1	C1MIER1	R/W	Undefined	H'E6E8842C	8, 16, 32
CAN1 Message Control Register 0 to 63	C1MCTL0 to C1MCTL63	R/W	H'00	H'E6E88800 to H'E6E8883F	8
CAN1 Receive FIFO Control Register	C1RFCR	R/W	H'80	H'E6E88848	8
CAN1 Receive FIFO Pointer Control Register	C1RFPCR	R/W	Undefined	H'E6E88849	8

Register Name	Symbol	R/W	Value after Reset	Address	Access Size
CAN1 Transmit FIFO Control Register	C1TFCR	R/W	H'80	H'E6E8884A	8
CAN1 Transmit FIFO Pointer Control Register	C1TFPCR	R/W	Undefined	H'E6E8884B	8
CAN1 Status Register	C1STR	R	H'0500	H'E6E88842	8, 16
CAN1 Mailbox Search Mode Register	C1MSMR	R/W	H'00	H'E6E88853	8
CAN1 Mailbox Search Status Register	C1MSSR	R	H'80	H'E6E88852	8
CAN1 Channel Search Support Register	C1CSSR	R/W	Undefined	H'E6E88851	8
CAN1 Acceptance Filter Support Register	C1AFSR	R/W	Undefined	H'E6E88856	8, 16
CAN1 Error Interrupt Enable Register	C1EIER	R/W	H'00	H'E6E8884C	8
CAN1 Error Interrupt Factor Judge Register	C1EIFR	R/W	H'00	H'E6E8884D	8
CAN1 Receive Error Count Register	C1RECR	R	H'00	H'E6E8884E	8
CAN1 Transmit Error Count Register	C1TECR	R	H'00	H'E6E8884F	8
CAN1 Error Code Store Register	C1ECSR	R/W	H'00	H'E6E88850	8
CAN1 Time Stamp Register	C1TSR	R	H'0000	H'E6E88854	8, 16
CAN1 Test Control Register	C1TCR	R/W	H'00	H'E6E88858	8
CAN1 Interrupt Enable Register	C1IER	R/W	H'00	H'E6E88860	8
CAN1 Interrupt Status Register	C1ISR	R/W	H'00	H'E6E88861	8
CAN1 Mailbox Search Mask Register	C1MBSMR	R/W	H'00	H'E6E88863	8
CAN1 Parity Error Control Register	C1PECR	R/W	H'00	H'E6E8885C	8
CAN1 Parity Error Address Capture Register	C1PEACR	R	H'0000	H'E6E8885E	16

Legend:

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing1 is ignored.

R: Read-only. When writing to the register, read out the value of these bits and write it back without alteration.

W: Write-only. The read value is undefined.

34.3.1 CANi Control Register (CiCTLR) (i = 0, 1)

CAN0 Control Register (C0CTLR)
CAN1 Control Register (C1CTLR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RBOC	BOM		SLPM	CANM		TSPS		TSRC	TPM	MLM	IDFM		MBM
Initial value:	0	0	0	0	0	1	0	1	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'0500>

Bit	Symbol	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
13	RBOC	0	R/W	Forcible Return From Bus-OFF Bit*1 When the RBOC bit is set to "1" (forcible return from bus-off) in bus-off state, the CAN module forcibly returns from the bus-off state. This bit is automatically set to 0. The error state changes from bus-off to error-active. When the RBOC bit is set to "1", registers CiRECR and CiTECR are set to "H'00" and the BOST bit in the CiSTR register is set to "0" (the CAN module is not in bus-off state). The other registers remain unchanged. No bus-off recovery interrupt request is generated by this recovery from the bus-off state. Use the RBOC bit only when the BOM bit = "00" (normal mode). 0: Nothing occurred 1: Forcible return from bus-off*2

Bit	Symbol	Initial Value	R/W	Description
12, 11	BOM	00	R/W	Bus-Off Recovery Mode Bit*3 The BOM bit is used to select bus-off recovery mode. When the BOM bit is "00", the recovery from bus-off is compliant with ISO11898-1, i.e. the CAN module re-enters CAN communication (error-active state) after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off. When the BOM bit is "01", as soon as the CAN reaches the bus-off state, the CANM bit in the CiCTLR register is set to "10" (CAN halt mode) and the CAN enters CAN halt mode. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to "H'00". When the BOM bit is "10", the CANM bit is set to 10b as soon as the CAN module reaches the bus-off state. The CAN module enters CAN halt mode after the recovery from the bus-off state, i.e. after detecting 11 consecutive recessive bits 128 times. A bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to "H'00". When the BOM bit is "11", the CAN module enters CAN halt mode by setting the CANM bit to "10" while the CAN module is still in bus-off state. No bus-off recovery interrupt request is generated when recovering from bus-off and registers CiTECR and CiRECR are set to "H'00". However, if the CAN module recovers from bus-off after detecting 11 consecutive recessive bits 128 times before the CANM bit is set to "10", a bus-off recovery interrupt request is generated. If the CPU requests an entry to CAN reset mode at the same time as the CAN module attempts to enter CAN halt mode (at bus-off entry when the BOM bit is "01", or at bus-off end when the BOM bit is "10"), then the CPU request to enter CAN reset mode has higher priority. 00: Normal mode (ISO11898-1 compliant) 01: Entry to CAN halt mode automatically at bus-off entry 10: Entry to CAN halt mode automatically at bus-off end 11: Entry to CAN halt mode (during bus-off recovery period) by a program request
10	SLPM	1	R/W	CAN Sleep Mode Bit*4*5 When the SLPM bit is set to "1", the CAN module enters CAN sleep mode. When the SLPM bit is set to "0", the CAN module exits CAN sleep mode. Refer to section 34.4, Operating Mode for detail. 0: Other than CAN sleep mode 1: CAN sleep mode
9, 8	CANM	01	R/W	CAN Operating Mode Select Bit*4 The CANM bit selects one of the following modes for the CAN module: CAN operation mode, CAN reset mode or CAN halt mode. Refer to section 34.4, Operating Mode for detail. CAN sleep mode is set by the SLPM bit. When the CAN module enters CAN halt mode according to the setting of the BOM bit, the CANM bit is automatically set to "10". 00: CAN operation mode 01: CAN reset mode 10: CAN halt mode 11: CAN reset mode (forcible transition)

Bit	Symbol	Initial Value	R/W	Description
7, 6	TSPS	00	R/W	Time Stamp Prescaler Select Bit*3 The TSPS bit selects the prescaler for the time stamp. The reference clock for the time stamp can be selected to be either 1-, 2-, 4- or 8-bit time periods. 00: Every bit time 01: Every 2-bit time 10: Every 4-bit time 11: Every 8-bit time
5	TSRC	0	R/W	Time Stamp Counter Reset Command Bit*6 The TSRC bit is used to reset the time stamp counter. When the TSRC bit is set to "1", the CiTSR register is set to H'0000. It is automatically set to 0. 0: Nothing occurred 1: Reset*2
4	TPM	0	R/W	Transmission Priority Mode Select Bit*3 The TPM bit specifies the priority of modes when transmitting messages. ID priority transmit mode or mailbox number transmit mode can be selected. All mailboxes are set for either ID priority transmission or mailbox number priority transmission. When the TPM bit is 0, ID priority transmit mode is selected and transmission priority complies with the CAN bus arbitration rule, as defined in the ISO 11898-1 Specifications. In ID priority transmit mode, mailboxes [0] to [63] (in normal mailbox mode), and mailboxes [0] to [55] (in FIFO mailbox mode), and the transmit FIFO are compared for the IDs of mailboxes configured for transmission. If two or more mailbox IDs are the same, the mailbox with the smaller number has higher priority. Only the next message to be transmitted from the transmit FIFO is included in the transmission arbitration. If a transmit FIFO message is being transmitted, the next pending message within the transmit FIFO is included in the transmission arbitration. When the TPM bit is 1, mailbox number transmit mode is selected and the transmit mailbox with the smallest mailbox number has the highest priority. In FIFO mailbox mode, the transmit FIFO has lower priority than normal mailboxes (mailboxes [0] to [55]). 0: ID priority transmit mode 1: Mailbox number priority transmit mode
3	MLM	0	R/W	Message Lost Mode Select Bit*3 The MLM bit specifies the operation when a new message is captured in the unread mailbox. Overwrite mode or overrun mode can be selected. All mailboxes (including the receive FIFO) are set to either overwrite mode or overrun mode. When the MLM bit is "0", all mailboxes are set to overwrite mode and the new message is overwriting the old message. When this bit is "1", all mailboxes are set to overrun mode and the new message is discarded. 0: Overwrite mode 1: Overrun mode

Bit	Symbol	Initial Value	R/W	Description
2, 1	IDFM	00	R/W	ID Format Mode Select Bit*3 The IDFM bit specifies the ID format. 00: Standard ID mode All mailboxes (including FIFO mailboxes) handle only standard IDs. 01: Extended ID mode All mailboxes (including FIFO mailboxes) handle only extended IDs. 10: Mixed ID mode All mailboxes (including FIFO mailboxes) handle both standard IDs and extended IDs. Standard IDs or extended IDs are specified by using the IDE bit in the corresponding mailbox in normal mail box mode. In FIFO mailbox mode, the IDE bit in the corresponding mailbox is used for mailboxes [0] to [55], the IDE bit in registers CiFIDCR0 and CiFIDCR1 is used for the receive FIFO, and the IDE bit in mailbox [56] is used for the transmit FIFO. 11: Do not use this combination
0	MBM	0	R/W	CAN Mailbox Mode Select Bit*3 When the MBM bit is "0" (normal mailbox mode), mailboxes [0] to [63] are configured as transmit or receive mailboxes. When the MBM bit is "1" (FIFO mailbox mode), mailboxes [0] to [55] are configured as transmit or receive mailboxes. Mailboxes [56] to [59] are configured as a transmit FIFO and mailboxes [60] to [63] as a receive FIFO. Transmit data is written into mailbox [56] (mailbox [56] is a window mailbox for the transmit FIFO). Receive data is read from mailbox [60] (mailbox [60] is a window mailbox for the receive FIFO). Table 34.4 lists the Mailbox Configuration. 0: Normal mailbox mode 1: FIFO mailbox mode

Notes:
1. Set the RBOC bit to "1" in bus-off state.
2. Bits RBOC and TSRC are automatically set back to "0" after being set to "1". It should be read as "0".
3. Write to bits BOM, MBM, IDFM, MLM, TPM, and TSPS in CAN reset mode.
4. When bits CANM and SLPM are changed, check the CiSTR register to ensure that the mode has been switched.
5. Write to the SLPM bit in CAN reset mode or CAN halt mode. When rewriting the SLPM bit, set only this bit to "0" or "1".
6. Set the TSRC bit to "1" in CAN operation mode.

Table 34.4 Mailbox Configuration

Mailbox	MBM Bit = "0" (Normal mailbox mode)	MBM Bit = "1" (FIFO mailbox mode)
Mailboxes [0] to [55]	Normal mailbox	Normal mailbox
Mailboxes [56] to [59]		Transmit FIFO
Mailboxes [60] to [63]		Receive FIFO

Notes: Points 1 to 5 below should be considered when the MBM bit is set to "1".

1. Transmit FIFO is controlled by the CiTFCR register.
   The CiMCTLj register of mailboxes [56] to [59] are disabled.
   Registers CiMCTL56 to CiMCTL59 cannot be used.
2. Receive FIFO is controlled by the CiRFCR register.
   The CiMCTLj register of mailboxes [60] to [63] are disabled.
   Registers CiMCTL60 to CiMCTL63 cannot be used.
3. Refer to the CiMIER1 register about the FIFO interrupts.
4. The corresponding bits in the CiMKIVLR register for mailboxes [56] to [63] are disabled. Set 0 to these bits.
5. Transmit/receive FIFOs can be used for both data frames and remote frames.

34.3.2 CANi Clock Select Register (CiCLKR) (i = 0, 1)

CAN0 Clock Select Register (C0CLKR)
CAN1 Clock Select Register (C1CLKR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CCLKS	
Initial	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
1, 0	CCLKS	0	R/W	CAN Clock Source Select Bits* The CCLKS bits select clock source from among the peripheral clock (clkp1 or clkp2) generated by the PLL frequency synthesizer, and an externally input clock. 00: Peripheral clock (clkp1) 01: Peripheral clock (clkp2) 10: Illegal value 11: Externally input clock

Note: * Write to the CCLKS bit in CAN reset mode.

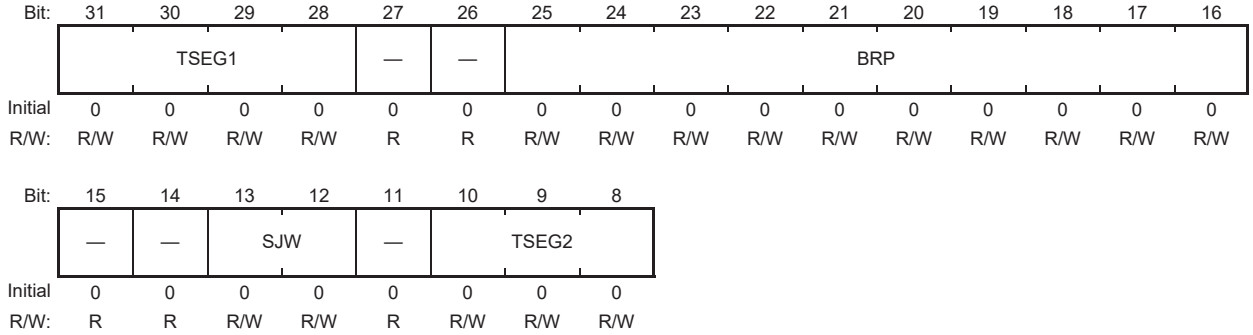
34.3.3 CANi Bit Configuration Register (CiBCR) (i = 0, 1)

For the bit timing configuration rule, refer to section 34.5, CAN Communication Speed Configuration.

Set the CiBCR register before entering CAN halt mode from CAN reset mode or CAN operation mode from CAN reset mode. After the setting is made once, this register can be written to in CAN reset mode or CAN halt mode.

The CiBCR register consists of 24 bits. A 32-bit read/write access should be performed carefully not to rewrite the CiCLKR register.

CAN0 Bit Configuration Register (C0BCR)
CAN1 Bit Configuration Register (C1BCR)



<After Reset: H'000000>

Bit	Symbol	Initial Value	R/W	Description
31 to 28	TSEG1	0000	R/W	Time Segment 1 Control Bits The TSEG1 bit is used to specify the total length of the propagation time segment (PROP_SEG) and phase buffer segment 1 (PHASE_SEG1) with the value of Tq. A value from 4 to 16 time quanta can be set. 0000: Do not use this combination 0001: Do not use this combination 0010: Do not use this combination 0011: 4 Tq 0100: 5 Tq 0101: 6 Tq 0110: 7 Tq 0111: 8 Tq 1000: 9 Tq 1001: 10 Tq 1010: 11 Tq 1011: 12 Tq 1100: 13 Tq 1101: 14 Tq 1110: 15 Tq 1111: 16 Tq
27, 26	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.

Bit	Symbol	Initial Value	R/W	Description
25 to 16	BRP	H'000	R/W	Prescaler Division Ratio Set Bits The BRP bit is used to set the peripheral bus clock periods contained in a Time Quantum. If the setting value is P (0 to 1023), the baud rate prescaler divides fCAN by P + 1.
15, 14	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
13, 12	SJW	00	R/W	Resynchronization Jump Width Control Bits The SJW bit is used to specify the resynchronization jump width with the value of Tq. A value from 1 to 4 time quanta can be set. Set the value smaller than or equal to that of the TSEG2 bit. 00: 1 Tq 01: 2 Tq 10: 3 Tq 11: 4 Tq
11	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
10 to 8	TSEG2	000	R/W	Time Segment 2 Control Bits The TSEG2 bit is used to specify the length of phase buffer segment 2 (PHASE_SEG2) with the value of Tq. A value from 2 to 8 time quanta can be set. Set the value smaller than that of the TSEG1 bit. 000: Do not use this combination 001: 2 Tq 010: 3 Tq 011: 4 Tq 100: 5 Tq 101: 6 Tq 110: 7 Tq 111: 8 Tq

34.3.4 CANi Mask Register k (CiMKRk) (i = 0, 1; k = 0 to 9)

For masking the function in FIFO mailbox mode, refer to section 34.7, Acceptance Filtering and Masking Function.

Write to registers CiMKR0 to CiMKR9 in CAN reset mode or CAN halt mode.

CAN0 Mask Register 0 (C0MKR0)
CAN0 Mask Register 1 (C0MKR1)
CAN0 Mask Register 2 (C0MKR2)
:
CAN0 Mask Register 9 (C0MKR9)
CAN1 Mask Register 0 (C1MKR0)
CAN1 Mask Register 1 (C1MKR1)
CAN1 Mask Register 2 (C1MKR2)
:
CAN1 Mask Register 9 (C1MKR9)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	SID											EID	
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EID															
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 29	—	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
28 to 18	SID	Undefined	R/W	Standard ID Bits The SID bit is the filter mask bit corresponding to the CAN standard ID bit. The SID bit is used to receive both standard ID and extended ID messages. When the SID bit is set to "0", the corresponding SID bit is not compared for the received ID and the mailbox ID. When the SID bit is set to "1", corresponding SID bit compares received ID with mailbox ID. 0: Corresponding SID bit is not compared 1: Corresponding SID bit is compared
17 to 0	EID	Undefined	R/W	Extended ID Bits The EID bit is the filter mask bit for CAN extended ID bit. This bit is used to receive extended ID messages. When the EID bit is set to "0", corresponding EID bit does not compare received ID with mailbox ID. When the EID bit is set to "1", corresponding EID bit compares received ID with mailbox ID. 0: Corresponding EID bit is not compared 1: Corresponding EID bit is compared

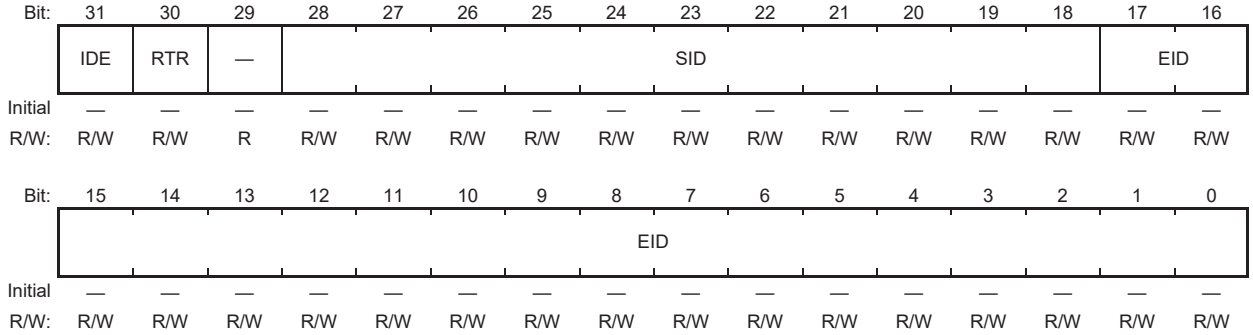
34.3.5 CANi FIFO Received ID Compare Registers (CiFIDCR0 and CiFIDCR1) (i = 0, 1)

Registers CiFIDCR0 and CiFIDCR1 are enabled when the MBM bit in the CiCTLR register is set to "1" (FIFO mailbox mode). Bits EID, SID, RTR, and IDE in registers CiMB60 to CiMB63 are disabled.

For the usage of these registers, refer to section 34.7, Acceptance Filtering and Masking Function.

Write to registers CiFIDCR0 and CiFIDCR1 in CAN reset mode or CAN halt mode.

CAN0 FIFO Received ID Compare Register 0 (C0FIDCR0)
CAN0 FIFO Received ID Compare Register 1 (C0FIDCR1)
CAN1 FIFO Received ID Compare Register 0 (C1FIDCR0)
CAN1 FIFO Received ID Compare Register 1 (C1FIDCR1)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31	IDE	Undefined	R/W	ID Extension Bit* The IDE bit sets the ID format to standard ID or extended ID. The IDE bit is enabled when the IDFM bit in the CiCTLR register is "10" (mixed ID mode). When the IDFM bit is "10", the IDE bit specifies the following operation. When both IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to "0", only standard ID frames can be received. When both IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to "1", only extended ID frames can be received. When the IDE bits in registers CiFIDCR0 and CiFIDCR1 are set to "0" or "1" individually, both standard ID and extended ID frames can be received. 0: Standard ID 1: Extended ID
30	RTR	Undefined	R/W	Remote Transmission Request Bit The RTR bit sets the specified frames format of data frame or remote frames. The RTR bit specifies the following operation. When both RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to "0", only data frames can be received. When both RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to "1", only remote frames can be received. When the RTR bits in registers CiFIDCR0 and CiFIDCR1 are set to "0" or "1" individually, both data frames and remote frames can be received. 0: Data frame 1: Remote frame

Bit	Symbol	Initial Value	R/W	Description
29	—	Undefined	R	Reserved bit The reset value is undefined. The write value should be "0". This bit is read as "0" after "0" is written to.
28 to 18	SID	Undefined	R/W	Standard ID Bits The SID bit sets the standard ID of data frames and remote frames. The SID bit is used to receive both standard ID and extended ID messages. 0: Corresponding SID bit is "0" 1: Corresponding SID bit is "1"
17 to 0	EID	Undefined	R/W	Extended ID Bits The EID bit sets the extended ID of data frames and remote frames. The EID bit is used to receive extended ID messages. 0: Corresponding EID bit is "0" 1: Corresponding EID bit is "1"

Note: * When the IDFM bit is not "10", the IDE bit should be written with "0".

34.3.6 CANi Mask Invalid Registers (CiMKIVLR0 and CiMKIVLR1) (i = 0, 1)

Each bit in registers CiMKIVLR0 and CiMKIVLR1 corresponds to a mailbox. The correspondence between the bits and mailboxes is as follows:

- Bit 0 in the CiMKIVLR0 register corresponds to mailbox 0 (MB0).
- Bit 31 in the CiMKIVLR0 register corresponds to mailbox 31 (MB31).
- Bit 0 in the CiMKIVLR1 register corresponds to mailbox 32 (MB32).
- Bit 31 in the CiMKIVLR1 register corresponds to mailbox 63 (MB63).

When each bit is "1", the acceptance mask for the mailbox corresponding to the bit number is disabled. In this case, a receiving message is stored into mailbox only its ID matches bits SID and EID in the CiMBj register.

Write to registers CiMKIVLR0 and CiMKIVLR1 either in CAN reset mode or CAN halt mode.

CAN0 Mask Invalid Register 0 (C0MKIVLR0)
CAN1 Mask Invalid Register 0 (C1MKIVLR0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB31 to 0	Undefined	R/W	Bit 31 corresponds to mailbox 31 (MB31), and bit 0 corresponds to mailbox 0 (MB0). 0: Mask valid 1: Mask invalid

CAN0 Mask Invalid Register 1 (C0MKIVLR1)
CAN1 Mask Invalid Register 1 (C1MKIVLR1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB63	MB62	MB61	MB60	MB59	MB58	MB57	MB56	MB55	MB54	MB53	MB52	MB51	MB50	MB49	MB48
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB47	MB46	MB45	MB44	MB43	MB42	MB41	MB40	MB39	MB38	MB37	MB36	MB35	MB34	MB33	MB32
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB63 to 32	Undefined	R/W	Bit 31 corresponds to mailbox 63 (MB63), and bit 0 corresponds to mailbox 32 (MB32). 0: Mask valid 1: Mask invalid

34.3.7 CANi Mailbox Register j (CiMBj) (i = 0, 1; j = 0 to 63)

Table 34.5 lists the CANi mailbox memory mapping and Table 34.6 lists the CAN data frame construction.

The value after reset of CANi Mailbox is undefined.

Write to the CiMBj register only when the associated CiMCTLj register is "H00" and the corresponding mailbox is not processing an abort request.

Refer to Table 34.5 for detailed addresses.

Table 34.5 CANi Mailbox Memory Mapping (i = 0, 1)

Address		Message Content
CAN0	CAN1	Memory Mapping
H'E6E80000 + 16 × j + 0	H'E6E88000 + 16 × j + 0	IDE, RTR, SID10 to SID6
H'E6E80000 + 16 × j + 1	H'E6E88000 + 16 × j + 1	SID5 to SID0, EID17, EID16
H'E6E80000 + 16 × j + 2	H'E6E88000 + 16 × j + 2	EID15 to EID8
H'E6E80000 + 16 × j + 3	H'E6E88000 + 16 × j + 3	EID7 to EID0
H'E6E80000 + 16 × j + 4	H'E6E88000 + 16 × j + 4	—
H'E6E80000 + 16 × j + 5	H'E6E88000 + 16 × j + 5	Data length code (DLC)
H'E6E80000 + 16 × j + 6	H'E6E88000 + 16 × j + 6	Data byte 0
H'E6E80000 + 16 × j + 7	H'E6E88000 + 16 × j + 7	Data byte 1
:	:	:
H'E6E80000 + 16 × j + 13	H'E6E88000 + 16 × j + 13	Data byte 7
H'E6E80000 + 16 × j + 14	H'E6E88000 + 16 × j + 14	Time stamp upper byte
H'E6E80000 + 16 × j + 15	H'E6E88000 + 16 × j + 15	Time stamp lower byte

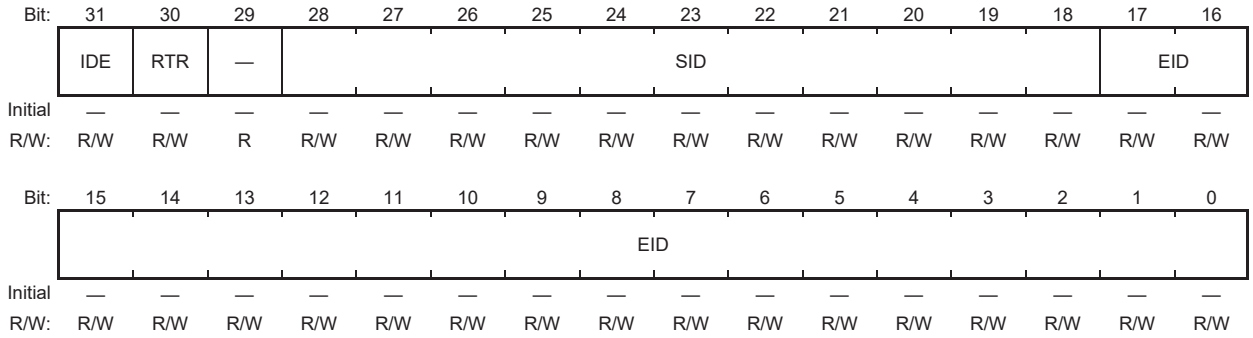
Table 34.6 CAN Data Frame Construction

SID10 to SID6	SID5 to SID0	EID17 to EID16	EID15 to EID8	EID7 to EID0	DLC3 to DLC0	DATA0	DATA1	…	DATA7

The previous value of each mailbox is retained unless a new message is received.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)

CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)



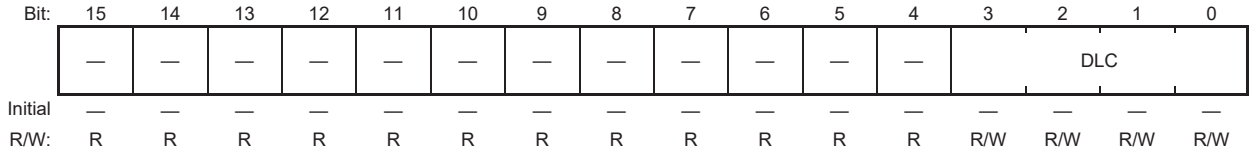
<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31	IDE	Undefined	R/W	ID Extension Bit*1 The IDE bit sets the ID format of standard IDs or extended IDs. The IDE bit is enabled when the IDFM bit in the CiCTLR register is "10" (mixed ID mode). When the IDFM bit is "10", the IDE bit specifies the following operation. Receive mailbox receives only ID format specified by the IDE bit. Transmit mailbox transmits with ID format specified by the IDE bit. Receive FIFO mailbox receives messages with the standard ID, extended ID, or both IDs specified by the IDE bit in registers CiFIDCR0 and CiFIDCR1. Transmit FIFO mailbox transmits messages with the standard ID or extended ID specified by the IDE bit in the relevant transmitting message. 0: Standard ID 1: Extended ID
30	RTR	Undefined	R/W	Remote Frame Request Bit The RTR bit sets the frame format of data frames or remote frames. This bit specifies the following operation: Receive mailbox receives only frames with the format specified by the RTR bit. Transmit mailbox transmits according to the frame format specified by the RTR bit. Receive FIFO mailbox receives the data frame, remote frame, or both frames specified by the RTR bit in registers CiFIDCR0 and CiFIDCR1. Transmit FIFO mailbox transmits the data frame or remote frame specified by the RTR bit in the relevant transmitting message. 0: Data frame 1: Remote frame
29	—	Undefined	R	Reserved bit The reset value is undefined. The write value should be "0". This bit is read as "0" after "0" is written to.
28 to 18	SID	Undefined	R/W	Standard ID Bits The SID bit sets the standard ID of data frames and remote frames. The SID bit is used to transmit or receive both standard ID and extended ID messages. 0: Corresponding SID bit is "0" 1: Corresponding SID bit is "1"

Bit	Symbol	Initial Value	R/W	Description
17 to 0	EID	Undefined	R/W	Extended ID Bits*2 The EID bit sets the extended ID of data frames and remote frames. The EID bit is used to transmit or receive extended ID messages. 0: Corresponding EID bit is "0" 1: Corresponding EID bit is "1"

Notes: 1. When the IDFM bit is not "10", it should be written with "0".
2. If the mailbox has received a standard ID message, the EID bit in the mailbox is undefined.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)
CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)

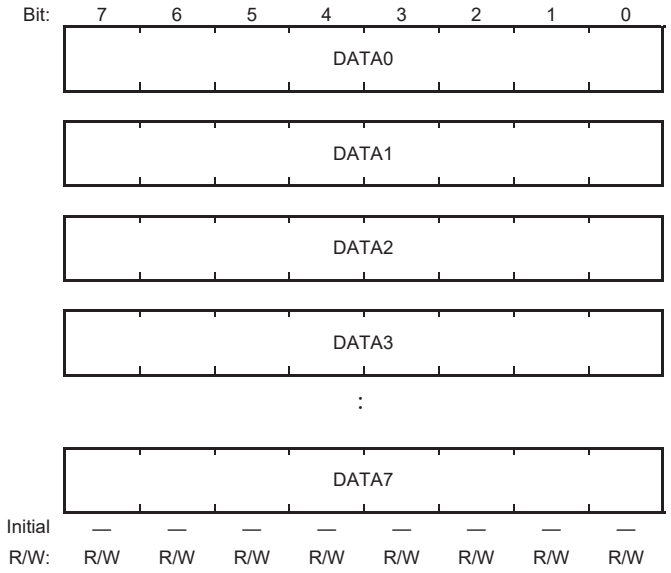


<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
15 to 4	—	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
3 to 0	DLC	Undefined	R/W	Data Length Code Bits* The DLC is used to set the number of data bytes to be transmitted in a data frame. When data is requested using a remote frame, the number of data bytes to be requested is set. When a data frame is received, the number of received data bytes is stored. When a remote frame is received, the number of requested data bytes is stored. 0000: Data length = 0 byte 0001: Data length = 1 byte 0010: Data length = 2 bytes 0011: Data length = 3 bytes 0100: Data length = 4 bytes 0101: Data length = 5 bytes 0110: Data length = 6 bytes 0111: Data length = 7 bytes 1xxx: Data length = 8 bytes Legend: *x* represents any value.

Note: * If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)
CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)

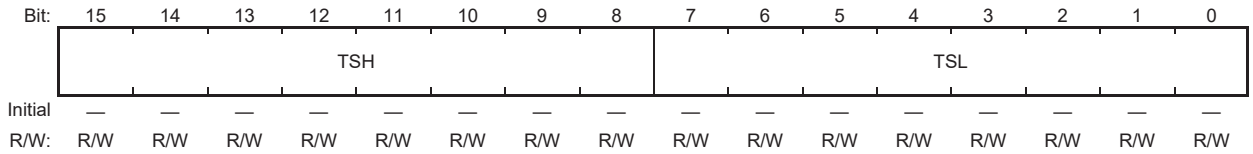


<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	DATA0 to 7	Undefined	R/W	Data Bytes 0 to 7*1*2 DATA0 to DATA7 store the transmitted or received CAN message data. Transmission or reception starts from DATA0. The bit order on the CAN bus is MSB first, and transmission or reception starts from bit 7.

Notes: 1. If the mailbox has received a message with n bytes less than 8 bytes, the values of DATAn to DATA7 in the mailbox are undefined.
2. If the mailbox has received a remote frame, the previous values of DATA0 to DATA7 in the mailbox are retained.

CAN0 Mailbox Register 0 to 63 (C0MB0 to 63)
CAN1 Mailbox Register 0 to 63 (C1MB0 to 63)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
15 to 8	TSH	Undefined	R/W	Time Stamp Higher Byte TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.
7 to 0	TSL	Undefined	R/W	Time Stamp Lower Byte TSL and TSH store the counter value of the time stamp when received messages are stored in the mailbox.

34.3.8 CANi Mailbox Interrupt Enable Registers (CiMIER0 and CiMIER1) (i = 0, 1)

Interrupts can be enabled individually for each mailbox.

In normal mailbox mode (all bits) and in FIFO mailbox mode (bits 23 to 0 in the CiMIER1 register and all bits in the CiMIER0 register), each bit corresponds to the mailbox with the related number. These bits enable or disable transmission/reception complete interrupts for the corresponding mailboxes.

- Bit 0 in the CiMIER0 register corresponds to mailbox 0 (MB0).
- Bit 31 in the CiMIER0 register corresponds to mailbox 31 (MB31).
- Bit 0 in the CiMIER1 register corresponds to mailbox 32 (MB32).
- Bit 31 in the CiMIER1 register corresponds to mailbox 63 (MB63).

In FIFO mailbox mode, bits 29, 28, 25, and 24 of the CiMIER1 register specify whether transmit/receive FIFO interrupts are enabled/disabled and timing when interrupt requests are generated.

Write to registers CiMIER0 and CiMIER1 only when the associated CiMCTLj register (i = 0, 1) (j = 0 to 63) is "H'00" and the corresponding mailbox is not processing a transmission or reception abort request. In FIFO mailbox mode, change the bits in the CiMIER1 register for the associated FIFO only when:

— The TFE bit in the CiTFCR register is 0 and the TFEST bit is 1, and
— The RFE bit in the CiRFCR register is 0 and the RFEST bit is 1.

CAN0 Mailbox Interrupt Enable Register 1 (C0MIER1)
CAN1 Mailbox Interrupt Enable Register 1 (C1MIER1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB63	MB62	MB61	MB60	MB59	MB58	MB57	MB56	MB55	MB54	MB53	MB52	MB51	MB50	MB49	MB48
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB47	MB46	MB45	MB44	MB43	MB42	MB41	MB40	MB39	MB38	MB37	MB36	MB35	MB34	MB33	MB32
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Normal mailbox mode

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB63 to MB32	Undefined	R/W	Interrupt Enable Bits Bit 31 corresponds to mailbox 63 (MB63), and bit 0 corresponds to mailbox 32 (MB32). 0: Interrupt disabled 1: Interrupt enabled

- FIFO mailbox mode (CiMIER1 only)

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31, 30	MB63 MB62	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
29	MB61	Undefined	R/W	Receive FIFO Interrupt Generation Timing Control Bit* Receive FIFO interrupt request is generated 0: Every time reception is completed 1: When receive FIFO becomes buffer warning by completion of reception
28	MB60	Undefined	R/W	Receive FIFO Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled
27, 26	MB59 MB58	Undefined	R	Reserved bits The reset value is undefined. The write value should be "0". These bits are read as "0" after "0" is written to.
25	MB57	Undefined	R/W	Transmit FIFO Interrupt Generation Timing Control Bit Transmit FIFO interrupt request is generated 0: Every time transmission is completed 1: When transmit FIFO becomes empty due to completion of transmission
24	MB56	Undefined	R/W	Transmit FIFO Interrupt Enable Bit 0: Interrupt disabled 1: Interrupt enabled
23 to 0	MB55 to MB32	Undefined	R/W	Interrupt Enable Bits Bit 23 corresponds to mailbox 55 (MB55), and bit 0 corresponds to mailbox 32 (MB32). 0: Interrupt disabled 1: Interrupt enabled

Note: * No interrupt request is generated when the receive FIFO becomes buffer warning from full. “Buffer warning” indicates a state in which the third unread message is stored in the receive FIFO.

CAN0 Mailbox Interrupt Enable Register 0 (C0MIER0)
CAN1 Mailbox Interrupt Enable Register 0 (C1MIER0)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MB31	MB30	MB29	MB28	MB27	MB26	MB25	MB24	MB23	MB22	MB21	MB20	MB19	MB18	MB17	MB16
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MB15	MB14	MB13	MB12	MB11	MB10	MB9	MB8	MB7	MB6	MB5	MB4	MB3	MB2	MB1	MB0
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
31 to 0	MB31 to MB0	Undefined	R/W	Interrupt Enable Bits Bit 31 corresponds to mailbox 31 (MB31), and bit 0 corresponds to mailbox 0 (MB0). 0: Interrupt disabled 1: Interrupt enabled

34.3.9 CANi Message Control Register j (CiMCTLj) (i = 0, 1; j = 0 to 63)

Write to the CiMCTLj register in CAN operation mode or CAN halt mode.

Do not use registers CiMCTL56 to CiMCTL63 in FIFO mailbox mode.

CAN0 Message Control Register 0 to 63 (C0MCTL0 to C0MCTL63)
CAN1 Message Control Register 0 to 63 (C1MCTL0 to C1MCTL63)

Registers CiMCTL32 to CiMCTL63

- Transmit mailbox setting enabled (When the TRMREQ bit is "1" and the RECREQ bit is "0")

Bit:	7	6	5	4	3	2	1	0
	TRM REQ	REC REQ	—	ONE SHOT	—	TRM ABT	TRMA CTIVE	SENT DATA
Initial	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R	R/W	R	R/W

- Receive mailbox setting enabled (When the TRMREQ bit is "0" and the RECREQ bit is "1")

Bit:	7	6	5	4	3	2	1	0
	TRM REQ	REC REQ	—	ONE SHOT	—	MSG LOST	INVAL DATA	NEWD ATA
Initial	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R/W	R	R/W	R	R/W

Registers CiMCTL0 to CiMCTL31

Bit:	7	6	5	4	3	2	1	0
	—	REC REQ	—	—	—	MSG LOST	INVAL DATA	NEWD ATA
Initial	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R/W	R	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	TRMREQ	0	R/W	Transmit Mailbox Request Bit*2*4 The TRMREQ bit selects transmit modes shown in Table 34.11. When TRMREQ bit is set to "1", the corresponding mailbox is configured for transmission of a data frame or a remote frame. When TRMREQ bit is set to "0", the corresponding mailbox is not configured for transmission of a data frame or a remote frame. If the TRMREQ bit is changed from "1" to "0" to cancel the corresponding transmission request, either the TRMABT or SENTDATA bit is set to "1". When setting the TRMREQ bit to "1", do not set the RECREQ bit to "1". To change the configuration of a mailbox from reception to transmission, first abort the reception and then set bits NEWDATA and MSGLOST to "0" before changing to transmission. 0: Not configured for transmission 1: Configured for transmission
	—	0	R	Reserved bit (Registers CiMCTL0 to CiMCTL31) This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
6	RECREQ	0	R/W	Receive Mailbox Request Bit*2*4*5 The RECREQ bit selects receive modes shown in Table 34.11. When the RECREQ bit is set to "1", the corresponding mailbox is configured for reception of a data frame or a remote frame. When the RECREQ bit is set to "0", the corresponding mailbox is not configured for reception of a data frame or a remote frame. Due to hardware protection the RECREQ bit cannot be set to "0" by writing "0" by a program during the following period. Hardware protection is started From the acceptance filter procedure. (the beginning of CRC field) Hardware protection is released For the mailbox that is specified to receive the incoming message, after the received data is stored into the mailbox or a CAN bus error occurs. (i.e. a maximum period of hardware protection is from the beginning of CRC field to the end of the 7th bit of EOF.) For the other mailboxes, after the acceptance filter procedure. If no mailbox is specified to receive the message, after the acceptance filter procedure. When setting the RECREQ bit to "1", do not set "1" to the TRMREQ bit. To change the configuration of a mailbox from transmission to reception, first abort the transmission and then set bits SENTDATA and TRMABT to "0" before changing to reception. 0: Not configured for reception 1: Configured for reception
5	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.

Bit	Symbol	Initial Value	R/W	Description
4	ONESHOT	0	R/W	One-shot Enable Bit*3 The ONESHOT bit can be used in the following two ways, receive mode and transmit mode: One-Shot Receive Mode When the ONESHOT bit is set to "1" in receive mode (RECREQ bit = "1" and TRMREQ bit = "0"), the mailbox receives a message only one time. The mailbox does not behave as a receive mailbox after having received a message one time. The behavior of bits NEWDATA and INVALDATA is the same as in normal reception mode. In one-shot receive mode, the MSGLOST bit is not set to "1". To set the ONESHOT bit to "0", first write "0" to the RECREQ bit and ensure that it has been set to "0". One-Shot Transmit Mode When the ONESHOT bit is set to "1" in transmit mode (RECREQ bit = "0" and TRMREQ bit = "1"), the CAN module transmits a message only one time. The CAN module does not transmit the message again if a CAN bus error or CAN bus arbitration lost occurs. When transmission is completed, the SENTDATA bit is set to "1". If transmission is not completed due to a CAN bus error or CAN bus arbitration lost, the TRMABT bit is set to "1". Set the ONESHOT bit to "0" after the SENTDATA or TRMABT bit is set to "1". 0: One-shot reception or one-shot transmission disabled 1: One-shot reception or one-shot transmission enabled
	—	0	R	Reserved bit (Registers CiMCTL0 to CiMCTL31) This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
3	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
2	TRMABT	0	R/W	Transmission Abort Complete Flag (Transmit mailbox setting enabled)*1*2 The TRMABT bit is set to "1" in the following cases: Following a transmission abort request, when the transmission abort is completed before starting transmission. Following a transmission abort request, when the CAN module detects CAN bus arbitration lost or a CAN bus error. In one-shot transmission mode (RECREQ bit = "0", TRMREQ bit = "1", and ONESHOT bit = "1"), when the CAN module detects CAN bus arbitration lost or a CAN bus error. The TRMABT bit is not set to "1" when data transmission is completed. In this case, the SENTDATA bit is set to "1". The TRMABT bit is set to "0" by writing "0" by a program. 0: Transmission has started, transmission abort failed because transmission is completed, or transmission abort is not requested 1: Transmission abort is completed

Bit	Symbol	Initial Value	R/W	Description
	MSGLOST	0	R/W	Message Lost Flag (Receive mailbox setting enabled)*1*2 The MSGLOST bit is set to "1" when the mailbox is overwritten or overrun by a new received message while the NEWDATA bit is "1". The MSGLOST bit is set to "1" at the end of the 6th bit of EOF. The MSGLOST bit is set to "0" by writing "0" by a program. In both overwrite and overrun modes, the MSGLOST bit is not set to "0" by writing "0" by a program during the 5 peripheral clock (clkp1) cycles following the 6th bit of EOF. 0: Message is not overwritten or overrun 1: Message is overwritten or overrun
1	TRMACTIVE	0	R	Transmission-in-Progress Status Flag (Transmit mailbox setting enabled) The TRMACTIVE bit is set to "1" when the corresponding mailbox of the CAN module begins transmitting a message. The TRMACTIVE is set to "0" when the CAN module has lost CAN bus arbitration, a CAN bus error occurs, or data transmission is completed. 0: Transmission is pending or transmission is not requested 1: From acceptance of transmission request to completion of transmission, or error/arbitration lost
	INVALDATA	0	R	Reception-in-Progress Status Flag (Receive mailbox setting enabled) After the completion of a message reception, the INVALDATA bit is set to "1" while the received message is being updated into the corresponding mailbox. The INVALDATA bit is set to "0" immediately after the message has been stored. If the mailbox is read while the INVALDATA bit is "1", the data is undefined. 0: Message valid 1: Message being updated
0	SENTDATA	0	R/W	Transmission Complete Flag (Transmit mailbox setting enabled)*1*2 The SENTDATA bit is set to "1" when data transmission from the corresponding mailbox is completed. The SENTDATA bit is set to "0" by writing "0" by a program. To set the SENTDATA bit to "0", first set the TRMREQ bit to "0". Bits SENTDATA and TRMREQ cannot be set to "0" simultaneously. To transmit a new message from the corresponding mailbox, set the SENTDATA bit to "0". 0: Transmission is not completed (pending) 1: Transmission is completed (success)
	NEWDATA	0	R/W	Reception Complete Flag (Receive mailbox setting enabled)*1*2 The NEWDATA bit is set to "1 when a new message is being stored or has been stored to the mailbox. The timing for setting this bit to "1" is simultaneous with the INVALDATA bit. The NEWDATA bit is set to "0" by writing "0" by a program. The NEWDATA bit is not set to "0" by writing "0" by a program while the related INVALDATA bit is "1". 0: No data has been received or "0" is written to the NEWDATA bit 1: A new message is being stored or has been stored to the mailbox

Notes: 1. Writing "0" only. Writing "1" has no effect.
2. When writing "0" to bits NEWDATA, SENTDATA, MSGLOST, TRMABT, RECREQ, and TRMREQ by a program, only the specified bit is set to "0" and the other bits are set to "1".
3. To enter one-shot receive mode, write "1" to the ONESHOT bit at the same time as setting the RECREQ bit to "1".

To exit one-shot receive mode, write "0" to the ONESHOT bit after writing "0" to the RECREQ bit and confirming it has been set to "0".

To enter one-shot transmit mode, write "1" to the ONESHOT bit at the same time as setting the TRMREQ bit to "1".

To exit one-shot transmit mode, write "0" to the ONESHOT bit after the message has been transmitted or aborted.

4. Do not set both the RECREQ and TRMREQ bits to "1".
5. When setting the RECREQ bit to "0", set bits MSGLOST, NEWDATA, RECREQ to "0" simultaneously.

34.3.10 CANi Receive FIFO Control Register (CiRFCR) (i = 0, 1)

Write to the CiRFCR registers in CAN operation mode or CAN halt mode.

CAN0 Receive FIFO Control Register (C0RFCR)
CAN1 Receive FIFO Control Register (C1RFCR)

Bit:	7	6	5	4	3	2	1	0
	RFEST	RFWST	RFFST	RFMLF	RFUST			RFE
Initial	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

<After Reset: H'80>

Bit	Symbol	Initial Value	R/W	Description
7	RFEST	1	R	Receive FIFO Empty Status Flag The RFEST bit is set to "1" (no unread message in receive FIFO) when the number of unread messages in the receive FIFO is "0". The RFEST bit is set to "1" when the RFE bit is set to "0". The RFEST bit is set to "0" (unread message in receive FIFO) when the number of unread messages in the receive FIFO is one or more. 0: Unread message in receive FIFO 1: No unread message in receive FIFO
6	RFWST	0	R	Receive FIFO Buffer Warning Status Flag The RFWST bit is set to "1" (receive FIFO is buffer warning) when the number of unread messages in the receive FIFO is 3. The RFWST bit is "0" (receive FIFO is not buffer warning) when the number of unread messages in the receive FIFO is less than 3 or equal to 4. The RFWST bit is set to "0" when the RFE bit is "0". 0: Receive FIFO is not buffer warning 1: Receive FIFO is buffer warning (3 unread messages)
5	RFFST	0	R	Receive FIFO Full Status Flag The RFFST bit is set to "1" (receive FIFO is full) when the number of unread messages in the receive FIFO is 4. The RFFST bit is "0" (receive FIFO is not full) when the number of unread messages in the receive FIFO is less than 4. The RFFST bit is set to "0" when the RFE bit is "0". 0: Receive FIFO is not full 1: Receive FIFO full (4 unread messages)
4	RFMLF	0	R	Receive FIFO Message Lost Flag The RFMLF bit is set to "1" (receive FIFO message lost has occurred) when the receive FIFO receives a new message and the receive FIFO is full. The timing for setting this bit to "1" is at the end of the 6th bit of EOF. The RFMLF bit is set to "0" by writing "0" by a program (writing "1" has no effect). In both overwrite and overrun modes, the RFMLF bit cannot be set to "0" (receive FIFO message lost has not occurred) by writing "0" by a program due to hardware protection during the five cycles of peripheral clock (clkp1) following the 6th bit of EOF, if the receive FIFO is full and determined to receive the message. 0: No receive FIFO message lost has occurred 1: Receive FIFO message lost has occurred

Bit	Symbol	Initial Value	R/W	Description
3 to 1	RFUST	000	R	Receive FIFO Unread Message Number Status Flag The RFUST bit indicates the number of unread messages in the receive FIFO. The value of the RFUST bit is initialized to "000" when the RFE bit is set to "0". 000: No unread message 001: 1 unread message 010: 2 unread messages 011: 3 unread messages 100: 4 unread messages 101: Reserved 110: Reserved 111: Reserved
0	RFE	0	R/W	Receive FIFO Enable Bit When the RFE bit is set to "1", the receive FIFO is enabled. When this bit is set to "0", the receive FIFO is disabled for reception and becomes empty (RFEST bit = "1"). Do not set this bit to "1" in normal mailbox mode (MBM bit in the CiCTLR register = "0"). Due to hardware protection, the RFE bit is not set to "0" by writing "0" by a program during the following period: The hardware protection is started From the acceptance filter procedure (the beginning of CRC field) The hardware protection is released If the receive FIFO is specified to receive the incoming message, after the received data is stored into the receive FIFO or a CAN bus error occurs. (i.e. maximum period of hardware protection is from the beginning of CRC field to the end of 7th bit of EOF.) If the receive FIFO is not specified to receive the message, after the acceptance filter procedure. 0: Receive FIFO disabled 1: Receive FIFO enabled

Figure 34.2 shows the receive FIFO mailbox operation.

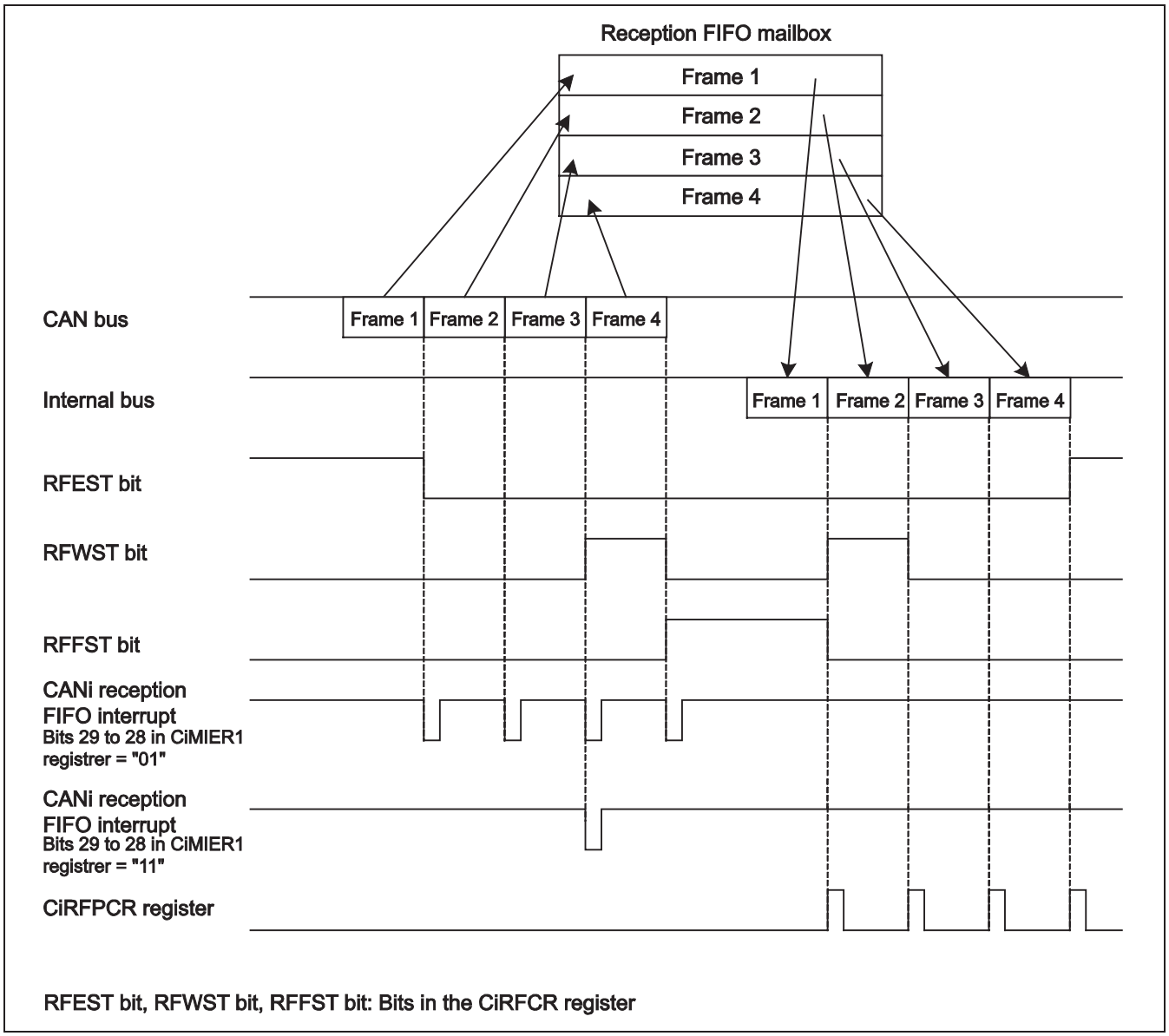


Figure 34.2 Receive FIFO Mailbox Operation
(Bits 29 and 28 in CiMIER1 Register = "01" and "11") (i = 0, 1)

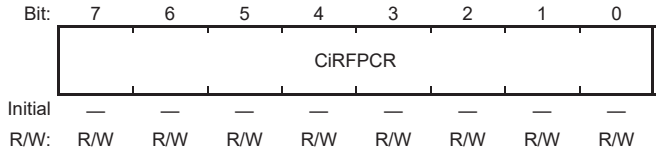
34.3.11 CANi Receive FIFO Pointer Control Register (CiRFPCR) (i = 0, 1)

When the receive FIFO is not empty, write "H'FF" to the CiRFPCR register by a program to increment the CPU-side pointer for the receive FIFO to the next mailbox location.

Do not write to the CiRFPCR register when the RFE bit in the CiRFCR register is "0" (receive FIFO disabled).

Both the CAN-side pointer and the CPU-side pointer are incremented when a new message is received and the RFFST bit is "1" (receive FIFO is full) in overwrite mode. When the RFMLF bit is "1" in this condition, the CPU-side pointer cannot be incremented by writing to the CiRFPCR register by a program.

CAN0 Receive FIFO Pointer Control Register (C0RFPCR)
CAN1 Receive FIFO Pointer Control Register (C1RFPCR)



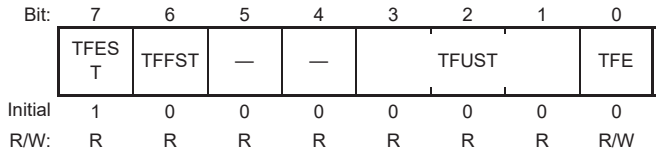
<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiRFPCR	Undefined	R/W	The CPU-side pointer for the receive FIFO is incremented by writing "H'FF"

34.3.12 CANi Transmit FIFO Control Register (CiTFCR) (i = 0, 1)

Write to the CiTFCR register in CAN operation mode or CAN halt mode.

CAN0 Transmit FIFO Control Register (C0TFCR)
CAN1 Transmit FIFO Control Register (C1TFCR)



<After Reset: H'80>

Bit	Symbol	Initial Value	R/W	Description
7	TFEST	1	R	Transmit FIFO Empty Status Bit The TFEST bit is set to "1" (no message in transmit FIFO) when the number of unsent messages in the transmit FIFO is "0". The TFEST bit is set to "1" when transmission from the transmit FIFO has been aborted. The TFEST bit is set to "0" (message in transmit FIFO) when the number of unsent messages in the transmit FIFO is not "0". 0: Unsent message in transmit FIFO 1: No unsent message in transmit FIFO

Bit	Symbol	Initial Value	R/W	Description
6	TFFST	0	R	Transmit FIFO Full Status Bit The TFFST bit is set to "1" (transmit FIFO is full) when the number of unsent messages in the transmit FIFO is 4. The TFFST bit is set to "0" (transmit FIFO is not full) when the number of unsent messages in the transmit FIFO is less than 4. The TFFST bit is set to "0" when transmission from the transmit FIFO has been aborted. 0: Transmit FIFO is not full 1: Transmit FIFO is full (4 unsent messages)
5, 4	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
3 to 1	TFUST	000	R	Transmit FIFO Unsent Message Number Status Bits The TFUST bit indicates the number of unsent messages in the transmit FIFO. After the TFE bit is set to "0", the value of the TFUST bit is initialized to "000" when transmission abort or transmission is completed. 000: No unsent message 001: 1 unsent message 010: 2 unsent messages 011: 3 unsent messages 100: 4 unsent messages 101: Reserved 110: Reserved 111: Reserved
0	TFE	0	R/W	Transmit FIFO Enable Bit When the TFE bit is set to "1", the transmit FIFO is enabled. When the TFE bit is set to "0", the transmit FIFO becomes empty (TFEST bit = "1") and then unsent messages from the transmit FIFO are lost as described below: If a message from the transmit FIFO is not scheduled for the next transmission or during transmission. Following the completion of transmission, a CAN bus error, CAN bus arbitration lost, or entry to CAN halt mode if a message from the transmit FIFO is scheduled for the next transmission or already during transmission. Before setting the TFE bit to set to "1" again, ensure that the TFEST bit has been set to "1". After setting the TFE bit to "1", write transmit data into the CiMB56 register. Do not set the TFE bit to "1" in normal mailbox mode (MBM bit in the CiCTLR register = "0"). 0: Transmit FIFO disabled 1: Transmit FIFO enabled

Figure 34.3 shows the transmit FIFO mailbox operation.

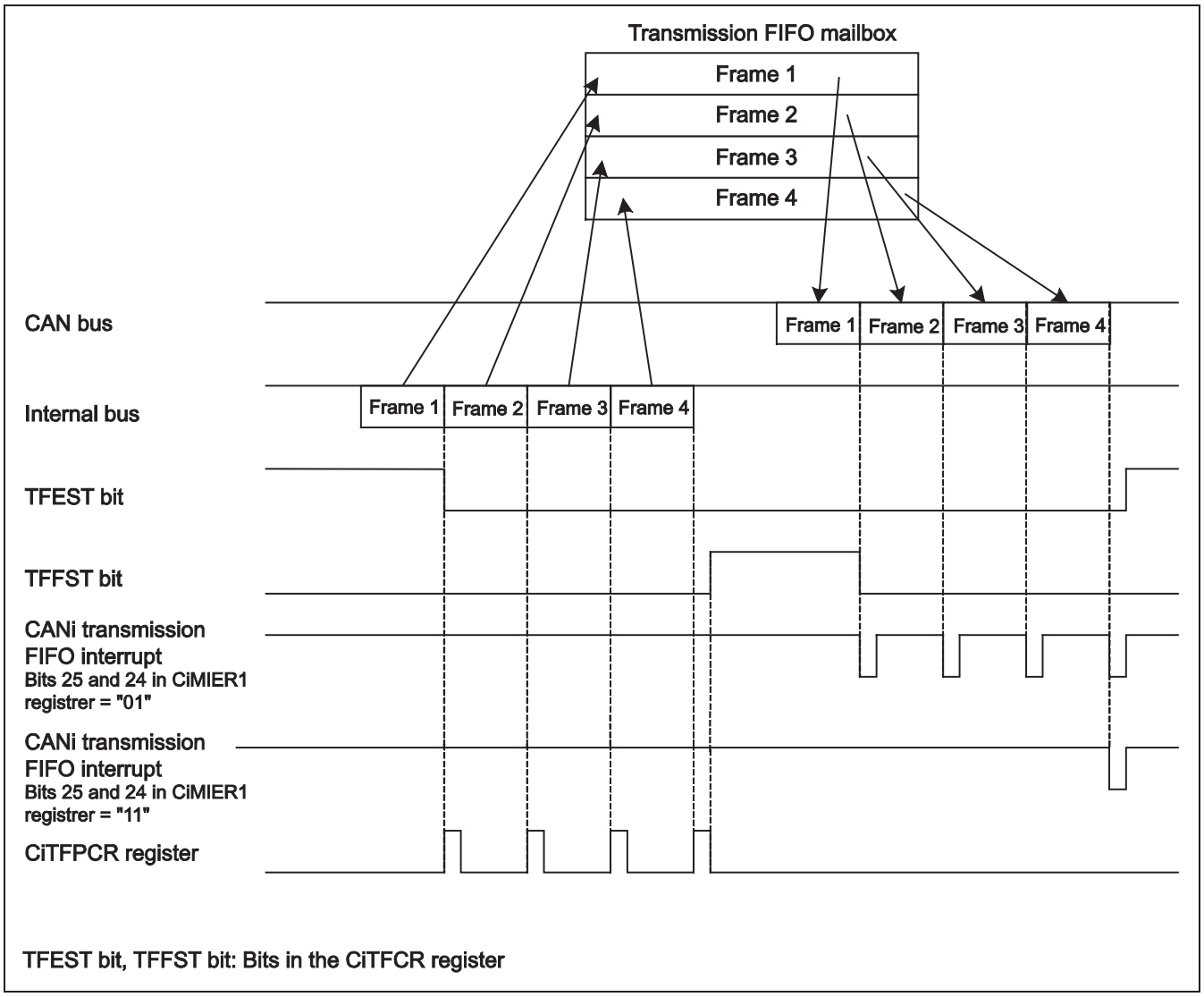


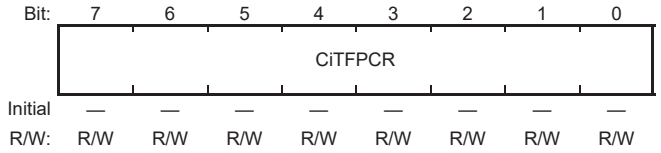
Figure 34.3 Transmit FIFO Mailbox Operation
(Bits 25 and 24 in CiMIER1 Register = "01" and "11") (i = 0, 1)

34.3.13 CANi Transmit FIFO Pointer Control Register (CiTFPCR) (i = 0, 1)

When the transmit FIFO is not full, write "H'FF" to the CiTFPCR register by a program to increment the CPU-side pointer for the transmit FIFO to the next mailbox location.

Do not write to the CiTFPCR register when the TFE bit in the CiTFPCR register is "0" (transmit FIFO disabled).

CAN0 Transmit FIFO Pointer Control Register (C0TFPCR)
CAN1 Transmit FIFO Pointer Control Register (C1TFPCR)

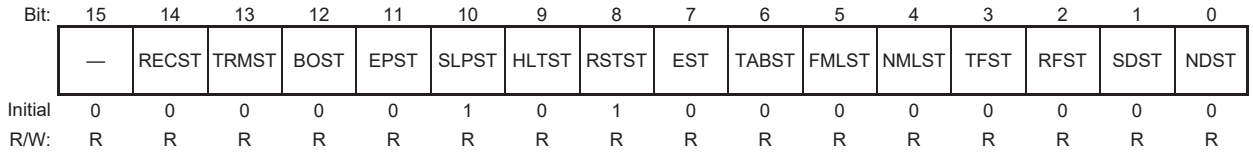


<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiTFPCR	Undefined	R/W	The CPU-side pointer for the transmit FIFO is incremented by writing "H'FF"

34.3.14 CANi Status Register (CiSTR) (i = 0, 1)

CAN0 Status Register (C0STR)
CAN1 Status Register (C1STR)



<After Reset: H'0500>

Bit	Symbol	Initial Value	R/W	Description
15	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
14	RECST	0	R	Receive Status Flag (receiver) The RECST bit is set to "1" when the CAN module performs as a receiver node. The RECST bit is set to "0" when the CAN module performs as a transmitter node or is in bus-idle state. 0: Bus idle or transmission in progress 1: Reception in progress
13	TRMST	0	R	Transmit Status Flag (transmitter) The TRMST bit is set to "1" when the CAN module performs as a transmitter node or is in the bus-off state. The TRMST bit is set to "0" when the CAN module performs as a receiver node or is in bus-idle state. 0: Bus idle or reception in progress 1: Transmission in progress or in bus-off state

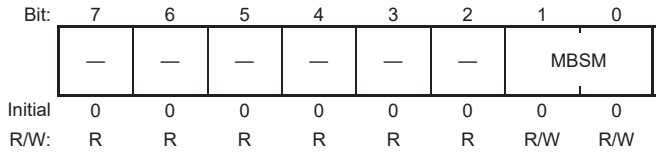
Bit	Symbol	Initial Value	R/W	Description
12	BOST	0	R	Bus-Off Status Flag The BOST bit is set to "1" when the value of the CiTECR register exceeds 255 and the CAN module is in the bus-off state (TEC ≥ 256). The BOST bit is set to "0" when the CAN module is not in the bus-off state. 0: Not in bus-off state 1: In bus-off state
11	EPST	0	R	Error-Passive Status Flag The EPST bit is set to "1" when the value of the CiTECR or CiRECR register exceeds 127 and the CAN module is in error-passive state (128 ≤ TEC < 256 or 128 ≤ REC < 256). The EPST bit is set to "0" when the CAN module is not in the error-passive state. TEC indicates the value of the transmit error counter (CiTECR register) and REC indicates the value of the receive error counter (CiRECR register). 0: Not in error-passive state 1: In error-passive state
10	SLPST	1	R	CAN Sleep Status Flag The SLPST bit is set to "1" when the CAN module is in CAN sleep mode. The SLPST bit is set to "0" when the CAN module is not in CAN sleep mode. 0: Not in CAN sleep mode 1: In CAN sleep mode
9	HLTST	0	R	CAN Halt Status Flag The HLTST bit is set to "1" when the CAN module is in CAN halt mode. The HLTST bit is set to "0" when the CAN module is not in CAN halt mode. Even when the state is changed from CAN halt mode to CAN sleep mode, the HLTST bit remains "1". 0: Not in CAN halt mode 1: In CAN halt mode
8	RSTST	1	R	CAN Reset Status Flag The RSTST bit is set to "1" when the CAN module is in CAN reset mode. The RSTST bit is "0" when the CAN module is not in CAN reset mode. Even when the state is changed from CAN reset mode to CAN sleep mode, the RSTST bit remains "1". 0: Not in CAN reset mode 1: In CAN reset mode
7	EST	0	R	Error Status Flag The EST bit is "1" when at least one error is detected by the CiEIFR register regardless of the value of the CiEIER register. The EST bit is set to "0" when no error is detected by the CiEIFR register. 0: No error occurred 1: Error occurred
6	TABST	0	R	Transmission Abort Status Flag The TABST bit is set to "1" when at least one TRMABT bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The TABST bit is set to "0" when all TRMABT bits are "0". 0: No mailbox with TRMABT bit = "1" 1: Mailbox(es) with TRMABT bit = "1"

Bit	Symbol	Initial Value	R/W	Description
5	FMLST	0	R	FIFO Mailbox Message Lost Status Flag The FMLST bit is set to "1" when the RFMLF bit in the CiRFCR register is "1" regardless of the value of the CiMIER register. The FMLST bit is set to "0" when the RFMLF bit is "0". 0: RFMLF bit = "0" 1: RFMLF bit = "1"
4	NMLST	0	R	Normal Mailbox Message Lost Status Flag The NMLST bit is set to "1" when at least one MSGLOST bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The NMLST bit is set to "0" when all MSGLOST bit is "0". 0: No mailbox with MSGLOST bit = "1" 1: Mailbox(es) with MSGLOST bit = "1"
3	TFST	0	R	Transmit FIFO Status Flag The TFST bit is set to "1" when the transmit FIFO is not full. The TFST bit is set to "0" when the transmit FIFO is full. The TFST bit is set to "0" when normal mailbox mode is selected. 0: Transmit FIFO is full 1: Transmit FIFO is not full
2	RFST	0	R	Receive FIFO Status Flag The RFST bit is set to "1" when the receive FIFO is not empty. The RFST bit is set to "0" when the receive FIFO is empty. The RFST bit is set to "0" when normal mailbox mode is selected. 0: No message in receive FIFO 1: Message in receive FIFO
1	SDST	0	R	SENTDATA Status Flag The SDST bit is set to "1" when at least one SENTDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The SDST bit is set to "0" when all SENTDATA bits are "0". 0: No mailbox with SENTDATA bit = "1" 1: Mailbox(es) with SENTDATA bit = "1"
0	NDST	0	R	NEWDATA Status Flag The NDST bit is set to "1" when at least one NEWDATA bit in the CiMCTLj register is "1" regardless of the value of the CiMIER register. The NDST bit is set to "0" when all NEWDATA bits are "0". 0: No mailbox with NEWDATA bit = "1" 1: Mailbox(es) with NEWDATA bit = "1"

34.3.15 CANi Mailbox Search Mode Register (CiMSMR) (i = 0, 1)

Write to the CiMSMR register in CAN operation mode or CAN halt mode.

CAN0 Mailbox Search Mode Register (C0MSMR)
CAN1 Mailbox Search Mode Register (C1MSMR)



<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
1, 0	MBSM	00	R/W	Mailbox Search Mode Select Bits The MBSM bit selects the search mode for the mailbox search function. When the MBSM bit is "00", receive mailbox search mode is selected. In this mode, the search targets are the NEWDATA bit in the CiMCTLj register (j = 0 to 63) for the normal mailbox and the RFEST bit in the CiRFCR register. When the MBSM bit is "01", transmit mailbox search mode is selected. In this mode, targets the SENTDATA bit in the CiMCTLj register. When the MBSM bit is "10", message lost search mode is selected. In this mode, targets the MSGLOST bit in the CiMCTLj register for the normal mailbox and the RFMLF bit in the CiRFCR register. When the MBSM bit is "11", channel search mode is selected. In this mode, the search target is the CiCSSR register. Refer to section 34.3.17, CANi Channel Search Support Register (CiCSSR) (i = 0, 1). 00: Receive mailbox search mode 01: Transmit mailbox search mode 10: Message lost search mode 11: Channel search mode

34.3.16 CANi Mailbox Search Status Register (CiMSSR) (i = 0, 1)

CAN0 Mailbox Search Status Register (C0MSSR)
CAN1 Mailbox Search Status Register (C1MSSR)

Bit:	7	6	5	4	3	2	1	0
	SEST	—	MBNST					
Initial	1	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

<After Reset: H'80>

Bit	Symbol	Initial Value	R/W	Description
7	SEST	1	R	Search Result Status Bit The SEST bit is set to "1" when no corresponding mailbox is found after searching all mailboxes. For example, in transmit mailbox search mode, the SEST bit is set to "1" when no SENTDATA bit for mailboxes is "1". The SEST bit is set to "0" when at least one SENTDATA bit is "1". When the SEST bit is "1", the value of the MBNST bits is undefined. 0: Search result found 1: No search result
6	—	0	R	Reserved bit This bit is always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to this bit.
5 to 0	MBNST	000000	R	Search Result Mailbox Number Status Bits The MBNST bit outputs the smallest mailbox number that is searched in each mode of the CiMSMR register. In receive mailbox, transmit mailbox, and message lost search modes, the value of the mailbox i.e., the search result to be output, is updated as described below: When the NEWDATA, SENTDATA or MSGLOST bit for the output mailbox is set to "0". When the NEWDATA, SENTDATA or MSGLOST bit for a higher-priority mailbox is set to "1". In receive mailbox search and message lost search modes, the receive FIFO (mailbox [60]) is output when the receive FIFO is not empty and there are no unread received messages or no lost messages in any of the normal mailboxes (mailboxes [0] to [55]). In transmit mailbox search mode, the transmit FIFO (mailbox [56]) is not output. Table 34.7 lists the behavior of MBNST bit in FIFO mailbox mode. In channel search mode, the MBNST bit outputs the corresponding channel number. After the CiMSSR register is read by a program, the next target channel number is output.

Table 34.7 Operation of MBNST Bit in FIFO Mailbox Mode

MBSM Bit	Mailbox [56] (Transmit FIFO)	Mailbox [60] (Receive FIFO)
"00"	Mailbox [56] is not output.	Mailbox [60] is output when no NEWDATA bit for the normal mailbox is set to "1" and the receive FIFO is not empty.
"01"		Mailbox [60] is not output.
"10"		Mailbox [60] is output when no MSGLOST bit for the normal mailbox is set to "1" and the RFMLF bit is set to "1" (receive FIFO message lost has occurred) in the receive FIFO.
"11"		Mailbox [60] is not output.

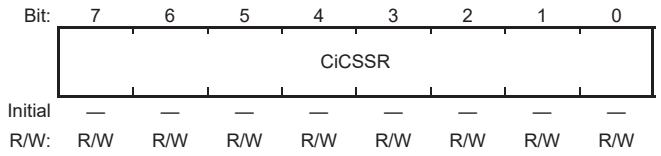
34.3.17 CANi Channel Search Support Register (CiCSSR) (i = 0, 1)

The bits in the CiCSSR register, which are set to "1", are encoded by an 8/3 encoder (the lower bit position, the higher priority) and output to the MBNST bits in the CiMSSR register.

The CiMSSR register outputs the updated value whenever the CiMSSR register is read by a program.

Write to the CiCSSR register only when the MBSM bit in the CiMSMR register is "11" (channel search mode). Write to this register in CAN operation mode or CAN halt mode.

CAN0 Channel Search Support Register (C0CSSR)
CAN1 Channel Search Support Register (C1CSSR)



<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiCSSR	Undefined	R/W	When the value for the channel search is input, the channel number is output to the CiMSSR register.

Figure 34.4 shows the write and read of registers CiCSSR and CiMSSR.

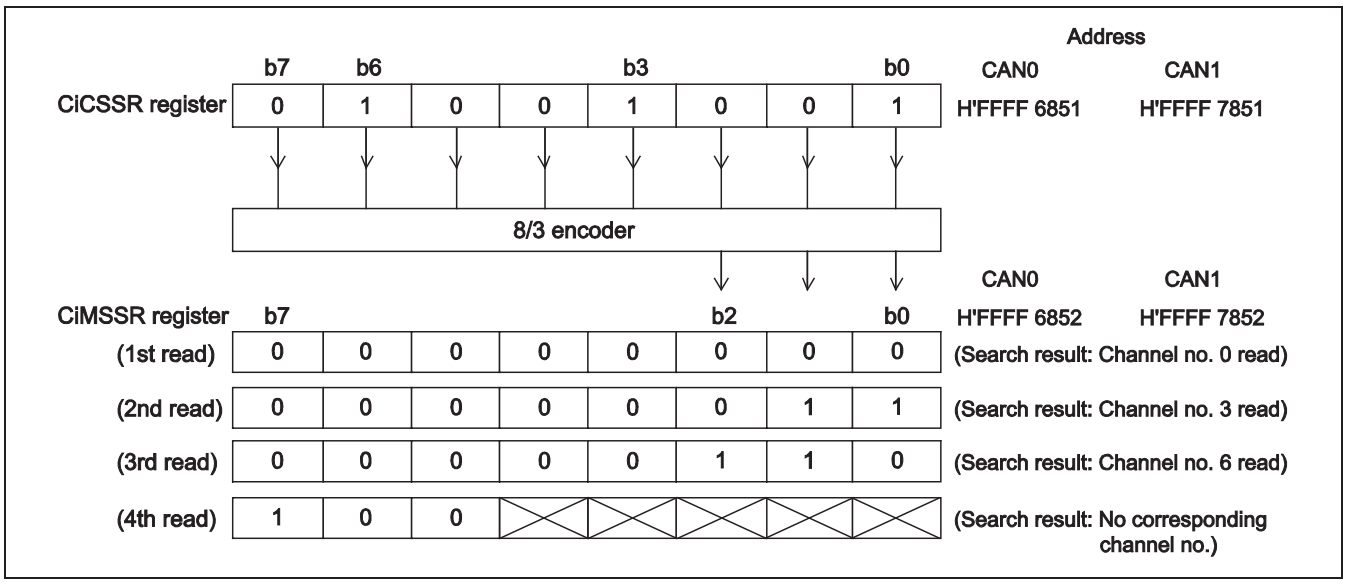


Figure 34.4 Write and Read of Registers CiCSSR and CiMSSR (i = 0, 1)

The value of the CiCSSR register is also updated whenever the CiMSSR register is read. When the CiCSSR register is read, the value before the 8/3 encoder conversion is read.

34.3.18 CANi Acceptance Filter Support Register (CiAFSR) (i = 0, 1)

The acceptance filter support unit (ASU) can be used for data table (8 bits × 256) search. In the data table, all standard IDs created by the user are set to be valid/invalid in bit units. When the CAFSR register is written with the 16-bit unit data including the SID bit in the CiMBj register (j = 0 to 63), in which a received ID is stored, a decoded row (byte offset) position and column (bit) position for data table search can be read. The ASU can be used for standard (11-bit) IDs only.

The ASU is enabled in the following cases:

- When the ID to receive cannot be masked by the acceptance filter.
  (Example) IDs to receive: H'078, H'087, H'111
- When there are too many IDs to receive and software filtering time is expected to be shortened.

Write to the CiAFSR register in CAN operation mode or CAN halt mode.

CAN0 Acceptance Filter Support Register (C0AFSR)
CAN1 Acceptance Filter Support Register (C1AFSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CiAFSR															
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: Undefined>

Bit	Symbol	Initial Value	R/W	Description
15 to 0	CiAFSR	Undefined	R/W	After the standard ID of a received message is written, the value converted for data table search can be read.

Figure 34.5 shows the write and read of CiAFSR register.

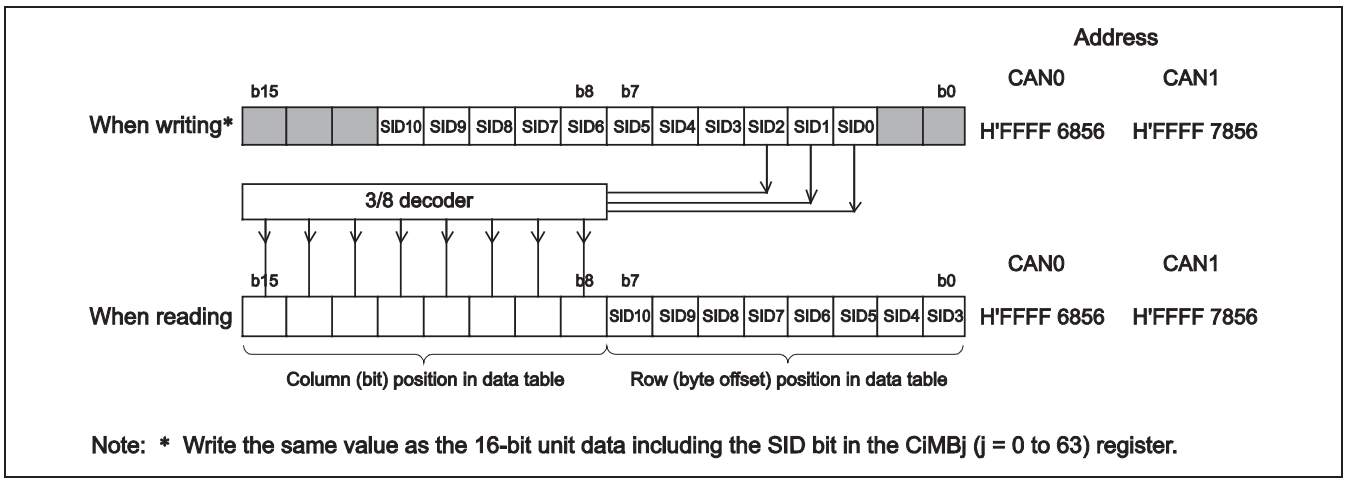


Figure 34.5 Write and Read of CiAFSR Register (i = 0, 1)

34.3.19 CANi Error Interrupt Enable Register (CiEIER) (i = 0, 1)

The CiEIER register is used to set the error interrupt enabled/disabled individually for each error interrupt source in the CiEIFR register.

Write to the CiEIER register in CAN reset mode.

CAN0 Error Interrupt Enable Register (C0EIER)
CAN1 Error Interrupt Enable Register (C1EIER)

Bit:	7	6	5	4	3	2	1	0
	BLIE	OLIE	ORIE	BORIE	BOEIE	EPIE	EWIE	BEIE
Initial	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	BLIE	0	R/W	Bus Lock Interrupt Enable Bit When the BLIE bit is "0", no error interrupt request is generated even if the BLIF bit in the CiEIFR register is set to "1". When the BLIE bit is "1", an error interrupt request is generated if the BLIF bit is set to "1". 0: Bus lock interrupt disabled 1: Bus lock interrupt enabled
6	OLIE	0	R/W	Overload Frame Transmit Interrupt Enable Bit When the OLIE bit is "0", no error interrupt request is generated even if the OLIF bit in the CiEIFR register is set to "1". When the OLIE bit is "1", an error interrupt request is generated if the OLIF bit is set to "1". 0: Overload frame transmit interrupt disabled 1: Overload frame transmit interrupt enabled
5	ORIE	0	R/W	Receive Overrun Interrupt Enable Bit When the ORIE bit is "0", an error interrupt request is not generated even if the ORIF bit in the CiEIFR register is set to "1". When the ORIE bit is "1", an error interrupt request is generated if the ORIF bit is set to "1". 0: Receive overrun interrupt disabled 1: Receive overrun interrupt enabled
4	BORIE	0	R/W	Bus-Off Recovery Interrupt Enable Bit When the BORIE bit is "0", an error interrupt request is not generated even if the BORIF bit in the CiEIFR register is set to "1". When the BORIE bit is set to "1", an error interrupt request is generated if the BORIF bit is set to "1". 0: Bus-off recovery interrupt disabled 1: Bus-off recovery interrupt enabled
3	BOEIE	0	R/W	Bus-Off Entry Interrupt Enable Bit When the BOEIE bit is "0", no error interrupt request is generated even if the BOEIF bit in the CiEIFR register is set to "1". When the BOEIE bit is "1", an error interrupt request is generated if the BOEIF bit is set to "1". 0: Bus-off entry interrupt disabled 1: Bus-off entry interrupt enabled

Bit	Symbol	Initial Value	R/W	Description
2	EPIE	0	R/W	Error-Passive Interrupt Enable Bit When the EPIE bit is "0", no error interrupt request is generated even if the EPIF bit in the CiEIFR register is set to "1". When the EPIE bit is "1", an error interrupt request is generated if the EPIF bit is set to "1". 0: Error-passive interrupt disabled 1: Error-passive interrupt enabled
1	EWIE	0	R/W	Error-Warning Interrupt Enable Bit When the EWIE bit is "0", no error interrupt request is generated even if the EWIF bit in the CiEIFR register is set to "1". When the EWIE bit is "1", an error interrupt request is generated if the EWIF bit is set to "1". 0: Error-warning interrupt disabled 1: Error-warning interrupt enabled
0	BEIE	0	R/W	Bus Error Interrupt Enable Bit When the BEIE bit is "0", no error interrupt request is generated even if the BEIF bit in the CiEIFR register is set to "1". When the BEIE bit is "1", an error interrupt request is generated if the BEIF bit is set to "1". 0: Bus error interrupt disabled 1: Bus error interrupt enabled

34.3.20 CANi Error Interrupt Factor Judge Register (CiEIFR) (i = 0, 1)

If an event corresponding to each bit occurs, the corresponding bit in the CiEIFR register is set to "1" regardless of the setting of the CiEIER register.

To set each bit to "0", write "0" by a program. If the set timing occurs simultaneously with the clear timing by the program, the bit becomes "1".

When writing "0" to a single bit by a program, only the specified bit is set to "0" and the other bits are set to "1". Writing "1" has no effect to these bit values.

CAN0 Error Interrupt Factor Judge Register (C0EIFR)
CAN1 Error Interrupt Factor Judge Register (C1EIFR)

Bit:	7	6	5	4	3	2	1	0
	BLIF	OLIF	ORIF	BORIF	BOEIF	EPIF	EWIF	BEIF
Initial	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	BLIF	0	R/W	Bus Lock Detect Flag* The BLIF bit becomes 1 if 32 consecutive dominant bits are detected on the CAN bus while the CAN module is in CAN operation mode. After the BLIF bit becomes 1, bus lock can be detected again after either of the following conditions is satisfied: • After this bit is set to 0 from 1, recessive bits are detected (bus lock is resolved). • After this bit is set to 0 from 1, the CAN module enters CAN reset mode and then enters CAN operation mode again (internal reset).0: No bus lock detected 1: Bus lock detected
6	OLIF	0	R/W	Overload Frame Transmission Detect Flag* The OLIF bit is set to "1" if the transmitting condition of an overload frame is detected when the CAN module performs transmission or reception. 0: No overload frame transmission detected 1: Overload frame transmission detected
5	ORIF	0	R/W	Receive Overrun Detect Flag* The ORIF bit is set to "1" when a receive overrun occurs. This bit is not to set to "1" in overwrite mode. In overwrite mode, a reception complete interrupt request is generated if an overwrite condition occurs and the ORIF bit is not set to "1". In normal mailbox mode, if an overrun occurs in any of mailboxes [0] to [63] in overrun mode, this bit is set to "1". In FIFO mailbox mode, if an overrun occurs in any of mailboxes [0] to [55] or the receive FIFO in overrun mode, this bit is set to "1". 0: No receive overrun detected 1: Receive overrun detected

Bit	Symbol	Initial Value	R/W	Description
4	BORIF	0	R/W	Bus-Off Recovery Detect Flag* The BORIF bit is set to "1" when the CAN module recovers from the bus-off state normally by detecting 11 consecutive bits 128 times in the following conditions: When the BOM bit in the CiCTLR register is "00". When the BOM bit is "10". When the BOM bit is "11". The BORIF bit is not set to "1" if the CAN module recovers from the bus-off state in the following conditions: When the CANM bit in the CiCTLR register is set to "01" or "11" (CAN reset mode). When the RBOC bit in the CiCTLR register is set to "1" (forcible return from bus-off). When the BOM bit is "01". When the BOM bit is "11" and the CANM bit is set to "10" (CAN halt mode) before normal recovery occurs. 0: No bus-off recovery detected 1: Bus-off recovery detected
3	BOEIF	0	R/W	Bus-Off Entry Detect Flag* The BOEIF bit is set to "1" when the CAN error state becomes bus-off (the TEC value exceeds 255). The BOEIF bit is also set to "1" when the BOM bit in the CiCTLR register is "01" (entry to CAN halt mode automatically at bus-off entry) and the CAN module becomes the bus-off state. 0: No bus-off entry detected 1: Bus-off entry detected
2	EPIF	0	R/W	Error Passive Detect Flag* The EPIF bit is set to "1" when the CAN error state becomes error-passive (the REC or TEC value exceeds 127). The EPIF bit is set to "1" only when the REC or TEC initially exceeds 127. Thus, if "0" is written to the EPIF bit by a program while the REC or TEC remains greater than 127, the EPIF bit is not set to "1" until the REC and TEC goes below 127 and then exceeds 127 again. 0: No error passive detected 1: Error passive detected
1	EWIF	0	R/W	Error Warning Detect Flag* The EWIF bit is set to "1" when the value of the receive error counter (REC) or transmit error counter (TEC) exceeds 95. The EWIF bit is set to "1" only when the REC or TEC initially exceeds 95. Thus, if "0" is written to the EWIF bit by a program while the REC or TEC remains greater than 95, the EWIF bit is not set to "1" until the REC and TEC goes below 95 and then exceeds 95 again. 0: No error warning detected 1: Error warning detected
0	BEIF	0	R/W	Bus Error Detect Flag* The BEIF bit is set to "1" when a bus error is detected. 0: No bus error detected 1: Bus error detected

Note: * Only "0" may be written to this bit. (Writing "1" has no effect.) When writing "0" to specific bits in software, write "0" to each bit to be cleared to "0" and "1" to all other bits.

Table 34.8 lists the behavior of bits BOEIF and BORIF according to BOM bit setting value.

Table 34.8 Behavior of Bits BOEIF and BORIF according to BOM Bit Setting Value

BOM Bit	BOEIF Bit	BORIF Bit
00	Set to "1" on entry to the bus-off state.	Set to "1" on exit from the bus-off state.
01		Do not set to "1".
10		Set to "1" on exit from the bus-off state.
11		Set to "1" if normal bus-off recovery occurs before the CANM bit is set to "10" (CAN halt mode).

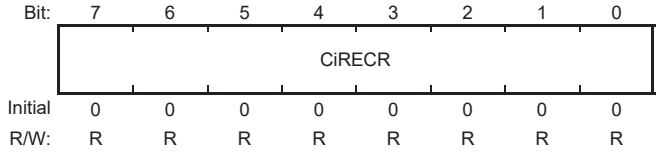
34.3.21 CANi Receive Error Count Register (CiRECR) (i = 0, 1)

The CiRECR register indicates the value of the receive error counter.

For the increment/decrement conditions of the receive error counter, refer to the CAN Specifications (ISO11898-1).

The value in bus-off state is undefined.

CAN0 Receive Error Count Register (C0RECR)
CAN1 Receive Error Count Register (C1RECR)



<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiRECR	H'00	R	Receive Error Count Function The CiRECR register increments or decrements the counter value according to error status of the CAN module during reception.

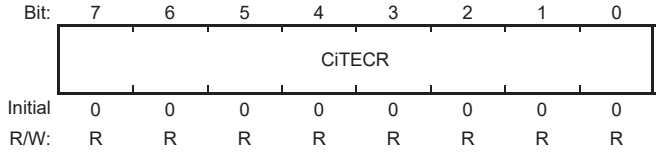
34.3.22 CANi Transmit Error Count Register (CiTECR) (i = 0, 1)

The CiTECR register indicates the value of the transmit error counter.

For the increment/decrement conditions of the transmit error counter, refer to the CAN Specifications (ISO11898-1).

The value in bus-off state is undefined.

CAN0 Transmit Error Count Register (C0TECR)
CAN1 Transmit Error Count Register (C1TECR)



<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 0	CiTECR	H'00	R	Transmit Error Count Function The CiTECR register increments or decrements the counter value according to error status of the CAN module during transmission.

34.3.23 CANi Error Code Store Register (CiECSR) (i = 0, 1)

The CiECSR register can be used to monitor whether an error has occurred on the CAN bus. Refer to the CAN Specifications (ISO11898-1) to check the generation conditions of each error.

To set each bit except the EDPM bit to "0", write "0" by a program. If the timing at which each bit is set to "1" and the timing at which "0" is written by a program are the same, the relevant bit is set to "1".

CAN0 Error Code Store Register (C0ECSR)
CAN1 Error Code Store Register (C1ECSR)

Bit:	7	6	5	4	3	2	1	0
	EDPM	ADEF	BE0F	BE1F	CEF	AEF	FEF	SEF
Initial	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	EDPM	0	R/W	Error Display Mode Select Bit*1*2 The EDPM bit selects the output mode of the CiECSR register. When the EDPM bit is set to "0", the CiECSR register outputs the first error code. When the EDPM bit is set to "1", the CiECSR register outputs the accumulated error code. 0: Output of first detected error code 1: Output of accumulated error code
6	ADEF	0	R/W	ACK Delimiter Error Flag*3*4 The ADEF bit is set to "1" when a form error is detected with the ACK delimiter during transmission. 0: No ACK delimiter error detected 1: ACK delimiter error detected
5	BE0F	0	R/W	Bit Error (dominant) Flag*3*4 The BE0F bit is set to "1" when a dominant bit error is detected. 0: No bit error (dominant) detected 1: Bit error (dominant) detected
4	BE1F	0	R/W	Bit Error (recessive) Flag*3*4 The BE1F bit is set to "1" when a recessive bit error is detected. 0: No bit error (recessive) detected 1: Bit error (recessive) detected
3	CEF	0	R/W	CRC Error Flag*3*4 The CEF bit is set to "1" when a CRC error is detected. 0: No CRC error detected 1: CRC error detected
2	AEF	0	R/W	ACK Error Flag*3*4 The AEF bit is set to "1" when an ACK error is detected. 0: No ACK error detected 1: ACK error detected

Bit	Symbol	Initial Value	R/W	Description
1	FEF	0	R/W	Form Error Flag*3*4 The FEF bit is set to "1" when a form error is detected. 0: No form error detected 1: Form error detected
0	SEF	0	R/W	Stuff Error Flag*3*4 The SEF bit is set to "1" when a stuff error is detected. 0: No stuff error detected 1: Stuff error detected

Notes: 1. Write to the EDPM bit in CAN reset mode or CAN halt mode.
2. If more than one error condition is detected simultaneously, all related bits are set to "1".
3. Writing "1" has no effect to these bit values.
4. When writing "0" to bits SEF, FEF, AEF, CEF, BE1F, BE0F, and ADEF by a program, only the specified bit is set to "0" and the other bits are set to "1".

34.3.24 CANi Time Stamp Register (CiTSR) (i = 0, 1)

When the CiTSR register is read, the value of the time stamp counter (16-bit free-running counter) at that moment is read.

The value of the time stamp counter reference clock is a multiple of 1 bit time, as configured by the TSPS bit in the CiCTLR register.

The time stamp counter stops in CAN sleep mode and CAN halt mode, and is initialized in CAN reset mode.

The time stamp counter value is stored to TSL and TSH in the CiMBj register when a received message is stored in a receive mailbox.

CAN0 Time Stamp Register (C0TSR)
CAN1 Time Stamp Register (C1TSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CiTSR															
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

<After Reset: H'0000>

Bit	Symbol	Initial Value	R/W	Description
15 to 0	CiTSR	All 0	R	Free-running counter value for the time stamp function

Note: Read the CiTSR register in 16-bit units.

34.3.25 CANi Test Control Register (CiTCR) (i = 0, 1)

Write to the CiTCR register in CAN halt mode only.

CAN0 Test Control Register (C0TCR)
CAN1 Test Control Register (C1TCR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	TSTM		TSTE
Initial	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
2, 1	TSTM	00	R/W	CAN Test Mode Select Bits The TSTM bit selects the CAN test mode. For details on the CAN test modes, see section 34.3.25 (1), Listen-Only Mode, section 34.3.25 (2), Self-Test Mode 0 (External Loop Back), and section 34.3.25 (3), Self-Test Mode 1 (Internal Loop Back). 00: Other than CAN test mode 01: Listen-only mode 10: Self-test mode 0 (external loop back) 11: Self-test mode 1 (internal loop back)
0	TSTE	0	R/W	CAN Test Mode Enable Bit When the TSTE bit is set to "0", CAN test mode is disabled. When the TSTE bit is set to "1", CAN test mode is enabled. 0: CAN test mode disabled 1: CAN test mode enabled

(1) Listen-Only Mode

The ISO 11898-1 recommends an optional bus monitoring mode. In listen-only mode, the CAN node is able to receive valid data frames and valid remote frames. It sends only recessive bits on the CAN bus, and the protocol controller is not required to send the ACK bit, overload flag, or active error flag.

Listen-only mode can be used for baud rate detection.

Do not request transmission from any mailboxes in this mode.

Figure 34.6 shows the connection when listen-only mode is selected.

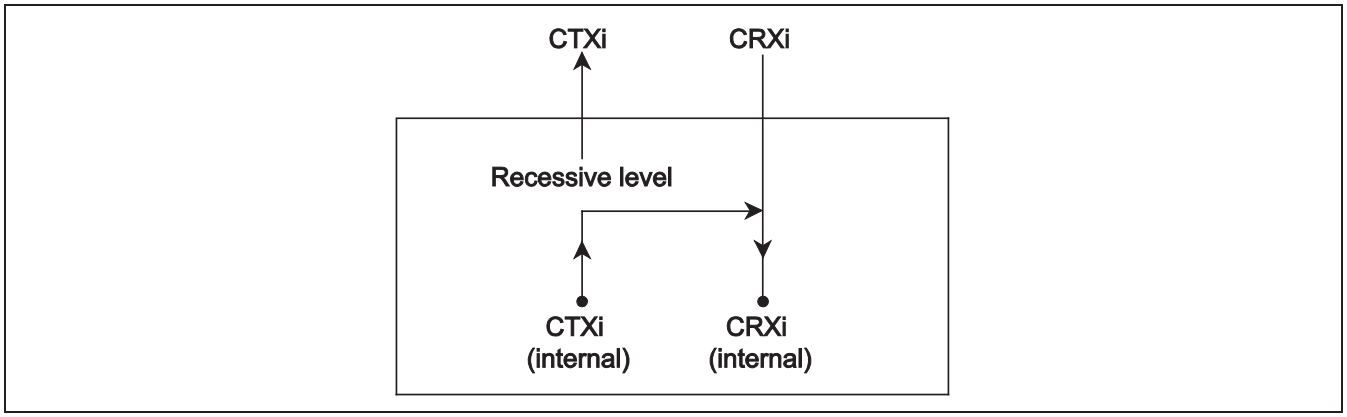


Figure 34.6 Connection when Listen-Only Mode is Selected

(2) Self-Test Mode 0 (External Loop Back)

Self-test mode 0 is provided for CAN transceiver tests.

In this mode, the protocol controller treats its own transmitted messages as messages received via the CAN transceiver and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

Connect the CANi_TX/CANi_RX pins to the transceiver.

Figure 34.7 shows the connection when self-test mode 0 is selected.

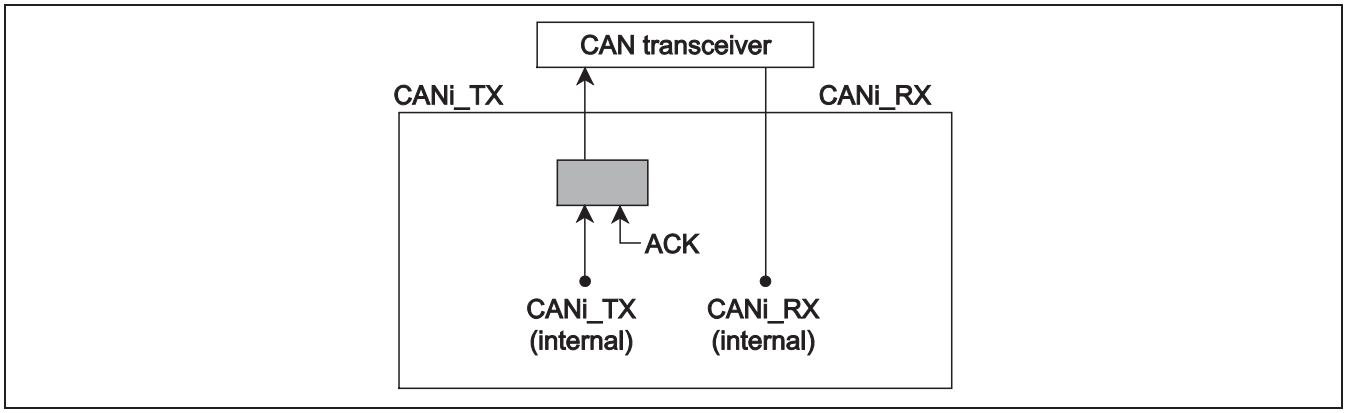


Figure 34.7 Connection when Self-Test Mode 0 is Selected

(3) Self-Test Mode 1 (Internal Loop Back)

Self-test mode 1 is provided for self-test functions.

In this mode, the protocol controller treats its transmitted messages as received messages and stores them into the receive mailbox. To be independent from external stimulation, the protocol controller generates the ACK bit.

In self-test mode 1, the protocol controller performs an internal feedback from the internal CANi_TX pin to the internal CANi_RX pin. The input value of the external CANi_RX pin is ignored. The external CANi_TX pin outputs only recessive bits. The CANi_TX/CANi_RX pins do not need to be connected to the CAN bus or any external device.

Figure 34.8 shows the connection when self-test mode 1 is selected.

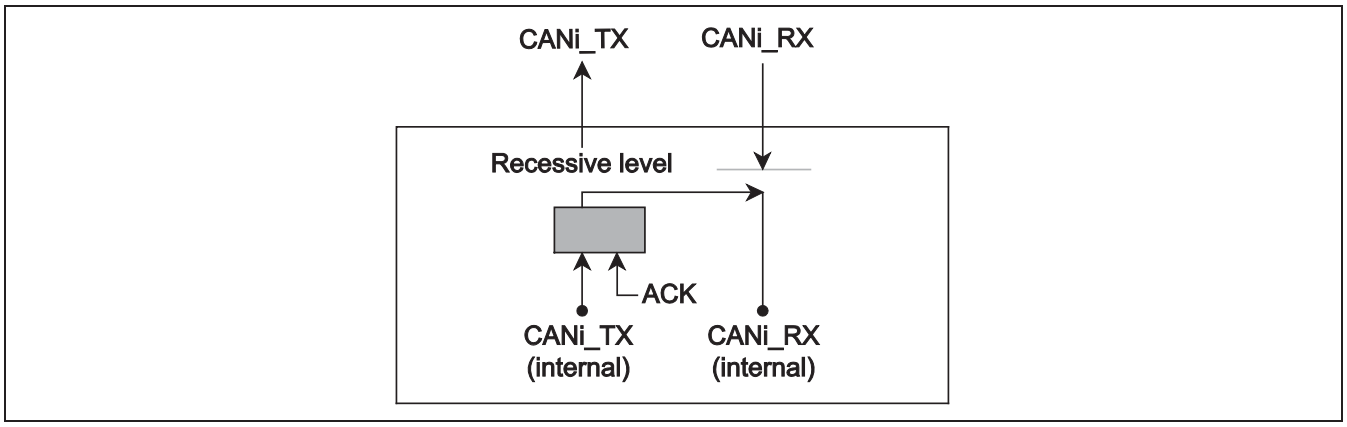


Figure 34.8 Connection when Self-Test Mode 1 is Selected

34.3.26 CANi Interrupt Status Register (CiISR) (i = 0, 1)

The CiISR register shows interrupt sources before masking by the CiIER register.

CAN0 Interrupt Status Register (C0ISR)
CAN1 Interrupt Status Register (C1ISR)

Bit:	7	6	5	4	3	2	1	0
	—	—	ERSF	RXFF	TXFF	RX M0F	RXM1 F	TXMF
Initial	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R	R

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
5	ERSF	0	R	Error (ERS) Interrupt Status Bit*1 The ERSF bit shows the error interrupt source status. 0: ERS interrupt source not detected 1: ERS interrupt source detected
4	RXFF	0	R/W	Reception FIFO (RXF) Interrupt Status Bit*2 The RXFF bit shows the FIFO receive interrupt source status. 0: RXF interrupt source not detected 1: RXF interrupt source detected The RXFF is cleared to "0" by writing "0" to it by software. (writing "1" has no effect)
3	TXFF	0	R/W	Transmission FIFO (TXF) Interrupt Status Bit*3 The TXFF bit shows the FIFO transmit interrupt source status. 0: TXF interrupt source not detected 1: TXF interrupt source detected The TXFF is cleared to "0" by writing "0" to it by software. (writing "1" has no effect)
2	RXM0F	0	R	Mailbox 0 Successful Reception (RXM0) Interrupt Status Bit*4 The RXM0F bit shows the successful reception interrupt source status for mailbox 0. 0: RXM0 interrupt source not detected 1: RXM0 interrupt source detected
1	RXM1F	0	R	Mailbox 1 to 63 Successful Reception (RXM1) Interrupt Status Bit*5 The RXM1F bit shows the successful reception interrupt source status for mailboxes 1 to 63. 0: RXM1 interrupt source not detected 1: RXM1 interrupt source detected
0	TXMF	0	R	Mailbox 32 to 63 Successful Transmission (TXM) Interrupt Status Bit*6 The TXMF bit shows the successful transmission interrupt source status for mailboxes 32 to 63. 0: TXM interrupt source not detected 1: TXM interrupt source detected

Notes: 1. The ERSF bit is set to "1" when a bit in one of the CiEIFR[j] registers is set to "1" due to a communication error while the corresponding bit in the CiEIER[j] register is set to "1" (j = 0 to 7).

2. The RXFF bit is set to "1" when bit 6 or 5 in the CiRFCR register is set to "1" because of a reception FIFO full or warning condition due to the setting of CiMIER[61].
3. The TXFF bit is set to "1" when the transmission FIFO message count reaches the specified value due to the setting of CiMIER[57].
4. After the NEWDATA bit in CiMCTL0 is set to "1" at the end of a receive operation, the RXM0F bit is set to "1" if storing of the receive data is complete (corresponding INVALDATA bit value changed from "1" to "0") and the CiMIER0[0] bit has been set to "1".
5. After the NEWDATA bit in CiMCTLj is set to "1" at the end of a receive operation, the RXM1F bit is set to "1" if storing of the receive data is complete (corresponding INVALDATA bit value changed from "1" to "0") and the bit in CiMIER0 or CiMIER1 corresponding to mailbox j has the been set to "1" (j = 1 to 63).
6. The TXMF bit is set to "1" when the bit in the CiMIER1 register corresponding to mailbox j is set to "1" while the value of the SENTDATA bit in the CiMCTLj register is "1" following a successful reception (j = 32 to 63).

34.3.27 CANi Interrupt Enable Register (CiIER) (i = 0, 1)

The CiIER register can be used by an application to cause some interrupts to be ignored while processing by an interrupt service routine is taking place. Each bit affects the individual interrupt source corresponding to it.

CAN0 Interrupt Enable Register (C0IER)
CAN1 Interrupt Enable Register (C1IER)

Bit:	7	6	5	4	3	2	1	0
	—	—	ERSIE	RXFIE	TXFIE	RXM 0IE	RXM 1IE	TXM IE
Initial	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
5	ERSIE	0	R/W	Error (ERS) Interrupt Enable Bit The ERSIE bit enables or disables the ERS interrupt controller. 0: ERS interrupt disabled 1: ERS interrupt enabled
4	RXFIE	0	R/W	Reception FIFO (RXF) Interrupt Enable Bit The RXFIE bit enables or disables the RXF interrupt controller. 0: RXF interrupt disabled 1: RXF interrupt enabled
3	TXFIE	0	R/W	Transmission FIFO (TXF) Interrupt Enable Bit The TXFIE bit enables or disables the TXF interrupt controller. 0: TXF interrupt disabled 1: TXF interrupt enabled
2	RXM0IE	0	R/W	Mailbox 0 Successful Reception (RXM0) Interrupt Enable Bit The RXM0IE bit enables or disables the RXM0 interrupt controller. 0: RXM0 interrupt disabled 1: RXM0 interrupt enabled
1	RXM1IE	0	R/W	Mailbox 1 to 63 Successful Reception (RXM1) Interrupt Enable Bit The RXM1IE bit enables or disables the RXM1 interrupt controller. 0: RXM1 interrupt disabled 1: RXM1 interrupt enabled
0	TXMIE	0	R/W	Mailbox 32 to 63 Successful Transmission (TXM) Interrupt Enable Bit The TXMIE bit enables or disables the TXM interrupt controller. 0: TXM interrupt disabled 1: TXM interrupt enabled

34.3.28 CANi Mailbox Search Mask Register (CiMBSMR) (i = 0, 1)

Write to the CiMBSMR register in CAN halt mode only.

CAN0 Mailbox Search Mask Register (C0MBSMR)
CAN1 Mailbox Search Mask Register (C1MBSMR)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	MB0SM
Initial	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
0	MB0SM	0	R/W	Mailbox 0 Search Mask Bit* When the MB0SM bit is set to "1", message box 0 is excluded from the search target for the CANi mailbox search status register.

Note: * The MB0SM bit is enabled in the search modes except channel search mode. In the RXM1 interrupt handling, this bit is usable to exclude message box 0 from the search target for the CiMSSR register in receive mailbox search mode.

34.3.29 CANi Parity Error Control Register (CiPECR) (i = 0, 1)

This register controls the function of the parity mode and displays a parity error flag.

Bit:	7	6	5	4	3	2	1	0
	PF	—	—	—	—	PIE	PME	PM
Initial	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

<After Reset: H'00>

Bit	Symbol	Initial Value	R/W	Description
7	PF	0	R	Parity error flag *2 This bit is set to “1” when a parity error is detected. The bit has to be cleared by the program. As long as this bit is set no further parity error can be detected and the address value in the Parity Error Address Capture Register keeps the address for the first captured parity error. 0: Parity error is not detected 1: Parity error is detected
6 to 3	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
2	PIE	0	R/W	Parity error interrupt *1 This bit controls the parity error interrupt enable. When this bit is configured to “0”, the parity error interrupt is disabled. When this bit is set to “1”, the parity error interrupt is enabled. The parity error interrupt is one of the factors in the CAN error interrupt. When a parity error interrupt is generated, the parity error flag (CANi Parity Error Control Register, bit 7) should be checked to determine the interrupt source. 0: Parity error interrupt is disabled 1: Parity error interrupt is enabled
1	PME	0	R/W	Parity enable bit This bit controls the Dual Port RAM parity functionality. When this bit is set to “0”, parity checkers are disabled keeping the parity generators still active to store the correct parity bit for each byte when writing to the Dual Port RAM. When this bit is set to “1”, parity checkers and parity generators are both active. 0: Parity checker off 1: Parity checker on

Bit	Symbol	Initial Value	R/W	Description
0	PM	0	R/W	Parity mode This bit controls the action of the CAN Module following the detection of a parity error. When this bit is programmed to “1” and a parity error is detected while in Operation Mode the CAN module forces the cancellation of a possible pending communication (either reception or transmission) and then enters Halt mode. When the pending communication is cancelled, the Reception Error Counter and Transmission Error Counter are initialized. If a parity error is detected while the CAN module is in its Reset or Halt mode no state transition will take place. In case where CPU requests transition to Reset Mode at the same time as a parity error occurs then the CPU request to enter Reset Mode will have the highest priority. When this bit is set to “0”, CAN module continues in Operation Mode and the pending communication is not canceled. Regardless of the setting of ParMode (PM) when a parity error occurs and ParModeEn (PME) bit is set to ‘1’ (parity function enabled): • a parity error flag is set in bit 7 of the CAN Parity Error Control Register • a parity error interrupt is generated (providing the ParIntEn (PIE) bit is asserted) • the address where a parity error occurs is captured in the CANi Parity Error Capture Address Register. When parity error is detected 0: Continue operation mode 1: Go to Halt mode

Notes: 1. Do not write to this bit in Operation Mode
2. Write “0” only (writing “1” has no effect)
3. The software sequence required to set these bits is described in section 34.10, CPU is prevented from writing this bit in operation mode by H/W write protection.

34.3.30 CANi Parity Error Address Capture Register (CiPEACR) (i = 0, 1)

This register displays the address where the parity error occurred.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	PA										
Initial	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

<After Reset: H'0000>

Bit	Symbol	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved bits These bits are always read as 0. The write value should always be 0. Operation is not guaranteed if a value other than 0 is written to these bits.
10 to 0	PA	H'000	R	Parity error captured address bits This register displays the address offset from a starting address of Mailbox 0 where parity error is detected. When a parity error is detected, the address in which the error occurred is captured in this register. Only the longword address is shown. The address is shown as below.

ParAddress value	Location
H'000 - H'00F	Mailbox 0*
H'010 – H'01F	Mailbox 1
H'020 – H'02F	Mailbox 2
...	…
H'3F0 – H'3FF	Mailbox 63
H'400 – H'41F	CiMKR 2 to 9
H'420 – H'427	FIFO ID 0 to 1
H'428 – H'42B	Mask Invalid 1
H'42C – H'42F	Interrupt enable 1
H'430 – H'433	CiMKR 0
H'434 – H'437	CiMKR 1
H'438 – H'43B	Mask Invalid 0
H'43C – H'43F	Interrupt enable 0

Note: * H'000 is the first byte of the mailbox 0.

Only the address related to the first parity error is reported. The program has to clear the ParFlag status to enable the capture of other locations leading to a parity error.

In case parity error is flagged at the same time from DPRAM CAN side parity checker and the DPRAM CPU side parity checker, the CPU side access address will be displayed in the parity error address capture register.

34.4 Operating Mode

The CAN module has the following four operating modes.

- CAN reset mode
- CAN halt mode
- CAN operation mode
- CAN sleep mode

Figure 34.9 shows the transition between CAN operating modes.

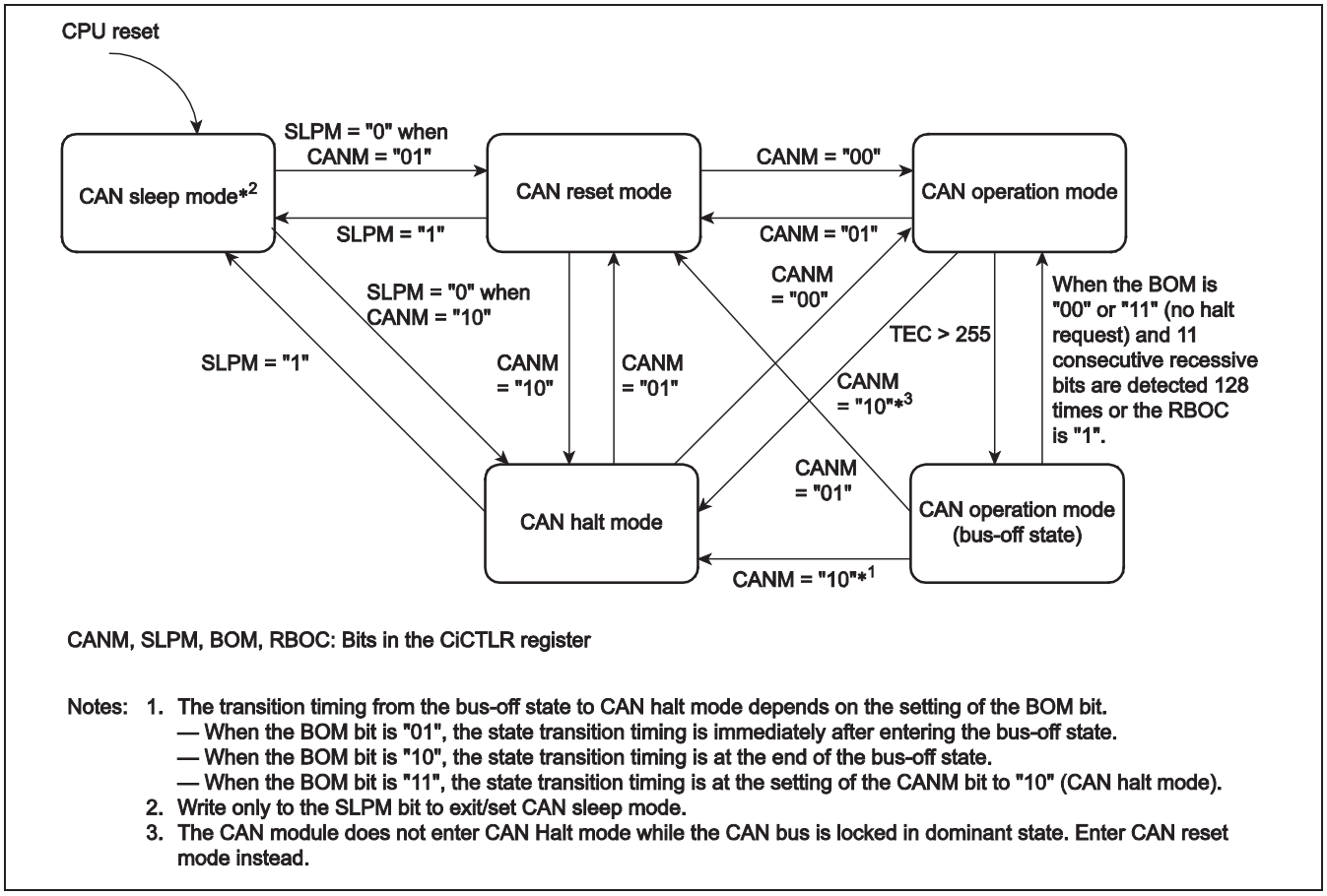


Figure 34.9 Transition between CAN Operating Modes (i = 0, 1)

34.4.1 CAN Reset Mode

CAN reset mode is provided for CAN communication configuration.

When the CANM bit in the CiCTLR register is set to "01" or "11", the CAN module enters CAN reset mode. Then the RSTST bit in the CiSTR register is set to "1". Do not change the CANM bit until the RSTST bit is set to "1". Configure the CiBCR register before exiting CAN reset mode to any other modes.

The following registers are initialized to their reset values after entering CAN reset mode and their initialized values are retained during CAN reset mode:

- CiMCTLj register
- CiSTR register (except bits SLPST and TFST)
- CiEIFR register
- CiRECR register
- CiTECR register
- CiTSR register
- CiMSSR register
- CiMSMR register
- CiRFCR register
- CiTFCR register
- CiTCR register
- CiECSR register (except EDPM bit)
- CiISR register
- CiMBSMR register

The following registers retain their values after entering CAN reset mode.

- CiCLKR register
- CiCTLR register
- CiSTR register (bits SLPST and TFST)
- Registers CiMIER0 and CiMIER1
- CiEIER register
- CiBCR register
- CiCSSR register
- CiECSR register (EDPM bit only)
- CiMBj register
- Registers CiMKR0 to CiMKR9
- Registers CiFIDCR0 and CiFIDCR1
- Registers CiMKIVLR0 and CiMKIVLR1
- CiAFSR register
- CiRFPCR register
- CiTFPCR register
- CiIER register

34.4.2 CAN Halt Mode

CAN halt mode is used for mailbox configuration and test mode setting.

When the CANM bit in the CiCTLR register is set to "10", CAN halt mode is selected. Then the HLTST bit in the CiSTR register is set to "1". Do not change the CANM bit until the HLTST bit is set to "1".

Refer to Table 34.9, Operation in CAN Reset Mode and CAN Halt Mode regarding the state transition conditions when transmitting or receiving.

All registers except bits RSTST, HLTST, and SLPST in the CiSTR register remain unchanged when the CAN module enters CAN halt mode.

Do not change registers CiCLKR, CiCTLR (except bits CANM and SLPM), and CiEIER in CAN halt mode. The CiBCR register can be changed in CAN halt mode only when listen-only mode is selected to use for automatic bit rate detection.

Table 34.9 Operation in CAN Reset Mode and CAN Halt Mode

Mode	Receiver	Transmitter	Bus-Off
CAN reset mode	CAN module enters CAN reset mode without waiting for the end of message reception	CAN module enters CAN reset mode after waiting for the end of message transmission (1, 4)	CAN module enters CAN reset mode without waiting for the end of bus-off recovery
CAN halt mode	CAN module enters CAN halt mode after waiting for the end of message reception (2, 3)	CAN module enters CAN halt mode after waiting for the end of message transmission (1, 2, 4)	• When the BOM bit is "B'00" A halt request from a program will be acknowledged only after bus-off recovery • When the BOM bit is "B'01" CAN module automatically enters CAN halt mode without waiting for the end of bus-off recovery (regardless of a halt request from a program) • When the BOM bit is "B'10" CAN module automatically enters CAN halt mode after waiting for the end of bus-off recovery (regardless of a halt request from a program) • When the BOM bit is "B'11" CAN module enters CAN halt mode (without waiting for the end of bus-off recovery) if a halt is requested by a program during bus-off

BOM bit: Bit in the CiCTLR register (i = 0, 1)

Notes: 1. If several messages are requested to be transmitted, mode transition occurs after the completion of the first message transmission. When CAN reset mode is being requested during suspend transmission, mode transition occurs when the bus is idle, the next transmission ends, or the CAN module becomes a receiver.
2. If the CAN bus is locked in dominant state, the program can detect this state by monitoring the BLIF bit in the CiEIFR register. The CAN module does not enter CAN Halt mode while the CAN bus is locked in dominant state. Enter CAN reset mode instead.
3. If a CAN bus error occurs during reception after CAN halt mode is requested, the CAN module enters CAN halt mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.
4. If a CAN bus error or arbitration lost occurs during transmission after CAN reset mode or CAN halt mode is requested, the CAN module enters the requested operating mode. However, the CAN module does not enter CAN Halt mode when the CAN bus is locked in dominant state.

34.4.3 CAN Sleep Mode

CAN sleep mode is used for reducing current consumption by stopping the clock supply to the CAN module. After MCU hardware reset or software reset, the CAN module starts from CAN sleep mode.

When the SLPM bit in the CiCTLR register is set to "1", the CAN module enters CAN sleep mode. Then the SLPST bit in the CiSTR register is set to "1". Do not change the value of the SLPM bit until the SLPST bit is set to "1". The other registers remain unchanged when the MCU enters CAN sleep mode.

Write to the SLPM bit in CAN reset mode and CAN halt mode. Do not change any registers (except the SLPM bit) during CAN sleep mode. Read operation is still allowed. When the SLPM bit is set to "0", the CAN module is released from CAN sleep mode. When the CAN module exits CAN sleep mode, the other registers remain unchanged.

34.4.4 CAN Operation Mode (Excluding Bus-Off State)

CAN operation mode is used for CAN communication.

When the CANM bit in the CiCTLR register is set to "B'00", the CAN module enters CAN operation mode.

Then bits RSTST and HLTST in the CiSTR register are set to "0". Do not change the value of the CANM bit until these bits are set to "0".

If 11 consecutive recessive bits are detected after entering CAN operation mode, the CAN module is in the following states:

- The CAN module becomes an active node on the network that enables transmission and reception of CAN messages.
- Error monitoring of the CAN bus, such as receive and transmit error counters, is performed.

During CAN operation mode, the CAN module may be in one of the following three sub-modes, depending on the status of the CAN bus:

- Idle mode: Transmission or reception is not being performed.
- Receive mode: A CAN message sent by another node is being received.
- Transmit mode: A CAN message is being transmitted. The CAN module may receive its own message simultaneously when self-test mode 0 (TSTM bit in the CiTCR register = "B'10") or self-test mode 1 (TSTM bit = "B'11") is selected.

Figure 34.10 shows the sub mode in CAN operation mode.

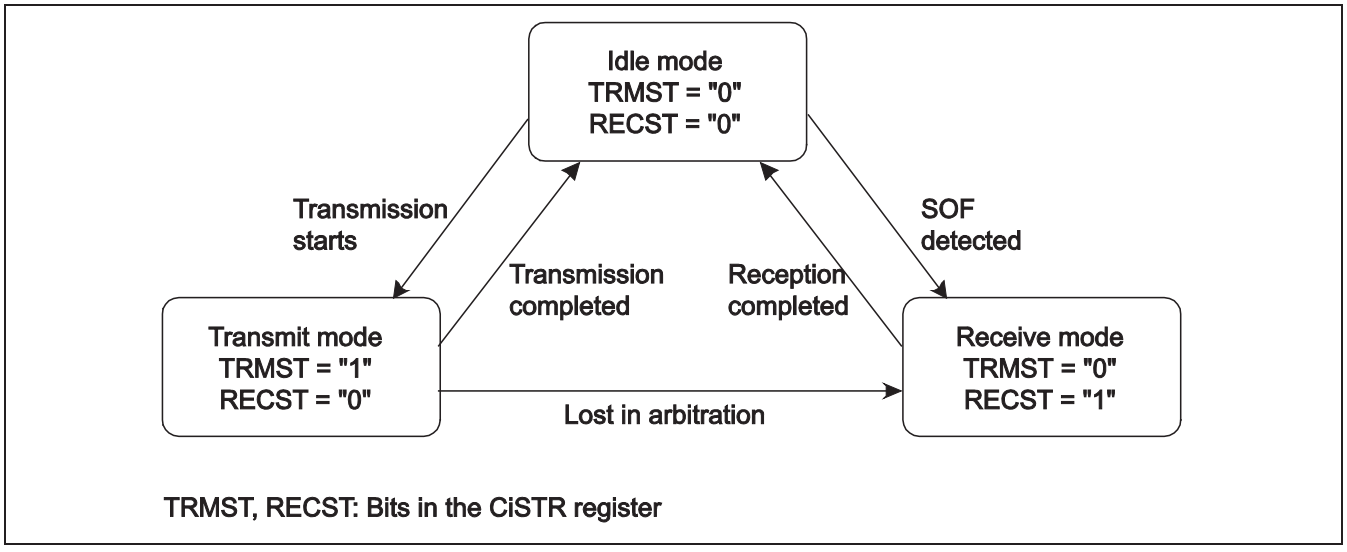


Figure 34.10 Sub Mode in CAN Operation Mode (i = 0, 1)

34.4.5 CAN Operation Mode (Bus-Off State)

The CAN module enters the bus-off state according to the increment/decrement rules for the transmit/error counters in the CAN Specifications.

The following cases apply when recovering from the bus-off state. When the CAN module is in bus-off state, the values of the associated registers, except registers CiSTR, CiEIFR, CiRECR, CiTECR and CiTSR, remain unchanged.

1. When the BOM bit in the CiCTLR register is "B'00" (normal mode)
   The CAN module enters the error-active state after it has completed the recovery from the bus-off state and CAN communication is enabled instantly. The BORIF bit in the CiEIFR register is set to "1" (bus-off recovery detected) at this time.
2. When the RBOC bit in the CiCTLR register is set to "1" (forcible return from bus-off)
   The CAN module enters the error-active state when it is in bus-off state and the RBOC bit is set to "1". CAN communication is enabled again after 11 consecutive recessive bits are detected. The BORIF bit is not set to "1" at this time.
3. When the BOM bit is "B'01" (entry to CAN halt mode automatically at bus-off entry)
   The CAN module enters CAN halt mode when it reaches the bus-off state. The BORIF bit is not set to "1" at this time.
4. When the BOM bit is "B'10" (entry to CAN halt mode automatically at bus-off end)
   The CAN module enters CAN halt mode when it has completed the recovery from bus-off. The BORIF bit is set to "1" at this time.
5. When the BOM bit is "B'11" (entry to CAN halt mode by a program) and the CANM bit in the CiCTLR register is set to "B'10" (CAN halt mode) during the bus-off state
   The CAN module enters CAN halt mode when it is in bus-off state and the CANM bit is set to "B'10" (CAN halt mode). The BORIF bit is not set to "1" at this time.
   If the CANM bit is not set to "B'10" during bus-off, the same behavior as (1) applies.

34.5 CAN Communication Speed Configuration

The following description explains about the CAN communication speed configuration.

34.5.1 CAN Clock Configuration

This MCU has a CAN clock selector. The CAN clock can be configured by setting the CCLKS bit in the CiCLKR register and the BRP bit in the CiBCR register.

Figure 34.11 shows the block diagram of CAN clock generator.

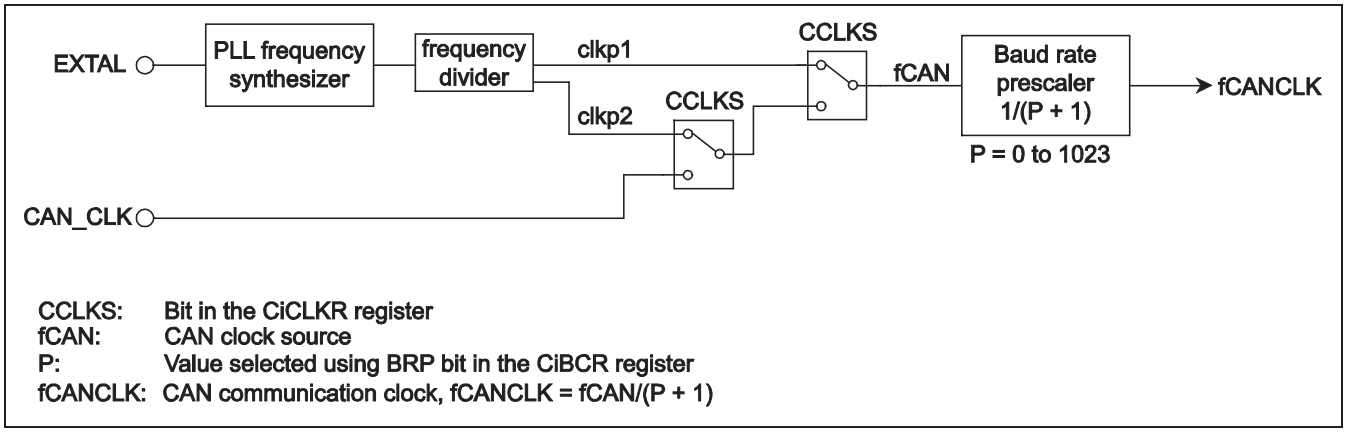


Figure 34.11 Block Diagram of CAN Clock Generator (i = 0, 1)

The CAN operating clock can be selected from the internal clock (clkp1, clkp2) from the CPG (PLL), and the external clock input to external pin (CAN_CLK).

In the initial state, clkp1 is selected. If an external clock input is to be selected, set the CiCLKR register (section 34.3.2) before accessing the CAN module. The range of frequencies that may be input as an external clock is 8 to 50 MHz.

34.5.2 Bit Timing Configuration

The bit time is a single bit time for transmitting/receiving a message and consists of the following three segments.

Figure 34.12 shows the bit timing.

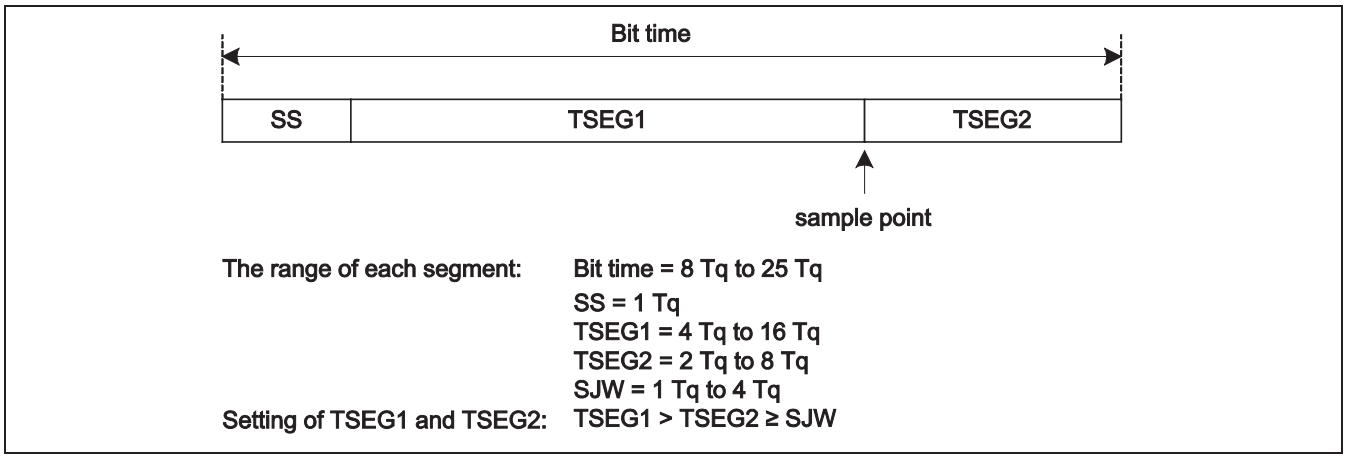


Figure 34.12 Bit Timing

34.5.3 Bit-rate

The bit rate depends on the division value of the fCAN (CAN clock source), the division value of the baud rate prescaler, and the number of Tq of one bit time.

$$\text{Bit rate [bps]} = \frac{fCAN}{\text{Baud rate prescaler division value}^* \times \text{number of Tq of one bit}} = \frac{fCANCLK}{\text{Number of Tq of one bit time}}$$

Note: * Division value of the baud rate prescaler = P + 1 (P: 0 to 1023)
P: Setting value of the BRP bit in the CiBCR register (i = 0, 1)

Table 34.10 lists bit rate examples.

Table 34.10 Example of Bit-rate

fCAN	40 MHz		32 MHz		20 MHz		16 MHz	
Bit-rate	**No. of Tq**	**P + 1**	**No. of Tq**	**P + 1**	**No. of Tq**	**P + 1**	**No. of Tq**	**P + 1**
1 Mbps	10Tq	4	8Tq	4	10Tq	2	8Tq	2
	20Tq	2	16Tq	2	20Tq	1	16Tq	1
500 kbps	10Tq	8	8Tq	8	10Tq	4	8Tq	4
	20Tq	4	16Tq	4	20Tq	2	16Tq	2
250 kbps	10Tq	16	8Tq	16	10Tq	8	8Tq	8
	20Tq	8	16Tq	8	20Tq	4	16Tq	4
83.3 kbps	8Tq	60	8Tq	48	8Tq	30	8Tq	24
	10Tq	48	16Tq	24	10Tq	24	16Tq	12
	16Tq	30			16Tq	15		
	20Tq	24			20Tq	12		
33.3 kbps	8Tq	150	8Tq	120	8Tq	75	8Tq	60
	10Tq	120	10Tq	96	10Tq	60	10Tq	48
	20Tq	60	16Tq	60	20Tq	30	16Tq	30
			20Tq	48			20Tq	24

34.6 Mailbox and Mask Register Structure

Figure 34.13 shows the structure of the CiMBj register.

There are 64 mailboxes with the same structure.

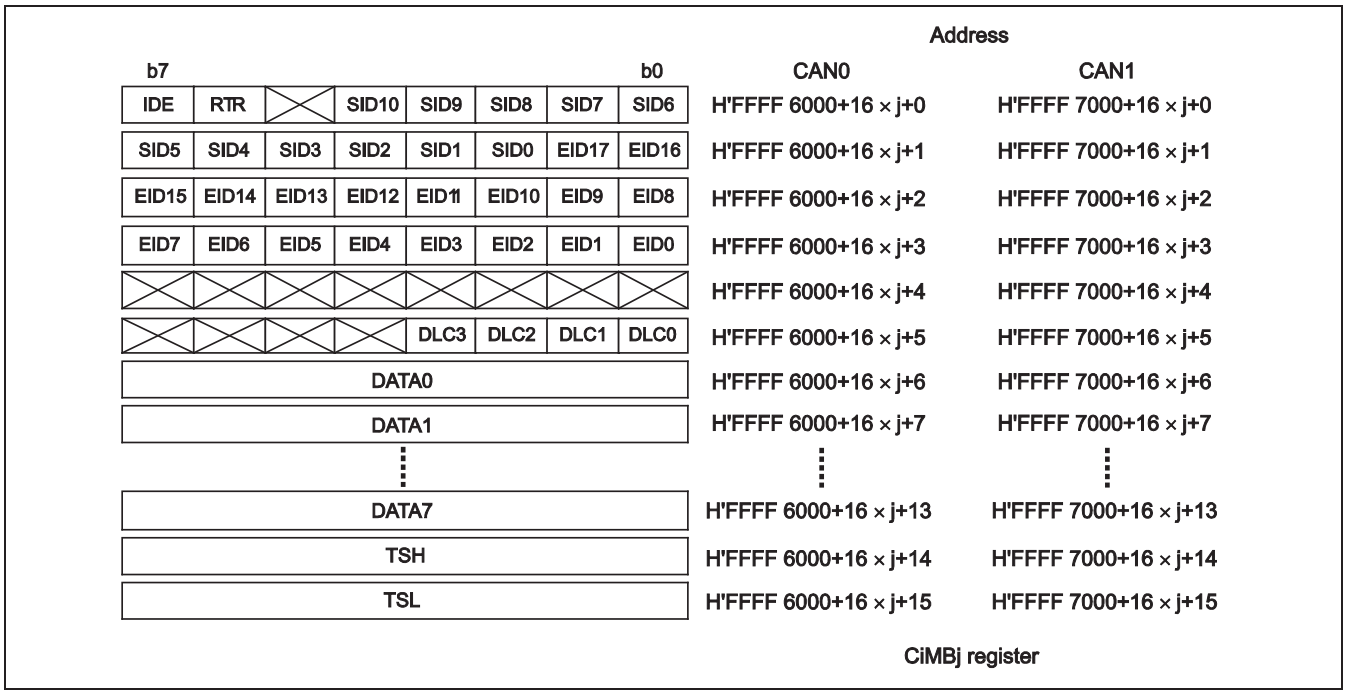


Figure 34.13 Structure of CiMBj Register (i = 0, 1; j = 0 to 63)

Figure 34.14 shows the structure of registers CiMKR0, CiMKR1, and CiMKR2 to CiMKR9.

There are 10 mask registers with the same structure.

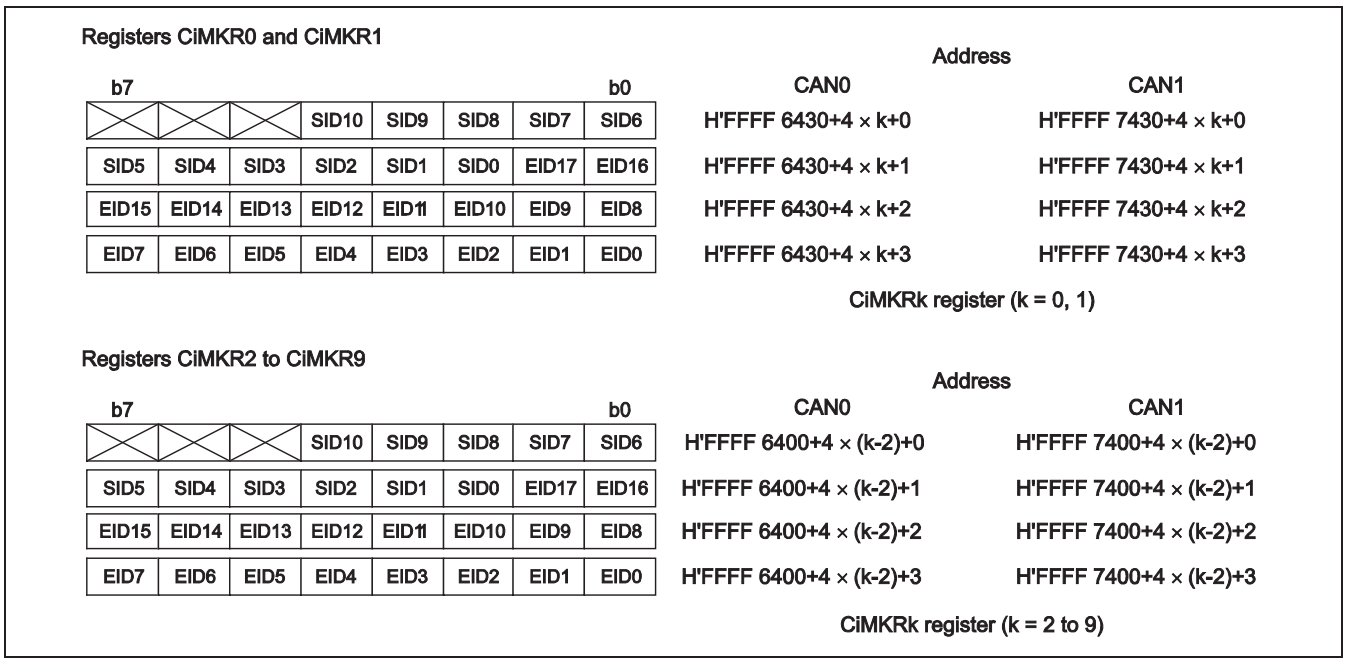


Figure 34.14 Structure of CiMKRk Register (i = 0, 1; k = 0 to 9)

Figure 34.15 shows the structure of the CiFIDCRn register.

There are 2 FIFO received ID compare registers with the same structure.

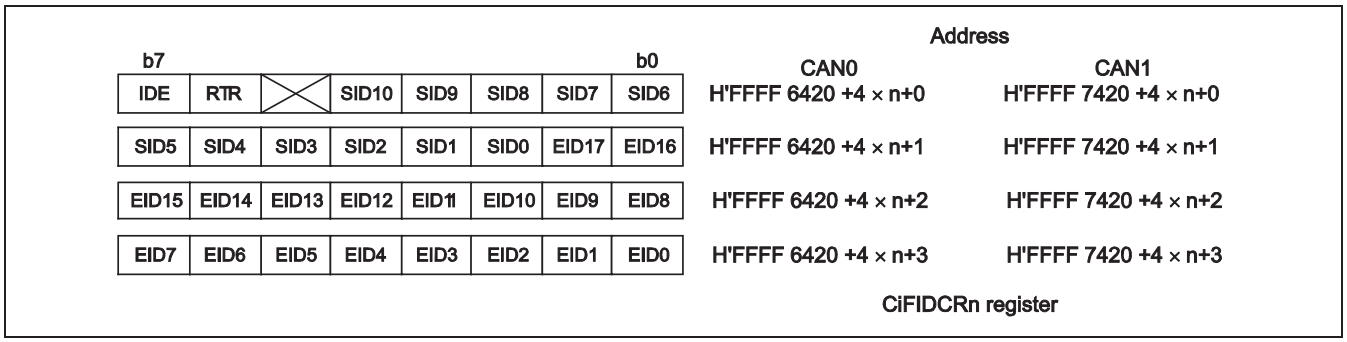


Figure 34.15 Structure of CiFIDCRn register (i = 0, 1; n = 0, 1)

34.7 Acceptance Filtering and Masking Function

Acceptance filtering allows the user to receive messages with a specified range of multiple IDs for mailboxes. Registers CiMKR0 to CiMKR9 can perform masking of the standard ID and the extended ID of 29 bits.

- The CiMKR0 register corresponds to mailboxes [0] to [15].
- The CiMKR1 register corresponds to mailboxes [16] to [31].
- The CiMKR2 register corresponds to mailboxes [32] to [35].
- The CiMKR3 register corresponds to mailboxes [36] to [39].
- The CiMKR4 register corresponds to mailboxes [40] to [43].
- The CiMKR5 register corresponds to mailboxes [44] to [47].
- The CiMKR6 register corresponds to mailboxes [48] to [51].
- The CiMKR7 register corresponds to mailboxes [52] to [55].
- The CiMKR8 register corresponds to mailboxes [56] to [59] in normal mailbox mode and the receive FIFO mailboxes [60] to [63] in FIFO mailbox mode.
- The CiMKR9 register corresponds to mailboxes [60] to [63] in normal mailbox mode and the receive FIFO mailboxes [60] to [63] in FIFO mailbox mode.

Registers CiMKIVLR0 and CiMKIVLR1 disable acceptance filtering individually for each mailbox.

The IDE bit in the CiMBj register is enabled when the IDFM bit in the CiCTLR register is "B'10" (mixed ID mode).

The RTR bit in the CiMBj register selects a data frame or a remote frame.

In FIFO mailbox mode, normal mailboxes (mailboxes [0] to [55]) use the single corresponding register among registers CiMKR0 to CiMKR7 for acceptance filtering. Receive FIFO mailboxes (mailboxes [60] to [63]) use two registers CiMKR8 and CiMKR9 for the acceptance filtering.
Also, the receive FIFO uses two registers CiFIDCR0 and CiFIDCR1 for ID comparison. Bits EID, SID, RTR, and IDE in registers CiMB60 to CiMB63 for the receive FIFO are disabled. As acceptance filtering depends on the result of two ID-mask sets, two ranges of IDs can be received into the receive FIFO.
Registers CiMKIVLR0 and CiMKIVLR1 are disabled for the receive FIFO.
If both setting of standard ID and extended ID are set in the IDE bits in registers CiFIDCR0 and CiFIDCR1 individually, both ID formats are received.
If both setting of data frame and remote frame are set in the RTR bits in registers CiFIDCR0 and CiFIDCR1 individually, both data and remote frames are received.
When combination with two ranges of IDs is not necessary, set the same mask value and the same ID into both of the FIFO ID/mask register sets.

Figure 34.16 shows the correspondence of mask registers to mailboxes. Figure 34.17 shows the acceptance filtering.

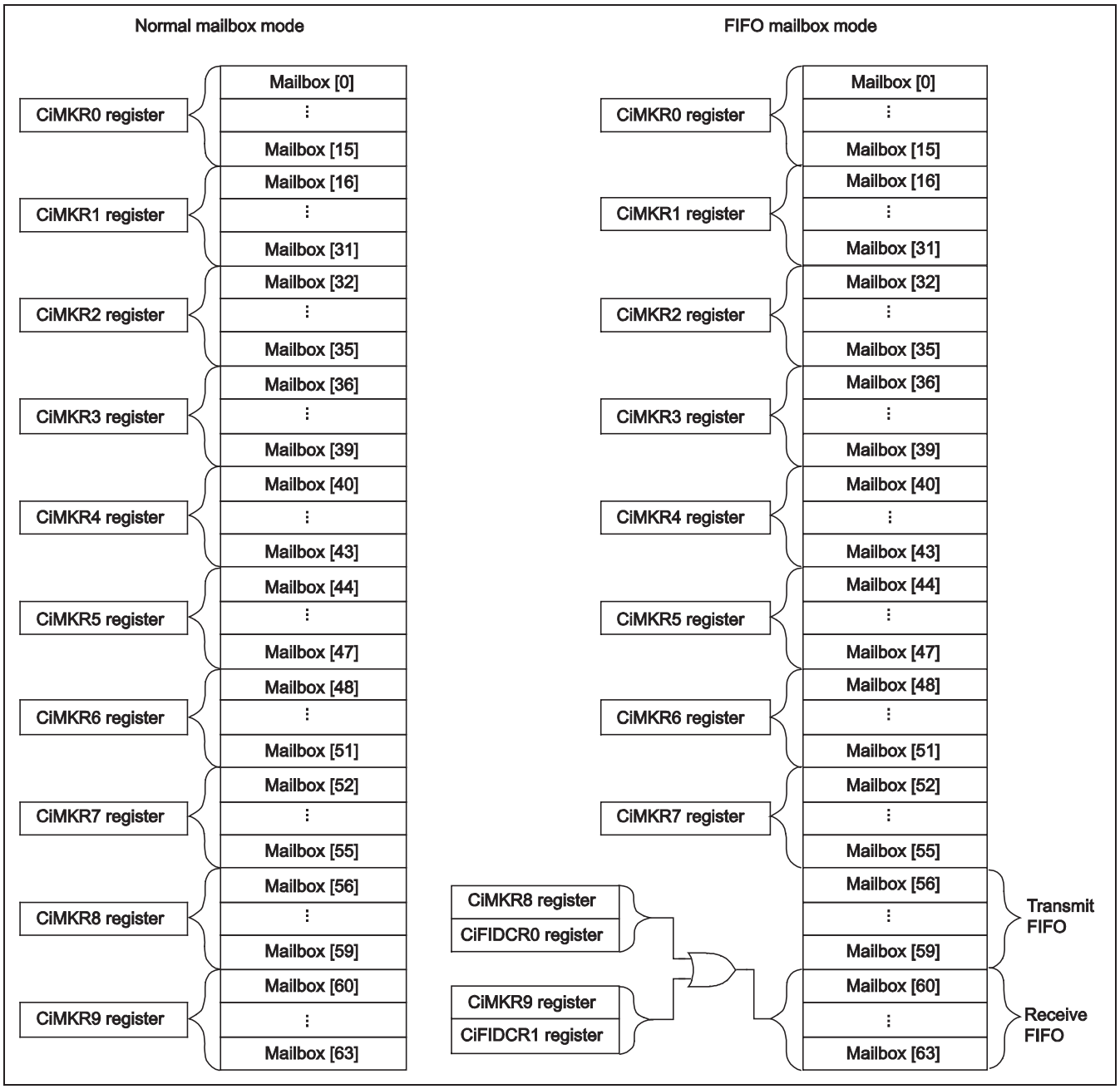


Figure 34.16 Correspondence of Mask Registers to Mailboxes (i = 0, 1)

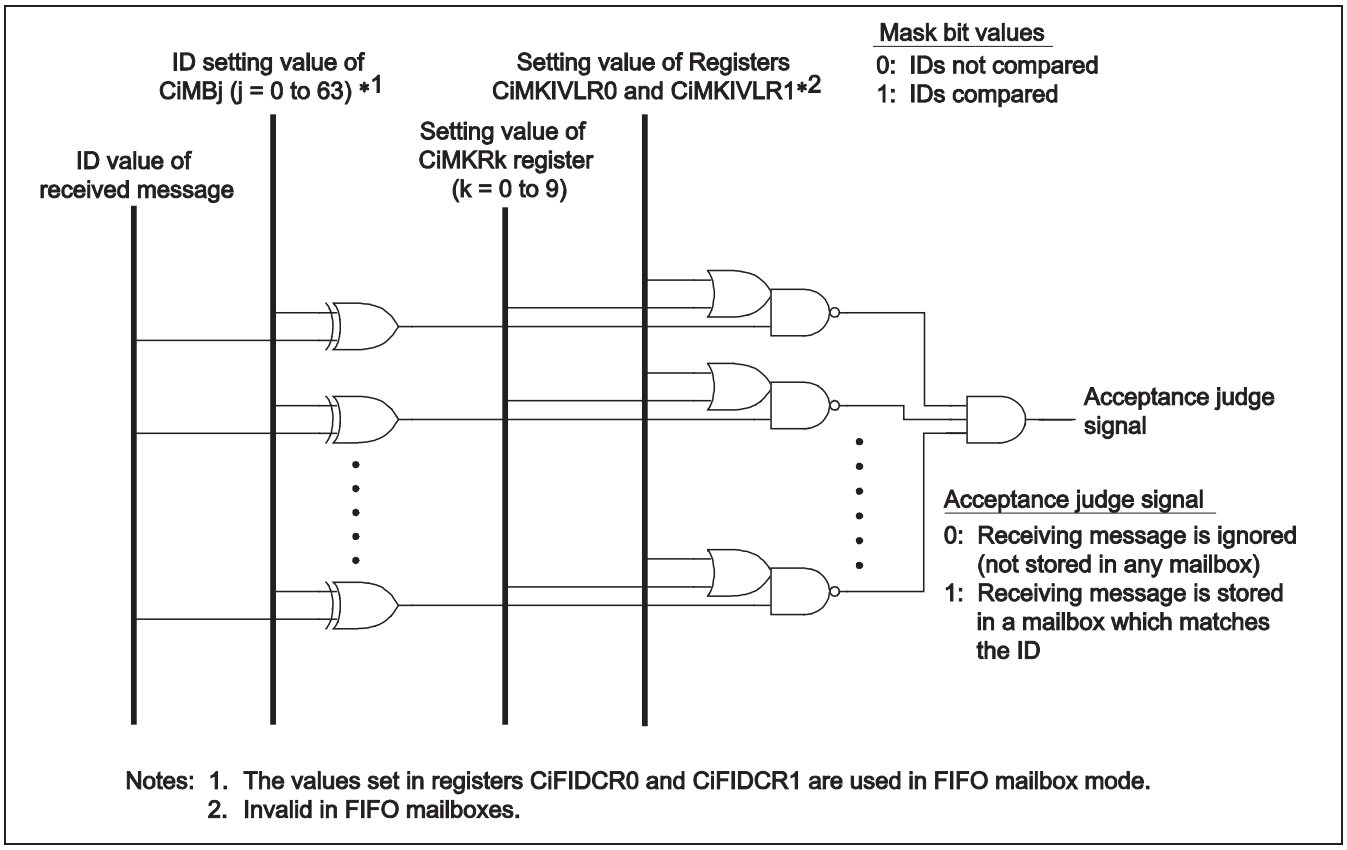


Figure 34.17 Acceptance Filtering (i = 0, 1)

34.8 Reception and Transmission

Table 34.11 lists the CAN communication mode configuration.

Table 34.11 Configuration for CAN Reception Mode and Transmission Mode

TRMREQ	RECREQ	ONESHOT	Communication Mode of Mailbox
0	0	0	Mailbox disabled or transmission being aborted
0	0	1	Configurable only when transmission or reception from a mailbox (programmed in one-shot mode) is aborted.
0	1	0	Configured as a receive mailbox for a data frame or a remote frame.
0	1	1	Configured as a one-shot receive mailbox for a data frame or a remote frame.
1	0	0	Configured as a transmit mailbox for a data frame or a remote frame.
1	0	1	Configured as a one-shot transmit mailbox for a data frame or a remote frame.
1	1	0	Do not set.
1	1	1	Do not set.

Note: TRMREQ, RECREQ, ONESHOT: Bits in CiMCTLj register (i = 0, 1; j = 32 to 63)

When a mailbox is configured as a receive mailbox or a one-shot receive mailbox, note the following:

1. Before a mailbox is configured as a receive mailbox or a one-shot receive mailbox, set the CiMCTLj register to "H'00".
2. A received message is stored into the first mailbox that matches the condition according to the result of receive mode configuration and acceptance filtering. Upon deciding a mailbox which stores the received message, the mailbox with the smaller number has higher priority.
3. In CAN operation mode, when a CAN module transmits a message whose ID matches with the ID/mask set of a mailbox configured to receive messages, the CAN module never receives the transmitted data. In self-test mode, however, the CAN module may receive its transmitted data. In this case, the CAN module sends an ACK.

When configuring a mailbox as a transmit mailbox or a one-shot transmit mailbox, note the following:

1. Before a mailbox is configured as a transmit mailbox or one-shot transmit mailbox, ensure that the CiMCTLj register is "H'00" and that there is no pending abort process.

34.8.1 Reception

Figure 34.18 shows an operation example of data frame reception in overwrite mode.

This example shows the operation of overwriting the first message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the CiMCTLj register.

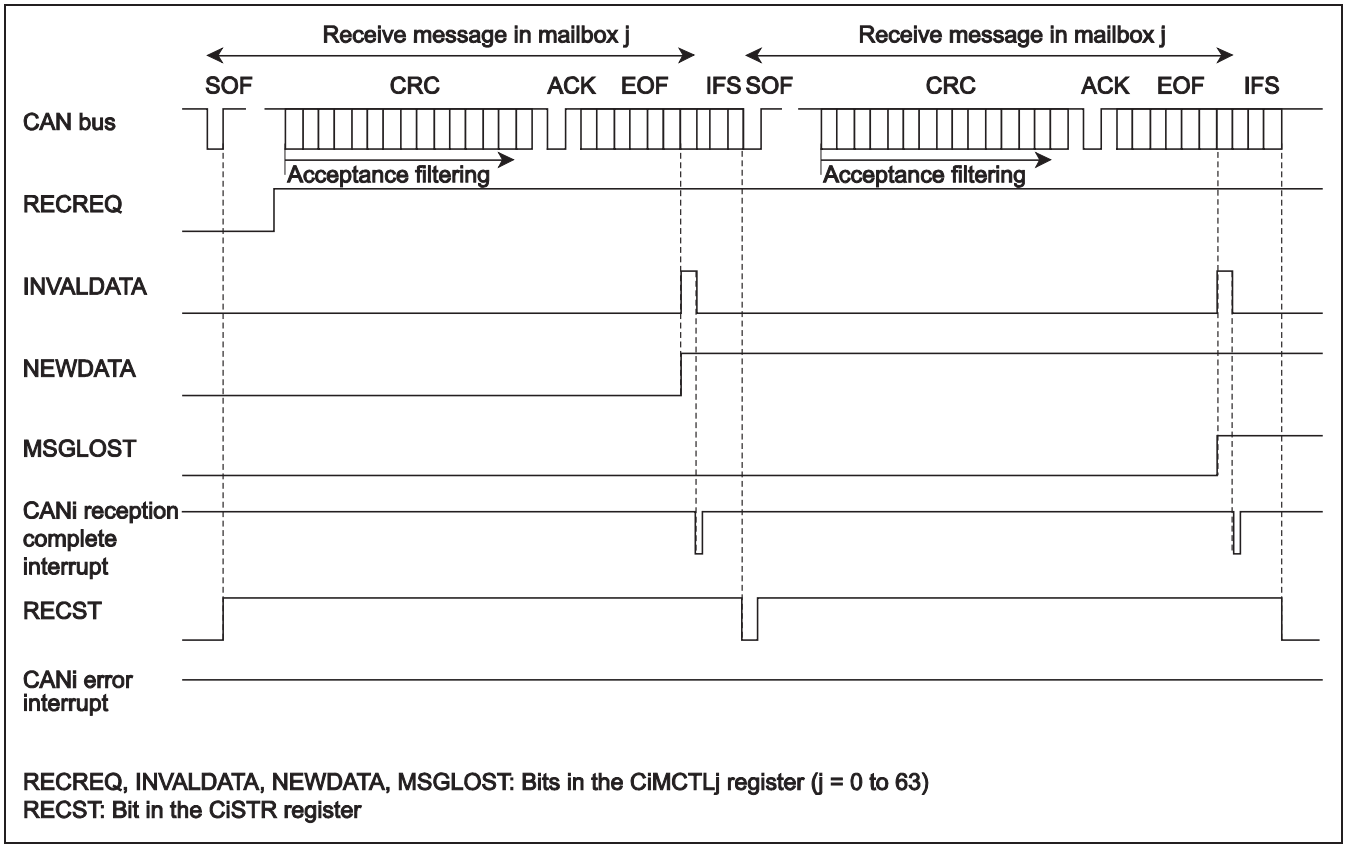


Figure 34.18 Operation Example of Data Frame Reception in Overwrite Mode (i = 0, 1)

1. When a SOF is detected on the CAN bus, the RECST bit in the CiSTR register is set to "1" (reception in progress) if the CAN module has no message ready to start transmission.
2. The acceptance filter procedure starts at the beginning of the CRC field to select the receive mailbox.
3. After a message has been received, the NEWDATA bit in the CiMCTLj register for the receive mailbox is set to "1" (new data being updated/stored in the mailbox). The INVALDATA bit in the CiMCTLj register is set to "1" (message is being updated) at the same time, and then the INVALDATA bit is set to "0" (message valid) again after the complete message is transferred to the mailbox.
4. When the interrupt enable bit in the CiMIER register for the receive mailbox is "1" (interrupt enabled), the CANi reception complete interrupt request is generated. This interrupt is generated when the INVALDATA bit is set to "0".
5. After reading the message from the mailbox, the NEWDATA bit needs to be set to "0" by a program.
6. In overwrite mode, if the next CAN message has been received into a mailbox whose NEWDATA bit is still set to "1", the MSGLOST bit in the CiMCTLj register is set to "1" (message has been overwritten). The new received message is transferred to the mailbox. The CANi reception complete interrupt request is generated the same as in 4.

Figure 34.19 shows the operation example of data frame reception in overrun mode. This example shows the operation of overrunning the second message when the CAN module receives two consecutive CAN messages that matches the receiving conditions of the CiMCTLj register.

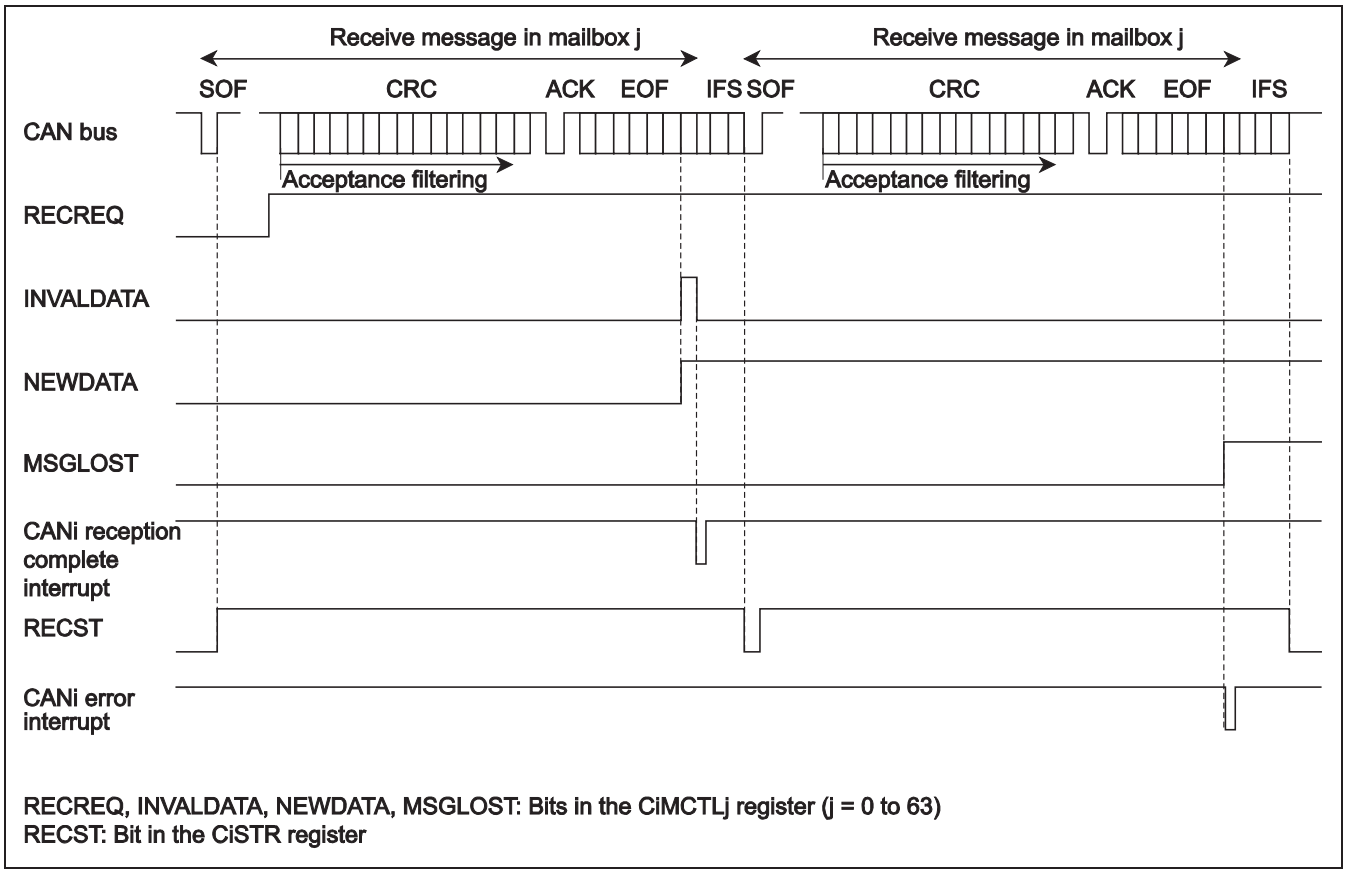


Figure 34.19 Operation Example of Data Frame Reception in Overrun Mode (i = 0, 1)

1. to 5. are the same as overwrite mode.

6. In overrun mode, if the next message has been received before the NEWDATA bit is set to "0", the MSGLOST bit in the CiMCTLj register is set to "1" (message has been overrun). The new received message is discarded and a CANi error interrupt request is generated if the corresponding interrupt enable bit in the CiEIER register is set to "1" (interrupt enabled).

34.8.2 Transmission

Figure 34.20 shows an operation example of data frame transmission.

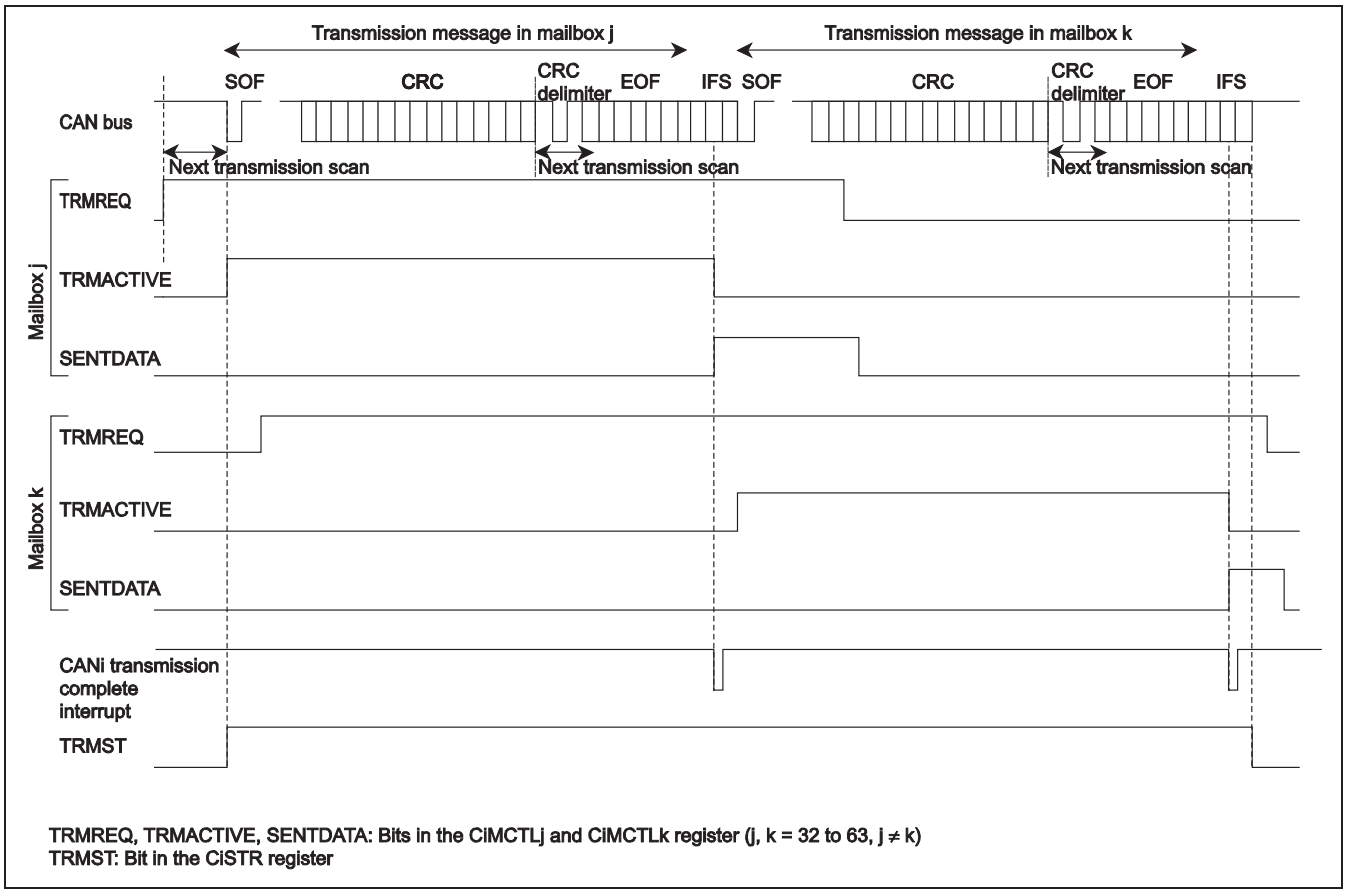


Figure 34.20 Operation Example of Data Frame Transmission (i = 0, 1)

1. When a TRMREQ bit in the CiMCTLj register is set to 1 (transmit mailbox) in bus-idle state, the mailbox scan procedure starts to decide the highest-priority mailbox for transmission. Once the transmit mailbox is decided, the TRMACTIVE bit in the CiMCTLj register is set to "1" (from when a transmission request is received until transmission is completed, or an error/arbitration lost has occurred), the TRMST bit in the CiSTR register is set to "1" (transmission in progress), and the CAN module starts transmission.*
2. If other TRMREQ bits are set, the transmission scan procedure starts with the CRC delimiter for the next transmission.
3. If transmission is completed without losing arbitration, the SENTDATA bit in the CiMCTLj register is set to "1" (transmission completed) and the TRMACTIVE bit is set to "0" (transmission is pending, or no transmission request). If the interrupt enable bit in the CiMIER register is "1" (interrupt enabled), the CANi transmission complete interrupt request is generated.
4. When requesting the next transmission from the same mailbox, set bits SENDTDATA and TRMREQ to "0", then set the TRMREQ bit to "1" after checking that bits SENDTDATA and TRMREQ have been set to "0".

Note: * If arbitration is lost after the CAN module starts transmission, the TRMACTIVE bit is set to "0". The transmission scan procedure is performed again to search for the highest-priority transmit mailbox from the beginning of the CRC delimiter. If an error occurs either during transmission or following the arbitration lost the transmission scan procedure is performed again from the start of the error delimiter to search for the highest-priority transmit mailbox.

34.9 CAN Interrupt

The CAN module provides the following CAN interrupts for each channel. Table 34.12 lists CAN interrupts.

- CANi reception complete interrupt (mailbox 0) [RXM0i]
- CANi reception complete interrupt (mailbox 1 to 63) [RXM1i]
- CANi transmission complete interrupt (mailbox 32 to 63) [TXMi]
- CANi reception FIFO interrupt [RXFi]
- CANi transmission FIFO interrupt [TXFi]
- CANi error interrupt [ERSi]

  There are eight types of interrupt sources for the CANi error interrupts. These sources can be determined by checking the CiEIFR register.
  - Bus error
  - Error-warning
  - Error-passive
  - Bus-off entry
  - Bus-off recovery
  - Receive overrun
  - Overload frame transmission
  - Bus lock

Table 34.12 CAN Interrupts

Module	Interrupt Symbol	Interrupt Source	Source Flag
CANi	ERSi	Bus lock detected	CiEIFR.BLIF
		Overload frame transmission detected	CiEIFR.OLIF
		Overrun detected	CiEIFR.ORIF
		Bus-off recovery detected	CiEIFR.BORIF
		Bus-off entry detected	CiEIFR.BOEIF
		Error-passive detected	CiEIFR.EPIF
		Error-warning detected	CiEIFR.EWIF
		Bus error detected	CiEIFR.BEIF
	RXFi	Receive FIFO message received (CiMIER1[29] = 0)	CiISR.RXFF
		Receive FIFO warning (CiMIER1[29] = 1)	
	TXFi	Transmit FIFO message transmission completed (CiMIER1[25] = 0)	CiISR.TXFF
		FIFO last message transmission completed (CiMIER1[25] = 1)	
	RXM0i	Mailbox 0 message received	CiMCTL0.NEWDATA
	RXM1i	Mailbox 1 to 63 message received	CiMCTL1.NEWDATA to CiMCTL63.NEWDATA
	TXMi	Mailbox 32 to 63 message transmission completed	CiMCTL32.SENTDATA to CiMCTL63.SENTDATA

Legend: i = 0, 1

(1) CANi reception complete interrupt (mailbox 0) [RXM0i]

After the CiMCTL0.NEWDATA bit is set by the completion of reception, if received data has been stored (the corresponding INVALDATA bit changes from "1" to "0"), the CiISR.RXM0F bit is set to "1" when CiMIER0[0] has been set to "1". When the mailbox 0 reception complete (RXM0) interrupt has been enabled, the RXM0 interrupt is requested to the interrupt controller.

To clear the RXM0 interrupt, clear the CiMCTL0.NEWDATA bit in the RXM0 interrupt handling routine. To change the CiIER.RXM0IE bit to disabled after having set the bit, make the change while no RXM0 interrupt is generated or during the RXM0 interrupt handling routine. This also applies to CiMIER0[0].

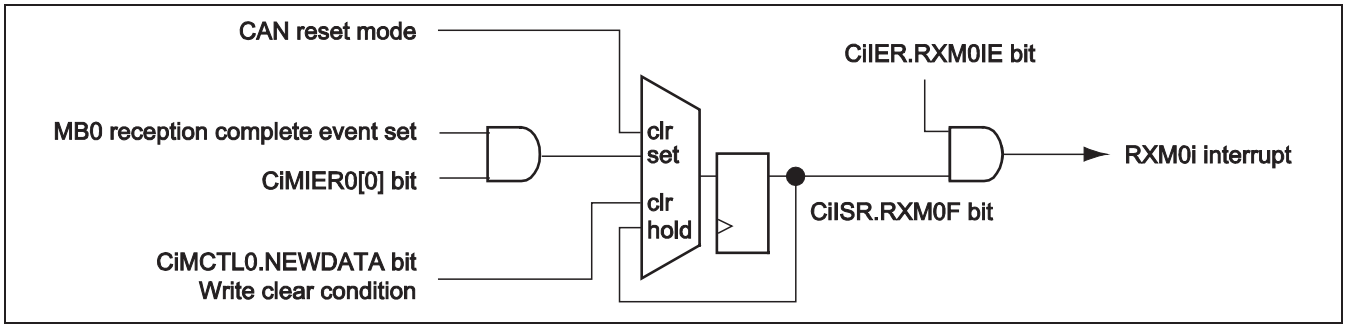


Figure 34.21 Block Diagram of CANi Reception Complete Interrupt (Mailbox 0) [RXM0i]

(2) CANi reception complete interrupt (mailbox 1 to 63) [RXM1i]

After the CiMCTLj.NEWDATA bit is set by the completion of reception, if received data has been stored (the corresponding INVALDATA bit changes from "1" to "0"), the CiISR.RXM1F bit is set to "1" when the CiMIER0 or CiMIER1 register bit corresponding to mailbox j has been set to "1". When the mailbox 1 to 63 reception complete (RXM1) interrupt has been enabled, the RXM1 interrupt is requested to the interrupt controller.

To clear the RXM1 interrupt, clear the CiMCTLj.NEWDATA bit in the RXM1 interrupt handling routine. To change the CiIER.RXM1IE bit to disabled after having set the bit, make the change while no RXM1 interrupt is generated or during the RXM1 interrupt handling routine. This also applies to CiMIER0[j] (j = 1 to 31) or CiMIER1[j-32] (j = 32 to 63).

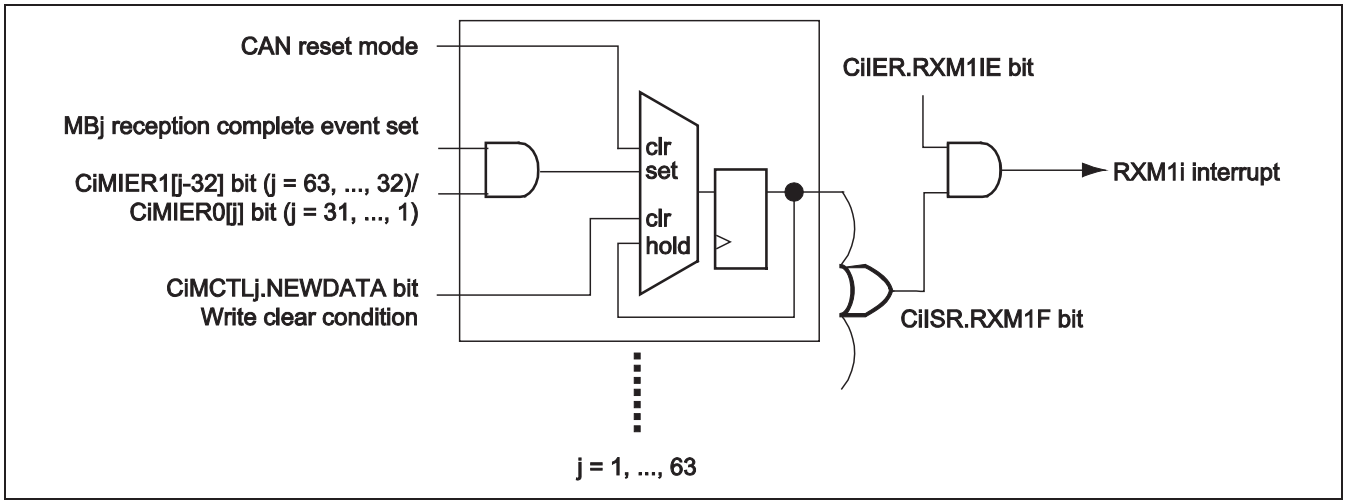


Figure 34.22 Block Diagram of CANi Reception Complete Interrupt (Mailbox 1 to 63) [RXM1i]

(3) CANi transmission complete interrupt (mailbox 32 to 63) [TXMi]

If the CiMCTLj.SENTDATA bit is set by the completion of transmission, the CiISR.TXMF bit is set to "1" when the CiMIER1 register bit corresponding to mailbox j has been set to "1". When the mailbox 32 to 63 transmission complete (TXM) interrupt has been enabled, the TXM interrupt is requested to the interrupt controller.

To clear the TXM interrupt, clear the CiMCTLj.SENTDATA bit in the TXM interrupt handling routine. To change the CiIER.TXMIE bit to disabled after having set the bit, make the change while no TXM interrupt is generated or during the TXM interrupt handling routine. This also applies to CiMIER1[j-32] (j = 32 to 63).

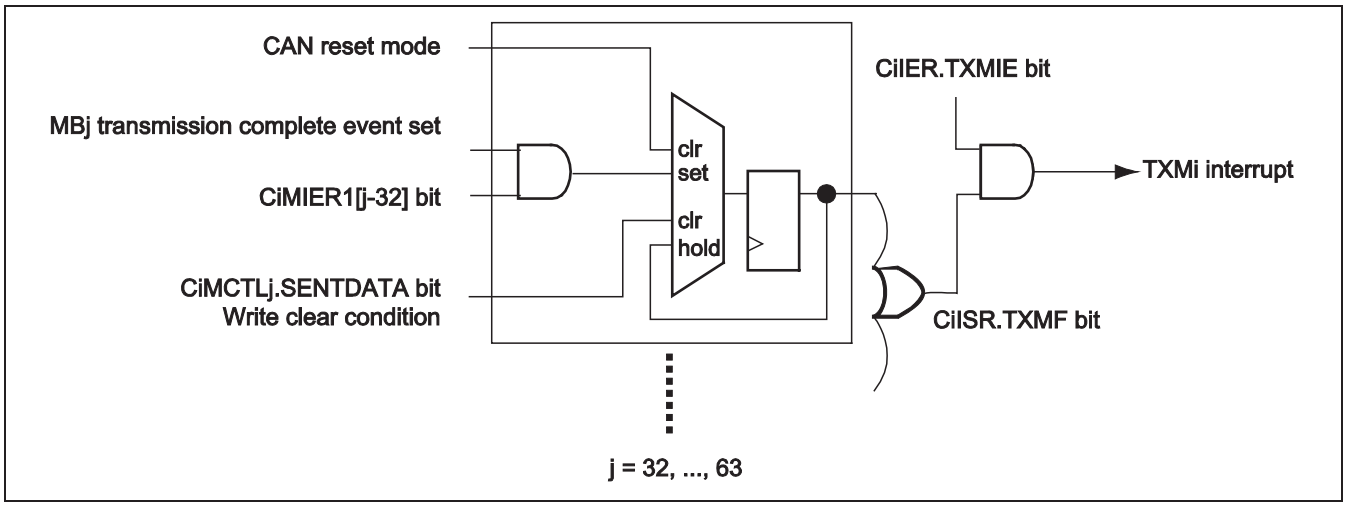


Figure 34.23 Block Diagram of CANi Transmission Complete Interrupt (Mailbox 32 to 63) [TXMi]

(4) CANi receive FIFO interrupt [RXFi]

If CiRFCR[6:5] are set by the reception of a receive FIFO message or by a warning with the settings of CiMIER1[29:28], the CiISR.RXFF bit is set to "1". When the receive FIFO (RXF) interrupt has been enabled with the CiIER.RXFIE bit, the RXF interrupt is requested to the interrupt controller.

To clear the RXF interrupt, clear the CiISR.RXFF bit in the RXF interrupt handling routine. To change the CiIER.RXFIE bit to disabled after having set the bit, make the change while no RXF interrupt is generated or during the RXF interrupt handling routine. This also applies to CiMIER1[28].

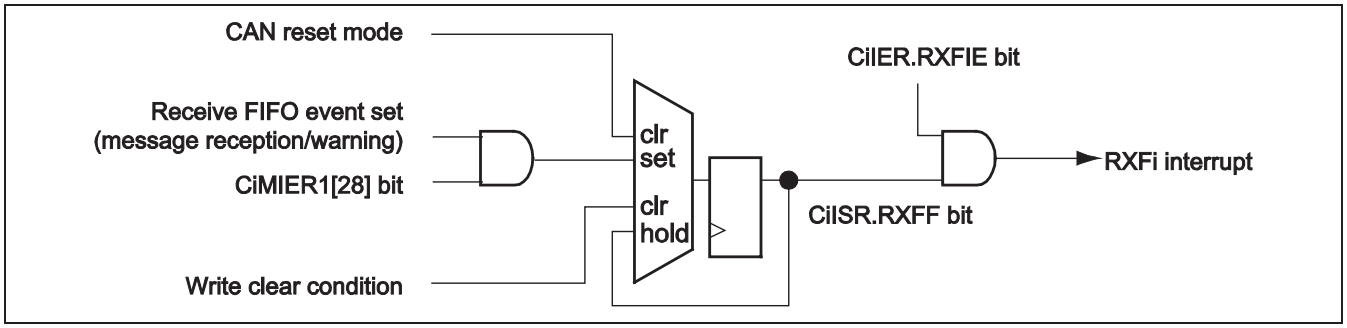


Figure 34.24 Block Diagram of CANi Receive FIFO Interrupt [RXFi]

(5) CANi transmit FIFO interrupt [TXFi]

When the transmission of a transmit FIFO message is counted for the specified number of times with the settings of CiMIER1 [25:24], the CiISR.TXFF bit is set to "1". When the transmit FIFO (TXF) interrupt has been enabled with the CiIER.TXFIE bit, the TXF interrupt is requested to the interrupt controller.

To clear the TXF interrupt, clear the CiISR.TXFF bit in the TXF interrupt handling routine. To change the CiIER.TXFIE bit to disabled after having set the bit, make the change while no TXF interrupt is generated or during the TXF interrupt handling routine. This also applies to CiMIER1[24].

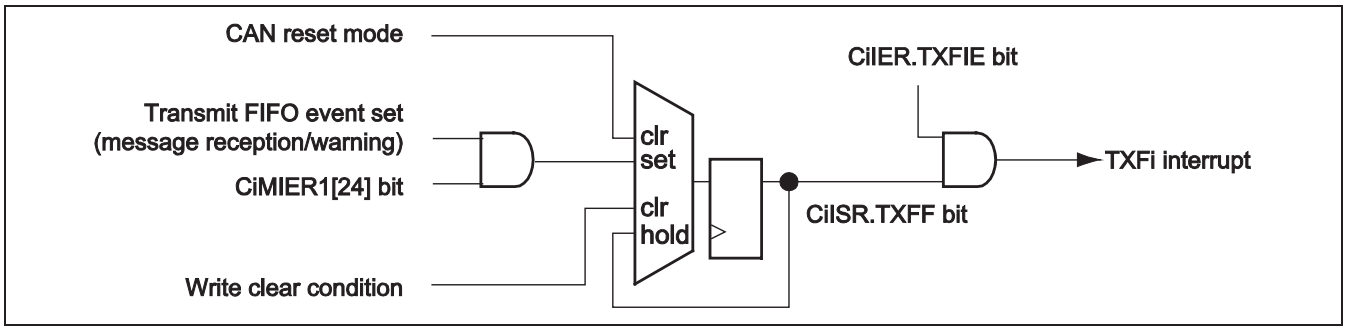


Figure 34.25 Block Diagram of CANi Transmit FIFO Interrupt [TXFi]

(6) CANi error interrupt [ERSi]

If CiEIFR[j] is set by a communication error, the CiISR.ERSF bit is set to "1" when the corresponding CiEIER[j] has been set to "1". When the error (ERS) interrupt has been enabled with the CiIER.ERSIE bit, the ERS interrupt is requested to the interrupt controller.

To clear the ERS interrupt, clear each CiEIFR[j] register bit in the ERS interrupt handling routine. To change the CiIER.ERSIE bit to disabled after having set the bit, make the change while no ERS interrupt is generated or during the ERS interrupt handling routine. This also applies to CiEIER[j] (j = 7 to 0).

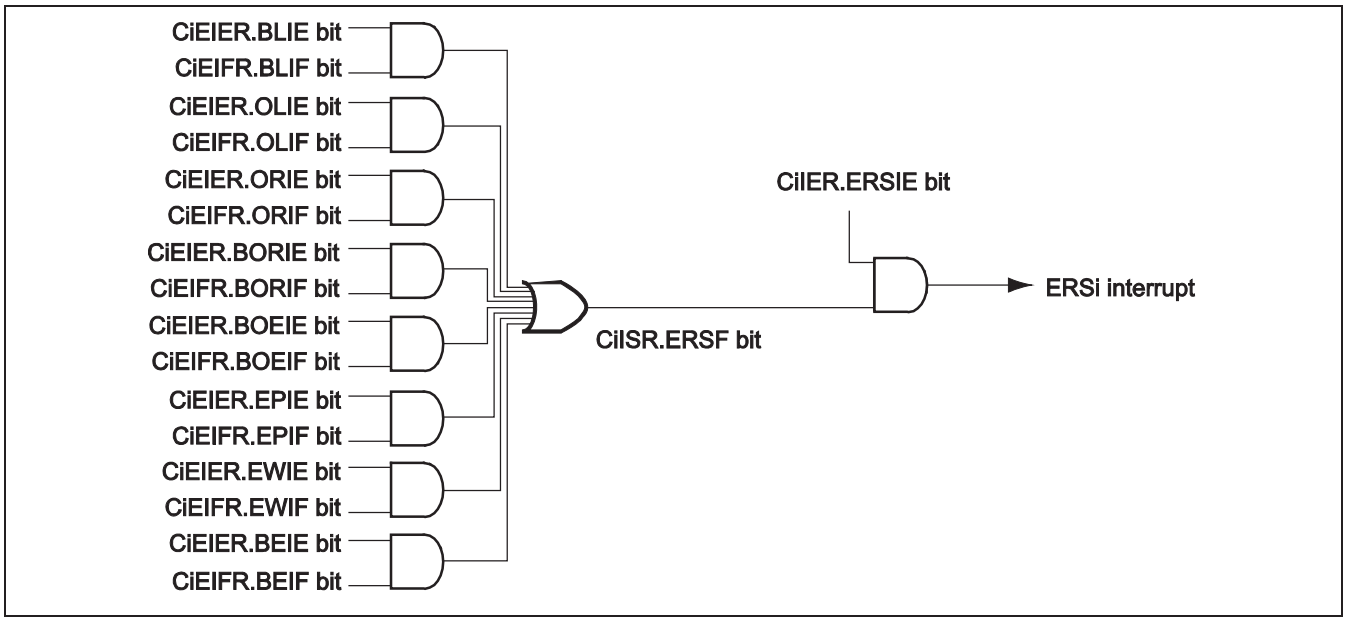


Figure 34.26 Block Diagram of CANi Error Interrupt [ERSi]

34.10 CAN Parity Check

The Parity bit generator for an Even Parity check is a simple XOR of each bit.

parity[0] = ^DataBus[7:0]

parity[1] = ^DataBus[15:8]

parity[2] = ^DataBus[23:16]

parity[3] = ^DataBus[31:24]

The Parity error detection for an Even Parity check is a simple XOR of each bit including the Parity bit. In case the result is equal to the Data Byte no error is generated. The detection logic is only working during read access for the selected byte.

parity_error[0] = { ^DataBus[7:0]} ^ parity[0]

parity_error[1] = { ^DataBus[15:8]} ^ parity[1]

parity_error[2] = { ^DataBus[23:16]} ^ parity[2]

parity_error[3] = { ^DataBus[31:24]} ^ parity[3]

Each memory location in the DPRAM consists of 36 bits. 32 bits are used for storage of user data. For each byte of a longword memory location a parity bit is allocated. The value of this parity bit is calculated by the parity generation logic for each byte and both data byte and parity bit are stored in memory during the same write access. The alignment of data bytes and corresponding parity bits in each memory location is shown in the following diagram:

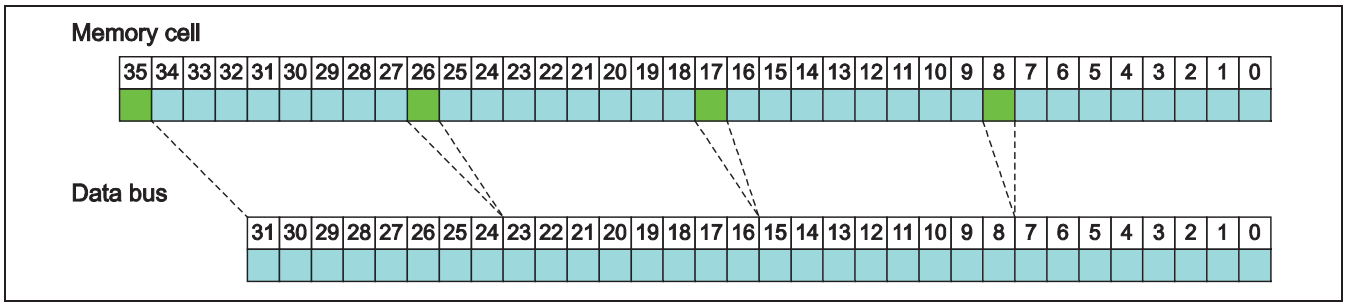


Figure 34.27 Parity bit alignment

35. Serial Communication Interface with FIFO (SCIF)

35.1 Overview

This LSI has serial communication interfaces with FIFO buffers (SCIF) that handles asynchronous communication and clock synchronous serial communication. The SCIF has two 16-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted communication. The following table lists the functions of each interface.

The presence of the SCK, RTS, and CTS pins depends on the product or channel. The synchronous mode and mode control functions are supported in the interface channel which has the pins related to these functions.

Modem control function is not supported by this product. The RTS# and CTS# pins, and related register bits are not supported also.

	Name	Function	Pin	Base Address	Remarks
0	SCIF-0	Asynchronous mode	RX0, TX0	H'E6E6 0000	—
1	SCIF-1	Asynchronous mode Clock synchronous mode	RX1, TX1 and SCK1*	H'E6E6 8000	Transmission/reception clock can be supplied externally from SCK1* pin.
2	SCIF-2	Asynchronous mode Clock synchronous mode	RX2, TX2 and SCK2*	H'E6E5 8000	Transmission/reception clock can be supplied externally from SCK2* pin.
3	SCIF-3	Asynchronous mode Clock synchronous mode	RX3, TX3 and SCK3*	H'E6EA 8000	Transmission/reception clock can be supplied externally from SCK3* pin.
4	SCIF-4	Asynchronous mode	RX4, TX4	H'E6EE 0000	—
5	SCIF-5	Asynchronous mode	RX5, TX5	H'E6EE 8000	—

Note: * SCKn respectively refer to SCIFn_SCK. (SCIF1: n = 1, SCIF2: n = 2, SCIF3: n = 3)

35.1.1 Features

The SCIF has the following features.

- Asynchronous serial communication mode

  The SCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support Universal Asynchronous Receiver/Transmitter (UART) or Asynchronous Communication Interface Adapter (ACIA). There is a choice of eight serial data transfer formats.

  — Data length: 7 or 8 bits

  — Stop bit length: 1 or 2 bits

  — Parity: Even/odd/none

  — Receive error detection: Parity, framing, and overrun errors

  — Break detection:

  A break is detected when a framing error lasts for more than 1 frame length at Space 0 (low level).

  When a framing error occurs, a break can also be detected by reading the RX pin level directly from the serial port register (SCSPTR).
- Clock synchronous serial communication mode

  The SCIF performs serial data communication synchronized with a clock. This feature enables serial data communication with other LSIs that support synchronous communication. There is a single serial data communication format for clock synchronous serial communication.

  — Data length: 8 bits

  — Receive error detection: Overrun errors
- Full-duplex communication capability

  The SCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 16-stage FIFO buffer structure, enabling continuous serial data transmission and reception.
- On-chip baud rate generator, enabling any bit rate to be selected

  The SCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock.
- Eight interrupt sources

  The SCIF has eight types of interrupt sources – receive-data-ready, receive-FIFO-data-full, break, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out and enables any of them to be requested independently.
- DMA data transfer

  When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer.
- The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.
- In asynchronous mode, a receive data ready (DR) or a timeout error (TO) can be detected during reception.

35.1.2 Block Diagram

Figure 35.1 shows the SCIF block diagram.

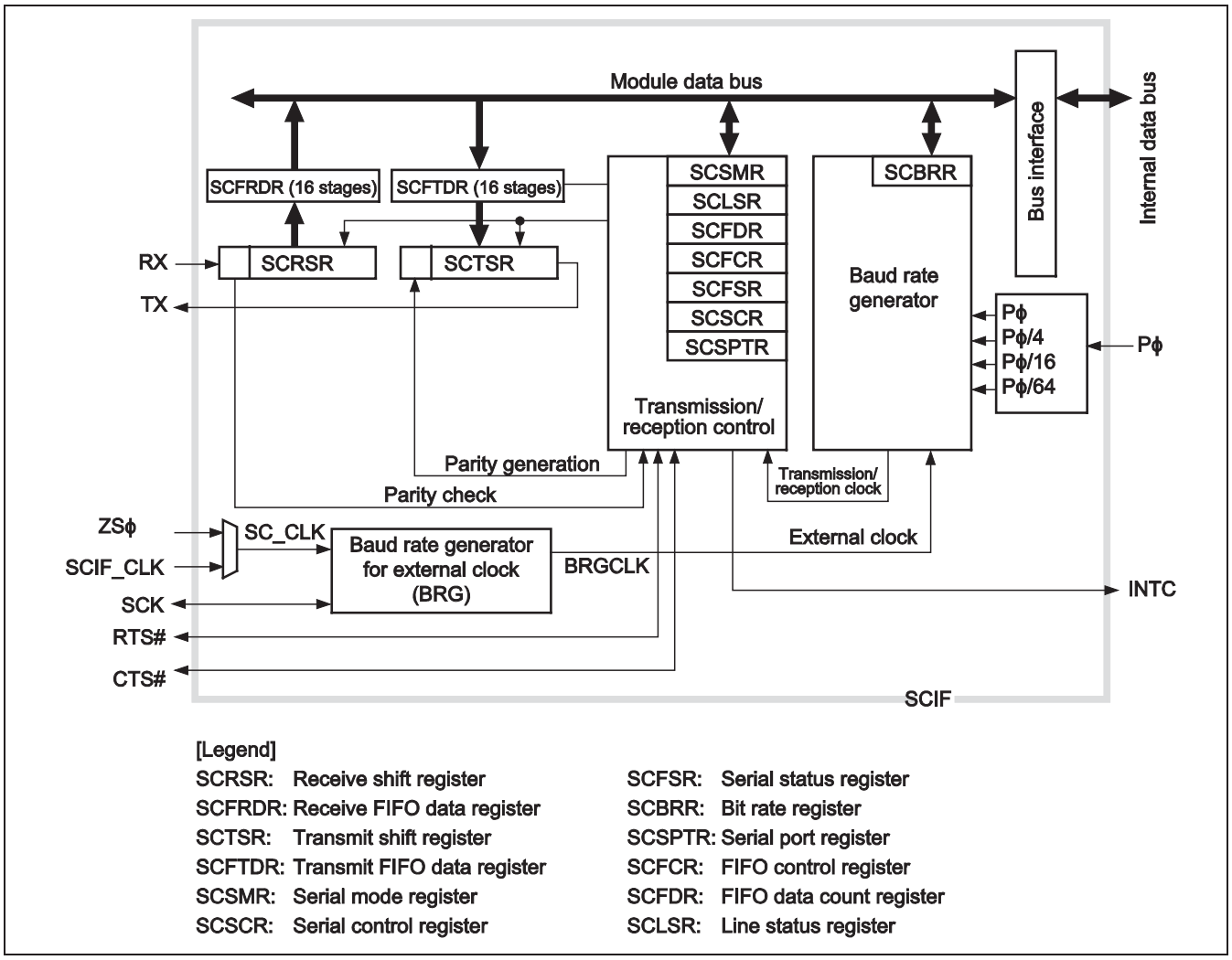


Figure 35.1 SCIF Block Diagram

35.1.3 Input/Output Pins

Table 35.1 shows the SCIF pin configuration. Pin functions can differ with the interface number. Other functions are also multiplexed on the same pins, so the multiplexed pin settings may restrict usage of the pins.

Table 35.1 Pin Configuration

Pin Name	Abbreviation	I/O	Function
Serial clock pin (SCIFn_SCK*)	SCK	I/O	Synchronous clock I/O
Receive data pin (RXn)	RX	Input	Receive data input
Transmit data pin (TXn)	TX	Output	Transmit data output
Baud rate generation clock pin	SCIF_CLK	Input	Clock for input to the baud rate generator for the external clock

Note: These pins are made to function as serial pins by setting up SCIF operation using bit C/A# in SCSMR, bits TE, RE, CKE[1:0] in SCSCR, and bit MCE in SCFCR. SCSPTR of the SCIF can be used to handle the transmission and detection of break states.

* n: Channel number

35.1.4 Register Configuration

Table 35.2 shows the registers in the SCIF.

Table 35.2 Register Configuration

Register Name	Abbreviation	R/W	Offset from Base Address	Initial Value	Access Size
Serial mode register	SCSMR	R/W	H'00	H'0000	16
Bit rate register	SCBRR	R/W	H'04	H'FF	8
Serial control register	SCSCR	R/W	H'08	H'0000	16
Transmit FIFO data register	SCFTDR	W	H’0C	Undefined	8
Serial status register	SCFSR	R/W*1	H'10	H'0060	16
Receive FIFO data register	SCFRDR	R	H’14	Undefined	8
FIFO control register	SCFCR	R/W	H'18	H'0000	16
FIFO data count register	SCFDR	R	H'1C	H'0000	16
Serial port register	SCSPTR	R/W	H'20	H'00XX*3	16
Line status register	SCLSR	R/W*2	H'24	H'0000	16
Frequency division register	DL	R/W	H'30	H'0000	16
Clock Select register	CKS	R/W	H'34	H'0000	16

Notes: 1. Only 0 can be written to bits 7 to 4, 1, and 0 to clear the flags. Bits 15 to 8, 3, and 2 are read-only bits and cannot be modified.
2. Only 0 can be written to bits 2 and 1 to clear the flags. Bits 15 to 3, and 1 are read-only bits and cannot be modified.
3. The initial values of SCSPTR bits 6, 4, 2, and 0 are undefined.

The table below lists the registers used in asynchronous mode, asynchronous mode with modem control, and clock synchronous mode. When setting up the registers, set the bits related to unsupported modes in each interface to their initial values. Otherwise, the SCIF may malfunction. Do not write to any registers other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from registers other than listed below are undefined.

Table 35.3 Register Settings in Each Mode

Bit	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
SCFRDR	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
SCFTDR	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
SCSMR	0	0	0	0	0	0	0	0	C	A	A	A	A	0	*	*
SCSCR	0	0	0	0	*	0	0	0	*	*	*	*	*	A	*	*
SCFSR	A	A	A	A	A	A	A	A	A	*	*	A	A	A	*	A
SCBRR	—	—	—	—	—	—	—	—	*	*	*	*	*	*	*	*
SCFCR	0	0	0	0	0	M	M	M	*	*	*	*	M	*	*	M
SCFDR	0	0	0	*	*	*	*	*	0	0	0	*	*	*	*	*
SCSPTR	0	0	0	0	0	0	0	0	M	M	M	M	C	C	*	*
SCLSR	0	0	0	0	0	0	0	0	0	0	0	0	0	A	0	*
DL	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
CKS	*	*	0	0	0	0	0	0	0	0	0	0	0	0	0	0

[Legend]

* : Used in any mode.

A : Used in asynchronous mode.

M : Used in asynchronous mode (modem control is enabled) (in addition to A).

C : Used in clock synchronous mode.

0 : Reserved (the write value should always be 0.)

— : Undefined

35.2 Register Descriptions

35.2.1 Receive Shift Register (SCRSR)

SCRSR is a register that receives serial data.

The SCIF sets serial data input to the SCRSR from the RX pin in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is transferred to the receive FIFO data register SCFRDR, automatically.

SCRSR cannot be read from and written to by the CPU.

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	—	—	—	—	—	—	—	—

35.2.2 Receive FIFO Data Register (SCFRDR)

SCFRDR is a 16-stage FIFO register that stores received serial data.

When the SCIF has received one byte of serial data, it transfers the received data from the receive shift register (SCRSR) to SCFRDR for storage, and reception is thus completed. SCRSR is then ready for reception, and is capable of receiving up to 16 consecutive bytes of data before SCFRDR is full.

SCFRDR is a read-only register and cannot be modified by the CPU. Note that the read value will be undefined while there is no receive data in SCFRDR. When SCFRDR is full of receive data, subsequent serial data is lost.

SCFRDR is read as an undefined value after a power-on reset.

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R

35.2.3 Transmit Shift Register (SCTSR)

SCTSR is a register that transmits serial data.

To perform serial data transmission, the SCIF first transfers transmit data from the transmit FIFO data register (SCFTDR) to SCTSR, then sends the data to the TX pin starting with the LSB (bit 0). When transmission of one byte is completed, the SCIF transfers the next transmit data from SCFTDR to SCTSR automatically, then starts transmission.

SCTSR cannot be read from and written to directly by the CPU.

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	—	—	—	—	—	—	—	—

35.2.4 Transmit FIFO Data Register (SCFTDR)

SCFTDR is an 8-bit FIFO register of 16 stages that stores data for serial transmission.

If SCTSR is empty after transmit data has been written to SCFTDR, the SCIF transfers the data from SCFTDR to SCTSR and starts serial transmission.

SCFTDR is a write-only register and cannot be read from by the CPU. Writing further data to SCFTDR is no longer possible when it is full (contains 16 bytes of transmit data). Attempts at writing data to the register in this situation are ignored.

SCFTDR is read as an undefined value on a power-on reset.

Bit:	7	6	5	4	3	2	1	0
Initial value:	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W

35.2.5 Serial Mode Register (SCSMR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	C/A#	CHR	PE	O/E#	STOP	—	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W

SCSMR is a 16-bit register that sets the SCIF's serial transfer format and selects the baud rate generator clock source.

SCSMR can always be read from and written to by the CPU.

SCSMR is initialized to H'0000 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	C/A#	0	R/W	Communication Mode Selects asynchronous mode or clock synchronous mode for the SCIF operation. 0: Asynchronous mode 1: Clock synchronous mode Note: Whether clock synchronous mode can be selected or not depends on the interface.
6	CHR	0	R/W	Character Length Selects 7 or 8 bits for asynchronous mode data length. In clock synchronous mode, the data length is fixed at 8 bits regardless of the CHR bit setting. 0: 8 bits 1: 7 bits* Note: * When the 7-bit data is selected, the MSB (bit 7) in the transmit FIFO data register (SCFTDR) is not transmitted.
5	PE	0	R/W	Parity Enable Determines whether parity bit is added in transmission or not, and parity bit is checked in reception in asynchronous mode or not. In clock synchronous mode, the parity bit is not added and checked regardless of the PE bit setting. When bit PE is set to 1, the parity (even or odd) specified by bit O/E# is added to transmit data. In reception, the parity bit is checked for the parity (even or odd) specified by bit O/E#. 0: Disables parity bit addition and check. 1: Enables parity bit addition and check.

Bit	Bit Name	Initial Value	R/W	Description
4	O/E#	0	R/W	Parity Mode Selects either even or odd parity to use in parity addition and check. In asynchronous mode, the O/E# bit setting is valid only when bit PE is set to 1, enabling parity bit addition and check. In clock synchronous mode or when parity addition or check is disabled in asynchronous mode, the O/E# bit setting is invalid. 0: Even parity*1 1: Odd parity*2 Notes: 1. When even parity is set, the parity bit is added in transmission so that the total number of 1-bits in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is even. 2. When odd parity is set, the parity bit is added in transmission so that the total number of 1-bits in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bits in the receive character plus the parity bit is odd.
3	STOP	0	R/W	Stop Bit Length Selects 1 bit or 2 bits as the stop bit length in asynchronous mode. The stop bit setting is valid only in asynchronous mode. Since the stop bit is not added in clock synchronous mode, the STOP bit setting is invalid in this mode. In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit. If it is 0, it is treated as the start bit of the next transmit character. 0: 1 stop bit*1 1: 2 stop bits*2 Notes: 1. In transmission, a single 1-bit (stop bit) is added to the end of a transmit character before it is sent. 2. In transmission, two 1-bits (stop bits) are added to the end of a transmit character before it is sent.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	CKS[1:0]	00	R/W	Clock Select 1 and 0 These bits select the clock source for the on-chip baud rate generator. The clock source can be selected from Pϕ, Pϕ/4, Pϕ/16, and Pϕ/64, according to the setting of bits CKS1 and CKS0. 00: Pϕ 01: Pϕ/4 10: Pϕ/16 11: Pϕ/64 Note: Pϕ: Peripheral clock (frequency dividing CPU clock into 12)

35.2.6 Serial Control Register (SCSCR)

SCSCR is a register that enables or disables transmission/reception by the SCIF, enables or disables interrupt requests, and selects transmission/reception clock source for the SCIF.

SCSCR can always be read from and written to by the CPU.

SCSCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	TEIE	—	—	—	TIE	RIE	TE	RE	REIE	TOIE	CKE[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	TEIE	0	R/W	Transmit End Interrupt Enable When a transmit-end request is enabled by the TIE bit, the TEIE bit selects the source of the transmit end interrupt request from the following: • Setting the TDFE flag in SCFSR • Setting the TEND flag in SCFSR 0: The transmit FIFO data empty (TDFE) interrupt request is used. 1: The transmit end (TEND) interrupt request is used.
10 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable Enables or disables a transmit-FIFO-data-empty interrupt (TDFE) request when the TEIE bit in SCSCR is pulled 0, if the following conditions are satisfied: • Serial transmit data has been transferred from SCFTDR to SCTSR, • The number of data bytes in SCFTDR is equal to or less than the transmit trigger count, and • The TDFE flag in SCFSR is set to 1. Enables or disables a transmit-end interrupt (TEND) request when the TEIE bit of SCSCR is set to 1, if the following conditions are satisfied: • Transmission was ended because there is no valid data in SCFTDR when the last bit of the transmit character in SCTSR was transmitted, and • The TEND flag of SCFSR is set to 1. 0: When the TEIE bit is 0, disables transmit-FIFO-data-empty interrupt (TDFE) request.* When the TEIE bit is 1, disables transmit-end interrupt (TEND) request.* 1: When the TEIE bit is 0, enables transmit-FIFO-data-empty interrupt (TDFE) request. When the TEIE bit is 1, enables transmit-end interrupt (TEND) request.
6	RIE	0	R/W	Receive Interrupt Enable Enables or disables a receive-FIFO-data-full interrupt request when the RDF flag in SCFSR is set to 1, a receive-data-ready interrupt request when the DR flag in SCFSR is set to 1, a receive-error interrupt request when the ER flag in SCFSR is set to 1, a break interrupt request when the BRK flag in SCFSR is set to 1, and an overrun error interrupt request when the ORER flag in SCLSR is set to 1. 0: Disables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests. 1: Enables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests.
5	TE	0	R/W	Transmit Enable Enables or disables the start of SCIF serial transmission. The SCIF starts serial transmission when transmit data is written to the SCFTDR while TE is 1. Before setting TE to 1, set SCSMR and SCFCR to specify the transmission format and reset the transmit FIFO. 0: Disables transmission.* 1: Enables transmission.*

Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	Receive Enable Enables or disables the start of SCIF serial reception. When RE is 1, the SCIF starts serial reception by detecting a start bit in asynchronous mode or by detecting a synchronization clock input in clock synchronous mode. Before setting RE to 1, set SCSMR and SCFCR to specify the reception format and reset the receive FIFO. 0: Disables reception.* 1: Enables reception. Note: Even if RE is cleared to 0, the DR, ER, BRK, RDF, FER, PER, TO and ORER flags are not affected, and retain their states.
3	REIE	0	R/W	Receive Error Interrupt Enable Enables or Disables generation of receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests. 0: Disables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.* 1: Enables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests. Note: * When REIE is 1, ER, BRK or ORER interrupt requests will occur even if RIE is cleared to 0. This setting is used to notify the interrupt controller of ER, BRK, and ORER interrupt requests during DMAC transfer.
2	TOIE	0	R/W	Timeout Interrupt Enable Enables or disables generation of timeout interrupt (TO) requests when the TO flag in SCLSR is set to 1. 0: Disables timeout interrupts (TO). 1: Enables timeout interrupts (TO).
1, 0	CKE[1:0]	00	R/W	Clock Enable 1 and 0 These bits select the SCIF clock source and enables or disables the clock output from the SCK pin. Whether the SCK pin functions as a serial clock output pin or a serial clock input pin is determined by combination of the CKE[1:0] bits settings. To specify synchronization clock output in clock synchronous mode, set C/A# to 1 in SCSMR then set CKE[1:0]. See Table 35.4 for the bit settings.

Table 35.4 Clock Selection

CKE[1:0]	Mode	Clock Source	SCK Pin
00	Asynchronous mode	Internal clock (Pϕ, Pϕ/4, Pϕ/16, Pϕ/64)	The SCK pin is not used. The SCK pin functions as an input pin (Input signals are ignored). (Initial value)
	Clock synchronous mode		The SCK pin outputs the synchronization clock. (Initial value)
01	Asynchronous mode		The SCK pin outputs the clock (with a frequency 16 times the bit rate).
	Clock synchronous mode		The SCK pin outputs the synchronization clock.
10	Asynchronous mode	Baud rate generator output for external clock or SCK	When SC_CLK is selected: The SCK pin is an input pin (Input signals are ignored). Set the SC_CLK frequency so that the frequency of BRGCLK is 16 times the bit rate.
			When SCK is selected: The SCK pin inputs the clock (with a frequency 16 times the bit rate).
	Clock synchronous mode	SCK*	The SCK pin inputs the synchronization clock.
11	Prohibited		

Notes: Some interfaces cannot select the clock synchronous mode.
* It is not allowed to set synchronous communication using SC_CLK for input.

35.2.7 Serial Status Register (SCFSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PER[3:0]				FER[3:0]				ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R	R	R/W*	R/W*

Note: Only 0 can be written to clear the flag.

SCFSR is a 16-bit register. The lower 8 bits are a status flag that indicates the operating status of the SCIF, and the upper 8 bits indicate the number of reception errors of data in the receive FIFO register.

SCFSR can always be read from and written to by the CPU. However, the flags ER, TEND, TDFE, BRK, RDF, and DR cannot be written by 1. The FER and PER flags are read-only flags and cannot be modified.

SCFSR is initialized to H'0060 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	PER[3:0]	All 0	R	Parity Error Count These bits indicate the number of parity errors of receive data stored in the receive FIFO data register (SCFRDR). After the ER is set in SCFSR, the value represented by bits 15 to 12 indicates the number of parity errors. If a parity error occurs in all 16-byte receive data in SCFRDR, PER3 to PER0 are cleared to 0.
11 to 8	FER[3:0]	All 0	R	Framing Error Count These bits indicate the number of framing errors of receive data stored in the receive FIFO data register (SCFRDR). After the ER bit is set in SCFSR, the value represented by bits 11 to 8 indicates the number of framing errors. If a framing error occurs in all 16-byte receive data in SCFRDR, FER3 to FER0 are cleared to 0.
7	ER	0	R/W*	Receive Error Indicates that a framing error or a parity error has occurred in reception.*1 The ER flag is not affected by an error and retains its previous state when the RE bit is 0 in SCSCR. If a receive error occurs, receive data will be transferred to SCFRDR and reception operation will be continued. Whether there is a receive error in data read from SCFRDR can be determined by the FER and PER bits in SCFSR. 0: Indicates that no framing or parity error has occurred in reception. [Clearing conditions] • A power-on reset is executed. • 0 is written to ER. 1: Indicates that a framing error or a parity error has occurred in reception. [Setting conditions] • The SCIF checks whether the stop bit at the end of receive data is 1, but the stop bit is 0.*2 • The number of 1-bits in receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/E# bit in SCSMR during reception. Note: In the 2-stop-bit mode, only the first stop bit is checked that the value is 1; the second stop bit is not checked.

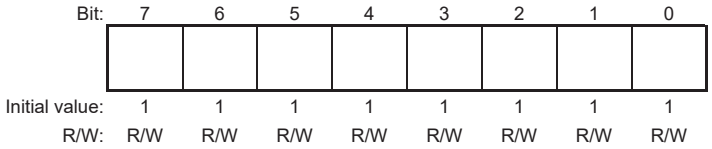
Bit	Bit Name	Initial Value	R/W	Description
6	TEND	1	R/W*	Indicates that transmission has been ended * because there was no valid data in SCFTDR when the last bit of the transmit character was transmitted. 0: Indicates that transmission is in progress. [Clearing conditions] • Transmit data is written to SCFTDR, and 0 is written to TEND. • Data is written to SCFTDR by the DMAC. 1: Indicates that transmission has been ended. [Setting conditions] • A power-on reset is executed. • The TE bit in SCSCR is 0. • There is no transmit data in SCFTDR when the last bit of a 1-byte serial transmission character is transmitted. Note: When transmit data is written to SCFTDR by the DMAC in clock synchronous mode, the TEND flag may not be cleared. Therefore, if the DMAC is used for transmission in clock synchronous mode, the TEND flag should be read using the following procedure. 1. Check that data transfer is completed in the DMAC. 2. Read the TEND flag. 3. If TEND = 1, clear the TEND flag to 0. 4. Read the TEND flag again. 5. Use the second read TEND flag.
5	TDFE	1	R/W*	Transmit FIFO Data Empty Indicates that the SCIF has transferred data from SCFTDR to SCTSR, the number of data bytes in SCFTDR becomes equal to or less than the transmit trigger count specified by the TTRG1 and TTRG0 bits in SCFCR, and SCFTDR is ready to be written by new transmit data. SCFTDR is a 16-byte FIFO register. The maximum number of bytes that can be written to when TDFE = 1 is “16 – [the transmit trigger count]”. If data exceeding this value is attempted to be written, the data will be ignored. The number of data bytes in SCFTDR is indicated by the upper bits of SCFDR. If the number of data written in SCFTDR is equal to or less than the transmit trigger count, this bit will be set to 1 even if it is cleared to 0 after it is read as 1. 0: Indicates that the number of transmit data written to SCFTDR exceeds the transmit trigger count. [Clearing conditions] • Transmit data exceeding the specified transmit trigger count have been written to SCFTDR, and 0 is written to TDFE. • Transmit data exceeding the specified transmit trigger count have been written to SCFTDR by the DMAC. 1: Indicates that the number of transmit data in SCFTDR is equal to or less than the transmit trigger count. [Setting conditions] • A power-on reset is executed. • The number of transmit data in SCFTDR is equal to or less than the transmit trigger count after transmission.

Bit	Bit Name	Initial Value	R/W	Description
4	BRK	0	R/W*	Break Detect Indicates that a receive data break signal has been detected. If a break signal is detected, receive data (H'00) transfer to SCFRDR is stopped. After the break is canceled and the receive signal returns to 1, the receive data transfer resumes. 0: Indicates that no break signal has been received. [Clearing conditions] • A power-on reset is executed. • 0 is written to BRK. 1: Indicates that a break signal has been received. [Setting condition] • Data with a framing error is received, followed by the space "0" (low level) for at least one frame length.
3	FER	0	R	Framing Error Indicates that a framing error has been found in the data that is to be read next from SCFRDR in asynchronous mode. 0: Indicates that there is no framing error in the receive data that is to be read from SCFRDR. [Clearing conditions] • A power-on reset is executed. • There is no framing error in the data that is to be read next from SCFRDR. 1: Indicates that there is a framing error in the receive data that is to be read from SCFRDR. [Setting condition] • There is a framing error in the data that is to be read next from SCFRDR.
2	PER	0	R	Parity Error This bit indicates that a parity error has been found in the data that is to be read next from SCFRDR in asynchronous mode. 0: Indicates that there is no parity error in the receive data that is to be read from SCFRDR. [Clearing conditions] • A power-on reset is executed. • There is no parity error in the data that is to be read next from SCFRDR. 1: Indicates that there is a parity error in the receive data that is to be read from SCFRDR. [Setting condition] • There is a parity error in the data that is to be read next from SCFRDR.

Bit	Bit Name	Initial Value	R/W	Description
1	RDF	0	R/W*	Receive FIFO Data Full Indicates that the received data has been transferred from SCRSR to SCFRDR, and the number of receive data bytes in SCFRDR becomes equal to or more than the receive trigger count specified by the RTRG1 and RTRG0 bits in SCFCR. SCFRDR is a 16-byte FIFO register. When RDF = 1, data equal to or more than the number of receive trigger data bytes can be read. When SCFRDR is empty, SCFRDR is read as an undefined value. The number of receive data bytes in SCFRDR is indicated by the lower bits of SCFDR. If the number of data in SCFRDR is equal to or more than the trigger count, this bit will be set to 1 even if it is cleared to 0. At this time, read receive data until the number of data in SCFRDR is less than the trigger count, read RDF as 1, and then clear RDF. 0: Indicates that the number of receive data bytes in SCFRDR is less than the specified receive trigger count. [Clearing conditions] • A power-on reset is executed. • SCFRDR is read until the number of receive data bytes in SCFRDR is less than the receive trigger count, and 0 is written to RDF. • SCFRDR is read by the DMAC until the number of receive data bytes in SCFRDR is less than the receive trigger count. 1: Indicates that the number of receive data bytes in SCFRDR is equal to or more than the specified receive trigger count. [Setting condition] • Receive data more than the receive trigger count have been stored in SDFRDR.
0	DR	0	R/W*	Receive Data Ready Indicates that the number of data bytes in SCFRDR is less than the receive trigger count and that no further data has been received for at least 15 etu after the stop bit of the data received last in asynchronous mode. This bit is not set in clock synchronous mode. 0: Indicates that data is being received or has been successfully received, and there is no receive data in SCFRDR. [Clearing conditions] • A power-on reset is executed. • All the receive data in SCFRDR has been read, and 0 is written to DR. • All the receive data in SCFRDR has been read by the DMAC. 1: Indicates that no further receive data has been received. [Setting condition] • The receive FIFO data register (SCFRDR) has the number of data byte that is below the receive trigger number of data bytes and no further data has arrived for at least 15 etu after the stop bit of the data received last. Note: etu: Elementary Time Unit (time for transfer of 1 bit) Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.

Note: Writing 0 is only available to clear the flag.

35.2.8 Bit Rate Register (SCBRR)



SCBRR is an 8-bit register that sets the serial transmission/reception bit rate in accordance with the baud rate generator operating clock selected by the CKS1 and CKS0 bits in SCSMR. This baud rate generator is intended for Pϕ, Pϕ/4, Pϕ/16, and Pϕ/64. For details on the baud rate generator for external clock, see section 35.6, Baud Rate Generator for External Clock (BRG).

SCBRR can always be read from and written to by the CPU except for during transfer.

SCBRR is initialized to H'FF by a power-on reset.

The SCBRR setting is determined by the following equation:

[Asynchronous mode]

$$N = \frac{P\phi}{64 \times 2^{2n-1} \times B} \times 10^6 - 1$$

[Clock synchronous mode]

$$N = \frac{P\phi}{8 \times 2^{2n-1} \times B} \times 10^6 - 1$$

B: Bit rate (bit/s)

N: SCBRR setting for the baud rate generator ($0 \leq N \leq 255$) (which satisfies the electrical characteristics)

Pϕ: Peripheral module operating frequency (MHz)

N: Baud rate generator input clock (n = 0, 1, 2, 3)
(See the Table 35.5 for the relation between n and the clock.)

Table 35.5 SCSMR Settings

n	Clock	SCSMR.CKS[1:0] Setting
0	Pϕ	00
1	Pϕ/4	01
2	Pϕ/16	10
3	Pϕ/64	11

The bit rate error in asynchronous mode is determined by the following equation:

$$\text{error (\%)} = \left\{ \frac{P\phi \times 10^6}{(N+1) \times B \times 64 \times 2^{2n-1}} - 1 \right\} \times 100$$

35.2.9 FIFO Control Register (SCFCR)

SCFCR is a register that resets data counts and sets the number of trigger data bytes for the transmit and receive FIFO registers. It also has a loopback test enable bit.

SCFCR can always be read from and written to by the CPU except for during transfer.

SCFCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	RSTRG[2:0]			RTRG[1:0]		TTRG[1:0]		MCE	TFRST	RF RST	LOO P
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 8	RSTRG[2:0]	000	R/W	RTS Output Active Trigger The RTS# signal is high when the number of receive data bytes stored in SCFRDR is equal to or more than the specified trigger number shown below: 000: 15 001: 1 010: 4 011: 6 100: 8 101: 10 110: 12 111: 14
7, 6	RTRG[1:0]	00	R/W	Receive FIFO Data Count Trigger These bits specify the number of receive data bytes that makes the RDF (receive data full) flag to be set in SCFSR. The RDF flag is set when the number of receive data bytes in SCFRDR is equal to or more than the specified trigger number shown below:

RTRG[1:0]	Asynchronous Mode	Clock Synchronous Mode
00	1	1
01	4	2
10	8	8
11	14	14

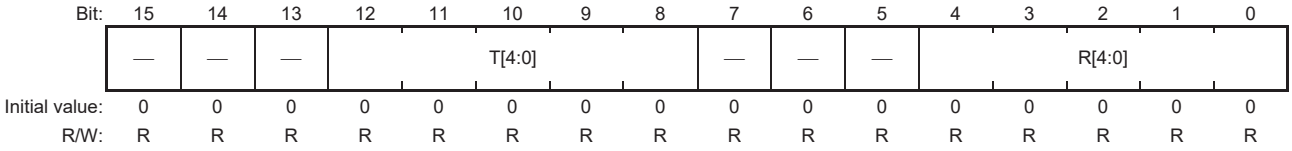
Bit	Bit Name	Initial Value	R/W	Description
5, 4	TTRG[1:0]	00	R/W	Transmit FIFO Data Count Trigger These bits specify the number of remaining transmit data bytes that makes the transmit FIFO data register empty (TDFE) flag to be set in SCFSR. The TDFE flag is set when the number of transmit data bytes in SCFTDR is equal to or less than the specified trigger count shown below, after transmission: 00: 8 (8) 01: 4 (12) 10: 2 (14) 11: 0 (16) Note: Values in parentheses indicate the empty space in SCFTDR in bytes.
3	MCE	0	R/W	Modem Control Enable Enables or disables modem control signals CTS# and RTS#. This bit should always be set to 0 in clock synchronous mode. Whether modem control can be selected or not depends on the interface. 0: Disables modem signals.* 1: Enables modem signals. Note: CTS# and RTS# control ports.
2	TFRST	0	R/W	Transmit FIFO Data Register Reset Enables or disables a transmit FIFO data register reset that empties the register. 0: Disables the reset.* 1: Enables the reset. Note: The register is reset by a power-on reset.
1	RFRST	0	R/W	Receive FIFO Data Register Reset Enables or disables a receive FIFO data register reset that empties the register. 0: Disables the reset.* 1: Enables the reset. Note: The register is reset by a power-on reset.
0	LOOP	0	R/W	Loopback Test Enables or disables the loopback test by internally connecting the transmit output pin (TX) and receive input pin (RX), and the RTS# pin and CTS# pin. If the loopback test is specified, the signal on the RTS# pin is internally conveyed to CTS# pin, and data transmission is automatically suspended when RTS# is asserted. 0: Disables the loopback test. 1: Enables the loopback test. Even if loopback test is specified by this bit, SCSPTR.RTSDT and SCSPTR.CTSDT bits does not reflect signal on loopback path, because those registers shows signals on RTS#/CTS# pins.

35.2.10 FIFO Data Count Register (SCFDR)

SCFDR is a 16-bit register that indicates the number of data bytes stored in SCFTDR and that in SCFRDR.

The upper 8 bits indicate the number of transmit data bytes in SCFTDR, and the lower 8 bits indicates the number of receive data bytes in SCFRDR.

SCFDR can always be read by the CPU.



Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12 to 8	T[4:0]	H'00	R	These bits show the number of data bytes untransmitted and still stored in SCFTDR. H'00 indicates that there is no transmit data in SCFTDR. H'10 indicates that SCFTDR is full of transmit data.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	R[4:0]	H'00	R	These bits show the number of receive data stored in SCFRDR in bytes. H'00 indicates that there is no receive data in SCFRDR. H'10 indicates that SCFRDR is full of receive data.

35.2.11 Serial Port Register (SCSPTR)

SCSPTR controls multiplexed input/output and data on the serial communication interface (SCIF) ports. Bits 1 and 0 control breaks in serial transmission/reception by reading input data from the RX pin and writing output data to the TX pin. Bits 3 and 2 read input data from and write output data to the SCK pin. Bits 5 and 4 read input data from and write output data to the CTS# pin. Bits 7 and 6 read input data from and write output data to the RTS# pin.

SCSPTR is a 16-bit register that can always be read from and written to by the CPU.

All SCSPTR bits except bits 6, 4, 2, and 0 are initialized to 0 by a power-on reset. The values of bits 6, 4, 2, and 0 are undefined.

Note: Whether modem control can be selected or not depends on the interface.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RTSIO	RTSDT	CTSIO	CTSDT	SCKIO	SCKDT	SPB2IO	SPB2DT
Initial value:	0	0	0	0	0	0	0	0	0	—	0	—	0	—	0	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	RTSIO	0	R/W	Serial Port RTS# Pin Input/Output Specifies input or output for the serial port RTS# pin. To actually set the RTS# pin as a port output pin to output the value set by the RTSDT bit, the MCE bit in SCFCR should be cleared to 0. 0: Indicates that this bit does not output the value of the RTSDT bit to the RTS# pin. 1: Indicates that this bit outputs the value of the RTSDT bit to the RTS# pin.
6	RTSDT	—	R/W	Serial Port RTS# Pin Data Specifies the input/output data level of the serial port RTS# pin. Whether the pin is set for input or output is determined by the RTSIO bit. When the pin is set for output, the value of the RTSDT bit is output to the RTS# pin. Regardless of the value of the RTSIO bit, the value of the RTS# pin is read from the RTSDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
5	CTSIO	0	R/W	Serial Port CTS# Pin Input/Output Specifies input or output for the serial port CTS# pin. To actually set the CTS# pin as a port output pin to output the value set by the CTSDT bit, the MCE bit in SCFCR should be cleared to 0. 0: Indicates that the CTSDT bit value is not output to the CTS# pin. 1: Indicates that the CTSDT bit value is output to the CTS# pin.

Bit	Bit Name	Initial Value	R/W	Description
4	CTSDT	—	R/W	Serial Port CTS# Pin Data Specifies the input/output data level of the serial port CTS# pin. Whether the pin is set for input or output is determined by the CTSIO bit. When the pin is set for output, the value of the CTSDT bit is output to the CTS# pin. Regardless of the value of the CTSIO bit, the value of the CTS# pin is read from the CTSDT bit. The initial value of this bit is undefined after a power-on. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
3	SCKIO	0	R/W	Serial Port Clock Pin Input/Output Specifies input or output for the serial port SCK pin. To actually set the SCK pin as a port output pin to output the value set by the SCKDT bit, the CKE[1:0] bits in SCSCR should be cleared to 0. 0: Indicates that the SCKDT bit value is not output to the SCK pin. 1: Indicates that the SCKDT bit value is output to the SCK pin.
2	SCKDT	—	R/W	Serial Port Clock Pin Data Specifies the input/output data level of the serial port SCK pin. Whether the pin is set for input or output is determined by the SCKIO bit. When the pin is set for output, the value of the SCKDT bit is output to the SCK pin. Regardless of the value of the SCKIO bit, the value of the SCK pin is read from the SCKDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
1	SPB2IO	0	R/W	Serial Port Break Input/Output Specifies the output condition of the serial port TX pin. To actually set the TX pin as a port output pin to output the value set by the SPB2DT bit, the TE bit in SCSCR should be cleared to 0. 0: Indicates that the SPB2DT bit value is not output to the TX pin. 1: Indicates that the SPB2DT bit value is output to the TX pin.
0	SPB2DT	—	R/W	Serial Port Break Data Specifies the input level of the serial port RX pin and the output level of the TX pin. The TX pin output conditions are determined by the SPB2IO bit. When the TX pin is set for output, the value of the SPB2DT bit is output to the TX pin. Regardless of the value of the SPB2IO bit, the value of the RX pin is read from the SPB2DT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.

Figures 35.2 to 35.6 show the block diagrams of the SCIF I/O ports.

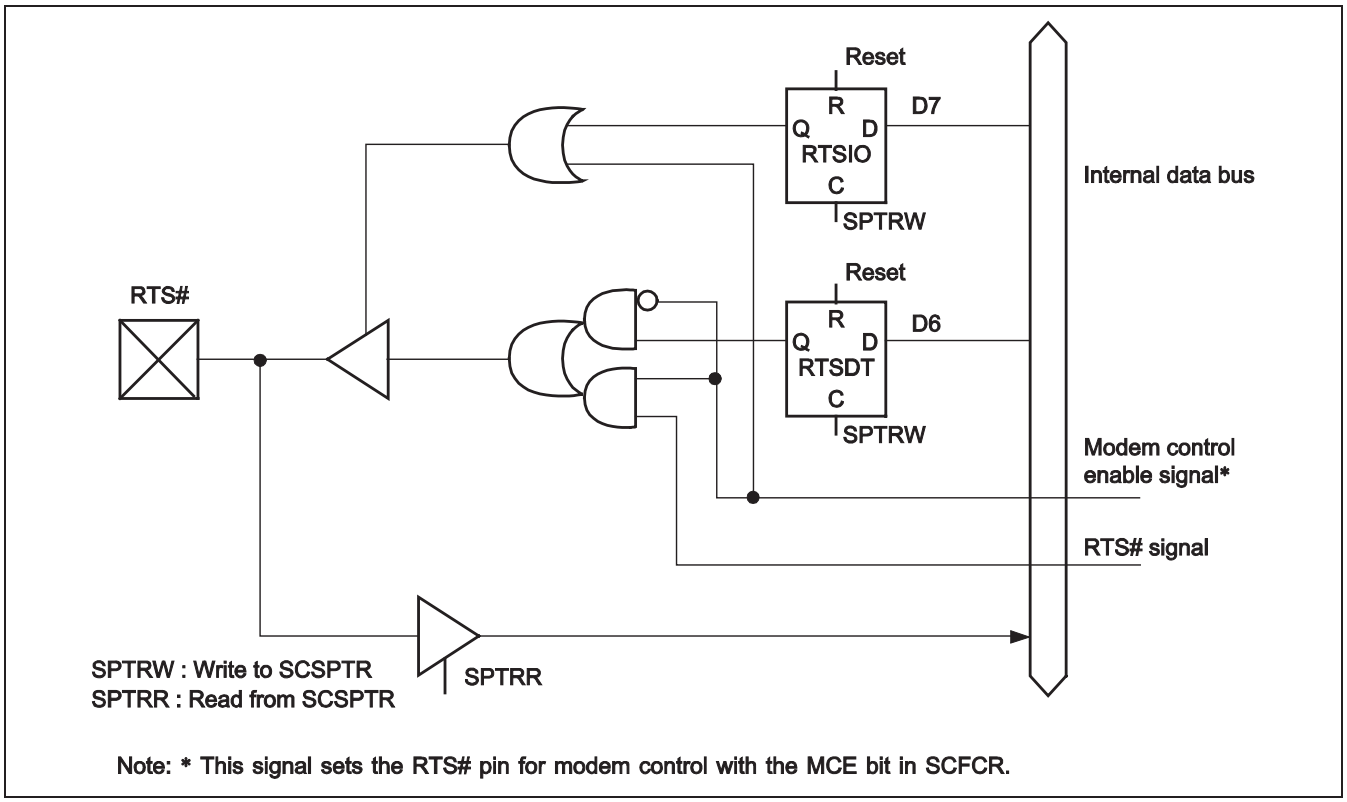


Figure 35.2 RTS# Pin

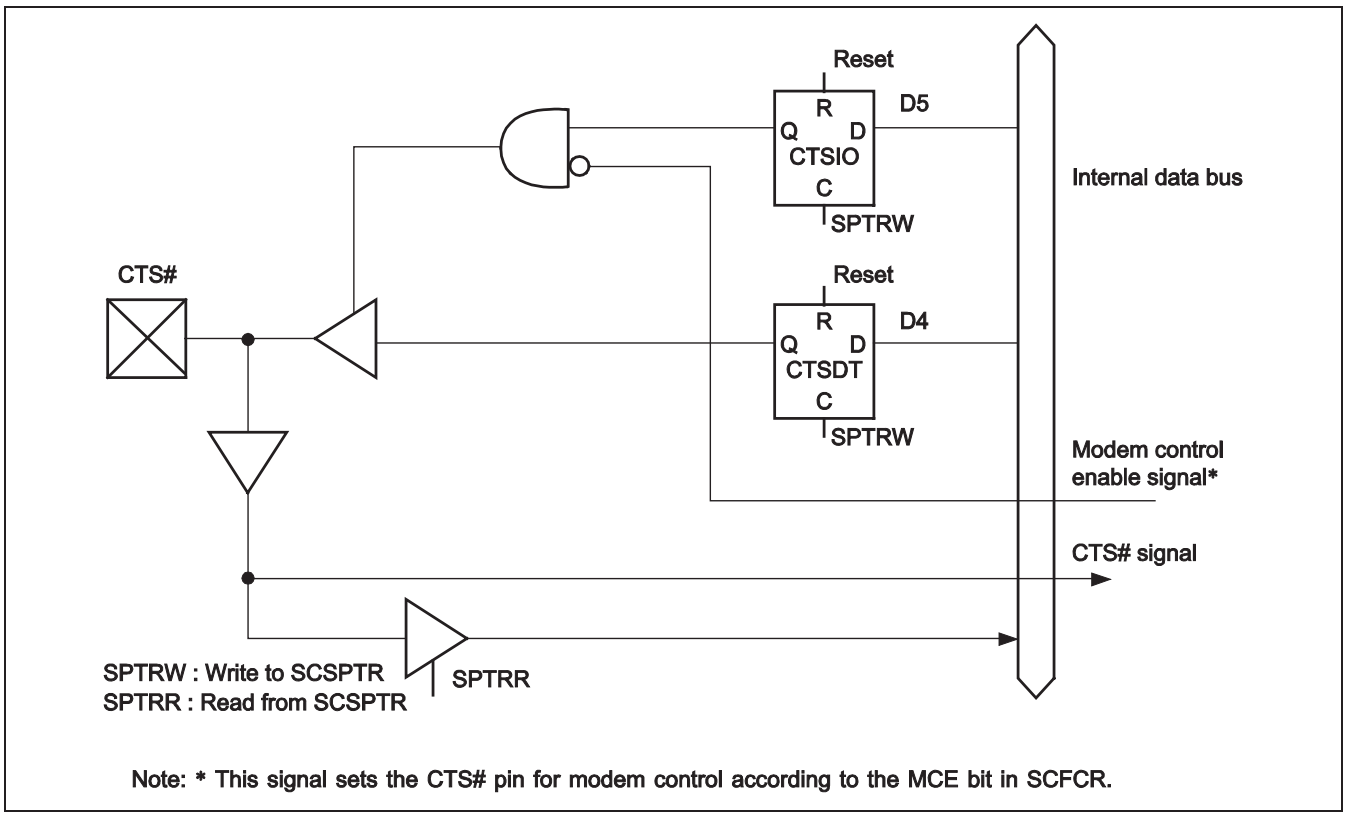


Figure 35.3 CTS# Pin

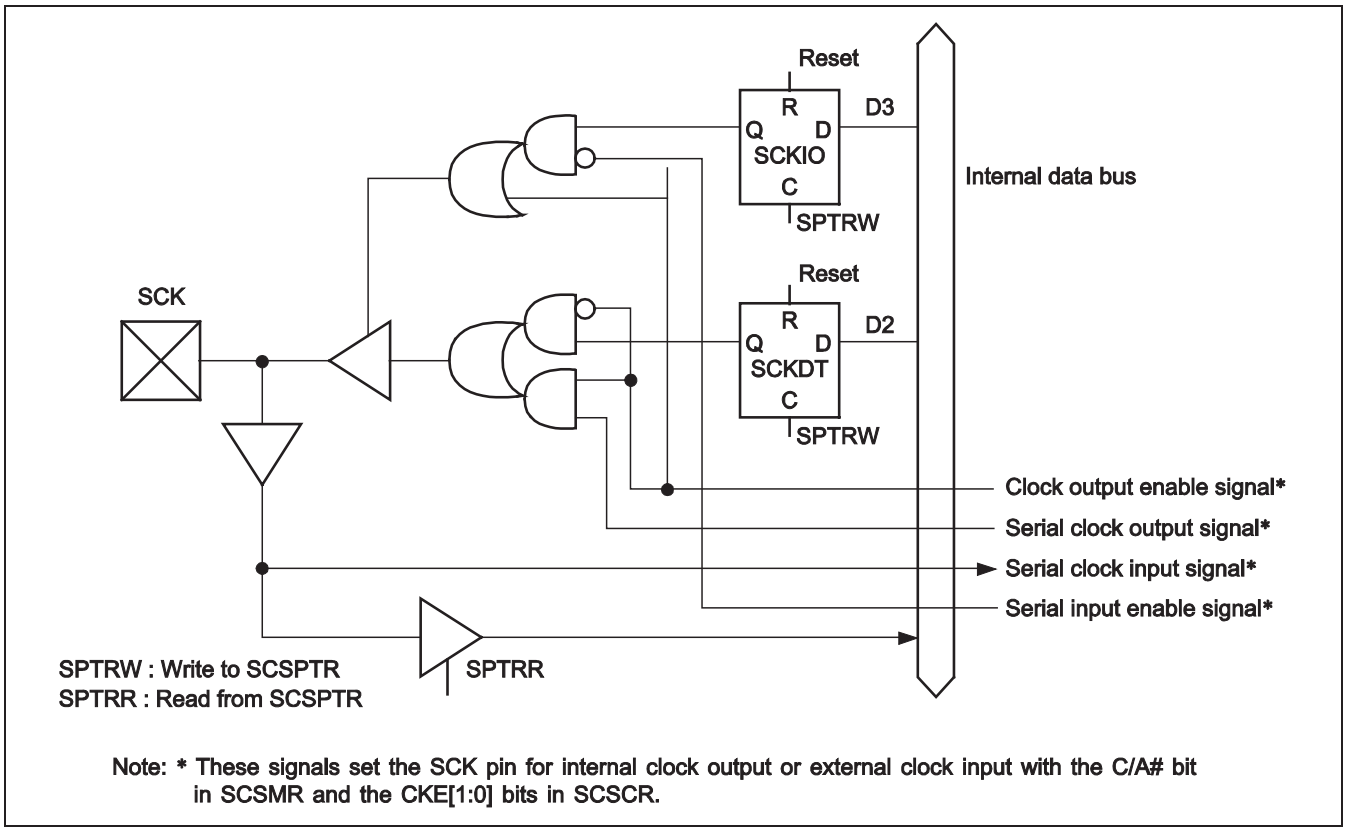


Figure 35.4 SCK Pin

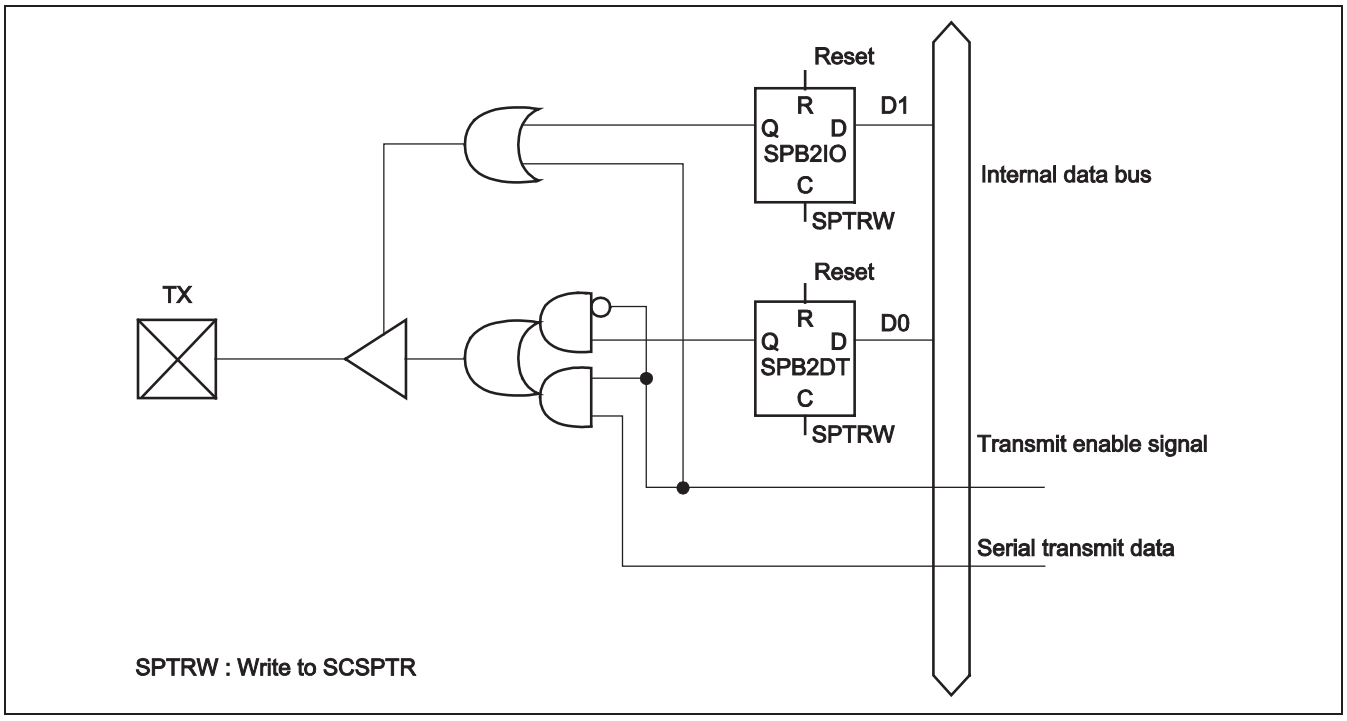


Figure 35.5 TX Pin

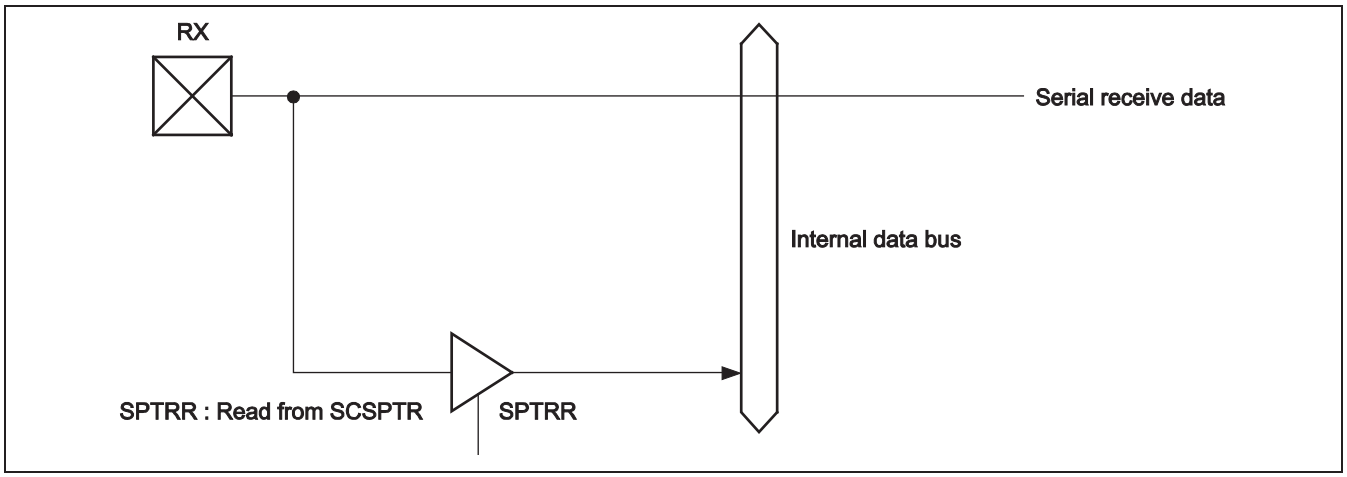


Figure 35.6 RX Pin

35.2.12 Line Status Register (SCLSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TO	—	ORER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R/(W)*

Note: Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TO	0	R/(W)*	Timeout Indicates that the number of data bytes in SCFRDR is less than the receive trigger count, and that no further data has been received for at least 15 etu after the stop bit of the last receive data in asynchronous mode. This bit is not set in clock synchronous mode. 0: Indicates that data is being received or has been successfully received and that there is no receive data in SCFRDR. [Clearing conditions] • A power-on reset is executed. • All the receive data in the SCFRDR has been read, and 0 is written to TO. 1: Indicates that no further receive data has been received (receive timeout). [Setting condition] • The number of data bytes in SCFRDR is less than the receive trigger count and no further data has been received for at least 15 etu after the stop bit of the last receive data.* Note: etu: Elementary Time Unit (time for transfer of 1 bit) Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	ORER	0	R/(W)*	Overrun Error Indicates that an overrun error has occurred in reception and abnormal termination is caused. If an overrun error occurs, the receive data prior to the overrun error is retained in SCFRDR and the data received subsequently is discarded. Any subsequent serial reception is disabled while the ORER flag is 1. To resume data reception after clearing the ORER flag, be sure to first read (or clear) data in the receive FIFO and handle the error, then clear the ORER flag. 0: Indicates that data is being received or has been successfully received. [Clearing conditions] • A power-on reset is executed. • 0 is written to ORER. 1: Indicates that an overrun error has occurred in reception. [Setting condition] • The next serial reception has been completed while SCFRDR is full of 16-byte data. Note: When bit RE in SCSCR is cleared to 0, the ORER flag is not affected and its previous state is retained.

Note: Writing 0 is only available to clear the flag.

35.3 Operation

35.3.1 Operation in Asynchronous Mode

In asynchronous mode, the SCIF performs serial communication, in which data is transmitted/received in character units using the attached start bit indicating the start of communication and stop bit indicating the end of communication.

Figure 35.7 shows the general format for asynchronous serial communication.

In asynchronous serial communication, the transmission line is usually kept marked (high level). The SCIF monitors the transmission line, and when it finds a space (low level), it regards the space as a start bit and starts serial communication.

One character in serial communication consists of a start bit (low level), followed by transmit/receive data (LSB-first; from the lowest bit), a parity bit (high or low level), and a stop bit (high level).

During reception in asynchronous mode, the SCIF performs synchronization at the falling edge of the start bit. Communication data is acquired at the center of each bit because the SCIF samples data at the eighth pulse of the clock which has a frequency of 16 times the bit rate.

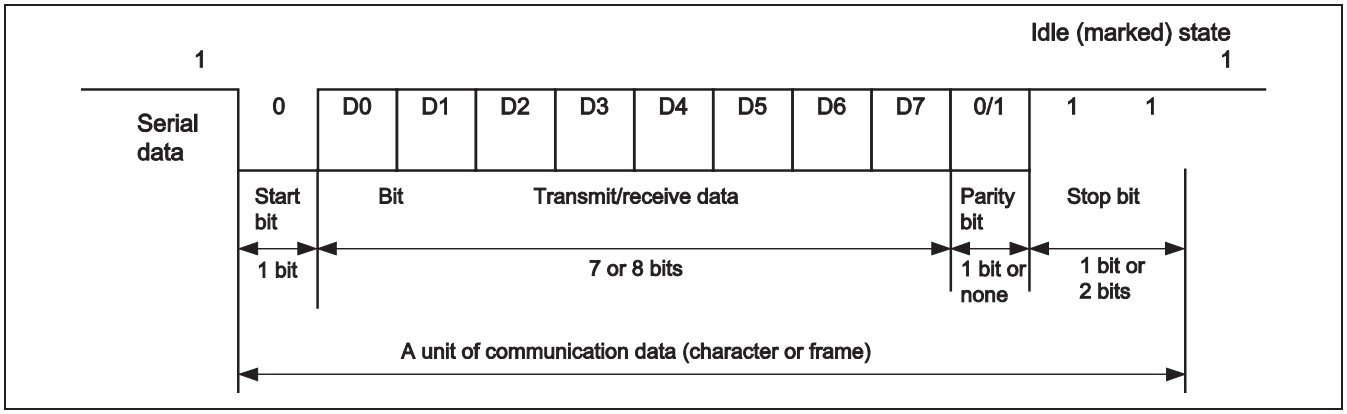


Figure 35.7 Data Format in Asynchronous Mode (Example of 8-Bit Data with Parity and Two Stop Bits)

(1) Transmission/Reception Format

Table 35.6 shows available data transfer formats. The SCIF supports 8 transfer formats, which can be specified by SCSMR.

Table 35.6 Serial Transmission/Reception Formats (Asynchronous Mode)

SCSMR Settings			Serial Transmission/Reception Format and Frame Length											
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	S	8-bit data								STOP		
		1	S	8-bit data								STOP	STOP	
	1	0	S	8-bit data								P	STOP	
		1	S	8-bit data								P	STOP	STOP
1	0	0	S	7-bit data							STOP			
		1	S	7-bit data							STOP	STOP		
	1	0	S	7-bit data							P	STOP		
		1	S	7-bit data							P	STOP	STOP	

[Legend]
S: Start bit
STOP: Stop bit
P: Parity bit

(2) Clock

The transfer clock can be selected from the following two clocks using the CKE[1:0] bits in SCSCR:

- Internal clock generated by the on-chip baud rate generator
- External clock generated by an external clock baud rate generator

(3) Data Transmission/Reception

(a) Initialization of SCIF (Asynchronous Mode)

Before transmitting/receiving data or changing the operating mode or communication format, the SCIF should be initialized using the sample flowchart for SCIF initialization shown in Figure 35.8.

[Notes]

Clearing the TE bit to 0 initializes SCTSR. However, SCFSR, SCFTDR, and SCFRDR contents are retained even if the TE and RE bits are cleared to 0.

The TE bit should be cleared to 0 after all transmit data has been sent and the TEND flag has been set in SCFSR. The TE bit can be cleared to 0 during transmission, but the data being transmitted will enter the marked state after clearing. In addition, before setting the TE bit to 1 to restart the transmission, set the TFRST bit to 1 in SCFCR to reset SCFTDR.

When an external clock is used, do not stop the clock during operation or initialization. If stopped, the operation will be unreliable. Furthermore, when the baud rate generator for external clock is also to be used, be sure to make settings for it before starting initialization of the SCIF.

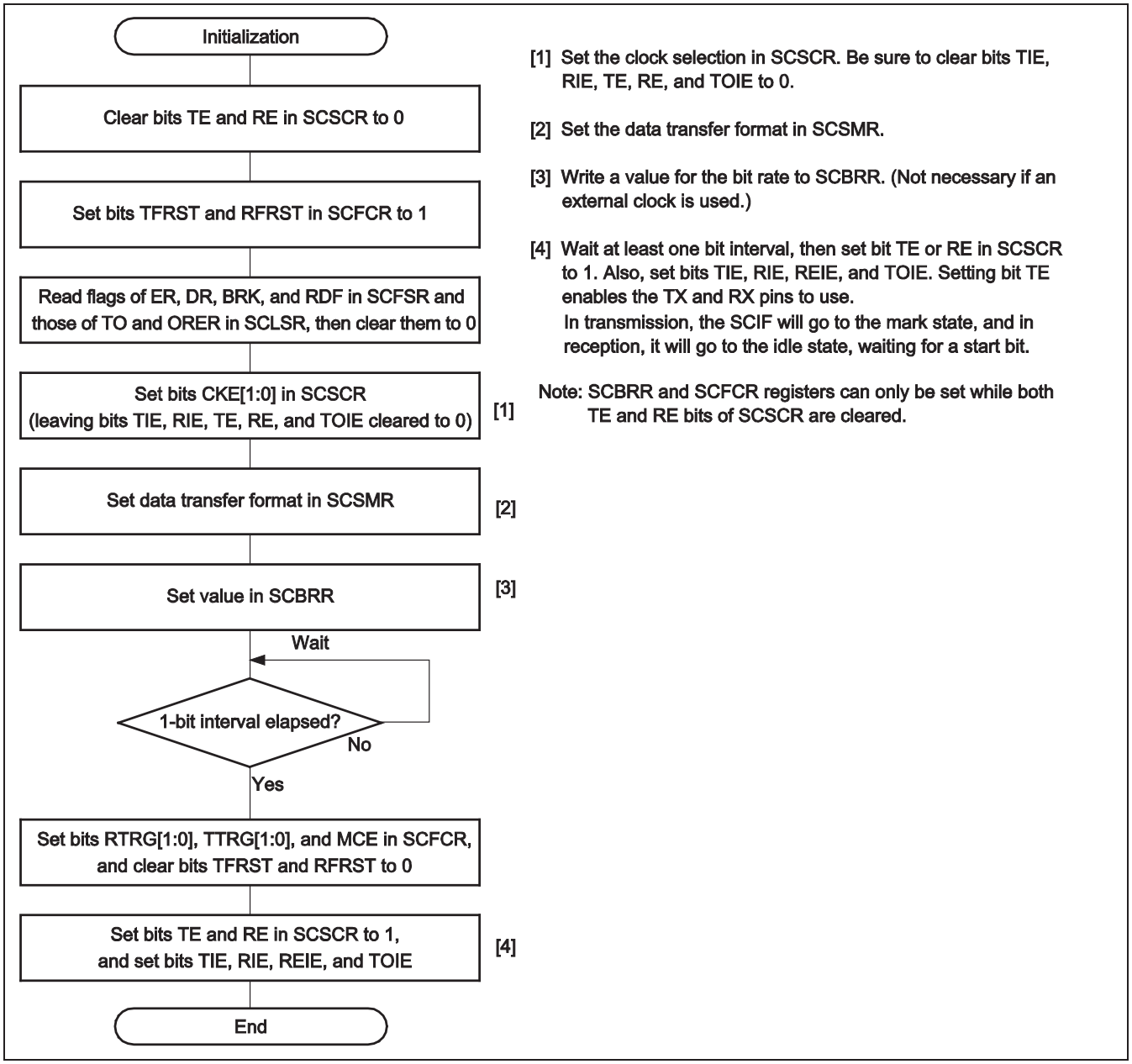


Figure 35.8 Sample Flowchart for Initializing the SCIF

(a) Serial Data Transmission (Asynchronous Mode)

Figure 35.9 shows a sample flowchart for serial transmission.

After the SCIF transmission operation is enabled, serial data transmission can be performed using the following procedure:

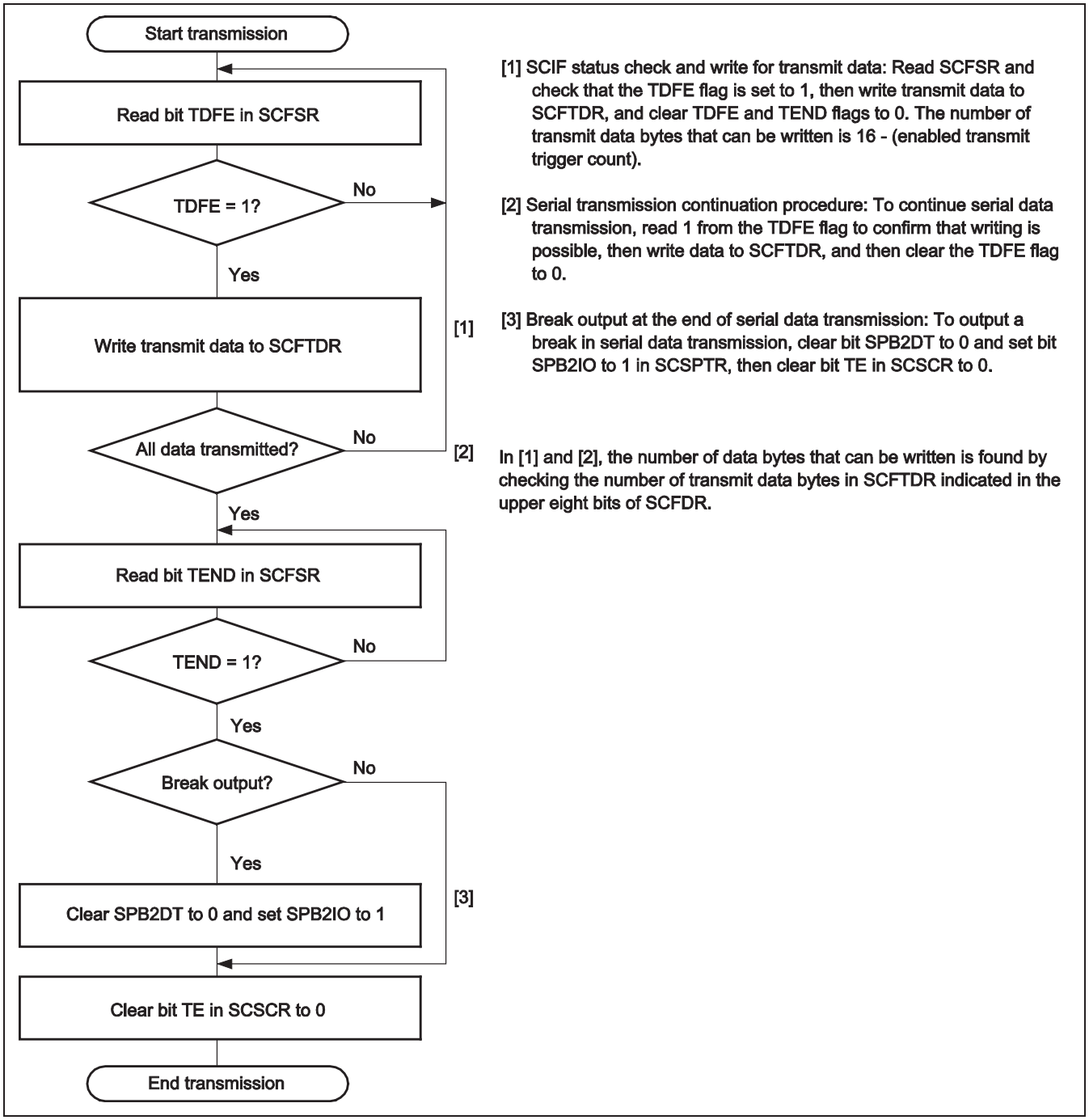


Figure 35.9 Sample Flowchart for Serial Transmission

In serial transmission, the SCIF operates as follows:

1. When data is written to SCFTDR, the SCIF transfers the data from SCFTDR to SCTSR and starts transmitting. Confirm that the TDFE flag in SCFSR is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is at least (16- (transmit trigger count)).
2. When data is transferred from SCFTDR to SCTSR and the SCIF starts transmission, consecutive transmission is performed until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR is equal to or less than the transmit trigger count specified in SCFCR, the TDFE flag is set. If the TIE and TEIE bits in SCSCR are set to 1 and 0, respectively at this time, a transmit-FIFO-data-empty interrupt (TDFE) request occurs. The serial transmit data is sent from the TX pin in the following order:
   A. Start bit: One 0-bit is output.
   B. Transmit data: 8- or 7-bit data is output in LSB-first order.
   C. Parity bit: One parity bit (even or odd parity) is output.
      A format that does not output a parity bit can also be selected.
   D. Stop bit(s): One or two 1-bits (stop bits) are output.
   E. Marked state: 1 is output continuously until the start bit that starts the next transmission is sent.
3. The SCIF checks transmit data in SCFTDR when sending the stop bit. If there is data in it, the SCIF transfers the data from SCFTDR to SCTSR, sends the stop bit, and then starts serial transmission of the next frame. If there is no transmit data, the SCIF sets the TEND flag to 1 in SCFSR and sends out the stop bit, and then the marked state is entered to output 1 continuously. At this time, if the TIE and TEIE bits in SCSCR are set to 1, a transmit-end interrupt (TEND) request occurs.

Figure 35.10 shows an example of transmission in asynchronous mode.

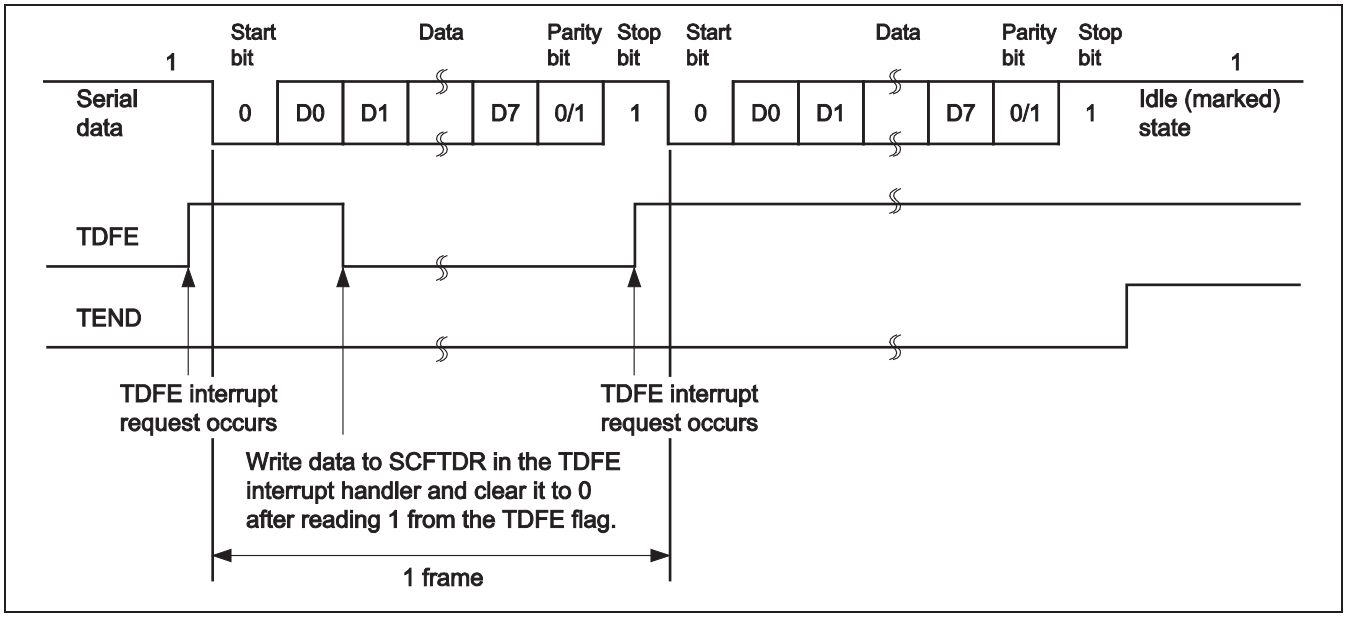


Figure 35.10 Sample SCIF Transmission Operation (Example of 8-Bit Data with Parity and One Stop Bit)

4. When modem control is enabled, transmission can be stopped or resumed in accordance with the CTS# input value. When CTS# is set to 1 during transmission, the marked state is entered after one frame of data transmission is ended. Setting CTS# to 0 restarts outputting the next transmit data from the start bit. Figure 35.11 shows an example of the operation with modem control enabled.

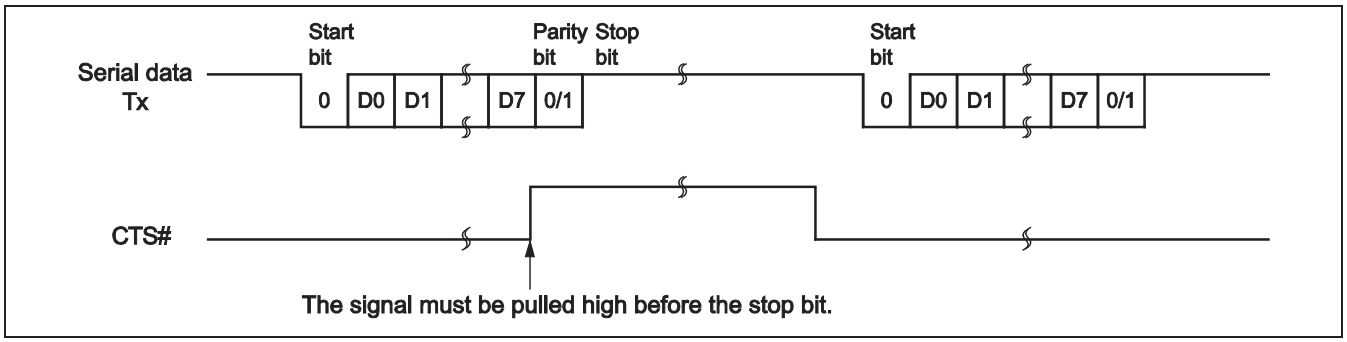


Figure 35.11 Sample Operation with Modem Control Enabled (CTS#)

(b) Serial Data Reception (Asynchronous Mode)

Figures 35.12 and 35.13 show sample flowcharts for serial reception.

After the SCIF reception operation is enabled, serial data reception can be performed using the following procedure:

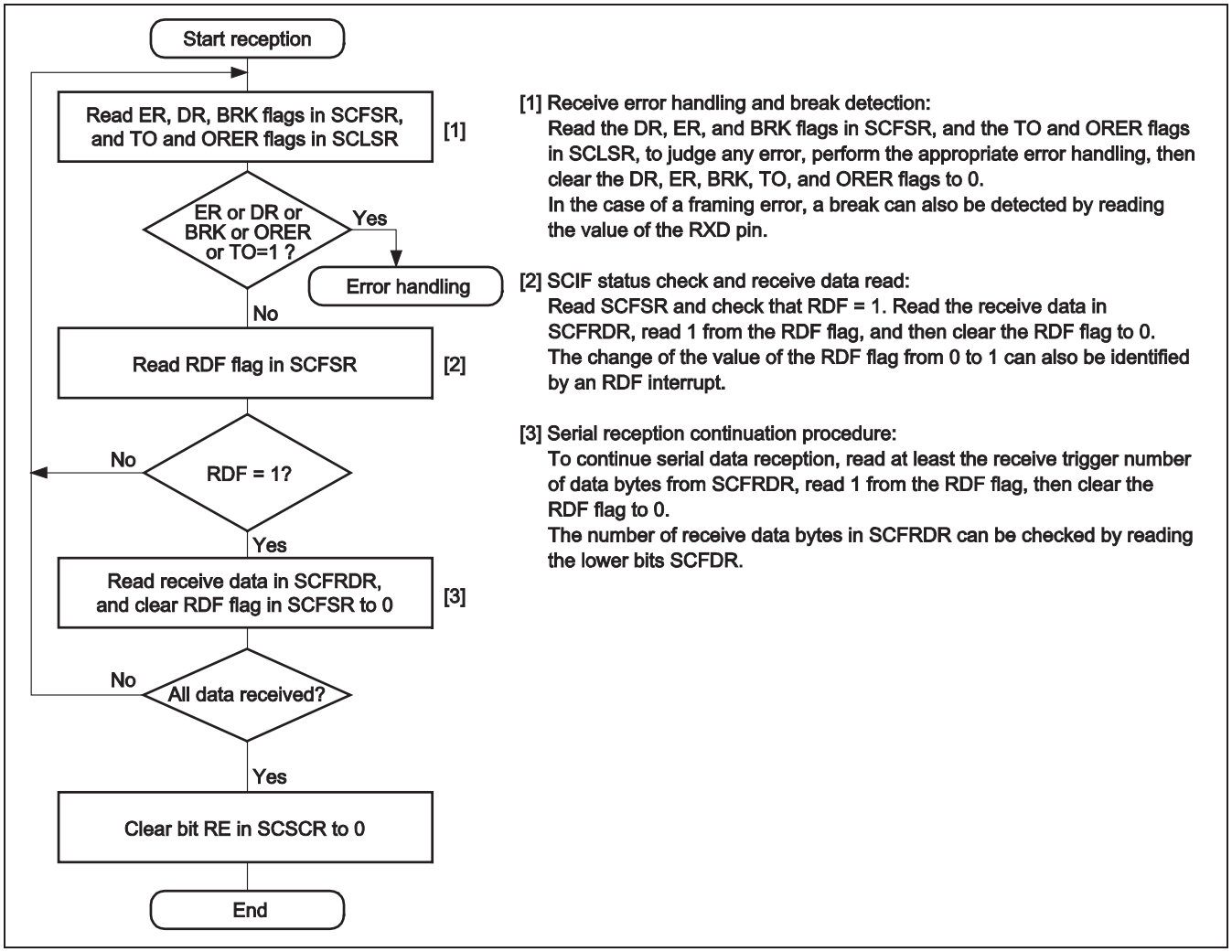
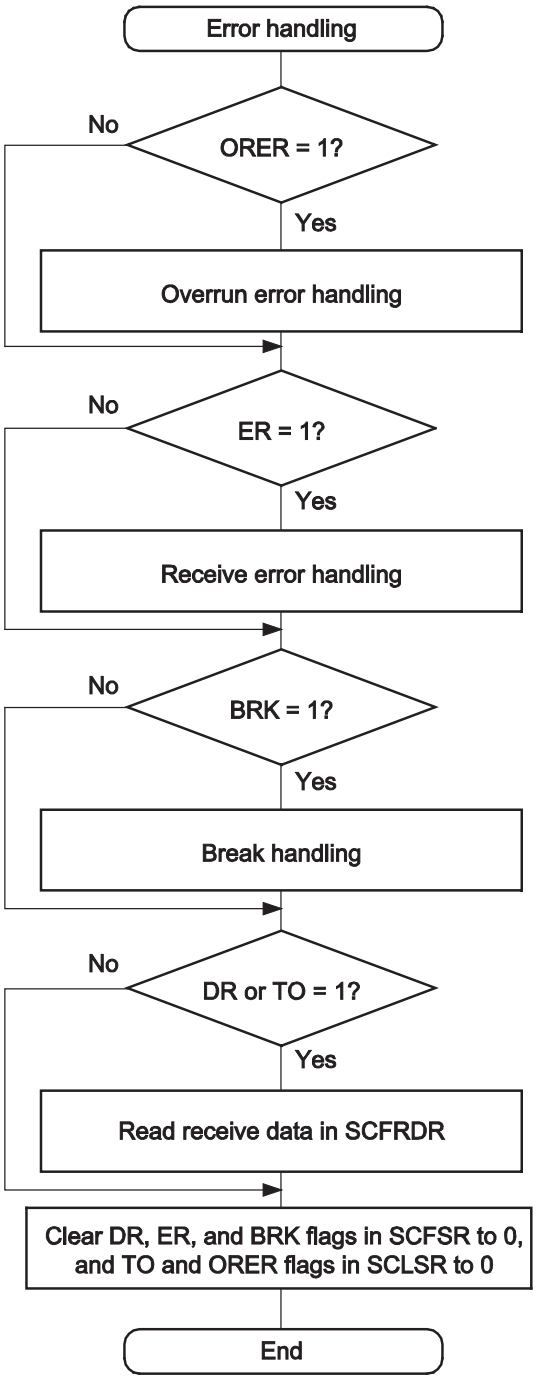


Figure 35.12 Sample Flowchart for Serial Reception (1)



Whether a framing error or parity error has occurred in the receive data that is to be read from SCFRDR can be determined by checking bits FER and PER in SCFSR.

Figure 35.13 Sample Flowchart for Serial Reception (2)

In serial reception, the SCIF operates as follows:

1. The SCIF monitors the transmission line, and when detecting the start bit 0, it performs internal synchronization and starts reception.
2. The SCIF stores the received data in SCRSR in LSB-to-MSB order.
3. The SCIF receives the parity bit and stop bit.
   After receiving these bits, the SCIF performs the following checks:
   A. Stop bit: The SCIF checks whether the stop bit is 1.
      If there are two stop bits, it checks only the first stop bit.
   B. Receive data: The SCIF checks that receive data can be transferred from the receive shift register (SCRSR) to SCFRDR.
   C. Overrun error: The SCIF checks that the ORER flag is 0, indicating that no overrun error has occurred.
   D. Break state: The SCIF checks that the BRK flag is 0, indicating that the break state is not set.
   If the SCIF can confirm the conditions of (b), (c), and (d), it stores the receive data in SCFRDR.

   Note: The SCIF continues to receive data even when a parity error or a framing error occurs.

4. If the RDF flag changes to 1 while the RIE bit in SCSCR is 1, a receive-FIFO-data-full interrupt (RDF) request occurs.
   If the DR flag changes to 1 while the RIE bit in SCSCR is 1, a receive-data-ready interrupt (DR) request occurs.
   If the TO flag changes to 1 while the TOIE bit in SCSCR is 1, a timeout interrupt (TO) request occurs.
   If the ER flag changes to 1 while the RIE or REIE bit in SCSCR is 1, a receive-error interrupt (ER) request occurs.
   If the BRK flag changes to 1 while the RIE or REIE bit in SCSCR is 1, a break interrupt (BRK) request occurs.
   If the ORER flag changes to 1 while the RIE or REIE bit in SCSCR is 1, an overrun-error interrupt (ORER) request occurs.

Figure 35.14 shows an example of reception in asynchronous mode.

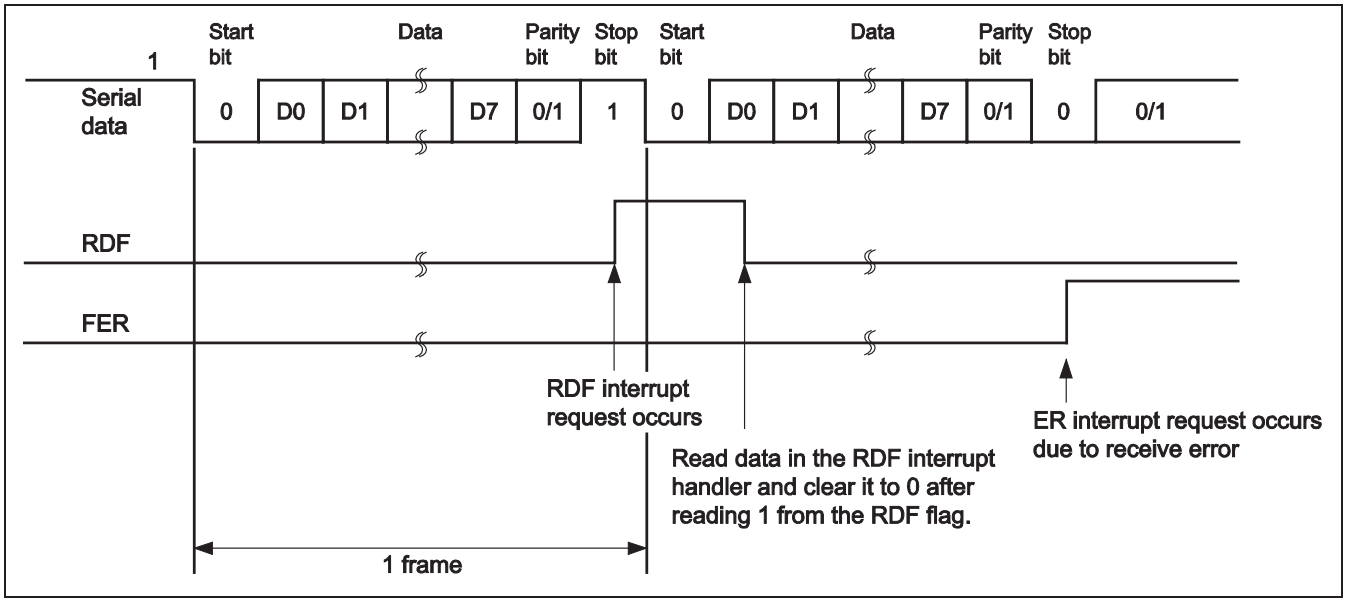


Figure 35.14 Sample SCIF Receive Operation (Example of 8-Bit Data with Parity and One Stop Bit)

5. When modem control is enabled, the RTS# signal is output when SCFRDR is empty. When RTS# is 0, data can be received. When RTS# is set to 1, the number of data bytes in SCFRDR is equal to or more than the RTS# output active trigger count.

Figure 35.15 shows an example of the operation with modem control enabled.

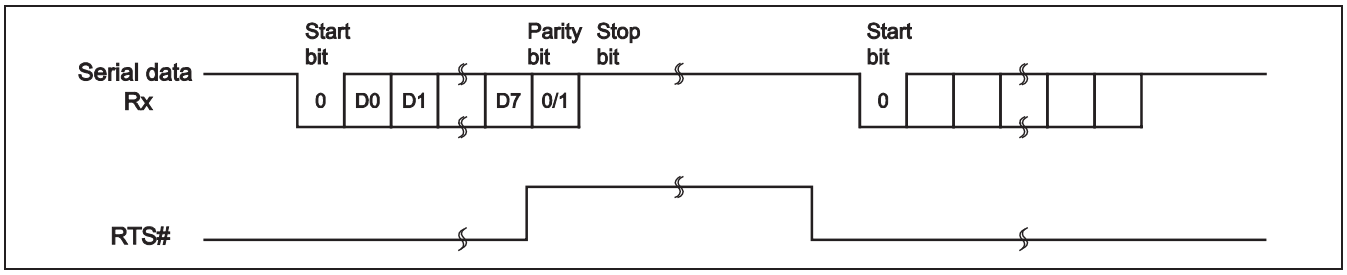


Figure 35.15 Example of the Operation with Modem Control Enabled (RTS#)

35.3.2 Operation in Clock Synchronous Mode

Clock synchronous mode, in which data is transmitted and received in synchronization with clock pulses, is suitable for fast serial communication.

Figure 35.16 shows the general format for clock synchronous serial communication. In the clock synchronous serial communication, data on the communication line is output between one falling edge of the synchronization clock and the next falling edge. The data decision is done at the rising edge of the clock.

In serial communication, each character is output starting with the LSB and ending with the MSB. After the MSB is output, the communication line retains the state of the last data.

In clock synchronous mode, the SCIF receives data in synchronization with a rising edge of the synchronization clock.

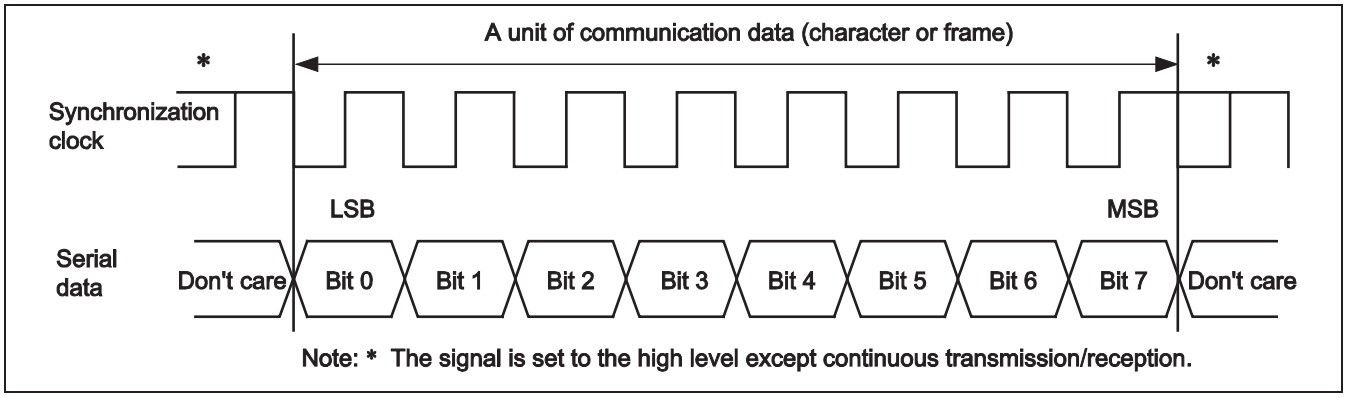


Figure 35.16 Data Format for Clock Synchronous Communication

(1) Data Transfer Format

The data transfer format is fixed to 8 bits. No parity bit can be added.

(2) Clock

The clock can be selected from the following two clocks using the C/A# bit in SCSMR and the CKE[1:0] bits in SCSCR:

- Internal clock generated by the on-chip baud rate generator
- External synchronization clock input at the SCK pin

When the SCIF is operated on an internal clock, the synchronization clock is output from the SCK pin. Eight synchronization clock pulses are output in one-character transfer, and when no transfer is performed the clock is fixed high. When only reception operation is performed, selecting an internal clock outputs clock pulses until the number of data bytes in the receive FIFO reaches the specified receive trigger count, while the RE bit in SCSCR is 1.

(3) Data Transmission/Reception

(a) Initialization of SCIF (Synchronous Mode)

Before transmitting/receiving data or changing the operating mode or communication format, the TE and RE bits in SCSCR to 0 and then the SCIF should be initialized using the sample flowchart for SCIF initialization shown in Figure 35.17.

[Note]

Clearing the TE bit to 0 initializes SCTSR. However, clearing the RE bit to 0 does not affect the RDF, PER, FER, and ORER flags and SCFRDR contents.

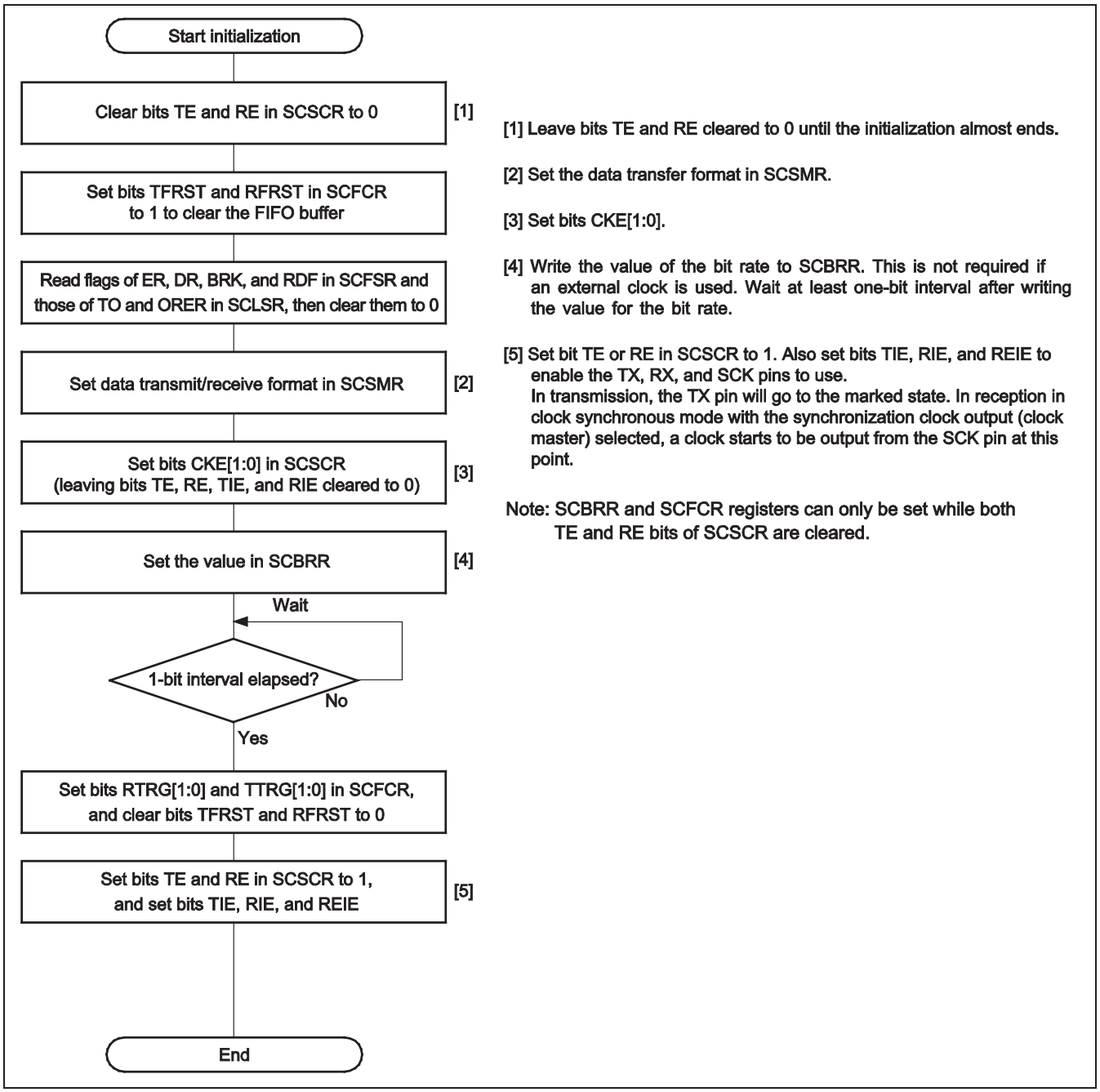


Figure 35.17 Sample Flowchart for SCIF Initialization

(b) Serial Data Transmission (Clock Synchronous mode)

Figure 35.18 shows a sample flowchart for serial transmission.

After the SCIF transmission operation is enabled, serial data transmission can be performed using the following procedure:

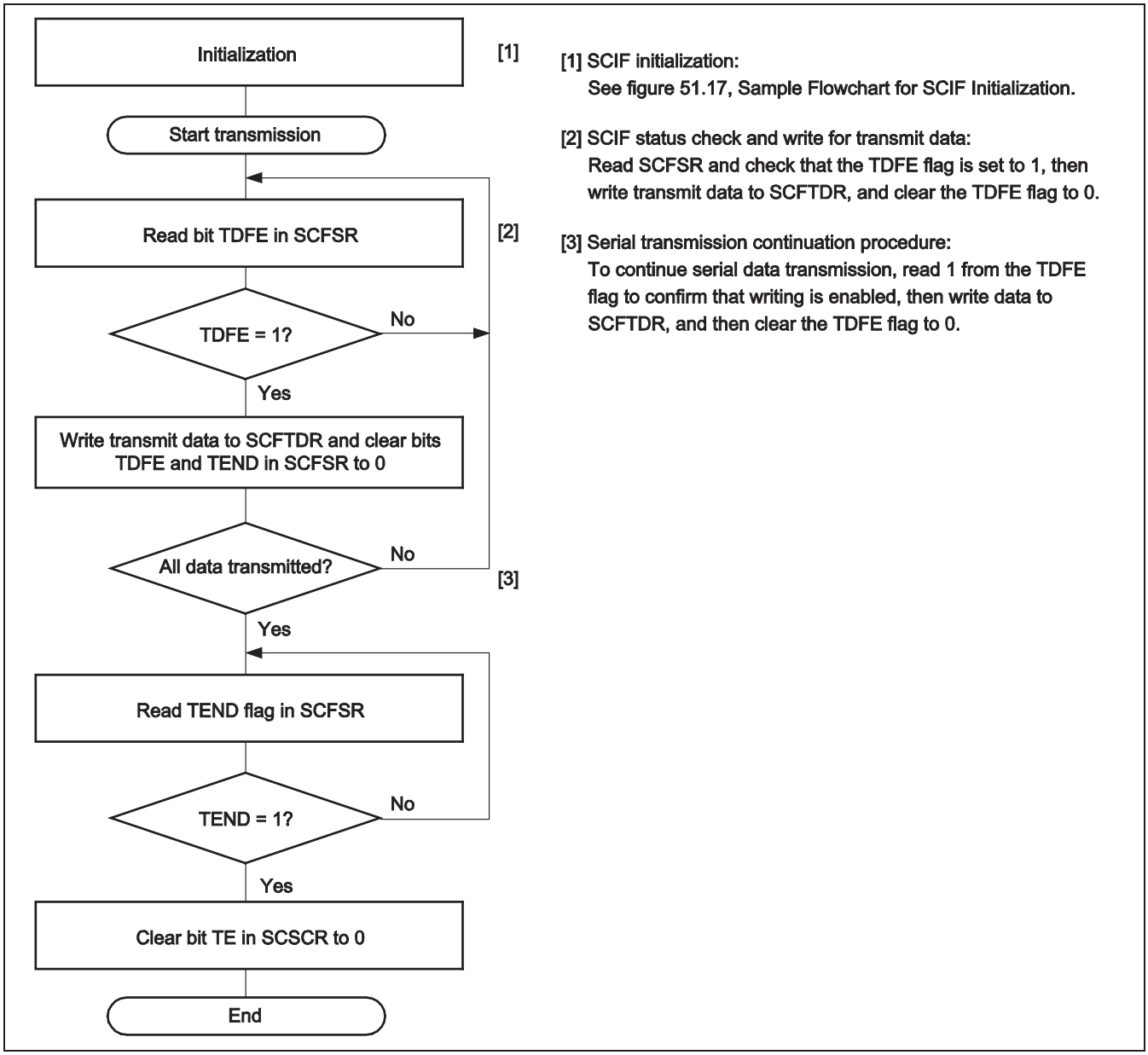


Figure 35.18 Sample Flowchart for Serial Transmission

In serial data transmission, the SCIF operates as described below:

1. When data is written to SCFTDR, the SCIF transfers the data from SCFTDR to SCTSR to start transmission. Confirm that the TDFE flag in SCFSR is set to 1 before writing transmit data to SCFTDR. The number of data bytes that can be written is at least (16- (the transmit trigger count)).
2. After the SCIF transfers data from SCFTDR to SCTSR and starts data serial transmission, the SCIF consecutively transmits it until there is no transmit data left in SCFTDR. When the number of transmit data bytes in SCFTDR is equal to or less than the transmit trigger count set in SCFCR, the TDFE flag is set. If the TIE and TEIE bits in SCSCR are set to 1 and 0, respectively at this time, a transmit-FIFO-data-empty interrupt (TDFE) request occurs. When the external clock is selected, data is output in synchronization with the input clock. The serial transmit data is output at the TX pin in the LSB-first order.
3. The SCIF checks transmit data in SCFTDR when sending the last bit. If there is transmit data, the SCIF transfers the data to SCTSR, and starts serial transmission of the next frame. If there is no transmit data left, the TEND flag in SCFSR is set to 1, and the transmit data pin (TX pin) retains its state after the last bit is sent. At this time, if the TIE and TEIE bits in SCSCR are set to 1, a transmit-end interrupt (TEND) request occurs.
4. After serial transmission ends, the SCK pin is fixed high.

Note: In clock synchronous mode, when transmit data is written to SCFTDR by the DMAC, the TEND flag may not be cleared. Therefore, if the DMAC is used for transmission in clock synchronous mode, read the TEND flag in the following method.

1. Confirm that data transfer is completed in the DMAC.
2. Read the TEND flag.
3. Clear the TEND flag to 0 if TEND = 1.
4. Read the TEND flag again.
5. Use the second-read TEND flag.

Figure 35.19 shows an example of SCIF serial transmission in clock synchronous mode.

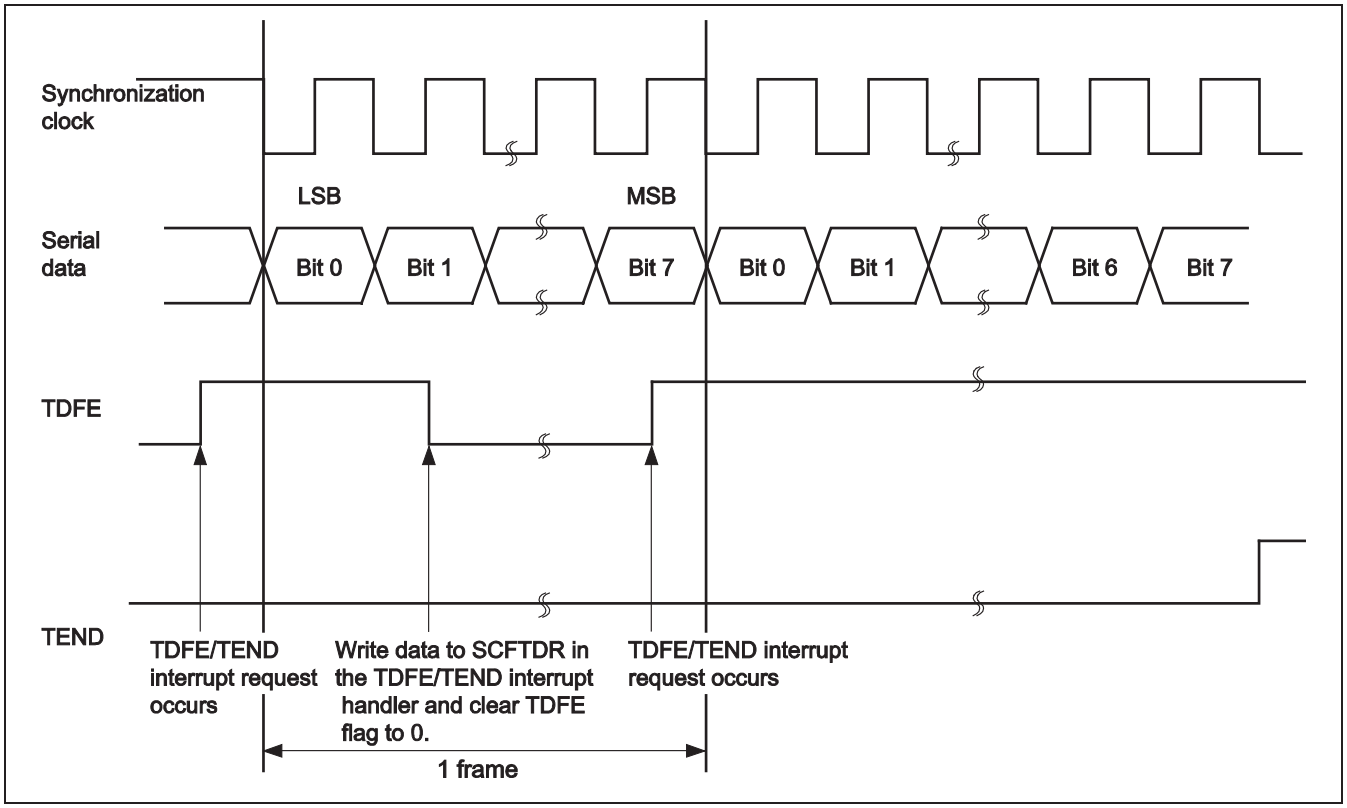


Figure 35.19 Example of SCIF Serial Transmission in Clock Synchronous Mode

(c) Serial Data Reception (Clock Synchronous Mode)

Figures 35.20 and 35.21 show sample flowcharts for serial reception.

The SCIF reception should be enabled before taking the following steps for serial data transmission.

When switching operating mode from asynchronous mode to clock synchronous mode without initializing the SCIF, check that the ORER, PER3 to PER0, and FER3 to FER0 flags are cleared to 0.

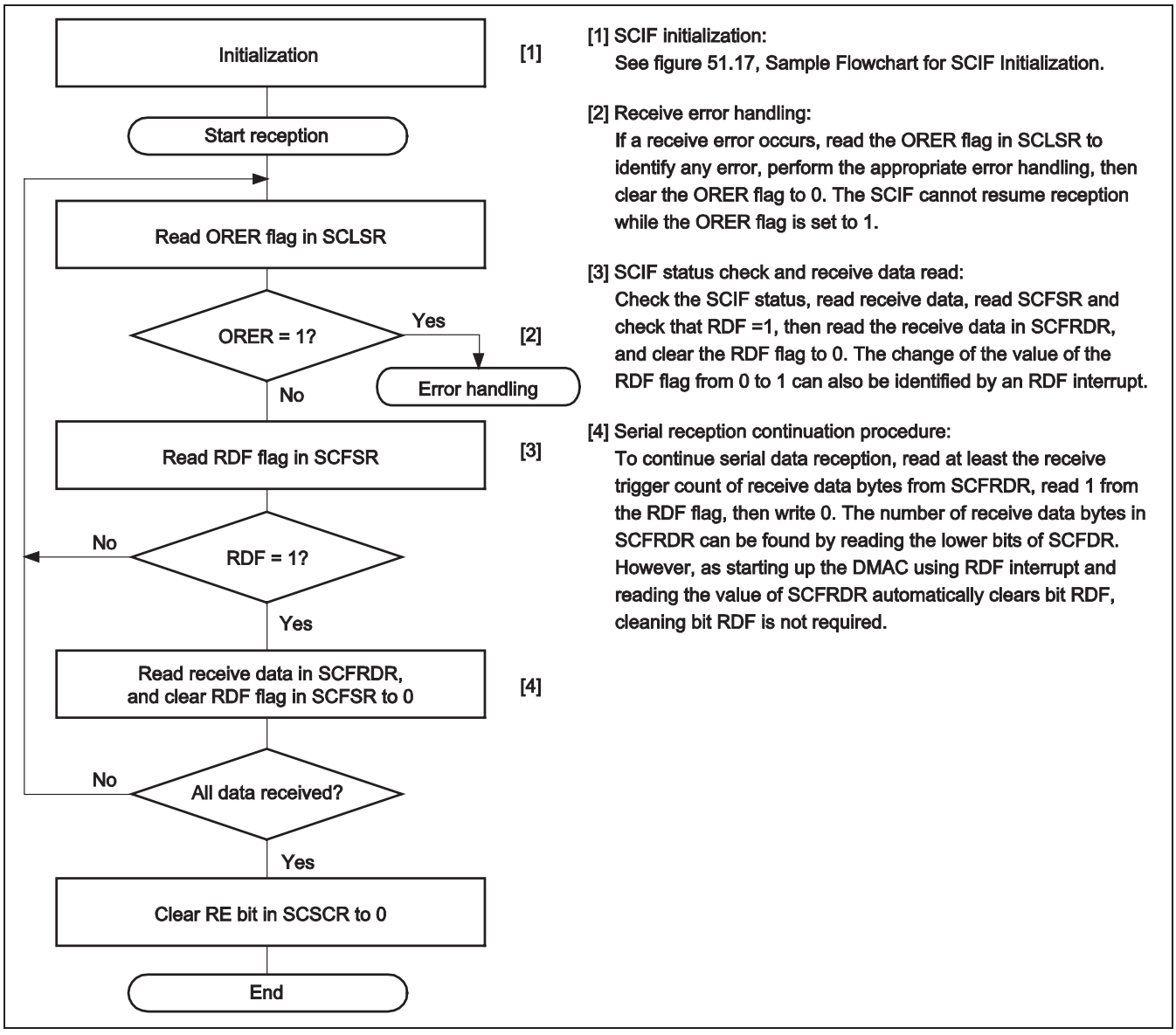


Figure 35.20 Sample Flowchart for Serial Data Reception

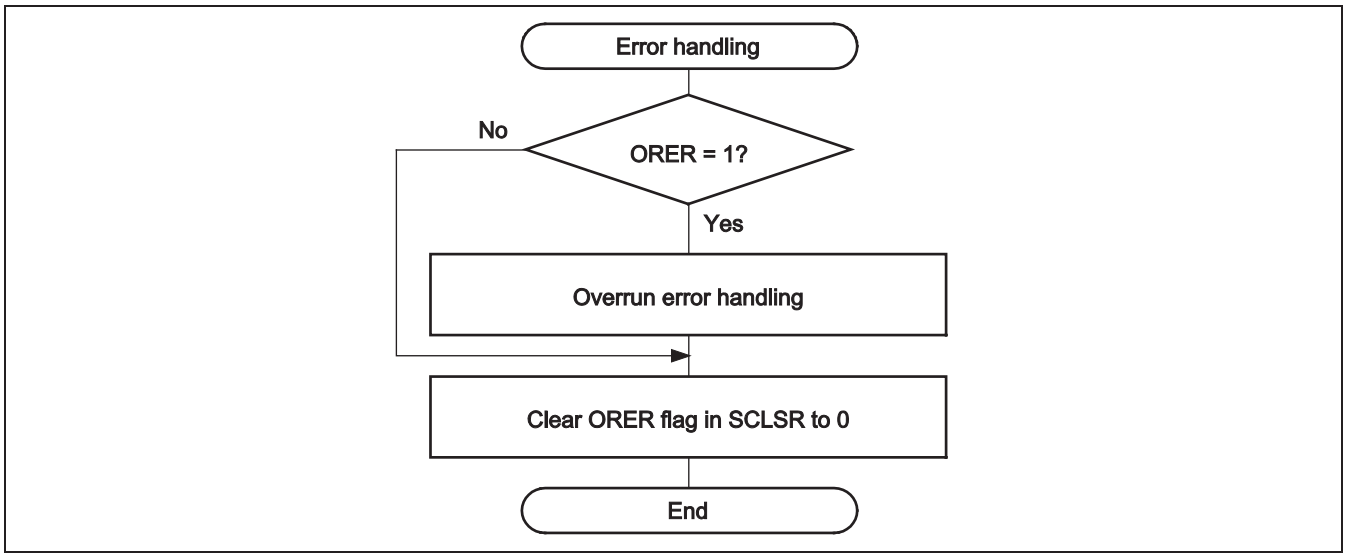


Figure 35.21 Sample Flowchart for Serial Data Reception

In serial data reception, the SCIF operates as described below:

1. The SCIF starts receiving data in synchronization with synchronization clock input or output.
2. The SCIF stores receive data in SCRSR in LSB-to-MSB order.
   After receiving the data, the SCIF first checks if the receive data can be transferred from SCRSR to SCFRDR, then starts storing the receive data in SCFRDR.
   If the SCIF detects an overrun error, the SCIF cannot receive subsequent data.
3. If the RDF flag changes to 1 while the RIE bit in SCSCR is 1, a receive-FIFO-data-full interrupt (RDF) request occurs. If the ORER flag changes to 1 while the RIE or REIE bit in SCSCR is 1, a break interrupt (BRI) request occurs.

Figure 35.22 shows an example of SCIF reception in clock synchronous mode.

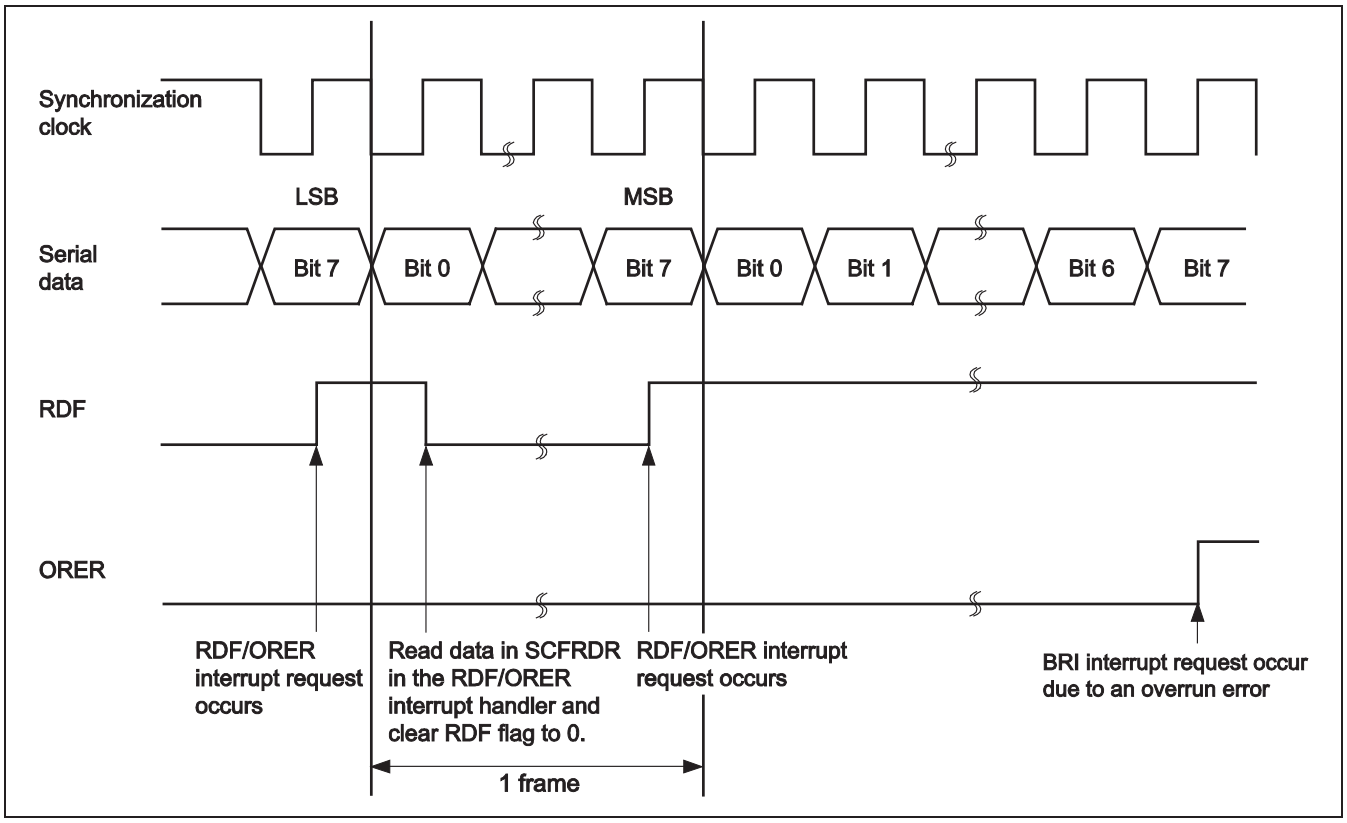
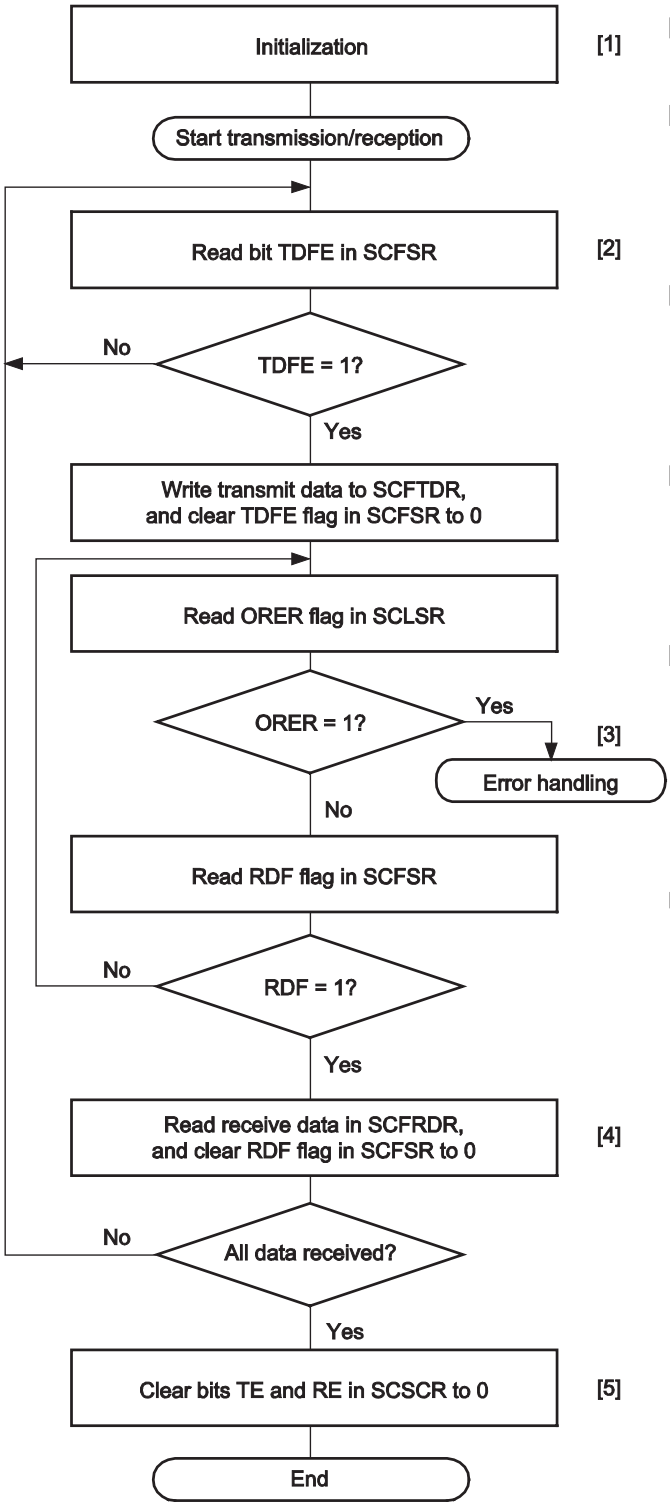


Figure 35.22 Example of SCIF Reception in Clock Synchronous Mode

(d) Simultaneous Serial Data Transmission/Reception (Clock Synchronous Mode)

Figure 35.23 shows a sample flowchart for simultaneous serial data transmission/reception.

The SCIF transmission and reception should be enabled before taking the following steps for simultaneous serial data transmission/reception.



[1] SCIF initialization:
See figure 51.17, Sample Flowchart for SCIF Initialization.

[2] SCIF status check and write for transmit data:
Read SCFSR and check that the TDFE flag is set to 1, then write transmit data to SCFTDR, and clear the TDFE flag to 0. The change of the value of the TDFE flag from 0 to 1 can also be identified by a TDFE/TEND interrupt.

[3] Receive error handling:
If a receive error occurs, read the ORER flag in SCLSR, perform the appropriate error handling, then clear the ORER flag to 0. The SCIF cannot resume reception while the ORER flag is set to 1.

[4] SCIF status check and read for receive data:
Read SCFSR and check that RDF =1, then read the receive data in SCFRDR, and clear the RDF flag to 0. The change of the value of the RDF flag from 0 to 1 can also be identified by an RDF interrupt.

[5] Serial transmission and reception continuation procedure:
To continue serial data transmission and reception, read RDF flag and SCFRDR, and finish clearing the RDF flag to 0 before receiving the MSB in the current frame.
Similarly, read 1 from the TDFE flag to confirm that writing is enabled before transmitting the MSB in the current frame. Then write data to SCFTDR and clear the TDFE flag to 0.

Note : When switching from transmission or reception to simultaneous transmission and reception, clear bits TE and RE to 0, and then set them to 1 simultaneously.

Figure 35.23 Sample Flowchart for Simultaneous Serial Data Transmission/Reception

35.4 SCIF Interrupt Sources and the DMAC

If the DMAC is used for transmission/reception, set and enable the DMAC before setting the SCIF.

Transmission Interrupts and DMA Transfer:

If the TDFE/TEND flag in SCFSR is set to 1 when the TDFE/TEND interrupt is enabled by the TIE bit, a TDFE/TEND interrupt request and a transmit-FIFO-data-empty DMA transfer request will occur. If the TDFE/TEND flag is set to 1 when TDFE/TEND interrupt is disabled by the TIE bit, only the transmit-FIFO-data-empty DMA transfer request will occur. (A transmit-FIFO-data-empty DMA transfer request is generated when the TDFE flag is set while TEIE is 0, or when the TEND flag is set while TEIE is 1. DMA transfer requests are not affected by the TEIE bit.)

When TDFE/TEND interrupt requests are enabled, the interrupt requests are cleared by the DMAC regardless of the interrupt handling program.

Reception Interrupts and DMA Transfer:

If the RDF/DR flag in SCFSR is set to 1 when RDF/DR interrupt is enabled by the RIE bit, an RDF/DR interrupt request occurs. If the RDF/DR flag is set to 1, a receive-FIFO-data-full DMA transfer request occurs. If the RDF/DR flag is set to 1 when RDF/DR interrupt is disabled by the RIE bit, and only a receive-FIFO-data-full DMA transfer request occurs and DMAC can be activated to perform data transfer.

Setting the RIE bit in SCSCR to 0 and the REIE it to 1 generates the ER/BRK/ORER interrupt requests without generating RDF/DR interrupt requests. When the BRK flag in SCFSR or the ORER flag in SCLSR is set to 1, BRK/ORER interrupt requests occur.

If the TO flag is set to 1 in SCLSR when TO interrupts are enabled by the TOIE bit, TO interrupt requests occur.

DR/TO interrupt requests generated by setting the DR or TO flag to 1 or receive-FIFO-data-full DMA transfer requests occur only in asynchronous mode.

When DR/TO interrupt requests are enabled to be issued, interrupt requests generated by the DR flag are cleared by the DMAC regardless of the interrupt handling program, however, those generated by the TO flag are not cleared by the DMAC. Therefore, the TO flag interrupt requests need to be cleared with the interrupt handling program. (The DR and TO flags are set at the same time, but cleared separately.)

Table 35.7 SCIF Interrupt Sources

Interrupt Source	DMAC Activation	Priority on Reset Release
Interrupts generated by receive error flag (ER)	Disabled	High
Interrupts generated by receive-FIFO-data-full (RDF), receive-data-ready (DR) or timeout (TO) *	Enabled	↕
Interrupts generated by break (BRK) or overrun error (ORER)	Disabled	↕
Interrupts generated by transmit FIFO data empty (TDFE)	Enabled	Low

Note: * RXI interrupts by means of the DR or TO flag are available only in asynchronous mode.

35.5 Usage Notes

Note the following on use of the SCIF.

(1) Break Detection and Operation

Break signals can also be detected by reading the RX pin value directly when a framing error (FER) is detected. In the break state, the input values from the RX pin are all 0s. So, the parity error flag (PER) may be set after the FER flag is set to 1.

Although the SCIF stops receive data transfer to SCFRDR after detecting a break, it continues data reception.

(2) Sending a Break Signal

The input/output condition and level of the TX pin are determined by the SPB2IO and SPB2DT bits in SCSPTR. This enables to send a break signal.

The pin does not function as the TX pin from the initialization of the serial transmitter to setting of the TE bit (enabling transmission). In this period, the marked state is substituted by the value of the SPB2DT bit. Therefore, the SPB2IO and SPB2DT bits should be set to 1 (designating output and high level) beforehand.

To send a break signal during serial transmission, clear the SPB2DT bit to 0 (low level), and then clear the TE bit to 0 (halting transmission). When the TE bit is cleared, the transmitter is initialized regardless of the current transmission state, and the TX pin outputs 0.

(3) Data Sampling Timing and Reception Margin in Asynchronous Mode

In asynchronous mode, the SCIF operates on the base clock with a frequency 16 times the bit rate.

In reception, the SCIF performs the internal synchronization by sampling the fall edge of the start bit using the base clock. In addition, the SCIF takes receive data at the rising edge of the eighth pulse on the base clock.

Figure 35.24 shows the timing of this operation.

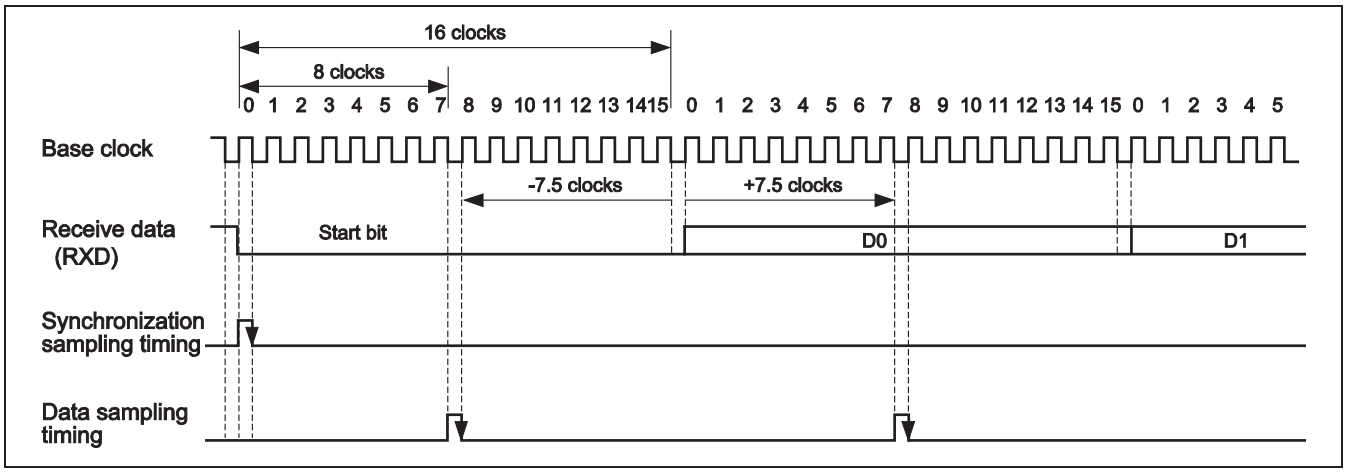


Figure 35.24 Timing Chart of Receive Data Sampling

The reception margin in asynchronous mode is given by expression (1).

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5)F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\% \quad \text{Expression (1)}$$

M: Receive margin (%)

N: Ratio of bit rate to clock (N = 16)

D: Clock duty (D = 0 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock frequency deviation

Assuming F = 0 and D = 0.5 for expression (1), the reception margin obtained with expression (2) is 46.875% as shown below:

Assuming D = 0.5 and F = 0

$M = (0.5 - 1/(2 \times 16)) \times 100\%$

$= 46.875\%$ ……expression (2)

This is a theoretical value. A reasonable margin allowed in system designs is 20% to 30%.

(4) Reception Margin and Baud Rate Error

The value of 46.875% obtained by the above expression (2) indicates the reception margin when the baud rate error is 0 (F = 0). If there is no error in the reception and transmission baud rates, reception is possible even with misalignment of approx. 1/2 bit. If there is an error in the reception and transmission baud rates, the errors are accumulated up to the stop bit reception, which reduces the reception margin. The allowable baud rate error can be obtained by modifying the F in expression (1). When D = 0.5:

$F = \{(15/32 - M)/(L - 0.5)\} \times 100\ (\%)$……expression (3)

By using expression (3), the relationship between the allowable error and reception margin with the frame length = 12 can be summarized as follows:

Allowed Error (%)	Reception Margin (%)
4.07	0
3.64	5
3.20	10
2.33	20
1.46	30

35.6 Baud Rate Generator for External Clock (BRG)

35.6.1 Overview

The SCIF incorporates a baud rate generator for external clock (abbreviated as BRG, hereafter). The BRG supplies a sampling clock (BRGCLK) to the SCIF core by dividing the external clock SC_CLK (selectable between SCIF_CLK and ZSϕ) by 1 to $2^{16} - 1$. In addition, the BRG switches the output between the external clock SCK and divided clock.

Figure 35.25 shows a block diagram of the BRG.

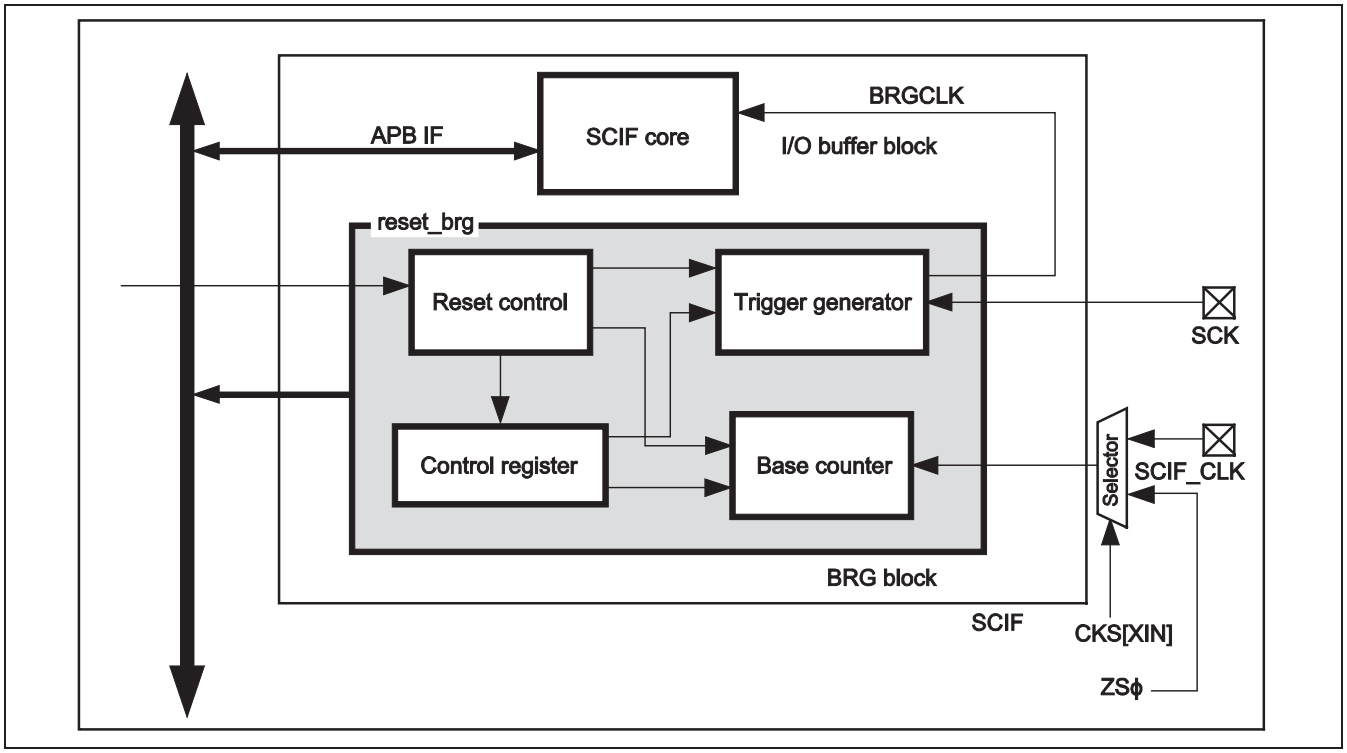


Figure 35.25 BRG Block Diagram

(1) Reset Controller:

The reset controller handles resetting the control register, base counter, and trigger generator.

(2) Control Register:

The control register has the frequency division register and clock select register.

(3) Base Counter:

The base counter is a 16-bit CLK synchronization counter that is used to determine the timing for generating a frequency divided clock.

(4) Trigger Generator:

The trigger generator generates rising-edge/falling-edge triggers for a frequency divided clock with the timing according to values of the frequency division register and base counter. The triggers are used to generate the frequency divided clock. In addition, the trigger generator switches the output between the SCK (external clock input) and frequency divided clock.

35.6.2 Register Configuration

Table 35.8 shows the registers in the BRG block.

Table 35.8 List of Registers

Name	Abbreviation	R/W	Initial Value	Relative Address	Access Size
Frequency division register	DL	R/W	H'0000	H'30	16
Clock select register	CKS	R/W	H'0000	H'34	16

35.6.2.1 Frequency Division Register (DL)

This register specifies the value of frequency division for the frequency divided clock generated by the BRG.

This register supports a 16-bit binary format that allows specifying a value in the rage of 1 to 65535.

Setting all 0s in this register makes the BRG output the frequency divided clock at the low level.

The value of frequency division is given by the following formula:

The value of frequency division = (clock input frequency)/(required baud rate × 16)

Table 35.9 shows how to use the baud rate generator with a 3.6864-MHz crystal resonator.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DL[15:0]	All 0	R/W	Specifies a division value of frequency clock generated in BRG. The value settings enabled in the range of 1 to 65535.

Table 35.9 Baud Rate (3.6864-MHz clock)

Baud Rate	Value of Frequency Division	Error Rate
50	4608	—
75	3072	—
110	2095	–0.022
134.5	1713	0.001
150	1536	—
300	768	—
600	384	—
1200	192	—
1800	128	—
2000	115	0.174
2400	96	—
3600	64	—
4800	48	—
7200	32	—
9600	24	—
14400	16	—
19200	12	—
38400	6	—
76800	3	—
115200	2	—

Note: — Indicates that the error rate is 0.

35.6.2.2 Clock Select Register (CKS)

This register switches the output between the frequency divided clock and specifies a source clock for the external baud rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CKS	XIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	CKS	0	R/W	This bit switches the output between the frequency divided clock (SC_CLK) and external clock (SCK). 0: Selects the frequency divided clock. 1: Selects the external clock.
14	XIN	0	R/W	Selects the baud rate generator clock source for the external clock between SCIF_CLK and ZSϕ. 0: Selects the external clock (SCIF_CLK). 1: Selects the internal clock (ZSϕ).
13 to 0	All 0	0	R	Reserved These bits are always read as 0. Only 0 should be written to these bits.

35.6.3 Restrictions in BRG

(1) Notes on Setting Frequency Division Register

1. For the initial setting of the register after a reset, at least one bit of waiting period is required to secure the clock stabilization time.
   (Example) One bit period when DL = 2

   $3.68\ (\text{MHz}) \times 1/2 \times 1/16 = 0.115\ (\text{MHz}) \rightarrow 8695\ (\text{ns})$

2. For modifying the register value after the setting stated in <1> above, at least one bit of waiting period at the maximum bit rate (DL = '65535') is required.
   The SCIF registers and BRG registers should be set as the following table:

- Asynchronous mode (SC_CLK external input)

SCIF		BRG	
Register Name	**Setting Value**	**Register Name**	**Setting Value**
SCSMR.C/A#	0	CKS	0000
SCSCR.CKE[1:0]	10	DL	1 to FFFF

- Asynchronous mode (SCK external input)

SCIF		BRG	
Register Name	**Setting Value**	**Register Name**	**Setting Value**
SCSMR.C/A#	0	CKS	8000
SCSCR[1:0]	10	DL	Don’t care

- Clock synchronous mode (external input)

SCIF		BRG	
Register Name	**Setting Value**	**Register Name**	**Setting Value**
SCSMR.C/A#	1	CKS	8000
SCSCR[1:0]	10	DL	Don’t care

3. The register settings for the baud rate generator for external clock should be made before starting initialization of the SCIF.

36. High Speed Serial Communication Interface with FIFO (HSCIF)

36.1 Overview

The RZ/G1C products have a high speed serial communication interface with built-in FIFO buffers (high-speed serial communication interface with FIFO: HSCIF) that handles asynchronous communication. The HSCIF has two 128-stage FIFO buffers separately for transmission and reception, which enables fast, efficient, and uninterrupted communication. The product has 3 channels. All functions of each channel are same.

36.1.1 Features

The HSCIF has the following features.

- Asynchronous serial communication mode
  The HSCIF performs serial data communication based on a character-by-character asynchronous system. This feature enables serial data communication with standard asynchronous communication chips that support universal asynchronous receiver/transmitter (UART) or asynchronous communication interface adapter (ACIA). There is a choice of eight serial data transfer formats.
  — Data length: 7 or 8 bits
  — Stop bit length: 1 or 2 bits
  — Parity: Even/odd/none
  — Receive error detection: Parity, framing, and overrun errors
  — Break detection:
    A break is detected when a framing error lasts for more than 1 frame length at space 0 (low level).
    When a framing error occurs, a break can also be detected by reading the HRX pin level directly from the serial port register (HSSPTR).
  — Sampling rate: Variable (integer number from 8 to 32)
- Capable of full-duplex communication
  The HSCIF has an independent transmitter and receiver that enable simultaneous transmission and reception. The transmitter and receiver both have a 128-stage FIFO buffer structure, enabling continuous serial data transmission and reception.
- On-chip baud rate generator, enabling any bit rate to be selected
  The HSCIF enables choice of a clock source for transmission/reception: a clock from the on-chip baud rate generator based on the internal clock or an external clock.
- Eight interrupt sources
  The HSCIF has eight types of interrupt sources: receive-data-ready, receive-FIFO-data-full, break detection, transmit-FIFO-data-empty, transmit-end, receive-error, overrun-error and time-out, and enables any of them to be requested independently.
- DMA data transfer
  When the transmit FIFO register is empty or the receive FIFO register has received data, issuing a DMA transfer request activates the DMA controller (DMAC) to execute a data transfer.
- Modem control functions (HRTS# and HCTS#) are stored.
- The amount of data in the transmit/receive FIFO registers and the number of receive errors in receive data in the receive FIFO register are available.
- A receive data ready (DR) or a timeout error (TO) can be detected during reception.

36.1.2 Block Diagram

Figure 36.1 shows the HSCIF block diagram.

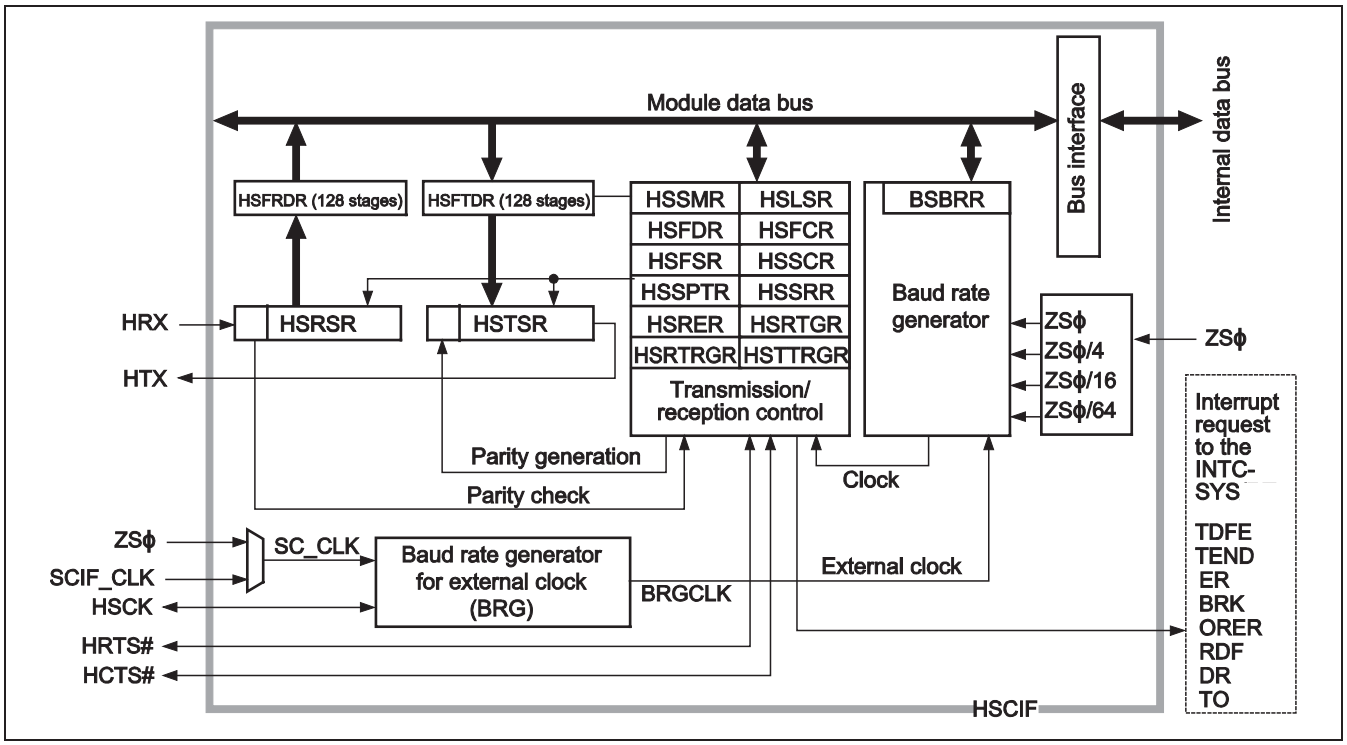


Figure 36.1 HSCIF Block Diagram

36.1.3 Pin Configuration

Table 36.1 shows the HSCIF pin configuration. These pins are multiplexed in other functions, so that the usage of the pins are may be restricted depending on the multiplexed pin settings.

Table 36.1 Pin Configuration

Name	Function	I/O	Descriptions
HSCK0	Serial clock pin	I/O	Clock I/O
HSCK1	Serial clock pin	I/O	Clock I/O
HSCK2	Serial clock pin	I/O	Clock I/O
HRX0	Receive data pin	Input	Receive data input
HRX1	Receive data pin	Input	Receive data input
HRX2	Receive data pin	Input	Receive data input
HTX0	Transmit data pin	Output	Transmit data output
HTX1	Transmit data pin	Output	Transmit data output
HTX2	Transmit data pin	Output	Transmit data output
HCTS0#	Modem control pin	I/O	Transmission enabled
HCTS1#	Modem control pin	I/O	Transmission enabled
HCTS2#	Modem control pin	I/O	Transmission enabled
HRTS0#	Modem control pin	I/O	Transmission request
HRTS1#	Modem control pin	I/O	Transmission request
HRTS2#	Modem control pin	I/O	Transmission request
SCIF_CLK	Baud rate generation clock pin	Input	Clock for input to the baud rate generator for the external clock

Note: These pins are made to function as serial pins by setting up HSCIF operation using bits TE, RE, CKE[1:0] in HSSCR, and bit MCE in HSFCR. HSSPTR of the HSCIF can be used to handle the transmission and detection of break states.

36.1.4 Register Configuration

Table 36.2 shows the registers in the HSCIF. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

Table 36.2 Register Configuration

Ch. No.	Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size
0	Serial mode register	HSSMR	R/W	H'0000	H'E62C 0000	16
	Bit rate register	HSBRR	R/W	H'FF	H'E62C 0004	8
	Serial control register	HSSCR	R/W	H'0000	H'E62C 0008	16
	Transmit FIFO data register	HSFTDR	W	—	H'E62C 000C	8
	Serial status register	HSFSR	R/(W)*1	H'0060	H'E62C 0010	16
	Receive FIFO data register	HSFRDR	R	H'XX	H'E62C 0014	8
	FIFO control register	HSFCR	R/W	H'0000	H'E62C 0018	16
	FIFO data count register	HSFDR	R	H'0000	H'E62C 001C	16
	Serial port register	HSSPTR	R/W	H'00XX	H'E62C 0020	16
	Line status register	HSLSR	R/(W)*2	H'0000	H'E62C 0024	16
	Sampling rate register	HSSRR	R/W	H'000F	H'E62C 0040	16
	Serial error register	HSRER	R	H'0000	H'E62C 0044	16
	RTS output active trigger register	HSRTGR	R/W	H'000F	H'E62C 0050	16
	Receive FIFO data count trigger register	HSRTRGR	R/W	H'0001	H'E62C 0054	16
	Transmit FIFO data count trigger register	HSTTRGR	R/W	H'0008	H'E62C 0058	16
1	Serial mode register	HSSMR	R/W	H'0000	H'E62C 8000	16
	Bit rate register	HSBRR	R/W	H'FF	H'E62C 8004	8
	Serial control register	HSSCR	R/W	H'0000	H'E62C 8008	16
	Transmit FIFO data register	HSFTDR	W	—	H'E62C 800C	8
	Serial status register	HSFSR	R/(W)*1	H'0060	H'E62C 8010	16
	Receive FIFO data register	HSFRDR	R	H'XX	H'E62C 8014	8
	FIFO control register	HSFCR	R/W	H'0000	H'E62C 8018	16
	FIFO data count register	HSFDR	R	H'0000	H'E62C 801C	16
	Serial port register	HSSPTR	R/W	H'00XX	H'E62C 8020	16
	Line status register	HSLSR	R/(W)*2	H'0000	H'E62C 8024	16
	Sampling rate register	HSSRR	R/W	H'000F	H'E62C 8040	16
	Serial error register	HSRER	R	H'0000	H'E62C 8044	16
	RTS output active trigger register	HSRTGR	R/W	H'000F	H'E62C 8050	16
	Receive FIFO data count trigger register	HSRTRGR	R/W	H'0001	H'E62C 8054	16
	Transmit FIFO data count trigger register	HSTTRGR	R/W	H'0008	H'E62C 8058	16
2	Serial mode register	HSSMR	R/W	H'0000	H'E62D 0000	16
	Bit rate register	HSBRR	R/W	H'FF	H'E62D 0004	8
	Serial control register	HSSCR	R/W	H'0000	H'E62D 0008	16
	Transmit FIFO data register	HSFTDR	W	—	H'E62D 000C	8
	Serial status register	HSFSR	R/(W)*1	H'0060	H'E62D 0010	16
	Receive FIFO data register	HSFRDR	R	H'XX	H'E62D 0014	8
	FIFO control register	HSFCR	R/W	H'0000	H'E62D 0018	16
	FIFO data count register	HSFDR	R	H'0000	H'E62D 001C	16

Ch. No.	Register Name	Abbreviation	R/W	Value after Reset	Address	Access Size
2	Serial port register	HSSPTR	R/W	H'00XX	H'E62D 0020	16
	Line status register	HSLSR	R/(W)*2	H'0000	H'E62D 0024	16
	Sampling rate register	HSSRR	R/W	H'000F	H'E62D 0040	16
	Serial error register	HSRER	R	H'0000	H'E62D 0044	16
	RTS output active trigger register	HSRTGR	R/W	H'000F	H'E62D 0050	16
	Receive FIFO data count trigger register	HSRTRGR	R/W	H'0001	H'E62D 0054	16
	Transmit FIFO data count trigger register	HSTTRGR	R/W	H'0008	H'E62D 0058	16

Notes: 1. Only 0 can be written to clear the flags. Bits 15 to 8, 3, and 2 are read-only bits and cannot be modified.
2. Only 0 can be written to clear the flags. Bits 15 to 3, and 1 are read-only bits and cannot be modified.

36.2 Register Descriptions

36.2.1 Receive Shift Register (HSRSR)

HSRSR is a register that receives serial data.

The HSCIF sets serial data input to the HSRSR from the HRX pin in the order received, starting with the LSB (bit 0), and converts it to parallel data. When one byte of data has been received, it is transferred to the receive FIFO register HSFRDR, automatically.

HSRSR cannot be read from and written to by the CPU.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—
R/W:	—	—	—	—	—	—	—	—

36.2.2 Receive FIFO Data Register (HSFRDR)

HSFRDR is a 128-stage FIFO register that stores received serial data.

When HSCIF has received one byte of serial data, it transfers the received data from the receive shift register (HSRSR) to HSFRDR for storage, and reception is thus completed. HSRSR is then ready for reception, and is capable of receiving up to 128 consecutive bytes of data before HSFRDR is full.

HSFRDR is a read-only register and cannot be modified by the CPU. Note that the read value will be undefined while there is no receive data in HSFRDR. When HSFRDR is full of receive data, subsequent serial data is lost.

HSFRDR is read as an undefined value after a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R

36.2.3 Transmit Shift Register (HSTSR)

HSTSR is a register that transmits serial data.

To perform serial data transmission, the HSCIF first transfers transmit data from the transmit fifo data register (HSFTDR) to HSTSR, then sends the data to the HTX pin starting with the LSB (bit 0). When transmission of one byte is completed, the HSCIF transfers the next transmit data from HSFTDR to HSTSR automatically, then starts transmission.

HSTSR cannot be read from and written to directly by the CPU.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—
R/W:	—	—	—	—	—	—	—	—

36.2.4 Transmit FIFO Data Register (HSFTDR)

HSFTDR is an 8-bit FIFO register of 128 stages that stores data for serial transmission.

If HSTSR is empty after transmit data has been written to HSFTDR, the HSCIF transfers the data from HSFTDR to HSTSR and starts serial transmission.

HSFTDR is a write-only register and cannot be read from by the CPU. Writing further data to HSFTDR is no longer possible when it is full. Attempts at writing data to the register in this situation are ignored.

HSFTDR is read as an undefined value on a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W

36.2.5 Serial Mode Register (HSSMR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CHR	PE	O/E#	STOP	—	CKS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W

HSSMR is a 16-bit register that sets the HSCIF's serial transfer format and selects the baud rate generator clock source.

HSSMR can always be read from and written to by the CPU.

HSSMR is initialized to H'0000 by a power-on reset.

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	CHR	0	R/W	Character Length Selects 7 or 8 bits for data length. When the 7-bit data is selected, the MSB (bit 7) in the transmit FIFO data register (HSFTDR) is not transmitted. 0: 8 bits 1: 7 bits
5	PE	0	R/W	Parity Enable Determines whether parity bit is added in transmission or not, and parity bit is checked in reception or not. When bit PE is set to 1, the parity (even or odd) specified by bit O/E# is added to transmit data. In reception, the parity bit is checked for the parity (even or odd) specified by bit O/E#. 0: Disables parity bit addition and check. 1: Enables parity bit addition and check.
4	O/E#	0	R/W	Parity Mode Selects either even or odd parity to use in parity addition and check. The O/E# bit setting is valid only when bit PE is set to 1, enabling parity bit addition and check. 0: Even parity 1: Odd parity When even parity is set, the parity bit is added in transmission so that the total number of 1-bit in the transmit character plus the parity bit is even. In reception, a check is performed to see if the total number of 1-bit in the receive character plus the parity bit is even. When odd parity is set, the parity bit is added in transmission so that the total number of 1-bit in the transmit character plus the parity bit is odd. In reception, a check is performed to see if the total number of 1-bit in the receive character plus the parity bit is odd.

Bit	Bit Name	Initial Value	R/W	Description
3	STOP	0	R/W	Stop Bit Length Selects 1 bit or 2 bits as the stop bit length. In reception, only the first stop bit is checked, regardless of the STOP bit setting. If the second stop bit is 1, it is treated as a stop bit. If it is 0, it is treated as the start bit of the next transmit character. 0: 1 stop bit*1 1: 2 stop bits*2 Notes: 1. In transmission, a single 1-bit (stop bit) is added to the end of a transmit character before it is sent. 2. In transmission, two 1-bit (stop bits) are added to the end of a transmit character before it is sent.
2	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
1, 0	CKS[1:0]	00	R/W	Clock Select 1 and 0 These bits select the clock source for the on-chip baud rate generator. The clock source can be selected from ZSϕ, ZSϕ/4, ZSϕ/16, and ZSϕ/64, according to the setting of bits CKS[1:0]. 00: ZSϕ 01: ZSϕ/4 10: ZSϕ/16 11: ZSϕ/64

36.2.6 Serial Control Register (HSSCR)

HSSCR is a register that enables or disables transmission/reception by the HSCIF, enables or disables interrupt requests, and selects transmission/reception clock source for the HSCIF.

HSSCR can always be read from and written to by the CPU.

HSSCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOT[1:0]		—	—	TEIE	—	—	—	TIE	RIE	TE	RE	REIE	TOIE	CKE[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TOT[1:0]	00	R/W	Set the time for a data ready (DR) or a timeout (TO) to be set in asynchronous mode. 00: 15 etu* 01: 31 etu 10: 47 etu 11: 63 etu Note: * ETU: Elementary Time Unit (time for transfer of one bit) Equivalent to 1.5 frames with an 8-bit, 1-stop-bit format.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11	TEIE	0	R/W	Transmit End Interrupt Enable When a transmit-end request is enabled by the TIE bit, the TEIE bit selects the source of the transmit end interrupt request from the following: • Setting the TDFE flag in HSFSR • Setting the TEND flag in HSFSR 0: The transmit FIFO data empty (TDFE) interrupt request is used. 1: The transmit end (TEND) interrupt request is used.
10 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7	TIE	0	R/W	Transmit Interrupt Enable Enables or disables a transmit-FIFO-data-empty interrupt (TDFE) request when the TEIE bit in HSSCR is pulled 0, if the following conditions are satisfied: • Serial transmit data has been transferred from HSFTDR to HSTSR, • The number of data bytes in HSFTDR is equal to or less than the transmit trigger count, and • The TDFE flag in HSFSR is set to 1. Enables or disables a transmit-end interrupt (TEND) request when the TEIE bit of HSSCR is set to 1, if the following conditions are satisfied: • Transmission was ended because there is no valid data in HSFTDR when the last bit of the transmit character in HSTSR was transmitted, and • The TEND flag of HSFSR is set to 1. 0: When the TEIE bit is 0, disables transmit-FIFO-data-empty interrupt (TDFE) request. When the TEIE bit is 1, disables transmit-end interrupt (TEND) request. 1: When the TEIE bit is 0, enables transmit-FIFO-data-empty interrupt (TDFE) request. When the TEIE bit is 1, enables transmit-end interrupt (TEND) request.
6	RIE	0	R/W	Receive Interrupt Enable Enables or disables a receive-FIFO-data-full interrupt request when the RDF flag in HSFSR is set to 1, a receive-data-ready interrupt request when the DR flag in HSFSR is set to 1, a receive-error interrupt request when the ER flag in HSFSR is set to 1, a break interrupt request when the BRK flag in HSFSR is set to 1, and an overrun error interrupt request when the ORER flag in HSLSR is set to 1. 0: Disables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests. 1: Enables receive-FIFO-data-full interrupt (RDF) requests, receive-data-ready interrupt (DR) requests, receive-error interrupt (ER) requests, break interrupt (BRK) requests, and overrun error interrupt (ORER) requests.
5	TE	0	R/W	Transmit Enable Enables or disables the start of HSCIF serial transmission. The HSCIF starts serial transmission when transmit data is written to the HSFTDR while TE is 1. Before setting TE to 1, set HSSMR and HSFCR to specify the transmission format and reset the transmit FIFO. 0: Disables transmission. 1: Enables transmission.

Bit	Bit Name	Initial Value	R/W	Description
4	RE	0	R/W	Receive Enable Enables or disables the start of HSCIF serial reception. When RE is 1, the HSCIF starts serial reception by detecting a start bit. Before setting RE to 1, set HSSMR and HSFCR to specify the reception format and reset the receive FIFO. 0: Disables reception.* 1: Enables reception. Note: * Even if RE is cleared to 0, the DR, ER, BRK, RDF, FER, PER, TO and ORER flags are not affected, and retain their states.
3	REIE	0	R/W	Receive Error Interrupt Enable Enables or Disables generation of receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests. 0: Disables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests.* 1: Enables receive-error interrupt (ER) requests, break interrupt (BRK) requests and overrun-error interrupt (ORER) requests. Note: * When REIE is 1, ER, BRK or ORER interrupt requests will occur even if RIE is cleared to 0. This setting is used to notify the interrupt controller of ER, BRK, and ORER interrupt requests during DMAC transfer.
2	TOIE	0	R/W	Timeout Interrupt Enable Enables or disables generation of timeout interrupt (TO) requests when the TO flag in HSLSR is set to 1. 0: Disables timeout interrupts (TO). 1: Enables timeout interrupts (TO).
1, 0	CKE[1:0]	00	R/W	Clock Enable 1 and 0 These bits select the HSCIF clock source and enables or disables the clock output from the HSCK pin. Whether the HSCK pin functions as a serial clock output pin or a serial clock input pin is determined by CKE[1:0] bit settings. See Table 36.3 for the bit settings.

Table 36.3 Clock Selection

CKE[1]	CKE[0]	Clock Source	HSCK Pin
0	0	Internal clock (ZSϕ, ZSϕ/4, ZSϕ/16, and ZSϕ/64)	The HSCK pin is not used. The HSCK pin functions as an input pin (input signals are ignored). (Initial value)
0	1		The HSCK pin outputs the clock (with a bit rate multiplied by the sampling rate).
1	0	Baud rate generator output for external clock or HSCK	When SC_CLK is selected: The HSCK pin is an input pin (input signals are ignored). Set the SC_CLK frequency so that the frequency of BRGCLK is multiplied by the sampling rate.
			When HSCK is selected: The HSCK pin inputs the clock (with the bit rate multiplied by the sampling rate).
	1	Prohibited	

Note: It is not allowed to set synchronous communication using SC_CLK for input.

36.2.7 Serial Status Register (HSFSR)

HSFSR is a 16-bit register. The lower 8 bits are status flags that indicate the operating status of the HSCIF, and the upper 8 bits are all reserved.

HSFSR can always be read from and written to by the CPU. However, the flags ER, TEND, TDFE, BRK, RDF, and DR cannot be written by 1. The FER and PER flags are read-only flags and cannot be modified.

HSFSR is initialized to H'0060 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	ER	TEND	TDFE	BRK	FER	PER	RDF	DR
Initial value:	0	0	0	0	0	0	0	0	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/(W)*	R/(W)*	R/(W)*	R/(W)*	R	R	R/(W)*	R/(W)*

Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	ER	0	R/(W)*	Receive Error Indicates that a framing error or a parity error has occurred in reception. The ER flag is not affected by an error and retains its previous state when the RE bit is 0 in HSSCR. If a receive error occurs, receive data will be transferred to HSFRDR and reception operation will be continued. Whether there is a receive error in data read from HSFRDR can be determined by the FER and PER bits in HSFSR. 0: Indicates that no framing or parity error has occurred in reception. [Clearing conditions] • A power-on reset is executed. • 0 is written to ER. 1: Indicates that a framing error or a parity error has occurred in reception. [Setting conditions] • The HSCIF checks whether the stop bit at the end of receive data is 1, but the stop bit is 0.* • The number of 1-bit in receive data plus the parity bit does not match the parity setting (even or odd) specified by the O/E# bit in HSSMR during reception. Note: * In the 2-stop-bit mode, only the first stop bit is checked that the value is 1; the second stop bit is not checked.

Bit	Bit Name	Initial Value	R/W	Description
6	TEND	1	R/(W)*	Transmit End Indicates that transmission has been ended because there was no valid data in HSFTDR when the last bit of the transmit character was transmitted. 0: Indicates that transmission is in progress. [Clearing conditions] • Transmit data is written to HSFTDR, and 0 is written to TEND. • Data is written to HSFTDR by the DMAC. 1: Indicates that transmission has been ended. [Setting conditions] • A power-on reset is executed. • The TE bit in HSSCR is 0. • There is no transmit data in HSFTDR when the last bit of a 1-byte serial transmission character is transmitted.
5	TDFE	1	R/(W)*	Transmit FIFO Data Empty Indicates that the HSCIF has transferred data from HSFTDR to HSTSR, the number of data bytes in HSFTDR becomes equal to or less than the transmit trigger count specified by the HSTTRGR, and HSFTDR is ready to be written by new transmit data. HSFTDR is a 128-byte FIFO register. The maximum number of bytes that can be written to when TDFE = 1 is "128 – [the transmit trigger count]". If data exceeding this value is attempted to be written, the data will be ignored. The number of data bytes in HSFTDR is indicated by the upper bits of HSFDR. If the number of data written in HSFTDR is equal to or less than the transmit trigger count, this bit will be set to 1 even if it is cleared to 0 after it is read as 1. 0: Indicates that the number of transmit data written to HSFTDR exceeds the transmit trigger count. [Clearing conditions] • Transmit data exceeding the specified transmit trigger count have been written to HSFTDR, and 0 is written to TDFE. • Transmit data exceeding the specified transmit trigger count have been written to HSFTDR by the DMAC. 1: Indicates that the number of transmit data in HSFTDR is equal to or less than the transmit trigger count. [Setting conditions] • A power-on reset is executed. • The number of transmit data in HSFTDR is equal to or less than the transmit trigger count after transmission.

Bit	Bit Name	Initial Value	R/W	Description
4	BRK	0	R/(W)*	Break Detect Indicates that a receive data break signal has been detected. If a break signal is detected, receive data (H'00) transfer to HSFRDR is stopped. After the break is canceled and the receive signal returns to 1, the receive data transfer resumes. 0: Indicates that no break signal has been received. [Clearing conditions] • A power-on reset is executed. • 0 is written to BRK. 1: Indicates that a break signal has been received. [Setting condition] • Data with a framing error is received, followed by the space "0" (low level) for at least one frame length.
3	FER	0	R	Framing Error Indicates that a framing error has been found in the data that is to be read next from HSFRDR. 0: Indicates that there is no framing error in the receive data that is to be read from HSFRDR. [Clearing conditions] • A power-on reset is executed. • There is no framing error in the data that is to be read next from HSFRDR. 1: Indicates that there is a framing error in the receive data that is to be read from HSFRDR. [Setting condition] • There is a framing error in the data that is to be read next from HSFRDR.
2	PER	0	R	Parity Error This bit indicates that a parity error has been found in the data that is to be read next from HSFRDR. 0: Indicates that there is no parity error in the receive data that is to be read from HSFRDR. [Clearing conditions] • A power-on reset is executed. • There is no parity error in the data that is to be read next from HSFRDR. 1: Indicates that there is a parity error in the receive data that is to be read from HSFRDR. [Setting condition] • There is a parity error in the data that is to be read next from HSFRDR.

Bit	Bit Name	Initial Value	R/W	Description
1	RDF	0	R/(W)*	Receive FIFO Data Full Indicates that the received data has been transferred from HSRSR to HSFRDR, and the number of receive data bytes in HSFRDR becomes equal to or more than the receive trigger count specified by the HSRTRGR. HSFRDR is a 128-byte FIFO register. When RDF = 1, data equal to or more than the number of receive trigger data bytes can be read. When HSFRDR is empty, HSFRDR is read as an undefined value. The number of receive data bytes in HSFRDR is indicated by the lower bits of HSFDR. If the number of data in HSFRDR is equal to or more than the trigger count, this bit will be set to 1 even if it is cleared to 0. At this time, read receive data until the number of data in HSFRDR is less than the trigger count, read RDF as 1, and then clear RDF. 0: Indicates that the number of receive data bytes in HSFRDR is less than the specified receive trigger count. [Clearing conditions] • A power-on reset is executed. • HSFRDR is read until the number of receive data bytes in HSFRDR is less than the receive trigger count, and 0 is written to RDF. • HSFRDR is read by the DMAC until the number of receive data bytes in HSFRDR is less than the receive trigger count. 1: Indicates that the number of receive data bytes in HSFRDR is equal to or more than the specified receive trigger count. [Setting condition] • Receive data more than the receive trigger count have been stored in HSFRDR.

Bit	Bit Name	Initial Value	R/W	Description
0	DR	0	R/(W)*	Receive Data Ready Indicates that the receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received. 0: Indicates that data is being received or has been successfully received, and there is no receive data in HSFRDR. [Clearing conditions] • A power-on reset is executed. • All the receive data in HSFRDR has been read, and 0 is written to DR. • All the receive data in HSFRDR has been read by the DMAC. 1: Indicates that no further receive data has been received. [Setting condition] The receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received. Note: * When the setting is 00, the time is 15 etu. This is equivalent to 1.5 frames in an 8-bit, 1-stop-bit format. etu: Elementary Time Unit (time for transfer of one bit)

Note: * Only 0 can be written to clear the flag.

36.2.8 Bit Rate Register (HSBRR)

HSBRR is an 8-bit register that sets the serial transmission/reception bit rate in accordance with the baud rate generator operating clock selected by the CKS[1:0] bits in HSSMR. This baud rate generator is intended for ZSϕ, ZSϕ/4, ZSϕ/16, and ZSϕ/64. For details on the baud rate generator for external clock, see section 36.5, Baud Rate Generator for External Clock (BRG).

HSBRR can always be read from and written to by the CPU except for during transfer.

HSBRR is initialized to H'FF by a power-on reset.

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The HSBRR setting is determined by the following equation:

[Asynchronous mode]

$$N = \frac{ZS\phi}{Sr \times 2^{2n+1} \times B} \times 10^6 - 1$$

B: Bit rate (bit/s)

N: HSBRR setting for the baud rate generator ($0 \le N \le 255$) (which satisfies the electrical characteristics)

ZSϕ: AXI bus clock operating frequency (MHz)

n: Baud rate generator input clock (n = 0, 1, 2, 3)
(See the Table 36.4 for the relation between n and the clock.)

Sr: Sampling rate (8 to 32)

Table 36.4 HSSMR Settings

n	Baud Rate Generator Input Clock	HSSMR Setting	
		CKS[1]	CKS[0]
0	ZSϕ	0	0
1	ZSϕ/4	0	1
2	ZSϕ/16	1	0
3	ZSϕ/64	1	1

The bit rate error in asynchronous mode is determined by the following equation:

$$\text{error (\%)} = \left\{ \frac{ZS\phi \times 10^6}{(N + 1) \times B \times Sr \times 2^{2n+1}} - 1 \right\} \times 100$$

36.2.9 FIFO Control Register (HSFCR)

HSFCR is a register that resets data counts for the transmit and receive FIFO registers. It also has a modem control and a loopback test enable bit.

HSFCR can always be read from and written to by the CPU except for during transfer.

HSFCR is initialized to H'0000 by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	MCE	TFRST	RFRST	LOOP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

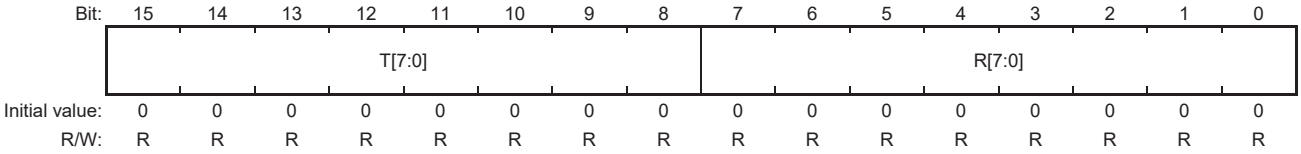
Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3	MCE	0	R/W	Modem Control Enable Enables or disables modem control signals HCTS# and HRTS#. 0: Disables modem signals.* 1: Enables modem signals. Note: * HCTS# and HRTS# control ports.
2	TFRST	0	R/W	Transmit FIFO Data Register Reset Enables or disables a transmit FIFO data register reset that empties the register. 0: Disables the reset.* 1: Enables the reset. Note: * The register is reset by a power-on reset.
1	RFRST	0	R/W	Receive FIFO Data Register Reset Enables or disables a receive FIFO data register (HSFRDR) reset that empties the register. 0: Disables the reset.* 1: Enables the reset. Note: * The register is reset by a power-on reset.
0	LOOP	0	R/W	Loopback Test Enables or disables the loopback test by internally connecting the transmit output pin (HTX) and receive input pin (HRX), and the HRTS# pin and HCTS# pin. 0: Disables the loopback test. 1: Enables the loopback test.

36.2.10 FIFO Data Count Register (HSFDR)

HSFDR is a 16-bit register that indicates the number of data bytes stored in HSFTDR and that in HSFRDR.

The upper 8 bits indicate the number of transmit data bytes in HSFTDR, and the lower 8 bits indicates the number of receive data bytes in HSFRDR.

HSFDR can always be read by the CPU.



Bit	Bit Name	Initial Value	R/W	Description
15 to 8	T[7:0]	H'00	R	These bits indicate the number of data bytes untransmitted and still stored in HSFTDR. H'00 indicates that there is no transmit data in HSFTDR, and H'80 indicates that HSFTDR is full of transmit data.
7 to 0	R[7:0]	H'00	R	These bits indicate the number of receive data stored in HSFRDR. H'00 indicates that there is no receive data in HSFRDR, and H'80 indicates that HSFRDR is full of receive data.

36.2.11 Serial Port Register (HSSPTR)

HSSPTR controls multiplexed input/output and data on the high speed serial communication interface (HSCIF) ports. Bits 1 and 0 control breaks in serial transmission/reception by reading input data from the HRX pin and writing output data to the HTX pin. Bits 3 and 2 read input data from and write output data to the HSCK pin. Bits 5 and 4 read input data from and write output data to the HCTS# pin. Bits 7 and 6 read input data from and write output data to the HRTS# pin.

HSSPTR is a 16-bit register that can always be read from and written to by the CPU.

All HSSPTR bits except bits 6, 4, 2, and 0 are initialized to 0 by a power-on reset. The values of bits 6, 4, 2, and 0 are undefined.

Note: Whether modem control can be selected or not depends on the channel.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RTSIO	RTSDT	CTSIO	CTSDT	SCKIO	SCKDT	SPB 2IO	SPB 2DT
Initial value:	0	0	0	0	0	0	0	0	0	—	0	—	0	—	0	—
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	RTSIO	0	R/W	Serial Port – RTS Port Input/Output Specifies input or output for the serial port HRTS# pin. To actually set the HRTS# pin as a port output pin to output the value set by the RTSDT bit, the MCE bit in HSFCR should be cleared to 0. 0: Indicates that this bit does not output the value of the RTSDT bit to the HRTS# pin. 1: Indicates that this bit outputs the value of the RTSDT bit to the HRTS# pin.
6	RTSDT	—	R/W	Serial Port – RTS Port Data Specifies the input/output data level of the serial port HRTS# pin. Whether the pin is set for input or output is determined by the RTSIO bit. When the pin is set for output, the value of the RTSDT bit is output to the HRTS# pin. Regardless of the value of the RTSIO bit, the value of the HRTS# pin is read from the RTSDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
5	CTSIO	0	R/W	Serial Port – CTS Port Input/Output Specifies input or output for the serial port HCTS# pin. To actually set the HCTS# pin as a port output pin to output the value set by the CTSDT bit, the MCE bit in HSFCR should be cleared to 0. 0: Indicates that the CTSDT bit value is not output to the HCTS# pin. 1: Indicates that the CTSDT bit value is output to the HCTS# pin.

Bit	Bit Name	Initial Value	R/W	Description
4	CTSDT	—	R/W	Serial Port – CTS Port Data Specifies the input/output data level of the serial port HCTS# pin. Whether the pin is set for input or output is determined by the CTSIO bit. When the pin is set for output, the value of the CTSDT bit is output to the HCTS# pin. Regardless of the value of the CTSIO bit, the value of the HCTS# pin is read from the CTSDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
3	SCKIO	0	R/W	Serial Port – Clock Port Input/Output Specifies input or output for the serial port HSCK pin. To actually set the HSCK pin as a port output pin to output the value set by the SCKDT bit, the CKE1 and CKE0 bits in HSSCR should be cleared to 0. 0: Indicates that the SCKDT bit value is not output to the HSCK pin. 1: Indicates that the SCKDT bit value is output to the HSCK pin.
2	SCKDT	—	R/W	Serial Port – Clock Port Data Specifies the input/output data level of the serial port HSCK pin. Whether the pin is set for input or output is determined by the SCKIO bit. When the pin is set for output, the value of the SCKDT bit is output to the HSCK pin. Regardless of the value of the SCKIO bit, the value of the HSCK pin is read from the SCKDT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.
1	SPB2IO	0	R/W	Serial Port – Break Input/Output Specifies the output condition of the serial port HTX pin. To actually set the HTX pin as a port output pin to output the value set by the SPB2DT bit, the TE bit in HSSCR should be cleared to 0. 0: Indicates that the SPB2DT bit value is not output to the HTX pin. 1: Indicates that the SPB2DT bit value is output to the HTX pin.
0	SPB2DT	—	R/W	Serial Port – Break Data Specifies the input level of the serial port HRX pin and the output level of the HTX pin. The HTX pin output conditions are determined by the SPB2IO bit. When the HTX pin is set for output, the value of the SPB2DT bit is output to the HTX pin. Regardless of the value of the SPB2IO bit, the value of the HRX pin is read from the SPB2DT bit. The initial value of this bit is undefined after a power-on reset. 0: Indicates that the input/output data is low level. 1: Indicates that the input/output data is high level.

36.2.12 Line Status Register (HSLSR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	TO	—	ORER
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/(W)*	R	R/(W)*

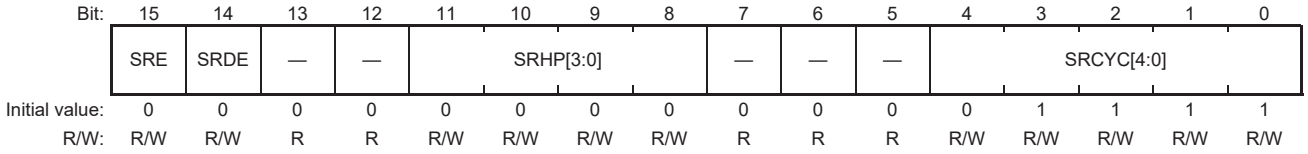
Note: * Only 0 can be written to clear the flag.

Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	TO	0	R/(W)*	Timeout Indicates that the receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received. 0: Indicates that data is being received or has been successfully received and that there is no receive data in HSFRDR. [Clearing conditions] • A power-on reset is executed. • All the receive data in the HSFRDR has been read, and 0 is written to TO. 1: Indicates that no further receive data has been received (receive timeout). [Setting condition] • The receive FIFO data register (HSFRDR) contains fewer bytes than the trigger number for reception and no further data have arrived over at least the time corresponding to the setting of HSSCR[15:14]* since the stop bit for the byte to have been received.* Note: * When the setting is 00, the time is 15 etu. This is equivalent to 1.5 frames in an 8-bit, 1-stop-bit format. etu: Elementary Time Unit (time for transfer of one bit)
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
0	ORER	0	R/(W)*	Overrun Error Indicates that an overrun error has occurred in reception and abnormal termination is caused. If an overrun error occurs, the receive data prior to the overrun error is retained in HSFRDR and the data received subsequently is discarded. Any subsequent serial reception is disabled while the ORER flag is 1. To resume data reception after clearing the ORER flag, be sure to first read (or clear) data in the receive FIFO and handle the error, then clear the ORER flag. 0: Indicates that data is being received or has been successfully received. [Clearing conditions] • A power-on reset is executed. • 0 is written to ORER. 1: Indicates that an overrun error has occurred in reception. [Setting condition] • The next serial reception has been completed while HSFRDR is full of 128-byte data. Note: When bit RE in HSSCR is cleared to 0, the ORER flag is not affected and its previous state is retained.

Note: * Only 0 can be written to clear the flag.

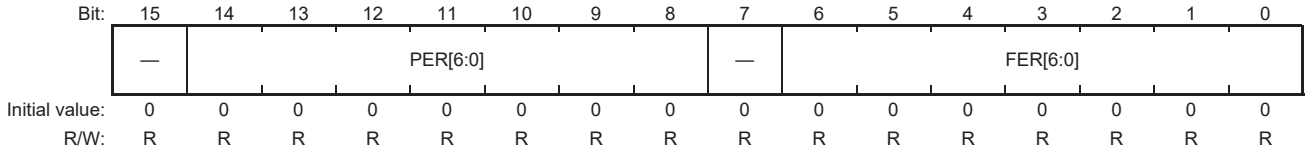
36.2.13 Sampling Rate Register (HSSRR)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SRE	SRDE	—	—	SRHP[3:0]				—	—	—	SRCYC[4:0]				
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SRE	0	R/W	Sampling Rate Register Enable (SRE) 0: Set the SRCYC[4: 0] bits to 15 (initial value). 1: Validates the setting of the SRCYC[4:0] bits.
14	SRDE	0	R/W	Sampling Point Register Enable (SRDE) 0: Invalidates the setting of the SRHP[3:0] bits and the sampling point will be (S+1)/2 for an odd sampling rate (S) and S/2 for an even sampling rate. 1: Validates the setting of the SRHP[3:0] bits.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
11 to 8	SRHP[3:0]	0000	R/W	Sampling Point Register (SRHP) The sampling point can be moved by setting the SDRE bit to 1 and setting a value in these bits. Normally, the sampling point is the point of S/2 or (S+1)/2 for a sampling rate of S. By setting a signed 4-bit integer in these bits, the sampling point can be shifted by the amount of the specified sampling clock cycles. This will improve the receive margin. When setting a value in these bits, take notice that the sampling point does not become a negative value or it does not exceed the sampling rate. The shifted sampling point must satisfy the setup margin and hold margin.
7 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4 to 0	SRCYC[4:0]	01111	R/W	Bits 4 to 0: Sampling Rate Register (SRCYC) Data transfer at a desired sampling rate can be enabled by setting the SRE bit to 1 and setting a value in these bits. Set a value of "S – 1" in these bits for a sampling rate of S. Note that the sampling rate must be from 8 to 32 (a value from 7 to 31 can be set in these bits). Set these bits to 15 (initial value) when the SRE bit is set to 0.

36.2.14 Serial Error Register (HSRER)



Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 8	PER[6:0]	H'00	R	Parity Error Count These bits indicate the number of data items in which a parity error occurred in the receive data stored in the receive FIFO data register (HSFRDR). After the ER bit in HSFSR is set, the value in bits 14 to 8 will be the number of data items in which a parity error occurred. If all 128 bytes of receive data in HSFRDR have parity errors, bits PER[6:0] will have the value 0.
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6 to 0	FER[6:0]	H'00	R	Framing Error Count These bits indicate the number of data items in which a framing error occurred in the receive data stored in the receive FIFO data register (HSFRDR). After the ER bit in HSFSR is set, the value in bits 6 to 0 will be the number of data items in which a framing error occurred. If all 128 bytes of receive data in HSFRDR have framing errors, bits FER[6:0] will have the value 0.

36.2.15 RTS Output Active Trigger Register (HSRTGR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RSTRG[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

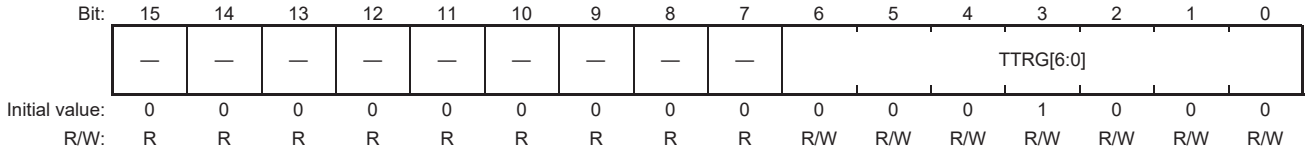
Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	RSTRG[6:0]	H'0F	R/W	RTS Output Active Trigger Count The HRTS# signal goes high when the number of receive data items stored in the receive FIFO data register (HSFRDR) exceeds the value set in these bits. The initial value is 15.

36.2.16 Receive FIFO Data Count Trigger Register (HSRTRGR)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RTRG[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	RTRG[6:0]	H'01	R/W	Receive FIFO Data Count Trigger These bits set the receive data item count at which the receive data full (RDF) flag in the serial status register (HSFSR) is set. The RDF flag is set when the number of receive data items stored in the receive FIFO data register (HSFRDR) equals or exceeds the value set in these bits. The initial value is 1.

36.2.17 Transmit FIFO Data Count Trigger Register (HSTTRGR)



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	TTRG[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	TTRG[6:0]	H'08	R/W	Transmit FIFO Data Count Trigger These bits set the untransmitted data item count at which the transmit FIFO data register empty (TDFE) flag in the serial status register (HSFSR) is set. The TDFE flag is set when the number of transmit data items in the transmit FIFO data register (HSFTDR) falls under the value set in these bits due to transmit operations. The initial value is 8.

36.3 Operation

36.3.1 Operation in Asynchronous Serial Communication Mode

In asynchronous serial communication mode, the HSCIF performs serial communication, in which data is transmitted/received in character units using the attached start bit indicating the start of communication and stop bit indicating the end of communication.

Figure 36.2 shows the general format for asynchronous serial communication.

In asynchronous serial communication, the transmission line is usually kept marked (high level). The HSCIF monitors the transmission line, and when it finds a space (low level), it regards the space as a start bit and starts serial communication.

One character in serial communication consists of a start bit (low level), followed by transmit/receive data (LSB-first; from the lowest bit), a parity bit (high or low level), and a stop bit (high level).

During reception in asynchronous mode, the HSCIF performs synchronization at the falling edge of the start bit. Transferred data is acquired at the center of each bit because the HSCIF samples on *S/2*th cycles of the clock which has a frequency of S times the bit rate, when the sampling rate as set in the sampling rate register (HSSRR) is S (if the sampling-rate setting is an odd number, the data is sampled on every *(S+1)/2*th pulse).

In addition, when the setting of the SRDE bit makes the setting of the sampling point bits effective, the point where the bits are latched can be intentionally moved from the centers of each bit.

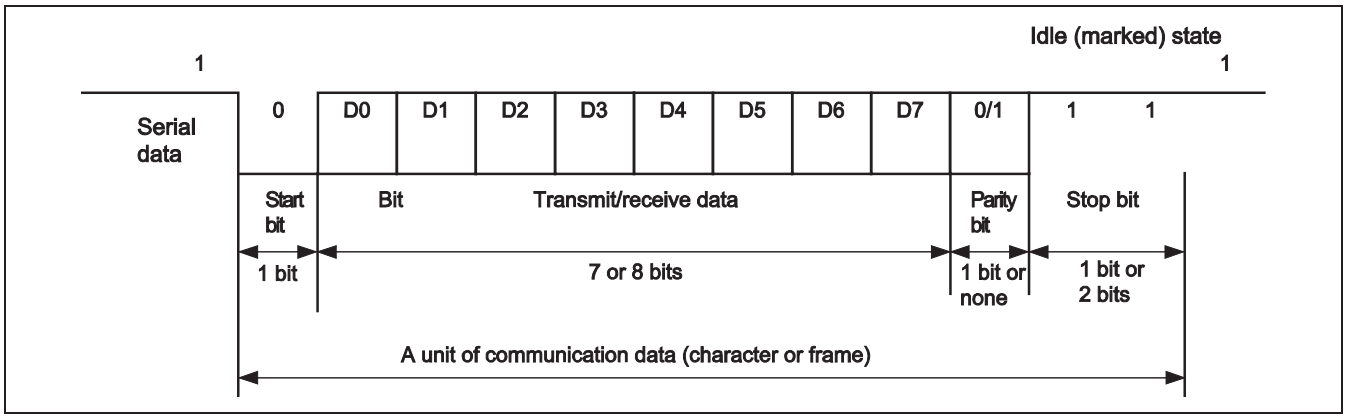


Figure 36.2 Data Format in Asynchronous Mode (Example of 8-Bit Data with Parity and Two Stop Bits)

(1) Transmission/reception format

Table 36.5 shows available data transfer formats. The HSCIF supports 8 transfer formats, which can be specified by HSSMR.

Table 36.5 Serial Transmission/Reception Formats (Asynchronous Mode)

SCSMR settings			Serial transmission/reception format and frame length											
CHR	PE	STOP	1	2	3	4	5	6	7	8	9	10	11	12
0	0	0	S	8-bit data								STOP		
0	0	1	S	8-bit data								STOP	STOP	
0	1	0	S	8-bit data								P	STOP	
0	1	1	S	8-bit data								P	STOP	STOP
1	0	0	S	7-bit data							STOP			
1	0	1	S	7-bit data							STOP	STOP		
1	1	0	S	7-bit data							P	STOP		
1	1	1	S	7-bit data							P	STOP	STOP	

[Legend]
S : Start bit
STOP : Stop bit
P : Parity bit

(2) Clock

The transfer clock can be selected from the following two clocks using the CKE[1:0] bits in HSSCR:

- Internal clock generated by the on-chip baud rate generator
- External clock generated by an external clock baud rate generator

(3) Data transmission/reception

(a) Initialization of HSCIF (asynchronous mode)

Before transmitting/receiving data or changing the operating mode or communication format, the HSCIF should be initialized using the sample flowchart for HSCIF initialization shown in Figure 36.3.

[Notes]

Clearing the TE bit to 0 initializes HSTSR. However, HSFSR, HSFTDR, and HSFRDR contents are retained even if the TE and RE bits are cleared to 0.

The TE bit should be cleared to 0 after all transmit data has been sent and the TEND flag has been set in HSFSR. The TE bit can be cleared to 0 during transmission, but the data being transmitted will enter the marked state after clearing.
In addition, before setting the TE bit to 1 to restart the transmission, set the TFRST bit to 1 in HSFCR to reset HSFTDR.

When an external clock is used, do not stop the clock during operation or initialization. If stopped, the operation will be unreliable. Furthermore, when the baud rate generator for external clock is also to be used, be sure to make settings for it before starting initialization of the HSCIF.

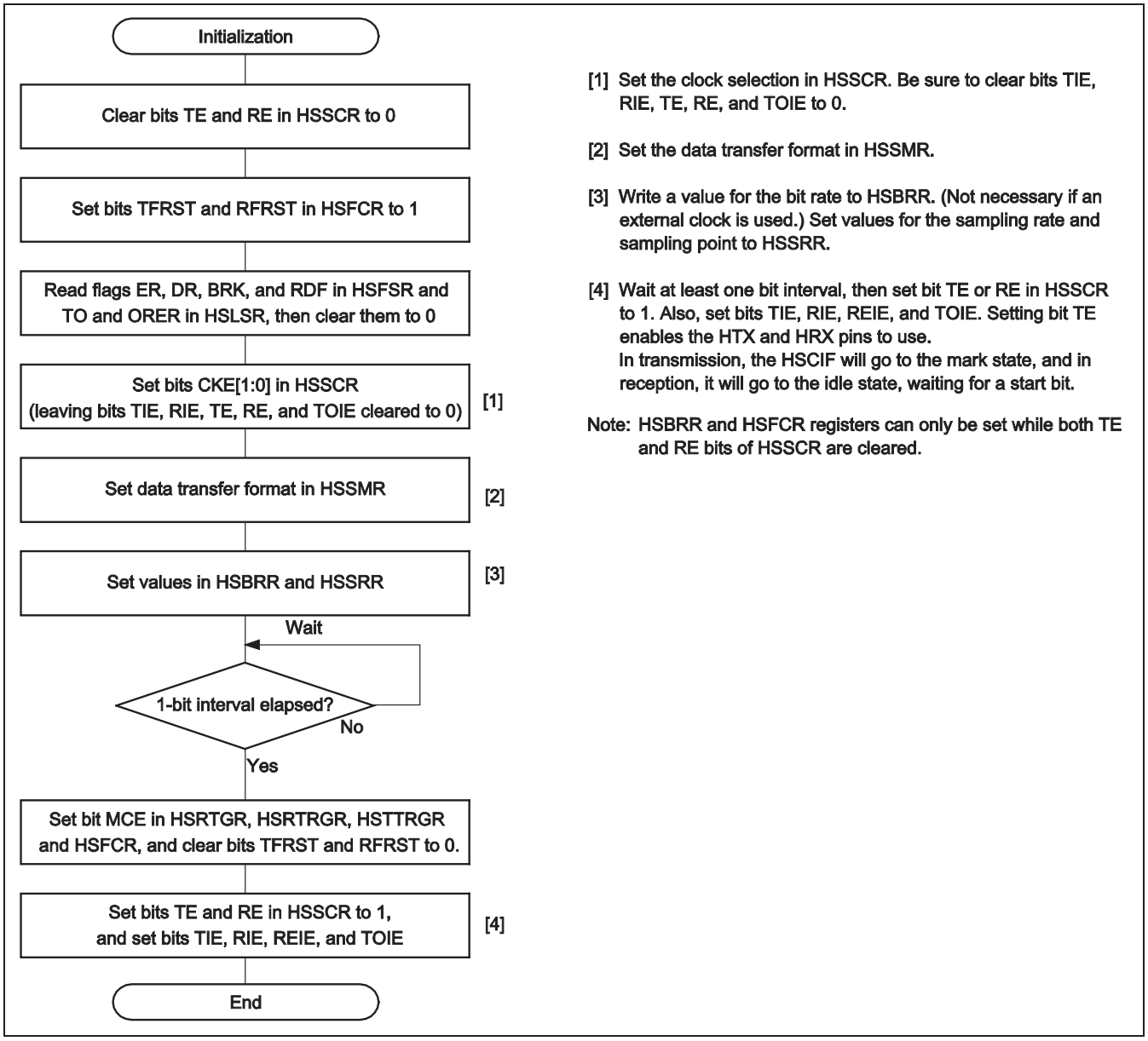


Figure 36.3 Sample Flowchart for Initializing the HSCIF

(b) Serial data transmission (asynchronous mode)

Figure 36.4 shows a sample flowchart for serial transmission.

After the HSCIF transmission operation is enabled, serial data transmission can be performed using the following procedure:

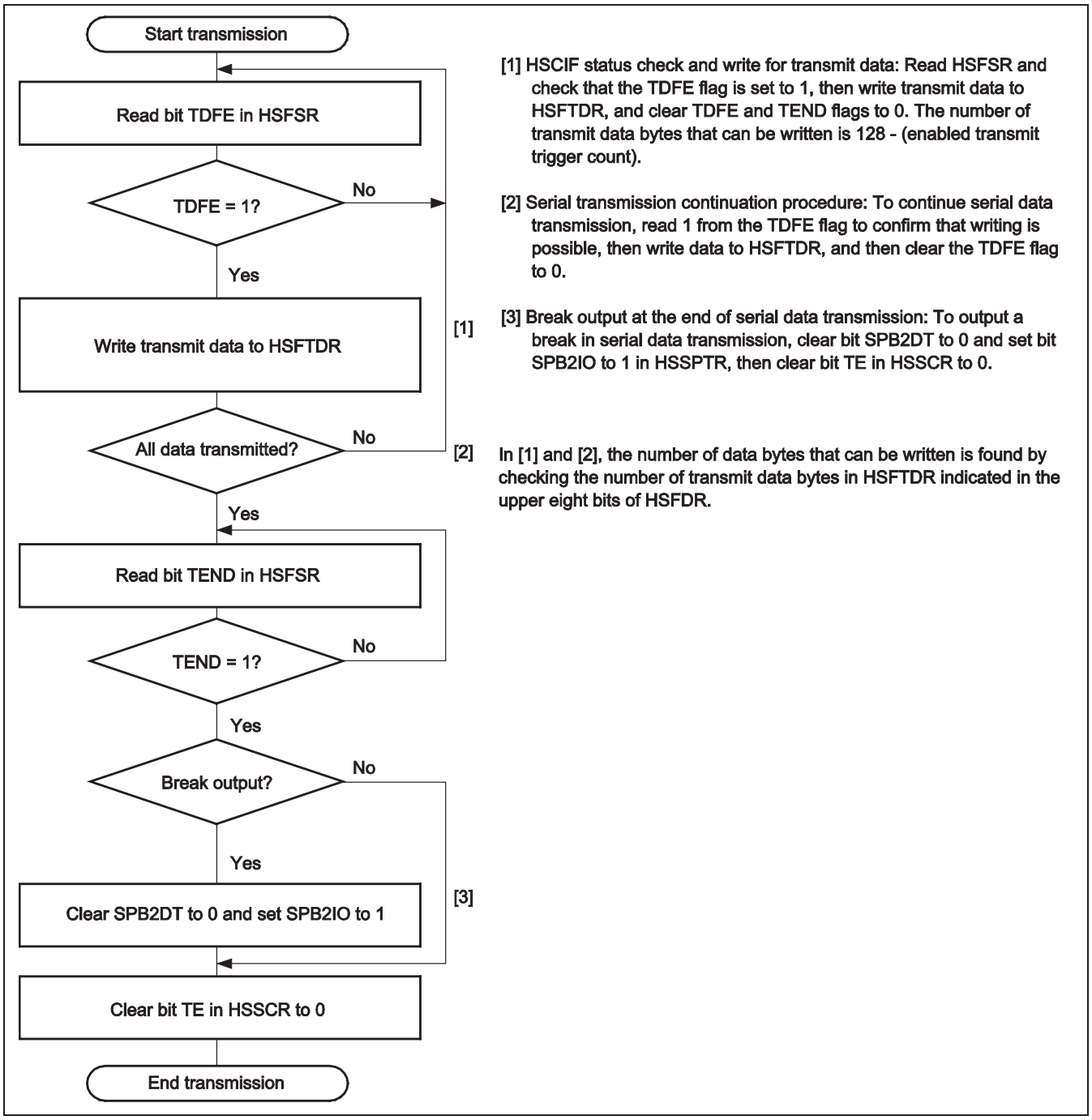


Figure 36.4 Sample Flowchart for Serial Transmission

In serial transmission, the HSCIF operates as follows:

1. When data is written to HSFTDR, the HSCIF transfers the data from HSFTDR to HSTSR and starts transmitting. Confirm that the TDFE flag in HSFSR is set to 1 before writing transmit data to HSFTDR. The number of data bytes that can be written is at least 128 – (transmit trigger count).
2. When data is transferred from HSFTDR to HSTSR and the HSCIF starts transmission, consecutive transmission is performed until there is no transmit data left in HSFTDR. When the number of transmit data bytes in HSFTDR is equal to or less than the transmit trigger count specified in HSTTRGR, the TDFE flag is set. If the TIE and TEIE bits in HSSCR are set to 1 and 0, respectively at this time, a transmit-FIFO-data-empty interrupt (TDFE) request occurs. The serial transmit data is sent from the HTX pin in the following order:
   A. Start bit: One 0-bit is output.
   B. Transmit data: 8- or 7-bit data is output in LSB-first order.
   C. Parity bit: One parity bit (even or odd parity) is output.
      A format that does not output a parity bit can also be selected.
   D. Stop bit(s): One or two 1-bit (stop bits) are output.
   E. Marked state: 1 is output continuously until the start bit that starts the next transmission is sent.
3. The HSCIF checks transmit data in HSFTDR when sending the stop bit. If there is data in it, the HSCIF transfers the data from HSFTDR to HSTSR, sends the stop bit, and then starts serial transmission of the next frame. If there is no transmit data, the HSCIF sets the TEND flag to 1 in HSFSR and sends out the stop bit, and then the marked state is entered to output 1 continuously. At this time, if the TIE and TEIE bits in HSSCR are set to 1, a transmit-end interrupt (TEND) request occurs.

Figure 36.5 shows an example of transmission in asynchronous mode.

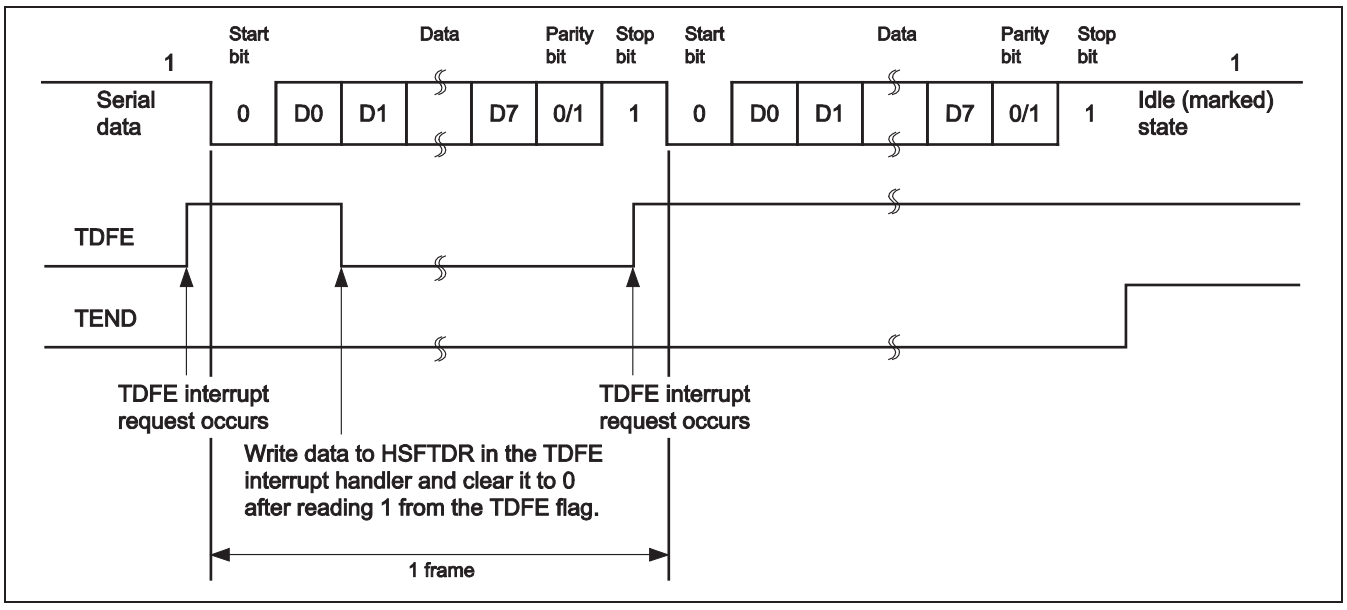


Figure 36.5 Sample HSCIF Transmission Operation (Example of 8-Bit Data with Parity and One Stop Bit)

4. When modem control is enabled, transmission can be stopped or resumed in accordance with the HCTS# input value. When HCTS# is set to 1 during transmission, the marked state is entered after one frame of data transmission is ended. Setting HCTS# to 0 restarts outputting the next transmit data from the start bit. Figure 36.6 shows an example of the operation with modem control enabled.

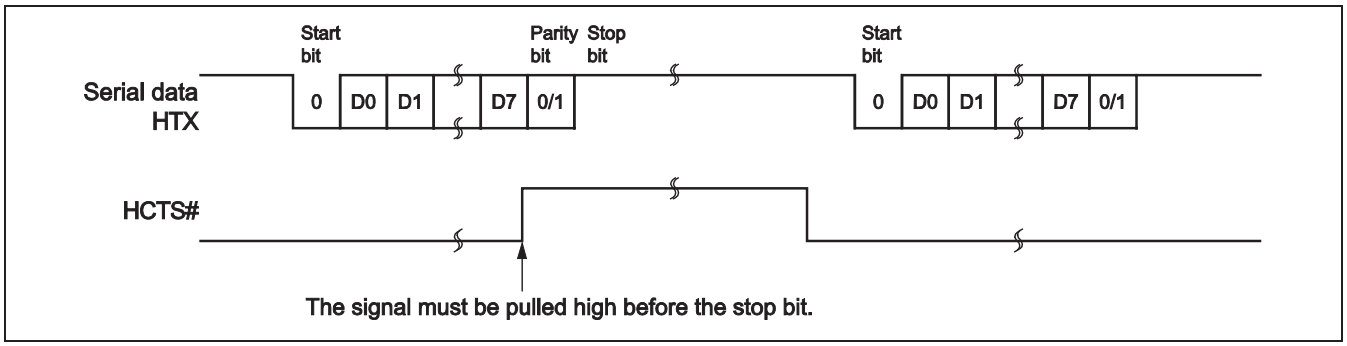


Figure 36.6 Sample Operation with Modem Control Enabled (HCTS#)

(c) Serial data reception (asynchronous mode)

Figures 36.7 and 36.8 show sample flowcharts for serial reception.

After the HSCIF reception operation is enabled, serial data reception can be performed using the following procedure:

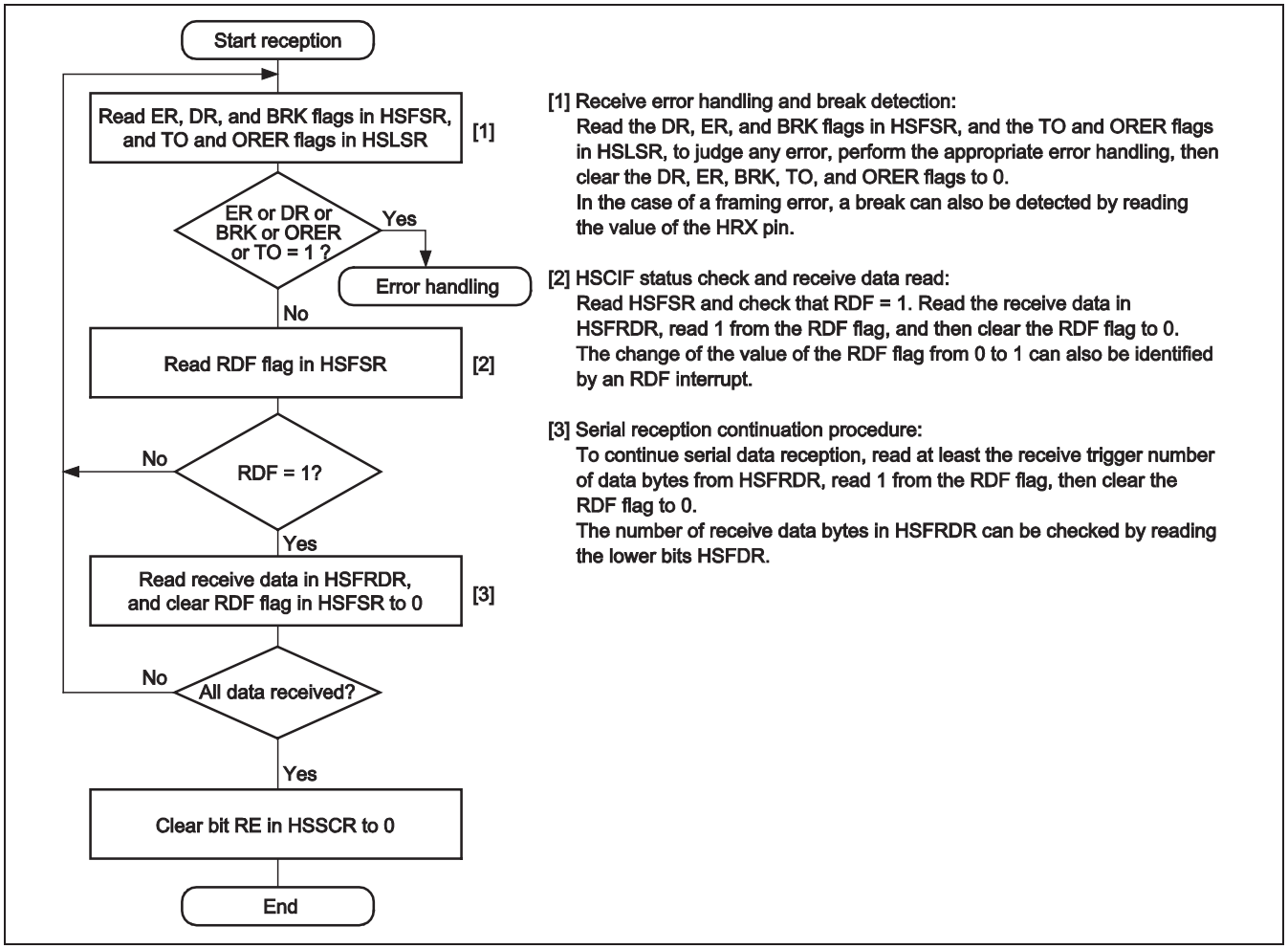
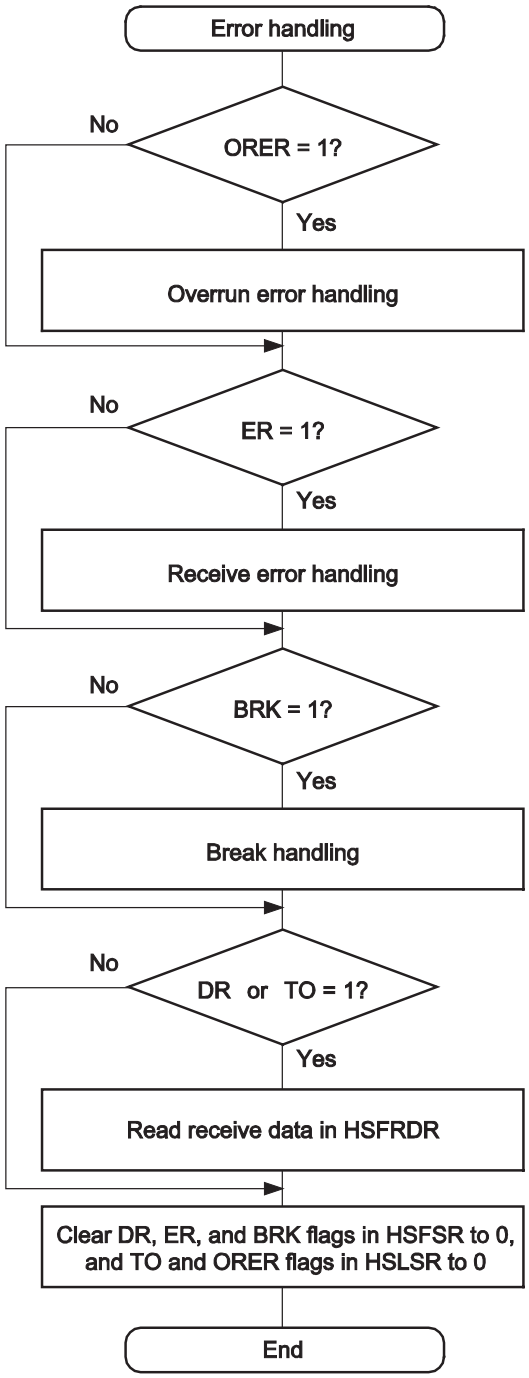


Figure 36.7 Sample Flowchart for Serial Reception (1)



Whether a framing error or parity error has occurred in the receive data that is to be read from HSFRDR can be determined by checking bits FER and PER in HSRER.

Figure 36.8 Sample Flowchart for Serial Reception (2)

In serial reception, the HSCIF operates as follows:

1. The HSCIF monitors the transmission line, and when detecting the start bit 0, it performs internal synchronization and starts reception.
2. The HSCIF stores the received data in HSRSR in LSB-to-MSB order.
3. The HSCIF receives the parity bit and stop bit.
   After receiving these bits, the HSCIF performs the following checks:
   A. Stop bit: The HSCIF checks whether the stop bit is 1.
      If there are two stop bits, it checks only the first stop bit.
   B. Receive data: The HSCIF checks that receive data can be transferred from the receive shift register (HSRSR) to HSFRDR.
   C. Overrun error: The HSCIF checks that the ORER flag is 0, indicating that no overrun error has occurred.
   D. Break state: The HSCIF checks that the BRK flag is 0, indicating that the break state is not set.
   If the HSCIF can confirm the conditions of (b), (c), and (d), it stores the receive data in HSFRDR.

Note: The HSCIF continues to receive data even when a parity error or a framing error occurs.

4. If the RDF flag changes to 1 while the RIE bit in HSSCR is 1, a receive-FIFO-data-full interrupt (RDF) request occurs.
   If the DR flag changes to 1 while the RIE bit in HSSCR is 1, a receive-data-ready interrupt (DR) request occurs.
   If the TO flag changes to 1 while the TOIE bit in HSSCR is 1, a timeout interrupt (TO) request occurs.
   If the ER flag changes to 1 while the RIE or REIE bit in HSSCR is 1, a receive-error interrupt (ER) request occurs.
   If the BRK flag changes to 1 while the RIE or REIE bit in HSSCR is 1, a break interrupt (BRK) request occurs.
   If the ORER flag changes to 1 while the RIE or REIE bit in HSSCR is 1, an overrun-error interrupt (ORER) request occurs.

Figure 36.9 shows an example of reception in asynchronous mode.

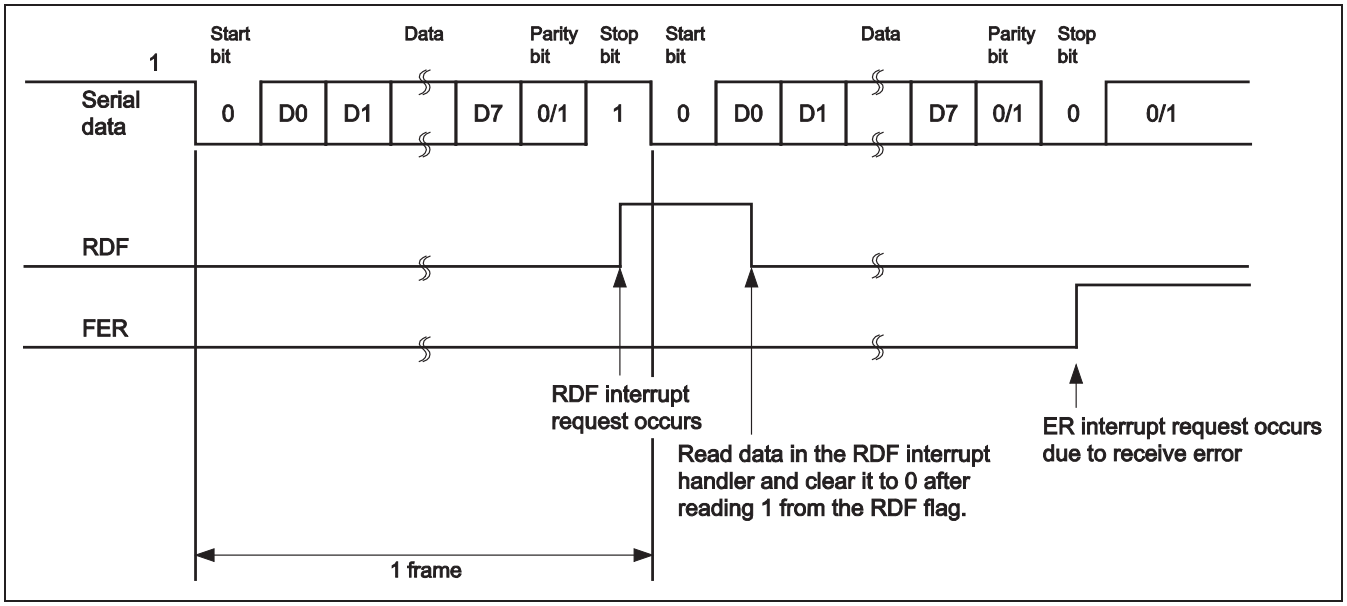


Figure 36.9 Sample HSCIF Receive Operation (Example of 8-Bit Data with Parity and One Stop Bit)

5. When modem control is enabled, the HRTS# signal is output when HSFRDR is empty. When HRTS# is 0, data can be received. When HRTS# is set to 1, the number of data bytes in HSFRDR is equal to or more than the RTS output active trigger count.

Figure 36.10 shows an example of the operation with modem control enabled.

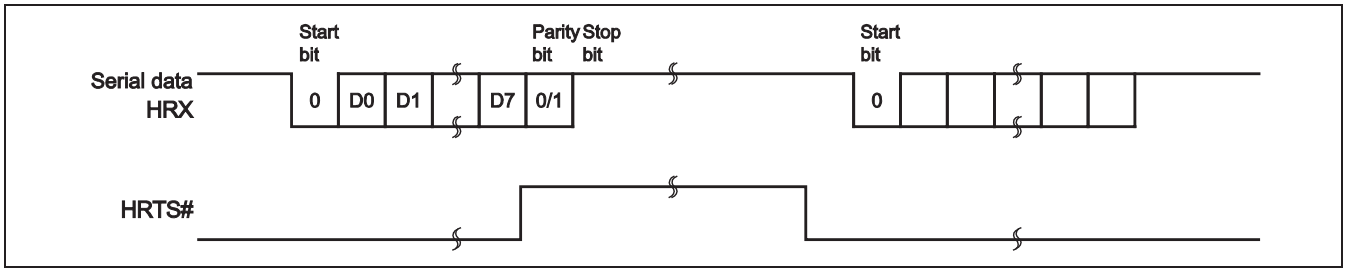


Figure 36.10 Example of the Operation with Modem Control Enabled (HRTS#)

36.3.2 HSCIF Interrupt Sources and the DMAC

If the DMAC is used for transmission/reception, set and enable the DMAC before setting the HSCIF.

Transmission interrupts and DMA transfer:
If the TDFE/TEND flag in HSFSR is set to 1 when the TDFE/TEND interrupt is enabled by the TIE bit, a TDFE/TEND interrupt request and a transmit-FIFO-data-empty DMA transfer request will occur. If the TDFE/TEND flag is set to 1 when TDFE/TEND interrupt is disabled by the TIE bit, only the transmit-FIFO-data-empty DMA transfer request will occur. (A transmit-FIFO-data-empty DMA transfer request is generated when the TDFE flag is set while TEIE is 0, or when the TEND flag is set while TEIE is 1. DMA transfer requests are not affected by the TEIE bit.)

When TDFE/TEND interrupt requests are enabled, the interrupt requests are cleared by the DMAC regardless of the interrupt handling program.

Reception interrupts and DMA transfer:
If the RDF/DR flag in HSFSR is set to 1 when RDF/DR interrupt is enabled by the RIE bit, an RDF/DR interrupt request occurs. If the RDF/DR flag is set to 1, a receive-FIFO-data-full DMA transfer request occurs. If the RDF/DR flag is set to 1 when RDF/DR interrupt is disabled by the RIE bit, and only a receive-FIFO-data-full DMA transfer request occurs and DMAC can be activated to perform data transfer.

Setting the RIE bit in HSSCR to 0 and the REIE it to 1 generates the ER/BRK/ORER interrupt requests without generating RDF/DR interrupt requests. When the BRK flag in HSFSR or the ORER flag in HSLSR is set to 1, BRK/ORER interrupt requests occur.

If the TO flag is set to 1 in HSLSR when TO interrupts are enabled by the TOIE bit, TO interrupt requests occur.

When DR/TO interrupt requests are enabled to be issued, interrupt requests generated by the DR flag are cleared by the DMAC regardless of the interrupt handling program, however, those generated by the TO flag are not cleared by the DMAC. Therefore, the TO flag interrupt requests need to be cleared with the interrupt handling program. (The DR and TO flags are set at the same time, but cleared separately.)

Table 36.6 HSCIF Interrupt Sources

Interrupt Source	DMAC Activation
Interrupts generated by receive error flag (ER)	Disabled
Interrupts generated by receive-FIFO-data-full (RDF), receive-data-ready (DR) or timeout (TO)	Enabled
Interrupts generated by break (BRK) or overrun error (ORER)	Disabled
Interrupts generated by transmit FIFO data empty (TDFE)	Enabled

36.4 Usage Notes

Note the following on use of the HSCIF.

(1) Break detection and operation

Break signals can also be detected by reading the HRX pin value directly when a framing error (FER) is detected. In the break state, the input values from the HRX pin are all 0s. So, the parity error flag (PER) may be set after the FER flag is set to 1.

Although the HSCIF stops receive data transfer to HSFRDR after detecting a break, it continues data reception.

(2) Sending a break signal

The input/output condition and level of the HTX pin are determined by the SPB2IO and SPB2DT bits in HSSPTR. This enables to send a break signal.

The pin does not function as the HTX pin from the initialization of the serial transmitter to setting of the TE bit (enabling transmission). In this period, the marked state is substituted by the value of the SPB2DT bit. Therefore, the SPB2IO and SPB2DT bits should be set to 1 (designating output and high level) beforehand.

To send a break signal during serial transmission, clear the SPB2DT bit to 0 (low level), and then clear the TE bit to 0 (halting transmission). When the TE bit is cleared, the transmitter is initialized regardless of the current transmission state, and the HTX pin outputs 0.

(3) Data sampling timing and reception margin in asynchronous mode

The HSCIF operates on the base clock with a frequency multiplied by the number which is set as a sampling rate for the bit rate.

In reception, the HSCIF performs the internal synchronization by sampling the falling edge of the start bit using the base clock. In addition, the HSCIF takes receive data at the rising edge of the S/2 pulse (when S is an even number) or (S+1)/2 pulse (when S is an odd number) on the base clock when sampling rate is S.

Figure 36.11 shows the timing of this operation when S = 16.

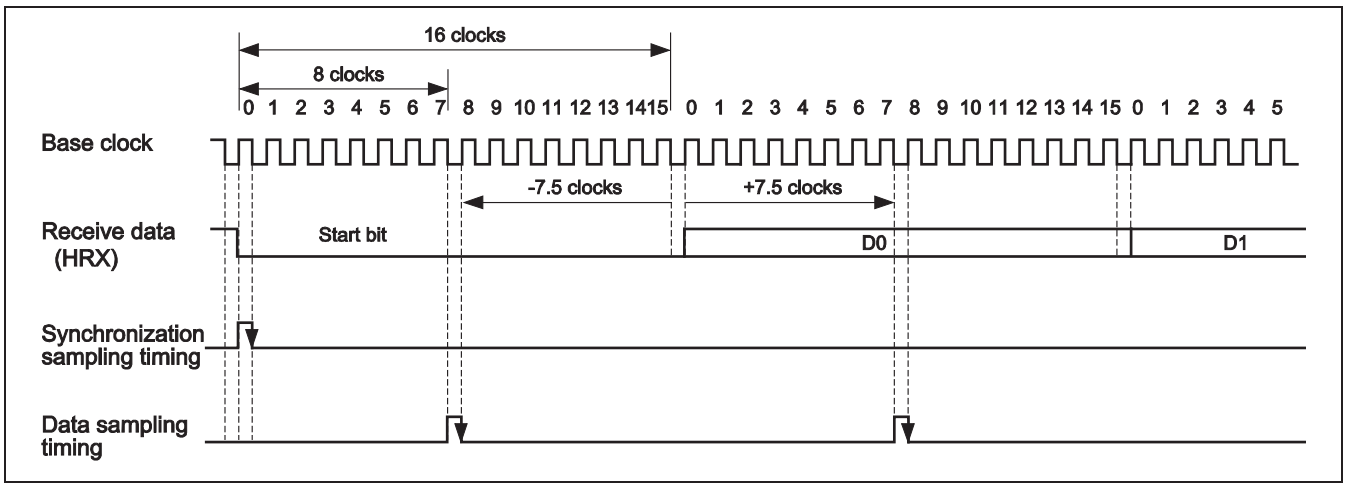


Figure 36.11 Timing Chart of Receive Data Sampling

The reception margin in asynchronous mode is given by expression (1).

$$M = \left| (0.5 - \frac{1}{2N}) - (L - 0.5) F - \frac{|D - 0.5|}{N} (1 + F) \right| \times 100\% \quad \text{Expression (1)}$$

M: Receive margin (%)

N: Ratio of bit rate to clock (N = sampling rate)

D: Clock duty (D = 0 to 1.0)

L: Frame length (L = 9 to 12)

F: Absolute value of clock frequency deviation

Assuming F = 0, D = 0.5 and sampling rate = 16 for expression (1), the reception margin obtained with expression (2) is 46.875% as shown below:

Assuming D = 0.5 and F = 0

M = (0.5 – 1/(2 × 16)) × 100%

= 46.875% ……expression (2)

This is a theoretical value. A reasonable margin allowed in system designs is 20% to 30%.

(4) Reception margin and baud rate error

The value of 46.875% obtained by the above expression (2) indicates the reception margin when the baud rate error is 0 (F = 0). If there is no error in the reception and transmission baud rates, reception is possible even with misalignment of approx. 1/2 bit. If there is an error in the reception and transmission baud rates, the errors are accumulated up to the stop bit reception, which reduces the reception margin. The allowable baud rate error can be obtained by modifying the F in expression (1). When D = 0.5:

F = {(15/32 – M)/(L – 0.5)} × 100 (%)……expression (3)

By using expression (3), the relationship between the allowable error and reception margin with the frame length = 12 can be summarized as follows:

Allowed Error (%)	Reception Margin (%)
4.07	0
3.64	5
3.20	10
2.33	20
1.46	30

(5) Usage method of SRHP bits

The method for using the SRHP bits in the sampling rate register is described below.

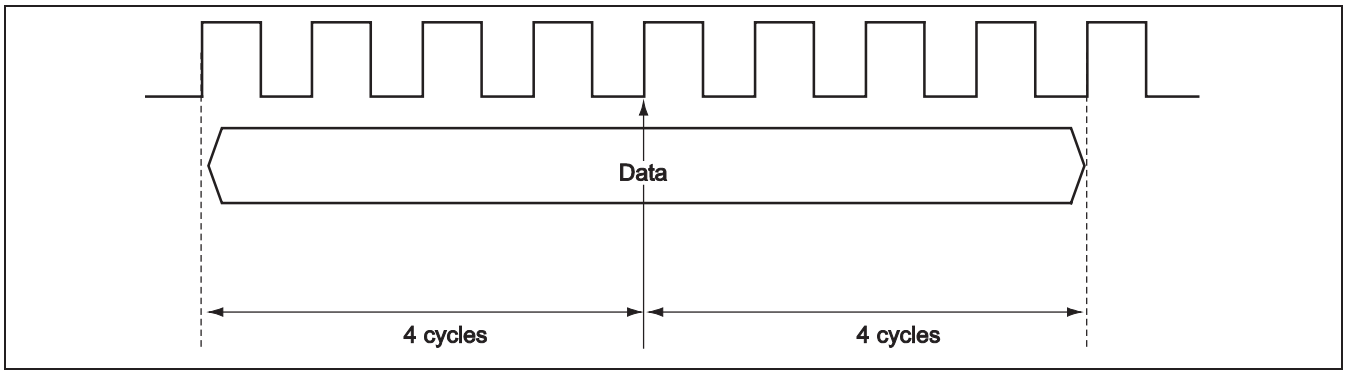


Figure 36.12 Sampling with Invalid SRHP Bits

Figure 36.12 shows a sampling example in which the SRHP bits are invalid (sampling rate = 8). In this case, the HSCIF samples data at half of the sampling rate, which is at the rising edge of the fourth pulse of the clock. This allows a setup margin and hold margin of 50% each to be provided.

However, if the ratio between the baud rate and sampling clock is not 1:1, either the setup margin or hold margin is omitted in data reception of a single frame. If the setup margin is omitted, the hold margin increases. On the other hand, if the hold margin is omitted, the setup margin increases. Figures 36.13 and 36.14 show examples.

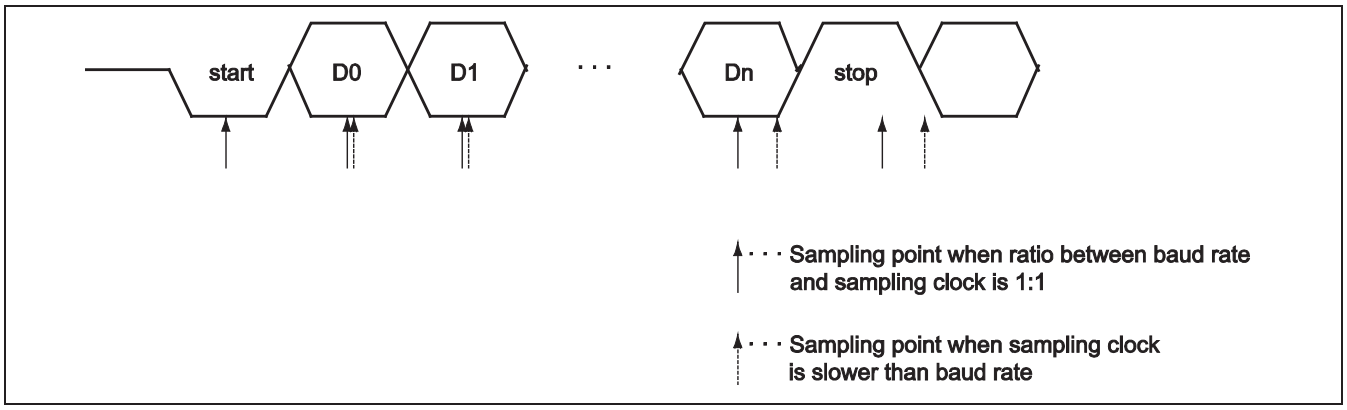


Figure 36.13 Sampling Point with Sampling Clock Slower Than Baud Rate

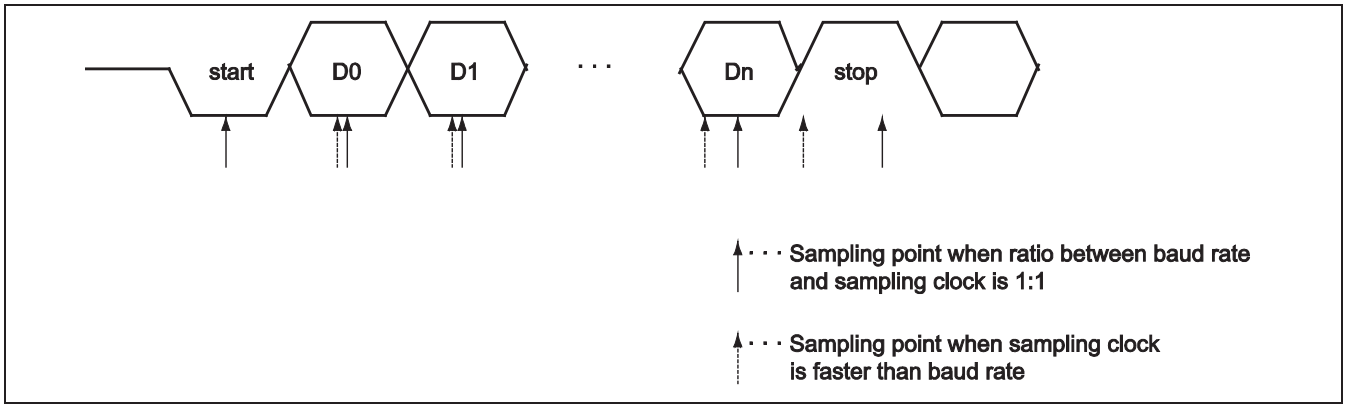


Figure 36.14 Sampling Point with Sampling Clock Faster Than Baud Rate

The ratio between the baud rate and sampling clock can be used to determine which margin among the setup margin and hold margin is to be omitted and which is to be increased. Based on this, the margin within a single frame can be increased by intentionally increasing the margin to be omitted in advance. The sampling point can be moved by setting a value in the SRHP bits. Figure 36.15 shows an example.

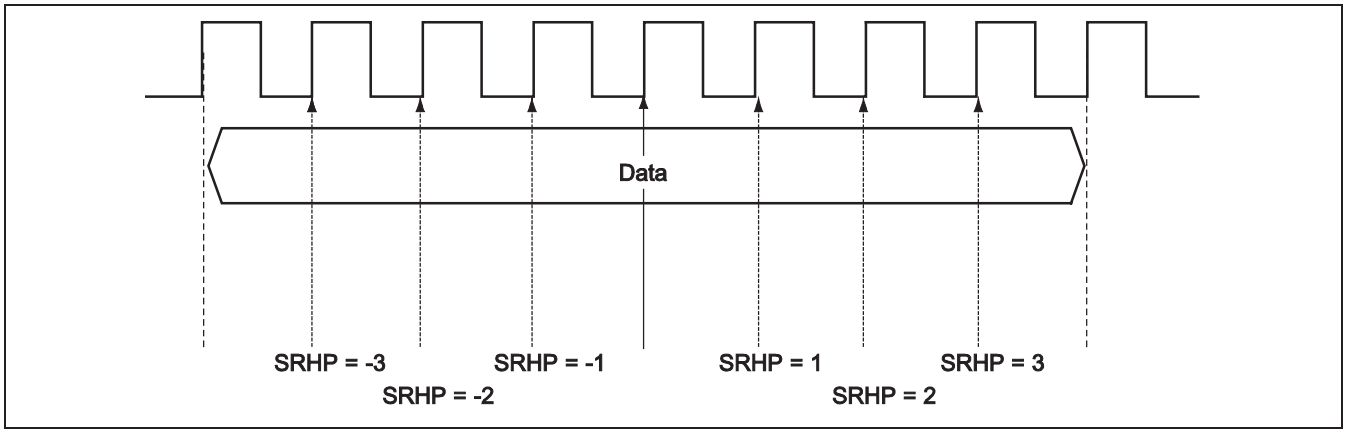


Figure 36.15 Sampling Point Moved by SRHP Bits

(6) Sampling rate and bit rate settings and respective margin

To set the baud rate in the HSCIF, in addition to setting the clock division ratio, the two registers, bit rate register (HSBRR) and sampling rate register (HSSRR), need to be set. These registers must be set so that the margin calculated by expression (1) in section 36.4 (3) will be a sufficient value.

The bit rate error is small when the value obtained by dividing the divided clock frequency used in the HSCIF with the sampling rate is near the desired baud rate. If there are many combinations of bit rate and sampling rate with the same bit rate error, choosing a combination with a large sampling rate provides a large margin. This is because when the bit rate error is constant in expression (1) in section 36.4 (3), that is, when the "absolute value of clock frequency deviation (F)" is constant, the margin (M) increases in accordance with the sampling rate (N).

If the sampling rate is made larger in a combination of bit rate and sampling rate with different bit rate errors, the bit rate error is increased. Accordingly, the "absolute value of clock frequency deviation (F)" on the right side in expression (1) in section 36.4 (3) gets larger and the margin (M) smaller.

Refer to the following procedure when selecting the sampling rate and bit rate settings.

1. Obtain the bit rate with the smallest bit rate error for sampling rates from 8 to 32.
2. Using expression (1) in section 36.4 (3), calculate the margin for each combination of sampling rate and bit rate which was obtained in step 1.
3. Select the combination with the largest margin among the combinations of sampling rate and bit rate.

36.5 Baud Rate Generator for External Clock (BRG)

36.5.1 Overview

The HSCIF incorporates a baud rate generator for external clock (abbreviated as BRG, hereafter). The BRG supplies a sampling clock (BRGCLK) to the HSCIF core by dividing the external clock SC_CLK (selectable between SCIF_CLK and ZSϕ) by 1 to $2^{16} - 1$. In addition, the BRG switches the output between the external clock HSCK and divided clock.

36.5.2 Block Descriptions

Figure 36.16 shows a block diagram of the BRG.

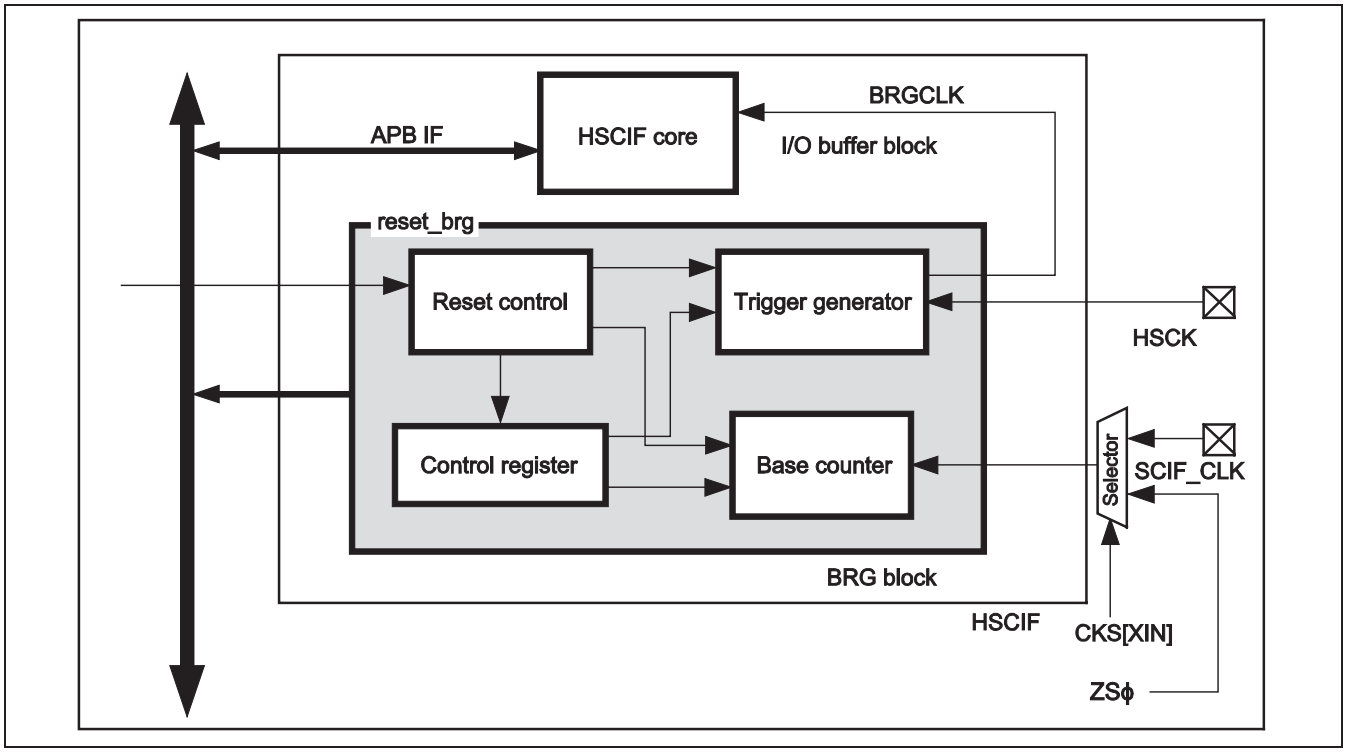


Figure 36.16 BRG Block Diagram

(1) Reset controller:

The reset controller handles resetting the control register, base counter, and trigger generator.

(2) Control register:

The control register has the frequency division register and clock select register.

(3) Base counter:

The base counter is a 16-bit CLK synchronization counter that is used to determine the timing for generating a frequency divided clock.

(4) Trigger generator:

The trigger generator generates rising-edge/falling-edge triggers for a frequency divided clock with the timing according to values of the frequency division register and base counter. The triggers are used to generate the frequency divided clock. In addition, the trigger generator switches the output between the HSCK (external clock input) and frequency divided clock.

36.5.3 BRG Register Configuration

Table 36.7 shows the registers in the BRG block.

Table 36.7 List of Registers

Ch. No.	Name	Code	R/W	Initial Value	Address	Access Size
0	Frequency division register 0	DL	R/W	H'00	H'E62C 0030	16
	Clock select register 0	CKS	R/W	H'00	H'E62C 0034	16
1	Frequency division register 1	DL	R/W	H'00	H'E62C 8030	16
	Clock select register 1	CKS	R/W	H'00	H'E62C 8034	16
2	Frequency division register 2	DL	R/W	H'00	H'E62D 0030	16
	Clock select register 2	CKS	R/W	H'00	H'E62D 0034	16

36.5.3.1 Frequency Division Register (DL)

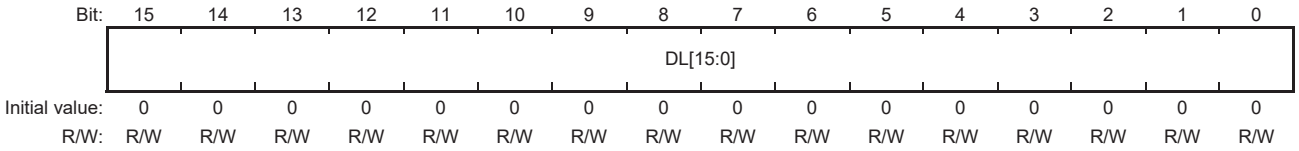
This register specifies the value of frequency division for the frequency divided clock generated by the BRG.

This register supports a 16-bit binary format that allows specifying a value in the range of 1 to 65535.

Setting all 0s in this register makes the BRG output the frequency divided clock at the low level.

The value of frequency division is given by the following formula:

The value of frequency division = (clock input frequency)/(required baud rate × sampling rate)



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	DL[15:0]	All 0	R/W	Specifies a division value of frequency clock generated in BRG. The setting value is enabled in the range of 1 to 65535.

Table 36.8 and Table 36.9 show how to use the baud rate generator with a 3.6864-MHz crystal resonator, and a 26-MHz crystal resonator.

Table 36.8 Baud Rate (3.6864-MHz clock)

Baud Rate	Value of Frequency Division	Sampling Rate	Error Rate*
50	4608	16	—
75	3072	16	—
110	4189	8	-0.002
134.5	1713	16	0.001
150	1536	16	—
300	768	16	—
600	384	16	—
1200	192	16	—
1800	128	16	—
2000	123	15	0.098
2400	96	16	—
3600	64	16	—
4800	48	16	—
7200	32	16	—
9600	24	16	—
14400	16	16	—
19200	12	16	—
38400	6	16	—
76800	3	16	—
115200	2	16	—

Note: * "—" Indicates that the error rate is 0.

Table 36.9 Baud Rate (26-MHz clock)

Baud Rate	Value of Frequency Division	Sampling Rate	Error Rate*
9600	129	21	0.025
19200	52	26	-0.160
38400	26	26	-0.160
57600	15	30	-0.309
115200	9	25	-0.309
230400	4	28	-0.756
460800	2	28	-0.756
921600	1	28	-0.756
1843200	1	14	-0.756
3250000	1	8	—

Note: * "—" Indicates that the error rate is 0.

36.5.3.2 Clock Select Register (CKS)

This register switches the output between the frequency divided clock and specifies a source clock for the external baud rate.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CKS	XIN	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	CKS	0	R/W	This bit switches the output between the frequency divided clock (SC_CLK) and external clock (HSCK). 0: Selects the frequency divided clock. 1: Selects the external clock.
14	XIN	0	R/W	Selects the baud rate generator clock source for the external clock between SCIF_CLK and ZSϕ. 0: Selects the external clock (SCIF_CLK). 1: Selects the internal clock (ZSϕ).
13 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

36.5.4 Restrictions in BRG

(1) Notes on setting frequency division register

1. For the initial setting of the register after a reset, at least one bit of waiting period is required to secure the clock stabilization time.
   (Example) One bit period when DL = 2
   3.68 (MHz) × 1/2 × 1/16 = 0.115 (MHz) → 8695 (ns)

2. For modifying the register value after the setting stated in <1> above, at least one bit of waiting period at the maximum bit rate (DL = '65535') is required.
   The HSCIF registers and BRG registers should be set as the following table:

- Asynchronous mode (SC_CLK external input)

HSCIF		BRG	
Register Name	**Setting Value**	**Register Name**	**Setting Value**
HSSCR.CKE[1:0]	B'10	CKS	H'0000
		DL	H'1 to H'FFFF

- Asynchronous mode (HSCK external input)

HSCIF		BRG	
Register Name	**Setting Value**	**Register Name**	**Setting Value**
HSSCR.CKE[1:0]	B'10	CKS	H'8000
		DL	Don't care

3. The register settings for the baud rate generator for external clock should be made before starting initialization of the HSCIF.

37. I2C Bus Interface (I2C)

37.1 Overview

37.1.1 Features

Five I2C bus interfaces conformant with the Philips Semiconductors (now NXP Semiconductors) I2C bus (Inter-IC bus) specification. However, the configuration of registers that control the I2C bus differs partly from the NXP Semiconductors register configuration. The I2C bus interface has the following features. Note that "module clock (MOD_CLK)" refers to the peripheral module clock (HPϕ) in this section.

- The I2C interfaces support the I2C bus specification from NXP Semiconductors
- Multi-master compatible
- Seven- or ten-bit address compatible master
- Seven-bit slave address
- Fast mode compatible
- Variable clock frequencies

Figure 37.1 shows a block diagram of the I2C bus interface.

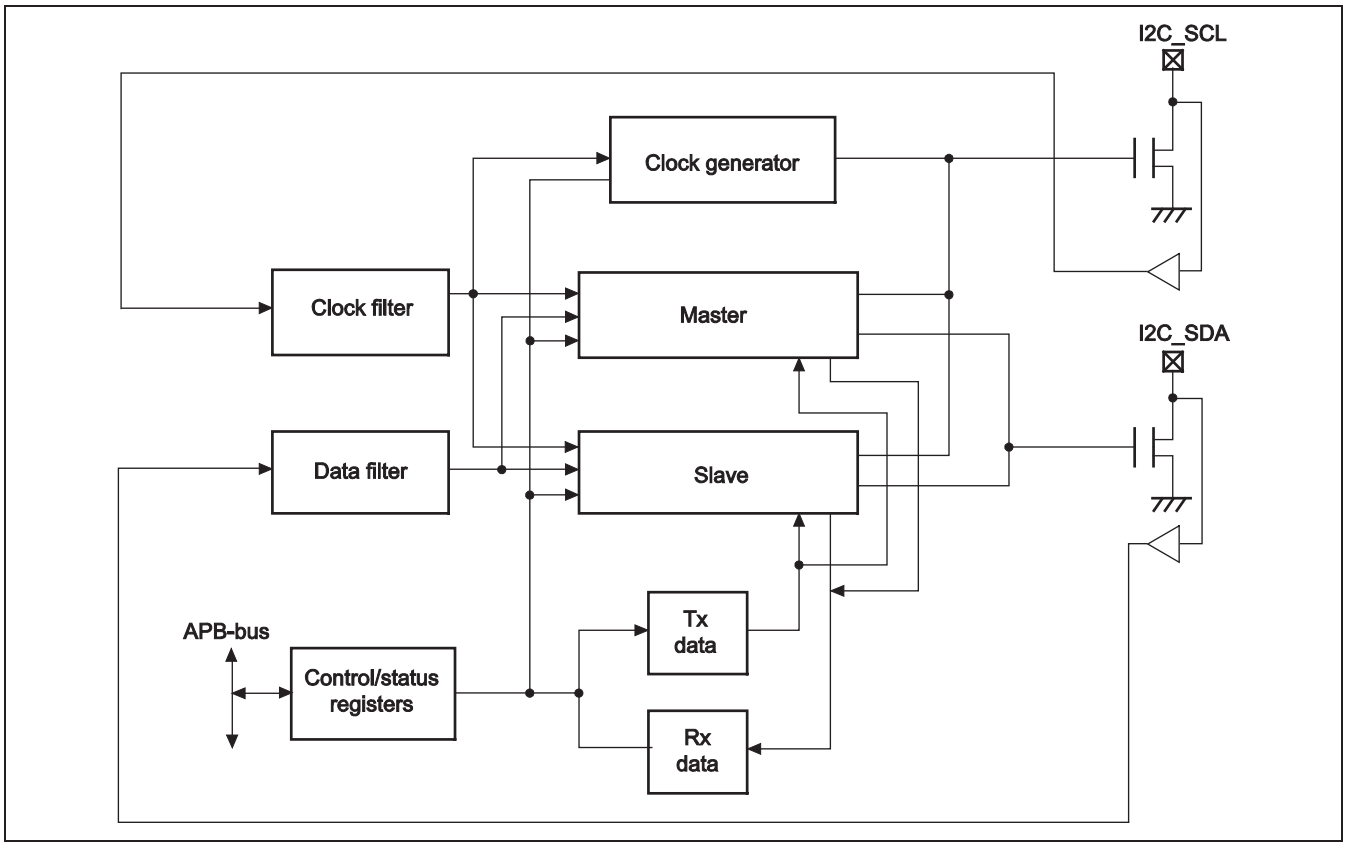


Figure 37.1 Block Diagram of I2C Bus Interface

37.1.2 Input/Output Pins

Table 37.1 lists the pins used in the I2C bus interface.

Table 37.1 I2C Bus Interface

Channel Number	Pin Name	I/O	Function	Output Buffer Type*
0	SCL	I/O	SCL: I2C serial clock input/output pin SDA: I2C serial data input/output pin	LVTTL
	SDA			
1	SCL			LVTTL
	SDA			
2	SCL			LVTTL
	SDA			
3	SCL			LVTTL
	SDA			
4	SCL			LVTTL
	SDA			

Note: * Output buffer type: "LVTTL" is low level drive only LVTTL buffer. LVTTL assigned channel pins are 3.3 V I/O.

The I2C buffer in this LSI is not compliant with the 5V-input. When turning off the I/O power source (3.3 V) of this LSI, turn off the power source of the pull-up resistors connected to the I2C pins.

37.2 Register Descriptions

The base address for each channel of registers of the I2C bus interface is as follows:

- I2C0: H'E650_8000
- I2C1: H'E651_8000
- I2C2: H'E653_0000
- I2C3: H'E654_0000
- I2C4: H'E652_0000

Each channel of the I2C bus interface has the registers below.

Table 37.2 Register Configuration (1)

Register Name	Abbreviation	R/W	Offset Address from Base Address	Size
Slave control register	ICSCR	R/W	H'00	32
Master control register	ICMCR	R/W	H'04	32
Slave status register	ICSSR	R/(W)*1	H'08	32
Master status register	ICMSR	R/(W)*2	H'0C	32
Slave interrupt enable register	ICSIER	R/W	H'10	32
Master interrupt enable register	ICMIER	R/W	H'14	32
Clock control register	ICCCR	R/W	H'18	32
Slave address register	ICSAR	R/W	H'1C	32
Master address register	ICMAR	R/W	H'20	32
Receive data register	ICRXD	R	H'24	32
Transmit data register	ICTXD	W	H'24	32
Clock control register 2	ICCCR2	R/W	H'28	32
SCL mask control register	ICMPR	R/W	H'2C	32
SCL high control register	ICHPR	R/W	H'30	32
SCL low control register	ICLPR	R/W	H'34	32

Notes: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted.
Values read from addresses other than those listed above are undefined.
Although the actual register name and its abbreviation have channel number as a suffix respectively, it is omitted in this section.

1. Only 0 can be written to bits 4 to 0 to clear the flags.
2. Only 0 can be written to bits 6 to 0 to clear the flags.

Table 37.3 Register Configuration (2)

Name	Abbreviation	Power-On Reset	Module Standby
Slave control register	ICSCR	H'0000 0000	Retained
Master control register	ICMCR	H'0000 0000*	Retained
Slave status register	ICSSR	H'0000 0000	Retained
Master status register	ICMSR	H'0000 0000	Retained
Slave interrupt enable register	ICSIER	H'0000 0000	Retained
Master interrupt enable register	ICMIER	H'0000 0000	Retained
Clock control register	ICCCR	H'0000 0000	Retained
Slave address register	ICSAR	H'0000 0000	Retained
Master address register	ICMAR	H'0000 0000	Retained
Receive data register	ICRXD	H'0000 0000	Retained
Transmit data register	ICTXD	—	—
Clock control register 2	ICCCR2	H'0000 0000	Retained
SCL mask control register	ICMPR	H'0000 0000	Retained
SCL high control register	ICHPR	H'0000 0000	Retained
SCL low control register	ICLPR	H'0000 0000	Retained

Note: * Bits 30, 29, 22, 21, 14, 13, 6, and 5 are undefined.

37.2.1 Slave Control Register (ICSCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	SDBS	SIE	GCAE	FNA
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 4	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
3	SDBS	0	R/W	Slave Data Buffer Select This bit is used to select the data buffer. Select the single-buffer mode supported in this module. When this bit is set to 1, the single-buffer mode is selected. SCL will be held low from the timing when the receive data register acquires the data packet until the SDR flag is cleared. 0: Setting prohibited 1: Single-buffer mode
2	SIE	0	R/W	Slave Interface Enable This bit must be set for the slave operation. If this bit is low, the slave interface is reset.
1	GCAE	0	R/W	General Call Acknowledgement Enable When slave devices are to issue an acknowledgement in response to a general call address sent from a master, this bit must be set to 1.
0	FNA	0	R/W	Forced Non Acknowledgement In the slave receive mode, the level of this bit is sent to the transmitting device as the acknowledge signal. This bit is set to 0 during the period that the data packet is being received, and set to 1 on completion of data reception. Forced non acknowledgement is returned to the master during slave reception. When the slave has received the last byte of data in a data packet, the slave communicates with the master by sending a NACK, meaning that the acknowledgement is not driven. The master issues a stop on the bus after receiving a NACK. The setting of this bit does not affect the acknowledgement of the slave address.

37.2.2 Slave Status Register (ICSSR)

Bits 0 to 4 among the status bits in the slave status register are cleared by writing 0 to the respective status bit positions. The individual bits are held 1 until 0 is written to (other than the GCAR and STM bits).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	GCAR	STM	SSR	SDE	SDT	SDR	SAR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6	GCAR	0	R	General Call Address Received Indicates that the address received from the bus is a general call address (H'00). This status bit does not cause an interrupt. This bit is automatically cleared by hardware when the SIE bit (bit 2 in the slave control register) is set to 0 or when the SSR bit (bit 4 in this register) is set to 1.
5	STM	0	R	Slave Transmit Mode Indicates whether the current slave transmit mode is read or write. When this bit is set to 0, the mode is write (slave reception). When this bit is set to 1, the mode is read (slave transmission). This status bit does not cause an interrupt. This bit is automatically cleared by hardware when the SIE bit (bit 2 in the slave control register) is set to 0 or when the SSR bit (bit 4 in the slave status register) is set to 1.
4	SSR	0	R/W*	Slave Stop Received A stop condition has been output on the bus. This status bit becomes active after the rising edge of SDA during reception of a stop bit.
3	SDE	0	R/W*	Slave Data Empty Indicates that data to be transmitted has been loaded into the shift register. At the start of byte data transmission, the contents of the ICTXD register are loaded into a shift register ready for outputting data on the bus. This status bit indicates that data has been loaded and the ICTXD register is again ready for further data. This status bit becomes active on the falling edge of SCL before reception of the first data bit. During the single-buffer mode, this bit must be reset every time new data has been written to ICTXD. This is because the slave holds SCL low to stop the bus while this bit is set to 1 even if a slave transmission cycle is started.
2	SDT	0	R/W*	Slave Data Transmitted A byte of data has been transmitted to the bus. This bit becomes active after the falling edge of SCL during reception of the last data bit.

Bit	Bit Name	Initial Value	R/W	Description
1	SDR	0	R/W*	Slave Data Received A byte of data has been received from the bus and is ready for reading from the receive data register. This bit becomes active after the falling edge of SCL during reception of the last data bit. During the single-buffer mode, this bit must be reset after data has been read from the ICRXD register. When SDBS is set to 1, SCL will be held low from the timing when the receive data register acquires the data packet until the SDR flag is cleared.
0	SAR	0	R/W*	Slave Address Received Indicates that the slave has recognized its own address on the bus (defined by the contents of the slave address register). If the general call acknowledgement enable bit is enabled in the slave control register, then this status bit is also set to 1 even if the address on the bus is a general call address. In this case, the GCAR bit in this register is used to determine whether or not the address is a general call address. The STM bit indicates whether the access is read (high) or write (low). This status becomes active after the falling edge of SCL during reception of the last address bit. The slave holds the SCL signal low from the start of the ACK phase until the software resets this status bit.

Note: * This bit can be read from or written to. Writing 0 clears this bit to 0 and writing 1 is ignored.

37.2.3 Slave Interrupt Enable Register (ICSIER)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	SSRE	SDEE	SDTE	SDRE	SARE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
4	SSRE	0	R/W	Slave Stop Received Interrupt Enable 0: Disables the SSR interrupt. 1: Enables the SSR interrupt.
3	SDEE	0	R/W	Slave Data Empty Interrupt Enable 0: Disables the SDE interrupt. 1: Enables the SDE interrupt.
2	SDTE	0	R/W	Slave Data Transmitted Interrupt Enable 0: Disables the SDT interrupt. 1: Enables the SDT interrupt.
1	SDRE	0	R/W	Slave Data Received Interrupt Enable 0: Disables the SDR interrupt. 1: Enables the SDR interrupt.
0	SARE	0	R/W	Slave Address Received Interrupt Enable 0: Disables the SAR interrupt. 1: Enables the SAR interrupt.

37.2.4 Slave Address Register (ICSAR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	SADD0_6	SADD0_5	SADD0_4	SADD0_3	SADD0_2	SADD0_1	SADD0_0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6 to 0	SADD0_6 to SADD0_0	All 0	R/W	Slave Address This is the unique 7-bit address allocated to the slave on the I2C bus. The slave interface compares this address with the first seven bits transmitted as the slave address, at the beginning of a data packet transmission.

37.2.5 Master Control Register (ICMCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	—	—	0	0	0	0	0	0	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	MDBS	FSCL	FSDA	OBPC	MIE	TSBE	FSB	ESG
Initial value:	0	—	—	0	0	0	0	0	0	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0, except bits 30, 29, 22, 21, 14, and 13, in which case, initial value is undefined.	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
7	MDBS	0	R/W	Master Data Buffer Select This bit is used to select the data buffer mode. Select the single-buffer mode supported in this module. When this bit is set to 1, the single-buffer mode is selected. SCL will be held low from the timing when the receive data register acquires the data packet until the MDR flag is cleared. 0: Setting prohibited 1: Single-buffer mode
6	FSCL	—	R/W	Forced SCL This bit controls the status of the I2C_SCL pin (reading reflects the current status of the I2C_SCL pin). When the OBPC bit is set, this bit directly controls the SCL line on the bus. During a read cycle, the level on this bit (which includes the reset level) will change depending on the level on I2C_SCL since it directly reflects the level on the I2C_SCL.
5	FSDA	—	R/W	Forced SDA This bit controls the status of the I2C_SDA pin (reading reflects the busy status level on the I2C bus). When the OBPC bit is set, then this bit directly controls the SDA line on the bus. During a read cycle, the level on this bit (which includes the reset level) will show the busy status of the I2C bus (1 for busy; 0 for not busy).
4	OBPC	0	R/W	Override Bus Pin Control When this bit is set to 1, the FSDA and FSCL bits in this register control SDA and SCL directly. This mode is used for testing purposes only.
3	MIE	0	R/W	Master Interface Enable When this bit is set to 1, the master interface is enabled. This bit is automatically cleared to 0 when this interface loses in arbitration of bus mastership. If 0 is not subsequently written to the bit, the value of the bit is restored to 1 on detection of a STOP condition on the I2C bus, and data transmission is retried. Regarding the state following a loss in arbitration of bus mastership, see the description of the MAL bit in ICMSR.

Bit	Bit Name	Initial Value	R/W	Description
2	TSBE	0	R/W	Start Byte Transmission Enable When this bit is set to 1, if the master issues a START or a repeated START condition, it continues by transmitting a start byte (01H) over the bus. The start byte is used for interfacing with slower microcontrollers that have I2C bus interfaces.
1	FSB	0	R/W	Forced Stop onto the Bus When this bit is set to 1, the master transmits a STOP condition on the bus at the end of the current transfer. If ESG is also set, the master immediately transmits a START condition and begins transmitting a new data packet. If ESG is not set, the master enters the idle state.
0	ESG	0	R/W	Enable Start Generation When this bit is set to 1, the master starts transmission of a data packet. If the bus is idle when ESG is set, the master transmits a START condition on the bus and then transmits the slave address. If the master is transferring data when ESG is set, at the end of that data byte transfer, the master transmits a repeated START condition before transmitting the slave address. When transmitting a data packet, the software must reset this bit when the slave address has been transmitted, otherwise a repeated START condition is transmitted after every transmission is completed.

37.2.6 Master Status Register (ICMSR)

The status bits (bits 0 to 6) in the master status register are cleared by writing 0 to the respective status bit positions. The individual status bits are held 1 until a reset by writing 0 to the appropriate bit position.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MNR	MAL	MST	MDE	MDT	MDR	MAT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*	R/W*

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6	MNR	0	R/W*	Master NACK Received When this bit is set to 1, this bit indicates that the master has received a NACK response (the SDA line is high during the acknowledge cycle on the bus) to either an address or data transmission.
5	MAL	0	R/W*	Master Arbitration Lost In a multi-master system, when this bit is set to 1, it indicates that the master has lost arbitration to other masters on the bus. At this point, MIE is reset and the master interface is disabled.
4	MST	0	R/W*	Master Stop Transmitted When this bit is set to 1, it indicates that the master has sent a STOP condition on the bus. A STOP condition can be sent either as a result of the setting of the forced stop bit in the control register, or from a NACK being received from a slave during a slave receive data packet.
3	MDE	0	R/W*	Master Data Empty At the start of a byte data transmission, the contents of the transmit data register are loaded into a shift register ready for transmitting on the bus. When this bit is set to 1, it indicates that the shift register has been loaded, so the transmit data register is ready to accept further data. During master transmission, the MDE bit is also set at the same time as the MAT bit is set after transmission of the slave address. In this case, you need to clear the MDE and MAT bits after the ICMCR's ESG bit is cleared. The clearing will restart the data transmission.
2	MDT	0	R/W*	Master Data Transmitted Byte data has been sent to the slave on the bus. This status bit becomes active after the falling edge of SCL during reception of the last data bit.

Bit	Bit Name	Initial Value	R/W	Description
1	MDR	0	R/W*	Master Data Received Byte data has been received from the bus and is in the receive data register. This status bit becomes active after the falling edge of SCL during reception of the last data bit. During single-buffer mode, this status bit must be reset after data has been read from the receive data register. When MDBS is set to 1, SCL will be held low from the timing when the receive data register acquires the data packet until the MDR flag is cleared. During master reception mode, the MDR bit is also set at the same time as the MAT bit is set after transmission of the salve address. In this case, you must clear the MDR and MAT bits after the ICMCR's ESG bit is cleared. Clearing will start the data reception
0	MAT	0	R/W*	Master Address Transmitted The master has been transmitted the slave address byte of a data packet. This bit becomes active after the falling edge of SCL during reception of the ACK bit following transmission of the address.

Note: * This bit can be read from or written to. Writing 0 clears this bit to 0 and writing 1 is ignored.

37.2.7 Master Interrupt Enable Register (ICMIER)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MNRE	MALE	MSTE	MDEE	MDTE	MDRE	MATE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
6	MNRE	0	R/W	Master NACK Received Interrupt Enable 0: Disables the MNR interrupt. 1: Enables the MNR interrupt.
5	MALE	0	R/W	Master Arbitration Lost Interrupt Enable 0: Disables the MAL interrupt. 1: Enables the MAL interrupt.
4	MSTE	0	R/W	Master Stop Transmitted Interrupt Enable 0: Disables the MST interrupt. 1: Enables the MST interrupt.
3	MDEE	0	R/W	Master Data Empty Interrupt Enable 0: Disables the MDE interrupt. 1: Enables the MDE interrupt.
2	MDTE	0	R/W	Master Data Transmitted Interrupt Enable 0: Disables the MDT interrupt. 1: Enables the MDT interrupt.
1	MDRE	0	R/W	Master Data Received Interrupt Enable 0: Disables the MDR interrupt. 1: Enables the MDR interrupt.
0	MATE	0	R/W	Master Address Transmitted Interrupt Enable 0: Disables the MAT interrupt. 1: Enables the MAT interrupt.

37.2.8 Master Address Register (ICMAR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SADD1_6	SADD1_5	SADD1_4	SADD1_3	SADD1_2	SADD1_1	SADD1_0	STM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
7 to 1	SADD1_6 to SADD1_0	All 0	R/W	Slave Address These bits are the address of the slave which the master communicates with.
0	STM1	0	R/W	Slave Transfer Mode This bit specifies the mode in which the slave operates. Bit STM1 sets the operating mode (transmit or receive mode) of the slave, which is an external slave device whose address matches the slave address (SADD1) sent from the master. The slave device is automatically set to transmit/receive mode by hardware on reception of the STM1 signal. When this bit is set to 1, it indicates a read operation. When this bit is cleared to 0, it indicates a write operation.

37.2.9 Clock Control Register (ICCCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SCGD						CDF		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
8 to 3	SCGD	All 0	R/W	SCL Clock Generation Divider When operation is in master mode, the SCL clock is generated from the internal clock by using SCGD as the ratio. This is also the operating clock in slave-mode operation while SCL is being held low to stop the bus after an overflow has occurred. SCGD must be specified in both master and slave modes. The formula expressing the relationship is: Equation 2: SCL rate calculation SCLfreq = I2Cck/(20 + SCGD × 8 + F[(tICF + tr + IntDelay) × I2Cck]) I2Cck: I2C internal clock frequency tICF: I2C SCL falling time (depending on external load) tr: I2C SCL rising time (depending on external load) IntDelay: LSI internal delay LVTTL (low drive only) buffer: 5 ns (typ.), 6 ns (max.). F[n]: n rounded up to an integer Suggested settings for CDF and SCGD for CPU speeds and the two I2C bus speeds are given in Table 37.4.
2 to 0	CDF	All 0	R/W	Clock Division Factor The internal clock used in most blocks in the I2C module is a divided module clock. The internal I2C clock is generated from the module clock using the CDF as the division ratio: Equation 1: I2C internal clock frequency calculation I2Cck = MOD_CLK/(1 + CDF) MOD_CLK: module clock frequency Ensure that minimum values for setup and hold times of the SDA signal relative to the SCL signal on the bus are satisfied. The clock frequency is to ensure that the glitch filtering will operate with glitches of up to 50 ns as described in the fast mode I2C specification. Note: CDF must be set so that the clock frequency (I2Cck) is lower than 20 MHz.

Table 37.4 Recommended Settings for CDF and SCGD*1

- Recommended register values for LVTTL buffer (low drive only)

	100 kHz		400 kHz	
Module Clock Frequency	**CDF*2**	**SCGD*3**	**CDF*2**	**SCGD*3**
130 MHz	6	20	6	3
Error		+2.04%		+0.93%

Notes: 1. These recommended values are for the SCL rate with an external load that produces tICF = 20 ns and tr = 35 ns.
Recalculate to obtain the actual values after measuring tICF and tr under actual conditions of usage.
2. Recommended value for CDF bit of ICCCR.
3. Recommended value for SCGD bit of ICCCR.

37.2.10 Receive and Transmit Data Registers (ICRXD and ICTXD)

Reading from or writing to these registers access different physical internal registers. When data is to be transmitted, the contents of the shift register are loaded via TXD. After data has been received into the shift register from the I2C bus, it is then loaded into RXD.

(1) Receive data register (ICRXD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RXD							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved When these bits are read, bits 31 to 24, 23 to 16, and 15 to 8 reflect the values of bits 7 to 0. The write value should always be 0.
7 to 0	RXD	All 0	R	Read Receive Data Data received by master or slave.

(2) Transmit data register (ICTXD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	TXD							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The write value should always be 0.
7 to 0	TXD	All 0	W	Write Transmit Data Data to be transmitted by master or slave.

37.2.11 Clock Control Register 2 (ICCCR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	CDFD	HLSE	SME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 3	—	All 0	R	Reserved When these bits are read, the value in bits 7 to 0 is set to bits 31 to 24, bits 23 to 16, and bits 15 to 8. The write value should always be 0.
2	CDFD	0	R/W	CDF Disable When this bit is set to 1, the module clock is used for internal clocks except the clock filter. For SCL rate computation, see equation 3 in Note 2. The clock filter always operates at a clock frequency divided by the CDF value.
1	HLSE	0	R/W	HIGH/LOW Separate Control Enable When this bit is set to 1, the SCGD setting is ignored and SCL is generated with the division ratio set by ICHPR during a high period and with the division ratio set by ICLPR during a low period. For SCL rate computation, see equation 3 in Note 2. The program should be prepared so that ICHPR and ICLPR should be written to before setting this bit.
0	SME	0	R/W	SCL Mask Enable When this bit is set to 1, a change of internal SCL is ignored after an SCL external input pin changes during the time equal to the number of internal clock cycles specified by ICMPR. For SCL rate computation, see equation 3 in Note 2. The program should be prepared so that ICMPR should be written to before setting this bit.

Notes: 1. The control bits should be set to "CDFD = 0, HLSE = 0, and SME = 0" or "CDFD = 1, HLSE = 1, and SME = 1". Otherwise, operation cannot be guaranteed. ICCCR2 should be written to prior to writing ICCCR.

2. Equation 3: SCL Rate Computation (CDFD = 1, HLSE = 1, and SME = 1)
   SCL freq = MOD_CLK/(8 + 2 × SMD + SCLD + SCHD), MOD_CLK: Module Clock Frequency
   SMD: SCL masked period (set by the SCL mask control register)
   SCLD: I2C SCL low clock period (set by the SCL HIGH control register)
   SCHD: I2C SCL high clock period (set by the SCL LOW control register)

Table 37.5 shows recommended register values for two types of I2C bus speeds.

Table 37.5 Recommended Register Values when CDFD = 1, HLSE = 1, and SME = 1

- Recommended Register Values for LVTTL buffer (low drive only)

Module Clock Frequency	100 kHz					400 kHz				
	CDF*1	SCGD*2	SMD*3	SCHD*4	SCLD*5	CDF*1	SCGD*2	SMD*3	SCHD*4	SCLD*5
130 MHz	6*6	0	10	632	640	6*6	0	15	135	152
Error	+0.00%					+0.00%				

Notes: 1. Recommended value for CDF bit of ICCCR.
2. Recommended value for SCGD bit of ICCCR.
3. Recommended value for SCGD bit of ICMPR.
4. Recommended value for SCGD bit of ICHPR.
5. Recommended value for SCGD bit of ICLPR.
6. In case of connecting to device, whose $t_{HD;DAT}$ is smaller than 100 ns, specifying 0 as CDF is recommended.

37.2.12 SCL Mask Control Register (ICMPR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	SMD							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved When these bits are read, the value in bits 7 to 0 is set to bits 31 to 24, bits 23 to 16, and bits 15 to 8. The write value should always be 0.
7 to 0	SMD	All 0	R/W	SCL Mask Division When SME = 1, a change of internal SCL is ignored after the external SCL changes during the time equal to the number of internal clock cycles specified by SMD. The value set in SMD should be smaller than SCHD or SCLD.

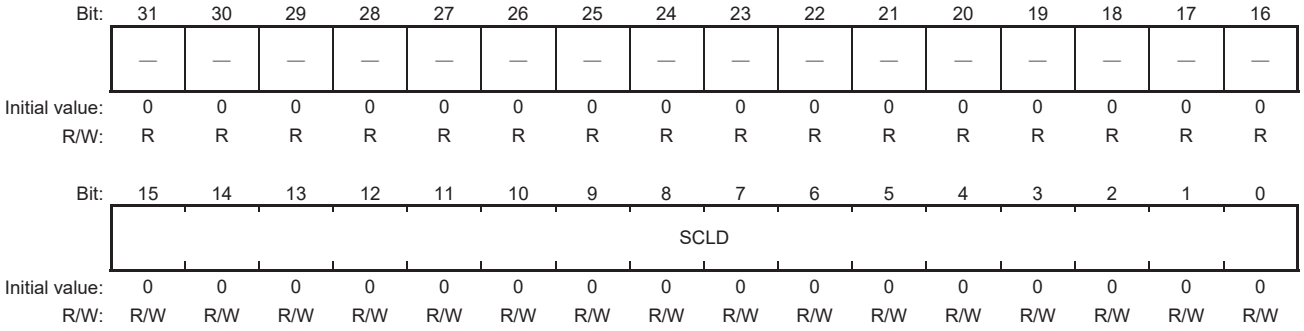
37.2.13 SCL HIGH Control Register (ICHPR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCHD															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should always be 0.
15 to 0	SCHD	All 0	R/W	SCL HIGH Clock Division When HLSE is 1 and internal SCL is driven high, the clock generated using the SCHD internal clock division ratio is output. The period over the SCL signal is driven high can be calculated by the formula below. Period over SCL is driven high = 1/MOD_CLK * (4 + SMD + SCHD) + (tICF + tpd – tr) tICF: I2C SCL falling time (depending on external load) tr: I2C SCL rising time (depending on external load) tpd: I2C0 to I2C4 is 6 ns (max.).

37.2.14 SCL LOW Control Register (ICLPR)



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should always be 0.
15 to 0	SCLD	All 0	R/W	SCL LOW Clock Division When HLSE is 1 and internal SCL is driven low, the clock generated using the SCLD internal clock division ratio is output. The period over the SCL signal is driven low can be calculated by the formula below. Period over SCL is driven low = 1/MOD_CLK * (4 + SMD + SCLD) + (tICF + tpd – tr) tICF: I2C SCL falling time (depending on external load) tr: I2C SCL rising time (depending on external load) tpd: I2C0 to I2C4 is 6 ns (max.).

37.3 Operations

37.3.1 Data and Clock Filters

These blocks filter out glitches on signals coming from the I2C bus. Glitches up to one internal clock period in width are rejected (for details on the internal clock frequency, see section 37.2.9, Clock Control Register (ICCCR)). This is for the faster I2C bus rate (400 kHz) but does not violate the slower I2C bus rate specification.

These blocks also resynchronize bus signals with the internal clock.

37.3.2 Clock Generator

The clock generator has two functions. Firstly, it generates the SCL (I2C bus clock) according to commands of the master or slave interface. Secondly, it controls the internal clock rate, used by filtering blocks and the master and slave interfaces. This clock functions as a clock enable signal of the registers in these blocks.

37.3.3 Master/Slave Interfaces

These two interfaces run independently and in parallel. The master interface controls the transmission of address and data on the I2C bus. The slave interface monitors the I2C bus and takes part in transmissions if its programmed address is seen on the bus. The interfaces communicate with the control/status registers independently. There is only one interrupt line output from the I2C module. The interrupt source is either the master or the slave.

37.3.4 Software Status Interlocking

To make the software interface with the I2C module as robust and thus simple as possible, various interlocking status mechanisms have been included in the operation of the master and slave interfaces. The status bits involved are:

(1) MDR and SDR

MDR or SDR is set to 1 when data is received. Clear the status after reading the receive data register. If data is received while MDR or SDR is set, the hardware recognizes that unread data remains in the receive data register and automatically holds SCL at the low level to suspend data transmission. In this case, transmission can be resumed by clearing the status after reading the receive data.

Consequently, when receiving data continuously, be sure to clear the status bit (MDR or SDR) after reading the receive data register.

(2) MDE and SDE

If the MDE or SDE status bit is still set when data in the transmit data register is to be transmitted on the I2C bus by the slave or master, the SCL line must be held low until the MDE or SDE status bit is reset. The MDE or SDE status bit being set indicates that the data currently held in the transmit data register has already been transmitted on the I2C bus.

The software must clear this status bit when it writes to the transmit data register after transmission of the next data byte has become possible. This is not required for the first byte of data to be transmitted on the bus.

(3) MAL

When the master loses arbitration, the MAL bit (of the master status register) is set and the MIE bit (of the master control register) is reset. At this point, master mode is invalid and the I2C bus interface enters the slave mode. When master operation is restarted, data transfer from the master begins after the MAL bit has been cleared.

(4) SAR

The SAR status bit is set when the slave identifies its address on the I2C bus. At this point the slave interface forces the SCL line low until the SAR status bit is reset.

This is particularly important when a slave transmit is about to take place on the bus, and the slave will transmit the data from the transmit data register. The software responds to the SAR status by writing the required data into the transmit data register and then resetting the SAR status bit. This allows the slave interface to continue the access.

Unless the SAR bit is in use, when the slave is about to receive data, the software might still be reading out data that was loaded in previous access from the receive data register. In this case the valid data still held in the receive data register is overwritten. However, this is avoided using the SAR status bit. After the software has read data in the receive data register, reset the SAR bit (if it is set). Then overwriting the receive data register is avoided.

37.3.5 I2C Bus Data Format

Figure 37.2 shows a timing chart for the I2C bus interface. Table 37.6 describes the meaning of each symbol in Figure 37.2.

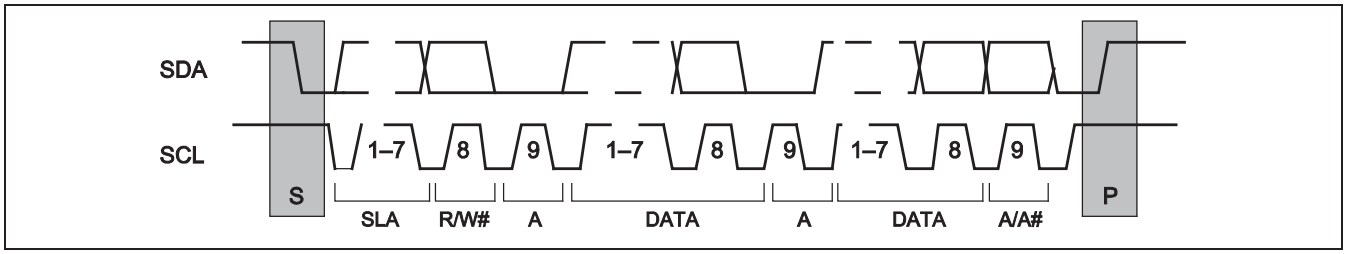


Figure 37.2 I2C Bus Timing

Table 37.6 Description on Symbols of I2C Bus Data Format

Symbol	Description
S	Indicates a start condition. A master device changes SDA from high to low while SCL is high level.
SLA	Indicates a slave address. A slave address is used when a master device selects a slave device.
R/$\overline{W}$	Indicates the direction of data transmission. If the R/$\overline{W}$ bit is 1, the data flows from the slave to the master device. If the bit is 0, the data flows from the master to the slave device.
A	Indicates data acknowledge. Data receiving device makes SDA low level (the slave device returns a data acknowledge signal in master transmission mode, and vice versa).
DATA	Indicates transmit or receive data. The data length is eight bits, which are transferred in the MSB first.
P	Indicates a stop condition. A master device changes SDA from low to high while SCL is high.

37.3.6 7-Bit Address Format

Figure 37.3 shows the format of data transfer from a master to a slave device (master data transmit format). Figure 37.4 shows the data transfer format (master data receive format) when a master device reads the second and the following byte data from a slave device.

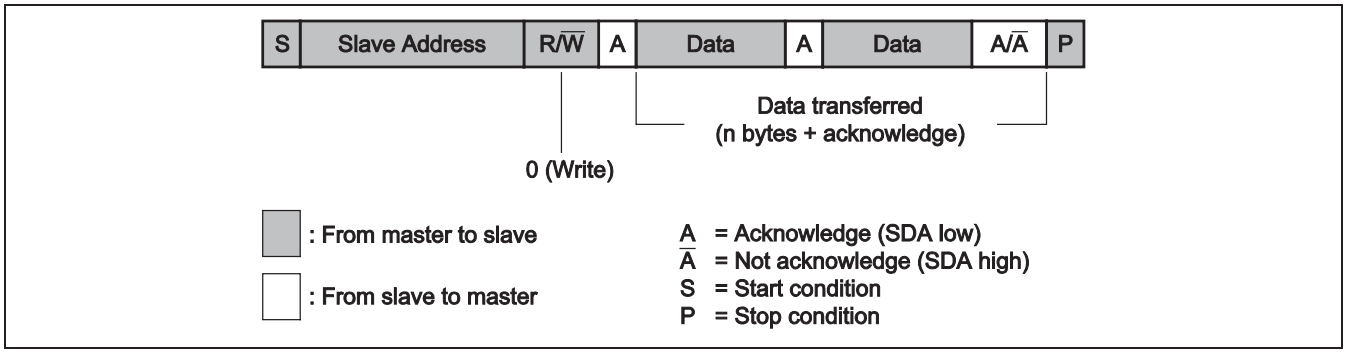


Figure 37.3 Master Data Transmit Format

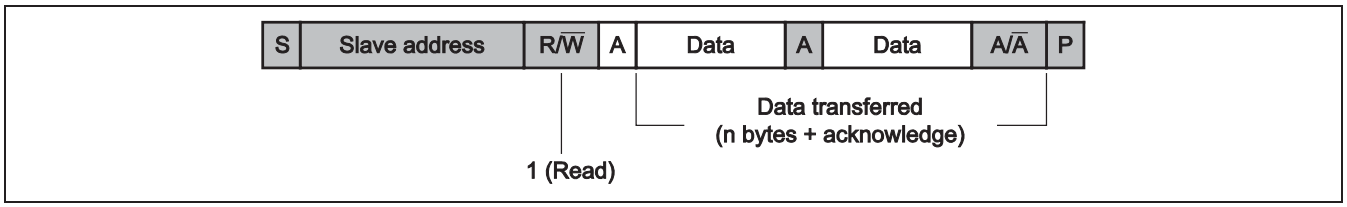


Figure 37.4 Master Data Receive Format

Figure 37.5 shows the combined format when the data transfer direction changes during one transfer. When changing the direction after the first transfer, the repeated START condition (Sr), slave address and R/$\overline{W}$ bits are transmitted. In this case, the R/$\overline{W}$ bit is set to the direction opposite to the first transfer direction. The repeated START condition is issued by the master at the end of a transmit or receive cycle if the enable start generation bit in the master control register has been set.

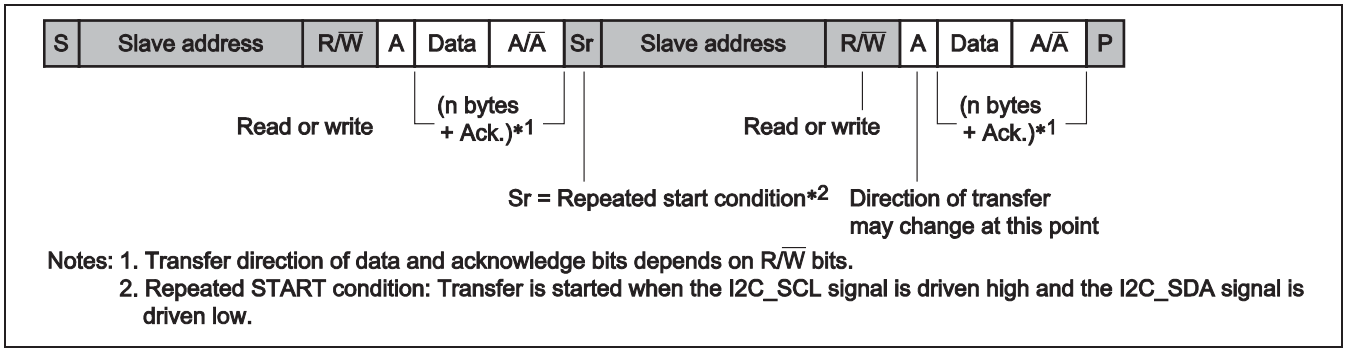


Figure 37.5 Combination Transfer Format of Master Transfer

37.3.7 10-Bit Address Format

Description is given below on the 10-bit address transfer format supported in master mode. This format has three transfer methods as the 7-bit address transfer format.

Figure 37.6 shows the data transmit format. The set value in the master address register is output in one byte following the first START condition (S). The value set in the transmit data register (TXD) is transmitted as a slave address in the second byte. Data on and after the third byte is transferred in the same way as the 7-bit address data.

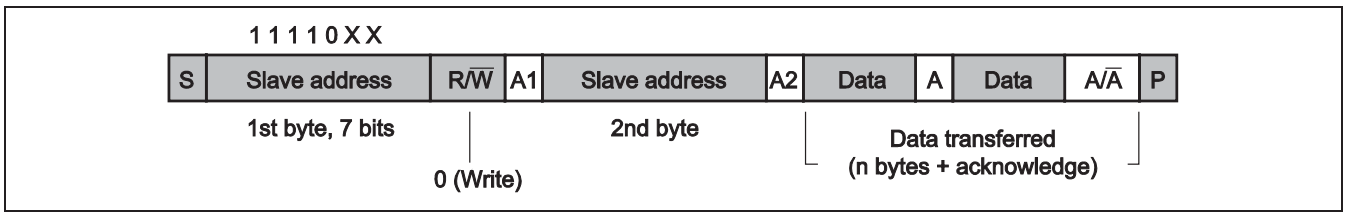


Figure 37.6 10-Bit Address Data Transmit Format

Figure 37.7 shows the data receive format. Two bytes of an address is transmitted in the same way as in the data transmit format. Then, repeated START condition (Sr) is transmitted and the value set in the address register is output. At this time, STM1 must be set to 1 (receive mode). Data is transferred in the same way as in the 7-bit address data receive format.

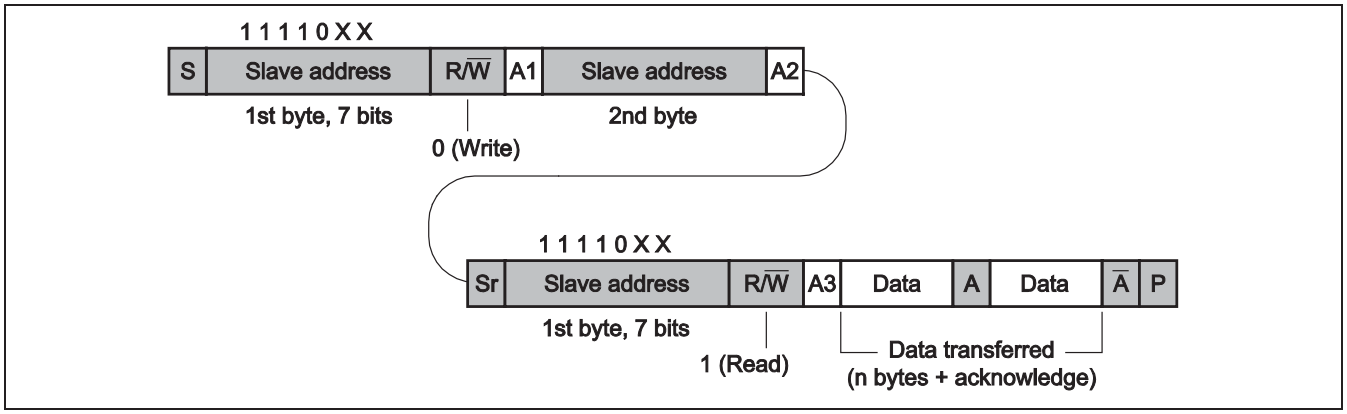


Figure 37.7 10-Bit Address Data Receive Format

Figure 37.8 shows the data transmit/receive combined format.

In the data transmit/receive combined format, data is transmitted after an address is transmitted with the first two bytes. Then, the repeated START condition (Sr) is transmitted instead of STOP condition (P). After Sr is transmitted, the procedure is the same as that in the data receive format.

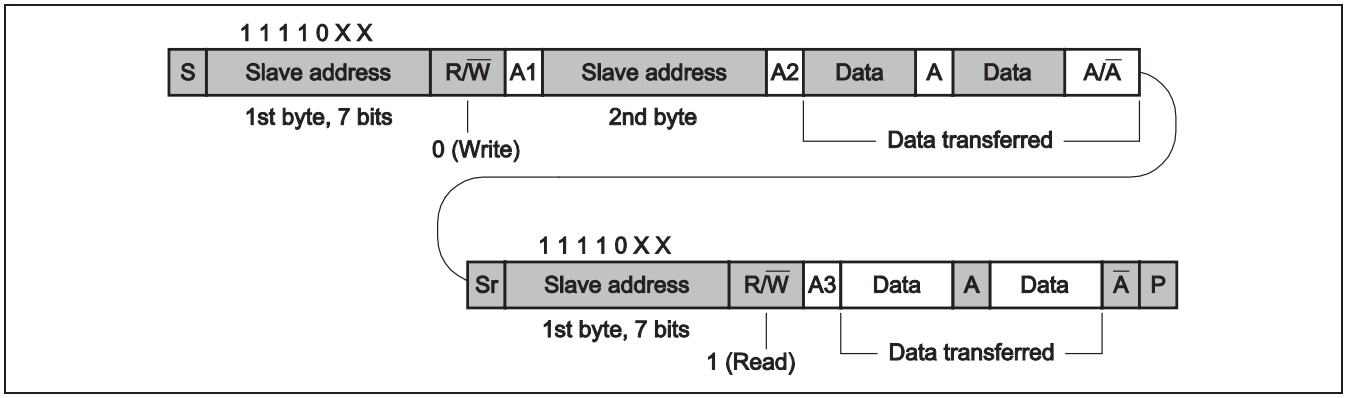


Figure 37.8 10-Bit Address Transmit/Receive Combined Format

37.3.8 Master Transmit Operation

The procedure and operations for transmission in master transmit mode are described below. Figure 37.9 shows the timing chart in master transmit mode. Setting the MDBS bit in the master control register allows the I2C to operate in single-buffer mode.

1. Set up the initial state by setting the slave address register, transmission data register, clock control register, and master interrupt enable register. Note that the setting of the clock control register must be in accord with the rate of transmission. Since slave mode is also required even when master mode is used, set the device address in the slave address register.
2. Monitor the FSDA bit in the master control register. Confirm that this bit is low, meaning that other I2C devices are not using the bus. After confirmation, set the MIE (bit 3) and ESG (bit 0) bits in the master control register to 1 to start master transmission.
3. After the transmit START condition, slave address, and data transfer direction bits are transmitted, an interrupt due to the MAT and MDE bits in the master status register is generated at the timing of (1) in Figure 37.9. At this time, clear the ESG bit to 0. To suspend the data transmission, the master device will hold SCL low until the MDE bit is cleared.
4. An interrupt due to the SAR bit is generated at the timing of (3) shown in Figure 37.9. If the IRQ handling in the slave device is delayed, the slave device extends the SCL period to suspend data transmission (at the timing of (7) in Figure 37.9). The slave device drives SDA low at the ninth clock and returns ACK.
5. Data is transmitted in units of nine bits: 8-bit data and 1-bit ACK. An interrupt of MDE (bit 3) is generated at the ninth clock before data transfer (at the timing of (2) in Figure 37.9). An interrupt of MDT (bit 2) is generated at the eighth clock after 1-byte data transfer (at the timing of (4) in Figure 37.9). Clear MDE to 0 after setting transmit data. An interrupt of SDR (slave data receive) of the slave device is generated at the eighth clock (at the timing of (6) in Figure 37.9). Clear SDR after the slave device reads the receive data. If this processing is delayed, the slave device extends the SCL period to suspend data transmit (at the timing of (8) in Figure 37.9).
6. To end data transfer, an interrupt of MNR (bit 6) in the master status register is generated at the ninth clock (at the timing of (5) in Figure 37.9) when ACK from the slave device is 1 (NACK). The master device receives this NACK and outputs the STOP condition. When data transmission ends on the master device side, set FSB (bit 1) in the master control register to 1 to output the STOP condition. After the I2C module fetches FSB on completion of transmission or reception of the last bit of byte data, it enters the stop state. Therefore in order to stop the communication after the predetermined number of byte data is transferred, the FSB bit needs to be set before the last byte data transfer is started.
7. The FSB bit needs to be set before the last byte data is transferred. In master transmit mode, after the last byte data is set, the MST (master stop transmitted) bit is checked by either interrupt or polling. At the same time MNR (master NACK received) bit must be checked. If NACK is returned, an error routine is executed to retransmit the last byte data.

Signal level changes of (1) to (6) in Figure 37.9 are generated after the falling edge of the clock.

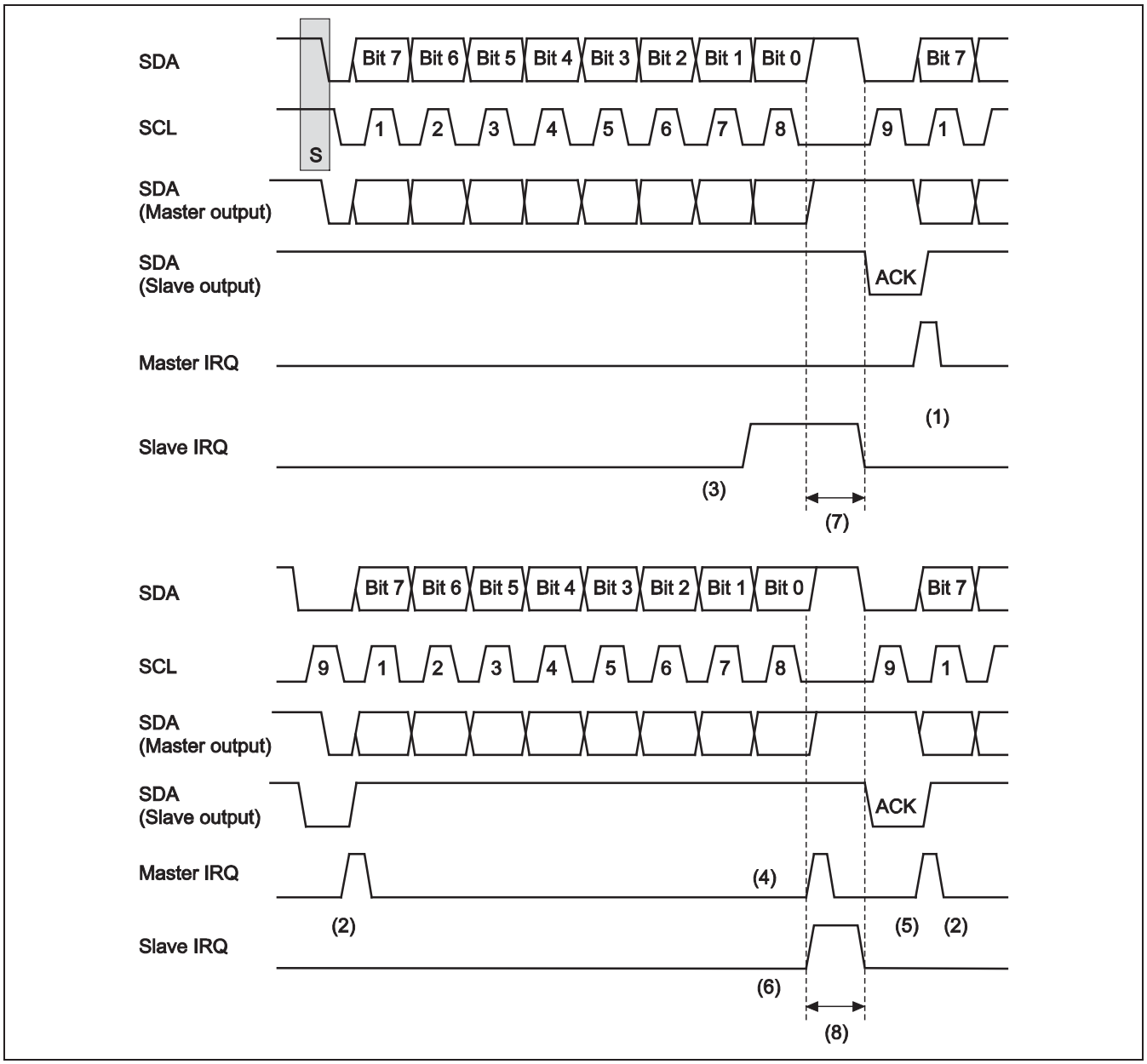


Figure 37.9 Data Transmit Mode Operation Timing

37.3.9 Master Receive Operation

The data receive procedure and operation in master receive mode are described below. Figure 37.10 shows the timing chart in master receive mode. Setting the MDBS bit in the master control register allows the I2C to operate in single-buffer mode.

1. In master receive mode, as to transmit of a slave address and a 1-bit signal indicating the data transfer direction, operation is the same as that in master transmit mode. At this time, set the data transfer direction to 1 (reception).
2. The slave device automatically enters the data transmit mode according to the signal that indicates the data transfer direction, and transmits 1-byte data in synchronization with the SCL clock output from the master device. The master device generates an interrupt of MDR (bit 1) at the eighth clock (at the timing of (2) in Figure 37.10). Clear the MDR bit after the master device reads receive data. If this processing is delayed, the master device extends the SCL period to suspend data transmission (at the timing of (3) in Figure 37.10).
3. The slave device generates an interrupt of the status SDT (bit 2) indicating 1-byte data transfer end at the eighth clock (at the timing of (2) in Figure 37.10) and an interrupt of the status SDE (bit 3) indicating data empty at the ninth clock (at the timing of (1) in Figure 37.10). Clear SDE after writing slave transmit data to TXD.
4. To end data transfer, set FSB (bit 1) in the master control register of the master device and output STOP condition. After the I2C module fetches FSB on completion of transmission or reception of the last of byte data, it enters the stop state. Therefore in order to stop the communication after predetermined number of byte data is transferred, FSB bit needs to be set before the last byte data transfer is started. After confirming reception of the last byte, even when the master receiver has completed the reception transaction, the protocol layer will inform the slave transmitter that retransmission is necessary if the last byte is incorrect.

Signal level changes of (1) to (3) in Figure 37.10 are generated after the falling edge of the clock.

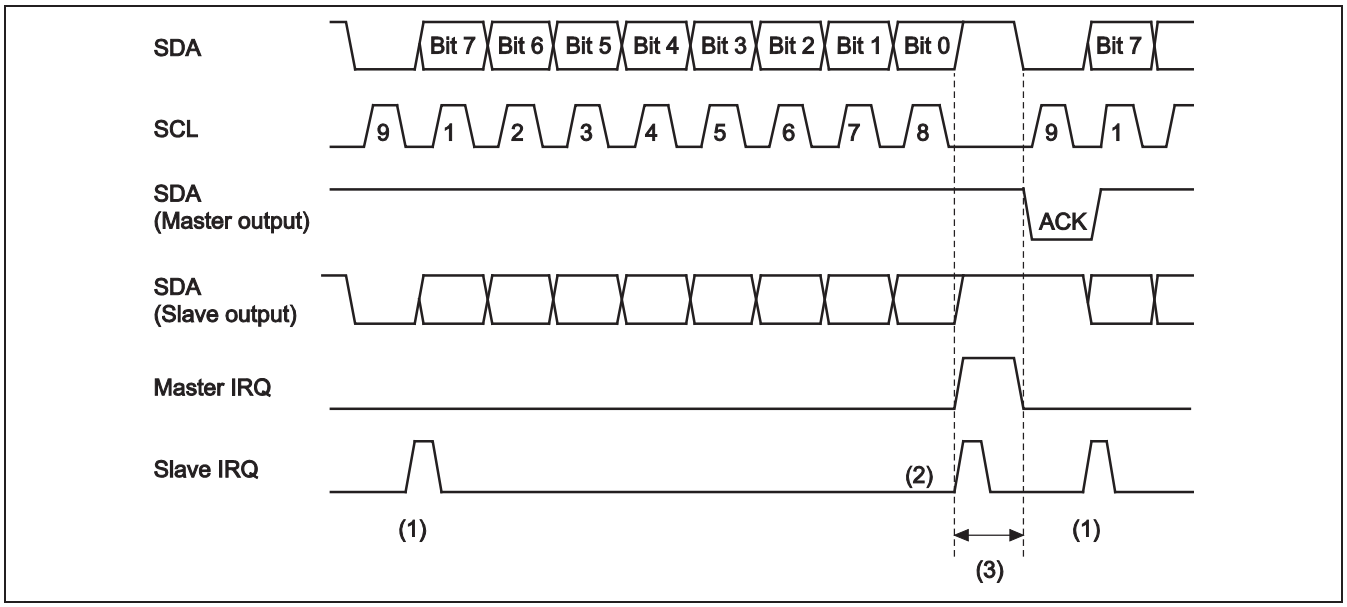


Figure 37.10 Data Receive Mode Operation Timing

37.4 Programming Examples

37.4.1 Master Transmitter

In order to set up the master interface to transmit a data packet on the I2C bus, follow the procedure below (an example for I2C0):

(1) Load value for the clock control register

(When the module clock frequency is 130 MHz and SCL clock frequency is set to 400 kHz)

1. Set the SCL clock generation divider bit (SCGD) to H'3.
2. Set the clock division ratio bit (CDF) to H'6 (I2C internal clock I2Cck: 18.57 MHz).

(2) Load value for the master control register, first data byte, and address

1. Master address register = address of slave being accessed and STM1 bit (write mode: 0)
2. Transmit data register = first data byte to be transmitted
3. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)

(3) Wait for outputting address

1. Wait for master event (an interrupt of the MAT and MDE bits in the master status register).
2. Set the master control register to H'88 (to suspend the data transmission, the master device will hold the SCL low until the MDE bit is cleared).

   If only one byte of data is transmitted, set the master control register to H'8A, meaning that the stop generation is enabled. This generates a stop on the bus as soon as one byte has been transmitted.
3. Reset the MAT and MDE bits.

(4) Monitor transmission of data

1. Wait for master event, MDE in the master status register.
2. Transmit data register = subsequent data.
3. Reset the MDE bit.

   Clear MDE after setting the last byte to be transmitted. After the last byte data is transmitted, MDE is generated. Before clearing MDE, you must set the master control register to H'8A (set the force stop control bit).

(5) Wait for end of transmission

1. Wait for the master event, MST in the master status register.
2. Reset the MST bit after confirming MNR (master NACK received).

37.4.2 Master Receiver

In order to set up the master interface to receive a data packet on the I2C bus, follow the procedure below:

(1) Load value for the clock control register

The same procedure as the master transmitter is applied. See the program example for the master transmitter.

(2) Load value for the master control register and address

1. Master address register = address of slave being accessed and STM1 bit (read mode: 1)
2. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)

(3) Wait for outputting address

1. Wait for master event (an interrupt of the MAT and MDR bits in the master status register).
2. Set the master control register to H'88 (to suspend the data transmission, the master device will hold the SCL low until the MDR bit is cleared).
   If only one byte of data is transmitted, set the master control register to H'8A, meaning that the stop generation is enabled. This generates a stop on the bus as soon as one byte has been transmitted.
3. Reset the MAT and MDR bits.

(4) Monitor reception of data

1. Wait for master event (the MDR bit in the master status register).
2. Read data from the received data register.
   If the next byte of data is the second to last byte to be transmitted by the slave device, the following applies to the receive interrupt (that is, MDR interrupt) in the second to last byte.
3. Set the master control register to H'8A (set the force stop control bit).
4. Reset the MDR bit.

(5) Wait for end of reception

1. Handle the receive interrupt (MDR) in the last byte: that is, read the data and clear the MDR.
2. Wait for master event, MST in the master status register.
3. Reset the MST bit.

37.4.3 Master Transmitter—Repeated START—Master Receiver

In order to set up the master interface to transmit a data packet on the I2C bus, issue a repeated START condition, then read byte data back from the slave, follows the procedure below:

(1) Load value for the clock control register

The same procedure as the master transmitter is applied. See the program example for the master transmitter.

(2) Load value for the master control register and address

1. Master address register = address of slave being accessed and STM1 bit (write mode: 0)
2. Transmit data register = first data byte to be transmitted
3. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)
4. Wait until slave-address transfer have started, and set master control register to H'88 (MDBS=1, MIE=1, ESG=0). (Start of slave address transfer can be checked by FSDA bit, or waiting enough time after setting ESG bit).

(3) Wait for outputting slave-address for master transmission

1. Wait for master event (an interrupt of the MAT and MDE bits in the master status register).
2. Set the master address register to address of slave being accessed and STM1 bit (read mode: 1).
   When the enable start generation bit in the master control register is still set, at the end of the byte transmission the master will issue a repeated START condition. Since the new address has been loaded above, the bus direction will be changed.
3. Reset the MAT and MDE bits.

(4) Monitor transmission of data

1. Wait for master event (an interrupt of the MDE bit in the master status register).
2. Master control register = H'89 (MDBS = 1, MIE = 1, ESG = 1)
3. Reset the MDE bit.

(5) Wait for outputting slave-address for master reception

1. Wait for master event (an interrupt of the MAT and MDR bits in the master status register).
2. Set the master control register to H'88. (To suspend stop the data transmission, the master device will hold the SCL low until the MDR bit is cleared.)
3. Reset the MAT and MDR bits.

(6) Monitor reception of data

1. Wait for master event (the MDR bit in the master status register).
2. Read data from the received data register.
   If the next byte of data is the second to last byte to be transmitted by the slave device, the following applies to the receive interrupt (that is, MDR interrupt) in the second to last byte.
3. Set the master control register to H'8A (set the force stop control bit).
4. Reset the MDR bit.

(7) Wait for end of reception

1. Handle the receive interrupt (MDR) in the last byte: that is, read the data and clear the MDR.
2. Wait for master event, MST in the master status register.
3. Reset the MST bit.

37.5 Usage Notes

In section 37.2.9, Clock Control Register (ICCCR), in the description of SCGD and CDF, following equation is described.

SCLfreq = I2Cck/(20 + SCGD × 8 + F[(tICF + tr + IntDelay) × I2Cck])

I2Cck: I2C internal clock frequency

tICF: I2C SCL falling time (depending on external load)

tr: I2C SCL rising time (depending on external load)

IntDelay: LSI internal delay

LVTTL (low drive only) buffer: 5 ns (typ.), 6 ns (max.).

F[n]: n rounded up to an integer

I2Cck = MOD_CLK/(1 + CDF)

MOD_CLK: module clock frequency

Based on parameter described above, this equation approximately estimates the SCL frequency, but includes some error in the resulting frequency. Before finalizing register setting to be used, measure actual SCL frequency on the board, and confirm that observed frequency satisfy the constraint. The reason why calculated result includes some error is parameters used in this equation varies depending on the characteristics of each sample. For example, tICF and tr depend on logical threshold of IO-cell, and intDelay depends on variation of fabrication process.

For adjustment of SCL frequency, modifying the setting of ICCCR[2:0].CDF and ICCCR[8:3].SCGD will be effective. Increasing the value of CDF or SCGD value will make SCL frequency lower. However, how they decrease SCL frequency is different. So, by increasing one register value and decreasing the other, SCL frequency can be adjusted.

38. Clock-Synchronized Serial Interface with FIFO (MSIOF)

This LSI includes clock-synchronized serial I/O module with FIFO (MSIOF). In this module, MPϕ is used as a module clock.

38.1 Features

- Number of channels: Three channels
- FIFO capacity: 32 bits × 64 stages for transmission and 32 bits × 128 stages for reception
  - For reception FIFO, receiving 1 FRAME with 2 groups with 64 words requires at most 128 FIFO stages.
- MSB first or LSB first selectable for data transmission and reception
- Synchronization by frame synchronization pulse, level, or left/right channel switch
- Supports master and slave modes
- Interrupts: One type
- Serial clock
- DMA transfer
- Serial format

  Supports serial formats: IIS, SPI (master and slave modes).
- CLK/SYNC (SPI) in common transmit/receive mode
  - Up to 26 MHz for all channels

Figure 38.1 shows a block diagram of the MSIOF.

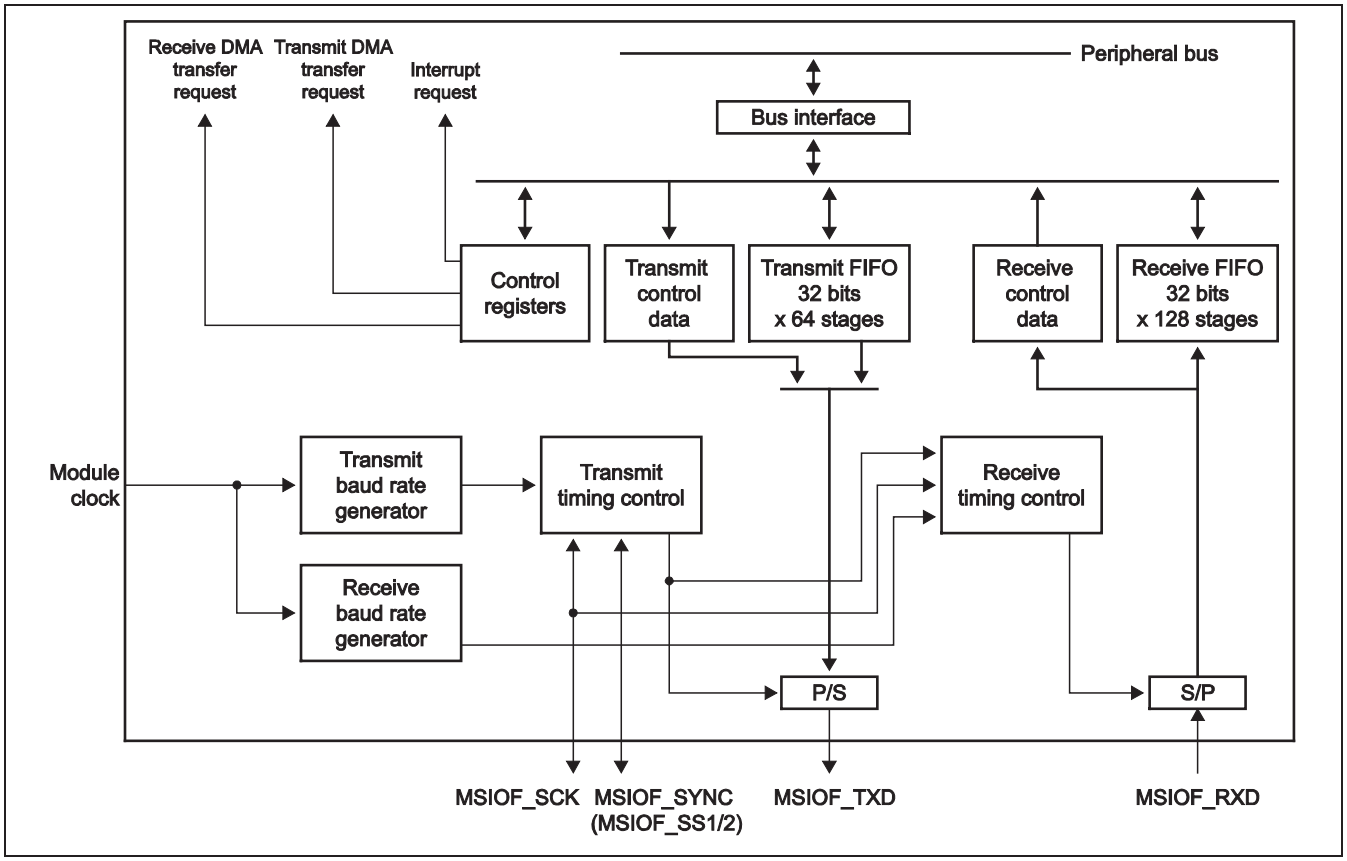


Figure 38.1 Block Diagram of MSIOF

38.2 Input/Output Pins

The pin configuration of this module is shown in Table 38.1.

Table 38.1 Pin Configuration

Name	Abbreviation	I/O	Function
MSIOF_SCK	SCK	I/O	MSIOF serial clock for transmission Works as SCK when a common clock is used for transmission and reception.
MSIOF_SYNC	SYNC	I/O	MSIOF frame synchronization signal for transmission Works as SYNC when a common synchronization signal is used for transmission and reception.
MSIOF_SS1	SS1	Output	MSIOF frame synchronization signal 1 for transmission This signal can work only master mode.
MSIOF_SS2	SS2	Output	MSIOF frame synchronization signal 2 for transmission This signal can work only master mode.
MSIOF_TXD (MOSI/MISO)	MOSI/MISO (TXD)	Output	MSIOF transmit data
MSIOF_RXD (MISO/MOSI)	MISO/MOSI (RXD)	Input	MSIOF receive data

38.3 Register Descriptions

Tables 38.2 and 38.3 show the MSIOF register configuration and Table 38.4 shows the register state in each processing mode.

Table 38.2 Module Base Address Summary

Module Name	Base Address
MSIOF0	H'E6E2 0000
MSIOF1	H'E6E1 0000
MSIOF2	H'E6E0 0000

Note: Address H'E6xx can be accessed only by CPU.

Table 38.3 Register Configuration

Name	Abbreviation	R/W	Address Offset	Access Size
MSIOF transmit mode register 1	SITMDR1	R/W	H'0000	32
MSIOF transmit mode register 2	SITMDR2	R/W	H'0004	32
MSIOF transmit mode register 3	SITMDR3	R/W	H'0008	32
MSIOF receive mode register 1	SIRMDR1	R/W	H'0010	32
MSIOF receive mode register 2	SIRMDR2	R/W	H'0014	32
MSIOF receive mode register 3	SIRMDR3	R/W	H'0018	32
MSIOF transmit clock select register	SITSCR	R/W	H'0020	16
MSIOF control register	SICTR	R/W	H'0028	32
MSIOF FIFO control register	SIFCTR	R/W	H'0030	32
MSIOF status register	SISTR	R/W	H'0040	32
MSIOF interrupt enable register	SIIER	R/W	H'0044	32
MSIOF transmit FIFO data register	SITFDR	W	H'0050	32
MSIOF receive FIFO data register	SIRFDR	R	H'0060	32

Table 38.4 Register States in Each Operating Mode

Abbreviation	Reset	Module Standby
SITMDR1	Initialized	Retained
SITMDR2	Initialized	Retained
SITMDR3	Initialized	Retained
SIRMDR1	Initialized	Retained
SIRMDR2	Initialized	Retained
SIRMDR3	Initialized	Retained
SITSCR	Initialized	Retained
SICTR	Initialized	Retained
SIFCTR	Initialized	Retained
SISTR	Initialized	Retained
SIIER	Initialized	Retained
SITFDR	Initialized	Initialized
SIRFDR	Undefined	Initialized

38.3.1 MSIOF Transmit Mode Register 1 (SITMDR1)

SITMDR1 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	PCON	SYNCMD[1:0]		SYNCCH[1:0]		SYNCAC	BITLSB	—	DTDL[2:0]			—	SYNCDL[2:0]		
Initial value:	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	FLD[1:0]		—	TXSTP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. 0: Slave mode 1: Master mode
30	PCON	0	R/W	Transfer Signal Connection 0: Setting prohibited 1: MSIOF_SCK and MSIOF_SYNC are used as common signals for transmission and reception (MSIOF_SCK and MSIOF_SYNC).
29, 28	SYNCMD[1:0]	00	R/W	SYNC Mode These bits specify the mode for the MSIOF_SYNC signal. 00: Frame start synchronization pulse 01: Reserved 10: Level mode/SPI 11: L/R mode
27, 26	SYNCCH[1:0]	00	R/W	Synchronization Signal Channel Select These bits are valid only in master mode. 00: The frame synchronization signal output at MSIOF_SYNC. 01: The frame synchronization signal output at MSIOF_SS1. 10: The frame synchronization signal output at MSIOF_SS2. 11: Setting prohibited
25	SYNCAC	0	R/W	MSIOF_SYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for MSIOF_SYNC Pin The value specified with TXDIZ in SICTR is output during transmission. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	SYNCDL[2:0]	000	R/W	Frame Synchronization Signal Timing Delay These bits extend the transmit frame synchronization signal. The value specified with TXDIZ in SICTR is output during transmission. These bits are invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. When L/R mode, these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited
15 to 4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3, 2	FLD[1:0]	00	R/W	Frame Synchronization Signal Interval Specify the minimum idle time between frames in the number of serial clock cycles. This setting is valid only in master mode. When L/R mode, these bits should always be set to 00. When SPI mode, these bits shall not be set to 00. 00: 0-clock-cycle delay 01: 1-clock-cycle delay 10: 2-clock-cycle delay 11: 3-clock-cycle delay
1	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	TXSTP	0	R/W	Transmission Stop 0: Setting prohibited 1: Temporarily stops transmission when the number of transmit FIFO stages is not enough to valid.

38.3.2 MSIOF Transmit Mode Register 2 (SITMDR2)

SITMDR2 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	GRP	—	BITLEN1					WDLEN1							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	GRP	0	R/W	Group Count The number of groups is set to the value specified in this bit + 1.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0]	01111	R/W	Data Size (8 to 32 bits) The word size (bits) of groups 1 is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size.
23 to 16	WDLEN1[7:0]	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 1 is set to WDLEN1 + 1 respectively. 8-bit value is set to WDLEN1.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.3 MSIOF Transmit Mode Register 3 (SITMDR3)

SITMDR3 is a 32-bit readable/writable register that specifies the MSIOF transmit mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2					WDLEN2							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2	01111	R/W	Word Size (1 to 32 bits) The word size of groups 2 is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size.
23 to 16	WDLEN2	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 2 are set to WDLEN2 + 1. 8-bit value is set to WDLEN2.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.4 MSIOF Receive Mode Register 1 (SIRMDR1)

SIRMDR1 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TRMD	—	SYNCMD[1:0]		—	—	SYNCAC	BITLSB	—	DTDL[2:0]			—	SYNCDL[2:0]		
Initial value:	1	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R/W	R/W	R/W

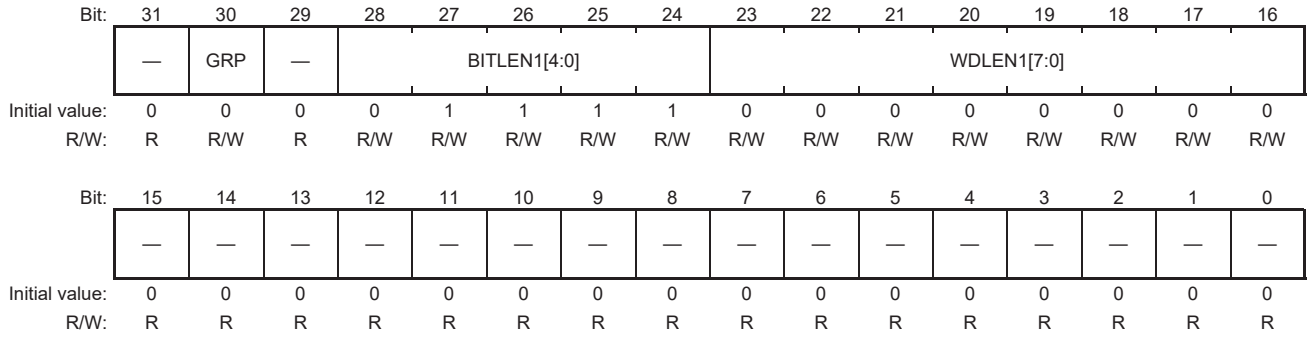
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TRMD	1	R/W	Transfer Mode Selects the transfer mode. This bit should be set to 0.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29, 28	SYNCMD [1:0]	00	R/W	SYNC Mode The mode setting in these bits should be the same as that in SITMDR1.SYNCMD. 00: Frame start synchronization pulse 01: Reserved 10: Level mode/SPI 11: L/R mode
27, 26	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
25	SYNCAC	0	R/W	SYNC Polarity 0: Active-high signal in synchronization pulse or level mode, or driven high then low in L/R mode 1: Active-low signal in synchronization pulse or level mode, or driven low then high in L/R mode This bit must have the same setting as the SYNCAC bit of SITMDR1.
24	BITLSB	0	R/W	MSB/LSB First 0: MSB first 1: LSB first
23	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
22 to 20	DTDL[2:0]	001	R/W	Data Pin Bit Delay for MSIOF_SYNC Pin B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited In case of SPI mode, only 000 is allowed to set to this field.
19	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
18 to 16	SYNCDL [2:0]	000	R/W	MSIOF_SYNC Timing Delay The synchronization signal is extended for the clock cycles specified in these bits. These bits are invalid when SYNCMD[1:0] = B'01. B'1xx is valid only in SPI mode. In SPI mode, these bits should be specified so that the sum of the delays specified through DTDL and SYNCDL becomes an integer value. In L/R mode, these bits should always be set to 000. 000: No bit delay 001: 1-clock-cycle delay 010: 2-clock-cycle delay 011: 3-clock-cycle delay 101: 0.5-clock-cycle delay 110: 1.5-clock-cycle delay Other than above: Setting prohibited In case of SPI mode, only 000 is allowed to set to this field.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.5 MSIOF Receive Mode Register 2 (SIRMDR2)

SIRMDR2 is a 32-bit readable/writable register that specifies the MSIOF receive mode.



Bit	Bit Name	Initial Value	R/W	Descriptions
31	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
30	GRP	0	R/W	Group Count The number of groups is set to the value specified in this bit + 1. Set the same value as the value specified by the GRP bit in SITMDR2.
29	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
28 to 24	BITLEN1[4:0]	01111	R/W	Word Size (8 to 32 bits) The word size (bits) of groups 1 is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size. Set the same value as the value specified by the BITLEN1 bits in SITMDR2.
23 to 16	WDLEN1[7:0]	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 1 is set to WDLEN1 + 1. When one or two groups are used, the 8-bit value is set to WDLEN1. Set the same value as the value specified by the WDLEN1 bits in SITMDR2.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.6 MSIOF Receive Mode Register 3 (SIRMDR3)

SIRMDR3 is a 32-bit readable/writable register that specifies the MSIOF receive mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	BITLEN2[4:0]					WDLEN2[7:0]							
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
28 to 24	BITLEN2[4:0]	01111	R/W	Word Size (1 to 32 bits) The word size is set to the value specified in these bits + 1. Either 8, 16, 24, or 32 bits can be specified as word size. Set the same value as the value specified by the BITLEN2 bits in SITMDR3.
23 to 16	WDLEN2[7:0]	H'00	R/W	Word Count (1 to 64 words) The word counts of groups 2 is set to WDLEN2 + 1. 8-bit value is set to WDLEN2. Set the same value as the value specified by the WDLEN2 bits in SITMDR3.
15 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.7 MSIOF Control Register (SICTR)

SICTR is a 32-bit readable/writable register that specifies the MSIOF operating state.

The values written to the TXE, RXE, TFSE, RFSE, TSCKE, and RSCKE bits become valid (can be read from the bits) several cycles after writing. These bits should not be modified at the same time. Modify one bit at a time, and check that the new value can be read from the bit, and then modify another bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TSCKIZ[1:0]		RSCKIZ[1:0]		TEDG	REDG	—	—	TXDIZ[1:0]		—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TSCKE	TFSE	RSCKE	RFSE	—	—	TXE	RXE	—	—	—	—	—	—	TXRST	RXRST
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	TSCKIZ[1:0]	00	R/W	Transmit Clock Input/Output Polarity Select in SPI Mode When Transmission is Disabled When SPI mode is not used, these bits must always be set to 00. These bits must always be set 10 or 11 when SPI mode. [Master mode] 00: Outputs MSIOF_SCK when transmission is disabled. 01: Setting prohibited 10: Outputs 0. 11: Outputs 1. [Slave mode] 00: Inputs MSIOF_SCK when transmission is disabled. 01: Setting prohibited 10: Inputs 0 through MSIOF_SCK when transmission is disabled. 11: Inputs 1 through MSIOF_SCK when transmission is disabled.
29, 28	RSCKIZ[1:0]	00	R/W	Receive Clock Polarity Select in SPI Mode Set the same value as the value specified by the TSCKIZ bits. Other setting is prohibited.
27	TEDG	0	R/W	Transmit Timing 0: Outputs transmit data at the rising edge of the clock. 1: Outputs transmit data at the falling edge of the clock.
26	REDG	0	R/W	Receive Timing 0: Samples receive data at the falling edge of the clock. 1: Samples receive data at the rising edge of the clock.
25, 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
23, 22	TXDIZ[1:0]	00	R/W	Pin Output When Transmission is Disabled These bits specify the MSIOF_TXD pin output state when transmission is disabled. 00: Outputs 0. 01: Outputs 1. 10: Output is in high-impedance state. 11: Setting prohibited
21 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	TSCKE	0	R/W	Transmit Serial Clock Output Enable This bit is valid in master mode. When this bit is set to 1, the MSIOF initializes the baud rate generator and initiates the operation. At the same time, the MSIOF outputs the clock generated by the baud rate generator to the MSIOF_SCK pin. After the clock is output, 1 can be read. When transmitting data, set this bit to 1 before setting the TFSE and TXE bits. After data transmission, clear the TFSE and TXE bits and then clear this bit to 0. [Write data] 0: Disables the MSIOF_SCK output. (Outputs the value specified with TSCKIZ.) 1: Enables the MSIOF_SCK output. [Read data] 0: Does not output MSIOF_SCK. (Outputs the value specified with TSCKIZ.) 1: Outputs MSIOF_SCK.
14	TFSE	0	R/W	Transmit Frame Synchronization Signal Output Enable This bit is valid in master mode. When this bit is set to 1, the MSIOF initializes the frame counter and initiates the operation. After the transmit frame synchronization signal is output, 1 can be read. When 0 is written to this bit, 0 is set after transmission of the frame. [Write data] 0: Disables the MSIOF_SYNC output. (Outputs the value specified with SYNCAC.) 1: Enables the MSIOF_SYNC output. [Read data] 0: Does not output MSIOF_SYNC. (Outputs the value specified with SYNCAC.) 1: Outputs MSIOF_SYNC.
13	RSCKE	0	R/W	Receive Serial Clock Output Enable The write value should always be 0.
12	RFSE	0	R/W	Receive Frame Synchronization Signal Output Enable The write value should always be 0.
11, 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
9	TXE	0	R/W	Transmit Enable When this bit is set to 1, the MSIOF starts data transmission from the beginning of the next frame (at the rising edge of the frame synchronization signal). After the valid data is output, 1 can be read. When value 1 set to this bit becomes valid, the MSIOF issues a transmit data transfer request according to the setting of the TFWM bits in SIFCTR. When transmit data is stored in the transmit FIFO, transmission of data from the MSIOF_TXD pin begins. When 0 is written to this bit, 0 is set after transmission of the frame. This bit is initialized upon a transmit reset. [Write data] 0: Disables the MSIOF_TXD output. (Outputs the value specified with TXDIZ.) 1: Enables the MSIOF_TXD output. [Read data] 0: Does not output MSIOF_TXD. (Outputs the value specified with TXDIZ.) 1: Outputs MSIOF_TXD.
8	RXE	0	R/W	Receive Enable When this bit is set to 1, the MSIOF starts data reception from the beginning of the next frame (at the rising edge of the frame synchronization signal). When value 1 set to this bit becomes valid, the MSIOF starts receiving data through the MSIOF_RXD pin. When receive data is stored in the receive FIFO, the MSIOF issues a receive data transfer request according to the setting of the RFWM bits in SIFCTR. This bit is initialized upon a receive reset. [Write data] 0: Disables data reception through MSIOF_RXD. 1: Enables data reception through MSIOF_RXD. [Read data] 0: Data is not received through MSIOF_RXD. 1: Data can be received through MSIOF_RXD.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
1	TXRST	0	R/W	Transmit Reset When value 1 set to this bit becomes valid, the MSIOF immediately sets transmit data through the MSIOF_TXD pin to 0, and initializes the transmit data registers and transmit-related status. When value 1 set to this bit becomes valid when PCON = 1, the RXRST bit is also becomes valid. The following registers and bits are initialized. SITFDR (Transmit FIFO write pointer) TDREQ bit in SISTR TXE bit This bit is read as 1 until the reset operation is completed for about 20 cycles of module clock. No data should be written to SICTR or the transmit FIFO during this time period. [Write data] 0: Does not reset transmit operation. 1: Resets transmit operation. [Read data] 0: Transmit operation reset is completed. 1: Transmit operation is being reset.
0	RXRST	0	R/W	Receive Reset When value 1 set to this bit becomes valid, the MSIOF immediately disables reception through the MSIOF_RXD pin, and initializes the receive data registers and receive-related status. The following registers and bits are initialized. SIRFDR (Receive FIFO read pointer) RDREQ bit in SISTR RXE bit This bit is read as 1 until the reset operation is completed for about 20 cycles of module clock. No data should be written to SICTR or read the receive FIFO during this time period. [Write data] 0: Does not reset receive operation. 1: Resets receive operation. [Read data] 0: Receive operation reset is completed. 1: Receive operation is being reset.

38.3.8 MSIOF Transmit Clock Select Register (SITSCR)

SITSCR is a 16-bit readable/writable register that specifies the conditions for generating transmit serial clock in master mode. SITSCR can be specified when the TRMD bit in SITMDR1 is set to B'1.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	MSSEL[1:0]		MSIMM	BRPS[4:0]					—	—	—	—	—	BRDV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
15, 14	MSSEL[1:0]	00	R/W	Master Clock Source Select The master clock is the clock input to the baud rate generator. 00: Selects module clock as the source of master clock. Others: Setting prohibited
13	MSIMM	0	R/W	Master Clock Direct Select When setting MSIMM = 1, the master clock source should be set to 26 MHz or lower. Set 0 when MSSEL = B'00. 0: Selects the clock output from the baud rate generator as the serial clock. 1: Setting is not available.
12 to 8	BRPS[4:0]	00000	R/W	Prescalar Setting These bits specify the master clock (MPϕ) division ratio in the count value of the prescalar in the baud rate generator. The specifiable value is from B'00000 (× 1/1) to B'11111 (× 1/32).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	BRDV[2:0]	000	R/W	Baud Rate Generator's Division Ratio These bits specify the frequency division ratio for the output stage of the baud rate generator. The final frequency division ratio of the baud rate generator is determined as BRPS × BRDV (1/1024 max.). 000: Prescalar output × 1/2 001: Prescalar output × 1/4 010: Prescalar output × 1/8 011: Prescalar output × 1/16 100: Prescalar output × 1/32 101: Setting prohibited 110: Setting prohibited 111: Prescalar output × 1/1 Note: B'111 is valid only when the BRPS[4:0] bits are set to B'00000 or B'00001.

38.3.9 MSIOF Transmit FIFO Data Register (SITFDR)

SITFDR is a 32-bit write-only register that specifies the transmit FIFO data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SITFD1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SITFD2[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SITFD1[15:0]	H'0000	W	These bits specify the upper 16 bits of the FIFO data to be output through MSIOF_TXD.
15 to 0	SITFD2[15:0]	H'0000	W	These bits specify the lower 16 bits of the FIFO data to be output through MSIOF_TXD.

38.3.10 MSIOF Receive FIFO Data Register (SIRFDR)

SIRFDR is a 32-bit read-only register that stores the receive FIFO data of the MSIOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SIRFD1[15:0]															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SIRFD2[15:0]															
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 16	SIRFD1[15:0]	Undefined	R	Store the upper 16 bits of the FIFO data received through MSIOF_RXD.
15 to 0	SIRFD2[15:0]	Undefined	R	Store the lower 16 bits of the FIFO data received through MSIOF_RXD.

38.3.11 MSIOF Status Register (SISTR)

Each bit in SISTR becomes an MSIOF interrupt source when the corresponding bit in SIIER is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	TFEMP	TDREQ	—	—	—	—	TEOF	—	TFS ERR	TFOVF	TFUDF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	RFFUL	RDREQ	—	—	—	—	REOF	—	RFS ERR	RFUDF	RFOVF	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31, 30	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
29	TFEMP	0	R/W	Transmit FIFO Empty This bit is set to 1, when the TXE bit in SICTR is 1, and transmit FIFO is empty. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: Transmit FIFO is not empty. 1: Transmit FIFO is empty.
28	TDREQ	0	R	Transmit Data Transfer Request This bit is set, when the empty space in the transmit FIFO exceeds the size specified by the TFWM bits in SIFCTR. When transferring transmit data through the DMAC, this bit is always cleared after one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the MSIOF again sets this bit to 1. This bit is valid when the TXE bit in SICTR is 1. This bit indicates a state; if the size of empty space in the transmit FIFO becomes less than the size specified by the TFWM bits in SIFCTR, the MSIOF clears this bit. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. However, when the TDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of empty space in the transmit FIFO has not exceeded the size specified by the TFWM bits in SIFCTR. 1: The size of empty space in the transmit FIFO has exceeded the size specified by the TFWM bits in SIFCTR.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
23	TEOF	0	R/W	Frame Transmission End This bit is set, when one-frame data transmission is completed. This bit is valid when the TXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: One-frame transmission end is not detected. 1: One-frame transmission end is detected.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERR	0	R/W	Transmit Frame Synchronization Error This bit is set, when the next transmit frame synchronization timing arrives before the previous data or control data transmission has been completed. If a transmit frame synchronization error occurs, the MSIOF performs transmission only for the slots that can be transferred. This bit is valid when the TXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No transmit frame synchronization error has occurred. 1: A transmit frame synchronization error has occurred.
20	TFOVF	0	R/W	Transmit FIFO Overflow A transmit FIFO overflow means that there has been an attempt to write to SITFDR when the transmit FIFO is full. If a transmit FIFO overflow occurs, the MSIOF ignores the write operation causing the overflow. This bit is valid when the TXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No transmit FIFO overflow has occurred. 1: A transmit FIFO overflow has occurred.
19	TFUDF	0	R/W	Transmit FIFO Underflow A transmit FIFO underflow means that loading for transmission has occurred when the transmit FIFO is empty. Output data is unknown when under flow is occurred. This bit is valid when the TXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No transmit FIFO underflow has occurred. 1: A transmit FIFO underflow has occurred.
18 to 14	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
13	RFFUL	0	R/W	Receive FIFO Full This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: Receive FIFO is not full. 1: Receive FIFO is full.
12	RDREQ	0	R	Receive Data Transfer Request This bit is set, when the valid data space in the receive FIFO exceeds the size specified by the RFWM bits in SIFCTR. When transferring receive data through the DMAC, this bit is always cleared by one DMAC access. After DMAC access, when the conditions for setting this bit are satisfied, the MSIOF again sets this bit to 1. This bit is valid when the RXE bit in SICTR is 1. This bit indicates a state; if the size of valid data space in the receive FIFO becomes less than the size specified by the RFWM bits in SIFCTR, the MSIOF clears this bit. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. However, when the RDMAE bit is 1, only a DMAC transfer request is issued. 0: The size of valid data space in the receive FIFO has not exceeded the size specified by the RFWM bits in SIFCTR. 1: The size of valid data space in the receive FIFO has exceeded the size specified by the RFWM bits in SIFCTR.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOF	0	R/W	Frame Reception End The MSIOF issues the frame reception end flag upon completion of one-frame data reception. This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: One-frame reception end is not detected. 1: One-frame reception end is detected.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
5	RFSERR	0	R/W	Receive Frame Synchronization Error A receive frame synchronization error occurs when the next receive frame synchronization timing arrives before the previous data or control data reception has been completed. If a receive frame synchronization error occurs, the MSIOF performs reception only for the slots that can be transferred. This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit will clear this bit. Writing 0 to this bit will be ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No receive frame synchronization error has occurred 1: A receive frame synchronization error has occurred
4	RFUDF	0	R/W	Receive FIFO Underflow A receive FIFO underflow means that reading of SIRFDR has occurred when the receive FIFO is empty. If a receive FIFO underflow occurs, the value read from SIRFDR is not guaranteed. This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No receive FIFO underflow has occurred. 1: A receive FIFO underflow has occurred.
3	RFOVF	0	R/W	Receive FIFO Overflow A receive FIFO overflow means that writing has been caused by receiving operation when the receive FIFO is full. If a receive FIFO overflow occurs, the receive data causing the overflow is lost. This bit is valid when the RXE bit in SICTR is 1. Writing 1 to this bit clears this bit. Writing 0 to this bit is ignored. If the interrupt request from this bit is enabled, an MSIOF interrupt is issued. 0: No receive FIFO overflow has occurred. 1: A receive FIFO overflow has occurred.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.12 MSIOF Interrupt Enable Register (SIIER)

SIIER is a 32-bit readable/writable register that enables the issuance of MSIOF interrupts. When each bit in this register is set to 1 and the corresponding bit in SISTR is set to 1, the MSIOF issues an interrupt.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TDMAE	—	TFEMPE	TDREQE	—	—	—	—	TEOFE	—	TFSERRE	TFOVFE	TFUDFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RDMAE	—	RFFULE	RDREQE	—	—	—	—	REOFE	—	RFSERRE	RFUDFE	RFOVFE	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31	TDMAE	0	R/W	Transmit Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The TDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
30	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
29	TFEMPE	0	R/W	Transmit FIFO Empty Enable 0: Disables interrupts due to transmit FIFO empty. 1: Enables interrupts due to transmit FIFO empty.
28	TDREQE	0	R/W	Transmit Data Transfer Request Enable 0: Disables interrupts due to transmit data transfer requests. 1: Enables interrupts due to transmit data transfer requests.
27 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	TEOFE	0	R/W	Frame Transmission End Enable 0: Disables a frame transmission end interrupt. 1: Enables a frame transmission end interrupt.
22	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
21	TFSERRE	0	R/W	Transmit Frame Synchronization Error Enable 0: Disables interrupts due to transmit frame synchronization errors. 1: Enables interrupts due to transmit frame synchronization errors.
20	TFOVFE	0	R/W	Transmit FIFO Overflow Enable 0: Disables interrupts due to transmit FIFO overflow. 1: Enables interrupts due to transmit FIFO overflow.
19	TFUDFE	0	R/W	Transmit FIFO Underflow Enable 0: Disables interrupts due to transmit FIFO underflow. 1: Enables interrupts due to transmit FIFO underflow.

Bit	Bit Name	Initial Value	R/W	Descriptions
18 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	RDMAE	0	R/W	Receive Data DMA Transfer Request Enable Specifies whether to send an interrupt as an interrupt request to the CPU or a transfer request to the DMAC. The RDREQE bit can be set as the request source. 0: Sends an interrupt request to the CPU. 1: Sends a DMA transfer request to the DMAC.
14	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
13	RFFULE	0	R/W	Receive FIFO Full Enable 0: Disables interrupts due to receive FIFO full. 1: Enables interrupts due to receive FIFO full.
12	RDREQE	0	R/W	Receive Data Transfer Request Enable 0: Disables interrupts due to receive data transfer requests. 1: Enables interrupts due to receive data transfer requests.
11 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	REOFE	0	R/W	Frame Reception End Enable 0: Disables a frame reception end interrupt. 1: Enables a frame reception end interrupt.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	RFSERRE	0	R/W	Receive Frame Synchronization Error Enable 0: Disables interrupts due to receive frame synchronization errors. 1: Enables interrupts due to receive frame synchronization errors.
4	RFUDFE	0	R/W	Receive FIFO Underflow Enable 0: Disables interrupts due to receive FIFO underflow. 1: Enables interrupts due to receive FIFO underflow.
3	RFOVFE	0	R/W	Receive FIFO Overflow Enable 0: Disables interrupts due to receive FIFO overflow. 1: Enables interrupts due to receive FIFO overflow.
2 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.3.13 MSIOF FIFO Control Register (SIFCTR)

SIFCTR is a 32-bit readable/writable register that indicates the area available for the transmit/receive FIFO transfer.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TFWM[2:0]			—	—	TFUA[6:0]							—	—	—	—
Initial value:	0	0	0	0	0	1	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RFWM[2:0]			RFUA[8:0]									—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 29	TFWM[2:0]	000	R/W	Transmit FIFO Watermark A transfer request of the transmit FIFO is issued by the TDREQE bit in SIIER. The transmit FIFO always operates as a 64-stage FIFO regardless of the setting of these bits. 000: Issues a transfer request when 64 stages of the transmit FIFO are empty. 001: Issues a transfer request when 32 or more stages of the transmit FIFO are empty. 010: Issues a transfer request when 24 or more stages of the transmit FIFO are empty. 011: Issues a transfer request when 16 or more stages of the transmit FIFO are empty. 100: Issues a transfer request when 12 or more stages of the transmit FIFO are empty. 101: Issues a transfer request when 8 or more stages of the transmit FIFO are empty. 110: Issues a transfer request when 4 or more stages of the transmit FIFO are empty. 111: Issues a transfer request when 1 or more stages of transmit FIFO are empty.
28, 27	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
26 to 20	TFUA[6:0]	H'40	R	Transmit FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'0000000 (full) to B'1000000 (empty).
19 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Descriptions
15 to 13	RFWM[2:0]	000	R/W	Receive FIFO Watermark A transfer request of the receive FIFO is issued by the RDREQE bit in SIIER. The receive FIFO always operates as a 128-stage FIFO regardless of the setting of these bits. 000: Issues a transfer request when 1 stage or more of the receive FIFO are valid. 001: Issues a transfer request when 4 or more stages of the receive FIFO are valid. 010: Issues a transfer request when 8 or more stages of the receive FIFO are valid. 011: Issues a transfer request when 16 or more stages of the receive FIFO are valid. 100: Issues a transfer request when 32 or more stages of the receive FIFO are valid. 101: Issues a transfer request when 64 or more stages of the receive FIFO are valid. 110: Issues a transfer request when 128 stages of the receive FIFO are valid. The setting of 111 is prohibited.
12 to 4	RFUA[8:0]	H'000	R	Receive FIFO Usable Area Indicate the number of words that can be transferred by the CPU or DMAC as B'000000000 (empty) to B'010000000 (full).
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

38.4 Operation

38.4.1 Operating Mode

(1) Common transmit/receive mode

Common clock and frame synchronization signals are used for transmission and reception.

Master mode: MSIOF_SCK and MSIOF_SYNC are output.
Slave mode: MSIOF_SCK and MSIOF_SYNC are input.

38.4.2 Serial Clocks

(1) Clock output in master mode

In master mode, the baud rate generator is used to generate the serial clock. The division ratio is from 1/1 to 1/1024.

(2) Clock input in slave mode

In slave mode, the clock input for transmission and reception is used as the serial clock.

(3) Multiple channel function

This module provides the multiple channel function as shown in Figure 38.2.

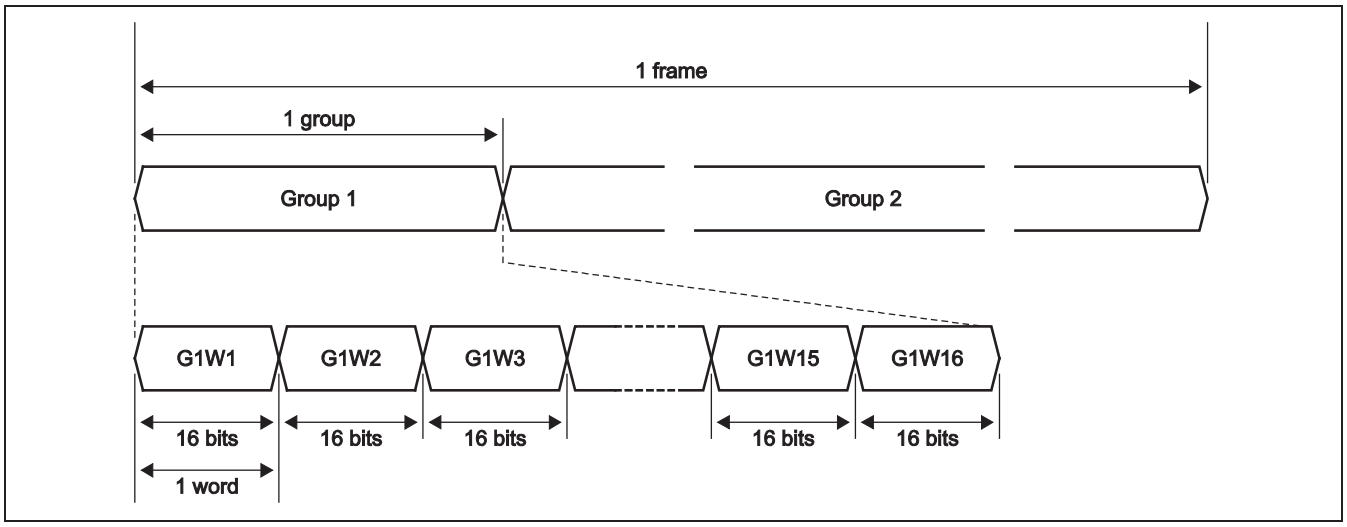


Figure 38.2 Multiple Channel Structure

The following conditions can be specified for the multiple channel function.

- Up to 2 groups in one frame
- Up to 64 words in one group
- 8, 16, 24, or 32 bits one word

38.4.3 Serial Timing

(1) MSIOF_SYNC

The MSIOF_SYNC is a frame synchronization signal. The following four modes are available.

- Frame start synchronization pulse: 1-bit-width pulse indicating the start of a frame
- Level/SPI: Level signal asserted during frame transmission
- L/R: 1/2-frame-width pulse indicating the first-half groups in a high level and the last-half groups in a low level

Figures 38.3 to 38.5 show the synchronization timing in these modes using the MSIOF_SYNC signal.

(a) Frame start synchronization pulse

The rising edge of the synchronization pulse indicates the start of a frame.

The delay between the rising edge of the synchronization signal and the start of data transmission or reception can be specified with the DTDL bits. The width of the synchronization pulse can be extended through the SYNCDL bit setting.

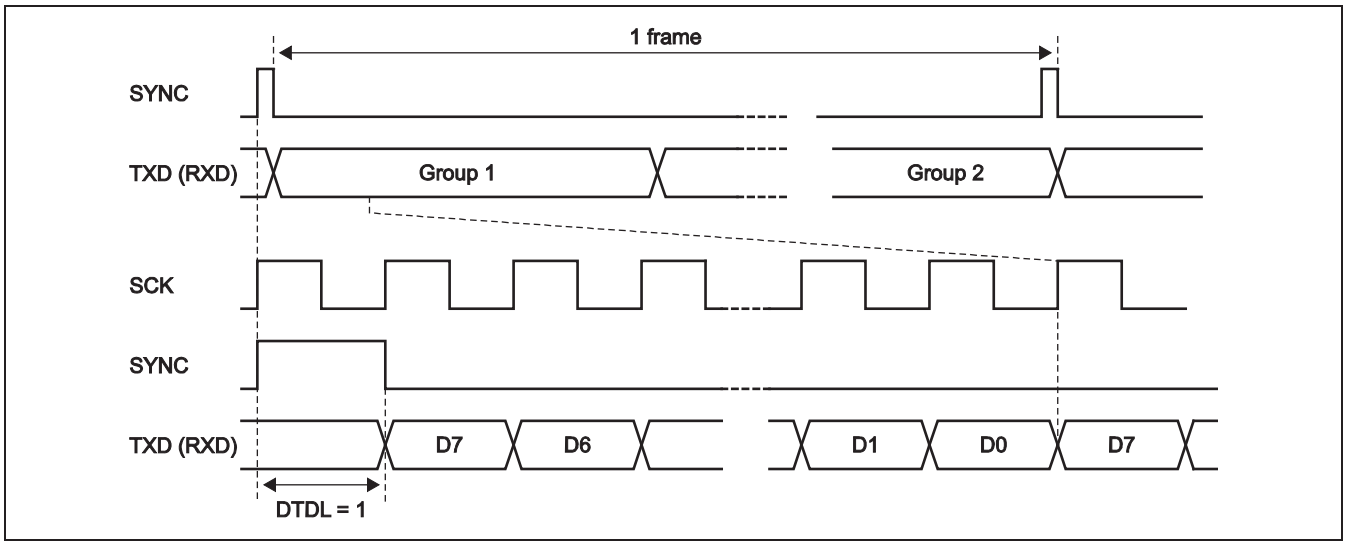


Figure 38.3 Synchronization Timing in Start Frame Synchronization Pulse Mode

(b) Level synchronization

The synchronization signal is driven high for the frame length.

The delay between the rising edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits and the delay between the end of transmission or reception and the falling edge of the synchronization signal can be specified with the SYNCDL bits (DTDL = 0 to 2 and SYNCDL = 0 to 3). This mode is available for the SPI master or slave operation.

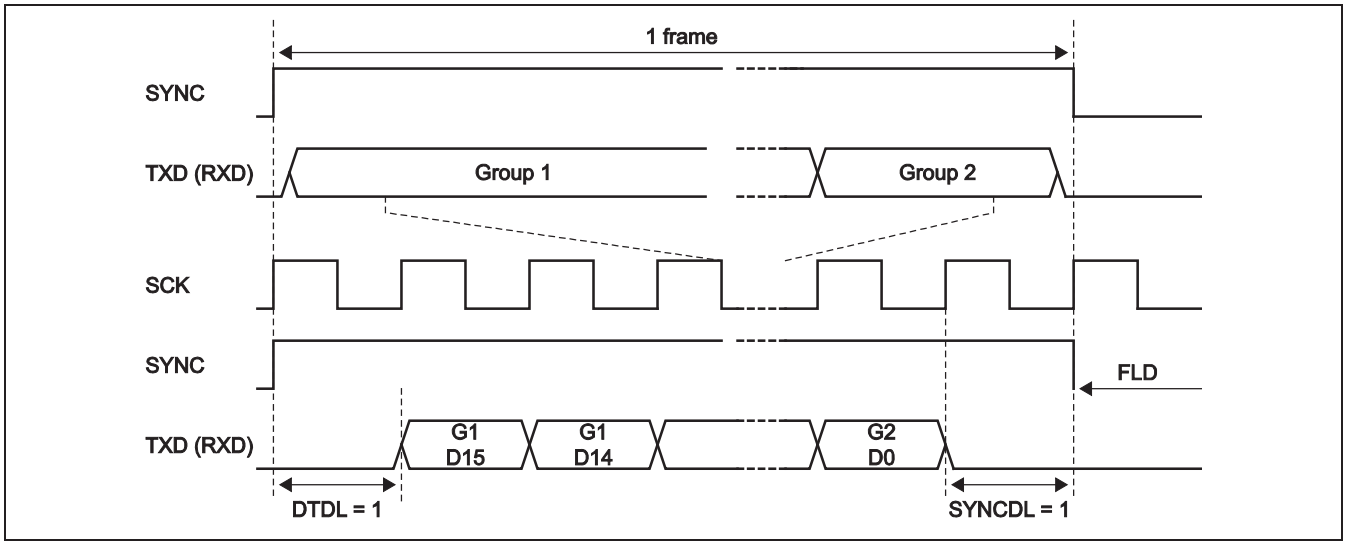


Figure 38.4 Synchronization Timing in Level Synchronization Mode

(c) L/R synchronization

A high level in the synchronization signal indicates the first-half groups and a low level indicates the last-half groups.

The delay between the rising or falling edge of the synchronization signal and the start of transmission or reception can be specified with the DTDL bits.

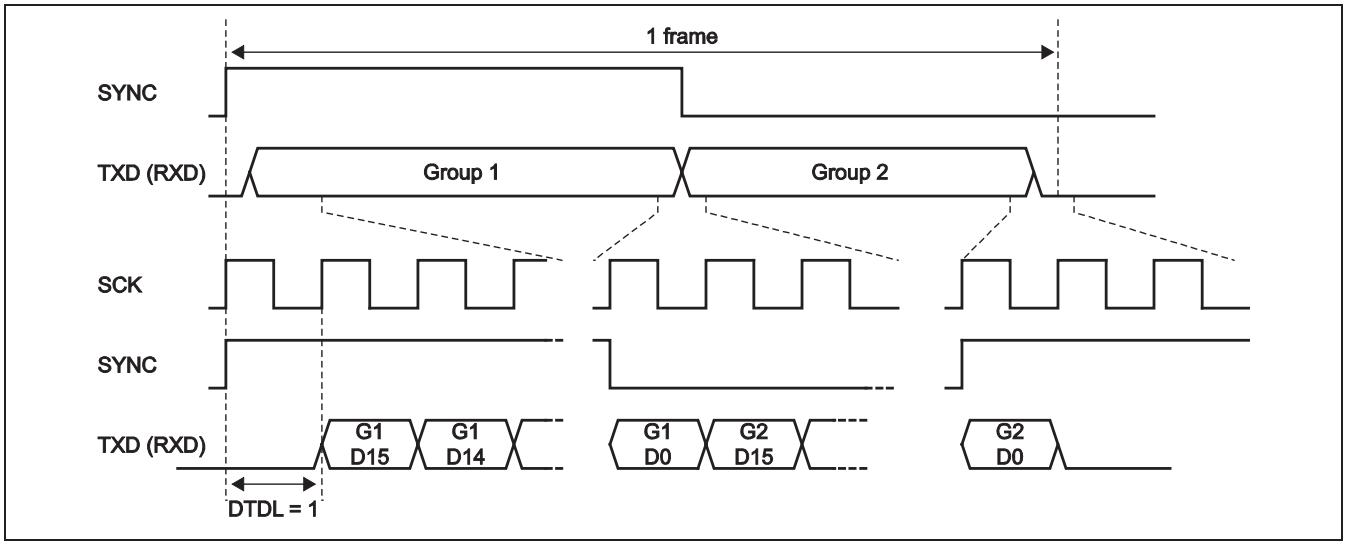


Figure 38.5 Synchronization Timing in L/R Synchronization Mode

(2) Transmit/receive timing

The timing of MSIOF_TXD transmission relative to MSIOF_SCK and of MSIOF_RXD can be specified as sampling on either edge, as listed below. The respective settings are made in TEDG and REDG bits of SICTR.

- Falling-edge sampling
- Rising-edge sampling

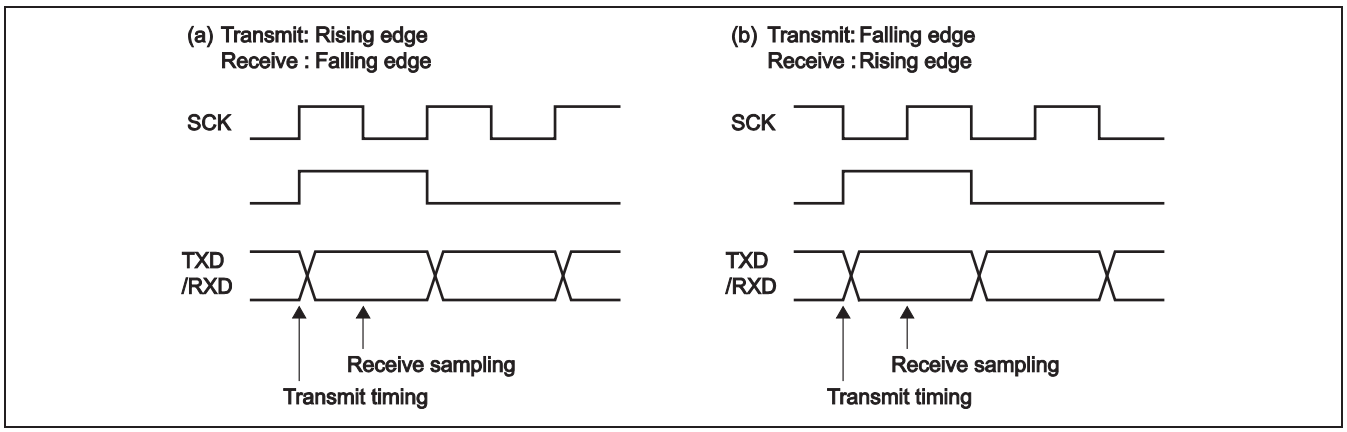


Figure 38.6 Transmit/Receive Timing

38.4.4 Transfer Data Allocation to Registers

(1) Transmit/receive data

Transmit/receive data (FIFO data and control data) should be written to or read from the following registers.

- Transmit FIFO data writing: SITFDR (32-bit access only by both CPU and DMAC)
- Receive FIFO data reading: SIRFDR (32-bit access only by both CPU and DMAC)

Figure 38.7 shows the bit alignment of these registers.

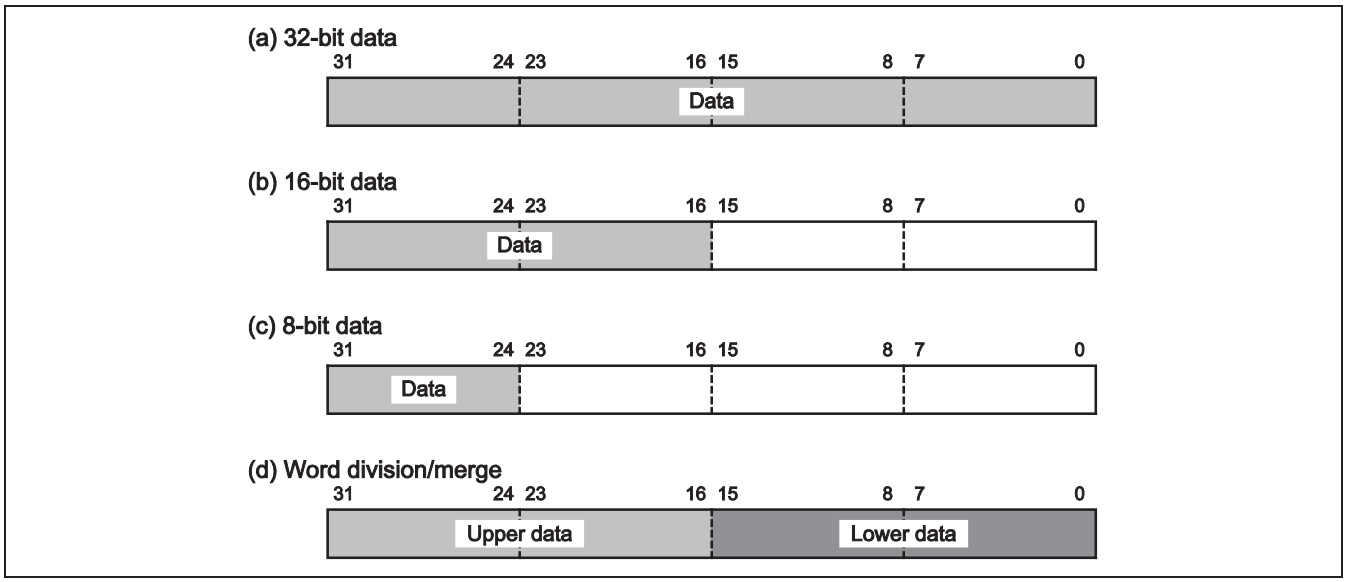


Figure 38.7 Transmit/Receive Data Bit Alignment

38.4.5 FIFO

(1) Overview

The transmit and receive FIFOs of the MSIOF have the following features.

- 32 bits × 64 stages for transmission and 32 bits × 128 stages for reception
- The FIFO pointer is updated in one read or write cycle regardless of the access size of the CPU or DMAC. (One access cannot be divided into multiple accesses.)

(2) Transfer request

A request for FIFO data transfer can be issued to the CPU or DMAC as the following interrupt sources.

- FIFO transmit request: TDREQ (interrupt source for transmission)
- FIFO receive request: RDREQ (interrupt source for reception)

The conditions for requesting FIFO data transfer can be specified separately for transmission and reception. The conditions for the transmit FIFO and receive FIFO are specified in the TFWM[2:0] bits and RFWM[2:0] bits in SIFCTR, respectively.

Table 38.5 Condition for Issuing Transmit Request

TFWM[2:0]	Number of Requested Stages	Condition for Transmit Request	Areas Used
000	1	64 stages of empty area	Smallest
001	32	32 or more stages of empty area	
010	40	24 or more stages of empty area	
011	48	16 or more stages of empty area	
100	52	12 or more stages of empty area	
101	56	8 or more stages of empty area	
110	60	4 or more stages of empty area	
111	64	1 or more stages of empty area	Largest

Table 38.6 Condition for Issuing Receive Request

RFWM[2:0]	Number of Requested Stages	Condition for Receive Request	Areas Used
000	1	1 or more stages of valid data	Smallest
001	4	4 or more stages of valid data	
010	8	8 or more stages of valid data	
011	16	16 or more stages of valid data	
100	32	32 or more stages of valid data	
101	64	64 or more stages of valid data	
110	128	128 stages of valid data	Largest

The maximum FIFO stages are always available even if the data area or empty area exceeds the size specified for the transfer condition. Accordingly, an overflow error or an underflow error occurs if the data area or empty area exceeds the maximum number of FIFO stages.

The FIFO transfer request is canceled when the specified condition is not satisfied even if the FIFO does not become empty or full.

(3) Number of FIFOs

The number of transmit and receive FIFO stages used are indicated by the following registers.

- Transmit FIFO: The number of empty FIFO stages is indicated by the TFUA[6:0] bits in SIFCTR.
- Receive FIFO: The number of valid data stages is indicated by the RFUA[8:0] bits in SIFCTR.

These registers show the number of data stages that can be transferred by the CPU. DMA transfer should be set the number of stage 1.

38.4.6 Transmit and Receive Procedures

(1) Transmission in master mode

Figure 38.8 shows an example of settings and operation for transmission in master mode.

No.	Operating flow	Description	Operation
1	SITMDR1/2/3 SITSCR SIFCTR SIIER setting	Operating mode Clock setting FIFO water mark Setting interrupt/DMA enable	
2	SICTR Set SICTR.TSCKE to 1	Transmission rate setting Baud rate generator starting	Output serial clock
3	TSCKE = 1 ? NO / YES	Read SICTR.TSCKE = 1	
4	SITFDR SITMDR1/2 setting	Write transmission data to FIFO	
5	Set SICTR.TXE to 1	Transmission enable	
6	TXE = 1 ? NO / YES	Read SICTR.TXE = 1	
7	Set SICTR.TFSE to 1	Starting MSIOF_SYNC output	
8	TFSE = 1 ? NO / YES	Read SICTR.TFSE = 1	
9	Starting transmission		Data transmission
10	TDREQ = 1 ? NO / YES		Generating interrupt/DMA request
11	Write transmission data to FIFO		
12	Transmission end ? NO / YES		
13	Set SICTR.TFSE to 0	Frame sync disable	
14	TFSE = 0 ? NO / YES	Read SICTR.TFSE = 0	
15	Set SICTR.TXE to 0	Transmission disable	
16	TXE = 0 ? NO / YES Finish	Read SICTR.TXE = 0	

Figure 38.8 Example of Transmit Procedure in Master Mode

(2) Reception in master mode (with SITMDR1.PCON = 1)

Figure 38.9 shows an example of settings and operation for reception in master mode with SITMDR1.PCON = 1.

No.	Operating flow	Description	Operation
1	SIRMDR1/2/3 SITMDR1/2/3 SITSCR SIFCTR SIIER setting	Operating mode Operating mode (for SPI dummy transmission) Serial clock FIFO water mark Interrupt/DMA setting	
2	SICTR Set SICTR.TSCKE to 1	Baud rate setting Baud rate generator starting	Output serial clock
3	TSCKE = 1 ? NO YES	Read SICTR.TSCKE = 1	
4	SITFDR SITMDR1/2 setting	Write dummy transmission data to SITFDR The number of dummy data should equal the number of reception data.	
5	Set SICTR.TXE to 1 Set SICTR.RXE to 1	Transmission enable Reception enable	
6	TXE = 1 ? RXE = 1 ? NO YES	Read SICTR.TXE = 1 Read SICTR.RXE = 1	
7	Set SICTR.TFSE to 1	Frame sync enable	Output MSIOF_SYNC
8	TFSE = 1 ? NO YES	Read SICTR.TFSE = 1	
9	Synchronizing with MSIOF_SYNC (1) Transmission FIFO dummy data (2) Reception data		Transmission and reception
10	TDREQ=1? RDREQ=1? NO YES		Generating interrupt/DMA request
11	Write dummy data to FIFO Read fifo data from SIRFDR	Transmission dummy data Reception data reading	
12	Transmission/ reception end? NO YES		
13	Set SICTR.TFSE to 0	Disable frame sync enable	
14	TFSE = 0 ? NO YES	Read SICTR.TFSE = 0	
15	Set SICTR.TXE and SICTR.RXE to 0	Disable transmission enable and reception enable	
16	TXE = 0 ? RXE = 0 ? NO YES Finish	Read SICTR.TXE = 0 Read SICTR.RXE = 0	

Figure 38.9 Example of Receive Procedure in Master Mode (SITMDR1.PCON = 1)

(3) Transmission in slave mode

Figure 38.10 shows an example of settings and operation for transmission in slave mode.

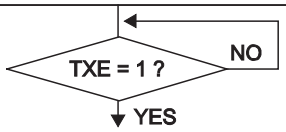
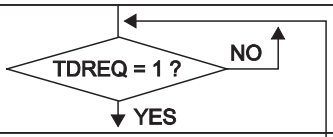
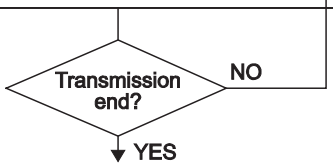
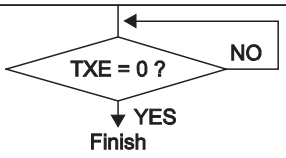
No.	Operating flow	Description	Operation
1	Master device setting	Depend on master device	Signal polarity
2	SITMDR1/2/3 SIFCTR SIIER setting	Operating mode FIFO water mark Interrupt/DMA enable	
3	SITFDR SITMDR1/2 setting	Transmission data setting	
4	Set SICTR.TXE to 1	Setting transmission enable	
5		Read SICTR.TXE = 1	
6	Data transmission synchronize with MSIOF_SYNC		Data transmission
7			Generating interrupt/DMA request
8	Write FIFO data to SITFDR	Data transmission	
9			
10	Set SICTR.TXE to 0	Transmission disable	
11		Read SICTR.TXE = 0	

Figure 38.10 Example of Transmit Procedure in Slave Mode

(4) Reception in slave mode

Figure 38.11 shows an example of settings and operation for reception in slave mode.

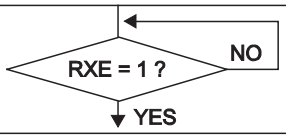
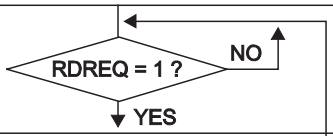
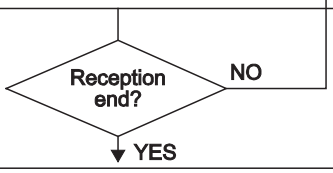
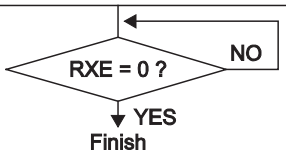
No.	Operating flow	Description	Operation
1	Master device setting	Depend on master device	Signal polarity
2	SIRMDR1/2/3 SIFCTR SIIER setting	Operating mode FIFO water mark Interrupt/DMA enable	
3	Set SICTR.RXE to 1	Setting receive enable	
4		Read SICTR.RXE = 1	
5	Data reception		Receive data
6			Generating interrupt/DMA request
7	Read SIRFDR	Data read from FIFO	
8			
9	Set SICTR.RXE to 0	Reception disable	
10		Read SICTR.RXE = 0	

Figure 38.11 Example of Receive Procedure in Slave Mode

(5) Reset

After a power-on reset is applied, module stop state is canceled, or a reset signal is asserted through the TXRST or RXRST setting in SICTR, it takes about 20 cycles of module clock to complete the internal reset of the module. During a period from the beginning of reset until the TXRST or RXRST value is read as 0, do not modify the control register or access the FIFOs.

The MSIOF can separately reset the transmit and receive units by setting the following bits to 1.

- Transmit reset: TXRST bit in SICTR
- Receive reset: RXRST bit in SICTR

Table 38.7 Transmit and Receive Reset

Type	Objects Initialized
Transmit reset	SITFDR (Transmit FIFO write pointer) TDREQ bits in SISTR TXE bit in SICTR
Receive reset	SIRFDR (Receive FIFO read pointer) RDREQ bits in SISTR RXE bit in SICTR

(6) Initial operating mode

After a power-on reset, both transmit and receive units are initialized to master mode (0 is output through MSIOF_SCK and MSIOF_SYNC). When using slave mode, keep the connected device outputting 0 until the operating mode setting is completed.

38.4.7 Interrupts

The MSIOF has one type of interrupt.

(1) Interrupt sources

Interrupts can be generated by several sources. Each source is shown as an MSIOF status in SISTR. Table 38.8 lists the MSIOF interrupt sources.

Table 38.8 MSIOF Interrupt Sources

No.	Classification	Bit Name	Function Name	Description
1	Transmission	TDREQ	Transmit FIFO transfer request	The transmit FIFO has empty space of specified size or more.
2		TFEMP	Transmit FIFO empty	The transmit FIFO is empty.
3		TEOF	Frame transmission end	Transmission of data with a length of one frame is completed.
4	Reception	RDREQ	Receive FIFO transfer request	The receive FIFO stores data of specified size or more.
5		RFFUL	Receive FIFO full	The receive FIFO is full.
6		REOF	Frame reception end	Reception of data with a length of one frame is completed.
7	Error	TFUDF	Transmit FIFO underflow	Serial data transmit timing has arrived while the transmit FIFO is empty.
8		TFOVF	Transmit FIFO overflow	The transmit FIFO is written to while it is full.
9		RFOVF	Receive FIFO overflow	Serial data is received while the receive FIFO is full.
10		RFUDF	Receive FIFO underflow	The receive FIFO is read while the receive FIFO is empty.
11		TFSERR	Transmit FS error	A transmit frame synchronization signal is input before the specified number of bits has been reached (in slave mode).
12		RFSERR	Receive FS error	A receive frame synchronization signal is input before the specified number of bits has been reached (in slave mode).

Whether an interrupt is issued from an interrupt source is determined by the SIIER settings. If an interrupt source bit is set to 1 and the corresponding bit in SIIER is set to 1, an MSIOF interrupt is issued.

(2) TDREQ and RDREQ

The transmit FIFO transfer request (TDREQ) and receive FIFO transfer request (RDREQ) are signals indicating the state. If the state changes after TDREQ or RDREQ is set, it is automatically cleared by the MSIOF.

When the DMA transfer is used, a DMA transfer request signal is pulled low for one cycle at the end of DMA transfer.

(3) Processing when errors occur

- Transmit FIFO underflow (TFUDF)
  The value specified with TXDIZ in SICTR is output.
- Transmit FIFO overflow (TFOVF)
  The contents of the transmit FIFO are protected, and the write operation causing the overflow is ignored.
- Receive FIFO overflow (RFOVF)
  Data causing the overflow is discarded and lost.
- Receive FIFO underflow (RFUDF)
  An undefined value is output on the bus.
- Transmit FS error (TFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.
- Receive FS error (RFSERR)
  The internal counter is reset according to the synchronization signal in which an error occurs.

38.4.8 Transmit and Receive Timing

Examples of the MSIOF serial transmission and reception are shown in Figures 38.12 and 38.13.

(1) 16-bit synchronization pulse

Synchronization pulse method, one group, one word, 16 bits in a word, no bit delay

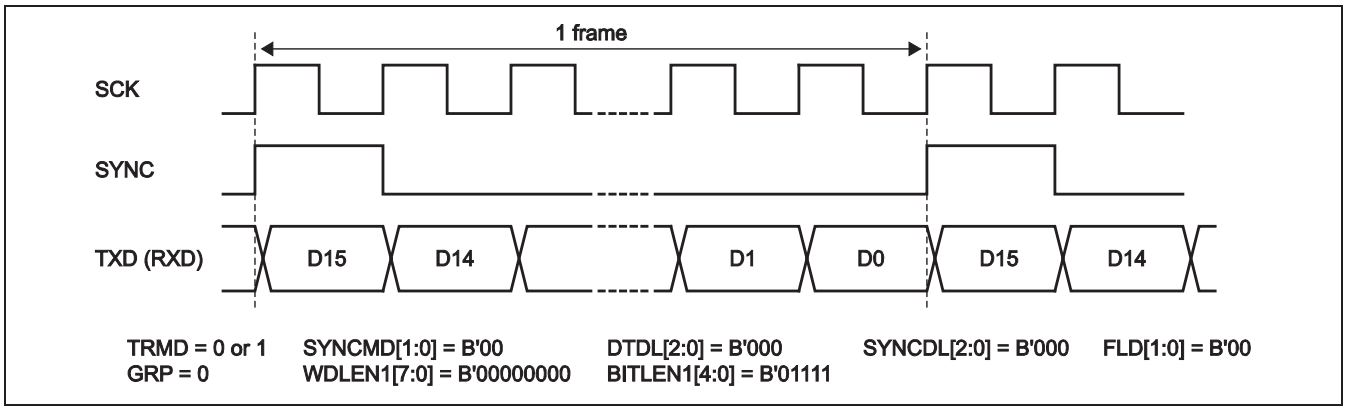


Figure 38.12 Transmit and Receive Timing (16 Bits)

(2) 32-bit synchronization pulse

Synchronization pulse method, one group, 32 words, 32 bits in a word, 1-bit delay

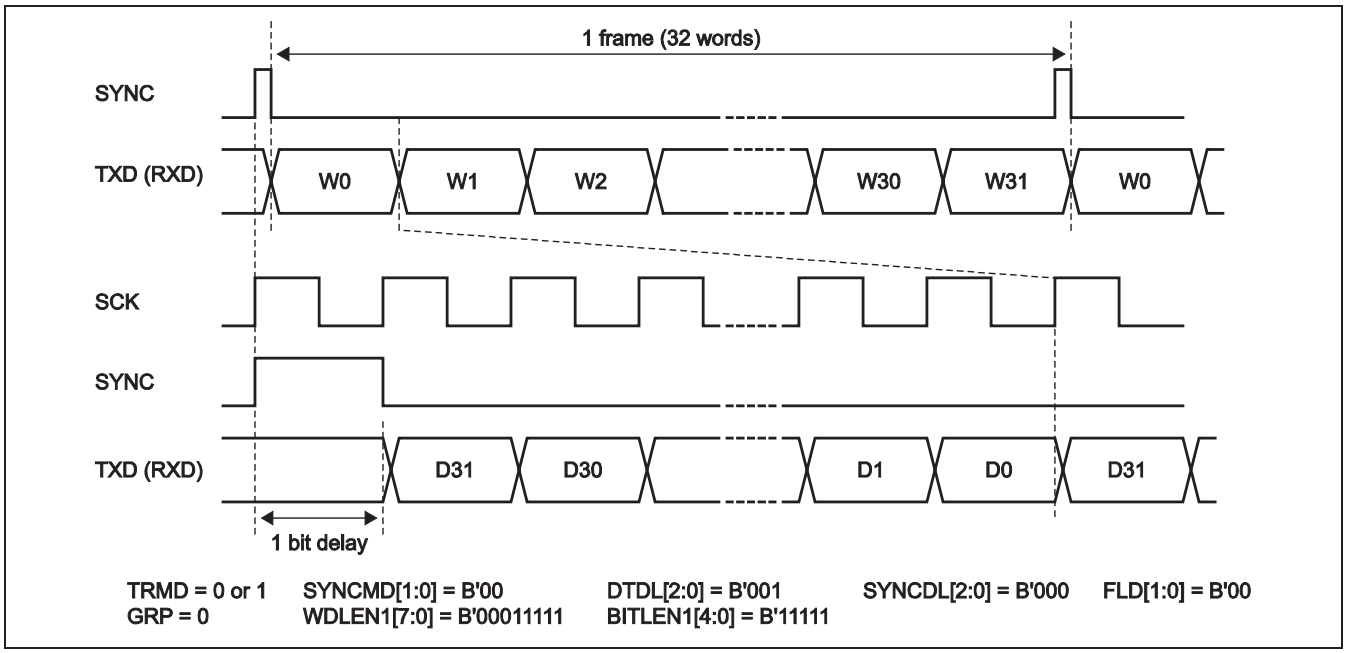


Figure 38.13 Transmit and Receive Timing (32 Bits)

(3) 32-bit iis transmission

L/R mode, 2 groups, 1 word for each group, 32-bit word for each group, 1-bit delay

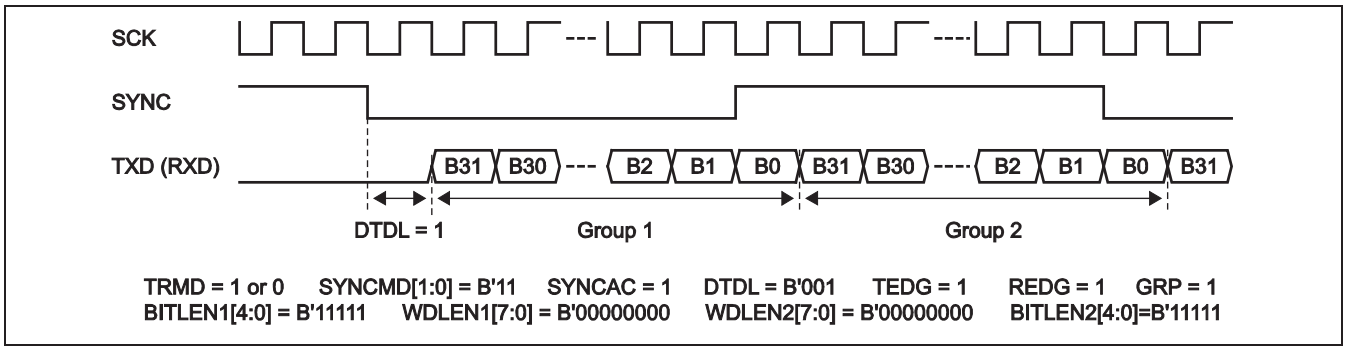


Figure 38.14 Transmit Timing (24-Bit IIS)

38.4.9 SPI

With the appropriate register settings, the MSIOF can be used as an SPI device.

(1) Example of SPI device connection

Figure 38.15 shows an example of connection with an SPI device.

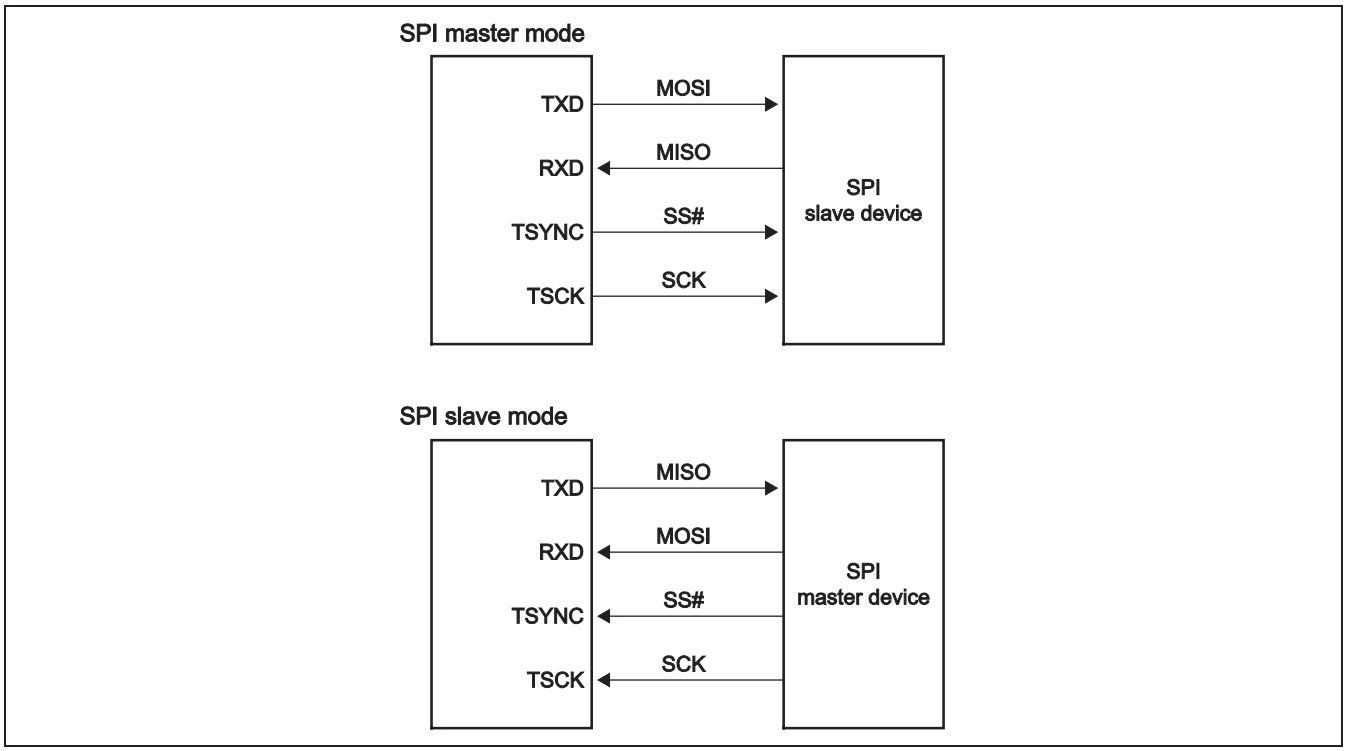


Figure 38.15 Example of SPI Device Connection

(2) SPI serial clock timing

Figures 38.16 and 38.17 show the data and clock timing in SPI mode. As shown in the figures, four types of serial transfer formats can be used.

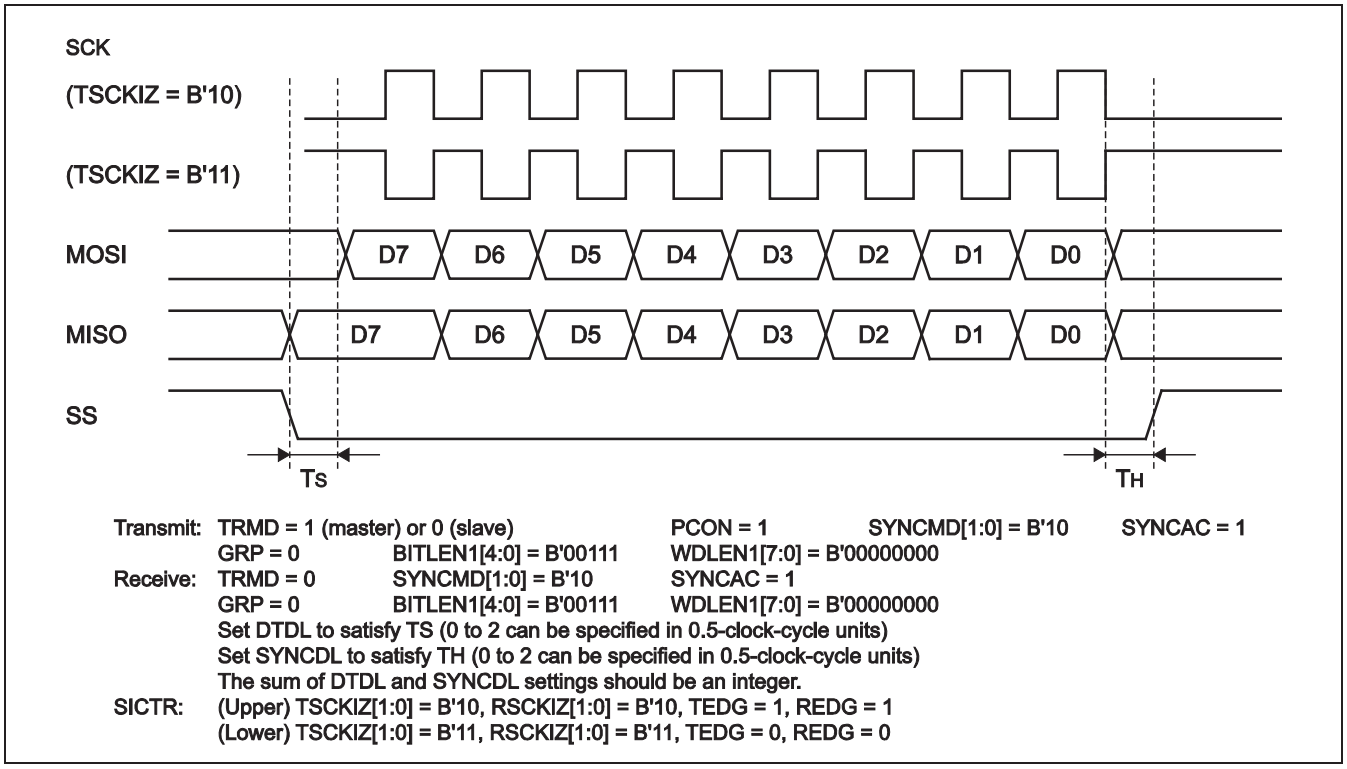


Figure 38.16 SPI Clock and Data Timing 1

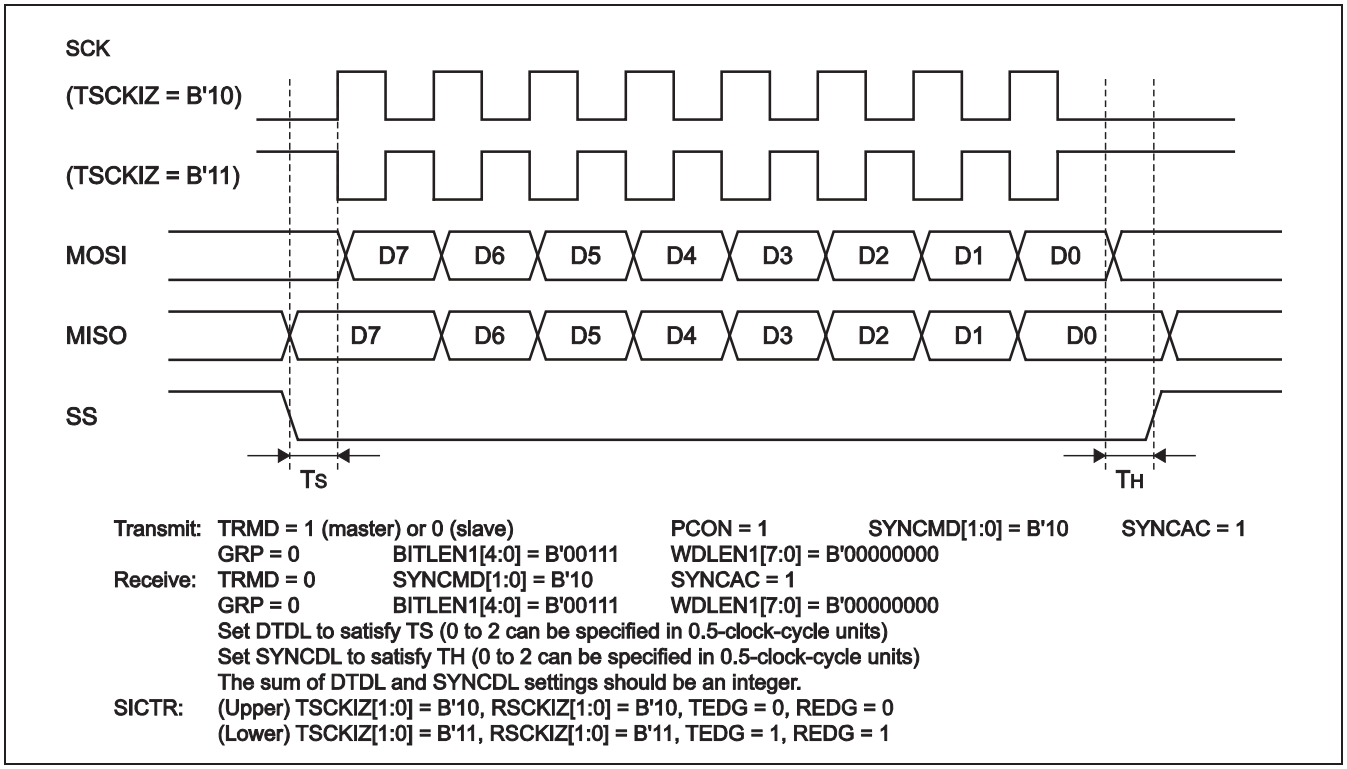


Figure 38.17 SPI Clock and Data Timing 2

38.4.10 Notes for Using SPI Mode

- For SPI master mode operation, set the FLD bits in SITMDR1 for at least 3 cycles of module clock.
- For SPI slave mode operation, set the frame synchronization signal interval to at least 4 cycles of module clock.
- For SPI slave mode operation, the setting for data delay should be always set to 0.
- For SPI slave mode operation, TXDIZ bits work on SS signal invalid state.
- Limitation:

  When the MSIOF operates with all of the following condition 1 to 3, the MSIOF in SPI slave mode cannot start the next transmission. The MSIOF cannot support SPI mode under following condition.

  1) MSIOF is in SPI slave mode (SITMDR1.TRMD = 0, SITMDR1.SYNCMD[1:0] = 10)

  2) SYNC (CS) signal is being asserted from master

  3) TXE or RXE in SICTR is set to 1 during SYNC (CS) is asserted

  — Description:

  This limitation means the MSIOF cannot respond to the SYNC (CS).

  It is necessary to control the MSIOF enabling timing by the master and system.

  — Work-around

  Use master mode for SPI.

  If use slave mode for SPI, consider following alternative.

  — Alternative

  If the master device can support handshaking, use the handshaking transmission.

  For the MSIOF in SPI slave mode, use with the GPIO output for SPI handshaking; the system operation must be tested and evaluated thoroughly by user.

38.4.11 IIS

This module can support IIS format with following setting which is shown in Figures 38.18 and 38.19. BITLEN1 and BITLEN2 bits will change by usage.

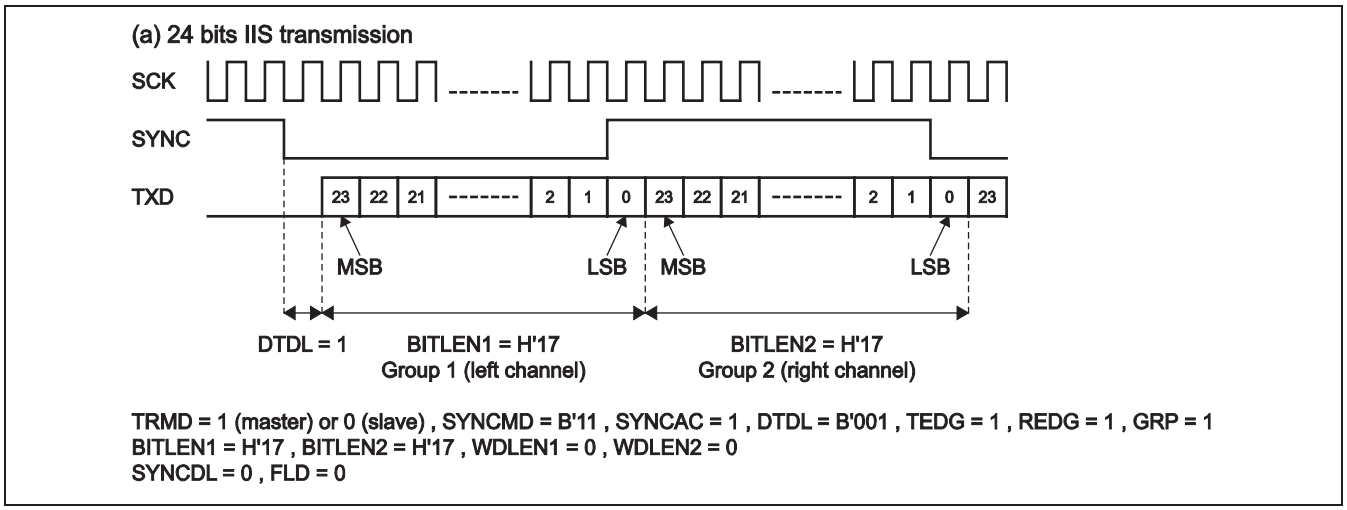


Figure 38.18 24 Bits IIS Transmission

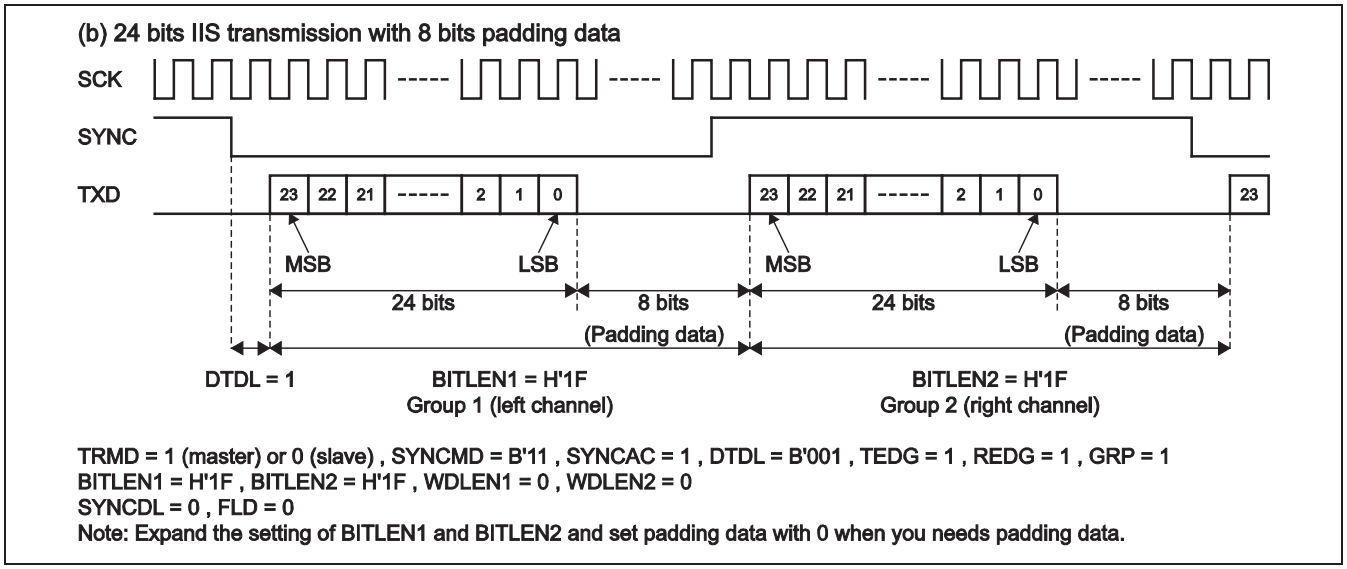


Figure 38.19 24 Bits IIS Transmission with 8 Bits Padding Data

39. Quad Serial Peripheral Interface

39.1 Overview

This LSI has two channels of QSPI. Features and functions of each product are basically the same, however, read value of WSWAP bit of SPCR register and BSWAP bit of SPCR register are always 0. See section 39.4.1.

39.2 Features

This module has the following features.

- Capable of serial communications through single-/dual-/quad-SPI operation
  - — Single-SPI operation
    Use of MOSI (master out–slave in), MISO (master in–slave out), SSL (slave select), and SPCLK (SPI clock) signals allows for serial access (four-wire method).
    Single-direction MOSI and MISO pins.
    Only master mode is available.
    SSL and SPCLK serve as output pins.
  - — Dual-SPI operation
    Use of IO1, IO0, SSL, and SPCLK signals allows for serial access (four-wire method).
    Bidirectional IO1 and IO0 pins.
    Only master mode is available.
  - — Quad-SPI operation
    Use of IO3 to IO0, SSL, and SPCLK signals allow for serial access (six-wire method).
    Bidirectional IO3 to IO0 pins.
    Only master mode is available.
- Transfer data length
  Transfer data length is selectable from 8 bits to 128 Gbits in single-SPI master mode or dual-/quad-SPI modes.
  Data is continuously transferred one through 4,294,967,296 times in 8-, 16-, or 32-bit units.
- Bit rate
  SPCLK is generated by the on-chip baud rate generator, by dividing QSPIϕ with division rate 1 to 4080 in master mode.
  (SPCLK can be generated by dividing QSPIϕ by the on-chip baud rate generator.)
- Buffer configuration
  8 bits × 32 buffers for transmission and 8 bits × 32 buffers for reception
- Shift registers
  32 bits each for transmission and reception
- SSL pin control function
  Master mode: Controllable delay from SSL output assertion to SPCLK operation (clock delay)
  Range: 0 to 8 SPCLK cycles (set in one SPCLK-cycle units)
  Controllable delay from SPCLK stoppage to SSL output negation (SSL negation delay)
  Range: 0 to 8 SPCLK cycles (set in one SPCLK-cycle units)
  Controllable wait for next-access SSL output assertion (next-access delay)
  Range: 0 to 8 SPCLK cycles (set in one SPCLK-cycle units)
  Capable of holding SSL output value from transfer end to next access
  Function for changing SSL polarity

- Master transfer control

  A transfer of up to four commands can be executed sequentially in looped execution.

  Single-SPI mode or dual-/quad-SPI write operation: A transfer can be started when data is written to the transmit buffer.

  Dual-/quad-SPI read operation: A transfer can be started when the SPI function is enabled while there is enough space for receiving the specified length of data in the receive buffer.

  IO3 to IO0 and MOSI output values can be specified during SSL negation.

  IO3 and IO2 output values can be specified in single-/dual-SPI modes.
- Interrupt sources

  Maskable interrupt sources:

  Receive buffer full interrupt

  Transmit buffer empty interrupt

  Error interrupt (underrun error, overrun error, and mode fault error)
- Others

  Provides loop back mode.

  Provides a function for initializing this module.

Hereafter, the single-/dual-/quad-SPI master modes are collectively called the maser mode.

39.3 Input/Output Pins

Table 39.1 shows the pin configuration.

Table 39.1 Pin Configuration

Name	Pin Name	I/O	Function
Clock pin	SPCLK	I/O	Clock input/output
Master transmit data pin/data 0 pin*1	MOSI/IO0	I/O	Master transmit data/data 0
Slave transmit data pin/data 1 pin*1	MISO/IO1	I/O	Slave transmit data/data 1
Data 2 pin*2	IO2	I/O	Data 2
Data 3 pin*2	IO3	I/O	Data 3
Slave select pin	SSL	I/O	Slave selection

Notes: 1. In single-SPI mode, MOSI and MISO are enabled; IO0 and IO1 in dual-/quad-SPI modes.
2. In single-/dual-SPI modes, a fixed value according to register setting is output; IO2 and IO3 are output in quad-SPI mode.

39.4 Register Descriptions

Table 39.2 shows the register configuration. The base address of QSPI0 is H'E6B1_0000, QSPI1 is H'EE20_0000.

Table 39.2 Register Configuration

Register Name	Abbreviation	R/W	Initial Value	Address	Access Size
Control register	SPCR	R/W	H'00000660	H'00	8, 16, 32
Slave select polarity register	SSLP	R/W	H'00000660	H'01	8, 16, 32
Pin control register	SPPCR	R/W	H'00000660	H'02	8, 16, 32
Status register	SPSR	R/(W)*	H'00000660	H'03	8, 16, 32
Data register	SPDR	R/W	Undefined	H'04	8, 16, 32
Sequence control register	SPSCR	R/W	H'0000FF00	H'08	8, 16, 32
Sequence status register	SPSSR	R	H'0000FF00	H'09	8, 16, 32
Bit Rate register	SPBR	R/W	H'0000FF00	H'0A	8, 16, 32
Data control register	SPDCR	R/W	H'0000FF00	H'0B	8, 16, 32
Clock delay register	SPCKD	R/W	H'00000000	H'0C	8, 16, 32
Slave select negation delay register	SSLND	R/W	H'00000000	H'0D	8, 16, 32
Next-access delay register	SPND	R/W	H'00000000	H'0E	8, 16, 32
Command register 0	SPCMD0	R/W	H'E001E001	H'10	16, 32
Command register 1	SPCMD1	R/W	H'E001E001	H'12	16, 32
Command register 2	SPCMD2	R/W	H'E001E001	H'14	16, 32
Command register 3	SPCMD3	R/W	H'E001E001	H'16	16, 32
Buffer control register	SPBFCR	R/W	H'00000000	H'18	8, 16, 32
Buffer data count register	SPBDCR	R/W	H'00000000	H'1A	16, 32
Transfer data length multiplier setting register 0	SPBMUL0	R/W	H'00000001	H'1C	32
Transfer data length multiplier setting register 1	SPBMUL1	R/W	H'00000001	H'20	32
Transfer data length multiplier setting register 2	SPBMUL2	R/W	H'00000001	H'24	32
Transfer data length multiplier setting register 3	SPBMUL3	R/W	H'00000001	H'28	32

Note: * Only 0 can be written to clear the flag.

39.4.1 Control Register (SPCR)

SPCR sets the operating mode. If the master/slave mode select bit (MSTR) is modified while the SPI function enable bit (SPE) is set to 1 (that is, this module is enabled), the subsequent operation cannot be guaranteed.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPRIE	SPE	SPTIE	SPEIE	MSTR	—	WSWAP	BSWAP	—	—	—	—	—	—	—	SSLP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MOIFE	MOIFV	—	IO3FV	IO2FV	SPLP	SPRFF	TEND	SPTEF	—	—	—	—	—
Initial value:	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	SPRIE	SPE	SPTIE	SPEIE	MSTR	—	WSWAP	BSWAP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	SPRIE	0	R/W	Receive Interrupt Enable Enables or disables generation of receive interrupt requests when the number of receive data units in the receive buffer is equal to or greater than the specified receive buffer data triggering number and the receive buffer full flag (SPRFF) in the status register (SPSR) is set to 1. 0: Disables the generation of receive interrupt requests. 1: Enables the generation of receive interrupt requests.
6	SPE	0	R/W	SPI Function Enable Setting this bit to 1 enables the SPI module function. Setting this bit to 0 initializes a part of the module function. 0: Disables the module function. 1: Enables the module function.
5	SPTIE	0	R/W	Transmit Interrupt Enable Enables or disables generation of transmit interrupt requests when the number of transmit data units in the transmit buffer is equal to or less than the specified transmit buffer data triggering number and the transmit buffer empty flag (SPTEF) in SPSR is set to 1. 0: Disables the generation of transmit interrupt requests. 1: Enables the generation of transmit interrupt requests.
4	SPEIE	0	R/W	Error Interrupt Enable Enables or disables generation of error interrupt requests when an underrun error, an overrun error, or a mode fault error is detected and the corresponding flag in SPSR is set to 1. 0: Disables the generation of error interrupt requests. 1: Enables the generation of error interrupt requests. Note: This setting is valid only in single-SPI slave mode.

Bit	Bit Name	Initial Value	R/W	Description
3	MSTR	0	R/W	Master/Slave Mode Select Selects the master or slave mode. This bit specifies the direction of the signals through the SPCLK and SSL pins. The slave mode can be selected only when the SPI operating mode is set to single-SPI. Master/slave switching should be done only while the SPE bit is 0; otherwise, the subsequent operation cannot be guaranteed. This module supports only the master mode; be sure to set this bit to 1 to use this module. 0: Slave mode 1: Master mode
2	—	0	R/W	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
1	WSWAP	0	R/W	Word Swap Selects word-swap of read-data for DMAC. By setting this bit to 1, read-data to DMAC is swapped in word units. That is, bit[31:16] and bit[15:0] are swapped. 0: No word swap for read-data for DMAC. 1: Perform word swap for read-data for DMAC. Note: The read value of this bit is always 0.
0	BSWAP	0	R/W	Byte Swap Selects byte-swap of read-data for DMAC. By setting this bit to 1, read-data to DMAC is swapped in byte units. That is, bit[31:24] and bit[23:16] are swapped, and at the same time, bit[15:8] and bit[7:0] are also swapped. 0: No byte swap for read-data for DMAC. 1: Perform byte swap for read-data for DMAC. Note: The read value of this bit is always 0.

39.4.2 Slave Select Polarity Register (SSLP)

SSLP sets the polarity of the SSL signal. If the contents of SSLP are modified while the SPE bit in the control register (SPCR) is set to 1, the subsequent operation cannot be guaranteed.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPRIE	SPE	SPTIE	SPEIE	MSTR	—	WSWAP	BSWAP	—	—	—	—	—	—	—	SSLP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MOIFE	MOIFV	—	IO3FV	IO2FV	SPLP	SPRFF	TEND	SPTEF	—	—	—	—	—
Initial value:	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	SSLP
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 1	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
0	SSLP	0	R/W	SSL Signal Polarity Setting Sets the polarity of the SSL signal. 0: SSL signal low-active 1: SSL signal high-active

39.4.3 Pin Control Register (SPPCR)

SPPCR sets the modes of the pins. If the contents of SPPCR are modified while the SPE bit in SPCR is set to 1, the subsequent operation cannot be guaranteed.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPRIE	SPE	SPTIE	SPEIE	MSTR	—	WSWAP	BSWAP	—	—	—	—	—	—	—	SSLP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MOIFE	MOIFV	—	IO3FV	IO2FV	SPLP	SPRFF	TEND	SPTEF	—	—	—	—	—
Initial value:	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	MOIFE	MOIFV	—	IO3FV	IO2FV	SPLP
Initial value:	0	0	0	0	0	1	1	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
5	MOIFE	0	R/W	Master-Mode Output Idle Value Fixing Enable Fixes the pin output value in an SSL negation period or the SSL keeping period during a burst transfer in master mode. In single-SPI mode, this bit setting applies to MOSI. In dual-SPI mode, the setting of this bit is applied to IO1 and IO0. In quad-SPI mode, the setting of this bit is applied to IO3 to IO0. 0: Output value equals final data from previous transfer. 1: Output value equals the value set in the MOIFV bit. Note: In dual-/quad-SPI modes, IO1 and IO0/IO3 to IO0 are driven to the Hi-Z state regardless of the setting of this bit (see section 39.5.2, Pin Control).
4	MOIFV	0	R/W	Master-Mode Output Idle Fixed Value If the MOIFE bit is 1 in master mode, this module, according to the setting of this bit, determines the output value during the SSL negation period. 0: Output pin idle fixed value equals 0. 1: Output pin idle fixed value equals 1.
3	—	0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.

Bit	Bit Name	Initial Value	R/W	Description
2	IO3FV	1	R/W	Single-/Dual-SPI Mode IO3 Output Fixed Value Fixes the output direction of the IO3 pin in single-/dual-SPI modes. This bit is valid only in single-/dual-SPI modes, and is not affected by the value of MOIFE or MOIFV bit. 0: IO3 output fixed value equals 0. 1: IO3 output fixed value equals 1.
1	IO2FV	1	R/W	Single-/Dual-SPI Mode IO2 Output Fixed Value Fixes the output direction of the IO2 pin in single-/dual-SPI modes. This bit is valid only in single-/dual-SPI modes, and is not affected by the value of MOIFE or MOIFV bit. 0: IO2 output fixed value equals 0. 1: IO2 output fixed value equals 1.
0	SPLP	0	R/W	Loopback Mode When the SPLP bit is set to 1, this module shuts off the path between the data I/O pin and the transmit/receive shift register, and connects the input path and the output path for the transmit/receive shift register. 0: Normal mode 1: Loopback mode Note: When the loopback mode is specified in dual-/quad-SPI modes, the SPI read/write access setting bit (SPRW) in command registers 0 to 3 (SPCMD0 to SPCMD3) should be set to 0 (write operation). Do not modify the setting of this bit during data transfer.

39.4.4 Status Register (SPSR)

SPSR indicates the operating status.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPRIE	SPE	SPTIE	SPEIE	MSTR	—	WSWAP	BSWAP	—	—	—	—	—	—	—	SSLP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	MOIFE	MOIFV	—	IO3FV	IO2FV	SPLP	SPRFF	TEND	SPTEF	—	—	—	—	—
Initial value:	0	0	0	0	0	1	1	0	0	1	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	SPRFF	TEND	SPTEF	—	—	—	—	—
Initial value:	0	1	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Note: Only 0 can be written to the flags after 1 is read.

Bit	Bit Name	Initial Value	R/W	Description
7	SPRFF	0	R	Receive Buffer Full Flag Indicates that the number of receive data units in the receive buffer is equal to or greater than the receive buffer data triggering number specified in the buffer control register. 0: The number of receive data units in the receive buffer is less than the receive buffer data triggering number. 1: The number of receive data units in the receive buffer is equal to or greater than the receive buffer data triggering number. [Clearing conditions] • The receive buffer data is read until the number of data units in the receive buffer becomes less than the specified receive buffer data triggering number. • Receive buffer data reset is enabled. • Power-on reset. [Setting condition] • The number of data units in the receive buffer is equal to or greater than the specified receive buffer data triggering number.

Bit	Bit Name	Initial Value	R/W	Description
6	TEND	1	R	Transmit End Flag This bit is set to 1 when transmission is completed, and this bit is 0 when transmission is not completed. [Clearing conditions] • When transmit data are moved from the transmit register to the transmit shift register. • When data reception is started in dual-/quad-SPI modes. [Setting conditions] • When the number of data units in the transmit buffer is zero when a serial transfer is completed (except when the dummy data transmission enable bit (TXDMY) is set to 1). • When there is not enough space for receiving the specified length of data in the receive buffer when a serial transfer is completed.
5	SPTEF	1	R	Transmit Buffer Empty Flag Indicates that the number of transmit data units in the transmit buffer is equal to or less than the transmit buffer data triggering number specified in the buffer control register. 0: The number of transmit data units in the transmit buffer exceeds the specified transmit buffer data triggering number. 1: The number of transmit data units in the transmit buffer is equal to or less than the specified transmit buffer data triggering number. [Clearing condition] • When data is written to the transmit buffer until the number of transmit data units in the transmit buffer exceeds the specified transmit buffer data triggering number. [Setting conditions] • When the number of transmit data units in the transmit buffer is equal to or less than the specified transmit buffer data triggering number. • When transmit buffer data reset is enabled. • Power-on reset.
4 to 0	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.

39.4.5 Data Register (SPDR)

SPDR accesses transmit/receive data buffer.

The transmit buffer (SPTXB) and receive buffer (SPRXB) are independent and are mapped to SPDR.

When data is written to SPDR, the data will be written to the transmit buffer.

When data is read from SPDR, the data will be read from the receive buffer.

SPDR should be read or written to in byte, word, or longword units.

When SPDR is read or written to with the longword-, word-, or byte-access width, the receive or transmit data should be read from or written to the following bits.

Longword: Bits 31 to 0
Word: Bits 15 to 0
Byte: Bits 7 to 0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPD31	SPD30	SPD29	SPD28	SPD27	SPD26	SPD25	SPD24	SPD23	SPD22	SPD21	SPD20	SPD19	SPD18	SPD17	SPD16
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPD15	SPD14	SPD13	SPD12	SPD11	SPD10	SPD9	SPD8	SPD7	SPD6	SPD5	SPD4	SPD3	SPD2	SPD1	SPD0
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

39.4.6 Sequence Control Register (SPSCR)

SPSCR sets the sequence control method when this module operates in master mode. If the contents of SPSCR are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	SPSC[1:0]		—	—	—	—	—	—	SPSS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPBR[7:0]								TXDMY	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SPSC[1:0]	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
1, 0	SPSC[1:0]	00	R/W	Sequence Control Specification These bits specify sequential operations when this module operates in master mode. In master mode, this module references SPCMD0 to SPCMD3 in the order according to the setting of these bits. 00: 0 → 0 → … 01: 0 → 1 → 0 → … 10: 0 → 1 → 2 → 0 → … 11: 0 → 1 → 2 → 3 → 0 → …

39.4.7 Sequence Status Register (SPSSR)

SPSSR indicates the sequence control status when this module operates in master mode.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	SPSC[1:0]		—	—	—	—	—	—	SPSS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPBR[7:0]								TXDMY	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	SPSS[1:0]	
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7 to 2	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
1, 0	SPSS[1:0]	00	R	Sequence Status During sequence control, these bits indicate one of SPCMD0 to SPCMD3 that is currently referenced. 00: SPCMD0 01: SPCMD1 10: SPCMD2 11: SPCMD3

39.4.8 Bit Rate Register (SPBR)

SPBR sets the bit rate when this module operates in master mode. If the contents of SPBR are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	SPSC[1:0]		—	—	—	—	—	—	SPSS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPBR[7:0]								TXDMY	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	SPBR[7:0]							
Initial value:	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

The bit rate is determined by combinations of SPBR settings and the values in the bit rate division setting bits (BRDV[1:0]) in SPCMD0 to SPCMD3.

In single-SPI slave mode, the bit rate depends on the input clock bit rate regardless of the setting of SPBR[1:0] and BRDV[1:0] bits.

When SPBR is set to 0, the base bit rate is selected.

The equation for calculating the bit rate when SPBR is not 0 is given below. In the equation, n denotes an SPBR setting (1, …, 255), and N denotes bit settings in the bits BRDV[1:0] (0, 1, 2, 3).

$$\text{Bit rate} = \frac{f(\text{QSPI}\phi)}{2 \times n \times 2^N}$$

Table 39.3 shows examples of the relationship between SPBR and BRDV[1:0] bits settings.

Table 39.3 Relationship between SPBR and BRDV[1:0] Settings

			Bit Rate	
SPBR[7:0] (n)	**BRDV[1:0] (N)**	**Division Ratio**	**QSPIϕ = 78 MHz**	**QSPIϕ = 97.5 MHz**
0	0	1	78.0 Mbps	97.50 Mbps
1	0	2	39.0 Mbps	48.75 Mbps
2	0	4	19.5 Mbps	24.38 Mbps
3	0	6	13.0 Mbps	16.25 Mbps
4	0	8	9.75 Mbps	12.19 Mbps
5	0	10	7.80 Mbps	9.75 Mbps
6	0	12	6.50 Mbps	8.13 Mbps
6	1	24	3.25 Mbps	4.06 Mbps
6	2	48	1.625 Mbps	2.03 Mbps
6	3	96	812.5 kbps	1.02 Mbps
255	3	4080	19.12 kbps	23.90 kbps

39.4.9 Data Control Register (SPDCR)

SPDCR enables or disables dummy data transmission when this module operates in master mode.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	SPSC[1:0]		—	—	—	—	—	—	SPSS[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPBR[7:0]								TXDMY	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	TXDMY	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
7	TXDMY	0	R/W	Dummy Data Transmission Enable Enables or disables dummy data transmission from the MOSI pin when the transmit buffer is empty in single-SPI master mode. The last output value in the previous transmit data is used as dummy data. Specifically, if this bit is set to 1 when the transmit buffer is empty, 0 is output from the MOSI pin as dummy data. This bit setting can be changed while the transmit end flag (TEND) in SPSR is 1. Otherwise, operation cannot be guaranteed. 0: Disables dummy data transmission. 1: Enables dummy data transmission.
6 to 0	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.

39.4.10 Clock Delay Register (SPCKD)

SPCKD sets a period (clock delay) from the beginning of SSL signal assertion to SPCLK oscillation when the clock delay setting enable bit (SCKDEN) in SPCMD0 to SPCMD3 is 1 in master mode. If the contents of SPCKD are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

Be sure to set this register to H'00 when using this module in single-SPI slave mode.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	SCKDL[2:0]			—	—	—	—	—	SLNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPNDL[2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	SCKDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2 to 0	SCKDL[2:0]	000	R/W	Clock Delay Setting These bits set a period (clock delay) from the beginning of SSL signal assertion to SPCLK oscillation when the SCKDEN bit in SPCMD0 to SPCMD3 is 1. 000: 1 SPCLK cycle 001: 2 SPCLK cycles 010: 3 SPCLK cycles 011: 4 SPCLK cycles 100: 5 SPCLK cycles 101: 6 SPCLK cycles 110: 7 SPCLK cycles 111: 8 SPCLK cycles

39.4.11 Slave Select Negation Delay Register (SSLND)

SSLND sets a period (SSL negation delay) from the transmission of a final SPCLK edge to the negation of the SSL signal during a serial transfer when the SSL negation delay setting enable bit (SLNDEN) in SPCMD0 to SPCMD3 is 1 in master mode. If the contents of SSLND are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

Be sure to set this register to H'00 when using this module in single-SPI slave mode.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	SCKDL[2:0]			—	—	—	—	—	SLNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPNDL[2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	SLNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2 to 0	SLNDL[2:0]	000	R/W	SSL Negation Delay Setting These bits set a period (SSL negation delay) from the transmission of a final SPCLK edge to the negation of the SSL signal during a serial transfer when the SLNDEN bit in SPCMD0 to SPCMD3 is 1. 000: 0.5 SPCLK cycles 001: 1.5 SPCLK cycles 010: 2.5 SPCLK cycles 011: 3.5 SPCLK cycles 100: 4.5 SPCLK cycles 101: 5.5 SPCLK cycles 110: 6.5 SPCLK cycles 111: 7.5 SPCLK cycles

39.4.12 Next-Access Delay Register (SPND)

SPND sets a period (next-access delay) from termination of a serial transfer to the beginning of the next serial transfer when the next-access delay enable bit (SPNDEN) in SPCMD0 to SPCMD3 is 1 in master mode. If the contents of SPND are modified while the SPE and MSTR bits in SPCR are 1, the subsequent operation cannot be guaranteed.

Be sure to set this register to H'00 when using this module in single-SPI slave mode.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	SCKDL[2:0]			—	—	—	—	—	SLNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPNDL[2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	SPNDL[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
2 to 0	SPNDL[2:0]	000	R/W	Next-Access Delay Setting These bits set a period (next-access delay) from termination of a serial transfer to the beginning of the next serial transfer when the SPNDEN bit in SPCMD0 to SPCMD3 is 1. 000: 1 SPCLK cycle 001: 2 SPCLK cycles 010: 3 SPCLK cycles 011: 4 SPCLK cycles 100: 5 SPCLK cycles 101: 6 SPCLK cycles 110: 7 SPCLK cycles 111: 8 SPCLK cycles

39.4.13 Command Register n (SPCMDn) (n = 0 to 3)

This module has four command registers (SPCMD0 to SPCMD3). SPCMD0 to SPCMD3 are used to set a transfer format in master mode. In master mode, this module sequentially references SPCMD0 to SPCMD3 according to the settings in the sequence control register (SPSCR), and executes the serial transfer that is set in the referenced SPCMD.

If the contents of currently referred-to SPCMD are modified while the TEND bit in SPSR indicates that communication has not been completed, the subsequent operation cannot be guaranteed. The currently referred-to SPCMD can be checked by reading the sequence status register (SPSSR). In addition, if the contents of SPCMD0 are modified during operation in single-SPI slave mode, the subsequent operation cannot be guaranteed.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SPIMOD[1:0]		SPRW	BRDV[1:0]		CPOL	CPHA
Initial value:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SPIMOD[1:0]		SPRW	BRDV[1:0]		CPOL	CPHA
Initial value:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

- Word access:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SCKDEN	SLNDEN	SPNDEN	LSBF	SPB[3:0]				SSLKP	SPIMOD[1:0]		SPRW	BRDV[1:0]		CPOL	CPHA
Initial value:	1	1	1	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	SCKDEN	1	R/W	Clock Delay Setting Enable Sets a period (clock delay) from the beginning of SSL signal assertion to SPCLK oscillation in master mode. If this bit is 0, this module sets the clock delay to 0 SPCLK cycle. If this bit is 1, this module starts SPCLK oscillation in compliance with the clock delay register (SPCKD) settings. For the continuous access in which SSL is kept asserted over the multiple commands, this bit can be set to 0 only when the pertinent command is the second or subsequent one. Otherwise, this bit should be set to 1. 0: A clock delay of 0 SPCLK cycle 1: A clock delay equal to SPCKD settings.

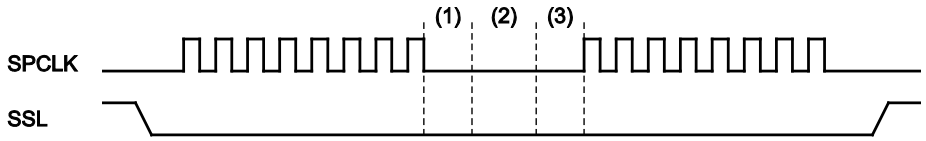
Bit	Bit Name	Initial Value	R/W	Description
14	SLNDEN	1	R/W	SSL Negation Delay Setting Enable Sets a period (SSL negation delay) from SPCLK oscillation stoppage to SSL signal negation in master mode. If this bit is 0, this module sets the SSL negation delay to 0 SPCLK cycle. If this bit is 1, this module negates the SSL signal in compliance with the slave select negation delay register (SSLND) settings. For the continuous access in which SSL is kept asserted over the multiplier commands, this bit can be set to 0 only when the pertinent command is not the last one. Otherwise, this bit should be set to 1. When using this module in single-SPI slave mode, set this bit to 1 and the slave select negation delay register (SSLND) to H'0. 0: An SSL negation delay of 0 SPCLK cycle 1: An SSL negation delay equal to SSLND settings.
13	SPNDEN	1	R/W	Next-Access Delay Enable Sets the period (next-access delay) from termination of a serial transfer to the beginning of the next serial transfer in master mode. If this bit is 0, this module sets the next-access delay to 0 SPCLK cycle. If this bit is 1, this module starts next serial transfer in compliance with the next-access delay register (SPND) settings. For the continuous access in which SSL is kept asserted over the multiple commands, this bit can be set to 0 only when the pertinent command is not the last one. Otherwise, this bit should be set to 1. When using this module in single-SPI slave mode, set this bit to 1 and the next-access delay register (SPND) to B'000. 0: A next-access delay of 0 SPCLK cycle. 1: A next-access delay equal to SPND settings.
12	LSBF	0	R/W	LSB First Sets the data format to MSB first or LSB first in master mode or single-SPI slave mode. 0: MSB first 1: LSB first
11 to 8	SPB[3:0]	0000	R/W	Transfer Data Length Setting These bits set the basic transfer data length for serial transfer. For LSB-first transfer, the transfer data is reversed within the data width specified with these bits. The actual amount of data to be transferred is determined by multiplying the value set with these bits by the value set with SPBMUL0 to SPBMUL3. 0000: 8 bits (1 byte) 0001: 16 bits (2 bytes) 0010: 32 bits (4 bytes) 0011 to 1111: Setting prohibited
7	SSLKP	0	R/W	SSL Signal Level Keeping Specifies whether or not the SSL signal level for the current command is to be kept from the end of the transfer for the current command to the beginning of the transfer for the next command in master mode. Setting this bit to 1 enables a transition to the next access while the SSL signal is kept asserted. 0: Negates all SSL signals upon completion of transfer. 1: Keeps the SSL signal level from the end of the transfer to the beginning of the next access.

Bit	Bit Name	Initial Value	R/W	Description
6, 5	SPIMOD[1:0]	00	R/W	SPI Operating Mode These bits select the operating mode of this module from single-, dual-, or quad-SPI. 00: Single-SPI 01: Dual-SPI 10: Quad-SPI 11: Setting prohibited
4	SPRW	0	R/W	SPI Read/Write Access Sets an access direction in dual-/quad-SPI modes. This bit is invalid in single-SPI mode 0: Write operation (IO1 and IO0/IO3 to IO0: Output) 1: Read operation (IO1 and IO0/IO3 to IO0: Input)
3, 2	BRDV[1:0]	00	R/W	Bit Rate Frequency Division Setting These bits are used to determine the bit rate in master mode. The settings of these bits and of the bit rate register (SPBR) together determine the bit rate. The base bit rate depends on the setting of the SPBR. The setting of this field selects division of the base bit rate by one, two, four, or eight. Individual BRDV[1:0] values can be set in each of command registers 0 to 3. Therefore, serial transfers can be at different bit rates for each of the commands. 00: Base bit rate 01: Two division of the base 10: Four division of the base 11: Eight division of the base
1	CPOL	0	R/W	SPCLK Polarity Setting Sets an SPCLK polarity. When data communication is performed between this quad serial peripheral interface module and another module, the same SPCLK polarity should be set for both modules. 0: Positive (SPCLK = 0 when idle) 1: Negative (SPCLK = 1 when idle)
0	CPHA	1	R/W	SPCLK Phase Setting Sets an SPCLK edge for latching and shifting data to be transferred. When data communication is performed between this quad serial peripheral interface module and another module, the same SPCLK edge should be set for both modules. 0: Data latch on odd edge, data shift on even edge 1: Data shift on odd edge, data latch on even edge Note: The first SPCLK edge is treated as the first edge.

Reference: Some serial flash memory datasheets refer to SPCLK specifications, which are determined by what this document refers to as CPOL and CPHA bits, as SPI modes 0 to 3. Assuming that SPI modes 0 to 3 are controlled by SPI mode bits [1:0], CPOL and CPHA in this document correspond to SPI mode bits 1 and 0, respectively.
In this module, the initial values of CPOL and CPHA are 0 and 1, respectively, selecting SPI mode 1 as the initial mode.

Notes: 1. When setting any or all of the clock delay period, SSL negation delay period, and next-access delay period to 0, be sure to set SSLKP to 1 to select the continuous access in which SSL is not negated. Otherwise, operation cannot be guaranteed. For the method of setting the various delay periods for the continuous access in which SSL is not negated, see below.

2. For the continuous access in which SSL is not negated, SPCLK clock stopping is followed by the SSL negation delay period, next-access delay period, and next command clock delay period, in this order. When setting any of the setting enable bit (SPCKDEN), SSL negation delay setting enable bit (SLNDEN), and next-access delay enable bit (SPNDEN) to 0, be sure to set the bit corresponding to the later period prior to the bit corresponding to the earlier period.



In the above figure, (1), (2), and (3) refer to the SSL negation delay period, next-access delay period, and next command clock delay period, respectively. When setting any of these bits to 0, be sure to set (3) first. In other words, setting 1 after 0 as in {(1), (2), (3)} = {0, 0, 1}, {0, 1, 1}, {0, 1, 0} … is prohibited. Allowed setting is {(1), (2), (3)} = {1, 1, 1}, {1, 1, 0}, {1, 0, 0}, {0, 0, 0}. If set otherwise, operation cannot be guaranteed.

3. When changing BRDV[1:0] or CPOL for each command for the continuous access in which the SSL level is held, be sure to insert the SSL negation delay period, next-access delay period, and clock delay period between commands. Otherwise, operation cannot be guaranteed.
4. When changing SPIMOD[1:0] or CPHA for each command for the continuous access in which the SSL level is held, be sure to insert one cycle or more between commands. Otherwise, operation cannot be guaranteed.

39.4.14 Buffer Control Register (SPBFCR)

SPBFCR resets the number of data units in the transmit buffer (SPTXB) or receive buffer (SPRXB) and sets the number of triggering data units.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXRST	RXRST	TXTRG[1:0]		—	RXTRG[2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TXBC[5:0]						—	—	RXBC[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Byte access:

Bit:	7	6	5	4	3	2	1	0
	TXRST	RXRST	TXTRG[1:0]		—	RXTRG[2:0]		
Initial value:	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TXRST	0	R/W	Transmit Buffer Data Reset Invalidates transmit data in the transmit buffer and resets the transmit buffer to an empty state. 0: Allows the transmit buffer normal operation. 1: Resets the transmit buffer.
6	RXRST	0	R/W	Receive Buffer Data Reset Invalidates receive data in the receive buffer and resets the receive buffer to an empty state. 0: Allows the receive buffer normal operation. 1: Resets the receive buffer.
5, 4	TXTRG[1:0]	00	R/W	Transmit Buffer Data Triggering Number Specifies the timing at which the transmit buffer empty state is determined, that is when the SPTEF flag in the status register is set. When the number of bytes of data in the transmit buffer (SPTXB) is equal to or less than the specified triggering number, the SPTEF flag is set to 1. 00: 31 bytes (1 byte available) 01: 30 bytes (2 bytes available) 10: 28 bytes (4 bytes available) 11: 0 byte (32 bytes available)
3	—	0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	RXTRG[2:0]	000	R/W	Receive Buffer Data Triggering Number Specify the timing at which the receive buffer full state is determined, that is when the SPRFF flag in the status register is set. When the number of bytes of data in the receive buffer (SPRXB) is equal to or greater than the specified triggering number, the SPRFF flag is set to 1. 000: 1 byte (31 bytes available) 001: 2 bytes (30 bytes available) 010: 4 bytes (28 bytes available) 011: 5 bytes (27 bytes available) 100: 8 bytes (24 bytes available) 101: 16 bytes (16 bytes available) 110: 24 bytes (8 bytes available) 111: 32 bytes (0 byte available)

39.4.15 Buffer Data Count Register (SPBDCR)

SPBDCR indicates the number of data units stored in the transmit buffer (SPTXB) and receive buffer (SPRXB). The upper eight bits indicate the number of transmit data units in the transmit buffer and the lower eight bits indicate the number of receive data units in the receive buffer.

- Longword access:

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TXRST	RXRST	TXTRG[1:0]		—	RXTRG[2:0]			—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TXBC[5:0]						—	—	RXBC[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

- Word access:

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TXBC[5:0]						—	—	RXBC[5:0]					
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15, 14	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
13 to 8	TXBC[5:0]	000000	R	Transmit Data Byte Counter Indicate the number of transmit data bytes in the transmit data buffer (SPTXB). B'000000 indicates that SPTXB is empty. B'100000 indicates that SPTXB is full.
7, 6	—	All 0	R	Reserved The write value should always be 0. Otherwise, operation cannot be guaranteed.
5 to 0	RXBC[5:0]	000000	R	Receive Data Byte Counter Indicates the number of receive data bytes in the receive data buffer (SPRXB). B'000000 indicates that SPRXB is empty. B'100000 indicates that SPRXB is full.

39.4.16 Transfer Data Length Multiplier Setting Register n (SPBMULn) (n = 0, 1, 2, 3)

SPBMUL0 to SPBMUL3 set the number of times to transfer the specific length of data defined by the transfer data length setting bits (SPB[3:0]) in SPCMD0 to SPCMD3. SPBMUL0 to SPBMUL3 correspond to SPCMD0 to SPCMD3, respectively. This register setting is valid only in master mode. In single-SPI slave mode, this register should be set to the initial value; other values are prohibited.

If a command register is referred to while the TEND bit in SPSR indicates that communication has not been completed and SPBMUL corresponding to the referred-to command register is modified, the subsequent operation is not guaranteed. The currently referred-to command register can be checked by reading the sequence status register (SPSSR).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SPBMUL[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	SPBMUL[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SPBMUL [31:0]	H'0000 0001	R/W	Transfer Data Length Multiplier Setting These bits set the multiplier for transfer data; that is, the number of times to transfer the specific length of data defined by SPB[3:0] bits in SPCMD0 to SPCMD3. The actual amount of data to be transferred is determined by SPB[3:0] × SPBMUL[31:0]. Setting these bits to H'00000000 allows the defined size of data to be transferred 4,294,967,296 times.

39.5 Operation

In this section, the serial transfer period means a period from the beginning of driving valid data to the fetching of the final valid data, and the SSL negation period means the idle period.

39.5.1 Overview of Operations

This module is capable of serial transfers in single-/dual-/quad-SPI master modes and single-SPI slave mode. Table 39.4 gives the features of single-/dual-/quad-SPI modes.

Table 39.4 Features of Each SPI Mode

	Single-SPI	Dual-SPI	Quad-SPI
Number of data lines	One input line and one output line	Two IO lines	Four IO lines
Data line direction	Single-directional	Bidirectional	Bidirectional
Slave operation	Not supported	Not supported	Not supported
Simultaneous transmission/reception	Supported	Not supported	Not supported

Table 39.5 gives the overview of master-mode operation.

Table 39.5 Overview of Master Mode

Items	Master Mode
MSTR bit setting in the control register	1
SPCLK signal	Output
MOSI signal (single-SPI)	Output
MISO signal (single-SPI)	Input
IO1 and IO0 (dual-SPI)/ IO3 to IO0 (quad-SPI)	Input/output
SSL signal	Output
Switching SSL polarity	Supported
Transfer rate	Up to QSPIϕ
Clock source	On-chip baud rate generator
Clock polarity	Positive/negative
Clock phase	Latch at rising/output at falling Latch at falling/output at rising
Transfer bit order	MSB first/LSB first
Transfer data length	(8/16/32) × (1 to 4,294,967,296) bits
Burst transfer	Supported
SPCLK delay control	Supported
SSL negation delay control	Supported
Next-access delay control	Supported
Transfer start method	Writing data to the transmit buffer when SPE = 1 There is space in the receive buffer when SPE = 1*
Sequence control	Supported
Transmit buffer empty detection	Supported
Receive buffer full detection	Supported
Overrun error detection	Not supported
Underrun error detection	Not supported
Mode fault error detection	Not supported

Note: * During single-SPI operation and dual-/quad-SPI mode write operation, a transfer is started by setting SPE to 1 and writing data to the transmit buffer. During dual-/quad-SPI mode read operation, a transfer is started by setting SPE to 1 when there is space for the specified length of data in the receive buffer.

39.5.2 Pin Control

This module automatically switches the pin states according to the status after write/read transfer in single-SPI master or slave mode or dual-/quad-SPI mode. The status of the data pins (MOSI/MISO/IO[3:0]) in the idle state depends on the MOIFE and MOIFV bit settings, the single-/dual-SPI mode IO3 output fixed value bit (IO3FV) setting, and the single-/dual-SPI mode IO2 output fixed value bit (IO2FV) setting. Table 39.6 shows the pin states in single-SPI master mode. Table 39.7 shows the pin states in dual-/quad-SPI modes.

Table 39.6 Pin States in Single-SPI Master Mode

Items	Single-SPI Master Mode
SSL	Output
SPCLK	Output
MOSI	Output
MISO	Input
MOSI in the idle state	MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value
MISO in the idle state	—
IO2	IO2FV setting value output or not used
IO3	IO3FV setting value output or not used

Table 39.7 Pin States in Dual-/Quad-SPI Modes

Items	Dual-SPI Mode	Quad-SPI Mode
SSL	Output	Output
SPCLK	Output	Output
IO0	I/O	I/O
IO1	I/O	I/O
IO2	IO2FV setting value output or not used	I/O
IO3	IO3FV setting value output or not used	I/O
IO0 in the idle state	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z
IO1 in the idle state	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z
IO2 in the idle state	IO2FV setting value output or not used	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z
IO3 in the idle state	IO3FV setting value output or not used	After writing: MOIFE = 0: Final output value MOIFE = 1: MOIFV setting value After reading: Hi-Z

39.5.3 Transfer Format

The SPI has four clock settings determined by the SPCLK polarity setting (CPOL) and SPCLK phase setting (CPHA) bits in SPCMD0 to SPCMD3. Figure 39.1 shows the data latch/shift timing based on each setting in an 8-bit MSB first transfer. In Figure 39.1, L indicates the latch timing and S indicates the shift timing. DATA corresponds to MISO/MOSI in single-SPI mode; IO1 and IO0 in dual-SPI mode; or IO3 to IO0 in quad-SPI mode. t_{ckd} indicates the clock delay period when the SCKDEN bit in SPCMD0 to SPCMD3 is set to 1. Similarly, t_{slnd} indicates the SSL negation delay period when the SLNDEN bit in SPCMD0 to SPCMD3 is set to 1, and t_{spnd} indicates the next-access delay period when the SPNDEN bit in SPCMD0 to SPCMD3 is set to 1.

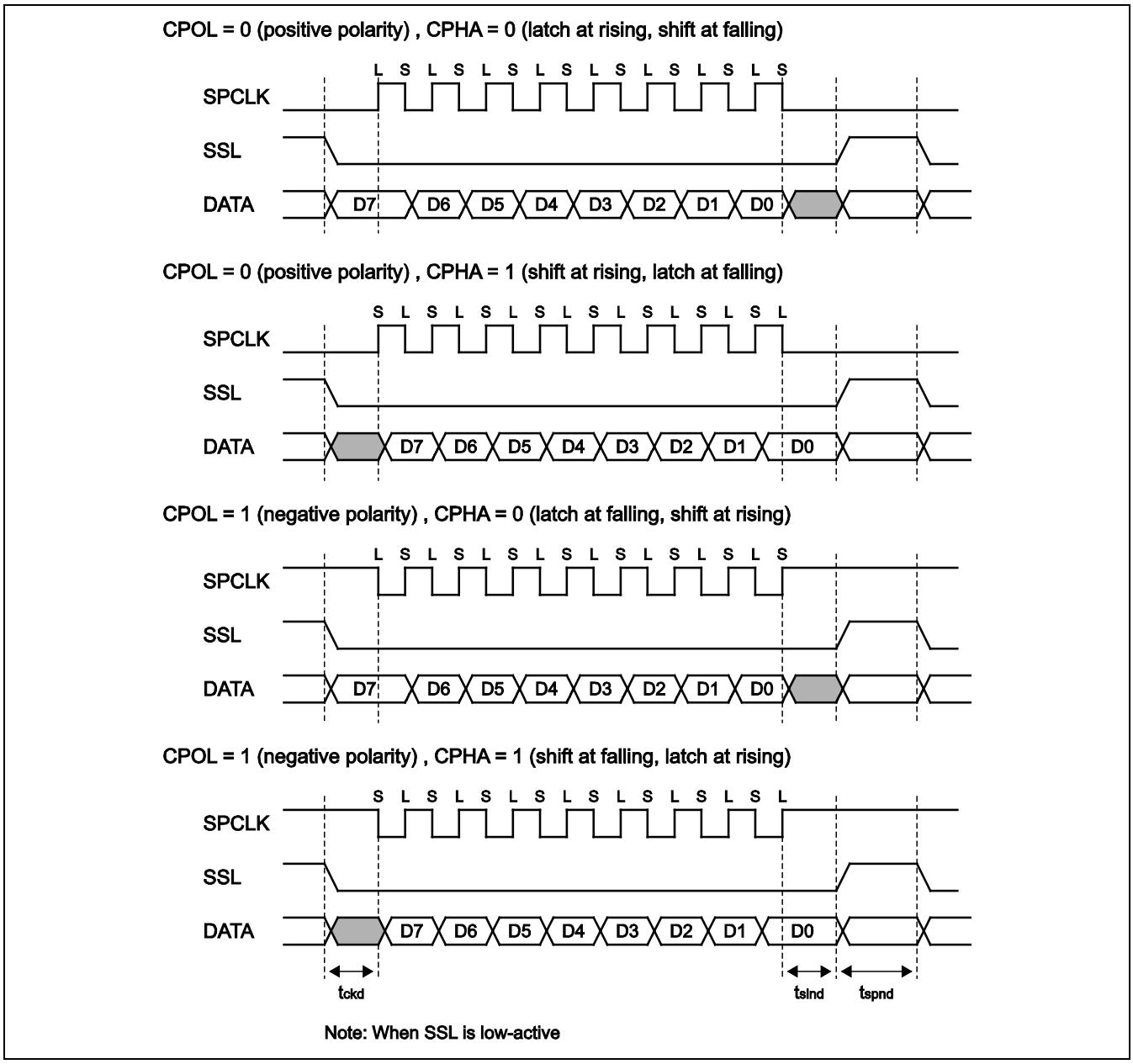


Figure 39.1 SPI Clock Setting and Transfer Timing

Note that when the base bit rate is used, transmission and reception when CPHA = 0 is not available.

The following describes 8-bit MSB first transfer in single-/dual-/quad-SPI modes when CPOL = 0 and CPHA = 0.

(1) Single-SPI mode

Figure 39.2 shows the transfer format in single-SPI mode. This mode provides transmission and reception simultaneously. Since one data line is used for serial communication both in transmission and reception, the communication speed is 1 bit per SPCLK clock cycle. Transfer data is specified using SPCMD0 to SPCMD3. For details of transfer data, see section 39.5.4, Transfer Data.

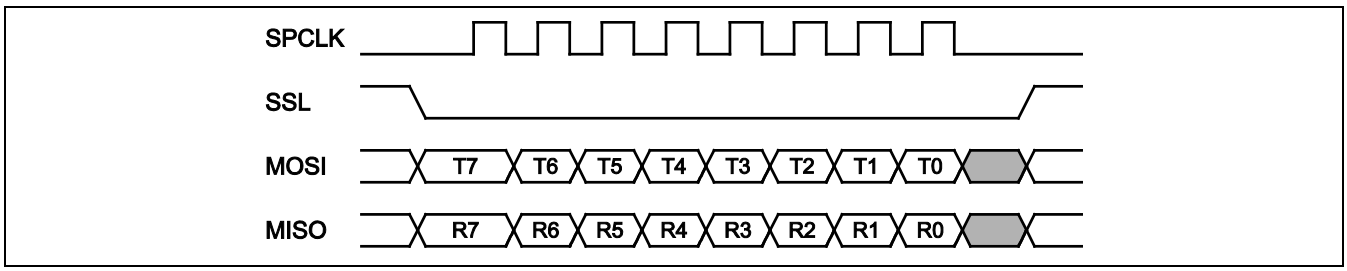


Figure 39.2 Transfer Format in Single-SPI Mode

(2) Dual-SPI mode

Figure 39.3 shows the transfer format in dual-SPI mode. This mode only provides operation of a single direction, that is, either transmission or reception. Transmission or reception can be set using the SPI read/write access setting bit (SPRW) in SPCMD0 to SPCMD3. Transmission is carried out by write operation and reception by read operation. The I/O directions of IO1 and IO0 are switched accordingly. Since two data lines are used for serial communication both in transmission and reception, the communication speed is 2 bits per SPCLK clock cycle. The start bit of the transfer data is output from IO1. Transfer data is specified using SPCMD0 to SPCMD3. For details of transfer data, see section 39.5.4, Transfer Data.

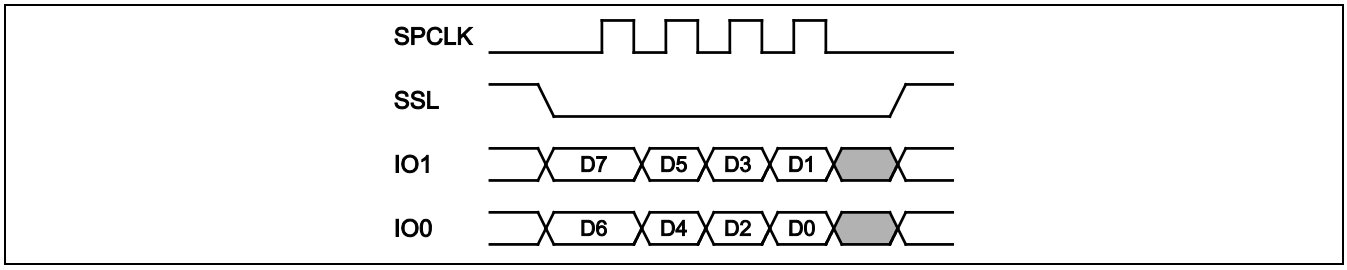


Figure 39.3 Transfer Format in Dual-SPI Mode

(3) Quad-SPI mode

Figure 39.4 shows the transfer format in quad-SPI mode. This mode provides operation of a single direction, that is, either transmission or reception. Transmission or reception can be set using the SPRW bit in SPCMD0 to SPCMD3. Transmission and reception are accomplished by writing and reading, respectively. The I/O directions of IO3 to IO0 are switched accordingly. Since four data lines are used for serial communication both in transmission and reception, the communication speed is 4 bits per SPCLK clock cycle. The start bit of the transfer data is output from IO3. Transfer data is specified using SPCMD0 to SPCMD3. For details of transfer data, see section 39.5.4, Transfer Data.

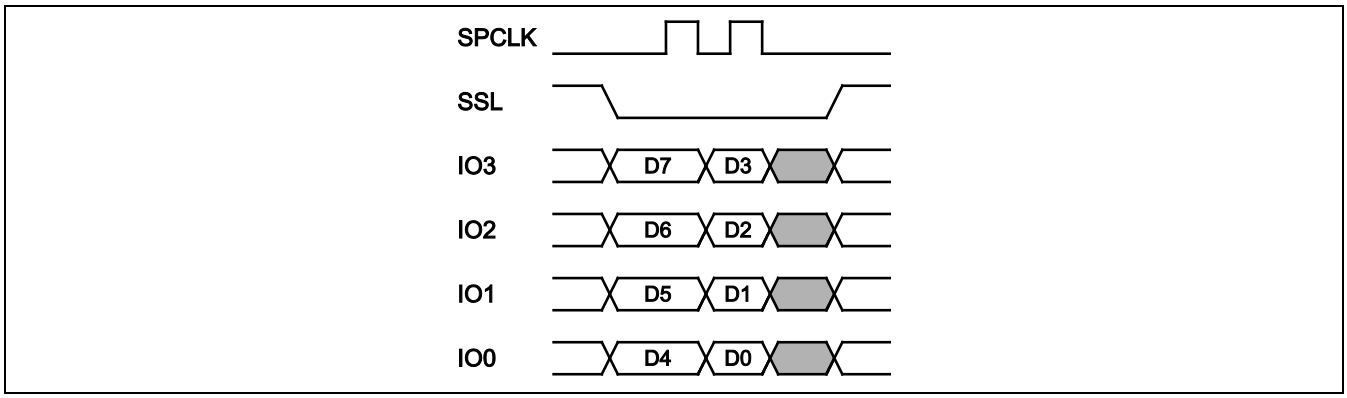


Figure 39.4 Transfer Format in Quad-SPI Mode

39.5.4 Transfer Data

The data format is determined by the SPB[3:0] and the LSB first (LSBF) bits in SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. In both MSB first and LSB first transfers, this module treats the specified size of data beginning at the MSB of the transmit shift register as transmit data, and the specified length of data beginning at the LSB of the receive shift register as receive data, regardless of whether the actual arrangement is MSB- or LSB-first. The following sections describe MSB-first and LSB-first transfers in 32-bit, 16-bit, and 8-bit data units.

(1) MSB-first transfer (32-bit data)

Figure 39.5 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 32-bit MSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 32-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module copies the data with MSB-aligned in the transmit buffer to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 32 bits or more, this module copies the 32-bit data beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 32 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 32 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.

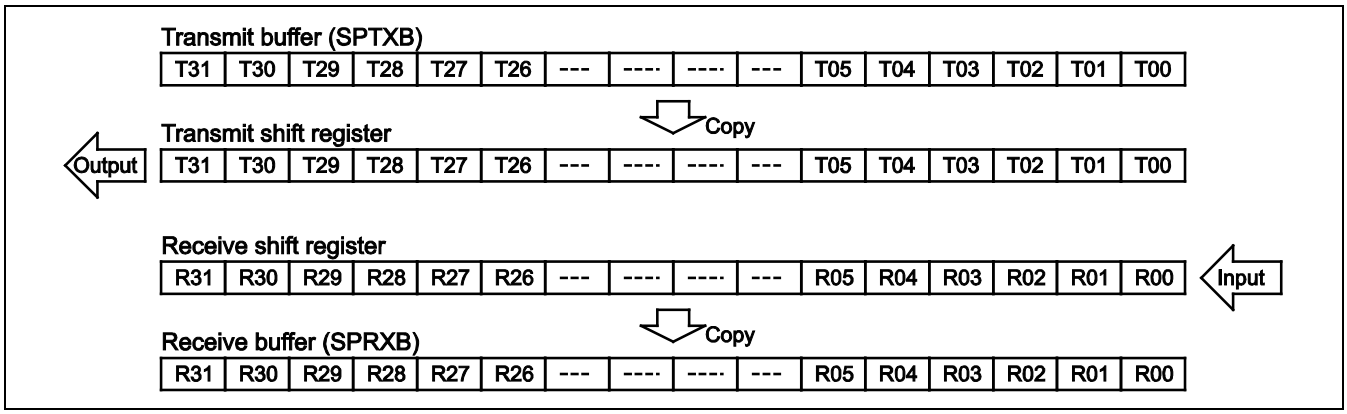


Figure 39.5 MSB-First Transfer (32-Bit Data)

(2) MSB-first transfer (16-bit data)

Figure 39.6 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 16-bit MSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 16-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module copies the data with MSB-aligned in the transmit buffer to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 16 bits or more, this module copies the 16-bit data beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 16 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 16 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.

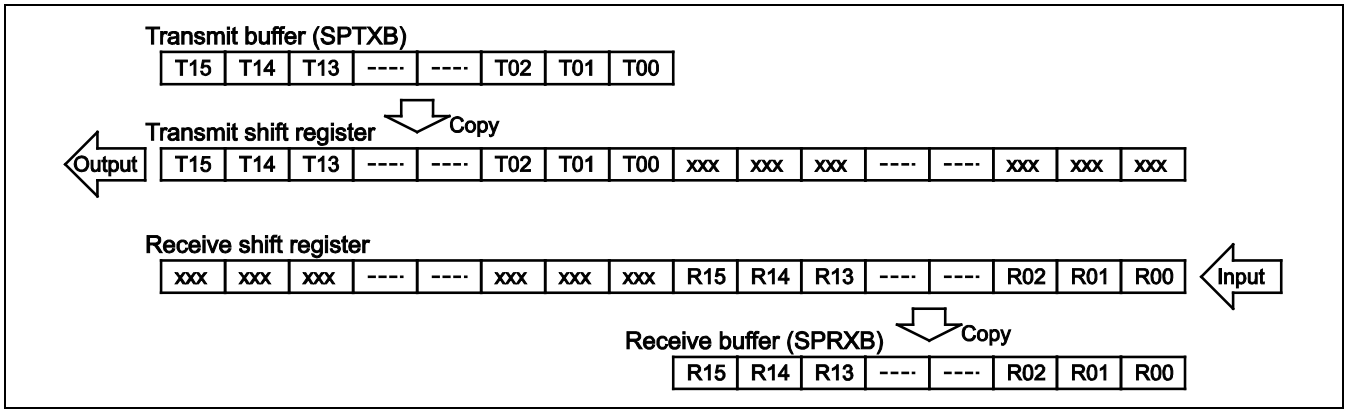


Figure 39.6 MSB-First Transfer (16-Bit Data)

(3) MSB-first transfer (8-bit data)

Figure 39.7 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs an 8-bit MSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 8-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module copies the data with MSB-aligned in the transmit buffer to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 8 bits or more, this module copies the 8-bit data beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 8 bits or more in master mode, data reception is not carried out. In order to start reception, data for the specified length of data should be read from the receive buffer to secure the space for 8 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.

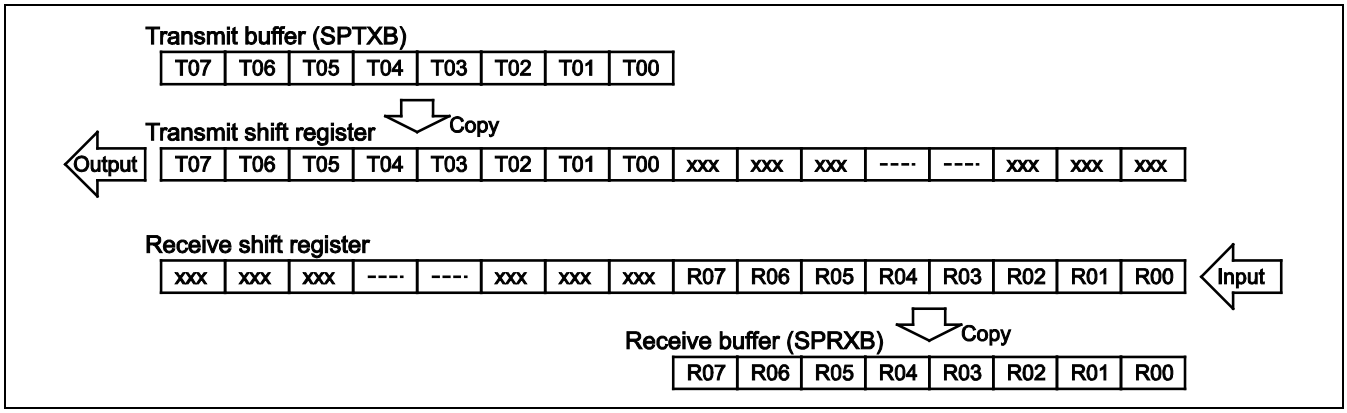


Figure 39.7 MSB-First Transfer (8-Bit Data)

(4) LSB-first transfer (32-bit data)

Figure 39.8 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 32-bit LSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 32-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module reverses the bit order in the 32-bit transmit data, copies it with MSB-aligned to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 32 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 32 bits or more, this module reverses the order of the bits of the 32-bit data, copies it beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 32 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 32 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.

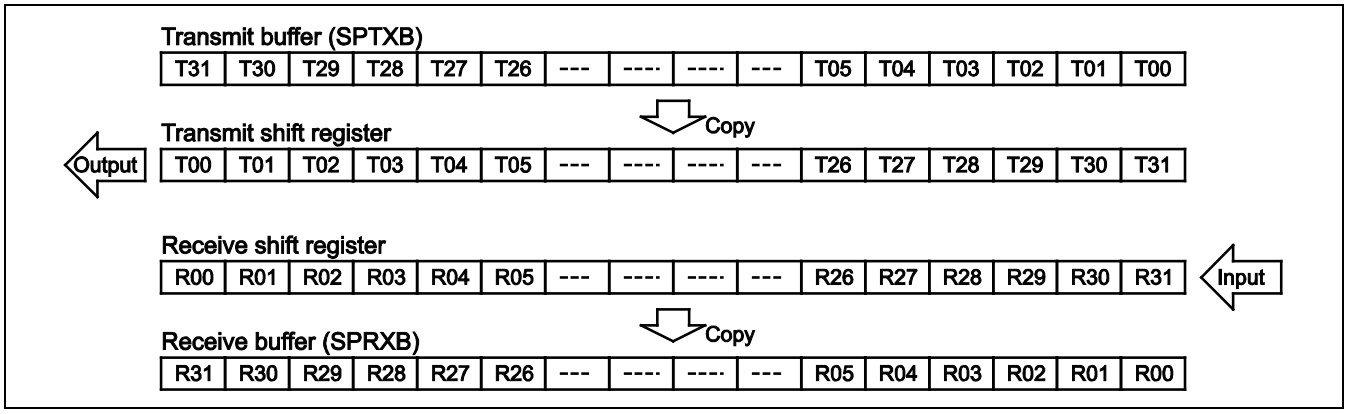


Figure 39.8 LSB-First Transfer (32-Bit Data)

(5) LSB-first transfer (16-bit data)

Figure 39.9 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs a 16-bit LSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 16-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module reverses the bit order in the 16-bit transmit data, copies it with MSB-aligned to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the receive shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 16 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 16 bits or more, this module reverses the bit order in the 16-bit data, copies it beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 16 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 16 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.

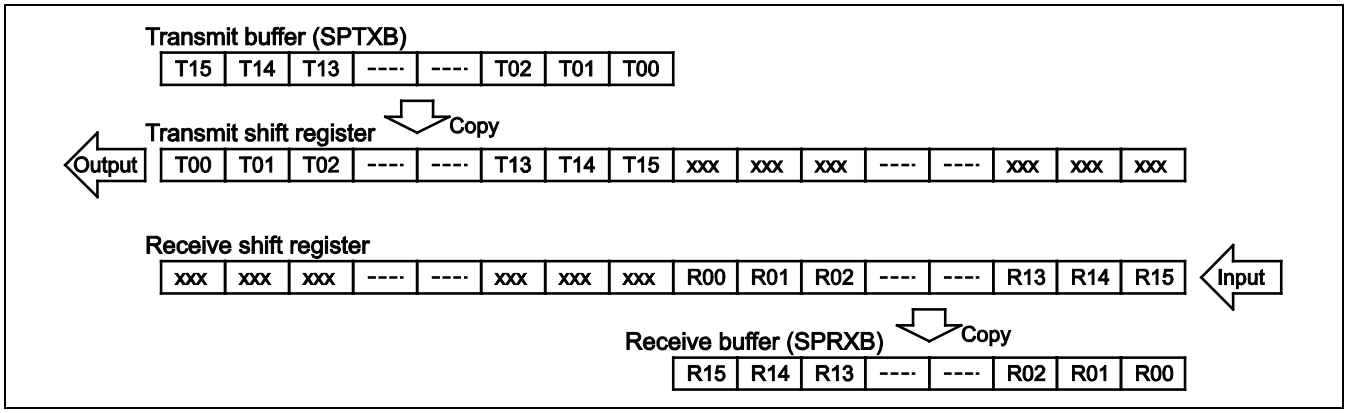


Figure 39.9 LSB-First Transfer (16-Bit Data)

(6) LSB-first transfer (8-bit data)

Figure 39.10 shows the operation of the transmit buffer and transmit shift register, and the receive shift register and receive buffer when this module performs an 8-bit LSB-first data transfer.

For data transmission, the CPU or direct memory access controller (DMAC) writes 8-bit transmit data to the transmit buffer (SPTXB). If the transmit shift register is empty, this module reverses the bit order in the 8-bit transmit data, copies it with MSB-aligned to the transmit shift register, and fills the transmit shift register. When data transmission is started, this module outputs data beginning at the MSB (bit 31) of the transmit shift register, and when the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the transmit shift register becomes empty.

For data reception, data received from the data pin is stored in the received shift register beginning at the LSB (bit 0). When the SPCLK clock cycle required for the serial transfer of 8 bits has passed, the receive shift register becomes full. If the receive buffer (SPRXB) has a space for 8 bits or more, this module reverses the bit order in the 8-bit data, copies it beginning at the LSB from the receive shift register to the receive buffer, and empties the receive shift register. If the receive buffer does not have a space for 8 bits or more in master mode, data reception is not carried out. In order to start reception, the specified length of data should be read from the receive buffer to secure the space for 8 bits or more in the receive buffer.

In actual transfer, this operation is repeated for the number of times defined by SPBMUL0 to SPBMUL3.

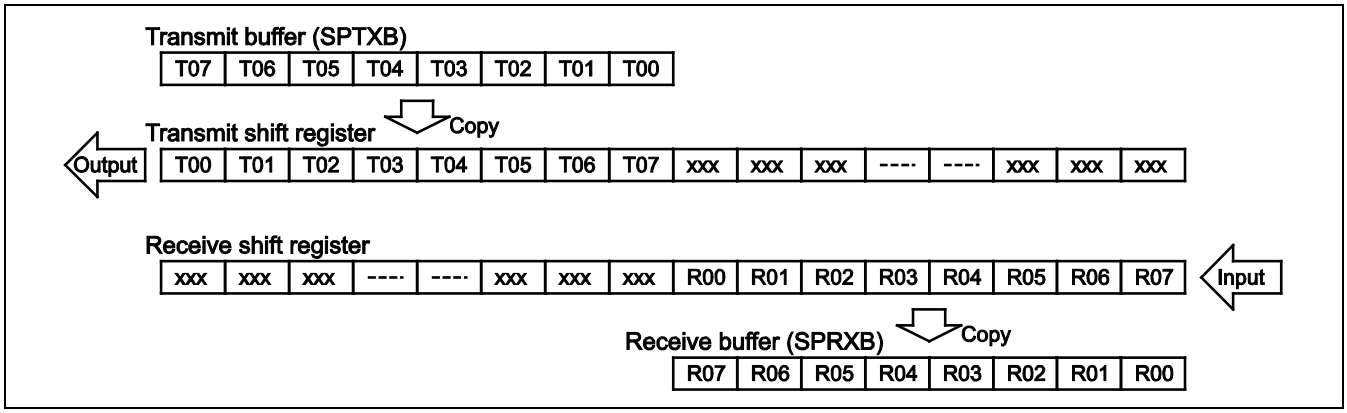


Figure 39.10 LSB-First Transfer (8-Bit Data)

39.5.5 Error Detection

In the normal serial transfer, the data written from SPDR to the transmit buffer is serially transmitted, and the serially received data can be read from the receive buffer of SPDR. If access is made to SPDR or serial transfer is started or completed, depending on the status of the transmit buffer/receive buffer, non-normal transfers may be executed in some cases.

This module detects certain types of non-normal transfers as underrun, overrun, or mode fault errors. Table 39.8 shows the relationship between non-normal transfer operations and the error detection function.

Table 39.8 Relationship between Non-Normal Transfer Operations and Error Detection Function

	Occurrence Condition	Operation	Error Detection
A	SPDR is written when the transmit buffer is full.	Missing write data.	Not detected
C	SPDR is read when the receive buffer is empty.	The output data is undefined.	Not detected

On operation A shown in Table 39.8, this module detects no error. Whether SPDR can be written to or not can be checked using the transmit data byte counter bits (TXBC[5:0]) in the buffer data count register (SPBDCR).

Similarly, on operation C shown in Table 39.8, this module detects no error. Whether the valid data is stored in the receive buffer or not can be checked by reading the receive data byte counter bits (RXBC[5:0]) in SPBDCR.

39.5.6 Initialization

If 0 is written to the SPE bit in SPCR, or a mode fault error is detected and the SPE bit is cleared to 0, this module disables the module function, and initializes a part of the module function. When a power-on reset is generated, this module initializes all of the module function.

When the SPE bit in SPCR is cleared to 0, this module performs the following initialization:

- Suspending any serial transfer that is being executed
- Initializing the transmit shift register and the receive shift register
- Initializing the internal state machine
- Initializing the sequence
- Initializing the TEND bit in SPSR

Initialization by clearing the SPE bit to 0 does not initialize the control bits of this module and the transmit/receive buffer. For this reason, this module can be started in the same transfer mode as prior to the initialization if the SPE bit is re-set to 1. However, clearing the SPE bit to 0 initializes the transmit shift register and the receive shift register and allows the data that is being transferred to be discarded.

39.5.7 SPI Operation

The operating modes of this module are listed below.

- Single-SPI master mode
- Dual-SPI mode/quad-SPI mode

The operation in each mode is described below.

(1) Single-SPI master mode

(a) Starting serial transfer

The serial transfer start conditions are: there is the specified length of data in the transmit buffer; and there is space for the specified length of data in the receive buffer.

(b) Terminating serial transfer

Irrespective of the clock setting, this module terminates the serial transfer after transmitting an SPCLK edge corresponding to the final sampling timing. After the serial transfer is completed, receive data is copied from the receive shift register to the receive buffer. If there is not enough space for the specified length of data in the receive buffer after receive data is copied from the receive shift register to the receive buffer, another serial transfer will not be performed.

(c) Sequence control

In single-SPI master mode, according to the sequence length that is assigned to the sequence control register (SPSCR), this module makes up a sequence comprised of a part or all of SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. This module contains a pointer to the SPCMD that makes up the sequence. The value of this pointer can be checked by reading SPSSR.

When the SPE bit in SPCR is set to 1 and the function of this module is enabled, this module loads the pointer to the commands in SPCMD0, and incorporates the SPCMD0 and SPBMUL0 settings into the transfer format at the beginning of serial transfer. This module increments the pointer each time the next-access delay period for a data transfer that corresponds to the referenced SPCMD0 to SPCMD3 ends. Upon completion of the serial transfer that corresponds to the final command comprising the sequence, this module sets the pointer in SPCMD0, and in this manner the sequence is executed repeatedly.

The following items are set in command registers SPCMD0 to SPCMD3: basic transfer data length, MSB or LSB first, clock settings, some of the bit rate settings, SPI transfer mode and transfer direction (only in dual-/quad-SPI modes), whether SSL level is held, a clock delay period, an SSL negation delay period, and a next-access delay period. The total amount of data to be transferred is determined by multiplying the basic length of data to be transferred by the value set with SPBMUL0 to SPBMUL3.

Figure 39.11 shows an operation example when SPSCR is set to H'02, and the sequence is configured based on SPCMD0 to SPCMD2 settings. In Figure 39.11, shaded areas of MOSI/MISO indicate invalid data. Periods (1) to (3) in Figure 39.11 indicate the followings.

(1) Clock delay period (SPCKD) setting value = B'000 (one SPCLK cycle)

(2) SSL negation delay period (SSLND) setting value = B'000 (one SPCLK cycle)

(3) Next-access delay period (SPND) setting value = B'000 (one SPCLK cycle)

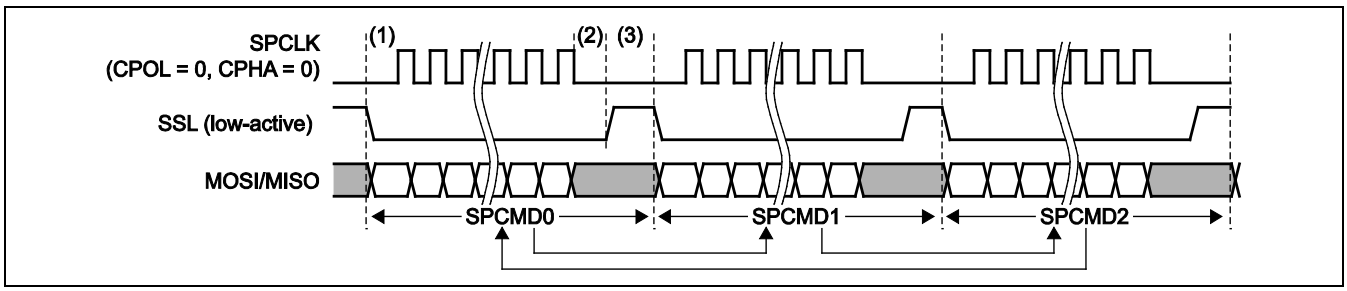


Figure 39.11 Sequence Control Operation

(d) Burst transfer

This module can execute burst transfer with the following two methods in single-SPI master mode.

One method uses the SPB[3:0] bits in SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. Setting SPB[3:0] to select 8, 16, or 32 bits and setting SPBMUL0 to SPBMUL3 to select one through 4,294,967,296 allows the specified length of data to be continuously transferred for the specified times, where the length is specified by SPB[3:0] and the number of times is specified by SPBMUL0 to SPBMUL3. However, if the transmit buffer (SPTXB) becomes empty during transfer, or the receive buffer (SPRXB) has no longer a space enough to receive the specified length of data defined by SPB[3:0], the clock is stopped until transfer is resumed. Figure 39.12 shows a burst transfer example in which SPB[3:0] are set to select 32 bits and SPBMUL to select four times thus specifying 128 bits as a total transfer data amount. The following describes operations (1) to (4) in the figure.

(1) First 32-bit data transfer

(2) Second 32-bit data transfer

(3) When the transmit buffer becomes empty or the receive buffer has no longer a space for 32 or more bits, the clock is stopped. Here, the MOSI continues outputting the previous value. When data is written to the transmit buffer or an enough space is created in the receive buffer, the clock output is resumed to restart transfer.

(4) Third and fourth 32-bit data transfer

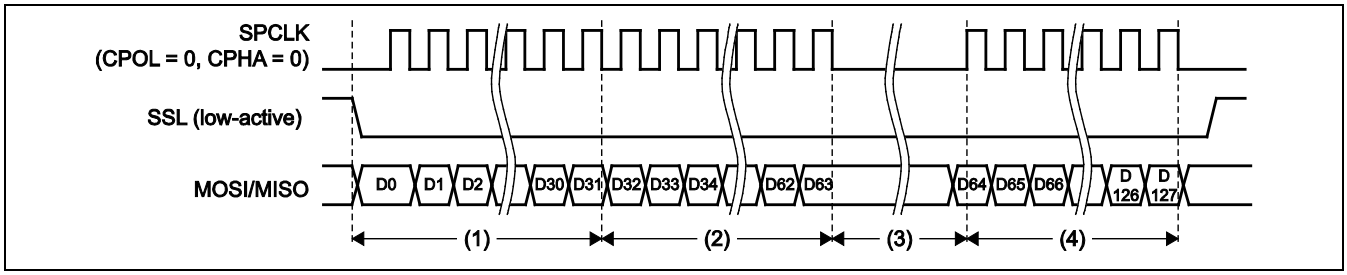


Figure 39.12 Burst Transfer Example in which Total Transfer Data Amount is 128 Bits (Single-SPI Master Mode Used)

In the other method, SSL is kept asserted after a serial transfer is completed until the next serial transfer. Setting the SSL signal level keeping bit (SSLKP) to 1 in SPCMD0 to SPCMD3 allows the SSL signal to be kept asserted after the transfer corresponding to the pertinent command register is completed until the next transfer. Figure 39.13 shows a burst transfer example in which the SSL signal level keeping function is used. The following describes operations (1) to (6) in the figure.

(1) Clock delay period according to the SPCMD0 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the first transfer in the burst transfer.

(2) SSL negation delay period according to the SPCMD0 setting. Since SSLKP is set to 1, SSL is not negated even after SSL negation delay period is over. The SSL negation delay period depends on the SLNDEN bit setting in SPCMD0. When SLNDEN is 1, the SSL negation delay period is determined by the SSLND setting, and the delay period is 0 SPCLK cycle when SLNDEN is 0.

(3) Next-access delay period according to the SPCMD0 setting. Since SSLKP is set to 1, SSL is not negated even during the next-access delay period. The next-access delay period depends on the SPNDEN bit setting in SPCMD0. When SPNDEN is 1, the next-access delay period is determined by the SPND setting, and the delay period is 0 SPCLK cycle when SPNDEN is 0.

(4) Clock delay period according to the SPCMD1 setting. The clock delay period depends on the SCKDEN bit setting in SPCMD1. When SCKDEN is 1, the clock delay period is determined by the SPCKD setting, and the delay period is 0 SPCLK cycle when SCKDEN is 0.

(5) SSL negation delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Since SSLKP in SPCMD1 is set to 0, SSL is negated after SSL negation delay period is over.

(6) Next-access delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Be sure to set SSLKP to 0 to negate SSL.

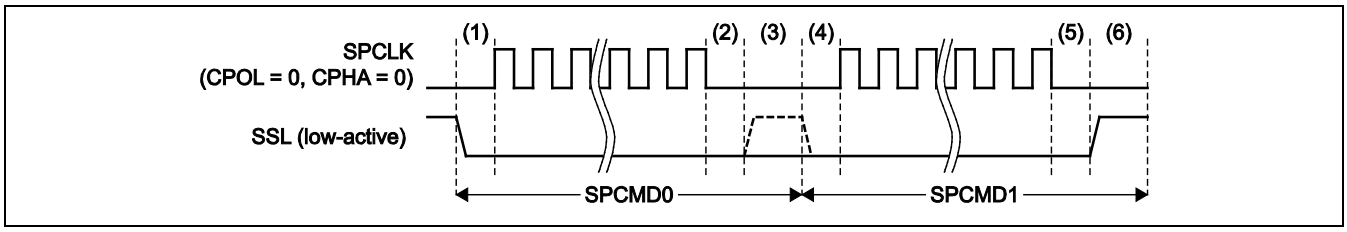


Figure 39.13 Burst Transfer Example in which SSL Signal Level Keeping Function is Used (Single-SPI Mode)

(e) Initialization flowchart

Figure 39.14 is a flowchart illustrating an example of initialization in SPI operation when this module is used in single-SPI master mode. For a description of how to set up the interrupt controller and direct memory access controller, see the descriptions given in the individual blocks.

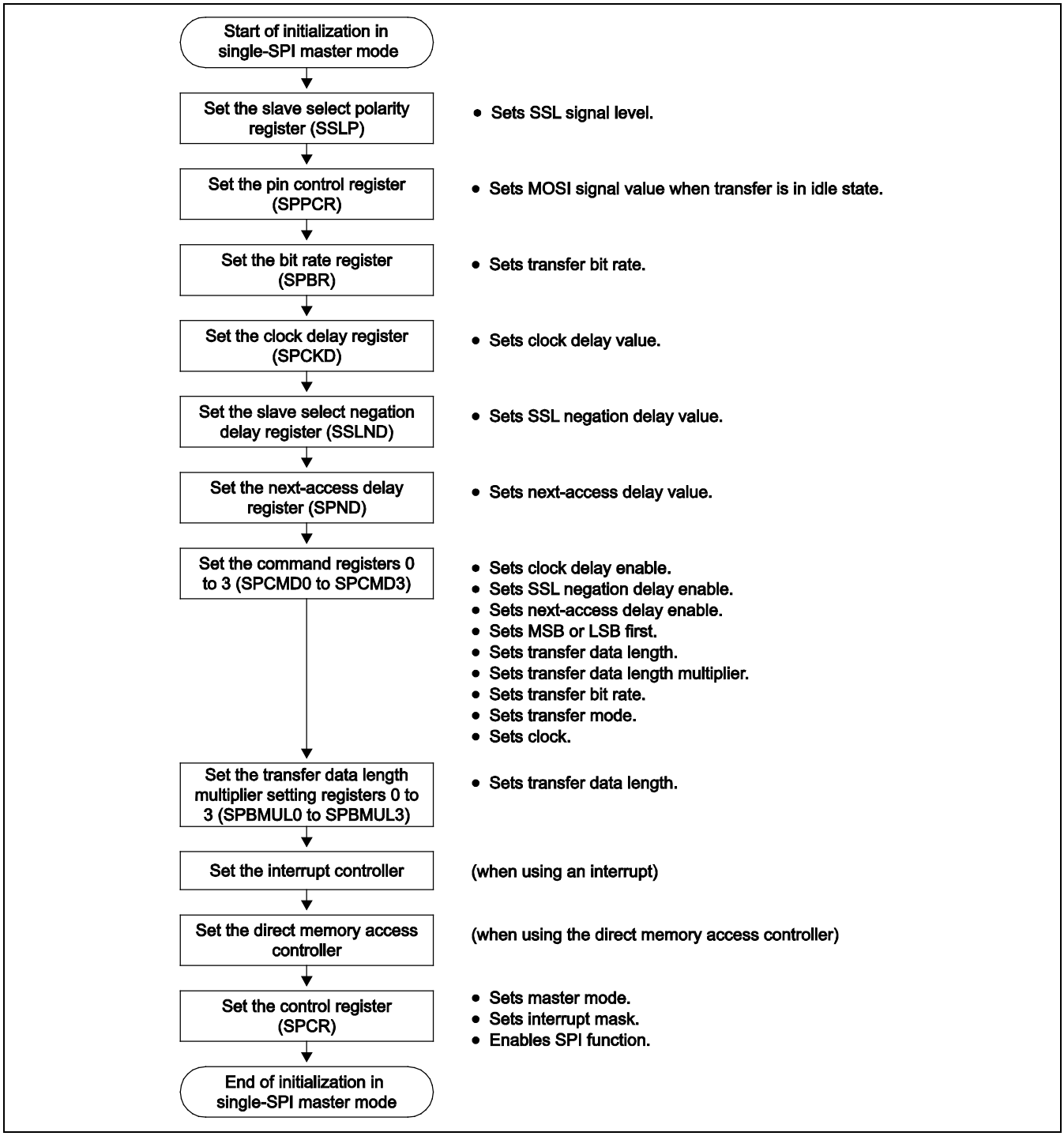


Figure 39.14 Example of Initialization Flowchart in Single-SPI Master Mode

(f) Transfer operation flowchart

Figure 39.15 is a flowchart illustrating a transfer in SPI operation when this module is used in single-SPI master mode. Burst transfer by setting the transfer data length is also executed based on this flowchart.

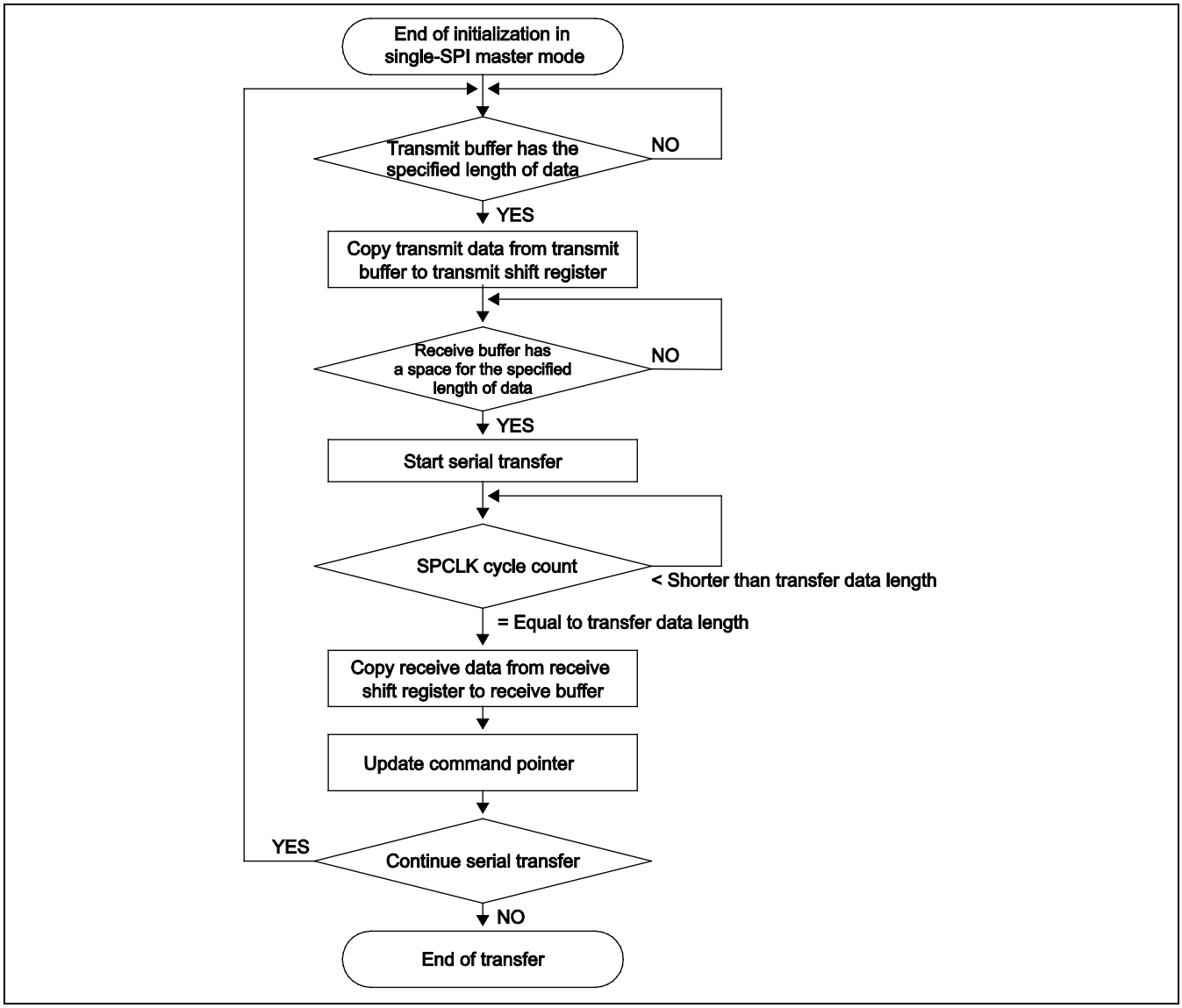


Figure 39.15 Transfer Operation Flowchart in Single-SPI Master Mode

(2) Dual-SPI/Quad-SPI mode

(a) Starting serial transfer

In dual-/quad-SPI modes, the serial transfer start condition differs depending on the data transfer direction (transmission or reception).

In data transmission, the serial transfer start condition is that there is the specified length of data in the transmit buffer.

In data reception, the serial transfer start condition is that there is a space for the specified length of data in the receive buffer.

(b) Terminating serial transfer

Irrespective of data transmission or reception, this module terminates the serial transfer after transmitting an SPCLK edge corresponding to the final sampling timing.

During idle cycles in dual-/quad-SPI modes, the IO pins are controlled differently depending on whether it is after write or read operation. Specifically, the IO pins output either the last output data or the fixed level depending on the register setting after write operation, whereas the IO pins are driven to the Hi-Z state after read operation. Figure 39.16 shows an example of the pin states after quad-SPI mode access is completed. The following describes operations (1) and (2) in the figure.

(1) During write operation, IO0 to IO3 serve as output pins. Thus, when SSL is negated upon completion of write operation, IO0 to IO3 output different values depending on the value of MOIFE in the SPPCR. Specifically, the IO pins output the level specified by MOIFV when MOIFE is 1, whereas the IO pins output the last output data when MOIFE is 0.

(2) During read operation, IO0 to IO3 serve as input pins. Thus, when SSL is negated upon completion of read operation, IO0 to IO3 are driven to Hi-Z state irrespective of the values of MOIFE and MOIFV.

For details on the pin control in dual-/quad-SPI modes, see section 39.5.2, Pin Control.

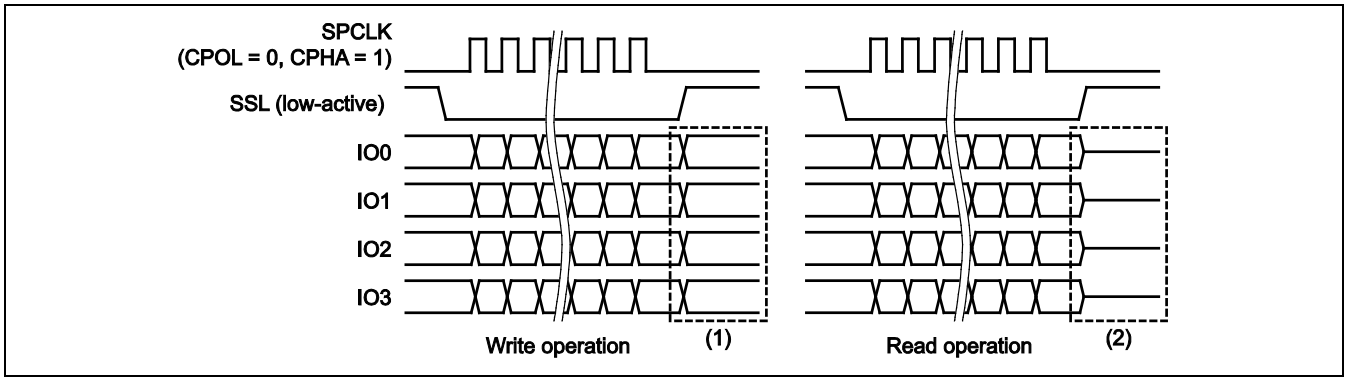


Figure 39.16 Example of Pin States after Quad-SPI Mode Access is Completed

(c) Sequence control

As with the single-SPI master mode, in dual-/quad-SPI modes, according to the sequence length that is assigned to SPSCR, this module makes up a sequence comprised of SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. For details on operation, see section 39.5.7 (1) (c), Sequence control.

Dual-/quad-SPI modes only provide operation of a single direction, that is, either transmission or reception for serial transfer. Transmission or reception is set using the SPI read/write access setting bit (SPRW) in SPCMD0 to SPCMD3. One of the three operating modes including dual-SPI mode, quad-SPI mode, and single-SPI master mode is set using the SPI operating mode setting bits (SPIMOD[1:0]) in SPCMD0 to SPCMD3. Combining these bits allows switching single-SPI master mode, dual-SPI mode transmission/reception, and quad-SPI mode transmission/reception to control sequence. Figure 39.17 shows an example of sequence configuration with transfer mode switching.

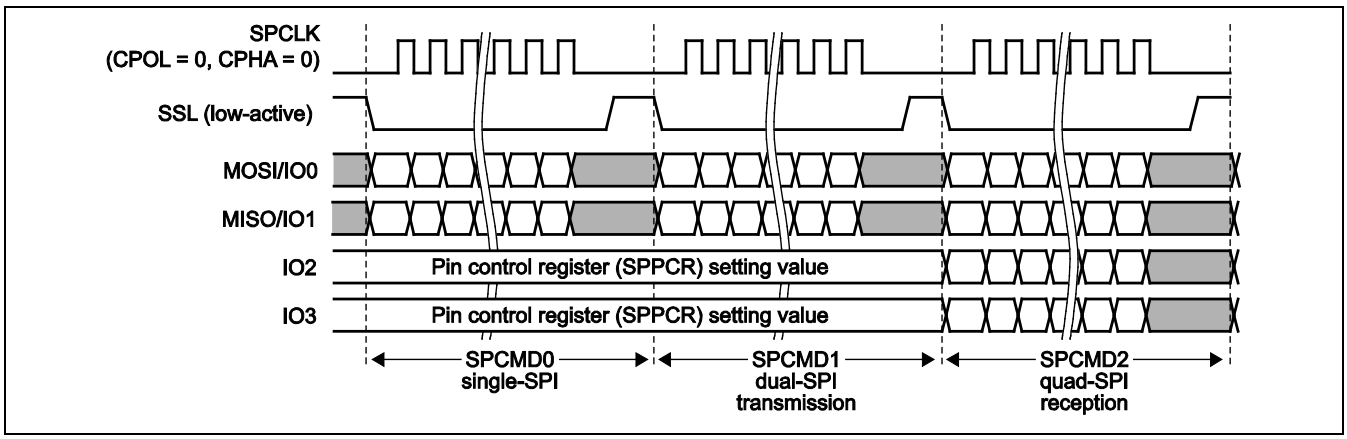


Figure 39.17 Example of Sequence Configuration with Transfer Mode Switching

Note the following when configuring a sequence in dual-/quad-SPI modes.

When all the commands configuring a sequence are dual-/quad-SPI read operations, the sequential operation is continued as long as the receive buffer has an enough space for the receive data.

To terminate read operation, clear the SPE bit to 0 in SPCR after receiving the required length of data, or execute write operation for the last sequence to empty the transmit buffer.

(d) Burst transfer

This module can execute burst transfer with the following two methods in dual/quad SPI modes.

One method uses the SPB[3:0] bits in SPCMD0 to SPCMD3 and SPBMUL0 to SPBMUL3. As with the single-SPI master mode, setting SPB[3:0] to select 8, 16, or 32 bits and setting SPBMUL0 to SPBMUL3 to select one through 4,294,967,296 allows the specified length of data to be continuously transferred for the specified times, where the length is specified by SPB[3:0] and the number of times is specified by SPBMUL0 to SPBMUL3. However, if the transmit buffer (SPTXB) becomes empty during transfer, or the receive buffer (SPRXB) has no longer a space enough to receive the specified length of data defined by SPB[3:0], the clock is stopped until transfer is resumed. This method is effective to transfer a large amount of data in dual-/quad SPI modes. Figure 39.18 shows a burst transfer example in which SPB[3:0] are set to select 32 bits and SPBMUL to select four times thus specifying 128 bits as a total transfer data amount. The following describes operations (1) to (4) in the figure.

(1) First 32-bit data transfer

(2) Second 32-bit data transfer

(3) When the transmit buffer becomes empty or the receive buffer has no longer a space for 32 or more bits, the clock is stopped. Here, when IO3 to IO0 serve as output pins, IO3 to IO0 continue outputting the previous value. When IO3 to IO0 serve as input pins, the inputs to IO3 to IO0 depend on the output value of the device to communicate with. When data is written to the transmit buffer or an enough space is created in the receive buffer, the clock output is resumed to restart transfer.

(4) Third and fourth 32-bit data transfers

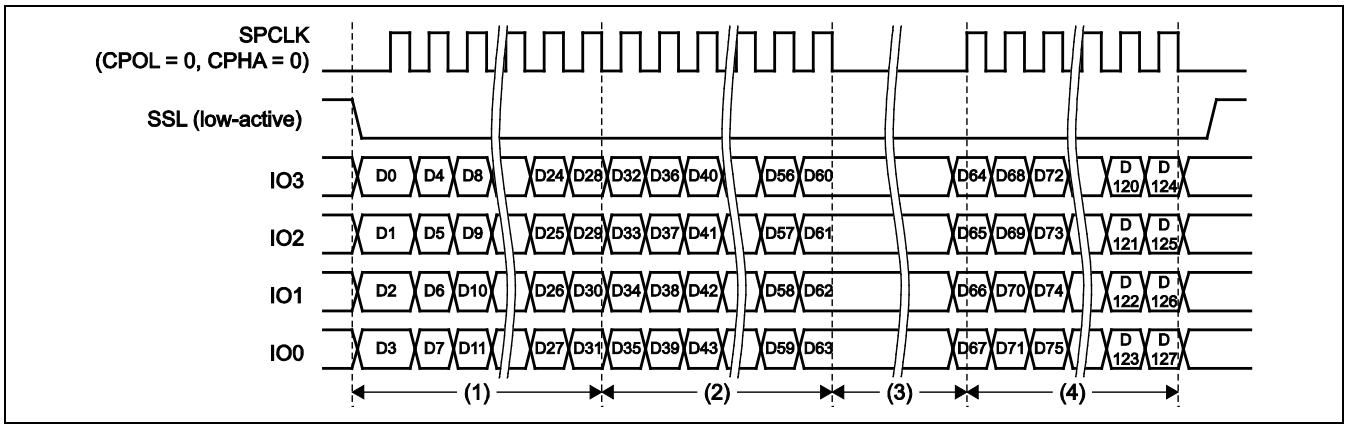


Figure 39.18 Burst Transfer Example in which Total Transfer Data Amount is 128 Bits (Quad-SPI Mode)

The other method uses the SSL signal level keeping function as in single-SPI master mode. Since this method allows switching the SPI transfer modes (single-/dual-/quad-SPI) during a transfer, it is particularly convenient when used with devices such as serial flash memory, where command data is written in single-SPI mode and data to be stored in memory is written in quad-SPI mode. Note, however, that at least one delay cycle should be inserted between transfers when switching the SPI transfer modes. Figure 39.19 shows a burst transfer example in which both single-SPI and quad-SPI modes are used. The following describes operations (1) to (6) in the figure.

(1) Clock delay period according to the SPCMD0 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the first transfer in the burst transfer.

(2) SSL negation delay period according to the SPCMD0 setting. Since SSLKP in SPCMD0 is set to 1, SSL is not negated even after SSL negation delay period is over. The SSL negation delay period depends on the SLNDEN bit setting in SPCMD0. When SLNDEN is 1, the SSL negation delay period is determined by the SSLND setting, and the delay period is 0 SPCLK cycle when SLNDEN is 0.

(3) Next-access delay period according to the SPCMD0 setting. Since SSLKP is set to 1, SSL is not negated even during the next-access delay period. The next-access delay period depends on the SPNDEN bit setting in SPCMD0. When SPNDEN is 1, the next-access delay period is determined by the SPND setting, and the delay period is 0 SPCLK cycle when SPNDEN is 0.

(4) Clock delay period according to the SPCMD1 setting. The clock delay period depends on the SCKDEN bit setting in SPCMD1. When SCKDEN is 1, the clock delay period is determined by the SPCKD setting, and the delay period is 0 SPCLK cycle when SCKDEN is 0.

(5) SSL negation delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Since SSLKP in SPCMD1 is set to 0, SSL is negated after SSL negation delay period is over.

(6) Next-access delay period according to the SPCMD1 setting. The setting must be made so that the delay period should be at least one SPCLK cycle for the last transfer in the burst transfer. Be sure to set SSLKP to 0 to negate SSL.

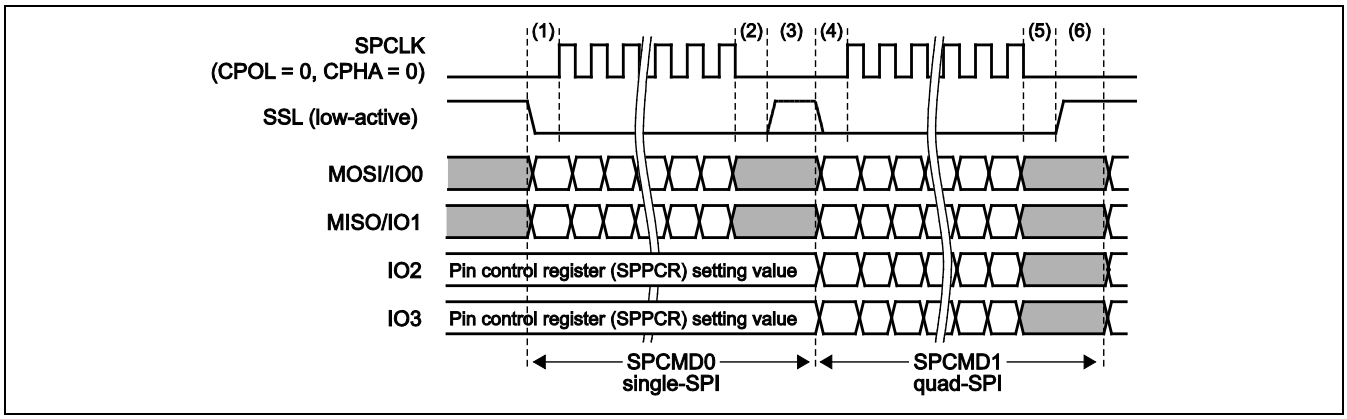


Figure 39.19 Burst Transfer Example in which SSL Signal Level Keeping Function is Used (Single- and Quad-SPI Modes Used)

(e) Initialization flowchart

Figure 39.20 is a flowchart illustrating an example of initialization in SPI operation when this module is used in dual-/quad-SPI mode. For a description of how to set up the interrupt controller and direct memory access controller, see the descriptions given in the individual blocks.

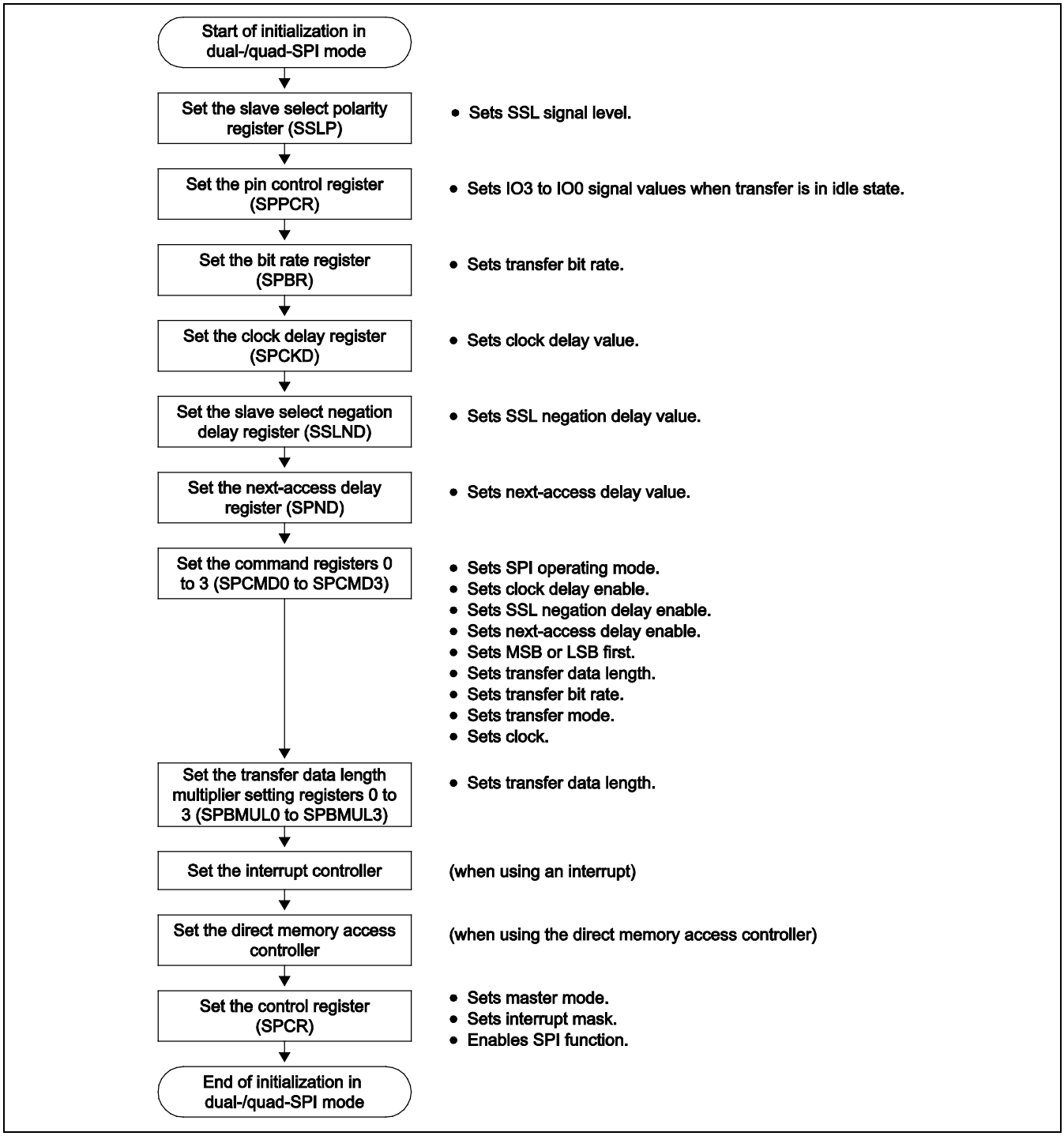


Figure 39.20 Example of Initialization Flowchart in Dual-/Quad-SPI Mode

(f) Transfer operation flowchart

Figure 39.21 is a flowchart illustrating a transfer in SPI operation when this module is used in dual-/quad-SPI mode.

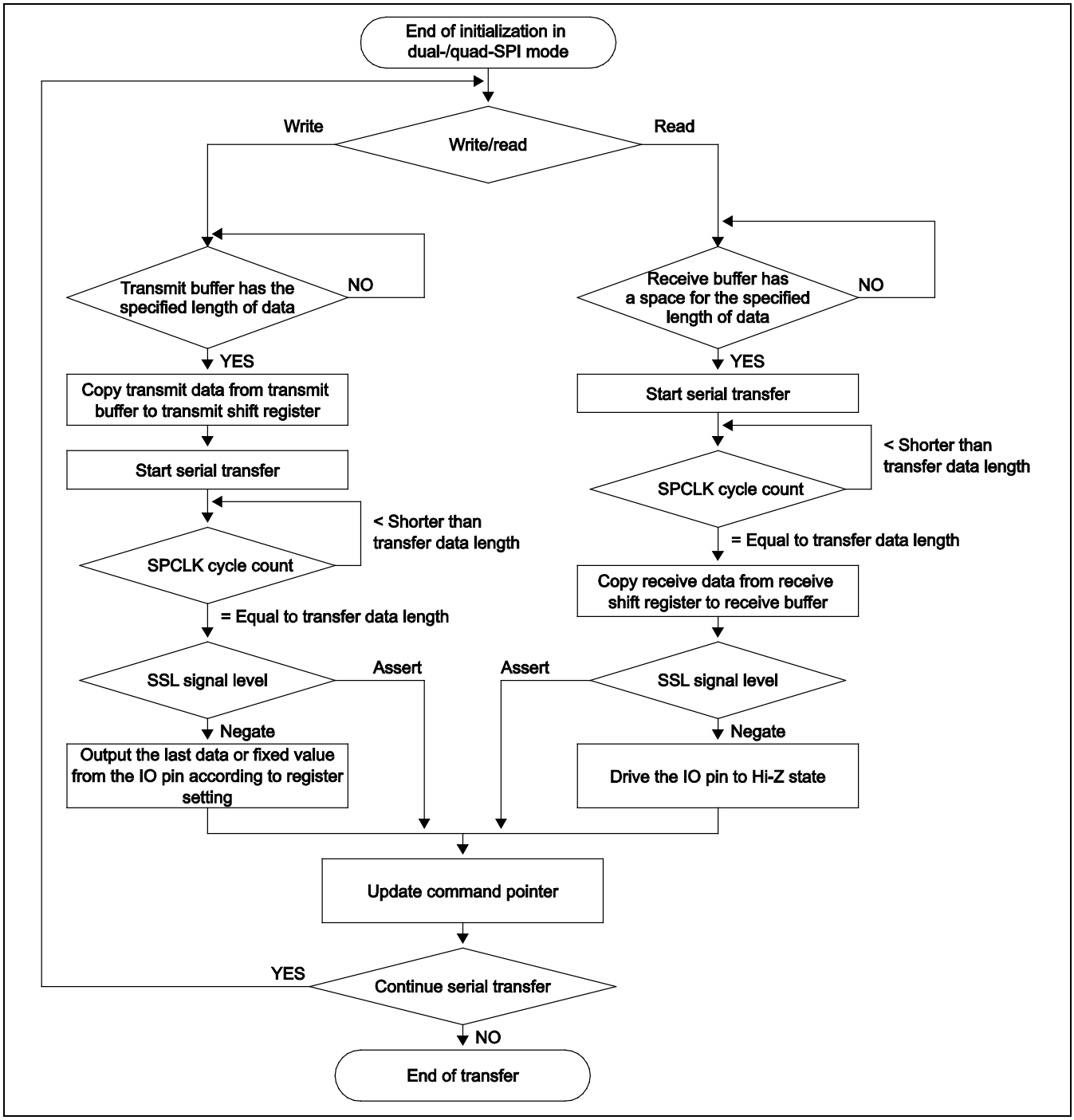


Figure 39.21 Transfer Operation Flowchart in Dual-/Quad-SPI Mode

39.5.8 Interrupt Sources

This module has interrupt sources of receive buffer full, transmit buffer empty, underrun error, overrun error, and mode fault error. In addition, the direct memory access controller can be activated by the receive buffer full or transmit buffer empty interrupt for data transfer.

Table 39.9 shows the interrupt sources.

When any of the interrupt conditions in Table 39.9 is met, an interrupt is generated. The interrupt sources should be cleared with data transfer by the CPU or direct memory access controller.

Table 39.9 Interrupt Sources

Name	Interrupt Source	Abbreviation	Interrupt Condition	Activation of Direct Memory Access Controller
SPRI	Receive buffer full	RXI	SPRIE = 1 and SPRFF = 1	Possible
SPTI	Transmit buffer empty	TXI	SPTIE = 1 and SPTEF = 1	Possible
SPEI	Underrun error	UDI	SPEIE = 1 and UDRF = 1	Not possible
	Overrun error	OVI	SPEIE = 1 and OVRF = 1	Not possible
	Mode fault error	MOI	SPEIE = 1 and MODF = 1	Not possible

39.5.9 Loopback Mode

This module provides loopback mode for testing. Writing 1 to the loopback mode bit (SPLP) in the pin control register (SPPCR) enables loopback mode. In loopback mode, this module disconnects the paths between the transmit/receive shift registers and the MISO/MOSI and IO3 to IO0 pins, and connects the outputs from the transmit shift register to the inputs to the receive shift register instead. Figure 39.22 shows a schematic internal connection in loopback mode.

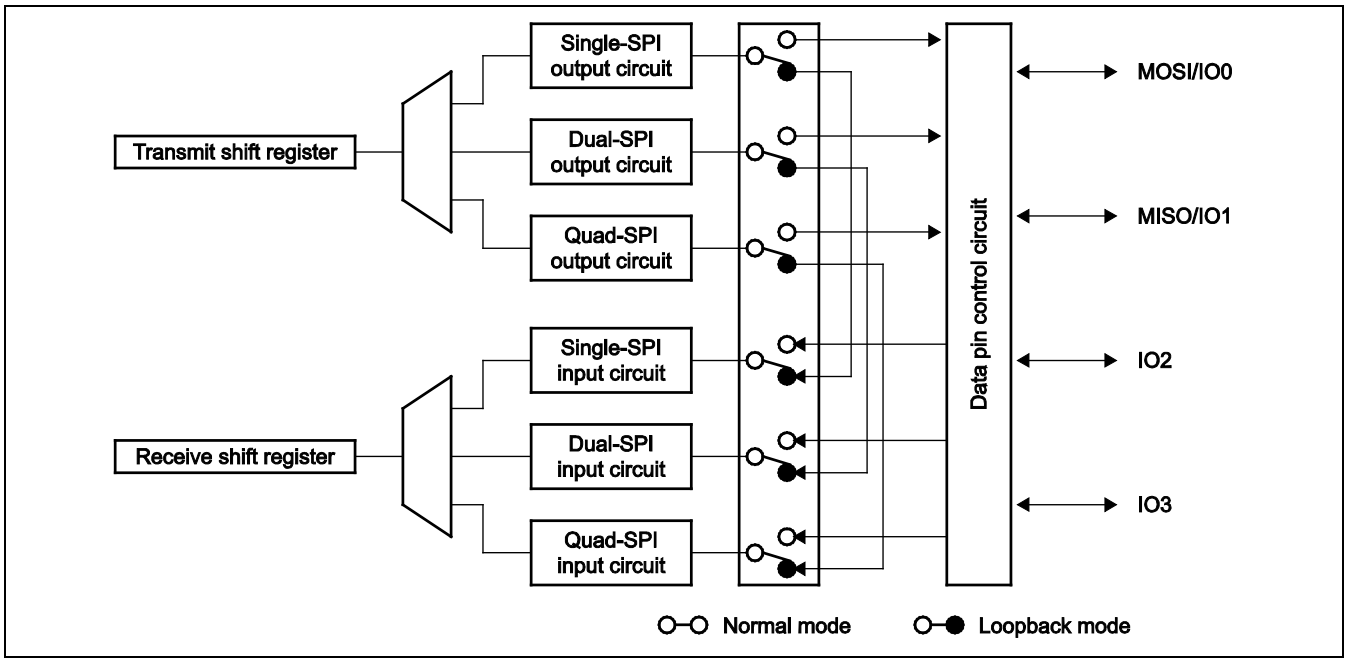


Figure 39.22 Schematic Internal Connection in Loopback Mode

40. SD Card/MMC Interfaces

40.1 Overview

40.1.1 Features

This LSI has three SD card interfaces (SDHI0 to SDHI2), one of which can also be used as MMC interfaces (SDHI1). The select setting of SDHI and MMC is unnecessary.

- SD memory/IO card interface (1-bit/4-bit SD bus)
- SD, SDHC, and SDXC SD memory card access supported
- Default, high-speed, UHS-I/SDR50, and SDR104 transfer modes supported
  SDR104 mode is only SDHI0 and SDHI1.
- SD clock (SDCLK) frequency = internal SDxϕ* frequency/2^n (n = 0 to 9)
- SDCLK = 156 MHz (SDR104)
- SDCLK = 78 MHz (SDR50)
- Error check function: CRC7 (for command/response), CRC16 (for data)
- Interrupt request: 2/CH
- Card detect function
- Write protect support
- MMC interface (1-bit/4-bit/8-bit MMC bus)
- eMMC device access supported
- Backward-compatible, high-speed, HS200 transfer modes supported
- MMCCLK = 156 MHz (HS200)
- High-priority interrupt (HPI) supported
- Alternative Boot operation supported

Note: * x = 0, 2

Development of the SD-related products needs the conclusion of the following agreement.

SD Host/Ancillary Product License Agreement (SD HALA)

40.1.2 Block Diagram

Figure 40.1 shows a block diagram of the SD host interface.

SDHI0 and SDHI2 is APB interface. SDHI1(MMC0) is AXI interface.

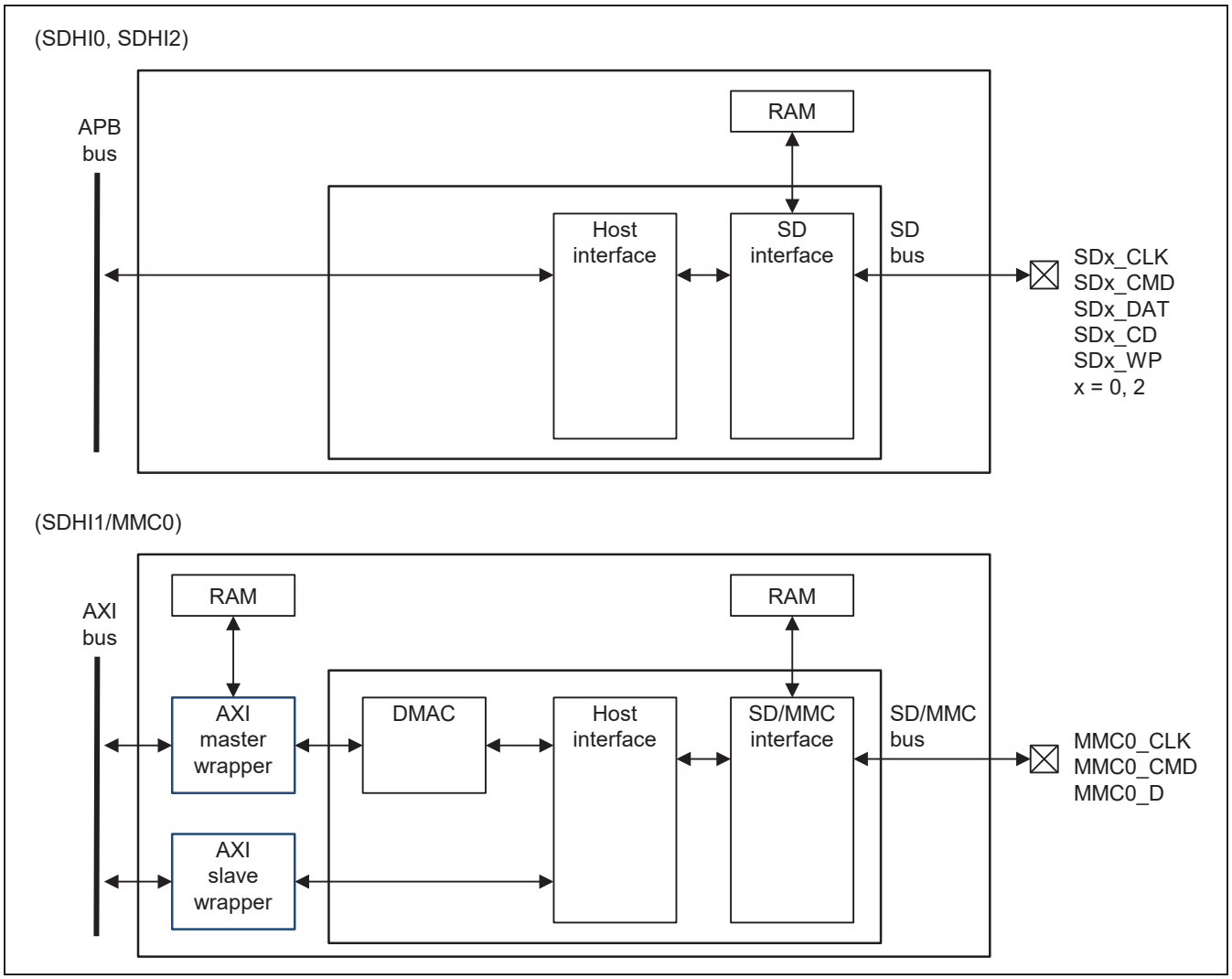


Figure 40.1 Block Diagram of SD Host Interface

40.1.3 Input / Output Pins

Table 40.1 lists the input and output pins used by the interface. The voltage of the SDHI terminal is variable. Therefore a power network is separate.

Table 40.1 Pin Configuration

PIN Name	I/O	Function	Voltage
SDx_CLK*	O	SD clock	Voltage switch of 1.8 V/3.3 V
SDx_CMD*	I/O	Command/response	Voltage switch of 1.8 V/3.3 V
SDx_DAT0*	I/O	Data [bit 0]	Voltage switch of 1.8 V/3.3 V
SDx_DAT1*	I/O	Data [bit 1]/SDIO interrupt	Voltage switch of 1.8 V/3.3 V
SDx_DAT2*	I/O	Data [bit 2]/Read wait	Voltage switch of 1.8 V/3.3 V
SDx_DAT3*	I/O	Data [bit 3]/Card detect	Voltage switch of 1.8 V/3.3 V
SDx_CD*	I	Card detect	3.3 V
SDx_WP*	I	Write protect	3.3 V
MMC0_CLK(SD1_CLK)	O	MMC clock	Voltage switch of 1.8 V/3.3 V
MMC0_CMD(SD1_CMD)	I/O	Command/response	Voltage switch of 1.8 V/3.3 V
MMC0_D0(SD1_DAT0)	I/O	Data [bit 0]	Voltage switch of 1.8 V/3.3 V
MMC0_D1(SD1_DAT1)	I/O	Data [bit 1]	Voltage switch of 1.8 V/3.3 V
MMC0_D2(SD1_DAT2)	I/O	Data [bit 2]	Voltage switch of 1.8 V/3.3 V
MMC0_D3(SD1_DAT3)	I/O	Data [bit 3]	Voltage switch of 1.8 V/3.3 V
MMC0_D4(SD1_CD)	I/O	Data [bit 4]	Voltage switch of 1.8 V/3.3 V
MMC0_D5(SD1_WP)	I/O	Data [bit 5]	Voltage switch of 1.8 V/3.3 V
MMC0_D6	I/O	Data [bit 6]	Voltage switch of 1.8 V/3.3 V
MMC0_D7	I/O	Data [bit 7]	Voltage switch of 1.8 V/3.3 V

Note: * x = 0, 2

It may lead to device destruction. Please the voltage setting and applied voltage to match.

41. USB2.0 Host (EHCI/OHCI)

41.1 Overview

This module is a USB2.0 host controller conforming to the Enhanced Host Controller Interface (EHCI) Specification for USB Rev. 1.1.

It can also be used as a dual-role device (DRD) in combination with a peripheral link module connected to the external UTMI+ interface.

41.1.1 Features

The following shows the features of this module.

Function	Description
Host function	• Supports High-speed (480 Mbps), Full-speed (12 Mbps), and Low-speed (1.5 Mbps) transfer. • Conforms to the Open Host Controller Interface (OHCI) Specification for USB Rev. 1.0a. • Conforms to the Enhanced Host Controller Interface (EHCI) Specification for USB Rev. 1.1.*1
Peripheral function	The peripheral function is available through a peripheral controller module connected to the external UTMI+ interface
Accessible memory space	32 bits
USB port count	Downstream port: 1 port for each channel Upstream port: 1 port*2
Other functions	• Dual-role device function (static switching between the USB host and peripheral functions)

Notes: 1. Some functions (specifications) are not supported.
2. Only when HS USB module is selected.
3. The peripheral function is assumed to be controlled by a HS USB module.

41.1.2 Input/Output Pins

Table 41.1 Pin Configuration of USB

Classification	Pin Name	Name	I/O	Description
USB bus interface	USB0_DP	USB channel 0 D+ data	I/O	D+ Input/output of the on-chip transceiver Connect this pin to the D+ pin of the USB bus channel 0
	USB0_DM	USB channel 0 D- data	I/O	D- Input/output of the on-chip transceiver Connect this pin to the D- pin of the USB bus channel 0
	USB1_DP	USB channel 1 D+ data	I/O	D+ Input/output of the on-chip transceiver Connect this pin to the D+ pin of the USB bus channel 1
	USB1_DM	USB channel 1 D- data	I/O	D- Input/output of the on-chip transceiver Connect this pin to the D- pin of the USB bus channel 1
Reference resistance	RREF	USB external reference resistor	I	Connect to external 5.6kΩ±1% resistor.
VBUS	USB0_VBUS	USB channel 0 VBUS	I	The external series resistor is not required Connect this pin to the USB VBUS channel 0. Supply 5V, even if the host function is used.
	USB1_VBUS	USB channel 1 VBUS	I	The external series resistor is not required Connect this pin to the USB VBUS channel 1. Supply 5V, even if the host function is used.
Over current	USB0_OVC	USB channel 0 Over current	I/O	Connect to over current detection pin of external power IC which supply VBUS power. This is low active signal
	USB1_OVC	USB channel 0 Over current	I/O	Connect to over current detection pin of external power IC which supply VBUS power. This is low active signal
Power Enable	USB0_PWEN	USB channel 0 Power enable	I/O	Connect to power enable pin of external power IC which supply VBUS power
	USB1_PWEN	USB channel 0 Power enable	I/O	Connect to power enable pin of external power IC which supply VBUS power

41.2 Register Configuration

41.2.1 Register Attributes

Table 41.2 Register Bit-field types

Register Attribute	Description
R/W	Register bits can be read and written.
RW1C	Register bits can be read. A clear bit may be set by writing “1”; writing 0 to RW1C bits has no effect.
RWT	Register bits can be read. An inversion bit may be set by writing “1”; writing 0 to RWT bits has no effect.
RW1S	Register bits can be read and written. A bit may be set to 1 by writing “1”; writing 0 to RW1S bits has no effect.
R	Register bits can only be read.
W	Register bits can only be written.
Reserved	Reserved bits are Read Only field.

41.2.2 Address Mappings

Table 41.3 EHCI/OHCI Base Address

EHCI/OHCI	Base Address
Channel 0	H'EE08 0000
Channel 1	H'EE0C 0000

H'FFC H'834	Reserved
H'800	UCOM registers
  H’40C	Reserved
H'400	Renesas UTMI + PHY setting registers
H'370	Reserved
H'360	Core defined registers
H'348	Reserved
H'340	Core defined registers
H'328	Reserved
H'300	Core defined registers
H’210	Reserved
H'200	AHB registers
H'1F4	Reserved
H'1F0	EHCI operational registers
H’16C	Reserved
H'160	EHCI operational registers
H’13C	Reserved
H'120	EHCI operational registers
H’110	Reserved
H'100	EHCI capabilityregisters
H’064	Reserved
H'000	OHCI operational registers

Figure 41.1 Address Map

41.2.3 Register Overview

Register Name	Abbreviation	Address Offset	Access Size	Remarks
HcRevision	HcRevision	H'000	32	OHCI operational registers
HcControl	HcControl	H'004	32	
HcCommandStatus	HcCommandStatus	H'008	32	
HcInterruptStatus	HcInterruptStatus	H'00C	32	
HcInterruptEnable	HcInterruptEnable	H'010	32	
HcInterruptDisable	HcInterruptDisable	H'014	32	
HcHCCA	HcHCCA	H'018	32	
HcPeriodCurrentED	HcPeriodCurrentED	H'01C	32	
HcControlHeadED	HcControlHeadED	H'020	32	
HcControlCurrentED	HcControlCurrentED	H'024	32	
HcBulkHeadED	HcBulkHeadED	H'028	32	
HcBulkCurrentED	HcBulkCurrentED	H'02C	32	
HcDoneHead	HcDoneHead	H'030	32	
HcFmInterval	HcFmInterval	H'034	32	
HcFmRemaining	HcFmRemaining	H'038	32	
HcFmNumber	HcFmNumber	H'03C	32	
HcPeriodicStart	HcPeriodicStart	H'040	32	
HcLSThreshold	HcLSThreshold	H'044	32	
HcRhDescriptorA	HcRhDescriptorA	H'048	32	
HcRhDescriptorB	HcRhDescriptorB	H'04C	32	
HcRhStatus	HcRhStatus	H'050	32	
HcRhPortStatus1	HcRhPortStatus1	H'054	32	
Reserved	—	H'058	—	
Reserved*	—	H'064 to H'0FC	—	

Note: * This area is read as 0. The write value should be 0.

Register Name	Abbreviation	Address Offset	Access Size	Remarks
HCIVERSION / CAPLENGTH	CAPL_VERSION	H'100	32	EHCI capability registers
HCSPARAMS	HCSPARAMS	H'104	32	
HCCPARAMS	HCCPARAMS	H'108	32	
HCSP_PORTROUTE	HCSP_PORTROUTE	H'10C	32	
Reserved*	—	H'110 to H'11C	32	
USBCMD	USBCMD	H'120	32	EHCI operational registers
USBSTS	USBSTS	H'124	32	
USBINTR	USBINTR	H'128	32	
FRINDEX	FRINDEX	H'12C	32	
CTRLDSSEGMENT	CTRLDSSEGMENT	H'130	32	
PERIODICLISTBASE	PERIODICLISTBASE	H'134	32	
ASYNCLISTADDR	ASYNCLISTADDR	H'138	32	
Reserved*	—	H'13C to H'15C	32	
CONFIGFLAG	CONFIGFLAG	H'160	32	
PORTSC1	PORTSC1	H'164	32	
Reserved	—	H'168	32	
Reserved *	—	H'16C to H'3FC	32	
INT_ENABLE	INT_ENABLE	H'200	32	AHB bridge registers
INT_STATUS	INT_STATUS	H'204	32	
AHB_BUS_CTR	AHB_BUS_CTR	H'208	32	
USBCTR	USBCTR	H'20C	32	
Reserved*	—	H'210 to H'2FC	32	
REVID	REVID	H'300	32	Core defined registers
Register Enable/Clock Gating Control	REGEN_CG_CTRL	H'304	32	
Suspend Control	SPD_CTRL	H'308	32	
Suspend/Resume Timer Setting	SPD_RSM_TIMSET	H'30C	32	
Overcurrent Detection Timer Setting	OC_TIMSET	H'310	32	
SBRN, FLADJ, PORTWAKECAP	SBRN_FLADJ_PW	H'314	32	
Reserved*	—	H'318 to H'7FC	—	
Reserved*	—	H'814 to H'81C	—	
Reserved*	—	H'824 to H'82C	—	
Reserved*	—	H'834 to H'BFC	—	

Note: * An undefined value is read. When this area is written to, operation is not defined.

41.3 Register Description

41.3.1 OHCI Operational Registers

41.3.1.1 HcRevision Register (offset: H'000)

Register symbol: HcRevision

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Revision							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 8	—	R	R	All 0	Reserved
7 to 0	Revision	R	R	H'10	This field contains the BCD representation of the version of the OHCI specification that is implemented by this host controller core. This core supports OHCI 1.0a and this field shows H'10.

41.3.1.2 HcControl Register (offset: H'004)

Register symbol: HcControl

The HcControl register defines the operating modes as the classic host controller. Most of the fields in this register are modified only by software, except HostControllerFunctionalState and RemoteWakeupConnected.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	RWE	RWC	IR	HCFS		BLE	CLE	IE	PLE	CBSR	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 11	Reserved	R	R	All 0	This field shows a BCD encoding of the EHCI revision number supported by this host controller core. This host controller core supports EHCI v.1.1.
10	RWE	RW	R	0	RemoteWakeupEnable This bit is used by software to enable or disable the remote wakeup feature upon the detection of upstream resume signaling. When this bit is set and the ResumeDetected bit in HcInterruptStatus is set, a remote wakeup is signaled to the host system. Setting this bit has no impact on the generation of hardware interrupt. 0: An interrupt due to remote wakeup is not generated. 1: An interrupt due to remote wakeup is generated.
9	RWC	RW	RW	0	RemoteWakeupConnected This bit indicates whether the host controller supports remote wakeup signaling. Software should set this bit to 1 in the initialization sequence if it is required to support remote wakeup. The host controller clears this bit to 0 upon hardware reset but does not alter it upon software reset. 0: The remote wakeup is not supported. 1: The remote wakeup is supported.
8	IR	RW	R	0	InterruptRouting This bit determines the routing of interrupts generated by events registered in HcInterruptStatus. If this bit is 0, all interrupts are routed to the normal host bus interrupt mechanism. If this bit is set to 1, interrupts are routed to the System Management Interrupt. Software clears this bit upon a hardware reset, but it does not alter this bit upon a software reset.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
7, 6	HCFS	RW	RW	00	HostControllerFunctionalState 00: USB Reset 01: USB Resume 10: USB Operational 11: USB Suspend. This field defines the functional state of the host controller. The transition to USB Operational state from another state causes SOF generation to show 1-ms frame boundary. Software controls this bit basically; this field may be changed by the host controller only when in the USB Suspend state. The host controller may move from the USB Suspend state to the USB Resume state after detecting the resume signaling from a downstream port. The host controller enters USB Suspend state after software reset, whereas it enters USB Reset state after hardware reset.
5	BLE	RW	R	0	BulkListEnable This bit is set to 1 in order to enable the processing of the Bulk list in the next Frame. If this bit is 0, processing of the Bulk list does not occur after the next SOF. The host controller checks this bit whenever it determines to process the list. When software modifies the Bulk list, it should set this bit to 0 before modifying the list. 0: The processing of the Bulk list is disabled. 1: The processing of the Bulk list is enabled.
4	CLE	RW	R	0	ControlListEnable This bit is set to 1 in order to enable the processing of the Control list in the next Frame. If this bit is 0, processing of the Control list does not occur after the next SOF. The host controller checks this bit whenever it determines to process the list. When software modifies the Control list, it should set this bit to 0 before modifying the list. 0: The processing of the Control list is disabled. 1: The processing of the Control list is enabled.
3	IE	RW	R	0	IsochronousEnable This bit is set to 1 in order to enable the processing of isochronous EDs. While processing the periodic list in a Frame, the host controller checks the status of this bit when it finds an Isochronous ED (F = 1). If this bit is 1 (enabled), the host controller continues processing the EDs. If this bit is 0 (disabled), the host controller halts processing of the periodic list (which contains only isochronous EDs right now) and begins processing the Bulk/Control lists. Setting this bit is guaranteed to take effect in the next Frame (not the current Frame). 0: The processing of the isochronous ED is disabled. 1: The processing of the isochronous ED is enabled.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
2	PLE	RW	R	0	PeriodicListEnable This bit is set to enable the processing of the periodic list in the next Frame. If cleared to 0 by software, processing of the periodic list does not occur after the next SOF. The host controller checks this bit before it starts processing the periodic list. 0: The processing of the periodic list is disabled. 1: The processing of the periodic list is enabled.
1, 0	CBSR	RW	R	00	ControlBulkServiceRatio This field specifies the service ratio between Control and Bulk EDs. In case of reset, software should restore the value in this field. **CBSR No. of Control EDs Over Bulk EDs Served** 00: 1:1 01: 2:1 10: 3:1 11: 4:1

41.3.1.3 HcCommandStatus Register (offset: H'008)

Register symbol: HcCommandStatus

The HcCommandStatus register is used by the host controller to receive commands issued by software, as well as reflecting the current status of the host controller.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SOC	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	OCR	BLF	CLF	HCR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	W	R/W	R/W	W

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 18	—	R	R	All 0	Reserved
17, 16	SOC	R	RW	00	SchedulingOverrunCount This field is incremented on each scheduling overrun error. It is initialized to B'00 and wraps around at B'11. This field is incremented when a scheduling overrun is detected even if SchedulingOverrun in HcInterruptStatus register has already been set.
15 to 4	—	R	R	All 0	Reserved
3	OCR	W	RW	0	OwnershipChangeRequest This bit is set by software to request a change of control of the host controller. When this bit is set to 1, the host controller sets the OwnershipChange bit in HcInterruptStatus register. After the changeover, this bit is cleared to 0. 0: The change of control of the host controller is not requested. 1: The change of control of the host controller is requested.
2	BLF	RW	RW	0	BulkListFilled This bit is used to indicate whether there are any TDs on the Bulk list. It is set by software whenever it adds a TD to an ED in the Bulk list. When the host controller begins to process the head of the Bulk list, it checks BLF bit. As long as BLF bit is 0, the host controller does not start processing the Bulk list. If BLF bit is 1, the host controller starts processing the Bulk list and sets BLF bit to 0. If the host controller finds a TD on the list, then the host controller set BLF bit to 1 causing the Bulk list processing to continue. If no TD is found on the Bulk list, and if software does not set BLF bit, then BLF bit remains at 0 when the host controller completes processing the Bulk list and Bulk list processing will stop. 0: TD exists in the Bulk list. 1: TD does not exist in the Bulk list.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
1	CLF	RW	RW	0	ControlListFilled This bit is used to indicate whether there are any TDs on the Control list. It is set by software whenever it adds a TD to an ED in the Control list. When the host controller begins to process the head of the Control list, it checks CLF bit. As long as CLF bit is 0, the host controller does not start processing the Control list. If CLF bit is 1, the host controller starts processing the Control list and sets CLF bit to 0. If the host controller finds a TD on the list, then the host controller set CLF bit to 1 causing the Control list processing to continue. If no TD is found on the Control list, and if software does not set CLF bit, then CLF bit remains at 0 when the host controller completes processing the Control list and Control list processing will stop. 0: TD exists in the Control list. 1: TD does not exist in the Control list.
0	HCR	W	RW	0	HostControllerReset This bit is set by software to initiate software reset of the host controller. Regardless of the functional state of the host controller, it moves to the USB Suspend state. This bit is cleared to 0 by the host controller upon the completion of the reset operation. 0: The software reset of the host controller is not requested. 1: The software reset of the host controller is requested.

41.3.1.4 HcInterruptStatus Register (offset: H'00C)

Register symbol: HcInterruptStatus

This register provides status on various events that cause hardware interrupts. When an event occurs, the host controller sets the corresponding bit in this register. When a bit becomes set, an interrupt is generated if the interrupt is enabled in the HcInterruptEnable register and the MasterInterruptEnable bit is set.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	OC	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RHSC	FNO	UE	RD	SF	WDH	SO
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31	—	R	R	0	Reserved
30	OC	RW	RW	0	OwnershipChange This bit is set by the host controller when software sets the OwnershipChangeRequest field in HcCommandStatus register. 0: The ownership change has not been requested. 1: The ownership change has been requested.
29 to 7	—	R	R	All 0	Reserved
6	RHSC	RW	RW	0	RootHubStatusChange This bit is set when the content of HcRhStatus or the content of any of HcRhPortStatus [NumberofDownstreamPort] has changed. 0: The status of root hub has not changed. 1: The status of root hub has changed.
5	FNO	RW	RW	0	FrameNumberOverflow This bit is set when the MSB of HcFmNumber (bit 15) changes value, from 0 to 1 or from 1 to 0, and after HccaFrameNumber has been updated. 0: The overflow of frame number has not occurred. 1: The overflow of frame number has occurred.
4	UE	RW	RW	0	UnrecoverableError This bit is set when the host controller detects a system error not related to USB (system bus error, for example). The host controller should not proceed with any processing nor signaling before the system error has been corrected. Software clears this bit after the host controller has been reset in that case. 0: The unrecoverable error has not occurred. 1: The unrecoverable error has occurred.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
3	RD	RW	RW	0	ResumeDetected This bit is set when the host controller detects that USB device is asserting resume signaling. This bit is not set when Software sets the USB Resume state. 0: The host controller has not detected resume signaling. 1: The host controller has detected resume signaling.
2	SF	RW	RW	0	StartofFrame This bit is set by the host controller at each start of a frame and after the update of HccaFrameNumber. The host controller also generates a SOF token at the same time. 0: The host controller has not started new frame. 1: The host controller has started new frame.
1	WDH	RW	RW	0	WritebackDoneHead This bit is set immediately after the host controller has written HcDoneHead to HccaDoneHead. Further updates of the HccaDoneHead will not occur until this bit has been cleared. Software should only clear this bit after it has saved the content of HccaDoneHead. 0: The write back to HccaDoneHead has not occurred. 1: The write back to HccaDoneHead has occurred.
0	SO	RW	RW	0	SchedulingOverrun This bit is set when the USB schedule for the current Frame overruns and after the update of HccaFrameNumber. A scheduling overrun also increments the SchedulingOverrunCount of HcCommandSttus register. 0: The scheduling overrun has not occurred. 1: The scheduling overrun has occurred.

41.3.1.5 HcInterruptEnable Register (offset: H'010)

Register symbol: HcInterruptEnable

Each enable bit in the HcInterruptEnable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptEnable register is used to control which events generate a hardware interrupt.

A hardware interrupt is generated when all conditions below are satisfied.

1. A bit is set in HcInterruptStatus register
2. The corresponding bit in HcInterruptEnable register is set
3. MIE (MasterInterruptEnable) bit in HcInterruptEnable register is set

Writing 1 to a bit in this register sets the corresponding bit, whereas writing 0 to a bit in this register leaves the corresponding bit unchanged. On read, the current value of this register is returned.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MIE	OCE	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RHSCE	FNOE	UEE	RDE	SFE	WDHE	SOE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31	MIE	RW	R	0	MasterInterruptEnable Writing 1 to this bit enables an interrupt generation due to events specified in the other bits of this register. This bit is used by software as a Master interrupt Enable. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to events specified in the other bits of this register is disabled. 1: An interrupt generation due to events specified in the other bits of this register is enabled.
30	OCE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the request of ownership change. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the request of ownership change is disabled. 1: An interrupt generation due to the request of ownership change is enabled. Write 1 to OC bit in HcInterruptDisable register in order to clear this bit.
29 to 7	—	R	R	All 0	Reserved

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
6	RHSCE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the change of the status of root hub. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the change of the status of root hub is disabled. 1: An interrupt generation due to the change of the status of root hub is enabled. Write 1 to RHSC bit in HcInterruptDisable register in order to clear this bit.
5	FNOE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the overflow of frame number. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the overflow of frame number is disabled. 1: An interrupt generation due to the overflow of frame number is enabled. Write 1 to FNO bit in HcInterruptDisable register in order to clear this bit.
4	UEE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the unrecoverable error. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the unrecoverable error is disabled. 1: An interrupt generation due to the unrecoverable error is enabled. Write 1 to UE bit in HcInterruptDisable register in order to clear this bit.
3	RDE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the detection of resume signaling. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the detection of resume signaling is disabled. 1: An interrupt generation due to the detection of resume signaling is enabled. Write 1 to RD bit in HcInterruptDisable register in order to clear this bit.
2	SFE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the start of frame. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the start of frame is disabled. 1: An interrupt generation due to the start of frame is enabled. Write 1 to SF bit in HcInterruptDisable register in order to clear this bit.

Bit	Bit Name	R/W		Initial Value	Description
		HCD	HC		
1	WDHE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the write back to HccaDoneHead. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the write back to HccaDoneHead is disabled. 1: An interrupt generation due to the write back to HccaDoneHead is enabled. Write 1 to WDH bit in HcInterruptDisable register in order to clear this bit.
0	SOE	RW	R	0	Writing 1 to this bit enables an interrupt generation due to the scheduling overrun. Writing 0 to this bit is ignored by the host controller. 0: An interrupt generation due to the scheduling overrun is disabled. 1: An interrupt generation due to the scheduling overrun is enabled. Write 1 to SO bit in HcInterruptDisable register in order to clear this bit.

41.3.1.6 HcInterruptDisable Register (offset: H'014)

Register symbol: HcInterruptDisable

Each disable bit in the HcInterruptDisable register corresponds to an associated interrupt bit in the HcInterruptStatus register. The HcInterruptDisable register is coupled with the HcInterruptEnable register. Thus, writing 1 to a bit in this register clears the corresponding bit in the HcInterruptEnable register, whereas writing 0 to a bit in this register leaves the corresponding bit in the HcInterruptEnable register unchanged.

When this register is read, the current value of the HcInterruptEnable register is returned.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	MID	OCD	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	RHSCD	FNOD	UED	RDD	SFD	WDHD	SOD
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

		R/W			
Bit	**Bit Name**	**HWD**	**HC**	**Initial Value**	**Description**
31	MID	RW	R	0	MasterInterruptDisable Writing 1 to this bit disables interrupt generation due to events specified in the other bits of this register. Writing 0 to this bit is ignored by the host controller. When read, the value of MIE bit in HcInterruptEnable register is returned.
30	OCD	RW	R	0	Writing 1 disables an interrupt generation due to the request of ownership change. Writing 0 is ignored by the host controller. When read, the value of OC bit in HcInterruptEnable register is returned.
29 to 7	—	R	R	All 0	Reserved
6	RHSCD	RW	R	0	Writing 1 disables an interrupt generation due to the change of the status of root hub. Writing 0 is ignored by the host controller. When read, the value of RHSC bit in HcInterruptEnable register is returned.
5	FNOD	RW	R	0	Writing 1 disables an interrupt generation due to the overflow of frame number. Writing 0 is ignored by the host controller. When read, the value of FNO bit in HcInterruptEnable register is returned.
4	UED	RW	R	0	Writing 1 disables an interrupt generation due to the unrecoverable error. Writing 0 is ignored by the host controller. When read, the value of UE bit in HcInterruptEnable register is returned.

Bit	Bit Name	R/W		Initial Value	Description
		HWD	HC		
3	RDD	RW	R	0	Writing 1 disables an interrupt generation due to the detection of resume signaling. Writing 0 is ignored by the host controller. When read, the value of RD bit in HcInterruptEnable register is returned.
2	SFD	RW	R	0	Writing 1 disables an interrupt generation due to the start of frame. Writing 0 is ignored by the host controller. When read, the value of SF bit in HcInterruptEnable register is returned.
1	WDHD	RW	R	0	Writing 1 disables an interrupt generation due to the write back to HccaDoneHead. Writing 0 is ignored by the host controller. When read, the value of WDH bit in HcInterruptEnable register is returned.
0	SOD	RW	R	0	Writing 1 disables an interrupt generation due to the scheduling overrun. Writing 0 is ignored by the host controller. When read, the value of SO bit in HcInterruptEnable register is returned.

41.3.1.7 HcHCCA Register (offset: H'018)

Register symbol: HcHCCA

The HcHCCA register contains the physical address of the Host Controller Communication Area.

As HCCA has 256-byte structure, this host controller core requires 256-byte alignment for HcHCCA register. Therefore, bit 0 through bit 7 always return 0 even after 1 is written to them.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	HcHCCA[31:24]								HcHCCA[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	HcHCCA[15:8]								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 8	HcHCCA	RW	R	H'000 0000	This field contains the base address of the Host Controller Communication Area. This host controller requires 256-byte alignment for the base address.
7 to 0	—	R	R	All 0	Reserved

41.3.1.8 HcPeriodicCurrentED Register (offset: H'01C)

Register symbol: HcPeriodCurrentED

The HcPeriodCurrentED register contains the physical address of the current Isochronous or Interrupt Endpoint Descriptor.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PECD[31:24]								PECD[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PECD[15:8]								PECD[7:4]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 4	PECD	R	RW	H'000 0000	PeriodCurrentED This is used by the host controller to point to the head of one of the Periodic lists which will be processed in the current Frame. The content of this register is updated by the host controller after a periodic ED has been processed.
3 to 0	—	R	R	All 0	Reserved

41.3.1.9 HcControlHeadED Register (offset: H'020)

Register symbol: HcControlHeadED

The HcControlHeadED register contains the physical address of the first Endpoint Descriptor of the Control list.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CHED[31:24]								CHED[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CHED[15:8]								CHED[7:4]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 4	CHED	RW	R	H'000 0000	ControlHeadED The host controller traverses the Control list starting with the HcControlHeadED pointer. The content is loaded from HCCA during the initialization of the host controller.
3 to 0	—	R	R	All 0	Reserved

41.3.1.10 HcControlCurrentED Register (offset: H'024)

Register symbol: HcControlCurrentED

The HcControlCurrentED register contains the physical address of the current Endpoint Descriptor of the Control list.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CCED[31:24]								CCED[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCED[15:8]								CCED[7:4]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 4	CCED	RW	RW	H'000 0000	ControlCurrentED This pointer is advanced to the next ED after serving the present one. The host controller will continue processing the list from where it left off in the last Frame. When it reaches the end of the Control list, the host controller checks the ControlListFilled of in HcCommandStatus. If set, it copies the content of HcControlHeadED to HcControlCurrentED and clears the bit. If not set, it does nothing. Software is allowed to modify this register only when the ControlListEnable of HcControl is cleared. When set, software only reads the instantaneous value of this register. Initially, this is set to zero to indicate the end of the Control list.
3 to 0	—	R	R	All 0	Reserved

41.3.1.11 HcBulkHeadED Register (offset: H'028)

Register symbol: HcBulkHeadED

The HcBulkHeadED register contains the physical address of the first Endpoint Descriptor of the Bulk list.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BHED[31:24]								BHED[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BHED[15:8]								BHED[7:4]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 4	BHED	RW	R	H'000 0000	BulkHeadED The host controller traverses the Bulk list starting with the HcBulkHeadED pointer. The content is loaded from HCCA during the initialization of the host controller.
3 to 0	—	R	R	All 0	Reserved

41.3.1.12 HcBulkCurrentED Register (offset: H'02C)

Register symbol: HcBulkCurrentED

The HcBulkCurrentED register contains the physical address of the current endpoint of the Bulk list.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	BCED[31:24]								BCED[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BCED[15:8]								BCED[7:4]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 4	BCED	RW	RW	H'000 0000	BulkCurrentED This is advanced to the next ED after the host controller has served the present one. The host controller continues processing the list from where it left off in the last Frame. When it reaches the end of the Bulk list, the host controller checks the ControlListFilled of HcControl. If set, it copies the content of HcBulkHeadED to HcBulkCurrentED and clears the bit. If it is not set, it does nothing. Software is only allowed to modify this register when the BulkListEnable of HcControl is cleared. When set, software only reads the instantaneous value of this register. This is initially set to zero to indicate the end of the Bulk list.
3 to 0	—	R	R	All 0	Reserved

41.3.1.13 HcDoneHead Register (offset: H'030)

Register symbol: HcDoneHead

The HcDoneHead register contains the physical address of the last completed Transfer Descriptor that was added to the Done queue. In normal operation, software is not required to read this register as its content is periodically written to the HCCA.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	DH[31:24]								DH[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DH[15:8]								DH[7:4]				—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 4	DH	R	RW	H'000 0000	DoneHead When a TD is completed, the host controller writes the content of HcDoneHead to the NextTD field of the TD. The host controller then overwrites the content of HcDoneHead with the address of this TD. This is set to zero whenever the host controller writes the content of this register to HCCA. It also sets the WritebackDoneHead of HcInterruptStatus.
3 to 0	—	R	R	All 0	Reserved

41.3.1.14 HcFmInterval Register (offset: H'034)

Register symbol: HcFmInterval

The HcFmInterval register contains a 14-bit value which indicates the bit time interval in a Frame, (i.e., between two consecutive SOFs), and a 15-bit value indicating the Full Speed maximum packet size that the host controller may transmit or receive without causing scheduling overrun. Software can carry out minor adjustment on the FrameInterval by writing a new value over the present one at each SOF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FIT	FSMPS[30:24]							FSMPS[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FI[13:8]						FI[7:0]							
Initial value:	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31	FIT	RW	R	0	FrameIntervalToggle Software writes the toggled value to this bit whenever it writes a new value to FI field. The value in this bit is also loaded to FRT bit in HcFmRemaining register whenever the value in FI field is loaded to FR field of the same register. Software can confirm that the value in FI field is loaded to FR field in HcFmReamining register by seeing the toggled value in FRT field in the same register.
30 to 16	FSMPS	RW	R	H'0000	FSLargestDataPacket The field specifies the largest amount of data in bits which can be sent or received by the HC in a single transaction at any given time without causing scheduling overrun. The host controller decides whether it can still continue the transfer by comparing the current position in frame with the value in this field. Software calculates the value and set it to this field.
15, 14	—	R	R	All 0	Reserved
13 to 0	FI	RW	R	H'2EDF	FrameInterval This specifies the interval between two consecutive SOFs in bit times for full speed mode of USB. Use with the value “H'2EDF” (= 11,999) to satisfy 1 ms length of frame.

41.3.1.15 HcFmRemaining Register (offset: H'038)

Register symbol: HcFmRemaining

The HcFmRemaining register is a 14-bit down counter showing the bit time remaining in the current Frame.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	FRT	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	FR[13:8]						FR[7:0]							
Initial value:	0	0	1	0	1	1	1	0	1	1	0	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31	FRT	R	RW	0	FrameRemainingToggle When FR field reaches 0, the value in FI field in HcFmInterval register is loaded to FR field. At the same time, the value in FIT bit in HcFmInterval register is loaded to this bit. Software can use this bit to confirm that the value in FI field in HcFmInterval register is exactly copied to FR field.
30 to 14	—	R	R	All 0	Reserved
13 to 0	FR	R	RW	H'2EDF	FrameRemaining This counter is decremented at each bit time. When it reaches 0, the value in FI field in HcFmInterval register is loaded to it at the next bit time boundary. When entering USB Operational state, the host controller re-loads the value in FI field in HcFmInterval register and uses the updated value from the next SOF.

41.3.1.16 HcFmNumber Register (offset: H'03C)

Register symbol: HcFmNumber

The HcFmNumber register is a 16-bit counter. It provides a timing reference among events happening in the host controller and software.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	FN[15:8]								FN[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 16	—	R	R	All 0	Reserved
15 to 0	FN	R	RW	H'0000	FrameNumber This field is incremented when HcFmRemaining register is re-loaded. It will be rolled over to H'0 after H'FFFF. When entering the USB Operational state, this will be incremented automatically. The content will be written to HCCA after the host controller has incremented the FrameNumber at each frame boundary and sent a SOF but before the host controller reads the first ED in that Frame. After writing to HCCA, the host controller will set SF bit in HcInterruptStatus register.

41.3.1.17 HcPeriodicStart Register (offset: H'040)

Register symbol: HcPeriodicStart

The HcPeriodicStart register has a 14-bit programmable value which determines when is the earliest time the host controller should start processing the periodic list.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	PS[13:8]						PS[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 14	—	R	R	All 0	Reserved
13 to 0	PS	RW	R	H'0000	PeriodicStart This field specifies when host controller starts processing the periodic list. Software calculates the adequate value and set it to this filed during initialization. The value is calculated roughly as 10% off from FI field in HcFmInterval register. When FR field in HcFmRemaining register reaches the value specified, processing of the periodic lists has priority over Control/Bulk processing. Therefore the host controller starts processing the Interrupt list after completing the current Control or Bulk transaction that is in progress.

41.3.1.18 HcLSThreshold Register (offset: H'044)

Register symbol: HcLSThreshold

The HcLSThreshold register contains an 11-bit value used by the host controller to determine whether to commit to the transfer of a maximum of 8-byte LS packet before EOF. Neither the host controller nor software is allowed to change this value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LST[11:8]				LST[7:0]							
Initial value:	0	0	0	0	0	1	1	0	0	0	1	0	1	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 12	—	R	R	All 0	Reserved
11 to 0	LST	RW	R	H'0628	LSThreshold This field specifies the threshold to decide whether the transfer can be still continued in the remaining time of the current frame for LS transfer. Only when the value in FR field of HcFrameRemaining register is larger than that in this field, the host controller can start LS transfer.

41.3.1.19 HcRhDescriptorA Register (offset: H'048)

Register symbol: HcRhDescriptorA

The HcRhDescriptorA register is the first register of two describing the characteristics of the Root Hub.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	POTPGT								—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	1	1	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	NOCP	OCPM	DT	NPS	PSM	NDP							
Initial value:	0	0	0	0	1	0	0	1	0	0	0	0	0	0	0	1
R/W:	R	R	R	R/W	R/W	R	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 24	POTPGT	RW	R	H'0F	PowerOnToPowerGoodTime This byte specifies the duration the host controller has to wait before accessing a powered-on port of the Root Hub. The unit of time is 2 ms. The duration is calculated as POTPGT * 2 ms.
23 to 13	—	R	R	All 0	Reserved
12	NOCP	RW	R	0	NoOverCurrentProtection This bit defines how the overcurrent status for the Root Hub ports is reported. When this bit is cleared, OCPM bit specifies global or per-port reporting. 0: Over-current status is reported collectively for all downstream ports 1: No overcurrent protection supported
11	OCPM	RW	R	1	OverCurrentProtectionMode This bit defines how the overcurrent status for the Root Hub ports is reported. This bit shows the same mode as PSM bit when it is reset. This bit is valid only if NOCP bit is cleared. 0: over-current status is reported collectively for all downstream ports. 1: over-current status is reported on a per-port basis.
10	DT	R	R	0	DeviceType This bit is always 0 in order to show that the root hub is not a compound device.
9	NPS	RW	R	0	NoPowerSwitching This bit is used to specify whether power switching is supported or port is always powered. When this bit is cleared, PSM bit specifies global or per-port switching. 0: Ports are power switched 1: Ports are always powered on when the HC is powered on

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
8	PSM	RW	R	1	PowerSwitchingMode This bit is used to specify how the power switching of the Root Hub ports is controlled. This bit is only valid if the NPS bit is cleared. 0: all ports are powered at the same time. 1: each port is powered individually. This mode allows port power to be controlled by either the global switch or per-port switching. If the PPCM bit in HcRhDescriptorB register is set, the port responds only to port power commands (Set/ClearPortPower). If the port mask is cleared, then the port is controlled only by the global power switch (Set/ClearGlobalPower).
7 to 0	NDP	R	R	H'01	NumberDownstreamPorts This field specifies the number of downstream ports supported by the Root Hub. The value in this field depends on the configuration of this host controller core.

41.3.1.20 HcRhDescriptorB Register (offset: H'04C)

Register symbol: HcRhDescriptorB

The HcRhDescriptorB register is the second register of two describing the characteristics of the Root Hub.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PPCM[15:8]								PPCM[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DR[15:8]								DR[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 16	PPCM	RW	R	H'0002	PortPowerControlMask Each bit indicates if a port is affected by a global power control command when PSM bit in HcRhDescriptorA register is set. When set, the port's power state is only affected by per-port power control (Set/ClearPortPower). When cleared, the port is controlled by the global power switch (Set/ClearGlobalPower). If the device is configured to global switching mode (PSM bit = 0), this field is not valid. bit 0: Reserved bit 1: Ganged-power mask on Port #1 bit 2: Ganged-power mask on Port #2
15 to 0	DR	RW	R	H'0000	DeviceRemovable Each bit is dedicated to a port of the Root Hub. When cleared, the attached device is removable. When set, the attached device is not removable. bit 0: Reserved bit 1: Device attached to Port #1 bit 2: Device attached to Port #2

41.3.1.21 HcRhStatus Register (offset: H'050)

Register symbol: HcRhStatus

The HcRhStatus register is divided into two parts. The lower word of this dword represents the Hub Status field and the upper word represents the Hub Status Change field. Reserved bits should always be written 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCIC	LPSC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	W	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	DRWE	—	—	—	—	—	—	—	—	—	—	—	—	—	OCI	LPS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31	CRWE	W	R	0	ClearRemoteWakeupEnable Writing 1 clears DRWE bit. Writing 0 has no effect.
30 to 18	—	R	R	All 0	Reserved
17	OCIC	RW	RW	0	OverCurrentIndicatorChange This bit is set by hardware when a change has occurred to the OCI bit. Writing 1 clears this bit when it is set. Writing 0 has no effect. 0: No change has occurred in over-current status. 1: A change has occurred in over-current status.
16	LPSC	RW	R	0	This bit has different meanings for read and write. (read) LocalPowerStatusChange This bit always returns 0 for read, since the Root Hub does not support the local power status feature. (write) SetGlobalPower In global power mode (PSM bit = 0 in HcRhDescriptorA register), this bit is written to 1 in order to turn on power to all ports (PPS bit in HcRhPortStatus[N] register is cleared). In per-port power mode, it sets PPS bit in HcRhPortStatus[N] register only on port whose PPCM bit in HcRhDescriptorB register is not set. Writing 0 has no effect.

written to this bit	PSM	PPCM[N]	description
0	—	—	no effect
1	0	—	PPS bit is set
	1	0	PPS bit is set
		1	no effect

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
15	DRWE	RW	R	0	(read) DeviceRemoteWakeupEnable This bit enables a CCS bit in HcRhPortStatus[N] register as a resume event, causing the transition from USB Suspend state to USB Resume state and setting the ResumeDetected interrupt. 0: CCS bit does not show a remote wakeup event. 1: CCS bit shows a remote wakeup event. (write) SetRemoteWakeupEnable Writing 1 sets this bit. Writing 0 has no effect.
14 to 2	—	R	R	All 0	Reserved
1	OCI	R	R	0	OverCurrentIndicator This bit reports overcurrent conditions when the global reporting is implemented. When set, an overcurrent condition exists. When cleared, all power operations are normal. If per-port overcurrent protection is implemented this bit is always ‘0’ 0: all power operations are normal 1: an overcurrent condition exists.
0	LPS	RW	RW	0	This bit has different meanings for read and write. (read) LocalPowerStatus This bit always returns 0 for read, since the Root Hub does not support the local power status feature. (write) ClearGlobalPower In global power mode (PSM bit = 0 in HcRhDescriptorA register), this bit is written to 1 in order to turn off power to all ports (PPS bit in HcRhPortStatus[N] register is cleared). In per-port power mode, it clears PPS bit in HcRhPortStatus[N] register only on port whose PPCM bit in HcRhDescriptorB register is not set. Writing 0 has no effect.

written to this bit	PSM	PPCM[N]	description
0	—	—	no effect
1	0	—	PPS bit is set
	1	0	PPS bit is set
		1	no effect

41.3.1.22 HcRhPortStatus[1] Register (offset: H'054)

Register symbol: HcRhPortStatus1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	PRSC	OCIC	PSSC	PESC	CSC
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	LSDA	PPS	—	—	—	PRS	POCI	PSS	PES	CCS
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 21	—	R	R	All 0	Reserved
20	PRSC	RW	RW	0	PortResetStatusChange This bit shows the port reset has been completed. This bit is set at the end of the 10-ms port reset signal. Writing 1 clears this bit. Writing 0 has no effect. 0: port reset has not been completed. 1: port reset has been completed
19	OCIC	RW	RW	0	PortOverCurrentIndicatorChange This bit shows that overcurrent condition has been detected, and is set when the host controller changes POCI bit. This bit is valid only if overcurrent conditions are reported on a per-port basis. Writing 1 clears this bit. Writing 0 has no effect. 0: no change has occurred in POCI bit. 1: change has occurred in POCI bit.
18	PSSC	RW	RW	0	PortSuspendStatusChange This bit is set when the full resume sequence has been completed. This sequence includes the 20-s resume pulse, LS EOP, and 3-ms resynchronization delay. Writing 1 clears this bit. Writing 0 has no effect. This bit is also cleared when PRSC bit is set. 0: resume sequence has not been completed. 1: resume sequence has been completed.
17	PESC	RW	RW	0	PortEnableStatusChange This bit is set when hardware events cause PES bit to be cleared. Writing 1 clears this bit. Writing 0 has no effect. 0: no change has occurred in PES bit 1: change has occurred in PES bit

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
16	CSC	RW	RW	0	ConnectStatusChange This bit is set whenever connect or disconnect event occurs. Writing 1 means to clear this bit. Writing 0 has no effect. If CCS bit is cleared and writing to SetPortReset, SetPortEnable, or SetPortSuspend occurs, this bit is set to force the driver to re-evaluate the connection status since these write should not occur if the port is disconnected. 0: no change has occurred in CCS bit 1: change has occurred in CCS bit
15 to 10	—	R	R	All 0	Reserved
9	LSDA	RW	RW	0	This bit has different meanings for read and write. (read) LowSpeedDeviceAttached This bit indicates the speed of the device attached to this port. When set, a Low Speed device is attached to this port. When cleared, a Full Speed device is attached to this port. This field is valid only when the CCS bit is set (which means device is connected). 0: full speed device attached 1: low speed device attached (write) ClearPortPower Writing 1 clears PPS bit. Writing 0 has no effect.
8	PPS	RW	RW	0	This bit has different meanings for read and write. (read) PortPowerStatus This bit reflects the port's power status. This bit is cleared if an overcurrent condition is detected. 0: port power is off. 1: port power is on. (write) SetPortPower Writing 1 sets PPS bit. Writing 0 has no effect. The HCD writes a 1 to set the PortPowerStatus bit. Writing 0 has no effect.
7 to 5	—	R	R	All 0	Reserved

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
4	PRS	RW	RW	0	This bit has different meanings for read and write. (read) PortResetStatus When this bit is set by writing to SetPortReset, port reset signaling is asserted. When reset is completed, this bit is cleared when PRSC bit is set. This bit cannot be set if CCS bit is cleared (which means no device is connected) 0: port reset signal is not active 1: port reset signal is active (write) SetPortReset Writing 1 asserts the port reset signaling. Writing 0 has no effect. When CCS bit is cleared (which means no device is connected), PRS bit is not set even with writing 1. But it causes CSC bit to be set instead. This informs that a disconnected port is attempted to be reset.
3	POCI	RW	RW	0	This bit has different meanings for read and write. (read) PortOverCurrentIndicator This bit is only valid when the host controller is configured in such a way that overcurrent conditions are reported on a per-port basis. If per-port overcurrent reporting is disabled, this bit always returns 0 for read. If cleared, all power operations are normal for this port. If set, an overcurrent condition exists on this port. 0: no overcurrent condition exists 1: overcurrent condition exists. (write) ClearSuspendStatus Writing 1 initiates the resume sequence. Writing 0 has no effect. A resume is initiated only if PSS bit is set.
2	PSS	RW	RW	0	This bit has different meanings for read and write. (read) PortSuspendStatus This bit indicates the port is suspended or in the resume sequence. This bit cannot be set when CCS bit is cleared (which means no device is connected). This bit is cleared with following conditions. The resume sequence is completed and PSSC bit is set. The port reset is completed and PRSC bit asset. The host controller is placed in USB Resume state. 0: Port is not suspended. 1: Port is suspended. (write) SetPortSuspend Writing 1 sets PSS bit. Writing 0 has no effect. When CCS bit is cleared (which means no device is connected), PSS bit is not set even with writing 1. But it causes CSC bit to be set instead. This informs that a disconnected port is attempted to be suspended.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
1	PES	RW	RW	0	This bit has different meanings for read and write. (read) PortEnableStatus This bit indicates whether the port is enabled or disabled. This host controller core clears this bit in case of an overcurrent condition, disconnect event, switched-off power, or operational bus error such as babble is detected. This change also sets PESC bit. This bit cannot be set when CCS bit is cleared (which means no device is connected). This bit is also set when port reset is completed and PRSC bit is set or when port is suspended and PSSC bit is set. 0: Port is disabled 1: Port is enabled. (write) SetPortEnable Writing 1 sets PES bit. Writing 0 has no effect. If CCS bit is cleared, this write does not set PES bit, but instead sets CSC bit. This informs the driver that it attempted to enable a disconnected port.
0	CCS	RW	RW	0	This bit has different meanings for read and write. (read) CurrentConnectStatus This bit reflects the current state of the downstream port. 0: no device is connected 1: device is connected (write) ClearPortEnable Writing 1 to this bit clears PES bit. Writing 0 has no effect.

41.3.2 EHCI Controller Capability Registers

41.3.2.1 HCIVERSION/CAPLENGTH Register (offset: H'102/H'100)

Register symbol: CAPL_VERSION

This register is used as an offset to add to register base to find the beginning of the operational register space.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Interface Version Number[15:8]								Interface Version Number[7:0]							
Initial value:	0	0	0	0	0	0	0	1	0	0	0	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Capability Registers Length[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 16	Interface Version Number	R	R	H'0110	This field shows a BCD encoding of the EHCI revision number supported by this host controller core. This host controller core supports EHCI v.1.1.
15 to 8	—	R	R	All 0	Reserved
7 to 0	Capability Registers Length	R	R	H'20	This field is used as an offset to add to register base to find the beginning of the operational register space. This field is prepared considering the compatibility with EHCI specification. This field has the value of H'20 since the operational register starts from H'20 offset.

41.3.2.2 HCSPARAMS Register (offset: H'104)

Register symbol: HCSPARAMS

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	Debug Port Number[3:0]				—	—	—	P_INDICATOR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	N_CC				N_PCC				Port Routing Rules	—	—	PPC	N_PORTS[3:0]			
Initial value:	0	0	0	1	0	0	0	1	1	0	0	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 24	—	R	R	All 0	Reserved
23 to 20	Debug Port Number	R	R	H'0	This field always shows H'0 since this host controller core has no debug port.
19 to 17	—	R	R	All 0	Reserved
16	P_INDICATOR	R	R	0	Port Indicators (P_INDICATOR). This field always shows 0 since this host controller core does not have the function of port indicator.
15 to 12	N_CC	R	R	H'1	Number of Companion Controller This field indicates the number of companion controllers.
11 to 8	N_PCC	R	R	H'1	Number of Ports per Companion Controller (N_PCC). This field indicates the number of ports supported per companion host controller. It is used to indicate the port routing configuration to software.
7	Port Routing Rules	R	R	1	Port Routing Rules. This field indicates the method used by this implementation for how all ports are mapped to companion controllers. 0: The first N_PCC ports are routed to the lowest numbered function companion host controller, the next N_PCC port are routed to the next lowest function companion controller, and so on. 1: The port routing is explicitly enumerated by the first N_PORTS elements of the HCSP-PORTROUTE array.
6, 5	—	R	R	All 0	Reserved
4	PPC	R	R	1	Port Power Control (PPC). This field indicates whether the host controller implementation includes port power control.
3 to 0	N_PORTS	R	R	H'1	This field specifies the number of physical downstream ports implemented as host controller

41.3.2.3 HCCPARAMS Register (offset: H'108)

Register symbol: HCCPARAMS

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	32-Frame Periodic List Capability	Per-Port Change Event Capability	Link Power Management Capability	Hardware Prefetch Capability
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EECP								Isochronous Scheduling Threshold				—	Asynchronous Schedule Park Capability	USB Error Interrupt	64-bit Addressing Capability
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 20	—	R	R	All 0	Reserved
19	32-Frame Periodic List Capability	R	R	1	This bit shows 1 since this host controller has 32-Frame Periodic List Capability. When set (1) this optional field indicates the host controller supports a 32 frame periodic schedule as specified by using the value B'11 in the USBCMD *Frame List Size* field. Software must treat a *Flame List Size* values (B'01 = 512 frames, B'10 = 256 frames) continues to be indicated through the *Programmable Frame List Flag*, where this bit only indicates programmability for a 32-frame list.
18	Per-Port Change Event Capability	R	R	1	This bit shows 1 since this host controller has Per-Port Change Event Capability. When set (1) this optional field indicates host controller support for pre-port change events and associated USBCMD *Pre-Port Change Event Enable*, USBSTS *Port-n Change Detect*, and USBINT *Port-n Change Interrupt Enable* fields. Note that software should treat those fields as reserved when this bit is cleared (0).
17	Link Power Management Capability	R	R	0	This bit shows 0 since this host controller doesn't have Link Power Management Capability. When set (1) this optional field indicates host controller support for this the Link Power Management L1 state and associated PORTSC *Suspend using L1*, *Suspend Status*, and *Device Address* field. Note that software should treat those fields as reserved then this bit is cleared (0).
16	Hardware Prefetch Capability	R	R	0	This bit shows 0 since this host controller does not have Hardware Prefetch Capability. This host controller doesn’t support this function.
15 to 8	EECP	R	R	H'00	EHCI Extended Capabilities Pointer (EECP).
7 to 4	Isochronous Scheduling Threshold	R	R	H'0	This field shows 0 since this host controller core does not support the function to cache the isochronous data structure.
3	—	R	R	0	Reserved
2	Asynchronous Schedule Park Capability	R	R	1	This bit shows 1 since this host controller core has Asynchronous Schedule Park Capability.

Bit	Bit Name	R/W		Initial Value	Description
		HCD	HC		
1	Programmable Frame List Flag	R	R	1	This bit shows 1 since this host controller core supports Programmable Frame List.
0	64-bit addressing Capability	R	R	0	This field shows 0 since this host controller core does not support 64-bit addressing.

41.3.2.4 HCSP-PORTROUTE Register (offset: H'10C)

Register symbol: HCSP_PORTROUTE

This operational register is valid only if Port Routing Rules field in HCSPARAMs register.

In that case, this register shows how OHCI controller is routed to each port.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Companion Port Route[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Companion Port Route[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	R/W	Initial Value	Description
31 to 0	Companion Port Route[31:0]	R	H'0000 0000	These bits show the port controlled by the OHCI host controller. This module provides only one OHCI host controller and this bit is read as 0.

41.3.3 EHCI Operational Registers

41.3.3.1 USBCMD Register (offset: H'120)

Register symbol: USBCMD

The Command Register indicates the command to be executed by the serial bus host controller. Writing to the register causes a command to be executed.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	Host-Initiated Resume Duration				Interrupt Threshold Control							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Per-Port Change Events Enable	Full Synchro-nized Prefetch	Asynchro-nous Schedule Prefetch Enable	Periodic Schedule Prefetch Enable	Asynchro-nous Schedule Park Mode Enable	—	Asynchronous Schedule Park Mode Count		Light Host Con-troller Reset	Interrupt on Async Advance Door-bell	Asynchron ous Schedule Enable	Periodic Schedule Enable	Frame List Size		HCRES ET	RS
Initial value:	0	0	0	0	1	0	1	1	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 28	—	R	R	All 0	Reserved
27 to 24	Host-Initiated Resume Duration	RW	R	H'0	This field is used by software to specify the minimum amount of time the host controller will drive the K-state during a host-initiated resume from LPM (L1) state and is conveyed to each LPM-enabled device (via the *HIRD* bits within an LPM Token's *bmAttributes* field) upon entry into a low-power state. Encoding for this field is identical to the definition for the similarly named *HIRD* field within an LPM Token. Specifically, a value H'0 equals to 50 µs and each additional increment adds 75 µs. For example, the value H'1 equals 125 µs and H'F equals 1175 µs.
23 to 16	Interrupt Threshold Control	RW	R	H'08	This field is used by system software to select the maximum rate at which the host controller core issue interrupts. If software writes an invalid value to this field, the results are undefined. **Value — Maximum Interrupt Interval** H'00: Reserved H'01: 1 micro-frame H'02: 2 micro-frames H'04: 4 micro-frames H'08: 8 micro-frames (default, equals to 1 MS) H'10: 16 micro-frames (2 MS) H'20: 32 micro-frames (4 MS) H'40: 64 micro-frames (8 MS) Software should not set this bit to 0 while Halted bit is equal to 0.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
15	Per-Port Change Events Enable	RW	R	0	This field is used by software to enable the per-port change event capability as defined by the *Port-n Change Detect* field in the USBSTS register and *Port-n Change Detect Enable* field in the USBINTR register. When this bit is set to 1, the per-port change event is enabled. When this bit is set to 0, the per-port change event is disabled.
14	Full Synchronized Prefetch	R	R	0	Since this host controller core does not have Hardware Prefetch Capability, this bit is fixed to 0.
13	Asynchronous Schedule Prefetch Enable	R	R	0	Since this host controller core does not have Hardware Prefetch Capability, this bit is fixed to 0.
12	Periodic Schedule Prefetch Enable	R	R	0	Since this host controller core does not have Hardware Prefetch Capability, this bit is fixed to 0.
11	Asynchronous Schedule Park Mode Enable	RW	R	1	Software uses to enable or disable Asynchronous Schedule Park Mode. When this bit is set to 1, Park mode is enabled. When this bit is set to 0, Park mode is disabled.
10	—	R	R	0	Reserved
9:8	Asynchronous Schedule Park Mode Count	RW	R	11	This field defines a count of the number of successive transactions the host controller core is allowed to execute from a high-speed queue head on the Asynchronous schedule before continuing traversal of the Asynchronous schedule. This function is enabled when Asynchronous Schedule Park Mode Enable is set to 1. Software should not write 0 to this bit.
7	Light Host Controller Reset	R	R	0	Since this host controller core does not support the function of Light Host Controller Reset, this bit is fixed to 0.
6	Interrupt on Async Advance Doorbell	RW	RW	0	This bit is used as a doorbell by software to tell the host controller to issue an interrupt the next time it advances asynchronous schedule. Software must write 1 to this bit to ring the doorbell. When the host controller has evicted all appropriate cached schedule state, it sets the Interrupt on Async Advance status bit in the USBSTS register. If the Interrupt on Async Advance Enable bit in the USBINTR register is 1 then the host controller will assert an interrupt at the next interrupt threshold. The host controller sets this bit to 0 after it has set the Interrupt on Async Advance status bit in the USBSTS register to 1. Software should not write 1 to this bit when the asynchronous schedule is disabled.
5	Asynchronous Schedule Enable	RW	R	0	This bit controls whether the host controller skips processing the Asynchronous Schedule. 0: Do not process the Asynchronous Schedule 1: Use the ASYNCLISTADDR register to access the Asynchronous Schedule.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
4	Periodic Schedule Enable	RW	R	0	This bit controls whether the host controller skips processing the Periodic Schedule. 0: Do not process the Periodic Schedule 1: Use the PERIODICLISTBASE register to access the Periodic Schedule.
3, 2	Frame List Size	RW	R	00	This field specifies the size of the frame list. The size the frame list and controls which bits in the Frame Index Register should be used for the Frame List Current index. This host controller core has 32-Frame Periodic List Capability. Value the number of frames in Frame List 00: 1024 frames (default) 01: 512 frames 10: 256 frames 11: 32 frames
1	HCRESET	RW	RW	0	Host Controller Reset (HCRESET). This control bit is used by software to reset the host controller. When software writes 1 to this bit, the Host Controller resets its internal pipelines, timers, counters, state machines, etc. to their initial value. Any transaction currently in progress on USB is immediately terminated. A USB reset is not driven on downstream ports. Registers other than the EHCI Operational registers are not affected by this reset. All operational registers, including port registers and port state machines are set to their initial values. Port ownership reverts to the companion host controller(s). Software must reinitialize the host controller in order to return the host controller to an operational state. This bit is set to 0 by the Host Controller when the reset process is complete. Software cannot terminate the reset process early by writing 0 to this register. Software should not set this bit to 1 when the HCHalted bit in the USBSTS register is 0.
0	RS	RW	RW	0	Run/Stop (RS). When this bit is set to 1, the host controller proceeds with execution of the schedule. The host controller continues execution as long as this bit is set to 1. When this bit is set to 0, the host controller completes the current and any actively pipelined transactions on the USB and then halts. The HCHalted bit in the status register indicates when the host controller has finished its pending pipelined transactions and has entered the stopped state. Software should not write 1 to this field unless the host controller is in the Halted state (i.e. HCHalted in the USBSTS register is 1).

41.3.3.2 USBSTS Register (offset: H'124)

Register symbol: USBSTS

This register indicates pending interrupts and various states of the host controller. The status resulting from a transaction on the serial bus is not indicated in this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port-n Change Detect[15:8]								Port-n Change Detect[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Asynchro-nous Schedule Status	Periodic Schedule Status	Reclama tion	HCHalte d	—	—	—	—	—	—	Interrupt on Async Advance	Host System Error	Frame List Rollover	Port Change Detect	USBERR INT	USBINT
Initial value:	0	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 16	Port-n Change Detect	RW	RW	H'0000	The definition of each bit is identical to the *Port Change Detect* field (bit 2 of this register) except these bits are specific to a given port, where bit 16 = Port 1, 17 = Port 2, etc. For example, if bit 17 is set to 1 then a port change event was detected on Port 2, the N_PORTS field in HCSPARAMS specifies how many ports are exposed by the host controller and thus how many bits in this field are valid. The behavior of the *Port Change Detect* and related fields even when Per-Port Change Events are enabled. This field is only used by software when the *Per-Port Change Events Enable* bit within the USBCMD register is set to 1.
15	Asynchronous Schedule Status	R	RW	0	This bit reports the current real status of the Asynchronous Schedule. If this bit is 0 then the status of the Asynchronous Schedule is disabled. If this bit is 1 then the status of the Asynchronous Schedule is enabled. When this bit and the Asynchronous Schedule Enable bit are the same value, the Asynchronous Schedule is either enabled (1) or disabled (0).
14	Periodic Schedule Status	R	RW	0	This bit reports the current real status of the Periodic Schedule. If this bit is 0 then the status of the Periodic Schedule is disabled. If this bit is 1 then the status of the Periodic Schedule is enabled. When this bit and the Periodic Schedule Enable bit are the same value, the Periodic Schedule is either enabled (1) or disabled (0).
13	Reclamation	R	RW	0	This is a read-only status bit, which is used to detect an empty asynchronous schedule. When this bit is 1, asynchronous schedule is empty.
12	HCHalted	R	RW	1	This bit is 0 whenever the Run/Stop bit is 1. The host controller sets this bit to 1 after it has stopped executing as a result of the Run/Stop bit being set to 0, either by software or by the host controller hardware (e.g. internal error).

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
11 to 6	—	R	RW	All 0	Reserved
5	Interrupt on Async Advance	RW	RW	0	System software can force the host controller to issue an interrupt the next time the host controller advances the asynchronous schedule by writing 1 to the Interrupt on Async Advance Doorbell bit in the USBCMD register. This status bit indicates the assertion of that interrupt source. This bit is cleared to 0 by writing 1 to it. Writing 0 occurs no effect.
4	Host System Error	RW	RW	0	The host controller sets this bit to 1 when a serious error occurs. When this error occurs, the host controller clears the Run/Stop bit in the Command register to prevent further execution of the scheduled TDs. This bit is cleared to 0 by writing 1 to it. Writing 0 occurs no effect.
3	Frame List Rollover	RW	RW	0	The host controller sets this bit to 1 when a frame list rollover event occurs. The exact *Frame List Index* value at which the rollover occurs depends on the frame list size, nothing this generally occurs when FRINDEX rolls over from its maximum value to 0. For example, if the frame list size (as programmed in the *Frame List Size* field of the USBCMD register) is 1024 then a frame list rollover would occur every time FRINDEX[13] toggles. Similarly, a frame list rollover event would occur every time FRINDEX[12] toggles for a 512 frame list, and when FRINDEX[11] toggles for a 256 frame list. Note this behavior is different for a 32 frame list where a rollover event occurs every time FRINDEX[13] toggles (same as 1024). This bit is cleared to 0 by writing 1 to it. Writing 0 occurs no effect.
2	Port Change Detect	RW	RW	0	The host controller sets this bit to 1 when it detects any change of port status. The detailed conditions those set this bit to 1 are as follows. The connection or disconnection of device is detected and Connect Status Change bit (bit 1) of PORTSC[n] register is changed from 0 to 1. The enabled status of port is detected and Port Enable/Disable bit (bit 3) of PORTSC[n] register is changed from 0 to 1. The over current is detected and Over-current Change bit (bit 5) of PORTSC[n] register is changed from 0 to 1. J-K transition is detected on the suspended port and Force Port Resume bit (bit 6) of PORTSC[n] register is changed from 0 to 1. This bit is cleared to 0 by writing 1 to it. Writing 0 occurs no effect.
1	USBERRINT	RW	RW	0	USB Error Interrupt (USBERRINT). The host controller sets this bit to 1 when completion of a USB transaction results in an error condition. If the TD on which the error interrupt occurred also had its IOC bit set, both this bit and USBINT bit are set. This bit is cleared to 0 by writing 1 to it. Writing 0 occurs no effect.

Bit	Bit Name	R/W		Initial Value	Description
		HCD	HC		
0	USBINT	RW	RW	0	USB Interrupt (USBINT). The host controller sets this bit to 1 on the completion of a USB transaction, which results in the retirement of a Transfer Descriptor that had its IOC bit set. The host controller also sets this bit to 1 when a short packet is detected (actual number of bytes received was less than the expected number of bytes). This bit is cleared to 0 by writing 1 to it. Writing 0 occurs no effect.

41.3.3.3 USBINTR Register (offset: H'128)

Register symbol: USBINTR

This register enables and disables reporting of the corresponding interrupt to the software. When a bit is set and the corresponding interrupt is active, an interrupt is generated to the host. Interrupt sources that are disabled in this register still appear in the USBSTS to allow the software to poll for events.

Each interrupt enable bit description indicates whether it is dependent on the interrupt threshold mechanism.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Port-n Change Event Enable[15:8]								Port-n Change Event Enable[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	Interrupt on Async Advance Enable	Host System Error Enable	Frame List Rollover Enable	Port Change Detect Enable	USB Error Interrupt Enable	USB Interrupt Enable
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 16	Port-n Change Event Enable	RW	R	H'0000	The definition for each bit in this field is identical to bit 2 of this register (Port Change Interrupt Enable bit) except these bits are specific to a given port, where bit 16 = Port 1, 17 = Port 2, etc. For example, if bit 17 is set to 1 then a port change event was detected on Port 2. When a bit in this field is 1 and the corresponding Port-n Change Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the *Port-n Change Detect* bit.
15 to 6	—	R	R	All 0	Reserved
5	Interrupt on Async Advance Enable	RW	R	0	When this bit is a one, and the Interrupt on Async Advance bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the Interrupt on Async Advance bit.
4	Host System Error Enable	RW	R	0	When this bit is 1, and the Host System Error Status bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Host System Error bit.
3	Frame List Rollover Enable	RW	R	0	When this bit is 1, and the Frame List Rollover bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Frame List Rollover bit.
2	Port Change Detect Enable	RW	R	0	When this bit is 1, and the Port Change Detect bit in the USBSTS register is 1, the host controller will issue an interrupt. The interrupt is acknowledged by software clearing the Port Change Detect bit.
1	USB Error Interrupt Enable	RW	R	0	When this bit is 1, and the USBERRINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBERRINT bit.

Bit	Bit Name	R/W		Initial Value	Description
		HCD	HC		
0	USB Interrupt Enable	RW	R	0	When this bit is 1, and the USBINT bit in the USBSTS register is 1, the host controller will issue an interrupt at the next interrupt threshold. The interrupt is acknowledged by software clearing the USBINT bit.

41.3.3.4 FRINDEX Register (offset: H'12C)

Register symbol: FRINDEX

This register is used by the host controller to index into the periodic frame list. The register updates every 125 microseconds (once each micro-frame). Bits [N:3] are used to select a particular entry in the Periodic Frame List during periodic schedule execution. The number of bits used for the index depends on the size of the frame list as set by system software in the Frame List Size field in the USBCMD register

This register can't be written unless the host controller is in the Halted state as indicated by HCHalted bit of USBSTS register. It is not allowed to write to this register while the Run/Stop bit is 1 either.

The host controller behaves slightly different when using a 32-frame Frame List Size, specifically it continues to count FRINDEX up to a full 1024 frames, transmit SOF values from 0 to 2047, and generate Frame List Rollover events (when enabled) every 1024 frames - exactly as if a 1024 frame list size was employed. The host controller will only reference 32 elements on the periodic schedule, however. This is accomplished by formulating the Periodic Frame List Element Address using {FRINDEX[N:3] modulo 32} rather than FRINDEX[N:3]. The same mapping should be done by system software whenever it needs to correlate the current FRINDEX value to a specific periodic schedule element. Note this new behavior only applies to a 32-frame list.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	Frame Index[13:8]						Frame Index[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 14	—	R	R	All 0	Reserved
13 to 0	Frame Index[13:0]	RW	RW	H'0000	The value in this register increments at the end of each time frame (e.g. micro-frame). Bits [N:3] are used for the Frame List current index. This means that each location of the frame list is accessed 8 times (frames or micro-frames) before moving to the next index. The following illustrates values of N based on the value of the Frame List Size field in the USBCMD register. **Frame List Size / Number of Frames / N** B'00 / 1024 / 12 B'01 / 512 / 11 B'10 / 256 / 10 B'11 / 32 / 12

41.3.3.5 CTRLDSSEGMENT Register (offset: H'130)

Register symbol: CTRLDSSEGMENT

Since this host controller does not have the 64-bit Addressing Capability and the 64-bit Addressing Capability bit in HCCPARAMS is 0, CTRLDSSEGMENT register is not used and fixed to H'00 0000.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	CTRLDS-SEGMENT[31:24]								CTRLDS-SEGMENT[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CTRLDS-SEGMENT[15:8]								CTRLDS-SEGMENT[7:0]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

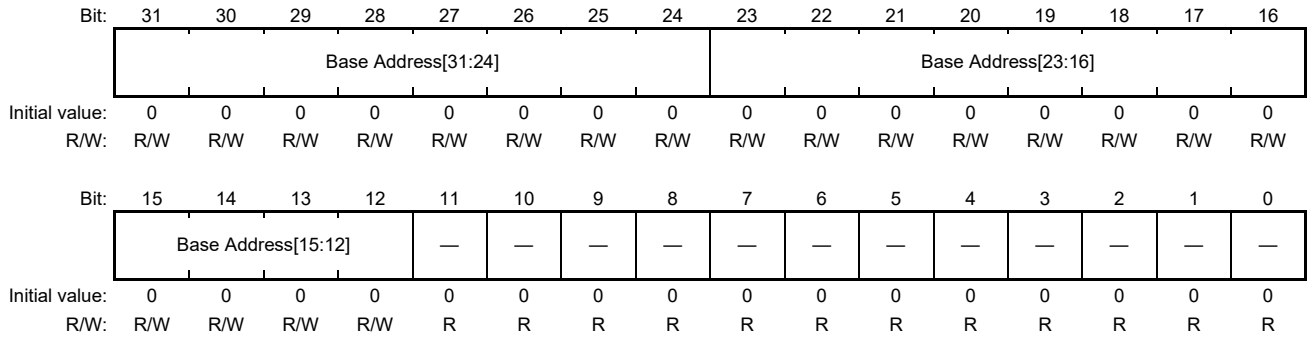
		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 0	CTRLDS-SEGMENT	R	R	H'0000 0000	This host controller does not support 64-bit addressing.

41.3.3.6 PERIODICLISTBASE Register (offset: H'134)

Register symbol: PERIODICLISTBASE

This register contains the beginning address of the Periodic Frame List in the system memory.

Software loads this register prior to starting the schedule execution by the host controller. The memory structure referenced by this physical memory pointer is assumed to be 4-Kbyte aligned. The contents of this register are combined with the Frame Index Register (FRINDEX) to enable the Host Controller to step through the Periodic Frame List in sequence.



Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 12	Base Address	RW	R	H'0 0000	This field defines the beginning address of the Periodic Frame List in the system memory. The pointer contained in this field should be 4-Kbyte aligned.
11 to 0	—	R	R	All 0	Reserved

41.3.3.7 ASYNCLISTADDR Register (offset: H'138)

Register symbol: ASYNCLISTADDR

This register contains the address of the next asynchronous queue head to be executed.

Bits [4:0] of this register cannot be modified by software and will always return H'00 when read. The memory structure referenced by this physical memory pointer is assumed to be 32-byte (cache line) aligned.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	LPL[31:24]								LPL[23:16]							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	LPL[15:8]								LPL[7:5]			—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 5	LPL	RW	RW	H'000 0000	Link Pointer Low (LPL). This field defines the address of the next asynchronous queue head to be executed. The pointer contained in this field should be 32-byte aligned.
4 to 0	—	R	R	All 0	Reserved

41.3.3.8 CONFIGFLAG Register (offset: H'160)

Register symbol: CONFIGFLAG

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CF
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

		R/W			
Bit	**Bit Name**	**HCD**	**HC**	**Initial Value**	**Description**
31 to 1	—	R	R	All 0	Reserved This field defines the address of the next asynchronous queue head to be executed. The pointer contained in this field should be 32-byte aligned.
0	CF	RW	R	0	Configuration Flag (CF). Software sets this bit as the last action in its process of configuring the host controller. This bit controls the default port-routing control logic. Bit values and side-effects are listed below. 0: Port routing control logic default-routes each port to OHCI host controller. 1: Port routing control logic default-routes all ports to this (EHCI) host controller.

41.3.3.9 PORTSC[1] Register (offset: H'164)

Register symbol: PORTSC1

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	Device Address							Suspend Status		WKOC_E	WKDSCNNT_E	WKCNNT_E	Port Test Control			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	Port Indicator Control		Port Owner	PP	Line Status		Suspend using L1	Port Reset	Suspend	Force Port Resume	Over-current Active Change	Over-current Active	Port Enabled/ Disabled Change	Port Enabled/ Disabled	Connect Status Change	Current Connect Status
Initial value:	0	0	1	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
31 to 25	Device Address	RW	RW	H'00	The 7-bit USB device address for the device attached to and immediately downstream of the associated root port. A value of zero indicates no device is present or support for this feature is not present.
24, 23	Suspend Status	R	RW	00	These two bits are used by software to determine whether the most recent L1 suspend request was successful, specifically 00: Success: State transition was successful (ACK) 01: Not Yet: Device was unable to enter the L1 state at this time (NYET). 10: Not Supported: Device does not support the L1 state (STALL) 11: Timeout/Error: Device failed to respond or an error occurred This field is updated by hardware immediately following the completion of an L1 transition request (via an LPM token). To avoid any race conditions with hardware, software should only consume the contents of this field when Suspend = 0 (port no longer in L1).
22	WKOC_E	RW	RW	0	Wake on Over-current Enable. Writing 1 to this bit enables the port to detect the over-current conditions as wake-up events. Writing 0 to this bit has no effect. This bit is zero if PP bit is zero.
21	WKDSCNNT_E	RW	RW	0	Wake on Disconnect Enable. Writing 1 to this bit enables the port to detect the device disconnects as wake-up events. Writing 0 to this bit has no effect. This bit is zero if PP bit is zero.
20	WKCNNT_E	RW	RW	0	Wake on Connect Enable. Writing 1 to this bit enables the port to detect the device connects as wake-up events. Writing 0 to this bit has no effect. This field is zero if PP bit is zero.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
19 to 16	Port Test Control	RW	R	0000	Port Test Control. A non-zero value indicates that it is operating in test mode and the specific test mode is indicated by the specific value. When this field is zero, the port is NOT operating in a test mode. Value test mode 0000: Test mode not enabled 0001: Test J_STATE 0010: Test K_STATE 0011: Test SE0_NAK 0100: Test Packet 0101: Test FORCE_ENABLE Other: Reserved
15, 14	Port Indicator Control	R	R	00	This field always shows B'00 since this host controller does not support Port Indicator Control.
13	Port Owner	RW	RW	1	This bit unconditionally goes to 0 when the Configured bit in the CONFIGFLAG register makes a transition from 0 to 1. This bit unconditionally goes to 1 whenever the Configured bit is zero. Software uses this field to release ownership of the port to a selected host controller (in the event that the attached device is not a high-speed device). Software writes 1 to this bit when the attached device is not a high-speed device. 0: EHCI controller owns the port. 1: OHCI controller owns the port.
12	PP	RW	RW	0	Port Power (PP). The function of this bit depends on the value of PPC bit in HCSPARAMS register. The behavior is as follows: PPC PP Operation 0 1 RO – The host controller does not have port power control switches. Each port is hard-wired to power. 1 1/0 R/W – The host controller has port power control switches. This bit represents the current setting of the switch (0 = off, 1 = on). When power is not available on a port (i.e. PP equals to 0), the port is non-functional and will not report attaches, detaches, etc. When an over-current condition is detected on a powered port and PPC bit is 1, the PP bit in each affected port may be transitioned by the host controller from 1 to 0 (which means removing power from the port).

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
11, 10	Line Status	R	RW	00	This field reflects the current logical levels of the D+ (bit 11) and D- (bit 10) signal lines. This field is used for detection of low-speed USB devices prior to the port reset and enable sequence. This field is valid only when Port Enable/Disable bit is 0 and Current Connect Status bit is set to 1. {bit11, bit10} USB state description 00 SE0 Not LS-device, perform EHCI reset. 10 J-state Not LS-device, perform EHCI reset. 01 K-state LS-device, change ownership from EHCI to OHCI. 11 Undefined Not LS-device, perform EHCI reset. The value in this field is undefined if PP bit is 0.
9	Suspend using L1	R	R	0	0: Suspend using L2
8	Port Reset	RW	RW	0	This bit shows the reset status of the port. When software writes 1 to this bit (from a zero), the bus reset is started. Software is required to write 0 to this bit to terminate the bus reset sequence. Software should keep this bit at 1 long enough to ensure the reset sequence completes as specified in the USB Specification. Do not write 1 to this bit when HCHalted bit in USBSTS register is 0. This bit is 0 if PP bit is 0. 0: The port is not in reset. 1: The port is in reset.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
7	Suspend	RW	RW	0	P*ort Enabled* Bit and *Suspend* bit of this register define the port states as follows: {Port Enabled, Suspend} — Port Status 0x — Disable 10 — Enable 11 — Suspend Software writes a one to this bit to transition a port to either the L1 or L2 suspend state. Which suspend state the host controller attempts depends on the value of the *Suspend Using L1* field. When in suspend state, downstream propagation of data is blocked on this port, except for port reset. If this bit is set to a one when a transaction is in progress then the blocking will not occur until the end of the current transaction. In the suspend state, the port is sensitive to resume detection. Note that the status of this bit does not change until the port is fully suspended and there may be a delay in suspending a port if a transaction is currently in progress on the USB. Addition status for L1-based transitions is provided to software via the *Suspend Status* field. Software writes 1 to this bit in order to set it. Writing 0 to this bit has no effect. Software can write to this bit only when PP bit is 1 and Port Owner bit is 0 and Current Connect Status bit is 1. The host controller unconditionally sets this bit to 0 when: Software sets Force Port Resume bit to 0 (from 1). Software sets Port Reset bit to 1 (from 0). Whenever Port Power is 0 This field is 0 if PP bit is 0.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
6	Force Port Resume	RW	RW	0	This bit indicates that the resume on the port is detected. 0: No resume signaling is detected or driven on the port. 1: The resume signaling is detected or driven on the port. The host controller set this bit to 1 if a J-to-K transition is detected while the port is in the Suspend state. When this bit transitions to 1 because a J-to-K transition is detected, the *Port Change Detect* and/or *Port-n Changes Detect* bits in the USBSTS register are also set to 1. If software sets this bit to 1, the host controller must not set the *Port Change Detect* and/or *Port-n Change Detect* bits. This functionality defined for manipulating this bit depends on the value of the *Suspend* and Suspend Using L1 bits. For example, if the port is not suspended (*Suspend* and *Enabled* bits are a one) and software transitions this bit to a one, then the effects on the bus are undefined. The resume signaling (Full-speed 'K') is driven on the port as long as this bit remains a one. For legacy (L2) transitions, Software should set this bit to 0 when the appropriate amount of time has elapsed. Writing 0 (from 1) causes the port to return to high speed mode (forcing the bus below the port into a high-speed idle). This bit will remain 1 until the port has switched to the high-speed idle. The host controller must complete this transition within 2 milliseconds of software setting this bit to 0. Software does not need to time resume signaling for L1 transactions as host controller hardware will automatically enforce the necessary timing and clear this bit when the port has fully resumed. Software can influence the amount of time hardware will drive resume signaling during L1 exit via the *Host-Initiated Resume Duration* field within the USBCMD register. This bit is 0 if PP bit is 0
5	Over-current Change	RW	RW	0	This bit indicates whether Over-current Active bit has been changed or not. Writing 1 to this bit clears it. Writing 0 to this bit has no effect. 0: Over-current Active bit has not changed. 1: Over-current Active bit has changed.
4	Over-current Active	R	RW	0	This bit shows the over-current status of the port. When the host controller detects the over-current condition, it disables the port and then sets this bit to 1. The host controller automatically clears this bit when the over-current condition has been removed. 0: No over-current condition exists on the port. 1: The over-current condition exists on the port.
3	Port Enable/Disable Change	RW	RW	0	This bit indicates whether Port Enabled/Disabled bit has been changed or not. This bit is set 1 only when a port is disabled due to the appropriate conditions existing at EOF2 point. Writing 1 to this bit clears it. Writing 0 to this bit has no effect. This bit is 0 if PP bit is 0.

Bit	Bit Name	R/W HCD	R/W HC	Initial Value	Description
2	Port Enabled/ Disabled	RW	RW	0	Ports can only be enabled by the host controller as a part of the reset and enable. Software cannot enable a port by writing 1 to this field. The host controller will only set this bit to 1 the reset sequence determines that the attached device is a high-speed device. Ports can be disabled by either a fault condition (disconnect event or other fault condition) or by software. When the port is disabled (0) downstream propagation of data is blocked on this port, except for reset. When Port Test Control is B'0101, the port is always enabled and this bit is set to 1 independent of the port status. This bit is 0 if PP bit is 0. 0: The port is disabled. 1: The port is enabled.
1	Connect Status Change	RW	RW	0	This bit indicates a change has occurred in the port's Current Connect Status. The host controller sets this bit for all changes to the port device connect status, even if software has not cleared an existing connect status change. Writing 1 to this bit clears it. Writing 0 to this bit has no effect. This field is 0 if PP bit is 0.
0	Current Connect Status	R	RW	0	This bit reflects the current state of the connection of the port. The host controller sets this bit to 1 when it detects the connection of device to the port. It also sets 1 to this bit with Port Test Control = B'0101, even when device is not connected. If it detects the device is disconnected, this bit is reset to 0. This bit is 0 if PP bit is 0 or if Port Owner bit is 0. 0: No device is present. 1: Device is present.

41.3.4 AHB Bridge Registers

41.3.4.1 INT_ENABLE Register (offset: H'200)

Register symbol: INT_ENABLE

This register enables or disables interrupt generation for each interrupt source bit in the INT_STATUS register. When a bit in this register is set to disabled, the interrupt signal is not asserted even when the interrupt condition for the corresponding source is satisfied and the corresponding source bit in the INT_STATUS register is set to 1.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	WAKEON_INTEN	UCOM_INTEN	USBH_INTBEN	USBH_INTAEN	AHB_INTEN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved The write value should be 0.
4	WAKEON_INTEN	0	R/W	Enables or disables interrupt generation due to WAKEON_INT (bit 4) in INT_STATUS. 0: Disabled 1: Enabled
3	UCOM_INTEN	0	R/W	Enables or disables interrupt generation due to UCOM_INT (bit 3) in INT_STATUS. 0: Disabled 1: Enabled
2	USBH_INTBEN	0	R/W	Enables or disables interrupt generation due to USBH_INTB (bit 2) in INT_STATUS. 0: Disabled 1: Enabled
1	USBH_INTAEN	0	R/W	Enables or disables interrupt generation due to USBH_INTA (bit 1) in INT_STATUS. 0: Disabled 1: Enabled
0	AHB_INTEN	0	R/W	Enables or disables interrupt generation due to AHB_INT (bit 0) in INT_STATUS. 0: Disabled 1: Enabled

41.3.4.2 INT_STATUS Register (offset: H'204)

Register symbol: INT_STATUS

This register indicates the state of the interrupt source in the AHB bridge and the state of each signal from the OHCI, EHCI, and UCOM modules.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	WAKEON_INT	UCOM_INT	USBH_INTB	USBH_INTA	AHB_INT
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved The write value should be 0.
4	WAKEON_INT	0	R/W	This bit indicates the state of the WAKEON interrupt from the host core. Writing 1 clears this bit. 0: No WAKEON interrupt has occurred. 1: A WAKEON interrupt has occurred.
3	UCOM_INT	0	R	This bit indicates the state of the interrupt from the UCOM registers. Use the UCOM2 registers to clear the interrupt. 0: No external register interrupt has occurred. 1: An external register interrupt has occurred.
2	USBH_INTB	0	R	This bit indicates the state of the EHCI interrupt. Use the HcInterruptStatus register (an OHCI operational register) to clear the interrupt. 0: No INTB interrupt has occurred. 1: An INTB interrupt has occurred.
1	USBH_INTA	0	R	This bit indicates the state of the OHCI interrupt. Use the USBSTS register (an EHCI operational register) to clear the interrupt. 0: No INTA interrupt has occurred. 1: An INTA interrupt has occurred.
0	AHB_INT	0	R/W	This bit indicates occurrence of an AHB bus error. Writing 1 clears this bit. 0: No AHB bus error has occurred. 1: An AHB bus error has occurred.

41.3.4.3 AHB_BUS_CTR Register (offset: H'208)

Register symbol: AHB_BUS_CTR

This register specifies the AHB master and slave functions.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PROT_TYPE				—	—	—	PROT_ MODE	—	—	ALIGN_ ADDRESS		—	—	MAX_BURST_ LEN	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R/W	R	R	R/W	R/W	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The write value should be 0.
15 to 12	PROT_TYPE	0000	R/W	These bits specify the MHPROT[3:0] value for transfer from the AHB master interface. Bit [15] 0: Indicates a non-cacheable transfer. 1: Indicates a cacheable transfer. Bit [14] 0: Indicates a non-bufferable transfer. 1: Indicates a bufferable transfer. Bit [13] 0: Indicates user access. 1: Indicates privileged access. Bit [12] 0: Indicates an opcode. 1: Indicates data. For details of each bit meaning, refer to the AMBA AHB specifications
11 to 9	—	All 0	R	Reserved The write value should be 0.
8	PROT_MOD E	0	R/W	This bit selects the MHPROT[3:0] mode for transfer from the AHB master interface. 0: The PROT_TYPE value is output as MHPROT[3:0]. 1: During DMA transfer, H'0000 is output as MHPROT[3:0] in the last burst and the PROT_TYPE value is output in other burst transfers.
7, 6	—	All 0	R	Reserved The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	ALIGN_ADDRESS	00	R/W	These bits specify the address alignment for transfer from the AHB master interface. 00: Burst transfer is issued so as not to extend beyond a 1-Kbyte boundary. 01: Burst transfer is issued so as not to extend beyond a 64-byte boundary. 10: Burst transfer is issued so as not to extend beyond a 32 -byte boundary. (The maximum burst length is limited to INCR8 because transfer goes beyond a 32-byte boundary if INCR16 is specified.) 11: Burst transfer is issued so as not to extend beyond a 16-byte boundary. (The maximum burst length is limited to INCR4 because transfer goes beyond a 16-byte boundary if INCR8 or a longer length is specified.)
3, 2	—	All 0	R	Reserved The write value should be 0.
1, 0	MAX_BURST_LEN	00	R/W	These bits specify the maximum burst length for transfer from the AHB master interface. 00: INCR16 01: INCR8 10: INCR4 11: SINGLE

41.3.4.4 USBCTR Register (offset: H'20C)

Register symbol: USBCTR

This register makes settings for the host core.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

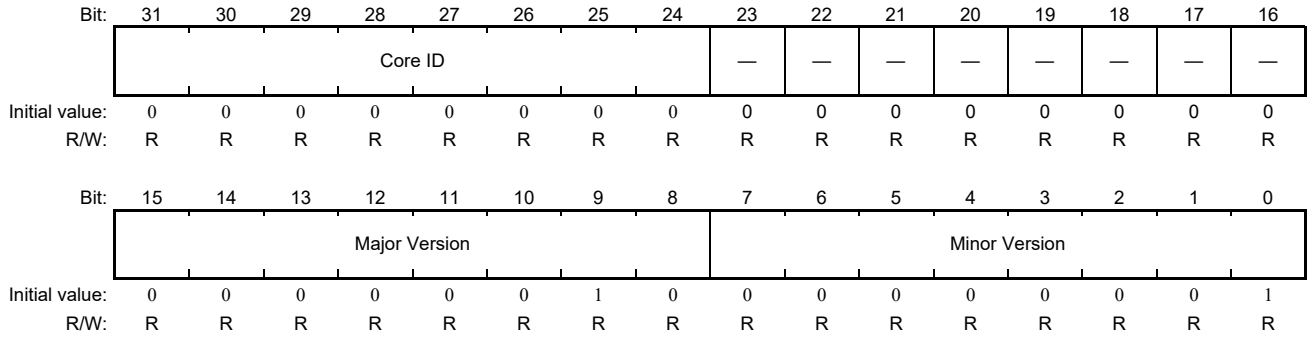
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	*Renesas Private*
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	H'0001	R	Reserved The write value should be H'0001.
0	*Renesas Private*	0	W	The write value shall be 0.

41.3.5 Core Defined Registers

41.3.5.1 REVID Register (offset: H'300)

Register symbol: REVID



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	Core ID	All 0	R	These bits indicate the ID of the host core.
23 to 16	—	All 0	R	Reserved The write value should be 0.
15 to 8	Major Version	H’02	R	These bits indicate the major version number of the host core.
7 to 0	Minor Version	H’01	R	These bits indicate the minor version number of the host core.

41.3.5.2 Register Enable/Clock Gating Control Register (offset: H'304)

Register symbol: REGEN_CG_CTRL

Some registers are read-only in the initial state.

When such registers should be written to, set the corresponding bits in this register.

In addition, the clock can be gated for the unused sections in the host and peripheral function circuits.

Set the corresponding bits as necessary.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	NONUSE_CLK_MSK	—	HOST_CLK_MSK	PERI_CLK_MSK	—	—	—	*Renesas Private*	—	—	—	—	—	—	—	*Renesas Private*
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R/W	R/W	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	*Renesas Private*
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	NONUSE_CLK_MSK	0	R/W	This bit enables masking of the clock for the unused one of the host and peripheral function circuits. 0: Not masked. 1: Masked.
30	—	0	R	Reserved The write value should be 0.
29	HOST_CLK_MSK	0	R/W	This bit forcibly masks the clock to some circuits in the host core. 0: Not masked. 1: Masked.
28	PERI_CLK_MSK	0	R/W	This bit forcibly masks the clock to some circuits in the peripheral controller. 0: Not masked. 1: Masked.
27 to 25	—	All 0	R	Reserved The write value should be 0.
24	*Renesas Private*	0	R/W	The write value shall be 0.
23 to 17	—	All 0	R	Reserved The write value should be 0.
16	*Renesas Private*	0	R/W	The write value shall be 0.
15 to 1	—	All 0	R	Reserved The write value should be 0.
0	*Renesas Private*	0	R/W	The write value shall be 0.

41.3.5.3 Suspend Control Register (offset: H'308)

Register symbol: SPD_CTRL

This register controls the SUSPENDM pin in the UTMI+ interface.

Through this register setting, SUSPENDM can be asserted when the Suspend state is entered, and UTMI+ interface SUSPENDM can be forcibly asserted.

The equivalent control is also applied to the SLEEPM pin.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SUSPENDM_ENABLE	*Renesas Private*	—	—	—	—	—	—	WKCNNT_ENABLE	*Renesas Private*	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	*Renesas Private*	*Renesas Private*	—	—	—	—	—	—	GLOBAL_SUSPENDM_P2	GLOBAL_SUSPENDM_P1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31	SUSPENDM_ENABLE	0	R/W	This bit provides a function to assert the UTMI+ interface SUSPENDM signal when the Suspend bit in the related OHCI or EHCI operational register is asserted. Setting this bit to 1 asserts the UTMI+ interface SUSPENDM signal in the target port after the Suspend-related bit in the OHCI or EHCI operational register shown below is set. This function is intended to reduce the power consumption in the UTMI+ PHY when this module enters the Suspend state. [Target OHCI and EHCI operational registers of this function] OHCI: Bit [2] (PSS bit) in the HcRhPortStatus register EHCI: Bit [7] (Suspend bit) in the PORTSC register
30	*Renesas Private*	0	R/W	The write value shall be 0.
29 to 24	—	All 0	R	Reserved The write value should be 0.
23	WKCNNT_ENABLE	0	R/W	Setting this bit to 1 deasserts SUSPENDM and SLEEPM when a change in the connection state is detected. This setting is valid when SUSPENDM_ENABLE or SLEEP_ENABLE is 1.
22	*Renesas Private*	0	R/W	The write value shall be 0.
21 to 10	—	All 0	R	Reserved The write value should be 0.
9	*Renesas Private*	0	R/W	The write value shall be 0.
8	*Renesas Private*	0	R/W	The write value shall be 0.
7 to 2	—	All 0	R	Reserved The write value should be 0.

Bit	Bit Name	Initial Value	R/W	Description
1	GLOBAL_SUSPENDM_P2	0	R/W	This bit provides a function to forcibly assert UTMI_P2SUSPENDM to 0. Setting this bit to 1 asserts the UTMI+ interface SUSPENDM pin (UTMI_P2SUSPENDM) in port 2. This function is intended to reduce the power consumption of the UTMI+ PHY by controlling this bit appropriately. [Note] Writing 1 to this bit is prohibited when the SUSPENDM_ENABLE bit is 1.
0	GLOBAL_SUSPENDM_P1	0	R/W	This bit provides a function to forcibly assert UTMI_P1SUSPENDM to 0. Setting this bit to 1 asserts the UTMI+ interface SUSPENDM pin (UTMI_P1SUSPENDM) for port 1. This function is intended to reduce the power consumption of the UTMI+ PHY by controlling this bit appropriately. [Note] Writing 1 to this bit is prohibited when the SUSPENDM_ENABLE bit is 1.

41.3.5.4 Suspend/Resume Timer Setting Register (offset: H'30C)

Register symbol: SPD_RSM_TIMSET

This register specifies the Connect/Disconnect detection time and Resume detection time when the clock from the UTMI+ PHY is stopped in the Suspend state.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	TIMER_CONNECT[15:0]															
Initial value:	0	0	0	0	0	0	0	1	0	1	0	0	1	1	1	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TIMER_RESUME[15:0]															
Initial value:	0	0	0	0	0	0	1	0	1	0	0	1	1	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	TIMER_CONNECT[15:0]	H'014E	R/W	These bits specify the timer value used to detect Device Connect or Disconnect while the UTMI+ interface SUSPENDM is asserted. Assuming that the clock from the UTMI+ PHY stops while SUSPENDM is asserted, whether Connect or Disconnect has occurred is checked using the AHB clock (HCLK). Set this timer value so that the detection time is 2.5 µs or longer according to the AHB clock frequency used. A value of 1 specifies one cycle (µs). Reference setting values: AHB clock is 100 MHz: H'FA or a greater value AHB clock is 200 MHz: H'1F4 or a greater value
15 to 0	TIMER_RESUME[15:0]	H'029B	R/W	These bits specify the timer value used to detect the RemoteWakeup signal from the device while the UTMI+ interface SUSPENDM is asserted. Assuming that the clock from the UTMI+ PHY stops while SUSPENDM is asserted, whether the RemoteWakeup signal has been received is checked using the AHB clock (HCLK). Set this timer value so that the detection time is 5 µs or longer according to the AHB clock frequency used. A value of 1 specifies one cycle (µs). Reference setting values: AHB clock is 100 MHz: H'1F4 or a greater value AHB clock is 200 MHz: H'3E8 or a greater value

41.3.5.5 Overcurrent Detection Timer Setting Register (offset: H'310)

Register symbol: OC_TIMSET

This register specifies the overcurrent detection time.

When the overcurrent detection input signal (USBn_OVC) is asserted to 0 continuously for the time specified in this register, occurrence of an overcurrent is detected.

[Note]

This register setting is ignored when the OCISEL bit (bit [5]) in the host COMMON/OHCI extended register (offset: H'360) is 1.

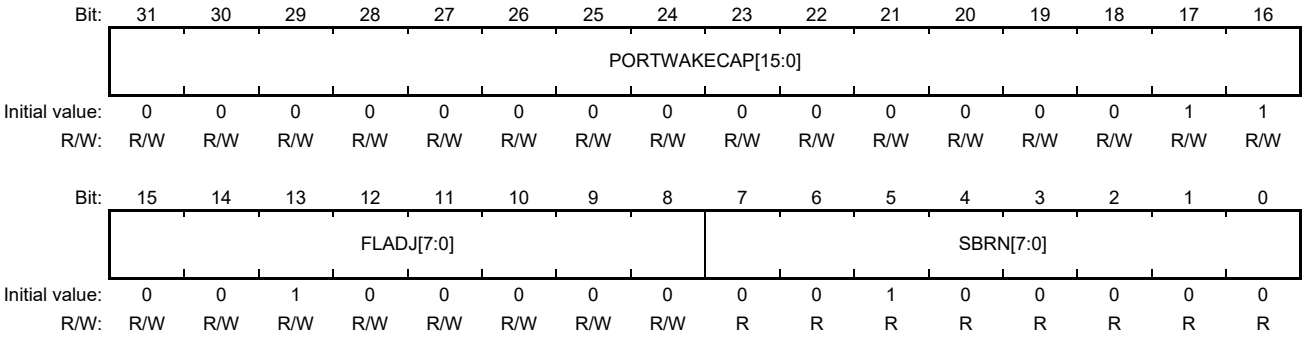
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	TIMER_OC[19:16]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TIMER_OC[15:0]															
Initial value:	0	0	0	0	1	0	0	1	1	0	1	0	1	0	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The write value should be 0.
19 to 0	TIMER_OC [19:0]	H’2 09AB	R/W	These bits specify the timer value used to detect an overcurrent. When the overcurrent detection input signal (USBn_OVC) is asserted to 0 continuously for the time specified in this field, this module determines that an overcurrent has occurred. Set this timer value so that the detection time is 1 to 2 ms or longer according to the AHB clock frequency used. A value of 1 specifies one cycle (μs). Note that occurrence of an overcurrent is detected when USBn_OVCis asserted to 0 continuously over a certain period. Specify the period in these bits according to the AHB clock frequency. Reference setting values: To specify 1 ms when the AHB clock is 100 MHz: H'1_86A0 or a greater value To specify 1 ms when the AHB clock is 200 MHz: H'3_0D40 or a greater value

41.3.5.6 SBRN, FLADJ, PORTWAKECAP Register (offset: H'314)

Register symbol: SBRN_FLADJ_PW



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	PORTWAKE CAP[15:0]	H'0003	R/W	The intended use of these bits are to establish a policy about which ports are to be used for wake events. This bit setting does not affect the operation of the host core.
15 to 8	FLADJ[7:0]	H'20	R/W	These bits adjust the length of one micro-frame in units of 16-HS-bit time. The initial value is H'20 (60000 HS-bit time).
7 to 0	SBRN[7:0]	H'20	R	These bits indicate the serial bus release number. This value is fixed to H'20.

41.4 Clock Specifications

41.4.1 Clock Gating Specifications

41.4.1.1 Overview

This module has a function for switching between the host and peripheral modes. In some case, no clock supply is needed for the unused circuits (stopping the clock causes no problem).

To reduce the power consumption through clock gating for the circuits that do not need clock supply, this module provides three clock control gating bits in the register enable/clock gating control register.

Control these bits appropriately to gate the clock supply to some circuits in the host core and peripheral controller.

Bit	Symbol
[31]	NONUSE_CLK_MSK
[29]	HOST_CLK_MSK
[28]	PERI_CLK_MSK

For the bus clock, the AHB clock for the AHB_IF module is excluded from the targets of clock gating assuming that there may be unexpected access from the system or switching between the host and peripheral modes through register settings. However, the AHB clock for the other circuits is gated.

41.5 Reset Specifications

41.5.1 Input Reset Specifications

This module has a software reset input from CPG module. Asserting this reset signal initializes all FFs in this module.

41.6 Interrupt Specifications

41.6.1 Interrupt Signal List

This module has the following six interrupt signal lines. Use all of them as level interrupts.

Interrupt Pin Name	Interrupt Type	Pulse/ Level	Minimum Pulse Width	Active Level	Synchro-nized with
U2H_INT	An interrupt signal output from the AHB_IF module. This is generated when a bus error occurs in the AHB master. It is controlled through the related AHB bridge register.	Level	—	H	HCLK
U2H_OHCI_INT	An interrupt signal output from OHCI. This is generated when data transfer is completed or a change in the USB bus state is detected in the FS or LS transfer. It is controlled through the related OHCI operational register.	Level	—	H	HCLK
U2H_EHCI_INT	An interrupt signal output from EHCI. This is generated when data transfer is completed or a change in the USB bus state is detected in the HS transfer. It is controlled through the related EHCI operational register.	Level	—	H	HCLK
U2H_WAKEON_INT	An interrupt signal output from EHCI. This is generated due to an EHCI wakeup event. It is controlled through the related EHCI operational register.	Level	—	H	HCLK
U2H_BIND_INT	Logical OR of the interrupt signals. (U2H_INT + U2H_OHCI_INT + U2H_EHCI_INT + U2H_WAKEON_INT)	Level	—	H	HCLK

41.6.2 Interrupt Sources and Control

41.6.2.1 U2H_INT Assertion Source and Control

Interrupt Enable Control in Register:

This interrupt signal is asserted when an interrupt source event occurs while the interrupt enable bit in the following register is set to enabled (1).

AHB bridge register: INT_ENABLE register (offset: H'200) Bit [0] (AHB_INTEN)

Interrupt Source:

A bus error occurs (MHRESP = 1) in the AHB master.

Clearing Interrupt:

To clear the interrupt, write 1 to the following register bit.

AHB bridge register: INT_STATUS register (offset: H'204) Bit [0] (AHB_INT)

41.6.2.2 U2H_OHCI_INT Assertion Sources and Control

Interrupt Enable Control in Registers:

This interrupt signal is asserted when an interrupt source event occurs while the interrupt enable bits in the following registers are set to enabled (1).

AHB bridge register: INT_ENABLE register (offset: H'200) Bit [1] (USBH_INTAEN)
OHCI operational register: HcInterruptEnable Register (offset: H'010) Bit [31] and bits [6:0]*

Note: * Set the necessary bits enabled as interrupt assertion source bits.

Interrupt Sources:

		Necessary Enable Settings in Register Bits							
			HcInterruptEnable						
			Bit[31]	Bit[6]	Bit[5]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
	Interrupt Source	USBH_INTAEN	MIE	RHSCE	FNOE	ROE	SFE	WDHE	SOE
1	Device connection is detected.	√	√	√					
2	Device disconnection is detected.	√	√	√					
3	Port power is turned off (overcurrent detection is not included).	√	√	√					
4	Babble error is detected during USB transfer.	√	√	√					
5	Resume process is completed.	√	√	√					
6	Overcurrent is detected.	√	√	√					
7	Bus reset process is completed.	√	√	√					
8	OHCI enters the Operational state (HCFS[1:0] = B'10) or Suspend state (HCFS[1:0] = B'11]) while the DR bit in the HcRhDescritorB register is 1.	√	√	√					
9	1 is written to the OHCI HcRhPort status bit [0] (ClearPortEnable) while no device is connected (CCS bit = 0).	√	√	√					
10	1 is written to the OHCI HcRhPort status bit [1] (SetPortEnable) while no device is connected (CCS bit = 0).	√	√	√					
11	1 is written to the OHCI HcRhPort status bit [2] (SetPortSuspend) while no device is connected (CCS bit = 0).	√	√	√					
12	1 is written to the OHCI HcRhPort status bit [3] (ClearSuspendStatus) while no device is connected (CCS bit = 0).	√	√	√					
13	1 is written to the OHCI HcRhPort status bit [4] (SetPortReset) while no device is connected (CCS bit = 0).	√	√	√					
14	Port power is turned off while no device is connected (CCS bit = 0).	√	√	√					
15	MSB of bits [15:0] (FrameNumber) in the HcFmNumber register changes.	√	√		√				
16	RemoteWakeup signal (Resume signal) from a device is detected.	√	√			√			
17	HccaFrameNumber is updated (this means almost the same as an SOF transmission).	√	√				√		
18	Transfer (including an error) ends and the host core updates HccaDoneHead.	√	√					√	
19	USB schedule overrun occurs for a frame.	√	√						√

√: Necessary

Clearing Interrupt:

To clear the interrupt, write 1 to one of the following register bits that corresponds to the interrupt source.

OHCI operational register: HcInterruptStatus register (offset: H'00C) Bits [6:0]

41.6.2.3 U2H_EHCI_INT Assertion Sources and Control

Interrupt Enable Control in Registers:

This interrupt signal is asserted when an interrupt source event occurs while the interrupt enable bits in the following registers are set to enabled (1).

AHB bridge register: INT_ENABLE register (offset: H'200) Bit [2] (USBH_INTBEN)
EHCI operational register: USBINTR register (offset: H'128) Bits [17:16] and bits [5:0]*

Note: * Set the necessary bits enabled as interrupt assertion source bits.

In addition, control the following register bits as necessary.

EHCI operational register: USBCMD register (offset: H'120) Bit [15] and bit [6]

Interrupt Sources:

		Necessary Enable Settings in Register Bits								
			USBCMD		USBINTR					
			Bit[15]	Bit[6]	Bit[17]	Bit[16]	Bit[5]	Bit[3]	Bit[2]	Bit[1]	Bit[0]
	Interrupt Source	USBH_INTBEN	Per-Port Change Event	Door-bell	Port-n Change Event		Async Advance	Frame List Roll-over	Port Change	USB ERRINT	USB INT
1	Device connection is detected.	√							√		
2	Device disconnection is detected.	√							√		
3	Overcurrent is detected.	√							√		
4	RemoteWakeup signal (Resume signal) from a device is detected.	√							√		
5	Babble state is detected on the USB bus.	√							√		
6	USB transfer with qTD IOC = 1 is successfully completed.	√									√
7	Short packet is received.	√									√
8	USB transfer ends with an error. (Retry fails three times, a babble error is detected, or STALL is received.)	√								√	
9	QH processing with bit [6] (Interrupt on Async Advance Doorbell) in the USBCMD register set to 1 is successfully completed.	√		√			√				
10	FrameIndex bit in the FRINDEX register returns from the maximum value to H'000 (rollover is detected).	√						√			
11	Port Change Detect event (interrupt sources 1 to 5) is detected in USB port 1.	√	√			√					
12	Port Change Detect event (interrupt sources 1 to 5) is detected in USB port 2.	√	√		√						

√: Necessary

Clearing Interrupt:

To clear the interrupt, write 1 to one of the following register bits that corresponds to the interrupt source.

EHCI operational register: USBSTS register (offset: H'124) Bits [17:16] and bits [5:0]

41.6.2.4 U2H_WAKEON_INT Assertion Sources and Control

Interrupt Enable Control in Registers:

This interrupt signal is asserted when an interrupt source event occurs while the interrupt enable bits in the following registers are set to enabled (1).

AHB bridge register: INT_ENABLE register (offset: H'200) Bit [4] (WAKEON_INTEN)
EHCI operational register: PORTSC[1:2] registers (offset: H'164 and H'168) Bits [22:20]*

Note: * Set the necessary bits enabled as interrupt assertion source bits.

Interrupt Sources:

		Necessary Enable Settings in Register Bits			
			PORTSC		
			Bit[22]	Bit[21]	Bit[20]
	Interrupt Source	WAKEON_INTEN	WKOC_E	WKDSCNNT_E	WKCNNT_E
1	Device connection is detected.	√			√
2	Device disconnection is detected.	√		√	
3	Overcurrent is detected.	√	√		
4	RemoteWakeup signal (Resume signal) from a device is detected.	√			

√: Necessary

Clearing Interrupt:

To clear the interrupt, write 1 to the following register bit.

AHB bridge register: INT_STATUS register (offset: H'204) Bit [4] (WAKEON_INT)

41.6.3 Interrupt Signal Deassertion Timing

After a register is accessed to clear an interrupt source, it may take a certain period of time until the corresponding interrupt is actually cleared. Therefore, a measure should be taken to prevent misdetection of the previous interrupt between register access for clearing and correct detection of the next interrupt.

41.6.3.1 Connection of Interrupt Signal Lines

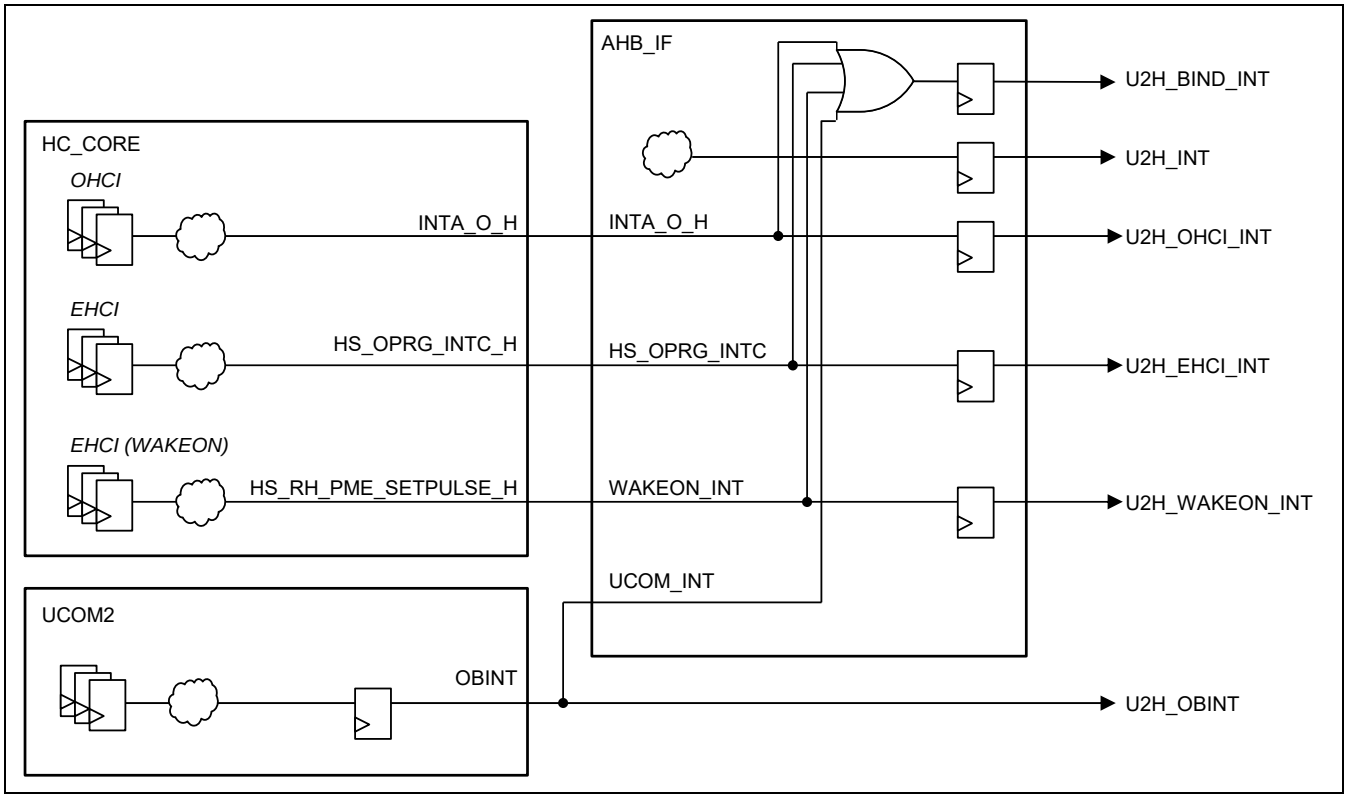


Figure 41.2 Connection diagram of Interrupt Signal Lines

41.7 Power Management

The system implementing this module provides the following two types of low-power control for the USB 2.0 core (including the UTMI+ PHY).

1. Controls the SUSPENDM and SLEEPM pins of the UTMI+ PHY.
2. Stops unnecessary clock supply to the host core internal circuits and the peripheral core through clock gating.

41.7.1 Controlling SUSPENDM and SLEEPM Pins of UTMI+ PHY

The following power-reducing effects are expected from assertion of the SUSPENDM and SLEEPM pins of the UTMI+ PHY.

- The power consumption in the UTMI+ PHY can be reduced (this depends on the PHY).
- The power consumption in the host core can be reduced because the clock from the PHY is stopped.

The SUSPENDM and SLEEPM pins of the UTMI+ PHY are not asserted in the default settings even when the EHCI or OHCI is placed in the Suspend state as described earlier.

See section 41.3.5.3, Suspend Control Register (offset: H'308), and set up the register appropriately.

41.7.2 Controlling Clock Gating Function

The clock supply to the unused one of the host and peripheral functions can be gated through register settings.

See section 41.3.5.2, Register Enable/Clock Gating Control Register (offset: H'304), and set up the register appropriately.

41.8 Operation

This section describes register operations required for the initial settings of this module and the registers required for the power consumption control.

41.8.1 Power control and Initialization

1. EHCI/OHCI module stop release and module reset assert.
2. PLLRESET release (Note: Refer to UGCTRL register in Section 42)
3. Wait min. 340 µs for USB PHY power stable.
4. USB0SEL[1:0] should be set to B'01 for EHCI/OHCI. (Note: Refer to UGCTRL2 register in Section 42)
5. Starting normal operation.

41.8.2 Transfer Overview

Transfer by the host controller must be performed in compliance with the following OHCI and EHCI specifications.

Open Host Controller Interface Specification for USB Rev 1.0a

Enhanced Host Controller Interface Specification for Universal Serial Bus Revision 1.0

42. USB High-Speed Module (HS-USB)

42.1 Overview

This module is a USB controller provided with the function controller function, and high-speed transfer and full-speed transfer are available. Provided with an on-chip USB transceiver, this module also supports all transfer types defined by the USB Specification.

This module can use up to 16 pipes. Furthermore, for pipes 1 to F, arbitrary endpoint numbers can be allocated according to peripheral devices to be communicated and user systems.

42.1.1 Features

(1) On-chip USB transceiver

(2) Achieves space-saving mount with less external elements

- On-chip D+ pull-up resistor (function operation mode)
- On-chip D+/D- terminating resistors (high-speed operation mode)
- On-chip D+/D- output resistors (full-speed operation mode)

(3) All Types of USB Transfers Supported

- Control transfer
- Bulk transfer
- Interrupt transfer (except for high bandwidth)
- Isochronous transfer (except for high bandwidth)

(4) Dedicated DMA interface

- On-chip 4-channel DMA interface

(5) Pipe configuration

- Up to sixteen pipes are selectable (including the default control pipe)
- Programmable pipe configuration
- Arbitrary endpoint numbers can be allocated to pipes 1 to F.
- Settable transfer conditions for each pipe are as follows:

Pipe 0:	A pipe only for control transfer with a 64-byte (fixed) single buffer
Pipes 1 and 2:	Bulk transfers/isochronous transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)
Pipes 3 to 5 and B to F:	Bulk transfer, continuous transfer mode, programmable buffer size (up to 2-Kbytes: double buffer can be specified)
Pipes 6 to 8:	Interrupt transfer, 64-byte fixed single buffer
Pipes 9 to A:	Interrupt transfer, Bulk transfer, continuous transfer mode, programmable (up to 2-Kbytes: double buffer can be specified)

(6) Other functions

- Transfer ending function using transaction count
- DMA transfer ending function using external triggers (TEND or WREND signal)
- SOF pulse output function
- BRDY interrupt event notification timing change function (BFRE)

- Function that automatically clears the buffer memory after the data for the pipe specified at the DnFIFO (n = 0 to 3) port has been read (DCLRM)
- NAK setting function (SHTNAK) for the response PID due to the transfer end
- The suspend and resume of whole LSI can be done by using USBHS.

(7) Embedded USB PHY

The embedded USB PHY consists of the following features.

- Contains the USB functions drivers and receivers for D+ and D- signaling

42.1.2 Input/Output Pins

Table 42.1 lists the input and output pins of the USB.

Table 42.1 Pin Configuration of USB

Classification	Pin Name	Name	I/O	Description
USB bus interface	USB0_DP	USB channel 0 D+ data	I/O	D+ Input/output of the on-chip transceiver Connect this pin to the D+ pin of the USB bus channel 0
	USB0_DM	USB channel 0 D- data	I/O	D- Input/output of the on-chip transceiver Connect this pin to the D- pin of the USB bus channel 0
	USB1_DP	USB channel 1 D+ data	I/O	D+ Input/output of the on-chip transceiver Connect this pin to the D+ pin of the USB bus channel 1
	USB1_DM	USB channel 1 D- data	I/O	D- Input/output of the on-chip transceiver Connect this pin to the D- pin of the USB bus channel 1
Reference resistance	RREF	USB external reference resistor	I	Connect to external 5.6kΩ±1% resistor.
VBUS	USB0_VBUS	USB channel 0 VBUS	I	The external series resistor is not required Connect this pin to the USB VBUS channel 0
	USB1_VBUS	USB channel 1 VBUS	I	The external series resistor is not required Connect this pin to the USB VBUS channel 1
Over current	USB0_OVC	USB channel 0 Over current	I/O	Connect to over current detection pin of external power IC which supply VBUS power. This is low active signal
	USB1_OVC	USB channel 0 Over current	I/O	Connect to over current detection pin of external power IC which supply VBUS power. This is low active signal
Power Enable	USB0_PWEN	USB channel 0 Power enable	I/O	Connect to power enable pin of external power IC which supply VBUS power
	USB1_PWEN	USB channel 0 Power enable	I/O	Connect to power enable pin of external power IC which supply VBUS power

42.2 Register Descriptions

HS-USB	Base Address
Channel 0	H'E659 0000
Channel 1	H'E659 8000

Table 42.2 lists the registers used in this module. Table 42.3 lists the register states in each processing mode.

Table 42.2 Register Configuration

Register Name	Abbreviation	R/W	Address Offset	Access Size
System configuration control register	SYSCFG	R/W	H'000	16
CPU bus wait register	BUSWAIT	R/W	H'002	16
System configuration status register	SYSSTS	R	H'004	16
Device state control register	DVSTCTR	R/W	H'008	16
Test mode register	TESTMODE	R/W	H'00C	16
CFIFO port register	CFIFO	R/W	H'014	16
CFIFO port select register	CFIFOSEL	R/W	H'020	16
CFIFO port control register	CFIFOCTR	R/W	H'022	16
D0FIFO port select register	D0FIFOSEL	R/W	H'028	16
D0FIFO port control register	D0FIFOCTR	R/W	H'02A	16
D1FIFO port select register	D1FIFOSEL	R/W	H'02C	16
D1FIFO port control register	D1FIFOCTR	R/W	H'02E	16
Interrupt enable register 0	INTENB0	R/W	H'030	16
BRDY interrupt enable register	BRDYENB	R/W	H'036	16
NRDY interrupt enable register	NRDYENB	R/W	H'038	16
BEMP interrupt enable register	BEMPENB	R/W	H'03A	16
SOF output configuration register	SOFCFG	R/W	H'03C	16
Interrupt status register 0	INTSTS0	R/W	H'040	16
BRDY interrupt status register	BRDYSTS	R/W	H'046	16
NRDY interrupt status register	NRDYSTS	R/W	H'048	16
BEMP interrupt status register	BEMPSTS	R/W	H'04A	16
Frame number register	FRMNUM	R/W	H'04C	16
μ frame number register	UFRMNUM	R/W	H'04E	16
USB address register	USBADDR	R	H'050	16
USB request type register	USBREQ	R	H'054	16
USB request value register	USBVAL	R	H'056	16
USB request index register	USBINDX	R	H'058	16
USB request length register	USBLENG	R	H'05A	16
DCP maximum packet size register	DCPMAXP	R/W	H'05E	16
DCP control register	DCPCTR	R/W	H'060	16
Pipe window select register	PIPESEL	R/W	H'064	16
Pipe configuration register	PIPECFG	R/W	H'068	16
Pipe buffer register	PIPEBUF	R/W	H'06A	16
Pipe maximum packet size register	PIPEMAXP	R/W	H'06C	16
Pipe cycle control register	PIPEPERI	R/W	H'06E	16

Register Name	Abbreviation	R/W	Address Offset	Access Size
Pipe 1 control register	PIPE1CTR	R/W	H'070	16
Pipe 2 control register	PIPE2CTR	R/W	H'072	16
Pipe 3 control register	PIPE3CTR	R/W	H'074	16
Pipe 4 control register	PIPE4CTR	R/W	H'076	16
Pipe 5 control register	PIPE5CTR	R/W	H'078	16
Pipe 6 control register	PIPE6CTR	R/W	H'07A	16
Pipe 7 control register	PIPE7CTR	R/W	H'07C	16
Pipe 8 control register	PIPE8CTR	R/W	H'07E	16
Pipe 9 control register	PIPE9CTR	R/W	H'080	16
Pipe A control register	PIPEACTR	R/W	H'082	16
Pipe B control register	PIPEBCTR	R/W	H'084	16
Pipe C control register	PIPECCTR	R/W	H'086	16
Pipe D control register	PIPEDCTR	R/W	H'088	16
Pipe E control register	PIPEECTR	R/W	H'08A	16
Pipe F control register	PIPEFCTR	R/W	H'08C	16
Pipe 1 transaction counter enable register	PIPE1TRE	R/W	H'090	16
Pipe 1 transaction counter register	PIPE1TRN	R/W	H'092	16
Pipe 2 transaction counter enable register	PIPE2TRE	R/W	H'094	16
Pipe 2 transaction counter register	PIPE2TRN	R/W	H'096	16
Pipe 3 transaction counter enable register	PIPE3TRE	R/W	H'098	16
Pipe 3 transaction counter register	PIPE3TRN	R/W	H'09A	16
Pipe 4 transaction counter enable register	PIPE4TRE	R/W	H'09C	16
Pipe 4 transaction counter register	PIPE4TRN	R/W	H'09E	16
Pipe 5 transaction counter enable register	PIPE5TRE	R/W	H'0A0	16
Pipe 5 transaction counter register	PIPE5TRN	R/W	H'0A2	16
Pipe B transaction counter enable register	PIPEBTRE	R/W	H'0A4	16
Pipe B transaction counter register	PIPEBTRN	R/W	H'0A6	16
Pipe C transaction counter enable register	PIPECTRE	R/W	H'0A8	16
Pipe C transaction counter register	PIPECTRN	R/W	H'0AA	16
Pipe D transaction counter enable register	PIPEDTRE	R/W	H'0AC	16
Pipe D transaction counter register	PIPEDTRN	R/W	H'0AE	16
Pipe E transaction counter enable register	PIPEETRE	R/W	H'0B0	16
Pipe E transaction counter register	PIPEETRN	R/W	H'0B2	16
Pipe F transaction counter enable register	PIPEFTRE	R/W	H'0B4	16
Pipe F transaction counter register	PIPEFTRN	R/W	H'0B6	16
Pipe 9 transaction counter enable register	PIPE9TRE	R/W	H'0B8	16
Pipe 9 transaction counter register	PIPE9TRN	R/W	H'0BA	16
Pipe A transaction counter enable register	PIPEATRE	R/W	H'0BC	16
Pipe A transaction counter register	PIPEATRN	R/W	H'0BE	16
D2FIFO port select register	D2FIFOSEL	R/W	H'0F0	16
D2FIFO port control register	D2FIFOCTR	R/W	H'0F2	16
D3FIFO port select register	D3FIFOSEL	R/W	H'0F4	16
D3FIFO port control register	D3FIFOCTR	R/W	H'0F6	16
Low power status register	LPSTS	R/W	H'102	16

Register Name	Abbreviation	R/W	Address Offset	Access Size
USB general control register	UGCTRL	R/W	H'E659 0180*	32
USB general control register 2	UGCTRL2	R/W	H'184	32

Note: * UGCTRL register is used for both HS-USB Channel 0 and HS-USB Channel 1

Table 42.3 Register States in Each Processing Mode

Abbreviation	Power-On Reset	Module Standby
SYSCFG	Initialized	Retained
BUSWAIT	Initialized	Retained
SYSSTS	Initialized	Retained
DVSTCTR	Initialized	Retained
TESTMODE	Initialized	Retained
CFIFO	Initialized	Retained
CFIFOSEL	Initialized	Retained
CFIFOCTR	Initialized	Retained
D0FIFOSEL	Initialized	Retained
D0FIFOCTR	Initialized	Retained
D1FIFOSEL	Initialized	Retained
D1FIFOCTR	Initialized	Retained
INTENB0	Initialized	Retained
BRDYENB	Initialized	Retained
NRDYENB	Initialized	Retained
BEMPENB	Initialized	Retained
SOFCFG	Initialized	Retained
INTSTS0	Initialized	Retained
BRDYSTS	Initialized	Retained
NRDYSTS	Initialized	Retained
BEMPSTS	Initialized	Retained
FRMNUM	Initialized	Retained
UFRMNUM	Initialized	Retained
USBADDR	Initialized	Retained
USBREQ	Initialized	Retained
USBVAL	Initialized	Retained
USBINDX	Initialized	Retained
USBLENG	Initialized	Retained
DCPMAXP	Initialized	Retained
DCPCTR	Initialized	Retained
PIPESEL	Initialized	Retained
PIPECFG	Initialized	Retained
PIPEBUF	Initialized	Retained
PIPEMAXP	Initialized	Retained
PIPEPERI	Initialized	Retained
PIPE1CTR	Initialized	Retained
PIPE2CTR	Initialized	Retained
PIPE3CTR	Initialized	Retained
PIPE4CTR	Initialized	Retained
PIPE5CTR	Initialized	Retained
PIPE6CTR	Initialized	Retained
PIPE7CTR	Initialized	Retained

Abbreviation	Power-On Reset	Module Standby
PIPE8CTR	Initialized	Retained
PIPE9CTR	Initialized	Retained
PIPEACTR	Initialized	Retained
PIPEBCTR	Initialized	Retained
PIPECCTR	Initialized	Retained
PIPEDCTR	Initialized	Retained
PIPEECTR	Initialized	Retained
PIPEFCTR	Initialized	Retained
PIPE1TRE	Initialized	Retained
PIPE1TRN	Initialized	Retained
PIPE2TRE	Initialized	Retained
PIPE2TRN	Initialized	Retained
PIPE3TRE	Initialized	Retained
PIPE3TRN	Initialized	Retained
PIPE4TRE	Initialized	Retained
PIPE4TRN	Initialized	Retained
PIPE5TRE	Initialized	Retained
PIPE5TRE	Initialized	Retained
PIPEBTRN	Initialized	Retained
PIPEBTRN	Initialized	Retained
PIPECTRN	Initialized	Retained
PIPECTRN	Initialized	Retained
PIPEDTRN	Initialized	Retained
PIPEDTRN	Initialized	Retained
PIPEETRN	Initialized	Retained
PIPEETRN	Initialized	Retained
PIPEFTRN	Initialized	Retained
PIPEFTRN	Initialized	Retained
PIPE9TRE	Initialized	Retained
PIPE9TRN	Initialized	Retained
PIPEATRE	Initialized	Retained
PIPEATRN	Initialized	Retained
D2FIFOSEL	Initialized	Retained
D2FIFOCTR	Initialized	Retained
D3FIFOSEL	Initialized	Retained
D3FIFOCTR	Initialized	Retained
LPSTS	Initialized	Retained
UGCTRL	Initialized	Retained
UGCTRL2	Initialized	Retained

42.2.1 System Configuration Control Register (SYSCFG)

SYSCFG enables or disables high-speed operation controls USB0_DP/USB1_DP and USB0_DM/USB1_DM pins, and enables or disables the operation of this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	HSE	—	—	DPRPU	—	—	—	USBE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	HSE	0	R/W	High-Speed Operation Enable 0: High-speed operation is disabled. When the function controller function is selected: Full-speed operation only 1: High-speed operation is enabled. (This module detects the transmission rate.) When HSE is 0, this module performs full-speed operation. When HSE is 1, this module executes the reset handshake protocol, and according to the result, this module automatically performs high-speed or full-speed operation. Change this bit while the DPRPU bit is 0.
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	DPRPU	0	R/W	D+ Line Resistance Control Enables or disables pull-up of the D+ line when the function controller function is selected. 0: Pull-up is disabled. 1: Pull-up is enabled. When this bit is set to 1 before using this module, this module pulls up the D+ line at 3.3V, and informs the USB host of ATTACH. Clearing this bit to 0 cancels the pull-up of the D+ line, and informs the USB host of DETACH. Set this bit to 1 when the function controller function is selected.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	USBE	0	R/W	USB Module Operation Enable Enables or disables the USB module operation. 0: The USB module operation is disabled. 1: The USB module operation is enabled. Table 42.4 lists the registers and bit names initialized when this bit is cleared to 0.

Table 42.4 Registers Initialized by Writing 0 in the USBE Bit

Register Name	Bit Name	Remarks
SYSSTS	LNST	
DVSTCTR	RHST	
INTSTS0	DVSQ	
USBADDR	USBADDR	
USEREQ	BRequest, bmRequestType	
USBVAL	wValue	
USBINDX	wIndex	
USBLENG	wLength	

42.2.2 CPU Bus Wait Register (BUSWAIT)

BUSWAIT specifies the number of access waits from the CPU to this module.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	BWAIT[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	BWAIT[3:0]	1111	R/W	CPU Bus Wait Specify the number of access waits to this module. 0000: 0 waits (2 access cycles) 0001: 1 wait (3 access cycles) 0010 to 1110: 2 to 14 waits (4 to 16 access cycles) 1111: 15 waits (17 access cycles) initial value The following restriction is provided for access cycles to the registers of addresses beginning with H'04 of this controller. Restriction for wait: The cycle of continuous accesses to the registers of this controller must be 80 ns or more. To satisfy this restriction, control waits using the frequency of system clock HPϕ. Choose the best value within the initial value of 17 clock cycles (maximum). This setting is the same as the waits in accesses to the FIFO port register. The maximum speed of accesses to the FIFO port is as follows: MBW = B'10 (32-bit width) : Max. 48 Mbytes/s MBW = B'01 (16-bit width) : Max. 24 Mbytes/s MBW = B'00 (8-bit width) : Max. 12 Mbytes/s

42.2.3 System Configuration Status Register (SYSSTS)

SYSSTS monitors the USB data bus line status (D+ and D- lines).

This register is initialized by a power-on reset or a USB reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	LINE[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	LNST[1:0]	Undefined*	R	USB Data Line Status Monitor Indicate the USB data bus line (D+ and D- lines) status. Table 42.5 shows the USB data bus line status. Read these bits after the attach processing (DPRPU = 1)

Note: * These bits depend on the state of the USB0_DP/USB1_DP, USB0_DM/USB1_DM, and USB0_OVC/USB1_OVC pins.

Table 42.5 USB Data Bus Line Status

LNST[1]	LNST[0]	Full-Speed Operation	High-Speed Operation	Chirp Operation
0	0	SE0	Squelch	Squelch
0	1	J-State	UnSquelch	Chirp J
1	0	K-State	Invalid	Chirp K
1	1	SE1	Invalid	Invalid

Legend:

Chirp: The reset handshake protocol (RHSP) is being executed with high-speed operation is enabled (HSE = 1 in SYSCFG).
Squelch: SE0 or idle state
UnSquelch: High-speed J-State or high-speed K-State
Chirp J: Chirp J-State
Chirp K: Chirp K-State
Invalid: Invalid

42.2.4 Device State Control Register (DVSTCTR)

DVSTCTR controls and monitors the USB data bus state.

This register is initialized by a power-on reset. The WKUP bit is initialized and the RESUME bit becomes undefined by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	WKUP	—	—	—	—	—	RHST[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	WKUP	0	R/W*	Wakeup Output Enables or disables the remote wakeup (resume signal output) to the USB bus when the function controller function is selected. 0: The remote wakeup signal is not output. 1: The remote wakeup signal is output. This module controls the remote wakeup signal output time. When this bit is set to 1, this module outputs 10 ms K-State and then clears this bit. The USB Specification requires the USB bus idle state to be maintained for at least 5 ms before transmitting the remote wakeup signal. For this reason, this module outputs K-State after waiting for 2 ms even if 1 is written in this bit immediately after the suspended state is detected. Write 1 in this bit only when the device is in the suspended state (DVSQ = 1xx in INTSTS0) and remote wakeup is enabled by the USB host. When setting this bit to 1, do not stop the internal clock even in the suspended state (Write 1 in this bit with SUSPM set to 1).
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	RHST[2:0]	000	R	Reset Handshake Indicate the reset handshake state. 000: Transmission rate is undefined. 100: The reset handshake processing is in progress. 010: Full-speed connection 011: High-speed connection When this module detects a USB bus reset with the HSE bit set to 1 for the port, these bits become B'100. After that, when this module outputs ChirpK and detects ChirpJK from the USB host three times, these bits become B'011. Unless high-speed mode is fixed within 2.5 ms after the ChirpK output, these bits become B'010. When this module detects a USB bus reset with the HSE bit set to 0 for the port, these bits become B'010. When the RHST bits are fixed to B'010 or B'011 after this module detected a USB bus reset, the DVST interrupt occurs.

42.2.5 Test Mode Register (TESTMODE)

TESTMODE controls the USB test signal output in high-speed operation mode.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	UTST[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	UTST[3:0]	0000	R/W	Test Mode Table 42.6 shows the test mode operation of this module. Control the USB test signal output in high-speed operation mode. These bits are valid only in high-speed operation mode. Use this test mode when the RHST bits in DVSTCTR are B'011. After the test with these bits, cancel this test mode by a power-on reset. Set these bits according to the SetFeature request from the USB host during high-speed communication. While these bits are B'0001 to B'0100, this module does not enter the suspended state.

Table 42.6 Test Mode Operation

Test Mode	UTST Bits Setting
Normal operation	B'0000
Test_J	B'0001
Test_K	B'0010
Test_SE0_NAK	B'0011
Test_Packet	B'0100
Test_Force_Enable	—
Reserved	B'0101 to B'0111

42.2.6 CFIFO Port Register

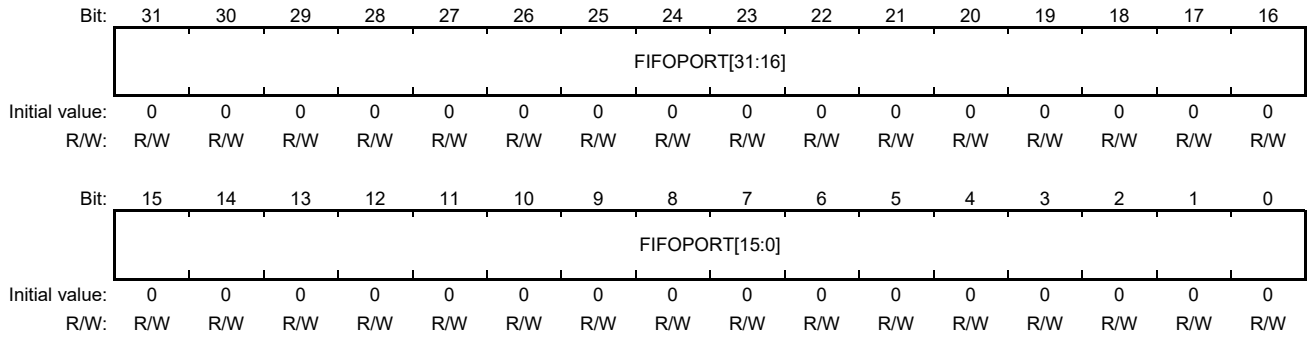
CFIFO is a port register to read data from or write data to the FIFO buffer memory.

Each FIFO port consists of this register (CFIFO) for data read/write from/to the FIFO buffer memory, the select registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL) to select pipes to be allocated to a FIFO port, and the control registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR).

Each FIFO port provides the following features.

- Make accesses to the FIFO buffer for DCP through the CFIFO port.
- Make accesses to the FIFO buffer with DMA transfers through the DMAC module for USB high-speed only.
- When using a function specific to FIFO ports (DMA transfer function, etc.), the pipe number (selected pipe) specified by the CURPIPE bits cannot be changed.
- Register groups of a FIFO port do not affect other FIFO ports.
- Do not allocate the same pipe number to different FIFO ports.
- There are two FIFO buffer states where the access mastership is on the CPU side and on the SIE side. When the FIFO buffer access mastership is on the SIE side, the CPU cannot make an access to the FIFO buffer.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	FIFOPORT [31:0]	All 0	R/W	FIFO Port Read receive data from the FIFO buffer or write transmit data to the FIFO buffer using these bits. Access to this register is enabled only when the FRDY bit in each control register (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFOCTR) is set to 1. Valid bits in this register vary with the value of the MBW bits. Table 42.7 shows the valid bits in this register.

Table 42.7 Operation of This Register when Accessed

Access Size	Bits 31 to 24	Bits 23 to 16	Bits 15 to 8	Bits 7 to 0
32 bits	N + 3 address	N + 2 address	N + 1 address	N + 0 address
16 bits	Write: Invalid, Read: Prohibited*		N + 1 address	N + 0 address
8 bits	Write: Invalid, Read: Prohibited*			N + 0 address

Note: * Reading an invalid register with word access or byte access is prohibited.

42.2.7 FIFO Port Select Registers (CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL, D3FIFOSEL)

CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL select pipes to be allocated to FIFO ports and control accesses to each FIFO port.

Do not specify the same pipe number for the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL When the CURPIPE bits in D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL are set to B'000, no pipe is specified.

Do not change any pipe number when DMA transfer is enabled.

This register is initialized by a power-on reset.

(1) CFIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	—	—	MBW[1:0]		—	—	—	—	ISEL	—	CURPIPO[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R/W	R/W	R	R	R	R	R/W	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies read mode of the DTLN bits in CFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the CFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of CFIFO receive data.
14	REW	0	R/W	Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.
13, 12	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	00	R/W	CFIFO Port Access Bit Width Specify the bit width for accesses to the CFIFO port. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read. When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time. When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory. When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.
9 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5	ISEL	0	R/W	CFIFO Port Access Direction when DCP is Selected 0: Buffer memory read is selected. 1: Buffer memory write is selected. To change this bit when the selected pipe is DCP, write 1 or 0 in this bit, read the value of this bit, confirm that the write value equals the read value, and then proceed with the next processing. If this bit is changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of this bit is rewritten, and then further access is enabled. Set this bit concurrently with the CURPIPE bits.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE [3:0]	0000	R/W	CFIFO Port Access Pipe Select Set the number of pipe to be used for data read or write through the CFIFO port. 0000: DCP 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A 1011: Pipe B 1100: Pipe C 1101: Pipe D 1110: Pipe E 1111: Pipe F To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing. Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.

Note: * Only reading 0 is enabled.

(2) D0FIFOSEL, D1FIFOSEL, D2FIFOSEL, D3FIFOSEL

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	RCNT	REW	DCLRM	DREQE	MBW[1:0]		—	—	DEZPM	—	—	—	CURPIPO[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	RCNT	0	R/W	Read Count Mode Specifies read mode of the DTLN bits in DnFIFOCTR. 0: Clears the DTLN bits after reading all receive data in the DnFIFO (or after reading receive data of one side of the double buffer). 1: Counts down the DTLN bits at each reading of DnFIFO receive data. When making an access to the DnFIFO with the BFRE bit set to 1, set this bit to 0.
14	REW	0	R/W*	Buffer Pointer Rewind Specifies whether to rewind the buffer pointer or not. 0: The buffer pointer is not rewound. 1: The buffer pointer is rewound. When the selected pipe is in the receive direction and this bit is set to 1 during FIFO buffer reading, the FIFO buffer can be read from the first data. (In the case of a double buffer, the first data of one side that is being read can be read again.) Do not set this bit to 1 concurrently with the CURPIPE setting change. Be sure to confirm that the FRDY bit is 1 when setting this bit to 1. When making an access to the DnFIFO with the BFRE bit set to 1, do not set this bit to 1 when the short packet data is completely read. To rewrite the FIFO buffer data from the first data for a pipe in the transmit direction, use the BCLR bit.
13	DCLRM	0	R/W	Buffer Memory Auto-Clear Mode after Reading Data of Selected Pipe Enables or disables buffer memory auto-clear mode after reading data of the selected pipe. 0: Buffer memory auto-clear mode is disabled. 1: Buffer memory auto-clear mode is enabled. When this bit is 1 and a Zero-Length packet is received while the FIFO buffer allocated to the selected pipe is empty or when a short packet is received with the BFRE bit set to 1 and the packet data is completely read, this module performs buffer clear (BCLR = 1 processing) of the FIFO buffer. When using this module with the BRDYM bit set to 1, be sure to set this bit to 0.
12	DREQE	0	R/W	DMA Transfer Request Enable Enables or disables making a DMA transfer request. 0: DMA transfer request is disabled. 1: DMA transfer request is enabled. To enable a DMA transfer request, set the CURPIPE bits and then set this bit to 1. Set this bit to 0 before changing the CURPIPE setting.

Bit	Bit Name	Initial Value	R/W	Description
11, 10	MBW[1:0]	00	R/W	FIFO Port Access Bit Width Specify the bit width for accesses to the DnFIFO port. 00: 8 bits 01: 16 bits 10: 32 bits 11: Setting prohibited When the selected pipe is in the receive direction and data read is started after these bits are set, do not change these bits until all data is completely read. When the selected pipe is in the receive direction, set the CURPIPE and MBW bits at the same time. When the selected pipe is in the transmit direction, no bit width can be changed (from 8 bits to 16/32 bits or from 16 bits to 32 bits) during data write to the buffer memory. When 8-bit width or 16-bit width is selected, data of odd bytes can also be written by controlling the byte access.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
7	DEZPM	0	R/W	DEZPM: Zero-Length Packet Addition Mode If the DMA transfer size that is set for the USBHS-DMAC modules is an integral multiple of the maximum packet size, a null packet is added after all of the data has been sent. 0: Disables addition of packets. 1: Enables addition of packets. This bit is applied to pipes used to write to the FIFO buffer. DEZPM must be set before starting DMA transfers. If the DEZPM bit is set after DMA transfers complete, no null packets are added. Note: This mode depends on the buffer size (PIPEBUF.BUFSIZE[4:0]). A null packet is added after transferring data up to buffer size which is defined by PIPEBUF.BUFSIZE[4:0]. When transfer data size is over 2Kbytes, this mode must not be used because max size of buffer is 2Kbytes. In that case, please add the null packet by SW with BVAL bit of FIFO Port Control Registers.
6 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

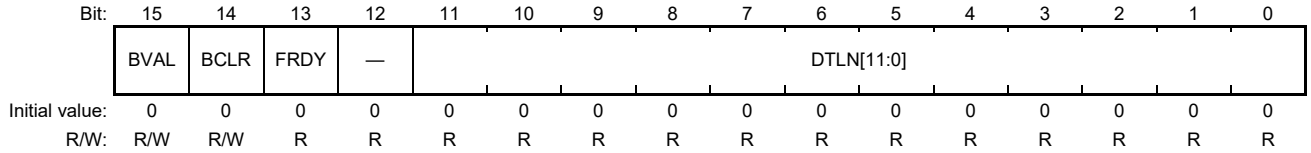
Bit	Bit Name	Initial Value	R/W	Description
3 to 0	CURPIPE [3:0]	0000	R/W	FIFO Port Access Pipe Select Set the number of pipe to be used for data read or write through the DnFIFO ports. 0000: No pipe 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A 1011: Pipe B 1100: Pipe C 1101: Pipe D 1110: Pipe E 1111: Pipe F To change these bits, write a value in these bits, read the value of these bits, confirm that the write value equals the read value, and then proceed with the next processing. Do not write the same pipe number in the CURPIPE bits in CFIFOSEL, DnFIFOSEL (n = 0 to 3). If these bits are changed in the middle of access to the FIFO buffer, accesses made before that time are retained, the value of these bits is rewritten, and then further access is enabled.

Note: * Only reading 0 is enabled.

42.2.8 FIFO Port Control Registers (CFIFOCTR, D0FIFOCTR, D1FIFOCTR, D2FIFOCTR, D3FIFOCTR)

CFIFOCTR and D0FIFOCTR, D1FIFOCTR, D2FIFOCTR and D3FIFIOCTR specify buffer memory write end and CPU buffer clear, as well as indicate whether the FIFO port is accessible or not. These registers correspond to each FIFO port.

These registers are initialized by a power-on reset.



Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BVAL	BCLR	FRDY	—	DTLN[11:0]											
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	BVAL	0	R/W*1	Buffer Memory Enable Flag This flag is set to 1 upon completion of data write in the FIFO buffer of the CPU of the pipe selected by the CURPIPE bits. 0: Invalid 1: Write end When the selected pipe is in the transmit direction, set this bit to 1 in the following cases. This module sets the FIFO buffer of the CPU to the SIE side to enable data transmission. To send a short packet, set this bit to 1 upon completion of data write. To send a Zero-Length packet, set this bit to 1 before writing data to the FIFO buffer. For pipes of continuous transfer mode, set this bit to 1 after writing data that is a positive integer multiple of MaxPacketSize and less than the BufferSize value. When data with the size specified by MaxPacketSize is written to a pipe of continuous transfer mode, this module writes 1 in this bit and sets the FIFO buffer of the CPU to the SIE side to enable data transmission. Set this bit to 1 when this module shows FRDY = 1. When the selected pipe is in the receive direction, do not set this bit to 1.
14	BCLR	0	R/W*2	CPU buffer clear Clears the CPU side FIFO buffer of the selected pipe. 0: Invalid 1: Clears the CPU side FIFO buffer. When the FIFO buffer assigned to the selected pipe is set to a double buffer, and even when both sides of the buffer are readable, this module clears only one side of the FIFO buffer. When the selected pipe is DCP, this module clears the FIFO buffer when this bit is set to 1 irrespective of whether the FIFO buffer is on the CPU side or SIE side. When clearing the SIE side FIFO buffer, be sure to set the PID bits in DCP to NAK and then set the BCLR bit to 1. When the selected pipe is in the transmit direction, and if 1 is written in the BVAL and BCLR bits at the same time, this module clears the previously written data, and makes a Zero-Length packet transmittable. When the selected pipe is not DCP, write 1 in this bit while the FRDY flag indicates 1.

Bit	Bit Name	Initial Value	R/W	Description
13	FRDY	0	R	FIFO Port Ready Indicates whether the CPU (DMAC) can access the FIFO port. 0: The FIFO port is not accessible. 1: The FIFO port is accessible. This module indicates FRDY = 1 in the following cases. However, since there is no data to read, no data can be read from the FIFO port. In these cases, set the BCLR bit to 1 to clear the FIFO buffer to make transmission/reception of the next data available. When a Zero-Length packet is received with the FIFO buffer assigned to the selected pipe empty When a short packet is received with BFRE set to 1 and the packet data is completely read
12	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
11 to 0	DTLN[11:0]	H'000	R	Receive Data Length Indicate the receive data length. The value of these bits during FIFO buffer reading varies as follows depending on the setting of the RCNT bit. When RCNT = 0: This module indicates the receive data length with these bits until the CPU (DMAC) finishes reading one side of the FIFO buffer. When BFRE is 1, this module retains the receive data length until the BCLR bit is set to 1 after the FIFO buffer read is completed. When RCNT = 1: This module decrements the value of the DTLN bits in each read cycle (-1 when MBW = 0, and -2 when MBW = 1) When reading out from a single FIFO buffer is complete, DTLN = 0 for this module. However, the behavior is different when double-buffering has been specified. If reading out of data from one side is not finished before the other side is full of received data, when all data have been read out from the first side, the DTLN bits reflect the amount of data received in the other side. When reading these bits during FIFO buffer reading while the RCNT bit is 1, note that this module updates the value in these bits within 150 ns after each FIFO port read cycle.

Notes: 1. Only writing 1 is enabled.
2. Only reading 0 and writing 1 are enabled.

42.2.9 Interrupt Enable Register 0 (INTENB0)

INTENB0 specifies masking of each interrupt when selection for function controller. When this module detects an interrupt for which 1 is written in the corresponding bit in this register by the software, this module generates a USB interrupt.

When interrupt source detection conditions are satisfied irrespective of the register setting (interrupt enable/disable), this module sets the corresponding status bit in INTSTS0.

When the software changes an interrupt enable bit (0 to 1) whose interrupt source status bit in INTSTS0 is set to 1, this module generates a USB interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBSE	RSME	SOFE	DVSE	CTRE	BEMPE	NRDYE	BRDYE	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBSE	0	R/W	VBUS_0 and VBUSIN_0 Interrupt Enable Enables or disables USB interrupt outputs when the VBINT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	RSME	0	R/W	Resume Interrupt Enable Enables or disables USB interrupt outputs when the RESM interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	SOFE	0	R/W	Frame Number Update Interrupt Enable Enables or disables USB interrupt outputs when the SOFR interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	DVSE	0	R/W	Device State Transition Interrupt Enable Enables or disables USB interrupt outputs when the DVST interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	CTRE	0	R/W	Control Transfer Stage Transition Interrupt Enable Enables or disables USB interrupt outputs when the CTRT interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	BEMPE	0	R/W	Buffer Empty Interrupt Enable Enables or disables USB interrupt outputs when the BEMP interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
9	NRDYE	0	R/W	Buffer Not Ready Response Interrupt Enable Enables or disables USB interrupt outputs when the NRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	BRDYE	0	R/W	Buffer Ready Interrupt Enable Enables or disables USB interrupt outputs when the BRDY interrupt is detected. 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

42.2.10 BRDY Interrupt Enable Register (BRDYENB)

BRDYENB enables or disables the BRDY bit to be set to 1 when the BRDY interrupt of a pipe is detected.

When this module detects the BRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBRDY bit of the pipe in BRDYSTS and also sets the BRDY bit in INTSTS0 and generates the BRDY interrupt.

When one or more PIPEBRDY bits in BRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BRDYE	PIPEE BRDYE	PIPED BRDYE	PIPEC BRDYE	PIPEB BRDYE	PIPEA BRDYE	PIPE9 BRDYE	PIPE8 BRDYE	PIPE7 BRDYE	PIPE6 BRDYE	PIPE5 BRDYE	PIPE4 BRDYE	PIPE3 BRDYE	PIPE2 BRDYE	PIPE1 BRDYE	PIPE0 BRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BRDYE	0	R/W	Pipe F BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BRDYE	0	R/W	Pipe E BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BRDYE	0	R/W	Pipe D BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BRDYE	0	R/W	Pipe C BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BRDYE	0	R/W	Pipe B BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA BRDYE	0	R/W	Pipe A BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BRDYE	0	R/W	Pipe 9 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BRDYE	0	R/W	Pipe 8 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BRDYE	0	R/W	Pipe 7 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
6	PIPE6 BRDYE	0	R/W	Pipe 6 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 BRDYE	0	R/W	Pipe 5 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BRDYE	0	R/W	Pipe 4 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BRDYE	0	R/W	Pipe 3 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BRDYE	0	R/W	Pipe 2 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BRDYE	0	R/W	Pipe 1 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 BRDYE	0	R/W	Pipe 0 BRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

42.2.11 NRDY Interrupt Enable Register (NRDYENB)

NRDYENB enables or disables the NRDY bit to be set to 1 when the NRDY interrupt of a pipe is detected.

When this module detects the NRDY interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPENRDY bit of the pipe in NRDYSTS and also sets the NRDY bit in INTSTS0 and generates an NRDY interrupt.

When one or more PIPENRDY bits in NRDYSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates an NRDY interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF NRDYE	PIPEE NRDYE	PIPED NRDYE	PIPEC NRDYE	PIPEB NRDYE	PIPEA NRDYE	PIPE9 NRDYE	PIPE8 NRDYE	PIPE7 NRDYE	PIPE6 NRDYE	PIPE5 NRDYE	PIPE4 NRDYE	PIPE3 NRDYE	PIPE2 NRDYE	PIPE1 NRDYE	PIPE0 NRDYE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF NRDYE	0	R/W	Pipe F NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE NRDYE	0	R/W	Pipe E NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED NRDYE	0	R/W	Pipe D NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC NRDYE	0	R/W	Pipe C NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB NRDYE	0	R/W	Pipe B NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA NRDYE	0	R/W	Pipe A NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 NRDYE	0	R/W	Pipe 9 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 NRDYE	0	R/W	Pipe 8 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 NRDYE	0	R/W	Pipe 7 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
6	PIPE6 NRDYE	0	R/W	Pipe 6 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 NRDYE	0	R/W	Pipe 5 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 NRDYE	0	R/W	Pipe 4 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 NRDYE	0	R/W	Pipe 3 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 NRDYE	0	R/W	Pipe 2 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 NRDYE	0	R/W	Pipe 1 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 NRDYE	0	R/W	Pipe 0 NRDY Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

42.2.12 BEMP Interrupt Enable Register (BEMPENB)

BEMPENB enables or disables the BEMP bit to be set to 1 when the BEMP interrupt of a pipe is detected.

When this module detects the BEMP interrupt of a pipe for which the software sets the corresponding bit in this register to 1, this module sets the PIPEBEMP bit of the pipe in BEMPSTS and the BEMP bit in INTSTS0 and generates the BEMP interrupt.

When one or more PIPEBEMP bits in BEMPSTS are 1 and the software changes the corresponding interrupt enable bit(s) in this register from 0 to 1, this module generates the BEMP interrupt.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BEMPE	PIPEE BEMPE	PIPED BEMPE	PIPEC BEMPE	PIPEB BEMPE	PIPEA BEMPE	PIPE9 BEMPE	PIPE8 BEMPE	PIPE7 BEMPE	PIPE6 BEMPE	PIPE5 BEMPE	PIPE4 BEMPE	PIPE3 BEMPE	PIPE2 BEMPE	PIPE1 BEMPE	PIPE0 BEMPE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEF BEMPE	0	R/W	Pipe F BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
14	PIPEE BEMPE	0	R/W	Pipe E BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
13	PIPED BEMPE	0	R/W	Pipe D BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
12	PIPEC BEMPE	0	R/W	Pipe C BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
11	PIPEB BEMPE	0	R/W	Pipe B BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
10	PIPEA BEMPE	0	R/W	Pipe A BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
9	PIPE9 BEMPE	0	R/W	Pipe 9 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
8	PIPE8 BEMPE	0	R/W	Pipe 8 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
7	PIPE7 BEMPE	0	R/W	Pipe 7 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

Bit	Bit Name	Initial Value	R/W	Description
6	PIPE6 BEMPE	0	R/W	Pipe 6 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
5	PIPE5 BEMPE	0	R/W	Pipe 5 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
4	PIPE4 BEMPE	0	R/W	Pipe 4 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
3	PIPE3 BEMPE	0	R/W	Pipe 3 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
2	PIPE2 BEMPE	0	R/W	Pipe 2 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
1	PIPE1 BEMPE	0	R/W	Pipe 1 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.
0	PIPE0 BEMPE	0	R/W	Pipe 0 BEMP Interrupt Enable 0: Interrupt outputs are disabled. 1: Interrupt outputs are enabled.

42.2.13 SOF Output Configuration Register (SOFCFG)

SOFCFG specifies an effective period of transactions, the BRDY interrupt status clear timing, and others.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	BRDYM	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6	BRDYM	0	R/W	Status Clear Timing of Each Pipe BRDY Interrupt Specifies the timing to clear the BRDY interrupt status of each pipe. 0: The software clears the status. 1: This module clears the status by reading or writing the FIFO buffer.
5 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

42.2.14 Interrupt Status Register 0 (INTSTS0)

INTSTS0 can know the interrupt generation by referring to the register when the function controller is selected.

Please permit interrupt by the status change that each bit of this register shows only when you select the function.

This register is initialized by a power-on reset. The DVSQ2 to DVSQ0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	VBINT	RESM	SOFR	DVST	CTRT	BEMP	NRDY	BRDY	VBSTS	DVSQ[2:0]			VALID	CTSQ[2:0]		
Initial value:	0	0	0	0/1	0	0	0	0	0/1	0	0	0/1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R	R	R	R	R	R	R	R/W	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	VBINT	0	R/W*6	VBUS_0 and VBUSIN_0 Interrupt Status*4*5 0: No VBUS_0 and VBUSIN_0 interrupt is generated. 1: A VBUS_0 and VBUSIN_0 interrupt is generated. This bit indicates 1 when this module detects a change in the VBUS_0 and VBUSIN_0 pin input level (high to low or low to high level). This module indicates the VBUS_0 and VBUSIN_0 pin input value using the VBSTS bit. When a VBINT interrupt occurs, read the VBSTS bit several times by the software and confirm that the read value is equal each time to eliminate chattering.
14	RESM	0	R/W*6	Resume Interrupt Status*4*5 0: No resume interrupt is generated. 1: A resume interrupt is generated. This bit indicates 1 when this module detects a falling of the DP_0 pin level in the suspended state (DVSQ = 1XX) with the function controller function selected.
13	SOFR	0	R/W*6	Frame Number Update Interrupt Status*4 0: No SOF interrupt is generated. 1: An SOF interrupt is generated. This module indicates SOFR = 1 at the frame number update timing. (This interrupt is detected every millisecond.) Even when an SOF packet from the USB host is corrupted, this module detects an SOFR interrupt using the internal interpolation.
12	DVST	0/1*1	R/W*6	Device State Transition Interrupt Status*4 0: No device state transition interrupt is generated. 1: A device state transition interrupt is generated. When this module detects a change in device state, this module updates the DVSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next device state transition.
11	CTRT	0	R/W*6	Control Transfer Stage Transition Interrupt Status*4 0: No control transfer stage transition interrupt is generated. 1: A control transfer stage transition interrupt is generated. When this module detects a control transfer stage transition, this module updates the CTSQ value and set this bit to 1. When this interrupt occurred, clear the status before this module detects the next stage transition in control transfers.

Bit	Bit Name	Initial Value	R/W	Description
10	BEMP	0	R	Buffer Empty Interrupt Status 0: No BEMP interrupt is generated. 1: A BEMP interrupt is generated. This module indicates BEMP = 1 when at least one of the PIPEBEMP bits in BEMPSTS corresponding to the pipes for which 1 is set in the PIPEBEMPE bits in BEMPENB is set to 1 (when this module detects a BEMP interrupt of one or more pipes for which BEMP interrupts are enabled by the software). For PIPEBEMP status assertion conditions, see section 42.3.2 (3), BEMP Interrupt. When the software writes 0 to all PIPEBEMP bits corresponding to the pipes for which interrupts are enabled by the PIPEBEMPE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
9	NRDY	0	R	Buffer Not Ready Interrupt Status 0: No NRDY interrupt is generated. 1: An NRDY interrupt is generated. This module indicates NRDY = 1 when at least one of the PIPENRDY bits in NRDYSTS corresponding to the pipes for which 1 is set in the PIPENRDYE bits in NRDYENB is set to 1 (when this module detects an NRDY interrupt of one or more pipes for which NRDY interrupts are enabled by the software). For PIPENRDY status assertion conditions, see section 42.3.2 (2), NRDY Interrupt. When the software writes 0 to all PIPENRDY bits corresponding to the pipes for which interrupts are enabled by the PIPENRDYE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
8	BRDY	0	R	Buffer Ready Interrupt Status Indicates the BRDY interrupt status. 0: No BRDY interrupt is generated. 1: A BRDY interrupt is generated. This module indicates BRDY = 1 when at least one of the PIPEBRDY bits in BRDYSTS corresponding to the pipes for which 1 is set in the PIPEBRDYE bits in BRDYENB is set to 1 (when this module detects a BRDY interrupt of one or more pipes for which BRDY interrupts are enabled by the software). For PIPEBRDY status assertion conditions, see section 42.3.2 (1), BRDY Interrupt. When the software writes 0 to all PIPEBRDY bits corresponding to the pipes for which interrupts are enabled by the PIPEBRDYE bits, this module clears this bit to 0. This bit cannot be cleared to 0 by writing 0 by the software.
7	VBSTS	0/1*3	R	VBUS Input Status 0: The VBUS pin is low level. 1: The VBUS pin is high level.

Bit	Bit Name	Initial Value	R/W	Description
6 to 4	DVSQ[2:0]	000/001*2	R	Device State 000: Powered state 001: Default state 010: Address state 011: Configuration state 1xx: Suspended state
3	VALID	0	R/W*6	USB Request Receive 0: Not detected 1: A setup packet is received.
2 to 0	CTSQ[2:0]	000	R	Control Transfer Stage 000: Idle stage or setup stage 001: Control read data stage 010: Control read status stage 011: Control write data stage 100: Control write status stage 101: Control write (NoData) status stage 110: Control transfer sequence error 111: Setting prohibited

Notes: 1. The initial value is B'0 after a power-on reset, and B'1 after a USB bus reset.
2. The initial value is B'000 after a power-on reset, and B'001 after a USB bus reset.
3. The initial value is 1 when the VBUS pin is high level, and is 0 when the VBUS pin is low level.
4. To clear the VBINT, RESM, SOFR, DVST, or CTRT bit, write 0 only to bits to be cleared and write 1 to the other bits. Do not write 0 to status bits that indicate 0.
5. When a status change shown in the VBINT or RESM bit is detected while the clock is halted (SUSPM = 0) and the corresponding interrupt is enabled, the interrupt is output. Clear the interrupt status of these bits by the software after the clock is enabled.
6. Only writing 0 is enabled.

42.2.15 BRDY Interrupt Status Register (BRDYSTS)

BRDYSTS indicates the BRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BRDY	PIPEE BRDY	PIPED BRDY	PIPEC BRDY	PIPEB BRDY	PIPEA BRDY	PIPE9 BRDY	PIPE8 BRDY	PIPE7 BRDY	PIPE6 BRDY	PIPE5 BRDY	PIPE4 BRDY	PIPE3 BRDY	PIPE2 BRDY	PIPE1 BRDY	PIPE0 BRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBRDY	0	R/W*1	Pipe F BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBRDY	0	R/W*1	Pipe E BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBRDY	0	R/W*1	Pipe D BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBRDY	0	R/W*1	Pipe C BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBRDY	0	R/W*1	Pipe B BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABRDY	0	R/W*1	Pipe A BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BRDY	0	R/W*1	Pipe 9 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BRDY	0	R/W*1	Pipe 8 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BRDY	0	R/W*1	Pipe 7 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BRDY	0	R/W*1	Pipe 6 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BRDY	0	R/W*1	Pipe 5 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
4	PIPE4BRDY	0	R/W*1	Pipe 4 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3BRDY	0	R/W*1	Pipe 3 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BRDY	0	R/W*1	Pipe 2 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BRDY	0	R/W*1	Pipe 1 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BRDY	0	R/W*1	Pipe 0 BRDY Interrupt Status*2 0: No interrupt is generated. 1: An interrupt is generated.

Notes: 1. To clear the status of each bit in this register when BRDYM is 0, write 0 only to bits to be cleared and write 1 to the other bits.
2. When BRDYM is 0, be sure to clear this interrupt before making an access to the FIFO.

42.2.16 NRDY Interrupt Status Register (NRDYSTS)

NRDYSTS indicates the NRDY interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF NRDY	PIPEE NRDY	PIPED NRDY	PIPEC NRDY	PIPEB NRDY	PIPEA NRDY	PIPE9 NRDY	PIPE8 NRDY	PIPE7 NRDY	PIPE6 NRDY	PIPE5 NRDY	PIPE4 NRDY	PIPE3 NRDY	PIPE2 NRDY	PIPE1 NRDY	PIPE0 NRDY
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFNRDY	0	R/W*	Pipe F NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEENRDY	0	R/W*	Pipe E NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDNRDY	0	R/W*	Pipe D NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECNRDY	0	R/W*	Pipe C NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBNRDY	0	R/W*	Pipe B NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEANRDY	0	R/W*	Pipe A NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9NRDY	0	R/W*	Pipe 9 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8NRDY	0	R/W*	Pipe 8 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7NRDY	0	R/W*	Pipe 7 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6NRDY	0	R/W*	Pipe 6 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5NRDY	0	R/W*	Pipe 5 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
4	PIPE4NRDY	0	R/W*	Pipe 4 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3NRDY	0	R/W*	Pipe 3 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2NRDY	0	R/W*	Pipe 2 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1NRDY	0	R/W*	Pipe 1 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0NRDY	0	R/W*	Pipe 0 NRDY Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: * To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

42.2.17 BEMP Interrupt Status Register (BEMPSTS)

BEMPSTS indicates the BEMP interrupt status of each pipe.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	PIPEF BEMP	PIPEE BEMP	PIPED BEMP	PIPEC BEMP	PIPEB BEMP	PIPEA BEMP	PIPE9 BEMP	PIPE8 BEMP	PIPE7 BEMP	PIPE6 BEMP	PIPE5 BEMP	PIPE4 BEMP	PIPE3 BEMP	PIPE2 BEMP	PIPE1 BEMP	PIPE0 BEMP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	PIPEFBEMP	0	R/W*	Pipe F BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
14	PIPEEBEMP	0	R/W*	Pipe E BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
13	PIPEDBEMP	0	R/W*	Pipe D BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
12	PIPECBEMP	0	R/W*	Pipe C BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
11	PIPEBBEMP	0	R/W*	Pipe B BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
10	PIPEABEMP	0	R/W*	Pipe A BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
9	PIPE9BEMP	0	R/W*	Pipe 9 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
8	PIPE8BEMP	0	R/W*	Pipe 8 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
7	PIPE7BEMP	0	R/W*	Pipe 7 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
6	PIPE6BEMP	0	R/W*	Pipe 6 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
5	PIPE5BEMP	0	R/W*	Pipe 5 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Bit	Bit Name	Initial Value	R/W	Description
4	PIPE4BEMP	0	R/W*	Pipe 4 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
3	PIPE3BEMP	0	R/W*	Pipe 3 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
2	PIPE2BEMP	0	R/W*	Pipe 2 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
1	PIPE1BEMP	0	R/W*	Pipe 1 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.
0	PIPE0BEMP	0	R/W*	Pipe 0 BEMP Interrupt Status 0: No interrupt is generated. 1: An interrupt is generated.

Note: * To clear the status of each bit in this register, write 0 only to bits to be cleared and write 1 to the other bits.

42.2.18 Frame Number Register (FRMNUM)

FRMNUM indicates the sources of isochronous errors and a frame number.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	OVRN	CRCE	—	—	—	FRNM[10:0]										
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

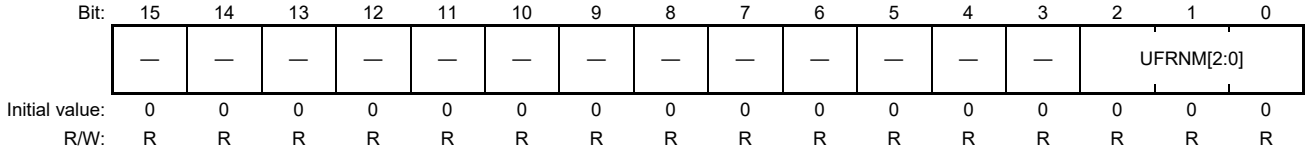
Bit	Bit Name	Initial Value	R/W	Description
15	OVRN	0	R/W*	Overrun/Underrun Detect Status Indicates whether an overrun or underrun error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. This module indicates OVRN = 1 in any of the following cases. When the IN token is received when transmit data write to the FIFO buffer is not completed in a transmit direction pipe of isochronous transfer type When the OUT token is received with no side of the FIFO buffer empty in a receive direction pipe of isochronous transfer type
14	CRCE	0	R/W*	Receive Data Error Indicates whether a CRC error or bit stuffing error is detected or not in a pipe that is performing isochronous transfer. 0: No error is detected. 1: An error is detected. Writing 0 to this bit by the software clears this bit to 0. At this time, write 1 to the other bits in this register. When a CRC error is detected, this module does not generate an internal NRDY interrupt request.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	FRNM [10:0]	H'000	R	Frame Number This module modifies this bit when an SOF is received and indicates the latest frame number. Read these bits twice and confirm that the read value is equal each time.

Note: * Only writing 0 is enabled.

42.2.19 μ Frame Number Register (UFRMNUM)

UFRMNUM indicates a μ frame number.

This register is initialized by a power-on reset.

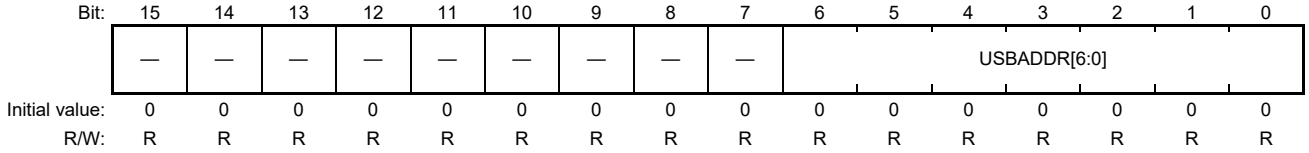


Bit	Bit Name	Initial Value	R/W	Description
15 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	UFRNM[2:0]	000	R	μ Frame Indicate a μ frame number. In high-speed operating mode, these bits indicate a μ frame number. In other operating modes, these bits indicate B'000. Read these bits twice and confirm that the read value is equal each time.

42.2.20 USB Address Register (USBADDR)

USBADDR indicates a USB address.

This register is initialized by a power-on reset or USB bus reset.



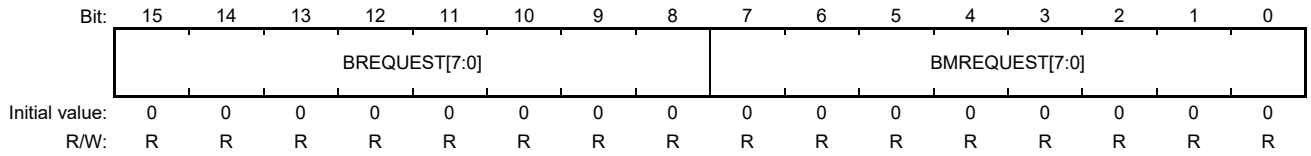
Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	USBADDR[6:0]	H'00	R	USB Address Indicate the USB address allocated by the host when the SET_ADRESS request is successfully processed. When this module detects a USB reset, these bits indicate H'00.

42.2.21 USB Request Type Register (USBREQ)

USBREQ stores the setup request for control transfers.

USBREQ stores the values of received bRequest and bmRequestType.

This register is initialized by a power-on reset or USB bus reset.

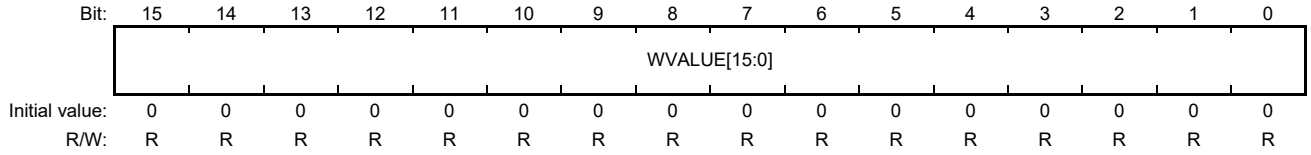


Bit	Bit Name	Initial Value	R/W	Description
15 to 8	BREQUEST [7:0]	H'00	R	Request Store the value of USB request bRequest. Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.
7 to 0	BMREQUEST TYPE[7:0]	H'00	R	Request Type Store the value of USB request bmRequestType. Indicate the USB request data received in the SETUP transaction. These bits cannot be modified.

42.2.22 USB Request Value Register (USBVAL)

USBVAL stores the value of received wValue.

This register is initialized by a power-on reset or USB bus reset.



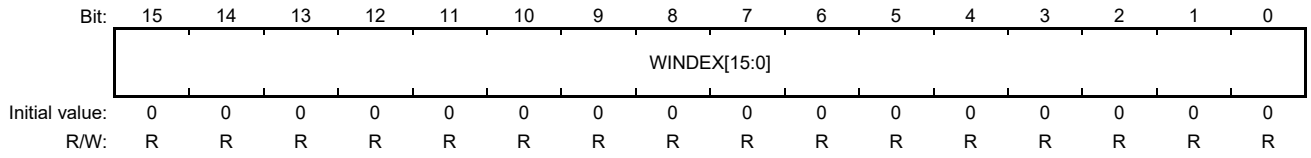
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WVALUE [15:0]	H'0000	R	Value Store the value of USB request wValue. Indicate the value of USB request wValue received in the SETUP transaction. These bits cannot be modified.

42.2.23 USB Request Index Register (USBINDX)

USBINDX stores the setup request for control transfers.

USBINDX stores the value of received wIndex.

This register is initialized by a power-on reset or USB bus reset.



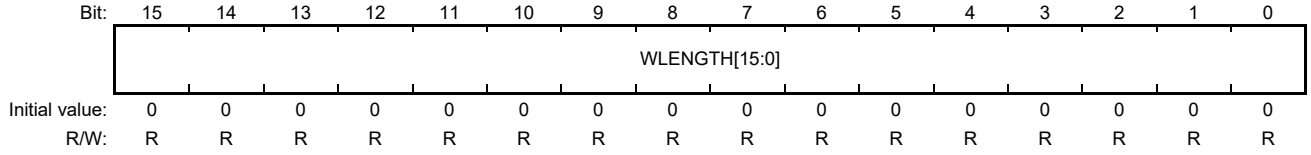
Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WINDEX [15:0]	H'0000	R	Index Store the value of USB request wIndex. Indicate the value of USB request wIndex received in the SETUP transaction. These bits cannot be modified.

42.2.24 USB Request Length Register (USBLENG)

USBLENG stores the setup request of control transfers.

USBLENG stores the value of received wLength.

This register is initialized by a power-on reset or USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	WLENGTH [15:0]	H'0000	R	Length Store the value of USB request wLength. Indicate the value of USB request wLength received in the SETUP transaction. These bits cannot be modified.

42.2.25 DCP Maximum Packet Size Register (DCPMAXP)

DCPMAXP specifies the maximum packet size of the DCP.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	MXPS[6:0]						
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6 to 0	MXPS [6:0]	H'40	R/W	Maximum Packet Size Set the payload of DCP data (maximum DCP packet size) in these bits. The initial value of these bits is H'40 (64 bytes). Set a value in the MXPS bits based on the USB Specification. Set the MXPS bits when PID = NAK, and the CURPIPE bits are not set. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS bits are 0 or set the PID bits to BUF.

42.2.26 DCP Control Register (DCPCTR)

DCPCTR is used to monitor the buffer memory status, change/check the data PID sequence bit, and set the response PID for a DCP.

This register is initialized by a power-on reset. The PID2 to PID0 bits in CCPL are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	—	—	—	—	—	SQCLR	SQSET	SQMON	PBUSY	—	—	CCPL	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	1	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates whether the DCP FIFO buffer is accessible or not. 0: The buffer is not accessible. 1: The buffer is accessible. This bit indicates as follows depending on the ISEL value. When ISEL = 0, this bit indicates whether the buffer is ready to read receive data. When ISEL = 1, this bit indicates whether the buffer is ready to write transmit data.
14 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	SQCLR	0	R/W*	Toggle Bit Clear The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA0. 0: Invalid 1: The expected value is set in DATA0. This bit always indicates 0. Do not set the SQCLR and SQSET bits to 1 at the same time. Set this bit to 1 when PID = NAK, and the CURPIPE bits are not set. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
7	SQSET	0	R/W*	Toggle Bit Set The expected value of the sequence toggle bit for the next transaction in DCP transfer can be set in DATA1. 0: Invalid 1: The expected value is set in DATA1. Do not set the SQCLR and SQSET bits to 1 at the same time. Set this bit to 1 when PID = NAK, and the CURPIPE bits are not set. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
6	SQMON	1	R	Sequence Toggle Bit Monitor Indicates the expected value of the sequence toggle bit for the next transaction in DCP transfer. 0: DATA0 1: DATA1 When the transaction is successfully completed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled. When the function controller function is selected, this module sets this bit to 1 (sets the expected value in DATA1) when the setup packet is successfully received. When the function controller function is selected, this module does not read this bit in IN transactions or OUT transactions in the status stage.
5	PBUSY	0	R	Pipe Busy Indicates whether the DCP communication state is shifted to the NAK state or not when the DCP changed the PID bits from BUF to NAK. 0: Transition to the NAC state is not completed. 1: Transition to the NAC state is completed. When this module starts the USB transaction for the corresponding pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to check whether changing the pipe setting is enabled or not.
4, 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	CCPL	0	R/W*	Control Transfer End Enable 0: Invalid 1: The control transfer end is enabled. When the software sets this bit to 1 while the corresponding PID bits are set to BUF, this module finishes the control transfer stage. That is, this module sends an ACK handshake in response to OUT transactions from the USB host in the control read transfer, and sends a Zero-Length packet in response to IN transactions from the USB host in control write and no-data control transfers. However, a SET_ADDRESS request is detected, this module automatically sends responses from the SETUP stage until the end of the status stage irrespective of the setting of this bit. When this module receives the next setup packet, this module clears this bit to 0. When VALID = 1, the software cannot write 1 to this bit.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Control responses of this module in control transfers. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response This module modifies these bits in the following cases. This module changes these bits to NAK upon receiving a SETUP packet. At this time, this module indicates VALID = 1. The software cannot modify these bits until the software sets VALID = 0. When this module receives data with a size exceeding the MaxPacketSize value while these bits are set to BUF by the software, this module indicates PID = STALL (11). When this module detects a control transfer sequence error, this module indicates PID = STALL (1x). When this module detects a USB bus reset, this module indicates PID = NAK. This module does not read the value of these bits during the SET_ADDRESS request processing (auto processing).

Note: * These bits are always read as 0. Only writing 1 is enabled.

42.2.27 Pipe Window Select Register (PIPESEL)

Make settings for pipes 1 to F using PIPESEL, PIPECFG, PIPEBUF, PIPEMAXP, PIPEPERI, PIPEnCTR, PIPEnTRE, and PIPEnTRN.

Specify a pipe to be used with PIPESEL, and then make function settings for each pipe in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI. The PIPEnCTR, PIPEnTRE, and PIPEnTRN registers can be set independently from pipe selection using PIPESEL.

Not only the selected pipe but also the corresponding bits in registers for all pipes are initialized by a power-on reset or USB bus reset.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	PIPESEL[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 4	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
3 to 0	PIPESEL [3:0]	0000	R/W	Pipe Window Select Specify a pipe number corresponding to PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI to be read or written. 0000: No pipe is selected. 0001: Pipe 1 0010: Pipe 2 0011: Pipe 3 0100: Pipe 4 0101: Pipe 5 0110: Pipe 6 0111: Pipe 7 1000: Pipe 8 1001: Pipe 9 1010: Pipe A 1011: Pipe B 1100: Pipe C 1101: Pipe D 1110: Pipe E 1111: Pipe F PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI corresponding to the pipe number specified by these bits can be read and written. When these bits are set to B'0000, all bits in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI are read as 0 and cannot be modified.

42.2.28 Pipe Configuration Register (PIPECFG)

PIPECFG specifies the transfer type, buffer memory access direction, and endpoint number for pipes 1 to F, selects continuous transfer mode or discontinuous transfer mode, and single buffer or double buffer, and also specifies whether to disable the operation of each pipe when data transfer finishes.

This register is initialized by a power-on reset. The TYPE1 and TYPE0 bits are also initialized by a USB bus reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TYPE[1:0]		—	—	—	BFRE	DBLB	CNTMD	SHTNAK	—	—	DIR	EPNUM[3:0]			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R	R	R	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15, 14	TYPE[1:0]	00	R/W	Transfer Type Select the transfer type of the pipe specified by the PIPESEL bits (selected pipe). Pipes 1 and 2 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Isochronous transfer Pipes 3 to 5, B to F 00: No pipe is used. 01: Bulk transfer 10: Setting prohibited 11: Setting prohibited Pipes 6 to 8 00: No pipe is used. 01: Setting prohibited 10: Interrupt transfer 11: Setting prohibited Pipes 9 and A 00: No pipe is used. 01: Setting prohibited 10: Interrupt transfer 11: Setting prohibited Before setting the selected pipe for PID = BUF (before starting USB communication using the selected pipe), be sure to set these bits to a value other than B'00. Modify these bits when the PID bits of the selected pipe are set to NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	BFRE	0	R/W	BRDY Interrupt Operation Specifies the BRDY interrupt output timing from this module to the CPU for the selected pipe. 0: At a BRDY interrupt timing during data transmission or reception 1: At a BRDY interrupt timing after reading data When this bit is set to 1 by the software and the selected pipe is used in the receive direction, this module detects the transfer end and outputs a BRDY interrupt when the packet is completely read. When a BRDY interrupt occurs with this setting, the software must set BCLR = 1. Unless BCLR = 1 is set, the FIFO buffer allocated to the selected pipe does not enter the receive ready state. When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt. For details, see section 42.3.2 (1), BRDY Interrupt. Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
9	DBLB	0	R/W	Double Buffer Mode Specifies a single buffer or double buffer for the FIFO buffer used in the selected pipe. 0: Single buffer 1: Double buffer This bit is valid when pipes 1 to 5, 9 to F are selected. When this bit is set to 1 by the software, this module allocates the FIFO buffer size specified by the BUFSIZE bits in PIPEBUF to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) × 64 × (DBLB + 1) [bytes] When this bit is set to 1 by the software and the selected pipe is used in the transmit direction, this module generates no BRDY interrupt. For details, see section 42.3.2 (1), BRDY Interrupt. Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

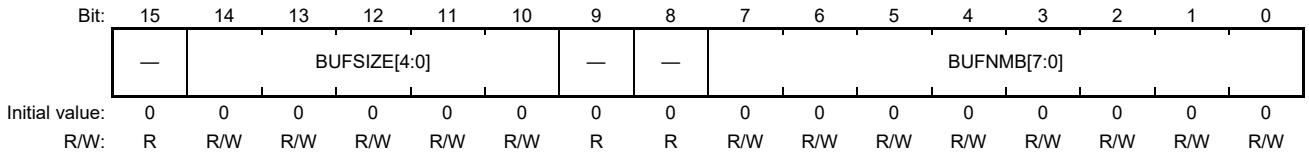
Bit	Bit Name	Initial Value	R/W	Description
8	CNTMD	0	R/W	Continuous Transfer Mode Selects continuous transfer mode or discontinuous transfer mode to be used in communication for the selected pipe. 0: Discontinuous transfer mode 1: Continuous transfer mode This bit is valid when pipes 1 to 5, 9 to F are selected by the PIPESEL bits and bulk transfer is selected (TYPE = 01). Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
7	SHTNAK	0	R/W	Pipe Disable at the Time of Transfer End Specifies whether to change the setting of the PID bits to NAK at the end of transfer when the selected pipe is in the receive direction. 0: The pipe is continued at the end of transfer. 1: The pipe is disabled at the end of transfer. This bit is valid when the selected pipe is either of pipes 1 to 5, 9 to F and is in the receive direction. When the software sets this bit to 1 for a receive direction pipe, this module changes the setting of the PID bits corresponding to the selected pipe to NAK for the selected pipe when this module determines the transfer end. When the following conditions are satisfied, this module determines the transfer end. When short packet data (including a Zero-Length packet) is correctly received. When the transaction counter is used and packets with a size of the transaction counter are correctly received. Modify this bit when PID = NAK. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. For transmit direction pipes, set this bit to 0.
6, 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
4	DIR	0	R/W	Transfer Direction Selects the transfer direction of the selected pipe. 0: Receive direction 1: Transmit direction When this bit is set to 0 by the software, this module uses the selected pipe in the receive direction. When this bit is set to 1, this module uses the selected pipe in the transmit direction. Modify this bit when PID = NAK, and no pipe number is specified by the CURPIPE bits. Furthermore, when changing the setting of this bit after USB communication using the selected pipe, set the ACLRM bit to 1 and clear it to 0 continuously by the software to clear the FIFO buffer allocated to the selected pipe, in addition to the three register states above. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
3 to 0	EPNUM [3:0]	0000	R/W	Endpoint Number Specify the endpoint number of the selected pipe. The setting of B'0000 means an unused pipe. Modify these bits when PID = NAK. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Set these bits so that the combination of the DIR setting and the EPNUM setting does not overlap the setting of other pipes (EPNUM = B'0000 is allowed in this case.)

42.2.29 Pipe Buffer Register (PIPEBUF)

PIPEBUF specifies the buffer size and buffer number for pipes 1 to F.

This register is initialized by a power-on reset.



Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14 to 10	BUFSIZE [4:0]	H'00	R/W	Buffer Size Specify the buffer size of the pipe specified by the PIPESEL bits (selected pipe) in units of blocks. One block is 64 bytes. 00000 (H'00): 64 bytes 00001 (H'01): 128 bytes : 11111 (H'1F): 2 Kbytes When DBLB = 1 is set by the software, this module allocates the FIFO buffer size specified by these bits to the selected pipe for two sides. Thus the size of the FIFO buffer that this module allocates to the selected pipe is as follows: (BUFSIZE + 1) × 64 × (DBLB + 1) [bytes] A value that can be set in these bits varies depending on pipes selected. For pipes 1 to 5, 9 to F: Set BUFSIZE to H'00 to H'1F. For pipes 6 to 8: Set BUFSIZE to H'00. When using the buffer with CNTMD = 1, set a value in multiples of MaxPacketSize in these bits. Modify these bits when PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
9, 8	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
7 to 0	BUFNMB [7:0]	H'00	R/W	Buffer Number Specify the FIFO buffer number of the selected pipe with a value from H'04 to H'FF. When the selected pipe is either of pipes 1 to 5, 9 to F, these bits can be set to a value according to user systems. Set BUFNMB to H'06 to H'4F. BUFNMB = 0 to 3 are for DCP only. BUFNMB = 4 is for pipe 6 only. However, when pipe 6 is not used, this is available for other pipes. When pipe 6 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 4. BUFNMB = 5 is for pipe 7 only. However, when pipe 7 is not used, this is available for other pipes. When pipe 7 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 5. BUFNMB = 6 is for pipe 8 only. However, when pipe 8 is not used, this is available for other pipes. When pipe 8 is selected, these bits cannot be modified and this module automatically allocates BUFNMB = 6. Modify these bits when PID = NAK, and no pipe number is set in the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

42.2.30 Pipe Maximum Packet Size Register (PIPEMAXP)

PIPEMAXP specifies the maximum packet size for pipes 1 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	MXPS[10:0]										
Initial value:	0	0	0	0	0	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
10 to 0	MXPS[10:0]	*	R/W	Maximum Packet Size Specify the payload of data (maximum packet size) of the selected pipe. The settable value range for each pipe is as follows: Pipes 1 and 2: 1 byte (H'001) to 1024 bytes (H'400) Pipes 3 to 5, 9 to F: 8 (H'008), 16 (H'010), 32 (H'020), 64 (H'040), or 512 bytes (H'200) (MXPS2 to MXPS0 bits are not provided.) Pipes 6 to 8: 1 byte (H'001) to 64 bytes (H'040) Set a value in the MXPS bits based on the USB Specification for each transfer type. To transmit an isochronous pipe in split transactions, set a value of 188 bytes or less in the MXPS bits. When changing the setting of this bit after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Do not write the FIFO buffer when the MXPS = 0 or set the PID bits to BUF.

Note: * The initial value is H'000 (when no pipe is selected by the PIPESEL bits in PIPESEL) or H'040 (when a pipe is selected).

42.2.31 Pipe Cycle Control Register (PIPEPERI)

PIPEPERI specifies whether to activate the buffer flush function or not at the time of an interval error during the isochronous IN transfer, and also specifies the interval error detection interval for pipes 1 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	IFIS	—	—	—	—	—	—	—	—	—	IITV[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R/W	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	IFIS	0	R/W	Isochronous IN Buffer Flush Specifies whether to flush the FIFO buffer when the pipe specified by the PIPESEL bits (selected pipe) is isochronous IN transfer type. 0: The FIFO buffer is not flushed. 1: The FIFO buffer is flushed. Buffer flush is a function that this module automatically clears the FIFO buffer when this module does not receive IN-Token from the USB host in a (μ) frame for each interval specified in the IITV bits when the function controller function is selected and the selected pipe is isochronous IN transfer type. When double buffer is selected (DBLB = 1), this module clears data of only the older side. The FIFO buffer is cleared when an SOF packet is received immediately after the (μ) frame where IN-Token is to be received. Even if the SOF packet is corrupted, the FIFO buffer is cleared at the time when the SOF packet is to be received using the internal interpolation. When the selected pipe is not isochronous transfer type, set this bit to 0.
11 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2 to 0	IITV[2:0]	000	R/W	Interval Error Detection Interval Specify the interval error detection interval of the selected pipe with a value of 2's n-th power of the frame timing. Set these bits when PID = NAK, and no pipe number is specified by the CURPIPE bits. When changing the setting of these bits after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. To change the setting of these bits after USB communication, set PID = NAK and then set ACLRM = 1 to initialize the interval timer. These bits are not provided for pipes 3 to F. Set B'000 in the position of these bits corresponding to pipes 3 to F.

42.2.32 Pipe n Control Register (PIPEnCTR) (n = 1 to F)

PIPEnCTR monitors the buffer memory status, changes/checks the data PID sequence bits, selects whether to use auto-response mode and buffer auto-clear mode, and specifies a response PID for pipes 1 to F. This register can be set independently of the pipe selection using PIPESEL.

This register is initialized by a power-on reset. The PID1 and PID0 bits are also initialized by a USB bus reset.

(1) PIPEnCTR (n = 1 to 5, 9 to F)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	INBUFM	—	—	—	ATREPM	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates the FIFO buffer status of the pipe. 0: The buffer is not accessible from the CPU. 1: The buffer is accessible from the CPU. The meaning of this bit differs depending on the settings of the DIR, BFRE, and DCLRM bits as shown in Table 42.8.
14	INBUFM	0	R	Transmit Buffer Monitor Indicates the FIFO buffer status of the selected pipe in the transmit direction. 0: The buffer memory contains no transmittable data. 1: The buffer memory contains transmittable data. When transmit direction (DIR = 1) is set for the pipe, this module sets this bit to 1 when the software (or DMAC) finishes writing data to the FIFO buffer for at least one register set. When this module finishes sending all data on the register set (writing is completed) of the FIFO buffer, this bit indicates 0. In the case of a double buffer (DBLB = 1), when this module finishes sending all data on both register sets and the software (or DMAC) has not completed writing of data for one register set, this bit indicates 0. When receive direction (DIR = 0) is set for the selected pipe, this bit indicates the same value as the BSTS bit.
13 to 11	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
10	ATREPM	0	R/W	Auto-Response Mode Enables or disables auto-response for the selected pipe. 0: Auto-response is disabled. 1: Auto-response is enabled. When the transfer type of the selected pipe is set to bulk transfer, this bit can be set to 1. When this bit is 1, this module sends responses to tokens from the USB host as follows: (1) When the selected pipe is set for Bulk-IN transfer (TYPE = B'01 and DIR = 1) When ATREPM = 1 and PID = BUF, this module sends a Zero-Length packet in response to the IN-Token. Each time this module receives ACK from the USB host (flow of one transaction: receiving IN-Token -> sending Zero Length packet -> receiving ACK), this module updates the sequence toggle bit (DATA-PID) by toggling it. No BRDY interrupt or BEMP interrupt is generated. (2) When the selected pipe is set for Bulk-OUT transfer (TYPE = B'01 and DIR = 0) When ATREPM = 1 and PID = BUF, this module sends NAK in response to the OUT-Token (or PING-Token) and generates an NRDY interrupt. Modify this bit when PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. Be sure to set this bit to 1 for USB communication when the FIFO buffer is empty. Do not write data to the FIFO buffer during USB communication with this bit set to 1. When the selected pipe is set for isochronous transfer, be sure to set this bit to 0.
9	ACLRM	0	R/W	Buffer Auto-Clear Mode Enables or disables buffer auto-clear mode for the selected pipe. 0: Buffer auto-clear mode is disabled. 1: Buffer auto-clear mode is enabled. (All buffers are initialized.) To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit. Table 42.9 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared. Modify this bit when PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
8	SQCLR	0	R/W*	Toggle Bit Clear Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is cleared in DATA0. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0. Set the SQCLR bit to 1 when PID = NAK. When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
7	SQSET	0	R/W*	Toggle Bit Set Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is set in DATA1. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA1. This module always indicates SQSET = 0. Set the SQSET bit to 1 when PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
6	SQMON	0	R	Toggle Bit Check Indicates the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: DATA0 1: DATA1 If the pipe is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.
5	PBUSY	0	R	Pipe Busy Indicates whether the pipe is currently used in the USB bus or not. 0: The selected pipe is not used in the USB bus. 1: The selected pipe is being used in the USB bus. When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Specify a response used in the next transaction for the selected pipe. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Tables 42.8 and 42.10 show the basic operation (with no error in packets) of this module in each setting of the PID bits. When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the pipe entered the NAK state. However, when this module changed these bits to NAK, the software does not have to check the PBUSY bit. This module modifies these bits in the following cases. • When the pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end. • When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11). • When this module detects a USB bus reset, this module indicates PID = NAK. Set these bits as follows: • To change the state from NAK (00) to STALL, write B'10. • To change the state from BUF (01) to STALL, write B'11. • To change the state from STALL (11) to NAK, write B'10 then B'00. • To change the state from STALL to BUF, set these bits to NAK and then to BUF.

Note: * Only reading 0 and writing 1 are enabled.

Table 42.8 Operations of BSTS Bit

DIR Bit	BFRE Bit	DCLRM Bit	Meaning of BSTS Bit
0	0	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
		1	Setting prohibited
	1	0	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 when the software sets BCLR = 1 after the buffer data read.
		1	Indicates 1 when the FIFO buffer becomes ready to read receive data from the buffer, and indicates 0 upon completion of the data read.
1	0	0	Indicates 1 when the FIFO buffer becomes ready to write transmit data to the buffer, and indicates 0 upon completion of the data write.
		1	Setting prohibited
	1	0	Setting prohibited
		1	Setting prohibited

Table 42.9 Data Cleared by This Module when ACLRM = 1

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer (both sides for double FIFO buffer) allocated to the pipe	
2	Interval count value when the pipe is isochronous transfer type	When resetting the interval count value
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	FIFO buffer toggle control	When changing the DBLB setting
5	Internal flags related to the transaction count	When forcibly terminating the transaction count function

Table 42.10 Operations of This Module in Each Setting of PID Bits

PID Bits	Transfer Type	Transfer Direction (DIR Bit)	Operation of This Module
B'00 (NAK)	Bulk or interrupt	Independent of the setting	Sends a NAK response to a token from the USB host.
	Isochronous	Independent of the setting	Sends no response to a token from the USB host.
B'01 (BUF)	Bulk	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response. Sends an ACK response to the PING token from the USB host when the FIFO buffer for the selected pipe is ready to receive. Otherwise, sends a NYET response.
	Interrupt	Receive direction (DIR = 0)	Receives data and sends an ACK response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, sends a NAK response.
	Bulk or interrupt	Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a NAK response.
	Isochronous	Receive direction (DIR = 0)	Receives data in response to the OUT token from the USB host when the FIFO buffer for the pipe is ready to receive. Otherwise, ignores the data.
		Transmit direction (DIR = 1)	Sends data in response to a token from the USB host when the FIFO buffer for the pipe is ready to transmit. Otherwise, sends a Zero-Length packet.
B'10 (STALL) or B'11 (STALL)	Bulk or interrupt	Independent of the setting	Sends a STALL response to a token from the USB host.
	Isochronous	Independent of the setting	Sends no response to a token from the USB host.

(2) PIPEnCTR (n = 6 to 8)

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	BSTS	—	—	—	—	—	ACLRM	SQCLR	SQSET	SQMON	PBUSY	—	—	—	PID[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15	BSTS	0	R	Buffer Status Indicates the state of the FIFO buffer of the selected pipe. 0: The buffer is not accessible. 1: The buffer is accessible. The meaning of this bit differs as shown in Table 42.8 depending on the settings of the DIR, BFRE, and DCLRM bits.
14 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ACLRM	0	R/W	Buffer Auto-Clear Mode*2*3 Enables or disables buffer auto-clear mode for the selected pipe. 0: Buffer auto-clear mode is disabled. 1: Buffer auto-clear mode is enabled. (All buffers are initialized.) To completely delete the data in the FIFO buffer allocated to the pipe, write 1 and then 0 continuously to the ACLRM bit. Table 42.11 shows data cleared by this module when this bit is set to 1 and then 0 and cases where such data is cleared. Modify this bit when PID = NAK, and the pipe is not set in the CURPIPE bits. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
8	SQCLR	0	R/W*1	Toggle Bit Clear*2*3 Set this bit to 1 to clear the expected value (in DATA0) of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is cleared in DATA0. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the pipe in DATA0. This module always indicates SQCLR = 0. Set the SQCLR bit to 1 when PID = NAK. When setting this bit to 1 after changing the PID bits for the pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Bit	Bit Name	Initial Value	R/W	Description
7	SQSET	0	R/W*1	Toggle Bit Set*2*3 Set this bit to 1 to set the expected value of the sequence toggle bit for the next transaction of the selected pipe. 0: Invalid 1: The expected value is set in DATA1. When the software sets this bit to 1, this module sets the expected value of the sequence toggle bit of the selected pipe in DATA1. This module always indicates SQSET = 0. Set the SQSET bit to 1 when PID = NAK. When setting this bit to 1 after changing the PID bits for the selected pipe from BUF to NAK, check that PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.
6	SQMON	0	R	Toggle Bit Check Indicates the expected value of the sequence toggle bit for the next transaction of the pipe. 0: DATA0 1: DATA1 If the selected pipe that is not the isochronous transfer type, when a transaction is successfully processed, this module toggles this bit. However, when a DATA-PID mismatch occurs in the receive direction transfer, this bit is not toggled.
5	PBUSY	0	R	Pipe Busy Indicates whether the selected pipe is currently used in the USB bus or not. 0: The selected pipe is not used in the USB bus. 1: The selected pipe is being used in the USB bus. When this module starts the USB transaction for the selected pipe, this module sets this bit to 1. This module clears this bit to 0 upon completion of each transaction. After the software sets PID = NAK, read this bit to see if changing the pipe setting is enabled or not.
4 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
1, 0	PID[1:0]	00	R/W	Response PID Specify a response used in the next transaction for the selected pipe. 00: NAK response 01: BUF response (depending on buffer state) 10: STALL response 11: STALL response These bits are set to NAK by default. To perform USB transfer with the selected pipe, change the setting of these bits to BUF. Tables 42.8 and 42.10 show the basic operation (with no error in packets) of this module in each setting of the PID bits. When changing these bits from BUF to NAK by the software while the pipe is in USB communication, write 00 (NAK) to these bits and then check PBUSY = 1 to confirm that the USB transfer of the selected pipe entered the NAK state. However, when this module changed these bits to NAK, the software needs not check the PBUSY bit. This module modifies these bits in the following cases. • When the selected pipe is in the receive direction and the software sets the SHTNAK bit of the selected pipe to 1, this module indicates PID = NAK when this module recognizes the transfer end. • When this module receives data with a payload exceeding the MaxPacketSize value for the pipe, this module indicates PID = STALL (11). • When this module detects a USB bus reset, this module indicates PID = NAK. Set these bits as follows: • To change the state from NAK (00) to STALL, write B'10. • To change the state from BUF (01) to STALL, write B'11. • To change the state from STALL (11) to NAK, write B'10 then B'00. • To change the state from STALL to BUF, set these bits to NAK and then to BUF.

Notes: 1. Only reading 0 and writing 1 are enabled.
2. Set the ACLRM, SQCLR, or SQSET bit when PID = NAK, and the selected pipe is not set in the CURPIPE bits.
3. When setting the ACLRM, SQCLR, or SQSET bit after changing the PID bits from BUF to NAK, check that PBUSY = 0 for the pipe. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

Table 42.11 Data Cleared by This Module when ACLRM = 1

No.	Data Cleared by the ACLRM Bit	Clearing Timing
1	All data in the FIFO buffer allocated to the selected pipe	
2	Not Support	
3	Internal flags related to the BFRE bit	When changing the BFRE setting
4	Internal flags related to the transaction count	When forcibly terminating the transaction count function

42.2.33 Pipe n Transaction Counter Enable Register (PIPEnTRE) (n = 1 to 5, 9 to F)

PIPEnTRE enables or disables the transaction counter function and clears the counter for pipes 1 to 5, 9 to F.

This register is initialized by a power-on reset.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	TRENB	TRCLR	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R	R

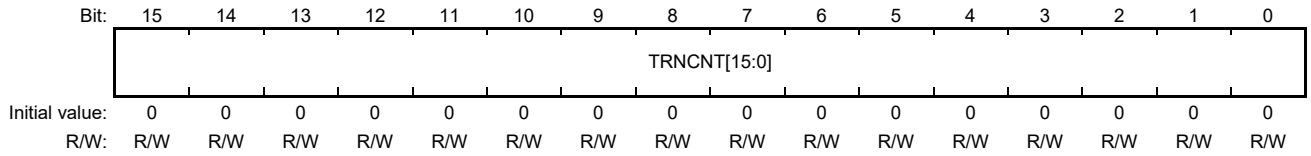
Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	TRENB	0	R/W	Transaction Counter Enable Enables or disables the transaction counter function. 0: The transaction counter function is disabled. 1: The transaction counter function is enabled. When the software sets the number of total packets in the TRNCNT bits in PIPEnTRN for the receive pipe and then sets this bit to 1, this module controls the following when it received the same number of packets as the setting of the TRNCNT bits. When continuous communication mode is used (CNTMD = 1), this module toggles the received data to the CPU even if the FIFO buffer is not full at the end of reception. When SHTNAK = 1, this module changes the PID bits for the corresponding pipe to NAK when this module received the same number of packets as the setting of the TRNCNT bits. When BFRE = 1, this module asserts the BRDY interrupt when this module received the same number of packets as the setting of the TRNCNT bits and read the receive data completely. For transmit pipes, set this bit to 0. When the transaction counter function is not used, set this bit to 0. When using the transaction counter function, set the TRNCNT bits and then set this bit to 1. Furthermore, set this bit to 1 before receiving the first packet that is included in the transaction count range.
8	TRCLR	0	R/W	Transaction Counter Clear Clears the current count value of the transaction counter for the pipe and indicates TRCLR = 0. 0: Invalid 1: The current count value is cleared.
7 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Note: Change the bits in this register when CSSTS = 0 and PID = NAK.
When changing the bits in this register after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK.

42.2.34 Pipe n Transaction Counter Register (PIPEnTRN) (n = 1 to 5, 9 to F)

PIPEnTRN is a transaction counter for pipes 1 to 5, 9 to F.

This register is initialized by a power-on reset, but the setting of this register is retained through a USB bus reset.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	TRNCNT [15:0]	All 0	R/W	Transaction Counter Writing: Specify the number of transactions of DMA transfer. Reading: When TRENB = 0, the set number of transactions is indicated. When TRENB = 1, the number of current transactions is indicated. This module increments (+1) the value of these bits when the following conditions are all satisfied. TRENB = 1 TRNCNT value ≠ current count value +1 when a packet is received. The payload of the received packet equals the value of the MXPS bits. This module clears these bits to 0 when any of the following is satisfied. When the following conditions are all satisfied — TRENB = 1 — TRNCNT value = current count value +1 when a packet is received. — The payload of the received packet equals the value of the MXPS bits. When the following conditions are all satisfied — TRENB = 1 — A short packet is received. When the following conditions are all satisfied — TRENB = 1 — The software sets the TRCLR bit to 1. For transmit pipes, set these bits to all 0. When the transaction counter function is not used, set these bits to all 0. Change these bits when CSSTS = 0, PID = NAK, and TRENB = 0. When setting these bits to 1 after changing the PID bits for the pipe from BUF to NAK, check that CSSTS = 0 and PBUSY = 0. However, the software does not have to check the PBUSY bit when this module changed the PID bits to NAK. When changing these bits, set TRNCNT = 1 and then set TRENB = 1.

42.2.35 Low Power Status register (LPSTS)

This register provides low power management control.

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	SUSPM	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R/W	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	SUSPM	0	R/W	SuspendM control 0: UTMI suspend mode 1: UTMI normal mode This bit should set to 1 when normal operating. UTMI clock is halted if this bit set to 0. Note: This controller denies register access without as follow registers if this bit set to 0. SYSCFG0 BUSWAIT INTENB1 LPSTS UGCTRL2
13 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

42.2.36 USB General Control Register (UGCTRL)

This register provides embedded USB PHY control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PLL RESET
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PLLRESET*	1	R/W	PLL Reset 0: PLL reset release 1: PLL reset assert

Note: * This bit affects to both HS-USB Channel 0 and HS-USB Channel 1.

42.2.37 USB General Control Register 2 (UGCTRL2)

This register provides embedded USB PHY control.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	USB0SEL		—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	USB0SEL	01	R/W	USB2.0 Selection 00: Reserved 01: Select EHCI/OHCI host module for USB2.0 10: Select HS USB module for USB2.0 11: Reserved
3 to 0	—	0001	R	Reserved These bits are always read as B'0001. The write value should always be B'0001.

42.3 Operation

42.3.1 System Control and Oscillation Control

This section describes register operations required for the initial settings of this module and the registers required for the power consumption control.

(1) Power control and Initialization

The following is the initialize power on procedure of USB subsystem.

1. Supply 1.8 V (VD181)
2. Supply 3.3 V (VD331) (Note: Do not supply 3.3 V when 1.8 V is not supplied.)
3. HS-USB module stop release and module reset assert.
4. PLLRESET release
5. Wait min. 340 µs for USB PHY power stable.
6. USB0SEL[1:0] should be set to B'10 for USB Function (HS-USB)
7. LPSTS.SUSPM set to normal mode.
8. Starting normal operation.

(2) Enabling High-Speed Operation

This module can set the USB transmission rate (communication bit rate) by the software.

When the function controller function is selected, high-speed operation or full-speed operation is selectable. To enable high-speed operation with this module, set the HSE bit in SYSCFG to 1. When high-speed operation is enabled, this module executes the reset handshake protocol and automatically sets the USB transmission rate. The reset handshake result can be checked by the RHST bits in DVSTCTR.

When high-speed operation is disabled, this module operates in full speed when the function controller function is selected.

(3) USB Data Bus Resistor Control

Figure 42.1 shows the connection between this module and the USB connector.

This module incorporates a pull-up resistor of the D+ signal. Specify pull-up using the DPRPU bits in SYSCFG.

Furthermore, this module controls the terminating resistors of the D+ and D- signals in high-speed operation, and the output resistors in full-speed operation. This module automatically switches the on-chip resistors after connection to the host controller detecting a reset handshake, suspended state, or resume.

When the DPRPU bit in SYSCFG is set to 0 during communication with the host controller, this module disables the pull-up resistors (or terminating resistors) of the USB data line. Therefore, the USB host can be notified of a disconnection from the device.

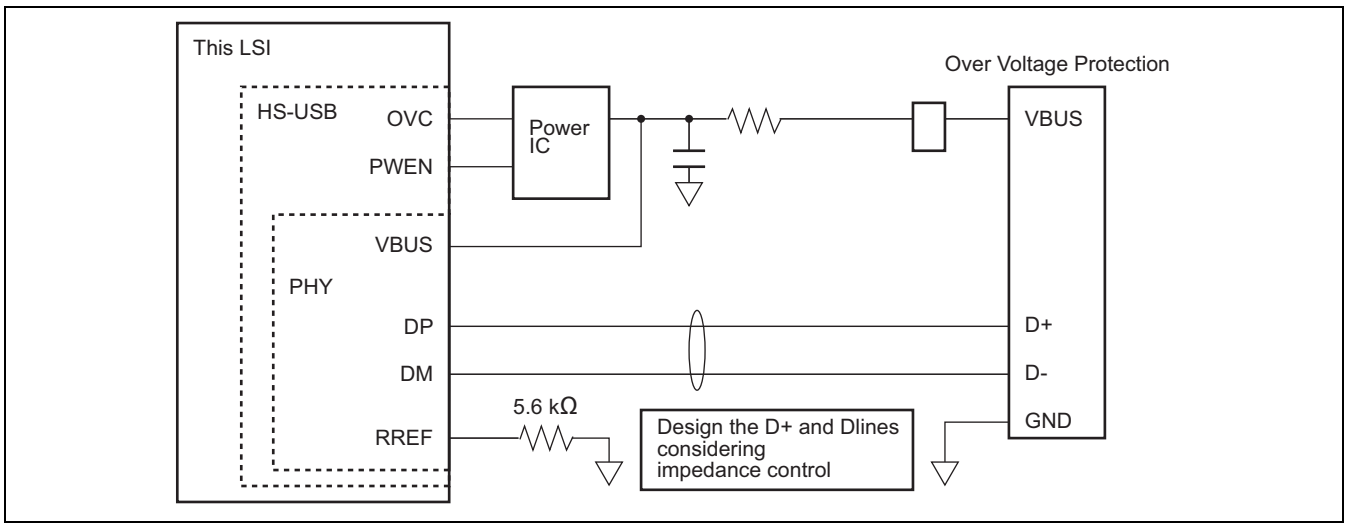


Figure 42.1 Connection to the USB Connector

(4) Software reset when the USB disconnection is detected

Issue a software reset of the USBHS module when the USB disconnection is detected. If the DMA interface is being used, issue a software reset of the USB-DMAC module as well. A software reset can be issued via a register in the CPG

Whether or not the USB disconnection is detected can be determined by the VBSTS in the INTSTS0 register when the function controller function is selected.

Note: USB-PHY might become inoperable to use by the instantaneous interruption of VBUS. As a result S/W on the LSI side (driver) becomes a state of the connection, and USB-PHY becomes a state of power cutoff. It's possible to cancel this state by putting the next way into effect by software.

1) When detecting a bus reset or cutoff of VBUS, please refer to the state bit of USB - PHY (USB_OFF bit of USBCR2 register in GPIO) and in case of USB_OFF = 1, set USB_START bit.
2) When 1) is performed and USB - PHY is started, USB_PHY_ON interrupt occurs, so please perform a soft reset to USBHS, USB-DMAC and do the setting by which USBHS,USB-DMAC is initialization and DP pull up --, etc. by this timing.

42.3.2 Interrupt Function

Table 42.12 lists the interrupt generating conditions of this module.

When any of the following interrupt generating conditions are satisfied and the interrupt output is enabled by the corresponding interrupt enable register, this module outputs a USB interrupt request to the interrupt controller (INTC).

Table 42.12 Interrupt Generating Conditions

Bit	Interrupt Name	Interrupt Generating Conditions	Function	Related Status
VBINT	VBUS interrupt	When VBUS input pin state change is detected (both L to H and H to L)		VBSTS
RESM	Resume interrupt	When a USB bus state change is detected in the suspended state (J-State to K-State or J-State to SE0)		—
SOFR	Frame number update interrupt	SOFRM = 0: When an SOF packet with a different frame number is received SOFRM = 1: When an SOF packet with a µ frame number of 0 cannot be received due to damage, etc.		—
DVST	Device state transition interrupt	When a device state transition is detected USB bus reset detected Suspended state detected SET_ADDRESS request received SET_CONFIGURATION request received		DVSQ
CTRT	Control transfer stage transition interrupt	When a control transfer stage transition is detected Setup stage completed Control write transfer status stage shifted Control read transfer status stage shifted Control transfer completed Control transfer sequence error occurred		CTSQ
BEMP	Buffer empty interrupt	When the buffer becomes empty after sending all buffer memory data When a packet with a size exceeding the maximum packet size is received		BEMPSTS.PIPEBEMP
NRDY	Buffer not ready interrupt	When NAK is sent in response to IN token, OUTtoken, or PING token When a CRC error or bit stuffing error occurred during data reception in isochronous transfer When an overrun or underrun error occurred during data reception in isochronous transfer		NRDYSTS.PIPENRDY
BRDY	Buffer ready interrupt	When the buffer becomes ready for reading or writing		BRDYSTS.PIPEBRDY
OVRCR	OVRCR interrupt	When an OVC input pin state change is detected		OVCMON

Note: These bits in this table are those of INTSTS0 if any register's name is not indicated.

Figure 42.2 shows a block diagram of the interrupt circuit of this module.

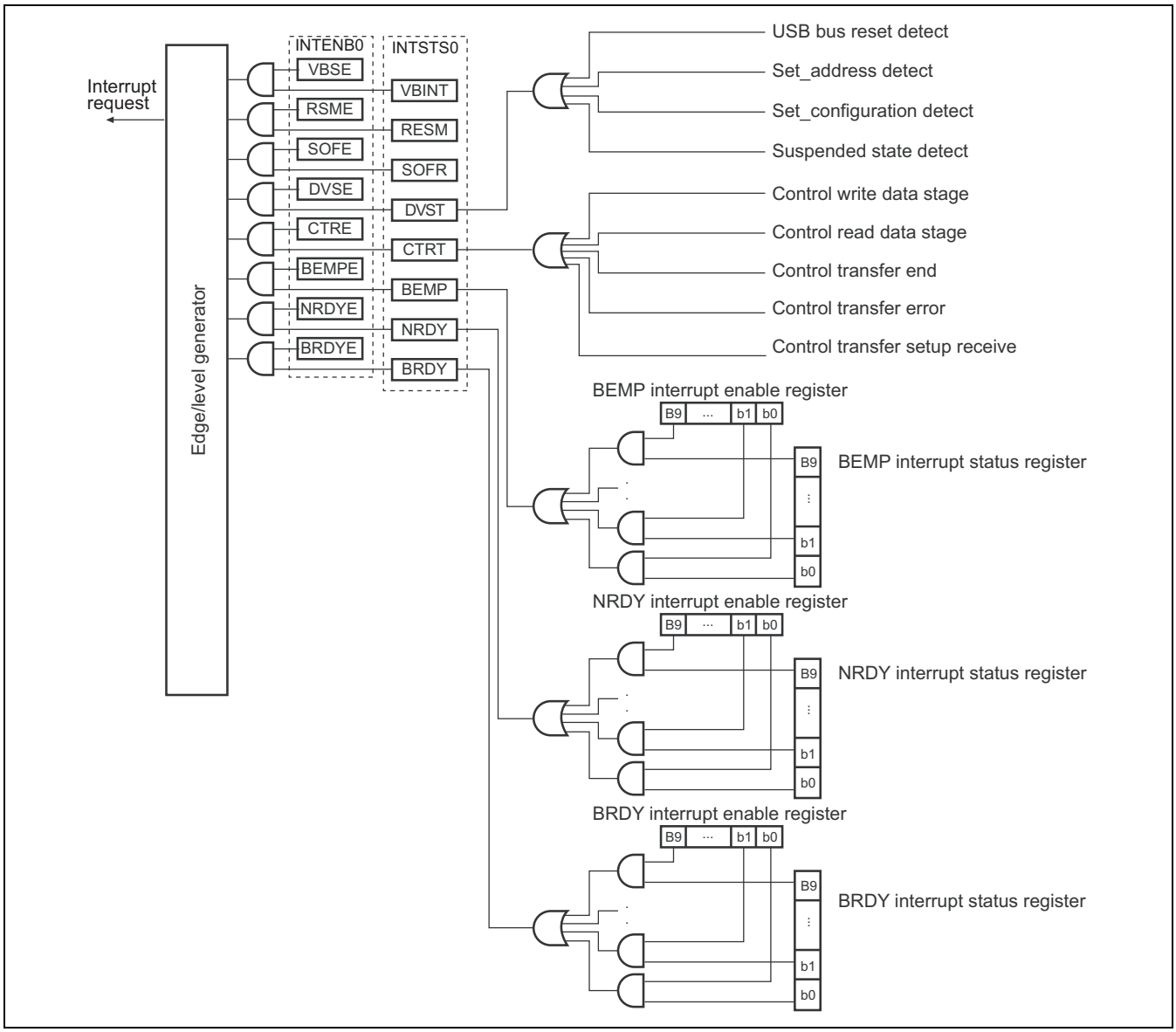


Figure 42.2 Block Diagram of Interrupt Circuit

(1) BRDY Interrupt

A BRDY interrupt can be generated. When the following conditions in each pipe are satisfied, this module sets the corresponding bit in BRDYSTS to 1. At this time, when the PIPEBRDYE bit for the pipe in BRDYENB is set to 1 and the BRDYE bit in INTENB0 is set to 1 by the software, this module generates a BRDY interrupt.

BRDY interrupt generating conditions and clearing method depend on the settings of the BRDYM bit and the BFRE bit for each pipe.

(a) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified

With this setting, a BRDY interrupt indicates that the FIFO port is accessible.

This module generates an internal BRDY interrupt request trigger when the following conditions are satisfied, and sets the PIPEBRDY bit corresponding to the request trigger pipe to 1.

1. Pipes set for the transmit direction
   - When the software changes the DIR bit from 0 to 1
   - When this module finishes sending a packet of the pipe while data write from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)
   - When continuous communication mode is selected, this module generates a BRDY interrupt request trigger upon completion of sending data for one side of the FIFO buffer.
   - When a double FIFO buffer is specified and one side of the FIFO buffer is empty when data write to the other side of the FIFO buffer is completed.

     Even if one side of the FIFO buffer becomes empty while the other side is in data write processing, no BRDY interrupt is generated until the ongoing data write finishes.
   - When this module generates a buffer flush for a pipe of isochronous transfer type
   - When the FIFO buffer becomes write enable state by writing 1 to the ACLRM bit

No BRDY interrupt request trigger is generated for the DCP (in data transmission of control transfer).

2. Pipes set for the receive direction
   - When this module receives a packet successfully and the FIFO buffer becomes ready for reading while data read access from the CPU to the FIFO buffer allocated to the pipe is disabled (BSTS = 0)
   - No BRDY interrupt request trigger is generated in transactions with incorrect data PID.
   - When continuous communication mode is selected, no BRDY interrupt request trigger is generated for packets with a MaxPacketSize data size and when the FIFO buffer still has available space.
   - When this module receives a short packet, this module generates a BRDY interrupt request trigger even if the buffer has available space.
   - When a transaction counter is used, this module generates a BRDY interrupt request trigger when this module receives a packet with a size of the set value even if the FIFO buffer still has available space.
   - When a double FIFO buffer is specified and one side of the FIFO buffer is ready for reading when data read from the other side of the FIFO buffer is completed

     Even if data read for one side of the FIFO buffer is completed while the other side is undergoing data read, no BRDY interrupt request trigger is generated until the ongoing data read finishes.

This interrupt is not generated in communication in the control transfer status stage.

The software can clear the PIPEBRDY interrupt status of the pipe by writing 0 to the PIPEBRDY bit for the pipe in BRDYSTS. At this time, write 1 to the bits corresponding to other pipes.

Be sure to clear the BRDY interrupt status before accessing the FIFO buffer.

(b) When BRDY interrupt disable (BRDYM = 0) and BRDY interrupt output enable (BFRE = 1) at the end of data read are specified

With this setting, this module determines that a BRDY interrupt is generated upon completion of reading all data of one transfer in a receive pipe, and sets the bit for the pipe in this register to 1.

This module determines that the last data of a transfer was received in either of the following cases.

- A Zero-Length packet or another short packet is received.
- A transaction counter (TRNCNT bits) is used and a packet with a size of the value of the TRNCNT bits is received.

When either of these conditions is satisfied and the data read is completed, this module determines that reading all data for one transfer is completed.

When this module receives a Zero-Length packet with the FIFO buffer empty, this module determines that reading all data for one transfer is completed when the Zero-Length packet data is toggled to the CPU. In this case, write 1 to the BCLR bit in the corresponding FIFOCTR register by the software to start the next transfer.

With this setting, this module generates no BRDY interrupt for transmit pipes.

The software can clear the PIPEBRDY interrupt status of the pipe to 0 by writing 0 to the PIPEBRDY bit for the pipe. At this time, write 1 to the bits corresponding to other pipes.

When using this mode, do not change the BFRE setting until the processing for one transfer is completed.

To change the BFRE bit during processing, clear all FIFO buffers for the pipe by the ACLRM bit.

(c) When BRDY interrupt enable (BRDYM = 1) and BRDY interrupt output enable (BFRE = 0) at data reception/transmission are specified

With this setting, the value of the PIPEBRDY bit varies with the value of the BSTS bit for each pipe. That is, this module indicates 1 or 0 of the BRDY interrupt status according to the FIFO buffer status.

1. Pipes set for the transmit direction

   When the FIFO port is ready to write data, the PIPEBRDY bit indicates 1. When the FIFO port is not ready to write data, the PIPEBRDY bit indicates 0.

   However, even if the transmit pipe of the DCP is ready to write data, no BRDY interrupt is asserted.
2. Pipes set for the receive direction

   When the FIFO port is ready to read data, the PIPEBRDY bit indicates 1. When all data is read from the FIFO port (reading disabled), the PIPEBRDY bit indicates 0.

   When this module receives a Zero-Length packet with the FIFO buffer empty, this module indicates 1 with the corresponding bit until 1 is written to BCLR by the software, and continues to assert the BRDY interrupt.

   With this setting, the software cannot clear the PIPEBRDY bit to 0.

   When BRDYM = 1, set the BFRE bit to 0 for all pipes.

Figure 42.3 shows the BRDY interrupt generation timing.

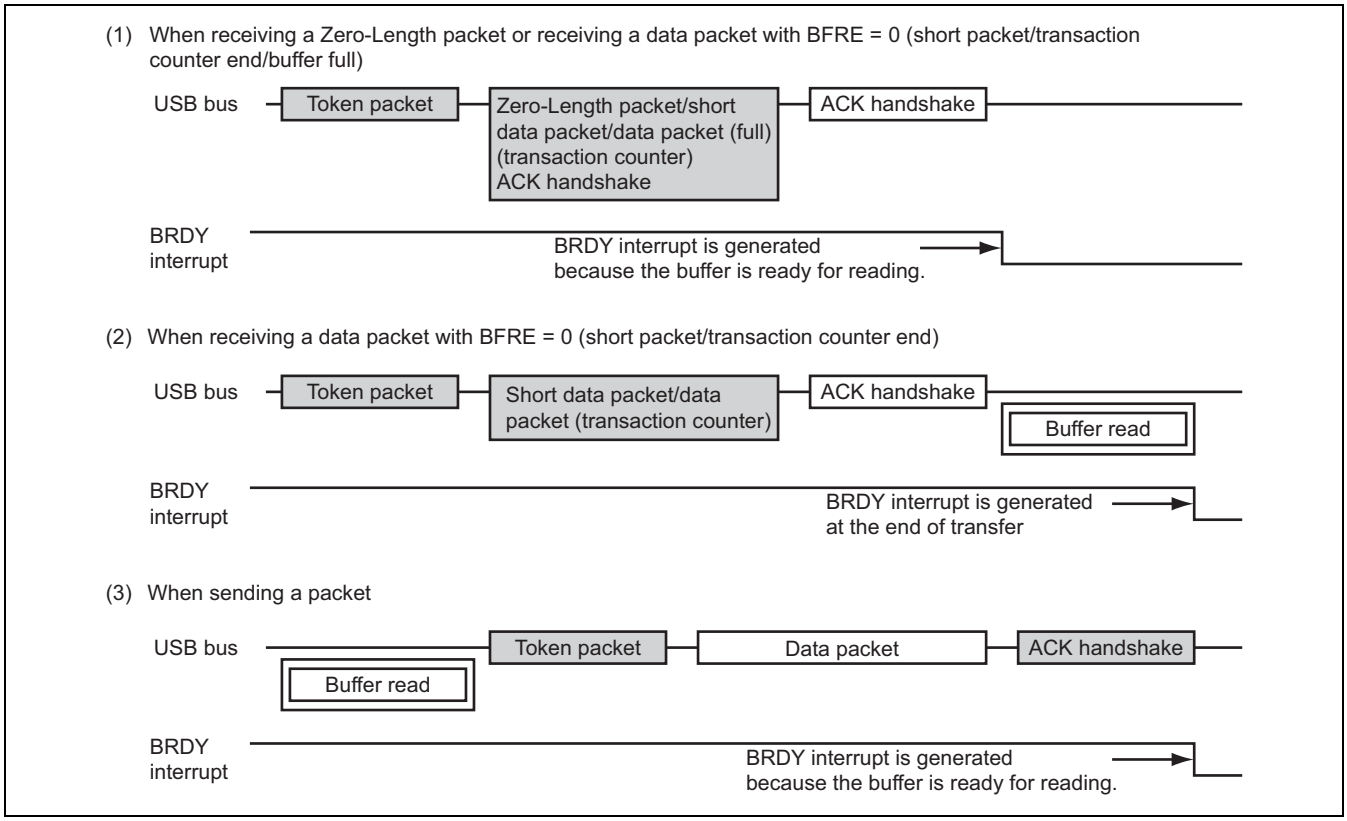


Figure 42.3 BRDY Interrupt Generation Timing

(2) NRDY Interrupt

When this module generates an internal NRDY interrupt request for the pipe in which PID = BUF is set by the software, this module indicates PIPENRDY = 1 for the pipe in NRDYSTS. At this time, when 1 is set in the corresponding bit in NRDYENB by the software, this module indicates NRDY = 1 in INTSTS0 and generates a USB interrupt.

The following shows the conditions for this module to generate an internal NRDY interrupt request for a pipe.

Furthermore, when executing the control transfer status stage, this module generates no interrupt request.

1. Pipes in the transmit direction
   - When this module receives an IN token with no transmit data in the FIFO buffer
     This module generates an NRDY interrupt request and indicates PIPENRDY = 1.
   - When the pipe in which the interrupt is generated is isochronous transfer type, this module sends a Zero-Length packet and indicates OVRN = 1.
2. Pipes in the receive direction pipe
   - When this module receives an OUT token with the FIFO buffer occupied
   - When the pipe in which the interrupt is generated is isochronous transfer type, this module generates an NRDY interrupt request when this module receives an OUT token, and indicates PIPENRDY = 1 and OVRN = 1.
   - When the pipe in which the interrupt is generated is not isochroous transfer type, this module generates an NRDY interrupt request when this module sends an NAK handshake response after receiving data following the OUT token, and indicates PIPENRDY = 1.
     However, this module generates no NRDY interrupt when resending data (in the case of DATA-PID mismatch) or when an error occurs in a data packet.
   - When this module receives a PING token with the FIFO buffer occupied
     This module generates an NRDY interrupt request when this module receives a PING token and indicates PIPENRDY = 1.
   - When a packet is not received correctly within the interval frame in an isochroous transfer-type pipe
     This module generates an NRDY interrupt request when this module receives SOF and indicates PIPENRDY = 1.

Figure 42.4 shows the NRDY interrupt generation timing when the function controller function is selected.

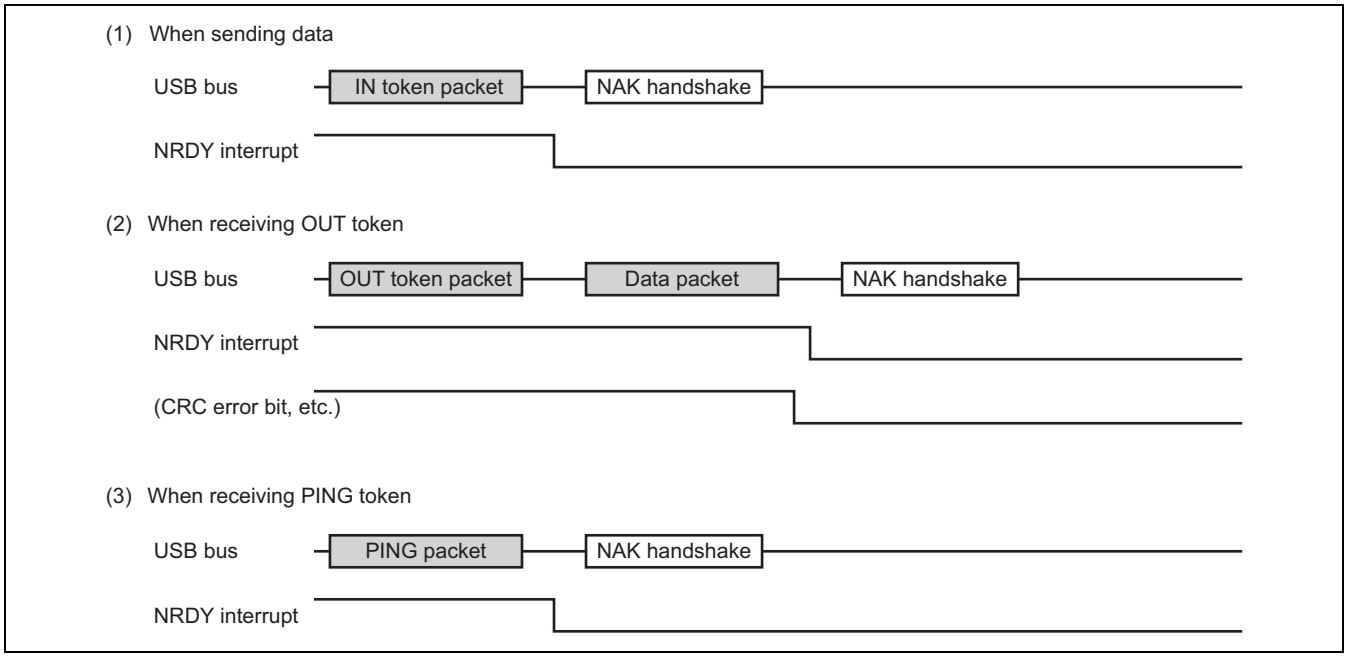


Figure 42.4 NRDY Interrupt Generation Timing when the Function Controller Function is selected

(3) BEMP Interrupt

When this module detects a BEMP interrupt for the pipe in which PID = BUF is set by the software, this module indicates PIPEBEMP = 1 for the pipe in BEMPSTS. At this time, when 1 is set in the corresponding bit in BEMPENB by the software, this module indicates BEMP = 1 in INTSTS0 and generates a USB interrupt.

This module generates an internal BEMP interrupt request in the following cases.

1. Transmit direction pipes
   — When the FIFO buffer for the pipe is empty at the end of transmission (including transmission of a Zero-Length packet)
   — When single buffer is set for the FIFO buffer, this module generates an internal BEMP interrupt request concurrently with a BRDY interrupt for pipes other than DCP.
   However, this module generates no internal BEMP interrupt request in the following cases.
   - In the case of double buffer, when the software (DMAC) already started writing data to the FIFO buffer of the CPU at the end of transmission for one-side data
   - When the buffer is cleared (empty) by writing 1 to the ACLRM or BCLR bit.
   - When sending a Zero-Length packet (IN transfer) of the control transfer status stage

2. Receive direction pipes
   — When this module receives a packet with a data size exceeding the MaxPacketSize value
   In this case, this module generates a BEMP interrupt request and indicates the PIPEBEMP = 1 for the pipe, ignores the received data, and changes the PID bits for the pipe to STALL (11).
   At this time, this module sends a STALL response.
   However, this module generates no BEMP interrupt request in the following cases.
   - When this module detects a CRC error or bit stuffing error in the receive data
   - When executing the SETUP transaction
     Writing 0 to the PIPEBEMP bits clears the status.
     Writing 0 to the PIPEBEMP bits has no effect on the operation of this module.

Figure 42.5 shows the BEMP interrupt generation timing when the function controller function is selected.

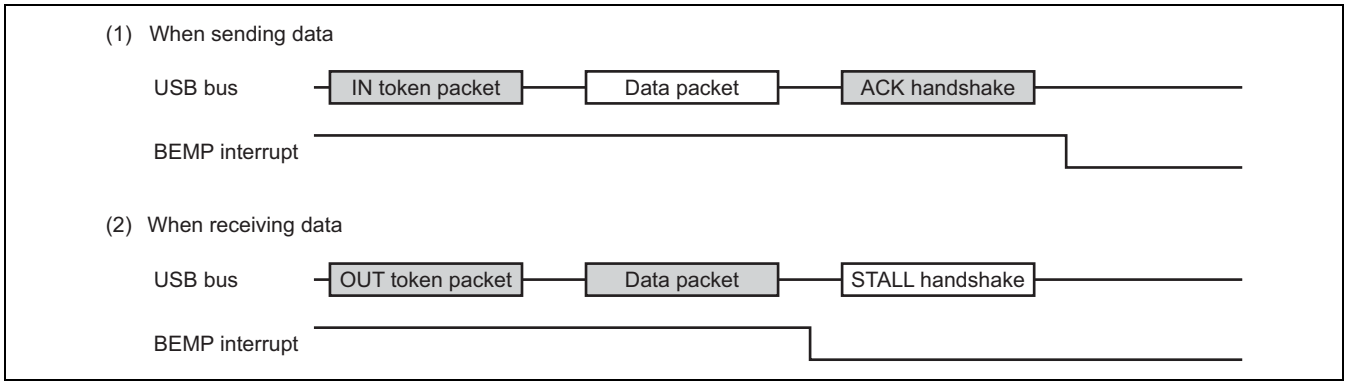


Figure 42.5 BEMP Interrupt Generation Timing when the Function Controller Function is selected

(4) Device State Transition Interrupt

Figure 42.6 shows the device state transitions of this module. This module controls device states and generates device state transition interrupts. However, when returning from the suspended state (detecting the resume signal), this module detects the transition with a resume interrupt. The device state transition interrupt is enabled or disabled by setting INTENB0. The current device state can be monitored using the DVSQ bits in INTSTS0.

When this module shifts to the default state, a device state transition interrupt occurs after executing the reset handshake protocol.

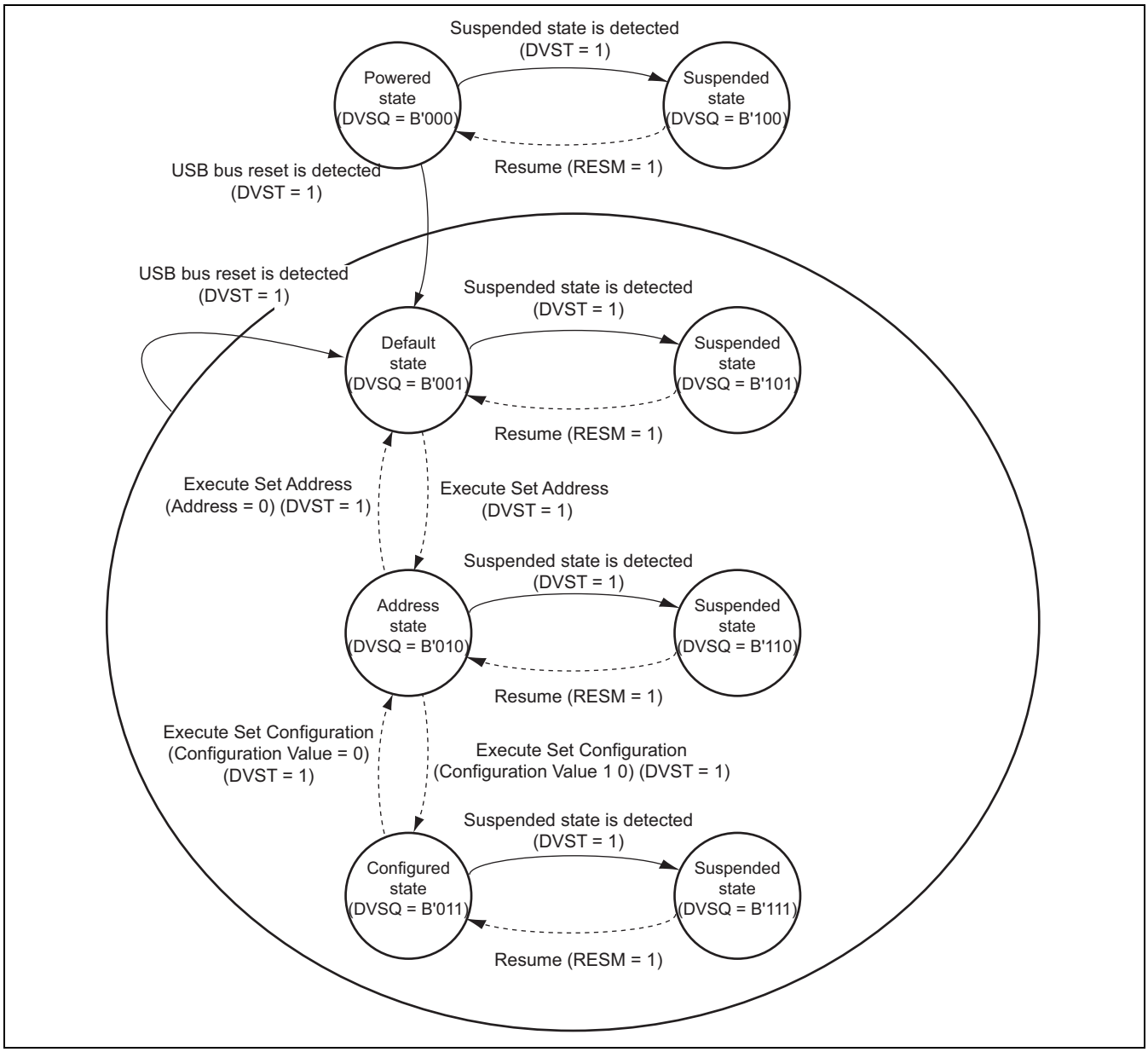


Figure 42.6 Device State Transitions

(5) Control Transfer Stage Transition Interrupt

Figure 42.7 shows control transfer stage transitions of this module. This module manages the sequence of control transfers and generates control transfer stage transition interrupts. Enabling or disabling each control transfer stage transition interrupt can be set by INTENB0. The current transfer stage after transition can be checked by the CTSQ bits in INTSTS0.

The following describes control transfer sequence errors. When an error occurs, the PID bits in DCPCTR indicate B'1x (STALL response).

1. Control read transfer
   - This module receives an OUT or PING token in response to the IN token in the data stage before starting data transfer.
   - This module receives an IN token in the status stage.
   - This module receives a packet with a data packet of DATAPID = DATA0 in the status stage.
2. Control write transfer
   - This module receives an IN token in response to the OUT token in the data stage before sending an ACK response.
   - This module receives a packet with the first data packet of DATAPID = DATA0.
   - This module receives an OUT or PING token in the status stage.
3. Control write no-data control transfer
   - This module receives an OUT or PING token in the status stage.

If the size of the receive data exceeds the wLength value of the USB request in the control write transfer data stage, this is not treated as a control transfer sequence error. This module sends ACK for normal end in response to a packet other than Zero-Length packet in the control read transfer status stage.

When a CTRT interrupt is generated (SERR = 1) due to a sequence error, CTSQ = B'110 is retained until the interrupt status is cleared (CTRT = 0) by the system. For this reason, while CTSQ = B'110, even if a new USB request is received, a CTRT interrupt at the end of the setup stage is not generated. (This module retains the setup stage end status and generates a setup stage end interrupt after the interrupt status is cleared by the software.)

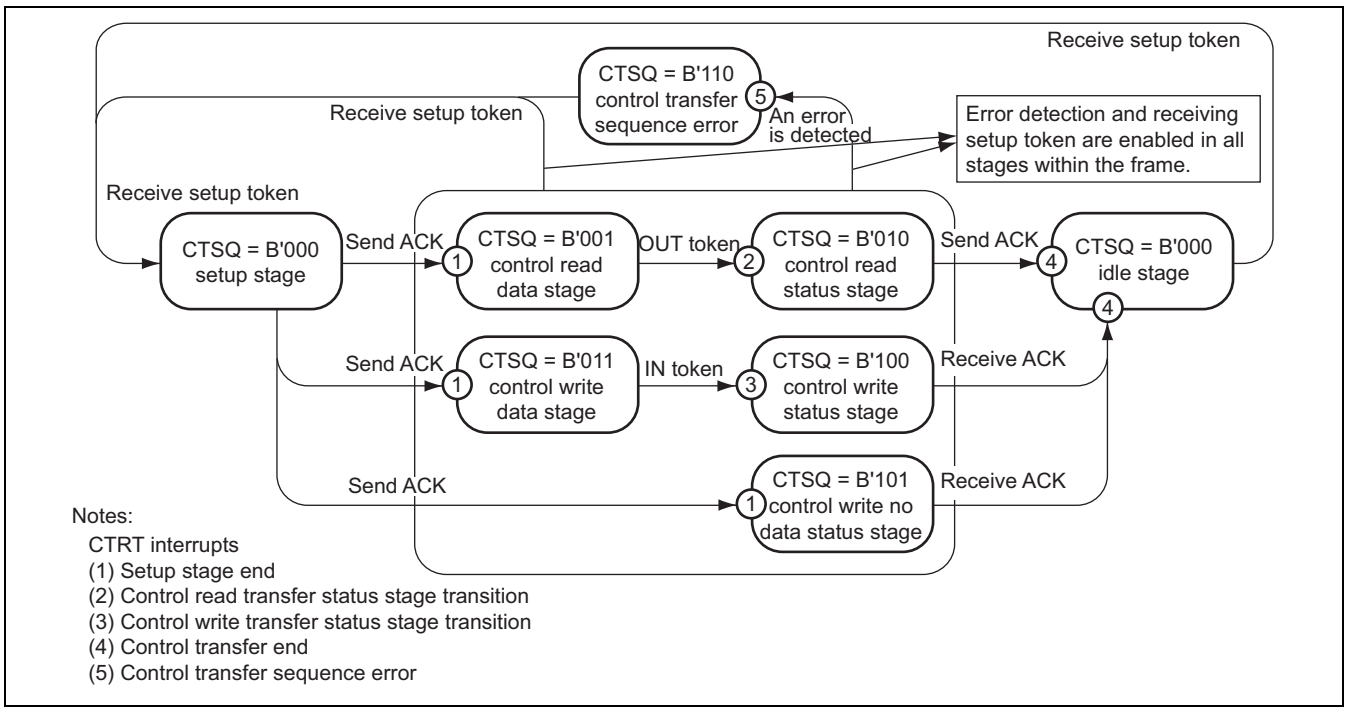


Figure 42.7 Control Transfer Stage Transitions

(6) Frame Update Interrupt

Figure 42.8 shows an example of the SOFR interrupt output timing of this module.

An SOFR interrupt is generated immediately after the frame number is updated.

When this module detects a new SOF packet during the full-speed operation, this module updates the frame number and generates an SOFR interrupt. In the high-speed operation, however, the frame number is not updated or no SOFR interrupt is generated unless the module enters the µ SOF lock state. Furthermore, the SOF interpolation function is not activated. The µ SOF lock state occurs when this module receives a µ SOF packet twice in a row with different frame numbers without an error.

The µ SOF lock monitoring start and stop conditions are as follows:

1. µ SOF lock monitoring start conditions
   USBE = 1
2. µ SOF lock monitoring stop conditions
   USBE = 0, receiving USB bus reset, or detection of suspended state

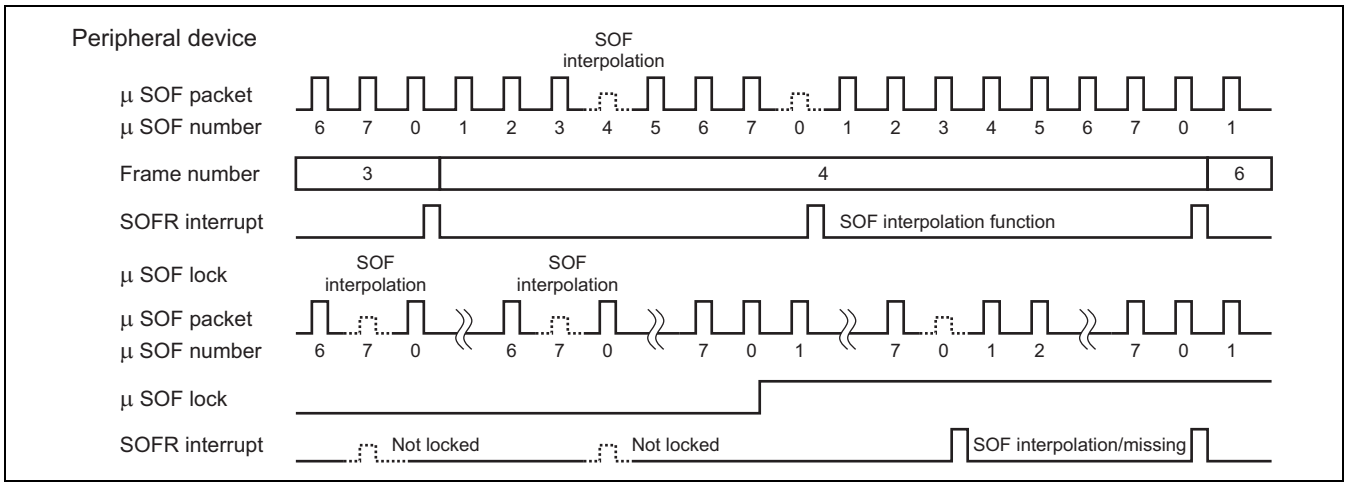


Figure 42.8 Example of SOFR Interrupt Output Timing

(7) VBUS Interrupt

When the VBUSIN_0 pin state changes, a VBUS interrupt is generated. The VBUSIN_0 pin level can be checked by the VBSTS bit in INTSTS0. The VBUS interrupt is used to check connection or disconnection to the host controller. However, when the system starts up with the host controller connected, the VBUSIN_0 pin state remains unchanged, and therefore the first VBUS interrupt is not generated.

(8) Resume Interrupt

When the function controller function is selected and the USB bus state changes (J-State to K-State or J-State to SE0) with the device state suspended, a resume interrupt is generated. The resume interrupt is used to detect the return from the suspended state.

42.3.3 Pipe Control

Table 42.13 lists the pipe settings of this module. In the USB data transfer, data must be transmitted or received using virtual pipes called “endpoint.” This module is provided with ten pipes for data transfer. Set each pipe according to system specifications.

Table 42.13 Pipe Settings

Register Name	Bit Name	Setting	Remarks
DCPCFG PIPECFG	TYPE	Transfer type	Pipes 1 to F: Setting allowed
	BFRE	BRDY interrupt mode	Pipes 1 to 5, B to F: Setting allowed
	DBLB	Double buffer	Pipes 1 to 5, B to F: Setting allowed Pipes 9, A: Setting allowed only when bulk transfer is selected
	CNTMD	Continuous transfer or discontinuous transfer	Pipes 1 to 2, 9, A: Setting allowed only when bulk transfer is selected Pipes 3 to 5, B to F: Setting allowed
	DIR	Transfer direction	IN or OUT selectable
	EPNUM	Endpoint number	Pipes 1 to F: Setting allowed Set a value other than 0000 when using pipes
	SHTNAK	Disabling pipes at the end of transfer	Pipes 1 to 2, 9, A: Setting allowed only when bulk transfer is selected Pipes 3 to 5, B to F: Setting allowed
PIPEBUF	BUFSIZE	Buffer memory size	DCP: Setting disallowed (256 bytes fixed) Pipes 1 to 5, A to F: Setting allowed (up to 2 Kbytes) Pipes 6 to 9: Setting disallowed (64 bytes fixed)
	BUFNMB	Buffer memory number	DCP: Setting disallowed (H'0 to H'3 fixed) Pipes 1 to 5, A to F: Setting allowed (H'8 to H'87) Pipes 6 to 9: Setting disallowed (H'4 to H'7 fixed)
DCPMAXP PIPEMAXP	MXPS	Maximum packet size	Setting conforming to the USB Specification
PIPEPERI	IFIS	Buffer flush	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to F: Setting disallowed
	IITV	Interval counter	Pipes 1, 2: Setting allowed only when isochronous transfer is selected Pipes 3 to F: Setting disallowed
DCPCTR PIPEnCTR	BSTS	Buffer status	For DCP, receive buffer status and transmit buffer status are switched by the ISEL bit.
	INBUFM	IN buffer monitor	Provided only for pipes 3 to 5, 9 to F.
	ATREPM	Auto-response mode	Pipes 1 to 5, 9 to F Setting allowed only when the function controller function is selected.
	ACLRM	Buffer auto-clear	Pipes 1 to F Setting allowed
	SQCLR	Sequence clear	Data toggle bit clear
	SQSET	Sequence setting	Data toggle bit setting
	SQMON	Sequence check	Data toggle bit check
	PBUSY	Pipe busy check	
	PID	Response PID	See section 42.3.3 (6), Response PID.

Register Name	Bit Name	Setting	Remarks
PIPEnTRE	TRENB	Transaction count enable	Pipes 1 to 5, 9 to F: Setting allowed
	TRCLR	Current transaction counter clear	Pipes 1 to 5, 9 to F: Setting allowed
PIPEnTRN	TRNCNT	Transaction counter	Pipes 1 to 5, 9 to F: Setting allowed

(1) Pipe Control Registers Switching Procedure

The following bits in the pipe control registers can be modified only when USB communication is set to disabled (PID = NAK).

Bits/registers that cannot be modified when USB communication is set to enabled (PID = BUF)

- Each bit in DCPCFG and DCPMAXP
- SQCLR and SQSET bits in DCPCTR
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI
- ATREPM, ACLRM, SQCLR, and SQSET bits in PIPEnCTR
- Each bit in PIPEnTRE and PIPEnTRN

When changing these bits from the state where USB communication is enabled (PID = BUF), follow the steps below.

1. Generate a pipe control register bit change request.
2. Change the PID bits for the pipe to NAK.
3. Wait until the PBUSY bit for the pipe is cleared to 0.
4. Change the bits in the pipe control registers.

The following bits in the pipe control registers can be modified only for pipe information that is not set in any of the CURPIPE bits in CFIFOSEL, D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL.

Bits/registers that cannot be modified while the CURPIPE bits in FIFO-PORT are being set

- Each bit in DCPCFG and DCPMAXP
- Each bit in PIPECFG, PIPEBUF, PIPEMAXP, and PIPEPERI

Before changing the pipe information, set the CURPIPE bits to a pipe other than that to be changed. For the DCP, clear the buffer by the BCLR bit after modifying the pipe information.

(2) Transfer Type

Specify the transfer type of each pipe by the TYPE bits in PIPEPCFG as follows:

- DCP: Setting is not required (fixed to control transfer).
- Pipes 1, 2: Set bulk transfer or isochronous transfer.
- Pipes 3 to 5, B to F: Set bulk transfer.
- Pipes 6 to 8: Set interrupt transfer.
- Pipes 9, A: Set Bulk transfer or interrupt transfer.

(3) Endpoint Number

Specify the endpoint number of each pipe by the EPNUM bits in PIPEPCFG. The endpoint number of the DCP is always 0. For other pipes, endpoint 1 to endpoint 15 are selectable.

- DCP: Setting is not required (fixed to endpoint 0).
- Pipes 1 to F: Set an endpoint number by selecting a number 1 to 15.
  However, set an endpoint number so that combinations of the DIR bit and the EPNUM bits do not overlap.

(4) Maximum Packet Size

Specify the maximum packet size of each pipe by the MXPS bits in DCPMAXP and PIPEMAXP. For the DCP and pipes 1 to 5, 9 to F, any of the maximum packet sizes defined in the USB Specification can be set. For pipes 6 to 8 a maximum packet size up to 64 bytes can be set. Specify a maximum packet size as follows before starting transfer (PID = BUF):

- DCP: Set 64 for high-speed operation.
- DCP: Set 8, 16, 32, or 64 for full-speed operation.
- Pipes 1 to 5: Set 512 for high-speed bulk transfer.
- Pipes 1 to 5: Set 8, 16, 32, or 64 for full-speed bulk transfer.
- Pipes 1, 2: Set a value from 1 to 1024 for high-speed isochronous transfer.
- Pipes 1, 2: Set a value from 1 to 1023 for full-speed isochronous transfer.
- Pipes 6 to 9: Set a value from 1 to 64.
- Pipe 9: Set 512 for high-speed bulk transfer.
- Pipe 9: Set 8, 16, 32, or 64 for full-speed bulk transfer.
- Pipes 9 to A: Set a value from 1 to 64 for interrupt transfer.
- Pipes B to F: Set 512 for high-speed bulk transfer.
- Pipes B to F: Set 8, 16, 32, or 64 for full-speed bulk transfer.

High Bandwidth in interrupt and isochronous transfers is not supported.

(5) Transaction Counter (Pipes 1 to 5, 9 to F: Read Direction)

When the specified number of transactions with data packet in the receive direction are completed, this module recognizes this as a transfer end. The transaction counter works when the pipe selected for the D0FIFOSEL, D1FIFOSEL, D2FIFOSEL and D3FIFOSEL ports is set for the data read (from the buffer memory) direction. The transaction counter is provided with the TRNCNT register to specify the number of transactions and the current counter to count transactions internally. When the current counter reaches the specified value, the buffer memory becomes ready for reading. The current counter of the transaction counter function can be initialized by the TRCLR bit to count transactions again from the beginning. The TRNCNT read data varies depending on the TRENB setting.

- TRENB = 0: The set transaction counter value is read.
- TRENB = 1: The internally counted current counter value is read.
- Change the CURPIPE bits according to the following.
- Do not change the CURPIPE bits until the transaction for the specified pipe finishes.
- Change the CURPIPE bits when the current counter is cleared.
- Control the TRCLR bit according to the following.
- Do not clear the current counter during transaction count and PID = BUF.
- Do not clear the current counter while data is remaining in the buffer.

(6) Response PID

Specify the response PID for each pipe by the PID bits in DCPCTR and PIPEnCTR.

This module operates as follows according to the response PID setting.

The response PID specifies a response to transactions from the host.

- NAK setting: NAK is always sent in response to a transaction.
- BUF setting: A response is sent to a transaction according to the buffer memory status.
- STALL setting: STALL is always sent in response to a transaction.

Note: This module always sends ACK in response to a setup transaction irrespective of the PID setting, and stores a USB request in the register.

This module modifies the PID bits in the following cases depending on transaction results.

- When the response PID is set by the hardware
  - NAK setting: This module sets PID to NAK in the following cases and always sends NAK in response to a transaction.
- When a SETUP token is successfully received (DCP only)
- When the SHTNAK bit in PIPECFG is set to 1 in a bulk transfer and the transaction counter stops counting or this module receives a short packet
  - BUF setting: This module does not set the PID bits to BUF.
  - STALL setting: This module sets PID to STALL in the following cases and always sends STALL in response to a transaction.
- When a maximum packet size exceeded error is detected in a receive data packet
- When a control transfer sequence error is detected (DCP only)

(7) Data PID Sequence Bit

When data is successfully transferred in the control transfer data stage, bulk transfer, or interrupt transfer, this module automatically toggles the data PID sequence bit. The sequence bit of the data PID transmitted next can be monitored by the SQMON bit in DCPCTR and PIPEnCTR. In a data transmission period, the sequence bit switches at the ACK handshake receive timing. In a data reception period, the sequence bit switches at the ACK handshake transmit timing. The data PID sequence bit can also be changed by the SQCLR and SQSET bits in DCPCTR and PIPEnCTR.

In control transfers, this module automatically sets the sequence bit during a stage transition. DATA0 is indicated at the end of the setup stage, and DATA1 is used for responses in the status stage. This does not require the setting of the sequence bit by the software.

Note that the software must also set the data PID sequence bit when sending or receiving a ClearFeature request.

The sequence bit cannot be modified by the SQSET bit for isochronous transfer pipes.

(8) Response PID = NAK Function

This module has a function to disable the pipe operation (Response PID = NAK) at the last data packet receive timing in a transfer (this module automatically identifies the last data packet receive timing at the short packet receive timing or using the transaction counter) by setting the SHTNAK bit in PIPECFG to 1.

This function allows reception of data packets in transfer units when the buffer memory is used as a double buffer. Furthermore, when the pipe operation is disabled, the software must set the response PID to BUF to enable the pipe operation.

This function is available only for bulk transfers.

(9) Auto-Response Mode

When the ATREPM bit in PIPEnCTR is set to 1 in a bulk transfer pipe (pipes 1 to 5, 9 to F), this module enters auto-response mode: OUT-NAK mode in OUT transfers (DIR = 0) or null auto-response mode in IN transfers (DIR = 1).

1. OUT-NAK mode

   When the ATREPM bit is set to 1 in a bulk OUT transfer pipe, this module sends NAK in response to an OUT token or PING token and outputs an NRDY interrupt. To change response mode from normal mode to OUT-NAK mode, specify OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, OUT-NAK mode is enabled. However, if an OUT token is received immediately before the pipe operation is disabled, this module receives the data of the token correctly and sends ACK to the host.

   To change response mode from OUT-NAK mode to normal mode, reset OUT-NAK mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). In normal mode, this module can receive OUT data and sends ACK in response to a PING token when the buffer is ready for receiving.

2. Null auto-response mode

   When the ATREPM bit is set to 1 in a bulk IN transfer pipe, this module continues to send Zero-Length packets. To change response mode from normal mode to null auto-response mode, specify null auto-response mode with the pipe operation disabled (Response PID = NAK), and then enable the pipe operation (Response PID = BUF). After that, null auto-response mode is enabled. However, specify null auto-response mode while the buffer is empty. Verify this by checking INBUFM = 0. Since INBUFM = 1 indicates that the buffer contains data, clear the buffer by setting the ACLRM bit. Do not write data to the buffer from the FIFO port during setting to null auto-response mode.

To change response mode from null auto-response mode to normal mode, delay the pipe operation disabled state (Response PID = NAK) for a time period for sending a Zero-Length packet (full-speed: 10 µs, high-speed: 3 µs), and then reset null auto-response mode. Normal mode allows writing from the FIFO port, and also allows sending packets to the host by enabling the pipe operation (Response PID = BUF).

42.3.4 FIFO Buffer Memory

(1) Allocating FIFO Buffer Memory

Figure 42.9 shows an example of the FIFO buffer memory map of this module. The FIFO buffer memory is an area shared by the CPU and this module. There are two FIFO buffer memory states where the access right is given to the system (CPU) or to this module (SIE).

The FIFO buffer memory provides independent areas for each pipe. A memory area is set with the block start number and the number of blocks (BUFNMB and BUFSIZE bits in PIPEBUF) in 64-byte units as one block.

When continuous transfer mode is selected by the CNTMD bit in PIPEnCFG, be sure to set the BUFSIZE bits to a value in integral multiples of the maximum packet size. When double buffer is selected by the DBLB bit in PIPEnCFG, two sides of the memory area specified by the BUFSIZE bits in PIPEBUF are provided for the same pipe.

Furthermore, three FIFO ports are used for accesses (data read/write) to the buffer memory. The number of a pipe to be allocated to the FIFO ports is specified by the CURPIPE bits in CFIFOSEL and DnFIFOSEL.

The buffer status of each pipe can be monitored by the BSTS and INBUFM bits in DCPCTR and PIPEnCTR. The access right to the FIFO ports can be checked by the FRDY bit in CFIFOCTR and DnFIFOCTR.

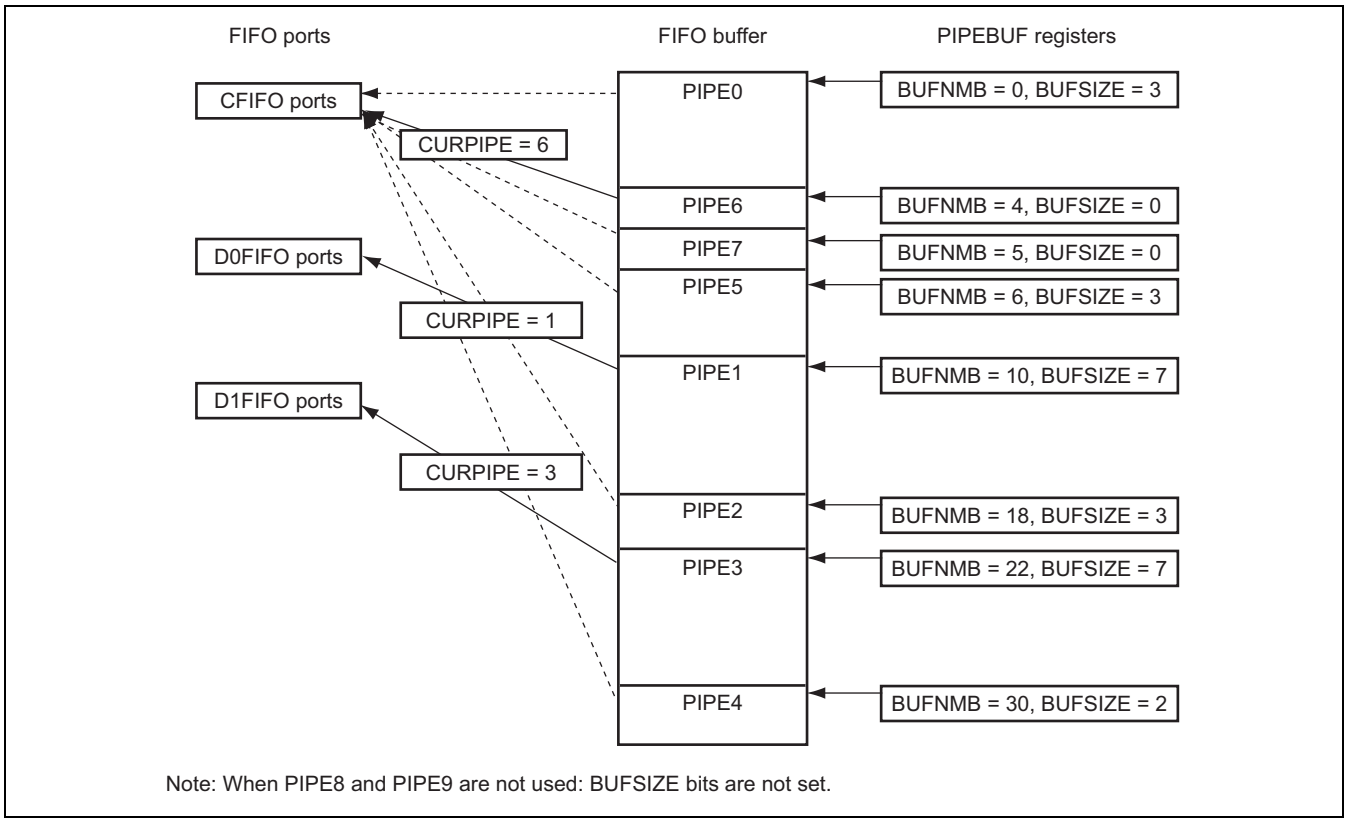


Figure 42.9 Example of Buffer Memory Map

- Buffer status

  Tables 42.14 and 42.15 show the buffer memory status of this module. The buffer memory status can be monitored by the BSTS bit in DCPCTR and the INBUFM bit in PIPEnCTR. The buffer memory access direction is specified by the DIR bit in PIPEnCFG or the ISEL bit in CFIFOSEL (when DCP is selected).

  The INBUFM bit is valid only for pipes 1 to 5, 9 to F in the transmit direction.

  When a transfer pipe in the transmit direction is set to double buffer, the BSTS bit is used to monitor the buffer status on the CPU side, and the INBUFM bit is used to monitor the buffer status on the SIE side. When data write to the FIFO port by the CPU (DMAC) takes time and buffer empty cannot be checked by the BEMP interrupt, the INBUFM bit is available to check completion of transmission.

Table 42.14 Buffer Memory Status That Varies Depending on the BSTS Bit

ISEL or DIR	BSTS	Buffer Memory Status
0 (receive direction)	0	No receive data in the buffer memory or data is being received. Data cannot be read from the FIFO port.
0 (receive direction)	1	Receive data in the buffer memory or a Zero-Length packet is received. Data can be read from the FIFO port. However, the buffer must be cleared because the FIFO port cannot be read when this module receives a Zero-Length packet.
1 (transmit direction)	0	Transmission of data is not completed. Data cannot be written to the FIFO port.
1 (transmit direction)	1	Transmission of data is completed. The CPU can write data to the buffer memory.

Table 42.15 Buffer Memory Status That Varies Depending on the INBUFM Bit

DIR	INBUFM	Buffer Memory Status
0 (receive direction)	Invalid	Invalid
1 (transmit direction)	0	Transmittable data is completely sent. No transmittable data is in the buffer memory.
1 (transmit direction)	1	Transmittable data is written from the FIFO port. The buffer memory contains transmittable data.

- FIFO buffer clear

  Table 42.16 shows clearing of the FIFO buffer memory of this module. The buffer memory can be cleared by the BCLR, DCLRM, and ACLRM bits.

Table 42.16 Buffer Clear

Bit Name	BCLR	DCLRM	ACLRM
Register	CFIFOCTR DnFIFOCTR	DnFIFOSEL	PIPEnCTR
Function	Clears the buffer memory of the CPU.	Automatically clears the buffer memory after reading data of the specified pipe.	Automatically clears the buffer memory by ignoring all received packets.
Clearing method	Writing 1 to this bit clears the buffer memory.	1: This mode is enabled. 0: This mode is disabled.	1: This mode is enabled. 0: This mode is disabled.

- Buffer area

  Table 42.17 shows a buffer memory map of this module. The buffer memory includes dedicated areas reserved beforehand for pipes and user areas provided for user settings.

  The buffer for DCP is a dedicated area commonly used in control read transfers and control write transfers.

  Areas for pipes 6 to 8 are allocated respectively in advance. However, when none of pipes 6 to 8 is used, the areas are available for pipes 1 to 5, 9 to F as user areas.

  Allocate different areas of the buffer memory to each pipe. Note that, when double buffer is specified, the size of an area is twice of the set value.

  Do not set the buffer size to a value smaller than the maximum packet size.

Table 42.17 Buffer Memory Map

Buffer Memory Number	Buffer Size	Pipe Setting	Remarks
H'0	64 bytes	Fixed only for DCP	Single buffer
H'1 to H'3	—	Unavailable	—
H'4	64 bytes	Fixed only for pipe 6	Single buffer
H'5	64 bytes	Fixed only for pipe 7	Single buffer
H'6	64 bytes	Fixed only for pipe 8	Single buffer
H'7 to H'7F	Max. 7616 bytes	User area for pipes 1 to 5, 9 to F	Double buffer and continuous transfer can be set

- Buffer auto-clear mode function

  When the ACLRM bit PIPEnCTR is set to 1, this module discards all data packets received. However, when this module receives a data packet successfully, it sends ACK to the host controller. This function is available only for the buffer memory read direction.

  Writing 1 and then 0 continuously to the ACLRM bit clears the buffer memory of the selected pipe irrespective of the access direction.

  Take at least 100 ns between writing 1 and writing 0 for the sequence execution time of the hardware.
- Buffer memory specifications (single buffer/double buffer setting)

  Single buffer or double buffer is selectable for pipes 1 to 5, 9 to F with the DBLB bit in PIPEnCFG. Double buffer is a function to provide two sides of the memory area specified by the BUFSIZE bits in PIPEBUF for the same pipe. Figure 42.10 shows an example of setting for the buffer memory of this module.

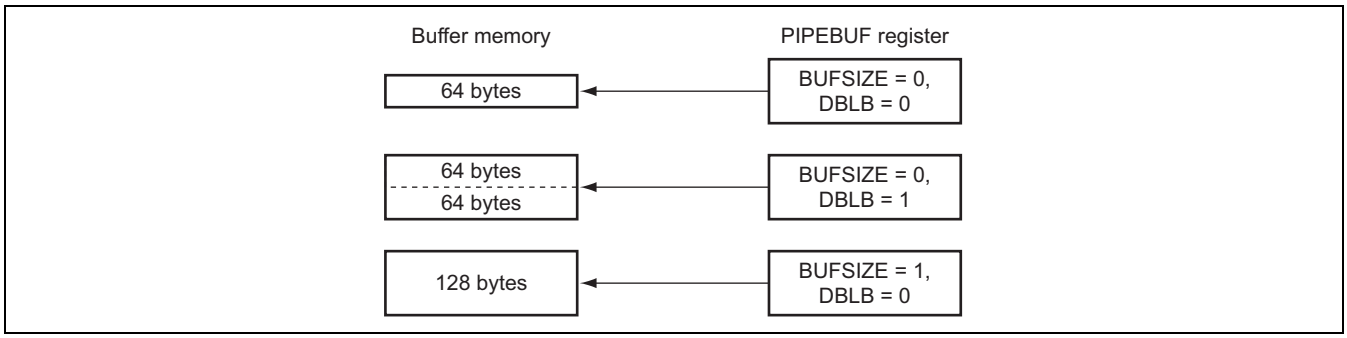


Figure 42.10 Example of Buffer Memory Setting

- Buffer memory operation (continuous transfer setting)

  Continuous transfer mode or discontinuous transfer mode is selectable with the CNTMD bit in PIPEnCFG. This selection is enabled for pipes 1 to 5, 9 to F.

  The continuous transfer mode function allows continuous transmission/reception of multiple transactions. When continuous transfer mode is selected, data up to the buffer size allocated to each pipe can be transferred without outputting an interrupt to the CPU.

  In continuous transmission mode, data in the buffer is divided by the maximum packet size and is then transmitted. To send data less than the buffer size (a short packet or a packet with a size of integral multiples of the maximum packet size and less than the buffer size), set BVAL = 1 after writing transmit data to the buffer.

  In continuous reception mode, no interrupt is generated until this module receives packets to the buffer size, the transaction count ends, or this module receives a short packet.

Table 42.18 shows the relationship between the CNTMD setting and determination of transmission/reception end of the FIFO buffer.

Table 42.18 Relationship between CNTMD Setting and Determination of Transmission/Reception End of FIFO Buffer

Transfer Mode	Determination of Buffer Readable State and Data Transmittable State
Discontinuous transfer (CNTMD = 0)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0): When this module receives one packet
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1): Any of the following cases: The software (or DMAC) writes data of the maximum packet size to the FIFO buffer. The software (or DMAC) writes data of a short packet (including 0 bytes) to the FIFO buffer, and then sets BVAL = 1.
Continuous transfer (CNTMD = 1)	Conditions for FIFO buffer readable state when data receive direction is selected (DIR = 0): When the bytes of data received in the FIFO buffer for the selected pipe equals the allocated bytes ((BUFSIZE + 1) × 64) When this module receives a short packet other than a Zero-Length packet When this module receives a Zero-Length packet when data is already stored in the FIFO buffer for the selected pipe When this module receives packets as large as the transaction counter value specified for the selected pipe by the software
	Conditions for FIFO buffer data transmittable state when data transmit direction is selected (DIR = 1): Any of the following cases: The volume of data written by the software (or DMAC) equals the size of one side of the FIFO buffer for the selected pipe. The software (or DMAC) writes data less than the size of one side of the FIFO buffer for the selected pipe to the FIFO buffer, and then sets BVAL = 1.

Figure 42.11 shows an example of buffer memory operation of this module.

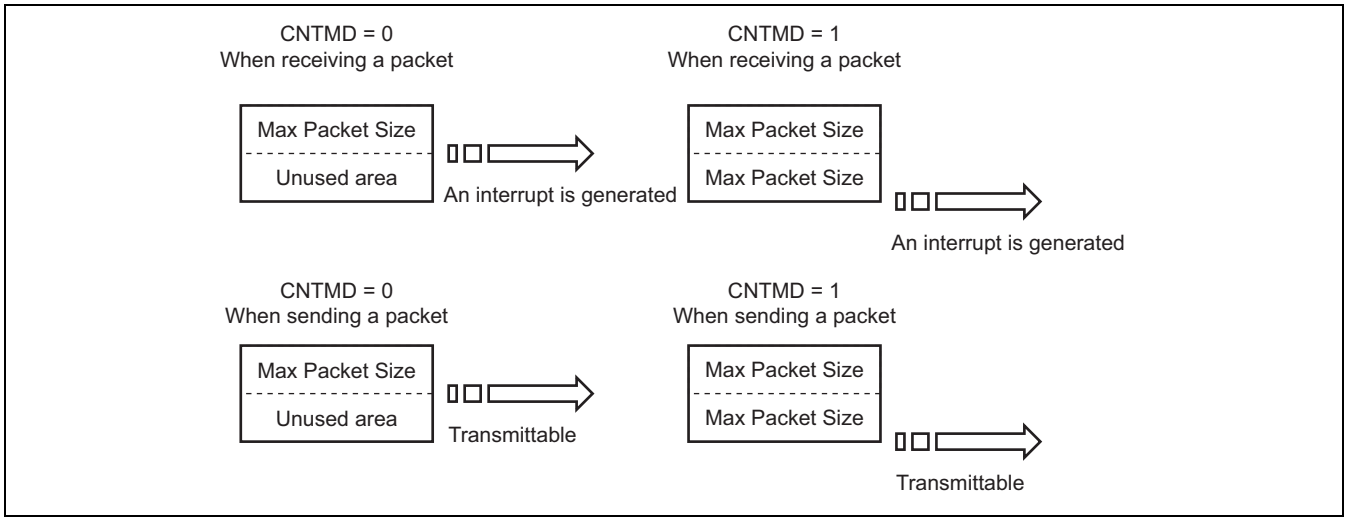


Figure 42.11 Example of Buffer Memory Operation

(2) FIFO Port Function

Table 42.19 lists the settings for the FIFO port functions of this module. During a data write access, when data up to buffer full (or up to the maximum packet size in discontinuous transfer) is written, the FIFO port automatically enters the data transmittable state. To make data less than buffer full (or the maximum packet size in discontinuous transfer) transmittable, set the BVAL bit in CFIFOCTR and DnFIFOCTR to 1 to set write end (DMA transfer: **TEND** signal). For transmission of a Zero-Length packet, clear the buffer using the BCLR bit in these registers and then set the BVAL bit to 1.

During a data read access, when all data is read, the FIFO port automatically enters the new packet receivable state. However, when receiving a Zero-Length packet (DTLN = 0), no data can be read. Therefore, clear the buffer using the BCLR bit in these registers. The receive data length can be checked by the DTLN bits in CFIFOCTR and DnFIFOCTR.

Table 42.19 FIFO Port Function Settings

Register Name	Bit Name	Function	Remarks
CFIFOSEL DnFIFOSEL	RCNT	Selects DTLN read mode.	
	REW	Rewinds the buffer memory (reread/rewrite).	
	DCLRM	Reads and clears receive data of the specified pipe.	DnFIFO only
	DREQE	Enables DMA transfer.	DnFIFO only
	MBW	Specify FIFO port access bit width.	
	BIGEND	Selects FIFO port endian.	
	ISEL	Selects FIFO port access direction.	DCP only
	CURPIPE	Select the current pipe.	
CFIFOCTR DnFIFOCTR	BVAL	Specifies buffer memory write end.	
	BCLR	Clears the buffer memory of the CPU.	
	DTLN	Check receive data length.	

(a) FIFO Port Selection

Table 42.20 shows pipes that can be selected in each FIFO port. Select a pipe to be accessed by the CURPIPE bits in CFIFOSEL and DnFIFOSEL. After selecting a pipe, confirm that the set CURPIPE value is read correctly, check FRDY = 1, and then make an access to the FIFO port. (If the previous pipe number is read, this controller is changing a pipe.)

Also select the bus width to be accessed by the MBW bits. The buffer memory access direction is specified by the DIR bit in PIPEnCFG. However, only the access direction of DCP is determined by the ISEL bit.

Table 42.20 FIFO Port Access

Pipe	Access	Available port
DCP	CPU access	CFIFO port register
Pipes 1 to F	CPU access	CFIFO port register
	DMA access	D0FIFO, D1FIFO, D2FIFO and D3FIFO port

(b) REW Bit

The current access to a pipe can be suspended temporarily, and it is also possible to make an access to another pipe to continue the ongoing pipe processing. This processing is allowed by using the REW bit in CFIFOSEL and DnFIFOSEL.

When the REW bit is set to 1 together with the CURPIPE bits in CFIFOSEL and DnFIFOSEL and a pipe is selected, the reading or writing pointer of the buffer memory is reset, which allows reading or writing data from the first byte. Furthermore, when a pipe is selected with the REW bit set to 0, data can be read or written following the data at the previous selection without resetting the reading or writing pointer of the buffer memory.

To make accesses to the FIFO port, select a pipe and check FRDY = 1.

(3) DMA Transfer (Dedicated DMA Interface)

(a) Overview of DMA Transfer

The FIFO port can be accessed by the DMAC for pipes 1 to F. When the buffer of a pipe specified for DMA transfer becomes accessible, this module outputs a DMA transfer request.

Specify the data transfer unit to the FIFO port by the MBW bits in DnFIFOSEL, and select a pipe used for DMA transfer by the CURPIPE bits in DnFIFOSEL. Do not change the selected pipe during a DMA transfer.

(b) DMA Transfer End Auto-Recognition

This module can terminate writing of data by DMA transfer to the FIFO buffer by controlling the DMA transfer end signal input. After sampling the transfer end signal, this module drives the buffer memory into the transmittable state (same state as BVAL = 1).

(c) DnFIFO Auto-Clear Mode (D0FIFO, D1FIFO, D2FIFO and D3FIFO Port Read Direction)

By setting the DCLRM bit in DnFIFOSEL to 1, this module automatically clears the buffer memory for the selected pipe upon completion of data read from the buffer memory.

Table 42.21 shows the relationship between packet reception and buffer memory clear by the software. As shown in the table, buffer clearing conditions vary with the BFRE setting. However, in any state that needs clearing, using the DCLRM bit makes buffer clearing by the software unnecessary. Thus DMA transfer is enabled without requiring any software control.

- This function is available only for the buffer memory read direction.

Table 42.21 Relationship between Packet Reception and Buffer Memory Clear by the Software

Buffer Status When Receiving a Packet	Register Setting			
	DCLRM = 0		DCLRM = 1	
	BFRE = 0	BFRE = 1	BFRE = 0	BFRE = 1
Buffer full	Clearing not required	Clearing not required	Clearing not required	Clearing not required
Zero-Length packet reception	Clearing required	Clearing required	Clearing not required	Clearing not required
Normal short packet reception	Clearing not required	Clearing required	Clearing not required	Clearing not required
Transaction count end	Clearing not required	Clearing required	Clearing not required	Clearing not required

42.3.5 Control Transfer (DCP)

The default control pipe (DCP) is used for data transfer in the control transfer data stage. The buffer memory for the DCP is a 64-byte single buffer of a fixed area used for both control read and control write. The buffer memory can be accessed only by the CFIFO ports.

(1) Setup Stage

1. This module always sends ACK in response to a normal setup packet to this module. The following describes the operation of this module in the setup stage.
   When this module receives a new setup packet, this module sets the following bits.
   — The VALID bit in INTSTS0 to 1
   — The PID bits in DCPCTR to NAK
   — The CCPL bit in DCPCTR to 0
2. When this module receives a data packet following a setup packet, this module stores the USB request parameters in USBREQ, USBVAL, USBINDX, and USBLENG.

Be sure to process responses to control transfers while VALID = 0. The PID bits cannot be set to BUF when VALID = 1, and therefore the data stage cannot be completed.

With the VALID bit function, this module can suspend the ongoing request processing if this module receives a new USB request during a control transfer, and send a response to the latest request.

This module also determines the direction bit (bit 8 of bmRequestType) of the received USB request and the request data length (wLength), identifies a control read transfer, control write transfer, and control write no-data transfer, and controls stage transitions. For an incorrect sequence, a sequence error of the control transfer stage transition interrupt occurs, and the error is reported to the software. For the stage control of this module, see Figure 42.7.

(2) Data Stage

Transfer data in response to the received USB request using the DCP. Before making an access to the DCP buffer memory, specify the access direction by the ISEL bit in CFIFOSEL.

When the transfer data size is larger than the DCP buffer memory size, use a BRDY interrupt for control write transfers and a BEMP interrupt for control read transfers.

In the high-speed control write transfer, this module sends responses using the NYET handshake according to the buffer memory status.

(3) Status Stage

Setting the CCPL bit to 1 with the PID bits in DCPCTR set to BUF finishes a control transfer.

After these settings, this module executes the status stage as follows according to the data transfer direction determined in the setup stage:

- Control read transfer
  This module sends a Zero-Length packet and receives an ACK response from the USB host.
- Control write transfer, no-data control transfer
  This module receives a Zero-Length packet from the USB host and sends an ACK response.

(4) Control Transfer Auto-Response Function

This module automatically responds to a correct SET_ADDRESS request. If any of the following errors occurs in the SET_ADDRESS request, the software must respond to the error.

- Other than control read transfer: bmRequestType ≠ H'00
- Request errors: wIndex ≠ H'00
- Other than no-data control transfer: wLength ≠ H'00
- Request errors: wValue > H'7F
- Control transfer of device state errors: DVSQ = B'011 (configured)

All requests other than SET_ADDRESS require a response made by the software.

42.3.6 Bulk Transfer (Pipes 1 to 5, 9 to F)

The buffer memory usage (single buffer/double buffer setting or continuous/discontinuous transfer mode setting) can be selected for bulk transfers. The buffer memory size can be set to up to 2 Kbytes. This module manages the buffer memory status and automatically responds to a PING packet and an NYET handshake.

(1) NYET Handshake Control

Table 42.22 lists NYET handshake responses of this module. This module sends a NYET response under the following conditions. However, when this module receives a short packet, this module sends ACK instead of NYET. The same is true of the control write transfer data stage.

Table 42.22 NYET Handshake Responses

Setting of PID Bits in DCPCTR	Buffer Memory Status	Token	Response	Remarks
NAK/STALL	—	SETUP	ACK	—
	—	IN/OUT/PING	NAK/STALL	—
BUF	—	SETUP	ACK	—
	RCV-BRDY1	OUT/PING	ACK	Receives a data packet when receiving an OUT token.
	RCV-BRDY2	OUT	NYET	Receives a data packet. Sends a “reception disable” response.
	RCV-BRDY2	OUT (Short)	ACK	Receives a data packet. Sends a “reception enable” response.
	RCV-BRDY2	PING	ACK	Sends a “reception enable” response.
	RCV-NRDY	OUT/PING	NAK	Sends a “reception disable” response.
	TRN-BRDY	IN	DATA0/1	Sends a data packet.
	TRN-NRDY	IN	NAK	TRN-NRDY

[Legend]
RCV-BRDY1: The buffer memory has available space for two packets or more when receiving an OUT or PING token.
RCV-BRDY2: The buffer memory has available space for only one packet when receiving an OUT token.
RCV-NRDY: The buffer memory is occupied when receiving an PING token.
TRN-BRDY: The buffer memory contains transmit data when receiving an IN token.
TRN-NRDY: The buffer memory contains no transmit data when receiving an IN token.

42.3.7 Interrupt Transfer (Pipes 6 to 8 and A)

This module performs interrupt transfer following the cycles controlled by the host controller. In interrupt transfers, this module ignores PING packets (no response), sends no NYET handshake, and sends ACK, NAK, and STALL responses.

This module does not support the High-Bandwidth interrupt transfer.

42.3.8 Isochronous Transfer (Pipes 1, 2)

This module is provided with the following functions for isochronous transfers.

- Reporting isochronous transfer error information
- Interval counter (IITV bits)
- Isochronous IN transfer data setup control (IDLY function)
- Isochronous IN transfer buffer flush function (IFIS bit)

This module does not support the isochronous High-Bandwidth transfer.

(1) Isochronous Transfer Error Detection

This module is provided with a function to detect the following error information so that the software can manage isochronous transfer errors. Tables 42.23 and 42.24 show the error detection priority of this module and interrupts generated as a result of error detection.

1. PID error
   — When the PID in a receive packet is invalid
2. CRC error, bit stuffing error
   — When a CRC error is found in a receive packet or bit stuffing is invalid
3. Maximum packet size exceeded error
   — When the data size of a receive packet is over the maximum packet size setting
4. Overrun/underrun error
   — When the buffer memory contains no data when this module receives an IN token in the IN direction (transmission) transfer
   — When the buffer memory is occupied when this module receives an OUT token in the OUT direction (reception) transfer
5. Interval error
   This module generates an interval error in the following cases.
   — When no IN token can be received in interval frames in the isochronous IN transfer
   — When this module receives an OUT token other than interval frames in the isochronous OUT transfer

Table 42.23 Error Detection when Receiving Tokens

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet).
2	CRC error, bit stuffing error	This module generates no interrupt (ignores as a damaged packet).
3	Overrun error, underrun error	This module generates an NRDY interrupt and sets the OVRN bit. This module sends a Zero-Length packet in response to the IN token. This module receives no data packet in response to the OUT token.
4	Interval error	This module generates an NRDY interrupt.

Table 42.24 Error Detection when Receiving Data Packets

Priority for Error Detection	Error	Interrupt and Status
1	PID error	This module generates no interrupt (ignores as a damaged packet).
2	CRC error, bit stuffing error	This module generates an NRDY interrupt and sets the CRCE bit.
3	Maximum packet size exceeded error	This module generates a BEMP interrupt and sets the PID bits to STALL.

(2) DATA-PID

This module does not support the High-Bandwidth transfer. The following lists responses to received PIDs when the function controller function is selected.

1. IN direction
   - DATA0: Sent correctly as the PID of data packet.
   - DATA1: Not sent
   - DATA2: Not sent
   - mDATA: Not sent
2. OUT direction (full-speed operation)
   - DATA0: Received correctly as the PID of a data packet.
   - DATA1: Received correctly as the PID of a data packet.
   - DATA2: The packet is ignored.
   - mDATA: The packet is ignored.
3. OUT direction (high-speed operation)
   - DATA0: Received correctly as the PID of a data packet.
   - DATA1: Received correctly as the PID of a data packet.
   - DATA2: Received correctly as the PID of a data packet.
   - mDATA: Received correctly as the PID of a data packet.

(3) Interval Counter

Intervals for isochronous transfers can be set by the IITV bits in PIPEPERI. The functions shown in Table 42.25 are made available with the interval counter.

Table 42.25 Interval Counter Functions

Transfer Direction	Function	Detection Conditions
IN	Transmit buffer flush	No IN token can be successfully received in the interval frame during the isochronous IN transfer.
OUT	Reporting reception of no token	No OUT token can be successfully received in the interval frame during the isochronous OUT transfer.

Since the interval counter is counted upon receiving an SOF or using the interpolated SOF, the isochronism can be maintained even if the SOF is damaged. The specifiable frame interval is 2^{IITV} frames or 2^{IITV} μ frames.

(a) Counter initialization

This module initializes the interval counter as follows:

- Power-on reset
  The IITV bits are initialized.
- Initializing buffer memory by ACLRM
  The IITV bits are not initialized but the interval counter is initialized. Clearing the ACLRM bit to 0 causes the counter to start counting from the set IITV value.
- USB bus reset.

After the interval counter is initialized, the interval counter starts counting in either of the following cases after a packet is correctly transferred.

1. When this module receives an SOF after sending data in response to the IN token with PID = BUF
2. When this module receives an SOF after receiving the OUT token data with PID = BUF

The interval counter is not initialized under the following conditions.

1. When PID = NAK or STALL
   The interval timer does not stop. Try to execute the transaction in the next interval.
2. USB bus reset and USB suspended
   The IITV bits are not initialized. When this module receives an SOF, the interval counter starts counting from the value before receiving the SOF.

(b) Interval count and transfer control

1. When the selected pipe is Isochronous-OUT transfer pipe
   When this module receives no data packet in (μ) frames at the intervals specified by the IITV bits, this controller generates an NRDY interrupt.
   When this module cannot receive data due to a CRC error in the data packet, FIFO buffer full, or other reasons, this module also generates an NRDY interrupt.
   An NRDY interrupt is generated at the SOF packet receive timing. Even if the SOF packet is damaged, this module generates an NRDY interrupt at the SOF packet receive timing using the internal interpolation function.
   When IITV ≠ 0, however, this module generates an NRDY interrupt at the SOF packet receive timing in each interval after the interval count starts.
   When PID = NAK is set by the software after the interval timer is activated, this module generates no NRDY interrupt even when this module receives an SOF packet.

The interval count start conditions vary with the set IITV value.

— When IITV = 0: The interval count starts from the next (μ) frame where the PID bits for the selected pipe is changed to BUF.

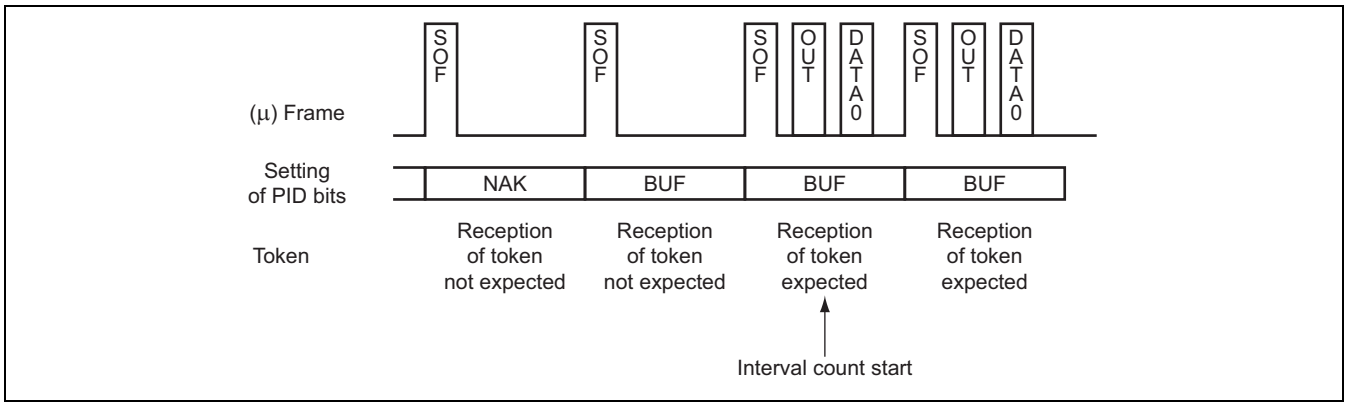


Figure 42.12 (μ) Frames and Expectation of Receiving a Token when IITV = 0

— When IITV ≠ 0: The interval count starts from the time when this module successfully receives the first data packet after the PID bits for the selected pipe is changed to BUF.

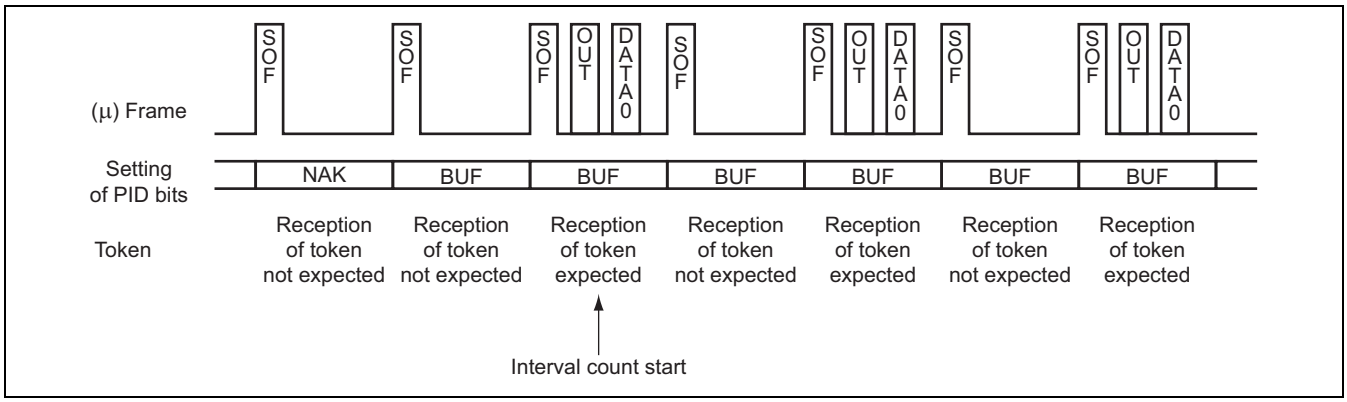


Figure 42.13 (μ) Frames and Expectation of Receiving a Token when IITV ≠ 0

2. When the selected pipe is Isochronous-IN transfer pipe

Use the selected pipe by combining with the setting of IFIS = 1. When IFIS = 0, this module sends data packets in response to received tokens irrespective of the IITV value.

When this module receives no IN-Token in (μ) frames at the intervals specified by the IITV bits with transmittable data stored in the FIFO buffer with IFIS = 1, this module clears the FIFO buffer.

When this module cannot receive data due to a CRC error or another bus error in the IN-Token, this module also clears the FIFO buffer.

The FIFO buffer is cleared at the SOF packet receive timing. Even if the SOF packet is damaged, this module clears the FIFO buffer at the SOF packet receive timing using the internal interpolation function.

The interval count start conditions vary with the set IITV value (same as Isochronous-OUT transfer).

When the function controller function is selected, the interval count start conditions are as follows:

— When this module is reset by the hardware (The set IITV value is also cleared to 0.)

— When ACLRM is set to 1 by the software

— When this module detects a USB reset

(4) Transmit Data Setup in Isochronous Transfer

In isochronous data transmission is selected, this module can send a data packet in the next frame after this module detects an SOF packet after writing data to the buffer. This function is referred to as the isochronous transfer transmit data setup function. With this function, the frame that started data transmission can be identified.

When the buffer memory is used as a double buffer, even if writing data to both buffers is completed, only one side that finished writing earlier becomes transferable. For this reason, even if multiple IN tokens are received in the same frame, only one packet of the buffer memory is sent.

When the buffer memory is ready for transmission in the IN token reception cycle, this module sends data and an ACK response. However, when the buffer memory is not ready for transmission, this module sends a Zero-Length packet and generates an underrun error.

Figure 42.14 shows an example of transmission using the isochronous transfer transmit data setup function of this module when IITV = 0 (each frame). Transmission of a Zero-Length packet is indicated as hatched “Null” in the figure.

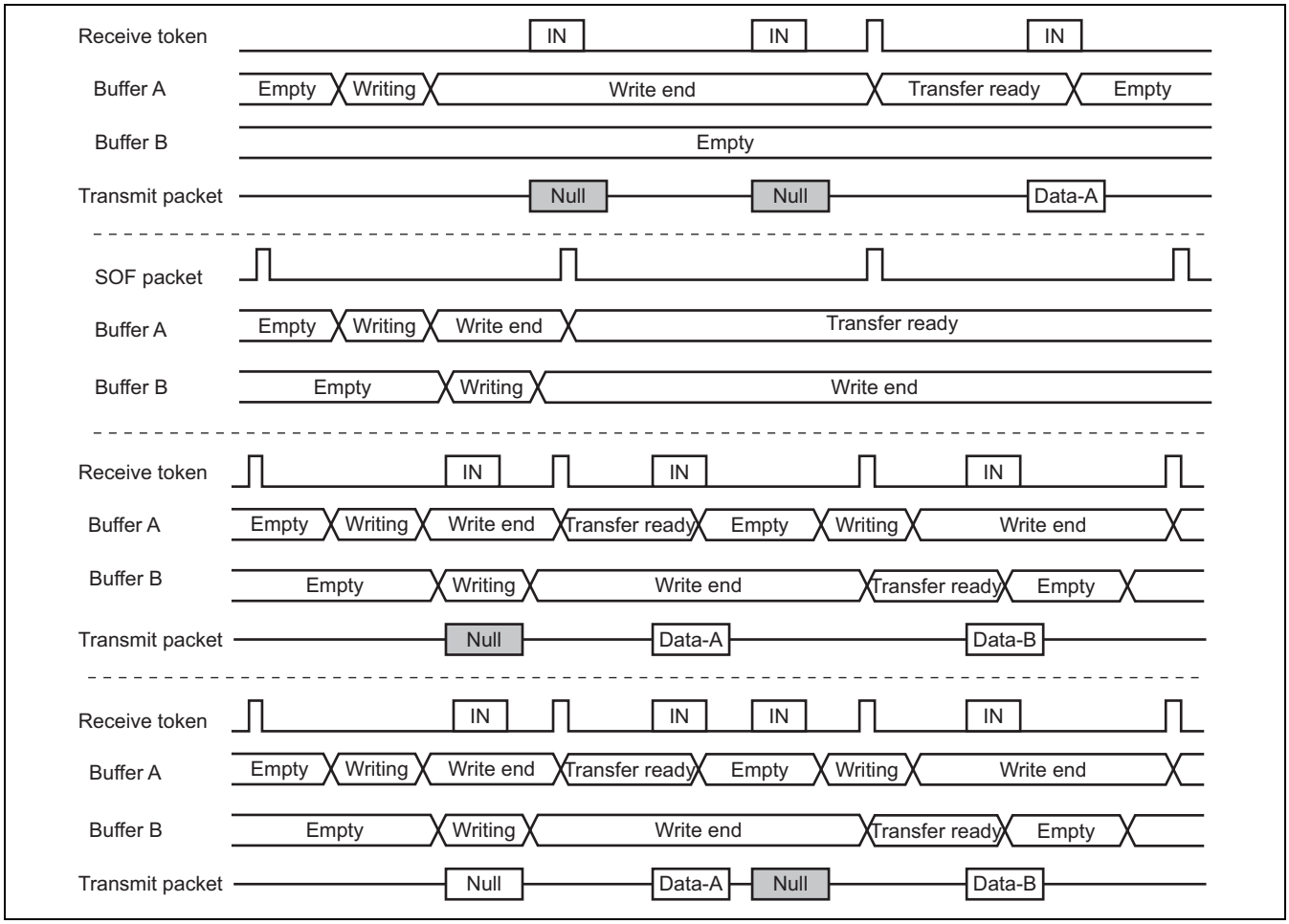


Figure 42.14 Example of Transmit Data Setup Function

(5) Transmit Buffer Flush in Isochronous Transfer

In isochronous data transmission is selected, this module receives no IN token in the interval frame. When this module receives the SOF or µ SOF packet of the next frame, this module regards the IN token as damaged and clears the buffer that is ready for transmission to make it writable.

At this time, when the buffer memory is used as a double buffer and writing data to both buffers is completed, this module regards the discarded buffer memory data as transmitted in the same interval frame, and drives the buffer memory that is not discarded due to the reception of an SOF or µ SOF packet into the transmission ready state.

The buffer flush function activation timing varies depending on the IITV value.

- When IITV = 0
  This module activates the buffer flush function from the next frame after the pipe is enabled.
- When IITV ≠ 0
  This module activates the buffer flush function from the first normal transaction.

Figure 42.15 shows an example of the buffer flush function of this module. For tokens before the interval frame (outside the specified interval), however, this module sends the data stored in the buffer according to the data setup state or sends a Zero-Length packet as an underrun error.

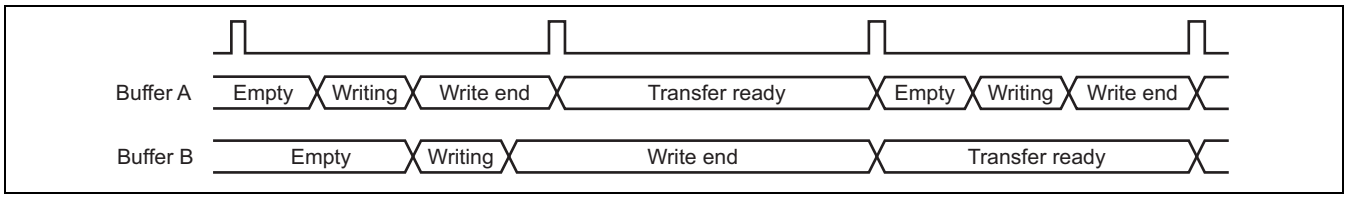


Figure 42.15 Example of Buffer Flush Function

Figure 42.16 shows an example of an interval error of this module. Interval errors are the following five. An interval error occurs at timing [1] in the figure, and the buffer flush function is activated.

When an interval error occurs, the buffer flush function is activated in the IN transfer and an NRDY interrupt occurs in the OUT transfer. Discriminate an NRDY interrupt (including a receive packet error) from an overrun error with the OVRN bit.

This module sends a response to the hatched tokens in the figure according to the buffer memory status.

1. IN direction
   — When the buffer is ready to transmit data, this module sends the data and an ACK response.
   — When the buffer is not ready to transmit data, this module sends a Zero-Length packet and generates an underrun error.
2. OUT direction
   — When the buffer is ready to receive data, this module receives data and sends an ACK response.
   — When the buffer is not ready to receive data, this module discards the data and generates an overrun error.

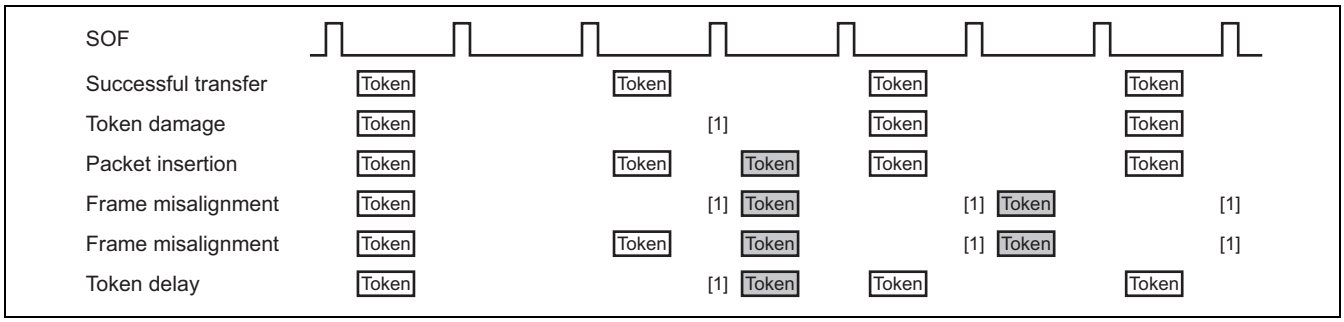


Figure 42.16 Example of Interval Error when IITV = 1

42.3.9 SOF Interpolation Function

In case this module cannot receive SOF packets at intervals of 1 ms (full-speed operation) or 125 µs (high-speed operation) due to damage or missing of SOF packets, this module interpolates the SOF. The SOF interpolation starts functioning when SYSCFG.USBE = 1 and at the SOF packet receive timing. Furthermore, the interpolation function is initialized in the following cases.

- Power-on reset
- USB bus reset
- When the suspended state is detected

The SOF interpolation functions with the following specifications.

- The frame intervals (125 µs or 1 ms) conform to the result of the reset handshake protocol.
- The SOF interpolation does not function until this module receives an SOF packet.
- After receiving the first SOF packet, 125 µs or 1 ms is counted by the internal 48-MHz clock to interpolate the SOF.
- After receiving the second SOF packet or a following packet, the SOF is interpolated using the previous receive intervals.
- The SOF interpolation does not function in the suspended state and during a USB bus reset.
  (When this module enters the suspended state in high-speed operation, the SOF interpolation continues for 3 ms from the final packet.)

This module activates the following functions based on the reception of SOF packets. When one or more SOF packets are lost, normal operation can be continued to perform the SOF interpolation.

- Updating frame numbers and µ frame numbers
- SOFR interrupt timing and µ SOF lock
- SOF pulse output
- Isochronous transfer interval count

When one or more SOF packets are lost in full-speed operation, the FRNM bits in FRMNUM are not updated. When one or more µ SOF packets are lost in high-speed operation, the UFRNM bits in the UFRMNUM are updated. However, when a µ SOF packet with UFRNM = B'000 is lost, the FRNM bits are not updated even if following µ SOF packets with UFRNM ≠ B'000 are successfully received.

42.4 Guidelines for Designing USB2.0 Hi-Speed Boards

42.4.1 USB Transmission Line.

The USB transmission line indicates the pattern that connects the USB connector and the USB transceiver with built-in this LSI.

The USB2.0 has three communication modes: Hi-Speed, Full-Speed and Low-Speed modes. The transmission speed in the Hi-Speed mode is 480 Mbps. Therefore, the USB transmission line must be designed as a high-frequency circuit. Impedance control is required for the USB transmission line.

- The characteristic impedance required for the USB Hi-Speed transmission line is differential impedance 90 Ω (±15%).
- The pattern width and pattern pitch for impedance control vary depending on the board thickness, material and layer configuration. For details, consult the board manufacturer.
- A maximum delay of 1 ns is allowed from the USB connector to this LSI. Therefore it is recommended that the pattern length from the USB device to the USB connector is less than 50 mm and the difference between the pattern lengths for D+ and D− is less than 2.5 mm for a generic PCB.
- The lower layer of the USB transmission line must be a solid ground plane. The ground must be wider than the USB transmission line by 2 mm or more. The power supply for a solid ground plane is VSS.
- Do not allocate other signal lines near to the USB transmission line. In particular, lines carrying widely fluctuating signals, such as clock and data bus lines, must be assigned far from the USB transmission line. Furthermore, layout of the USB transmission lines must be such that they do not cross with other signal lines.
- Locate the USB transmission line on the same layer without passing it through a through-hole. Do not create stubs.
- Place the USB transmission lines so that they are equally spaced from each other.
- Locate the USB transmission line as far as possible from the oscillator, power supply circuit, and other I/O connectors.
- Try to avoid bending the USB transmission line as far as possible. If it is absolutely necessary to bend it, do not bend it at acute or right angles. Bend it moderately, at not more than 45 degrees, or bend it into an arc.
- It is recommended to guard ring the clock, reset, read, write and chip select signals with grounds.

When a resistance is connected to the USB transmission line, locate it near to the USB transmission line. The connecting wire must be as short as possible.

42.4.2 Power Supply and Ground Pattern

Analog power supply:	VCCQA_USB(3.3 V), VDDA_USBPLL(1.2V)
Digital power supply:	VDD(1.2V), VCCQ(3.3V)
Analog ground:	VSSA_USB
Digital ground:	VSS

- It is recommended to separate power supplies and ground patterns into digital and analog.
- Connect the power supplies and grounds firmly on wide areas.
- Tantalum solid electrolytic capacitors or ceramic capacitors having excellent high-frequency characteristics are recommended as capacitors for power supplies.
- Aluminum electrolytic capacitors affect the jitter value during measurement of EYE diagram. Use the capacitors after adequately designing and testing them.
- It is recommended to place decoupling capacitors with values of 0.1 µF, 0.01 µF, and 0.001 µF as close as possible to the USB power supply.

42.4.3 Oscillation

- USB clock is supplied by the internal PLL.
- Provide an oscillation circuit near the clock input pin for USB (EXTAL). It is recommended to guard ring EXTAL with a ground.
- When using a crystal resonator, consult its manufacturer to determine the circuit constant.

42.4.4 VBUS

- The HS-USB subsystem can connect 5V VBUS signal to USB0_VBUS and USB1_VBUS pin. It enables to detect VBUS level but it can’t supply power to device.

42.4.5 RREF Pin

- Provide a resistor (hereafter called reference resistor) of 5.6kΩ ±1%, between the RREF pin and VSSA_USB.
- Locate the reference resistor as close as possible to this LSI.
- The RREF pin, the reference resistor, VSSA_USB should be wired on wide areas and the shortest length.
- Use a wiring pattern for and only for the reference resistor, VSSA_USB. The pattern should be connected to the analog ground. The pattern should be designed avoiding the possibility for common impedance between RREF and other signals.
- To prevent cross talk, very-frequently switched signals such as DP, DM, clocks, and control signals for addresses and data, should not be placed near to the reference resistor, and their patterns should neither get across nor go parallel to the wiring pattern between the reference resistor and the RREF pin.

It is recommended to guard ring the reference resistor and its wiring pattern with ground.

43. USB High-Speed DMAC (USB-DMAC)

43.1 Overview

43.1.1 Features

- Three types of clock: ZSϕ, HPϕ and HS-USB local bus clock (48 MHz), which are asynchronously absorbed in the local bus bridge and AXI bus bridge.
- The AXI bus interface functions are implemented.
- The AXI bus interface handles data transfer with the memory and register settings.
- Data communication is performed using the local DMA protocol.
- Supports two channels that can work concurrently.
- Interrupts
  - Setting count end interrupt
  - USB-DMAC is composed of USB-DMAC0 and USB-DMAC1. There are 2 channels in USB-DMAC0 and 2 channels in USB-DMAC1.
  - Transfer end interrupt upon receiving a short packet from the USB-IP

    This function allows generation of an interrupt even in the case where DMA transfer ends after receiving data less than the transfer size set in the DMAC.
  - Timeout interrupt

    A timeout interrupt can be generated after the specified cycles after the last HS-USB transfer request. (This interrupt is used for the timeout when the final packet received is Max packet.)
  - Interrupts can also be generated when a NULL packet is received or an address error is detected.

Table 43.1 Main Functions of This Module

Item	Description
Application	Transfer between USB-IP (FIFO) and AXI bus (4-Gbyte arbitrary space)
Purpose of DMA transfer	High-speed data transfer between USB-IP and AXI bus
DMA transfer end notification to the software	Interrupt signals (transfer count end, USB-IP short packet reception, timeout, etc.)
Transfer space/transfer address direction	4-Gbyte arbitrary space (forward direction) to 4-Gbyte arbitrary space (forward direction)
Maximum transfer count	16,777,216
Transfer unit	8, 16, or 32 bytes
Control signals generated	Address/data read/data write conforming to the USB-IP local bus interface and AXI bus protocols
Number of channels	2 (parallel operation enabled)
Bus specification	AXI bus, local bus (USB-IP local bus)
Clock	AXI bus clock (ZSϕ: 260 MHz), HPB bus clock (HPϕ: 130 MHz) USB local bus clock (48 MHz) Note: The restrictions of ratio of the clock ZSϕ ≥ HPϕ ≥ 48 MHz Please don't change the clock frequency during USB-DMAC0 or USB-DMAC1 transferring.

Item	Description
Maximum transfer rate	IN transfer: About 350 Mbps (USB-DMAC0) OUT transfer: About 340 Mbps (USB-DMAC0) IN transfer: About 175 Mbps (USB-DMAC1) OUT transfer: About 170 Mbps (USB-DMAC1)

Table 43.2 Bus Access Type

	Supported Access Type
AXI bus access (USB-DMAC master)	8-byte read/write 16-byte read/write 32-byte read/write
USB-DMAC register setting	4-byte read/write 8-byte read/write

The configuration of this module is shown below.

This module is provided with buffers and bus bridges and controls transfers between the AXI bus and USB High-Speed module (HS-USB).

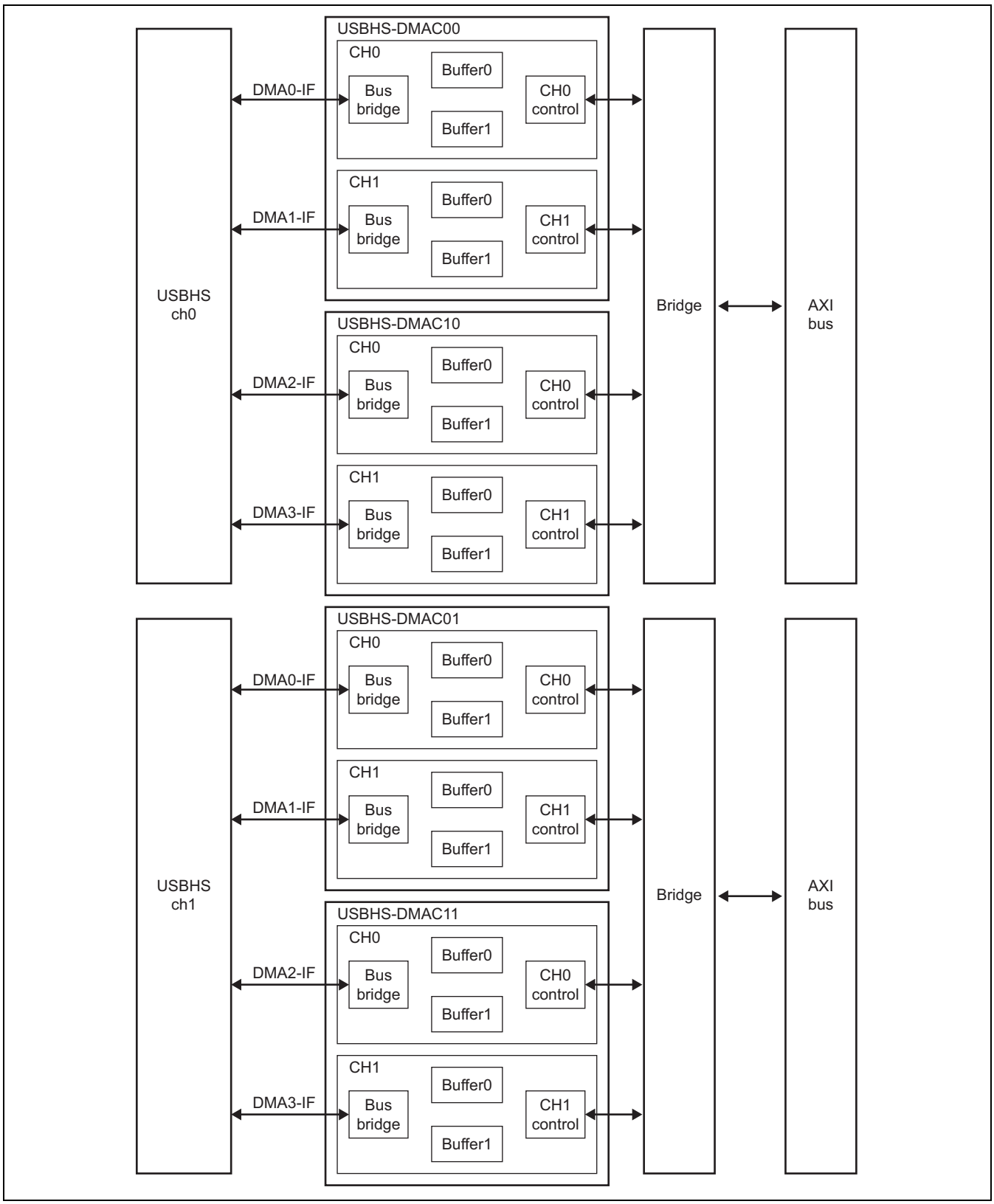


Figure 43.1 USB-DMAC Configuration

43.2 Register Descriptions

USB-DMAC Base Address

USB-DMAC	Base Address
USB-DMAC00	H'E65A 0000
USB-DMAC10	H'E65B 0000
USB-DMAC01	H'E65A 8000
USB-DMAC11	H'E65B 8000

Table 43.3 shows the register configuration. Table 43.4 shows the register states in each processing mode.

Table 43.3 Register Configuration

Register Name	Abbreviation	R/W	Address Offset	Access Size
DMA0 VCR register	USBDMA0_VCR	R/W	H'000	32
DMA0 Software reset register	USBDMA0_SWR	R/W	H'008	32
DMA0 interrupt source register	USBDMA0_DMICR	R	H'010	32
DMA0 source address register_0	USBDMA0_SAR_0	R/W	H'020	32
DMA0 destination address register_0	USBDMA0_DAR_0	R/W	H'024	32
DMA0 transfer count register_0	USBDMA0_TCR_0	R/W	H'028	32
DMA0 timeout count register_0	USBDMA0_TOCNTR_0	R	H'02C	32
DMA0 timeout constant register_0	USBDMA0_TOCSTR_0	R/W	H'030	32
DMA0 channel control register_0	USBDMA0_CHCR_0	R/W	H'034	32
DMA0 final transaction valid data transfer enable register_0	USBDMA0_TEND_0	R/W	H'038	32
DMA0 source address register_1	USBDMA0_SAR_1	R/W	H'040	32
DMA0 destination address register_1	USBDMA0_DAR_1	R/W	H'044	32
DMA0 transfer count register_1	USBDMA0_TCR_1	R/W	H'048	32
DMA0 timeout count register_1	USBDMA0_TOCNTR_1	R	H'04C	32
DMA0 timeout constant register_1	USBDMA0_TOCSTR_1	R/W	H'050	32
DMA0 channel control register_1	USBDMA0_CHCR_1	R/W	H'054	32
DMA0 final transaction valid data transfer enable register_1	USBDMA0_TEND_1	R/W	H'058	32
DMA0 operation register	USBDMA0_DMAOR	R/W	H'060	32
DMA1 VCR register	USBDMA1_VCR	R/W	H'000	32
DMA1 Software reset register	USBDMA1_SWR	R/W	H'008	32
DMA1 interrupt source register	USBDMA1_DMICR	R	H'010	32
DMA1 source address register_0	USBDMA1_SAR_0	R/W	H'020	32
DMA1 destination address register_0	USBDMA1_DAR_0	R/W	H'024	32
DMA1 transfer count register_0	USBDMA1_TCR_0	R/W	H'028	32
DMA1 timeout count register_0	USBDMA1_TOCNTR_0	R	H'02C	32
DMA1 timeout constant register_0	USBDMA1_TOCSTR_0	R/W	H'030	32
DMA1 channel control register_0	USBDMA1_CHCR_0	R/W	H'034	32
DMA1 final transaction valid data transfer enable register_0	USBDMA1_TEND_0	R/W	H'038	32
DMA1 source address register_1	USBDMA1_SAR_1	R/W	H'040	32
DMA1 destination address register_1	USBDMA1_DAR_1	R/W	H'044	32

Register Name	Abbreviation	R/W	Address Offset	Access Size
DMA1 transfer count register_1	USBDMA1_TCR_1	R/W	H'048	32
DMA1 timeout count register_1	USBDMA1_TOCNTR_1	R	H'04C	32
DMA1 timeout constant register_1	USBDMA1_TOCSTR_1	R/W	H'050	32
DMA1 channel control register_1	USBDMA1_CHCR_1	R/W	H'054	32
DMA1 final transaction valid data transfer enable register_1	USBDMA1_TEND_1	R/W	H'058	32
DMA1 operation register	USBDMA1_DMAOR	R/W	H'060	32

Table 43.4 Register States in Each Processing Mode

Abbreviation	Power-On Reset	Module Standby
USBDMA0_VCR	Initialized	Retained
USBDMA0_SWR	Initialized	Retained
USBDMA0_DMICR	Initialized	Retained
USBDMA0_SAR_0	Initialized	Retained
USBDMA0_DAR_0	Initialized	Retained
USBDMA0_TCR_0	Initialized	Retained
USBDMA0_TOCNTR_0	Initialized	Retained
USBDMA0_TOCSTR_0	Initialized	Retained
USBDMA0_CHCR_0	Initialized	Retained
USBDMA0_TEND_0	Initialized	Retained
USBDMA0_SAR_1	Initialized	Retained
USBDMA0_DAR_1	Initialized	Retained
USBDMA0_TCR_1	Initialized	Retained
USBDMA0_TOCNTR_1	Initialized	Retained
USBDMA0_TOCSTR_1	Initialized	Retained
USBDMA0_CHCR_1	Initialized	Retained
USBDMA0_TEND_1	Initialized	Retained
USBDMA0_DMAOR	Initialized	Retained
USBDMA1_VCR	Initialized	Retained
USBDMA1_SWR	Initialized	Retained
USBDMA1_DMICR	Initialized	Retained
USBDMA1_SAR_0	Initialized	Retained
USBDMA1_DAR_0	Initialized	Retained
USBDMA1_TCR_0	Initialized	Retained
USBDMA1_TOCNTR_0	Initialized	Retained
USBDMA1_TOCSTR_0	Initialized	Retained
USBDMA1_CHCR_0	Initialized	Retained
USBDMA1_TEND_0	Initialized	Retained
USBDMA1_SAR_1	Initialized	Retained
USBDMA1_DAR_1	Initialized	Retained
USBDMA1_TCR_1	Initialized	Retained
USBDMA1_TOCNTR_1	Initialized	Retained
USBDMA1_TOCSTR_1	Initialized	Retained
USBDMA1_CHCR_1	Initialized	Retained
USBDMA1_TEND_1	Initialized	Retained
USBDMA1_DMAOR	Initialized	Retained

43.2.1 DMA0/1 VCR Register (USBDMA0_VCR/USBDMA1_VCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERR_SNT	ERR_RCV
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	ERR_SNT	0	R/W	Send Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.
0	ERR_RCV	0	R/W	Receive Error Response 0: No error is generated. [Clearing condition] Writing 0 after reading 1. 1: An error is generated.

43.2.2 DMA0/1 Software Reset Register (USBDMA0_SWR/USBDMA1_SWR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	SWR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	SWR	0	R/W	Software Reset 0: Cancels reset. 1: Resets entire system. (No effect for register setting) Note: On software reset, this bit should be held high for long enough until the internal circuit stabilizes. When this bit is set to 1, it is recommended to allow several tens of clocks if operating at 260 MHz for a reset period before clearing the reset (setting this bit to 0) as a precaution.

43.2.3 DMA0/1 Interrupt Source Register (USBDMA0_DMICR/USBDMA1_DMICR)

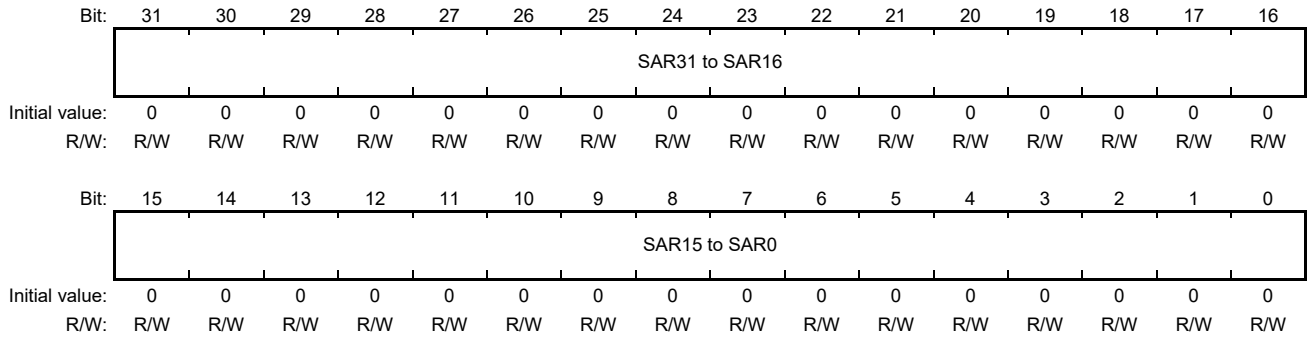
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	SHBSY1	—	—	—	—	—	—	—	SHBSY0	—	—	—	—	—	—	AE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	TR1	BUF1	RW1	NULL1	TO1	SP1	TE1	—	TR0	BUF0	RW0	NULL0	TO0	SP0	TE0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31	SHBSY1	0	R	CH1 AXI Bus Busy Flag Monitor 0: The AXI bus is idle. 1: The AXI bus is busy.
30 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	SHBSY0	0	R	CH0 AXI Bus Busy Flag Monitor 0: The AXI bus is idle. 1: The AXI bus is busy.
22 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	AE	0	R	Address Error Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (AE in the DMA operation register is reflected.)
15	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
14	TR1	0	R	CH1 Transaction End: Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 1 control register is reflected.)
13	BUF1	0	R	CH1 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 1 control register is reflected.)
12	RW1	0	R	CH1 Final Buffer Access Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 1 control register is reflected.)
11	NULL1	0	R	CH1 NULL Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 1 control register is reflected.)

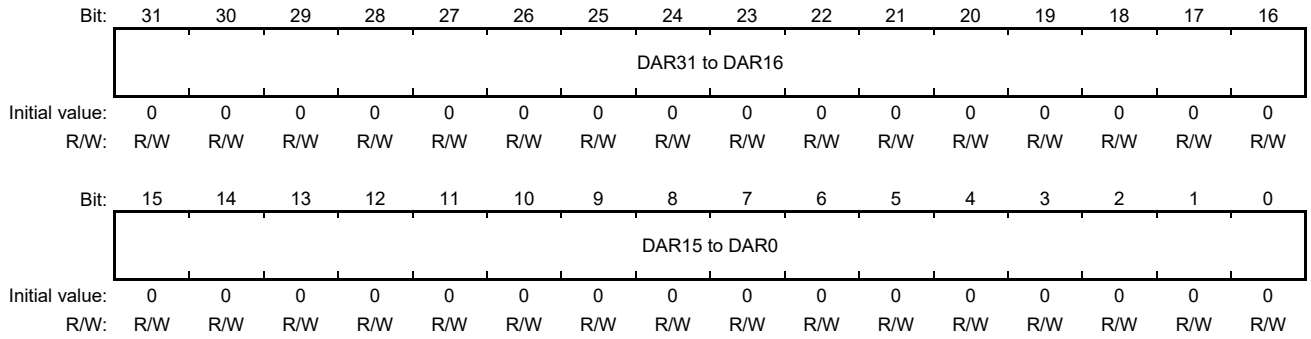
Bit	Bit Name	Initial Value	R/W	Description
10	TO1	0	R	CH1 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 1 control register is reflected.)
9	SP1	0	R	CH1 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 1 control register is reflected.)
8	TE1	0	R	CH1 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 1 control register is reflected.)
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	TR0	0	R	CH0 Transaction End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TR in the channel 0 control register is reflected.)
5	BUF0	0	R	CH0 Buffer End Detect Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (BUF in the channel 0 control register is reflected.)
4	RW0	0	R	CH0 RWEND Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (RW in the channel 0 control register is reflected.)
3	NULL0	0	R	CH0 NULL Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (NULL in the channel 0 control register is reflected.)
2	TO0	0	R	CH0 Timeout Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TO in the channel 0 control register is reflected.)
1	SP0	0	R	CH0 Short Packet Receive Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (SP in the channel 0 control register is reflected.)
0	TE0	0	R	CH0 Transfer End Interrupt Source 0: No interrupt is generated. 1: An interrupt is generated. (TE in the channel 0 control register is reflected.)

43.2.4 DMA0/1 Source Address Registers 0 and 1 (USBDMA0_SAR_0/USBDMA1_SAR_1)



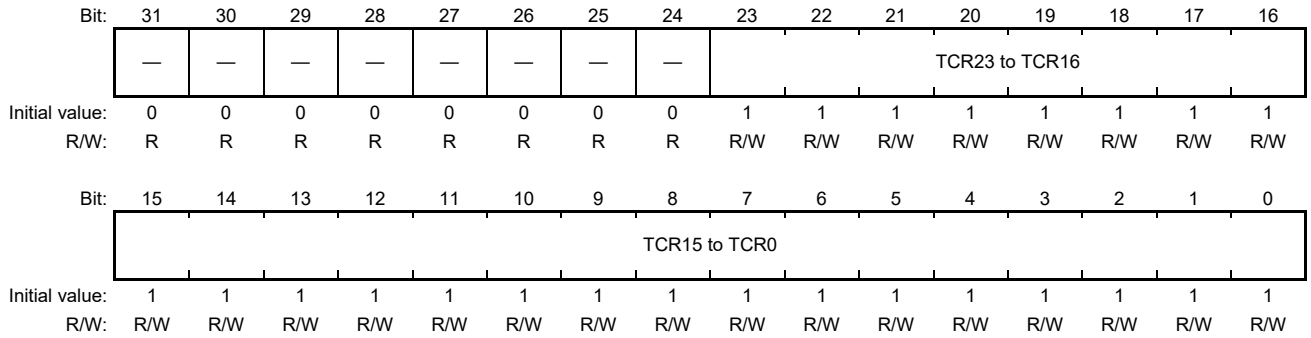
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	SAR31 to SAR0	H'0000 0000	R/W	Source Address (H'0000 0000 to H'FFFF FFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer source address during a DMA transfer.

43.2.5 DMA0/1 Destination Address Registers 0 and 1 (USBDMA0_DAR_0/USBDMA1_DAR_1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	DAR31 to DAR0	H'0000 0000	R/W	Destination Address (H'0000 0000 to H'FFFF FFFF (4 Gbytes)) Set a value of 8-byte, 16-byte, or 32-byte boundary. Indicate the next transfer destination address during a DMA transfer.

43.2.6 DMA0/1 Transfer Count Registers 0 and 1 (USBDMA0_TCR_0/USBDMA1_TCR_1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 24	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
23 to 0	TCR23 to TCR0	H'FF FFFF*	R/W	Transfer Count • When H'00 0001 is set, total transfer volume is as follows: Transfer size = 32 bytes: 32 × 1 bytes Transfer size = 16 bytes: 16 × 1 bytes Transfer size = 8 bytes: 8 × 1 bytes • When H'FF FFFF is set, 16,777,215 times • When H'00 0000 is set, 16,777,216 times (maximum) • Indicate 0 when a DMA transfer completes successfully.

Note: * To read this register, read the internal transfer counter value (the TCR counter value) directly. This register is read as all 1 after a reset is cleared because the initial value of the TCR counter is all 1 (H'FF FFFF). When DMA is enabled (DE in USBDMA0/1_CHCR is asserted), the TCR counter is loaded with the value set in this register and decrements during DMA transfers. This means that the remaining transfer count is read back. Note that the read value may be different from the one set in this register due to this reason.

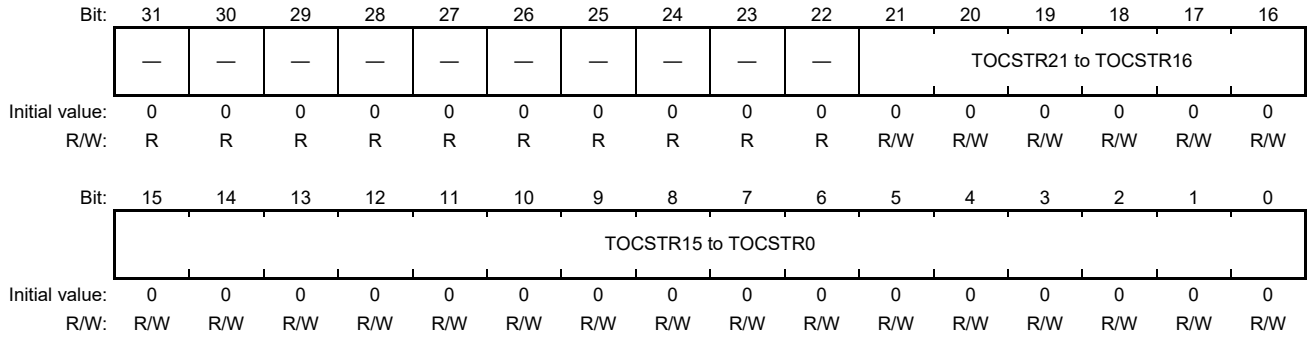
43.2.7 DMA0/1 Timeout Count Registers 0 and 1 (USBDMA0_TOCNTR_0/USBDMA1_TOCNTR_1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	TOCNTR21 to TOCNTR16					
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TOCNTR15 to TOCNTR0															
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCNTR21 to TOCNTR0	H'3F FFFF	R	Timeout Counter Value (H'00 0000 to H'27 AC40) Indicate the remaining timeout count during timeout counting. (Countable up to H'3F FFFF (approximately 21 ms) by the hardware. See the descriptions of the USBDMA0/1_TOCSTR register.)

43.2.8 DMA0/1 Timeout Constant Registers 0 and 1 (USBDMA0_TOCSTR_0/USBDMA1_TOCSTR_1)



Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21 to 0	TOCSTR21 to TOCSTR0	H'00 0000	R/W	Timeout Constant Value (H'00 0000 to H'27 AC40) Set a timeout value (at 200 MHz cycle). The maximum timeout time is approximately 13ms. (Setting up to H'3F FFFF (approximately 21 ms) is allowed by the hardware.)

43.2.9 DMA0/1 Channel Control Registers 0 and 1 (USBDMA0_CHCR_0/USBDMA1_CHCR_1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	FTE	—	—	—	SPIM	TRE	BUFE	RWE	NULLE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TR	BUF	RW	NULL	—	—	—	—	TS1	TS0	IE	TOE	TO	SP	TE	DE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	FTE	0	(R)/W	Forced TE Set Register When a NULL packet is received, the TE bit is forced to 1 to terminate the transfer by setting 1 in this register. (The DREQE bit of the USB-IP should also be controlled accordingly. For details on the control procedure and restrictions, see section 43.3.2 (3), DMA transfer flow.) This bit is always read as 0. 0: No effect (nothing happens). 1: Forces the TE bit to 1.
23 to 21	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
20	SPIM	0	R/W	Short Packet Receive Interrupt Mask Enables or disables the reflection of the short packet (SP) receive flag in the interrupt signal. If this bit is set to 1, no interrupts are generated when an SP is received. However, the SP receive flag (the SP bit) is set regardless of this register setting. 0: The short packet receive interrupt is enabled (default). 1: The short packet receive interrupt is disabled.
19	TRE	0	R/W	Transaction End Detect Interrupt Flag Enable Enables or disables the reflection of TR in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the TR bit is always 0.) 0: The TR flag is disabled. 1: The TR flag is enabled.
18	BUFE	0	R/W	Buffer End Detect Interrupt Flag Enable Enables or disables the reflection of BUF in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the BUF bit is always 0.) 0: The BUF flag is disabled. 1: The BUF flag is enabled.

Bit	Bit Name	Initial Value	R/W	Description
17	RWE	0	R/W	Final Buffer Access Detect Interrupt Flag Enable Enables or disables the reflection of RW in the interrupt signal and the DMA stop/restart control. (When this bit is set to 0, the RW bit is always 0.) 0: The RW flag is disabled. 1: The RW flag is enabled.
16	NULLE	0	R/W	NULL Receive Interrupt Flag Enable Enables or disables the reflection of the NULL receive interrupt flag (NULL) in the interrupt signal. 0: The NULL receive interrupt flag is disabled. 1: The NULL receive interrupt flag is enabled.
15	TR	0	R/W*	Transaction End Detect Interrupt Flag When the transaction end is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A transaction end receive interrupt is generated.
14	BUF	0	R/W*	Buffer End Detect Interrupt Flag When the end of the buffer is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A buffer end detect interrupt is generated.
13	RW	0	R/W*	Final Buffer Access Detect Interrupt Flag When the final access to the buffer is detected, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A final buffer access detect interrupt is generated.
12	NULL	0	R/W*	NULL Receive Interrupt Flag When NULL packet is received, an interrupt is generated. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A NULL packet receive interrupt is generated.
11 to 8	—	All 0	R	Reserved The bits should always be written as 0.
7, 6	TS1 to TS0	00	R/W	DMA Transfer Size 00: 8 bytes 01: 16 bytes 10: 32 bytes 11: Setting prohibited Specify the same transfer size and address boundary when setting addresses in USBDMA0/1_SAR and USBDMA0/1_DAR as a transfer source and transfer destination. If TS = 11 is set, an address error is generated and DMA transfer is disabled.

Bit	Bit Name	Initial Value	R/W	Description
5	IE	0	R/W	Interrupt Enable Enables or disables an interrupt request to the CPU when DMA transfer ends. When AE, TE, SP, TO, NULL, RW, BUF, or TR bit is set with this bit set to 1, an interrupt request is output to the CPU. However, when the TRE, BUFE, RWE, NULLE, or TOE bit is set to disabled, no interrupt due to TR, BUF, RW, NULL, or TO is generated. 0: An interrupt request is disabled. 1: An interrupt request is enabled.
4	TOE	0	R/W	Timeout Enable Enables or disables the reflection of the timeout flag (TO) in the interrupt. 0: Timeout flag is disabled. 1: Timeout flag is enabled.
3	TO	0	R/W*	Timeout Flag After a transfer request REQ is negated, a timeout interrupt is generated after the specified cycles. (Used for timeout when the final packet is Max packet.) 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: Timeout is generated.
2	SP	0	R/W*	Short Packet Receive Flag A transfer end interrupt is generated upon receiving a short packet from the USB-IP. For example, if DMA transfer size is set to 1 MB but actual data transfer is 900 KB, this interrupt is generated when transfer of 900 KB finishes. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: A short packet is received.
1	TE	0	R/W*	Transfer End Flag When a DMA transfer ends with USBDMA0/1_TCR = 0, the TE bit is set to 1. When a DMA address error occurs before USBDMA0/1_TCR is cleared to 0 and the transfer is suspended by clearing the DE bit and the DME bit in USBDMA0/1_DMAOR, the TE bit is not set to 1. To clear the TE bit, write 0 after reading 1. When TE = 1, DMA transfer is disabled even if the DE bit is set to 1. 0: DMA transfer is in progress or suspended. [Clearing condition] Writing 0 after reading 1. 1: DMA transfer end (TCR = 0)
0	DE	0	R/W	DMA Enable Enables or disables DMA transfer. Setting the DME bit in USBDMA0/1_DMAOR and the DE bit for the corresponding channel to 1 starts a DMA transfer, provided that all interrupt flags are 0. Clearing the DE bit to 0 suspends the ongoing transfer after the transfer of one transaction is completed. 0: DMA transfer is disabled. 1: DMA transfer is enabled.

Note: * Only writing 0 to clear the flag is enabled.

43.2.10 DMA0/1 Final Transaction Valid Data Transfer Enable Registers 0 and 1 (USBDMA0_TEND_0/USBDMA1_TEND_1)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	EDTEN31 to EDTEN16															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	EDTEN15 to EDTEN0															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	EDTEN31 to EDTEN0	H'0000 0000	R/W	Final Transaction Valid Data Transfer Enable (valid only for IN transfers) Specify valid data size in units of bytes in the final transaction of data transfer (see section 43.3.2, DMA Transfer Function). H’8000 0000: 32 bytes × (n-1) + 1 byte H’C000 0000: 32 bytes × (n-1) + 2 bytes : H’FFFF FFFF: 32 bytes × (n-1) + 32 bytes Notes: 1. n: Transfer count setting (TCR) 2. For the 8-byte transfer, set EDTEN23 to EDTEN0 to 0. For the 16-byte transfer, set EDTEN15 to EDTEN0 to 0.

43.2.11 DMA0/1 Operation Register (USBDMA0_DMAOR/USBDMA1_DMAOR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	TID1 and TID0		RM	PR1 and PR0		AE	DME
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W*	R/W*	R/W	R/W	R/W	R/W*	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	TID1 and TID0	00	R/W*	Response Error Channel Identity Information TID1 indicates the channel 1 error information, and TID0 indicates the channel 0 error information. TID1 0: No error 1: Channel 1 response packet error TID0 0: No error 1: Channel 0 response packet error [Setting condition] When a CH0 (1) response error occurs [Clearing condition] Clearing ERR_RCV in USBDMA0/1_VCR (Channel 0/channel 1 concurrent clear)
4	RM	0	R/W	Response Error Mask Mode 0: A response error is output. 1: A response error is masked.
3, 2	PR1 and PR0	00	R/W	Priority Mode Specify the priority of channels to execute transactions when transfer requests are made simultaneously in both channel 0 and channel 1 as follows: 00: Channel 0 > Channel 1 01: Channel 1 > Channel 0 10: Setting prohibited (If PR = 10 is set, channel 0 > channel 1) 11: Setting prohibit

Bit	Bit Name	Initial Value	R/W	Description
1	AE	0	R/W*	Address Error Flag Indicates that an address error interrupt occurred when setting USBDMA0/1_SAR or USBDMA0/1_DAR. This flag is set to 1 when the value of USBDMA0/1_SAR or USBDMA0/1_DAR differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited). When the AE bit is set to 1, DMA transfer is not enabled even if the DE bit in DMACHCR and the DME bit in USBDMA0/1_DMAOR are set to 1. 0: No address error interrupt is generated by the DMAC. [Clearing condition] Setting USBDMA0/1_SAR and USBDMA0/1_DAR to values that match the transfer size boundary. 1: An address error interrupt is generated.
0	DME	0	R/W	DMA Master Enable Enables or disables DMA transfers for all channels. When the DME bit and the DE bit in USBDMA0/1_CHCR are set to 1, DMA transfer is enabled, provided that all interrupt flags in USBDMA0/1_CHCR of the transfer channel are 0. Clearing the DME bit suspends the DMA transfer for all channels. 0: DMA transfer for all channels is disabled. 1: DMA transfer for all channels is enabled.

Note: * Only writing 0 to clear the flag is enabled.

43.3 Operation

43.3.1 Interrupt/Error Detection Function

This section describes the interrupt/error detection function that is implemented in this module.

Table 43.5 lists the mask, source, and flag registers for each interrupt type.

Table 43.5 Registers by Interrupts/Errors

	Interrupt Generation	Interrupt Mask Register	Interrupt Mask Register (Individual Mask)	Source Register	Flag Register
Transfer count end	√	X*1_CHCR_x.IE	—	X*1_DMICR.TEx	X*1_CHCR_x.TE
Short packet receive	√	X*1_CHCR_x.IE	X*1_CHCR_x.SPIM	X*1_DMICR.SPx	X*1_CHCR_x.SP
NULL packet receive	√	X*1_CHCR_x.IE	X*1_CHCR_x.NULLE	X*1_DMICR.NULLx	X*1_CHCR_x.NULL
Timeout	√	X*1_CHCR_x.IE	X*1_CHCR_x.TOE	X*1_DMICR.TOx	X*1_CHCR_x.TO
Transaction end detect	√	X*1_CHCR_x.IE	X*1_CHCR_x.TRE*	X*1_DMICR.TRx	X*1_CHCR_x.TR
Buffer end detect	√	X*1_CHCR_x.IE	X*1_CHCR_x.BUFE*	X*1_DMICR.BUFx	X*1_CHCR_x.BUF
Final buffer access detect	√	X*1_CHCR_x.IE	X*1_CHCR_x.RWE*	X*1_DMICR.RWx	X*1_CHCR_x.RW
Address error	√	X*1_CHCR_x.IE	—	X*1_DMICR.AE	X*1_DMAOR.AE
Response packet error	—	—	—	—	X*1_VCR.ERR_SNT X*1_VCR.ERR_RCV

Legend: X*1: USBDMA0/USBDMA1

Note: These registers not only mask interrupt generation but also disable error processing (flag sources and flag clearing).

Table 43.6 shows the processing to be executed when different interrupts occur. DMA transfer control is not affected when the NULL packet is received, timeout, or response packet error interrupt occurs. When the transfer count end interrupt occurs, processing is restarted. Processing can be resumed or restarted after interrupts occur from other sources.

Table 43.6 Processing to be Executed When Interrupts Occur (Suspend/Resume/Restart)

	Suspend/Resume	Terminate/Restart	Suspend/Resume/Restart Control Mask Register
Transfer count end	—	√	—
Short packet receive	√	√	—
NULL packet receive	—	√*	—
Timeout	—	√	—
Transaction end detect	√	√	USBDMA0/1_CHCR_x.TRE
Buffer end detect	√	√	USBDMA0/1_CHCR_x.BUFE
Final buffer access detect	√	√	USBDMA0/1_CHCR_x.RWE
Address error	√	√	—
Response packet error	—	—	—

Note: * When a NULL packet is received, processing is forced to be terminated and restarted by the FTE bit (see section 43.3.2 (3), DMA transfer flow.).

The internal circuit is reloaded register values when restarted, but not when resumed.

Table 43.7 lists the interrupt generating conditions.

Table 43.7 Interrupt Generating Conditions

Interrupt Name	Interrupt Conditions
Transfer count end interrupt	When the final data transfer of the specified transfer count (in the USBDMA0/1_TCR register) completes IN transfer: When the final access to USB-IP completes OUT transfer: When the data transmission to the AXI completes
Short packet receive interrupt	When the data transfer at the time the end of a transaction is detected completes
NULL packet receive interrupt	When a NULL packet is detected or the forced TE register is set
Timeout interrupt	When the specified time elapses after the last transfer request
Transaction end detect interrupt	When the end of a transaction is detected
Buffer end detect interrupt	When the end of the buffer is detected
Final buffer access detect interrupt	When the final access to the buffer is detected
Address error interrupt	When invalid access to the DMAC register is attempted (With invalid USBDMA0/1_SAR/USBDMA0/1_DAR values or invalid transfer size (TS) specified)
Response packet error	Error Transmission (ERR_SNT) When accessed by a transaction that is not supported Error Reception (ERR_RCV) When received a response packet error from the system

Figure 43.2 shows a block diagram of the interrupt circuit.

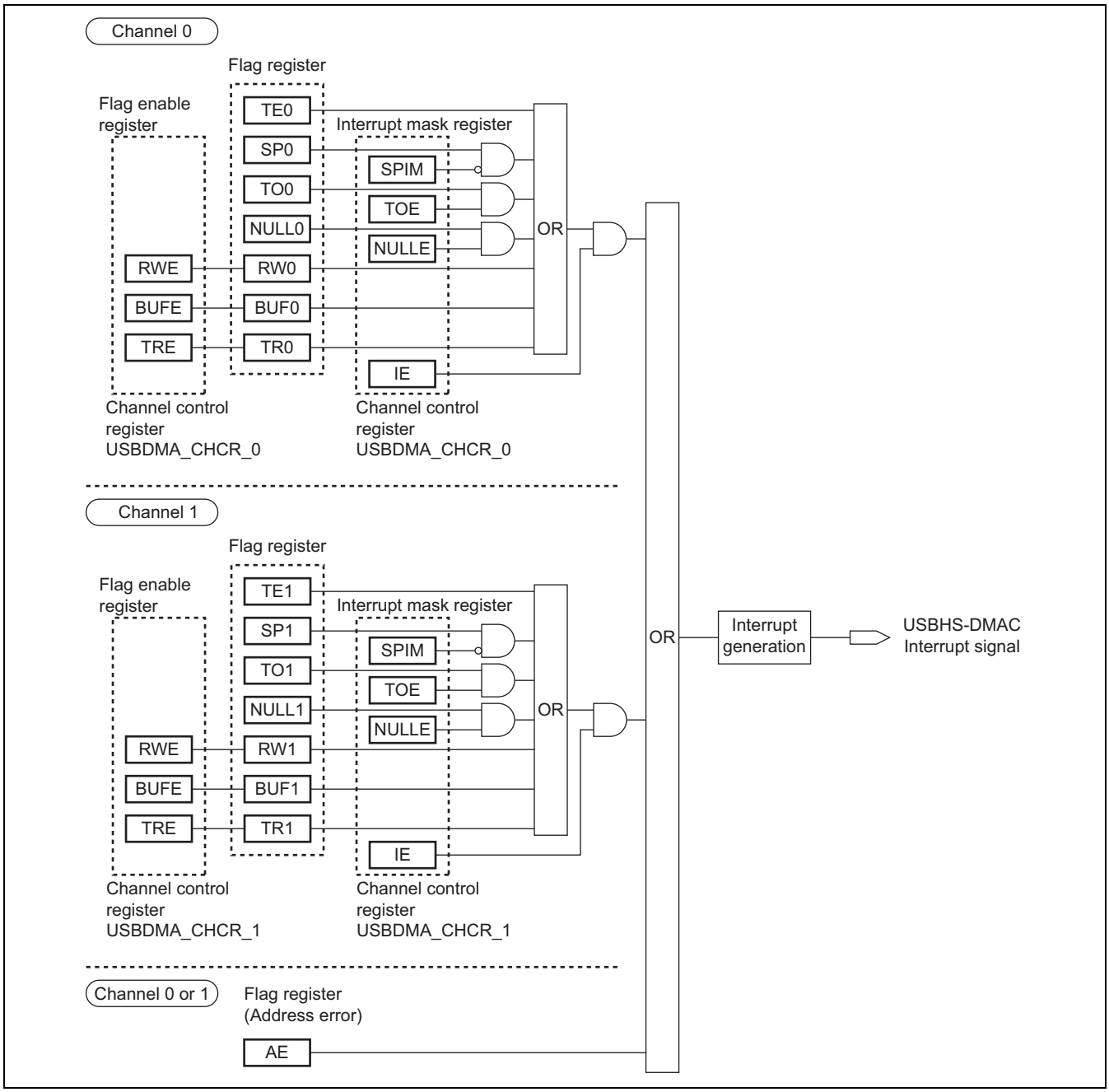


Figure 43.2 Block Diagram of Interrupt Circuit

(1) Transfer count end interrupt (TE flag)

Can be generated when the specified number of transfers complete or the FTE bit in the channel control register (USBDMA0/1_CHCR_0 to USBDMA0/1_CHCR_1) is set to 1. When the IE bit in the USBDMA0/1_CHCR_0 to USBDMA0/1_CHCR_1 is set to 0, no interrupts are generated. However, the TE bit in USBDMA0/1_CHCR_0 to USBDMA0/1_CHCR_1 and the TE0 or TE1 bit in the interrupt source register (USBDMA0/1_DMICR) are set to 1 regardless of the IE bit setting.

The internal transfer counter is loaded with the value set in the USBDMA0/1_TCR_x register and decrements based on the AXI clock every time one transaction (8-/16-/32-byte) completes. When the transfer count value reaches 0 (the end of a transfer count), the counter sets the TE (transfer end) flag from 0 to 1 (when the FTE bit is set, it is reflected on the TE flag immediately). The TE bit is cleared by writing 0 to it after reading it as 1 by software.

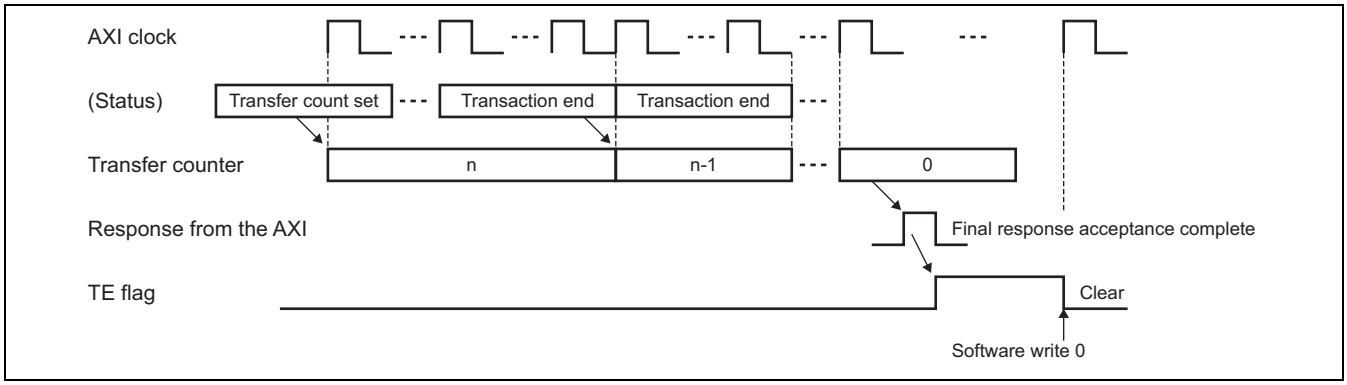


Figure 43.3 Transfer Count End Interrupt (TE) Generation Timing

(2) Short packet receive interrupt (SP flag)

Can be generated when a short packet is detected. When the SPIM bit in the USBDMA0/1_CHCR_x register is set to 1, no interrupts are generated. However, the SP bit (SP flag) in the USBDMA0/1_CHCR_x register and the SP0 or SP1 bit in the USBDMA0/1_DMICR register are set to 1, regardless of the SPIM bit setting. The SP bit is cleared by writing 0 to it after reading it as 1 by software.

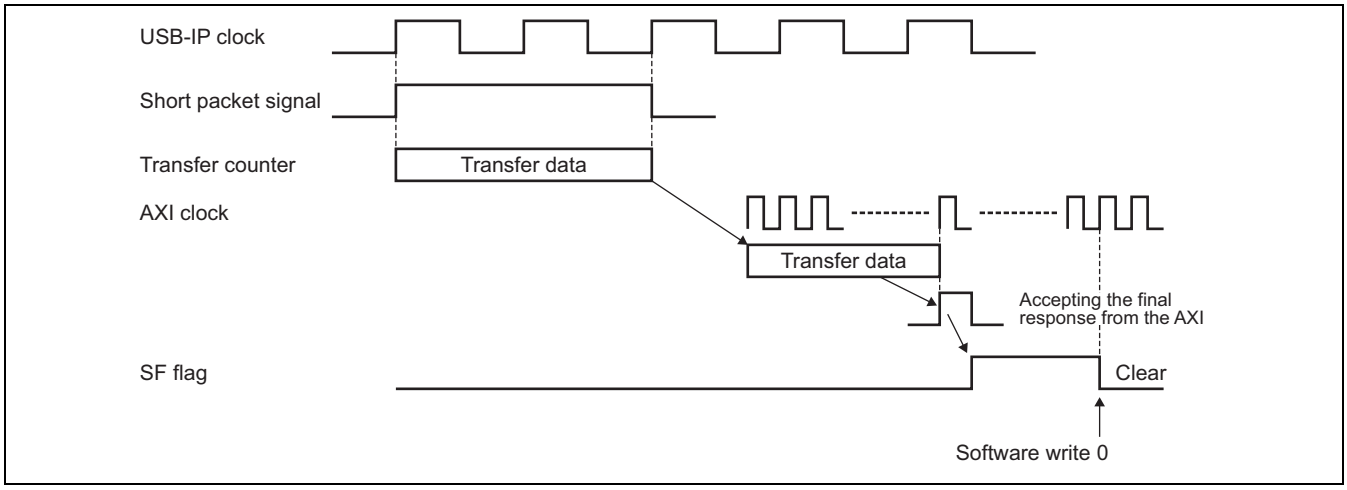


Figure 43.4 Short Packet Receive Interrupt (SP) Generation Timing

(3) NULL packet receive interrupt (NULL flag)

Can be generated when a NULL packet is detected. When the NULLE bit in the USBDMA0/1_CHCR_x register is set to 0, no interrupts are generated. However, the NULL bit (NULL flag) in the USBDMA0/1_CHCR_x register and the NULL0 or NULL1 bit in the USBDMA0/1_DMICR register are set to 1, regardless of the NULLE bit setting. Note also that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a NULL packet is received. The software is responsible for implementing special processing if necessary since in this module this interrupt is designed only to signal the software that a NULL packet is received.

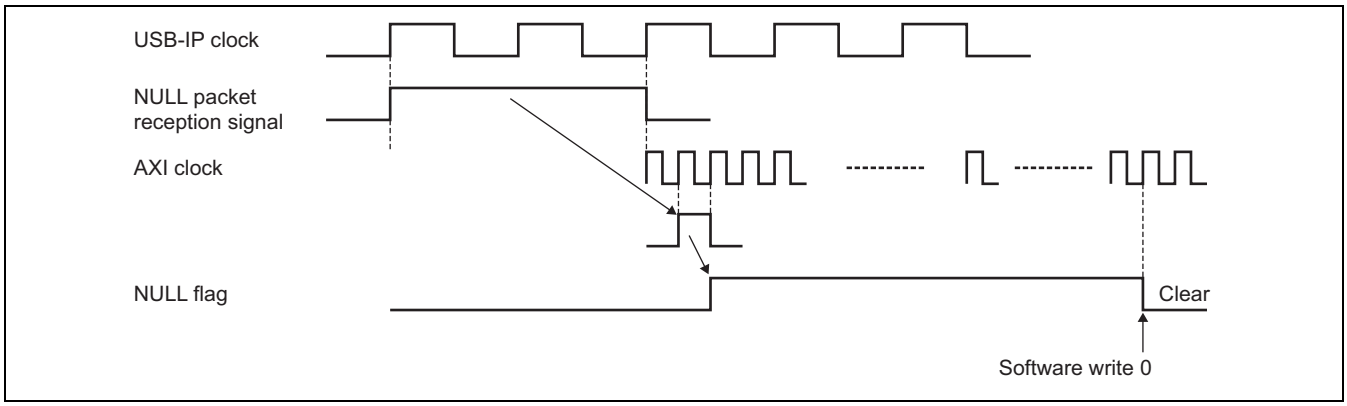


Figure 43.5 NULL Packet Receive Interrupt (NULL) Generation Timing

(4) Timeout interrupt (TO flag)

Can be generated when the time period that is specified in the timeout constant register (USBDMA0/1_TOCSTR_0 or USBDMA0/1_TOCSTR_1) elapses after the final transfer request is received from the USB-IP. On detecting the final transfer request, the internal counter is loaded with the value set in the USBDMA0/1_TOCSTR_x register and starts counting down. When the counter reaches 0, it generates a timeout interrupt. Note that the DMA transfer control in this module, such as stop, suspend, or resume, is not affected when a timeout interrupt occurs. The TO bit is cleared by writing 0 to it after reading it as 1 by software. Figure 43.6 and 43.7 show the timeout interrupt generation timing.

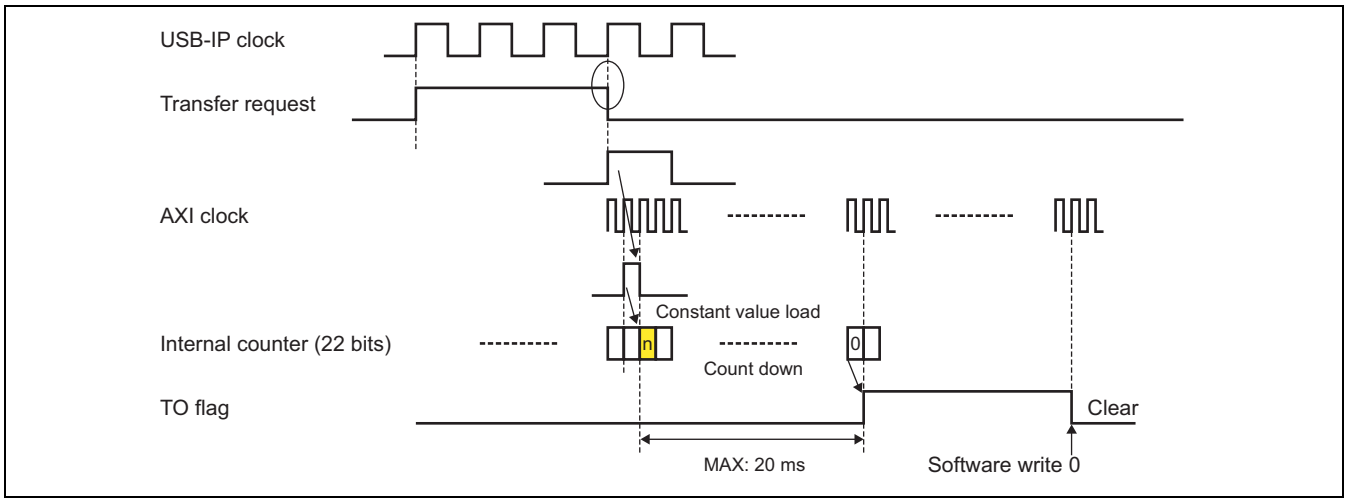


Figure 43.6 Timeout Interrupt (TO) Generation Timing

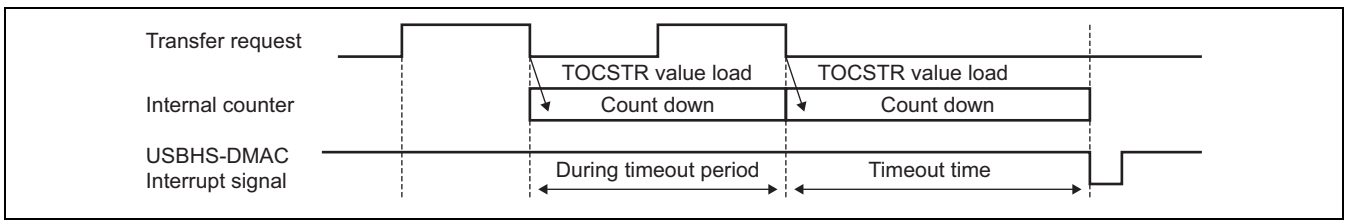


Figure 43.7 Timeout Interrupt Timing

The functions described in section 43.3.1 (5) to 43.3.1 (9) are added to detect and notify the transitions on an individual signal line to the software, but no use is defined. They can be used as required.

(5) Transaction end detect interrupt (TR flag)

Can be generated when the end of a transaction is detected within the USB-IP. Note that the TR bit in the USBDMA0/1_CHCR_x register and the TR0 or TR1 bit in the USBDMA0/1_DMICR register are not reflected in the interrupt signal when the TRE bit in the USBDMA0/1_CHCR_x register is set to 0.

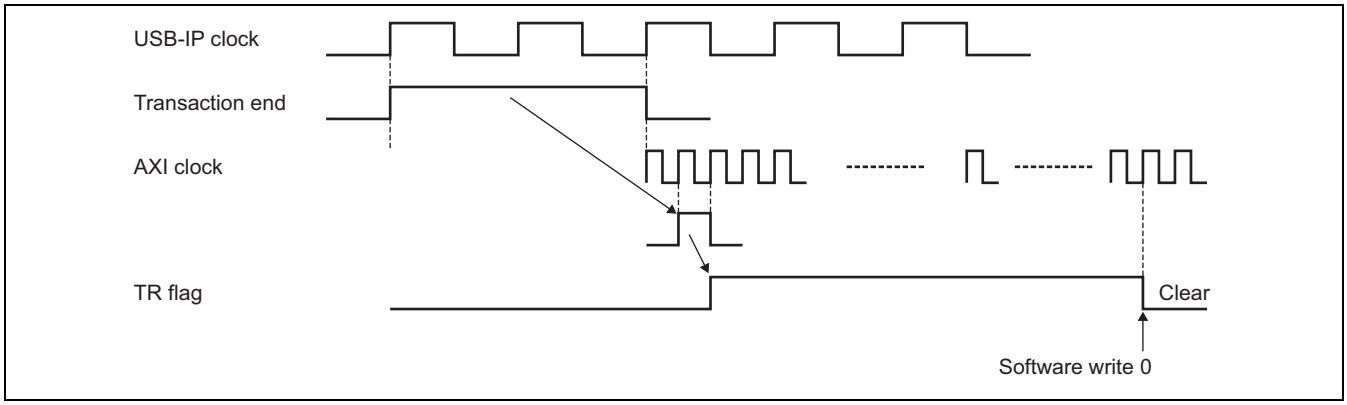


Figure 43.8 Transaction End Detect Interrupt Timing

(6) Buffer end detect interrupt (BUF flag)

Can be generated when the end of the buffer in the USB-IP is detected. Note that the BUF bit in the USBDMA0/1_CHCR_x register and the BUF0 or BUF1 bit in the USBDMA0/1_DMICR register are not reflected in the interrupt signal when the BUFE bit in the USBDMA0/1_CHCR_x register is set to 0.

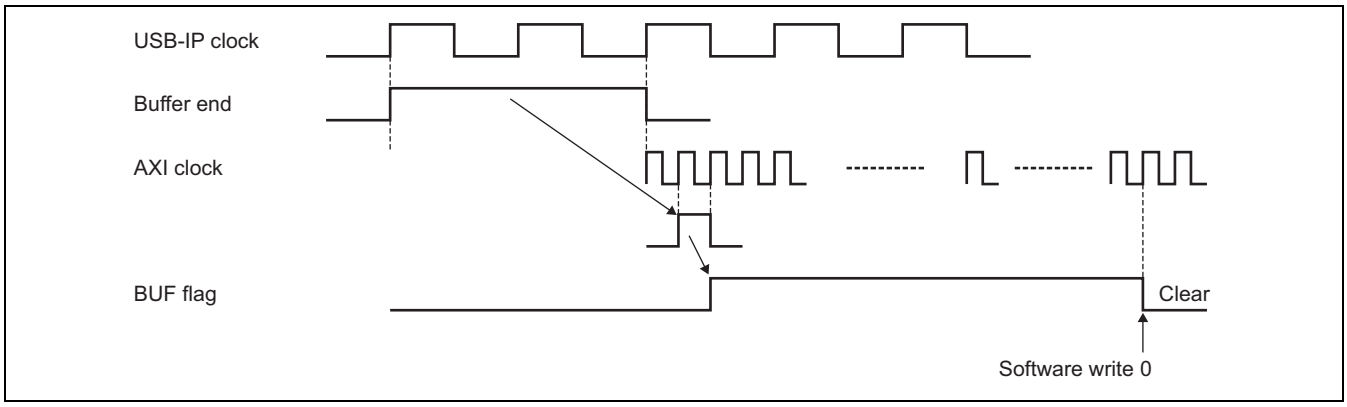


Figure 43.9 Buffer End Detect Interrupt Timing

(7) Final buffer access detect interrupt (RW flag)

Can be generated when the final access to the buffer in the USB-IP is detected. Note that the RW bit in the USBDMA0/1_CHCR_x register and the RW0 or RW1 bit in the USBDMA0/1_DMICR register are not reflected in the interrupt signal when the RWE bit in the USBDMA0/1_CHCR_x register is set to 0.

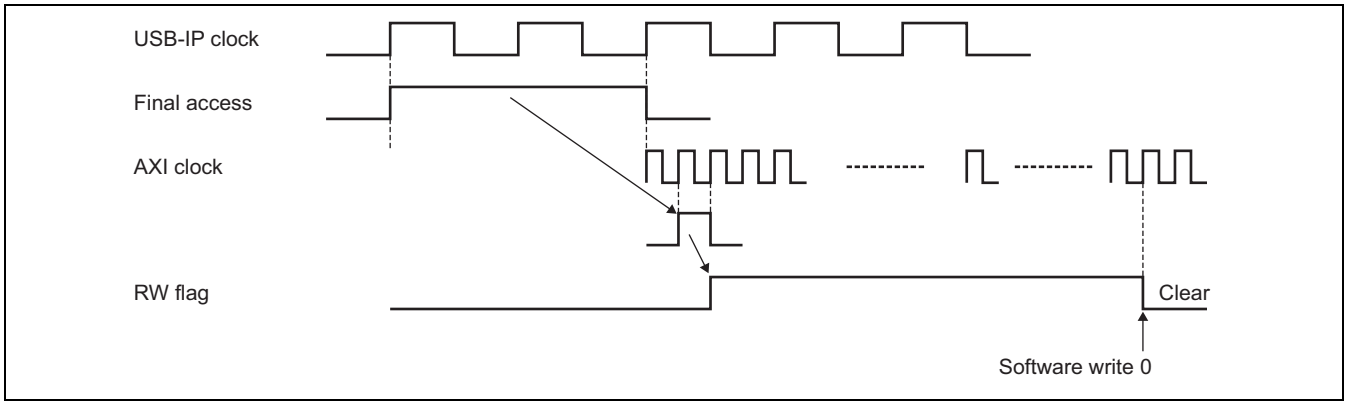


Figure 43.10 Final Buffer Access Detect Interrupt Timing

(8) Address error detection

This is a flag that indicates an address error interrupts has occurred when setting the source address register (USBDMA0/1_SAR0 to USBDMA0/1_SAR1) and the destination address register (USBDMA0/1_DAR0 to USBDMA0/1_DAR1). When the value written to the USBDMA0/1_SAR or USBDMA0/1_DAR register differs from the transfer size (TS) boundary, and when the TS bits are set to 11 (setting prohibited), the AE bit in the USBDMA0/1_DMAOR register is set to 1. There is no distinction between CH0 and CH1 for an address error (the AE bit is set to 1 when an address error occurs on CH0 or CH1).

While the AE is set, no DMA transfer is allowed even if the DE bit in the USBDMA0/1_CHCR_x register and the DME bit in the USBDMA0/1_DMAOR register are set to 1. The address error interrupt is cleared by setting correct addresses in USBDMA0/1_SAR_x and USBDMA0/1_DAR_x.

Table 43.8 Address Error Detection Conditions When Setting Transfer Sizes

Transfer Size	Address Error Detection Conditions
TS = B'00 (8-byte transfer)	When data that is not aligned to 8-byte boundaries is written to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers (Writes to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers are valid.)
TS = B'01 (16-byte transfer)	When data that is not aligned to 16-byte boundaries is written to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers (Writes to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers are valid.)
TS = B'10 (32-byte transfer)	When data that is not aligned to 32-byte boundaries is written to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers (Writes to the USBDMA0/1_SAR/ USBDMA0/1_DAR registers are valid.)
—	When B'11 (setting prohibited) is written to the TS bit (Writes to the TS bit are valid.)

(9) Response packet error detection

This function reports response packet errors when the interface between the AXI and this module is accessed in ways that are not listed in Table 43.2.

(a) Transmitting response packet errors

When a response packet error occurs during accessing from the AXI to this module, the ERR_SNT bit in the USBDMA0/1_VCR register is set to 1.* The error signal is also sent to the AXI bus if the RM bit in the USBDMA0/1_DMAOR register is 0. If the RM bit is set to 1, the error signal is masked (0 is signaled).

Note: * When a response packet error occurs, the ERR_SNT bit is set to 1 regardless of the RM bit setting. The ERR_SNT bit is cleared by writing 0 after reading 1.

Table 43.9 Response Packet Error Generation

USBDMA0_DMAOR (RM bit) Setting	1 (Mask Mode)	0 (Normal Mode)
Response packet error signal notification to AXI	Signals the fixed value (0) to the AXI bus without determining if there is a response packet error.	Reports a response packet error to the AXI bus when it is accessed with a transfer size other than those supported in this module (4-byte read/write and 8-byte read).

(b) Receiving response packet errors

When a response packet error occurs during accessing from this module to the AXI, the ERR_RCV bit in the USBDMA0/1_VCR register is set to 1. The TID bit in the USBDMA0/1_DMAOR register indicates on which channel of this module the error has occurred (TID[1] = 1 means it has occurred on CH1 and TID[0] = 1 on CH0).

The ERR_RCV bit is cleared by writing 0 after reading 1.

43.3.2 DMA Transfer Function

(1) Operating mode

The following operating modes (a) to (b) are supported according to the setting of the PR bit in the DMA operation register (USBDMA0/1_DMAOR).

(a) CH0 first control

Forces CH1 to wait to start a DMA transfer until a DMA transfer completes on CH0.

When there is a timing conflict in starting a DMA transfer between CH0 and CH1, CH0 takes precedence over CH1. If a DMA transfer is in progress on CH1 when CH0 tries to start a DMA transfer, CH0 waits to start it until the ongoing DMA transfer completes on CH1.

(b) CH1 first control

Forces CH0 to wait to start a DMA transfer until a DMA transfer completes on CH1.

When there is a timing conflict in starting a DMA transfer between CH1 and CH0, CH1 takes precedence over CH0. If a DMA transfer is in progress on CH0 when CH1 tries to start a DMA transfer, CH1 waits to start it until the ongoing DMA transfer completes on CH0.

Figure 43.11 shows an overview of the processing of the AXI bridge in each operating mode.

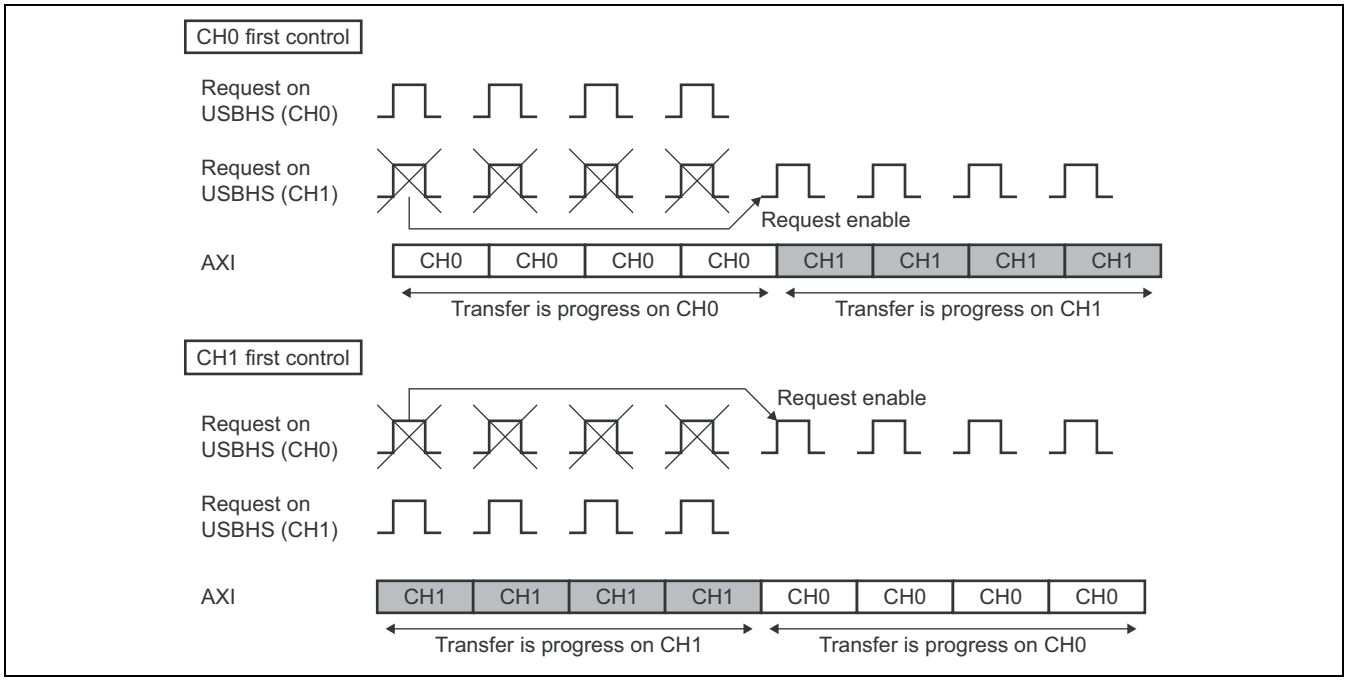


Figure 43.11 Overview of AXI Bridge Processing in Each Mode

(2) Transfer size

The transfer size on the AXI can be selected by setting the channel control register (the TS bit).

8-, 16-, and 32-byte can be set for each channel independently.

The following consideration should be observed during IN transfers.

The minimum transfer size that can be set to the TS bit is 8 bytes while the USB-IP can control transfers in 1-byte units. For example, if valid transfer data that is "8 × (n – 1) + α" (α is less than 7 bytes) in size is to be transferred to the USB-IP with the transfer size set to 8 bytes and the transfer count set to n, α is transferred as a valid transfer unit by controlling byte enables according to the DMA final transaction valid data transfer enable register (the EDTEN bits) setting. Likewise, data is transferred in "transfer size x transfer count" (the final transaction is controlled by EDTEN) for 16- and 32-byte transfer sizes. The EDTEN setting is valid only for IN transfer and is don't care for OUT transfer.

Figure 43.12 shows an example of EDTEN setting. When only EDTEN31 in EDTEN31 to EDTEN0 is 1, one byte is enabled. When only EDTEN31 and EDTEN30 in EDTEN31 to EDTEN0 are 1, two bytes are enabled. Therefore, the total transfer volumes in the example shown above are calculated as "(32 bytes × (n – 1)) bytes + 10 bytes" for 32-byte transfer, "(16 bytes × (n – 1)) bytes + 7 bytes" for 16-byte transfer, and "(8 bytes × (n – 1)) bytes + 2 bytes" for 8-byte transfer. EDTEN15 to EDTEN0 in 16-byte transfer, EDTEN23 to EDTEN0 in 8-byte transfer are invalid (their values are ignored).

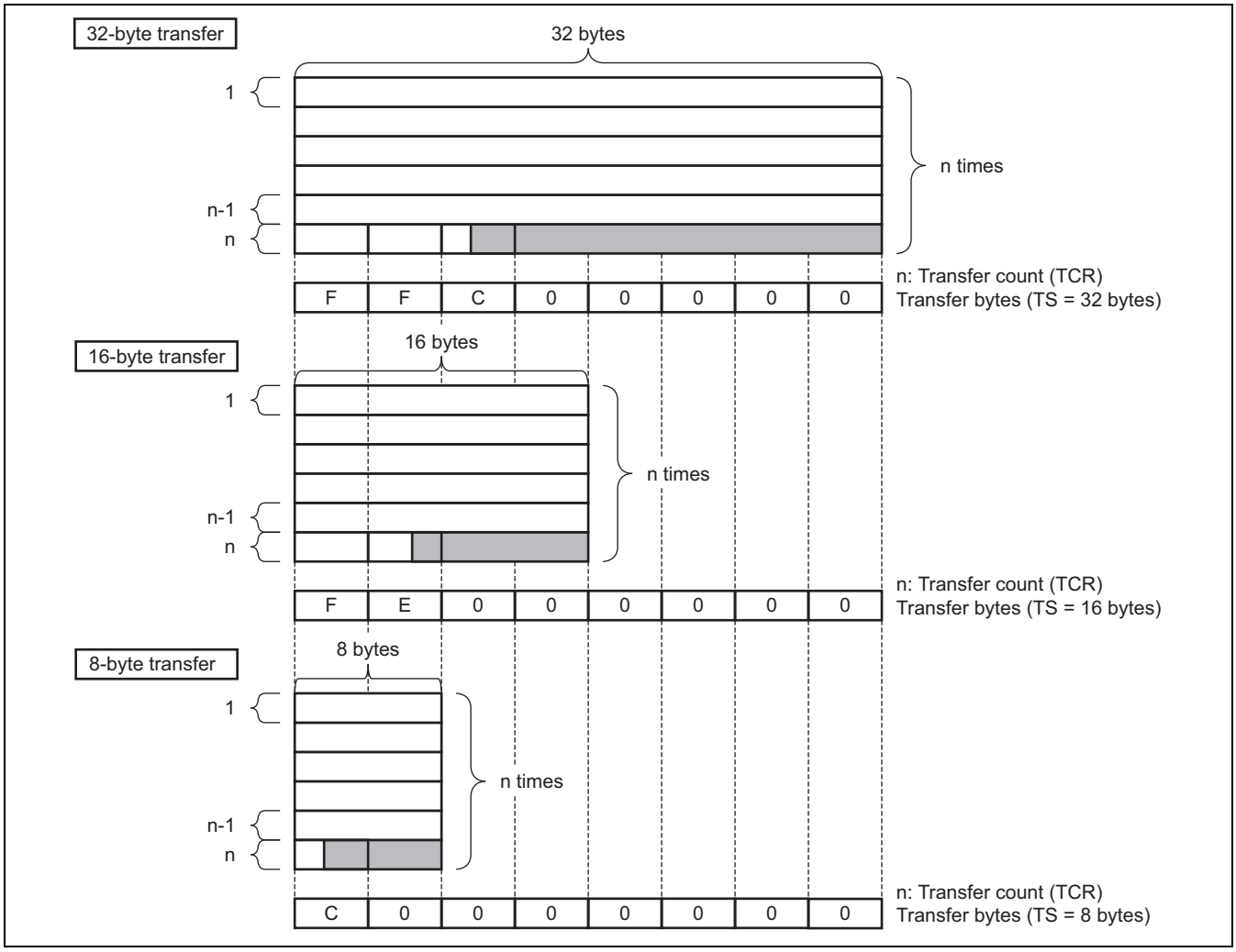


Figure 43.12 Example of Final Transaction Valid Data Transfer Enable (EDTEN) Setting

(3) DMA transfer flow

After the DMA source address register (USBDMA0/1_SAR), DMA destination address register (USBDMA0/1_DAR), DMA transfer count register (USBDMA0/1_TCR), DMA channel control register (USBDMA0/1_CHCR), final valid data transfer enable register (USBDMA0/1_TEND), and DMA operation register (USBDMA0/1_DMAOR) are set appropriately, the DMAC starts data transfer in the following sequence. The DMA timeout constant register (USBDMA0/1_TOCSTR) may also need to be set.

If the transfer enabling conditions are set as DE = 1, DME = 1, TE = 0, AE = 0, SP = 0, and (TR = 0, BUF = 0, RW = 0), transfers are performed according to the transfer request enables and transfer requests from the USB-IP. The transfer direction (IN/OUT transfer) is determined by the direction signal from the USB-IP. The transfer size is determined by the setting of TS1 to TS0.

Every time one AXI transaction (in the transfer size specified in the TS bit) completes, the internal counter of this module decrements the USBDMA0/1_TCR value by one. When the specified transfer count ends (the USBDMA0/1_TCR value reaches 0), it means all transfers complete. At this time, an USB-DMAC interrupt is generated if the IE bit in the USBDMA0/1_CHCR register is set to 1.

When a NULL packet is received, transfer can be stopped or restarted by setting FTE = 1 after negating the DREQE bit of the HS-USB module. Follow the steps described later in "Control when a NULL packet is received".

Table 43.10 shows the conditions for each DMA transfer.

Table 43.10 DMA Transfer Conditions

Transfer enabling condition	TE = 0, SP = 0, (*TR = 0, BUF = 0, RW = 0)
Transfer (starting) condition	When a transfer request is enabled by the USB-IP When a transfer request is issued by the USB-IP
Transfer completing (then restarting) condition	When the transfer count ends (the TE flag is set to 1), (can be restarted by setting DE and DME to 1.) When FTE = 1 (when DREQE = 1 in the HS-USB module is also set), and the steps described later should be followed. When reset (can enter into standby state by releasing the reset.)
Transfer suspending (then resuming) condition	When DE = 0 or DME = 0 (can be resumed by setting DE = 1 or DME = 1.) When SP = 1 (can be resumed by clearing the SP flag.) When RW = 1, BUF = 1, and TR = 1 (can be resumed by clearing the RW, BUF, and TR flag.)* When the module stops (can be resumed by resuming the module.)

Note: * Can be ignored when the RWE, BUFE, and TRE bits are disabled (set to 0).

Figure 43.13 illustrates the high-level DMA transfer flow.

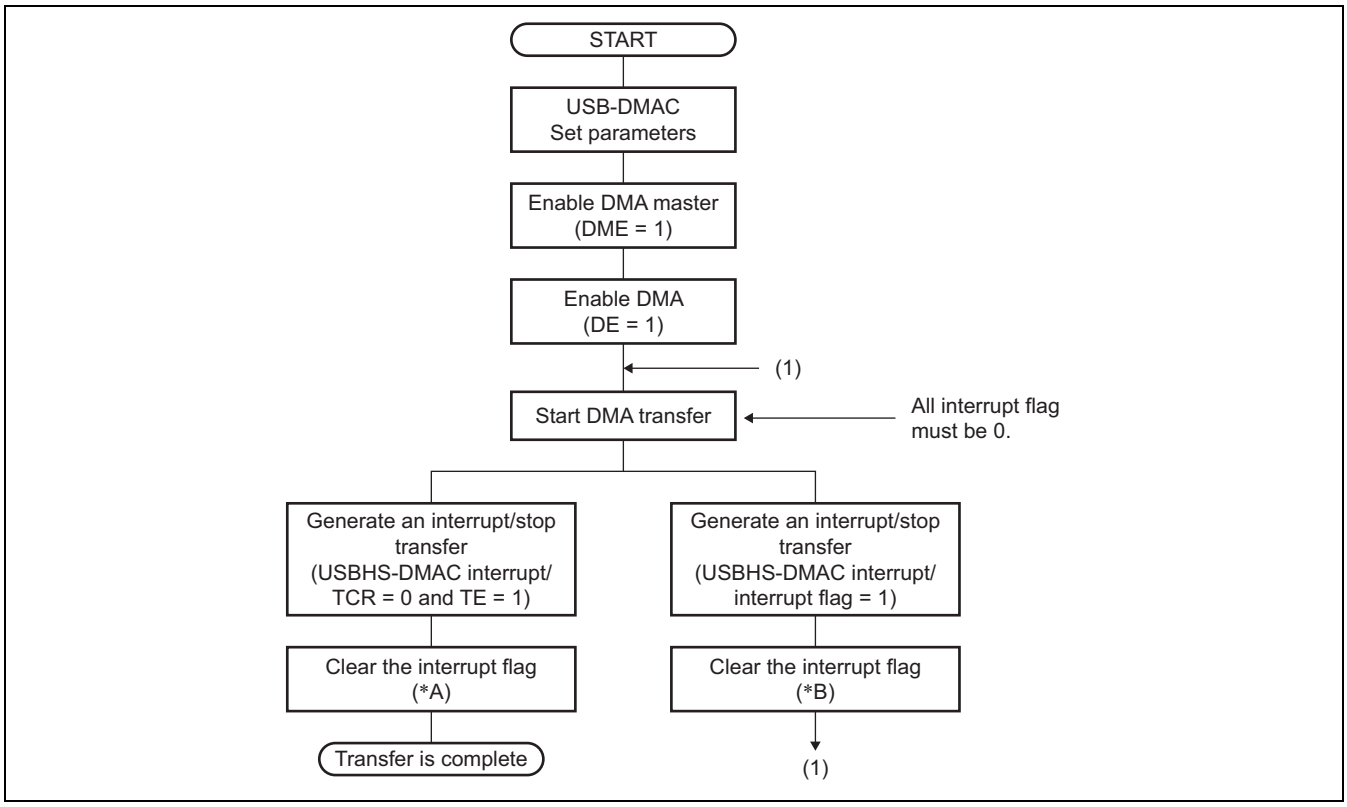


Figure 43.13 DMA Transfer Flow Overview

Where A and B apply to the following flags:

(Note that RW, BUF, and TR are not set when RWE, BUFE, and TRE are disabled, respectively.)

*A: TE flag

*B: SP, (RW, BUF, TR) flags

When to change USBDMAC parameters

USB-DMAC parameters (such as destination address or transfer count) should be changed while all interrupt flags are cleared and DE = 0 and DME = 0 are set (a transfer is started with the latest parameters when DME = 1 and DE = 1 are set). Furthermore, USB-DMAC parameters should not be changed while the DMA is enabled (DME = 1 and DE = 1).

What to do if freeze

If a transfer should freeze during operation, issue a software reset after setting DE = 0 and DME = 0 and clearing all interrupt flags. All hardware except configuration registers is initialized. Restart by setting DME and DE to 1 after updating USB-DMAC parameters if necessary.

Control when a timeout occurs

Since this module assumes bus access in the transfer units listed in Table 43.2, it cannot be restarted when a timeout occurs in an irregular case where it is being accessed with any size that are not in the table. This irregular case should be handled by software, such as by issuing a software reset (to both CH0 and CH1).

Control when a NULL packet is received

When a NULL packet is received during a DMA transfer, the DMA transfer can be suspended and resumed on each channel independently by controlling the FTE bit of this module and the DREQE bit of the HS-USB module in the following sequence.

[Control sequence]

During a DMA transfer (A)

(1) A NULL packet is received (an interrupt is generated and the NULL flag is detected).
(2) The DREQE bit of the HS-USB module is negated (= 0).
(3) Wait for the internal bus to be stabilized.
(4) Perform three actions at the same time; setting the FTE bit, clearing the NULL bit and negating the DE bit.

An interrupt is generated due to TE.

(5) Clear the interrupt caused by TE.
(6) Set the parameters (such as TCR or DAR) for the next transfer.
(7) Assert the DE bit (= 1). The DMA is restarted.
(8) Assert the DREQE bit (= 1).

Start a DMA transfer (B).

[Restrictions]

1) FTE bit set timing
   If this module is accessing the AXI (SHBSYx bit = 1) when setting the FTE bit, you need to wait to set the FTE bit until this module's internal buffer is empty and the AXI bus access is complete (SHBSYx bit = 0). Note that if you accidentally set the FTE bit while an AXI bus access is in progress, the transfer fails and transfer data may be lost or the transfer may be unable to be restarted.
2) DREQE bit assert (negate clear) timing
   It is necessary to allow at least 20clk@ZSϕ after the DE bit is asserted and before the DREQE is asserted. This is because DREQE needs to be asserted after transfers enabled by the DE bit are ready internally to be started. Asserting DREQE immediately after DE may cause malfunction such as initiating unnecessary bus access.
3) Fractional byte and NULL packet reception
   This module assumes bus access in the transfer units listed in Table 43.2 and goes out of control when it receives a NULL packet in an unsupported transfer unit. Therefore, data transfer in any transfer unit that is not in the table is prohibited.
4) IN/OUT switching after NULL packet reception
   After a NULL is received, transfers cannot be restarted with the transfer direction switched from OUT to IN. This is because this module still considers the terminated transfer as an OUT transfer until the transfer count reaches its end. Note that if you switch the transfer direction to IN transfer accidentally after a NULL packet is received, a conflict occurs between an IN and an OUT transfers, which may cause illegal bus access.
   Use CH0 and CH1 with their transfer direction fixed, or if the transfer direction needs to be switched on the same channel, make sure to do it every time a transfer completes successfully due to the end of transfer count or is terminated by software reset.

Figure 43.14 shows the state transitions for DMA transfers.

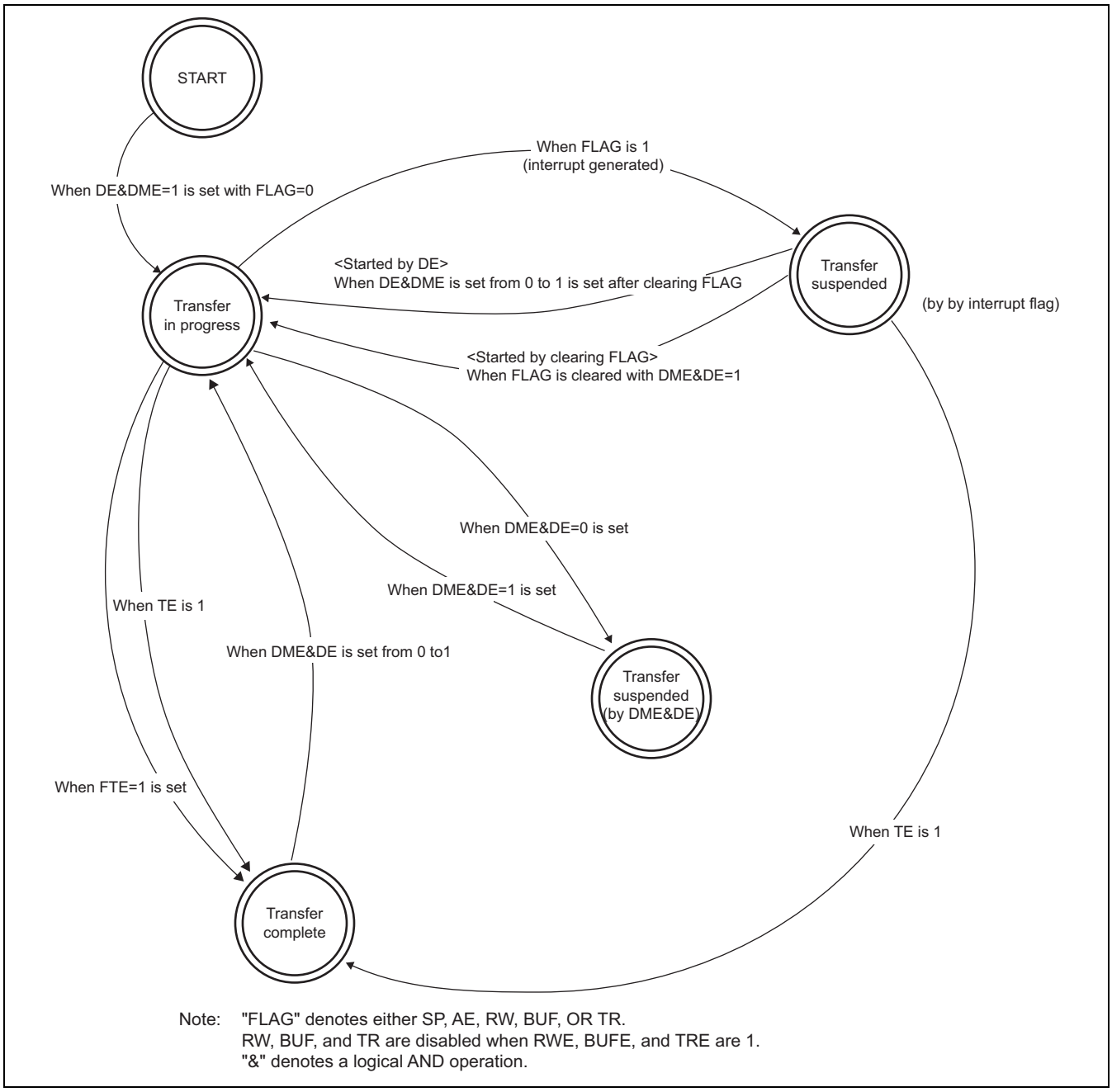


Figure 43.14 State Transitions for DMA Transfer

(4) Control sequence

Figure 43.15 shows an outline of the control sequence of this module.

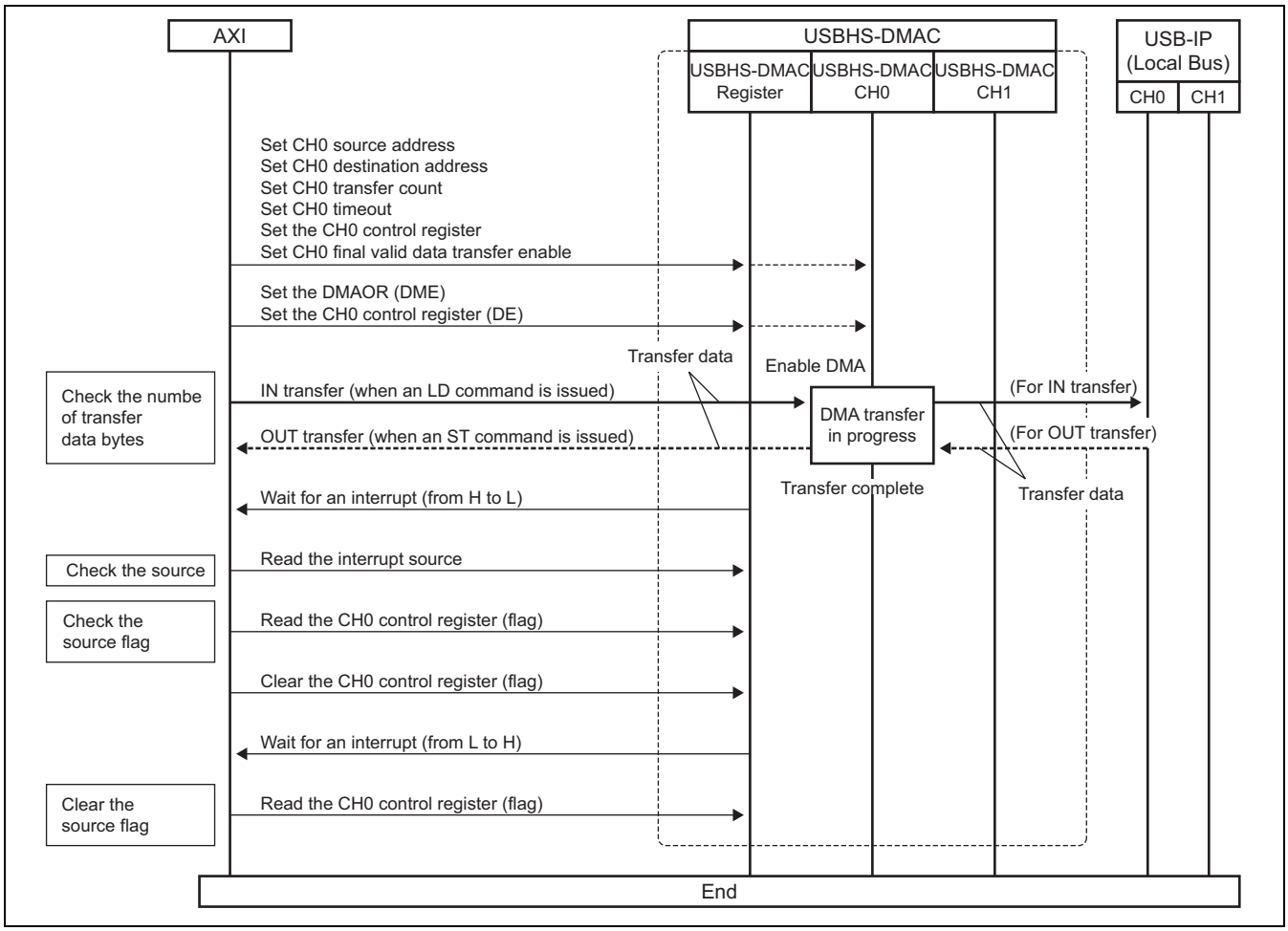


Figure 43.15 Control Sequence Overview

(5) Internal buffer configuration

This module has 64 bytes (64 bits × 8 words) of internal buffer for each of two channels. Thus, the total capacity of this module's internal buffers is 128 bytes (1,024 bits).

The internal buffers are composed of two planes each of which is organized as 64 bits × 4 words and are readable /writable on per-plane basis from the USB-IP local bus or AXI bus (plane 1 is writable when plane 0 is readable or vice versa). For 16-byte transfers, only 2 words in plane 0 and 2 words in plane 1 are used. For 8-byte transfers, only 1 word in plane 0 and 1 word in plane 1 are used.

Note that these internal buffers cannot be accessed directly by software.

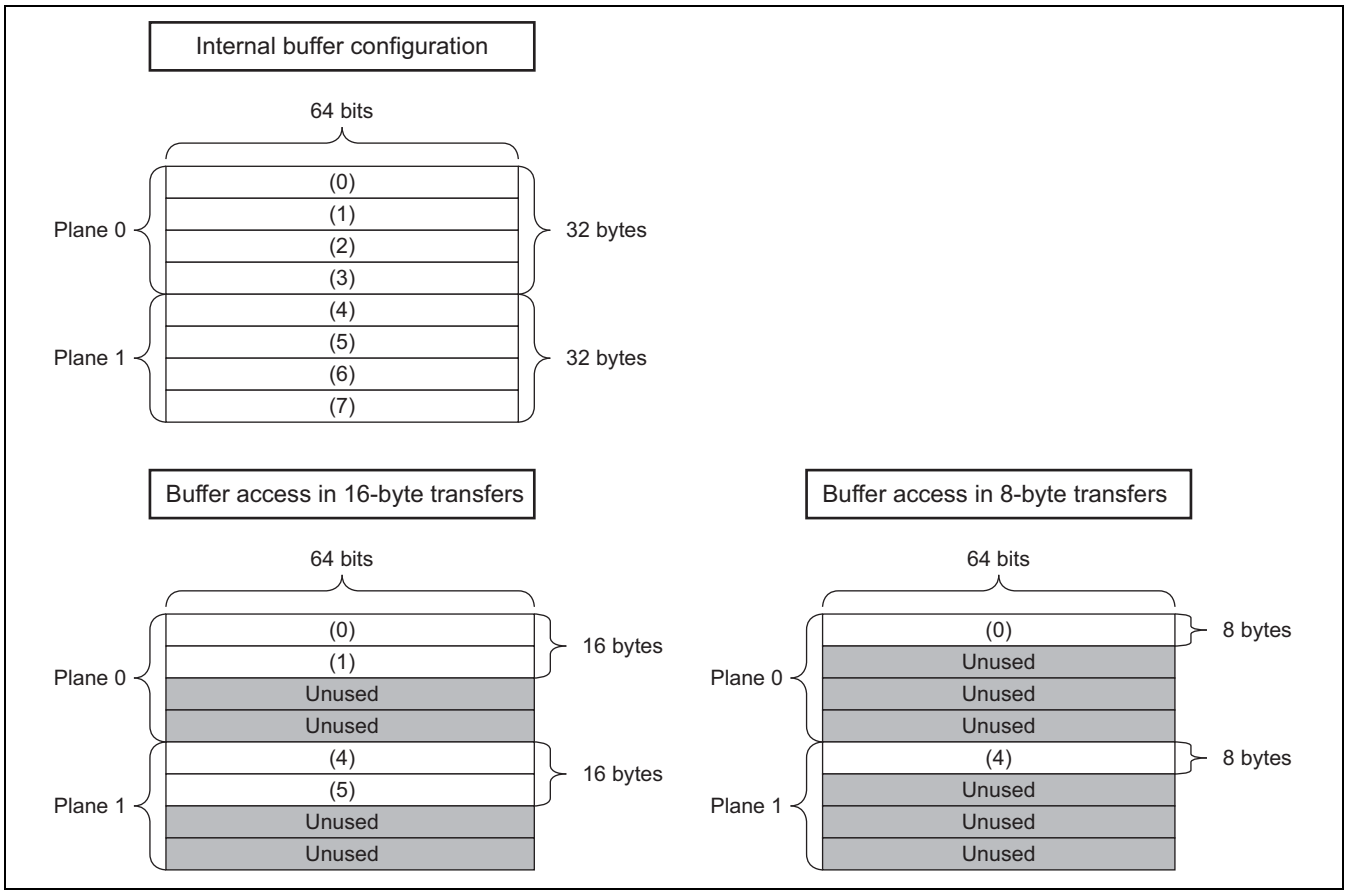


Figure 43.16 Internal Buffer Configuration and Used Area for Each Transfer Size

(6) Internal buffer control (hardware control, for reference)

(a) IN transfer (from AXI to USB)

Retrieves transfer data from a source on the AXI bus and writes it to this module's internal buffer. Reads the written data from the internal buffer and writes it to the USB-IP.

Figure 43.17 shows how the planes of this module's internal buffers are controlled during an IN transfer. In this figure, "read" and "write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words* and 1 word* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 and a transfer the read data to the USB-IP are complete, the readable plane flag is toggled (every time 2 words* and 1 word* are read for 16-byte and 8-byte transfers, respectively). Access to the AXI is prohibited during the period when both the writable plane flag and readable plane flag are set on the same plane as a read/write access conflict may occur.

Note: * 1 word = 64 bits

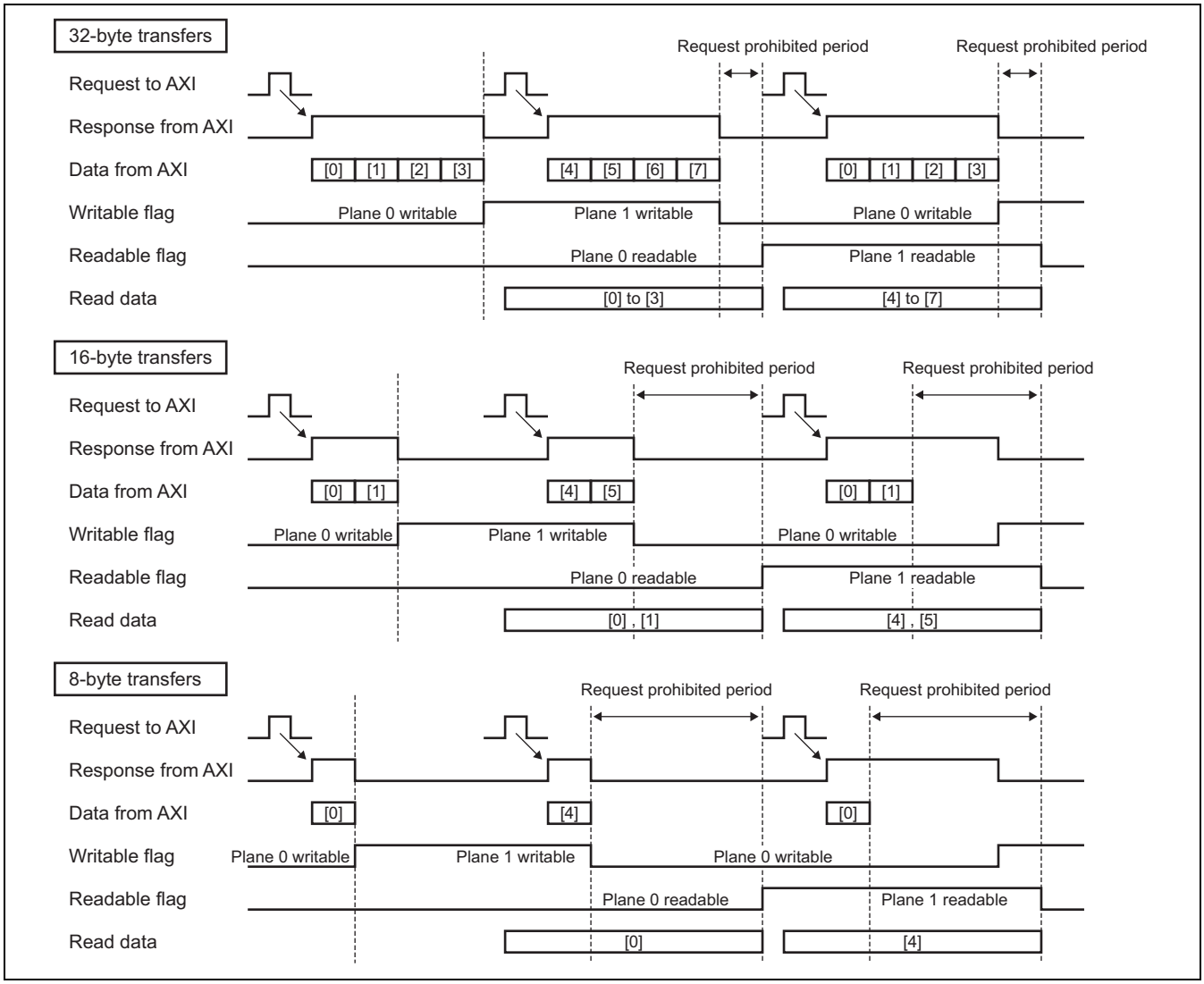


Figure 43.17 Read/Write Control for Internal Buffer: From AXI to USB (IN Transfer)

(b) OUT transfer (from USB to AXI)

Writes data read from the USB-IP to the internal buffers. Reads the written data from this module's internal buffers and writes it to the destination on the AXI bus (OUT transfer).

Figure 43.18 shows how the planes of this module's internal buffers are controlled during an OUT transfer. In this figure, "read" and "write" indicate read/write operations to this module's internal buffers.

When a write to plane 0 or plane 1 is complete, the writable plane flag is toggled (every time 2 words* and 1 word* are written for 16-byte and 8-byte transfers, respectively). When a read from plane 0 or plane 1 is complete, the readable plane flag is toggled (every time 2 words* and 1 word* are read for 16-byte and 8-byte transfers, respectively). Access to the AXI is prohibited during the period when both the writable plane flag and readable plane flag are set the same plane as a read/write access conflict may occur.

Note: * 1 word = 64 bits

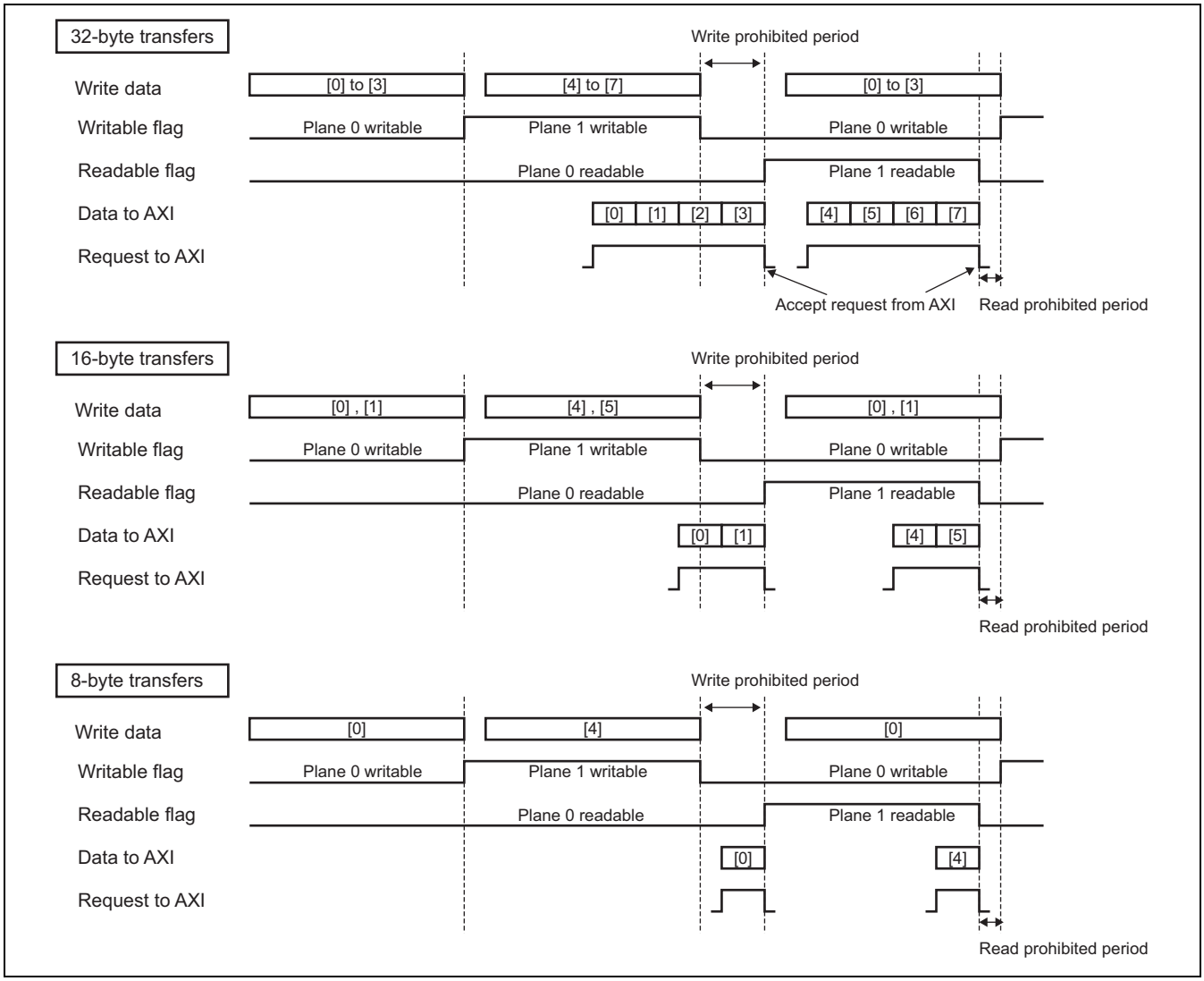


Figure 43.18 Read/Write Control for Internal Buffer: From USB to AXI (OUT Transfer)

43.4 DDM (Descriptor DMAC)

The DDM is a module that reconfigures USBDMAC. The OS on the main CPU is highly sophisticated and the overhead from interrupt notification to reconfiguration increases. To solve this problem, the DDM reconfigures the USBDMAC in a fast response time on behalf of the CPU.

Figure 43.19 shows the relationship diagram of DDM USBDMAC connection.

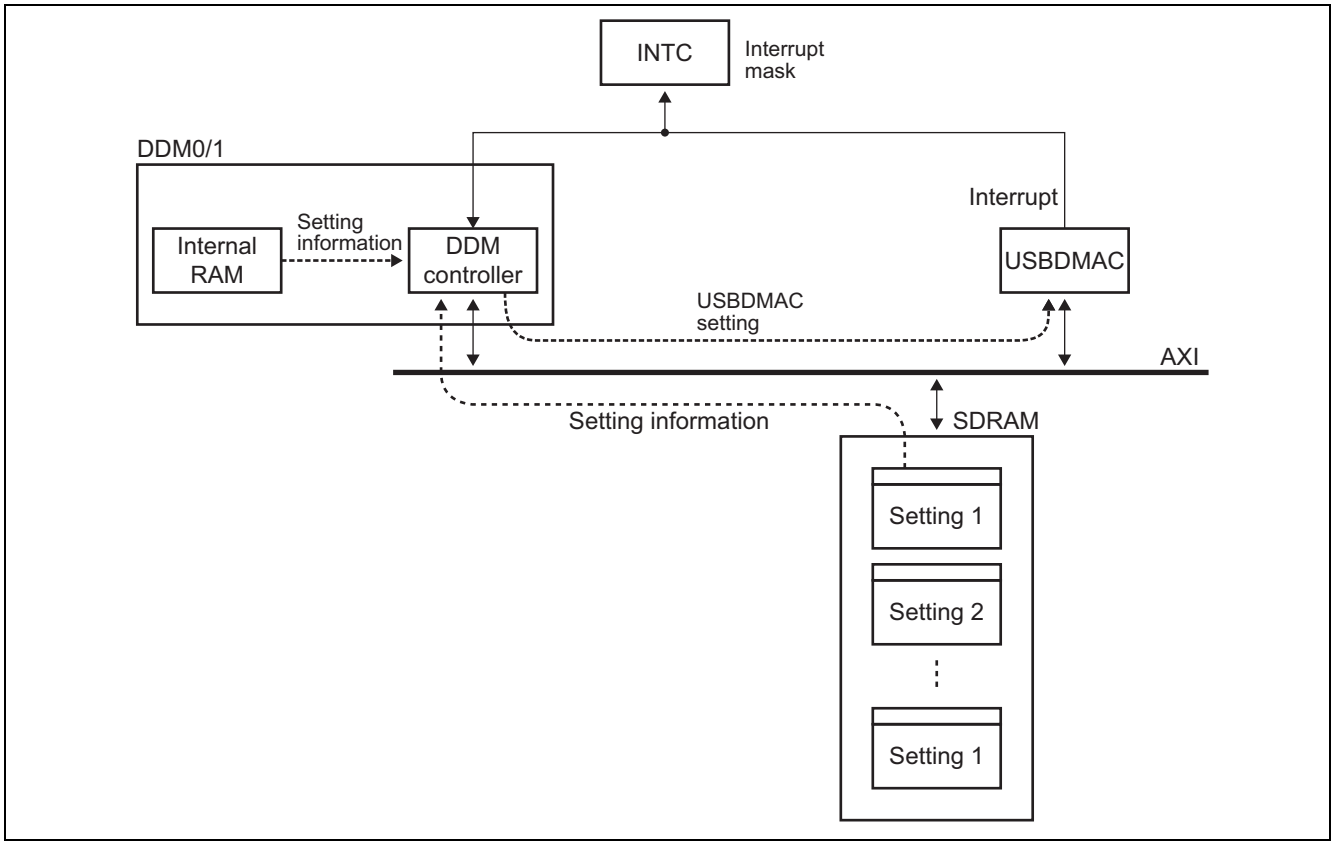


Figure 43.19 Relationship Diagram of DDM Connection

43.4.1 DDM Register Descriptions

DDM Base Address

DDM	Base Address
Channel 0	H'E65C 0000
Channel 1	H'E668 0000

Table 43.11 shows the DDM register configuration. Table 43.12 shows the register states in each operating mode.

Table 43.11 DDM Control Registers

Name	Register Abbreviation	R/W	Initial Value	Address Offset	Access Size (Bits)
DDM interrupt source mask register	DDIREQMSK	R/W	H'00000000	H'0008	32
DDM interrupt source register	DDIREQSTA	R	H'00000000	H'000C	32
DDM CH1 start source mask register 1	DDINTMSK11	R/W	H'00000000	H'0038	32
DDM CH1 start source mask register 2	DDINTMSK12	R/W	H'00000000	H'003C	32
DDM CH1 descriptor pointer	DDPTR1	R/W	H'00000000	H'0050	32
DDM CH1 control register	DDCTRL1	R/W	H'80000000	H'0054	32
DDM CH2 start source mask register 1	DDINTMSK21	R/W	H'00000000	H'0068	32
DDM CH2 start source mask register 2	DDINTMSK22	R/W	H'00000000	H'006C	32
DDM CH2 descriptor pointer	DDPTR2	R/W	H'00000000	H'0080	32
DDM CH2 control register	DDCTRL2	R/W	H'80000000	H'0084	32
DDM CH3 start source mask register 1	DDINTMSK31	R/W	H'00000000	H'0098	32
DDM CH3 start source mask register 2	DDINTMSK32	R/W	H'00000000	H'009C	32
DDM CH3 descriptor pointer	DDPTR3	R/W	H'00000000	H'00B0	32
DDM CH3 control register	DDCTRL3	R/W	H'80000000	H'00B4	32
DDM CH4 start source mask register 1	DDINTMSK41	R/W	H'00000000	H'00C8	32
DDM CH4 start source mask register 2	DDINTMSK42	R/W	H'00000000	H'00CC	32
DDM CH4 descriptor pointer	DDPTR4	R/W	H'00000000	H'00E0	32
DDM CH4 control register	DDCTRL4	R/W	H'80000000	H'00E4	32
DDM CH5 start source mask register 1	DDINTMSK51	R/W	H'00000000	H'00F8	32
DDM CH5 start source mask register 2	DDINTMSK52	R/W	H'00000000	H'00FC	32
DDM CH5 descriptor pointer	DDPTR5	R/W	H'00000000	H'0110	32
DDM CH5 control register	DDCTRL5	R/W	H'80000000	H'0114	32
DDM CH6 start source mask register 1	DDINTMSK61	R/W	H'00000000	H'0128	32
DDM CH6 start source mask register 2	DDINTMSK62	R/W	H'00000000	H'012C	32
DDM CH6 descriptor pointer	DDPTR6	R/W	H'00000000	H'0140	32
DDM CH6 control register	DDCTRL6	R/W	H'80000000	H'0144	32
DDM CH7 start source mask register 1	DDINTMSK71	R/W	H'00000000	H'0158	32
DDM CH7 start source mask register 2	DDINTMSK72	R/W	H'00000000	H'015C	32
DDM CH7 descriptor pointer	DDPTR7	R/W	H'00000000	H'0170	32
DDM CH7 control register	DDCTRL7	R/W	H'80000000	H'0174	32
DDM CH8 start source mask register 1	DDINTMSK81	R/W	H'00000000	H'0188	32
DDM CH8 start source mask register 2	DDINTMSK82	R/W	H'00000000	H'018C	32
DDM CH8 descriptor pointer	DDPTR8	R/W	H'00000000	H'01A0	32
DDM CH8 control register	DDCTRL8	R/W	H'80000000	H'01A4	32

Table 43.12 Register States in Each Operating Mode

Abbreviation	Power-On Reset	Module Standby
DDIREQMSK	Initialized	Retained
DDIREQSTA	Initialized	Retained
DDINTMSK11	Initialized	Retained
DDINTMSK12	Initialized	Retained
DDPTR1	Initialized	Retained
DDCTRL1	Initialized	Retained
DDINTMSK21	Initialized	Retained
DDINTMSK22	Initialized	Retained
DDPTR2	Initialized	Retained
DDCTRL2	Initialized	Retained
DDINTMSK31	Initialized	Retained
DDINTMSK32	Initialized	Retained
DDPTR3	Initialized	Retained
DDCTRL3	Initialized	Retained
DDINTMSK41	Initialized	Retained
DDINTMSK42	Initialized	Retained
DDPTR4	Initialized	Retained
DDCTRL4	Initialized	Retained
DDINTMSK51	Initialized	Retained
DDINTMSK52	Initialized	Retained
DDPTR5	Initialized	Retained
DDCTRL5	Initialized	Retained
DDINTMSK61	Initialized	Retained
DDINTMSK62	Initialized	Retained
DDPTR6	Initialized	Retained
DDCTRL6	Initialized	Retained
DDINTMSK71	Initialized	Retained
DDINTMSK72	Initialized	Retained
DDPTR7	Initialized	Retained
DDCTRL7	Initialized	Retained
DDINTMSK81	Initialized	Retained
DDINTMSK82	Initialized	Retained
DDPTR8	Initialized	Retained
DDCTRL8	Initialized	Retained

43.4.2 DDM Interrupt Source Mask Register (DDIREQMSK)

The DDM Interrupt Source Mask Register enables and disables interrupt sources from the DDM.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR8	END8	ERR7	END7	ERR6	END6	ERR5	END5	ERR4	END4	ERR3	END3	ERR2	END2	ERR1	ENS1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	CM8	0	R/W	Interrupt Output by CH8 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
22	CM7	0	R/W	Interrupt Output by CH7 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
21	CM6	0	R/W	Interrupt Output by CH6 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
20	CM5	0	R/W	Interrupt Output by CH5 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
19	CM4	0	R/W	Interrupt Output by CH4 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
18	CM3	0	R/W	Interrupt Output by CH3 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
17	CM2	0	R/W	Interrupt Output by CH2 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
16	CM1	0	R/W	Interrupt Output by CH1 Counter consistent 0: Disables interrupt output. 1: Enables interrupt output.
15	ERR8	0	R/W	Interrupt Output by CH8 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
14	END8	0	R/W	Interrupt Output by CH8 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.

Bit	Bit Name	Initial Value	R/W	Descriptions
13	ERR7	0	R/W	Interrupt Output by CH7 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
12	END7	0	R/W	Interrupt Output by CH7 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
11	ERR6	0	R/W	Interrupt Output by CH6 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
10	END6	0	R/W	Interrupt Output by CH6 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
9	ERR5	0	R/W	Interrupt Output by CH5 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
8	END5	0	R/W	Interrupt Output by CH5 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
7	ERR4	0	R/W	Interrupt Output by CH4 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
6	END4	0	R/W	Interrupt Output by CH4 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
5	ERR3	0	R/W	Interrupt Output by CH3 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
4	END3	0	R/W	Interrupt Output by CH3 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
3	ERR2	0	R/W	Interrupt Output by CH2 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
2	END2	0	R/W	Interrupt Output by CH2 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.
1	ERR1	0	R/W	Interrupt Output by CH1 DDM_ERR 0: Disables interrupt output. 1: Enables interrupt output.
0	END1	0	R/W	Interrupt Output by CH1 DDM_END 0: Disables interrupt output. 1: Enables interrupt output.

43.4.3 DDM Interrupt Source Register (DDIREQSTA)

The DDM Interrupt Source Register indicates the currently output interrupt source. This register is read-only. You cannot clear the interrupt source in this register. Clear the interrupt source by using the control register of each channel.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	CM8	CM7	CM6	CM5	CM4	CM3	CM2	CM1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

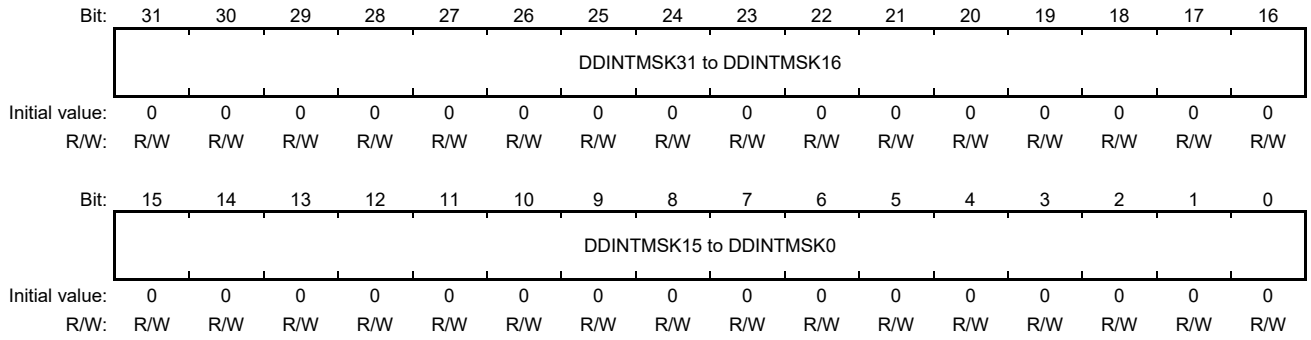
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	ERR8	END8	ERR7	END7	ERR6	END6	ERR5	END5	ERR4	END4	ERR3	END3	ERR2	END2	ERR1	ENS1
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 24	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.
23	CM8	0	R	Interrupt output by CH8 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
22	CM7	0	R	Interrupt output by CH7 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
21	CM6	0	R	Interrupt output by CH6 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
20	CM5	0	R	Interrupt output by CH5 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
19	CM4	0	R	Interrupt output by CH4 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
18	CM3	0	R	Interrupt output by CH3 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
17	CM2	0	R	Interrupt output by CH2 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
16	CM1	0	R	Interrupt output by CH1 Counter consistent 0: The interrupt is not output. 1: The interrupt is output.
15	ERR8	0	R	Interrupt output by CH8 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.

Bit	Bit Name	Initial Value	R/W	Descriptions
14	END8	0	R	Interrupt output by CH8 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
13	ERR7	0	R	Interrupt output by CH7 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
12	END7	0	R	Interrupt output by CH7 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
11	ERR6	0	R	Interrupt output by CH6 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
10	END6	0	R	Interrupt output by CH6 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
9	ERR5	0	R	Interrupt output by CH5 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
8	END5	0	R	Interrupt output by CH5 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
7	ERR4	0	R	Interrupt output by CH4 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
6	END4	0	R	Interrupt output by CH4 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
5	ERR3	0	R	Interrupt output by CH3 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
4	END3	0	R	Interrupt output by CH3 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
3	ERR2	0	R	Interrupt output by CH2 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
2	END2	0	R	Interrupt output by CH2 DDM_END 0: The interrupt is not output. 1: The interrupt is output.
1	ERR1	0	R	Interrupt output by CH1 DDM_ERR 0: The interrupt is not output. 1: The interrupt is output.
0	END1	0	R	Interrupt output by CH1 DDM_END 0: The interrupt is not output. 1: The interrupt is output.

43.4.4 DDM CHn Start Source Mask Registers 1 to 2 (DDINTMSKn1/DDINTMSKn2)

DDM CHn Start Source Mask Registers 1 to 2 mask DDM start sources.



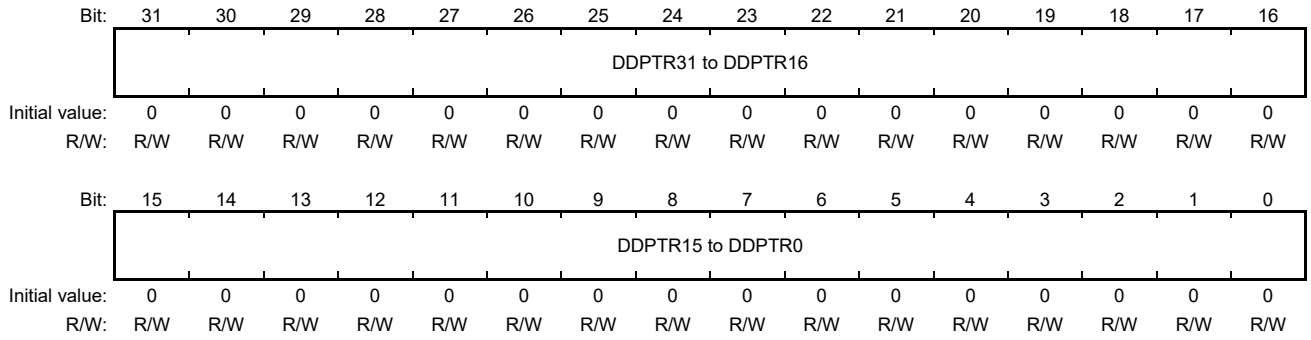
Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDINTMSK31 to DDINTMSK0	H'0000 0000	R/W	Start Source Mask 0: Does not mask the start source. 1: Masks the start source.

The current source assignment is as follows:

Bit Name	Bit	Assigned Start Source
DDINTMSKn (n = 1, 2)	31 to 20	Reserved
	19	DMACHCR19 TE bit
	18	DMACHCR18 TE bit
	17	DMACHCR17 TE bit
	16	DMACHCR16 TE bit
	15	DMACHCR15 TE bit
	14	DMACHCR14 TE bit
	13	DMACHCR13 TE bit
	12	DMACHCR12 TE bit
	11	DMACHCR11 TE bit
	10	DMACHCR10 TE bit
	9	DMACHCR9 TE bit
	8	DMACHCR8 TE bit
	7	DMACHCR7 TE bit
	6	DMACHCR6 TE bit
	5	DMACHCR5 TE bit
	4	DMACHCR4 TE bit
	3	DMACHCR3 TE bit
	2	DMACHCR2 TE bit
	1	DMACHCR1 TE bit
	0	DMACHCR0 TE bit
DDINTMSKn (n = 1, 2)	31 to 2	Reserved
	1	USBDMAC1 Interrupt
	0	USBDMAC0 Interrupt

43.4.5 DDM CHn Descriptor Pointer (DDPTRn)

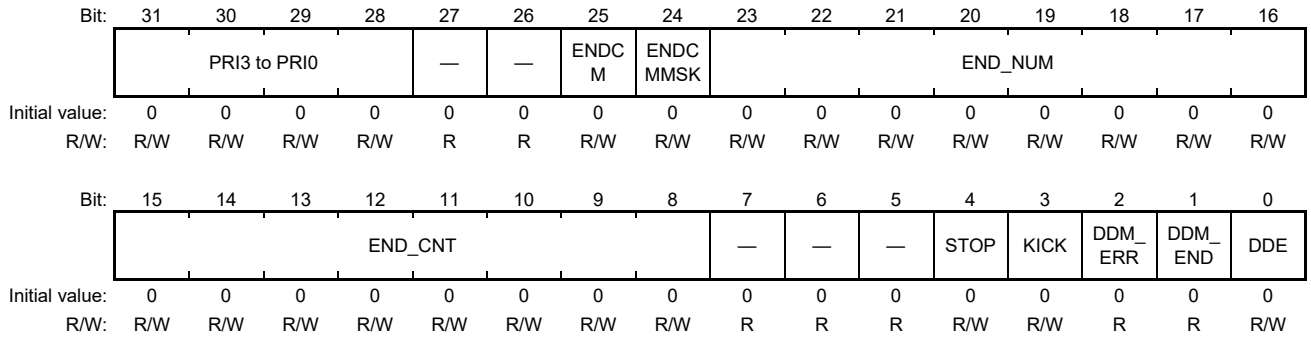
The DDM CHn Descriptor Pointer indicates the start address of setting code allocated onto memory.



Bit	Bit Name	Initial Value	R/W	Descriptions
31 to 0	DDPTR31 to DDPTR0	H'0000 0000	R/W	Descriptor pointer.

43.4.6 DDM CHn Control Register (DDCTRLn)

The DDM CHn Control Register controls start and stop of DDM.



Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	PRI3 to PRI0				—	—	ENDCM	ENDCMMSK	END_NUM							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	END_CNT								—	—	—	STOP	KICK	DDM_ERR	DDM_END	DDE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R	R	R/W	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	PRI3 to PRI0	H'0	R/W	PRI value on the AXI bus.
27, 26	—	00	R	Reserved
25	ENDCM	0	R/W	Descriptor end Counter Consistent Detection Writing 0 is possible to clear the flag. 0: Counter consistent is not detected. 1: Counter consistent is detected.
24	ENDCMMSK	0	R/W	Descriptor end Counter Consistent Detection Mask 0: Masks the ENDCM. (END_CNT is cleared to 0) 1: Does not mask the ENDCM.
23 to 16	END_NUM	All 0	R/W	Number of descriptor ends
15 to 8	END_CNT	All 0	R/W	Descriptor end Counter
7 to 5	—	000	R	Reserved
4	STOP	0	R/W	Forced Stop Function 0: Does not perform forced stop. 1: Performs forced stop.
3	KICK	0	R/W	Forced Start Function without Start Source 0: Does not perform forced start. 1: Performs forced start. This bit is automatically cleared to 0 after 1 is written.
2	DDM_ERR	0	R	Error Occurrence. The error is cleared by setting the DDE bit to 0. 0: No error occurred. 1: An error occurred.
1	DDM_END	0	R	DDM End. DDM end is cleared by setting the DDE bit to 0. 0: The DDM did not end. 1: The DDM ended.
0	DDE	0	R/W	Start Enable 0: Does not enable DDM start. 1: Enables DDM start according to the start source.

43.4.7 Internal RAM

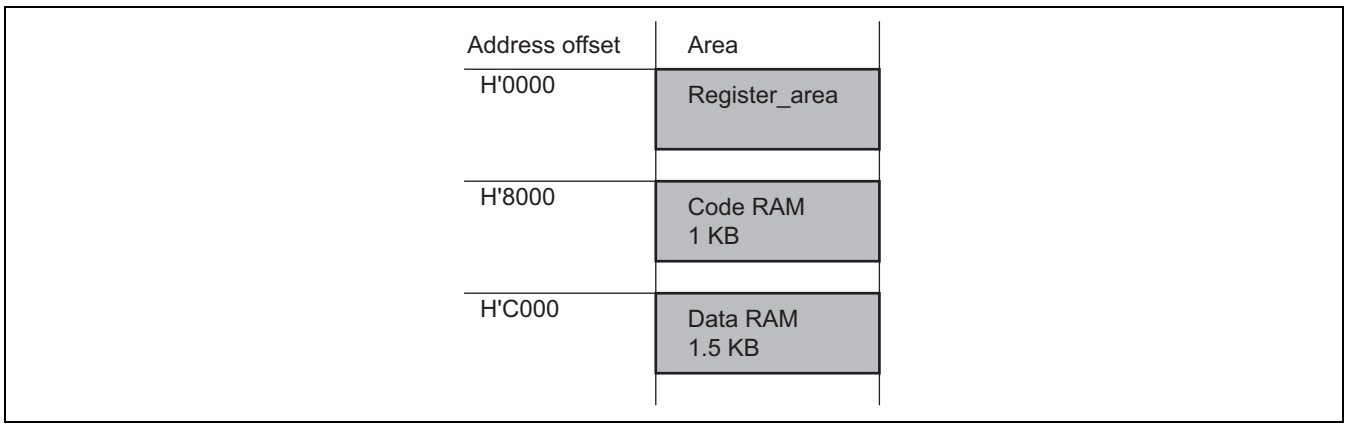


Figure 43.20 Internal RAM

DDM builds in RAM. It is the 2nd page composition of Code RAM and Data RAM. DDM can access without AXI. Access size is arbitrary. In addition, a functional difference is not in both depending on the way of calling depending on which Code RAM and Data RAM were conscious of the use.

43.4.8 Principles of Operation

To reconfigure the USBDMAC by using the DDM, use the following procedure:

1. Describing setting codes
2. Starting and ending the DDM

(1) Describing setting codes

(a) Data structure

A setting code is fixed-length data consisting of four longwords.

Setting code data consists of the following fields, starting from the beginning:

Field	bit
Operation field	32 bits
Address field	32 bits
Data field	32 bits
Bit mask field	32 bits

Note: Arrange a setting code in 16 bytes boundary.

The following describes the operation field.

(b) Operation field

The structure of the operation field is as follows:

Bit	Bit Name	Descriptions
31 to 16	HEADER	Indicates DDM setting data. H'DDDD: Normal DDM setting code Usually, set this value. H'EEEE: DDM end code Set this value when ending the channel without starting the DDM the next time. If the HEADER bits have other values, a DDM_ERR interrupt occurs. The channel of the DDM stops immediately.
15 to 8	OPERAND	Operand attribute B'00xxyyzz 00: immediately 01: register 10: pointer 11: pointer (Register value) xx: Bit mask field yy: Data field zz: Address field
7 to 4	SIZE	Specify the data access size to be set. 0000: Bytes 0001: Words 0010: Longwords
3	ENDFLG	End Flag of Setting Processing Based on This Start Source 0: Continuation 1: Setting end. The DDM waits for the next start source.
2 to 0	OPC	Operation Code 000: read (cmp/eq) (read) 001: write (write) 010: rmodw (read modify write) 011: add (addition) 100: jmp/eq (branch) 101: ror (rotate right) Others: DDM_ERR interrupt occurs

The address field, data field, and bit mask field each consist of 32 bits. The data field and bit mask field use the LSB side for word- and byte-size access.

Four of register R0-R3 of longword size can be used for every Ch.

(c) read (cmp/eq)

The read (cmp/eq) code reads the target address and compares the address with the expected values written in the data field and bit mask field.

When the comparison result becomes true, the TFLG internal variable is set to 1. TFLG is cleared to 0 when jmp/eq is executed or operation with ENDFLG is performed.

Description example 1:

The read (cmp/eq) code in this example reads the H'FE00 802C address in longwords and checks if bit 1 is set to 1.

H'DDDD 0020
H'FE00 802C
H'0000 0002
H'0000 0002

Description example 2:

The read (cmp/eq) code in this example reads the R1 in longwords and checks if bit 1 is set to 1.

H'DDDD 0120
H'0000 0001
H'0000 0002
H'0000 0002

(d) write

The write code writes data to the target address.

Description example 1:

The write code in this example accesses the H'FE00 802C address in longwords and writes H'0010 5400.

H'DDDD 0021
H'FE00 802C
H'0010 5400
H'FFFF FFFF (don't care)

Description example 2:

The write code in this example accesses the H'FE00 802C address in longwords and writes the value of H'0000 0001 address to H'FE00 802C address.

H'DDDD 0821
H'FE00 802C
H'0000 0001
H'FFFF FFFF (don't care)

(2) Description example 3:

The write code in this example accesses the H'FE00 802C address in longwords and writes the value of pointer of R1 to the H'FE00 802C address.

H'DDDD 0C21
H'FE00 802C
H'0000 0001
H'FFFF FFFF (don't care)

(a) rmodw

The rmodw code reads the target address and performs modify-write according to the values of the bit mask field.

Description example:

The rmodw code in this example reads the H'FE00 802C address in longwords and applies H'54 modify-write to bits 11 to 4.

H'DDDD 0022
H'FE00 802C
H'0000 0540
H'0000 0FF0

(b) add

The add code reads the target address and performs add-modify-write according to the values of the bit mask field.

Description example:

The add code in this example reads the H'FE00 802C address in longwords and applies H'200 add-modify-write to bits 11 to 0.

H'DDDD 0023
H'FE00 802C
H'0000 0200
H'0000 0FFF

Use 0 as the addition data corresponding to the area where the bit mask is 0.

(c) jmp/eq

If TFLG is set to 1 by the cmp/eq code, jmp/eq changes the descriptor pointer to the values of the data field. Descriptor pointer change by jmp/eq is not reflected in execution based on the next start source. Changing the descriptor pointer for the next start requires that the CHn descriptor pointer be reconfigured.

Description example:

The jmp/eq code in this example changes the descriptor pointer when TFLG is 1 to H'E558 000E.

H'DDDD 0024
H'0000 0000 (don't care)
H'E558 000E
H'0000 0000 (don't care)

(d) ror

The ror code reads the target address and performs rotate-right-write according to the values of the bit mask field. The shifted lower bits are rotated to higher bits. The ror command shifts according to the value of the data field.

Description example:

The ror code in this example reads the H'FE00 802C address in longwords and applies 8-bits right-shift.

H'DDDD 0025
H'FE00 802C
H'0000 0008
H'00FF FFFF

(e) Settings description order

Describe settings in the following order:

(1) Clearing the start source (source output side, not the DDM start source mask register)
(2) Changing the DDM source mask setting as required
(3) Reconfiguring registers such as DMAC
(4) Reconfiguring the next descriptor pointer

If several start sources are set, the last write may be unable to catch up with the next start. In such a case, end next descriptor pointer setting in (4) in read after write (do not end it in write).

(f) Example of setting DMAC restart

Use DDM CH1. The following shows an example of describing setting codes for reconfiguration when the TE bit of the DMAC1 CH0 channel control register is HI.

```
//TE bit read
    H'DDDD 0020
    H'FE00 802C
    H'0000 0002
    H'0000 0002
//TE bit clear
    H'DDDD 0021
    H'FE00 802C
    H'0010 5400
    H'FFFF FFFF
//SAR setting
    H'DDDD 0021
    H'FE00 8020
    H'5800 0000
    H'FFFF FFFF
//DAR setting
    H'DDDD 0021
    H'FE00 8024
    H'0000 0000
    H'FFFF FFFF
//TCR setting
    H'DDDD 0021
```

H'FE00 8028
H'0000 0010
H'FFFF FFFF
//DE bit write. DMA start
H'DDDD 0021
H'FE00 802C
H'0010 5401
H'FFFF FFFF
//Next descriptor pointer write.
H'DDDD 0021
H'E65C 0050
H'5800 02D0
H'FFFF FFFF
//Setting end by this start. (dummy read)
H'DDDD 0028
H'E65C 0050
H'0000 0000
H'0000 0000

(3) Start and end

(a) Starting the DDM

Make necessary settings in the DDM.

- Enabling interrupt output as required
  - Setting a DDM start source
    - Setting a descriptor pointer

After setting the above, set the DDM Enable bit of the DDM control register to 1 to enable DDM start.

Setting example:
Enable the interrupt by DDM CH1 end.
Address: H'E65C 0008 Write data: H'0000 0001
Enable DDM CH1 start when the DMAC1 TE bit is changed.
Address: H'E65C 0030 Write data: H'0000 1000
Set the DDM CH1 descriptor pointer to H'5800 0210.
Address: H'E65C 0050 Write data: H'5800 0210
Enable DDM CH1 start.
Address: H'E65C 0054 Write data: H'0000 0001

Set the KICK bit to forced start after setting the DDM Enable bit to 1. Do not set these bits at the same time.

(b) Ending the DDM

When the DDM ends, the DDM_END bit is set to 1. DDM end is cleared by setting the DDE bit to 0. To restart the DDM, you must clear the DDM_END bit by setting the DDE bit to 0.

Procedure for stopping the DDM by the STOP bit
Set the STOP bit to 1. Keep the DDE bit at 1.
Check that the DDM_END bit is 1.
Set the DDE bit to 0.

44. RCLK Watchdog Timer

44.1 Overview

This LSI includes the RCLK watchdog timer (RWDT).

This LSI can be reset by the overflow of the counter when the value of the counter has not been updated because of a system runaway.

The RWDT is a single-channel timer that uses the RCLK as an input and can be used as a watchdog timer.

RCLK is a clock, which is generated by the clock pulse generator (CPG).

44.1.1 Features

- One channel is provided.
- Can be used as a watchdog timer. Reset is generated when the counter overflows.
- A counter input clock can be chosen from:
  Clocks (RCLK/1 to RCLK/(128 × 60 × 30)) that are obtained by dividing the RCLK.

44.1.2 Block Diagram

Figure 44.1 shows block diagrams of the RWDT.

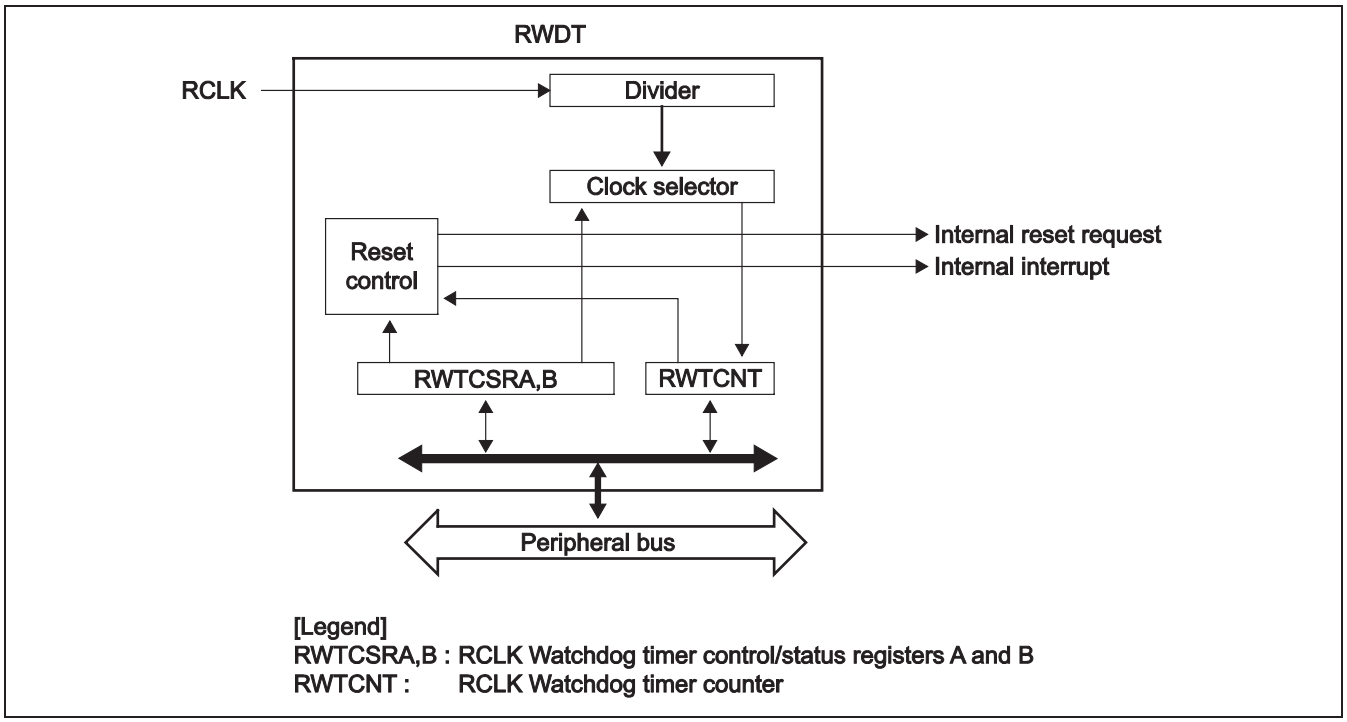


Figure 44.1 Block Diagram of RWDT

44.2 Register Descriptions for RWDT

Table 44.1 shows the RWDT register configuration. Table 44.2 shows the register state in each processing mode.

Table 44.1 Register Configuration of RWDT

Name	Abbreviation	R/W	Address	Access Size
RCLK watchdog timer counter	RWTCNT	R/W	H'E602 0000	16/32*
RCLK watchdog timer control/status register A	RWTCSRA	R/W	H'E602 0004	8/32*
RCLK watchdog timer control/status register B	RWTCSRB	R/W	H'E602 0008	8/32*

Note: * Write is performed in 32 bits and read in 16 or 8 bits.

Table 44.2 Register State of RWDT in Each Processing Mode

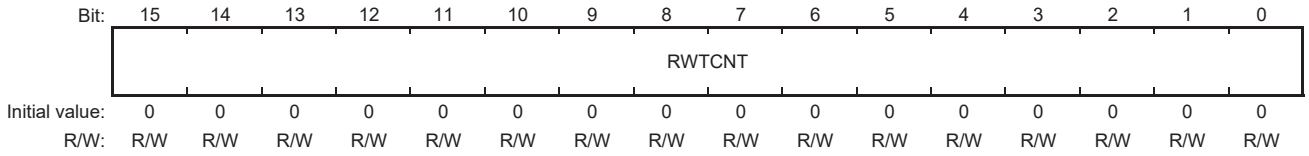
Register Abbreviation		Reset Caused by Other than Overflow	Reset Caused by Overflow*
Register	Bit		
RWTCNT	All	Initialized	Initialized
RWTCSRA	WOVF	Initialized	Retained
	Other than WOVF	Initialized	Initialized
RWTCSRB	All	Initialized	Initialized

Note: * RWDT overflow reset.

44.2.1 RCLK Watchdog Timer Counter (RWTCNT)

RWTCNT is a 16-bit readable/writable register that increments on the selected clock. When an overflow occurs, it generates a Reset. The RWTCNT counter is initialized to H'0000 by a power-on reset and RWDT software reset.

Use a long word access to write to the RWTCNT counter, with H'5A5A in the upper byte. Use a word access to read RWTCNT.



Bit	Bit Name	Initial Value	R/W	Description
15 to 0	RWTCNT	0	R/W	Timer Counter Up Bits

44.2.2 RCLK Watchdog Timer Control/Status Register A (RWTCSRA)

RWTCSRA is an 8-bit readable/writable register composed of bits to select the clock used for the count, overflow flag, and enable bit.

Use a long word access to write to RWTCSRA, with H'A5A5A5 in the upper byte. Use a byte access to read RWTCSRA.

Bit:	7	6	5	4	3	2	1	0
	TME	—	WRFLG	WOVF	WOVFE	CKS0[2:0]		
Initial value:	0	0	0	0	1	1	1	1
R/W:	R/W	R	R	R/(W)	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7	TME	0	R/W	Starts and stops timer operation. 0: Timer disabled: Count-up stops and RWTCNT value is retained 1: Timer enabled
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
5	WRFLG	0	R	Write Status Flag When this bit is 1, write access to RWTCNT is prohibited. If it isn't maintained, operation isn't secured. This bit indicates the period that the writing to RWTCNT is masked for synchronization after the writing to RWTCNT Confirm that this flag is 0 when RWTCNT is written to continuously.
4	WOVF	0	R/(W)	Indicates that the RWTCNT has overflowed. This bit isn't initialized by a generated reset by an overflow of RWDT. Write 0 to this bit before using the RWDT. 0: No overflow 1: RWTCNT has overflowed Note: Only 0 can be written to clear the flag.
3	WOVFE	1	R/W	Overflow Interrupt Disable/Enable 0: Disables interrupts due to overflow 1: Enables interrupts due to overflow

Bit	Bit Name	Initial Value	R/W	Description
2 to 0	CKS0[2:0]	111	R/W	RTC Clock Select These bits select the clock to be used for the RWTCNT count from the eight types obtainable by dividing the RCLK. The overflow period that is shown inside the parenthesis in the table is the value when the RCLK is 31.7 kHz*. Note. *: 1560 MHz / (1024 * 48) = 31.73828125 kHz. 000: Rϕ (2.1 s (RWTCNT: H'FF00 = 8.06 ms)) 001: Rϕ/4 (8.2 s (RWTCNT: H'FF00 = 32.2 ms)) 010: Rϕ/16 (33.0 s (RWTCNT: H'FF00 = 129.0 ms)) 011: Rϕ/32 (66.0 s (RWTCNT: H'FF00 = 258.0 ms)) 100: Rϕ/64 (132.0 s (RWTCNT: H'FF00 = 516.0 ms)) 101: Rϕ/128 (264.0 s (RWTCNT: H'FF00 = 1.03 s)) 110: Rϕ/1024 (2112.0 s (RWTCNT: H'FF00 = 8.25 s)) 111: RCLK select expanded mode The clock cycle varies depending on the CKS1 bit in RWTCSRB. Its initial value is Rϕ/4096 (8438.0 s (RWTCNT: H'FF00 = 33.0 s)). Note: These overflow periods are calculated from the rounded value of Rϕ = 31.7 kHz.

Note: If bits CKS0[2:0] are modified when the RWDT is operating, the up-count may not be performed correctly. Ensure that the bits CKS0[2:0] are modified only when the RWDT is not operating.

44.2.3 RCLK Watchdog Timer Control/Status Register B (RWTCSRB)

RWTCSRB is an 8-bit readable/writable register composed of bits to select the clock used for the count.

Use a word access to write to RWTCSRB, with H'A5A5A5 in the upper byte. Use a byte access to read RWTCSRB.

Bit:	7	6	5	4	3	2	1	0
	—	—	CKS1[5:0]					
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7, 6	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5 to 0	CKS1[5:0]	All 0	R/W	RCLK Select for RCLK Select Expanded Mode Selects the clock used for the RWTCNT count when the CKS0 bit in RWTCSRA is B'111. The following table shows the time values used to cause an overflow from the counter H'0000 (Overflow time from counter H'FF00). Assuming that Rϕ/128 = 264 s (1.01 s), the overflow cycle in the table is calculated for the case when the RCLK is 31.7 kHz.

CKS1[5:4] / CKS1[3:0]	B'00	B'01	B'10	B'11
H'0	8438 s (33 s)			
H'1	264 s (1.01 s)	1320 s (5.05 s)	264 min (1.01 min)	— (5.05 min)
H'2	528 s (2.02 s)	2640 s (10.1 s)	528 min (2.02 min)	— (10.1 min)
H'3	1055 s (3.03 s)	5280 s (15.2 s)	1056 min (3.03 min)	— (15.2 min)
H'4	4219 s (4.04 s)	— (20.2 s)	— (4.04 min)	— (20.2 min)
H'5	— (5.05 s)	— (25.3 s)	— (5.05 min)	— (25.3 min)
H'6	— (6.06 s)	— (30.3 s)	— (6.06 min)	— (30.3 min)
H'7	— (7.07 s)	— (35.4 s)	— (7.07 min)	— (—)
H'8	— (8.08 s)	— (40.4 s)	— (8.08 min)	— (—)
H'9	— (9.09 s)	— (45.5 s)	— (9.09 min)	— (—)
H'A	— (10.1 s)	— (50.5 s)	— (10.1 min)	— (—)
H'B	— (—)	— (55.6 s)	— (—)	— (—)
H'C	— (—)	— (60.6 s)	— (—)	— (—)
from H'D	— (—)	— (—)	— (—)	— (—)

Note: — (—): Reserved, — (xxx): Not recommendable
These overflow periods are calculated from the rounded value of Rϕ = 31.7 kHz.

Note: If the CKS1[5] to CKS1[0] bits are modified when the RWDT is running, the up-count may not be performed correctly. Ensure that these bits are modified only when the RWDT is not running.

44.2.4 Notes on Register Access

RWTCSRA: Bits TME, CKS0

RWTCSRB: Bits CKS1

After writing a value in this register, it is possible to read that value immediately, but it is not reflected in operation. 2 cycles of RCLK need to be inputted until the set-up value is reflected.

RWTCNT: Bits 15 to 0

After writing a value in this register, it is possible to read that value immediately, but it is not reflected in operation. 2 cycles of RCLK need to be inputted until the set-up value is reflected. Writing to this register, once started, is protected from further write operations until the writing operation has been completed. Read RWTCSRA. If WRFLG is 0, the next value can be written in RWTCNT.

The writing procedure to RWTCNT, RWTCSRA, and RWTCSRB differs from that of other registers with the purpose of preventing an unintended write. The procedure for writing to these registers is given below.

Writing to RWTCNT, RWTCSRA, and RWTCSRB:

- These registers must be written by a long word transfer instruction. They cannot be written by a byte or word transfer instruction.
- When writing to RWTCNT, set the upper byte to H'5A5A and transfer the lower byte as the write data. When writing to RWTCSRA and RWTCSRB, set the upper byte to H'A5A5A5 and transfer the lower byte as the write data.

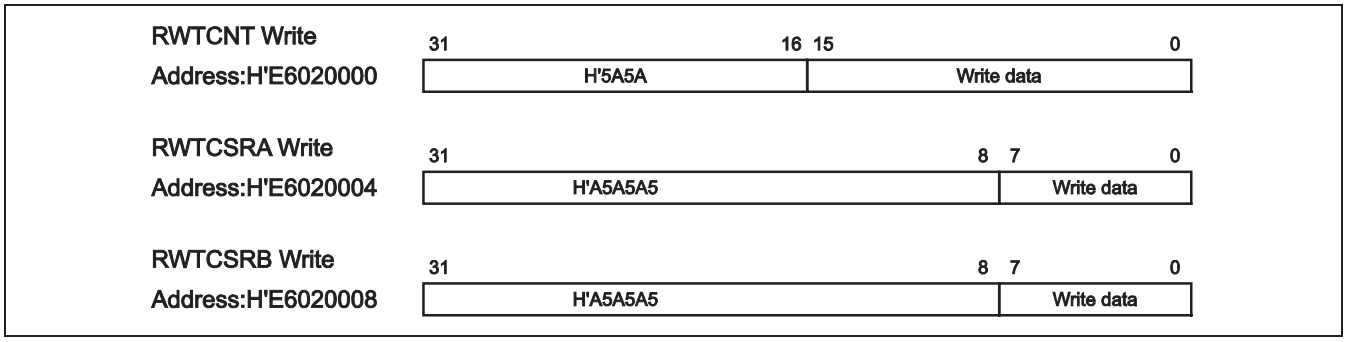


Figure 44.2 Writing to RWTCNT, RWTCSRA, and RWTCSRB

44.3 RWDT Usage

44.3.1 Control of System Runaway

After a reset, RWDT is disabled. When the counter overflow occurs after the counter starts, an internal reset is again generated. By this function, a reset can be automatically generated even when this LSI has caused a system runaway. While this LSI is operating correctly, write H'0000 (or the set value) to RWTCNT periodically so that RWTCNT does not overflow.

Take the following steps to use the RWDT.

1. Clear the TME bit in RWTCSRA to 0 to temporarily stop counting.
   (Confirm that RCLK was input more than 2 cycles.)
2. Write H'0000 or the set value in RWTCNT.
3. Clear the WOVF bit in RWTCSRA to 0.
4. Set the kind of count clock to the CKS0[2:0] bits in RWTCSRA, and CKS1[5:0] bits in RWTCSRB.
5. Confirm that RWTCSRA.WRFLG becomes 0.
   If WRFLG is 1, wait until it'll be 0.
6. Start the counting by setting the TME bit in RWTCSRA to 1.
   (TME and CKS0 can't be set at the same time. When setting that at the same time, behavior isn't guaranteed.)
7. While this LSI is operating correctly, write H'0000 (or the set value) to RWTCNT periodically so that RWTCNT does not overflow.
8. When RWTCNT overflows, Reset is generated because the RWDT sets the WOVF flag in RWTCSRA to 1. At this time, RWTCNT, RWTCSRA (excluding the WOVF bit), and RWTCSRB are initialized.

Execute a power-on reset or a software reset at that time and initialize RWDT.

When not initializing and using RWDT, behavior isn't guaranteed.

44.3.2 Module Stop

A setup of a stop of the Clock by a Module Stop signal is possible when RWDT is an Idle state. The Idle state of RWDT is when the condition of following all was satisfied.

- When RWTCSRA.TME bit is 0
- When RWTCSRA.WRFLG is 0
- When 3 or more cycles have passed in RCLK since the last Register access

44.3.3 Debugging Operation

When debugging the CPU core, stop counting up RWTCNT and retain the value of RWTCNT.

45A. Compare Match Timer 0 (CMT0)

45A.1 Features

- Two channels
- 16 bits/32 bits can be selected as counter size (bit-width).
- Provided with 32-bit constant registers and 32-bit up counters that can be written or read at any time.
- Following four clocks can be selected as counter clocks:
  — RCLK: 1/1, 1/8, 1/32, and 1/128
- One-shot operation or free-running operation is selectable.
- Compare match or overflow can be selected as interrupt source.
- Counter operation can be enabled or disabled at the time of debugging of CPU core using the debugging mode operation selector.

Figure 45A.1 shows a block diagram of the CMT0.

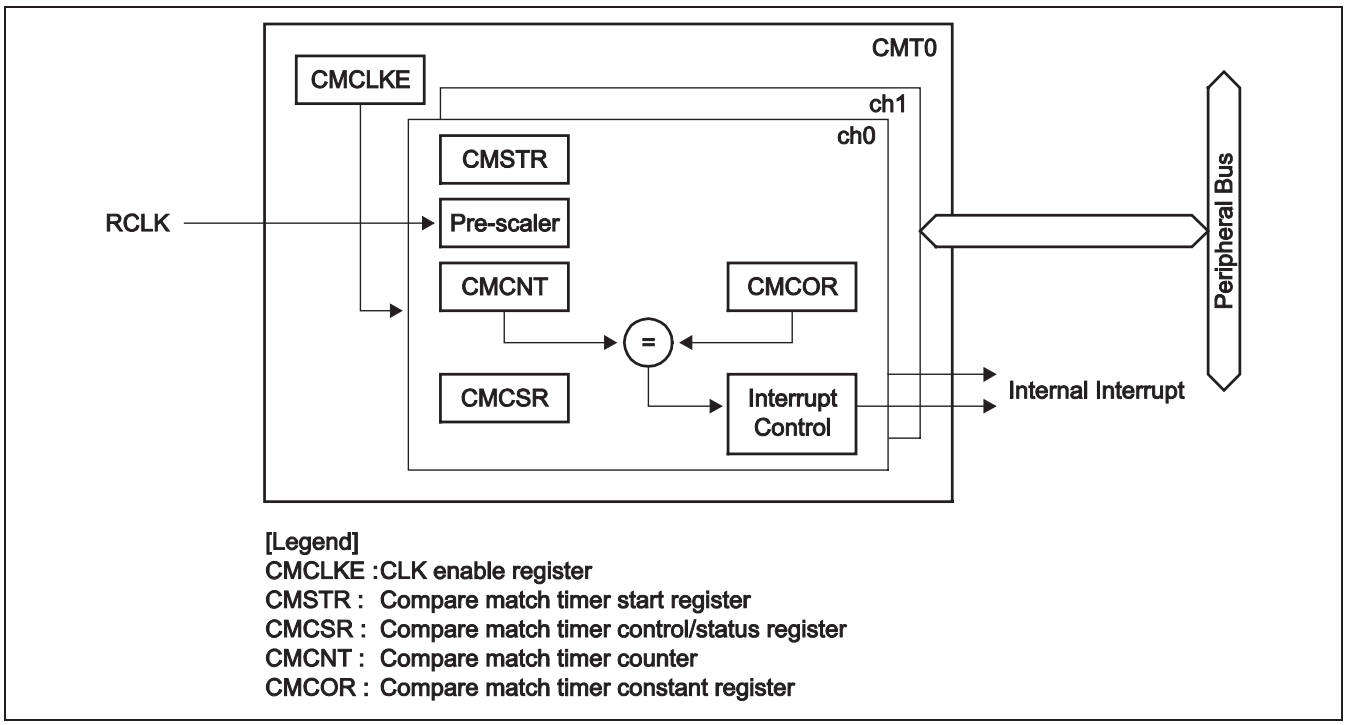


Figure 45A.1 Block Diagram of CMT0

45A.2 Register Descriptions

Table 45A.1 shows the CMT0 register configuration. Table 45A.2 shows the register states in each operating mode.

Table 45A.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
CLK enable register	CMCLKE	R/W	H'FFCA 1000	32
Compare match timer start register 0	CMSTR0	R/W	H'FFCA 0500	32
Compare match timer control/status register 0	CMCSR0	R/W	H'FFCA 0510	32
Compare match timer counter 0	CMCNT0	R/W	H'FFCA 0514	32
Compare match timer constant register 0	CMCOR0	R/W	H'FFCA 0518	32
Compare match timer start register 1	CMSTR1	R/W	H'FFCA 0600	32
Compare match timer control/status register 1	CMCSR1	R/W	H'FFCA 0610	32
Compare match timer counter 1	CMCNT1	R/W	H'FFCA 0614	32
Compare match timer constant register 1	CMCOR1	R/W	H'FFCA 0618	32

Table 45A.2 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Module Standby
CMCLKE	Initialized	Retained
CMSTR0	Initialized	Retained
CMCSR0	Initialized	Retained
CMCNT0	Initialized	Retained
CMCOR0	Initialized	Retained
CMSTR1	Initialized	Retained
CMCSR1	Initialized	Retained
CMCNT1	Initialized	Retained
CMCOR1	Initialized	Retained

45A.2.1 CLK Enable Register (CMCLKE)

CMCLKE is a 32-bit register, which specifies clock supply to each channel. When there are unused channels, set 0 to this register, for stop supplying clock to the channel. It is prohibited to stop clock supply, while counter is working.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	Ch1 clke	Ch0 clke	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 7	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
6	Ch1clke	1	R/W	0: Clock isn't supplied to ch1. 1: Clock is supplied to ch1.
5	Ch0clke	1	R/W	0: Clock isn't supplied to ch0. 1: Clock is supplied to ch0.
4 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

45A.2.2 Compare Match Timer Start Registers 0 and 1 (CMSTR0, CMSTR1)

CMSTRn (n = 0/1) is a 32-bit register which specifies the operation of compare match timer counters (CMCNTn).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	1	R/W	Count Start These bits specify start/halt of compare match timer counter (CMCNTn). 0: CMCNTn halts 1: CMCNTn starts counting

45A.2.3 Compare Match Timer Control/Status Registers 0 and 1 (CMCSR0, CMCSR1)

CMCSRn (n = 0/1) is a 32-bit register that indicates the occurrence of compare matches, enables interrupts, and sets the counter input clocks.

Do not change bits other than the CMF and OVF bits, while compare match timer counter (CMCNTn) is under counting.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	—	—	—	CMS	CMM	—	—	CMR[1:0]		DBGIVD	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	1	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNTn) and compare match timer constant register (CMCORn) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNTn and CMCORn values have not matched. [Clearing condition] Write 0 to CMF 1: CMCNTn and CMCORn values have matched. Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNTn) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNTn has not overflowed. [Clearing condition] Write 0 to OVF 1: CMCNTn has overflowed. Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNTn is prohibited, while this this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNTn is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNTn.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	CMS	0	R/W	Compare Match Timer Counter Size Specify whether the compare match timer counter (CMCNTn) is used as a 16-bit counter or a 32-bit counter. This bit specifies the valid size of compare match timer constant register (CMCORn). 0: Operates as a 32-bit counter. 1: Operates as a 16-bit counter. Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
8	CMM	1	R/W	Compare Match Mode Specify counter operation mode. 0: One-shot operation 1: Free-running operation Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
7, 6	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable an internal interrupt request in a compare match. 00: Disables an internal interrupt request. 01: Setting prohibited 10: Enables an internal interrupt request. 11: Setting prohibited Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debug mode. 0: Stops the counter operation in debug mode. 1: Enables the counter operation even in debug mode. Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits select the input clock to CMCNTn. When the count start bit (STR0) in CMSTRn is set to 1, CMCNTn begins incrementing with the clock selected by these bits. 000: Setting prohibited 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: RCLK/8 101: RCLK/32 110: RCLK/128 111: RCLK/1 Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.

45A.2.4 Compare Match Timer Counters 0 and 1 (CMCNT0, CMCNT1)

CMCNTn (n = 0 to 1) is a 32-bit register that is used as an up-counter.

To specify counter operation, set compare match timer control/status register n (CMCSRn), before starting operation of corresponding channel.

When the 16-bit counter operation is selected by the CMS bit, bits 31 to 16 of this register become invalid. When data is written to this register in 16-bit mode, write H'0000 to the upper 16 bits.

When CMCNTn is read during the counter operation, the read value may be wrong because different clock is used between counter and bus-interface. For exact value, read this register continuously, until same values are read from this register.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R/W	Compare match timer counter bit31 to 0 Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.

45A.2.5 Compare Match Timer Constant Registers 0 and 1 (CMCOR0, CMCOR1)

CMCORn (n = 0/1) is a 32-bit register that sets the compare match period with CMCNTn.

When the 16-bit counter operation is selected by the CMS bit in CMCSRn, bits 15 to 0 of this register become valid. Write H'0000 to upper 16bits in 16-bit counter operation.

An overflow is detected when CMCNTn is cleared to 0 and this register is H'FFFFFFFF.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 1	R/W	Compare match timer constant register bit31 to 0 Note: Refer to section 45A.3.5, CMT0 Register Access, for the note regarding writing to or reading from this bit.

45A.3 Operation

45A.3.1 Counter Operation

The CMT0 starts the operation of the counter by writing 1 to the STR0 bit in CMSTRn after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits, during the compare match timer n (CMCNTn) is under operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CMCSRn to 0. When the value in CMCNTn matches the value in CMCORn, the value in CMCNTn is cleared to H'00000000 and the CMF bit in CMCSRn is set to 1. Counting by CMCNTn stops after it has been cleared.

  To detect an overflow interrupt, set the value in CMCORn to H'FFFFFFFF. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'00000000 and the CMF and OVF bits in CMCSRn are set to 1.

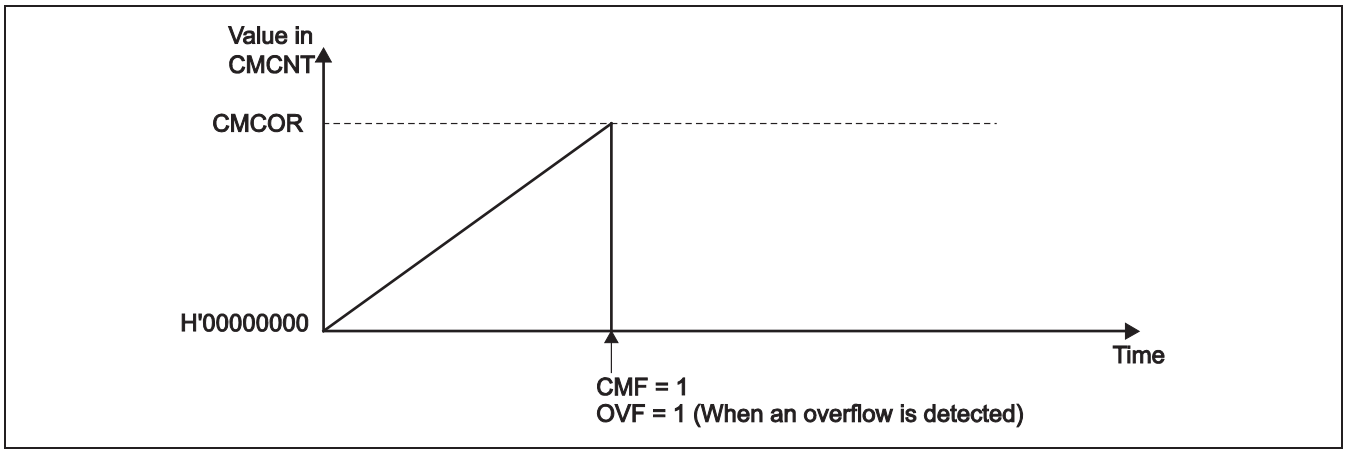


Figure 45A.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CMCSRn to 1. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'00000000 and the CMF bit in CMCSRn is set to 1. CMCNTn resumes counting-up after it has been cleared.

  To detect an overflow interrupt, set CMCORn to H'FFFFFFFF. When the values in CMCNTn and CMCORn match, CMCNTn is cleared to H'00000000 and the CMF and OVF bits in CMCSRn are set to 1.

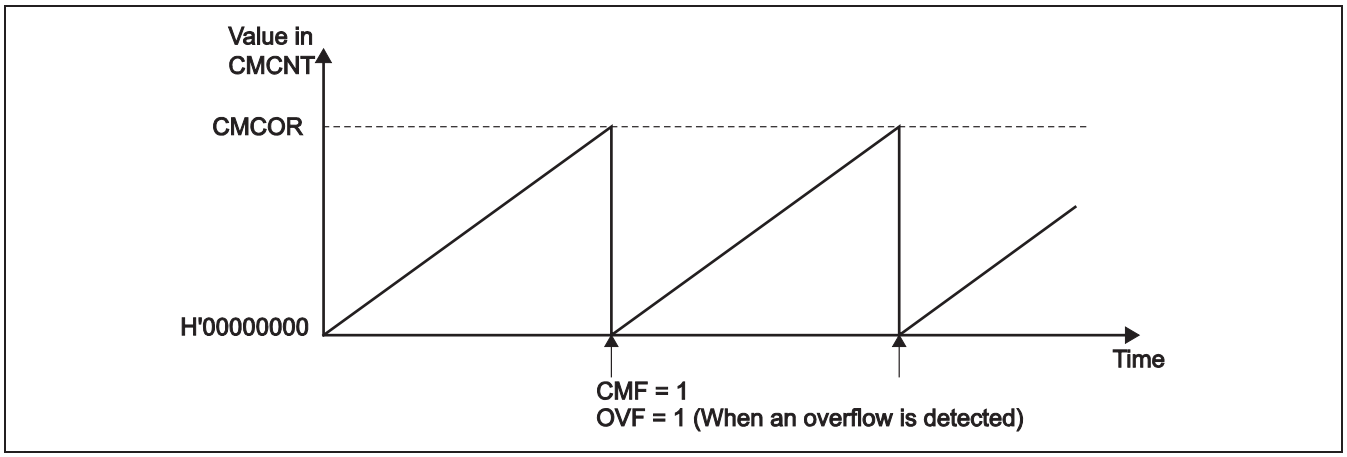


Figure 45A.3 Counter Operation (Free-Running Operation)

45A.3.2 Counter Size

In this module, the size of the counter can be selected from 16, or 32 bits. This is selected by the CMS bit in CMCSRn.

When the 16-bit size is selected, H'0000 should be used as upper 16 bits of write data to CMCORn. To detect an overflow interrupt, CMCORn must be set to H'0000FFFF.

45A.3.3 Timing for Counting by CMCNTn

In this module, the clock for the counter can be selected from among the following:

- RCLK: 1/1, 1/8, 1/32, and 1/128

The clock for the counter is selected by the CKS bits in CMCSRn. CMCNTn is incremented at the rising edge of the selected clock.

45A.3.4 Internal Interrupt Request to CPU

By CMR bits in CMCSRn, internal interrupt request to the CPU at a compare match can be asserted.

To clear the internal interrupt request to the CPU, the CMF bit should be set to 0. Set the CMF bit to 0 in the handling routine for the CMT0 interrupt.

45A.3.5 CMT0 Register Access

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK), for reflecting written data to counter behavior.

CMCSRn: Bits CKS, CMM, CMS, CMR, DBGIVD

CMCORn: Bits 31 to 0

CMSTRn: Bit STR0

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK), for reflecting written data to counter behavior.

And for following registers, write access is prohibited, while previously written data is under writing. Do not perform next write access, while CMCSRn.WRFLG is 1.

CMCNT*: Bits 31 to 0

45A.3.6 Compare Match Flag Set/Clear Timing

The CMF bit in CMCSRn is set to 1 by the compare match signal generated when CMCORn and CMCNTn match. The compare match signal is generated upon the final state of the match (timing at which the CMCNTn value is updated to 0). Consequently, after CMCORn and CMCNTn match, a compare match signal will not be generated until a CMCNTn counter clock is input. Figure 45A.4 shows the set timing of the CMF bit.

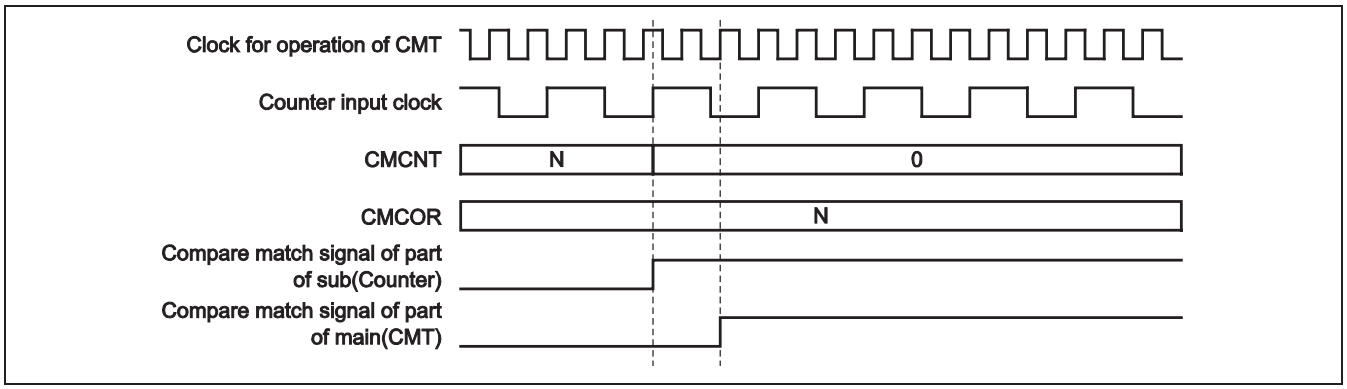


Figure 45A.4 CMF Set Timing

Set the CMF bit as 0. The CMF flag is cleared immediately.

45A.3.7 CMT0 Usage

Take the following steps to use the CMT0.

1. Clear the STR0 bit in CMSTRn to 0 to temporarily stop counting.
   (Confirm that RCLK was input more than 2 cycles.)
2. Write H'00000000 on CMCNTn.
3. Set counter size, compare match mode, type of counter clock and interrupt request and clear the bit of OVF and CMF in CMCSRn.
4. Set the value on CMCORn.
5. Confirm that CMCSRn.WRFLG is 0.
   If WRFLG is 1, wait until it'll be 0.
6. Start the counting by setting the STR0 bit in CMSTRn to 1.
   (Refer to section 45A.3.5, CMT0 Register Access)

45A.3.8 Module Stop/CMCLKE Setting

When counter is not used, clock of this module can be stopped by CMCLKE register. Please confirm that, following conditions are satisfied, before stopping counter’s clock.

- CMSTRn.STR0 bit is 0
- CMCSRn.WRFLG is 0
- 3 or more cycles have passed in RCLK, since the last Register access

45B. Compare Match Timer 1 (CMT1)

45B.1 Features

- Eight channels
- 16 bits/32 bits/48 bits can be selected as counter size (bit-width).
- 48-bit constant registers and 48-bit up counters that can be written or read at any time.
- For channel 0 to 4, following twelve clocks can be selected as counter clock.
  - CPEXϕ: 1/8, 1/32, 1/128, and 1/1
  - RCLK: 1/1, 1/8, 1/32, and 1/128
  - Pseudo 32 kHz: 1/1, 1/8, 1/32, and 1/128
- For channel 5 to 7, following four clocks can be selected as counter clock.
  - RCLK: 1/1,1/8, 1/32, and 1/128
- One-shot operation or free-running operations are selectable.
- Compare match can be used as interrupt source.
- Support Module standby mode.
- RCLK-synchronous counter start/stop mode for channel 0
- Counter operation can be enabled or disabled at the time of debugging of CPU core using the debugging mode operation selector.

Figure 45B.1 shows a block diagram of the CMT1.

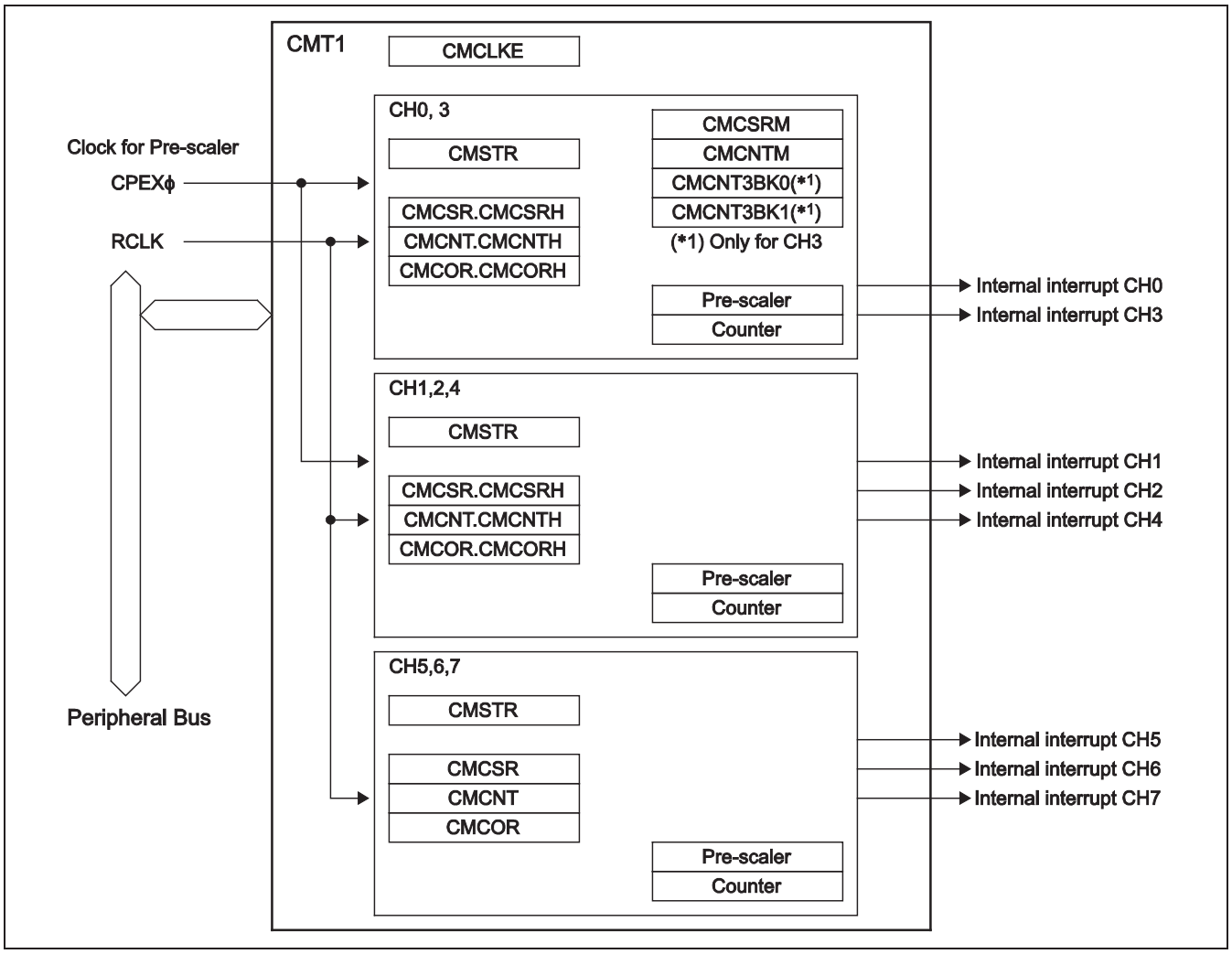


Figure 45B.1 Block Diagram of CMT1

45B.2 Register Descriptions

Table 45B.1 shows the CMT1 register configuration. Table 45B.2 shows the register states in each operating mode.

Table 45B.1 Register Configuration

Register Name	Abbreviation	R/W	Address	Access Size
CLK enable register	CMCLKE	R/W	H'E613 1000	32
Compare match timer start register 0	CMSTR0	R/W	H'E613 0000	32
Compare match timer control/status register 0	CMCSR0	R/W	H'E613 0010	32
Compare match timer counter 0	CMCNT0	R/W	H'E613 0014	32
Compare match timer constant register 0	CMCOR0	R/W	H'E613 0018	32
Compare match timer control/status register H0	CMCSRH0	R/W	H'E613 0020	32
Compare match timer counter H0	CMCNTH0	R/W	H'E613 0024	32
Compare match timer constant register H0	CMCORH0	R/W	H'E613 0028	32
Compare match timer match control/status register 0	CMCSRM0	R/W	H'E613 0040	32
Compare match timer match counter 0	CMCNTM0	R	H'E613 0044	32
Compare match timer start register 1	CMSTR1	R/W	H'E613 0100	32
Compare match timer control/status register 1	CMCSR1	R/W	H'E613 0110	32
Compare match timer counter 1	CMCNT1	R/W	H'E613 0114	32
Compare match timer constant register 1	CMCOR1	R/W	H'E613 0118	32
Compare match timer control/status register H1	CMCSRH1	R/W	H'E613 0120	32
Compare match timer counter H1	CMCNTH1	R/W	H'E613 0124	32
Compare match timer constant register H1	CMCORH1	R/W	H'E613 0128	32
Compare match timer start register 2	CMSTR2	R/W	H'E613 0200	32
Compare match timer control/status register 2	CMCSR2	R/W	H'E613 0210	32
Compare match timer counter 2	CMCNT2	R/W	H'E613 0214	32
Compare match timer constant register 2	CMCOR2	R/W	H'E613 0218	32
Compare match timer control/status register H2	CMCSRH2	R/W	H'E613 0220	32
Compare match timer counter H2	CMCNTH2	R/W	H'E613 0224	32
Compare match timer constant register H2	CMCORH2	R/W	H'E613 0228	32
Compare match timer start register 3	CMSTR3	R/W	H'E613 0300	32
Compare match timer control/status register 3	CMCSR3	R/W	H'E613 0310	32
Compare match timer counter 3	CMCNT3	R/W	H'E613 0314	32
Compare match timer constant register 3	CMCOR3	R/W	H'E613 0318	32
Compare match timer control/status register H3	CMCSRH3	R/W	H'E613 0320	32
Compare match timer counter H3	CMCNTH3	R/W	H'E613 0324	32
Compare match timer constant register H3	CMCORH3	R/W	H'E613 0328	32
Compare match timer counter 3 backup 0	CMCNT3BK0	R	H'E613 0330	32
Compare match timer counter 3 backup 1	CMCNT3BK1	R	H'E613 0334	32
Compare match timer match control/status register 3	CMCSRM3	R/W	H'E613 0340	32
Compare match timer match counter 3	CMCNTM3	R	H'E613 0344	32
Compare match timer start register 4	CMSTR4	R/W	H'E613 0400	32
Compare match timer control/status register 4	CMCSR4	R/W	H'E613 0410	32
Compare match timer counter 4	CMCNT4	R/W	H'E613 0414	32
Compare match timer constant register 4	CMCOR4	R/W	H'E613 0418	32

Register Name	Abbreviation	R/W	Address	Access Size
Compare match timer control/status register H4	CMCSRH4	R/W	H'E613 0420	32
Compare match timer counter H4	CMCNTH4	R/W	H'E613 0424	32
Compare match timer constant register H4	CMCORH4	R/W	H'E613 0428	32
Compare match timer start register 5	CMSTR5	R/W	H'E613 0500	32
Compare match timer control/status register 5	CMCSR5	R/W	H'E613 0510	32
Compare match timer counter 5	CMCNT5	R/W	H'E613 0514	32
Compare match timer constant register 5	CMCOR5	R/W	H'E613 0518	32
Compare match timer start register 6	CMSTR6	R/W	H'E613 0600	32
Compare match timer control/status register 6	CMCSR6	R/W	H'E613 0610	32
Compare match timer counter 6	CMCNT6	R/W	H'E613 0614	32
Compare match timer constant register 6	CMCOR6	R/W	H'E613 0618	32
Compare match timer start register 7	CMSTR7	R/W	H'E613 0700	32
Compare match timer control/status register 7	CMCSR7	R/W	H'E613 0710	32
Compare match timer counter 7	CMCNT7	R/W	H'E613 0714	32
Compare match timer constant register 7	CMCOR7	R/W	H'E613 0718	32

Table 45B.2 Register States in Each Operating Mode

Register Abbreviation	Power-On Reset	Module Standby
CMCLKE	Initialized	Retained
CMSTR0	Initialized	Retained
CMCSR0	Initialized	Retained
CMCNT0	Initialized	Retained
CMCOR0	Initialized	Retained
CMCSRH0	Initialized	Retained
CMCNTH0	Initialized	Retained
CMCORH0	Initialized	Retained
CMCSRM0	Initialized	Retained
CMCNTM0	Initialized	Retained
CMSTR1	Initialized	Retained
CMCSR1	Initialized	Retained
CMCNT1	Initialized	Retained
CMCOR1	Initialized	Retained
CMCSRH1	Initialized	Retained
CMCNTH1	Initialized	Retained
CMCORH1	Initialized	Retained
CMSTR2	Initialized	Retained
CMCSR2	Initialized	Retained
CMCNT2	Initialized	Retained
CMCOR2	Initialized	Retained
CMCSRH2	Initialized	Retained
CMCNTH2	Initialized	Retained
CMCORH2	Initialized	Retained
CMSTR3	Initialized	Retained

Register Abbreviation	Power-On Reset	Module Standby
CMCSR3	Initialized	Retained
CMCNT3	Initialized	Retained
CMCOR3	Initialized	Retained
CMCSRH3	Initialized	Retained
CMCNTH3	Initialized	Retained
CMCORH3	Initialized	Retained
CMCNT3BK0	Initialized	Retained
CMCNT3BK1	Initialized	Retained
CMCSRM3	Initialized	Retained
CMCNTM3	Initialized	Retained
CMSTR4	Initialized	Retained
CMCSR4	Initialized	Retained
CMCNT4	Initialized	Retained
CMCOR4	Initialized	Retained
CMCSRH4	Initialized	Retained
CMCNTH4	Initialized	Retained
CMCORH4	Initialized	Retained
CMSTR5	Initialized	Retained
CMCSR5	Initialized	Retained
CMCNT5	Initialized	Retained
CMCOR5	Initialized	Retained
CMSTR6	Initialized	Retained
CMCSR6	Initialized	Retained
CMCNT6	Initialized	Retained
CMCOR6	Initialized	Retained
CMSTR7	Initialized	Retained
CMCSR7	Initialized	Retained
CMCNT7	Initialized	Retained
CMCOR7	Initialized	Retained

45B.2.1 CLK Enable Register (CMCLKE)

CMCLKE is a 32bits register, which specify clock supply to each channel. When there are unused channels, set ‘0’ as this register, to stop supplying clock to the channel. It is prohibited to stop clock supply, while counter is working.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Ch7 clke	Ch6 clke	Ch5 clke	Ch4 clke	Ch3 clke	Ch2 clke	Ch1 clke	Ch0 clke
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15 to 8	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
7	Ch7clke	1	R/W	0: Clock isn’t supplied to ch7 1: Clock is supplied to ch7
6	Ch6clke	1	R/W	0: Clock isn’t supplied to ch6 1: Clock is supplied to ch6
5	Ch5clke	1	R/W	0: Clock isn’t supplied to ch5 1: Clock is supplied to ch5
4	Ch4clke	1	R/W	0: Clock isn’t supplied to ch4 1: Clock is supplied to ch4
3	Ch3clke	1	R/W	0: Clock isn’t supplied to ch3 1: Clock is supplied to ch3
2	Ch2clke	1	R/W	0: Clock isn’t supplied to ch2 1: Clock is supplied to ch2
1	Ch1clke	1	R/W	0: Clock isn’t supplied to ch1 1: Clock is supplied to ch1
0	Ch0clke	1	R/W	0: Clock isn’t supplied to ch0 1: Clock is supplied to ch0

45B.2.2 Compare Match Timer Start Registers 0 to 7 (CMSTRn)

CMSTRn (n = 0 to 7) is a 32-bit register which specify the operation of compare match timer counter (CMCNTn). Refer to section 45B.3.5, Register Access, for register value update timing.

(1) CMSTR0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	STR0RS	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8	STR0RS	0	R/W	RCLK-Synchronous Counter Start/Stop Mode Select 0: Normal operation Channel 0 starts or stops counting, immediately after data is written to STR0. 1: RCLK-synchronous counter start/stop mode Channel 0 starts or stops counting on detecting an RCLK rising edge, after data is written to STR0.
7 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	0	R/W	Count Start 0 These bits specify start/halt of compare match timer counter 0 (CMCNT0). 0: CMCNT0 halts 1: CMCNT0 start counting

(2) CMSTRn (n = 1 to 4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	0	R/W	Count Start 0 These bits specify start/halt of compare match timer counter (CMCNTn). 0: CMCNTn halts 1: CMCNTn starts counting

(3) CMSTRn (n = 5 to 7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	STR0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	STR0	1	R/W	Count Start 0 These bits specify start/halt of compare match timer counter (CMCNTn). 0: CMCNTn halts 1: CMCNTn starts counting

45B.2.3 Compare Match Timer Control/Status Registers 0 to 7 (CMCSRn)

CMCSRn (n = 0 to 7) is a 32-bit register that indicates the occurrence of compare match, enable interrupt and set the counter input clock.

Do not change bits other than the CMF and OVF bits, while compare match timer counter (CMCNTn) is under counting.

(1) CMCSR0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	CH0 STTF	CH0 STPF	CH0 STPF	CMS	CMM	—	—	CMR[1:0]		DBG IVD	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R/(W)	R/(W)	R/W	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNT0) and compare match timer constant register (CMCOR0) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNT0 and CMCOR0 values have not matched [Clearing conditions] • Write 0 to this bit 1: CMCNT0 and CMCOR0 values have matched Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNT0) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNT0 has not overflowed [Clearing conditions] • Write 0 to this bit 1: CMCNT0 has overflowed Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNT0 is prohibited, while this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNT0 is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNT0.

Bit	Bit Name	Initial Value	R/W	Description
12	CH0STTF	0	R/(W)	Channel 0 Start Flag When RCLK-synchronous channel 0 counter start/stop mode is selected, this flag indicates whether the counter in channel 0 started on detecting an RCLK rising edge after 1 was written to the STR0 bit in CMSR. 0: Channel 0 counter has not started. [Clearing condition] • Write 0 to CH0STTF. 1: Channel 0 counter has started. Note: Only 0 can be written to clear the flag.
11	CH0STPF	0	R/(W)	Channel 0 Stop Flag When RCLK-synchronous channel 0 counter start/stop mode is selected, this flag indicates whether the counter in channel 0 stopped on detecting an RCLK rising edge after 1 was written to the STR0 bit in CMSR. 0: Channel 0 counter has not stopped. [Clearing condition] • Write 0 to CH0STPF. 1: Channel 0 counter has stopped. Note: Only 0 can be written to clear the flag.
10	CH0SSIE	0	R/W	Channel 0 Start/Stop Interrupt Enable When RCLK-synchronous channel 0 counter start/stop mode is selected, this bit enables or disables an interrupt due to the start or stop of the counter in channel 0. 0: Disables an interrupt due to start or stop of channel 0 counter. 1: Enables an interrupt due to start or stop of channel 0 counter.
9	CMS	0	R/W	Compare Match Timer Counter Size This bit and CMCSRH0.CMSH select whether the compare match timer counter 0 (CMCNTH0[15:0], and CMCNT0[31:0]) is used as a 16-bit counter, a 32-bit counter, or a 48-bit counter. This bit also specifies valid size of the compare match timer constant register 0 (CMCORH0[15:0], and CMCOR0[31:0]). CMCSRH0[9].CMSH, and CMCSR0[9].CMS: 1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter
8	CMM	0	R/W	Compare Match Mode Specify operation mode of the counter. 0: One-shot operation 1: Free-running operation
7	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
6	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable internal interrupt request in a compare match. 00: Disables internal interrupt request 01: Setting prohibited 10: Enables an internal interrupt request 11: Setting prohibited
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debugging mode. 0: Stops the counter operation in debugging mode. 1: Continues the counter operation even in debugging mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits and CMCSRH0.CKSH select the clock input to CMCNT0. When the count start bit (STR0) for the corresponding channel is set to 1, CMCNT0 begins incrementing with the clock selected by these bits. CMCSRH0.CKSH[0]+CMCSR0.CKS[2:0]: x000: CPEXϕ/8 x001: CPEXϕ/32 x010: CPEXϕ/128 x011: CPEXϕ/1 0100: RCLK/8 0101: RCLK/32 0110: RCLK/128 0111: RCLK/1 1100: Pseudo 32 kHz/8 1101: Pseudo 32 kHz/32 1110: Pseudo 32 kHz/128 1111: Pseudo 32 kHz/1

(2) CMCSRn (n = 1 to 4)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	—	—	—	CMS	CMM	—	—	CMR[1:0]		DBGIVD	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNTn) and compare match timer constant register (CMCORn) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNTn and CMCORn values have not matched [Clearing conditions] • Write 0 to this bit 1: CMCNTn and CMCORn values have matched Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNTn) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNTn has not overflowed [Clearing conditions] • Write 0 to this bit 1: CMCNTn has overflowed Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNTn is prohibited, while this this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNTn is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNTn.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	CMS	0	R/W	Compare Match Timer Counter Size This bit and CMCSRHn.CMSH specify whether the compare match timer counter (CMCNTHn[15:0] and CMCNTn[31:0]) is used as a 16-bit counter, a 32-bit counter, or a 48-bit counter. This setting becomes the valid size for the compare match timer constant register (CMCORHn[15:0], CMCORn[31:0]). CMCSRHn[9].CMSH+CMCSRn[9].CMS: 1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter
8	CMM	0	R/W	Compare Match Mode Specify counter operation mode. 0: One-shot operation 1: Free-running operation
7, 6	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable internal interrupt request in a compare match. 00: Disables internal interrupt request 01: Setting prohibited 10: Enables an internal interrupt request 11: Setting prohibited
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debugging mode. 0: Stops the counter operation in debugging mode. 1: Continues the counter operation even in debugging mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits and CMCSRHn.CKSH specify the input clock to CMCNTn. When the count start bit (STR0) for the corresponding channel is set to 1, CMCNTn begins incrementing with the clock selected by these bits. CMCSRHn.CKSH[0], CMCSRn.CKS[2:0]: x000: CPEXϕ/8 x001: CPEXϕ/32 x010: CPEXϕ/128 x011: CPEXϕ/1 0100: RCLK/8 0101: RCLK/32 0110: RCLK/128 0111: RCLK/1 1100: Pseudo 32 kHz/8 1101: Pseudo 32 kHz/32 1110: Pseudo 32 kHz/128 1111: Pseudo 32 kHz/1

(3) CMCSRn (n = 5 to 7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CMF	OVF	WRFLG	—	—	—	CMS	CMM	—	—	CMR[1:0]		DBGIVD	CKS[2:0]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1
R/W:	R/(W)	R/(W)	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
15	CMF	0	R/(W)	Compare Match Flag This flag indicates whether values of the compare match timer counter (CMCNTn) and compare match timer constant register (CMCORn) have matched or not. Software cannot write 1 to the bit. When one-shot is selected for the counter operation, counting resumes by clearing this bit. 0: CMCNTn and CMCORn values have not matched [Clearing conditions] • Write 0 to this bit 1: CMCNTn and CMCORn values have matched Note: Only 0 can be written to clear the flag.
14	OVF	0	R/(W)	Overflow Flag This flag indicates whether the compare match timer counter (CMCNTn) has overflowed or not. Software cannot write 1 to this bit. 0: CMCNTn has not overflowed [Clearing conditions] • Write 0 to this bit 1: CMCNTn has overflowed Note: Only 0 can be written to clear the flag.
13	WRFLG	0	R	Write State Flag Write access to CMCNTn is prohibited, while this this bit is 1. Further behavior is not guaranteed, if data is written while this bit is 1. This bit indicates CMCNTn is in synchronization period for setting previously written data. Confirm that this flag is 0, before writing to CMCNTn.
12 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

Bit	Bit Name	Initial Value	R/W	Description
9	CMS	0	R/W	Compare Match Timer Counter Size Selects whether the compare match timer counter (CMCNTn) is used as a 16-bit counter or a 32-bit counter. This setting becomes the valid size for the compare match timer constant register (CMCORn). 0: Operates as a 32-bit counter. 1: Operates as a 16-bit counter.
8	CMM	1	R/W	Compare Match Mode Specify counter operation mode. 0: One-shot operation 1: Free-running operation
7, 6	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
5, 4	CMR[1:0]	00	R/W	Compare Match Request These bits enable or disable internal interrupt request in a compare match. 00: Disables internal interrupt request 01: Setting prohibited 10: Enables an internal interrupt request 11: Setting prohibited
3	DBGIVD	1	R/W	Debug Mode Operation Select Sets the counter operation in debugging mode. 0: Stops the counter operation in debugging mode. 1: Continues the counter operation even in debugging mode.
2 to 0	CKS[2:0]	111	R/W	Clock Select These bits select the clock input to CMCNTn. When the count start bit (STR0) in CMSTRn is set to 1, CMCNTn begins incrementing with the clock selected by these bits. 000: Setting prohibited 001: Setting prohibited 010: Setting prohibited 011: Setting prohibited 100: RCLK/8 101: RCLK/32 110: RCLK/128 111: RCLK/1

Notes: 1. CMCSR0 to CMCSR7
2. Refer to section 45B.3.5, Register Access, for the note regarding writing to or reading from the following bits.

45B.2.4 Compare Match Timer Control/Status Registers H0 to 4 (CMCSRHn)

CMCSRHn is a 32-bit register which specify the counter size and input clocks.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	CMSH	—	—	—	—	—	—	—	—	CKSH
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R	R	R	R	R	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
9	CMSH	0	R/W	Compare Match Timer Counter Size This bit and CMCSRn.CMS specify whether the compare match timer counter (CMCNTHn[15:0] and CMCNTn[31:0]) is used as a 16-bit counter, a 32-bit counter, or a 48-bit counter. This bit also specify valid size for the compare match timer constant register (CMCORHn[15:0], CMCORn[31:0]). CMCSRHn.CMSH[9], CMCSRn.CMS[9]: 1x: Operates as a 48-bit counter 00: Operates as a 32-bit counter 01: Operates as a 16-bit counter
8 to 1	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
0	CKSH	0	R/W	Clock Select This bit and CMCSRn.CKS[2:0] select the clock input to CMCNT. When the count start bit (STR0) for the corresponding channel is set to 1, CMCNTn begins incrementing with the clock selected by these bits. CMCSRHn.CKSH[0], CMCSRn.CKS[2:0]: x000: CPEXϕ/8 x001: CPEXϕ/32 x010: CPEXϕ/128 x011: CPEXϕ/1 0100: RCLK/8 0101: RCLK/32 0110: RCLK/128 0111: RCLK/1 1100: Pseudo 32kHz/8 1110: Pseudo 32kHz/32 1101: Pseudo 32kHz/128 1111: Pseudo 32kHz/1

Note: CMSH, CKSH For write or read, refer to section 45B.3.5, Register Access.

45B.2.5 Compare Match Timer Counters 0 to 7 (CMCNTn)

CMCNTn (n = 0 to 7) is a 32-bit register which is used as an up-counter of each channel.

To specify counter operation, set compare match timer control/status register n (CMCSRn), before starting operation of corresponding channel. When the 16-bit counter operation is selected by the CMCSRH.CMSH and CMCSR.CMS bits, bits 31 to 16 of this register is invalid. When data is written to this register in 16-bit mode, write H'0000 to the upper 16 bit.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R/W	Compare match timer counter bit31 to 0 Note: For access to this register, refer to section 45B.3.5, Register Access.

45B.2.6 Compare Match Timer Counters H 0 to 4 (CMCNTHn)

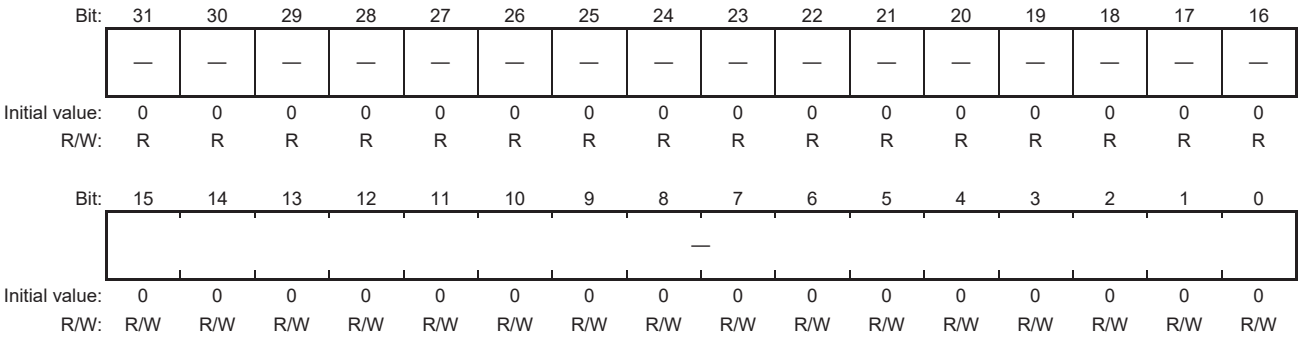
CMCNTHn (n = 0 to 4) is a 32-bit register which is used as an up-counter for channel0 to 4.

To specify counter operation, set compare match timer control/status register n (CMCSRn/CMCSRHn), before starting operation of corresponding channel. When the 48-bit counter operation is selected by the CMCSRHn.CMSH and CMCSRn.CMS bits, bits 15 to 0 of this register become valid as the upper 16-bit of 48-bit counter. The value written to this register is reflected to counter behavior, when lower data is written to CMCNTn. Write the upper data to this register first. The value is not reflected to counter's behavior, if data is not written to CMCNTn later.

When reading the value of 48-bit counter, upper 16-bit can be read out by reading bits 15 to 0 of this register.

At the same time of the reading, the value of 48-bit counter is stored to the read-buffer. After reading CMCNTHn, lower 32-bit can be read out by reading CMCNTn.

Note: If CMCNTn is read out before reading CMCNTHn, the read out value of 48-bit counter may not be correct.



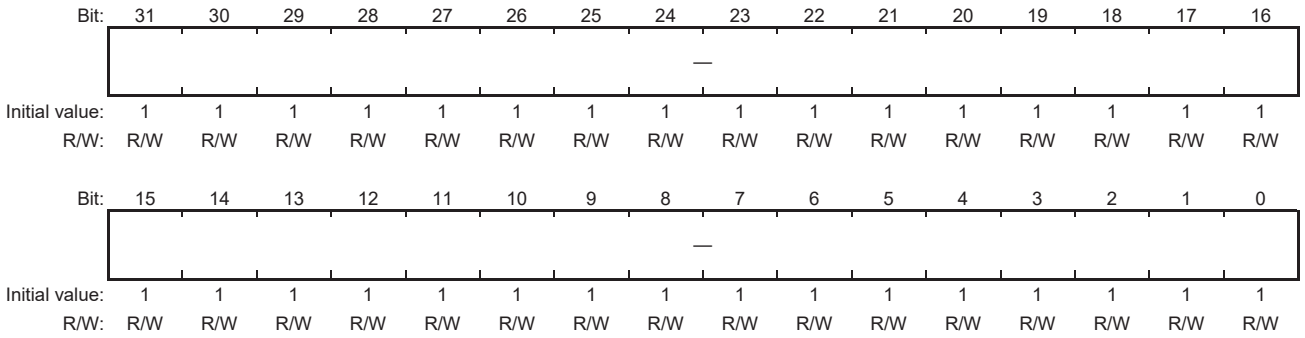
Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 0	—	All 0	R/W	Compare match timer counter H bit15 to 0 Note: For access to this register, refer to section 45B.3.5, Register Access.

45B.2.7 Compare Match Timer Constant Registers 0 to 7 (CMCORn)

CMCORn is a 32-bit register which specify the compare match period of CMCNTn for each channel.

When the 16-bit counter operation is selected by the CMCSRHn.CMSH and CMCSRn.CMS bits, bits 31 to 16 of this register is invalid. When data is written to this register in 16-bit operation mode, write H'0000 as upper 16bit.

An overflow is detected when CMCNTn is cleared to 0 and this register is H'FFFF FFFF (when the 16-bit counter operation it is H'0000 FFFF).



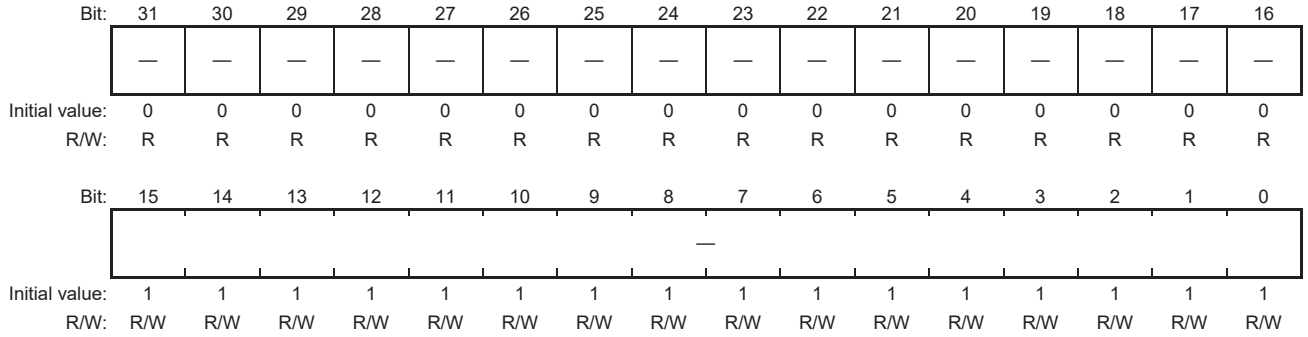
Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 1	R/W	Compare match timer constant register bit31 to 0 Note: For access to this register, refer to section 45B.3.5, Register Access.

45B.2.8 Compare Match Timer Constant Registers H0 to 4 (CMCORHn)

CMCORHn is a 32-bit register which specify the compare match period with CMCNTHn for channel0 to 4.

When the 48-bit counter operation is selected by the CMCSRHn.CMSH and CMCSRn.CMS bits, bits 15 to 0 of this register become valid as the upper 16-bit of 48-bit counter.

An overflow is detected when CMCNTHn is cleared to 0 and this register is H'FFFF.



Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
15 to 0	—	All 1	R/W	Compare match timer constant register H bit15 to 0 Note: For access to this register, refer to section 45B.3.5, Register Access.

45B.2.9 Compare Match Timer Counter 3 Backup 0 (CMCNT3BK0)

CMCNT3BK0 is a 32-bit register which stores a copy of the CMCNT3 value immediately after the counter in channel 0 stops in RCLK-synchronous channel 0 counter start/stop mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Compare match timer counter 3 backup 0 bit31 to 0

45B.2.10 Compare Match Timer Counter 3 Backup 1 (CMCNT3BK1)

CMCNT3BK1 is a 32-bit register which stores a copy of the CMCNT3 value immediately after the counter in channel 0 starts in RCLK-synchronous channel 0 counter start/stop mode.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Compare match timer counter 3 backup 1 bit31 to 0

45B.2.11 Compare Match Timer Match Control/Status Registers 0 and 3 (CMCSRMn)

CMCSRMn is a 32-bit register which resets to compare match timer match counter, and sets the counter start/halt. This register is only present in channels 0 and 3.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

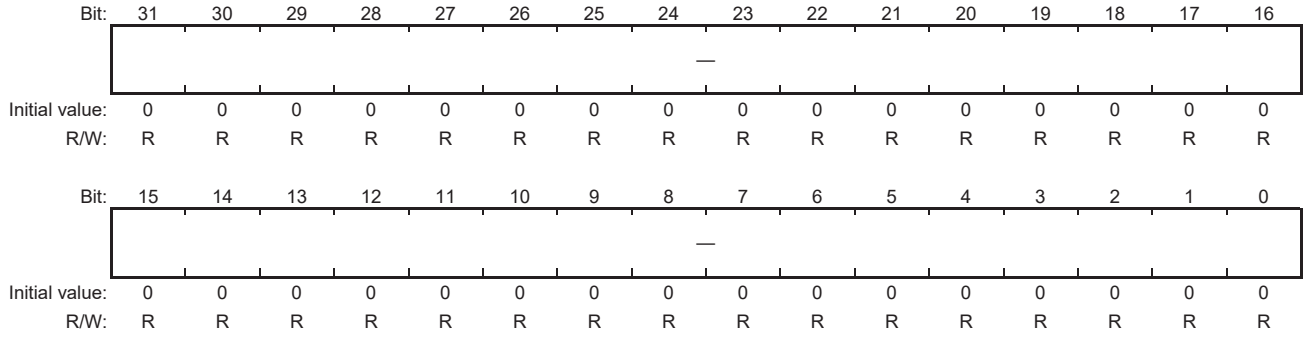
Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	WRFLG	—	—	—	—	—	—	—	—	—	—	—	—	—	CMPCLR	CMPSTART
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
15	WRFLG	0	R	Write state flag. When this Bit is 1, CMCNTMn cannot be cleared. After CMCNTMn is cleared, this bit become 1 for a while (*), for indicating synchronization period. Needs to confirm this flag is 0 or wait the period enough when continuously clearing. Note: * In the maximum, "Counter input clock 6 cycle" • Counter input clock CMCSRn.CKS2 = 0: CPEXϕ CMCSRn.CKS2 = 1: RCLK
14 to 2	—	All 0	R	Reserved This bit is always read as 0. The write value should always be 0.
1	CMPCLR	0	R/W	Counter Clear [When writing] 0: No operation 1: Clears counter When CMPCLR and CMPSTART are written 1 at the same time, the counter starts after clearing the counter. [When reading] This bit is always read as 0.
0	CMPSTART	0	R/W	Count Start This bit specifies start/halt of the compare match timer match counter (CMCNTMn) of each channel. 0: CMCNTMn Halts 1: CMCNTMn Starts counting

45B.2.12 Compare Match Timer Match Counters 0 and 3 (CMCNTMn)

CMCNTMn is a 32-bit register which is used as an up-counter. This register is only present in channels 0 and 3.

A counter operation is set by the compare match timer match control/status register (CMCSRMn). After the counter CMCNTn starts, this counter increases whenever at a compare match.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	All 0	R	Compare match timer match counter bit31 to 0

45B.3 Operation

45B.3.1 Counter Operation

The CMT1 starts the operation of the counter by writing H'1 to the STR0 bit in CMSTRn after each register has been set. Complete all of the settings before starting the operation. Do not change the register settings other than clearing flag bits, while the compare match timer (CMCNTn) is under operation.

The counter operates in one of two ways.

- One-Shot Operation

  One-shot operation is selected by setting the CMM bit in CMCSRn to H'0. When the value in CMCNTn matches the value in CMCORn, the value in CMCNTn is cleared to H'0000 0000 and the CMF bit in CMCSRn is set to H'1. Counting by CMCNTn stops after it has been cleared.

  To detect an overflow interrupt, set the value in CMCORn to H'FFFF FFFF. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'0000 0000 and the CMF and OVF bits in CMCSRn are set to H'1.

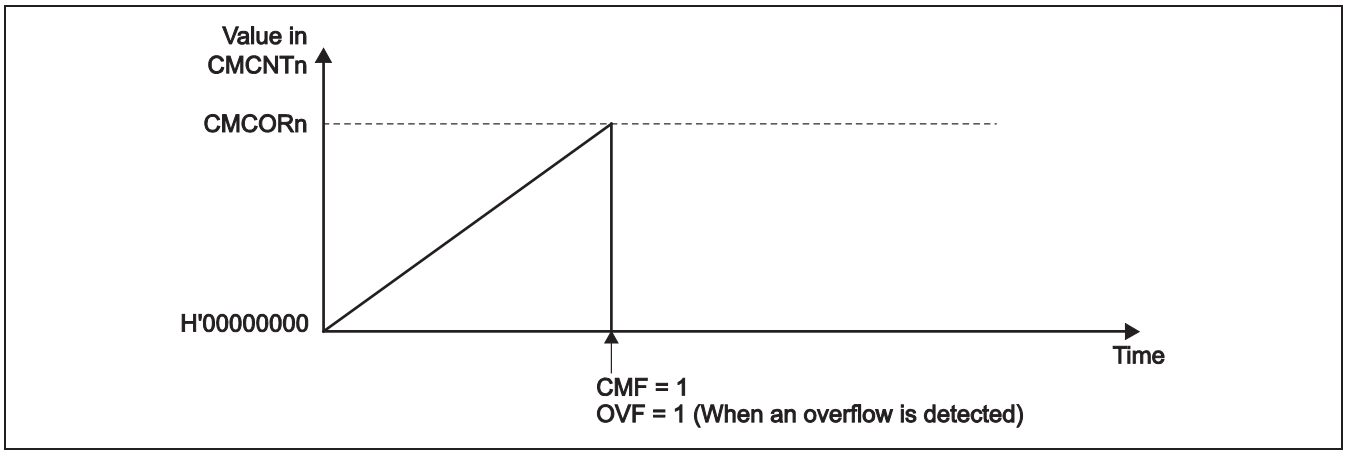


Figure 45B.2 Counter Operation (One-Shot Operation)

- Free-Running Operation

  Free-running operation is selected by setting the CMM bit in CMCSRn to H'1. When the value in CMCNTn matches the value in CMCORn, CMCNTn is cleared to H'0000 0000 and the CMF bit in CMCSRn is set to H'1. CMCNTn resumes counting-up after it has been cleared.

  To detect an overflow interrupt, set CMCORn to H'FFFF FFFF. When the values in CMCNTn and CMCORn match, CMCNTn is cleared to H'0000 0000 and the CMF and OVF bits in CMCSRn are set to H'1.

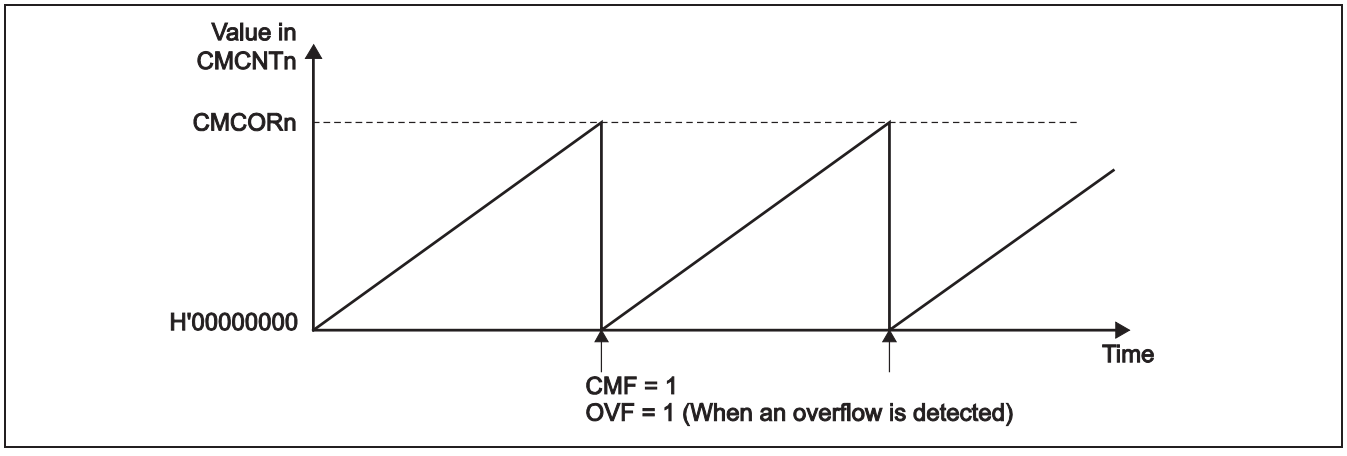


Figure 45B.3 Counter Operation (Free-Running Operation)

45B.3.2 Counter Size

In this module, the size of the counter can be selected from 16, 32, or 48 bits. This is selected by the CMS bit in CMCSRn and CMSH bit in CMCSRHn.

When the 16-bit/32-bit size is selected, upper 32 bits/16 bits of CMCORn is ignored. To detect an overflow interrupt, the value 1 must be set to valid bits of CMCORn.

(for example, H'00000000FFFF, H'0000FFFFFFFF)

45B.3.3 Timing for Counting by CMCNTn

In this module, the clock for the counter can be selected from among the following:

Channels 0 to 4:	CPEXϕ clock:	1/1, 1/8, 1/32, and 1/128
	RCLK:	1/1, 1/8, 1/32, and 1/128
	Pseudo 32-kHz:	1/1, 1/8, 1/32 and 1/128
Channel 5 to 7:	RCLK:	1/1, 1/8, 1/32, and 1/128

CPEXϕ is a clock from PLL1 via common divider. For details of these clocks, refer to section 7, Clock Pulse Generator (CPG).

Pseudo 32-kHz is a clock, which is generated inside this module. Refer to section 45B.3.8, Pseudo 32-kHz Counter.

The clock for the counter is selected by the CKS bits in CMCSRn and CKSH bit in CMCSRHn. CMCNTn is incremented at the rising edge of the selected clock.

45B.3.4 Internal Interrupt Request to CPU

By CMR bits in CMCSRn, internal interrupt request to the CPU at a compare match can be asserted.

To clear the internal interrupt request to the CPU, the CMF bit should be set to H'0. Set the CMF bit to 0 in the handling routine for the CMT1 interrupt.

45B.3.5 Register Access

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK), for reflecting written data to counter behavior.

- CMCSRn: Bits CH0SSIE(ch0), CMS, CMM, CMR[1:0], DBGIVD, CKS[2:0]
- CMCORn, CMCORHn
- CMSTRn: Bit STR0RS, STR0
- CMCSRMn: Bit CMPCLR, CMPSTART

After writing to following registers, written data can be read after writing has finished. However, it takes 2 cycles in counter input clock (RCLK or CPEXϕ), for reflecting written data to counter behavior. After writing data to this register, next write access is prohibited, until CMCSRn.WRFLG become 0.

- CMCNTn, CMCNTHn

45B.3.6 Compare Match Flag Set/Clear Timing

The CMF bit in CMCSRn is set to 1 by the compare match signal generated when CMCORn and CMCNTn match. The compare match signal is generated upon the final state of the match (timing at which the CMCNTn value is updated to H'0000). Consequently, after CMCORn and CMCNTn match, a compare match signal will not be generated until a CMCNTn counter clock is input. Figure 45B.4 shows the set timing of the CMF bit.

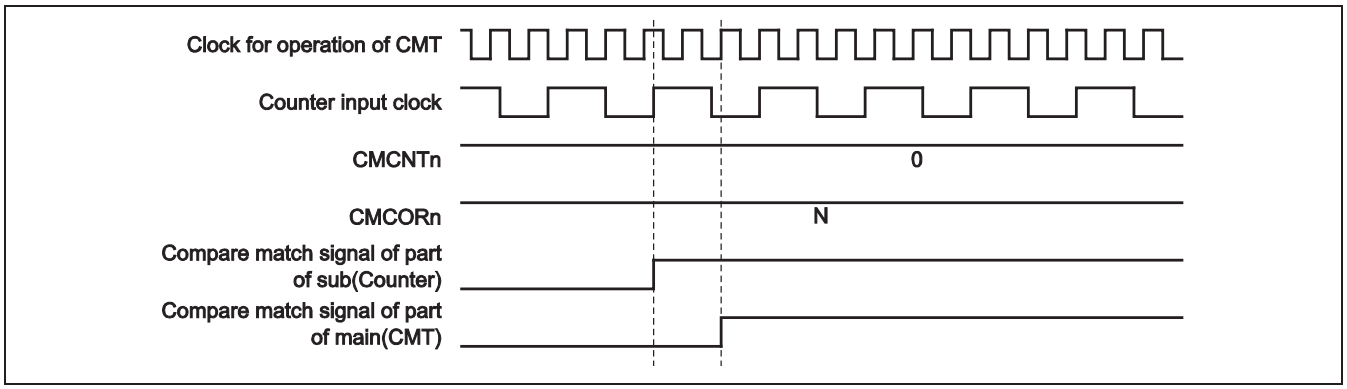


Figure 45B.4 CMF Set Timing

Set the CMF bit to 0. The CMF flag is cleared immediately.

45B.3.7 RCLK-Synchronous Counter Start/Stop Mode in Channel 0

The CMT1 provides the RCLK-synchronous counter start/stop mode in channel 0, in which channels 0 and 3 can be used together for time measurement.

Figure 45B.5 shows a flow chart for preparation.

Figure 45B.6 shows a flow chart for starting measurement.

Figure 45B.7 shows a flow chart for stopping measurement.

Figure 45B.8 shows a timing chart when measurement starts.

Figure 45B.9 shows a timing chart when measurement stops.

Figure 45B.10 shows how to calculate the time measured by the counters.

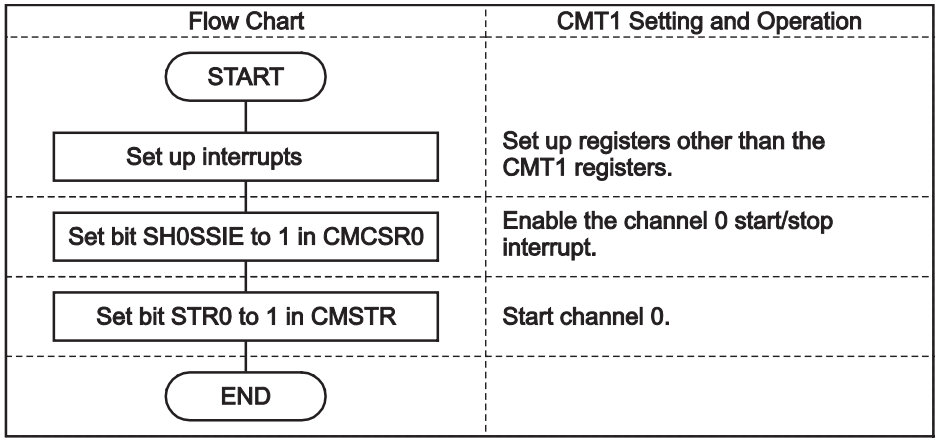


Figure 45B.5 Flow Chart for Preparation

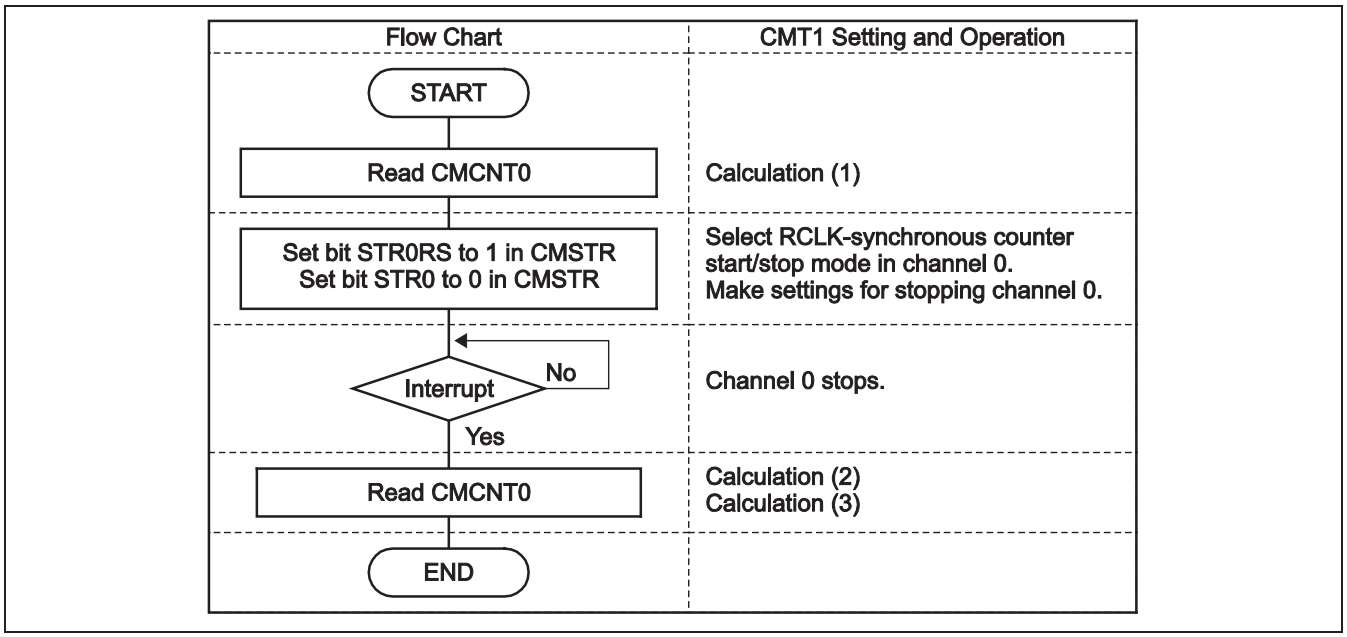


Figure 45B.6 Flow Chart for Starting Measurement

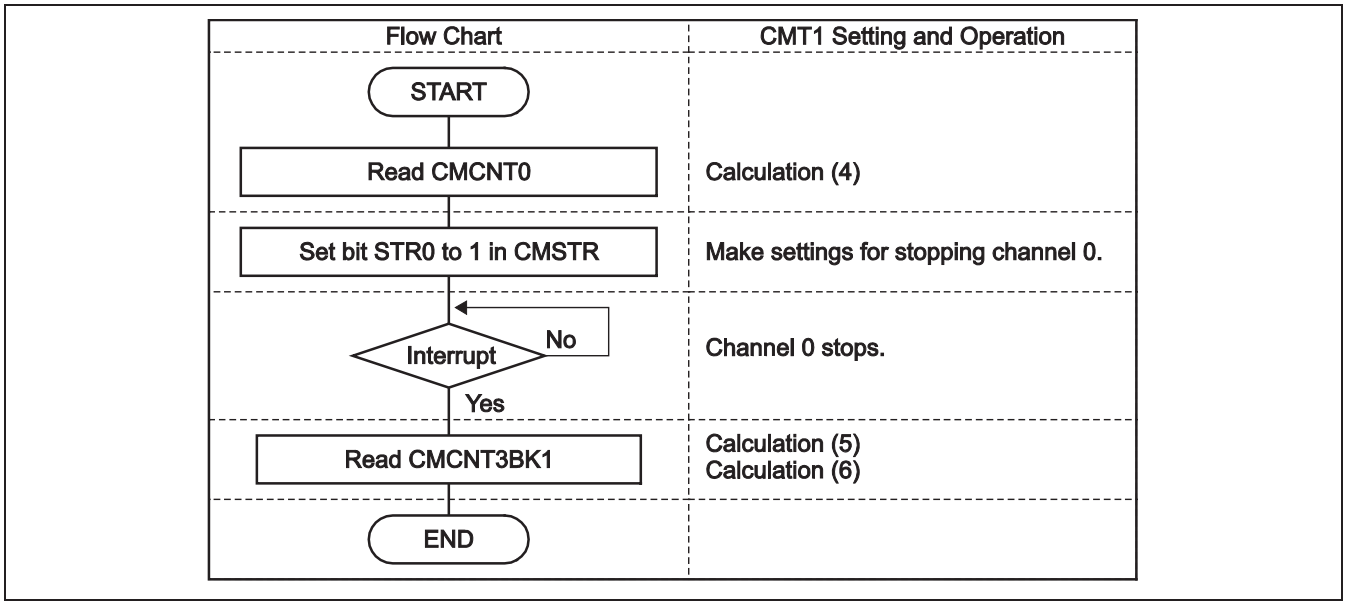


Figure 45B.7 Flow Chart for Stopping Measurement

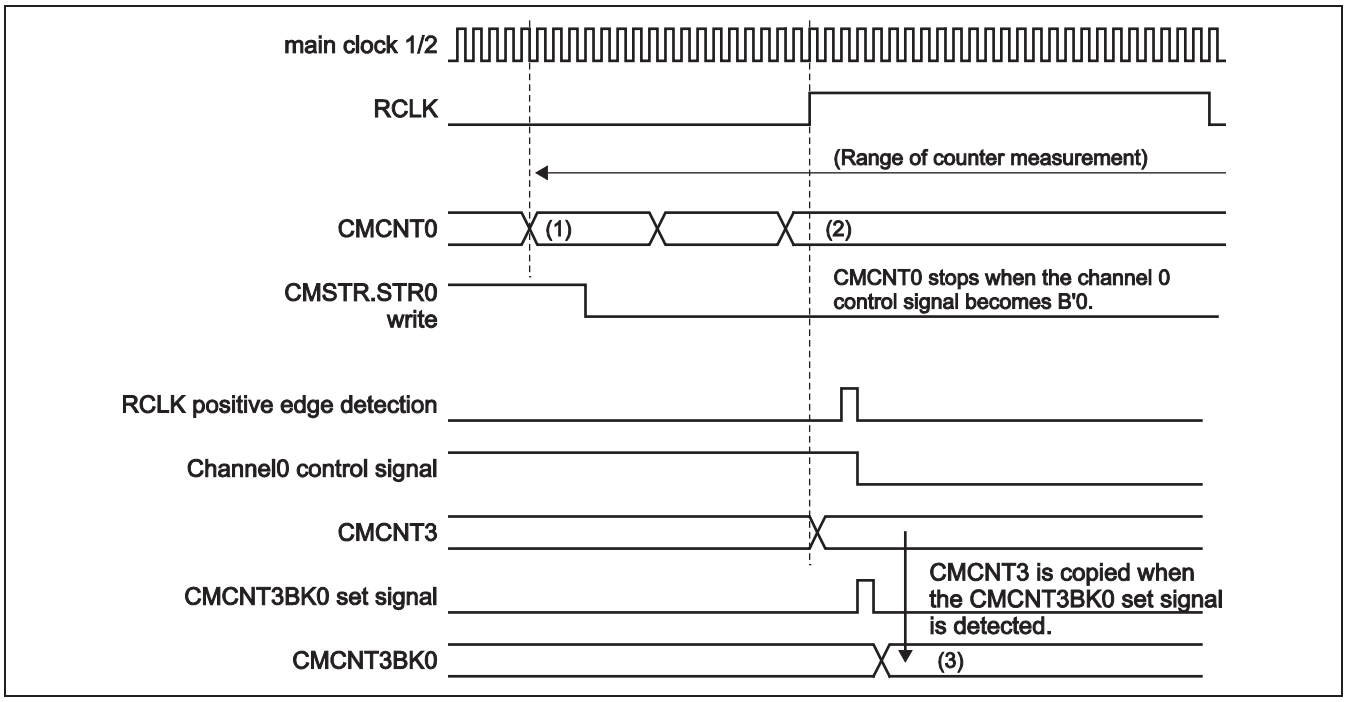


Figure 45B.8 Timing Chart When Measurement Starts

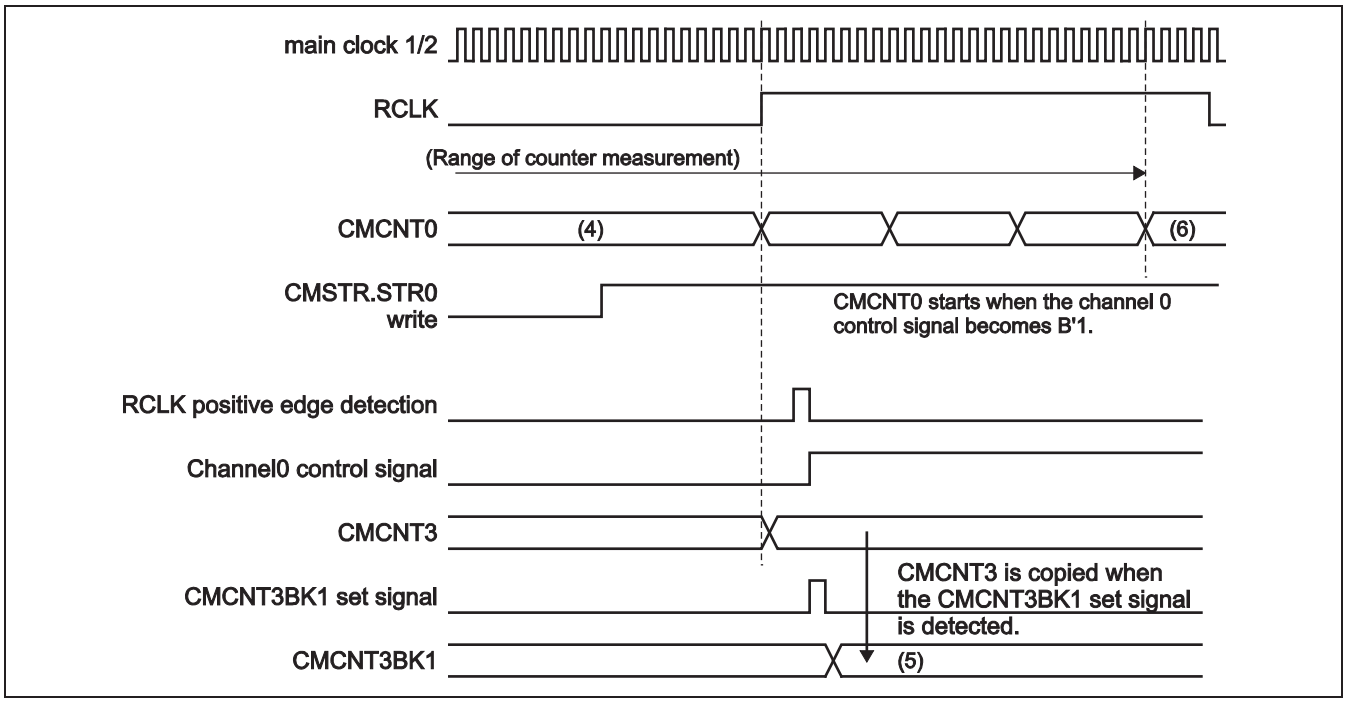


Figure 45B.9 Timing Chart When Measurement Stops

$$(((2) - (1)) + ((6) - (4) - 1)) \times Tapc + ((5) - (3)) \times Tr$$

Tapc : Cycle of main clock 1/2

Tr : Cycle of RCLK

Figure 45B.10 Calculation of Time Measured by Counters

45B.3.8 Pseudo 32-kHz Counter

Pseudo 32-kHz clock is created inside this module, based on RCLK by Pseudo 32-kHz Counter. By removing 3 edge of RCLK every 128 cycle, Pseudo 32-kHz clock is generated. By this edge removing, frequency of this clock becomes 128/131 of RCLK.

45B.3.9 CMT1 Usage

Take the following steps to use the CMT1.

1. Clear the STR0 bit in CMSTRn to 0 to temporarily stop counting.
   (Confirm that Counter input clock was input more than 2 cycles.)
2. Write H'00000000 on CMCNTn.
3. Set counter size, compare match mode, kind of count clock and interrupt request and clear the bit of OVF and CMF in CMCSRn.
4. Set the value on CMCORn.
5. Confirm that CMCSRn.WRFLG is 0.
   If WRFLG is 1, wait until it'll be 0.
6. Start the counting by setting the STR0 bit in CMSTRn to 1 (refer to section 45B.3.5, Register Access).

45B.3.10 Module Stop/ CMCLKE Setting

When counter is not used, clock of this module can be stopped by CMCLKE register. Please confirm that, following conditions are satisfied, before stopping counter’s clock.

- CMSTRn.STR0 bit is 0
- CMCSRn.WRFLG is 0
- 3 or more cycles have passed in Counter input clock since the last Register access

46. Timer Unit (TMU)

This LSI includes a 32-bit timer unit (TMU) with 12 channels (channels 0 to 11).

Channels 0 to 2, 3 to 5, 6 to 8, and 9 to 11 are grouped into timers 0, 1, 2 and 3, respectively.

For channels 0 to 2, CPϕ is provided as a base clock. For channels 3 to 11, Pϕ is provided.

46.1 Features

TMU has the following features:

- Auto-reload type 32-bit down counter is provided for each channel
- Input capture function provided: Channels 5 and 8
- Selection of rising edge or falling edge as external clock input edge when external clock is selected or input capture function is used: Channels 3 to 8
- 32-bit timer constant register for auto-reload use, readable/writable at any time, and 32-bit down-counter are provided for each channel
- Selection of five counter input clocks: Channels 0 to 2
  Five peripheral clocks (CPϕ/4, CPϕ/16, CPϕ/64, CPϕ/256, and CPϕ/1024)
- Selection of six counter input clocks: Channels 3 to 8
  External clock (TCLK1/2), and five peripheral clocks (Pϕ/4, Pϕ/16, Pϕ/64, Pϕ/256, and Pϕ/1024)
- Selection of five counter input clocks: Channels 9 to 11
  Five peripheral clocks (Pϕ/4, Pϕ/16, Pϕ/64, Pϕ/256, and Pϕ/1024)
- Two interrupt sources
  One underflow source (each channel) and one input capture source (channels 5 and 8)

Figure 46.1 show block diagrams of TMU.

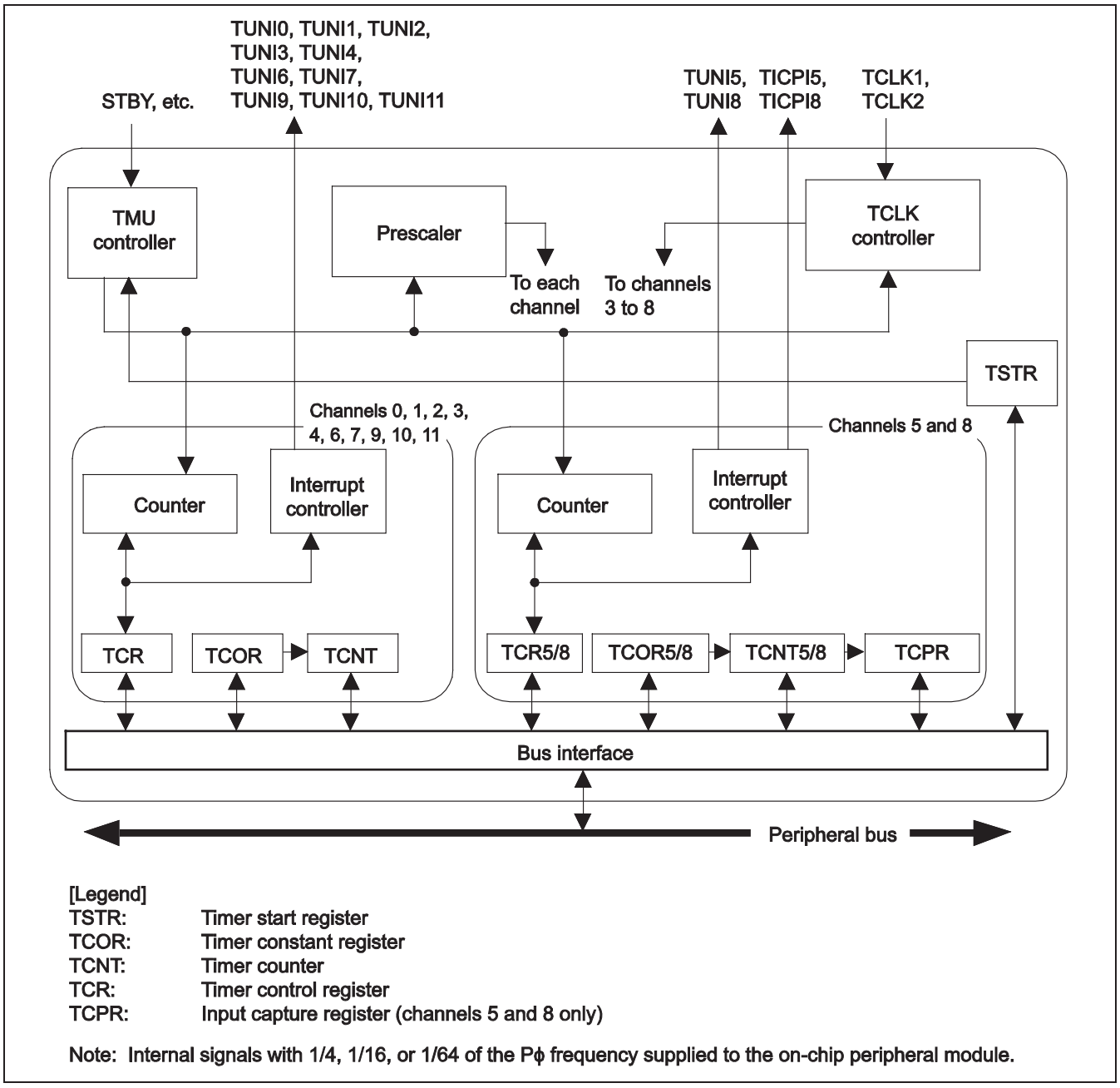


Figure 46.1 Block Diagram of TMU

46.2 Input/Output Pins

Table 46.1 shows the pin configuration of the TMU.

Table 46.1 Pin Configuration

Name	Abbreviation	I/O	Function
Clock input 1	TCLK1	Input	External clock input pin for channels 3 to 5/ input capture control input pin for channel 5
Clock input 2	TCLK2	Input	External clock input pin for channels 6 to 8/ input capture control input pin for channel 8

46.3 Register Descriptions

The TMU has the following registers. Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

Table 46.2 Register Configuration (1)

Channel	Name	Abbreviation	R/W	Address	Size
Common to 0 to 2	Timer start register 0	TSTR0	R/W	H'E61E 0004	8
0	Timer constant register 0	TCOR0	R/W	H'E61E 0008	32
	Timer counter 0	TCNT0	R/W	H'E61E 000C	32
	Timer control register 0	TCR0	R/W	H'E61E 0010	16
1	Timer constant register 1	TCOR1	R/W	H'E61E 0014	32
	Timer counter 1	TCNT1	R/W	H'E61E 0018	32
	Timer control register 1	TCR1	R/W	H'E61E 001C	16
2	Timer constant register 2	TCOR2	R/W	H'E61E 0020	32
	Timer counter 2	TCNT2	R/W	H'E61E 0024	32
	Timer control register 2	TCR2	R/W	H'E61E 0028	16
Common to 3 to 5	Timer start register 1	TSTR1	R/W	H'FFF6 0004	8
3	Timer constant register 3	TCOR3	R/W	H'FFF6 0008	32
	Timer counter 3	TCNT3	R/W	H'FFF6 000C	32
	Timer control register 3	TCR3	R/W	H'FFF6 0010	16
4	Timer constant register 4	TCOR4	R/W	H'FFF6 0014	32
	Timer counter 4	TCNT4	R/W	H'FFF6 0018	32
	Timer control register 4	TCR4	R/W	H'FFF6 001C	16
5	Timer constant register 5	TCOR5	R/W	H'FFF6 0020	32
	Timer counter 5	TCNT5	R/W	H'FFF6 0024	32
	Timer control register 5	TCR5	R/W	H'FFF6 0028	16
	Input capture register 5	TCPR5	R	H'FFF6 002C	32
Common to 6 to 8	Timer start register 2	TSTR2	R/W	H'FFF7 0004	8
6	Timer constant register 6	TCOR6	R/W	H'FFF7 0008	32
	Timer counter 6	TCNT6	R/W	H'FFF7 000C	32
	Timer control register 6	TCR6	R/W	H'FFF7 0010	16
7	Timer constant register 7	TCOR7	R/W	H'FFF7 0014	32
	Timer counter 7	TCNT7	R/W	H'FFF7 0018	32
	Timer control register 7	TCR7	R/W	H'FFF7 001C	16
8	Timer constant register 8	TCOR8	R/W	H'FFF7 0020	32
	Timer counter 8	TCNT8	R/W	H'FFF7 0024	32
	Timer control register 8	TCR8	R/W	H'FFF7 0028	16
	Input capture register 8	TCPR8	R	H'FFF7 002C	32
Common to 9 to 11	Timer start register 3	TSTR3	R/W	H'FFF8 0004	8
9	Timer constant register 9	TCOR9	R/W	H'FFF8 0008	32
	Timer counter 9	TCNT9	R/W	H'FFF8 000C	32
	Timer control register 9	TCR9	R/W	H'FFF8 0010	16

Channel	Name	Abbreviation	R/W	Address	Size
10	Timer constant register 10	TCOR10	R/W	H'FFF8 0014	32
	Timer counter 10	TCNT10	R/W	H'FFF8 0018	32
	Timer control register 10	TCR10	R/W	H'FFF8 001C	16
11	Timer constant register 11	TCOR11	R/W	H'FFF8 0020	32
	Timer counter 11	TCNT11	R/W	H'FFF8 0024	32
	Timer control register 11	TCR11	R/W	H'FFF8 0028	16

Table 46.3 Register Configuration (2)

Channel	Name	Abbreviation	Power-On Reset	Module Standby
Common to 0 to 2	Timer start register	TSTR0	H'00	Retained
0	Timer constant register 0	TCOR0	H'FFFF FFFF	Retained
	Timer counter 0	TCNT0	H'FFFF FFFF	Retained
	Timer control register 0	TCR0	H'0000	Retained
1	Timer constant register 1	TCOR1	H'FFFF FFFF	Retained
	Timer counter 1	TCNT1	H'FFFF FFFF	Retained
	Timer control register 1	TCR1	H'0000	Retained
2	Timer constant register 2	TCOR2	H'FFFF FFFF	Retained
	Timer counter 2	TCNT2	H'FFFF FFFF	Retained
	Timer control register 2	TCR2	H'0000	Retained
Common to 3 to 5	Timer start register 1	TSTR1	H'00	Retained
3	Timer constant register 3	TCOR3	H'FFFF FFFF	Retained
	Timer counter 3	TCNT3	H'FFFF FFFF	Retained
	Timer control register 3	TCR3	H'0000	Retained
4	Timer constant register 4	TCOR4	H'FFFF FFFF	Retained
	Timer counter 4	TCNT4	H'FFFF FFFF	Retained
	Timer control register 4	TCR4	H'0000	Retained
5	Timer constant register 5	TCOR5	H'FFFF FFFF	Retained
	Timer counter 5	TCNT5	H'FFFF FFFF	Retained
	Timer control register 5	TCR5	H'0000	Retained
	Input capture register 5	TCPR5	Retained	Retained
Common to 6 to 8	Timer start register 2	TSTR2	H'00	Retained
6	Timer constant register 6	TCOR6	H'FFFF FFFF	Retained
	Timer counter 6	TCNT6	H'FFFF FFFF	Retained
	Timer control register 6	TCR6	H'0000	Retained
7	Timer constant register 7	TCOR7	H'FFFF FFFF	Retained
	Timer counter 7	TCNT7	H'FFFF FFFF	Retained
	Timer control register 7	TCR7	H'0000	Retained
8	Timer constant register 8	TCOR8	H'FFFF FFFF	Retained
	Timer counter 8	TCNT8	H'FFFF FFFF	Retained
	Timer control register 8	TCR8	H'0000	Retained
	Input capture register 8	TCPR8	Retained	Retained
Common to 9 to 11	Timer start register 3	TSTR3	H'00	Retained
9	Timer constant register 9	TCOR9	H'FFFF FFFF	Retained
	Timer counter 9	TCNT9	H'FFFF FFFF	Retained
	Timer control register 9	TCR9	H'0000	Retained
10	Timer constant register 10	TCOR10	H'FFFF FFFF	Retained
	Timer counter 10	TCNT10	H'FFFF FFFF	Retained
	Timer control register 10	TCR10	H'0000	Retained
11	Timer constant register 11	TCOR11	H'FFFF FFFF	Retained
	Timer counter 11	TCNT11	H'FFFF FFFF	Retained
	Timer control register 11	TCR11	H'0000	Retained

46.3.1 Timer Start Registers (TSTRn) (n = 0 to 3)

TSTR are 8-bit readable/writable registers that select whether to run or halt the TCNT.

- (TSTR0)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR2	STR1	STR0
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR2	0	R/W	Counter Start 2 Selects whether to run or halt TCNT2. 0: TCNT2 count halted 1: TCNT2 counts
1	STR1	0	R/W	Counter Start 1 Selects whether to run or halt TCNT1. 0: TCNT1 count halted 1: TCNT1 counts
0	STR0	0	R/W	Counter Start 0 Selects whether to run or halt TCNT0. 0: TCNT0 count halted 1: TCNT0 counts

- (TSTR1)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR5	STR4	STR3
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR5	0	R/W	Counter Start 5 Selects whether to run or halt TCNT5. 0: TCNT5 count halted 1: TCNT5 counts
1	STR4	0	R/W	Counter Start 4 Selects whether to run or halt TCNT4. 0: TCNT4 count halted 1: TCNT4 counts
0	STR3	0	R/W	Counter Start 3 Selects whether to run or halt TCNT3. 0: TCNT3 count halted 1: TCNT3 counts

- (TSTR2)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR8	STR7	STR6
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR8	0	R/W	Counter Start 8 Selects whether to run or halt TCNT8. 0: TCNT8 count halted 1: TCNT8 counts
1	STR7	0	R/W	Counter Start 7 Selects whether to run or halt TCNT7. 0: TCNT7 count halted 1: TCNT7 counts
0	STR6	0	R/W	Counter Start 6 Selects whether to run or halt TCNT6. 0: TCNT6 count halted 1: TCNT6 counts

- (TSTR3)

Bit:	7	6	5	4	3	2	1	0
	—	—	—	—	—	STR11	STR10	STR9
Initial value:	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
7 to 3	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
2	STR11	0	R/W	Counter Start 11 Selects whether to run or halt TCNT11. 0: TCNT11 count halted 1: TCNT11 counts
1	STR10	0	R/W	Counter Start 10 Selects whether to run or halt TCNT10. 0: TCNT10 count halted 1: TCNT10 counts
0	STR9	0	R/W	Counter Start 9 Selects whether to run or halt TCNT9. 0: TCNT9 count halted 1: TCNT9 counts

46.3.2 Timer Constant Registers (TCORn) (n = 0 to 11)

TCOR are 32-bit readable/writable registers. After underflow has been generated according to the result of the TCNT countdown, the value of TCOR is set to TCNT and TCNT continues countdown from the value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	1	R/W	Value constant supply for counter.

46.3.3 Timer Counters (TCNTn) (n = 0 to 11)

TCNT are 32-bit readable/writable registers that count down upon the input clock selected using the bits TPSC2 to TPSC0 in TCR.

When a TCNT countdown results in an underflow, the UNF in TCR of corresponding channel is set. At the same time, the value of TCOR is set to TCNT and TCNT continues countdown from that value.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1	1
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	1	R/W	Timer Counter Down Bits

46.3.4 Timer Control Registers (TCRn) (n = 0 to 11)

TCR are 16-bit readable/writable registers that select a count clock and edge when an external clock is selected, and control an interrupt generation when the flag that indicates the generation of a TCNT is set to 1. TCR of channels 5 and 8 control the input capture function and generation of an interrupt during the input capture.

- TCR0, TCR1, TCR2, TCR3, TCR4, TCR6, TCR7, TCR9, TCR10, TCR11

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	UNF	—	—	UNIE	CKEG		TPSC		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R/W	R	R	R/W	R/W	R/W	R/W	R/W	R/W

- TCR5, TCR8

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	ICPF	UNF	ICPE		UNIE	CKEG		TPSC		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9	ICPF*1	0	R/W	Input Capture Interrupt Flag Status flag, provided in channels 5 and 8 only, which indicates the occurrence of input capture. 0: No input capture has occurred [Clearing condition] When 0 is written to ICPF 1: Input capture has occurred [Setting condition] When an input capture occurs*2
8	UNF	0	R/W	Underflow Flag Status flag which indicates the occurrence of a TCNT underflow. 0: TCNT has not underflow [Clearing condition] When 0 is written to UNF 1: TCNT has underflow [Setting condition] When TCNT underflows*2

Bit	Bit Name	Initial Value	R/W	Description
7, 6	ICPE*[1]	00	R/W	Input Capture Control A function of channels 5 and 8 only: determines whether the input capture function can be used, and when used, whether or not to enable interrupts. Use the CKEG bits to designate use of either the rising or falling edge of the TCLK pin to set the values of TCNT5 and TCNT8 to TCPR5 and TCPR8, respectively. Only when the ICPF bits in TCR5 and TCR8 are 0, the values of TCNT5 and TCNT8 are set to TCPR5 and TCPR8. When the ICPF bit is set to 1, neither TCPR5 nor TCPR8 is set even when input capture is generated. 00: Input capture function is not used. 01: Reserved (setting prohibited) 10: Input capture function is used. Interrupt due to input capture (TICPI5 and TICPI8) is not enabled. 11: Input capture function is used. Interrupt due to input capture (TICPI5 and TICPI8) is enabled.
5	UNIE	0	R/W	Underflow Interrupt Control Controls enabling of interrupt generation when the status flag (UNF) indicating TCNT underflow has been set to 1. 0: Interrupt due to underflow (TUNI) is not enabled 1: Interrupt due to underflow (TUNI) is enabled
4, 3	CKEG	00	R/W	Clock Edge Select an input edge of the external clock when the external clock is selected, or when the input capture function is used. 00: Count/capture register set on rising edge 01: Count/capture register set on falling edge 1X: Count/capture register set on both rising and falling edge
2 to 0	TPSC	000	R/W	Timer Prescaler 2 to 0 Select the TCNT count clock. 000: Count on (input-clock)/4 001: Count on (input-clock)/16 010: Count on (input-clock)/64 011: Count on (input-clock)/256 100: Count on (input-clock)/1024 101: Setting prohibited 110: Setting prohibited 111: Count on external clock (TCLK) (Not usable in channels 0, 1, 2, 9, 10 and 11) Note: Input-clock is CPϕ for channel 0/1/2, and Pϕ for channel 3/4/5/6/7/8/9/10/11.

[Legend]

X: Don't care

Notes: 1. Reserved in channels 0, 1, 2, 3, 4, 6, 7, 9, 10, and 11 (initial value is 0 and read-only).

2. Writing 1 does not change the value.

46.3.5 Input Capture Registers n (TCPRn)

TCPR5 and TCPR8 are read-only 32-bit registers used for the input capture function provided only in channels 5 and 8. The ICPE and CKEG bits in TCR5 and TCR8 control the input capture function. When an input capture occurs, the value of TCNT5 is copied to TCPR5, and the value of TCNT8 is copied to TCPR8. The values of TCNT5 and TCNT8 are set in TCPR5 and TCPR8, respectively, only when the ICPF bits in TCR5 and TCR8 are 0.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	—	R/W	Input capture function (channel 5 and 8)

46.4 Operation

Each channel has a 32-bit timer counter (TCNT) and 32-bit timer constant register (TCOR). TCNT counts down. The auto-reload function enables synchronized counting and external-event counting. Channels 5 and 8 have an input capture function.

46.4.1 Counter Operation

When the bits STR8 to STR0 in TSTR0 to TSTR3 are set to 1, TCNT of corresponding channel starts counting. When TCNT underflows, the UNF flag of corresponding TCR is set. In this case, if the UNIE bit in TCR is set to 1, an interrupt request is sent to the CPU. Also, the value is copied from TCOR to TCNT and the down-count operation is continued (Auto reload function).

(1) Procedure for setting count operation

Figure 46.2 shows an example of the procedure for setting the count operation.

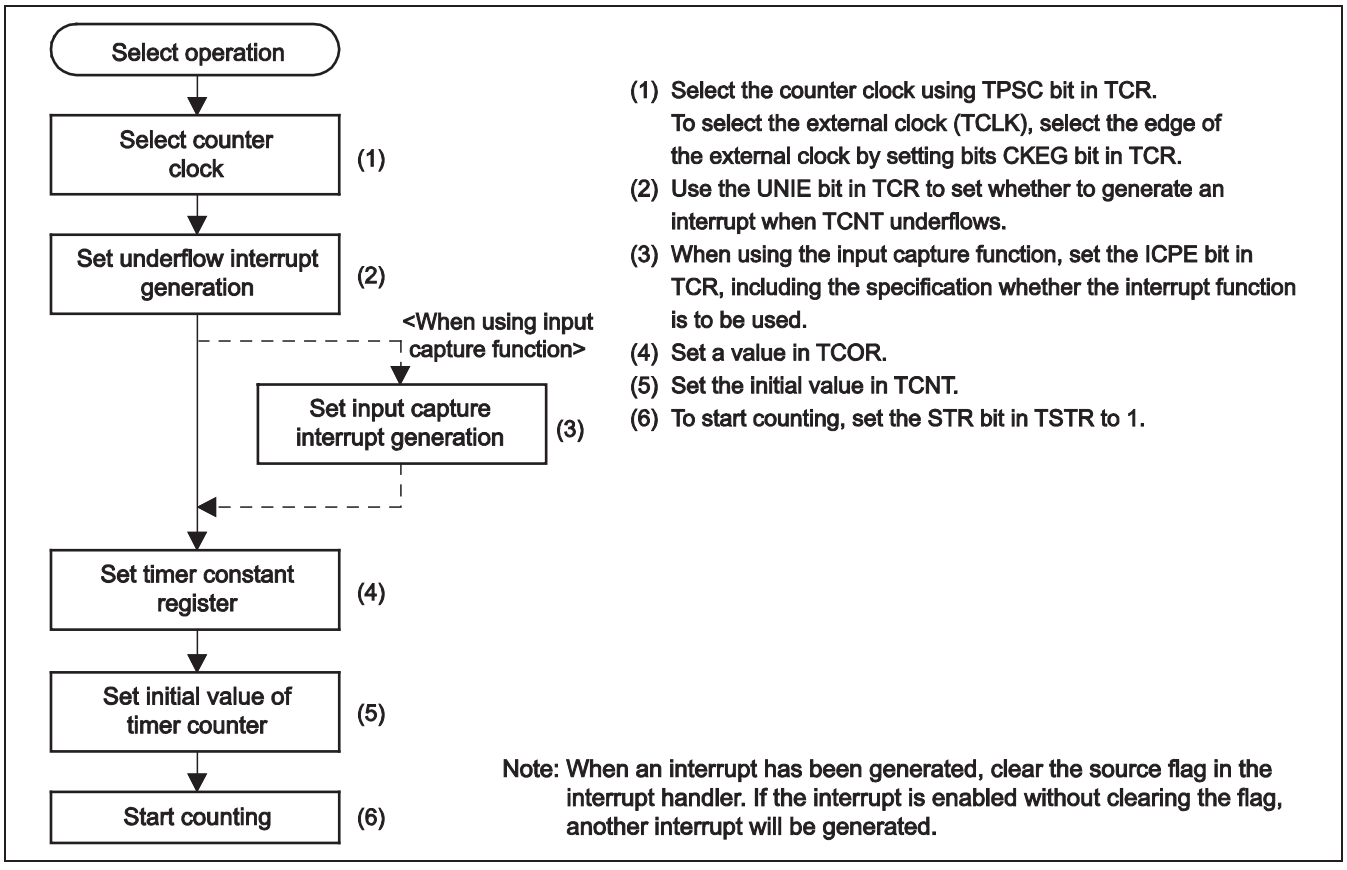


Figure 46.2 Procedure for Setting Count Operation

(2) Auto-reload count operation

Figure 46.3 shows the TCNT auto-reload operation.

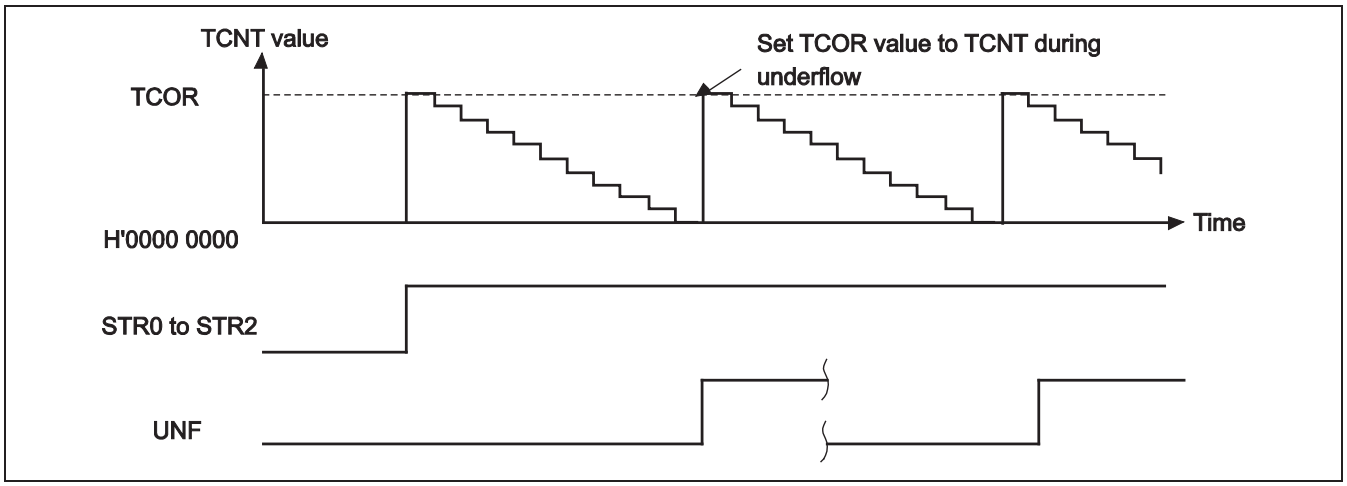


Figure 46.3 TCNT Auto-Reload Operation

(3) TCNT count timing

- Internal clock operation

  Five clocks (Pϕ/4, Pϕ/16, Pϕ/64, Pϕ/256, Pϕ/1024) that are created by dividing peripheral clocks are selected as count clocks by setting bits TPSC2 to TPSC0 in TCR. Figure 46.4 shows the timing.

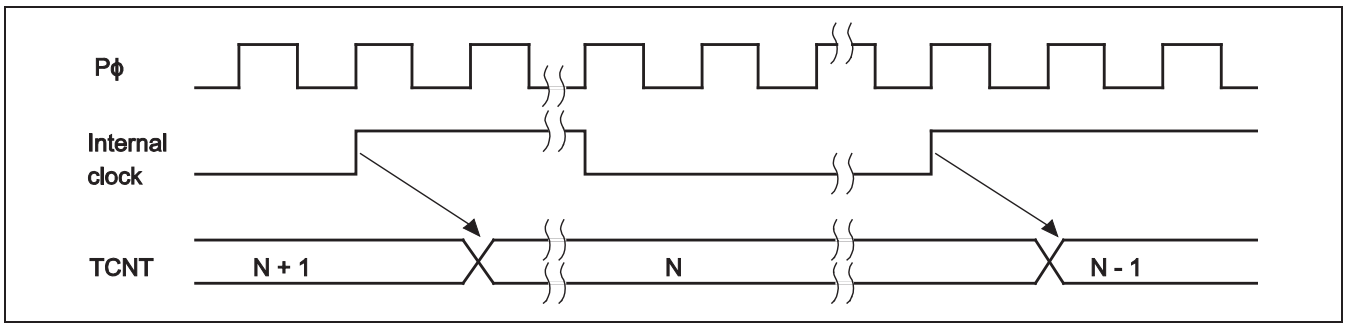


Figure 46.4 Count Timing when Internal Clock is Operating

- External clock operation

  Set the bits TPSC3 to TPSC0 in TCR to select the external clock pin (TCLK) as the timer clock. Use the bits CKEG1 and CKEG0 in TCR to select the detection edge. Rise, fall, or both can be selected.

  Figure 46.5 shows the timing for both-edge detection.

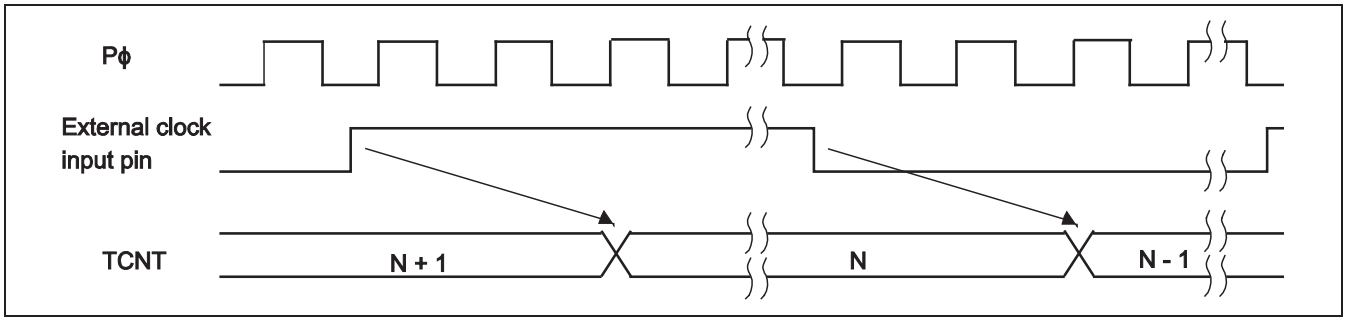


Figure 46.5 Count Timing when External Clock is Operating

46.4.2 Input Capture Function

Channels 5 and 8 have the input capture function. When using the input capture function, follow the procedure shown below.

1. Set the timer operating clock as an internal clock with bits TPSC3 to TPSC0 in TCR.
2. Set use of the input capture function and whether to generate an interrupt on using it with bits ICPE1 and ICPE0 in TCR.
3. Specify either rising edge or falling edge of the TCLK pin to be used to set the value of TCNT to TCPR5 and TCPR8 with bits CKEG1 and CKEG0 in TCR.

Only when an input capture is occurred and the ICPF bits in TCR5 and TCR8 are 0, the values of TCNT5 and TCNT8 are set in TCPR5 and TCPR8, respectively.

Figure 46.6 shows the operating timing when the input capture function is used (the rising edge of TCLK is used).

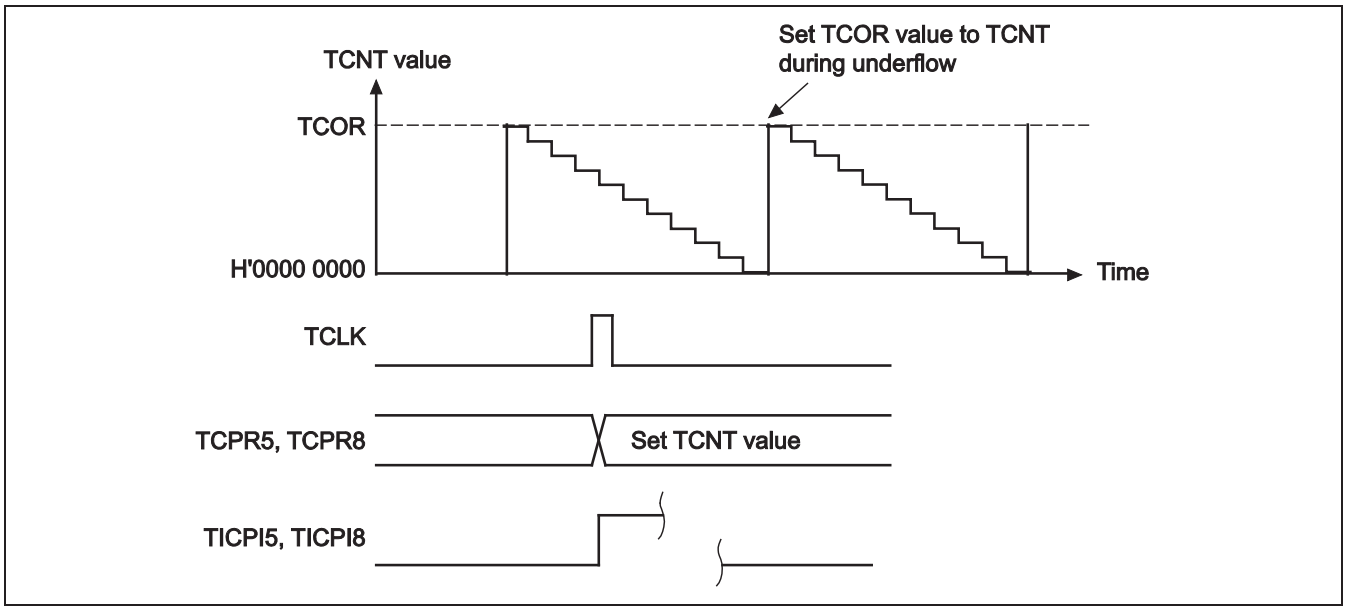


Figure 46.6 Operating Timing when Using Input Capture Function

46.5 Interrupt

The TMU interrupt sources are underflow interrupt or input capture interrupt when the input capture function is used. The underflow interrupt is generated at each channel. The input capture interrupt is generated at channels 5 and 8 only.

An underflow interrupt request is generated (for each channel) when both the UNF bit and the interrupt enable bit for that channel are set to 1.

When the input capture function is used and the input capture request is generated, an interrupt request is generated if the ICPF bit in TCR5 or TCR8 is 1 and the input capture control bits ICPE1 and ICPE0 in TCR5 and TCR8 are 11.

Table 46.4 shows the TMU interrupt sources.

Table 46.4 TMU Interrupt Sources

Channel	Interrupt Sources	Description
0	TUNI0	Underflow interrupt 0
1	TUNI1	Underflow interrupt 1
2	TUNI2	Underflow interrupt 2
3	TUNI3	Underflow interrupt 3
4	TUNI4	Underflow interrupt 4
5	TUNI5	Underflow interrupt 5
	TICPI5	Input capture interrupt 5
6	TUNI6	Underflow interrupt 6
7	TUNI7	Underflow interrupt 7
8	TUNI8	Underflow interrupt 8
	TICPI8	Input capture interrupt 8
9	TUNI9	Underflow interrupt 9
10	TUNI10	Underflow interrupt 10
11	TUNI11	Underflow interrupt 11

46.6 Usage Notes

46.6.1 Writing to Registers

When writing to the TMU registers, clear the start bits (STR11 to STR0) of the corresponding TSTR channel to stop the timer counting.

Writing to TSTR and clearing bits UNF and ICPF in TCR can be executed during counting. To clear flags UNF and ICPF during counting, do not change the values of bits other than those to be cleared.

46.6.2 Reading TCNT Register

Reading from TCNT is performed synchronously with the timer count operation. When timer counting and register read processing are performed simultaneously, the value before TCNT counting down is read.

46.6.3 External Clock Frequency

The frequency of external clock (TCLK) for each channel should be Pϕ/4 or less.

47. PWM Timer

47.1 Overview

This LSI incorporates a seven-channel pulse width modulation (PWM) timer.

47.1.1 Features

- PWM output cycle settable (10 bits)
- PWM output cycle settable within the range from 2 cycles to $2^{24} \times 1024$ cycles of internal bus clock Pϕ (i.e. from 30.77 ns to 264 seconds when Pϕ = 65 MHz)
- High-level width of the PWM output signal settable (10 bits)
- Continuous pulse output or single pulse output selectable

47.1.2 Block Diagram

Figure 47.1 shows a block diagram of the PWM timer.

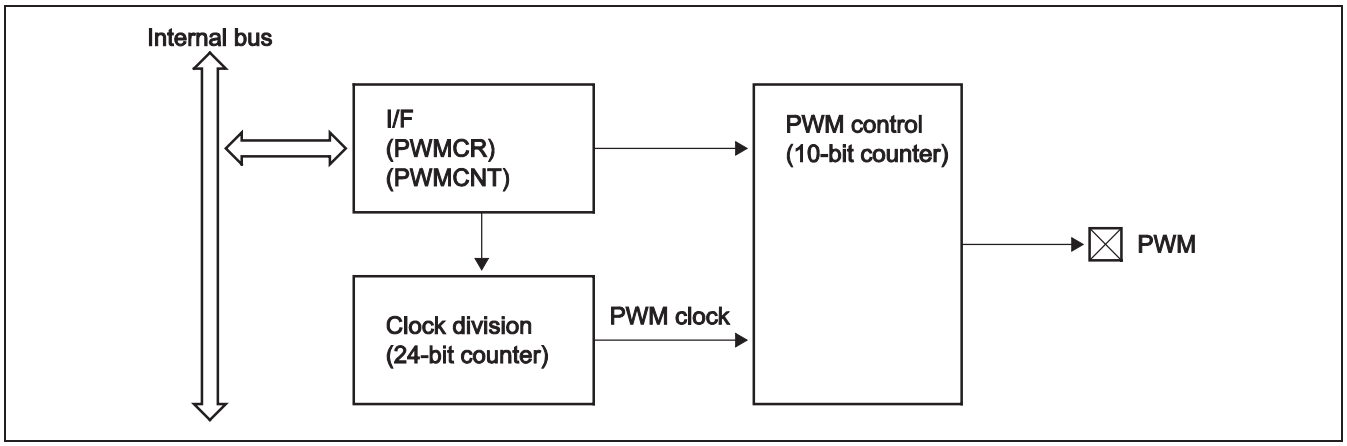


Figure 47.1 Block Diagram of PWM Timer

47.1.3 Input/Output pins

Table 47.1 shows the pin configuration of the PWM timer.

Table 47.1 Pin Configuration

Pin Name	I/O	Function
PWM0	Output	PWM0 timer pulse output
PWM1	Output	PWM1 timer pulse output
PWM2	Output	PWM2 timer pulse output
PWM3	Output	PWM3 timer pulse output
PWM4	Output	PWM4 timer pulse output
PWM5	Output	PWM5 timer pulse output
PWM6	Output	PWM6 timer pulse output

47.1.4 Register Descriptions

Table 47.2 lists the registers of the PWM timer.

Table 47.2 List of Registers

Channel	Name	Abbreviation	R/W	Address	Access Size
0	PWM control register	PWMCR	R/W	H'E6E3 0000	32
	PWM count register	PWMCNT	R/W	H'E6E3 0004	32
1	PWM control register	PWMCR	R/W	H'E6E3 1000	32
	PWM count register	PWMCNT	R/W	H'E6E3 1004	32
2	PWM control register	PWMCR	R/W	H'E6E3 2000	32
	PWM count register	PWMCNT	R/W	H'E6E3 2004	32
3	PWM control register	PWMCR	R/W	H'E6E3 3000	32
	PWM count register	PWMCNT	R/W	H'E6E3 3004	32
4	PWM control register	PWMCR	R/W	H'E6E3 4000	32
	PWM count register	PWMCNT	R/W	H'E6E3 4004	32
5	PWM control register	PWMCR	R/W	H'E6E3 5000	32
	PWM count register	PWMCNT	R/W	H'E6E3 5004	32
6	PWM control register	PWMCR	R/W	H'E6E3 6000	32
	PWM count register	PWMCNT	R/W	H'E6E3 6004	32

Note: Do not access addresses other than those listed above. If access is attempted, a malfunction may occur.

Table 47.3 Register States in Each Operating Mode

Name	Abbreviation	Power-on Reset	Module Standby
PWM control register	PWMCR	H'0000 0000	Retained
PWM count register	PWMCNT	H'0000 0000	Retained

The registers of the PWM timer are mapped into the internal bus address space.

47.2 Register Description

Registers in the PWM timer are allocated to and arranged in the address space of the internal bus.

Legend for Register Description

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

R: Read-only. When the bit is reserved, the write value should always be 0.

—/W: Write-only. The read value is undefined.

47.2.1 PWM Control Register (PWMCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	CC0			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	CCMD	—	—	—	SYNC	—	—	—	—	—	—	SS0	—	—	—	EN0
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R	R	R	R/W	R	R	R	R	R	R	R/W	R	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 20	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
19 to 16	CC0	0000	R/W	Clock Control The clock frequency of the PWM counter is obtained by dividing the frequency of the clock signal Pϕ. When the Pϕ frequency is f MHz, the following PWM clock frequencies are obtained. 0000: f MHz 0001: f MHz/2^2 0010: f MHz/2^4 0011: f MHz/2^6 0100: f MHz/2^8 0101: f MHz/2^{10} 0110: f MHz/2^{12} 0111: f MHz/2^{14} 1000: f MHz/2^{16} 1001: f MHz/2^{18} 1010: f MHz/2^{20} 1011: f MHz/2^{22} 1100: f MHz/2^{24} When 1101, 1110, or 1111 is set, the PWM clock frequency is f MHz/2^{24}.

Bit	Bit Name	Initial Value	R/W	Description
15	CCMD	0	R/W	CC0 Frequency Division Mode Changes the PWM clock frequency set by the clock control (CC0) bits. 0: The PWM clock frequency set by CC0 is used. 1: The PWM clock frequency set by CC0 is changed as follows: 1 - 0000: f MHz/2 1 - 0001: f MHz/2^3 1 - 0010: f MHz/2^5 1 - 0011: f MHz/2^7 1 - 0100: f MHz/2^9 1 - 0101: f MHz/2^{11} 1 - 0110: f MHz/2^{13} 1 - 0111: f MHz/2^{15} 1 - 1000: f MHz/2^{17} 1 - 1001: f MHz/2^{19} 1 - 1010: f MHz/2^{21} 1 - 1011: f MHz/2^{23} If 1100, 1101, 1110, or 1111 is set for CC0, the PWM clock frequency is f MHz/2^{24} irrespective of the CCMD value.
14 to 12	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
11	SYNC	0	R/W	Specifies whether to allow the set values in the PWM count register (PWMCNT) to be reflected in the timer operation synchronously with setting the PWM control register (PWMCR). 0: Allows the PWMCNT set values to be reflected in the timer operation irrespective of PWMCR setting. 1: Allows the PWMCNT set values to be reflected in the timer operation synchronously with PWMCR setting. For details, refer to section 47.3, Description of Operation.
10 to 5	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
4	SS0	0	R/W	Single Pulse Output 0: The timer operates in continuous pulse output mode. 1: The timer operates only for a single cycle and then stops.
3 to 1	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
0	EN0	0	R/W	Channel Enable 0: The channel is held in the idle state, and outputs a high level. 1: The channel outputs high and low levels in a predetermined cycle. This bit is automatically cleared in single pulse output mode.

47.2.2 PWM Count Register (PWMCNT)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	CYC0									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	PH0									
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 26	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
25 to 16	CYC0	H’000	R/W	PWM Cycle Sets the PWM output cycle. The cycle set by these bits is the sum of the high-level and low-level periods. Setting H'000 is prohibited.
15 to 10	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
9 to 0	PH0	H’000	R/W	PWM High-Level Period Sets the period for which the PWM timer outputs a high-level signal. Setting H'000 is prohibited.

Note: For the CYC0 and PH0 bits, set the number of cycles to be counted of the PWM clock signal whose frequency has been set by the CC0 and CCMD bits in the PWM control register.

47.3 Description of Operation

The duty ratio of a PWM output pulse can be obtained by setting a high-level period and a cycle. The timer channel counts the PWM clock signal pulses using a 10-bit counter to generate the PWM output pulse having the specified period and cycle. When the channel function is enabled (EN0 = 1), the timer outputs a high level until the counter value reaches the value set in the PH0 bits of the PWM count register (PWMCNT). The output goes low when the PH0 value is reached, and is held low until the counter value reaches the value set in the CYC0 bits of PWMCNT. When the CYC0 value is reached, the output goes high and the counter is reset.

Unless the channel function is enabled, the output is held high, and the counter is held in the reset state.

Figure 47.2 shows the PWM state transition during the operation described above.

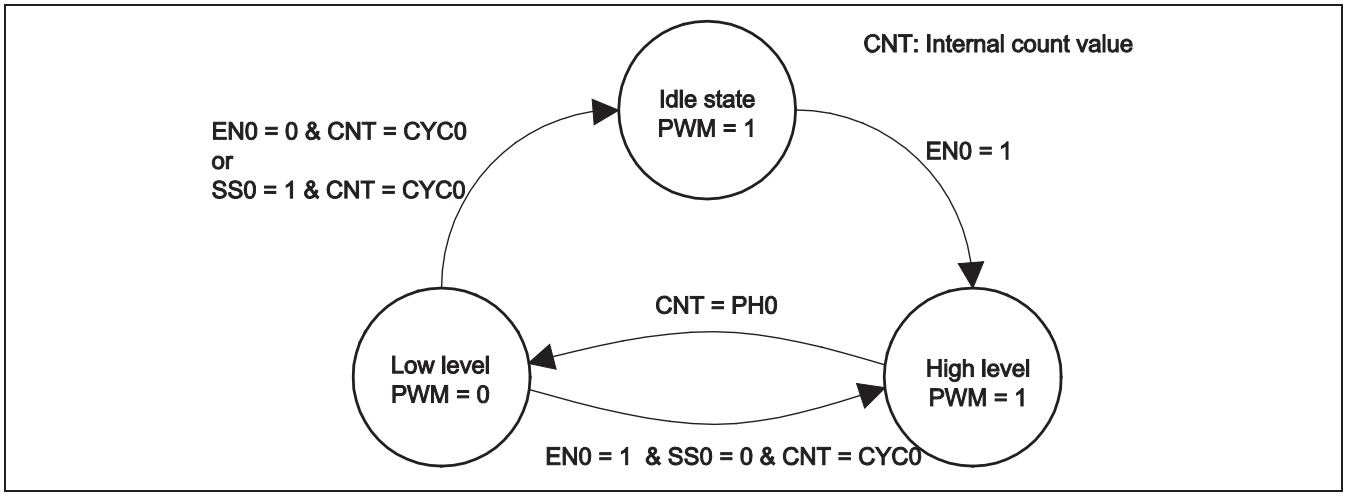


Figure 47.2 PWM Timer State Transition

Note that after a channel has been enabled by writing 1 to EN0, the number of clock pulses before output of the first falling edge from a channel is greater than the value set in the PWM control register and PWM count register by up to four cycles of the Pϕ clock. After that, the PWM output rises and falls according to a set timing.
Figure 47.3 schematically shows this output timing. This figure shows an internal operation.

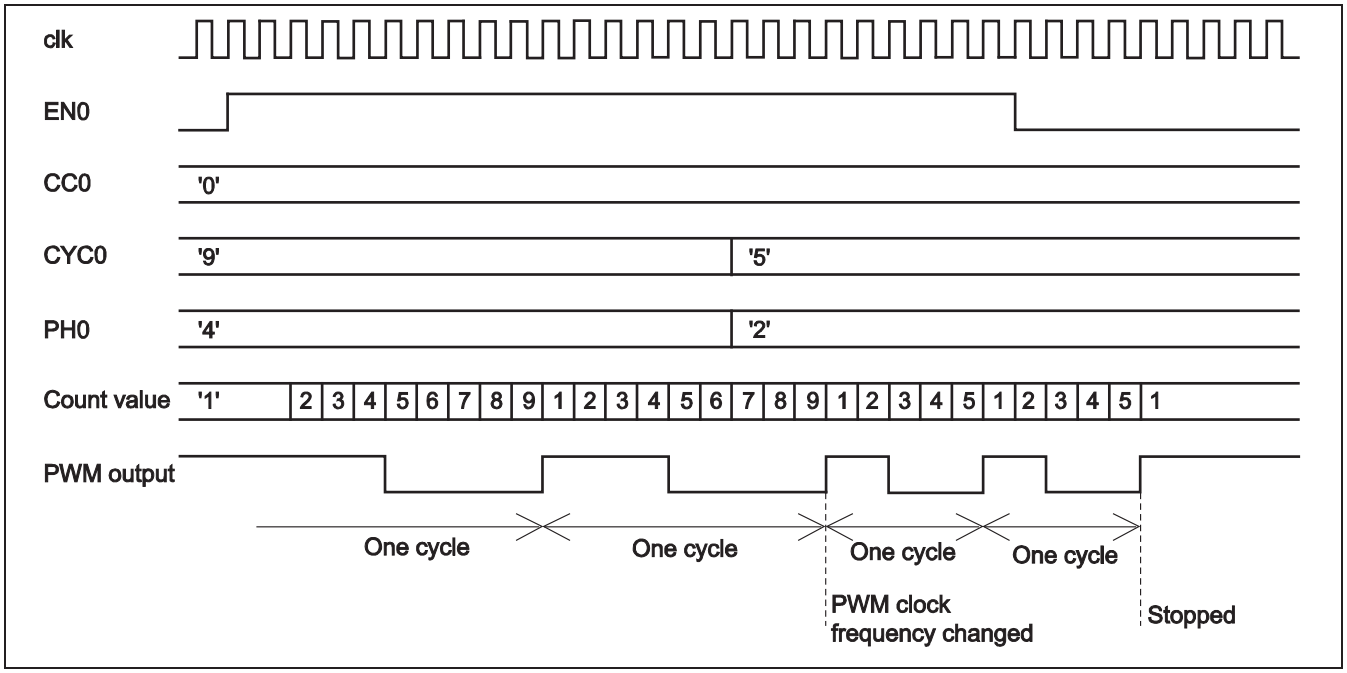


Figure 47.3 PWM Output Timing

1. The period from enabling the channel to the first falling edge output from the channel is the sum of a set value and up to four cycles of the Pϕ clock.
2. After that, the PWM high and low widths are the same as the set values.
3. When the PWM count register is changed during operation (EN0 = 1), timing of the output will be in accord with the new settings after output of the current cycle has been completed.
4. When the CC0 and CCMD bit values in the PWM control register are changed during operation (EN0 = 1), timing of the output will be in accord with the new settings after output of the current cycle has been completed.
5. To stop the timer operation, write 0 to the EN0 bit. The timer stops operation after completing the output of the current cycle. Note that, however, if 1 is written to EN0 again before completing the output of the current cycle, the timer does not stop but continues to operate.
6. For the PWM timer output, continuous pulse output mode and single pulse output mode are supported. In continuous pulse output mode, the timer outputs pulses continuously while EN0 is 1. In single pulse output mode, the timer outputs a single pulse. In this mode, EN0 is automatically cleared.
7. To change the values of the clock control bits (CC0) and the CC0 frequency division mode bit (CCMD) in the PWMCR register and of the PWM cycle bits (CYC0) and the PWM high-level period bits (PH0) in the PWMCNT register at the same time during the PWM operation, the following procedure should be followed:
   1. Write 1 to the SYNC bit. (Write the original set values to the other bits in PWMCR.)
   2. Change the PWMCNT value.
   3. Change the CC0 and CCMD values in PWMCR. (Write the original set values to the other bits in PWMCR. The SYNC bit should be held at 1.)

   By following the above procedure, the new PWMCNT value is reflected in the timer operation synchronously with PWMCR setting.
   When changing only the PWMCNT value while SYNC = 1, writing to PWMCR is required after changing the PWMCNT value. In this case, write the same values as the original set values to the PWMCR bits. On the other hand, when changing only the PWMCR value, writing to PWMCNT is not required.
   If PWMCNT and PWMCR values are changed while SYNC = 0, the change to the values might not be completed within a single PWM output cycle but actually take two or more cycles. This may disturb the period or duty cycle of the PWM output.
   Note that, when the PWCNT value is changed while SYNC = 1, the new values are read from PWMCNT even before PWMCR is set.

47.4 Usage Note

When using the PWM timer, note the following points.

When the CYC0 value is equal to or smaller than PH0 value in the PWM count register, the PWM output is held high. In this case, to start pulse output, clear EN0 to 0, set CYC0 to the value greater than the PH0 value, and then set EN0 to 1.

Note that, a maximum period equivalent to CYC0 = H'3FF at the set PWM clock frequency may be required before pulse output is started.

48. IR Receiver (IR)

48.1 Overview

This LSI incorporates an IR receiver (IR). The internal bus clock used in this module is 65 MHz.

48.1.1 Features

The IR receiver has the following features:

- Receiver block
  - Automatic leader code detection
  - Synchronization protection (prevention of malfunction caused by noise) circuit incorporated during leader code detection
  - Up to 64 bits of code per frame receivable
  - Up to 2 frame of code receivable

48.1.2 Block Diagram

A block diagram of the IR receiver is shown in Figure 48.1.

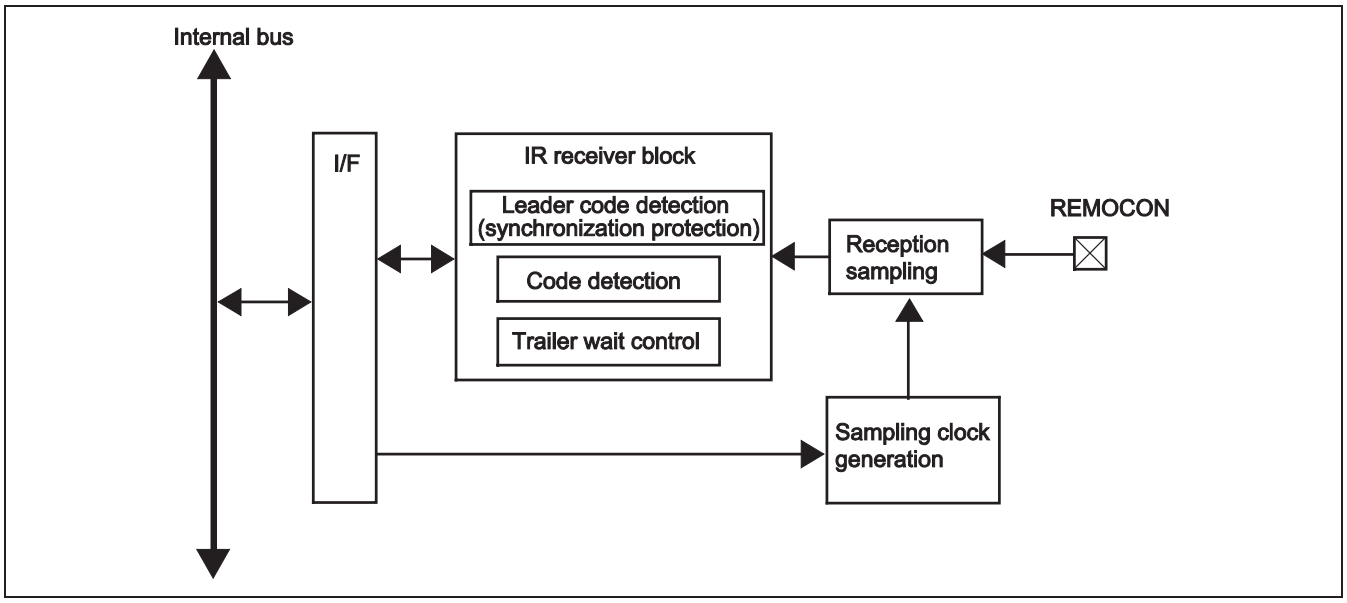


Figure 48.1 Block Diagram of IR Receiver

48.1.3 Input/Output Pins

Table 48.1 shows the pin configuration of the IR receiver.

Table 48.1 Pin Configuration

Pin Name	Function	I/O	Description
REMOCON	IR input data pin	Input	IR receive data input pin

48.1.4 Register Configuration

Table 48.2 shows the register configuration of the IR receiver. The registers of the IR receiver are mapped into the internal bus address space.

Do not write to any addresses other than listed below. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed below are undefined.

Table 48.2 Register Configuration

Register Name	Abbreviation	R/W	Value after Reset*1	Address	Access Size
IR mode register	IRMODE	R/W	H'0000 0000	H'E6E5 0000	32
IR command register	IRCOMM	R/W	H'0000 0000	H'E6E5 0004	32
IR status register	IRST	R/(W)*2	H'0000 0000	H'E6E5 0008	32
clkp division ratio	CPD	R/W	H'0000 00FA	H'E6E5 000C	32
Leader high period (upper and lower limits) register	LDHL	R/W	H'080C 0564	H'E6E5 0010	32
Leader low period (upper and lower limits) register	LDLL	R/W	H'0370 0320	H'E6E5 0014	32
"0" bit period (upper and lower limits) register	BS0L	R/W	H'00F6 00B6	H'E6E5 0018	32
"1" bit period (upper and lower limits) register	BS1L	R/W	H'01EA 016A	H'E6E5 001C	32
"0" or "1" bit high period (upper and lower limits) register	BSHL	R/W	H'00AA 0036	H'E6E5 0020	32
Trailer wait time register	TWP	R/W	H'0000 1450	H'E6E5 0024	32
Receive frame total bit number register	RNOFBS	R/W	H'0000 3820	H'E6E5 0028	32
Receive code register 1-1	RCODE11	R	H'0000 0000	H'E6E5 002C	32
Receive code register 1-2	RCODE12	R	H'0000 0000	H'E6E5 0030	32
Receive code register 2-1	RCODE21	R	H'0000 0000	H'E6E5 0034	32
Receive code register 2-2	RCODE22	R	H'0000 0000	H'E6E5 0038	32

Notes: 1. The value is initialized by a reset.
2. Only 0 can be written to bits 7 and 6, to clear flags.

48.2 Register Descriptions

The registers of the IR receiver are mapped into the internal bus address space.

Legend for Register Description

Initial value: Register value after a reset.

—: Undefined value

R/W: Readable/writable. The written value can be read.

R/WC0: Readable/writable. Writing 0 initializes the bit. Writing 1 is ignored.

R/WC1: Readable/writable. Writing 1 initializes the bit. Writing 0 is ignored.

R: Read-only. The write value should always be 0.

—/W: Write-only. The read value is undefined.

48.2.1 IR Mode Register (IRMODE)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RCDENDE	RFRENDE	RBUFM	INVERT	RMODE			RECON
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
7	RCDENDE	0	R/W	Receive Code End Interrupt Enable 0: Disables the RCDEND interrupt request. 1: Enables the RCDEND interrupt request.
6	RFRENDE	0	R/W	Receive Frame End Interrupt Enable 0: Disables the RFREND interrupt request. 1: Enables the RFREND interrupt request.
5	RBUFM	0	R/W	Receive Register Mode 0: Double buffer mode. Receive data is written to the RCODE11-RCODE12 registers and the RCODE21-RCODE22 registers. 1: Single buffer mode. Receive data is written to only the RCODE11-RCODE12 registers.
4	INVERT	0	R/W	Receive Signal Polarity Inversion 0: An inverted signal is being input to the REMOCON input pin. 1: A non-inverted signal is being input to the REMOCON input pin.
3 to 1	RMODE	000	R/W	Receive Operating Mode Specifies the operating mode of the IR receiver. 000: Leader code is included. 001: Leader code is not included. 010 to 111: Reserved
0	RECON	0	R/W	IR Receiver Start Setting this bit to 1 starts a receive operation. This bit should be set after all the registers have been set. When this bit is set to 0, the internal IR state and registers RCODE 11/12/21/22 are initialized; other registers are not initialized.

48.2.2 IR Command Register (IRCOMM)

The IR receiver supports error detection for the remote control format in which one frame is composed of four bytes of data (32 bits): the compo code byte following the leader, the inverse of the compo code, an instruction code byte, and its inverse, in that order.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	XCM								ARC			—	ICC	—	—	RCDM
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R	R	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
15 to 8	XCM	H'00	R/W	Specified Compo Code Specifies the reference compo code to be compared with the compo code of receive data. If the comparison result does not satisfy the condition specified by the ARC (Acknowledge Receive Code) bits, data is not written to the RCODE11-RCODE12 and RCODE21-RCODE22 registers.
7 to 5	ARC	000	R/W	Acknowledge Receive Code Data is identified as receive data and is written to the RCODE11-RCODE12 and RCODE21-RCODE22 registers only if the condition specified by the ARC and ICC (Instruction/Compo Code Check) bits is satisfied. In this case, an interrupt is generated. 000: Any compo code 001: The lower four bits of the compo code and of the XCM field match. 010: The upper four bits of the compo code and of the XCM field match. 011: The compo code matches the XCM field. 101: The lower four bits of the compo code and of the XCM field do not match. 110: The upper four bits of the compo code and of the XCM field do not match. 111: The compo code does not match the XCM field.
4	—	0	R	Reserved The read value is always 0. The write value should always be 0.
3	ICC	0	R/W	Instruction/Compo Code Check Data is identified as receive data and is written to the RCODE11-RCODE12 and RCODE21-RCODE22 registers only if the condition specified by the ARC and ICC bit is satisfied. In this case, an interrupt is generated. 0: Any compo code and instruction code 1: The compo code matches its inverted code, and the instruction code matches its inverted code.

Bit	Bit Name	Initial Value	R/W	Description
2, 1	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
0	RCDM	0	R/W	Receive Code Buffer Mode 0: Receive data is stored in the RCODE11 or RCODE21 register in the order of Rn[8]→Rn[15], Rn[24]→Rn[31], Rn[0]→Rn[7], and Rn[16]→Rn[23], and in the RCODE12 or RCODE22 register in the order of Rn[40]→Rn[47], Rn[56]→Rn[63], Rn[32]→Rn[39], and Rn[48]→Rn[55]. 1: Receive data is stored in the RCODE11-RCODE12 or RCODE21-RCODE22 registers in the order from Rn[0] to Rn[63].

48.2.3 IR Status Register (IRST)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RCDEND	RFREND	—	—	—	—	—	RSEL12
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R/WC0	R/WC0	R	R	R	R	R	R

Note: Only 0 can be written to bits 7 and 6, to clear flags.

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
7	RCDEND	0	R/WC0	Frame Receive Code End Status This bit is set to 1 when a frame of bitstream data (not including a trailer) that includes the compo and instruction codes satisfying the ARC and ICC conditions has been completely received. This bit is cleared by writing 0 to it. This bit is set by hardware, and cannot be set by writing 1 to it.
6	RFREND	0	R/WC0	Frame Receive End Status This bit is set to 1 when a frame of bitstream data (including trailer) that includes the compo and instruction codes satisfying the ARC and ICC conditions has been completely received. This bit is cleared by writing "0" to it. This bit is set by hardware, and cannot be set by writing "1" to it.
5 to 1	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
0	RSEL12	0	R	Receive Code Buffer Specification Status 0: The next receive data will be stored in the RCODE11 and RCODE12 registers. 1: The next receive data will be stored in the RCODE21 and RCODE22 registers. Note that this bit is set to 0 by hardware at a reset or when the RECON bit is cleared to 0 (when the IR receiver is stopped). The bit value changes when all the codes in a frame have been received. When the RBUFM bit is 1, this bit is fixed to 0. The write value should be 0.

48.2.4 clkp Division Ratio Register (CPD)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	CPD												
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	1	0	1	0
R/W:	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 13	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
12 to 0	CPD	H'00FA	R/W	clkp Division Ratio Sets the division ratio for generating a sampling clock for IR input signal. If the clock clkp is 65 MHz and the CPD bits are set to 325 (decimal number), the sampling clock period is 5 μs (325/65M); the IR receiver samples the input signal to determine the input level (0 or 1) at this sampling rate. These bits are initialized to H'00FA (250 in decimal number) at power-on reset.

48.2.5 Leader High Period (Upper and Lower Limits) Register (LDHL)

LDHL specifies the high period of a leader. Consecutive high-level detection period specified by the TN and DN bits in the receive frame total bit number register (RNOFBS) is not included in the leader high period specified in this register.

The values to be set in LDHL are the ratios of the leader high period to the sampling clock period generated according to the value specified by the clkp division ratio register (CPD).

LDHU and LDHL define the allowable upper and lower limits of the leader high period, respectively. For example, if the frequency of the clock clkp is 65 MHz, leader high period is 8.6 ms, the value of the CPD bits is decimal 325, and the allowable limits of the leader high period is from 6.9 ms to 10.3 ms, the values in registers LDHU and LDHL are 2060 (10.3 ms/5 µs) and 1380 (6.9 ms/5 µs), respectively.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	LDHU											
Initial value:	0	0	0	0	1	0	0	0	0	0	0	0	1	1	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LDHL											
Initial value:	0	0	0	0	0	1	0	1	0	1	1	0	0	1	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
27 to 16	LDHU	H'80C	R/W	Leader High Period Upper Limit Sets the allowable upper limit of the leader high period.
15 to 12	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
11 to 0	LDHL	H'564	R/W	Leader High Period Lower Limit Sets the allowable lower limit of the leader high period.

48.2.6 Leader Low Period (Upper and Lower Limits) Register (LDLL)

LDLL specifies the low period of a leader. Continuous low-level detection period specified by the TN and DN bits in the receive frame total bit number register (RNOFBS) is not included in the leader low period specified in this register.

The values to be set in LDLL are the ratios of the leader low period to the sampling clock period specified by the clkp division ratio register (CPD).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	LDLU											
Initial value:	0	0	0	0	0	0	1	1	0	1	1	1	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	LDLL											
Initial value:	0	0	0	0	0	0	1	1	0	0	1	0	0	0	0	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
27 to 16	LDLU	H'370	R/W	Leader Low Period Upper Limit Sets the allowable upper limit of leader low period.
15 to 12	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
11 to 0	LDLL	H'320	R/W	Leader Low Period Lower Limit Sets the allowable lower limit of leader low period.

48.2.7 "0" Bit Period (Upper and Lower Limits) Register (BS0L)

BS0L specifies the "0" bit period.

The values to be set in BS0L are the ratios of the "0" bit period to the sampling clock period specified by the clkp division ratio register (CPD).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BS0U											
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	1	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BS0L											
Initial value:	0	0	0	0	0	0	0	0	1	0	1	1	0	1	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
27 to 16	BS0U	H'0F6	R/W	"0" Bit Period Upper Limit Sets the allowable upper limit of the "0" bit period.
15 to 12	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
11 to 0	BS0L	H'0B6	R/W	"0" Bit Period Lower Limit Sets the allowable lower limit of the "0" bit period.

48.2.8 "1" Bit Period (Upper and Lower Limits) Register (BS1L)

BS1L specifies the "1" bit period.

The values to be set in BS1L are the ratios of the "1" bit period to the sampling clock period specified by the clkp division ratio register (CPD).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BS1U											
Initial value:	0	0	0	0	0	0	0	1	1	1	1	0	1	0	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BS1L											
Initial value:	0	0	0	0	0	0	0	1	0	1	1	0	1	0	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
27 to 16	BS1U	H'1EA	R/W	"1" Bit Period Upper Limit Sets the allowable upper limit of the "1" bit period.
15 to 12	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
11 to 0	BS1L	H'16A	R/W	"1" Bit Period Lower Limit Sets the allowable lower limit of the "1" bit period.

48.2.9 "0" or "1" Bit High Period (Upper and Lower Limits) Register (BSHL)

BSHL specifies the high period of the "0" or "1" bit.

The values to be set in BSHL are the ratios of the high period to the sampling clock period specified by the clkp division ratio register (CPD).

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	BSHU											
Initial value:	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	BSHL											
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	0	1	1	0
R/W:	R	R	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 28	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
27 to 16	BSHU	H'0AA	R/W	"0" or "1" Bit High Period Upper Limit Sets the allowable upper limit of the high period of the "0" or "1" bit.
15 to 12	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
11 to 0	BSHL	H'036	R/W	"0" or "1" Bit High Period Lower Limit Sets the allowable lower limit of the high period of the "0" or "1" bit.

48.2.10 Trailer Wait Time Register (TWP)

TWP sets the wait time in a trailer.

The bit value is the ratio of the wait period to the sampling clock period specified by the clkp division ratio register (CPD).

After the time specified by this register has been elapsed, the IR receiver returns to the initial state and goes to the mode of detecting the next edge of the signal.

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	TWP															
Initial value:	0	0	0	1	0	1	0	0	0	1	0	1	0	0	0	0
R/W:	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 16	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
15 to 0	TWP	H'1450	R/W	Trailer Wait Time Sets the wait time in a trailer.

48.2.11 Receive Frame Total Bit Number Register (RNOFBS)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	TN			DN			—	RNOFBS						
Initial value:	0	0	1	1	1	0	0	0	0	0	1	0	0	0	0	0
R/W:	R	R	R/W	R/W	R/W	R/W	R/W	R/W	R	R/W	R/W	R/W	R/W	R/W	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 14	—	All 0	R	Reserved The read value is always 0. The write value should always be 0.
13 to 11	TN	111	R/W	Specifies the maximum number of times the receiver should attempt to receive a low- or high-level signal at the reception sampling frequency during leader code reception. (For details, refer to section 48.3, Description of Operation.) 000: Three times 001: Four times ….. 111: Ten times Set the value equal to or greater than that set in the DN bits.
10 to 8	DN	000	R/W	Specifies the number of times the receiver should detect a low- or high-level signal consecutively to determine the pulse level (low or high) during leader code reception. (For details, refer to section 48.3, Description of Operation.) 000: Three times 001: Four times ….. 111: Ten times Set the value equal to or smaller than that set in the TN bits.
7	—	0	R	Reserved The read value is always 0. The write value should always be 0.
6 to 0	RNOFBS	H'20	R/W	Sets the total number of bits in a frame. Set a value according to the format of the signal input to the IR receiver. The maximum settable value is H'40.

48.2.12 Receive Code Register 1-1 (RCODE11)

RCODE11 is a register in which receive codes are stored.

Error detection is supported for the 32-bit format with a compo code. For details, refer to section 48.2.2, IR Command Register (IRCOMM).

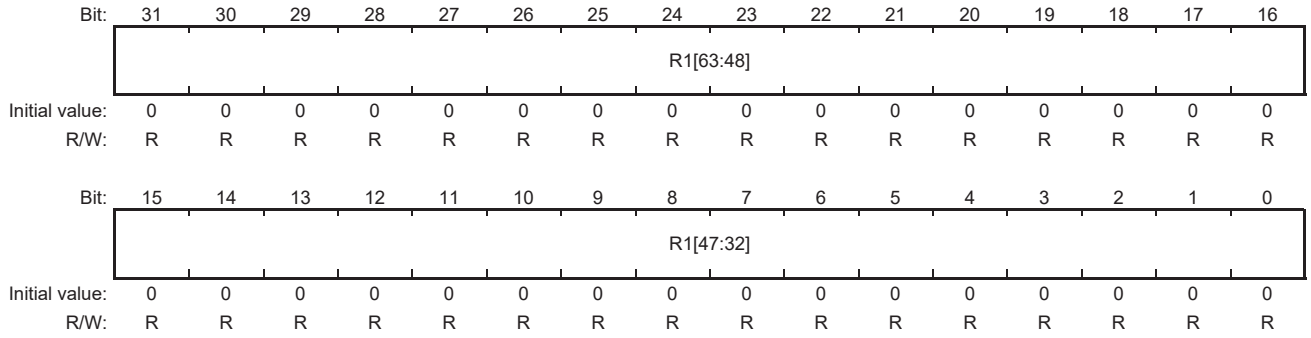
Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	R1[31:16]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	R1[15:0]															
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	R1[31:0]	H'0000 0000	R	Receive Code This register is not overwritten until it is read. RCDM = 1: Data is written in the received order to bits R1[0]→R1[31]. RCDM = 0: Data is written in the received order to bits R1[8]→R1[15], R1[24]→R1[31], R1[0]→R1[7], and then R1[16]→R1[23]. Data is written to RCODE11 and RCODE12, in that order. (Before receiving data, storing order and the total number of bits in a frame should be set in the RCDM and RNOFBS bits, respectively.)

48.2.13 Receive Code Register 1-2 (RCODE12)

RCODE12 is a register in which receive codes are stored.

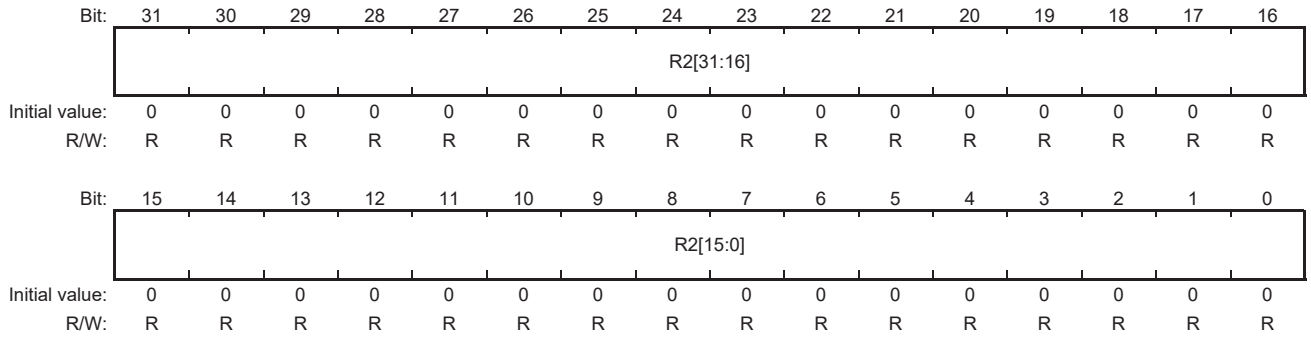


Bit	Bit Name	Initial Value	R/W	Description
31 to 0	R1[63:32]	H'0000 0000	R	Receive Code This register is not overwritten until the receive code register 1-1 (RCODE11) is read. RCDM = 1: Data is written in the received order to bits R1[32]→R1[63]. RCDM = 0: Data is written in the received order to bits R1[40]→R1[47], R1[56]→R1[63], R1[32]→R1[39], and then R1[48]→R1[55]. Data is written to RCODE11 and RCODE12, in that order. (Before receiving data, storing order and the total number of bits in a frame should be set in the RCDM and RNOFBS bits, respectively.)

48.2.14 Receive Code Register 2-1 (RCODE21)

RCODE21 is a register in which receive codes are stored.

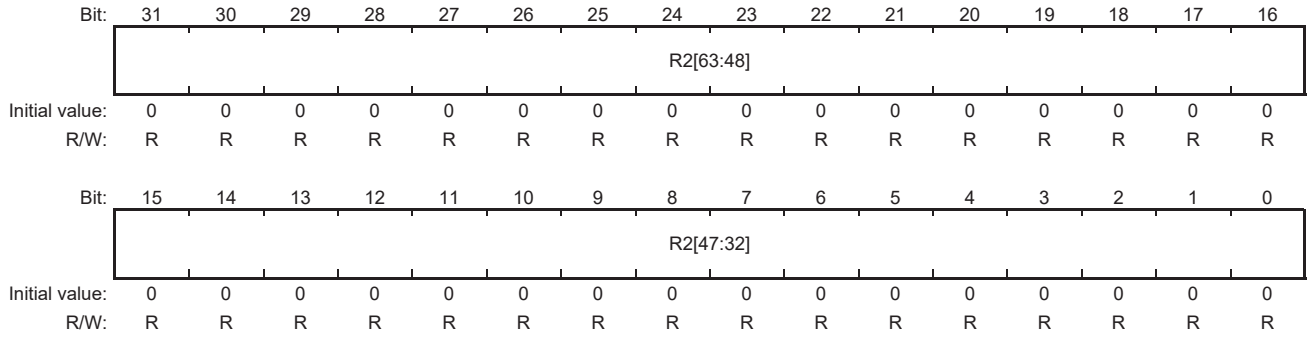
Error detection is supported for the 32-bit format with a compo code. For details, refer to section 48.2.2, IR Command Register (IRCOMM).



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	R2[31:0]	H'0000 0000	R	Receive Code This register is not overwritten until it is read. RCDM = 1: Data is written in the received order to bits R2[0]→R2[31]. RCDM = 0: Data is written in the received order to bits R2[8]→R2[15], R2[24]→R2[31], R2[0]→R2[7], and then R2[16]→R2[23]. Data is written to RCODE21 and RCODE22, in that order. (Before receiving data, storing order and the total number of bits in a frame should be set in the RCDM and RNOFBS bits, respectively.)

48.2.15 Receive Code Register 2-2 (RCODE22)

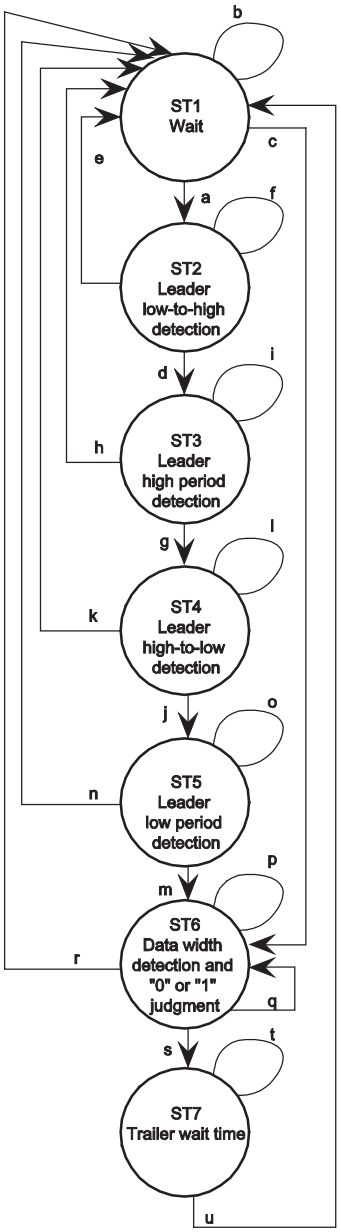
RCODE22 is a register in which receive codes are stored.



Bit	Bit Name	Initial Value	R/W	Description
31 to 0	R2[63:32]	H'00000000	R	Receive Code This register is not overwritten until the receive code register 2-1 (RCODE21) is read. RCDM = 1: Data is written in the received order to bits R2[32]→R2[63]. RCDM = 0: Data is written in the received order to bits R2[40]→R2[47], R2[56]→R2[63], R2[32]→R2[39], and then R2[48]→R2[55]. Data is written to RCODE21 and RCODE22, in that order. (Before receiving data, storing order and the total number of bits in a frame should be set in the RCDM and RNOFBS bits, respectively.)

48.3 Description of Operation

48.3.1 Overview of IR Receiver Operation



ST1: Wait
The global counter, sampling period counter (1), sampling period counter (2), and rising edge counter (3) are all reset.
a. In the case of RECON = 1, high level detection, and the data format including a leader code.
b. High level detection wait state
c. In the case of RECON = 1, high level detection, and the data format not including a leader code.

ST2: Leader low-to-high detection
The sampling period counter (1) is started. A maximum of TN times of attempts are made to detect a high level DN times consecutively. The global counter is started.
d. A high level is detected DN times consecutively.
e. TN times of attempts are made but failed, or a timeout*1 occurs.
f. Attempting is in progress.

ST3: Leader high period detection
The sampling period counter (2) is started. The counter is incremented each time a high level is detected. When a falling edge is detected, the counter value is compared with the LDHL register value. The sampling period counter (1) is reset.
g. The high period of a leader code is within the range between LDHU and LDHL.
h. The high period of a leader code is out of the range between LDHU and LDHL, or a timeout*1 occurs.
i. High level counting is in progress.

ST4: Leader high-to-low detection
The sampling period counter (1) is started. DN consecutive times of low-level detection are tried a maximum of TN times. The sampling period counter (2) is reset.
j. A low level is detected DN times consecutively.
k. TN times of attempts are made but failed, or a timeout*1 occurs.
l. Attempting is in progress.

ST5: Leader low period detection
The sampling period counter (2) is started. The counter is incremented each time a low level is detected. When a rising edge is detected, the counter value is compared with the LDLL register value. The sampling period counter (1) is reset.
m. The low period of a leader code is within the range between LDLU and LDLL.
n. The low period of a leader code is out of the range between LDLU and LDLL, or a timeout*1 occurs.
o. Low level counting is in progress.

ST6: Data width detection and "0" or "1" judgment
The sampling period counter (2) is reset and then started, and is incremented until a rising edge is detected. The counter value at the detection of the falling edge is compared with the BSHL register value, and the counter value at the detection of the following rising edge is compared with the BS0L and BS1L register values. The bit is judged as "0", "1", or "other than 0 and 1" according to the result of these comparisons.
The rising edge counter (3) is incremented each time a rising edge is detected.
p. A rising edge has not been detected.
q. A bit is judged as "0" or "1", and the value of the rising edge counter (3) is smaller than the number of bits specified by RNOFBS.
r. A bit is judged as "other than 0 and 1", or a timeout*1 occurs.
s. A bit is judged as "0" or "1", and the value of the rising edge counter (3) has reached the number of bits specified by RNOFBS.
When the compo code bits and instruction code bits satisfy the conditions specified by the ARC and ICC bits, the data is set in the receive code registers, and the receive code end interrupt is generated.

ST7: Trailer wait time
The sampling period counter (1) is started. The sampling period counter (2) and the rising edge counter (3) are reset.
t. The counter value has not reached the value specified by TWP.
u. The counter value has reached the value specified by TWP. The receive frame end interrupt is generated.

Notes: 1. A timeout occurs when the following time has elapsed after the start of the global counter.
36096 × sampling period
2. The receiver is returned to ST1 by a reset or clearing RECON to 0.

Figure 48.2 Operation Flow of IR Receiver

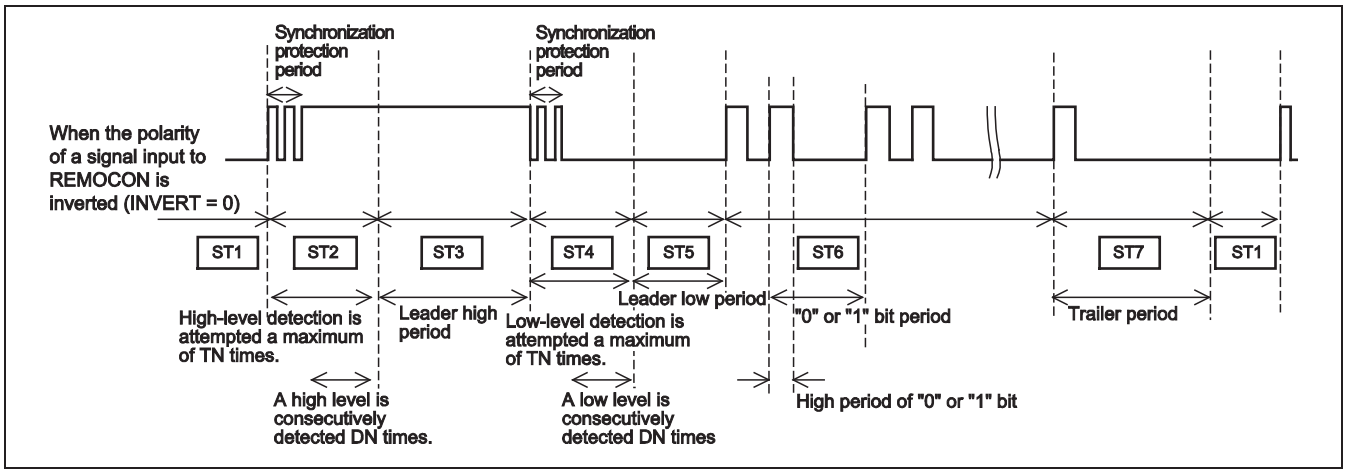


Figure 48.3 Operation Flow of IR Receiver (Continued from Figure 48.2)

48.3.2 Basic Use of IR Receiver

1. Initialize registers.

   The following registers should be set before using the IR receiver.

   Example: When the RMODE bit is B'000 (the mode in which leader code is included.)

   — CPD : Set the clkp division ratio.
   — LDHL : Set the leader high period (upper and lower limits).
   — LDLL : Set the leader low period (upper and lower limits).
   — BS0L : Set the "0" bit period (upper and lower limits).
   — BS1L : Set the "1" bit period (upper and lower limits).
   — BSHL : Set the "0" or "1" bit high period (upper and lower limits).
   — IRCOMM (XCM bits) : Set the specified compo code.
   — IRCOMM (ARC bits) : Set the acknowledge receive code.
   — IRCOMM (ICC bit) : Set the instruction/compo code check.
   — IRCOMM (RCDM bit) : Set receive code buffer mode.
   — IRMODE (RBUFM bit) : Set double buffer mode.
   — TWP : Set the trailer wait time.
   — RNOFBS : Set the total number of bits in a receive frame.
2. Set the interrupt, if required.
3. Lastly, set the RECON bit to 1 to start receive operation.

   Receive data is stored in the RCODE11 and RCODE12 registers.

   When RCDM = 1, data is written in the received order to bits R1[0]→R1[31].

   When RCDM = 0, data is written in the received order to bits R1[8]→R1[15], R1[24]→R1[31], R1[0]→R1[7], and then R1[16]→R1[23].

   When data has been stored in the RCODE11 and RCODE12 registers, the next receive data is automatically stored in the RCODE21 and RCODE22 registers.
4. Detect the interrupt signal and read the receive data from the buffers.
5. When all the data has been received, set the RECON bit to 0 to stop the IR receiver.

48.3.3 Interrupt Source

Table 48.3 shows the interrupt sources of the IR receiver.

To clear these interrupts, write 0 to the RFREND and RCDEND bits in the IR status register.

Table 48.3 Interrupt Sources

Interrupt System	Interrupt Source (Flag Register)	Description
IR receiver interrupt	Receive frame end interrupt (RFREND)	This interrupt is requested when a frame (including a trailer) has been completely received in the IR receiver block, where the received compo and instruction codes satisfy the conditions specified by the ARC and ICC bits.
	Receive code end interrupt (RCDEND)	This interrupt is requested when all the codes in a frame (excluding a trailer) have been received in the IR receiver block, where the received compo and instruction codes satisfy the conditions specified by the ARC and ICC bits.

49. System Controller (SYSC)

49.1 Overview

The SYSC module controls the supply of power (*) to CPUs (Cortex-A7), SGX with the aim of low leakage power.

Note: (*) Actual control of power shut off for those domains (CPUs (Cortex-A7), SGX) are not supported. Only control for deactivating or activation those domains by controlling clocks distribution and reset assert are supported. Description of power-resume or power-shutoff in this manual means power control in the meaning above.

49.1.1 Features

- Support shutoff and resumption of power in the following four power domains.
  Cortex-A7 CPU0/CPU1 (including the L1 cache)
  Cortex-A7 SCU (including the L2 cache)
  SGX
- Only power to the domains listed below is on (i.e. the domains are in the power-resume state) after a power-on reset.
  Cortex-A7 CPU0 and Cortex-A7 SCU, if MD6 = 1 and MD7 = 0 (Cortex-A7 boot)
  Other domains are in the shutoff state after a power-on reset.
- Control of supplying and shutting off power is independent for each target domain, with the following exceptions.
  SCU of the Cortex-A7s can't be switched off while power to either or both of Cortex-A7 CPU0/1 is on.
- Resumption of the supply of power to Cortex-A7s (CPU0 to CPU1 and SCU) is controlled by interrupts in each domain.
- Power for Cortex-A7s (CPU0 to CPU1) can be shut off by WFI instructions

49.1.2 Block Diagram

Figure 49.1 is block diagrams of the SYSC.

Connected to the internal peripheral bus (the APB bus), the SYSC operates in coordination with the CPG, the RESET module, the CPU, and the debugger; it contains a module that controls the objects of power shutoff.

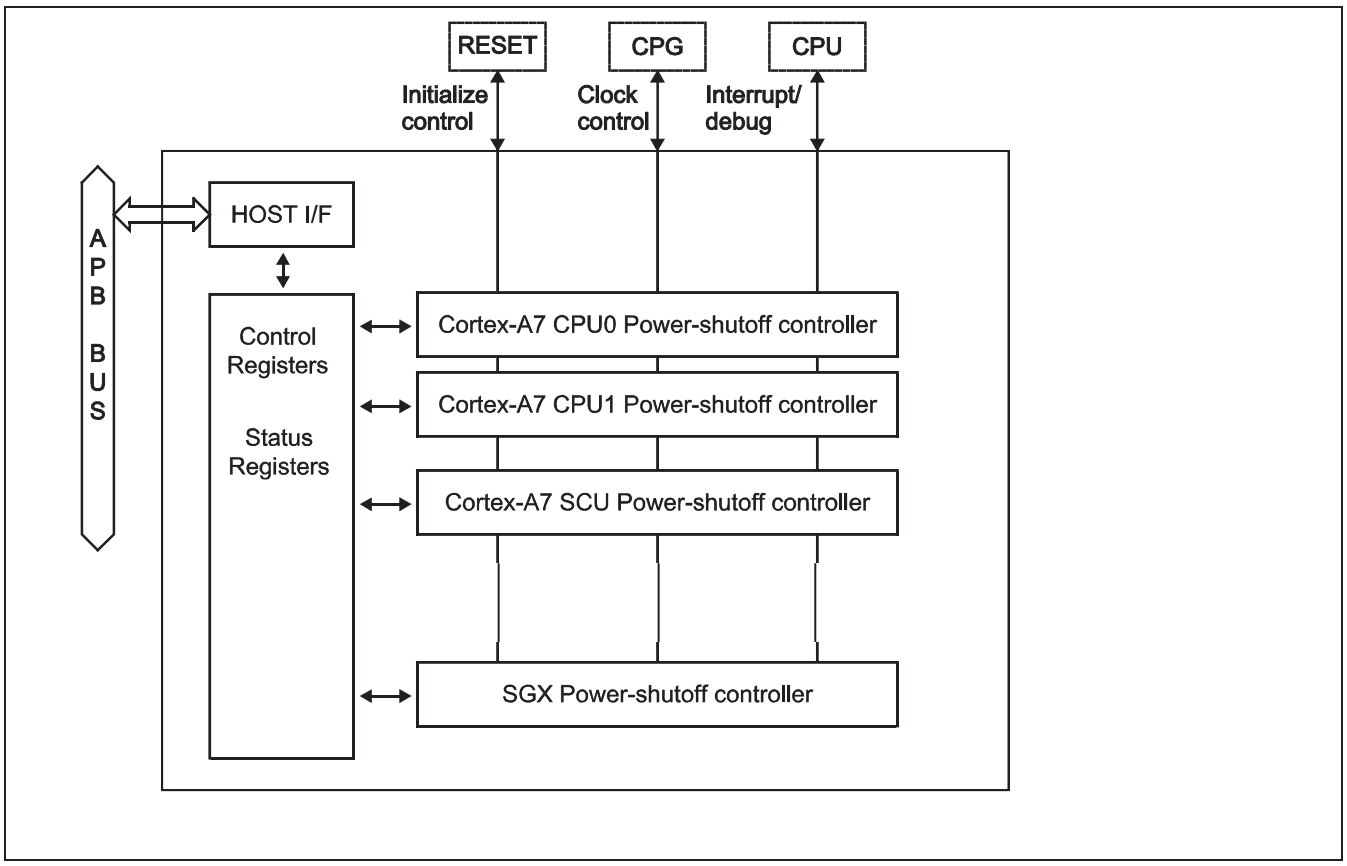


Figure 49.1 Block Diagram of the SYSC

49.1.3 Input/output Pins

The SYSC has no input/output pins.

49.2 Register Configuration

Tables 49.1 to 49.2 list the SYSC registers.

Base-address of SYSC is H'E618 0000.

Do not write to addresses other than those listed below, otherwise normal operation cannot be guaranteed. Values read from other addresses are undefined.

[Legend]

Initial value: Register value after a reset

—: Undefined value

R/W: Readable/writable. The written value can be read.

R: Read-only. The write value should always be the initial value.

—/W: Write-only. The read value is undefined.

Table 49.1 List of Registers (Common Registers)

Name	Abbreviation	R/W	Initial Value	Address	Access size
SYSC Status Register	SYSCSR	R	H'0000 0003	H'0000	32
Interrupt Status Register	SYSCISR	R	H'0000 0000	H'0004	32
Interrupt Status Clear Register	SYSCISCR	—/W	—	H'0008	32
Interrupt Enable Register	SYSCIER	R/W	H'0000 0000	H'000C	32
Interrupt Mask Register	SYSCIMR	R/W	H'0131 11EF	H'0010	32
Cortex-A7 Wake Up Mask Register	WUPMSKCA7	R/W	H'0000 0000	H'0018	32
External Event Request Status Register 2	SYSCEERSR2	R	H'0000 0000	H'002C	32
External Event Request Status Clear register 2	SYSCEERSCR2	—/W	—	H'0030	32
External Event Request Status Enable Register 2	SYSCEERSER2	R/W	H'0000 0000	H'0034	32

Table 49.2 List of Registers (Power Control Registers for each domain)

Name	Abbreviation	R/W	Initial Value	Address	Access size
Power status register 1	PWRSR1	R	H'0000 0010	H'0080	32
Power shutoff control register 1	PWROFFCR1	—/W	—	H'0084	32
Power shutoff status register 1	PWROFFSR1	R	H'0000 0000	H'0088	32
Power resume control register 1	PWRONCR1	—/W	—	H'008C	32
Power resume status register 1	PWRONSR1	R	H'0000 0000	H'0090	32
Power shutoff/resume error register 1	PWRER1	R	H'0000 0000	H'0094	32
Power status register 2	PWRSR2	R	H'0000 0001	H'00C0	32
Power shutoff control register 2	PWROFFCR2	—/W	—	H'00C4	32
Power shutoff status register 2	PWROFFSR2	R	H'0000 0000	H'00C8	32
Power resume control register 2	PWRONCR2	—/W	—	H'00CC	32
Power resume status register 2	PWRONSR2	R	H'0000 0000	H'00D0	32
Power shutoff/resume error register 2	PWRER2	R	H'0000 0000	H'00D4	32
Power status register 3	PWRSR3	R	H'0000 0010	H'0100	32
Power shutoff control register 3	PWROFFCR3	—/W	—	H'0104	32
Power shutoff status register 3	PWROFFSR3	R	H'0000 0000	H'0108	32
Power resume control register 3	PWRONCR3	—/W	—	H'010C	32
Power resume status register 3	PWRONSR3	R	H'0000 0000	H'0110	32
Power shutoff/resume error register 3	PWRER3	R	H'0000 0000	H'0114	32
Power status register 6	PWRSR6	R	H'0000 001E	H'01C0	32
Power shutoff status register 6	PWROFFSR6	R	H'0000 0000	H'01C8	32
Power resume status register 6	PWRONSR6	R	H'0000 0000	H'01D0	32
Power shutoff/resume error register 6	PWRER6	R	H'0000 0000	H'01D4	32

49.2.1 Common Registers

These registers are used to control the shutting off of power to the various modules with respect to the common settings, the interrupts, as well as external events.

49.2.1.1 SYSC Status Register (SYSCSR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PONENB	POFFENB
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1	PONENB	1	R	This bit indicates whether the SYSC is ready to accept power resume requests. Any power resume request issued when the SYSC is disabled from accepting power resume requests will be ignored. 1: Power resume request is acceptable. 0: Power resume request is not accepted.
0	POFFENB	1	R	This bit indicates whether the SYSC is ready to accept power shutoff requests. Any power shutoff request issued when the SYSC is disabled from accepting power shutoff requests will be ignored. 1: Power shutoff request is acceptable. 0: Power shutoff request is not acceptable.

49.2.1.2 Interrupt Status Register (SYSCISR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	CA7-SCU	0	R	Indicates Cortex-A7 SCU power-processing status. This bit is set to 1 when the CA7-SCU bit in the interrupt enable register is 1 upon completion of the Cortex-A7 SCU power shutoff or power resume processing. If the CA7-SCU bit in the interrupt enable register is 0, this bit is not set to 1 even when the Cortex-A7 SCU power shutoff or power resume processing is completed. An interrupt request is issued when the CA7-SCU bit in the interrupt mask register is 0 and this bit is 1. 0: Power shutoff or power resume processing of Cortex-A7 SCU is not completed. 1: Power shutoff or power resume processing of Cortex-A7 SCU is completed.
20	SGX	0	R	Indicates SGX power-processing status. This bit is set to 1 when the SGX bit in the interrupt enable register is 1 upon completion of the SGX power shutoff or power resume processing. If the SGX bit in the interrupt enable register is 0, this bit is not set to 1 even when the SGX power shutoff or power resume processing is completed. An interrupt request is issued when the SGX bit in the interrupt mask register is 0 and this bit is 1. 0: Power shutoff or power resume processing of SGX is not completed. 1: Power shutoff or power resume processing of SGX is completed.
19 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	CA7-CPU[1:0]	00	R	Indicates Cortex-A7 CPU1-0 power-processing status. This bit is set to 1 when the CA7-CPU[1:0] bit in the interrupt enable register is 1 upon completion of the Cortex-A7 core CPU1-0 power shutoff or power resume processing. If the CA7-CPU[1:0] bit in the interrupt enable register is 0, this bit is not set to 1 even when power shutoff or power resume processing for the Cortex-A7 core CPU1-0 is completed. An interrupt request is issued when the CA7-CPU[1:0] bit in the interrupt mask register is 0 and this bit is 1. 0: Power shutoff or power resume processing of Cortex-A7 CPU1-0 is not completed. 1: Power shutoff or power resume processing of CPU1-0 is completed.
4 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

49.2.1.3 Interrupt Status Clear Register (SYSCISCR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	—	0	0	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	—/W	—/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	—	—	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	—/W	—/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	CA7-SCU	—	—/W	Specify clear of Cortex-A7 SCU interrupt status. Writing 1 to this bit clears the CA7-SCU bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored.
20	SGX	—	—/W	Specify clear of SGX interrupt status. Writing 1 to this bit clears the SGX bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored.
19 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	CA7-CPU[1:0]	—	—/W	Specify clear of Cortex-A7 CPU1-0 interrupt status. Writing 1 to this bit clears the CA7-CPU[1:0] bit in the interrupt status register (SYSCISR) to 0. Writing 0 to this bit is ignored.
4 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

49.2.1.4 Interrupt Enable Register (SYSCIER)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	CA7-SCU	0	R/W	Specifies that the status is indicated in the CA7-SCU bit in the interrupt status register (SYSCISR) when the Cortex-A7 SCU power shutoff or power resume processing is completed. 0: Does not indicate the status when power shutoff or power resume processing is completed. 1: Indicates the status when power shutoff or power resume processing is completed.
20	SGX	0	R/W	Specifies that the status is indicated in the SGX bit in the interrupt status register (SYSCISR) when the SGX power shutoff or power resume processing is completed. 0: Does not indicate the status when power shutoff or power resume processing is completed. 1: Indicates the status when power shutoff or power resume processing is completed.
19 to 7	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
6, 5	CA7-CPU[1:0]	00	R/W	Specifies that the status is indicated in the CA7-CPU[1:0] bit in the interrupt status register (SYSCISR) when power shutoff or power resume processing for the Cortex-A7 core CPU1-0 is completed. 0: Does not indicate the status when power shutoff or power resume processing is completed. 1: Indicates the status when power shutoff or power resume processing is completed.
4 to 0	—	0	R	Reserved These bits are always read as 0. The write value should always be 0.

49.2.1.5 Interrupt Mask Register (SYSCIMR)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	CA7-SCU	SGX	—	—	—	—
Initial value:	0	0	0	0	0	0	0	1	0	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	CA7-CPU[1:0]		—	—	—	—	—
Initial value:	0	0	0	1	0	0	0	1	1	1	1	0	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 25	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
24	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
23, 22	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
21	CA7-SCU	1	R/W	Controls the interrupt output when the Cortex-A7 SCU power shutoff or power resume processing is completed. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1. 0: Does not mask the interrupt when the Cortex-A7 SCU power shutoff or power resume processing is completed. 1: Masks the interrupt when the Cortex-A7 SCU power shutoff or power resume processing is completed.
20	SGX	1	R/W	Controls the interrupt output when the SGX power shutoff or power resume processing is completed. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1. 0: Does not mask the interrupt when the SGX power shutoff or power resume processing is completed. 1: Masks the interrupt when the SGX power shutoff or power resume processing is completed.
19 to 17	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
16	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
15 to 13	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
12	—	1	R	Reserved This bit is always read as 1. The write value should always be 1.
11 to 9	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
8, 7	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

Bit	Bit Name	Initial Value	R/W	Description
6, 5	CA7-CPU[1:0]	11	R/W	Controls the interrupt output when power shutoff or power resume processing for the Cortex-A7 core CPU [1:0] is completed. If this bit is 1, no interrupt is issued even if the pertinent bit in the interrupt status register (SYSCISR) is set to 1. 0: Does not mask the interrupt when power shutoff or power resume processing for the Cortex-A7 core CPU [1:0] is completed. 1: Masks the interrupt when power shutoff or power resume processing for the Cortex-A7 core CPU [1:0] is completed.
4	—	0	R	Reserved This bit is always read as 0. The write value should always be 0.
3 to 0	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.

49.2.1.6 Cortex-A7 Wake Up Mask Register (WUPMSKCA7)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CSD[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R/W	R/W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ[1:0]		—	—	—	—	—	—	IRQ[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R	R	R	R	R/W	R/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 18	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
17, 16	CSD[1:0]	00	R/W	Enable/Disable wake up Cortex-A7 CPU0-1 + SCU area when receiving CSD[1:0] factor 0: Enable 1: Disable This setting is available only when Cortex-A7 SCU area is in OFF state
15 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	FIQ[1:0]	00	R/W	Enable/Disable wake up Cortex-A7 CPU0-1 + SCU area when receiving FIQ[1:0] factor 0: Enable 1: Disable This setting is available only when Cortex-A7 SCU area is in OFF state.
7 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	IRQ[1:0]	00	R/W	Enable/Disable wake up Cortex-A7 CPU0-1 + SCU area when receiving IRQ[1:0] factor 0: Enable 1: Disable This setting is available only when Cortex-A7 SCU area is in OFF state.

49.2.1.7 External Event Request Status Register2 (SYSCEERSR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA7[1:0]		—	—	IRQ_CA7[1:0]		—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	FIQ_CA7[1:0]	00	R	If the FIQ_CA7[1:0] bit in the external event request status enable register is 1, this bit is set to 1 when a power resume request due to an FIQ interrupt is accepted by the Cortex-A7 core CPU1-0. If the FIQ_CA7[1:0] bit in the external event request status enable register is 0, this bit is not set to 1 even when a power resume request due to an FIQ interrupt is accepted. This bit is also set to 1 when the request is accepted when power for the Cortex-A7 core CPU1-0 is not shut off. 0: The power resume request due to an FIQ interrupt has not been accepted by the Cortex-A7 core CPU1-0. 1: The power resume request due to an FIQ interrupt has been accepted by the Cortex-A7 core CPU1-0. This bit is set, only when condition above is satisfied in Cortex-A7/SCU is power-shutoff state.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	IRQ_CA7[1:0]	00	R	If IRQ_CA7[1:0] bit in the external event request status enable register is 1, this bit is set to 1 when a power resume request due to an IRQ interrupt is accepted by the ARM core CPU1-0. If the IRQ_CA7[1:0] bit in the external event request status enable register is 0, this bit is not set to 1 even when a power resume request due to an IRQ interrupt is accepted. This bit is also set to 1 when the request is accepted when power for the Cortex-A7 core CPU1-0 is not shut off. 0: The power resume request due to an IRQ interrupt has not been accepted by the Cortex-A7 CPU1-0. 1: The power resume request due to an IRQ interrupt has been accepted by the Cortex-A7 core CPU1-0. This bit is set, only when condition above is satisfied in Cortex-A7/SCU is power-shutoff state.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

49.2.1.8 External Event Request Status Clear Register2 (SYSCEERSCR2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA7[1:0]		—	—	IRQ_CA7[1:0]		—	—	—	—
Initial value:	0	0	0	0	0	0	—	—	0	0	—	—	0	0	0	0
R/W:	R	R	R	R	R	R	—/W	—/W	R	R	—/W	—/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	FIQ_CA7[1:0]	—	—/W	Writing 1 to this bit clears FIQ_CA7[1:0] bit in the external event request status register 2 (SYSCEERSR2) to 0. If 0 is written to this bit or the pertinent bit in the external event request status register is 0, nothing happens. If the pertinent bit in the external event request status register is set to 1 and 1 is written to this bit simultaneously to clear it to 0, setting the bit to 1 takes precedence.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	IRQ_CA7[1:0]	—	—/W	Writing 1 to this bit clears the IRQ_CA7[1:0] bit in the external event request status register2 (SYSCEERSR2) to 0. If 0 is written to this bit or the pertinent bit in the external event request status register is 0, nothing happens. If the pertinent bit in the external event request status register is set to 1 and 1 is written to this bit simultaneously to clear it to 0, setting the bit to 1 takes precedence.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

49.2.1.9 External Event Request Status Enable Register2 (SYSCEERSER2)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	FIQ_CA7[1:0]		—	—	IRQ_CA7[1:0]		—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R/W	R/W	R	R	R/W	R/W	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 10	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
9, 8	FIQ_CA7[1:0]	00	R/W	Specifies that the status be indicated in the FIQ_CA7[1:0] bit in the external event request status register (SYSCOFSR) when a power resume request due to an FIQ interrupt is accepted by the Cortex-A7 core CPU1-0. 0: Does not indicate the status when a power resume request is accepted. 1: Indicates the status when a power resume request is accepted.
7, 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	IRQ_CA7[1:0]	00	R/W	Specifies that the status be indicated in IRQ_CA7[1:0] bit in the external event request status register (SYSCOFSR) when a power resume request due to an IRQ interrupt is accepted by the Cortex-A7 core CPU1-0. 0: Does not indicate the status when a power resume request is accepted. 1: Indicates the status when a power resume request is accepted.
3 to 0	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.

49.2.2 Power Control Registers for ARM CPUs

These registers control power status of Cortex-A7 CPUs.

In the detailed description those registers, the register names corresponding to the modules Cortex-A7 is denoted as n = 6.

49.2.2.1 Power Status Register n (PWRSRn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	PWRUP_CPU [1:0]		—	—	PWRDWN_CPU [1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	1	1	1	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 6	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
5, 4	PWRUP_CPU[1:0]	B'01	R	Indicates the non-power-shutoff state of CPU1-0 0: Not in non-power-shutoff state 1: In non-power-shutoff state
3, 2	—	All 1	R	Reserved These bits are always read as 1. The write value should always be 1.
1, 0	PWRDWN_CPU[1:0]	B'10	R	Indicates the power-shutoff state of CPU1-0 0: Not in power-shutoff state 1: In power-shutoff state

49.2.2.2 Power Shutoff Status Register n (PWROFFSRn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CPU[1:0]	00	R	Indicates the power shutoff sequence execution status of CPU1-0. 0: The power shutoff sequence not being executed 1: The power shutoff sequence being executed

49.2.2.3 Power Resume Status Register n (PWRONSRn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CPU[1:0]	00	R	Indicates the power resume sequence execution status of CPU1-0. 0: The power resume sequence not being executed 1: The power resume sequence being executed

49.2.2.4 Power Shutoff/Resume Error Register n (PWRERn)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	CPU[1:0]	
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 2	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
1, 0	CPU[1:0]	00	R	Indicates whether a power shutoff or power resume request by a preceding register write to CPU1-0 was accepted or not. 0: Either a preceding power shutoff or power resume request to CPU1-0 was accepted. 1: Either a preceding power shutoff or power resume request to CPU1-0 was not accepted.

49.2.3 Power Control Registers for SGX and SCU of Cortex-A7

These registers control power shutoff/resume of following modules. In the detailed description of these registers that follows, the register names corresponding to the modules are denoted as "n (n: 2/3)". The "n" and the module names correspond as follows:

SGX: n = 2
Cortex-A7 SCU: n = 3

49.2.3.1 Power Status Register n (PWRSRn) (n = 2/3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	PWR UP	—	—	—	PWR DWN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0/1	0	0	0	0/1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 5	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
4	PWRUP	0 for n = 2 1 for n = 3	R	Indicates the power non-shutoff status of a given module. 0: The module is not in the power non-shutoff state. 1: The module is in the power non-shutoff state.
3 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PWRDWN	0 for n = 3 1 for n = 2	R	Indicates the power shutoff status of a given module. 0: The module is not in the power shutoff state. 1: The module is in the power shutoff state.

49.2.3.2 Power Shutoff Control Register n (PWROFFCRn) (n = 2/3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWR DWN
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PWRDWN	—	—/W	Specify the start of power-shutoff sequence. Writing 1 to this bit when the POFFENB bit in the SYSC status register is 1 starts the power shutoff sequence for the module. In this case, the ERR bit in the power shutoff/resume error register n is set to 0. Writing 1 to this bit when the POFFENB bit in the SYSC status register is 0 does not start the power shutoff sequence. In this case, the ERR bit in the power shutoff/resume error register n is set to 1. 0: Does not shut off power for the module. 1: Starts the power shutoff sequence for the module. When the power shutoff sequence is started, during the execution of the power shutoff sequence the shutoff processing status is indicated in the DWNSTATE bit in the power shutoff status register n. The PWRUP bit in the power status register n is set to 0. Upon completion of the power shutoff sequence, the PWRDWN bit in the power status register n is set to 1. The pertinent bit in the interrupt status register is set to 1 if it is enabled by the setting of the interrupt status enable register. If 1 is written to this bit when the module is in the power shutoff state, such a request is ignored. In this case, too, if 1 is written when the POFFENB bit is 1, the pertinent bit in the power shutoff/resume error register is set to 0, and if 1 is written when the POFFENB bit is 0, the pertinent bit in the power shutoff/resume error register is set to 1.

Note: Write the value H'0000 0002 to register that have address H'E6150840 before write 1 to “Power Shutoff Control” register.

49.2.3.3 Power Shutoff Status Register n (PWROFFSRn) (n = 2/3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	DWN STATE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	DWNSTATE	0	R	Indicates the power shutoff sequence execution status for the module. 0: The power shutoff sequence not being executed 1: The power shutoff sequence being executed

49.2.3.4 Power Resume Control Register n (PWRONCRn) (n = 2/3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	PWR UP
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	—
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	—/W

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	PWRUP	—	—/W	Specify the start of power-resume sequence. Writing 1 to this bit when the PONENB bit in the SYSC status register is 1 starts the power resume sequence for the module. In this case, the ERR bit in the power shutoff/resume error register n is set to 0. Writing 1 to this bit when the PONENB bit in the SYSC status register is 0 does not start the power resume sequence. In this case, the ERR bit in the power shutoff/resume error register n is set to 1. 0: Does not resume power for the module. 1: Starts the power resume sequence for the module. When the power resume sequence is started, during the execution of the power resume sequence the resume processing status is indicated in the UPSTATE bit in the power resume status register n. The PWRDWN bit in the power status register n is set to 0. Upon completion of the power resume sequence, the PWRUP bit in the power status register n is set to 1. The pertinent bit in the interrupt status register is set to 1 if it is enabled by the setting of the interrupt status enable register. If 1 is written to this bit when the module is in the power non-shutoff state, such a request is ignored. In this case, too, if 1 is written when the PONENB bit is 1, the pertinent bit in the power shutoff/resume error register is set to 0, and if 1 is written when the PONENB bit is 0, the pertinent bit in the power shutoff/resume error register is set to 1.

49.2.3.5 Power Resume Status Register n (PWRONSRn) (n = 2/3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	UP STATE
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	UPSTATE	0	R	Indicates the power resume sequence execution status for the module. 0: The power resume sequence not being executed 1: The power resume sequence being executed

49.2.3.6 Power Shutoff/Resume Error Register n (PWRERn) (n = 2/3)

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	ERR
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 1	—	All 0	R	Reserved These bits are always read as 0. The write value should always be 0.
0	ERR	0	R	Indicates that either a power shutoff or power resume request by a preceding register write to the module was issued when such requests were not acceptable. 0: Either a preceding power shutoff or power resume request to the module was accepted. 1: Either a preceding power shutoff or power resume request to the module was not accepted.

49.3 Operations

49.3.1 Power Control of ARM CPUs

The ARM CPUs can be powered off by executing the WFI instruction. Similarly, power of ARM CPU core can be resumed either by controlling the CPG (APMU) registers or by an IRQ or FIQ interrupt.

For detail of power control by CPG (APMU) registers, see section 7B, Advanced Power Management Unit for AP-System Core (APMU).

(1) Power Control by WFI Instruction and Interrupts

The power shutdown by the WFI instruction is performed only when Cortex-A7 CPU n* power status control register (CA7CPUnCR*) is in the core standby mode. In case of other setting, power shutdown sequence is not activated by the WFI instruction. See section 7B, Advanced Power Management Unit for AP-System Core (APMU).

Power can be resumed by an IRQ or FIQ interrupt on the ARM core. After resuming power of Cortex-A7 CPUs by IRQ/FIQ, read the value of SYSCOFSR2 registers. Without reading those registers after power-resuming, the shutdown sequence of related CPUs will not start.

Note: * n = 0, 1.

49.3.2 Power Control of non-ARM-CPU modules

Power control on modules other than the ARM CPUs can be performed exclusively by means of SYSC registers. Such power control should be performed with reference to the flowchart given below:

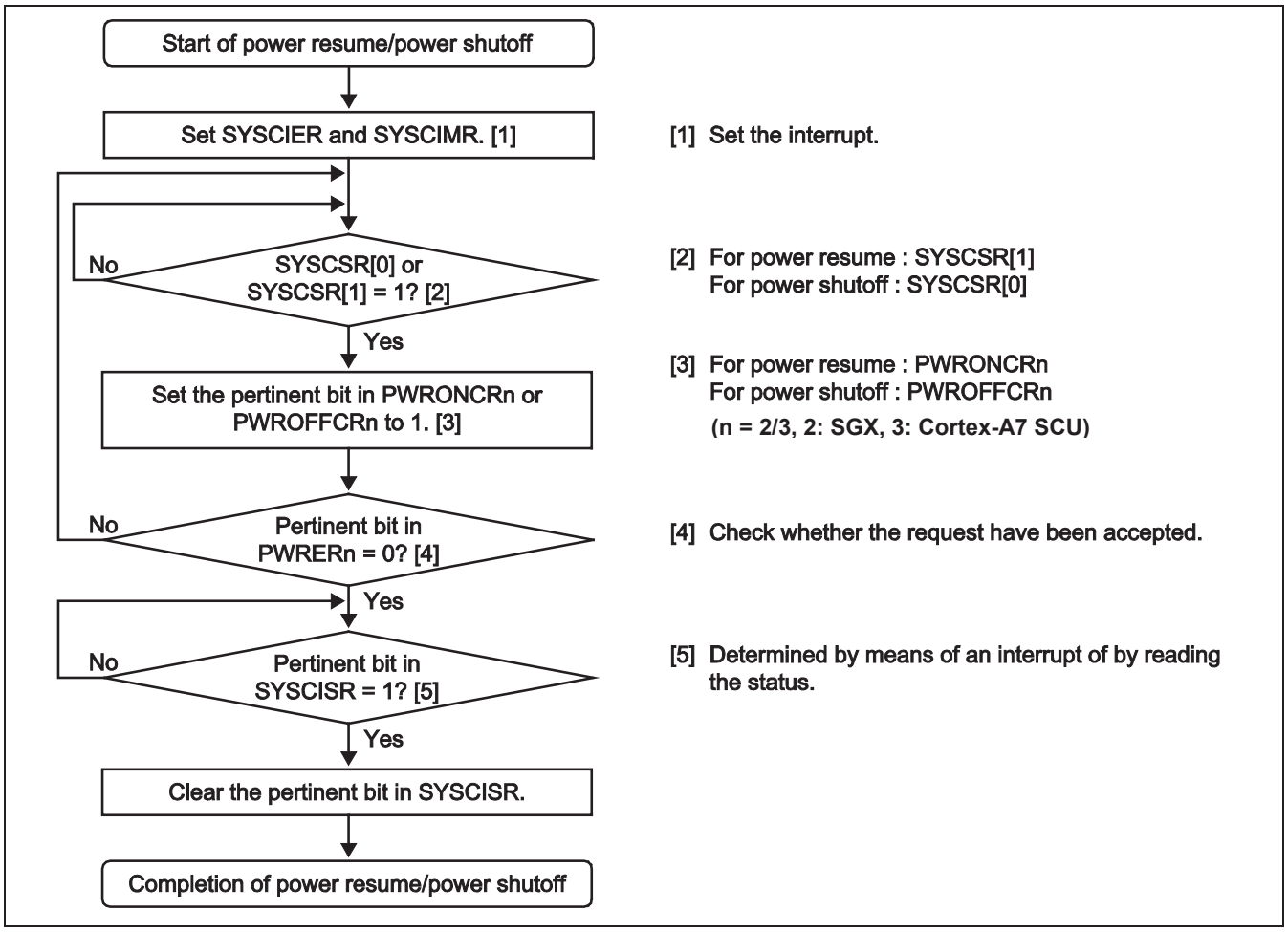


Figure 49.2 Power Resume/Shutoff Flowchart on non-ARM-CPU by Means of SYSC Registers

49.4 Usage Notes

1. For modules other than the ARM CPUs, resume or shutoff sequences on more than one module cannot be executed simultaneously. Whether or not a resume or shutoff sequence can be accepted is indicated in the SYSC status register.
2. The ARM CPUs can simultaneously execute resume or shutoff sequences for the CPU0 to CPU1 of the ARM core only if those sequences are simultaneously activated. Resume and shutoff sequences cannot be executed simultaneously even for the CPU0 to CPU1 of the ARM core.
3. If power for the ARM core is controlled by the WFI instruction or interrupts, such actions can potentially be in contention with power control by means of the SYSC register at an unexpected timing. Such control should be performed with references to the flowchart shown in Figure 49.2.
4. For a module for which power is shut down, register settings and memory contents are not retained; any necessary information should be saved before power is shut off.
5. Shut off and resuming power requires several hundreds of microseconds.

50. CoreSight

50.1 Overview

50.1.1 Features

- JTAG interface
  - — Supports dedicated 5-pin JTAG and SWD

  Supports the cross trigger between following IPs.
  - — Cortex-A7 CPUn.
  - — CoreSight
- Tracing function
  - — ETM is installed for each Cortex-A7 CPU
  - — A maximum of 16 bits × 390 Mbps (145-MHz DDR) trace* data pin output
  - — 16-Kbyte embedded trace FIFO (ETF)

Note: * Design frequency of internal logic. This is limited by IO buffer performance.

50.1.2 Block Diagram

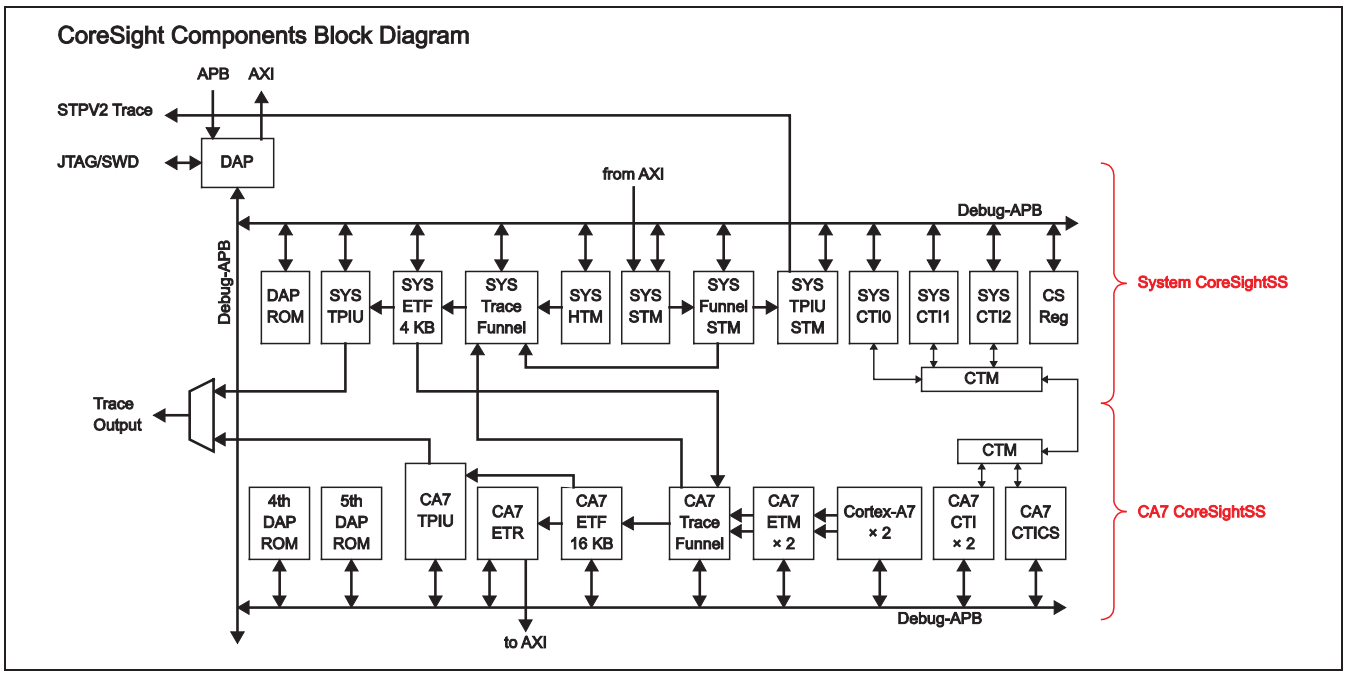


Figure 50.1 Block Diagram of CoreSight

50.1.3 Input/Output Pins

50.1.3.1 JTAG Pins

5-pin JTAG and SWD are supported as dedicated pins.

Table 50.1 JTAG Pins

Function Name	JTAG1 1.8V	JTAG2 1.8V	JTAG3 1.8V	I/O
TRST	TRST#	MMC0_CMD	SD2_CMD	Input
TCK/SWCLK	TCK	MMC0_D0	SD2_DAT0	Input
TMS/SWDIO	TMS	MMC0_D1	SD2_DAT1	Input/output
TDI	TDI	MMC0_D2	SD2_DAT2	Input
TDO/SWO	TDO	MMC0_CLK	SD2_CLK	Output
EDBGREQ	—	MMC0_D3	SD2_DAT3	IN

Notes: 1. Please refer section 5, Pin Function Controller (PFC) to know the other initial states of pull-up/down control each pins. Basically, the pull-up control initial states of JTAG2/3 multiplexed with SD/MMC pins are disabled.
2. If the JTAG Ports are not selected by debug related MD pins (MD[11:10], MD[21:20], MDT[1:0] pins are all low level), TRST# pin of JTAG1 should be set Low level or drove with the same level of PRESET# pin.
3. JTAG1, JTAG2 and JTAG3 and Trace ports support 1.8 V only.

50.1.3.2 Trace Pins

A maximum of 16-bit trace ports are supported as multiplexed pins.

Table 50.2 Trace Pins

Function Name	Pin Name	I/O
ARM_TRACEDATA_0	MMC0_D0	Output
ARM_TRACEDATA_1	SD0_DAT1	Output
ARM_TRACEDATA_2	SD0_DAT2	Output
ARM_TRACEDATA_3	SD0_DAT3	Output
ARM_TRACEDATA_4	MMC0_D6	Output
ARM_TRACEDATA_5	MMC0_D7	Output
ARM_TRACEDATA_6	MMC0_CLK	Output
ARM_TRACEDATA_7	MMC0_CMD	Output
ARM_TRACEDATA_8	MMC0_D2	Output
ARM_TRACEDATA_9	MMC0_D3	Output
ARM_TRACEDATA_10	MMC0_D4	Output
ARM_TRACEDATA_11	MMC0_D5	Output
ARM_TRACEDATA_12	SD2_CLK	Output
ARM_TRACEDATA_13	SD2_CMD	Output
ARM_TRACEDATA_14	SD2_DAT0	Output
ARM_TRACEDATA_15	SD2_DAT1	Output
TRACECLK	SD0_CLK	Output
TRACECTL	MMC0_D1	Output
CTIREQ	SD0_DAT0	Input
CTIACK	SD0_CMD	Output

50.2 Address Map

Table 50.3 CoreSight Address Map

System Address (CPU View)	Debug-APB address (Debugger View)	module
H'E6F00000 to H'E6F00FFF	H'80000000 to H'80000FFF	DAP ROM
H'E6F01000 to H'E6F01FFF	H'80001000 to H'80001FFF	SYS-ETF
H'E6F02000 to H'E6F02FFF	H'80002000 to H'80002FFF	SYS-CTI0
H'E6F03000 to H'E6F03FFF	H'80003000 to H'80003FFF	SYS-TPIU
H'E6F04000 to H'E6F04FFF	H'80004000 to H'80004FFF	SYS-TraceFunnel
H'E6F05000 to H'E6F06FFF	H'80005000 to H'80006FFF	Reserved
H'E6F07000 to H'E6F07FFF	H'80007000 to H'80007FFF	SYS-HTM
H'E6F08000 to H'E6F08FFF	H'80008000 to H'80008FFF	SYS-CTI2
H'E6F09000 to H'E6F09FFF	H'80009000 to H'80009FFF	SYS-STM
H'E6F0A000 to H'E6F0AFFF	H'8000A000 to H'8000AFFF	SYS-TPIU-STM
H'E6F0B000 to H'E6F0BFFF	H'8000B000 to H'8000BFFF	SYS-TraceFunnel-STM
H'E6F0C000 to H'E6F0CFFF	H'8000C000 to H'8000CFFF	SYS-CTI1
H'E6F0D000 to H'E6F1EFFF	H'8000D000 to H'8001EFFF	Reserved
H'E6F1F000 to H'E6F1FFFF	H'8001F000 to H'8001FFFF	CS-Reg
H'E6F20000 to H'E6F7FFFF	H'80020000 to H'8007FFFF	Reserved
H'E6F80000 to H'E6F80FFF	H'80080000 to H'80080FFF	2nd DAP ROM
H'E6F86000 to H'E6F9FFFF	H'80086000 to H'8009FFFF	Reserved
H'E6FA0000 to H'E6FA0FFF	H'800A0000 to H'800A0FFF	3rd DAPROM
H'E6FA1000 to H'E6FAFFFF	H'800A1000 to H'800AFFFF	Reserved
H'E6FC0000 to H'E6FC0FFF	H'800C0000 to H'800C0FFF	4th DAP ROM
H'E6FC1000 to H'E6FC1FFF	H'800C1000 to H'800C1FFF	CA7-ETF
H'E6FC2000 to H'E6FC2FFF	H'800C2000 to H'800C2FFF	CA7-CTICS
H'E6FC3000 to H'E6FC3FFF	H'800C3000 to H'800C3FFF	CA7-TPIU
H'E6FC4000 to H'E6FC4FFF	H'800C4000 to H'800C4FFF	CA7-TraceFunnel
H'E6FC5000 to H'E6FC5FFF	H'800C5000 to H'800C5FFF	CA7-ETR
H'E6FC6000 to H'E6FDFFFF	H'800C6000 to H'800DFFFF	Reserved
H'E6FE0000 to H'E6FE0FFF	H'800E0000 to H'800E0FFF	5th DAPROM
H'E6FE1000 to H'E6FEFFFF	H'800E1000 to H'800EFFFF	Reserved
H'E6FF0000 to H'E6FF0FFF	H'800F0000 to H'800F0FFF	CA7-DBG (CPU0)
H'E6FF1000 to H'E6FF1FFF	H'800F1000 to H'800F1FFF	CA7-PMU (CPU0)
H'E6FF2000 to H'E6FF2FFF	H'800F2000 to H'800F2FFF	CA7-DBG (CPU1)
H'E6FF3000 to H'E6FF3FFF	H'800F3000 to H'800F3FFF	CA7-PMU (CPU1)
H'E6FF8000 to H'E6FF8FFF	H'800F8000 to H'800F8FFF	CA7-CTI (CPU0)
H'E6FF9000 to H'E6FF9FFF	H'800F9000 to H'800F9FFF	CA7-CTI (CPU1)
H'E6FFC000 to H'E6FFCFFF	H'800FC000 to H'800FCFFF	CA7-ETM (CPU0)
H'E6FFD000 to H'E6FFDFFF	H'800FD000 to H'800FDFFF	CA7-ETM (CPU1)

Note: Do not write to any addresses other than listed above. Operations cannot be guaranteed if writing is attempted. Values read from addresses other than those listed above are undefined.

50.3 Cross Trigger Connection

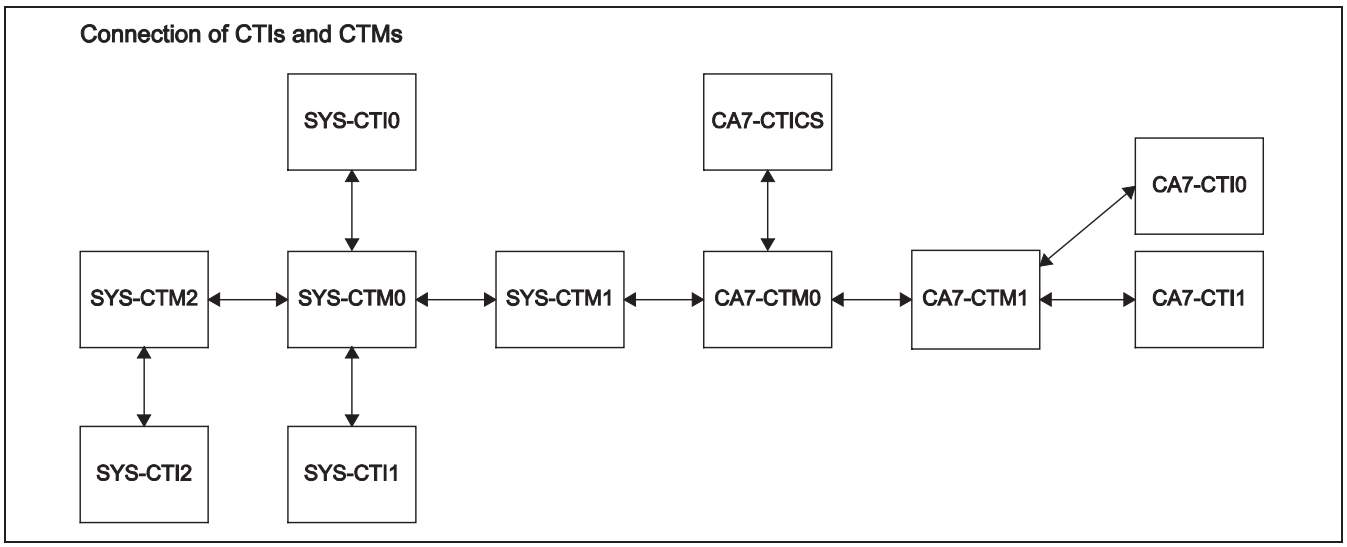


Figure 50.2 Cross Trigger Connection

50.4 SYS-CTI0 Trigger Connection

Table 50.4 SYS-CTI0 Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	HTMEXTOUT[1]	SYS-HTM
[6]	HTMEXTOUT[0]	SYS-HTM
[5]	HTMTRIGGGER	SYS-HTM
[4]	Not in use	
[3]	ACQCOMP	SYS-ETF
[2]	FULL	SYS-ETF
[1]	Not in use	
[0]	Not in use	

Table 50.5 SYS-CTI0 Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	Reserved (not in use)	
[6]	Not in use	
[5]	HTMEXTIN[1]	SYS-HTM
[4]	HTMEXTIN[0]	SYS-HTM
[3]	TRIGIN	SYS-TPIU
[2]	FLUSHIN	SYS-TPIU
[1]	TRIGIN	SYS-ETF
[0]	FLUSHIN	SYS-ETF

50.5 SYS-CTI1 Trigger Connection

Table 50.6 SYS-CTI1 Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	ASYNCOUT	SYS-STM
[6]	TRIGOUTHETE	SYS-STM
[5]	TRIGOUTSW	SYS-STM
[4]	TRIGOUTSPTE	SYS-STM
[3]	Not in use	
[2]	Not in use	
[1]	Not in use	
[0]	Not in use	

Table 50.7 SYS-CTI1 Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	Not in use	
[5]	HWEVENTS[3:2]	SYS-STM
[4]	HWEVENTS[1:0]	SYS-STM
[3]	TRIGIN	SYS-TPIU-STM
[2]	FLUSHIN	SYS-TPIU-STM
[1]	Not in use	
[0]	Not in use	

50.6 SYS-CTI2 Trigger Connection

Table 50.8 SYS-CTI2 Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	Reserved (not in use)	
[6]	Not in use	
[5]	Not in use	
[4]	Not in use	
[3]	Not in use	
[2]	Not in use	
[1]	Not in use	
[0]	Not in use	

Table 50.9 SYS-CTI2 Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	Reserved (not in use)	
[6]	Not in use	
[5]	Not in use	
[4]	Not in use	
[3]	Not in use	
[2]	Not in use	
[1]	Not in use	
[0]	Not in use	

50.7 CA7-CTI[0-1] Trigger Connection

Table 50.10 CA7-CTI[0, 1] Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	Not in use	
[6]	ETMTRIGGER	ETM-A7
[5]	COMMRX	Cortex-A7
[4]	COMMTX	Cortex-A7
[3]	EXTOUT[1]	ETM-A7
[2]	EXTOUT[0]	ETM-A7
[1]	nPMUIRQ	Cortex-A7
[0]	DBGTRIGGER	Cortex-A7

Table 50.11 CA7-CTI[0, 1] Trigger Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	DBGRESTART	Cortex-A7
[6]	nCTIIRQ	INTC for ARM
[5]	Not in use	
[4]	EXTIN[3]	ETM-A7
[3]	EXTIN[2]	ETM-A7
[2]	EXTIN[1]	ETM-A7
[1]	EXTIN[0]	ETM-A7
[0]	DBGRQ	Cortex-A7

50.8 CA7-CTICS Trigger Connection

Table 50.12 CA7-CTICS Trigger Inputs

Trigger Input Bit	Trigger Signal	Source Device
[7]	Not in use	
[6]	Not in use	
[5]	Not in use	
[4]	Not in use	
[3]	ACQCOMP	A7-ETF
[2]	FULL	A7-ETF
[1]	ACQCOMP	A7-ETR
[0]	FULL	A7-ETR

Table 50.13 CA7-CPU-CTICS Outputs

Trigger Output Bit	Trigger Signal	Destination Device
[7]	TRIGIN	A7-ETR
[6]	FLUSHIN	A7-ETR
[5]	Not in use	
[4]	Not in use	
[3]	TRIGIN	A7-TPIU
[2]	FLUSHIN	A7-TPIU
[1]	TRIGIN	A7-ETF
[0]	FLUSHIN	A7-ETF

50.9 Register Description

50.9.1 LOCKACCESS Register

Address CPU view: H'E6F1FFB0 Debugger view: H'8001FFB0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
R/W:	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W	W

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	—	W	Lock Access Register See CoreSight Architecture Specification

50.9.2 LOCKSTATUS Register

Address CPU view: H'E6F1FFB4 Debugger view: H'8001FFB4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 0	—	H'0000 0003	R	Lock Status Register See CoreSight Architecture Specification

50.9.3 Peripheral ID4 Register

Address CPU view: H'E6F1FFD0 Debugger view: H'8001FFD0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	4KB count				JEP106 continuation code			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 4	4KB count	All 0	R	
3 to 0	JEP106 continuation code	H'4	R	

50.9.4 Peripheral ID0 Register

Address CPU view: H'E6F1FFE0 Debugger view: H'8001FFE0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Part No.0							
Initial value:	0	0	0	0	0	0	0	0	1	0	1	0	1	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	Part No.0	H'AA	R	

50.9.5 Peripheral ID1 Register

Address CPU view: H'E6F1FFE4 Debugger view: H'8001FFE4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	JEP106 ID code[3:0]				Part No.1			
Initial value:	0	0	0	0	0	0	0	0	0	0	1	1	1	1	1	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 4	JEP106 ID code[3:0]	H'3	R	
3 to 0	Part No.1	H'F	R	

50.9.6 Peripheral ID2 Register

Address CPU view: H'E6F1FFE8 Debugger view: H'8001FFE8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Rev				1'b1	JEP106 ID code[6:4]		
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 4	Rev	H'0	R	
3	1'b1	1	R	
2 to 0	JEP106 ID code[6:4]	H'2	R	

50.9.7 Peripheral ID3 Register

Address CPU view: H'E6F1FFEC Debugger view: H'8001FFEC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	RevAnd				CustomrModified			
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 4	RevAnd	H'0	R	
3 to 0	CustomrModified	H'0	R	

50.9.8 Component ID0 Register

Address CPU view: H'E6F1FFF0 Debugger view: H'8001FFF0

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Preamble							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	1	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	Preamble	H'0D	R	

50.9.9 Component ID1 Register

Address CPU view: H'E6F1FFF4 Debugger view: H'8001FFF4

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Component class				Preamble			
Initial value:	0	0	0	0	0	0	0	0	1	1	1	1	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 4	Component class	H'F	R	
3 to 0	Preamble	H'0	R	

50.9.10 Component ID2 Register

Address CPU view: H'E6F1FFF8 Debugger view: H'8001FFF8

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Preamble							
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	1	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	Preamble	H'05	R	

50.9.11 Component ID3 Register

Address CPU view: H'E6F1FFFC Debugger view: H'8001FFFC

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—	—
Initial value:	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	—	—	—	—	—	—	—	Preamble							
Initial value:	0	0	0	0	0	0	0	0	1	0	1	1	0	0	0	1
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit	Bit Name	Initial Value	R/W	Description
31 to 8	—	All 0	R	Reserved
7 to 0	Preamble	H'B1	R	

51. Electrical Characteristics

51.1 Absolute Maximum Ratings

Table 51.1.1 Absolute Maximum Ratings

Item	Value	Unit	Remarks
Power supply voltage (3.3 V) (VCCQ, VCCQ_SD/VCCQ_MMC(SDHI), VCCQA_USB, VCCQA_LVDS, VCCQA_ADC, VCCQA_DAC)	-0.3 to +4.2	V	
Power supply voltage (1.8 V) (VCCQ18, VCCQ_SD/VCCQ_MMC(SDR50/SDR104))	-0.3 to +2.6	V	
Power supply voltage (1.5V) (VDDQ_M0)	-0.3 to +2.6	V	
Power supply voltage (1.2 V) (VDD, VDD_CPGPLL, VDD_DDRPLL, VDDA_USBPLL, VDDA_LVDSPLL)	-0.3 to +1.6	V	
Input voltage (3.3-V I/O)	-0.3 to VCCQ + 0.3	V	*1
Input voltage (3.3-V I/O [SDHI])	-0.3 to VCCQ_SD/VCCQ_MMC + 0.3	V	*1
Input voltage (1.8-V I/O)	-0.3 to VCCQ18 + 0.3	V	*2
Input voltage (1.8-V I/O [SDHI (SDR50/SDR104)])	-0.3 to VCCQ_SD/VCCQ_MMC + 0.3	V	*2
Input voltage (1.5-V I/O [DDR3])	-0.3 to VDDQ_M0 + 0.3	V	*3
Input voltage (USB0_OVC pin, USB1_OVC pin [USB2.0])	-0.3 to VCCQ + 0.3	V	*1
Input voltage (USB0_VBUS pin, USB1_VBUS pin [USB2.0])	-0.3 to + 5.5	V	
Output voltage (3.3-V I/O)	-0.3 to VCCQ + 0.3	V	*1
Output voltage (3.3-V I/O [SDHI])	-0.3 to VCCQ_SD/VCCQ_MMC + 0.3	V	*1
Output voltage (1.8-V)	-0.3 to VCCQ18 + 0.3	V	*2
Output voltage (1.8-V I/O [SDHI (SDR50/SDR104)])	-0.3 to VCCQ_SD/VCCQ_MMC + 0.3	V	*2
Output voltage (1.5-V I/O [DDR3])	-0.3 to VDDQ_M0 + 0.3	V	*3
Operating temperature	-40 to +115	°C	Tc (case)
	-40 to +85	°C	Ta (ambient)
Storage temperature	-55 to +125	°C	Ta (ambient)

Notes: Permanent damage to the LSI may result if absolute maximum ratings are exceeded. In normal operation, this LSI should be used within the specifications described in the following descriptions. If this LSI is not used within the specifications, the reliability of this LSI may lower.

Voltages are referenced at GND = VSS = 0 V.

1. Do not exceed 4.2 V.
2. Do not exceed 2.6 V.
3. Do not exceed 1.875 V.

51.2 Power Supply

Table 51.2.1 Power Supply

Item	Symbol	Voltage			Unit	Remarks
		Min.	Typ.	Max.		
Power supply (Internal)	VDD	1.16	1.21	1.26	V	VDD for power supply and VSS for ground
Power supply (3.3-V I/O)	VCCQ	3.0	3.3	3.6	V	VCCQ for power supply and VSS for ground
Power supply (3.3-V I/O [SDHI])	VCCQ_SD0, VCCQ_SD2, VCCQ_MMC	3.0	3.3	3.6	V	VCCQ_SD0, VCCQ_SD2, VCCQ_MMC for power supply and VSS for ground
Power supply (1.8-V I/O [VCCQ18])	VCCQ18	1.7	1.8	1.9	V	VCCQ18 for power supply and VSS for ground
Power supply (1.8-V I/O [SDHI(SDR50/SDR104)])	VCCQ_SD0, VCCQ_SD2, VCCQ_MMC	1.7	1.8	1.9	V	VCCQ_SD0, VCCQ_SD2, VCCQ_MMC for power supply and VSS for ground
Power supply (1.5-V I/O [DDR3])	VDDQ_M0	1.425	1.5	1.575	V	VDDQ_M0 for power supply and VSS for ground
Power supply (PLL [CPG])	VDD_CPGPLL0, VDD_CPGPLL1, VDD_CPGPLL3	1.16	1.21	1.26	V	VDD_CPGPLL0, VDD_CPGPLL1, VDD_CPGPLL3 for power supply and VSS_CPGPLL0, VSS_CPGPLL1, VSS_CPGPLL3 for ground respectively V
Power supply (PLL [DDR3])	VDD_DDRPLL1, VDD_DDRPLL2	1.16	1.21	1.26	V	VDD_DDRPLL1, VDD_DDRPLL2 for power supply and VSS_DDRPLL1, VSS_DDRPLL2 for ground respectively
Power supply (PLL [USB2.0])	VDDA_USBPLL	1.16	1.21	1.26	V	VDDA_USBPLL for power supply and VSSA_USB for ground
Power supply (USB2.0)	VCCQA_USB	3.0	3.3	3.6	V	VCCQA_USB for power supply and VSSA_USB for ground
Power supply (LVDS)	VCCQA_LVDS	3.0	3.3	3.6	V	VCCQA_LVDS for power supply and VSSQA_LVDS for ground
	VDDA_LVDSPLL	1.16	1.21	1.26	V	VDDA_LVDSPLL for power supply and VSS for ground
Power supply (ADC [DVDEC])	VCCQA_ADC	3.0	3.3	3.6	V	VCCQA_ADC for power supply and VSSQA_ADC for ground
Power supply (DAC [DVENC])	VCCQA_DAC	3.0	3.3	3.6	V	VCCQA_DAC for power supply and VSSQA_DAC for ground

51.3 Sequence of Turning On/Off Power Supplies

51.3.1 Sequence of Turning On/Off Power Supplies with Different Voltage Levels

This subsection specifies the sequence of turning on/off power supplies with different voltage levels: 1.2-V power supplies (hereinafter referred to as VDD12 and the LSI pins are VDD, VDD_CPGPLL0, VDD_CPGPLL1, VDD_CPGPLL3, VDD_DDRPLL1, VDD_DDRPLL2, VDDA_USBPLL, VDDA_LVDSPLL), 1.5-V power supplies (referred to as VDD15, and the LSI pin is VDDQ_M0), 1.8-V power supplies (referred to as VDD18, and the LSI pins are VCCQ18, and VCCQ_SD0/VCCQ_MMC(SDR104), VCCQ_SD2(SDR50)), 3.3-V power supplies (referred to as VDD33, and the LSI pins are VCCQ, VCCQ_SD0/VCCQ_SD2/VCCQ_MMC(SDHI), and VCCQA_USB, VCCQA_LVDS, VCCQA_ADC, VCCQA_DAC), and grounds (referred to VSS**, and the LSI pins are VSS, VSS_CPGPLL0, VSS_CPGPLL1, VSS_CPGPLL3, VSS_DDRPLL1, VSS_DDRPLL2, and VSSA_USB, VSSQA_LVDS, VSSQA_ADC, VSSQA_DAC).

(1) Turning On Power Supply

There are no restrictions on the power-on sequence. Ensure that all other power supplies rise from the ground (VSS**) level within 300 ms of any single power supply rising from the ground (VSS**) level.

(2) Turning Off Power Supply

There are no restrictions on the power-off sequence. Ensure that all other power supplies fall to the ground (VSS**) level within 300 ms of any single power supply being turned off.

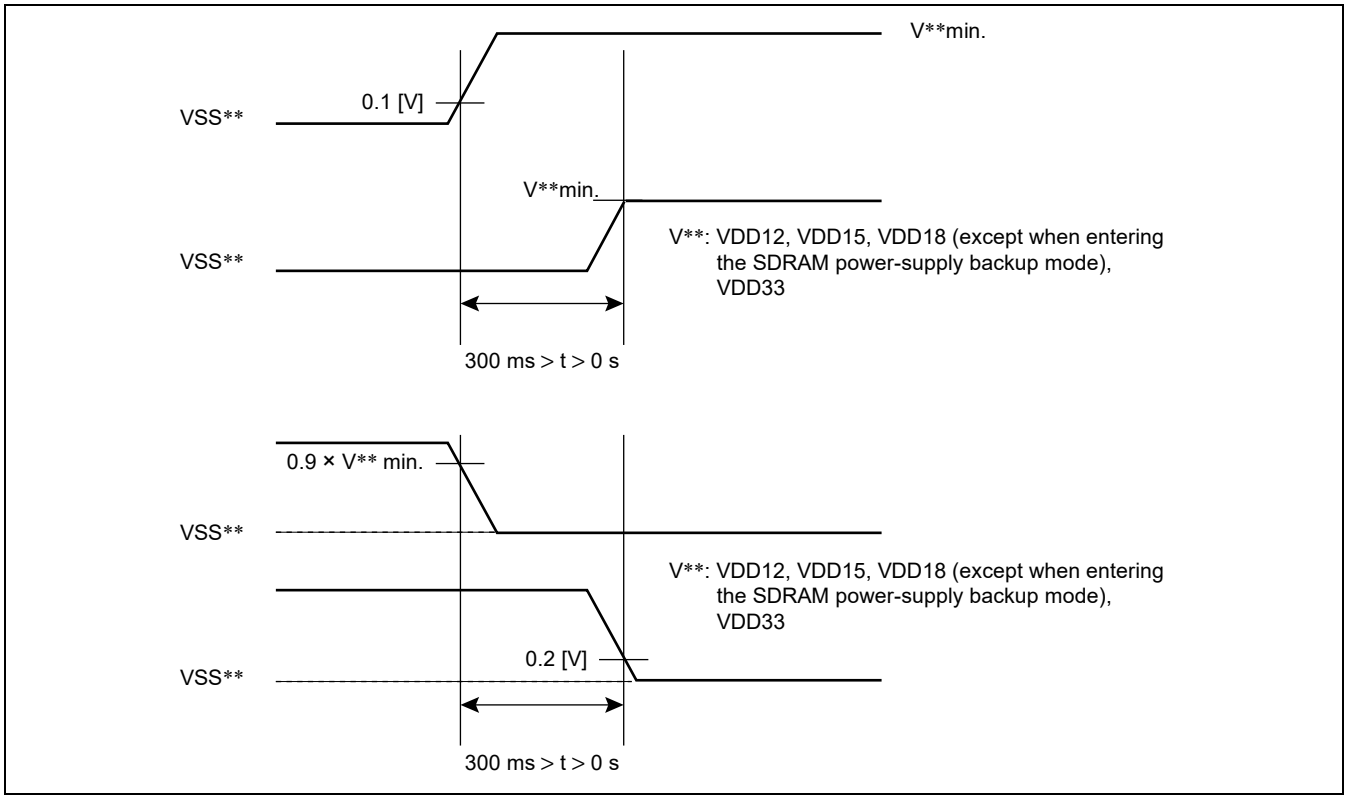


Figure 51.3.1 Sequence of Turning On Power Supplies with Different Voltage Levels

51.3.2 Sequence of Turning On/Off Power Supplies with Same Voltage Levels

This subsection specifies the sequence of turning on/off several power supplies with the same voltage levels (VDD12 power supplies, VDD18 power supplies, and VDD33 power supplies). The sequence of turning on/off VDD12 power supplies is shown in Figure 51.3.2. The voltage difference specified for the VDD12 supplies also applies to the VDD18 and VDD33 power supplies.

(1) Turning On Power Supply

There are no restrictions on the power-on sequence. Note that the voltage difference between the power supplies with the same voltage levels must be 0.3 V or lower.

(2) Turning Off Power Supply

There are no restrictions on the power-off sequence. Note that the voltage difference between the power supplies with the same voltage levels must be 0.3 V or lower.

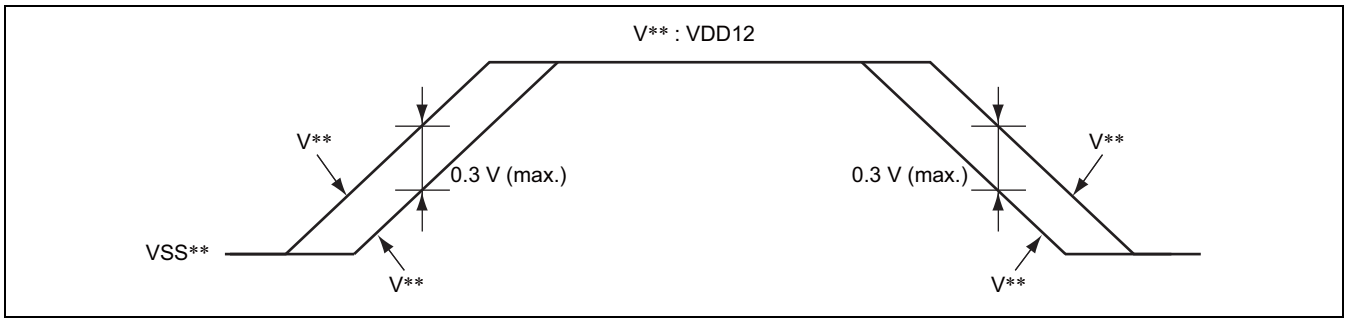


Figure 51.3.2 Sequence of Turning On/Off Power Supplies with Same Voltage Levels

51.4 DC Characteristics

Table 51.4.1 Supply Current

Conditions: Each power supply and ground are separated, ground is 0 V respectively,
Tc = -40 to +115 ºC (-20 to +115 °C for SDR104 only).

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Supply current (internal)	Normal	IDD	—	—	4000	mA	VDD = 1.26 V
Supply current (3.3-V I/O)	Normal	ICCQ	—	—	200	mA	VCCQ = 3.6 V Local bus Access only case Current from/to external load is not included.
Supply current (3.3-V I/O [SDHI])	Normal	ICCQ_SD0	—	—	18.0	mA	VCCQ_SDn = VCCQ_MMC = 3.6 V (n = 0, 2)
		ICCQ_SD2	—	—	18.0		
		ICCQ_MMC	—	—	18.0		
Supply current (1.8-V I/O)	Normal	ICCQ18	—	—	30.0	mA	VCCQ18 = 1.9 V
Supply current (1.8-V I/O [SDHI] (SDR50, SDR104))	Normal	ICCQ_SD0	—	—	30.0	mA	VCCQ_SDn = VCCQ_MMC = 1.9 V (n = 0, 2)
		ICCQ_SD2	—	—	30.0		
		ICCQ_MMC	—	—	30.0		
Supply current (1.5-V I/O [DDR3])	Normal	IDDQ_M0	—	—	450	mA	VDDQ_M0 = 1.575 V
Supply current (PLL [CPG])		IDD_CPGPLL0	—	—	5.0	mA	VDD_CPGPLLn = 1.26 V (n = 0, 1, 3)
		IDD_CPGPLL1	—	—	5.0		
		IDD_CPGPLL3	—	—	5.0		
Supply current (PLL [DDR3])		IDD_DDRPLLn	—	—	10.0	mA	VDD_DDRPLLn = 1.26 V (n = 1, 2)
Supply current (PLL [USB2.0])		IDDA_USBPLL	—	—	100.0	mA	VDDA_USBPLL = 1.26 V
Supply current (USB2.0)	Normal	ICCQA_USB	—	—	70.0	mA	VCCQA_USB = 3.6 V
Supply current (LVDS)	Normal	ICCQA_LVDS	—	—	64.0	mA	VCCQA_LVDS = 3.6 V
	Normal	IDDQA_LVDSPLL	—	—	2.5	mA	VDDA_LVDSPLL = 1.26 V
Supply current (ADC [DVDEC])	Normal	ICCQA_ADC	—	—	60.0	mA	VCCQA_ADC = 3.6 V
Supply current (DAC [DVENC])	Normal	ICCAQ_DAC	—	—	20.0	mA	VCCQA_DAC = 3.6 V

Table 51.4.2 DC Characteristics (3.3-V I/O)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	2.0	—	VCCQ + 0.3	V	VCCQ = 3.0 to 3.6 V	—
Input low voltage	VIL	-0.3	—	0.8	V		
Schmitt Input high voltage	VT+	—	—	2.2	V	VCCQ = 3.0 to 3.6 V	PRESET#
Schmitt Input low voltage	VT-	0.8	—	—	V		
Output high voltage	VOH	2.4	—	VCCQ + 0.3	V	VCCQ = 3.0 to 3.6 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	All pins*2
Pin capacitance	CL	—	—	15	pF		DP/DM only
Input leakage current	ILI	—	—	1	µA	VCCQ = 3.0 to 3.6 V	All input pins*1
Input leakage current	ILI	—	—	10	µA		DP/DM only
Output leakage current	ILO	—	—	1	µA		Hi-Z output*1
Output leakage current	ILO	—	—	10	µA		DP/DM only
Pull-up current	IPU	8	—	250	µA		Vin = VSS

Notes: 1. This excludes pins with pull-up resistors, which are off and USBn_DP/USBn_DM. (n = 0, 1)
2. Except power supply and USB pins.

Table 51.4.3 DC Characteristics (3.3-V I/O [SDHI])

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage	VIH	0.625 × VCCQ_SD	—	VCCQ_SD + 0.3	V	VCCQ_SD = 3.0 to 3.6 V	—
Input low voltage	VIL	VSS - 0.3	—	0.25 × VCCQ_SD	V	VSS = 0 V	—
Output high voltage	VOH	0.75 × VCCQ_SD	—	—	V		IOH = -2 mA VCCQ_SDmin
Output low voltage	VOL	—	—	0.125 × VCCQ_SD	V		IOL = 2 mA VCCQ_SDmin
Pin capacitance	CL	—	—	10	pF		—
Input leakage current	ILI	—	—	1	µA		—
Output leakage current	ILO	—	—	1	µA		Hi-Z output

Table 51.4.4 DC Characteristics (1.8-V I/O [SDHI (SDR50, SDR104)])

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Input high voltage	VIH	1.27	—	2.00	V	VSS = 0 V	—
Input low voltage	VIL	VSS – 0.3	—	0.58	V		—
Output high voltage	VOH	1.4	—	—	V		IOH = -2 mA
Output low voltage	VOL	—	—	0.45	V		IOL = 2 mA
Pin capacitance	CL	—	—	10	pF		—
Input leakage current	ILI	—	—	1	µA		—
Output leakage current	ILO	—	—	1	µA		Hi-Z output

Table 51.4.5 DC Characteristics (1.8-V I/O)

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Input high voltage	VIH	VCCQ18 × 0.8	—	VCCQ18 + 0.3	V	—	—
Input low voltage	VIL	-0.3	—	VCCQ18 × 0.2	V		
Output high voltage	VOH	0.7 × VCCQ18	—	VCCQ18 + 0.3	V	VCCQ18 = 1.7 to 1.9 V	IOH = -4 mA
Output low voltage	VOL	-0.3	—	0.4	V		IOL = 4 mA
Pin capacitance	CL	—	—	10	pF	—	—
Input leakage current	ILI	—	—	1	µA	VCCQ18 = 1.7 to 1.9 V	All input pins
Output leakage current	ILO	—	—	1	µA		Hi-Z output
Pull-up current	IPU	6	—	240	µA	—	Vin = VSS

Table 51.4.6 DC Characteristics (1.5-V I/O [DDR3])

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
Input high voltage (MDQ pin)	VIH	VREF + 0.1	—	—	V	VDDQ_M0 = 1.425 to 1.575 V	M0DQ, M0DQS pins
Input low voltage (MDQ pin)	VIL	—	—	VREF – 0.1	V		
Input high voltage	VIH	0.7 × VDDQ_M0	—	—	V	VDDQ_M0 = 1.425 to 1.575 V	M0BKPRST#, M0SDBUP pins
Input low voltage	VIL	—	—	0.3 × VDDQ_M0,	V		
Differential input reference voltage	VREF	0.49 × VDDQ_M0	0.50 × VDDQ_M0	0.51 × VDDQ_M0	V	VDDQ_M0 = 1.425 to 1.575 V	*1
DC differential input voltage	VIHD	0.2	—	—	V	M0DQS = H, VIN = 0.5 × VDDQ_M0, VDD = 1.0 Vtyp, VDDQ_M0 = 1.425 to 1.575 V	M0DQS pins
DC differential input voltage	VILD	—	—	-0.2	V	M0DQS = L, VIN = 0.5 × VDDQ_M0, VDD = 1.16 to 1.26V, VDDQ_M0 = 1.425 to 1.575 V	
DC differential input voltage	VIN	0.5 × VDDQ_M0 – 0.250	—	0.5 × VDDQ_M0 + 0.250	V	VIHD = 200 mV or VILD = -200 mV, VDD = 1.16 to 1.26V, VDDQ_M0 = 1.425 to 1.575 V	
Input high voltage	VIH (AC)	VREF + 0.175	—	—	V	—	—
Input low voltage	VIL (AC)	—	—	VREF - 0.175	V	—	—
AC differential input cross point voltage	VIX (AC)	VDDQ_M0 – 0.15	—	VDDQ_M0 + 0.15	V	—	M0DQS pin *2
AC differential output cross point voltage	VOX (AC)	VREF – 0.125	—	VREF + 0.125	V	—	M0CK, M0DQS pins
High Hi-Z leak current	IOZH	—	—	4	µA	—	Other than M0ZQ pin
Low Hi-Z leak current	IOZL	-4	—	—	µA	—	
High Hi-Z leak current	IOZH	—	—	5	µA	—	M0ZQ pin
Low Hi-Z leak current	IOZL	-5	—	—	µA	—	
Pin capacitance	CL	—	—	10	pF	—	All pins*3

Notes: 1. Peak to peak ac noise on VREF may not exceed ±2 % of VREF.
2. The VIX (AC) indicates the voltage at which differential input signals cross each other. The typical value of VIX (AC) is expected to be 0.5 × VDDQ_M0.
3. Except power supply pins.

Table 51.4.7 DDR3 Interface ODT Characteristics

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement conditions	Remarks
ODT resistance (60 Ω)	RTT60	54.0	—	96.0	Ω	VDD = 1.26 V, VDDQ_M0 = 1.5 V	—
VM deviation	ΔVM	-6	—	+6	%		*

Note: VM is a voltage value measured with the ODT turned on without any load applied to this LSI chip. ΔVM is obtained by the following formula:
ΔVM = (2 × VM / VDDQ_M0 -1) × 100

Table 51.4.8 USB High-Speed Transceiver Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input	Common mode voltage range	V_{HSCM}	-50	—	500	mV	—
	Squelch threshold	V_{HSSQ}	100	—	150	mV	
Output	Idle state	V_{HSOI}	-10	—	10	mV	—
	High level voltage	V_{HSOH}	360	—	440	mV	
	Low level voltage	V_{HSOL}	-10	—	10	mV	
	Chirp J state	V_{CHIRPJ}	700	—	1100	mV	
	Chirp K state	V_{CHIRPK}	-900	—	-500	mV	

Table 51.4.9 USB Low-/Full-speed Transceiver Characteristics

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
Input	High voltage (driven)	V_{IH}	2.0	—	—	V	—
	Low voltage	V_{IL}	—	—	0.8	V	—
	Differential input sensitivity	V_{DI}	0.2	—	—	V	|DP-DM|
	Differential common mode range	V_{CM}	0.8	—	2.5	V	—
Output	High voltage (driven)	V_{OH}	2.8	—	3.6	V	I_{OH} = -200 µA
	Low voltage	V_{OL}	0.0	—	0.3	V	I_{OL} = 2 mA
	Output signal crossover voltage	V_{CRS}	1.3	—	2.0	V	C_L = 50 pF (Full-speed), C_L = 200 to 600 pF (Low-speed)

Table 51.4.10 USB High-Speed Output Driver Impedance

Item		Symbol	Min.	Typ.	Max.	Unit	Remarks
DP pull-up resistor (on-chip)	Idle state	R_{PU}	0.9	—	1.575	kΩ	—
	Receiving state		1.425	—	3.090	kΩ	—
Pull-down resistor (on-chip)		R_{PD}	14.25	—	24.80	kΩ	—

Table 51.4.11 DC Characteristics of VBUS, USB_EXTAL pin

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
VBUS input voltage	VIH	4.02	—	5.25	V	—
	VIL	-0.3	—	0.5	V	—
USB_EXTAL input voltage	VIH	VCCQA_USB – 0.5	—	VCCQA_USB + 0.3	V	—
	VIL	-0.3	—	0.5	V	—

Table 51.4.12 DC Characteristics of LVDS pin*

Item	Symbol	Min.	Typ.	Max.	Unit	Measurement condition	Remarks
Differential output voltage	|Vod|	0.250	—	0.450	V	R_L = 100 Ω	—
Difference Vod between ‘H’ and ‘L’	ΔVod	—	—	50	mV	R_L = 100 Ω	—
Output offset voltage	Vos	1.125	—	1.375	V	R_L = 100 Ω	—
Difference Vos between ‘H’ and ‘L’	ΔVos	—	—	50	mV	R_L = 100 Ω	—

Note: * TXCLKOUTP, TXCLKOUTM, TXOUT0P, TXOUT0M, TXOUT1P, TXOUT1M, TXOUT2P, TXOUT2M, TXOUT3P, TXOUT3M

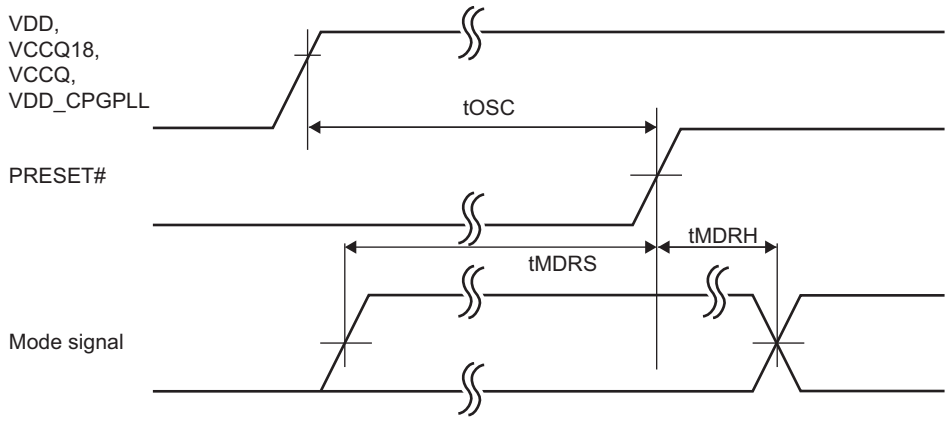
51.5 Clock and Reset Timings

Table 51.5.1 Clock and Reset Timings

Conditions: VCCQ = 3.3 V ± 0.3 V, VCCQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = -40 to +115 °C

Pin	Item	Symbol	Min.	Max.	Unit	Figures
PRESET#, EXTAL	Power-on oscillation settling time	tOSC	20	—	ms	Figure 51.5.1
Mode signal*	MD reset setup time	tMDRS	20	—	ms	
Mode signal*	MD reset hold time	tMDRH	3	—	ns	

Note: * MDn (n = 0, 1, 2, ...) and MDT[1:0]. For details of mode signals, refer to section 3.2, Mode Pin Settings.



Note for PRESET# input
1. Note electromagnetic noise because that may cause malfunctions of the LSI.
2. Note an intermediate voltage level input because that may influence the long-term reliability of the LSI.

Figure 51.5.1 Reset when Turning on Power Supply

51.6 LBSC

51.6.1 Normal Read/Write, Burst ROM Read and DMA Access

Table 51.6.1 Normal Read/Write Access Timing

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address output delay time	tDA	0.0	—	6.0	ns	Figure 51.6.1
CS# output delay time	tDCS	0.0	—	6.0	ns	
BS# output delay time	tDBS	0.0	—	6.0	ns	
RD# output delay time	tDRD	0.0	—	6.0	ns	
RD/WR# output delay time	tDRW	0.0	—	6.0	ns	
Read data setup time	tSD	11.0	—	—	ns	
Read data hold time	tHD	0.0	—	—	ns	
WE# output delay time	tDWE	0.0	—	6.0	ns	
Write data output delay time	tDD	0.0	—	6.0	ns	
External wait signal setup time	tSEW	11.0	—	—	ns	
External wait signal hold time	tHEW	0.0	—	—	ns	

Table 51.6.2 Burst ROM Read Access Timing

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Address output delay time	tDABST	0.0	—	6.0	ns	Figure 51.6.2
CS# output delay time	tDCSBST	0.0	—	6.0	ns	
RD# output delay time	tDRDBST	0.0	—	6.0	ns	
Read data setup time	tSDBST	11.0	—	—	ns	
Read data hold time	tHDBST	0.0	—	—	ns	

Table 51.6.3 DMA Signal Access Timing

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 40 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
DMA transfer request signal setup time	tSDRQ	11.0	—	—	ns	Figure 51.6.3
DMA transfer request signal hold time	tHDRQ	0.0	—	—	ns	
Delay time for DMA transfer end acknowledge signal output	tDDAK	0.0	—	6.0	ns	
Delay time for DMA acceptance signal output	tDDRK	0.0	—	6.0	ns	

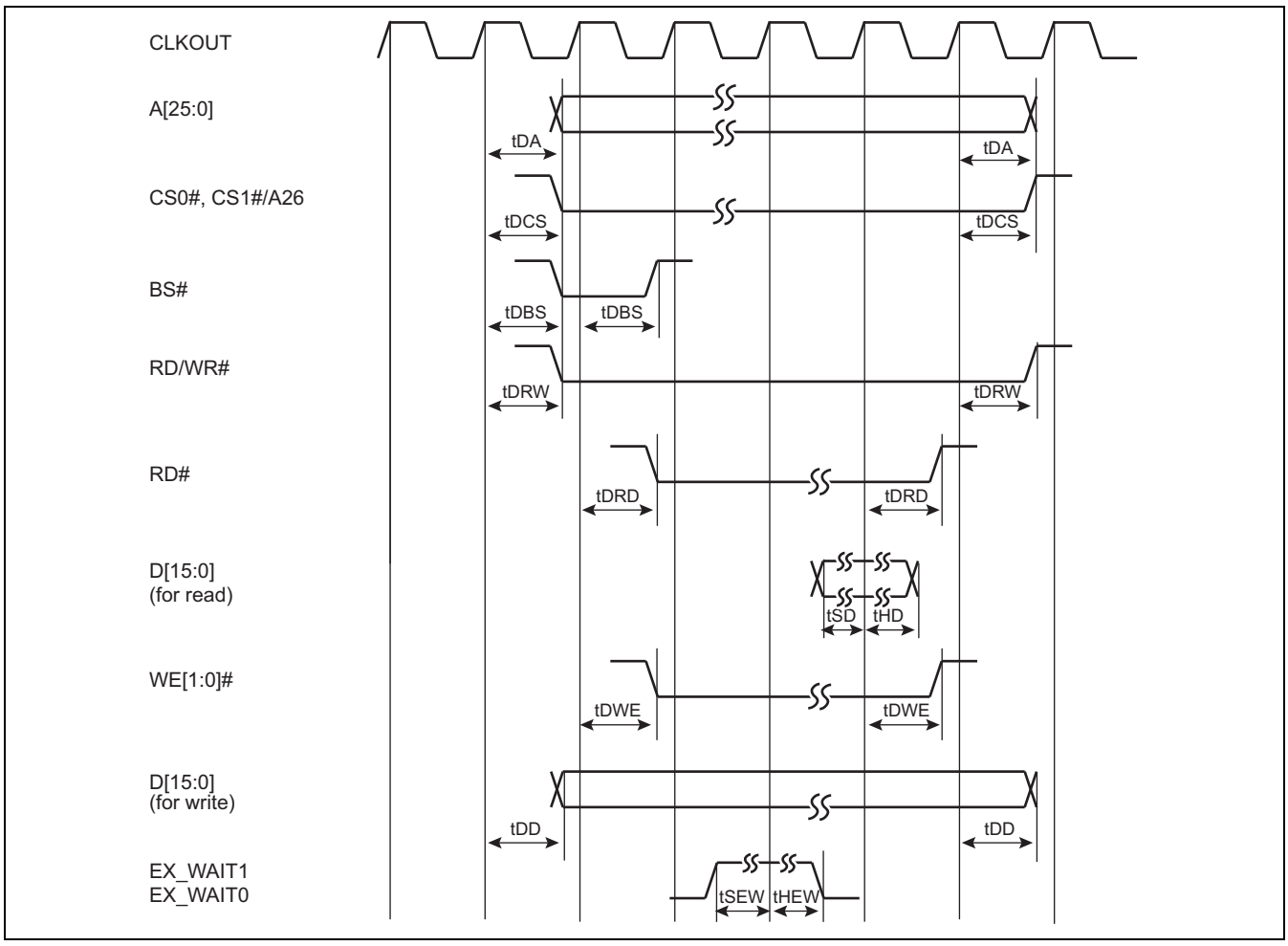


Figure 51.6.1 Normal Read/Write Access Timing

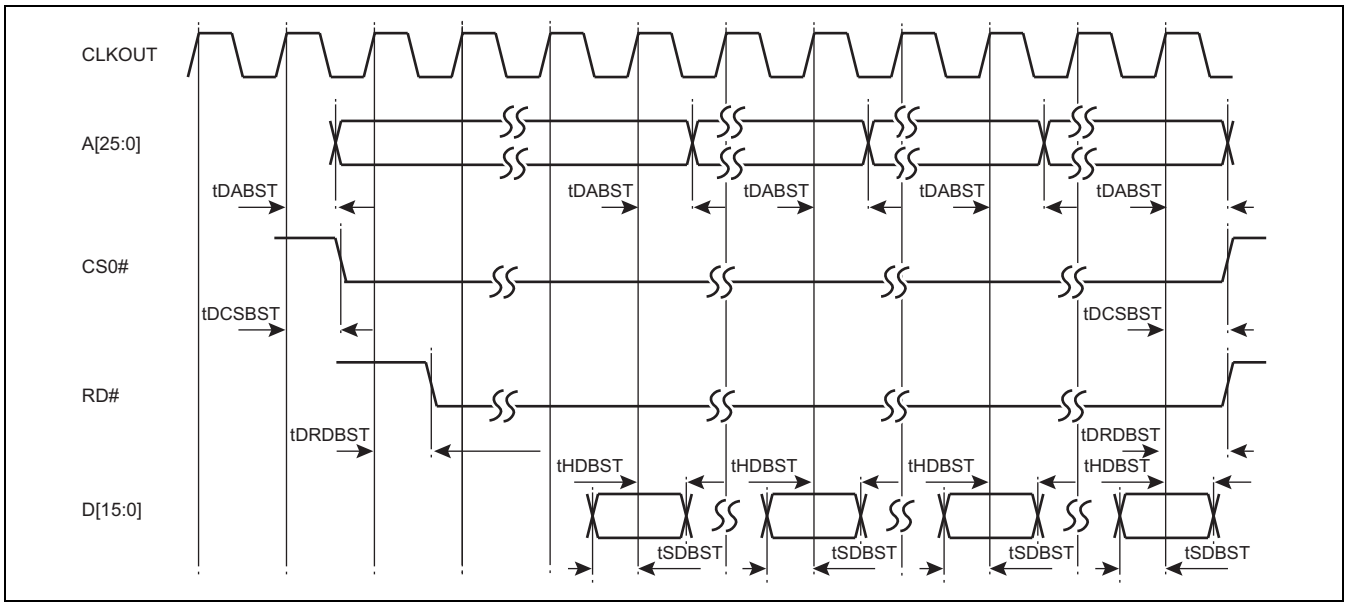


Figure 51.6.2 Burst ROM Read Access Timing

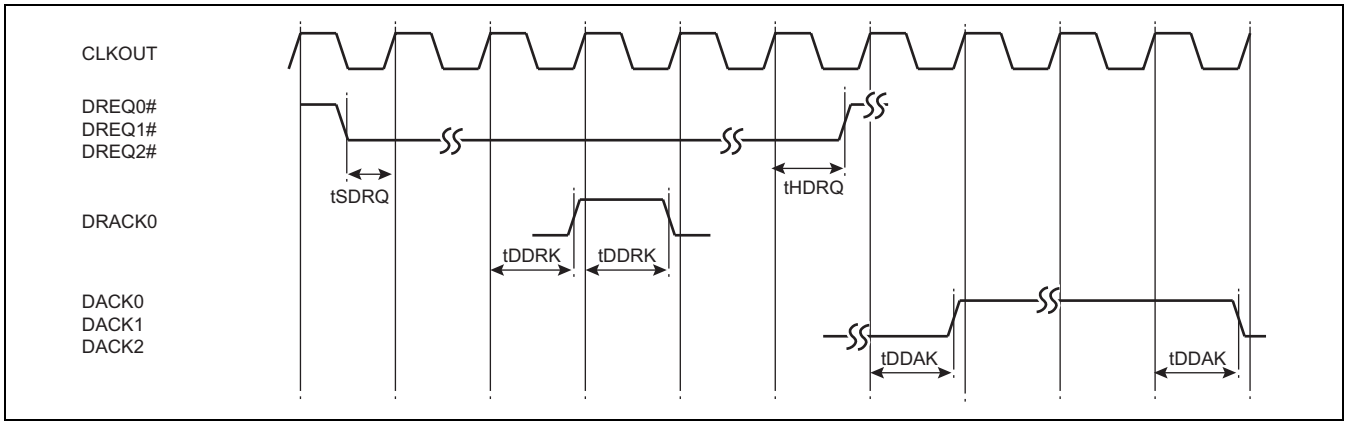


Figure 51.6.3 DMA Signal Access Timing

51.7 DBSC3 Access Timing

Table 51.7.1 DBSC3 Access Timing (DDR3)

Conditions: VDDQ_M0 = 1.5 V ± 0.075 V, GND = VSS = 0 V, Tc = –40 to +115 °C

Item	Symbol	Min.	Max.	Unit	Figure	Remarks
MCK average clock period	tCK(avg)	2.000	2.500	ns	Figure 51.7.2	
MCK absolute high pulse width	tCH(abs)	0.44	0.56	tCK(avg)	Figure 51.7.2	*1
MCK absolute low pulse width	tCL(abs)	0.44	0.56	tCK(avg)	Figure 51.7.2	*1
Command and Address output setup time to MCK, MCK#	tOS(1T)	520	—	ps	Figure 51.7.3	*1
	tOS(2T)	1500	—	ps		*1
Command and Address output hold time from MCK, MCK#	tOH(1T)	520	—	ps	Figure 51.7.3	*1
	tOH(2T)	520	—	ps		*1
Control and Address pulse width for each output	tOPW(1T)	0.8	—	tCK(avg)	Figure 51.7.3	*1
	tOPW(2T)	1.5	—	tCK(avg)		*1
Write Latency	WL	CWL	—	tCK(avg)	Figure 51.7.4	
MDQS, MDQS# rising edge to MCK, MCK# rising edge (write)	tWDQSS	-0.18	0.18	tCK(avg)	Figure 51.7.4	*1
MDQS, MDQS# falling edge setup time to MCK, MCK# rising edge (write)	tWDSS	0.27	—	tCK(avg)	Figure 51.7.4	*1
MDQS, MDQS# falling edge hold time from MCK, MCK# rising edge (write)	tWDSH	0.27	—	tCK(avg)	Figure 51.7.4	*1
MDQS, MDQS# differential high pulse width (write)	tWDQSH	0.45	0.55	tCK(avg)	Figure 51.7.5	*1
MDQS, MDQS# differential low pulse width (write)	tWDQSL	0.45	0.55	tCK(avg)	Figure 51.7.5	*1
MDQS, MDQS# differential WRITE Preamble (write)	tWPRE	0.9	—	tCK(avg)	Figure 51.7.5	*1
MDQS, MDQS# differential WRITE Postamble (write)	tWPST	0.3	—	tCK(avg)	Figure 51.7.5	*1
MDQ and MDM output setup time to MDQS, MDQS# (write)	tWDS	260	—	ps	Figure 51.7.6	*1
MDQ and MDM output hold time from DQS, DQS# (write)	tWDH	250	—	ps	Figure 51.7.6	*1
MDQ and MDM output pulse width for each output (write)	tWDIPW	0.35	—	tCK(avg)	Figure 51.7.6	*1
Read latency	RL	CL	—	tCK(avg)	Figure 51.7.7	
MDQS, MDQS# rising edge input access time from rising MCK, MCK# (read)	tRDQSCK	-300	1450	ps	Figure 51.7.7	*1
MDQS, MDQS# differential input high pulse width (read)	tRQSH	0.375	0.625	tCK(avg)	Figure 51.7.8	*1
MDQS, MDQS# differential input low pulse width (read)	tRQSL	0.375	0.625	tCK(avg)	Figure 51.7.8	*1
MDQS, MDQS# differential READ Preamble (read)	tRPRE	0.9	—	tCK(avg)	Figure 51.7.8	*1
MDQS, MDQS# differential READ Postamble (read)	tRPST	0.3	—	tCK(avg)	Figure 51.7.8	*1
MDQS, MDQS# to MDQ skew, per group, per access (read)	tRDQSQ	—	190	ps	Figure 51.7.9*2	*1

Item	Symbol	Min.	Max.	Unit	Figure	Remarks
MDQ input hold time from MDQS, MDQS# (read)	tRQH	0.35	—	tCK(avg)	Figure 51.7.9*2	*1

Notes: The signal timing is based on the following electric potential:
For MCK output, MDQS input/output: Differential input/output cross point voltage
For MDQ input: MVREF
For outputs other than MCK or MDQS: 0.5 × VDDQ_M0

1. Each timing specification are defined by assuming to connect DDR3-1333Mbps memory products
2. tWDQSH, tWDQSL specification are defined to guarantee operating with DDR-1333Mbps or DDR3-1600Mbps memory products which follows JEDEC JESD79-3E standards. (refer to Table 51.7.2 below)

   Minimum value of tWDQSH, tWDQSL can be calculated by using tCK(avg) according to either 1500ps (with min clock period of DDR3-1333Mbps product) or 1250ps (with min clock period of DDR3-1600Mbps product)

   Maximum value of tWDQSH, tWDQSL can be calculated by using tCK(avg) as 2500ps (with max clock period of both DDR3-1333Mbps and DDR3-1600Mpbs product)

Table 51.7.2 tDQSH/tDQSL Standard Specification of DDR3-1333Mbps/1600Mbps Products

			1333 Mbps		1600 Mbps	
Item	Symbol	Unit	Min.	Max.	Min.	Max.
MCK average clock period	tCK(avg)	ns	1.5	2.5	1.25	2.5
MDQS High/Low pulse width (Write)	tWDQSH/ tWDQSL	tCK(avg)	0.45	0.55	0.45	0.55
		ns	0.675	1.375	0.563	1.375

- Reference Load and VTT Termination of AC Timing

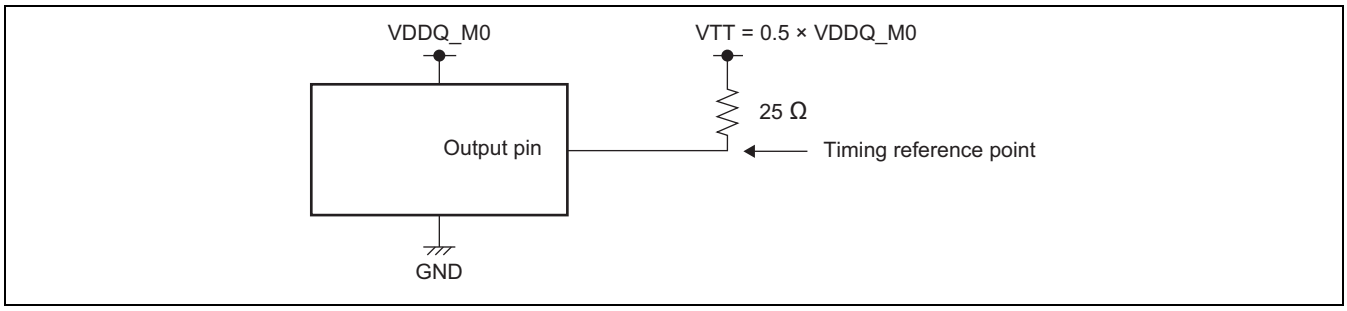


Figure 51.7.1 Reference Load for AC Timing

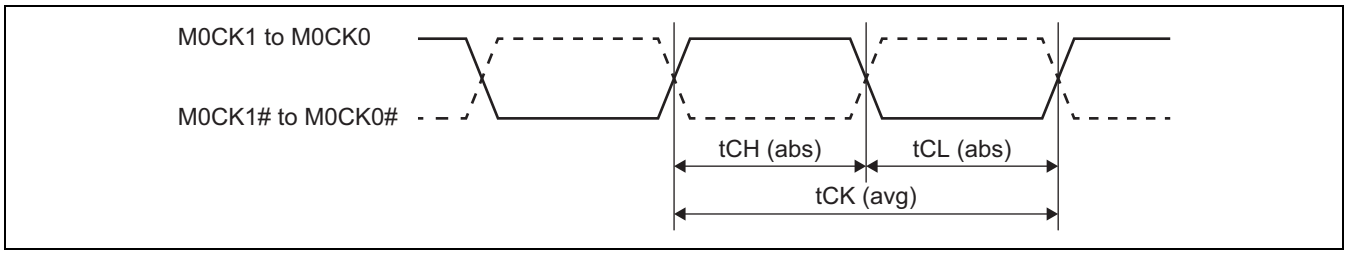


Figure 51.7.2 MCK Clock Output

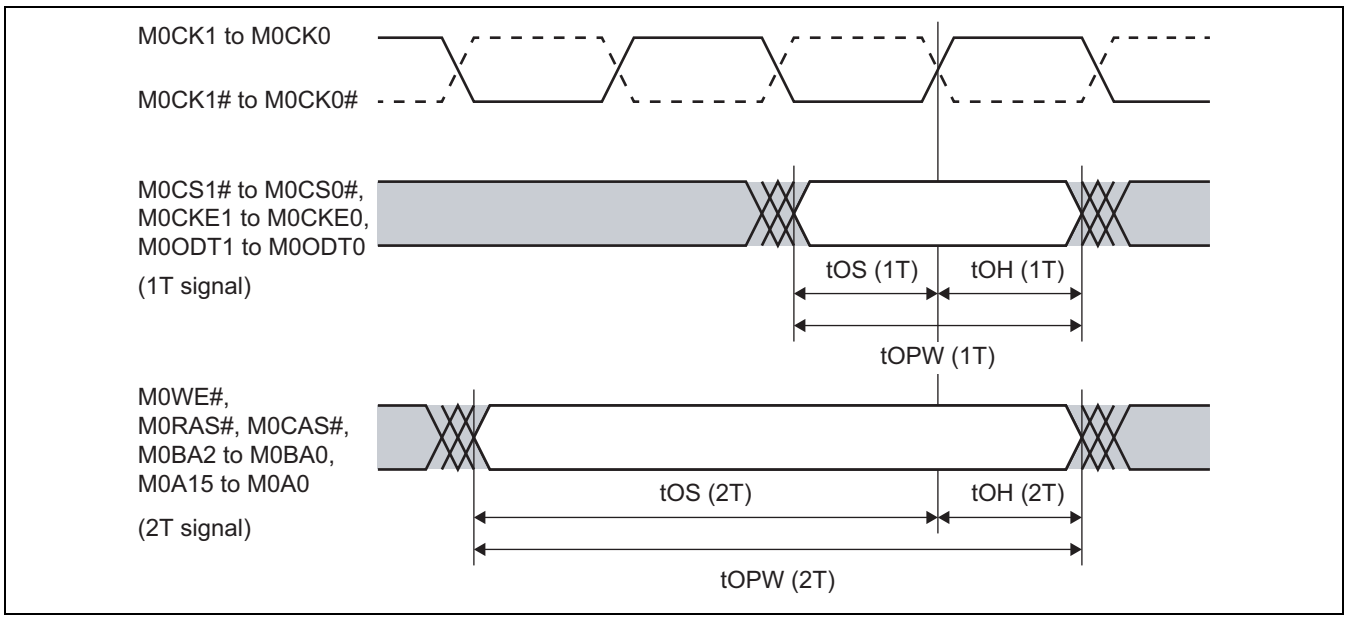


Figure 51.7.3 Address and Command Output Timing relative to MCK Output

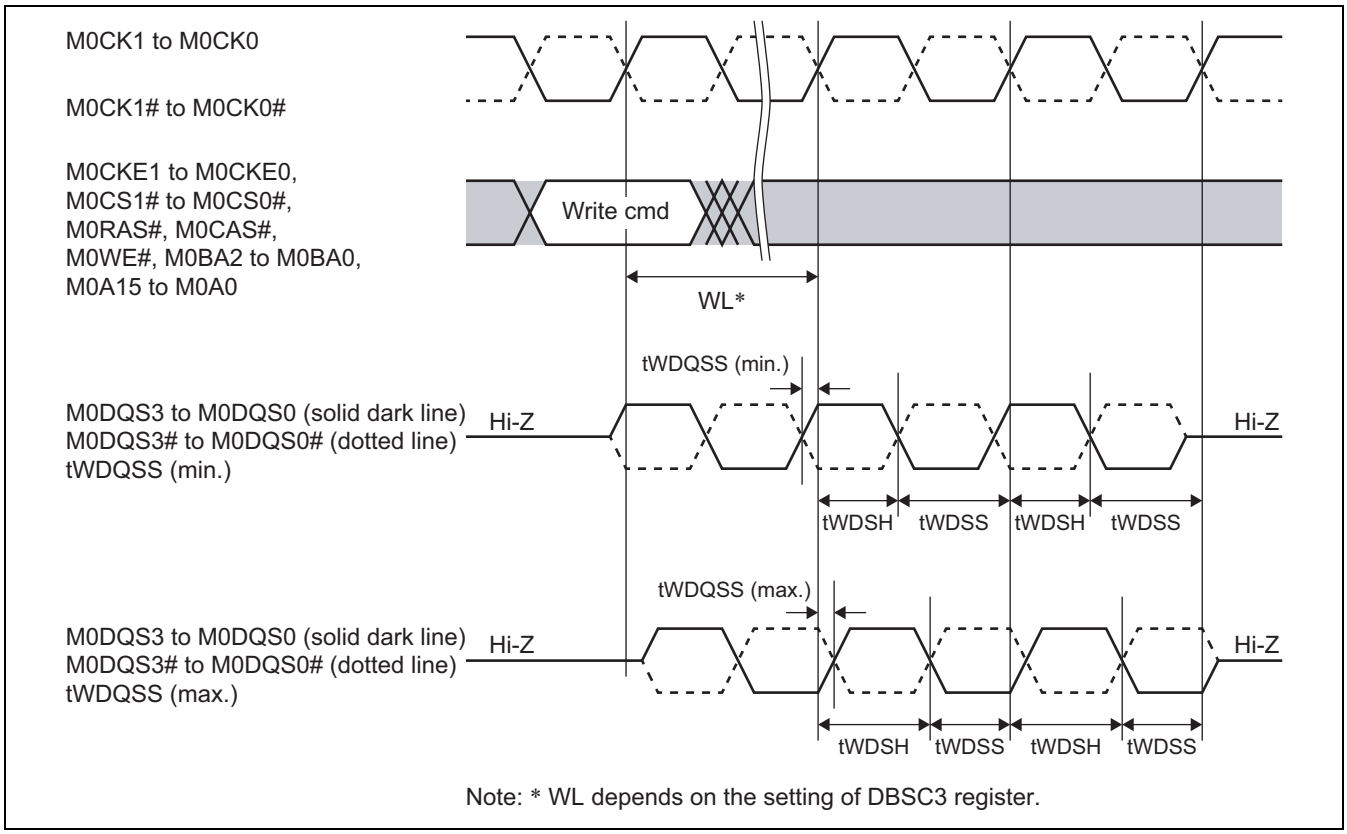


Figure 51.7.4 MDQS Output Timing relative to MCK Output (write)

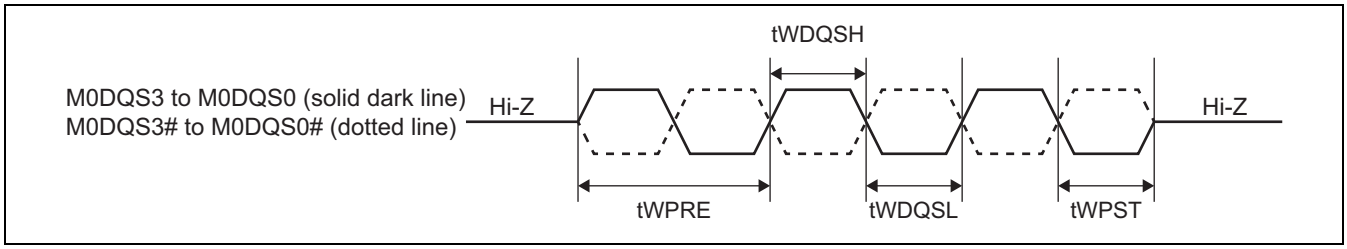


Figure 51.7.5 MDQS Output Timing (write)

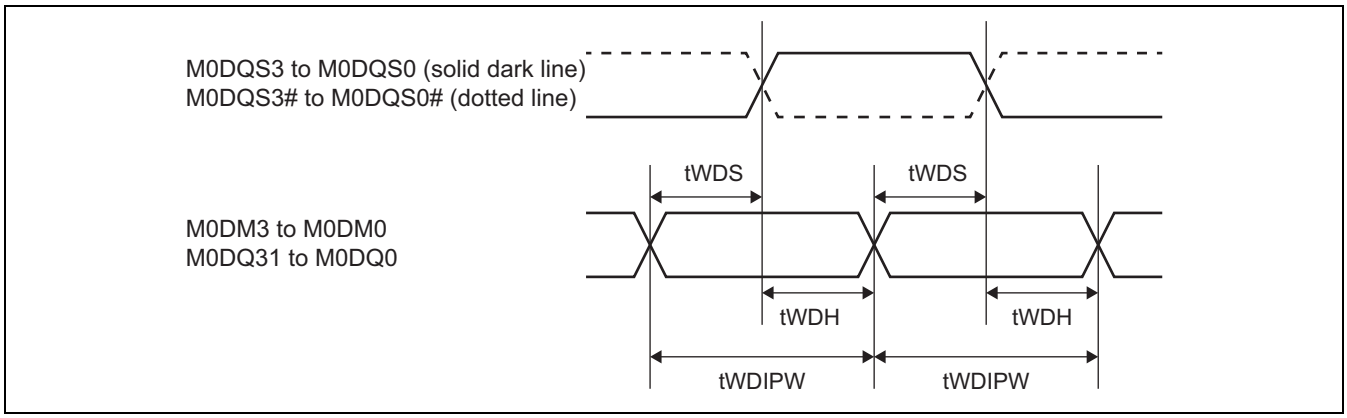


Figure 51.7.6 MDQ/MDM Output Timing relative to MDQ (write)

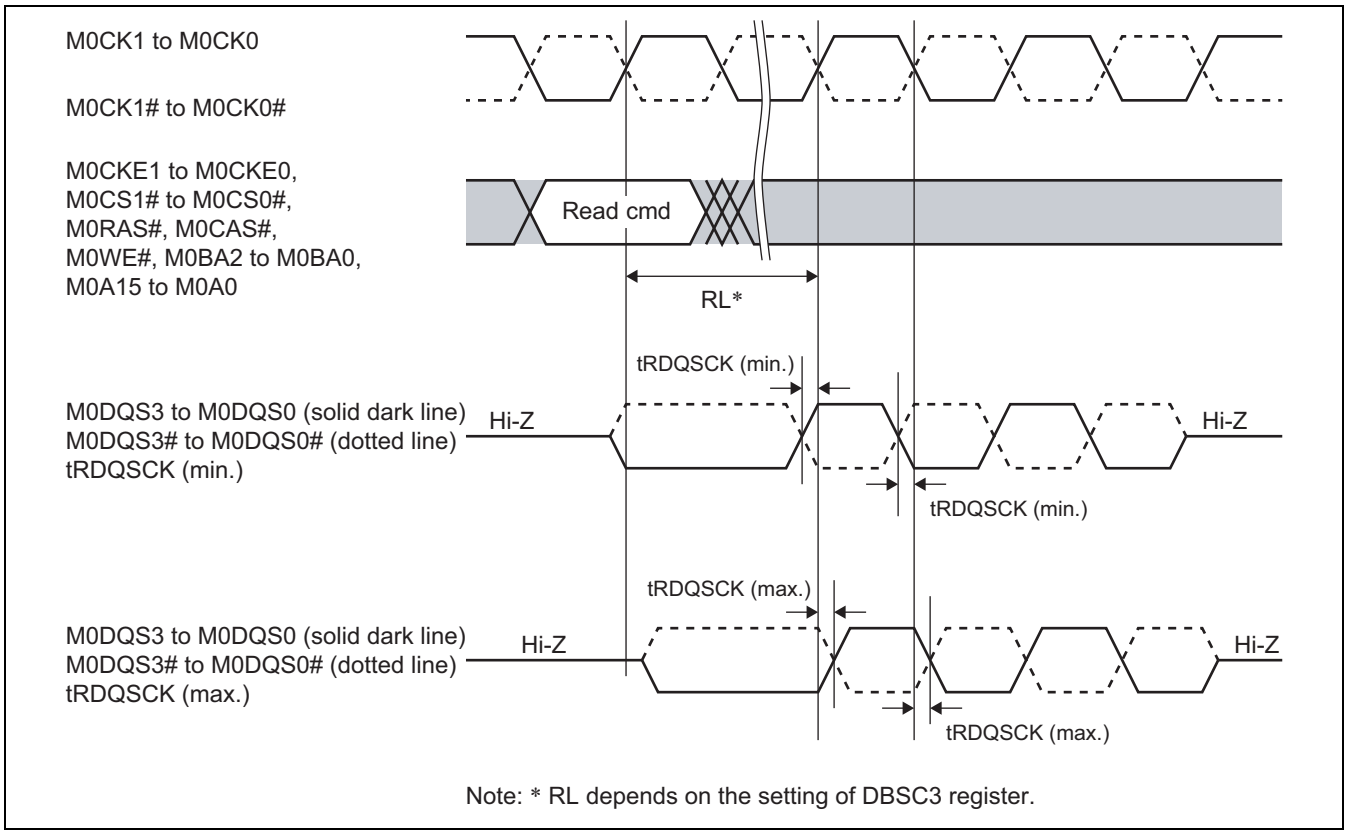


Figure 51.7.7 MDQS Input Timing relative to MCK Output (read)

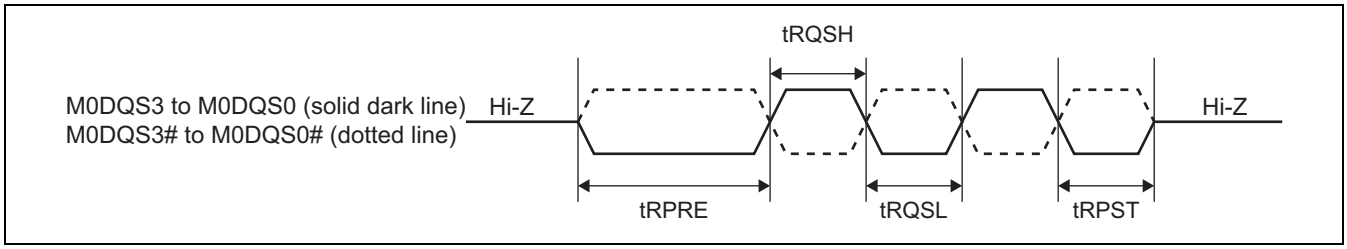


Figure 51.7.8 MDQS Input Timing (read)

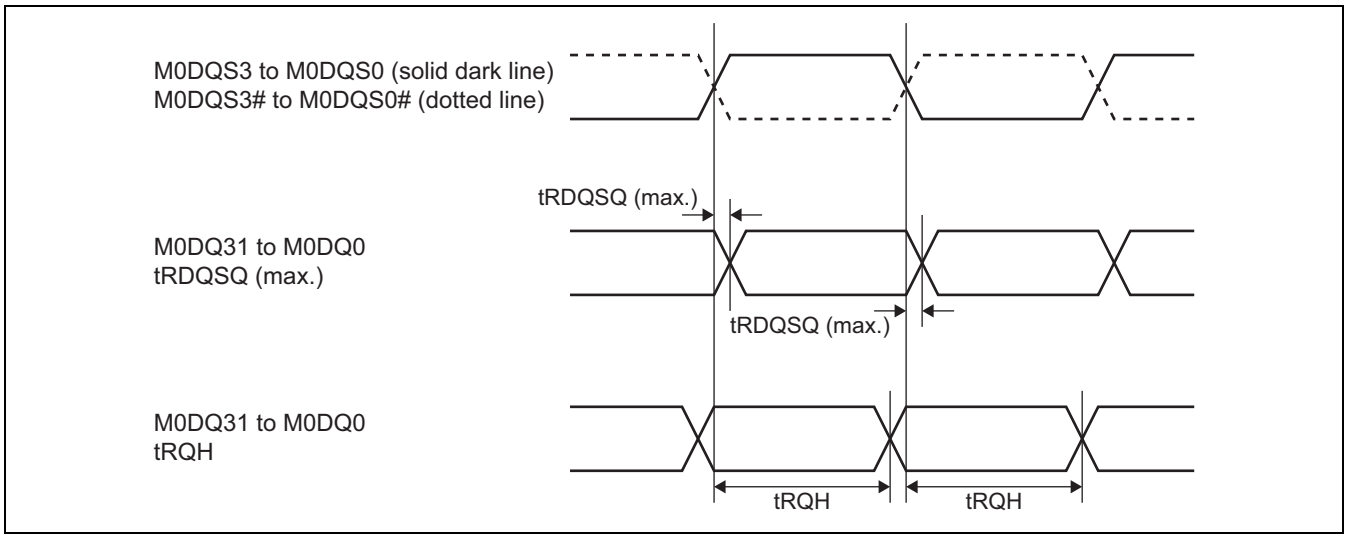


Figure 51.7.9 MDQ Input Timing relative to MDQS (read)

51.8 Display Unit (DU)

Table 51.8.1 DOTCLKIN Timing

Conditions: VCCQ = VCCQ_SD2 = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc= −40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
DOTCLKIN cycle time	tDICYC	10	—	200	ns	Figure 51.8.1
DOTCLKIN High level time	tDCKIH	3	—	—	ns	
DOTCLKIN Low level time	tDCKIL	3	—	—	ns	

Table 51.8.2 Display Signal Timing

Conditions: VCCQ = VCCQ_SD2 = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 20 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Display input control signal*1 setup time	tDS1	5	—	—	ns	Figure 51.8.2 (relative to DOTCLKIN)
Display input control signal*1 hold time	tDH1	3	—	—	ns	
DOTCLKOUT output cycle time	tDCYC	10	—	200	ns	Figure 51.8.3 (relative to DOTCLKOUT)
DOTCLKOUT output high level width	tDCKH	2	—	—	ns	
Display input control signal*1 setup time*2	tDS2	13	—	—	ns	
Display input control signal*1 hold time*2	tDH2	-6	—	—	ns	
Display output control signal*1 output delay time	tDD	2	—	8.5	ns	
Display digital data*1 output delay time	tDD	2	—	8.5	ns	
Display digital data 2*1 output delay time*3	tDD2	2	—	8.5	ns	
EXHSYNC# input low level width	tEXHLW	4tDCYC	—	—	ns	Figure 51.8.4
EXHSYNC# input high level width	tEXHHW	4tDCYC	—	—	ns	
EXVSYNC# input low level width	tEXVLW	3HC	—	—	tDCYC	
ODDF# setup time 1*4	tOD1	(ys+yw) × HC	—	—	tDCYC	
ODDF# setup time 2*4	tOD2	1HC	—	—	tDCYC	

Notes: 1. For correspondence between these signals and pin names, refer to Table 51.8.3.
2. Clock signal is input from DOTCLKIN and then output from DOTCLKOUT without being frequency-divided.
3. This electrical characteristic is applicable when the DR0D bit (bit 21) in the display output control register (DORCR) is set to 1. When the DR1D bit is cleared to 0, this characteristic is the same as the display digital data output delay time (tDD). Min value of tDCYC will be twice. This electrical characteristic applies to only DU0 output.
4. ys, yw and HC in Min value of ODDF# setup time 1 and ODDF# setup time 2 (tOD1 and tOD2);
ys: From rise of VSYNC to display start position in the vertical direction of the display screen (unit: raster line)
yw: Vertical display period of display screen (unit: raster line)
HC: Horizontal scan period (unit: dot clock).

Table 51.8.3 Correspondence between Signals in Notes and Pin Names

Signal in Note	Pin Name
Display input control signals	DU*_EXVSYNC/DU*_VSYNC
	DU*_EXHSYNC/DU*_HSYNC
	DU*_EXODDF/DU*_ODDF/DISP/CDE
Display output control signals	DU*_EXVSYNC/DU*_VSYNC
	DU*_EXHSYNC/DU*_HSYNC
	DU*_EXODDF/DU*_ODDF/DISP/CDE
	DU*_DISP
	DU*_CDE
Display digital data/display digital data 2	DU*_DR7(_Yn_DATAm)
	DU*_DR6(_Yn_DATAm)
	DU*_DR5(_Yn_DATAm)
	DU*_DR4(_Yn_DATAm)
	DU*_DR3(_Yn_DATAm)
	DU*_DR2(_Yn_DATAm)
	DU*_DR1(_Yn_DATAm)
	DU*_DR0(_Yn_DATAm)
	DU*_DG7(_C/Yn_DATAm)
	DU*_DG6(_C/Yn_DATAm)
	DU*_DG5(_C/Yn_DATAm)
	DU*_DG4(_C/Yn_DATAm)
	DU*_DG3(_C/Yn_DATAm)
	DU*_DG2(_C/Yn_DATAm)
	DU*_DG1(_C/Yn_DATAm)
	DU*_DG0(_C/Yn_DATAm)
	DU*_DB7(_Cn_DATAm)
	DU*_DB6(_Cn_DATAm)
	DU*_DB5(_Cn_DATAm)
	DU*_DB4(_Cn_DATAm)
	DU*_DB3(_Cn_DATAm)
	DU*_DB2(_Cn_DATAm)
	DU*_DB1(_Cn_DATAm)
	DU*_DB0(_Cn_DATAm)

Note: * Blank, 0, or 1; for details of pin name, refer to section 20, Display Unit (DU).

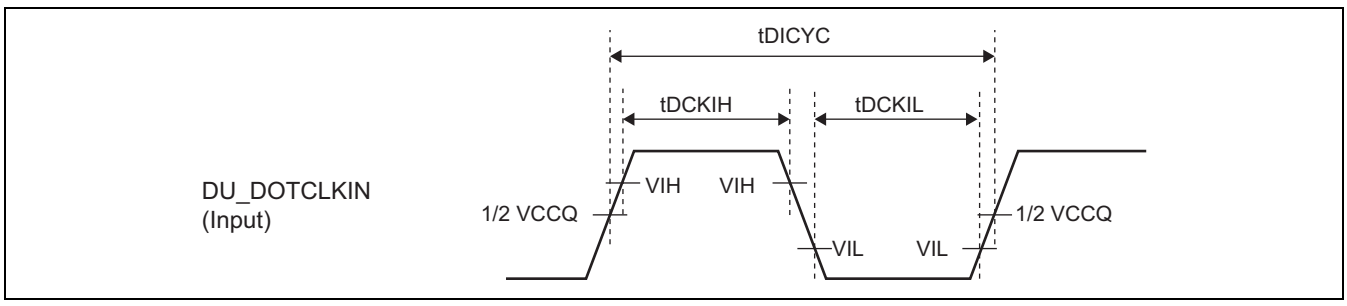
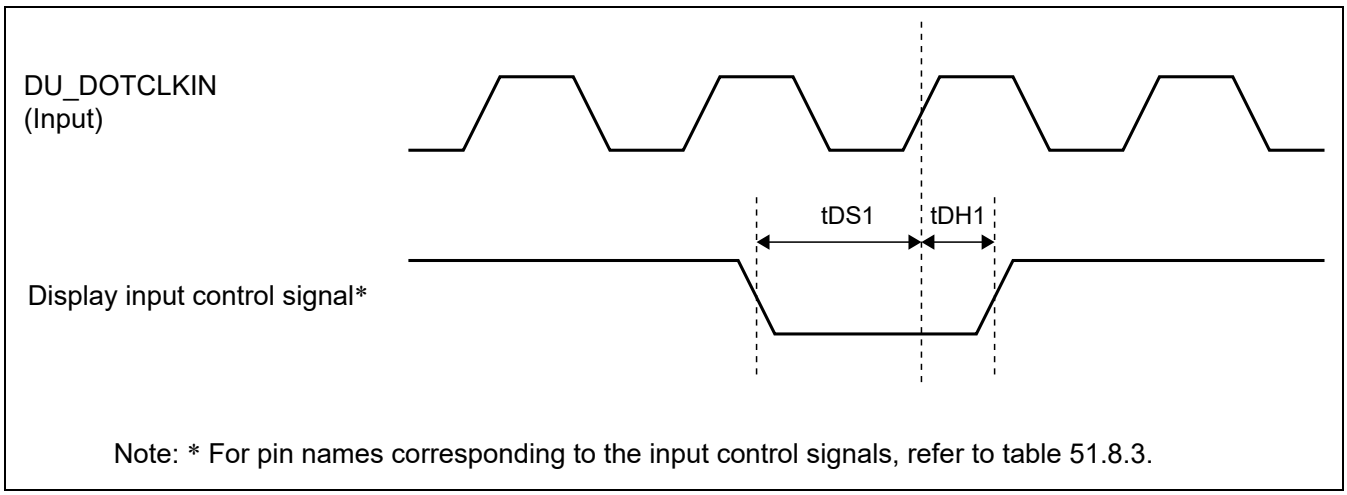
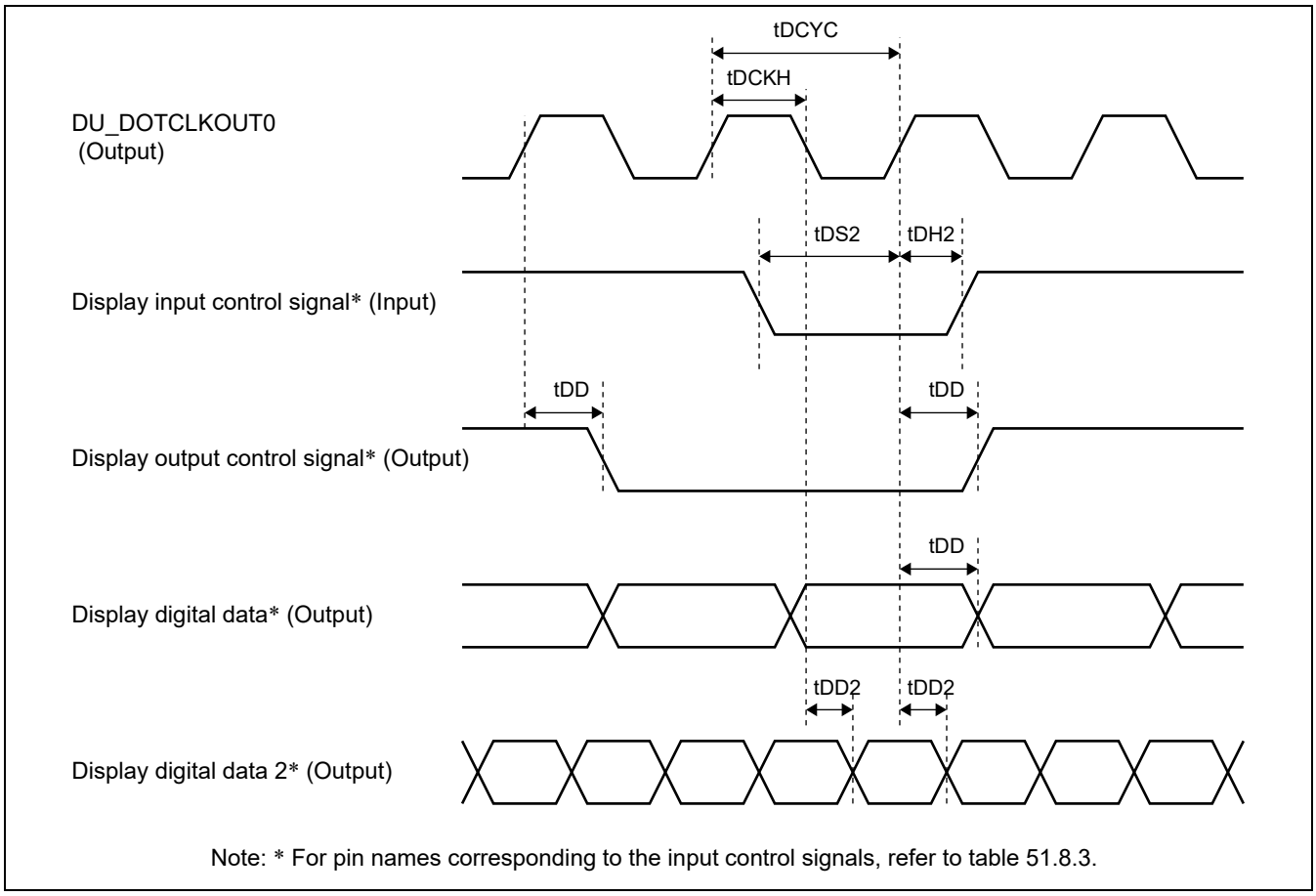


Figure 51.8.1 DOTCLKIN Clock Input Timing



Note: * For pin names corresponding to the input control signals, refer to table 51.8.3.

Figure 51.8.2 Display Signal Timing (Relative to DOTCLKIN)



Note: * For pin names corresponding to the input control signals, refer to table 51.8.3.

Figure 51.8.3 Display Signal Timing (Relative to DOTCLKOUT)

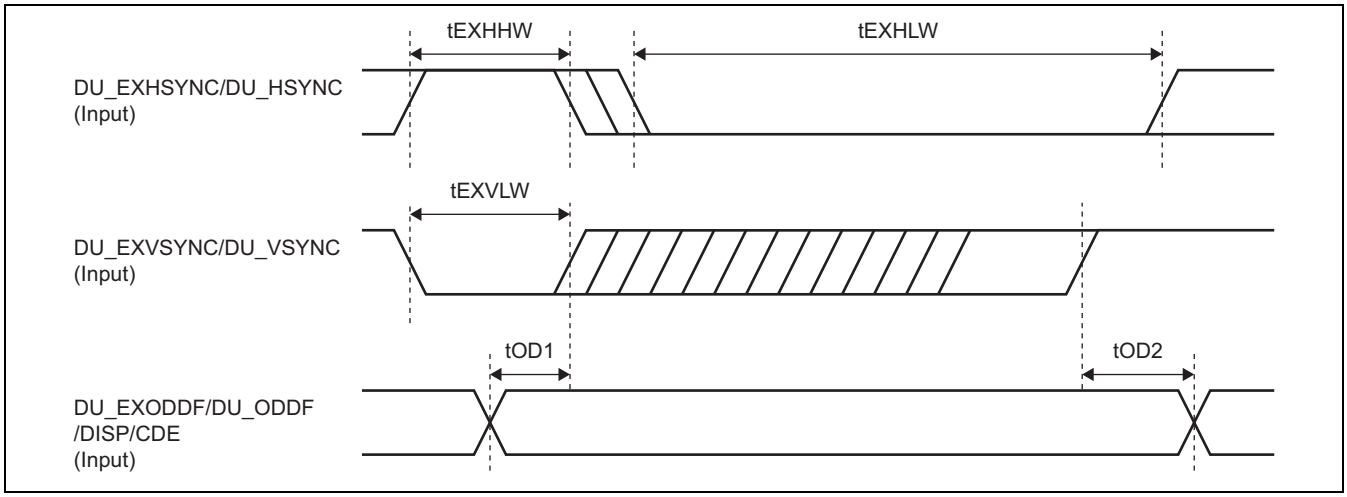


Figure 51.8.4 TV Sync Mode Display Signal Timing

51.9 LVDS

Table 51.9.1 LVDS Dot Clock Input Timing

Conditions: VCCQ = VCCQ_SD2 = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
DU_DOTCLKIN cycle time	tDICYC	11.5	—	32.0	ns	Figure 51.9.1
DU_DOTCLKIN high level width	tDCKIH	3.0	—	—	ns	
DU_DOTCLKIN low level width	tDCKIL	3.0	—	—	ns	

Table 51.9.2 LVDS Module Signal Timing

Conditions: VCCQA_LVDS = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 5 pF, RL = 100 Ω

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Data delay time (bit 0 data)	t0	2/7 tDCYC -0.20	—	2/7 tDCYC +0.20	ns	Figure 51.9.2
Data delay time (bit 1 data)	t1	3/7 tDCYC -0.20	—	3/7 tDCYC +0.20	ns	
Data delay time (bit 2 data)	t2	4/7 tDCYC -0.20	—	4/7 tDCYC +0.20	ns	
Data delay time (bit 3 data)	t3	5/7 tDCYC -0.20	—	5/7 tDCYC +0.20	ns	
Data delay time (bit 4 data)	t4	6/7 tDCYC -0.20	—	6/7 tDCYC +0.20	ns	
Data delay time (bit 5 data)	t5	7/7 tDCYC -0.20	—	7/7 tDCYC +0.20	ns	
Data delay time (bit 6 data)	t6	8/7 tDCYC -0.20	—	8/7 tDCYC +0.20	ns	

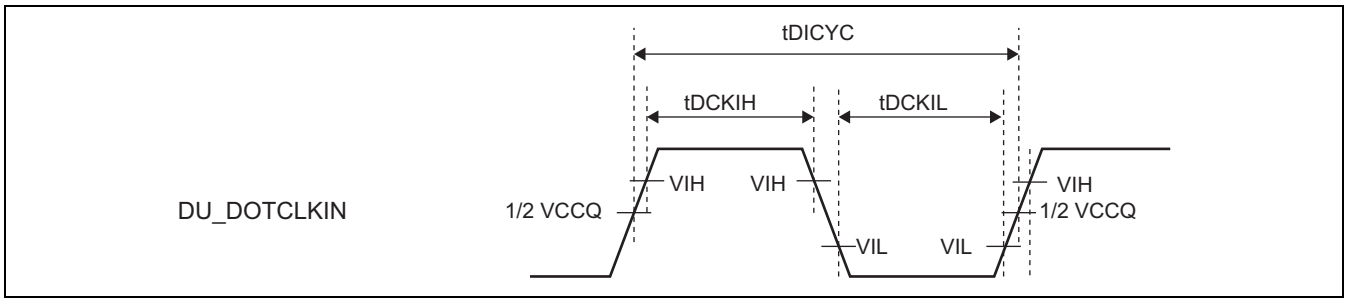


Figure 51.9.1 DU_DOTCLKIN Clock Input Timing

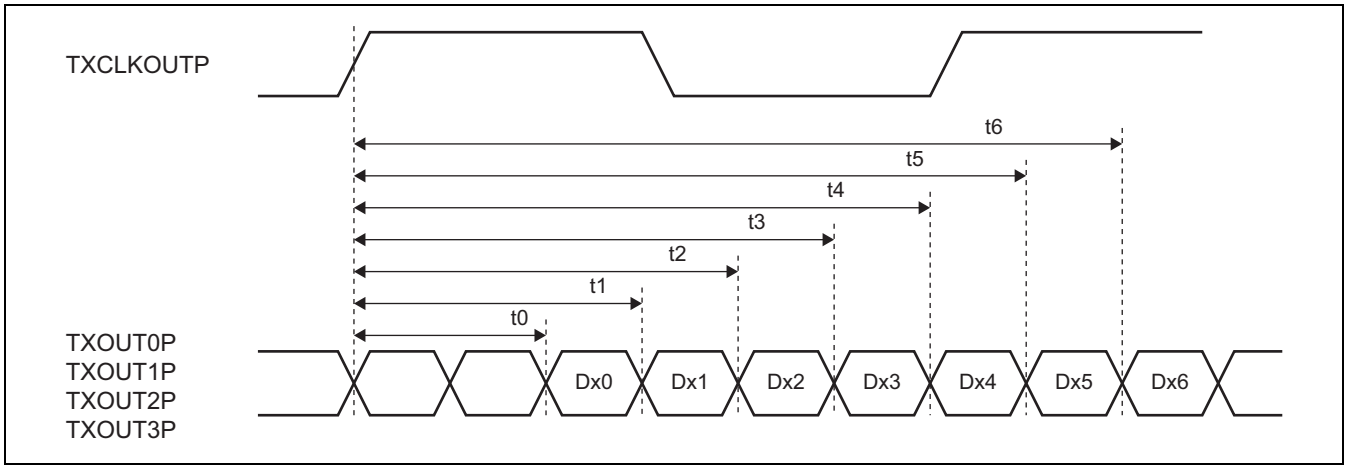


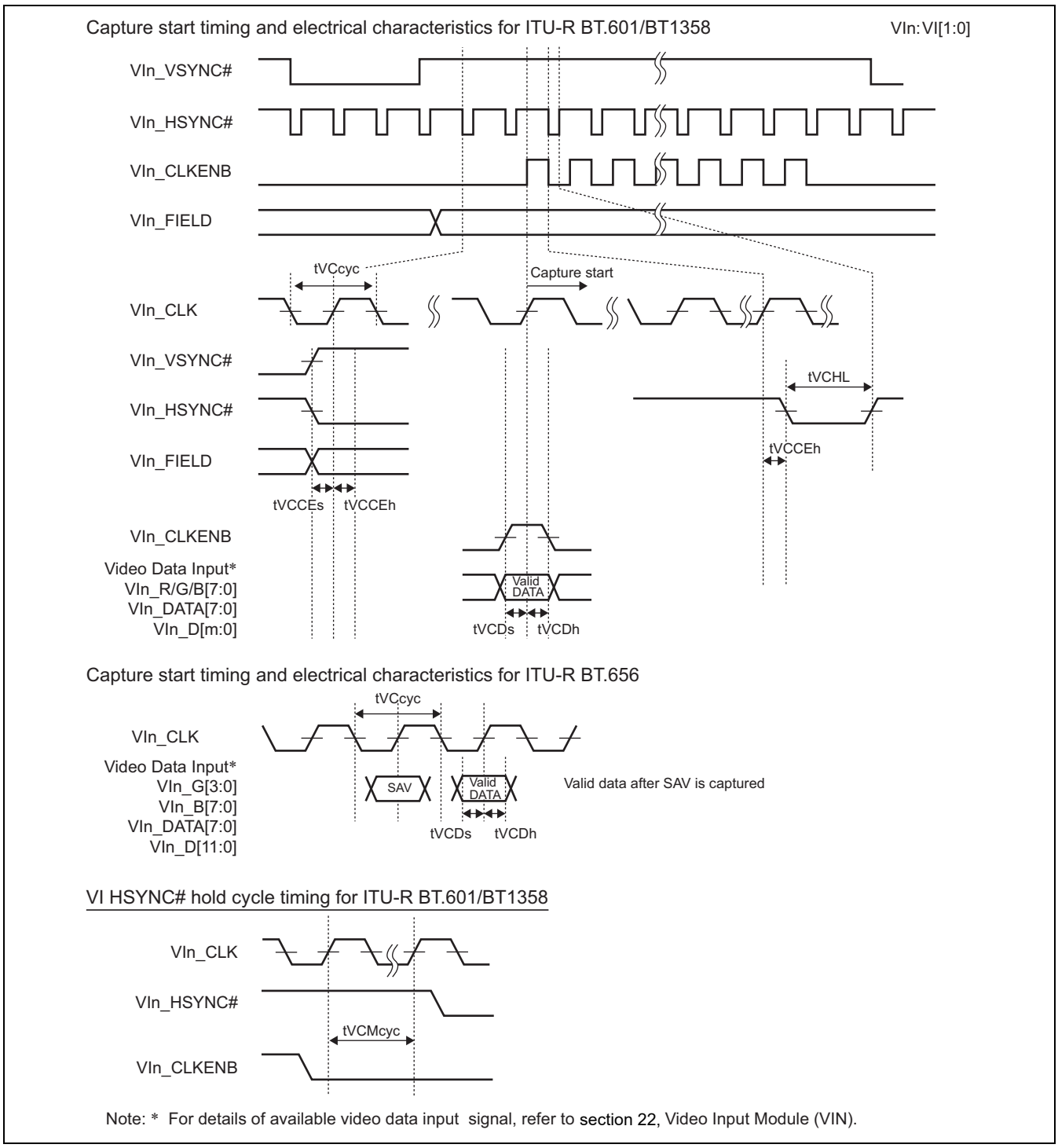
Figure 51.9.2 Display Output Timing

51.10 Video Input Module (VIN)

Table 51.10.1 VIN Signal Timing

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
VI_CLK cycle time	tVCcyc	10	37	—	ns	Figure 51.10.1
Data setup time	tVCDs	3.5	—	—	ns	
Data hold time	tVCDh	1.5	—	—	ns	
Sync signal setup time	tVCCEs	3.5	—	—	ns	
Sync signal hold time	tVCCEh	1.5	—	—	ns	
VI_HSYNC# hold cycle	tVCMcyc	8	—	—	tVCcyc	
VI_HSYNC# Low period	tVCHL	300	—	—	ns	



Note: * For details of available video data input signal, refer to section 22, Video Input Module (VIN).

Figure 51.10.1 Capture start timing and electrical characteristics

51.11 SSI Interface

Table 51.11.1 SSI Interface Signal Timing

Conditions: VCCQ = VCCQ_SD = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 30 pF (other than tRC: Rise-edge clock timing)

Item	Symbol	Min.	Typ.	Max.	Unit	Note	Figure
Output clock cycle	tO	80	—	15625	ns	—	Figure 51.11.1
Input clock cycle	tI	66	—	15625	ns	—	
Output clock high-cycle	tHC	35	—	—	ns	—	
Output clock low-cycle	tLC	35	—	—	ns	—	
Input clock high-cycle	tHC	28	—	—	ns	—	
Input clock low-cycle	tLC	28	—	—	ns	—	
Rise-edge clock timing	tRC	—	—	20	ns	Output (100 pF)	
Output delay	tD	−5	—	19	ns	—	Figures 51.11.2 to 51.11.5
	tD	—	—	22	ns	—	Figure 51.11.6
Setup time	tS	15	—	—	ns	—	Figures 51.11.2 to 51.11.6
Hold time	tH	5	—	—	ns	—	
Audio clock frequency	fAUDIO	3.072	—	25	MHz	—	Figure 51.11.7

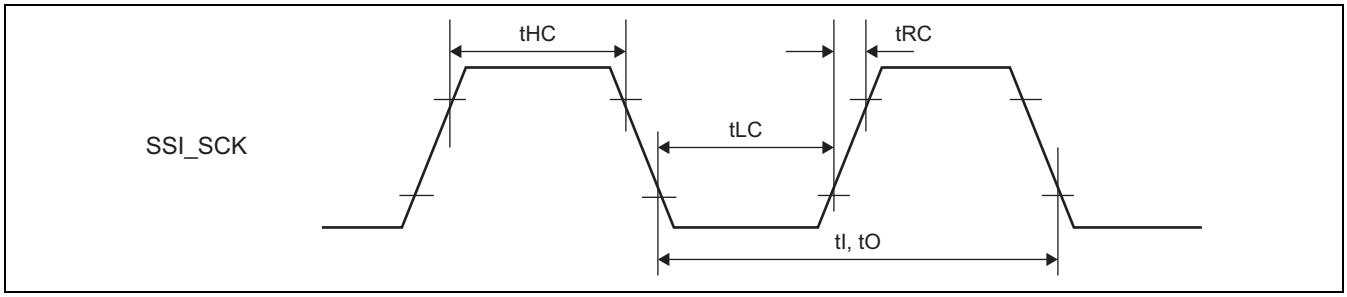


Figure 51.11.1 SCK Clock Input/output Timing

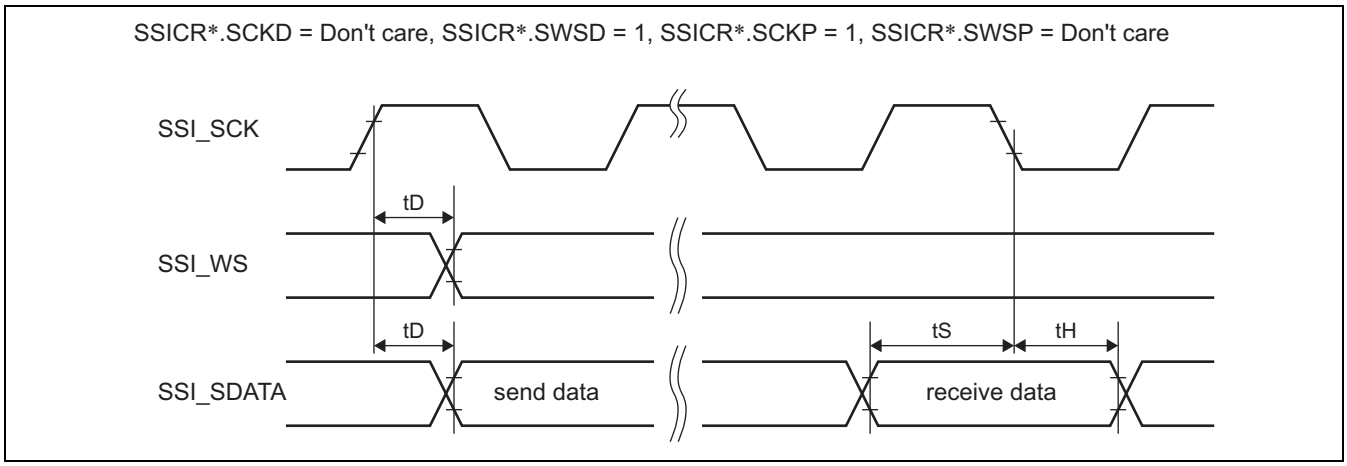


Figure 51.11.2 SSI Timing (1)

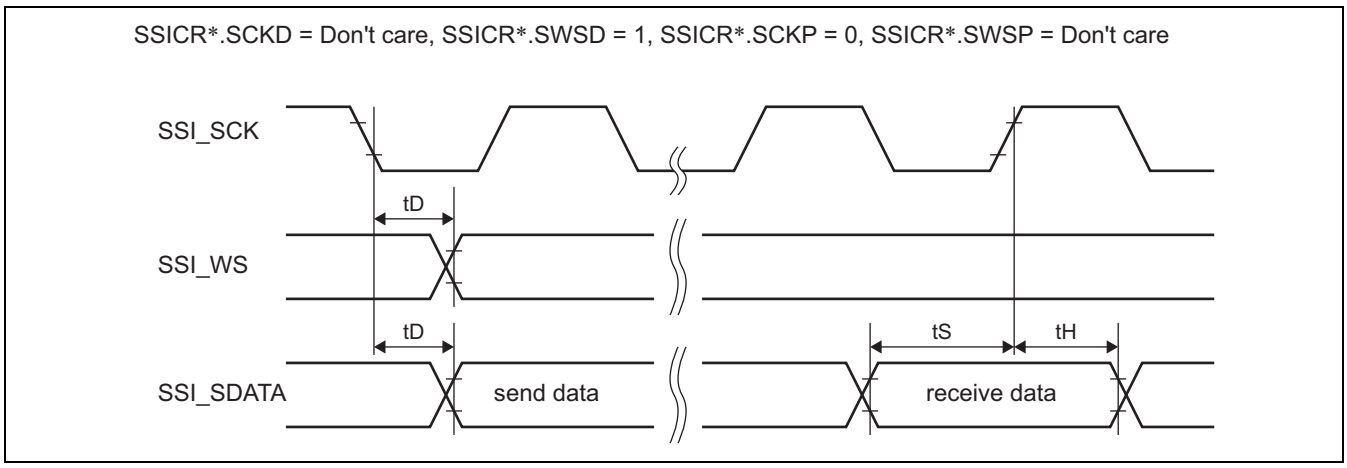


Figure 51.11.3 SSI Timing (2)

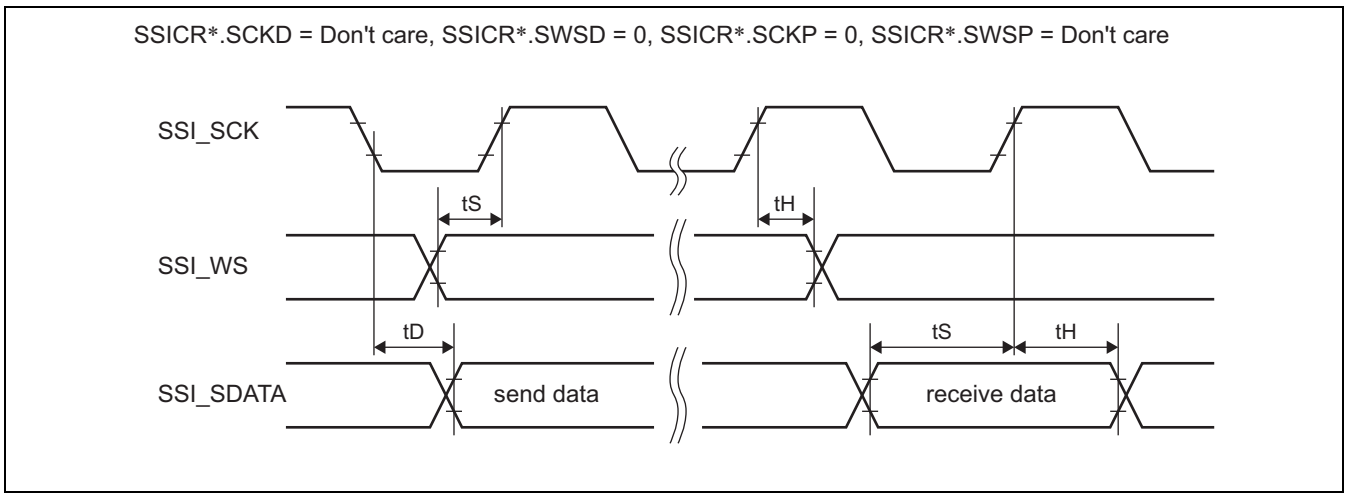


Figure 51.11.4 SSI Timing (3)

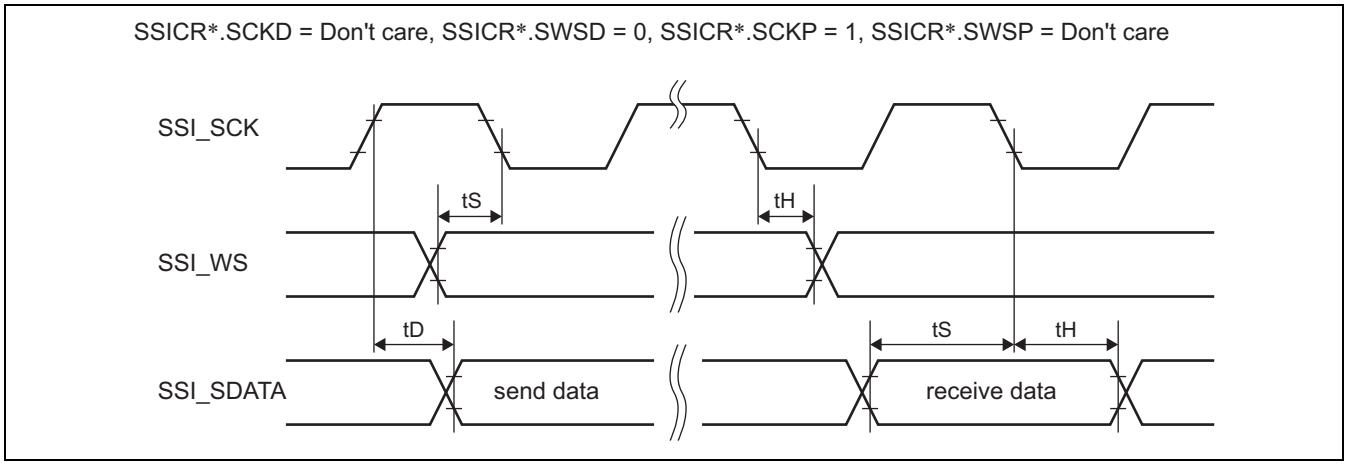


Figure 51.11.5 SSI Timing (4)

The follows are output timings of the MSB bit in the setting of the slave transmission by non-compression.
Send data is no padding bit with a left justify format or a right justify format.
SSICR*.SCKD=0, SSICR*.SWSD=0, SSICR*.DEL=1, SSICR*.TRMD=1
SSICR*.SDTA=0 or SSICR*.SDTA=1 and moreover SSICR*.SWL=SSICR*.DWL

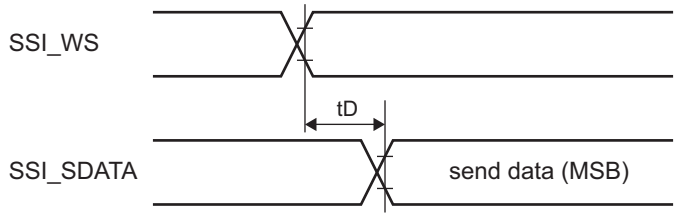


Figure 51.11.6 SSI Timing (5)

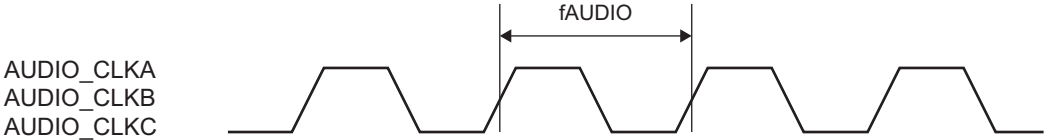


Figure 51.11.7 AUDIO_CLK Input Timing

51.12 Ethernet MAC Controller Signal Timing

Table 51.12.1 Ethernet MAC Controller Signal Timing (RMII)

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
ETH_REF_CLK clock input frequency	fRTcyc	50 – 50 ppm	—	50 + 50 ppm	MHz	Figure 51.12.1
ETH_TX_EN output delay time	tRTEND	2.5	—	12	ns	
ETH_TXD1, ETH_TXD0 output delay time	tRETDD	2.5	—	12	ns	
ETH_CRS_DV setup time	tRRDVS	4	—	—	ns	Figure 51.12.2
ETH_CRS_DV hold time	tRRDVH	2.5	—	—	ns	
ETH_RXD1, ETH_RXD0 setup time	tRERDS	4	—	—	ns	
ETH_RXD1, ETH_RXD0 hold time	tRERDH	2.5	—	—	ns	
ETH_RX_ER setup time	tRRERS	4	—	—	ns	Figure 51.12.3
ETH_RX_ER hold time	tRRERH	2.5	—	—	ns	

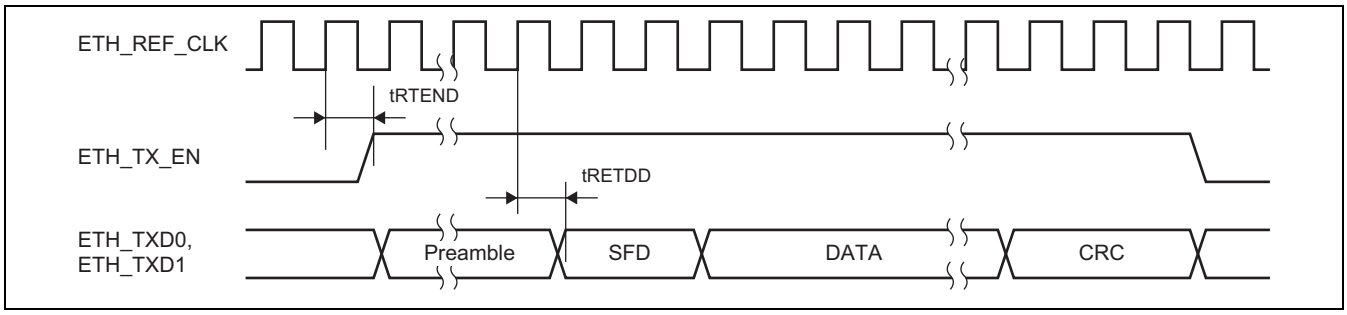


Figure 51.12.1 RMII Transmission Timing

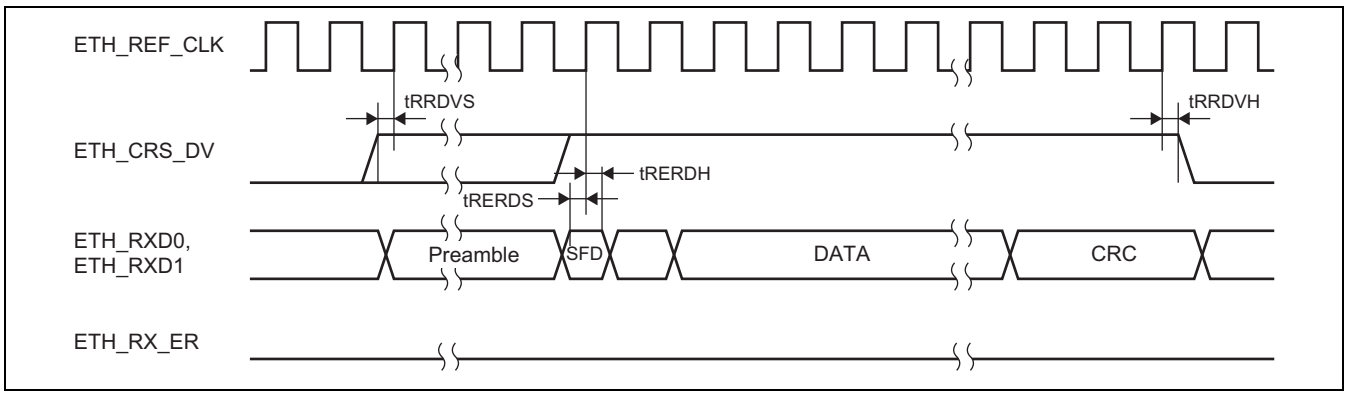


Figure 51.12.2 RMII Reception Timing (Normal Operation)

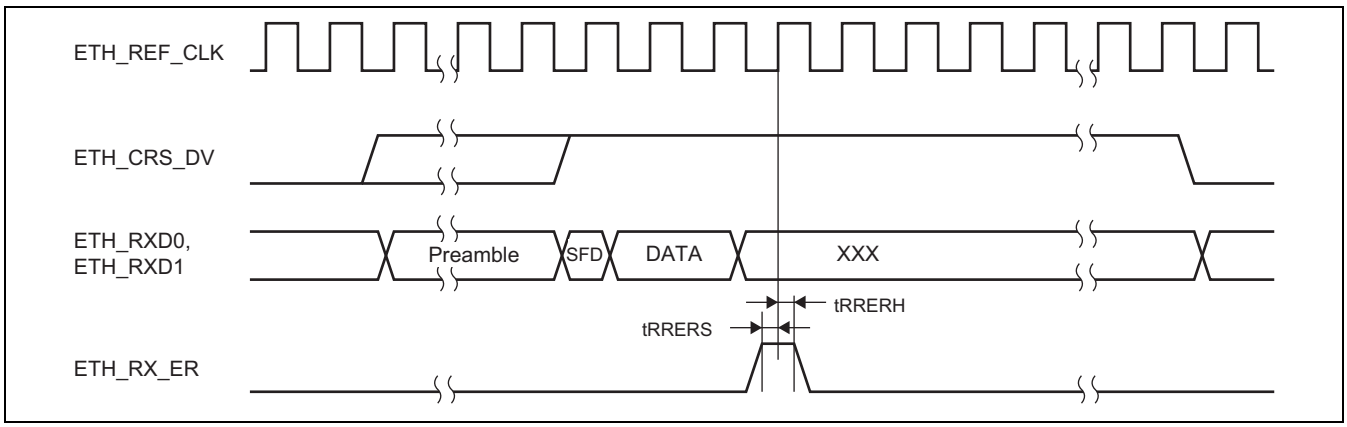


Figure 51.12.3 RMII Reception Timing (Case When Error Occurs)

(1) ETH_MDC timing specification (setup time and hold time)

Although ETH_MDC is a reference clock for the serial management interface (SMI), ETH_MDC input setup time and ETH_MDC input hold time are not specified.

(2) ETH_MDIO timing provision (setup time and hold time)

The AC specifications for the SMI (PHY side) from the IEEE are as follows:

ETH_MDC input cycle ≥ 400 ns.

ETH_MDC input pulse width at each level ≥ 160 ns

ETH_MDIO input setup and hold times ≥ 10 ns (PHY latches the MAC output on rising edges of ETH_MDC).

ETH_MDIO output delay time = 0 to 300 ns (delay time from a rising edge of ETH_MDC)

The ETH_MDC output, ETH_MDIO output, and ETH_MDIO input latching depend on software adjusting settings in the PHY interface register (PIR). Adjust the ETH_MDC output (period) and ETH_MDIO output (timing of changes) to satisfy the AC input specs on the PHY side. To adjust the timing of ETH_MDIO input latching, consider the AC output specifications on the PHY side.

51.13 Ethernet AVB Module Signal Timing

Table 51.13.1 Ethernet Control Timing (MII)

Conditions: VCCQ = 3.3 ± 0.3 V, Tc = -40 to +115 °C, GND = VSS = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_TX_CLK cycle time	tTcyc	40	—	—	ns	Figure 51.13.1
AVB_TX_EN output delay time	tTEND	0	—	25	ns	
AVB_TXD[3:0] output delay time	tETDD	0	—	25	ns	
AVB_RX_CLK cycle time	tRcyc	40	—	—	ns	Figure 51.13.2
AVB_RX_DV setup time	tRDVS	10	—	—	ns	
AVB_RX_DV hold time	tRDVH	10	—	—	ns	
AVB_RXD[3:0] setup time	tERDS	10	—	—	ns	
AVB_RXD[3:0] hold time	tERDH	10	—	—	ns	
AVB_RX_ER setup time	tRERS	10	—	—	ns	Figure 51.13.3
AVB_RX_ER hold time	tRERH	10	—	—	ns	
AVB_MAGIC output delay time	tMAGICD	0	—	25	ns	Figure 51.13.4

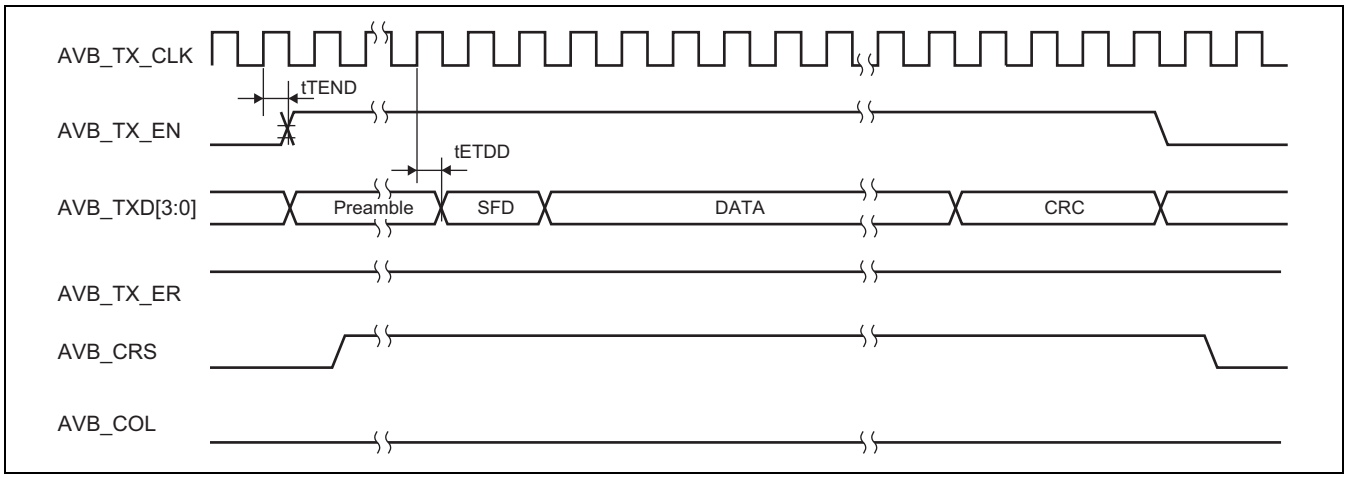


Figure 51.13.1 MII Transmission Timing (Normal Operation)

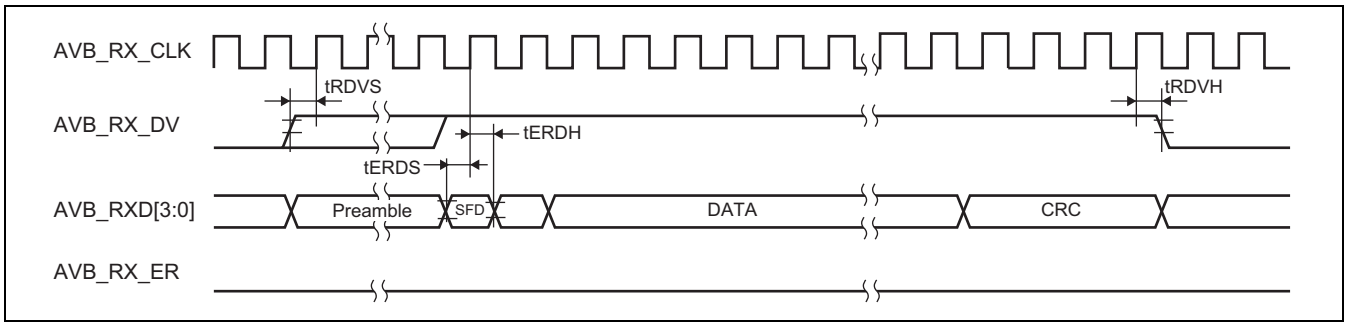


Figure 51.13.2 MII Reception Timing (Normal Operation)

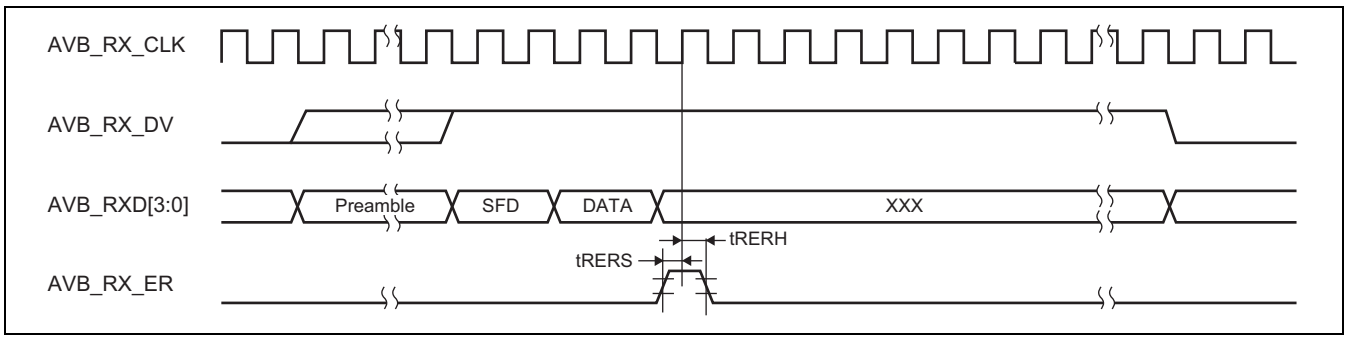


Figure 51.13.3 MII Reception Timing (Case When Error Occurs)

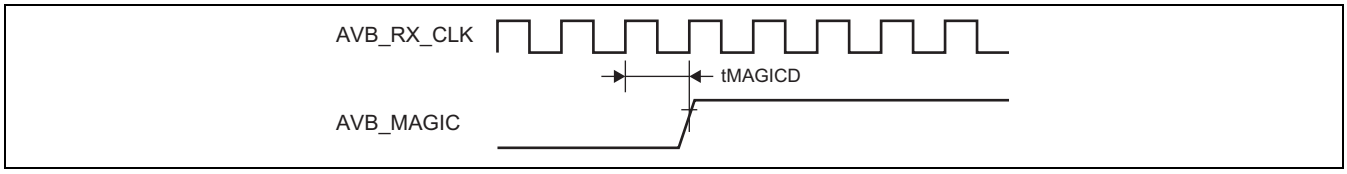


Figure 51.13.4 AVB_MAGIC Output Timing

Table 51.13.2 Ethernet Control Timing (GMII)

Conditions: VCCQ = 3.3 ± 0.3 V, Tc = -40 to +115 °C, GND = VSS = 0 V, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
AVB_GTXREFCLK clock input frequency	fREF125CK	125 – 100 ppm	—	125 + 100 ppm	MHz	—
AVB_GTX_CLK cycle time	tGTcyc	7.5	—	8.5	ns	Figure 51.13.5
AVB_TX_EN output delay time	tGTEND	0.5	—	5.5	ns	
AVB_TXD[7:0] output delay time	tGETDD	0.5	—	5.5	ns	
AVB_RX_CLK cycle time	tGRcyc	8	—	—	ns	Figure 51.13.6
AVB_RX_DV setup time	tGRDVS	2	—	—	ns	
AVB_RX_DV hold time	tGRDVH	0	—	—	ns	
AVB_RXD[7:0] setup time	tGERDS	2	—	—	ns	
AVB_RXD[7:0] hold time	tGERDH	0	—	—	ns	
AVB_RX_ER setup time	tGRERS	2	—	—	ns	Figure 51.13.7
AVB_RX_ER hold time	tGRERH	0	—	—	ns	
AVB_MAGIC output delay time	tGMAGICD	0	—	25	ns	Figure 51.13.8

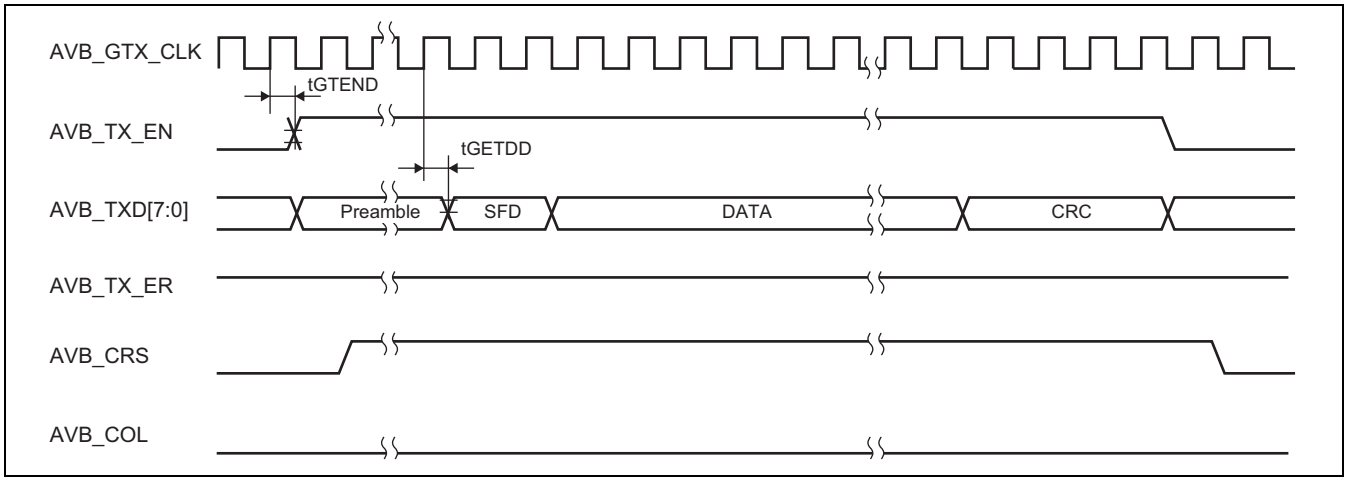


Figure 51.13.5 GMII Transmission Timing (Normal Operation)

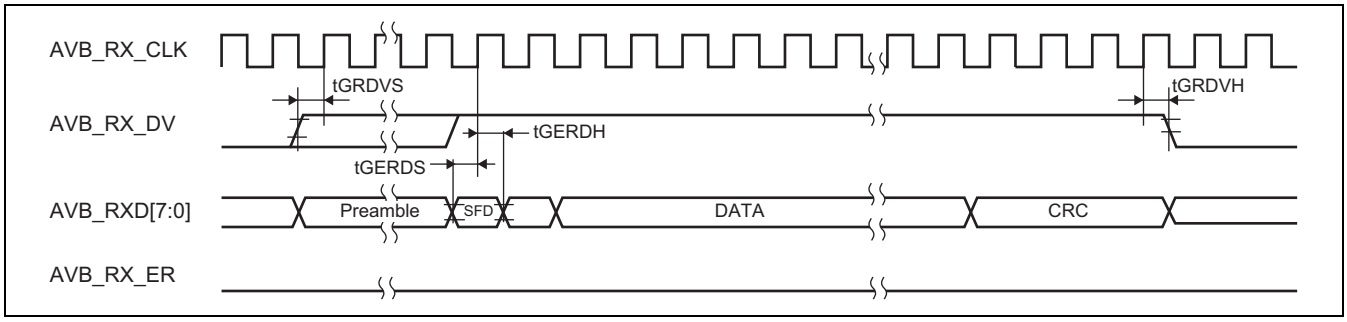


Figure 51.13.6 GMII Reception Timing (Normal Operation)

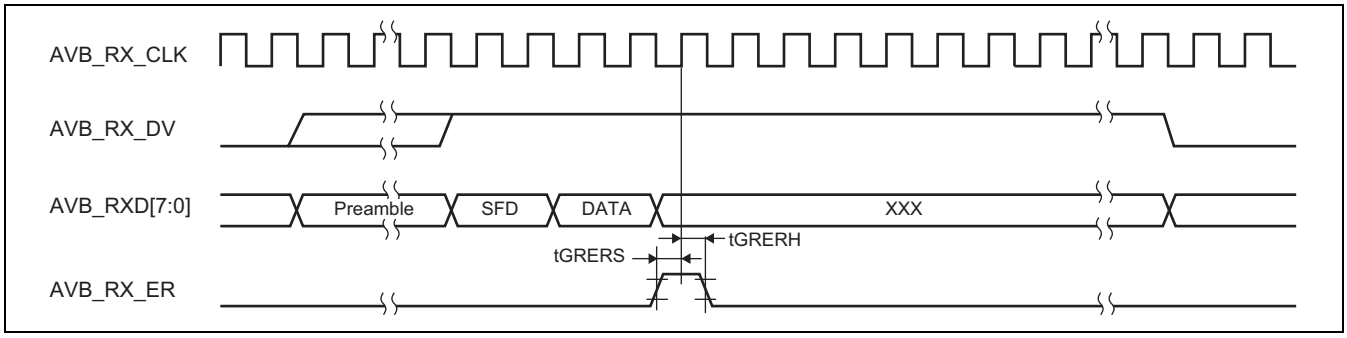


Figure 51.13.7 GMII Reception Timing (Case When Error Occurs)

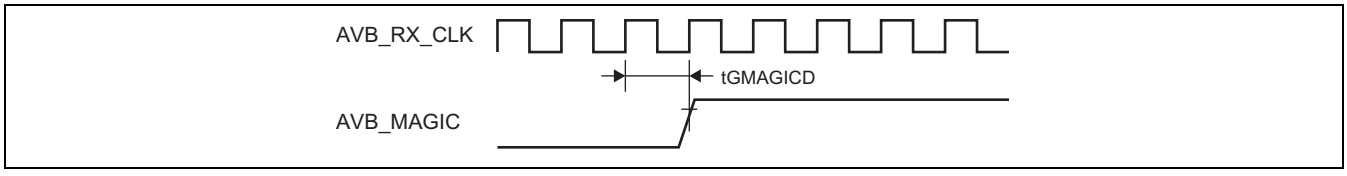


Figure 51.13.8 AVB_MAGIC Output Timing

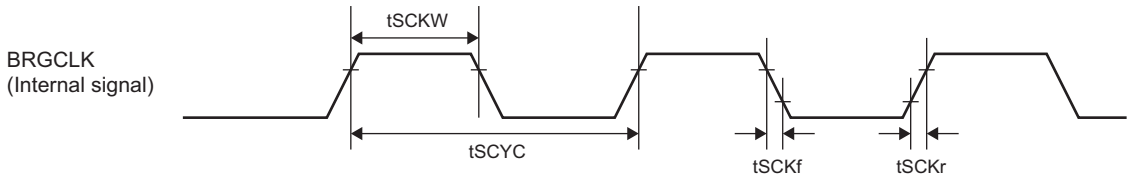
51.14 SCIF

Table 51.14.1 SCIF Signal Timing

Conditions: VCCQ = VCCQ_SDn = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
Input clock cycle (asynchronous)	tSCYC	4	—	—	tCYC	Figure 51.14.1
Input clock cycle (synchronous)	tSCYC	8	—	—	tCYC	
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.8	tCYC	
Input clock fall time	tSCKf	—	—	0.8	tCYC	
Transmit data delay time	tTXD	—	—	4	tCYC	Figure 51.14.2
Receive data setup time (synchronous)	tRXS	5	—	—	tCYC	
Receive data hold time (synchronous)	tRXH	2	—	—	tCYC	

Note: tCYC is for one cycle of the Pϕ clock.



Note: The output signal (BRGCLK) of the external baud rate generator (BRG) is an SCIF internal signal.
Set the input signal and the DL and CKS registers of the BRG so that the BRGCLK signal can satisfy the above specification.

Figure 51.14.1 Input Clock Timing

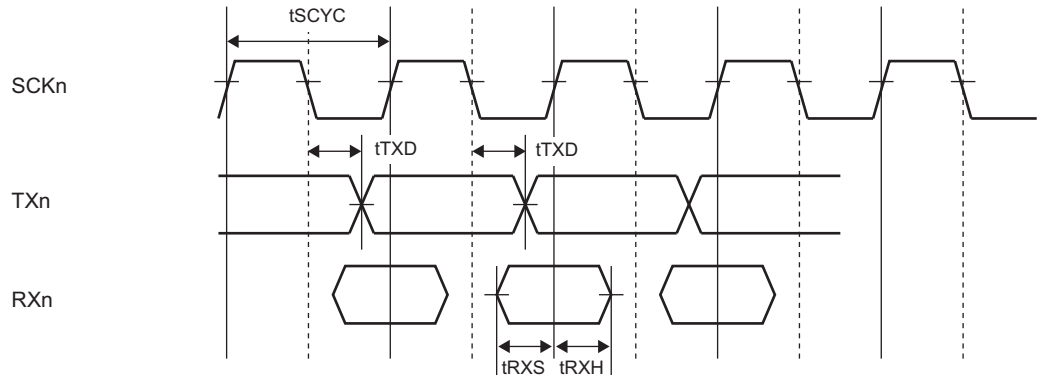


Figure 51.14.2 Input/output Timing in Synchronous Mode

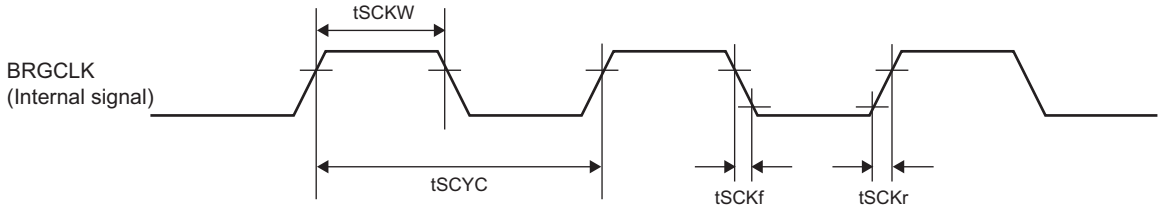
51.15 HSCIF

Table 51.15.1 HSCIF Signal Timing

Conditions: VCCQ = VCCQ_SDn = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Input clock cycle (asynchronous)	tSCYC	4	—	—	tCYC	Figure 51.15.1
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.8	tCYC	
Input clock fall time	tSCKf	—	—	0.8	tCYC	

Note: tCYC is for one cycle of the ZSϕ clock.



Note: The output signal (BRGCLK) of the external baud rate generator (BRG) is an HSCIF internal signal.
Set the input signal and the DL and CKS registers of the BRG so that the BRGCLK signal can satisfy the above specification.

Figure 51.15.1 Input Clock Timing

51.16 I2C

Table 51.16.1 I2C Signal Timing

Conditions: VCCQ = VCCQ_SD2 = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C, CL = 400 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
I2C_SCL frequency	tICYC	—	—	400	kHz	Figure 51.16.1
I2C_SCL low level time	tLOW	1 / (2 × tICYC) – 100	—	—	ns	
I2C_SCL high level time	tHIGH	600	—	—	ns	
I2C_SCL/I2C_SDA falling time	tICF	—	—	250	ns	
I2C_SDA bus free time	tICBF	1300	—	—	ns	
I2C_SCL start condition hold time	tICH	600	—	—	ns	
I2C_SCL repeat-start condition setup time	tICS	600	—	—	ns	
I2C_SDA stop condition setup time	tICST	600	—	—	ns	
I2C_SDA setup time	tDAS	100	—	—	ns	
I2C_SDA hold time	tICDH	0	—	900	ns	

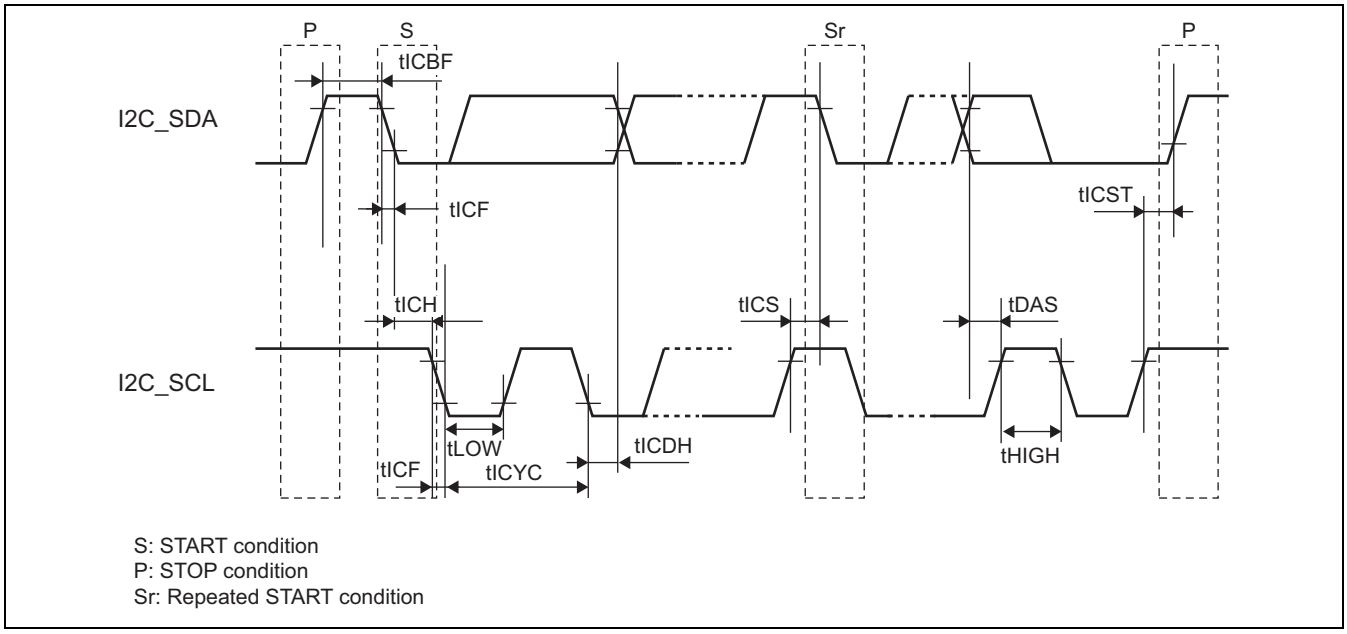


Figure 51.16.1 I2C Signal Timing

51.17 MSIOF

Table 51.17.1 MSIOF Module Signal Timing

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Max.	Unit	Figures
MSIOF_SCK clock cycle time	tMSCYC	2 × tpcyc*	—	ns	Figures 51.17.1 to 51.17.4
MSIOF_SCK output clock high-level width	tMSWHO	0.4 × tMSCYC	—	ns	
MSIOF_SCK output clock low-level width	tMSWLO	0.4 × tMSCYC	—	ns	
MSIOF_SCK input high-level width	tMSWHI	0.4 × tMSCYC	—	ns	
MSIOF_SCK input low-level width	tMSWLI	0.4 × tMSCYC	—	ns	
MSIOF_SYNC input setup time in slave mode	tTSFSS	10	—	ns	
MSIOF_SYNC input hold time in slave mode	tTSFSH	5	—	ns	
MSIOF_TXD output delay time1 in slave mode	tTSDD1	0	30	ns	
MSIOF_TXD output delay time2 in slave mode	tTSDD2	0	30	ns	
MSIOF_RXD input setup time in slave mode	tTSRDS	10	—	ns	
MSIOF_RXD input hold time in slave mode	tTSRDH	5	—	ns	
MSIOF_SYNC output delay time in master mode	tTMSFD	-3	8	ns	
MSIOF_TXD output delay time in master mode	tTMDD	-3	8	ns	
MSIOF_RXD input setup time in master mode	tTMRDS	20	—	ns	
MSIOF_RXD input hold time in master mode	tTMRDH	5	—	ns	

Note: * tpcyc is a cycle time of peripheral clock (MPϕ)

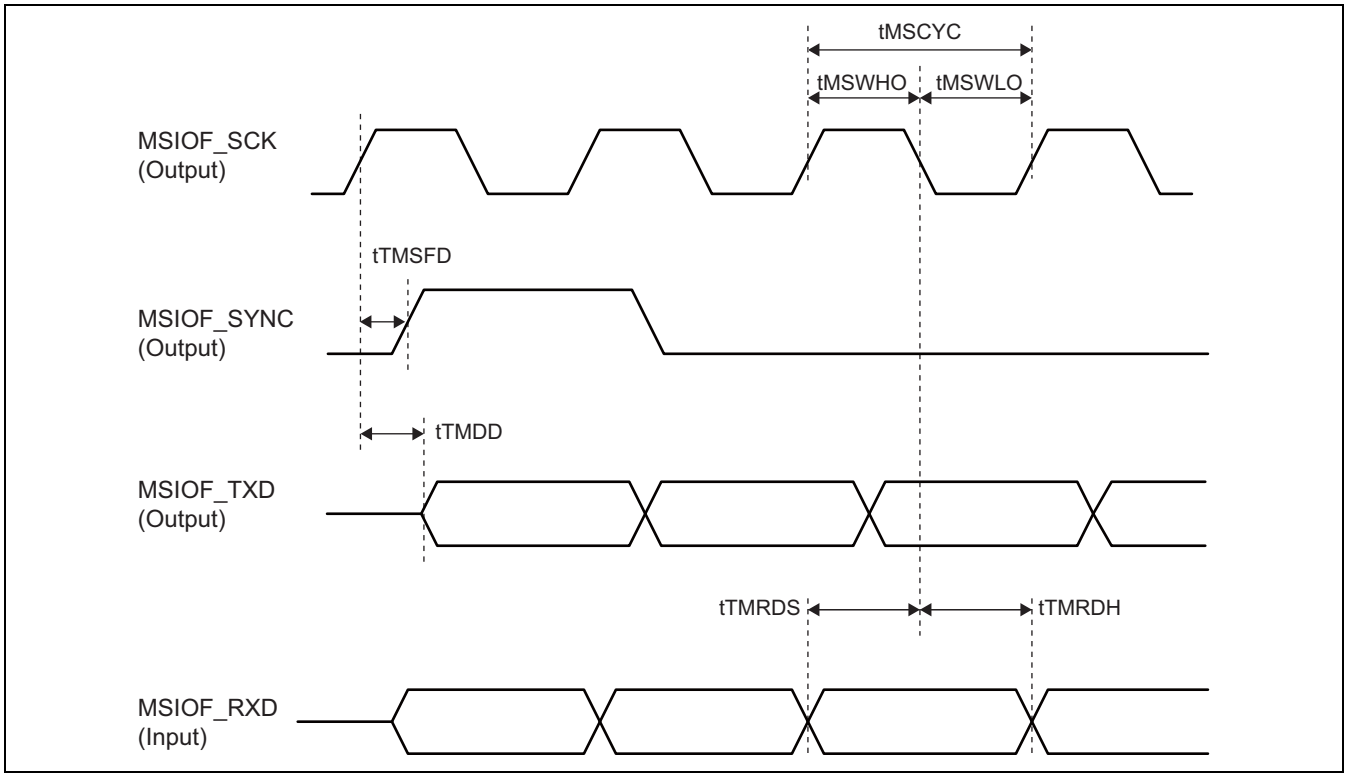


Figure 51.17.1 MSIOF Timing (Master Mode) (TEDG = 0, REDG = 0)

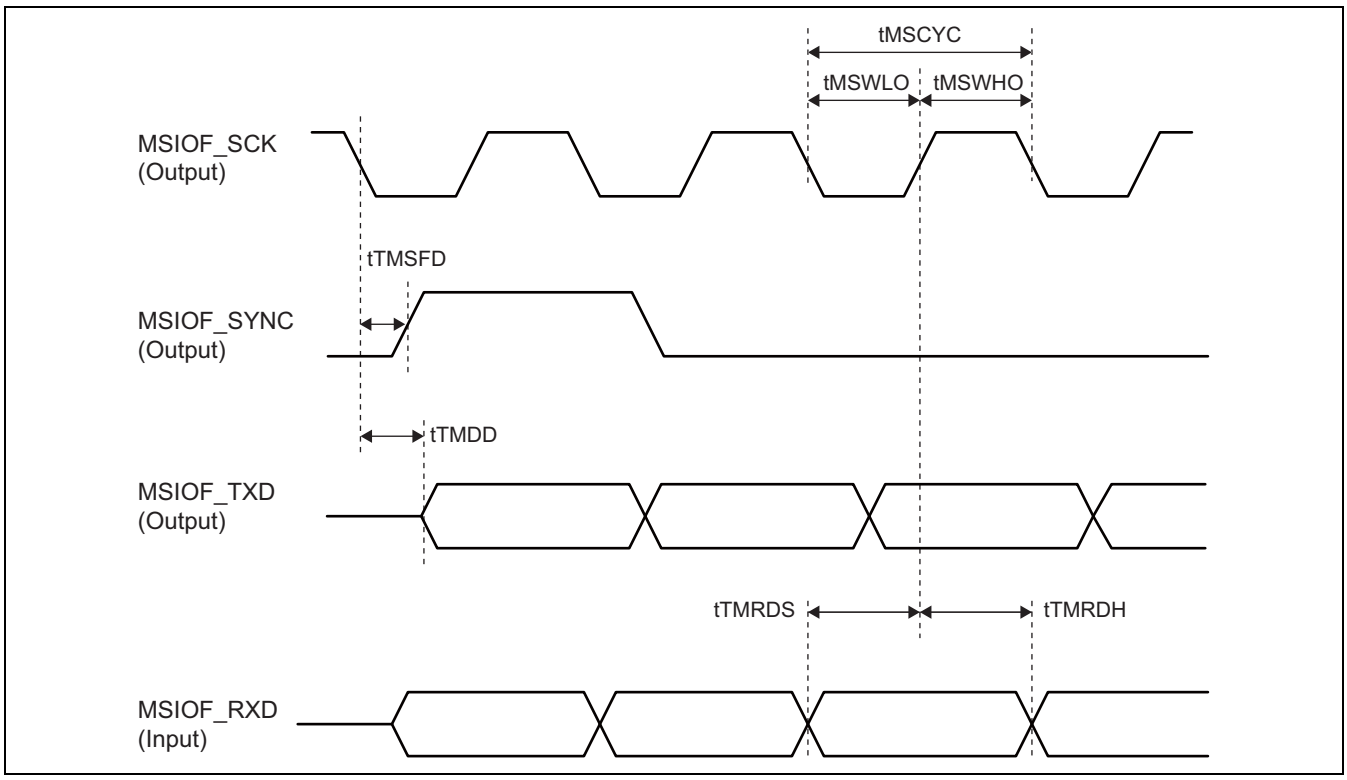


Figure 51.17.2 MSIOF Timing (Master Mode) (TEDG = 1, REDG = 1)

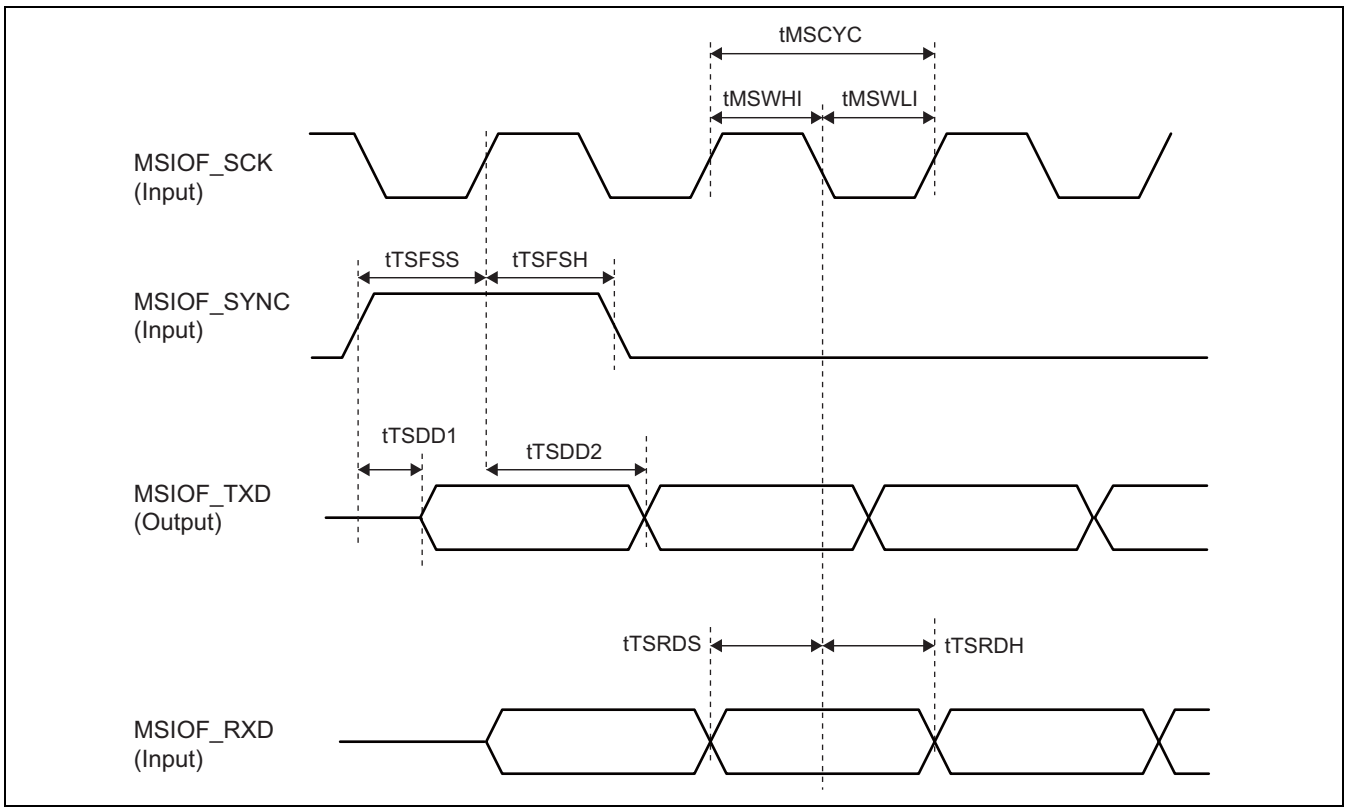


Figure 51.17.3 MSIOF Timing (Slave Mode) (TEDG = 0, REDG = 0)

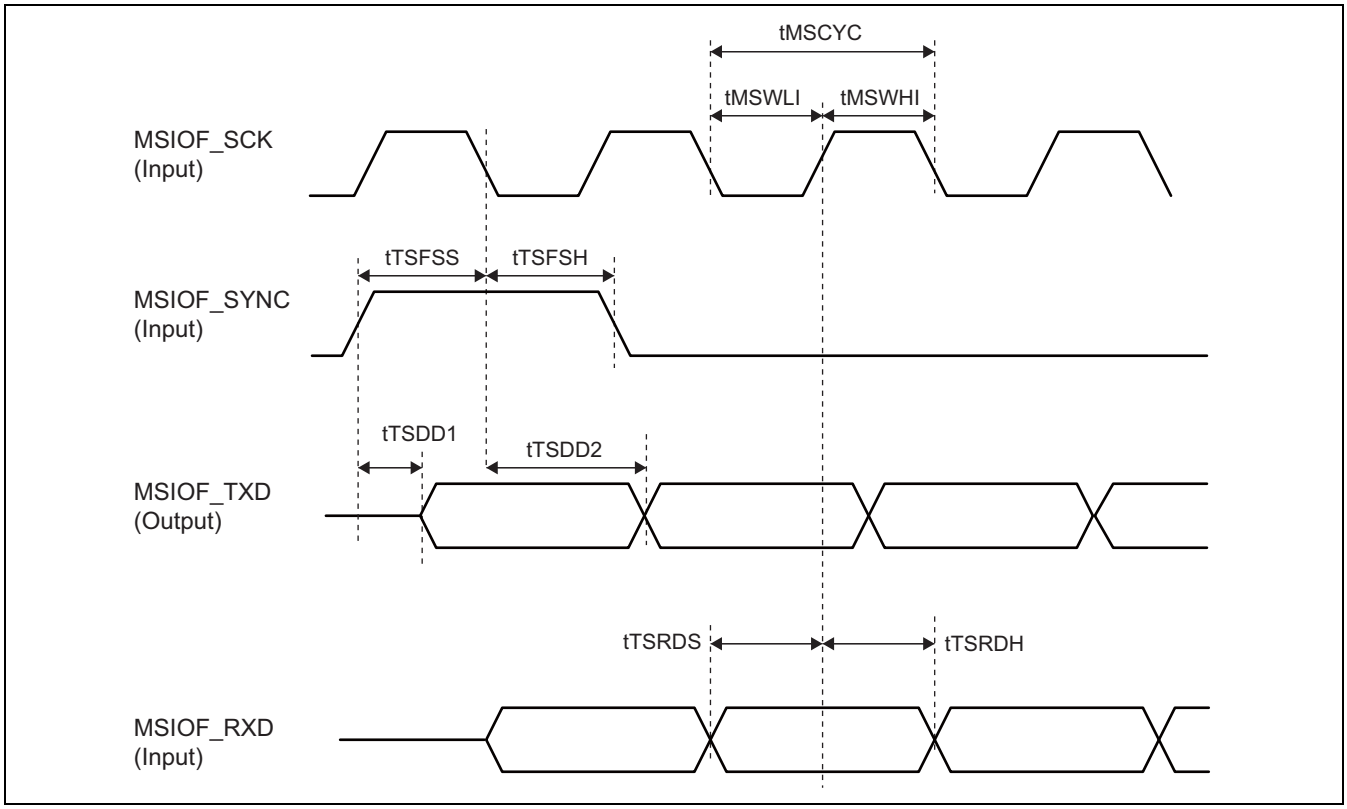


Figure 51.17.4 MSIOF Timing (Slave Mode) (TEDG = 1, REDG = 1)

51.18 QSPI

Table 51.18.1 QSPI Signal Timing

Conditions: VCCQ = 3.3 V ± 0.3 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
QSPICLK clock cycle	tQScyc	1	—	4080	Tcyc	Figures 51.18.1 to 51.18.3
Data input setup time	tSU	5.0	—	—	ns	
Data input hold time	tH	0.0	—	—	ns	
SSL setup time	tLEAD	1 to 8	—	—	tQScyc	
SSL hold time	tLAG	0.5 to 7.5	—	—	tQScyc	
Data output delay time	tOD	—	—	3.05	ns	
Data output hold time	tOH	-1.4	—	—	ns	
Continuous transfer delay time	tTD	1	—	8	tQScyc	

Note: Tcyc is a cycle time of QSPI clock (QSPIϕ).

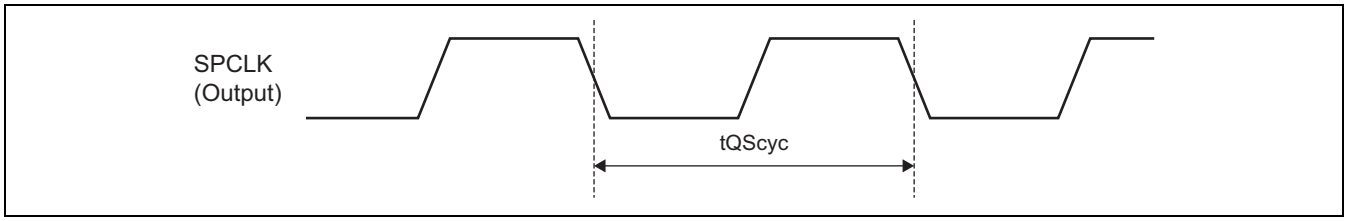


Figure 51.18.1 Clock Timing

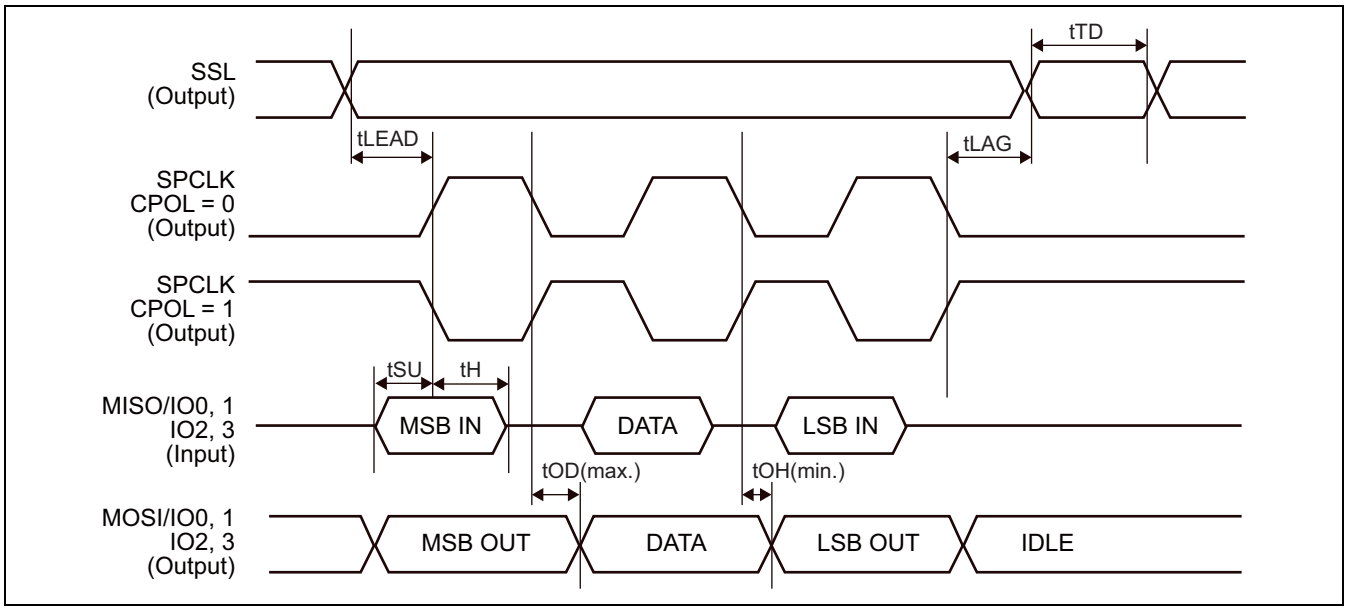


Figure 51.18.2 Sending and Receiving Timing (CPHA = 0)

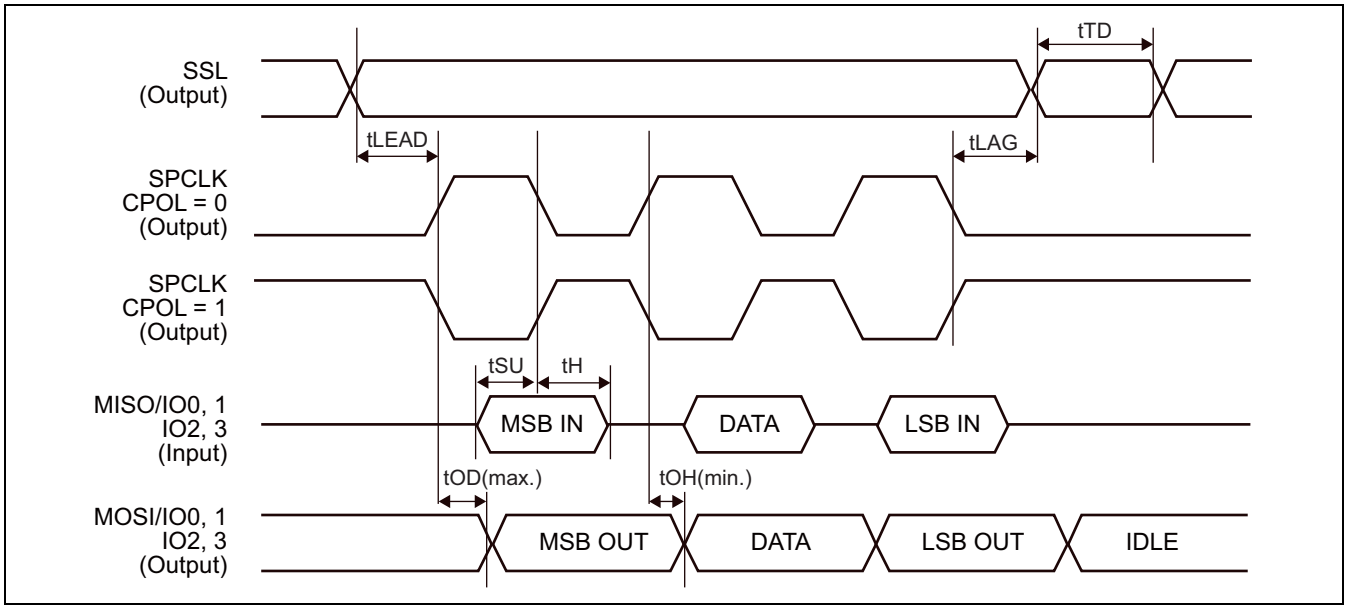


Figure 51.18.3 Sending and Receiving Timing (CPHA = 1)

51.19 USB Signal Timing

Table 51.19.1 USB High-speed Signal Timing

Conditions: VCCQ = VCCQA_USB = 3.3 V ± 0.3 V, VDDA_USBPLL = 1.21 V ± 0.05 V, GND = VSS = 0 V,
Tc = –40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
High-speed data rate	THSDRAT	479.76	480	480.24	Mb/s	—

Table 51.19.2 USB Low-/full-speed Signal Timing

Conditions: VCCQ = VCCQA_USB = 3.3 V ± 0.3 V, VDDA_USBPLL = 1.21 V ± 0.05 V, GND = VSS = 0 V,
Tc = –40 to +115 °C, CL = 50 pF

Item		Symbol	Min.	Typ.	Max.	Unit	Figure
Low-speed*	Rise time	tR	75	—	300	ns	Figure 51.19.1
	Fall time	tF	75	—	300	ns	
	Differential Rise and Fall Time Matching (t_R/t_F)	tRFM	80	—	125	%	
Full-speed	Rise time	tR	4	—	20	ns	
	Fall time	tF	4	—	20	ns	
	Differential Rise and Fall Time Matching (t_R/t_F)	tRFM	90	—	111.11	%	

Note: * The USB 2.0 Function module does not support Low-speed.

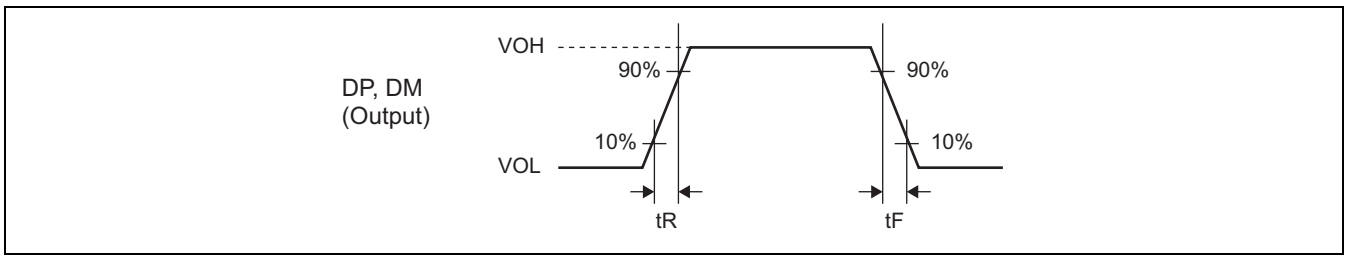


Figure 51.19.1 Low-/full-speed Data Signal Rise and Fall Time

Table 51.19.3 USB 2.0 External Clock Accuracy

Conditions: VCCQ = VCCQA_USB = 3.3 V ± 0.3 V, VDDA_USBPLL = 1.21 V ± 0.05 V, GND = VSS = 0 V,
Tc = –40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
External clock accuracy (USB_EXTAL, USB_XTAL)	—	—	48.000	—	MHz	Frequency deviation: ±100 ppm or less

51.20 TMU

Table 51.20.1 TMU Signal Timing

Conditions: VCCQ = VCCQ_SD = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
TCLK clock cycle	tTCLKCY	4	—	16.37	tCYC	Figure 51.20.1

Note: tCYC is for one cycle of the Pϕ clock.

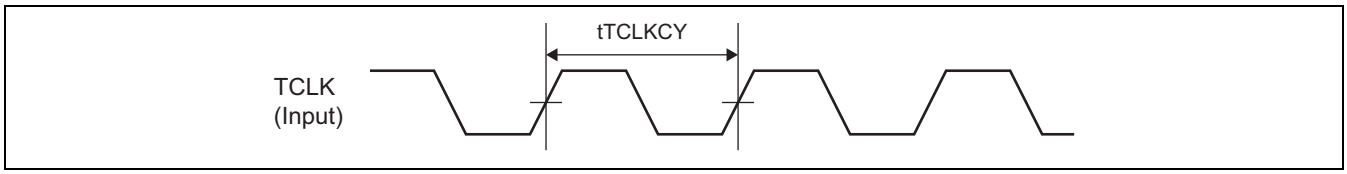


Figure 51.20.1 TMU Signal Timing

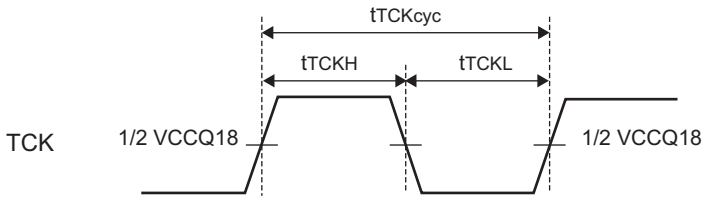
51.21 CoreSight

Table 51.21.1 JTAG Interface Signal Timing

Conditions: VCCQ18 = 1.8 V ± 0.1 V, GND = VSS = 0 V, Tc = −40 to +115 °C, CL = 30 pF

Item	Symbol	Min.	Typ.	Max.	Unit	Figures
TCK Input clock cycle	tTCKcyc	50*	—	—	ns	Figure 51.21.1
TCK Input clock pulse width (high level)	tTCKH	20	—	—	ns	
TCK Input clock pulse width (low level)	tTCKL	20	—	—	ns	
TDI/TMS setup time	tTDIS	15	—	—	ns	Figure 51.21.2
TDI/TMS hold time	tTDIH	15	—	—	ns	
TDO output delay time	tTDO	0	—	14	ns	

Note: * The cycle is 500 ns (2 MHz) during boundary scan operation.



Note: When the clock is input from the TCK pin.

Figure 51.21.1 TCK Input Timing

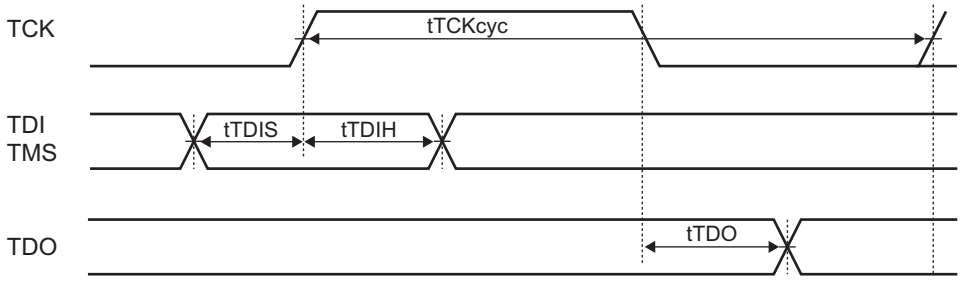


Figure 51.21.2 Data Transfer Timing

51.22 CAN

Table 51.22.1 CAN Signal Timing

Conditions: VCCQ = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Figure
Input clock cycle (asynchronous)	tSCYC	20	—	—	ns	Figure 51.22.1
Input clock pulse width	tSCKW	0.4	—	0.6	tSCYC	
Input clock rise time	tSCKr	—	—	0.2	tCYC	
Input clock fall time	tSCKf	—	—	0.2	tCYC	

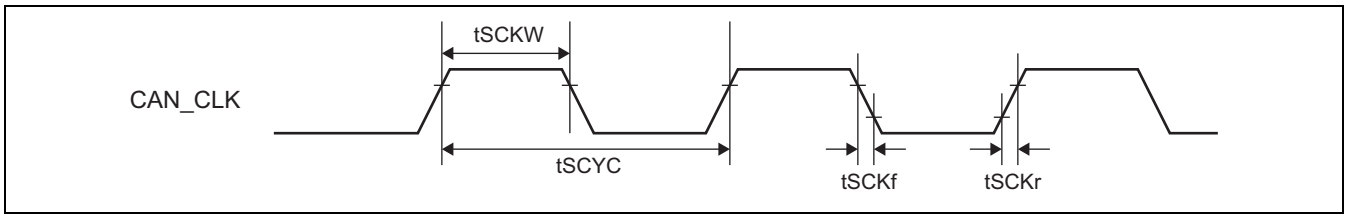


Figure 51.22.1 Input Clock Timing

51.23 Digital Video Encoder

Table 51.23.1 Characteristics of D/A Converter for the Digital Video Encoder

Conditions: VCCQA_DAC = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Video Clock input frequency	fclk	—	27.0	—	MHz	—
Video Clock input duty	fduty	45	—	55	%	—
Resolution	Rn	—	10	—	bit	—
Differential linearity error	DNL	—	—	±0.5	LSB	—
Integral linearity error	INL	—	—	±2.0	LSB	—
Analog output voltage	V_{opp}	—	1.30	—	Vp-p	—

51.24 Digital Video Decoder

Table 51.24.1 Characteristics of A/D Converter for the Digital Video Decoder

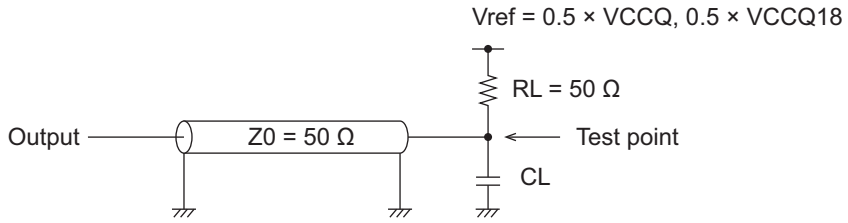
Conditions: VCCQA_ADC = 3.3 ± 0.3 V, GND = VSS = 0 V, Tc = -40 to +115 °C

Item	Symbol	Min.	Typ.	Max.	Unit	Remarks
Reference voltage (VRP)	VRP	—	1.7	—	V	—
Reference voltage (VRM)	VRM	—	0.9	—	V	—
Video Clock input frequency	fclk	—	27.0	—	MHz	—
Video Clock input duty	fduty	45	—	55	%	—
Resolution	Rn	—	10	—	bit	—
Differential linearity error	DNL	—	—	±1	LSB	—
Integral linearity error	INL	—	—	±3	LSB	—
A/D conversion range	Vin	—	1.6	—	Vpp	Condition: (VPR-VRM) × 2

51.25 AC Characteristics Test Circuit

51.25.1 Single-Ended Push-Pull Output

3.3 V and 1.8 V single-ended push-pull output test circuit.

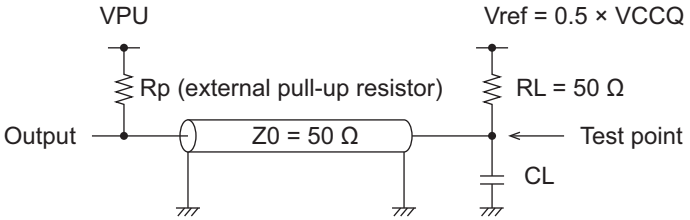


Note: For the value of CL, refer to each table condition of the module AC timing.

Figure 51.25.1 AC Output Load Equivalent Circuit (VCCQ, VCCQ_SD, VCCQ18)

51.25.2 Single-Ended I2C LVTTL

3.3V single-ended I2C LVTTL output test circuit.

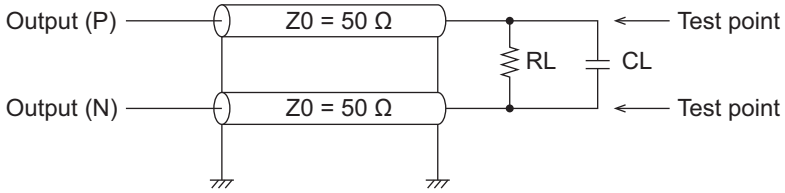


Note: For the value of CL, refer to each table condition of the module AC timing.

Figure 51.25.2 AC Output Load Equivalent Circuit (VCCQ)

51.25.3 Differential Output (LVDS)

3.3 V differential output test circuit.



Note: For the value of CL and RL, refer to each table condition of the module AC timing.

Figure 51.25.3 AC Output Load Equivalent Circuit (VCCQA_LVDS)

51.25.4 Differential Output USB 2.0 Low-Speed and Full-Speed

3.3 V differential output test circuit (USB 2.0 Low-speed and Full-speed).

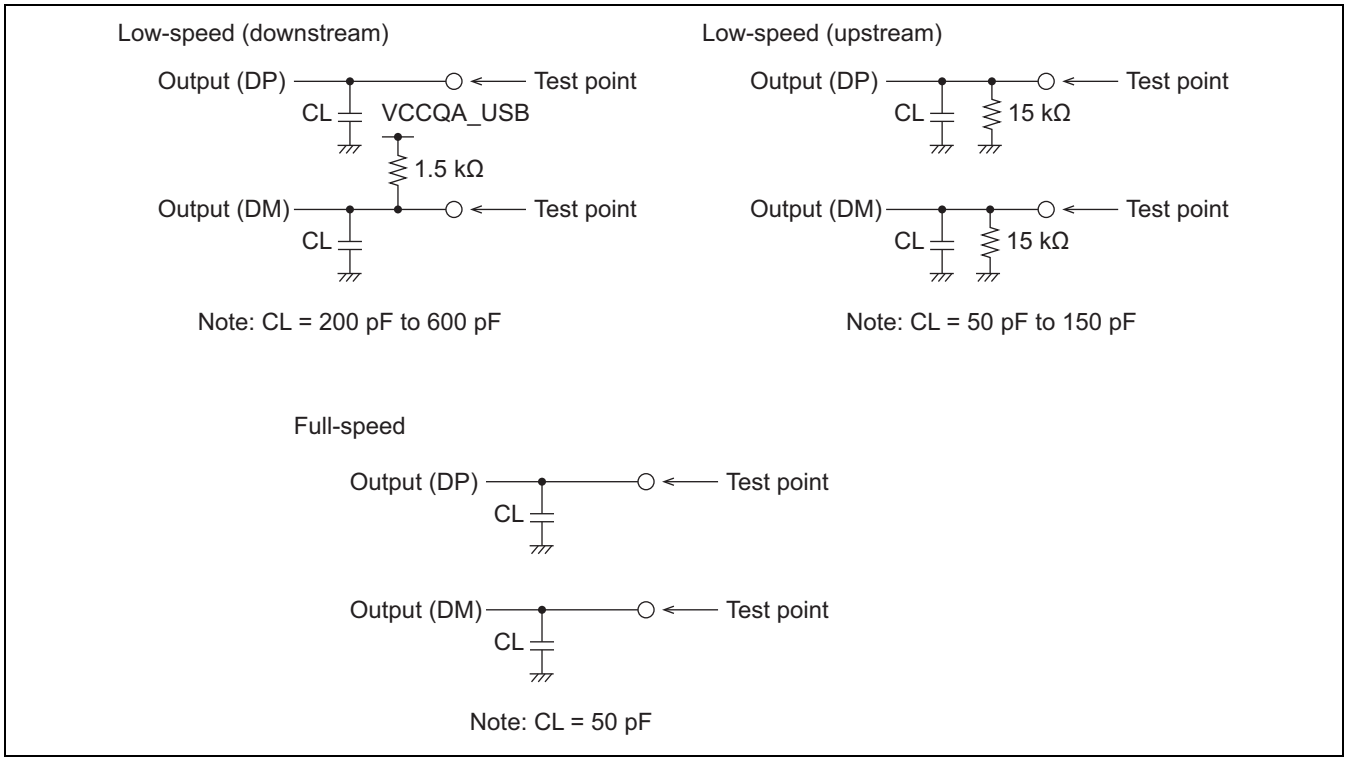


Figure 51.25.4 AC Output Load Equivalent Circuit

51.25.5 Differential Output USB 2.0 High-Speed

3.3 V differential output test circuit (USB 2.0 High-speed).

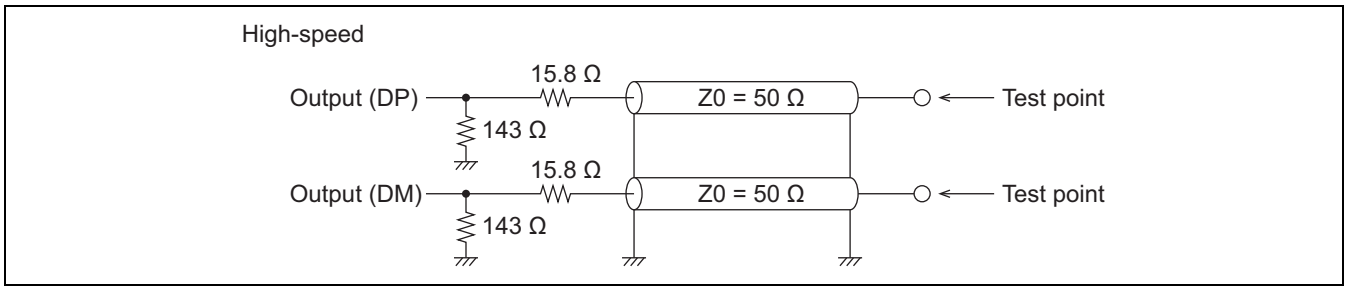
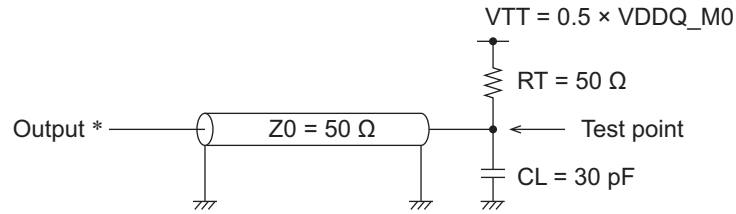


Figure 51.25.5 AC Output Load Equivalent Circuit

51.25.6 SSTL Single-Ended Output (DDR3 Interface)

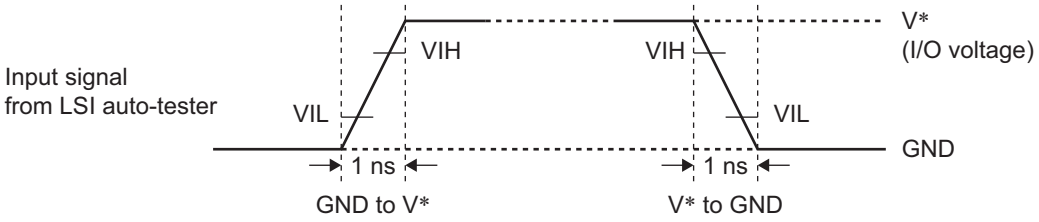
1.5 V single ended output test circuit (address and control signal).



Note: * MRESET#, MCS#, MODT, MWE#, MRAS#, MCAS#, MA[15:0], and MBA[2:0] pins

Figure 51.25.6 AC Output Load Equivalent Circuit (VDDQ_M0)

51.25.7 AC Test Input Signal Wave Form



Notes: Excluding USB.
* For each I/O voltage, refer to module AC timing specification.

Figure 51.25.7 AC Test Input Signal Wave Form

Appendix A. Product Register (PRR)

A.1 Overview

PRR indicates the product version and which of the ARM Cortex cores is present.

A.2 Register Descriptions

The following describes the details of the product register (PRR).

Register Name	Abbreviation	R/W	Address	Initial Value (Power-On Reset by PRESET# Pin)	Initial Value (Software Reset)	Access Size
Product register	PRR	R	H'FF00 0044	*	*	32 bits

Bit:	31	30	29	28	27	26	25	24	23	22	21	20	19	18	17	16
	—	—	—	—	—	CA7EN					—	—	—	—	—	—
Initial value:	1	1	1	1	1	*	*	*	*	*	0	0	0	0	0	0
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Bit:	15	14	13	12	11	10	9	8	7	6	5	4	3	2	1	0
	—	PRODUCT							CUT							
Initial value:	0	*	*	*	*	*	*	*	*	*	*	*	*	*	*	*
R/W:	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R	R

Note: * The settings of these bits are explained overleaf. Bits 31 to 27 are fixed, they depend on the product and the configuration you have ordered. Bits for processors that are never present in a given product are read as 1.

Bit	Bit Name	Initial Value	R/W	Description
31 to 27	—	B'11111	R	Bit 31 Reserved. The read value is always 1. Bit 30 Reserved. The read value is always 1. Bit 29 Reserved. The read value is always 1. Bit 28 Reserved. The read value is always 1. Bit 27 Reserved. The read value is always 1.
26 to 22	CA7EN	It depends on the product. See the description.	R	Bit 26 Cortex-A7 State 0: The product has two Cortex-A7 CPUs. 1: The product does not have two Cortex-A7 CPUs. Bit 25 Reserved. The read value is always 1. Bit 24 Reserved. The read value is always 1. Bit 23 Cortex-A7 CPU1 State 0: The product has Cortex-A7 CPU1. 1: The product does not have Cortex-A7 CPU1. Bit 22 Cortex-A7 CPU0 State 0: The product has Cortex-A7 CPU0. 1: The product does not have Cortex-A7 CPU0.
21 to 15	—	All 0	R	Reserved

Bit	Bit Name	Initial Value	R/W	Description
14 to 8	PRODUCT	See the description.	R	Product ID Number 101 0011
7 to 0	CUT	See the description.	R	Cut Number ES1.0: 0000 0000 ES2.0: 0001 0000 ES3.0: 0010 0000

Possible Configuration of the ARM Cortex Cores are Cortex-A7 CPU0 and Cortex-A7 CPU1 of product.

Main Revisions and Additions in this Edition

Minor revisions such as corrections of errors in spelling and modifications of wording are not included in the revision history.

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	Page	Contents	Summary
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