

# RZ/G2L-SBC, Single Board Computer

User's Manual: Hardware and Software

Renesas Microprocessor  
RZ Family RZ/G Series

OPN  
US157-G2LSBCPOCZ

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

- 1. Precaution against Electrostatic Discharge (ESD)**

A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
- 2. Processing at power-on**

The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
- 3. Input of signal during power-off state**

Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
- 4. Handling of unused pins**

Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
- 5. Clock signals**

After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
- 6. Voltage application waveform at input pin**

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between  $V_{IL}$  (Max.) and  $V_{IH}$  (Min.).
- 7. Prohibition of access to reserved addresses**

Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
- 8. Differences between products**

Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

## Introduction

This user manual describes the RZ/G2L based single board computer. This system architecture is of a generic single-board computer based on the Renesas RZ/G2L series SoC. It is a fully capable general purpose computer module aimed at HMI, industrial, and robotics applications.

This SBC features a Renesas RZ/G2L MPU as the main processor and runs a Linux distro built on Yocto OE using the Renesas VLP 3.0.5 package as its source.

One of the key highlights is the ease at which the board can be used to quickly create a PoC using a wide array of peripheral ports and proven accessories / modules. It comes equipped with an extensive set of features and interfaces, including onboard Wi-Fi, PMOD interface and dual ethernet ports.

## Features

The RZ/G2L-SBC board contains the following features:

- RZ/G2L or Dual core Cortex®A55 SoC with on-chip Cortex M33 core for real time applications.
- 1 GiB DDR4 (single chip of 4 Gbit)
- Micro SD card socket for OS image and rootfs
- QSPI for boot
- Temperature sensor with on-chip EEPROM holding board configuration data.
- Onboard Laird 802.11 Wi-Fi/BT module
- 40-pin Header connector (Raspberry Pi 3B compatible)
- Four USB 2.0 Type-A ports
- Dual Gigabit Ethernet ports
- 3.5mm Audio Port
- Mini- HDMI supporting full HD displays.
- MIPI-CSI port (Arduino compatible)
- MIPI-DSI port (Raspberry Pi compatible)
- Dual expansion ports for adapter board interfacing:
  - 40-pin DSI display modules.
  - 6 pin I2C touch modules.
  - ADC.
  - Bootstrapping.
  - External power and ground.
- USB Type-C Power connector
- Status LED indicators
- Board dimensions: 82 mm \* 50 mm
- Mount: Double-sided mounting (10 layers)

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## Glossary

| Terms   | Description   |
|---|---|
| 802.11 - Wi-Fi  | The technical name of the standard specification for Wi-Fi is 802.11. This is also the working group that develops and maintains the standards for Wi-Fi that everyone conforms to.   |
| ADC – Analog to digital converter                       | A hardware unit that converts an input analog signal to a digital value by measuring its immediate voltage at a fixed resolution.   |
| BSP – Board Support Package                             | BSP is an essential software package that has bootloaders, Linux kernel, a minimal user space and programming tools; allowing the device to boot. This core software allows the system to boot into an operating system, enables all the features and allows application development.   |
| CAN – Controller area network                           | This is a standardized communication protocol used widely on automotive and aerospace systems. It connects various ECU's known as nodes and uses two wires / lines as a pair carrying differential signals. This method of signaling allows long length cable to interface different systems on the machine with reliable signals. The CAN protocol has multiple specifications and is an ISO standard. It supports flexible data rates reaching as high as 8Mbps. Most automobiles have CAN networks in them, and it is a part of OBD-2 specification which is mandatory law in most of the world for automotive machines like cars.   |
| DAC – Digital to analog converter                       | A hardware unit that takes digital value and exerts a corresponding analog voltage on an output line.   |
| I2C - Inter Integrated circuit protocol:                | This is a communication protocol used to implement digital communication between two devices (chips / board) using only two wires. It is a standardized specification and is used widely to implement low to medium data rate data transfers both among devices on the same circuit board as well as external add on peripheral boards. I2C can be implemented across a few meters in distance. I2C is half duplex meaning only one device can communicate at a time. Speeds range from 100 Kbps to 3Mbps while 100 / 400 Kbps are the typical operating mode. The other major advantage of this protocol is that it allows many devices to be on the same two lines reducing the cost of the interfacing. This is ideal when there are many devices like sensors that transfer limited amounts of data periodically. I2C can support up to 127 independent directly addressable devices on the same channel. |
| IEEE- Institute of Electrical and Electronics Engineers | IEEE is the world's largest technical professional organization dedicated to advancing technology for the benefit of humanity. It is a major technical organization covering vast fields of engineering and a major standards organization.   |
| MCU – Micro controller unit                             | A micro controller unit is a self-contained unit that has the core processing as well as core memory within the same device. It often contains the core software programmed into the chip itself. This allows the device to start executing with minimal external devices / circuitry. Some microcontrollers can be powered on a mere breadboard.   |
| MPU – Micro processing unit                             | An MPU is a processing unit is a CPU that contains only the processing core and interfaces for external peripherals. A microprocessor is usually a powerful CPU in its class. However, it requires a very large number of external circuitries to achieve its functionality like external memory, disk drives, etc.   |
| PMIC – Power management IC                              | This is a specific chip on the board that manages multiple power supply lines at various levels. It manages the respective supplies along with sequences which control power on and power off cycles.   |
| SBC – Single board computer                             | It is a standard term that means a tiny computer in the form factor of a single circuit board usually just inches in area. This board is self-sufficient in every way and can give you a usable computer with just a power supply, keyboard, mouse, and display.  |
| SiP – System in Package                                 | SiP is a device where multiple silicon IP's are combined to form a single device. It's one of the densest chips where all the typically external devices like flash memory, DDR RAM and even Wi-Fi module are all packaged into a single chip. These usually used in very niche application that require ultra small size and low thermal requirement.  |

|                                   |   |
|-----------------------------------|---|
| SoC- System on Chip               | A system on chip is a complete hardware platform packaged on to a single chip. It contains the CPU, internal fast memory, interrupt controllers, pin controllers, ROM memory, and a number of other peripherals and even sensors; all packaged into the same IC. An SoC despite the high level of integration does not necessarily power on and run by itself. Microcontrollers are often independent SoC's that can work on their own. However, SoC's often combine MPU's and MCU's into the same chip. This allows very powerful systems to be built in a compact form factor but do require external supporting peripherals like DDR RAM and flash memory and power management IC's.                                   |
| SPI - Serial Peripheral interface | SPI is another standard interface used to interface other devices on the board or attaching peripheral boards. It specifies 3 wires / lines to achieve fast full duplex data transfer. Two devices can send / receive data at the same time in this protocol. The protocol is also a high-speed protocol where typical operating speeds start at 5Mbps and go over 50Mbps. This high speed allows interfacing high speed devices like memory, Wi-Fi, subsystems made of independent microcontrollers, etc. While only 3 lines are needed to interface two devices, a fourth line is used as a device selector allowing multiple devices to share the same interface. However, only two devices may communicate at a time. |

## RZ/G2L-SBC, Single Board Computer

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### 1. Overview

RZ/G2L-SBC Board is a power-efficient, graphics-enabled development board in a popular single-board computer format with well-supported expansion interfaces. This Renesas RZ/G2L processor-based platform is ideal for developing cost-efficient HMI, industrial, robotics, and a range of energy-efficient design applications. The RZ/G2L processor has two 1.2GHz Arm® Cortex®-A55 cores, a 200MHz Cortex-M33 core, a MALI 3D GPU, and an Image Scaling Unit. This processor SoC is equipped with an on-chip plus H.264 video (1920 x 1080) encode/decode function in silicon, making it ideal for implementing cost-effective embedded vision and display applications.

RZ/G2L-SBC is engineered in a compact Raspberry Pi form factor with a versatile set of expansion interfaces, including Gigabit Ethernet, 801.11ac Wi-Fi, and Bluetooth 5, four USB 2.0 host ports, a MIPI DSI display with touch and CSI camera interfaces, a CANFD interface, a PMOD interface, a Pi-HAT-compatible 40-pin expansion header, and two expansion sockets for a daughter card.

The board supports analog audio applications via audio codec and stereo headphone jack. It also pins out five 12-bit ADC inputs for interfacing with analog sensors through an expansion module (not included). 5V input power is sourced via a USB-C connector and managed via a single-chip Renesas RAA215300 PMIC device.

The onboard memory includes 1GB DDR4, 64 MiB QSPI NOR flash memory, and a microSD slot for removable boot media.

Software enablement includes CIP Kernel-based Linux BSP (maintained for 10 years+) plus reference designs that highlight demo implementations of HMI applications. Onboard 10-pin JTAG/SWD mini-SMT header (unpopulated) and 40-pin GPIO header enable the use of an external debugger and USB-serial cable.

### 1.1 Physical View

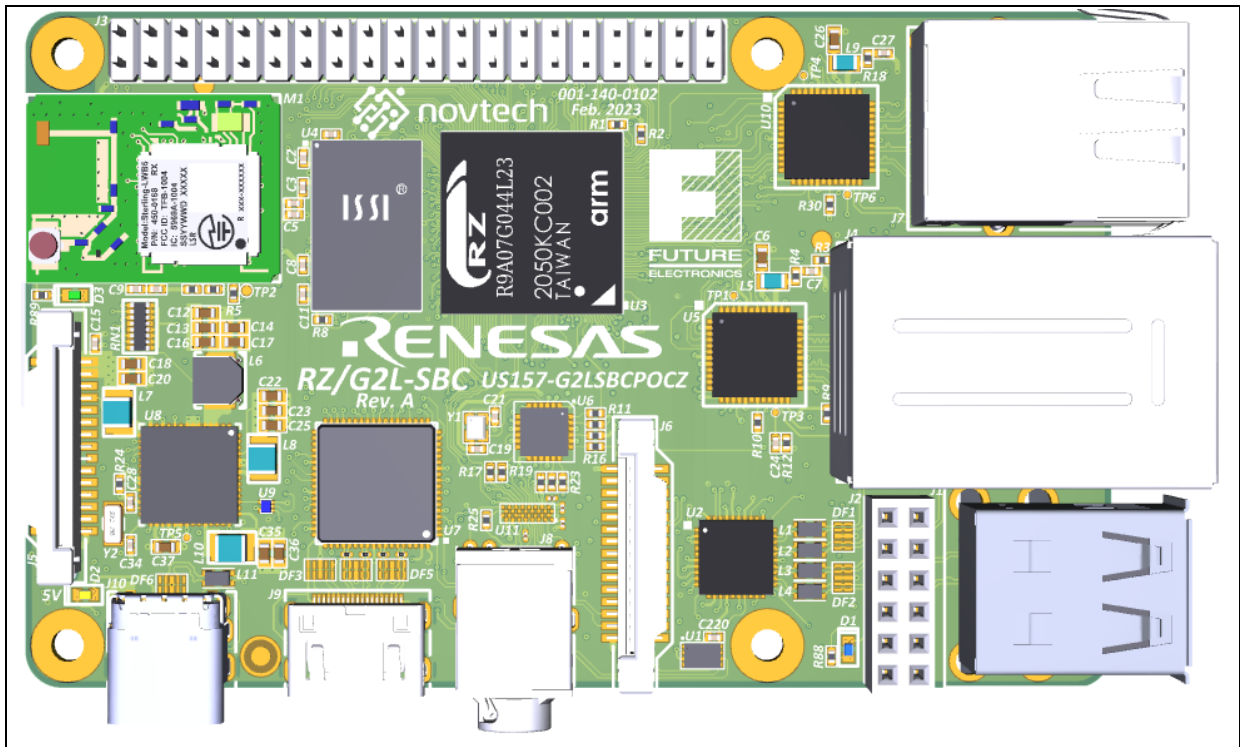


Figure 1: Top side view of the RZ/G2L-SBC

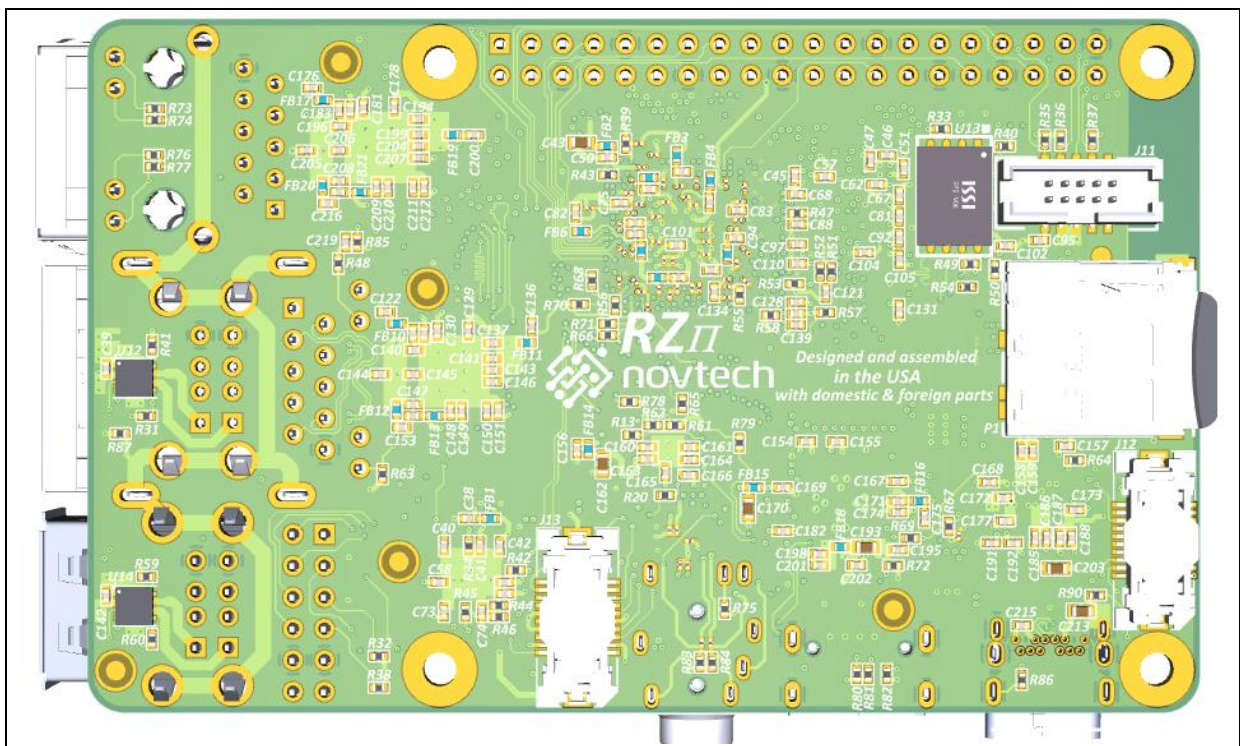


Figure 2: Bottom side of the RZ/G2L-SBC

## 2. Required Resources

### 2.1 Development Tools and Software

The following tools are used for development:

- SEGGER JLink software ([SEGGER - The Embedded Experts - Downloads - J-Link / J-Trace](#)).
- Tera Term ([Download File List - Tera Term - OSDN](#)) on Windows PC for accessing UART.
- Minicom on Ubuntu host machine for accessing UART on Linux.

### 2.2 Hardware

The following hardware would be needed to work with the RZ/G2L-SBC:

- Renesas RZ/G2L Board.
- Windows PC with Tera Term software and admin privileges.
- Ubuntu 20.04 host environment as native install or VM or docker environment: For working on Yocto distros.
- UART TTL cables (Raspberry pi compatible) featuring FTDI chipset. We do not recommend PL2302-based UART TTL cables as they have demonstrated issues with Windows drivers.
- Micro USB cables to interface with a host machine.
- Jumper wires/plugs.
- Mini-HDMI to HDMI display interface cable.
- Ethernet cables for networking.
- Power supply that can provide 5V at 3 A with USB-C pins. (not included in the package).
- Waveshare 5" DSI display module with a capacitive touch interface (optional: not included in the package).
- OV5640 camera module (optional: not included in the package).

### 3. RZ/G2L SoC MPU Architecture

The RZ/G2L MPU is a feature-packed SoC (System on Chip) that can support a variety of applications. Below is an overview of SoCs.

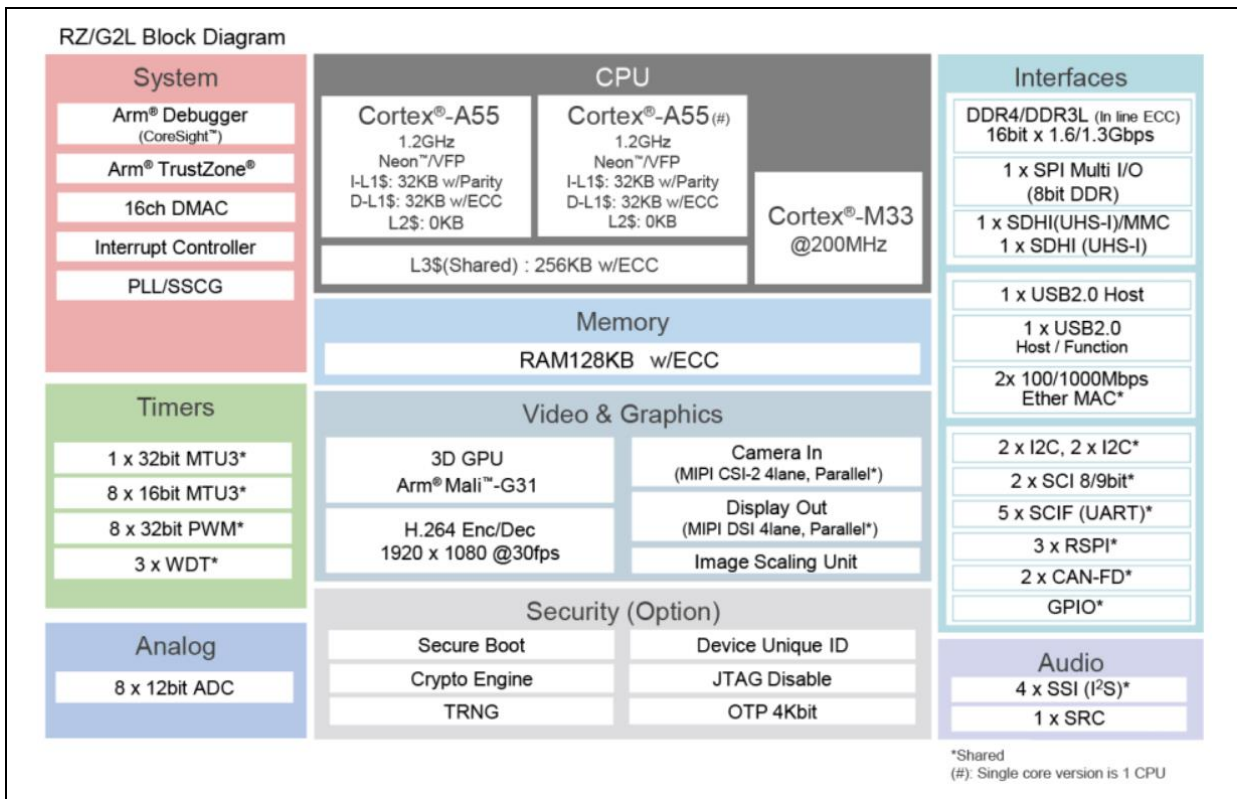


Figure 3: RZ/G2L SoC (System on Chip) Overview

#### 3.1 Operational Flow

The diagram below will show the operational flow of the RZ/G2L-SBC system during power ON.

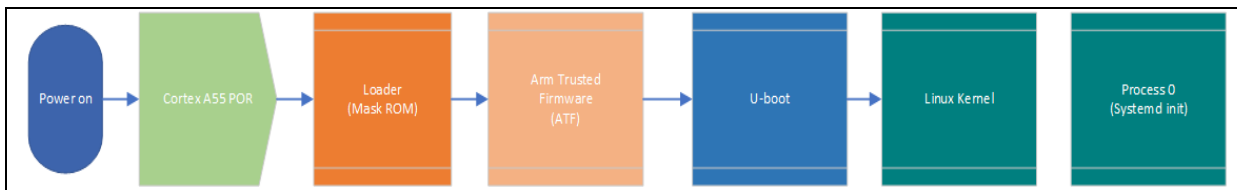


Figure 4: RZ/G2L-SBC boot operational flow

By default, the main processor will be in power OFF state to conserve battery. When the power is supplied, the PMIC immediately cycles power and puts the Cortex A55 into a POR state. This kickstarts the boot process with the Loader and ends with the Linux booting into user space.

While u-boot passes full control to the Linux kernel, arm trust zone remains active along with op-tee within the Arm core’s trust zone of operations.

The exact boot time depends on the boot environment and the number of services in the initialization process.



### 4. Functional Overview

This section delves into the functional and design aspects of the RZ/G2L-SBC. The below image highlights the key hardware components in the RZ/G2L SoC.

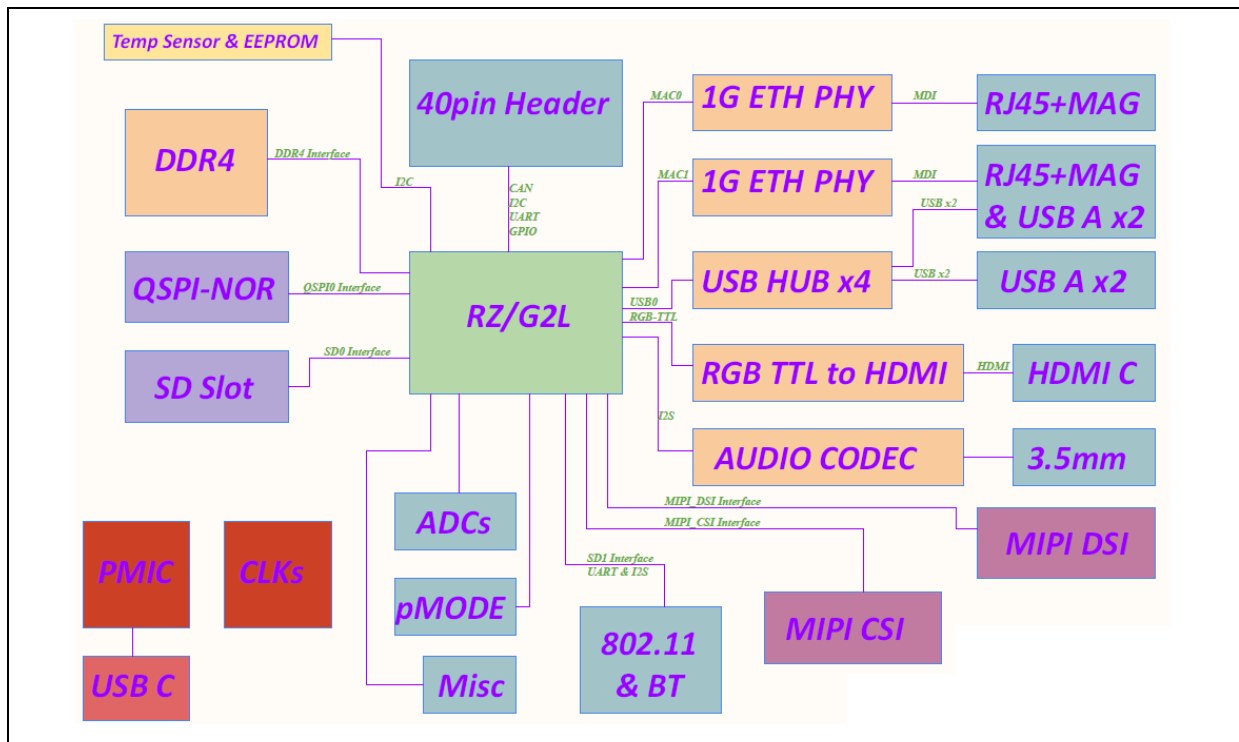


Figure 5: RZ/G2L SBC System Overview

Table 1: Main Components on RZ/G2L-SBC

| Component Number | Component Name  | Type (Manufacturer)                            |
|------------------|---|--|
| U1               | Temperature Sensor Digital, Local -55°C ~ 125°C<br>11 b 8-HWSON (2x3)                             | CAT34TS02 (Onsemi)                             |
| U2               | USB Controller  | UPD720115K8-611-BAK-A-ND (Renesas Electronics) |
| U3               | MPU RZ/G2L  | R9A07G044L23GBG (Renesas Electronics)          |
| U4               | DDR4 SDRAM 512MB  | IS43QR16256A-093PBLI-TR (ISSI)                 |
| U5               | Ethernet Phy 10BASE-TE, 100BASE-TX, 1GBASE-T  | PEF7071VV16 (MaxLinear)                        |
| U6               | VersaClock® Programmable Clock Generator  | 5P35023B-000NLGI8 (Renesas Electronics)        |
| U7               | HDMI Transmitter  | SiI9022A/4A – QFN (SiliconImage)               |
| U8               | PMIC  | RAA215300 (Renesas Electronics)                |
| U9               | AND GATE 2IN SOT-23-5 Vcc 1.65V to 5.5V   | 7UL1G08FS (Toshiba)                            |
| U10              | Ethernet Phy 10BASE-TE, 100BASE-TX, 1GBASE-T  | PEF7071VV16 (MaxLinear)                        |
| U11              | Audio Codec with Advanced Accessory Detect  | DA7219 (Renesas Electronics)                   |
| U12              | Dual USB Port Power Supply Controller - Covering the Industrial Temperature Range of -40C to +85C | ISL61852FIRZ (Renesas Electronics)             |
| U13              | QSPI Flash 512MBIT SPI/QUAD 8WSO  | S25FS512SDSNFB010 (Infineon)                   |

|     |   |                                    |
|-----|---|------------------------------------|
| U14 | Dual USB Port Power Supply Controller - Covering the Industrial Temperature Range of -40C to +85C | ISL61852FIRZ (Renesas Electronics) |
| M1  | Integrated 802.11 b/g/n Wi-Fi Module  | iWi-L-WB (Laird)                   |
| Y1  | Crystal resonator for XIN   | XRCGB24M000F0L00R0 (Murata)        |
| Y2  | Crystal resonator for XIN   | ST3215SB32768H5HPWAA (Kyocera-AVW) |

**Table 2: Primary connectors on RZ/G2L-SBC**

| Components Number | Component Name   | Type (Manufacturer)           |
|-------------------|--|-------------------------------|
| J1                | USB 2 & 3  | USB-A-D-RA (Adam Tech)        |
| J2                | PMOD   | PPPC062LFBN-RC (Sullins)      |
| J3                | 40-Pin Header (Raspberry Pi 3B compliant)                    | -                             |
| J4                | USB 0 & 1, 10/100/1000 Ethernet 2                            | YKGU-6101NL (Ingke)           |
| J5                | MIPI-CSI   | 1-1734248-5 (TE Connectivity) |
| J6                | MIPI-DSI   | 1-1734248-5 (TE Connectivity) |
| J7                | 10/100/1000 Ethernet 1                                       | YKGD-8069NL (Ingke)           |
| J8                | Audio I/O (Speaker/Microphone)                               | ASJ-192-Y (Adam Tech)         |
| J9                | Mini-HDMI  | 10029449-001RLF (FCI)         |
| J10               | USB-Type-C Power Input                                       | C-ARA1-AK515 (CNC Tech)       |
| J11               | 20-pin JTAG connector  | 3221-10-0300-00 (CNC Tech)    |
| J12               | Expansion Connector to Display adapter & boot strapping pins | 528850274 (Molex)             |
| J13               | Expansion Connector to Display adapter & boot strapping pins | 528850274 (Molex)             |
| P1                | microSD card slot  | MEM2051-00-195-00-A (GCT)     |



## 4.1 Overview of Connectors

Given below is the basic positioning of the top-level connectors.

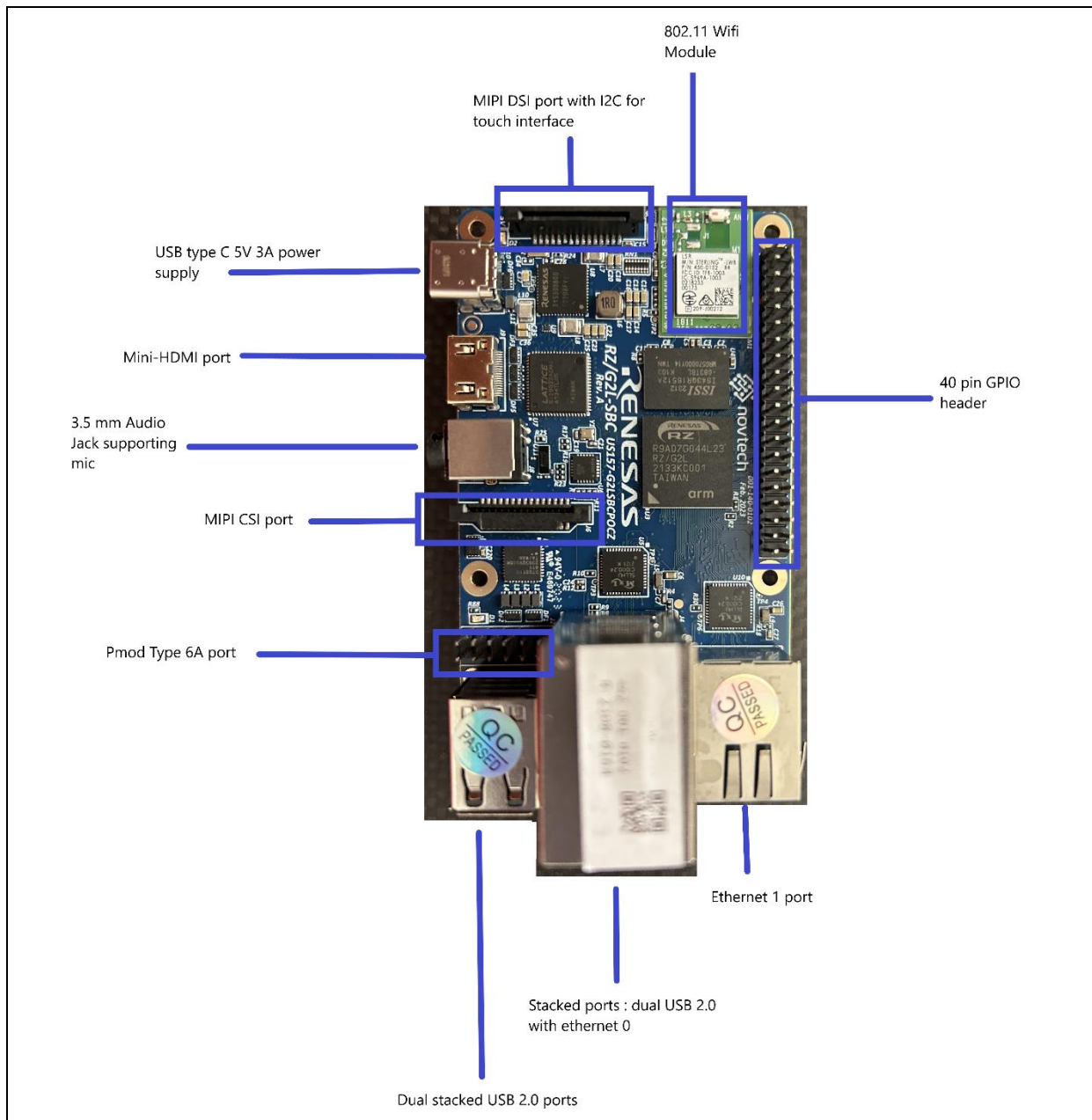


Figure 6: RZ/G2L-SBC top side connectors.

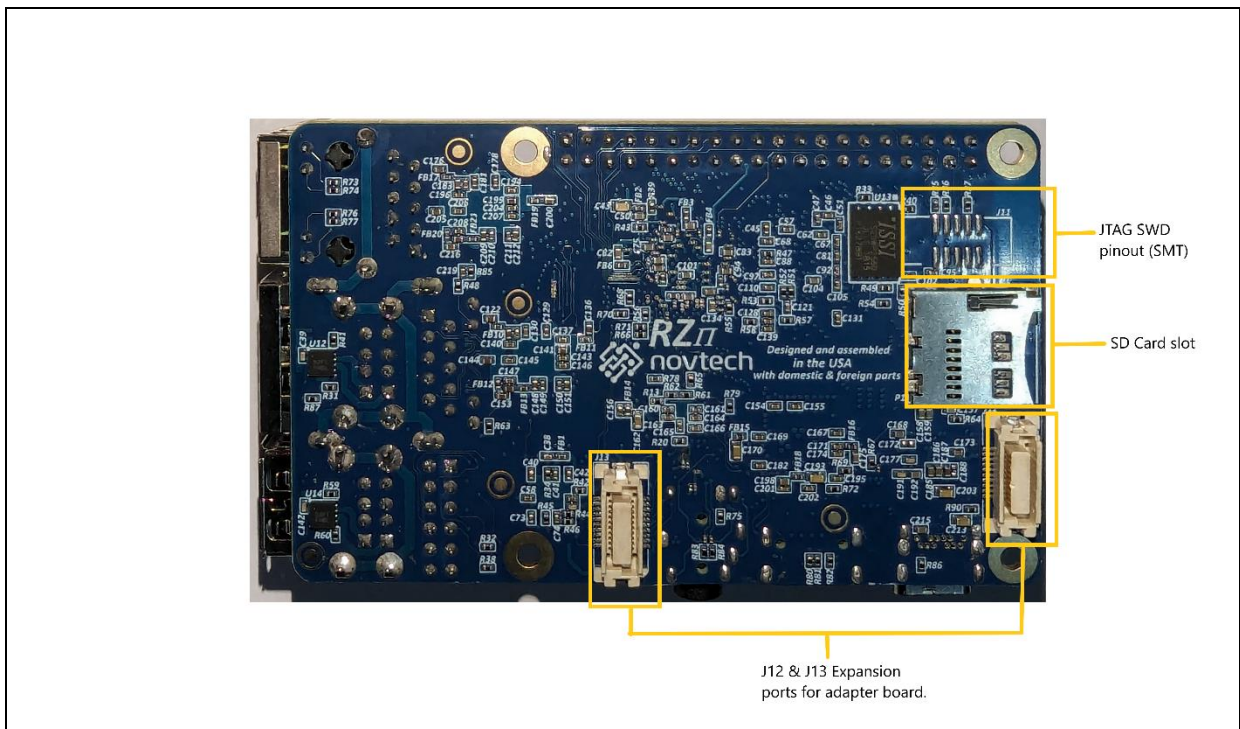


Figure 7: RZ/G2L-SBC Bottom view connectors.

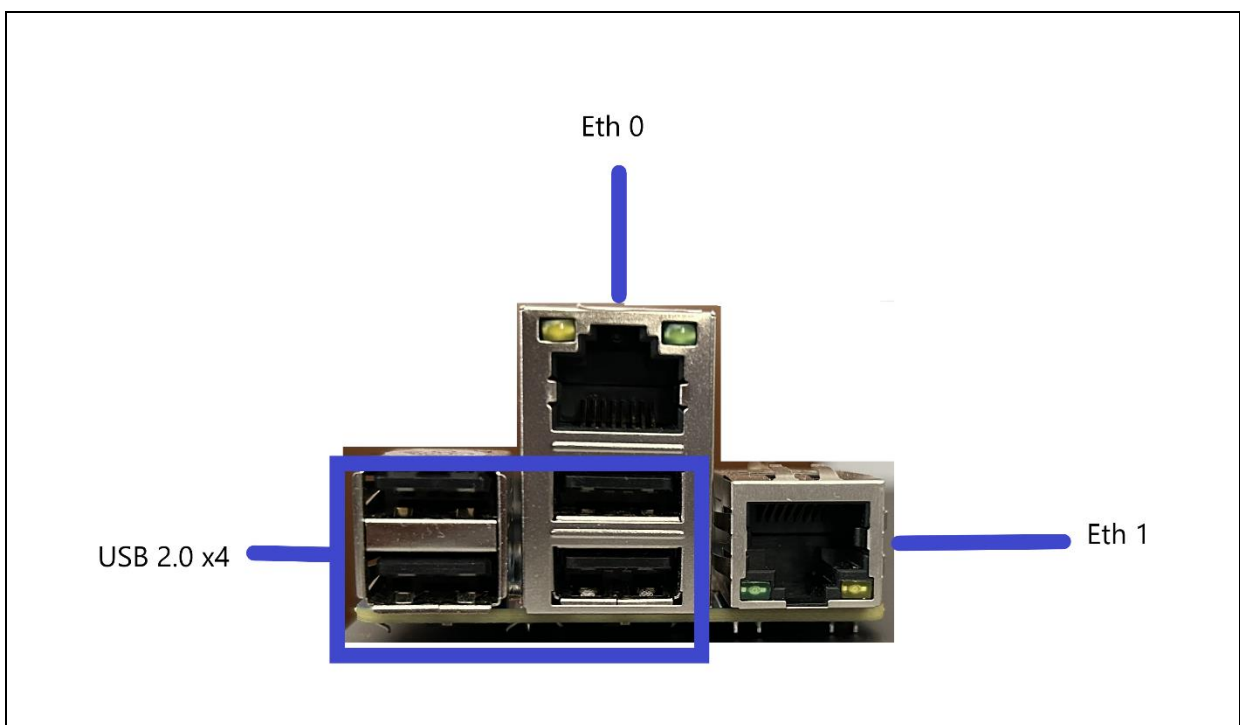


Figure 8: RZ/G2L-SBC side view I/O ports.

## 4.2 Power Supply

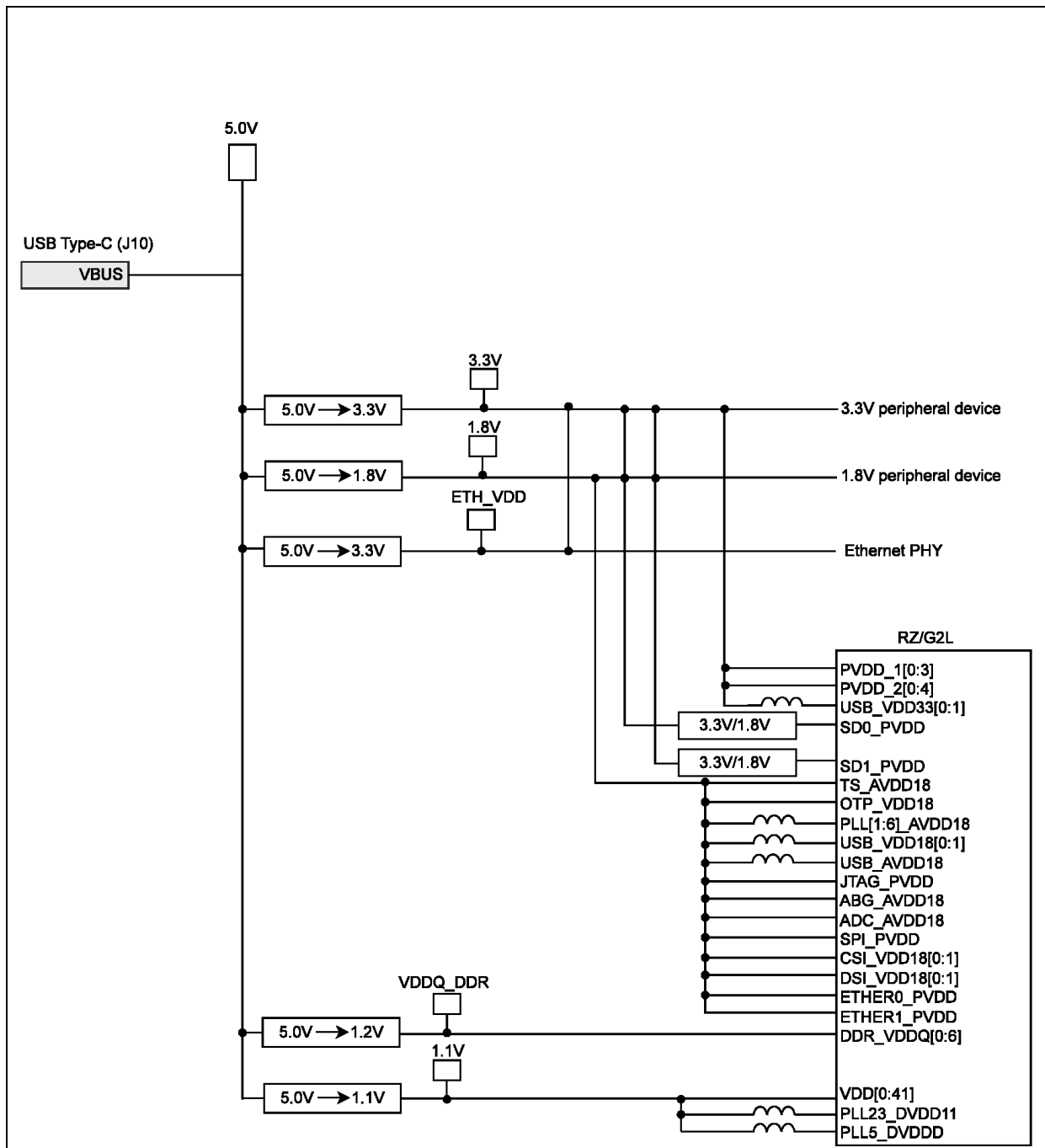
This section delves into the RZ/G2L-SBC's power supply architecture. The RZ/G2L-SBC uses a simple design, with a 5V supply as the single external power source.

### 4.2.1 USB Type-C Power

This board has one USB Type-C receptacle for power input with USB Power Delivery. The USB type-C power connector is meant to connect to a 5V power supply. The RZ/G2L-SBC requires a minimum of 3A power to prevent brownouts. However, we recommend a 4.5 -5A power supply as several ports support peripherals consuming substantial power.

### 4.2.2 Power rails

Given below is the basic power supply design. It's a simple design that uses an input power supply from USB-C or one of the routed pins marked as 5V in the 40-pin GPIO or the adapter board and routes it through a series of converters to generate different power lines.



**Figure 9: Power supply rails.**

The Input power of 5V is used to generate 5 independent power lines:

- Two independent 3.3 V lines for peripherals and ethernet.
- A 1.8V master supply line
- A 1.2V master supply line
- A 1.1V master supply line

The 1.2V line is used by the RZ/G2L SoC and the DDR4 SDRAM, while the 1.1V line is exclusively used by the RZ/G2L SoC. The RZ/G2L also draws power to its internal IP blocks from the 1.8V line.

This design is aimed at simplicity and hence omits the use of any power and reset switches. The POR behavior is strictly controlled by the PMIC and its passives.

### 4.2.3 Power Supply Regulation

The power supply is regulated by Renesas RAA215300 low-cost 9 channel PMIC IC.

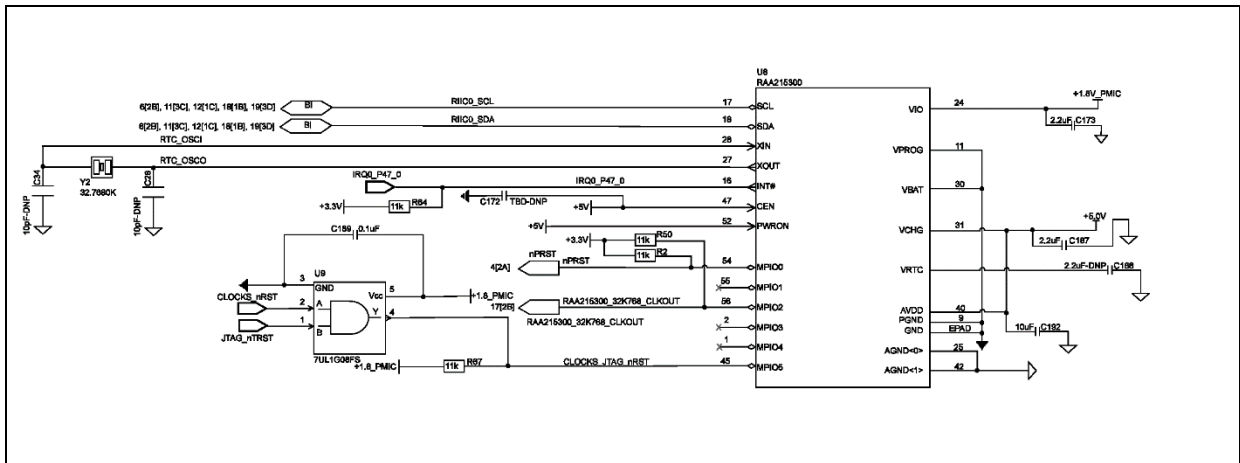


Figure 10: Block Diagram of Power Supply Regulation using RAA215300.

### 4.3 Power Management Integrated Circuit- PMIC

All LDOs are cycled as per the POR cycle. Any control is exercised by the RZ/G2L through the I2C interface. However, the LDO's are always turned-on post PoR.

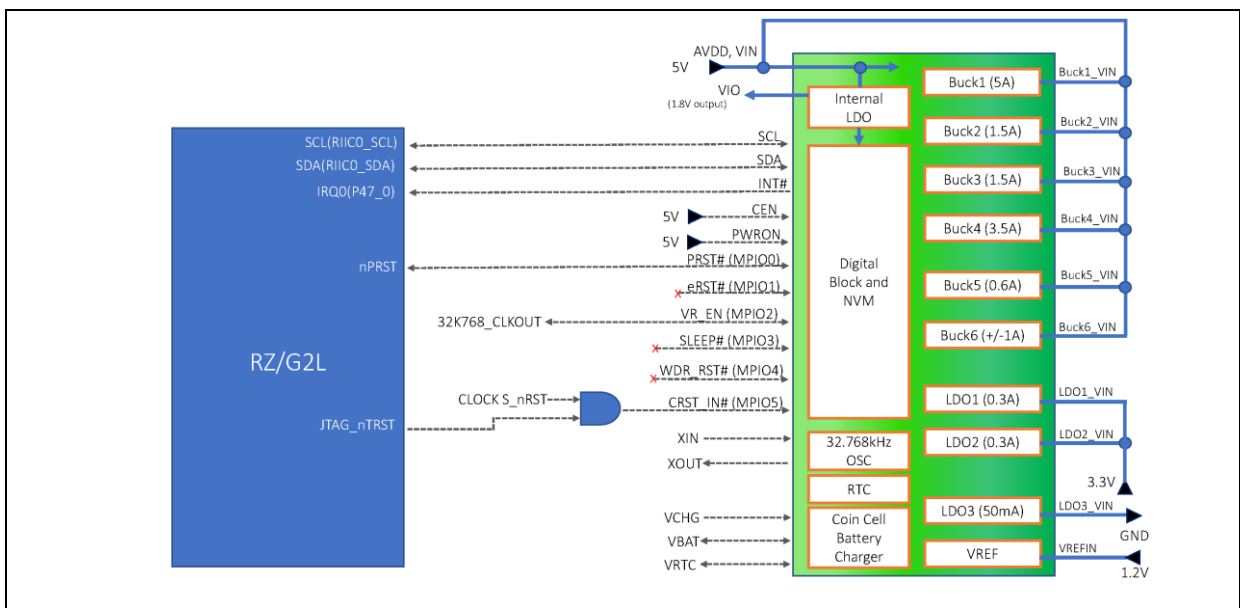


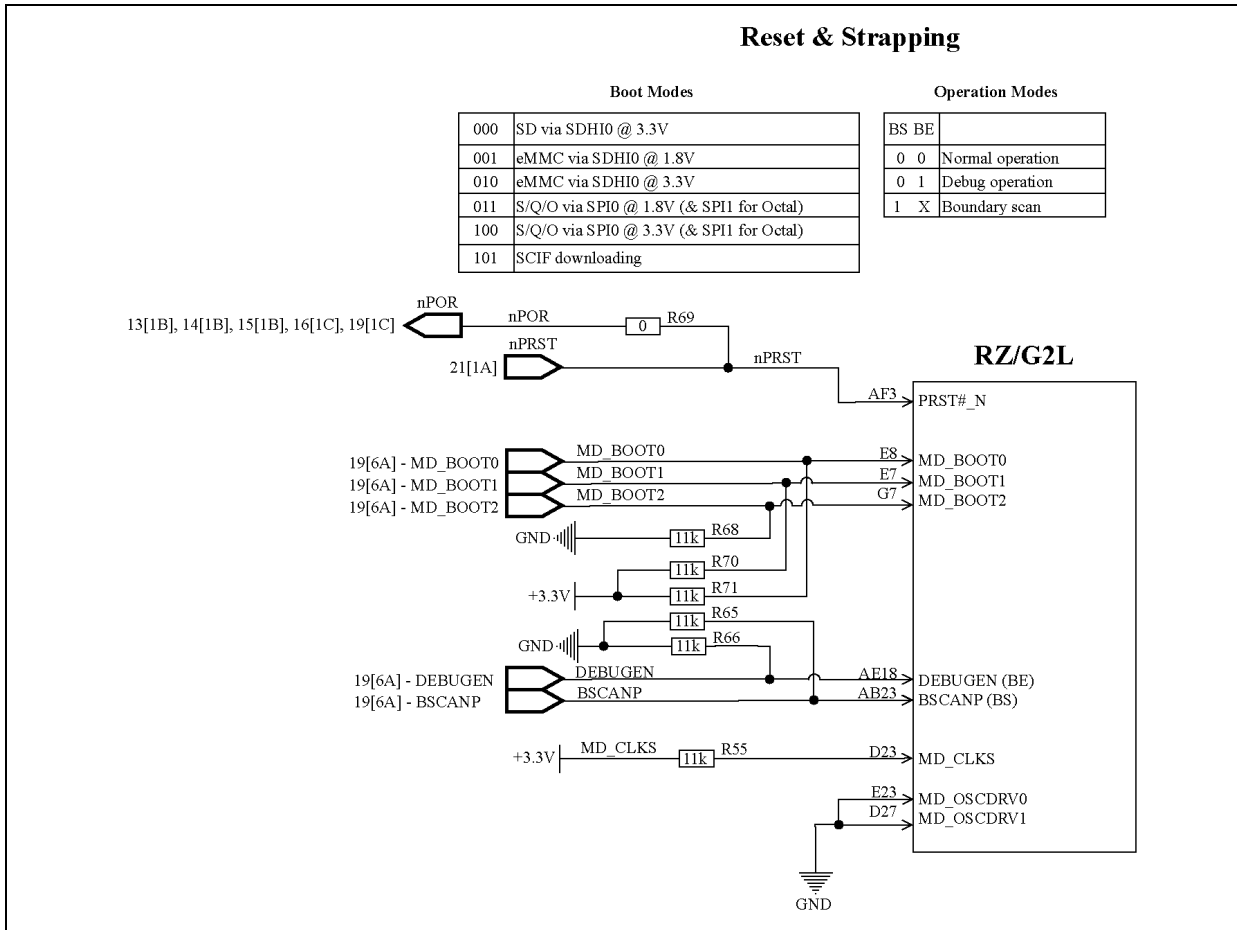
Figure 11: Block diagram of PMIC interface to RZ/G2L

### 4.4 RESET Control

The RZ/G2L-SBC has a simplified PoR behavior. It's by default set up to boot from QSPI0 which is achieved through external pull-up and pull-down resistors to a default code of 011. The default boot mode of 011 is for booting from QSPI0 but setting the operating voltage to 1.8V. The bootstrapping lines can be accessed externally through J12 port in the bottom (through an adapter board). This makes it possible to alter the boot flow using these pins.

In addition to the boot order, the SoC has two more lines DEBUGEN (BE) & BSCANP (BS). These lines control the boot mode which can be JTAG boundary scan or a debug mode. The figure below shows all the necessary information.

**Note:** Debug mode and boundary scan are mutually exclusive. Only one of DEBUGEN / BSCANP can be active at a time. Never enable both.



**Figure 12: Reset Control Logic**

### 4.5 Clock Configuration

The RZ/G2L-SBC design uses a Renesas VersaClock-3S as a singular programmable clock generator as the master clock source for the entire board. It drives the source clock for not just the RZ/G2L-SoC but all other devices that use an external clock input. This reduces the design complexity by reducing the use of passives and PLL's per peripheral while using a single 24 MHz crystal XTALL.

**Note:**

- ✓ MIPI DSI interface supports operation up to FHD @60 fps rates.
- ✓ SD Interface supports UHS-I mode of 50MBps (SDR50) and 104MBps (SDR104)

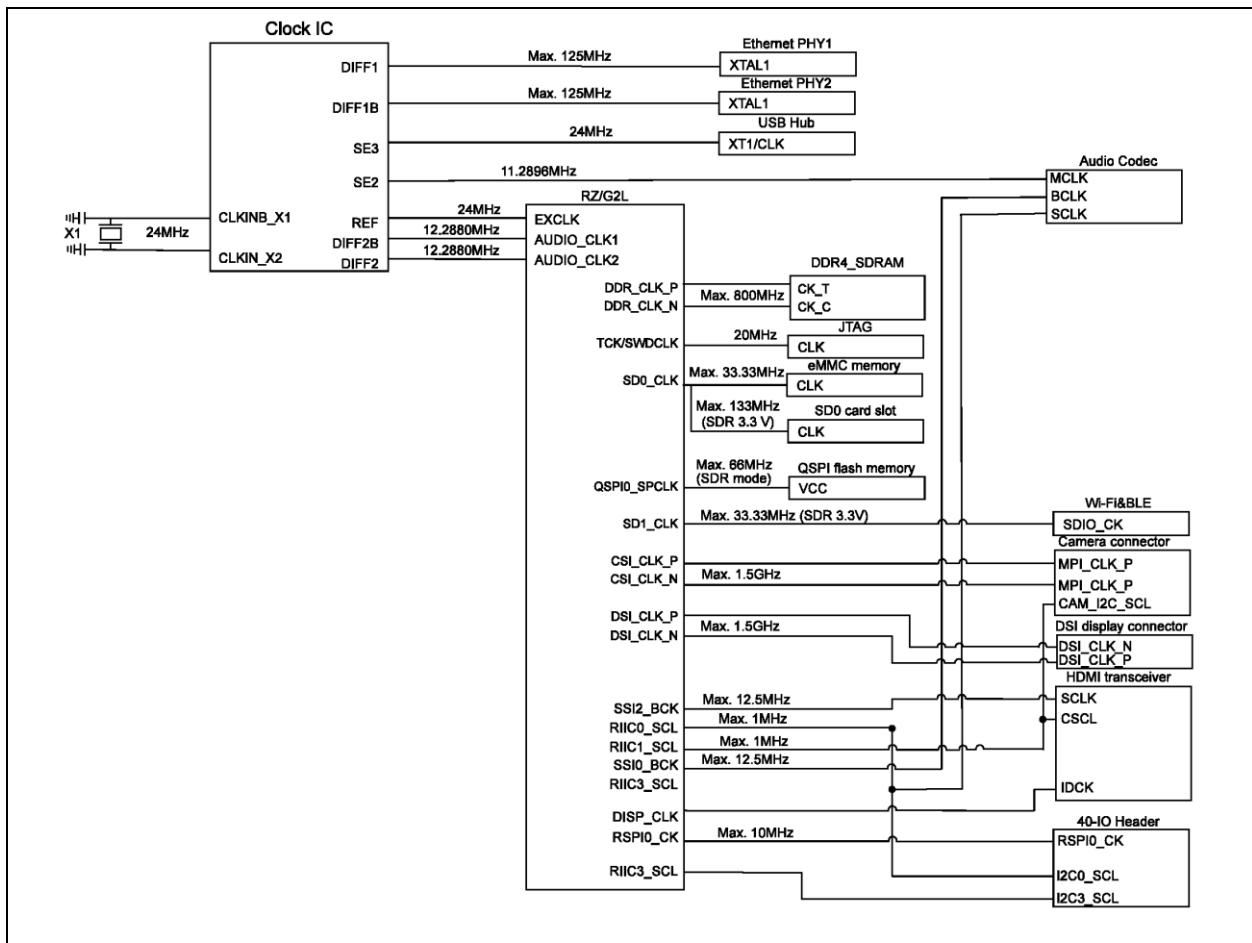


Figure 13: Block diagram of Clock interfacing.

## 4.6 Peripheral Interface

### 4.6.1 Gigabit Ethernet

The RZ/G2L-SBC comes with two Gigabit ethernet ports. They are identified as Eth 0 and Eth 1 in the Linux environment. They are both gigabits capable. The Gigabit Ethernet Interface is controlled by the Ethernet controller (E-MAC) that conforms to the definition of the MAC (Media Access Control) layer that is built-in to the RZ/G2L. The Ethernet clock is sourced from a clock generator connected to the Ethernet PHY.

This interface complies with IEEE802.3 PHY RGMII.

ETH0 is connected to PHY 2 and ETH1 is connected to PHY1. Please be mindful of the order.



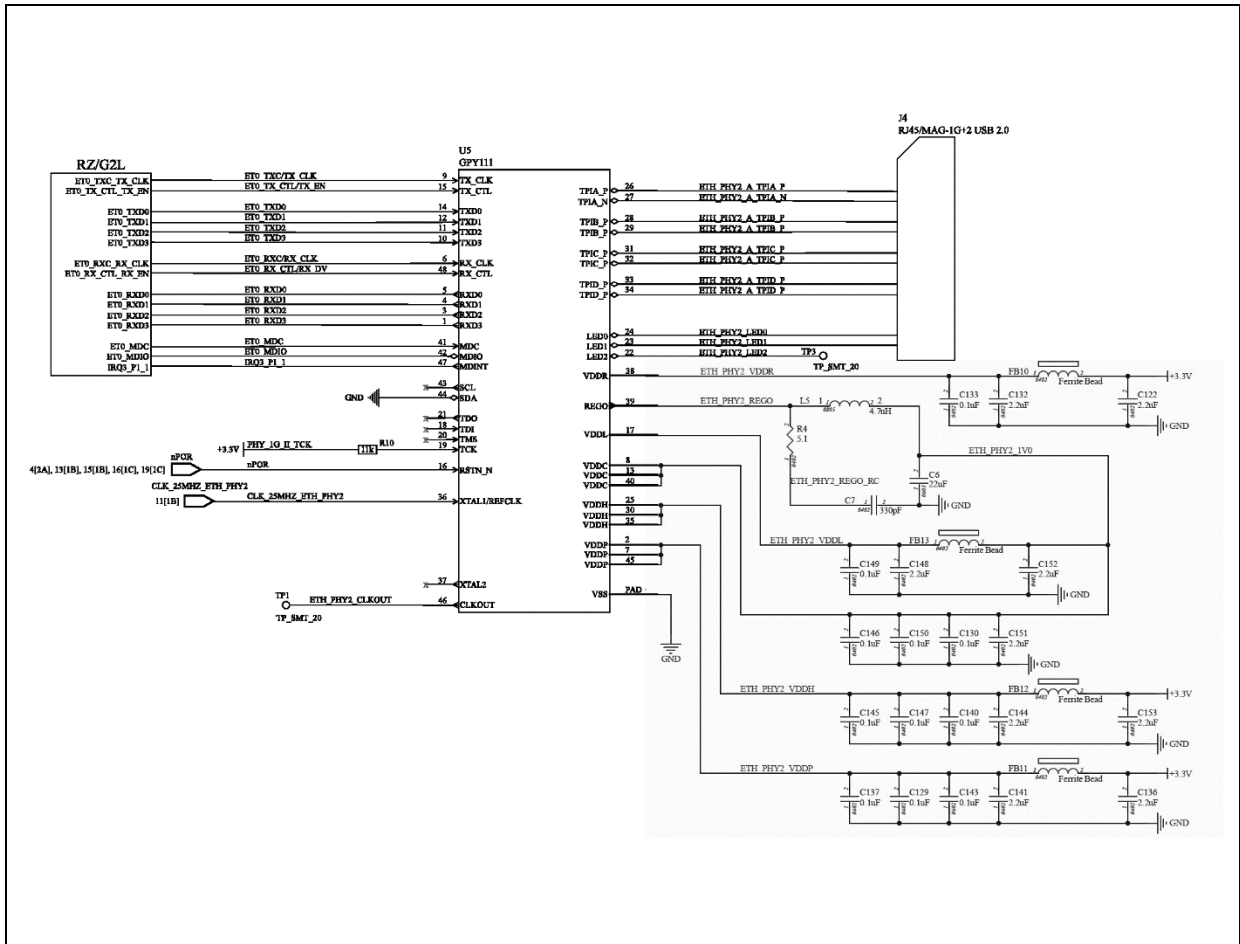


Figure 14: Ethernet 0 PHY interfacing.



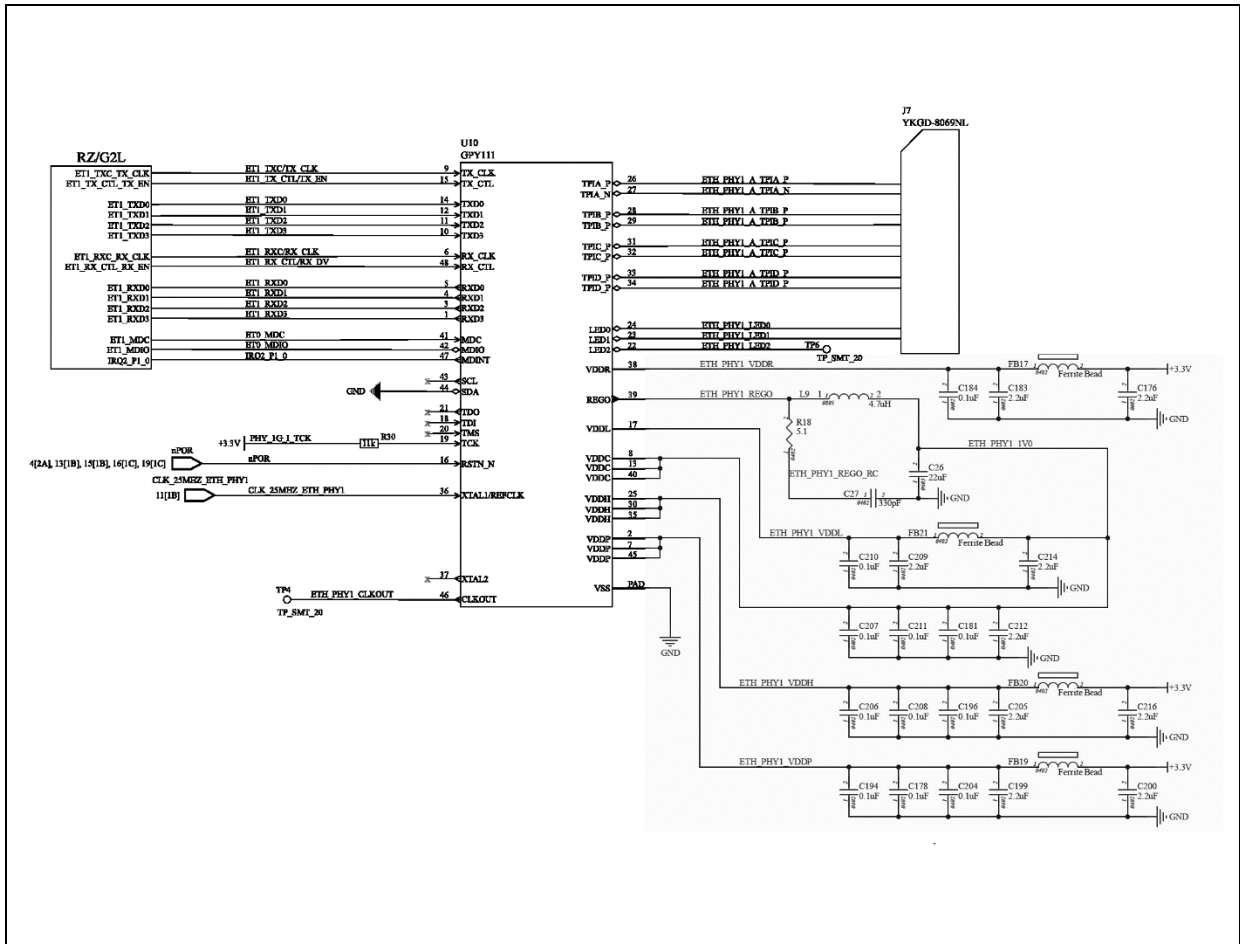


Figure 15: Ethernet 1 PHY interfacing.

### 4.6.2 USB 2.0 Ports

The SBC has 4 USB 2.0 ports which are of type A. The primary USB hub is the Renesas [UPD720115](#) ([μPD720115](#)) which is a 4-port hub conforming to USB battery charging specification version 1.2. It has one upstream port and 4 downstream ports. The USB hub is connected directly to the RZ/G2L SoC's USB 1 data ports. The RZ/G2L SoC has a single USB 2.0 Host Interface channel.

The USB 0 channel (OTG interface) is routed to the USB-C power supply port. However, the actual OTG lines are not connected, and only the data lines are routed to the USB-C port. When the board is powered through the 40-pin io or the bottom expansion connectors, it frees up the USB-C port. It can then be used for connecting peripherals. Please note that the USB-C has not been tested as a peripheral interface so far.

The power supply to the four USB 2.0 ports downstream is controlled through two external power regulators: Renesas [ISL6185](#). The ISL 6185 isolates and protects the internal circuit from the external USB peripheral while providing higher levels of 5V power through supply sourcing.

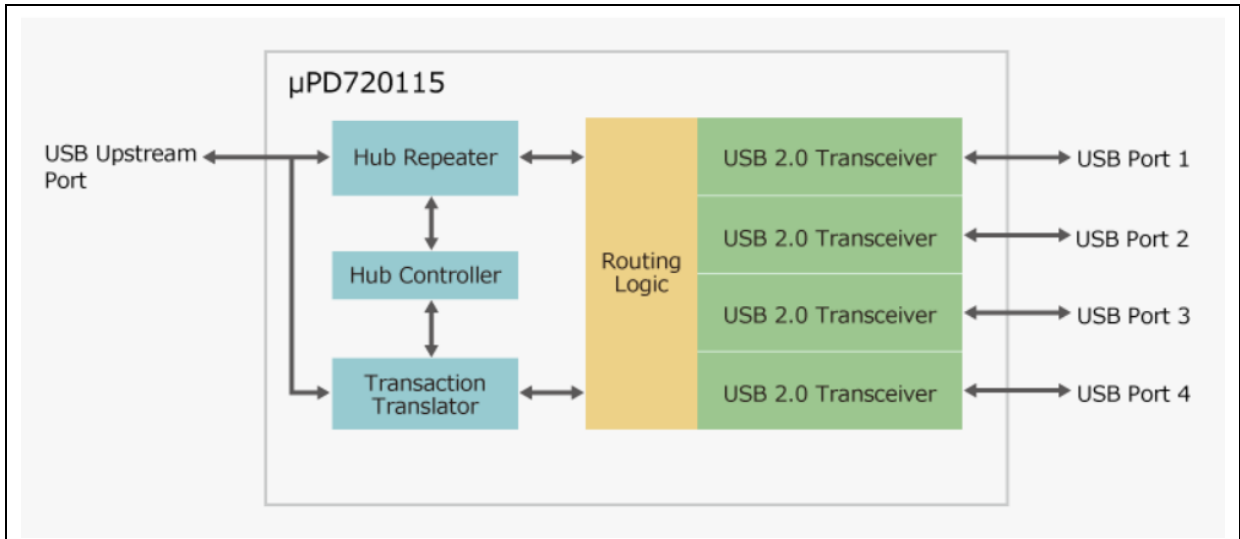


Figure 16: UPD720115 block diagram.

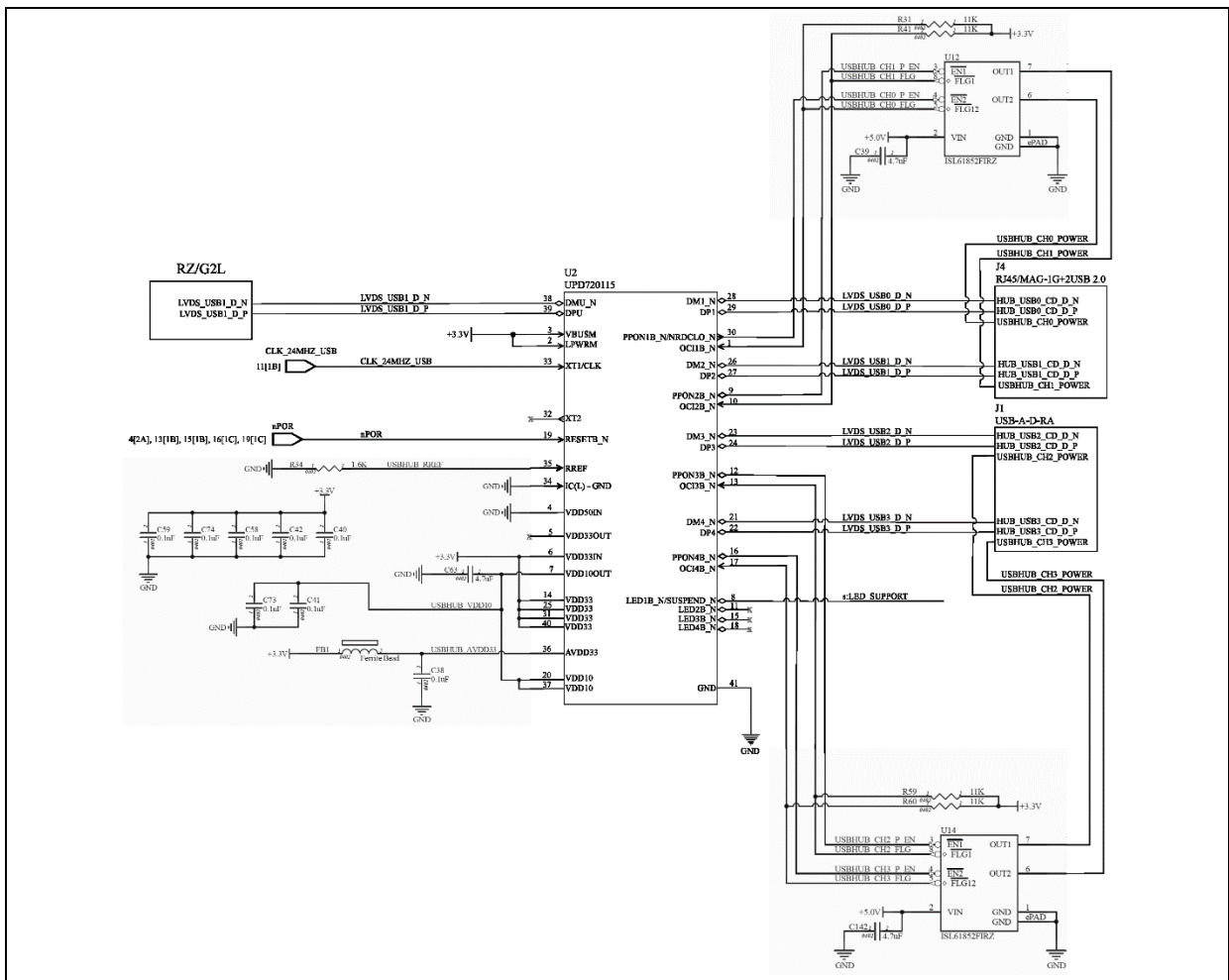


Figure 17: USB 2.0 Hub Block Diagram

### 4.6.3 MIPI CSI Interface

The RZ/G2L-SBC comes with a dual channel MIPI CSI port labelled as J6. It's located right next to the 3.5 mm audio jack. The CSI port 15 pin camera port is verified to work with OV5640 camera module. It supports two data channels and One I2C channel. It is directly interfaced to the RZ/G2L SoC.

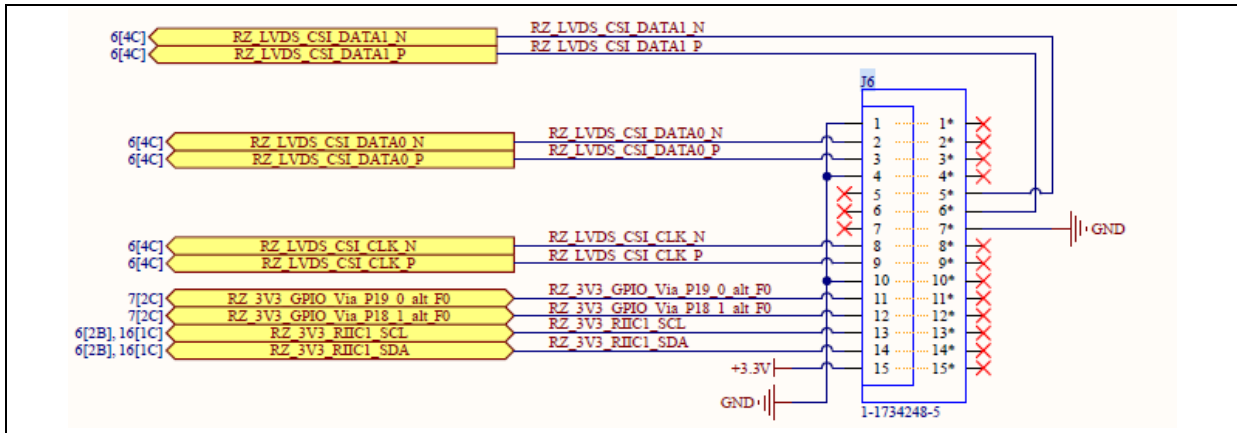


Figure 18: CSI Interface Schematic

### 4.6.4 MIPI DSI Interface

The RZ/G2L-SBC comes with a dual channel MIPI DSI port labelled as J5. It's located toward the edge of the board next to the Wi-Fi chipset. The 15-pin display port is verified to work with Waveshare 5" DSI display with a capacitive touch interface module. It supports two data channels and One I2C channel. It is directly interfaced to the RZ/G2L SoC.

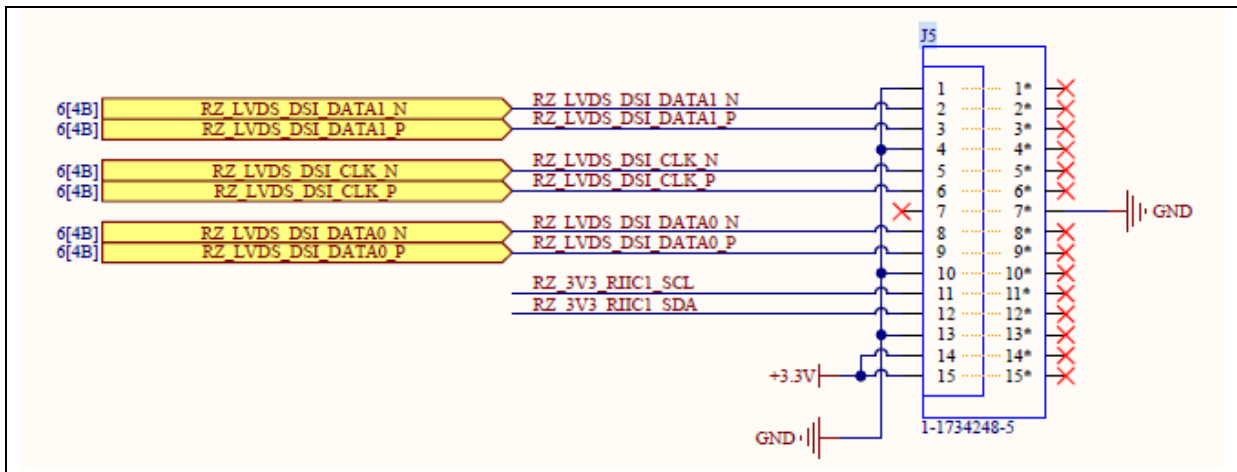


Figure 19: DSI Schematic

### 4.6.5 Audio DAC with 3.5mm Jack

The RZ/G2L-SBC comes with an onboard audio DAC from Renesas: DA7219. The audio DAC is interfaced to RZ/G2L SoC to its SS1 and I2C 0. The SSI 1 is used for audio streaming of I2S data while the I2C interface is used for mux and peripheral control.

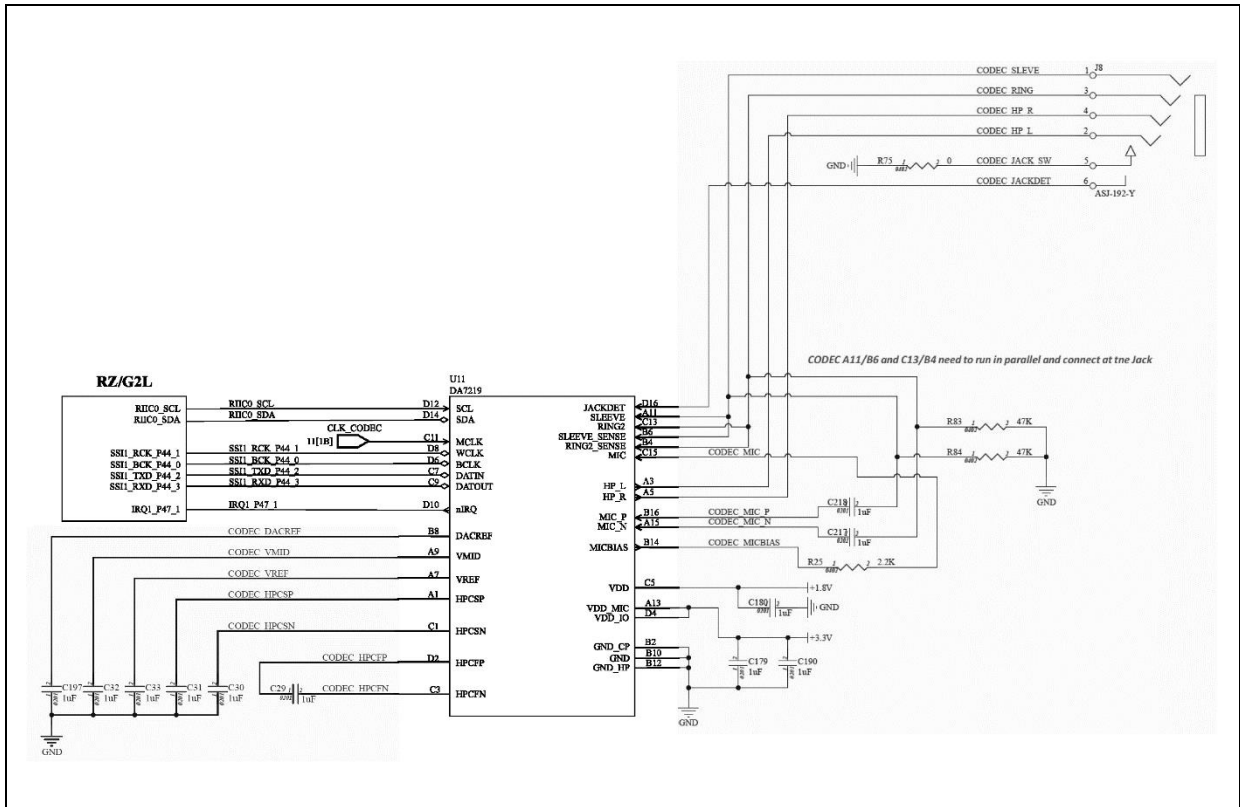


Figure 20: Audio CODEC Interface Block Diagram

### 4.6.6 HDMI Display Subsystem

The RZ/G2L-SBC comes with a HDMI display output which is derived from the RGB parallel interface from RZ/G2L SoC through an RGB to HDMI converter interface IC. The physical HDMI port is a mini-HDMI type (not micro). The HDMI signal source is the RGB parallel LVDS interface. A RGB to HDMI bridge IC is used to convert RGB to HDMI protocol. The bridge is fully supported, and the HDMI is enabled with EDID feature.

Note: The LVDS interface is source for both the external HDMI bridge as well as the on chip DSI IP blocks. So only one interface may be active at a time. Under no circumstances should both interfaces be turned on at the same time as there is limitation with regards to the ISP unit.

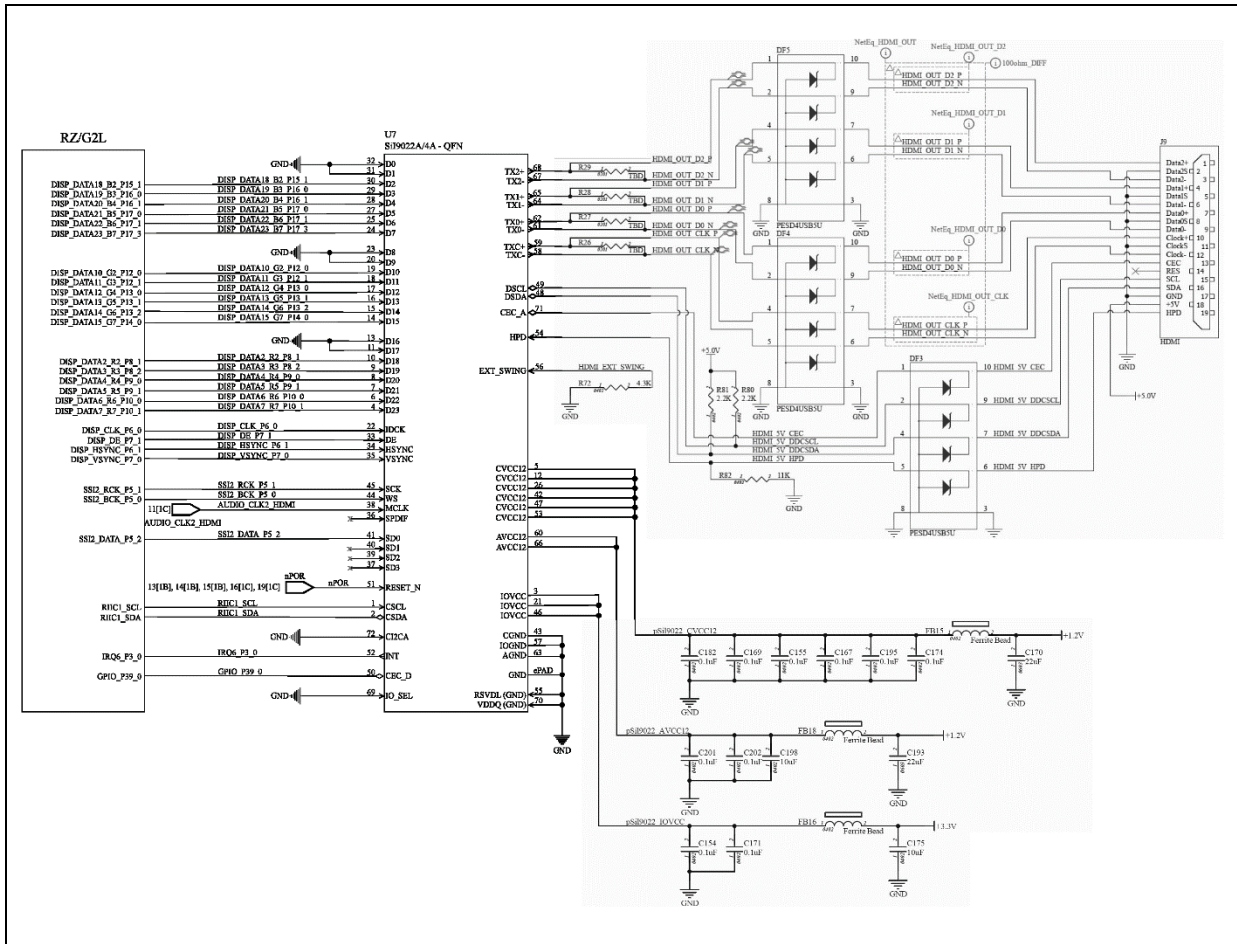


Figure 21: HDMI Bridge and mini HDMI port interfacing.

### 4.6.7 40-pin I/O Header

The RZ/G2L-SBC comes with a 40-pin GPIO interface which is broadly compliant with Raspberry Pi 3 40-pin GPIO interface and provides additional interfaces like two CAN ports. The diagram below shows the pin configuration along with marking of the bottom I/O ports for reference of the orientation of the board.



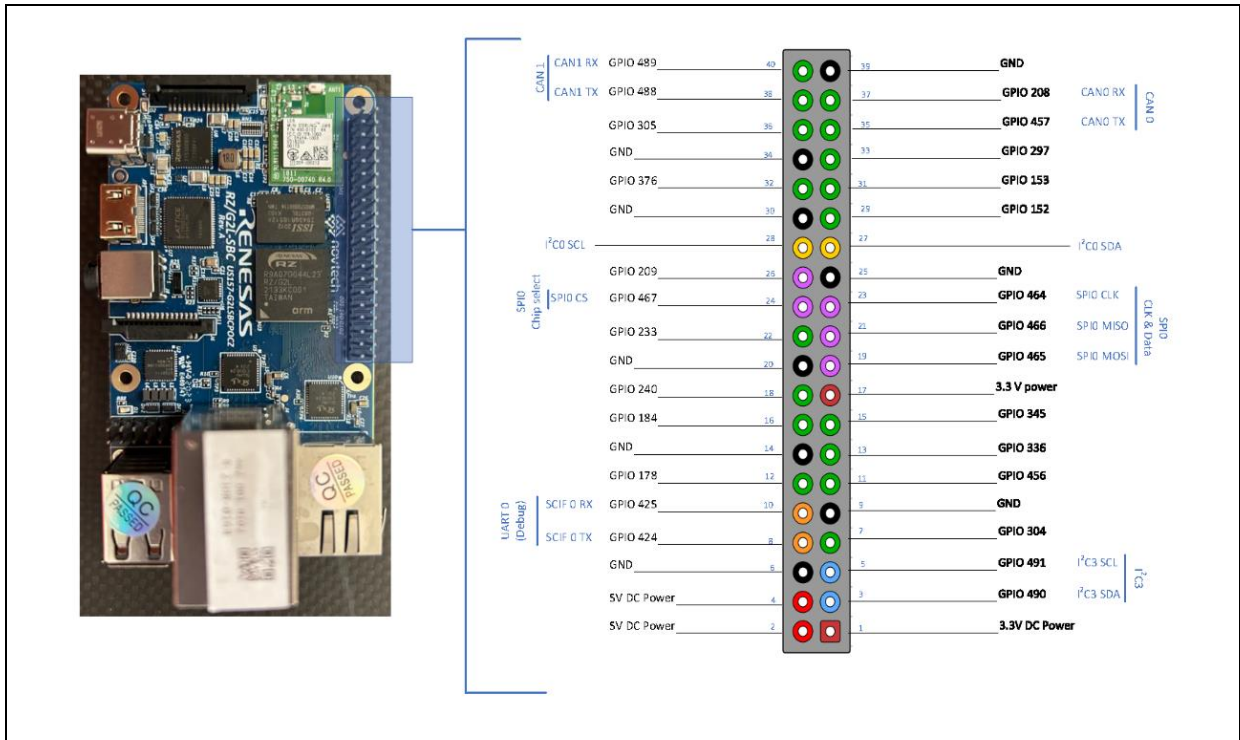


Figure 22: 40 PIN GPIO map with orientation details.

### 4.6.8 PMOD Type 6A Standard Interface

The RZ/G2L-SBC is equipped with a 2x6 pin header routed to the PMOD Type-6A interface conforming to the 1.3.0 specification of PMOD. It includes the alternate pin functions from the specification.

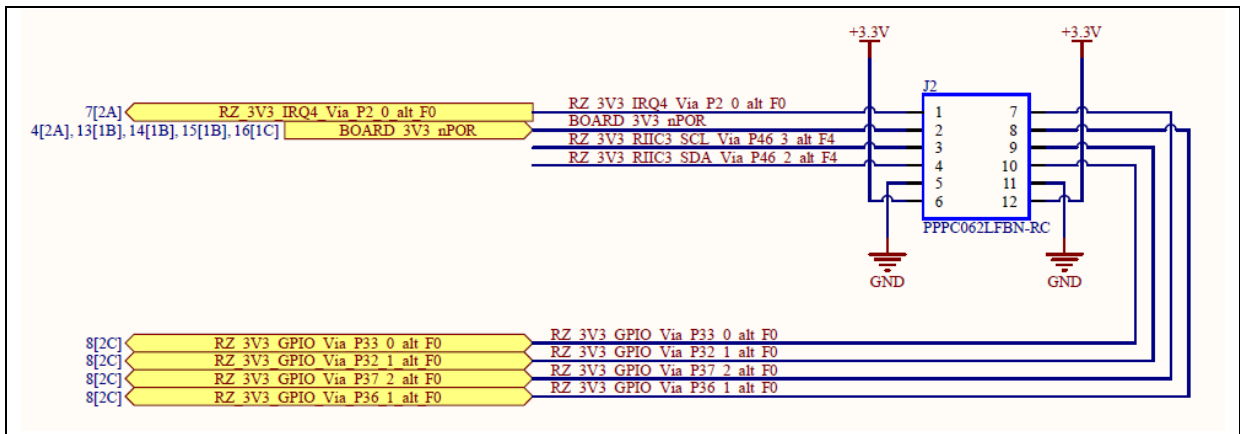


Figure 23: Schematic of PMOD Type 6 A pin header J2.

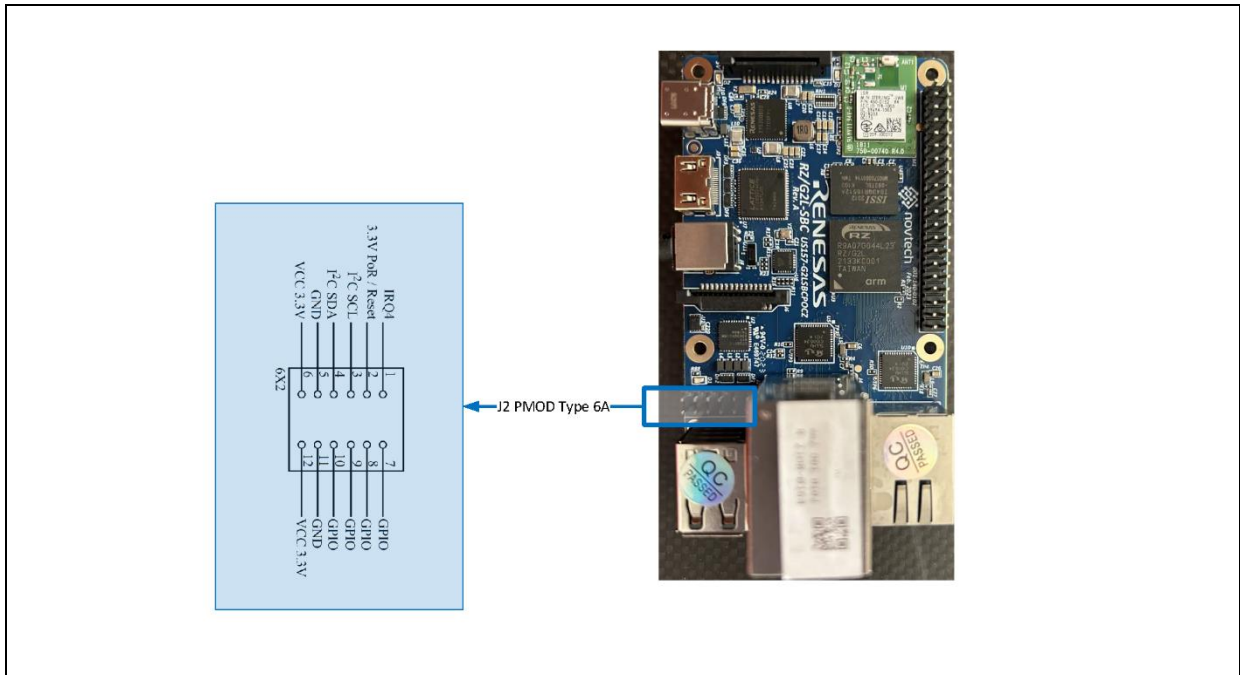


Figure 24: PMOD Type 6A 2x6 0.1mm pin out with orientation details.

### 4.6.9 uSD-Card Interface

The RZ/G2L-SBC comes with a spring-loaded micro-sd card slot. This is intended to be the primary storage as well as the OS boot device. The SD card is connected to channel 0 of the RZ/G2L SoC SD/MMC interface. The SoC SDIO interface is compliant with memory card standard version 3.0 and supports UHS-1 mode of 50 MB/s (SDR50) and 104 MB/s (SDR104).

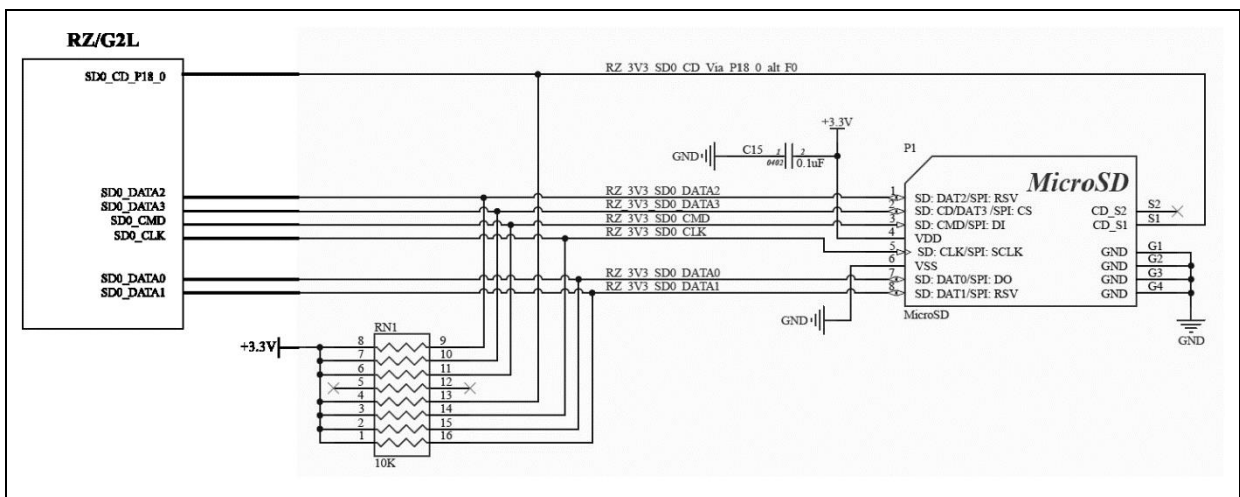


Figure 25: uSD-Card interface block diagram.

### 4.6.10 JTAG SWD Debug

The JTAG/SWD interface is an SMT pin out on the bottom side of the board marked as J11. It uses the standard 10-pin interfacing when populated. By default, this is not populated on the board. In addition to populating the pins of J11, the use of J12 port to set BSCANP is necessary to trigger JTAG boundary scan of the RZ/G2L SoC. The SBC by itself will not be able to initiate the JTAG boundary scan mode. All the interface lines have pullups.

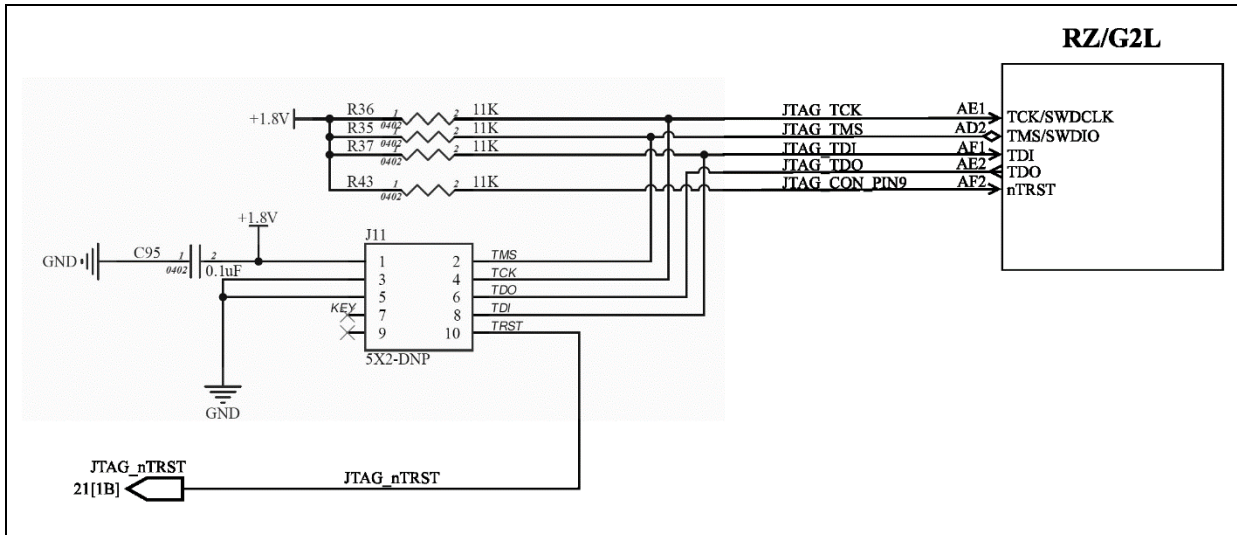


Figure 26: JTAG/SWD Block Diagram

### 4.6.11 Expansion Connector

The RZ/G2L-SBC has two connectors in the bottom J12 and J13 that contain pin outs for the ADC inputs, Bootstrapping (boot mode selection), and the QSPI1 interface in addition to a few GPIO's. This is meant to be used in conjunction with an adapter/daughter board. The primary uses of this are mostly on custom versions where factory flashing, and other manufacturing functions are controlled by these lines. The ADC input lines are also mapped to J13 connector.

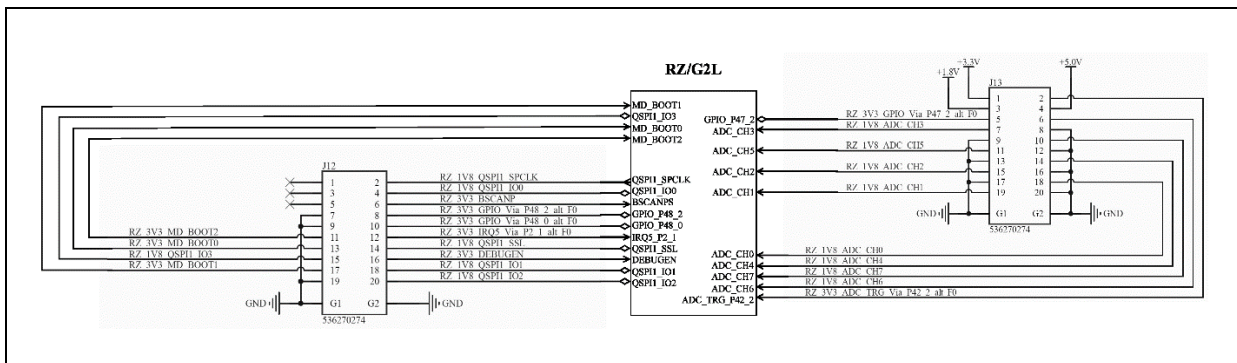


Figure 27: Block diagram of Bottom Connectors.

Please refer to the appendix for details on the adaptor board and flashing tools.

## 4.7 Memory

The RZ/G2L-SBC design uses 4 types of memory.

1. QSPI NOR Flash
2. DDR4 SDRAM
3. EEPROM
4. SD-Card

### 4.7.1 QSPI Flash

The QSPI flash memory is controlled by the SPI multi-I/O bus controller (SPIBSC) that is built into the RZ/G2L. This memory supports both single data rate (SDR) and double data rate (DDR) transfers at 66MHz and 50MHz clock frequency. QSPI0 interfaces to a Cypress S25FS512SDSNFB010 64MiB NOR



Flash module. The QSPI is the default boot device which contains the firmware: Arm Trusted Firmware (ATF), OPTEE (loaded but disabled by default) and U-Boot.

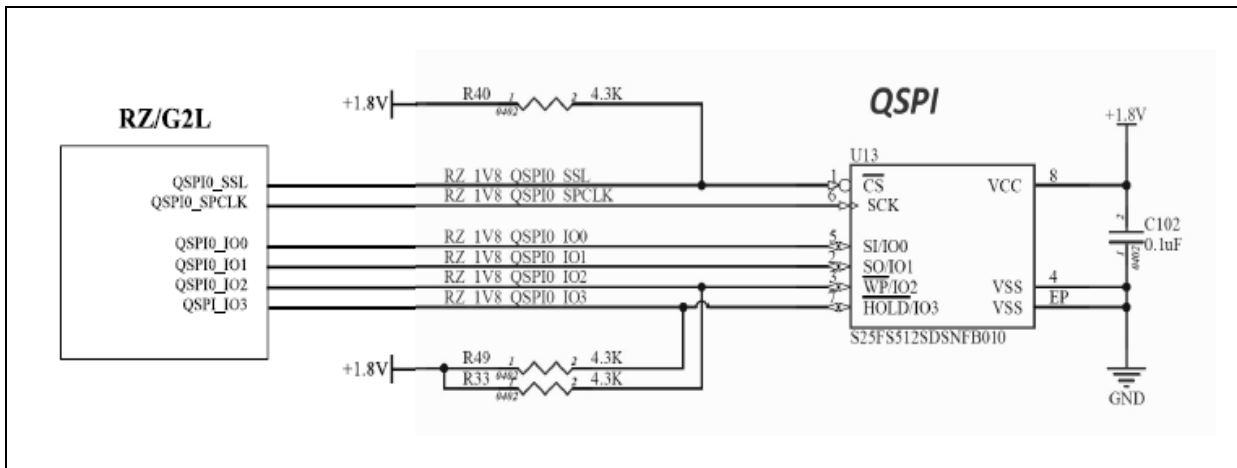


Figure 28: QSPI interface.

Note: The pull up resistor on clock line “QSPI0\_SPCLK” is optional and has been omitted in this design.

### 4.7.2 DDR4 SDRAM

The DDR4 SDRAM is controlled by the DDD3L/DDR4 SDRAM Memory Controller (MEMC) that is built-in to the RZ/G2L. This interface supports up to DDR4-1600 SDRAM, a data bus width of 16-bit, and inline ECC.

This interface complies with JEDEC STANDARD JESD79-4C.

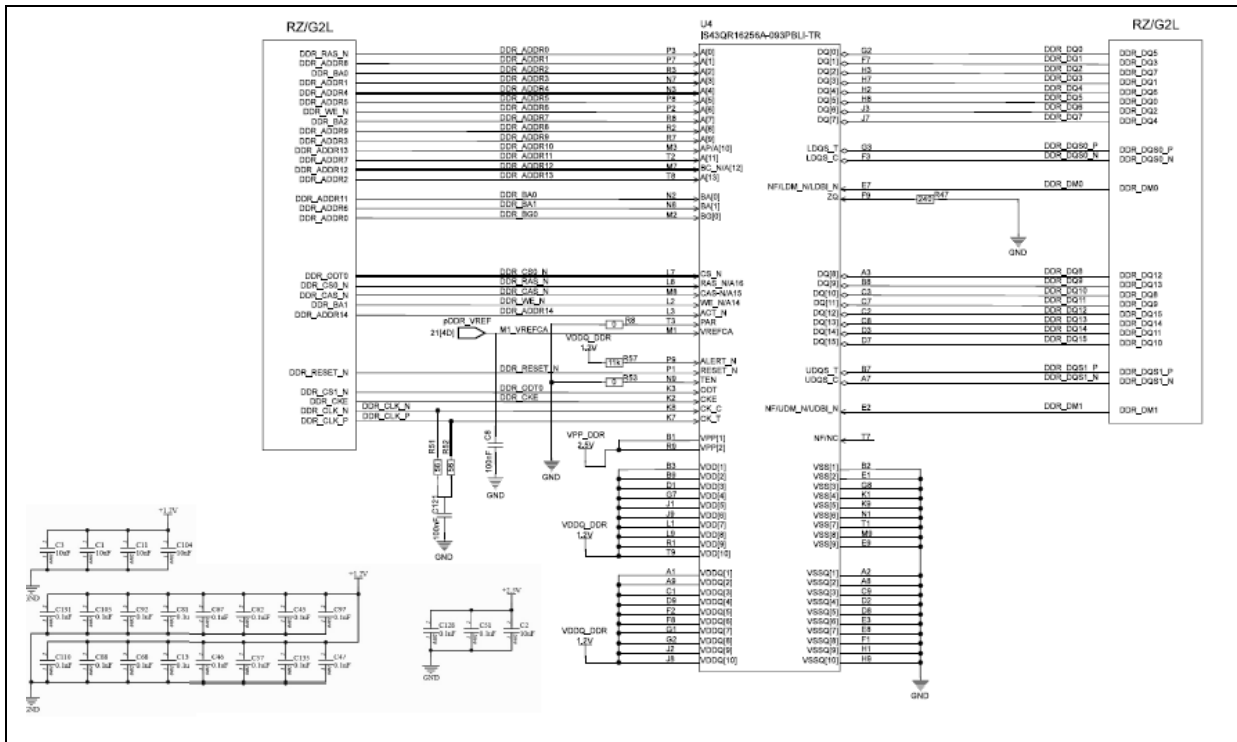
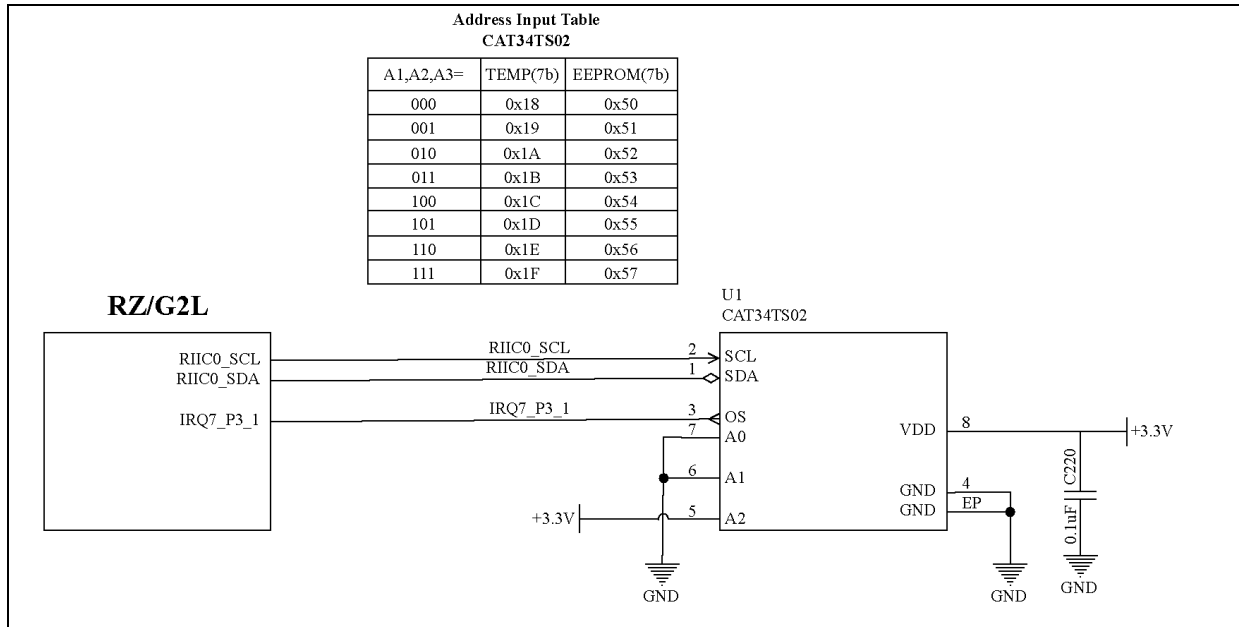


Figure 29: DDR4 SDRAM Interface

### 4.7.3 EEPROM with temperature sensor.

The RZ/G2L-SBC has an onboard [CAT34TS02](#) I<sup>2</sup>C Temperature sensor with on-chip EEPROM, which is meant to hold factory data like Serial number, manufacturer name, etc. It is currently only used to hold the ethernet MAC ID's. Please note that each board has its own registered MAC ID, which is stored on the EEPROM and read by u-boot during bootup. The EEPROM also has a built-in temperature sensor that can be read over the I<sup>2</sup>C interface. The EEPROM is configured as 16 pages of 16 bytes each for a total of 256 KiB (2 kilobits) of memory. Currently, two MAC IDs occupy 6 bytes of memory each for a total of 12 bytes.



**Figure 30: I2C EEPROM Block Diagram**

| Parameter              | Value                              | Description   |
|------------------------|------------------------------------|---|
| I <sup>2</sup> C speed | 100KHz / 400 KHz                   | It supports the standard and fast modes of operation.   |
| EEPROM memory size     | 2 kib / 256 bytes                  |   |
| EEPROM memory ordering | 16 pages of 16 bytes each          | Page bank array configuration   |
| Temperature range      | -20 °C to +125 °C                  |   |
| Operating Voltage      | 3.3V                               |   |
| Temperature alarm      | Programmable over I <sup>2</sup> C | Three programmable trigger settings for high, low and critical temperatures to raise interrupt over line IRQ 7. |

### 4.8 GPIO Internals

The RZ/G2L SoC has a unique way of GPIO organization. It's not the typical banked GPIO interface that one might be used to. The RZ/G2L has individual GPIO LSI logic directly attached to the register outputs. This creates a notation for GPIO pins attached to ports which are basically bits in a register.

Px\_y :

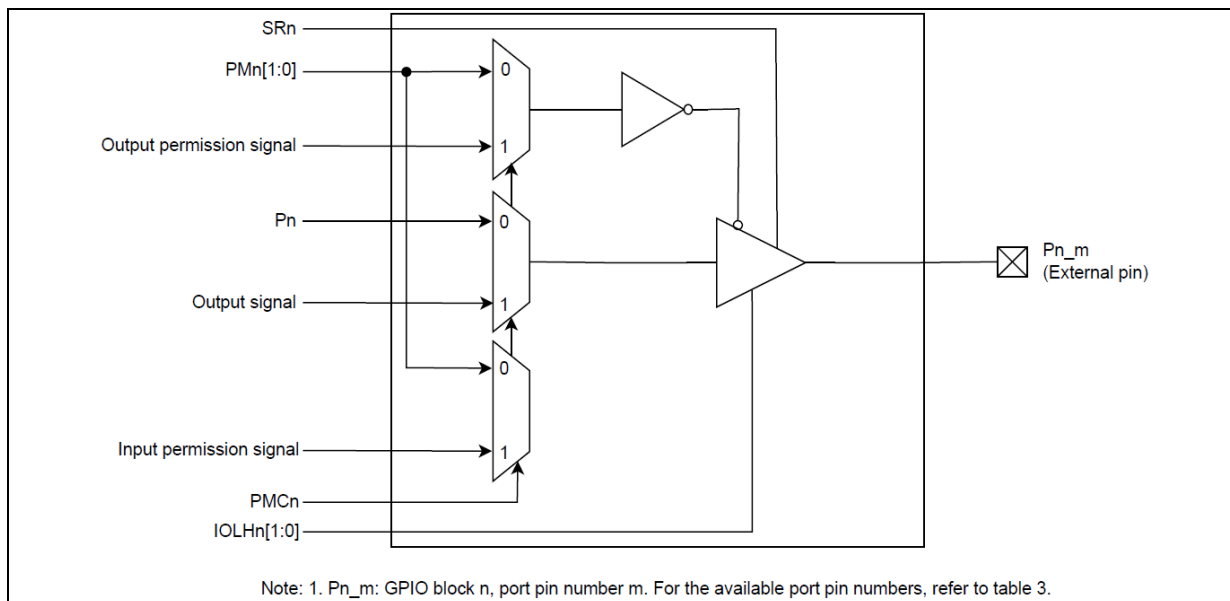
P= port a.k.a 8 bit register set number.

x= port number

y= port bit

Each bit in a port control register corresponds to a single gpio logic module. While each port has 8 bits, most of the ports (registers) are only using the lower two to three bits for gpio line outs. The

upper bits are used for other special functions at times. The table below maps all the available ports to bits.



**Figure 31: Multiplexed peripheral functions configuration diagram for GPIO pins**

RZ/G2L can support up to 123 general-purpose I/O pins from 49 ports in the following table:

**Table 3: GPIO-supported pins in RZ/G2L**

| Port name | External Terminal Name |      |      |       |       |       |
|-----------|------------------------|------|------|-------|-------|-------|
|           | Bit7-5                 | Bit4 | Bit3 | Bit2  | Bit1  | Bit0  |
| PORT 10   | -                      | -    | -    | -     | P0_1  | P0_0  |
| PORT 11   | -                      | -    | -    | -     | P1_1  | P1_0  |
| PORT 12   | -                      | -    | -    | -     | P2_1  | P2_0  |
| PORT 13   | -                      | -    | -    | -     | P3_1  | P3_0  |
| PORT 14   | -                      | -    | -    | -     | P4_1  | P4_0  |
| PORT 15   | -                      | -    | -    | P5_2  | P5_1  | P5_0  |
| PORT 16   | -                      | -    | -    | -     | P6_1  | P6_0  |
| PORT 17   | -                      | -    | -    | P7_2  | P7_1  | P7_0  |
| PORT 18   | -                      | -    | -    | P8_2  | P8_1  | P8_0  |
| PORT 19   | -                      | -    | -    | -     | P9_1  | P9_0  |
| PORT 1A   | -                      | -    | -    | -     | P10_1 | P10_0 |
| PORT 1B   | -                      | -    | -    | -     | P11_1 | P11_0 |
| PORT 1C   | -                      | -    | -    | -     | P12_1 | P12_0 |
| PORT 1D   | -                      | -    | -    | P13_2 | P13_1 | P13_0 |
| PORT 1E   | -                      | -    | -    | -     | P14_1 | P14_0 |
| PORT 1F   | -                      | -    | -    | -     | P15_1 | P15_0 |
| PORT 20   | -                      | -    | -    | -     | P16_1 | P16_0 |
| PORT 21   | -                      | -    | -    | P17_2 | P17_1 | P17_0 |
| PORT 22   | -                      | -    | -    | -     | P18_1 | P18_0 |
| PORT 23   | -                      | -    | -    | -     | P19_1 | P19_0 |
| PORT 24   | -                      | -    | -    | P20_2 | P20_1 | P20_0 |
| PORT 25   | -                      | -    | -    | -     | P21_1 | P21_0 |
| PORT 26   | -                      | -    | -    | -     | P22_1 | P22_0 |
| PORT 27   | -                      | -    | -    | -     | P23_1 | P23_0 |
| PORT 28   | -                      | -    | -    | -     | P24_1 | P24_0 |
| PORT 29   | -                      | -    | -    | -     | P25_1 | P25_0 |
| PORT 2A   | -                      | -    | -    | -     | P26_1 | P26_0 |
| PORT 2B   | -                      | -    | -    | -     | P27_1 | P27_0 |
| PORT 2C   | -                      | -    | -    | -     | P28_1 | P28_0 |
| PORT 2D   | -                      | -    | -    | -     | P29_1 | P29_0 |
| PORT 2E   | -                      | -    | -    | -     | P30_1 | P30_0 |
| PORT 2F   | -                      | -    | -    | -     | P31_1 | P31_0 |
| PORT 30   | -                      | -    | -    | -     | P32_1 | P32_0 |

|         |   |       |       |       |       |       |
|---------|---|-------|-------|-------|-------|-------|
| PORT 31 | - | -     | -     | -     | P33_1 | P33_0 |
| PORT 32 | - | -     | -     | -     | P34_1 | P34_0 |
| PORT 33 | - | -     | -     | -     | P35_1 | P35_0 |
| PORT 34 | - | -     | -     | -     | P36_1 | P36_0 |
| PORT 35 | - | -     | -     | P37_2 | P37_1 | P37_0 |
| PORT 36 | - | -     | -     | -     | P38_1 | P38_0 |
| PORT 37 | - | -     | -     | P39_2 | P39_1 | P39_0 |
| PORT 38 | - | -     | -     | P40_2 | P40_1 | P40_0 |
| PORT 39 | - | -     | -     | -     | P41_1 | P41_0 |
| PORT 3A | - | P42_4 | P42_3 | P42_2 | P42_1 | P42_0 |
| PORT 3B | - | -     | P43_3 | P43_2 | P43_1 | P43_0 |
| PORT 3C | - | -     | P44_3 | P44_2 | P44_1 | P44_0 |
| PORT 3D | - | -     | P45_3 | P45_2 | P45_1 | P45_0 |
| PORT 3E | - | -     | P46_3 | P46_2 | P46_1 | P46_0 |
| PORT 3F | - | -     | P47_3 | P47_2 | P47_1 | P47_0 |
| PORT 40 | - | P48_4 | P48_3 | P48_2 | P48_1 | P48_0 |

-: unused pins

Note: Please note that the RZ/G2L has only 1 gpiochip interface to control all the supported pins mentioned in the table 3.

## 5. Yocto OE Build

This section describes how to prepare a host system, download dependencies, and then perform a full yocto build. The following sub-sections are step-by-step process of performing a successful yocto build.

### 5.1 Build Host Environment Setup

#### Requirements

- Ubuntu 20.04 LTS (64bit) is recommended as a build environment as we are using 'Dunfell' version.
- Development packages for Yocto:  
Refer to official Yocto documentation ([Yocto Project Documentation](#)) to get started.  
Refer to the official Yocto quick build guide ([Yocto Project Quick Build — The Yocto Project® 3.1.27 documentation](#)) for a quick start.

The files listed in the table below are part of the release package. These are essential files to be used for the RZ/G2L-SBC Yocto build.

| File            | Description   |
|-----------------|---|
| rzsbcb_yocto.sh | Custom Yocto build script that downloads the base yocto package and other downloaded zip files, arranges the layers, applies relevant meta layers, sets up the environment and initiates a build. |
| site.conf       | An override file that targets for a specific build version.   |
| README.md       | A readme file describing all the necessary info about the build process.  |

**Table 4: Pre-requisite files from release package**

#### Install packages on Ubuntu Host.

1. Update the ubuntu package manager.

```
$ sudo apt update
```

2. Install necessary packages and tools which are used by the yocto build.

```
$ sudo apt install -y gawk wget git-core diffstat unzip texinfo gcc-multilib \
build-essential chrpath socat cpio python python3 python3-pip python3-pexpect \
xz-utils debianutils iputils-ping libssl1.2-dev xterm p7zip-full libyaml-dev \
rsync curl locales bash-completion
```

3. Configure local git account for the user.

```
$ git config --global user.name "Your Name"
$ git config --global user.email "you@example.com"
```

4. Download the following packages provided by Renesas.

| File name                        | Version | Download Link   | Comments   |
|----------------------------------|---------|---|--|
| RTK0EF0045Z13001ZJ-v1.1.2_EN.zip | 1.1.2   | <a href="#">rz-mpu-graphics-library-evaluation-version</a>    | This is the Mali driver and graphics package that enables the Mali GPU in the SoC. |
| RTK0EF0045Z15001ZJ-v1.1.0_EN.zip | 1.1.0   | <a href="#">rz-mpu-video-codec-library-evaluation-version</a> | Video codec package  |

**Table 5: List of packages to manually download for Yocto Build**

5. We assume that all the downloaded zip files from Table 5 are collected at the path 'Downloads/renesas-yocto' in the user's home directory creating paths '~/.Downloads/renesas-yocto/\*.zip'. If your locations are different, you must substitute the appropriate paths in the following steps.

- Copy all the above downloaded zip files to a build folder (For e.g., '~/.yocto' as shown below) in Ubuntu Host PC.

```
$ cd ~/Downloads/rz-sbc
$ mkdir ~/.yocto
$ mv *.zip ~/.yocto
```

- Copy the file 'rzsbc\_yocto.sh', **site.conf** and the file 'README.md' from the release package into '~/.yocto' folder. (This example assumes the Pre-requisite files that are described in Table 4 are located at package unpacked location ~/Downloads/Renesas-yocto/ rz-sbc-qt-v1.0)

```
$ cd ~/Downloads/renesas-yocto/ rz-sbc-qt-v1.0/src
$ cp README.md ~/.yocto
$ cp rzsbc_yocto.sh ~/.yocto
$ cp site.conf ~/.yocto
```

- Eventually, all the necessary files for the yocto build should be present in '~/.yocto' folder as shown below.

```
renesas@builder-pc:~/.yocto$ ls -l
README.md
RTK0EF0045Z13001ZJ-v1.1.2_EN.zip
RTK0EF0045Z15001ZJ-v1.1.0_EN.zip
rzsbc_yocto.sh
site.conf
```

## 5.2 Initiate Yocto Build

Add execute permission to rzsbc\_yocto.sh.

```
renesas@builder-pc:~/.yocto$ chmod a+x rzsbc_yocto.sh
```

Commence build:

```
renesas@builder-pc:~/.yocto$ ./rzsbc_yocto.sh build
```

Note: Please note that this build requires internet access and will take several hours. Use a build system with high core count, lot of RAM memory and a fast SSD to have quicker builds.

## 5.3 Collect the build output

After building Yocto, the output folder should be located at:

```
~/Yocto/yocto_rzsbc_board/build/tmp/deploy/images/rzpi`
```

The output folder outline should look as follows:

```
renesas@builder-
pc:~/yocto/yocto_rzsbc_board/build/tmp/deploy/images/rzpi$ tree
.
├── b12_bp-rzpi.bin
├── b12_bp-rzpi.srec
├── b12-rzpi.bin
├── bootloader_flash.py
├── bootloader-windows-script
│   ├── config.ini
│   └── flash_bootloader.bat
```

```
|— images
|   |— bl2_bp-rzpi.srec
|   |— fip-rzpi.srec
|   |— Flash_Writer_SCIF_rzpi.mot
|— Readme.txt
|— tools
|   |— cygterm.cfg
|   |— flash_bootloader.ttl
|   |— TERATERM.INI
|   |— ttermpro.exe
|   |— ttpcmn.dll
|   |— ttpfile.dll
|   |— ttpmacro.exe
|   |— ttpset.dll
|   |— ttxssh.dll
|— core-image-qt.env
|— core-image-qt-rzpi-20240315151046.rootfs.manifest
|— core-image-qt-rzpi-20240315151046.rootfs.tar.bz2
|— core-image-qt-rzpi-20240315151046.rootfs.wic
|— core-image-qt-rzpi-20240315151046.testdata.json
|— core-image-qt-rzpi.manifest -> core-image-qt-rzpi-
20240315151046.rootfs.manifest
|— core-image-qt-rzpi.tar.bz2 -> core-image-qt-rzpi-
20240315151046.rootfs.tar.bz2
|— core-image-qt-rzpi.testdata.json -> core-image-qt-rzpi-
20240315151046.testdata.json
|— core-image-qt-rzpi.wic -> core-image-qt-rzpi-20240315151046.rootfs.wic
|— filesystem-windows-script
|   |— config.ini
|   |— flash_filesystem.bat
|   |— images
|   |   |— core-image-qt-rzpi.wic
|   |— README.md
|   |— tools
|   |   |— AdbWinApi.dll
|   |   |— cygterm.cfg
|   |   |— fastboot.bat
|   |   |— fastboot.exe
|   |   |— flash_system_image.ttl
|   |   |— TERATERM.INI
|   |   |— ttermpro.exe
|   |   |— ttpcmn.dll
|   |   |— ttpfile.dll
|   |   |— ttpmacro.exe
|   |   |— ttpset.dll
|   |   |— ttxssh.dll
|— fip-rzpi.bin
```

```
|— fip-rzpi.srec
|— Flash_Writer_SCIF_rzpi.mot
|— Image -> Image--5.10.184-cip36+gitAUTOINC+5cf70d0c96-r1-rzpi-
20240315131812.bin
|— Image--5.10.184-cip36+gitAUTOINC+5cf70d0c96-r1-rzpi-20240315131812.bin
|— overlays
|   |— rzpi-can.dtbo
|   |— rzpi-dsi.dtbo
|   |— rzpi-ext-i2c.dtbo
|   |— rzpi-ext-spi.dtbo
|   └─ rzpi-ov5640.dtbo
|— README.md
|— rzpi--5.10.184-cip36+gitAUTOINC+5cf70d0c96-r1-rzpi-20240315131812.dtb
|— rzpi.dtb -> rzpi--5.10.184-cip36+gitAUTOINC+5cf70d0c96-r1-rzpi-
20240315131812.dtb
|— sd_flash.sh
|— uEnv.txt
└─ uload-bootloader
    |— bl2_bp-rzpi.bin
    |— fip-rzpi.bin
    |— uload_bootloader_flash.py
    |— uload-bootloader-windows-script
    |   |— config.ini
    |   |— Readme.txt
    |   └─ tools
    |       |— cygterm.cfg
    |       |— TERATERM.INI
    |       |— ttermpro.exe
    |       |— ttpcmn.dll
    |       |— ttpfile.dll
    |       |— ttpmacro.exe
    |       |— ttpset.dll
    |       |— ttxssh.dll
    |       └─ uload-flash_bootloader.ttl
    └─ uload-flash_bootloader.bat
        └─ uload-readme.txt

10 directories, 75 files
```



## 6. Creating bootable SD card

This section describes all the tools and methods for creating the Linux bootable SD card under different environments.

### 6.1 Linux Host

This section explores the SD-flashing tools available in the Linux environment.

There is a helper script `sd\_flash.sh` in the root directory of the Yocto build output / release directory for this purpose.

Run the following command to learn how to use the script:

```
$ ./sd_flash.sh
```

The script needs an argument to run successfully. The argument is the device to be flashed the rootfs into. In this case, the device needs to flash its SD card. You will have to identify the correct device name which represents the SD card on Linux.

The below example shows how to identify an SD card on Ubuntu 22.0.4. The command 'lsblk' is executed to check all available storage devices. You can see that the 32GB SD card is being represented under the device name 'sdb' in the result (its full name is /dev/sdb). The command also shows you where the drive partitions are mounted in the filesystem.

```
$ lsblk
NAME        MAJ:MIN RM   SIZE RO TYPE MOUNTPOINTS
sda         8:0     0 119.2G 0 disk
├─sda1      8:1     0   976M 0 part /boot
├─sda2      8:2     0   977M 0 part [SWAP]
├─sda3      8:3     0   977M 0 part /boot/efi
└─sda4      8:4     0 116.4G 0 part /var/snap/firefox/common/host-hunspell
sdb         8:16    1   31.6G 0 disk
nvme0n1    259:0   0   1.1T 0 disk /data1
```

Please identify the device name of the sd-card to be flashed. Then, pass it to the script as argument as shown in the example here:

```
$ ./sd_flash.sh /dev/sdb
```

After executing SD card flashing script successfully, the SD card is automatically unmounted.

Note: Due to the various Linux distributions having different disk management arrangements, the script may fail to create the card. Hence, we are unable to assure that the script will work in every Linux environment. In the case where it fails, you might need to modify the call for creating the filesystem like the calls to ext4fs in the script. Please pay attention to the script and ensure that it succeeds.

The script is tested on ubuntu 22.0.4.

### 6.2 Windows Host

The preferred way to flash the image onto the SD card is to simply use Balaena etcher to flash the: core-image-qt-rzpi.wic image file onto the SD-card. You can use any etcher that can create bootable media

## 7. Programming / Flashing Firmware to RZ/G2L-SBC

The RZ/G2L-SBC comes with the most recent firmware images. However, there might be cases where a firmware update may be needed, such as in a factory setting where volume flashing is being performed or a custom version designed by the end user. The Renesas BSP provides firmware update tools to make it seamless to perform these tasks under multiple OS environments.

The RZ/G2L-SBC images consist of:

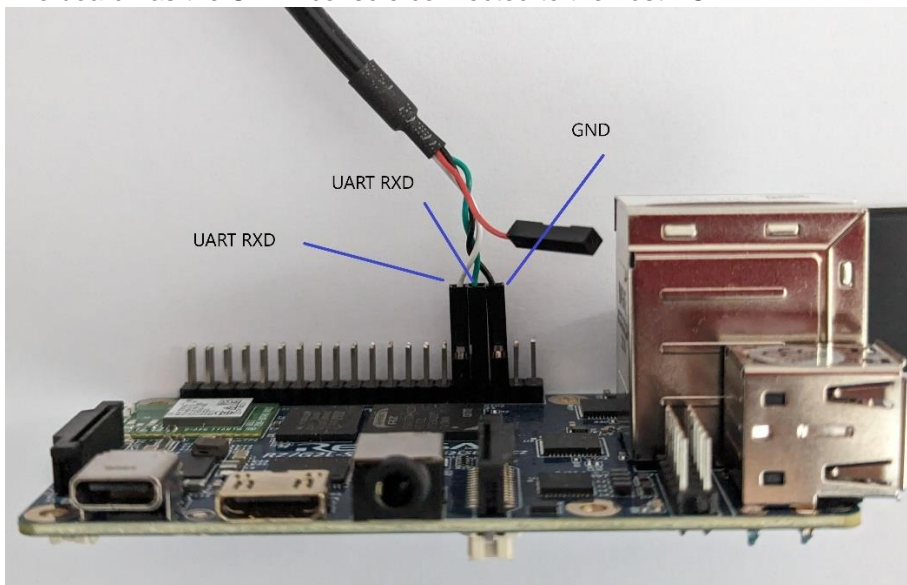
1. Trusted firmware
2. Multi-stage bootloaders.
3. Linux demo distribution.

The SBC board is designed to boot from QSPI EEPROM containing the trusted firmware and bootloaders. However, the SBC does not have an emmc storage and the Linux image is expected to be available on an SD card or on a TFTP server.

### 7.1 Hardware Setup

To perform a firmware flashing, you need to ensure the following:

1. The board has the UART console connected to the host PC.



2. The SD card with the Linux boot image from the release.
3. A 5V 3A USB-C power supply.

Other interfaces are not necessary for this purpose.

### 7.2 Flash bootloader on u-boot console

If users want to update the Bootloader without touching the hardware setup, we support a method for flashing the Bootloader on the U-Boot console. This is especially useful when end customers need to update firmware as part of a field service. This is a straightforward method.

The sub-directory `u-boot` in Yocto build output / release folder contains the toolset for sd-card flashing. The subdirectory contains its readme (u-boot-readme.txt) file with the flashing procedure.

Default bootloader images (.bin) are in the subdirectory ``/boot/uload-bootloader`` of the root filesystem in sd card. You can put your own bootloader images there and perform a flashing.

Before performing the flashing:

- ✓ Make sure the board is powered off,
- ✓ Connect the debug serial port (SCIF0 - TXD, RXD, GND) to your Linux PC
- ✓ Insert the sd-card with the Linux image (you don't need a separate image for this).
- ✓ Ensure that Teraterm application is installed on your windows pc.
- ✓ Ensure that minicom and FTDI drivers are loaded properly on Linux host pc.
- ✓ Ensure that the scripts in the process have execute permissions.

### 7.2.1 Linux Host

The Linux flashing script is named: `uload_bootloader_flash.py`.

The script has options and the details of using it are provided in the `upload-readme.txt` file at the same location. You know more about the command by issuing a ``-h`` option while invoking the script.

```
./uload_bootloader_flash.py -h
```

Please note that the script by default tries to access `/dev/ttyUSB0` without any arguments passed. This works on most systems which have a single FTDI cable attached to a single USB port.

Here are the simplest steps to flash:

Step 1. Ensure that the hardware setup is accurate, as described above.

Step 2. Start the script `uload_bootloader_flash.py`.

```
renesas@builder-pc:~/yocto/yocto_rzsbcb_board/build/tmp/deploy/images/rzpi$ cd
uload-bootloader
renesas@builder-pc:~/yocto/yocto_rzsbcb_board/build/tmp/deploy/im-
ages/rzpi$ ./uload_bootloader_flash.py
```

Step 3. Power on the board. The flashing should automatically start and complete.

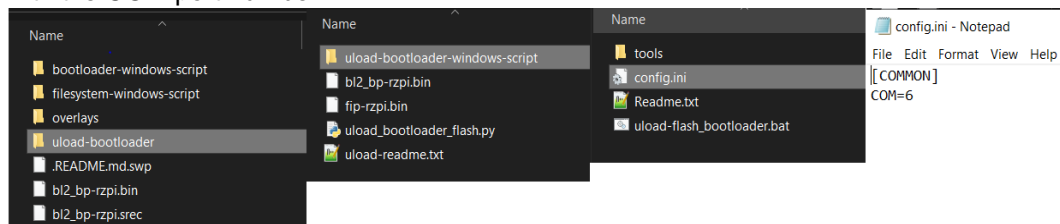
Step 4. Once the flashing is complete, power-cycle the board.

### 7.2.2 Windows Host

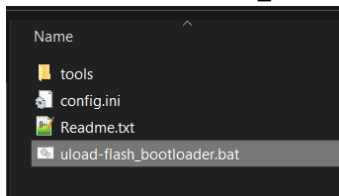
Windows host uses its own script that is cleanly tucked into the sub directory of `uload-bootloader` called `uload-bootloader-windows-script`. The sub-directory has its own `Readme.txt` describing everything that's needed.

The Windows script is also a script that only depends on the teraterm TTL scripting tool.

Step 1. Navigate through the release to the Windows utility directory and update the config.ini with the COM port number.



Execute the uoload-flash\_bootloader.bat



Step 2. Notice application windows open and perform flashing. Once the flashing is completed, it will disconnect from the UART port. Power-cycle the board.

## 8. Accessing Supported Features

In this section, we will explore the features and interfaces available on the RZ/G2L-SBC.

### 8.1 QT Demo Applications

The Linux root file system contains a few QT applications for demo purposes. They can be launched from the taskbar at the top of the screen. They can also be launched through the UART console. When you login to the console, you will find all the demo apps in the home directory of root user.

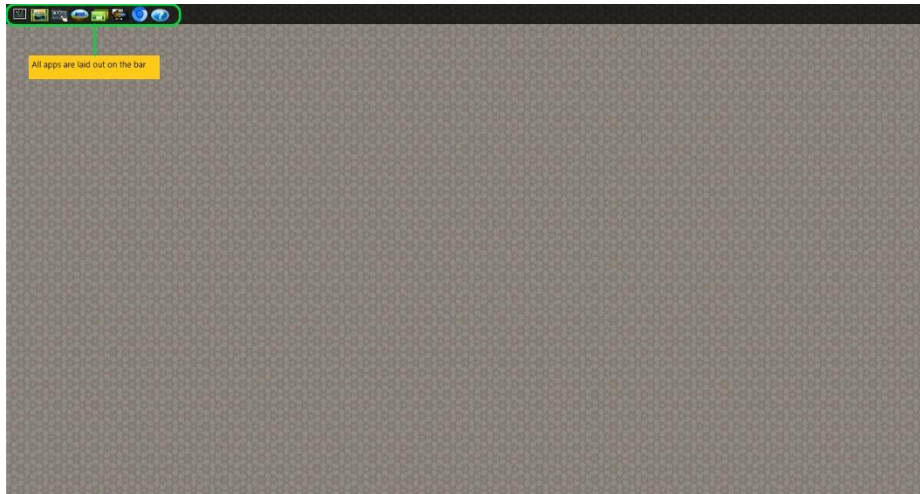
```
root@rzpi:~# cd /home/root/demo/scripts/
root@rzpi:~/demo/scripts# ls
Help.sh Qmlvideofx-demo.sh QtCinematicExperience-demo.sh Qteverwhere-demo.sh
Qt-launch-demo.sh QtSmarthome-demo.sh
```

Most of the demo apps are launched through their corresponding shell script or the UI launchers on the taskbar.

For example, QT smart home demo application can be executed as follows:

```
root@rzpi:~# cd /home/root/demo/scripts/
root@rzpi:~/demo/scripts# ./QtSmarthome-demo.sh
```

The following figure shows all the demo apps on the taskbar:

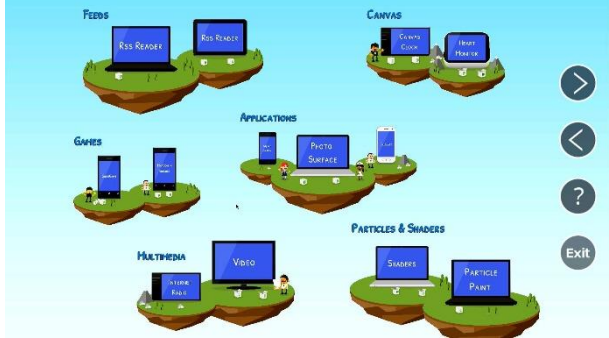




**Figure 32: All the demo apps are on the taskbar on the main screen.**

Each demo app offers a unique blend of functionality and user interface, catering to diverse needs and preferences. However, due to the main memory limitation, not all of them can run successfully on the RZ/G2L-SBC.

The following table describes the details for each demo app.

| Qt demo application name                  | Screenshot   | Description   |
|---|--|---|
| Qt Smart Home (QtSmarthome-demo.sh)       |  | <ul style="list-style-type: none"> <li>- This application shows how you can control and adjust various home operations. Some activities are the control of windows, blinds, heating, and lighting.</li> <li>- The operations are activated by a change in weather conditions, and you can also adjust the weather as you like in the "weather god control" mode.</li> </ul> |
| Qt Graphical Effects (Qmlvideofx-demo.sh) | <p>This demo application does not run properly when rendering videos due to its heavy size. There is no screenshot for it.</p> |   |

|  |   |   |
|--|---|---|
| <p>Qt everywhere<br/>(QtEVERWHERE-<br/>demo.sh)</p>                              |    | <ul style="list-style-type: none"> <li>- This application contains several Qt Quick 2 applications which you can launch by tapping the devices.</li> <li>- The applications are separated into several areas such as Games, Multimedia, Feeds, Canvas, Applications and Particles &amp; Shaders.</li> </ul>           |
| <p>Qt Quick<br/>(Qt-launch-<br/>demo.sh)</p>                                     |    | <ul style="list-style-type: none"> <li>- This demo application shows new features in QT Quick 2.0.</li> <li>- There are "Qt Quick - Front" where font rendering performs, "Qt Quick - Canvas" where shapes are created visually, "Qt Quick - Particle System" where special effects follow your cursor,...</li> </ul> |
| <p>Qt Cinematic<br/>Experience<br/>(QtCINEMATIC<br/>Experience-<br/>demo.sh)</p> |  | <ul style="list-style-type: none"> <li>- This UX demo application presents some graphical features of Qt5.</li> <li>- The name 'Cinematic Experience' reflects how it's possible to build user interfaces with increased dynamics.</li> </ul>   |

## 8.2 40-Pin IO Expansion Interface

The 40 IO Expansion Interface on RZG2L-SBC has support for:

- I2C channel 0
- I2C channel 3
- SPI channel 0
- SCIF channel 0,
- CAN channel 0
- CAN channel 1
- GPIO pin-function (default).



**Note:**

The GPIO pin array is multiplexed with peripheral IO lines. However, by default, they are mostly GPIO's.

By default, I2C channel 0 and SCIF channel 0 are enabled.

The rest of the pins are GPIO's by default. Other functions are enabled by editing the uEnv.txt on the SD-card and enabling the appropriate device tree overlay file (DT overlays). This is also how some of the dedicated drivers are enabled like display. Please ensure that you reboot the board for the overlay to take effect.

### 8.2.1 U-Boot Environment

The u-boot environment file is named 'uEnv.txt' and is present in the 'boot' directory. It contains boot configuration settings to be processed by the u-boot and configuration to be passed on to the Linux kernel. The full description of the U-boot environment is beyond the scope of this document. However, we cover the necessary aspects and settings that are relevant to the SBC and most frequently used.

The table below provides a list of all the overlay options available in the provided kernel.

| Config                           | Value if set | Loading           | Description  |
|----------------------------------|--------------|-------------------|--|
| <b>fdtfile</b>                   | rzpi.dtb     | rzpi.dtb          | Main device tree file to be loaded from the filesystem   |
| <b>enable_overlay_i2c</b>        | 1 or 'yes'   | rzpi-ext-i2c.dtbo | Enables the i2c driver enumeration and reconfigures the relevant IO pins to connect to the I2C peripheral. |
| <b>enable_overlay_spi</b>        | 1 or 'yes'   | rzpi-ext-spi.dtbo | Enables the SPI driver enumeration and reconfigures the relevant IO pins to connect to the SPI peripheral. |
| <b>enable_overlay_can</b>        | 1 or 'yes'   | rzpi-can.dtbo     | Enables the CAN driver enumeration and reconfigures the relevant IO pins to connect to the CAN peripheral. |
| <b>enable_overlay_dsi</b>        | 1 or 'yes'   | rzpi-dsi.dtbo     | Enables the waveshare DSI to display touch panel driver enumeration and reroutes the video to DSI.         |
| <b>enable_overlay_csi_ov5640</b> | 1 or 'yes'   | rzpi-ov5640.dtbo  | Enables the OV5640 CSI camera driver enumeration and loads the v4l2 pipelines.                             |

There is a 'readme.txt' file in '/boot' folder with the descriptions of the FDT overlay information. This is usually more up-to-date with the build.

**Note:**

The Linux shell command 'sync' needs to be run after changing files on the rootfs to ensure that the data is flushed to the actual physical storage. Without it there is a possibility that the changes may not take effect in the actual file.

Device tree file changes require the SBC to be rebooted to take effect.

### 8.2.2 GPIO (General Purpose I/O pins)

By default, most pins are configured as GPIO's on the SBC's 40-pin GPIO pin header. This section describes what those pins are and how to access them. The io pins are explored in detail in Figure 22: 40 PIN GPIO map with orientation details. The explanation of the Linux GPIO framework is beyond the



scope of this document. In this section, we mostly deal with the identification of pin and port numbers and how to access them.

Linux sysfs uses `/sys/class/gpio` entries to control the GPIO bank. The following table maps out the pins and their functions to the IO port header:

| GPIO Pin number | Function              | group | pin | J3        |            | pin | group | Function              | GPIO Pin Number |
|-----------------|-----------------------|-------|-----|-----------|------------|-----|-------|-----------------------|-----------------|
|                 |                       |       |     | Left side | Right side |     |       |                       |                 |
|                 | 3.3V                  |       |     | 1         | 2          |     |       | 5V                    |                 |
| 490             | I <sup>2</sup> C3 SDA | 46    | 2   | 3         | 4          |     |       | 5V                    |                 |
| 491             | I <sup>2</sup> C3 SCL | 46    | 3   | 5         | 6          |     |       | GND                   |                 |
| 304             | GPIO                  | 23    | 0   | 7         | 8          | 0   | 38    | SCIF0 TX              | 424             |
|                 | GND                   |       |     | 9         | 10         | 1   | 38    | SCIF0 RX              | 425             |
| 456             | GPIO                  | 42    | 0   | 11        | 12         | 2   | 7     | GPIO                  | 178             |
| 336             | GPIO                  | 27    | 0   | 13        | 14         |     |       | GND                   |                 |
| 345             | GPIO                  | 28    | 1   | 15        | 16         | 0   | 8     | GPIO                  | 184             |
|                 | 3.3V                  |       |     | 17        | 18         | 0   | 15    | GPIO                  | 240             |
| 465             | SPI0 MOSI             | 43    | 1   | 19        | 20         |     |       | GND                   |                 |
| 466             | SPI0 MISO             | 43    | 2   | 21        | 22         | 1   | 14    | GPIO                  | 233             |
| 464             | SPI0 CK               | 43    | 0   | 23        | 24         | 3   | 43    | SPI0 CS               | 467             |
|                 | GND                   |       |     | 25        | 26         | 1   | 11    | GPIO                  | 209             |
|                 | I <sup>2</sup> C0 SDA |       |     | 27        | 28         |     |       | I <sup>2</sup> C0 SCL |                 |
| 152             | GPIO                  | 4     | 0   | 29        | 30         |     |       | GND                   |                 |
| 153             | GPIO                  | 4     | 1   | 31        | 32         | 0   | 32    | GPIO                  | 376             |
| 297             | GPIO                  | 22    | 1   | 33        | 34         |     |       | GND                   |                 |
| 457             | CAN0 TX               | 42    | 1   | 35        | 36         | 1   | 23    | GPIO                  | 305             |
| 208             | CAN0 RX               | 11    | 0   | 37        | 38         | 0   | 46    | CAN1 TX               | 488             |
|                 | GND                   |       |     | 39        | 40         | 1   | 46    | CAN1 RX               | 489             |

The SoC uses bank ID and io line number to identify the GPIO port. The pin mux uses a unique Px\_y notation for the physical pins. Linux, however, uses a linear GPIO pin number list and internally maps the GPIO numbers to the appropriate GPIO line.

The following method is used to identify the correct Linux pin number:

Step 1: We start with the Px\_y io pin from the schematic. Identify the port values as per the table below.

**Table 6: Symbol definition for GPIO Px\_y Notation**

| Symbol / variable in notation | Description   |
|-------------------------------|---|
| <b>x</b>                      | Group number / port number  |
| <b>y</b>                      | Pin number in port (0:8)  |
| <b>G</b>                      | Group in (always 8 bit which is the size of the port register). Constant 8.                   |
| <b>P<sub>base</sub></b>       | Pin base: starting io pin number (constant 120). All external Linux gpio pins start from 120. |

Step 2: Calculate the Linux port ID using the following formula:

$$\text{Linux\_pin\_number} = (\text{x} * \text{G}) + \text{y} + \text{P}_{\text{base}}$$

Example for J3 PIN 7:

$$(23*8) + 0 + 120 = 304 = \text{pinum}$$

To set the GPIO pin, change the directory to the GPIO sysfs directory and set values as shown below:

```
root@rzpi:~# cd /sys/class/gpio/
root@rzpi:/sys/class/gpio# echo 304 > export
```

There will be a new directory that represents the GPIO pin. In this example, it will be the P23\_0 directory.

```
root@rzpi:/sys/class/gpio# ls
P23_0 export gpiochip120 unexport
```

Inside the P23\_0 directory, some control interfaces are created by the Linux sysfs to manage the GPIO pin:

```
root@rzpi:/sys/class/gpio# cd P23_0
root@rzpi:/sys/class/gpio/P23_0# ls
active_low device direction edge power subsystem uevent value
```

**Note:**

The Linux sysfs is not populated with all the gpio's. They are usually mapped for use within the kernel. So, to get the gpio handle, its necessary to call an export on it so that the kernel driver makes it available by populating a new directory with the pin number and, control handles placed in it. For detail, refer to the official document: <https://docs.kernel.org/5.10/admin-guide/gpio/sysfs.html>

### 8.2.2.1 Setting I/O pin direction

To control the input/output of the GPIO pin, either “in” or “out” should be written to the “direction” interface. Writing as “out” defaults to initializing the value as low.

```
root@rzpi:/sys/class/gpio# echo out > P23_0/direction
```

### 8.2.2.2 Reading the GPIO

To read the state high/low of the GPIO pin, print out the value of the “value” interface.

```
root@rzpi:/sys/class/gpio# cat P23_0/value
0
```

Value 0 means the I/O pin is low; Value 1 means the I/O pin is high.

### 8.2.2.3 Setting the GPIO

The ability to control the pin's output is only available when the direction is set to 'out' / output mode. To set the high/low value of the GPIO pin (output pin), either "1" or "0" should be written to the "value" interface. Any nonzero value is treated as high.

```
root@rzpi:/sys/class/gpio# echo 1 > P23_0/value
root@rzpi:/sys/class/gpio# cat P23_0/value
1
root@rzpi:/sys/class/gpio# echo 0 > P23_0/value
root@rzpi:/sys/class/gpio# cat P23_0/value
0
```

You can always read the current state of the port by reading back the value interface.

### 8.2.3 Enabling I2C function (channel 3 – RIIC3)

Edit `uEnv.txt` and uncomment the line as follows to enable I2C channel 3 on the 40 IO expansion interface:

Change the following line:

```
#enable_overlay_i2c=1
```

To

```
enable_overlay_i2c=1
```

Then reboot the RZ/G2L-SBC.

To check if the I2C channel 3 is enabled, run the following command, and check the result:

```
root@rzpi:~# i2cdetect -l
i2c-3  i2c          Renesas RIIC adapter          I2C adapter
i2c-1  i2c          Renesas RIIC adapter          I2C adapter
i2c-4  i2c          i2c-1-mux (chan_id 0)        I2C adapter
i2c-0  i2c          Renesas RIIC adapter          I2C adapter
root@rzpi:~#
```

To map out all the devices present on I2C bus, execute the following command:

```
root@rzpi:~# i2cdetect -y -r 3
   0  1  2  3  4  5  6  7  8  9  a  b  c  d  e  f
00:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
10:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
20:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
30:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
40:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
50:  50  --  --  --  --  --  --  --  --  --  --  --  --  --  --
60:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
70:  --  --  --  --  --  --  --  --  --  --  --  --  --  --  --
```

Any device present on the bus will be marked with the appropriate i2c device ID.

### 8.2.4 SPI function (channel 0 – RSPI0)

Edit `uEnv.txt` as follows to enable SPI channel 0 on the 40 IO expansion interface:

Change the following line:

```
#enable_overlay_spi=1
```

To

```
enable_overlay_spi=1
```

This will enable the SPI module.

Run the following command to config the SPI:

```
root@rzpi:~# spi-config -d /dev/spidev0.0 -q  
/dev/spidev0.0: mode=0, lsb=0, bits=8, speed=2000000, spiready=0
```

Connect Pin 19 (RSPI0 MOSI) to Pin 21 (RSPI0 MISO), then run the below command and check the result. The idea is to transmit on MOSI and read back on MISO to validate the transfer.

```
root@rzpi:~# echo -n -e "1234567890" | spi-pipe -d /dev/spidev0.0 -s 10000000 |  
hexdump  
00000000 3231 3433 3635 3837 3039  
0000000a
```

### 8.2.5 CAN function (channel 0,1 - CAN 0,CAN 1)

Edit `uEnv.txt` as follows to enable CAN channel 0,1 on 40 IO expansion interface:

Change the following line:

```
#enable_overlay_can=1
```

To

```
enable_overlay_can=1
```

To verify that the CAN channels are enabled, run the following command and check the result:

```
root@rzpi:~# ip a | grep can  
3: can0: <NOARP,ECHO> mtu 16 qdisc noop state DOWN group default qlen 10  
    link/can  
4: can1: <NOARP,ECHO> mtu 16 qdisc noop state DOWN group default qlen 10  
    link/can  
root@rzpi:~#
```

Then set up for CAN devices. Now you can up/down the interface or send data over CAN channels.

The below example shows the communication between two CAN channels.

```
root@rzpi:~# ip link set can0 down
root@rzpi:~# ip link set can0 type can bitrate 500000
root@rzpi:~# ip link set can0 up
[ 48.120419] IPv6: ADDRCONF(NETDEV_CHANGE): can0: link becomes ready
root@rzpi:~# ip link set can1 down
root@rzpi:~# ip link set can1 type can bitrate 500000
root@rzpi:~# ip link set can1 up
[ 69.906039] IPv6: ADDRCONF(NETDEV_CHANGE): can1: link becomes ready
root@rzpi:~# candump can0 & cansend can1 123#01020304050607
[1] 271
   can0 123  [7]  01 02 03 04 05 06 07
root@rzpi:~# candump can1 & cansend can0 123#01020304050607
[2] 273
   can0 123  [7]  01 02 03 04 05 06 07
   can1 123  [7]  01 02 03 04 05 06 07
root@rzpi:~#
```

### 8.3 Wi-Fi 802.11 Module

RZ/G2L-SBC comes equipped with an onboard wireless 802.11 module. The image is ready with all the necessary tools to connect to Wi-Fi. The Wi-Fi can be configured on the command line, which can either be on the desktop UI or the UART tty from the host.

The following shows how to enable the 802.11 Wi-Fi module and connect to a network.

```
root@rzpi:~# connmanctl
connmanctl> enable wifi
Enabled wifi
connmanctl> agent on
Agent registered
connmanctl> scan wifi
Scan completed for wifi
connmanctl> services
   xDredme10zW          wifi_0025ca329da3_78447265646d6531307a57_managed_psk
                        wifi_0025ca329da3_hidden_managed_psk
   REL-GLOBAL          wifi_0025ca329da3_52454c2d474c4f42414c_managed_ieee8021x
   R-GUEST             wifi_0025ca329da3_522d4755455354_managed_none
   RVC-WLS             wifi_0025ca329da3_5256432d574c53_managed_ieee8021x
connmanctl> connect wifi_0025ca329da3_78447265646d6531307a57_managed_psk
Agent RequestInput wifi_0025ca329da3_78447265646d6531307a57_managed_psk
  Passphrase = [ Type=psk, Requirement=mandatory ]
Passphrase? nFjey48aT9pk
connmanctl> exit
```

To confirm the Wi-Fi is connected, ping to the outside world:

```
root@rzpi:~# ping www.google.com
PING www.google.com(hkg07s39-in-x04.1e100.net (2404:6800:4005:813::2004)) 56 data bytes
64 bytes from hkg07s39-in-x04.1e100.net (2404:6800:4005:813::2004): icmp_seq=1 ttl=57
time=43.2 ms
64 bytes from hkg07s39-in-x04.1e100.net (2404:6800:4005:813::2004): icmp_seq=2 ttl=57
time=81.1 ms
64 bytes from hkg07s39-in-x04.1e100.net (2404:6800:4005:813::2004): icmp_seq=3 ttl=57 time=124
ms
```

**Note:**

The ethernet interfaces may potentially interfere with the routing the communication through the Wi-Fi. If issues start appearing, use the following to disable the ethernet ports.

```
root@rzpi:~# ifconfig eth0 down
root@rzpi:~# ifconfig eth1 down
```

## 8.4 On-board Audio Codec with Stereo Jack

The RZ/G2L-SBC comes equipped with an onboard audio codec: Renesas DA7219. The audio codec is connected to the DAI interface (SSI 1) of the SoC configured to I2S data format for the audio data while the control interface is on the I2C 0 interface.

The SBC board has a 3.5mm headset Jack labeled J8. It uses a 6-pin connector.

You can play and record audio directly using ALSA tools. However, it's restricted to PCM wave files only. The image comes equipped with a fully configured GStreamer that lets you play other types of audio files like MP3.

The following shows the two commands to play audio files.

```
root@rzpi:~# aplay /home/root/audios/04_16KH_2ch_bgm_maoudamashii_healing01.wav
root@rzpi:~# gst-play-1.0 /home/root/audios/COMMON6_MPEG2_L3_24KHZ_160_2.mp3
```

`aplay` command supports only `wav` format audio files.

`gst-play-1.0` command supports `wav`, `mp3` and `aac` formats.

The following shows commands to record an audio.

```
root@rzpi:~# arecord -f S16_LE -r 48000 audio_capture.wav
```

Press Ctrl+C if you want to stop recording.

In the above command:

-f S16\_LE : audio format (signed 16 bit little endian)

-r 48000 : sample rate of the audio file (48KHz)

To verify the recorded file, you can play it by the following command:

```
root@rzpi:~# aplay audio_capture.wav
```

To adjust the level of the audio record/playback, use the following command to open the ALSA mixer GUI:

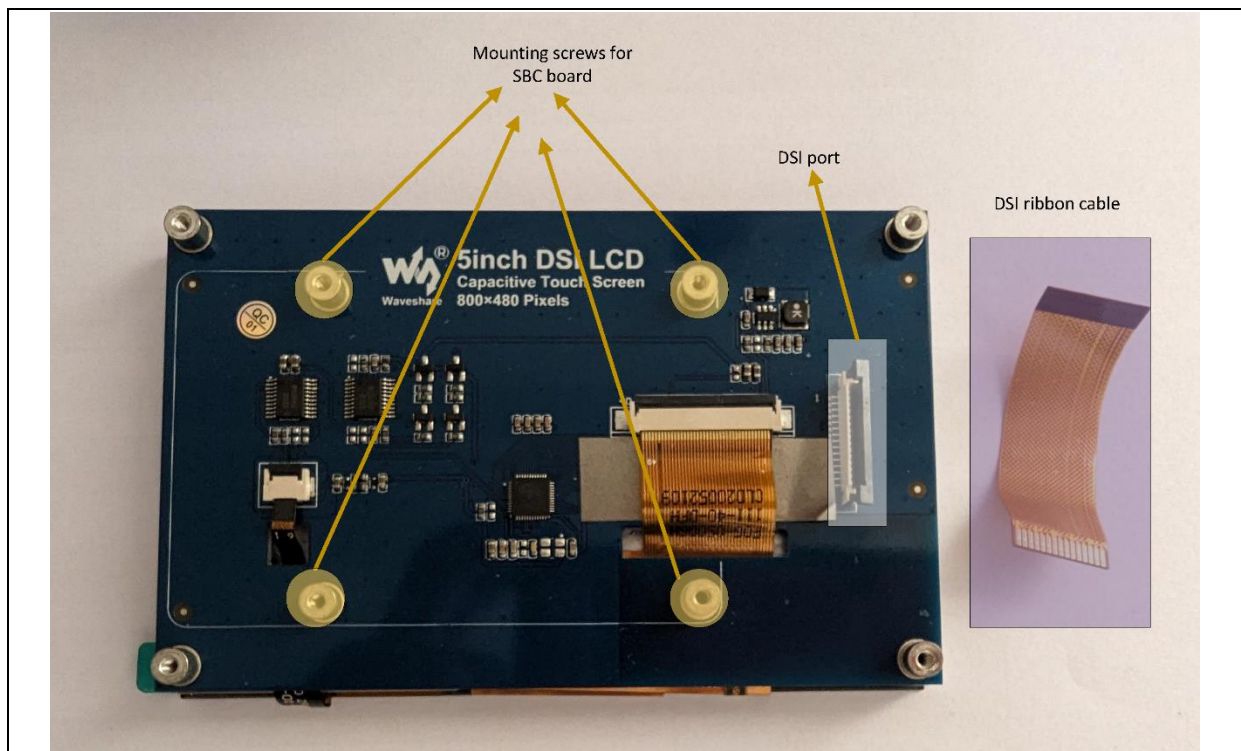
```
root@rzpi:~# alsamixer
```

## 8.5 MIPI DSI Display Touch Panel

RZ/G2L-SBC has a MIPI DSI interface that supports both a display module and a touch interface. The DSI port supports dual-channel DSI and one I2C interface in the connector.

### 8.5.1 Hardware Interfacing

Given below are pictures of Waveshare 5" DSI display panel with touch screen assembly. The pictures are self-explanatory.



**Figure 33: Waveshare 5" DSI touch panel read side picture with flat ribbon cable.**

FPC connector locking and unlocking is done by pulling up the black notch or pushing it down. Unlock the connector by pulling up the notch as shown below.



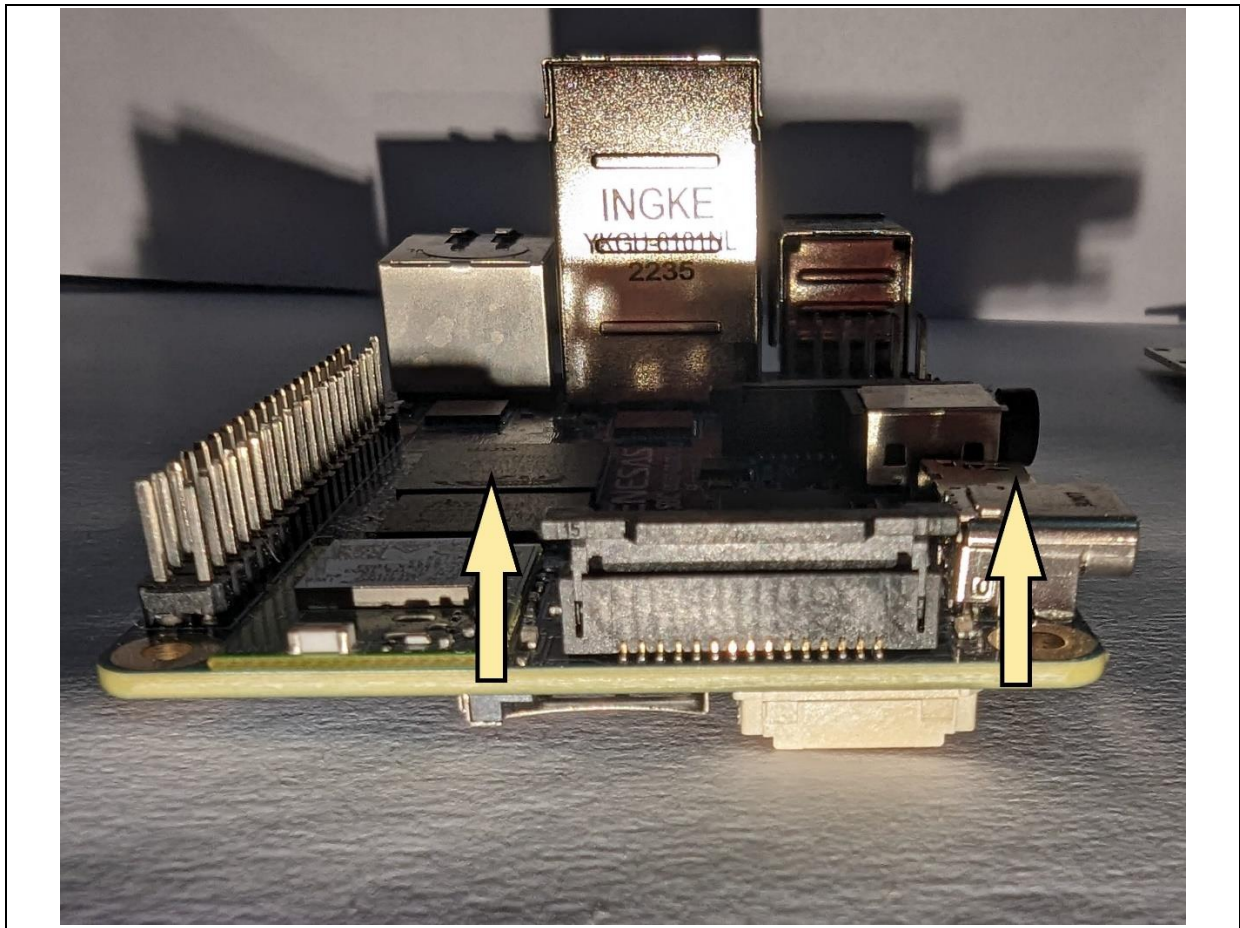
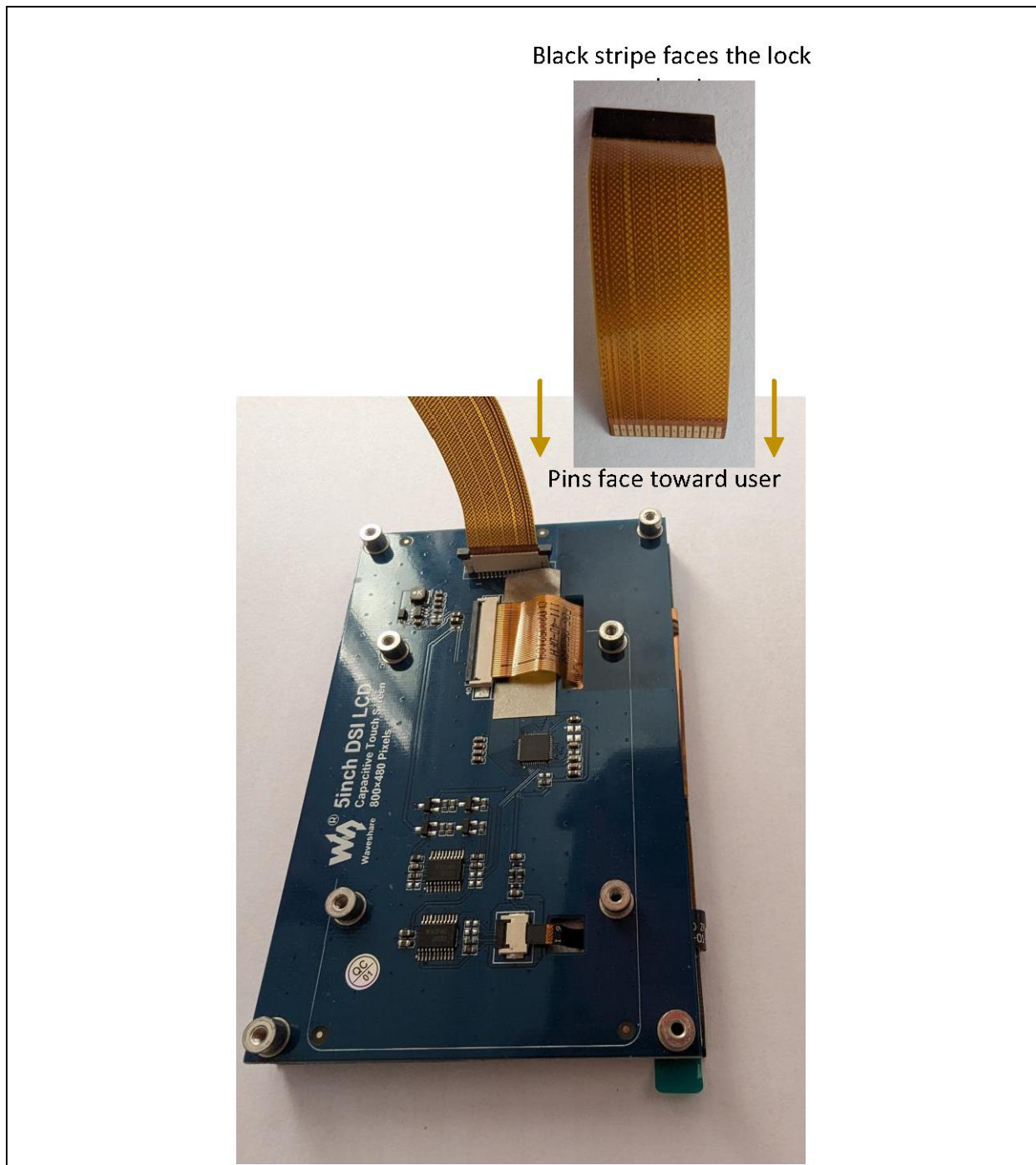


Figure 34: DSI port notch lock open by pulling it up.



**Figure 35: Waveshare DSI touch display DSI port interfacing cable orientation.**

Mount the RZ/G2L-SBC on to the rear end of the display panel.

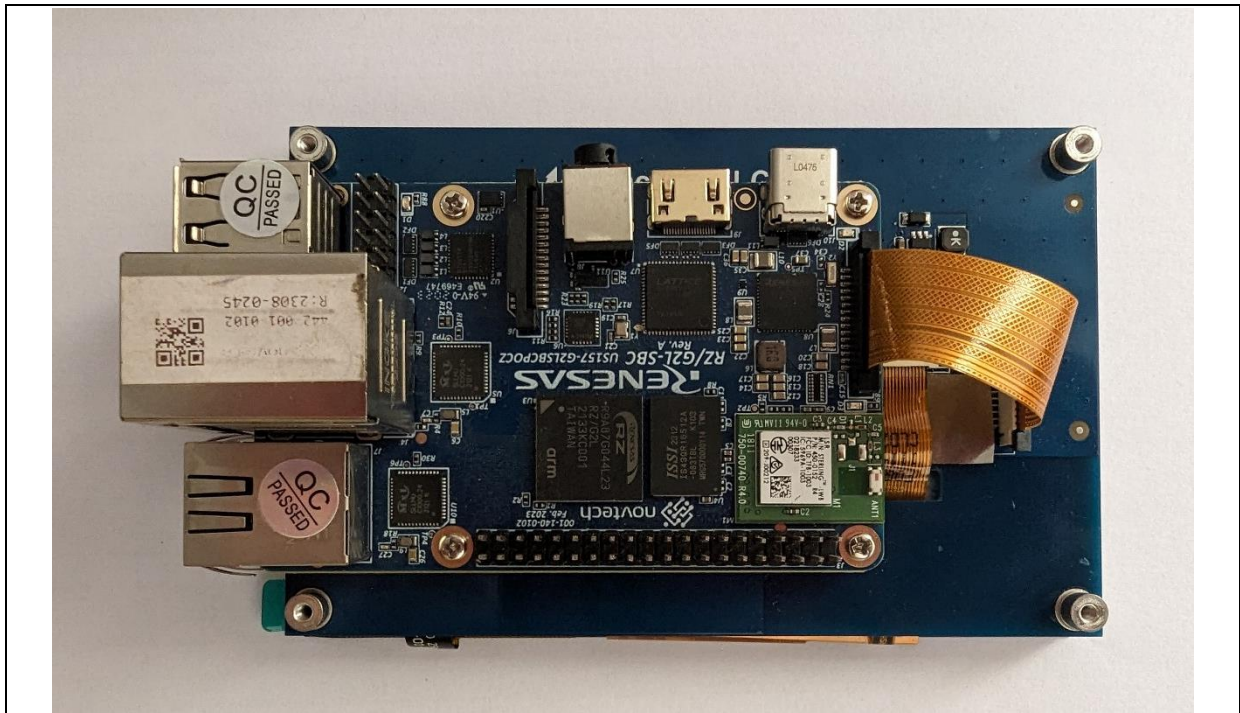


Figure 36: RZ/G2L-SBC mounted to the Waveshare DSI panel and interfaced.

Insert the other end of the FPC cable into the RZ/G2L-SBC DSI port and lock it. The locking mechanism is shown below.

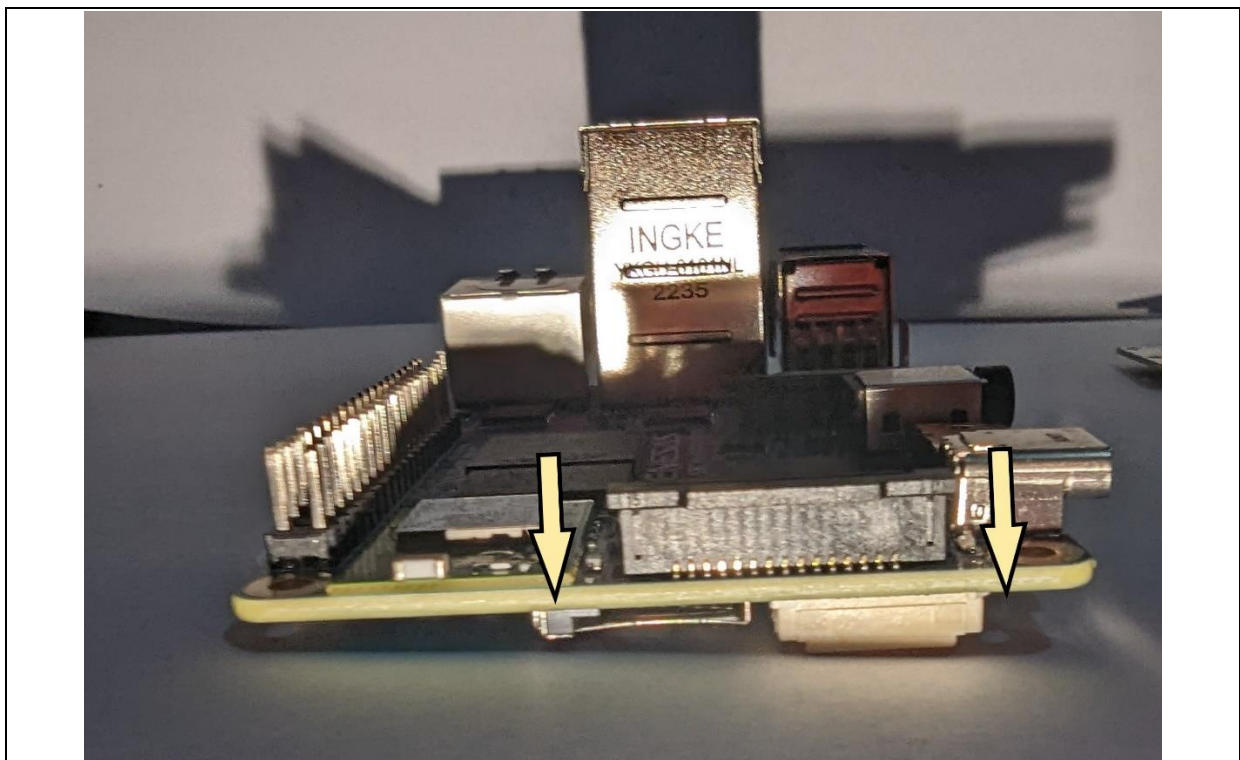


Figure 37: DSI port notch in the lock position. The cable is not shown to keep the notch in clear view.





**Figure 38: Metal support screws supplied by Waveshare**

The Waveshare DSI display panel comes with four metal supports that raise the display along with the rear attached SBC off the surface to provide sturdy support with clearance. However, these are not high enough for the RZ/G2L-SBC due to the SBC having dual ethernet ports where one port is too high sitting on the two USB ports. We still recommend that you use a support stand, even an off-market custom one, to ensure that the DSI cable is off the ground.

Remember that the DSI port includes an I<sup>2</sup>C two-wire interface that supports a touch panel interface without any extra cabling.

**Note:**

The dark solid stripe on the flat cable always faces the black locking mechanism of the connector. Do not insert the cable in reverse as this could potentially damage the board due to wrong electricals.

### 8.5.2 Enabling DSI panel drivers

The Linux distribution supports the Waveshare 5-inch Touchscreen MIPI-DSI LCD capacitive touch panel.

By default, the video output is directed toward the mini-HDMI port. To enable the panel drivers and reroute the display to the DSI panel, you need to enable the panel driver DT overlay in uEnv.txt.

Open the `uEnv.txt` and change the following line:

```
#enable_overlay_dsi=1
```

To

```
enable_overlay_dsi=1
```

Reboot the SBC board.

**Note:**

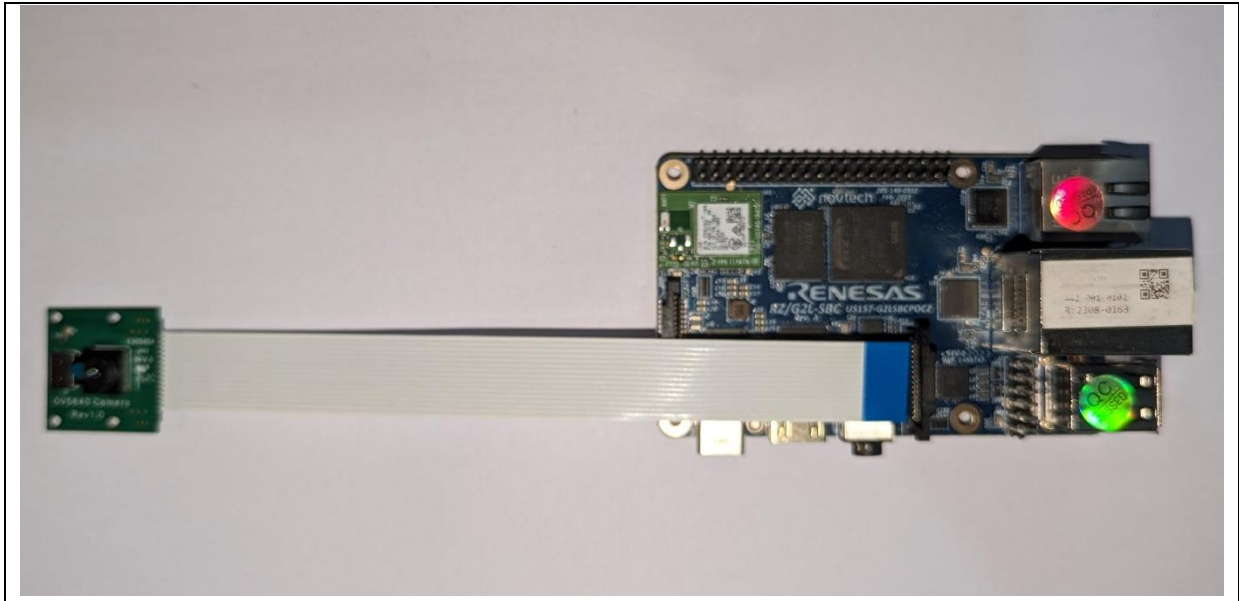
Enabling the MIPI DSI panel overlay disables the HDMI display. You can only use one at a time.

### 8.6 MIPI CSI2 with Arducam 5MP OV5640 Camera Module

RZG2L-SBC supports the MIPI CSI-2 camera interface. The Linux distribution supports the Arducam 5MP MIPI OV5640 image sensor-based module.

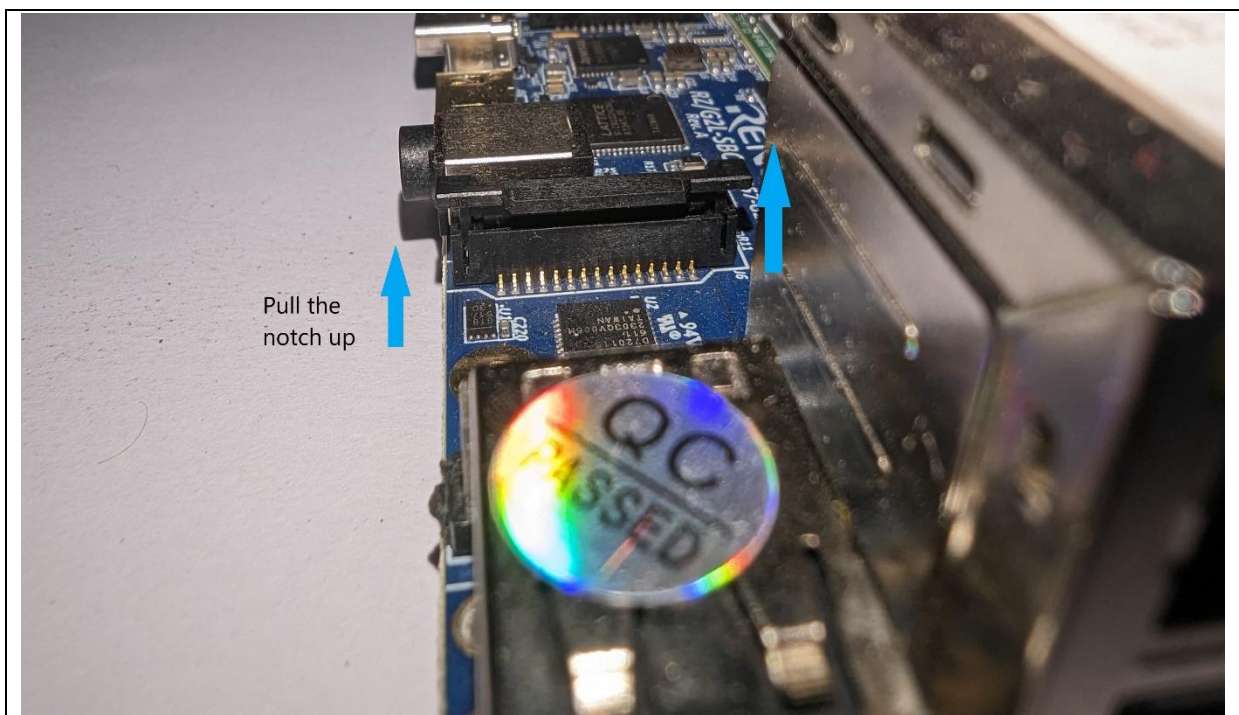
### 8.6.1 Hardware Interfacing

The Arducam OV5640 camera module is easily installed into the RZ/G2L-SBC.



**Figure 39: Orientation of the camera module. Blue stripe upward.**

The black notch must be pulled up to unlock it.



**Figure 40: Pull the notch up to unlock it.**

Insert the flat cable in the correct orientation, as depicted in the pictures.

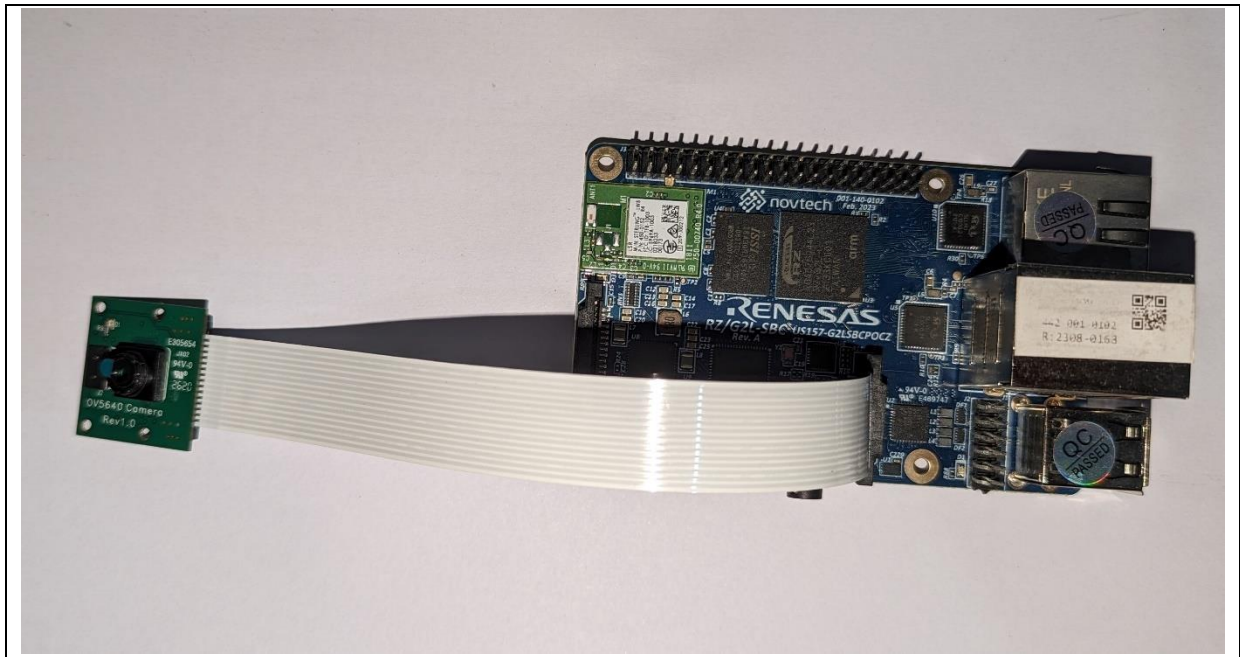


Figure 41: CSI module inserted.

Push down on the notch to lock it with the flat cable inserted.

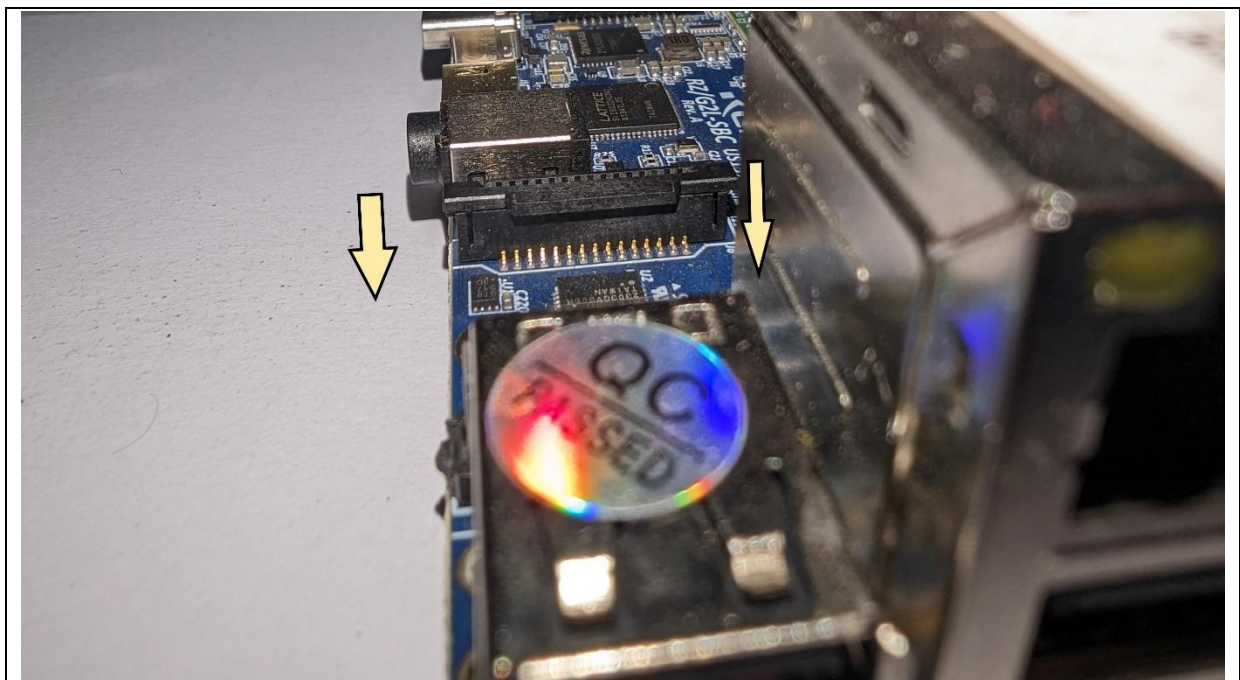


Figure 42: Push down the notch to lock it when you have inserted the flat cable

### 8.6.2 Enabling CSI camera drivers

To enable the camera, edit the uEnv.txt and enable the following line:

```
#enable_overlay_csi_ov5640=1
```

To

```
enable_overlay_csi_ov5640=1
```

Reboot the board.

### 8.6.3 Accessing the Camera

Before initializing the camera capture, it needs to be enabled and configured. The Linux distribution has a helper script (v4l2-init.sh) in the /home/root directory to enable and configure the camera.

```
root@rzpi:~# cd /home/root/  
root@rzpi:~# ./v4l2-init.sh  
Link CRU/CSI2 to ov5640 1-003c with format UYVY8_2X8 and resolution 1280x960  
root@rzpi:~#
```

The `v4l2-init.sh` script helps enable the CSI-2 module and select the camera's supported display resolution.

To change the resolution, edit the v4l2-init.sh and change the resolution lines as depicted below.

```
# Available resolution of OV5640.  
# Please choose one of a following resolution then comment out the rest.  
ov5640_res=1280x960  
#ov5640_res=1920x1080
```

Run the following to initiate a video capture session and preview the video on the screen.

```
root@rzpi:~# gst-launch-1.0 v4l2src device=/dev/video0 ! videoconvert !  
waylandsink
```

This will start a continuous stream of camera feed to the active video display.

## 8.7 Package Management

The distribution comes with Debian package manager 'apt-get' and 'dpkg' for binary package handling.

Note:

The package manager is preinstalled in the image. However, there is no default package repository configured. This is meant to be setup by the user.

### 8.7.1 Setting up Debian as a backend source

Follow the steps below to configure the Debian package repository and install packages according to your needs.

1. Create sources.list file to address packages repository:  
sources.list is a critical configuration file for packages installation and updates used by package managers on Debian-based Linux distributions. The sources.list file contains a list of URLs or repository addresses where the package manager can find software packages. These repositories may be maintained by the Linux distribution itself or by third-party individuals or organizations.

Create sources.list file which is located in /etc/apt/sources.list.d directory as follows to configure Debian package repository:

```
root@rzpi:~# vi /etc/apt/sources.list.d/sources.list
```



Next, add the following contents into sources.list.

```
deb [arch=arm64] http://ports.ubuntu.com/ focal main multiverse universe
deb [arch=arm64] http://ports.ubuntu.com/ focal-security main multiverse universe
deb [arch=arm64] http://ports.ubuntu.com/ focal-backports main multiverse universe
deb [arch=arm64] http://ports.ubuntu.com/ focal-updates main multiverse universe
```

2. Update the defined package index for apt-get.

```
root@rzpi:~# apt-get update
```

Please make sure you have internet access before running apt-get update.

In the contents of sources.list file, each line has [arch=arm64]. This is because the RZ/G2L SoC is an ARM 64 (aarch64) core. This can be verified by the lscpu command:

```
root@rzpi:~# lscpu
Architecture:          aarch64
CPU op-mode(s):       32-bit, 64-bit
Byte Order:           Little Endian
CPU(s):                2
...
Vendor ID:            ARM
```

By specifying [arch=arm64] in sources.list file, apt-get will filter for the proper binary packages in the repository. This will limit the existing APT sources to arm64 only. However, if we use a repository which is entirely hosting ARM 64 bit (aarch64) packages, we don't need to specify [arch=arm64] in the sources.list entry. For example:

```
deb http://deb.debian.org/debian bullseye main contrib non-free
```

Remember that sources doesn't have to be a single origin. Its very common to add multiple repositories and sources for packages and manage them using keys.

The source management is beyond the scope of this document.

3. Installing packages using apt-get:

To install a package using apt-get, use the following command:

```
root@rzpi:~# apt-get install <package-name>
```

## 8.7.2 Using DPKG to install packages

The utility 'dpkg' is the low-level package manager for Debian-based systems. It is the local systemwide package manager. It handles installation, removal, provisioning about package.deb file, indexing and other aspects of packages installed on the system. However, it does not perform any cloud operations. Dpkg also doesn't handle dependency resolution. This is another task handled by a high-level manager like 'apt-get'. In fact, 'dpkg' is the backend for 'apt-get'. While 'apt-get' handles fetching and indexing, the local installations and management of the packages are performed by the 'dpkg' manager.

Basic dpkg commands:

- dpkg -i <package.deb>: Installs a package.deb package.
- dpkg -r <package>: Removes a package.
- dpkg -l <pattern>: Lists installed packages matching <pattern>.
- dpkg -s <package>: Provides information about an installed package.

You can install any <package>.deb using dpkg with the following command:

```
root@rzpi:~# dpkg -i <package>.deb
```

After installing a package using dpkg, if you need to resolve dependency issues, use the following command:

```
root@rzpi:~# apt-get install -f
```

## 8.8 Chromium web browser

The distro image in this release comes with open-source chromium browser. It is a fully featured version.

You can use the following command line to launch a chromium window with a url it will load on launch.

```
root@rzpi:~# chromium --no-sandbox --in-process-gpu --use-gl=desktop  
https://google.com
```

Please note that

Note:

It is a must to have an input device (USB mouse or touchscreen) plugged in before you start the browser. The lack of an input device will cause a "Segmentation fault".

## 9. Appendix

### 9.1 Factory Firmware Flashing using Serial Downloader (SCIF) mode

In most cases, the RZ/G2L-SBC comes preloaded with the latest firmware. The preferred method of updating the firmware is through the SD card flashing method, as described in Programming / Flashing Firmware to RZ/G2L-SBC.

However, there are cases where you might require the use of a serial downloader. This is more common in a factory environment where the boards are being programmed for the first time or in cases where the board is bricked.

This is considered hardware flashing because it requires the board to be put into the SCIF a.k.a serial download mode by altering the bootstrapping pins.

Note:

The RZ/G2L-SBC does not have any interfaces in the main board to alter the boot mode. The boot strapping pins are routed through the bottom connectors J12 & J13. Hence the process requires the use of an adapter board which is not included in the package.

#### 9.1.1 Required Hardware

This flashing process requires the use of boot mode change, which is achieved using an adapter board (not included in the package).

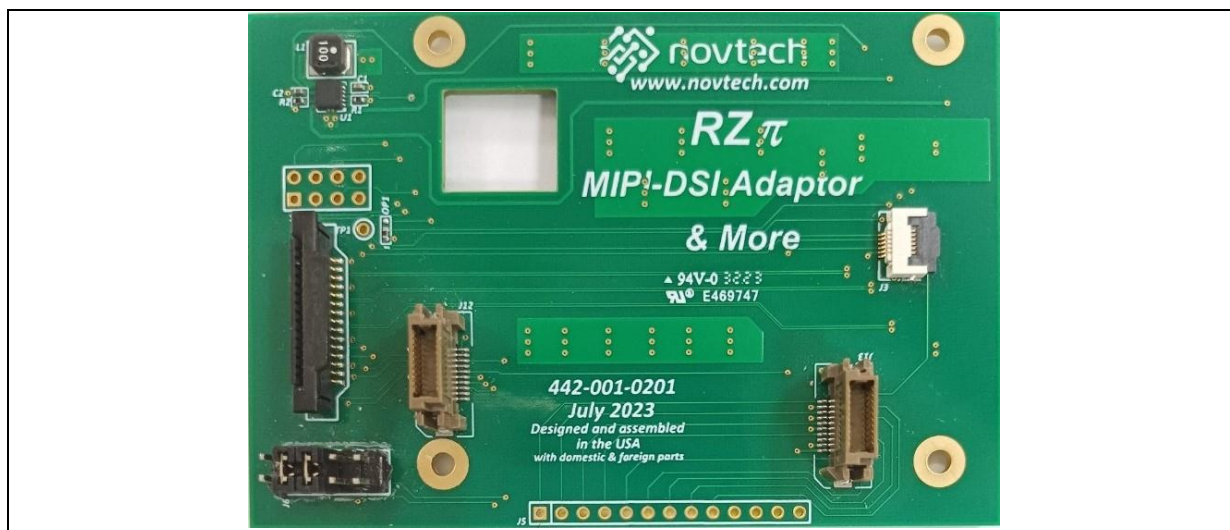


Figure 43: Adaptor board

#### 9.1.2 Flashing Bootloader/Firmware using Linux host

The build contains a support script `bootloader\_flash.py` for flashing bootloader on Linux. The script is part of the Yocto build. The official release is a qualified yocto build from Renesas and is a full package with all tools and scripts.

The Python script is present at the root of the release directory.

Please run the following command to learn how to use the script:

```
$ ./bootloader_flash.py -h
```

Before performing a flashing:

- ✓ Make sure the board is powered off,
- ✓ Connect the debug serial port (SCIF0 - TXD, RXD, GND) to your Linux PC
- ✓ Connect the adapter board with jumpers set to serial load boot mode.

By default, the script uses /dev/ttyUSB0 when no arguments are passed.

Here are the steps:

Step 1. Ensure that the hardware setup is accurate.

Step 2. Start the script.

Step 3. Power on the board

```
renesas@builder-
pc:~/yocto/yocto_rzsbcb_board/build/tmp/deploy/images/rzpi$ ./bootloader_flash.
py
Please power on board. Make sure you changed switches to SCIF download mode.
SCIF Download mode
(C) Renesas Electronics Corp.
-- Load Program to System RAM -----
please send !
Writing Flash Writer application...

Flash writer for RZ/G2 Series V1.06 Aug.10,2022
Product Code : RZ/G2L
>
Elapsed time: Flash Writer: 23.976105 seconds
true
command not found
>
SUP
Scif speed UP
Please change to 921.6Kbps baud rate setting of the terminal.
>
>
>XLS2
===== Qspi writing of RZ/G2 Board Command =====
Load Program to Spiflash
Writes to any of SPI address.
ISS : IS25WP256
Program Top Address & Qspi Save Address
===== Please Input Program Top Address =====
Please Input : H
```

```
'11E00
==== Please Input Qspi Save Address ===
  Please Input : H
'
  Please Input : H'00000
Work RAM(H'50000000-H'53FFFFFF) Clear....
please send !
Writing BL2...
( '.' & CR stop load)
SPI Data Clear(H'FF) Check :H'00000000-0000CFFF,Clear OK
H'00000000-0000CFFF Erasing.....Erase Completed
SAVE SPI-FLASH.....
===== Qspi Save Information =====
  SpiFlashMemory Stat Address : H'00000000
  SpiFlashMemory End Address  : H'0000CB28
=====
>
>XLS2
==== Qspi writing of RZ/G2 Board Command =====
Load Program to Spiflash
Writes to any of SPI address.
  ISS : IS25WP256
Program Top Address & Qspi Save Address
==== Please Input Program Top Address =====
  Please Input : H
'00000
==== Please Input Qspi Save Address ===
  Please Input : H
'1D200
Work RAM(H'50000000-H'53FFFFFF) Clear....
please send !
Writing fip ...
( '.' & CR stop load)
SPI Data Clear(H'FF) Check :H'0001D000-000D7FFF,Clear OK
H'0001D000-000D7FFF
Erasing.....
.....
Closed serial port.
Elapsed time: 81.550220 seconds
```

Power cycle the board after the script completes.

### 9.1.3 Flashing Bootloader/Firmware using Windows host

The subdirectory `bootloader-windows-script` from Yocto build output/release directory contains the Windows scripts. The Windows tool has its own `Readme.txt` file with the necessary information about the scripts.

Before performing a flashing:

- ✓ Make sure the board is powered off,
- ✓ Connect the debug serial port (SCIF0 - TXD,RXD,GND) to your Linux PC
- ✓ Connect the adapter board with jumpers set to serial load boot mode.
- ✓ Ensure that TeraTerm application is installed on your windows pc.

Here are the steps:

Step 1. Ensure that the hardware setup is accurate.

Step 2. Edit config.ini and set the correct com port number.

Step 3. Start the script flash\_bootloader.bat.

Step 4. Power on the board

The script uses Tera Term's TTL to complete the flashing of the firmware. Upon completion, it will disconnect the port.

Power cycle the SBC to boot new firmware.

### 9.2 How to get the console after bootup

Once the RZ/G2L-SBC has booted, on the UART terminal you will be able to login using the default user 'root'. There is no password. Leave the password field empty and just hit the return / enter key.

```

COM10 - Tera Term VT
File Edit Setup Control Window Help
[ OK ] Started telephony.service...
[ OK ] Started ucp.service...
[ OK ] Started rng-tools.service...
[ OK ] Started Login Service...
[ OK ] Started UIN initializing setting.
[ OK ] Started WatchdogTimer.
[ OK ] Started save/restore Sound Card State.
[ OK ] Started IPv6 Packet Filtering Framework.
[ OK ] Started IPv4 Packet Filtering Framework.
[ OK ] Reached target Network (Pre).
[ OK ] Reached target Sound Card.
[ OK ] Started Connection service...
[ OK ] Started Network Service...
[ OK ] Started rng-tools.service.
[ OK ] Started telephony.service.
[ OK ] Loading modules backported from Summit Linux version LRD-REL-11.39.0.18-0-g5de64d7583da
[ 8.141953 ] Backport generated by backports-git v11.39.0.18
[ 8.258748 ] Bluetooth: Core ver 2.22
[ 8.266526 ] HCI Registered protocol family 31
[ 8.274569 ] Bluetooth: HCI device and connection manager initialized
[ 8.284589 ] Bluetooth: HCI socket layer initialized
[ 8.294575 ] Bluetooth: L2CAP socket layer initialized
[ 8.303489 ] Bluetooth: SCO socket layer initialized
[ OK ] Started Network Service.
[ 8.458422 ] Generic PHY 11c20000.ethernet-ffffffff:01: attached PHY driver [Generic PHY] (miibus:phy_addr=11c20000.ethernet-ffffffff:01, irq=POLL)
[ OK ] Started Login Service.
[ 8.531593 ] Generic PHY 11c20000.ethernet-ffffffff:04: attached PHY driver [Generic PHY] (miibus:phy_addr=11c20000.ethernet-ffffffff:04, irq=POLL)
[ OK ] Started Connection service.
[ OK ] Reached target Network.
[ OK ] Starting BusHi MMC/SD Stack...
[ OK ] Started Network Router Discovery Daemon.
[ OK ] Started Permit User Sessions.
[ OK ] Started Network Communication Framework agent...
[ OK ] Started Permit User Sessions.
[ OK ] Started BusHi MMC/SD Stack.
[ OK ] Started Getty on ttyS0.
[ OK ] Started Serial Getty on ttySC0.
[ OK ] Reached target Login Prompts.
[ OK ] Started Network Service...
[ OK ] Starting UIN supplicant...
[ OK ] Started Target Communication Framework agent.
[ OK ] Reached target Multi-User System.
[ OK ] Starting Update UTMP about System Runlevel Changes...
[ OK ] Started System Journal Compositio...
[ OK ] Started Update UTMP about System Runlevel Changes.
[ OK ] Started UIN supplicant.
[ OK ] Created slice User Slice of UID 0.
[ OK ] Started User Runtime Directory /run/user/0...
[ OK ] Started User Runtime Directory /run/user/0.
[ OK ] Started User Manager for UID 0...
[ 9.546616 ] audit: type=1006 audit(1608598644.856:2): pid=218 uid=0 old-auid=4294967295 auid=0 tty=(none) old-ses=4294967295 ses=1 res=1
[ OK ] Started Network Service.
[ OK ] Started User Manager for UID 0.
[ OK ] Started Session c1 of user root.

Poky (Yocto Project Reference Distro) 3.1.26 rpi1 ttySC0
BSP: //3.0.5
LSI:
Version: 3.0.5
rpi1 login: root
Last login: Sun Sep 20 10:44:04 UTC 2020
root@rpi1:~#

```

Figure 44: Root login of Linux console over UART 0.

## 10. Troubleshooting

### 10.1 Unable to run support scripts for Bootloader/Firmware flashing on Linux

Not all Linux distributions ship with the Python3 package and its modules, which are required to run the support scripts described in the Programming / Flashing Firmware to RZ/G2L-SBC section 'Flash bootloader on u-boot console— and in the appendix section 'Flashing Bootloader/Firmware using Linux host'.

To make sure your Linux machine can run the support scripts successfully, execute the following commands (This example is for Ubuntu 20.04):

```
$ sudo apt update
$ sudo apt install -y python3 python3-pip
$ pip3 install pyserial==3.5 argparse==1.4.0
```

The above commands try to update packages on your Linux machine to the latest. Then, they install the python3 package and the python3 pip tool which is used to install python3's modules. And finally, they install the necessary modules (['pyserial'](#) and ['argparse'](#)) with the specific versions for running the support scripts.

### 10.2 Flashing tools failing halfway

The flashing tools are used to update the core firmware in the QSPI memory, which forms the core part of the booting process. This should never fail. When a firmware flashing tool fails, the result is often an unbootable a.k.a 'bricked' device. The only way to recover from this is to use a SCIF boot and the respective flashing process described in the appendix section. 'Factory Firmware Flashing using Serial Downloader (SCIF) mode'.

### 10.3 Running many Qt demo apps slow down the system

QT applications are generally RAM-heavy, and their memory requirement scales up with display characteristics and object complexity. The Qt demo applications in the Linux distro image have been validated to work on the RZ/G2L-SBC over a 10" 1080p HDMI and the Waveshare 5" DSI touch display units. However, some applications can freeze or stutter, especially when other processes are running, the screen size is large, or the framerates are high. One of the limitations in this regard is the 1GiB DDR memory, which limits usable memory for GFX.

Methods to enhance QT application performance:

1. Reduce the application's memory consumption by optimizing QT for using the MALI GPU for animations and reducing the number of objects to be rendered. Simply reducing the framerate can often achieve better performance.
2. Custom board for a custom application: The RZ/G2L SoC supports 2GiB DDR4 SDRAM. If the application requires it, we recommend a custom version of the board with 2GiB DDR SDRAM memory. Please be advised that the existing board is still highly capable of running high GFX applications, as seen in the demos.

### 10.4 DHCP Failure

DHCP depends on the network infrastructure and sometimes takes over 30 seconds or fails completely. When the DHCP fails, the SBC will self-assign an IP address from the address range 169.254.x.y pattern series. This series of addresses is called the automatic private IP addresses.

This is often a network issue. At times, eth0 can take longer to get the IP address. If eth0 is not responding, please recheck with eth1. Your individual network topology will affect the board's ability to get an IP address through DHCP.



## 10.5 'Ifconfig' doesn't list the Wi-Fi interface

The Wi-Fi is not active by default at boot. While all the drivers and subsystems are loaded, the Wi-Fi has to be enabled with the command 'enable Wi-Fi' in conmanctl utility as described in the section 'Wi-Fi 802.11 Module'.

## 10.6 IP configuration

IP address is a bit tricky to get right. It often won't show up unless the port is powered up, and it gets complicated to identify the interface name and ensure there is an address on it. There is some trial and error involved in this step for flashing the system image. You can manually assign the IP address to your host if necessary. Refer to the following for more info on Windows IP settings:

1. [How to configure a static IP on Windows 10 or 11 | Windows Central](#)
2. [Change TCP/IP settings - Microsoft Support](#)

## 11. References

### 11.1 RZ/G2L SoC

Product page: [RZ/G Series \(Linux-based MPU\) | Renesas](#)

Wiki: [RZ/G Series 32/64-bit MPU - Renesas.info](#)

### 11.2 External resources

#### 11.2.1 QT development

Qt official page: [Qt | Tools for Each Stage of Software Development Lifecycle](#)

Qt documentation: [Qt Documentation | Home](#)

#### 11.2.2 Yocto Project

Official Yocto manual: [Yocto Project Reference Manual — The Yocto Project © 4.3.999 documentation](#)

#### 11.2.3 Linux Kernel Documentation

[The Linux Kernel documentation — The Linux Kernel documentation](#)

#### 11.2.4 Arm Developer Documentation

Main page: <https://developer.arm.com/documentation/>

Armv8 Architecture manual: [Arm Architecture Reference Manual for A-profile architecture](#)

Generic Interrupt Controller (GIC) architecture specification: [Arm Generic Interrupt Controller \(GIC\) Architecture Specification](#)

Armv8-A Register manual: [Arm Armv8-A Architecture Registers](#)

Armv8-A Known issues: [Arm Architecture Reference Manual for A-profile architecture: Known issues](#)

Arm Yocto SystemReady IR implimentation: [Deploying Yocto on SystemReady IR compliant hardware \(arm.com\)](#)

Arm TrustZone SMCC protocol: [SMC Calling Convention \(SMCCC\) \(arm.com\)](#)

Arm 64-bit ISA architecture: [Arm A64 Instruction Set Architecture](#)

#### 11.2.5 JEDEC DDR4

[DDR4 SDRAM STANDARD | JEDEC](#)

#### 11.2.6 PMOD Specification

Wiki: [Pmod Interface - Wikipedia](#)

Specification document: [pmod-interface-specification-1\\_3\\_1.pdf \(digilent.com\)](#)

#### 11.2.7 Essential Linux Tutorial

[Linux/Unix Tutorial \(geeksforgeeks.org\)](#)

[Linux/Unix Tutorial - javatpoint](#)

[UNIX / LINUX Tutorial \(tutorialspoint.com\)](#)

### 11.2.8 Linux Kernel Development

[HOWTO do Linux kernel development — The Linux Kernel documentation](#)

[Linux Kernel - GeeksforGeeks](#)

[The Linux Kernel Module Programming Guide \(sysprog21.github.io\)](#)

[A Beginner's Guide to Linux Kernel Development \(LFD103\) - Linux Foundation - Training](#)

### 11.2.9 Linux Kernel Driver Development

Basic intro: [Device Drivers in Linux - GeeksforGeeks](#)

Drive docs: [Driver Basics — The Linux Kernel documentation](#)

Kernel docs: [Device Drivers — The Linux Kernel documentation](#)

Lab: [Character device drivers — The Linux Kernel documentation \(linux-kernel-labs.github.io\)](#)

**Revision History**

| Rev. | Date      | Description |                 |
|------|-----------|-------------|-----------------|
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