Tsi352 Evaluation Board User Manual

80D6000_MA002_02

September 22, 2009

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Printed in U.S.A.

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1. Tsi352 Evaluation Board User Manual

This document discusses the following:

- "Board Design" on page 5
- "Board Layout" on page 13
- "Build of Materials (BOM)" on page 22

Related Documents

- *Tsi352 PCI-to-PCI Bridge User Manual*
- *Tsi352 Evaluation Board Schematic*
- *Tsi352 Pinlist*

1.1 Overview

This document is divided in two sections: board design and board layout. In board design, the components on the board and board functionary are explained. In the board layout section the component placement and the setting options are explained.

1.1.1 Board Specification

The following sections detail the components, connectors, form factor, and power supply of the evaluation board.

1.1.1.1 PCI-to-PCI Bridge

- Device: Tsi352 32 bit PCI-to-PCI transparent bridge
- Primary PCI: 32 bit and 66 MHz
- Secondary PCI: 32 bit and 66 MHz
- Clocking Mode: Synchronized primary and secondary clocking
- Signaling Standard: 3.3V PCI and 5V PCI
- Supply Voltage: 3.3V
- Package: 160 pin PQFP

1.1.1.2 Primary PCI Connector

- 32-bit universal PCI finger connector
- Support both 3.3V and 5V PCI slot
- Compliant with *PCI Specification (Revision 2.3)*

1.1.1.3 Secondary PCI Connector

- Four 3.3 V 32-bit PCI connector slots
- PCI clocking generated from Tsi352
- Compliant with *PCI Specification (Revision 2.3)*
- Supports both the Tsi352 internal arbiter (66 MHz) and the external PCI arbiter (33 MHz)
- 3.3V PCI Signaling

1.1.1.4 Form Factor

- Form Factor: 4-layers Micro ATX Add-in Card with extended height
- Size: 5.5" x 7.5"

1.1.1.5 Power Supply

- PCI Finger Edge Connector: +3.3 V, +5 V, +12 V, -12 V
- Maximum allowable load on secondary side plug-in connectors: 25 W

1.1.2 Evaluation Board Part Number

The Tsi352 evaluation board part number is Tsi352-RDK1.

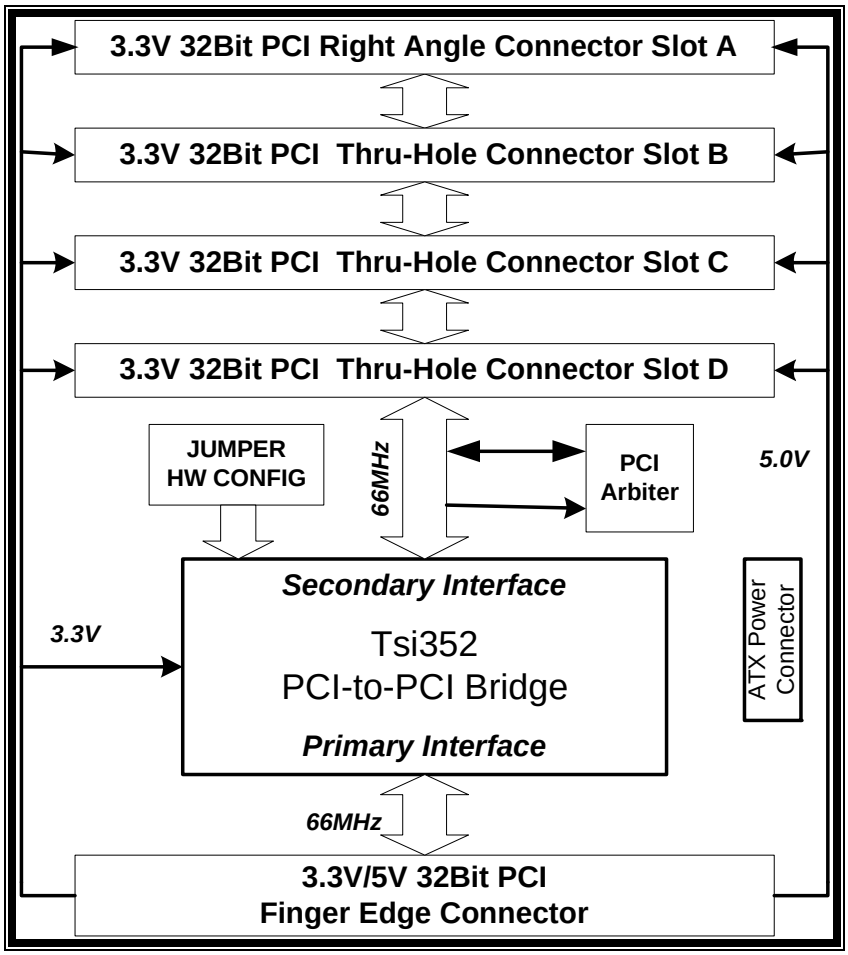
2. Board Design

The following sections explain the design of the evaluation board, its components, and their functionality.

2.1 Overview

The Tsi352 PCI-to-PCI bridge evaluation board evaluates all the features of the Tsi352. The primary PCI interface of the Tsi352 is wired to a PCI finger connector. The secondary PCI interface is wired to four, 32-bit, 3.3 V PCI connectors. Figure 1 shows the board block diagram.

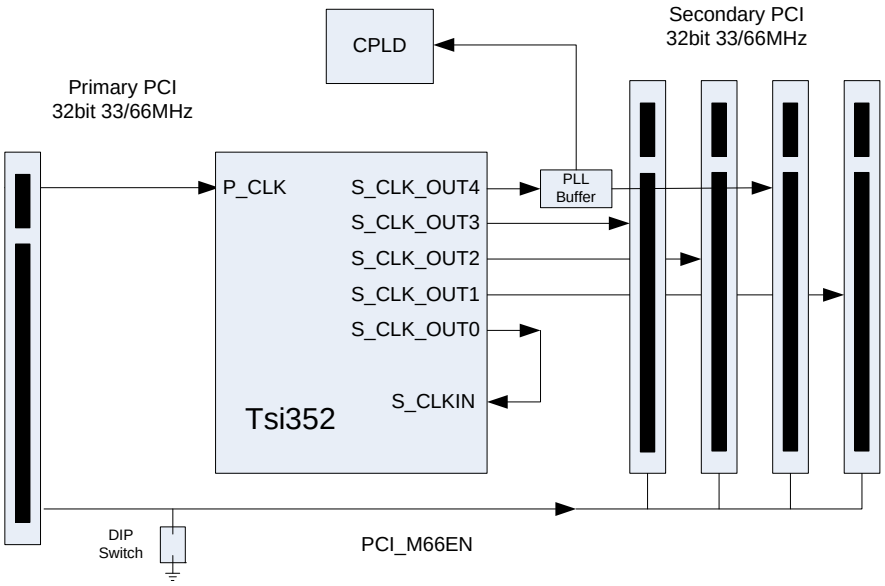
Figure 1: Board Block Diagram



2.2 Clocking

Tsi352 is a synchronous device. The secondary clock outputs are synchronous to the primary clock input. Figure 2 shows the board clocking distribution.

Figure 2: Clock Signals



2.2.1 Domains

Primary and secondary clocking domains are explained in the following sections.

2.2.1.1 Primary PCI Clock Domain

The primary clock is sourced from the PCI host. The primary clock must be synchronous with the primary PCI bus (*PCI Specification (Revision 2.3)*).

The PCI host sets the clock frequency based on its M66EN signal level. However, the Tsi352 evaluation card has the option of forcing the PCI host's M66EN signal low with a DIPSwitch setting (see “Switches” on page 16).

2.2.1.2 Secondary PCI Clock Domain

Tsi352 has four secondary clock outputs. These outputs provide PCI_CLK for four on-board PCI connectors, S_CLKIN, and the CPLD. The secondary clock outputs are derived from the primary PCI clock input. S_CLKOUT0 is used for the Tsi352’s secondary PCI clock input.

A zero-delay PLL buffer is used to fan out S_CLKOUT4 to two outputs: one output is used for the PCI slot and the other is used for the CPLD.

Table 1: S_PCICLK[0:4] Assignment

Tsi352 S_CLKOUT	Net Name on board	Connection	Notes
S_CLKOUT0	S_CLKIN	Tsi352 S_CLK_IN	-
S_CLKOUT1	S_CLKOUT0	PCI Slot J4	-
S_CLKOUT2	S_CLKOUT1	PCI Slot J3	-
S_CLKOUT3	S_CLKOUT3	PCI Slot J1	-
S_CLKOUT4	S_CLKOUT2A	PCI Slot J2	PLL Buffer Output
S_CLKOUT4	S_CLKOUT2B	CPLD U3	PLL Buffer Output

2.2.2 M66EN Signal

The M66EN signal from primary side PCI finger connector is directly routed to four on-board PCI connectors.

The evaluation board DIP switch is attached to the M66EN signal in order to force M66EN to ground, which sets the 33MHz PCI clock (see “Switches” on page 16).

2.3 PCI Bus Arbitration

The Tsi352 evaluation board supports both internal and external arbitration for the secondary PCI bus.

The evaluation board DIP switch is used for internal and external arbiter selection (see “Switches” on page 16).

2.3.1 Internal PCI Arbiter

The Tsi352 has an internal arbiter for arbitration on the secondary PCI interface. The arbitration signals are connected to the four PCI connectors on the board.

Tables 2 shows the Tsi352 arbitration signal assignments to secondary PCI slots.

Table 2: Arbitration Assignment

Tsi352 REQ/GNT Signals	Connector
0	J4
1	J3
2	J2
3	J1

2.3.2 Secondary PCI Bus Arbitration with a CPLD

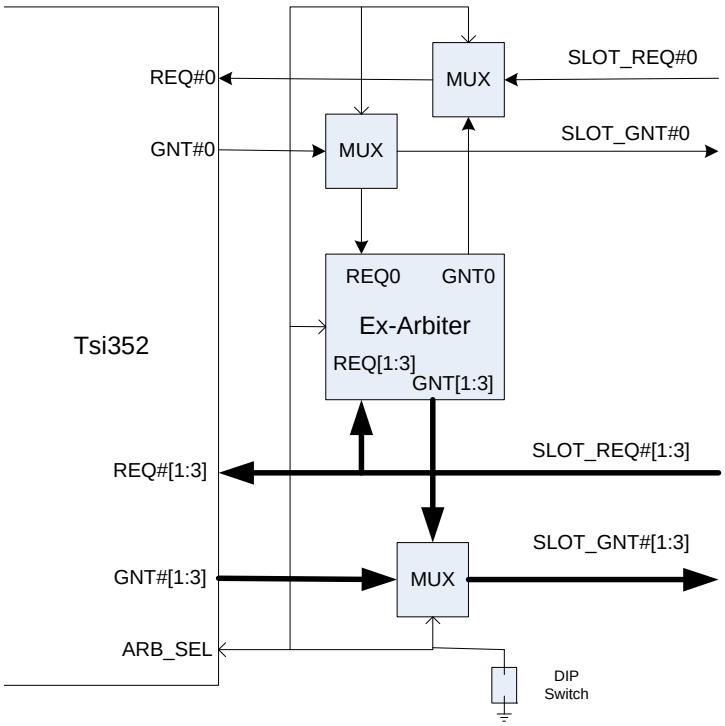
A CPLD is used to implement external PCI bus arbitration. The five channel arbitration (including Tsi352) uses a round-robin architecture with no specific priority. The maximum PCI frequency that the CPLD-based arbiter can support is 33MHz 9due to a CPLD limitation.

The evaluation board uses the Xilinx XCR3064XL-6VQ44C CPLD

Figure 3 shows the external PCI arbiter architecture. Two multiplexer devices (MUX) control the routing of the bus request and bus grant signals between the internal arbiter and the external arbiter. The DIP switch (bit 7) is used to enable internal or external arbiter (see “Switches” on page 16).

Switching the DIP switch (bit7) ON enables the Tsi352 internal arbiter and turns LED D7 off. Switching the DIP switch (bit7)OFF means the external arbiter is used and turns LED D7 on. For more information, see “LEDs” on page 20.

Figure 3: Secondary PCI Bus Arbitration Diagram



2.3.2.1 Disabling the Internal Arbiter

When the Tsi352's internal PCI arbiter is disabled, the S_GNT0_b pin is reconfigured to be the Tsi352's external request pin. The S_REQ0_b pin is reconfigured to be the external grant pin.

2.4 Power

The board draws power from the mother board through the finger connector. The finger connector can carry enough current to supply the evaluation board. The maximum power consumption for the evaluation card is shown in Tables 3 (excluding secondary plug-in cards).

Table 3: Maximum Current Draw (no plug-in card on the secondary side)

Rail	Current
-12 V	0A
+12 V	0A
5 V	0A
3.3 V	800mA
3.3 VAUX	0A

2.4.1 Finger Connector Current Limit

When plug-in cards are added to the evaluation board, the current draw must not exceed the capacity of the finger connector. The maximum current draw per rail for the bridge board with cards plugged-in is shown in Tables 4.

Table 4: Maximum recommended Current draw Per Rail

Rail	Current	Power
-12 V	1 A	12 W
+12 V	1 A	12 W
5 V	8 A	40 W
3.3 V	10 A	33 W
3.3 VAUX	1 A	3.3 W

The total power consumption must be limited to the 25 W budget from all power rails on the primary finger connector (*PCI Specification (Revision 2.3)*).

2.4.1.1 Optional ATX Power Connector

If the total power requirement of plug-in cards exceeds the current draw indicated in Tables 4, an auxiliary ATX power supply can be used to augment the power capacity of the system. The evaluation board has an ATX power supply connector assembly option. This connector is typically not installed.

When the optional ATX power connector is used, both the ATX power supply and PCI finger connector supply must come from the same supply source.

2.4.2 Tsi352 Core Voltage Isolation

The Tsi352 supply voltage plane can be isolated from the evaluation board's 3.3 V plane. in order to evaluate the current draw of the Tsi352.

The connection from the Tsi352 supply to the board 3.3 V is accomplished through the R5, R6, and R7 0 Ohm resistors. Current can be measured by removing the resistors and inserting an amp meter between the test points TP19 and TP18 on the board.

2.4.3 PRSNT Pin Power Setting on Primary PCI

The finger connector's PRSNT[1:2] pins are wired to indicate a power requirement of 25 W. This is the maximum power the PRSNT[1:2] pins can indicate for an add-in card.

The PRSNT pin on the secondary side is not used

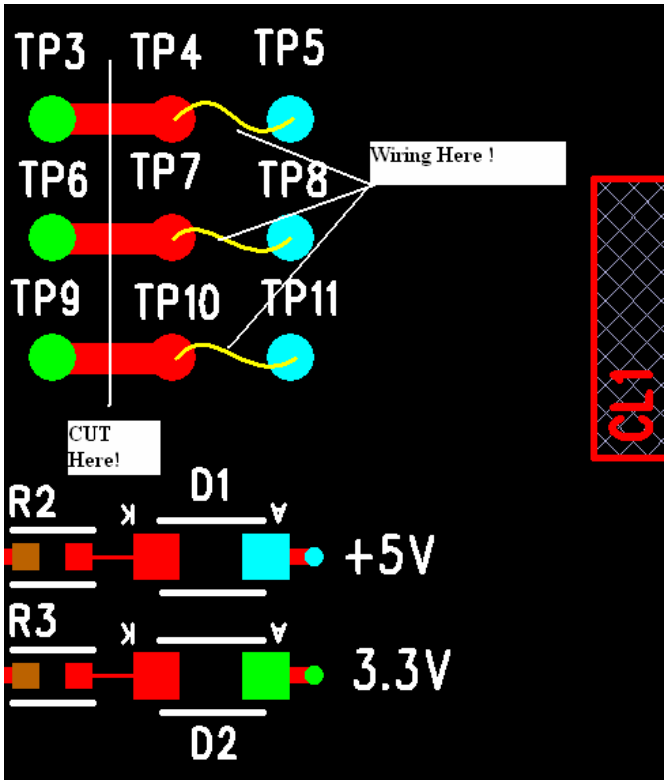
2.4.4 Primary and Secondary Side VIO

The evaluation board can be used in 3.3 V or 5 V PCI systems. P_VIO is connected to the VIO supply from the PCI finger connector. The primary side input/output signaling uses the same voltage as the system. The secondary side voltage is independent of the primary side voltage. The secondary side signaling voltage is hard-wired to 3.3 V by connecting S_VIO and VIO pins of PCI connectors to the 3.3 V supply.

If 5 V signaling is required on the secondary side, the board traces must be modified in the following manner (see Figure 4):

- Cut the traces between TP3 and TP4, TP6 and TP7, and TP9 and TP10
- Solder jumper wires (AWG22) between the 5 V test pads (TP5, TP8, and TP11) and the SVIO test pads (TP4, TP7, and TP10)

Figure 4: Modified PCB Traces for 5 V Signalling on the Secondary PCI Bus



2.5 Interrupts and IDSEL

The add-in card interrupts are routed directly to the PCI system host. The Tsi352 is not involved with interrupt routing. The connection of the interrupt lines from the PCI connectors to the finger connector is arranged so that INTA of each PCI connector is routed to a different interrupt on the finger connector. The add-in card is numbered using the S_AD[24:27] lines.

Tables 5 maps the interrupt connections.

Table 5: Interrupt Mapping

Primary PCI Finger Connector Interrupt	J1	J2	J3	J4
PCI_INTA_b	PCI_INTB_b	PCI_INTA_b	PCI_INTD_b	PCI_INTC_b
PCI_INTB_b	PCI_INTC_b	PCI_INTB_b	PCI_INTA_b	PCI_INTD_b
PCI_INTC_b	PCI_INTD_b	PCI_INTC_b	PCI_INTB_b	PCI_INTA_b
PCI_INTD_b	PCI_INTA_b	PCI_INTD_b	PCI_INTC_b	PCI_INTB_b

Tables 6 shows the secondary PCI slot IDSEL assignments.

Table 6: Secondary PCI Slots IDSEL Assignment

Slots Number	Bus Arbitration	IDSEL	Device ID	INTA Routing to Primary PCI
J1	REQ3/GNT3	S_AD27	0xB	P_INTB
J2	REQ2/GNT2	S_AD26	0xA	P_INTC
J3	REQ1/GNT1	S_AD25	0x9	P_INTD
J4	REQ0/GNT0	S_AD24	0x8	P_INTA

2.6 Resets

The Tsi352 is reset from the system host reset signal (from the finger connector). The secondary side reset is driven by the Tsi352.

There is no manual reset on the evaluation board.

3. Board Layout

In the board layout section of this document the component placement and the setting options are explained.

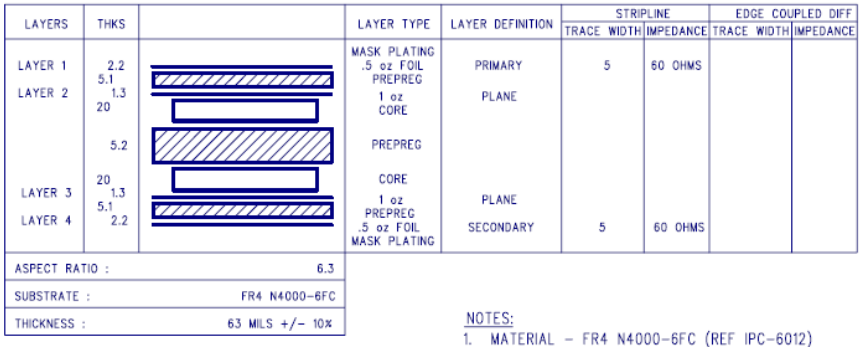
3.1 PCB Layers

The Tsi352 Printed Circuit Board (PCB) stack up is made of the following four layers:

- Layer 1: PCB primary side (where most traces are routed)
- Layer 2: Ground plane
- Layer 3: Power planes
- Layer 4: Secondary side

Figure 5 shows the four layers of the board.

Figure 5: PCB Stack Up



3.2 Board Dimensions

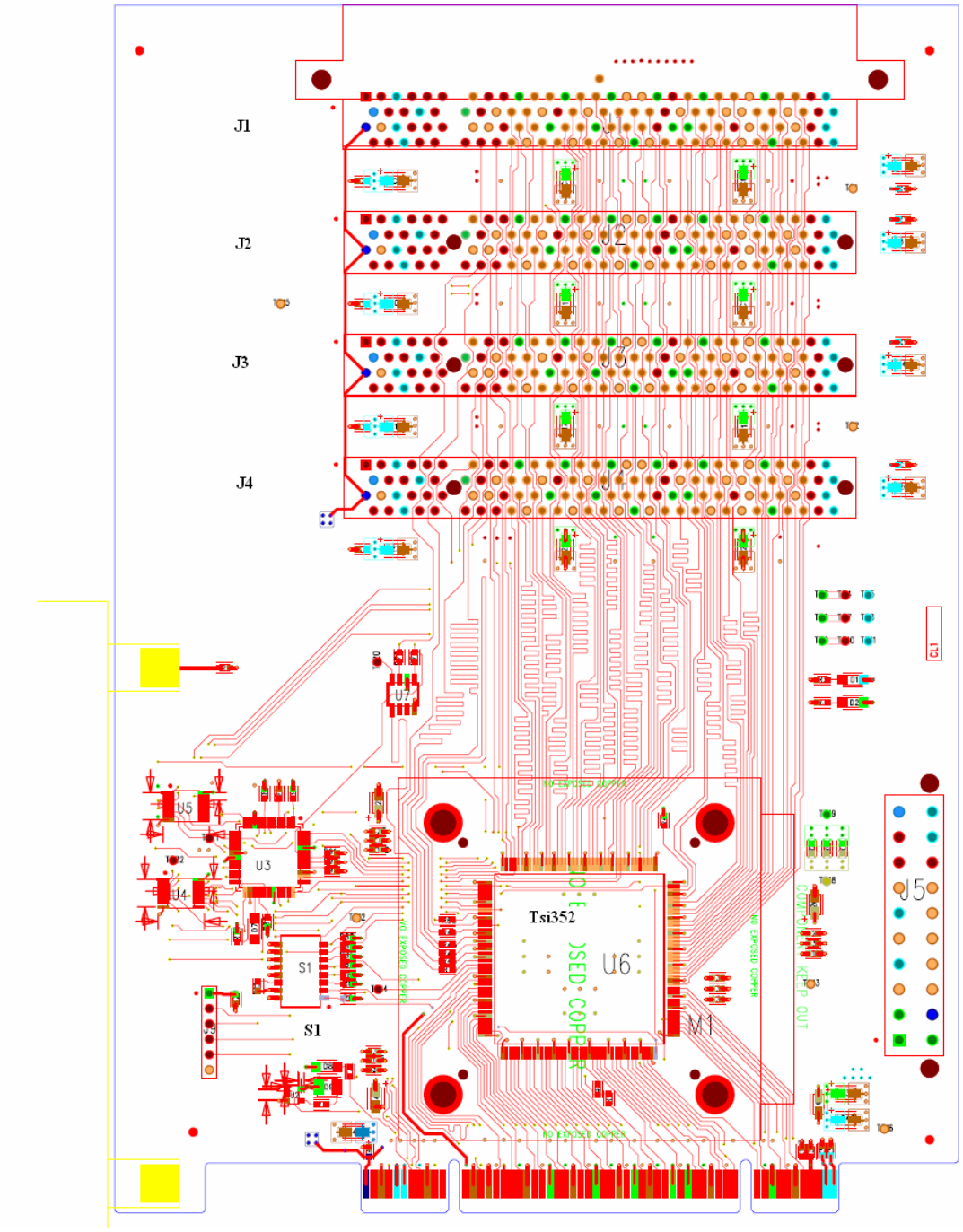
The board dimensions are based on PCI standard for a 32-bit Variable Height Short Add-in card. However, the height of the card exceeds the maximum specified in the standard. The board dimensions are:

- Width = 5.5"
- Height = 8.0"

3.3 Component Placement

The placement of the components, connectors, and switches are shown in Figure 6.

Figure 6: Component Placement



3.4 Switches

The only hardware switch for board configuration is the 8-bit DIP switch, S1. S1 has eight small slide switches identified with numbers 1 to 8.

Tip The OFF position represents the electrical high or logic 1, and the ON position represents electrical level low or logic 0.

Figure 7: S1 DIP switch package/ individual switch position

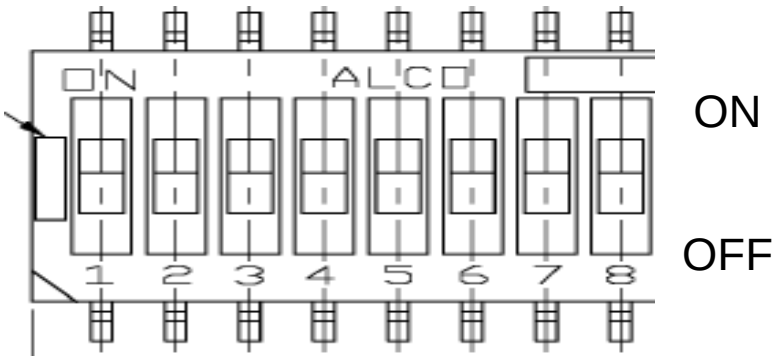


Table 7 shows the setting for the S1 DIP switch.

Table 7: DIP Switch S1 Settings

Bit	Description	Default	On/Off setting
1	MS0: Multifunction Selection	ON	MS[0:1] Configuration Setting (see “Multifunction Signals” on page 17)
2	MS1: Multifunction Selection	ON	MS[0:1] Configuration Setting (see “Multifunction Signals” on page 17)
3	SCAN_TM_b: Scan Test Mode Enable	OFF	ON: Enable scan test mode OFF: Normal Operation
4	P_MFUNC: Multi Function Pin: HS_ENUM, PLOCK_b, or PCLKRUN_b, depending on MS[1:0] setting	OFF	ON: For test purpose only OFF: Normal Operation
5	S_MFUNC: Multi Function Pin: HS_SWITCH, SLOCK_b, or SCLKRUN_b, depending on MS[1:0] setting	OFF	ON: For test purpose only OFF: Normal Operation
6	P_RST_b	OFF	ON: Force P_RST# to low for test purpose only. OFF: Normal operation.

Table 7: DIP Switch S1 Settings

Bit	Description	Default	On/Off setting
7	S_CFN_ARB_b	ON	ON: Enable Tsi352 internal PCI arbiter. OFF: Enable external CPLD PCI arbiter
8	PCI_M66EN	OFF	ON: Force PCI_M66EN to low for 33MHz clocking operation OFF: Normal operation (PCI clock frequency is determined by primary PCI_CLKin and PCI_M66EN# signal level from the secondary plug-in cards)

3.4.1 Multifunction Signals

The MS[0:1] settings configure the Tsi352's Hot Swap, PCI LOCK, CLOCK RUN, and Power Management functionality (see Table 8).

Table 8: MS[0:1] Configuration Setting

MS0	MS1	P_MFUNC	S_MFUNC	MODE	Resistors Installed	Resistors Removed
0	0	HS_ENUM_b	HS_SWITCH_b	Hot Swap	R8, R65, R66	R9
0	1	P_CLKRUN_b	S_CLKRUN_b	Clock Run Mode	R65, R66	R8, R9
1	BPCC	P_LOCK_b[a]	S_LOCK_b	PCI Lock Function	R8, R9, R65, R66	-
BPCC	1	1 = Enable Power Management 0 = Disable Power Management			R8, R9, R65, R66	R8, R9

a. PCI LOCK function is disabled with R8 and R9 removed, and is supported with R8 and R9 installed. Populate R8 and R9 or not has no effect on BPCC power management function.

3.4.1.1 Configuring Functionality

The board supports the following functionality when programmed with proper signal setting (see Table 8) and populated with 0 ohm resistors (see Table 9).

- Power Management
- PCI Lock

The board does not directly support Hot Swap and CLOCK RUN features. However, some test options are implemented on the board to facilitate the evaluation or emulation of Hot Swap and CLOCK RUN features.

Table 9: 0 Ohm Resistors Used for Hardware Multifunction Configuration

Resistor	Connection Description	Default Population	Notes
R65	Connect Tsi352 signal P_MFUNC to S1 bit4 and net ENUM_PLOCK_PCLKRUN#	Installed	-
R9	Connect PCI finger connector signal LOCK# to net ENUM_PLOCK_PCLKRUN#	Removed	Does not support P_LOCK_b
R66	Connect Tsi352 signal S_MFUNC to S1 bit5 and net HSSW_SLOCK_SCLKRUN#	Installed	-
R8	Connect PCI slots signal S_LOCK# to net HSSW_SLOCK_SCLKRUN#	Installed	-

By default, Hot Swap is enabled and the 0 ohm resister R9 is not installed to prevent conflict from the P_LOCK_b signal on the primary PCI bus.

3.5 Connectors

Board connectors are used to add cards and power supplies to the Tsi352 board.

3.5.1 J1 through J4 - PCI Plug-in Card

J1, J2, J3, J4 are used to connect plug-in card on Tsi352's secondary PCI side. The connector's pin assignment uses standard PCI 32-bit, 3.3V connectors.

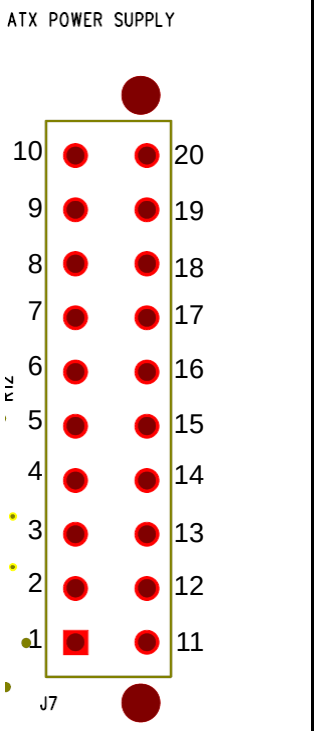
3.5.2 J5 - ATX Power Connector

This connector is not installed on the Tsi352 board. This connector is only required if the voltage drop is high at the plug-in card.

When the optional ATX power connector is used, both the ATX power supply and PCI finger connector supply must come from the same power supply source

Table 10 shows the pin assignments for the J5 connector

Table 10: J5 Pin Assignment

Pin#	Signal Assignment	J5 pin location
1	3.3V	
2	3.3V	
3	GND	
4	5V	
5	GND	
6	5V	
7	GND	
8	N/C	
9	N/C	
10	12V	
11	3.3V	
12	-12V	
13	GND	
14	GND	
15	GND	
16	GND	
17	GND	
18	N/C	
19	5V	
20	5V	

3.5.3 Finger connector

The pin assignment for the finger connector are standard PCI 32-bit universal connectors.

The Finger connector JTAG signals TDI and TDO are connected together on the board.

3.6 LEDs

The LEDS on the board are used to identify the board activity shown in Table 11.

Table 11: LED description

LED Designation	Color	Signal Assignment	Description
D1	Green	5V supply	ON when 5V supply is present
D2	Green	3.3V supply	ON when 3.3V supply is present
D7	Green	LED_ARB_b	ON when the external PCI arbiter is enabled
D8	Red	HS_ENUM_b	ON when HE_ENUM_b is asserted during Hot Swap mode
D9	Blue	HS_LED	ON when HS_LED is asserted during Hot Swap mode

3.7 Test Points

Test points are provided on the Tsi352 board to facilitate signal probing.

Table 12: Tsi352 Test Points

Test Point Designation	Signal Name	Notes
TP1	GND	-
TP2	GND	-
TP3	3.3V	Connected to SVIO
TP4	SVIO	Connected to 3.3V
TP5	5V	-
TP6	3.3V	Connected to SVIO
TP7	SVIO	Connected to 3.3V
TP8	5V	-
TP9	3.3V	Connected to SVIO
TP10	SVIO	Connected to 3.3V
TP11	5V	-
TP12	GND	-
TP13	GND	-

Table 12: Tsi352 Test Points

Test Point Designation	Signal Name	Notes
TP14	HSLED_SCANEN	-
TP15	GND	-
TP16	GND	-
TP17	S_FRAME#	On secondary side of PCB
TP18	3.3V_352	Used for current measurement
TP19	3.3V	Used for current measurement
TP20	CY2305 CLKOUT	S_CLKOUT measurement
TP21	Tsi352 S_REQ_b[0]	-
TP22	Tsi352 S_GNT_b[0]	-

4. Build of Materials (BOM)

Table 13: Build of Materials

Item	Reference Designation	Part Number	Manufacturer	Description
1	C1,C3,C5-6,C8, C10-12,C14,C16-18, C20,C22-26,C39-43	TAJA106K016R	AVX	TANT SMT, 10UF, +/-10%, 16V, 3216-18
2	C2,C4,C7,C9,C13, C15,C19,C21, C27-28,C33-34,C44, C57-59,C61-63, C66-68,C70-72,C74, C78-79,C83,C103	06033D104MAT2A	AVX	X5R CER SMT, 0.1UF, +/-20%, 25V, 0603
3	C29,C36,C45-56, C88,C97-99, C120-144	0603ZC103K	AVX	X7R CER SMT, 0.01UF, +/-10%, 10V, 0603
4	C30-31,C37-38,C73, C76,C81-82	GRM188R71H102MA01D	MURATA	X7R CER SMT, 0.001UF, +/-20%, 50V, 0603
5	C60,C64-65,C146	0603ZD105KAT2A	AVX	X5R CER SMT, 1UF, +/-10%, 10V, 0603
6	D1-2	HSMG-C150	AGILENT	GREEN LED, UNTINTED, DIFFUSED
7	D7	HSMG-C150	AGILENT	GREEN LED, UNTINTED, DIFFUSED
8	D8	HSMH-C150	AGILENT	RED LED, UNTINTED, DIFFUSED
9	D9	HSMN-A100	AGILENT	BLUE LED
10	J1	RBB60DHAS-S793	SULLINS	PCI 3.3V, 32BIT, RIGHT ANGLE, 100MIL ROW-TO-ROW
11	J2-4	145154-4	AMP	PCI MOTHERBOARD, 32BIT, 3.3V, THRU
12	J5	39-29-9202	MOLEX	ATX PWR JACK, 0.165" PITCH, MINI-FIT JR.
13	J9	54101-T06-06	FCI	1X6, 0.1IN HDR
14	R1	ERJ-3EKF1103V	PANASONIC	RES SMT, 110K OHM, 0.1W, 1%, 0603
15	R2-3,R28,R31,R35, R39	ERJ-3GEYJ151V	PANASONIC	RES SMT, 150 OHM, 0.1W, 5%, 0603

Table 13: Build of Materials

Item	Reference Designation	Part Number	Manufacturer	Description
16	R4,R10-11,R18-27, R29-30,R32-34, R36-38,R40-42, R80-94	ERJ-3GEYJ472V	PANASONIC	RES SMT, 4.7 KOHM, 0.1W, 5%, 0603
17	R5-9,R12,R17,R47, R64-66,R68,R70	9C06031A0R00JLHFT	YAGEO	RES SMT, 0 OHM, 0.1W, 5%, 0603
18	R13,R71-73	ERJ-3GEYJ301V	PANASONIC	RES SMT, 300 OHM, 0.1W, 5%, 0603
19	R43-46,R74-76	ERJ-3GEYJ330V	PANASONIC	RES SMT, 33 OHM, 0.1W, 5%, 0603
20	S1	2-1437590-2	TYCO	DIPSWITCH,8SWITCHES
21	U2	74LVC1G14	TI	SINGLE SCHMITT-TRIGGER INVERTER
22	U3	XCR3064XL-6VQ44C	XILINX	CPLD, 64 MACROCELL, 36 USER I/O
23	U4-5	SN74CB3T3257	TI	4BIT 1-OF-2 FET MULTIPLEXER/DEMULTIPLEXER,5VTOLERANT
24	U6	Tsi352	IDT	PCI TO PCI BRIDGE, 32BIT, 66MHZ
25	U7	CY2305	CYPRESS	1-TO-4 3.3V ZERO DELAY CLOCK BUFFER

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