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RENESAS

User's Manual

Phase-out/Discontinued

μPD720130

USB2.0 to IDE Bridge

Document No. S16412EJ3V0UM00 (3rd edition)
Date Published March 2005 NS CP (N)

Printed in Japan

[MEMO]

NOTES FOR CMOS DEVICES

① VOLTAGE APPLICATION WAVEFORM AT INPUT PIN

Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (MAX) and V_{IH} (MIN) due to noise, etc., the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (MAX) and V_{IH} (MIN).

② HANDLING OF UNUSED INPUT PINS

Unconnected CMOS device inputs can be cause of malfunction. If an input pin is unconnected, it is possible that an internal input level may be generated due to noise, etc., causing malfunction. CMOS devices behave differently than Bipolar or NMOS devices. Input levels of CMOS devices must be fixed high or low by using pull-up or pull-down circuitry. Each unused pin should be connected to V_{DD} or GND via a resistor if there is a possibility that it will be an output pin. All handling related to unused pins must be judged separately for each device and according to related specifications governing the device.

③ PRECAUTION AGAINST ESD

A strong electric field, when exposed to a MOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop generation of static electricity as much as possible, and quickly dissipate it when it has occurred. Environmental control must be adequate. When it is dry, a humidifier should be used. It is recommended to avoid using insulators that easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors should be grounded. The operator should be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions need to be taken for PW boards with mounted semiconductor devices.

④ STATUS BEFORE INITIALIZATION

Power-on does not necessarily define the initial status of a MOS device. Immediately after the power source is turned ON, devices with reset functions have not yet been initialized. Hence, power-on does not guarantee output pin levels, I/O settings or contents of registers. A device is not initialized until the reset signal is received. A reset operation must be executed immediately after power-on for devices with reset functions.

⑤ POWER ON/OFF SEQUENCE

In the case of a device that uses different power supplies for the internal operation and external interface, as a rule, switch on the external power supply after switching on the internal power supply. When switching the power supply off, as a rule, switch off the external power supply and then the internal power supply. Use of the reverse power on/off sequences may result in the application of an overvoltage to the internal elements of the device, causing malfunction and degradation of internal elements due to the passage of an abnormal current.

The correct power on/off sequence must be judged separately for each device and according to related specifications governing the device.

⑥ INPUT OF SIGNAL DURING POWER OFF STATE

Do not input signals or an I/O pull-up power supply while the device is not powered. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements.

Input of signals during the power off state must be judged separately for each device and according to related specifications governing the device.

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M8E 02. 11-1

Major Revisions in this Edition

Page	Description
	CHAPTER 1 OVERVIEW
p. 13	Addition of μPD720130GC-9EU-SIN, 720130GC-9EU-A and addition of a remark in **1.1 Ordering Information**
p. 16	Addition of μPD720130GC-9EU-SIN, 720130GC-9EU-A in **1.4.1 Pin configuration (Top view)** in **1.4 Pin Information**

The mark ★ shows major revised points.

INTRODUCTION

Readers

This manual is intended for engineers who intend to make USB2.0 to IDE bridge system by using the μPD720130.

Purpose

This manual explains the functions of the μPD720130 in the following arrangement.

Arrangement

This manual includes the following chapters.

- Overview
- Pin Functions
- USB Descriptor Information
- Request-Decode Table
- Stall or No Handshake
- Serial ROM Information
- Combo Mode
- Power Control Information
- Board Design Guideline
- Electrical Specifications

Reading This Manual

It is assumed that the readers of this manual have general knowledge of electricity, logic circuits, USB specification, USB mass storage class specification, and AT Attachment with Packet Interface-6 (ATA/ATAPI-6) specification.

Conventions

Data significance:	Higher significant digits on the left and lower significance digits on the right
Active low representation:	xxxB (B suffixed to pin name or signal name)
Note:	Footnote for item marked with **Note** in the text
Caution:	Information requiring special attention
Remark:	Supplementary information
Numeric notation:	Binary … xxxx or xxxxB Decimal … xxxx Hexadecimal … xxxxH

Related Documents

The related documents indicated in this document may include preliminary versions.

- μPD720130 Data Sheet: S16302E
- μPD720130 Application Note: S16447E
- ET-0148 User's Manual: S16429E

Be sure to read the latest version of the following documents when using the μPD720130.

- Universal Serial Bus Specification 2.0
- Universal Serial Bus Mass Storage Class Specification Overview (including documents listed in the Overview)
- AT Attachment with Packet Interface-6 (ATA/ATAPI-6) specification

Terms

The terms and symbols used in this document are explained below.

- Control read
  A request using the following sequence for control transfer:

  Setup token – IN token – OUT token

  This is a request reads data from a device. It is therefore called a control read.

  Example: GET_DESCRIPTOR Device

  IN token is used in data stage and more IN tokens may be used.
  OUT token is used in status stage.

- No data control
  A request using the following sequence for control transfer.

  Setup token – IN token

  This is a request that has no data stage.
  It is therefore “No data control”.

  Example: SET_ADDRESS

- Null
  The term “Null” used for the USB is expressed as “0” in this document.
  For example, “Null data” is referred to as “0-byte data”.

CONTENTS

LIST OF FIGURES (1/2)

LIST OF FIGURES (2/2)

LIST OF TABLES

CHAPTER 1 OVERVIEW

This document describes the functions of the μPD720130.

This device is designed to perform a bridge between USB 2.0 and ATA/ATAPI. The device integrates CISC processor, firmware ROM, ATA/ATAPI controller, endpoint controller (EPC), serial interface engine (SIE), and USB2.0 transceiver into a single chip. The USB 2.0 protocol and class specific protocol (bulk only protocol) are handled by USB2.0 transceiver, SIE, and EPC. And the transport layer is performed by V30MZ CISC processor. The V30MZ's firmware is located in an embedded ROM. In the future, the device will be released to support external Flash Memory / EEPROM option for functionality upgrades.

The operational mode of the device can be changed by external pins' setting MD1 and MD0.

Pin		Boot Mode	Status
MD1	MD0		
0	0	Mode 0	NEC reserved
0	1	External ROM Boot (Mode 1)	For future extension (Not available)
1	0	Internal ROM Boot (Mode 2)	Available
1	1	Debug mode (Mode 3)	NEC reserved

If Mode 2 is selected, the V30MZ is run by the firmware in embedded ROM. This mode can be used to implement USB to IDE bridge system easily. The system can be simply built with power circuitry, serial ROM which has vendor ID, product ID and the μPD720130 with mode 2 setting. Mode 1 is provided for future extension. If Mode 1 is selected, V30MZ is run by the firmware in external Flash or EEPROM. The function for the μPD720130 can then be extended by customers' code. Mode 0 and 3 are provided for the debugging. These settings are only for NEC and are not available for implementation.

1.1 Ordering Information

	Part Number	Package
	μPD720130GC-9EU	100-pin plastic TQFP (Fine pitch) (14 × 14)
★	μPD720130GC-9EU-SIN	100-pin plastic TQFP (Fine pitch) (14 × 14)
★	μPD720130GC-9EU-A	100-pin plastic TQFP (Fine pitch) (14 × 14)

★ **Remark** μPD720130GC-9EU-A is a lead-free product.

1.2 Features

This section explains the main features of this chip.

(1) Compliant with Universal Serial Bus Specification Revision 2.0 (Data Rate 12/480 Mbps)
The device is the bus/self powered high-speed capable device and is working at 12 Mbps data rate (FS: full speed) or 480 Mbps date rate (HS: high speed). The μPD720130 were certified by USB implementers forum and granted with USB 2.0 high-speed Logo (TID :40320125). And the evaluation board ET-148 has been certified by USB implementers forum, too (TID :10330107).

(2) Compliant with AT Attachment with Packet Interface-6 (ATA/ATAPI-6). The IDE controller in this device supports PIO Mode 0-4, Multi Word DMA Mode 0-2, Ultra DMA Mode 0-4, and LBA48. Support for ATA Master device.

(3) Bus powered USB2.0 to IDE bridge system
The device supports bus powered operation if the power consumption for total USB2.0 to IDE bridge system is less than the specification for bus powered device. The μPD720130 has some functionalities for supporting power supply control for IDE device.

(4) Combo mode function
The μPD720130 presents itself as one IDE controller in handling one IDE device. It is possible for the μPD720130 to coexist with another IDE controller like 1394 IDE bridge in handling to the same IDE device. The μPD720130 has pins to communicate to other IDE controller to arbitrate IDE bus.

(5) Automatic FS mode/HS mode selection function.
The FS or HS mode is automatically switched from chirp sequence.
The configuration of the Endpoint in each mode is shown below.

- FS mode

Configuration for endpoint	Setup Data		8 bytes
	Control IN/OUT		64 bytes/64 bytes
	Endpoint 1	Bulk IN	64 bytes × 2 (bank configuration)
	Endpoint 2	Bulk OUT	64 bytes × 2 (bank configuration)

- HS mode

Configuration for endpoint	Setup Data		8 bytes
	Control IN/OUT		64 bytes/64 bytes
	Endpoint 1	Bulk IN	512 bytes × 2 (bank configuration)
	Endpoint 2	Bulk OUT	512 bytes × 2 (bank configuration)

(6) High-speed data transfer
The transfer rate between endpoint controller and IDE controller is up to 120 Mbyte/second with the use of internal local bus. Actual transfer rate between PC and USB device depends on PC system.

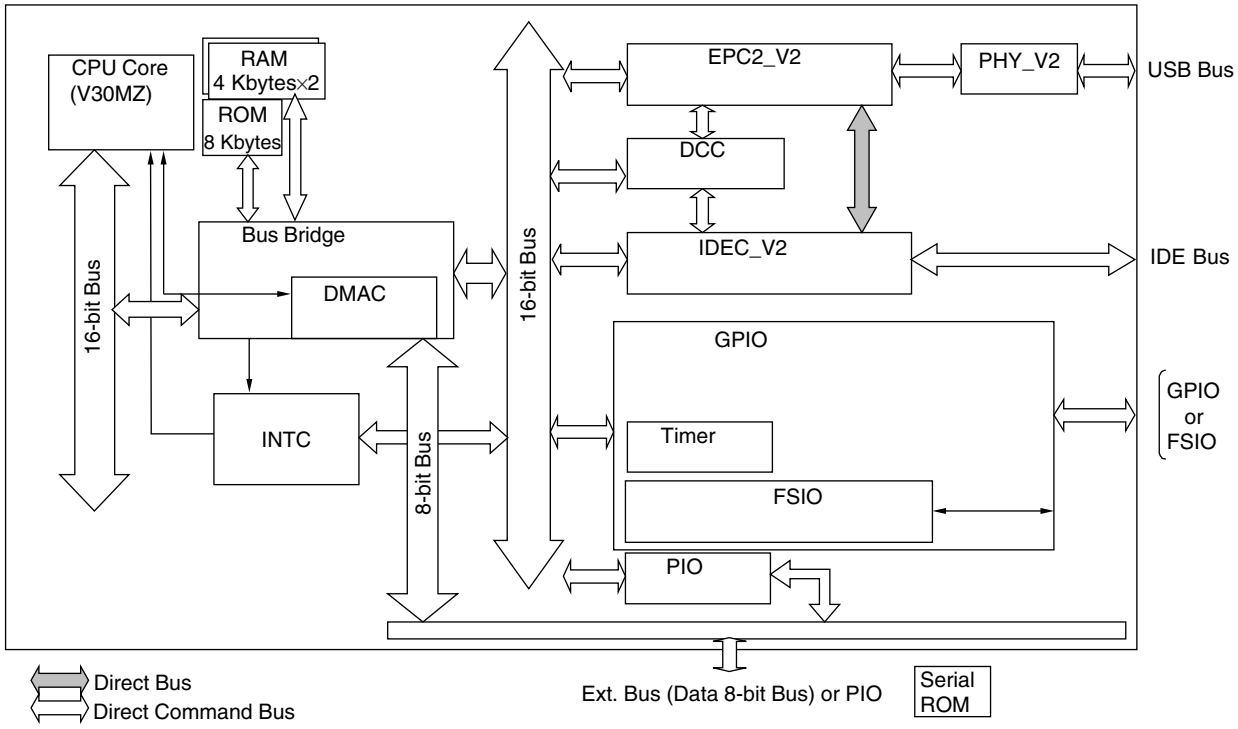
1.2.1 Switching from full-speed operation to high-speed operation

A high speed (HS) device must operate in the full speed (FS) mode when it is connected to host controller / hub which complied with USB1.x specification. The endpoint controller and PHY core implemented in this chip will operate as FS mode after system reset. Host controller / hub and device will perform a special sequence called “Chirp handshake” during USB bus reset to determine each other’s speed capability. When Chirp handshake between host controller / hub and device succeed, this device switches to HS mode. If not, the device works continuously in FS mode.

Because the μPD720130 automatically selects the endpoint buffer size and the protocol of data transmission/ reception, the system can operate without having to distinguish FS or HS operating.

1.3 Block Diagram

Figure 1-1. Block Diagram



V30MZ	: CISC CPU core
RAM	: 8-Kbyte work RAM for firmware
ROM	: 8-Kbyte ROM for built-in firmware
PHY_V2	: USB2.0 transceiver with serial interface engine
EPC_V2	: Endpoint controller
IDEC_V2	: IDE controller
DCC	: ATA direct command controller
Bus Bridge	: Internal / external bus controller and DMA controller
INTC	: Interrupt controller (82C59 like)
GPIO	: General purpose 8-bit I/O controller
PIO	: Multipurpose 14-bit I/O controller
FSIO	: Flexible serial I/O

1.4 Pin Information

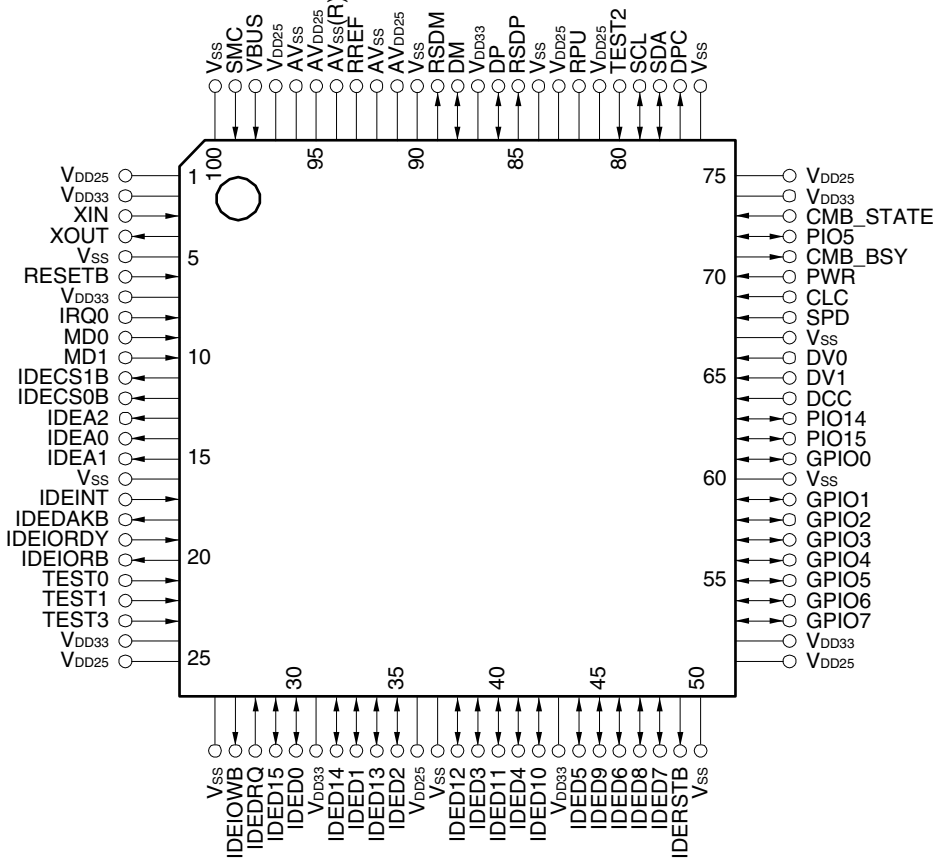
1.4.1 Pin configuration (Top view)

- 100-pin plastic TQFP (Fine pitch) (14 × 14)

  μPD720130GC-9EU

★ μPD720130GC-9EU-SIN

★ μPD720130GC-9EU-A



Remark The pin functions are Mode 2.

1.4.2 Pin list

The pin function differs depending on the Function setting.

(1) Mode 0 (MD0 = Low, MD1 = Low) and Mode 3 (MD0 = High, MD1 = High)

Prohibited to these settings.

(2) Mode 1 (MD0 = High, MD1 = Low)

Not Available, now. It is for future extension.

(3) Mode 2 (MD0 = Low, MD1 = High)

Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name	Pin No.	Pin Name
1	V_{DD25}	26	V_{SS}	51	V_{DD25}	76	V_{SS}
2	V_{DD33}	27	IDEIOWB	52	V_{DD33}	77	DPC
3	XIN	28	IDEDRQ	53	GPIO7	78	SDA
4	XOUT	29	IDED15	54	GPIO6	79	SCL
5	V_{SS}	30	IDED0	55	GPIO5	80	TEST2
6	RESETB	31	V_{DD33}	56	GPIO4	81	V_{DD25}
7	V_{DD33}	32	IDED14	57	GPIO3	82	RPU
8	IRQ0	33	IDED1	58	GPIO2	83	V_{DD25}
9	MD0	34	IDED13	59	GPIO1	84	V_{SS}
10	MD1	35	IDED2	60	V_{SS}	85	RSDP
11	IDECS1B	36	V_{DD25}	61	GPIO0	86	DP
12	IDECS0B	37	V_{SS}	62	PIO15	87	V_{DD33}
13	IDEA2	38	IDED12	63	PIO14	88	DM
14	IDEA0	39	IDED3	64	DCC	89	RSDM
15	IDEA1	40	IDED11	65	DV1	90	V_{SS}
16	V_{SS}	41	IDED4	66	DV0	91	AV_{DD25}
17	IDEINT	42	IDED10	67	V_{SS}	92	AV_{SS}
18	IDEDAKB	43	V_{DD33}	68	SPD	93	RREF
19	IDEIORDY	44	IDED5	69	CLC	94	AV_{SS}(R)
20	IDEIORB	45	IDED9	70	PWR	95	AV_{DD25}
21	TEST0	46	IDED6	71	CMB_BSY	96	AV_{SS}
22	TEST1	47	IDED8	72	PIO5	97	V_{DD25}
23	TEST3	48	IDED7	73	CMB_STATE	98	VBUS
24	V_{DD33}	49	IDERSTB	74	V_{DD33}	99	SMC
25	V_{DD25}	50	V_{SS}	75	V_{DD25}	100	V_{SS}

Remarks 1. 1% precision reference resistor of 2.43 kΩ should be connected between AV_{SS}(R) and RREF.

2. 1% precision resistor of 39 Ω should be connected between RSDP and DP. The same resistor should also be connected between RSDM and DM.

CHAPTER 2 PIN FUNCTIONS

2.1 Pin Table for Mode 1 (MD0 = High, MD1 = Low)

Not Available (For future extension)

2.2 Pin Table for Mode 2 (MD0 = Low, MD1 = High)

Table 2-1. Pin Table for Mode 2 (1/2)

Pin Name	I/O	Buffer Type	Active Level	Function
XIN	I	2.5 V input		System clock input or oscillator in
XOUT	O	2.5 V output		Oscillator out
RESETB	I	3.3 V Schmitt input	Low	Asynchronous reset signal
MD(1:0)	I	3.3 V input		Function mode setting
IDECS(1:0)B	O (I/O)	5 V tolerant output	Low	IDE chip select
IDEA(2:0)	O (I/O)	5 V tolerant output		IDE address bus
IDEINT	I (I/O)	5 V tolerant input	High	IDE interrupt request from device to controller
IDEDAKB	O (I/O)	5 V tolerant output	Low	IDE DMA acknowledge
IDEIORDY	I (I/O)	5 V tolerant input	High	IDE IO channel ready
IDEIORB	O (I/O)	5 V tolerant output	Low	IDE IO read strobe
IDEIOWB	O (I/O)	5 V tolerant output	Low	IDE IO write strobe
IDEDRQ	I (I/O)	5 V tolerant input	High	IDE DMA request from device to controller
IDED(15:0)	I/O	5 V tolerant I/O		IDE data bus
IDERSTB	O (I/O)	5 V tolerant output	Low	IDE reset from controller to device
DCC	I (I/O)	3.3 V input		IDE controller operational mode setting
DV(1:0)	I (I/O)	3.3 V input		Device select
CLC	I (I/O)	3.3 V input		System clock setting
PWR	I (I/O)	3.3 V input		Bus-powered /self-powered select
CMB_BSY	O (I/O)	3.3 V output		Combo IDE bus busy
CMB_STATE	I (I/O)	3.3 V input		Combo IDE bus state
DPC	O (I/O)	3.3 V output		Power control signalling for IDE device
SDA	I/O	3.3 V I/O		Serial ROM data signaling
SCL	I/O	3.3 V I/O		Serial ROM clock signaling
VBUS	I	5 V Schmitt input [Note]		VBUS monitoring
DP	I/O	USB high speed D+ I/O		USB's high speed D+ signal
DM	I/O	USB high speed D– I/O		USB's high speed D– signal
RSDP	O	USB full speed D+ output		USB's full speed D+ signal and R_S resistor terminal
RSDM	O	USB full speed D– output		USB's full speed D– signal and R_S resistor terminal
RPU	A	USB pull-up control		USB's 1.5kΩ pull-up resistor control
RREF	A	Analog		Reference resistor

Table 2-1. Pin Table for Mode 2 (2/2)

Pin Name	I/O	Buffer Type	Active Level	Function
SPD	I (I/O)	3.3 V input		NEC Electronics reserved
SMC	I	3.3 V input		Scan mode control
TEST(3:0)	I	3.3 V input		Test mode setting
GPIO(7:0)	I/O	3.3 V Schmitt I/O		General purpose IO port (for future extension)
PIO(15:14)	I/O	3.3 V I/O		IO port (for future extension)
PIO(5)	I/O	3.3 V Schmitt I/O		IO port (for future extension)
IRQ0	I	3.3 V Schmitt input	High	External interrupt input (for future extension)
AV_{DD25}				2.5 V V_{DD} for analog circuit
V_{DD25}				2.5 V V_{DD}
V_{DD33}				3.3 V V_{DD}
AV_{SS}				V_{SS} for analog circuit
V_{SS}				V_{SS}

Note VBUS pin may be used to monitor for VBUS line even if V_{DD33}, V_{DD25}, and AV_{DD25} are shut off. System must ensure that the input voltage level for VBUS pin is less than 3.0 V to avoid exceeding the absolute maximum rating.

Remarks 1. "5 V tolerant" means that the buffer is 3.3 V buffer with 5 V tolerant circuit.

2. The signal marked as "(I/O)" in the above table operates as I/O signals during testing. However, they are not used as I/O during normal usage.

2.3 Description of Pin Functions for Mode 2

The section describes either a signal either is analog, power, input, output or I/O (bi-directional).

- **Power supply**

Pin Name	Pin No.	Direction	Function
AV_{DD25}	91, 95	Power	+2.5 V analog power supply
V_{DD25}	1, 25, 36, 51, 75, 81, 83, 97	Power	+2.5 V power supply
V_{DD33}	2, 7, 24, 31, 43, 52, 74, 87	Power	+3.3 V power supply
AV_{SS}	92, 94, 96	Power	Analog ground
V_{SS}	5, 16, 26, 37, 50, 60, 67, 76, 84, 90, 100	Power	Ground

- **System clock and reset**

Pin Name	Pin No.	Direction	Caution
XIN	3	I	System clock input or Oscillator input. Connect to 30-MHz clock source or X'tal.
XOUT	4	O	If 30-MHz clock input is connect to XIN, this signal must be left opened. Otherwise, connects to 30-MHz X'tal.
RESETB	6	I	Asynchronous reset signal input

Remark No power-on-reset circuit is included on this chip, so the system has to provide a system reset to this chip at the power-on time like as "power-on reset".

- **IDE interface**

Pin Name	Pin No.	Direction	Function
IDECS(1:0)B	11,12	O	IDE chip select
IDEA(2:0)	13, 15, 14	O	IDE address bus
IDEINT	17	I	IDE interrupt request from device to controller
IDEDAKB	18	O	IDE DMA acknowledge
IDEIORDY	19	I	IDE IO channel ready
IDEIORB	20	O	IDE IO read strobe
IDEIOWB	27	O	IDE IO write strobe
IDEDRQ	28	I	IDE DMA request from device to controller
IDED(15:0)	29, 32, 34, 38, 40, 42, 45, 47, 48, 46, 44, 41, 39, 35, 33, 30	I/O	IDE data bus
IDERSTB	49	O	IDE reset from controller to device

Remark For details of IDE operations, see the **AT Attachment with Packet Interface-6 (ATA/ATAPI-6 Specification)**.

- **USB interface**

Pin Name	Pin No.	Direction	Function
DP	86	I/O	USB's D+ high-speed signal
RSDP	85	O	USB's D+ full-speed signal Connected to DP with a 39 Ω 1% precision R_S resistor.
DM	88	I/O	USB's D– high-speed signal
RSDM	89	O	USB's D– full-speed signal Connected to DM with a 39 Ω 1% precision R_S resistor.
PRU	82	Analog	RPU must be connected with a 1.5 kΩ 1% precision resistor to DP.
RREF	93	Analog	RREF must be connected with a 1% precision reference resistor of 2.43 kΩ to AV_{SS}(R) pin (94 pin).

- **Test and NEC Electronics private pins**

Pin Name	Pin No.	Direction	Caution
TEST(3:0)	23, 80, 22, 21	I	Connect to ground for normal operation.
SMC	99	I	Connect to ground for normal operation.
SPD	68	I	Connect to 3.3 V for normal operation.

- **System interface**

Pin Name	Pin No.	Direction	Function
SDA	78	I/O	Serial ROM data Pull up to 3.3 V with an appropriate resistor.
SCL	79	I/O	Serial ROM clock and also indicates the size of serial ROM which system uses on circuit board. 1: If Serial ROM size ≤ 2 Kbytes, serial ROM clock pulled up to 3.3 V with an appropriate resistor. 0: If Serial ROM size > 2 Kbytes, serial ROM clock pulled down to ground with an appropriate resistor.
MD(1:0)	10, 9	I	Device mode setting MD1 MD0 Setting Notice 0 0 Mode 0 Reserved 0 1 Mode 1 Invalid (Not available) 1 0 Mode 2 Available 1 1 Mode 3 Reserved
IRQ0	8	I	External interrupt input for future extension. This signal is not used in Mode 2. Connect to ground for normal operation.
GPIO(7:0)	53 - 59, 61	I/O	General purpose IO port for future extension. These signals are not used in Mode 2. Connect to ground for normal operation.
PIO(15:14)	62, 63	I/O	Multipurpose IO port for future extension. These signals are not used in Mode 2. Connect to ground for normal operation.
PIO5	72	I/O	Multipurpose IO port for future extension. This signal is not used in Mode 2. Connect to ground for normal operation.

- **Function control setting**

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Pin Name	Pin No.	Direction	Function
VBUS	98	I	VBUS monitoring 1: VBUS line is available from attached to host. 0: VBUS line is not available from detached from host. VBUS pin may be used to monitor for VBUS line even if V_{DD33}, V_{DD25}, and AV_{DD25} are shut off. So, system must ensure that the input voltage level for VBUS pin is less than 3.0 V due to avoid exceeding the absolute maximum rating.
PWR	70	I	Bus or self powered setting 1: Bus powered 0: Self powered This setting can be changed by data in serial ROM.
DCC Note	64	I	IDE controller operational mode setting The function of this pin depends on connected IDE device. For ATA device, ATA Direct Command Controller handles the protocol sequence for Multi Word DMA and Ultra DMA. If ATA Direct Command Controller is disabled, this device uses only PIO mode to communicate with ATA device. For ATAPI device, ATA Direct Command Controller does not supports any ATAPI command. ATA Direct Command Controller is always disabled for ATAPI device. 1: The IDE controller communicates with ATA device by fastest mode such as Ultra DMA Mode 4. And the IDE controller communicates with ATAPI device by available fastest mode such as PIO Mode 4, Multi Word DMA mode 2, or Ultra DMA Mode 4. 0: The IDE controller communicates with ATA device by fastest PIO such as PIO Mode 4 because ATA Direct Command Controller is disabled even if ATA device supports Multi Word DMA or / and Ultra DMA. And the IDE controller communicates with ATAPI device by available fastest PIO or Multi Word DMA such as PIO Mode 4 or Multi Word DMA Mode 2 even if ATAPI device supports Ultra DMA Also, the setting for Direct Command Controller can be changed by data in serial ROM.
DV(1:0)	65, 66	I	IDE device select The meaning of setting is related to CLC and PWR. Refer to **Table 2-2** for proper setting. If target IDE device is fixed, it is preferred not to use the automatically IDE device detection. This setting can be changed by data in serial ROM.

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Pin Name	Pin No.	Direction	Function
CLC	69	I	System clock setting. There are two system clock speeds for this device. One is 7.5 MHz. It is preferred for bus powered system. Another one is 60 MHz. The meaning of setting is related to DV(1:0) and PWR. Refer to **Table 2-2** for proper setting. This setting can be changed by data in serial ROM.
CMB_BSY	71	O	IDE bus request to other IDE controller 1: This device request or is using IDE bus. 0: This device does not request or does not use IDE bus.
CMB_STATE	73	I	IDE bus request from other IDE controller 1: Other IDE controller request or is using IDE bus. 0: Other IDE controller does not request or does not use IDE bus. If there is any other IDE controller in system, this pin should be pulled down.
DPC	77	O	Power control signalling for IDE device. Refer to **CHAPTER 8 POWER CONTROL INFORMATION**.

Note DCC pin is provided to support HDD in Compact Flash(CF) or PCMCIA card. There may be inconsistency between operational mode information from CF and actual operation of HDD. At that case, this device can not find actual HDD operation mode and system may not work correctly. It is preferable for enclosure system to provide the external switch in providing “high” or “low” indication.

Table 2-2. IDE Controller Status and Pin Settings

No.	Device Power	Internal Clock	ATA/ATAPI	PWR pin	CLC pin	DV1 pin	DV0 pin
0	Bus Powered	7.5 MHz	No device connected	1	1	1	1
1			ATA	1	1	1	0
2			ATAPI	1	1	0	1
3			Reserved	1	1	0	0
4		60 MHz	No device connected	1	0	1	1
5			ATA	1	0	1	0
6			ATAPI	1	0	0	1
7			Reserved	1	0	0	0
8	Self Powered	60 MHz	No device connected	0	1	1	1
9			Combo (ATA)	0	1	1	0
10			Combo (ATAPI)	0	1	0	1
11			Combo Auto device detect	0	1	0	0
12			No device connected	0	0	1	1
13			ATA	0	0	1	0
14			ATAPI	0	0	0	1
15			Auto device detect	0	0	0	0

Remarks 1. Setting of no. 0, 3, 4, 7, 8, and 12 are prohibited to use.

2. For Bus powered setting, there are some critical considerations such as power consumption for the total system should be observed.

2.4 Pin Status at the Particular State in Mode 2

Pin Name	Hard-ware Reset	Function Setting State			USB Bus Reset State		Unconfigured State		Configured State		Suspend State		Combo State
		Bus	Self	Combo	Bus	Self / Combo	Bus	Self / Combo	Bus	Self / Combo	Bus	Self / Combo	IDE Bus Release
XIN /XOUT	Active	←	←	←	←	←	←	←	←	←	←	←	←
RESRETB	Active	Inactive	←	←	←	←	←	←	←	←	←	←	←
IDECS(1:0)B	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEA(2:0)	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEINT	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEDAKB	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEIORDY	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEIORB	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEIOWB	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDEDRQ	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDED(15:0)	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
IDERSTB	HZ	HZ	Active	Active	HZ	Active	HZ	Active	Active	Active	HZ	Active	HZ
GPIO(7:0)	HZ	←	←	←	←	←	←	←	←	←	←	←	←
PIO(15:14)	HZ	←	←	←	←	←	←	←	←	←	←	←	←
PIO5	HZ	←	←	←	←	←	←	←	←	←	←	←	←
DCC	HZ	Input	←	←	←	←	←	←	←	←	←	←	←
DV(1:0)	HZ	Input	←	←	←	←	←	←	←	←	←	←	←
SPD	HZ	Input	←	←	←	←	←	←	←	←	←	←	←
CLC	HZ	Input	←	←	←	←	←	←	←	←	←	←	←
PWR	HZ	Input	←	←	←	←	←	←	←	←	←	←	←
CMB_BSY	HZ	HZ	HZ	Output	HZ	HZ/ Output	HZ	HZ/ Output	HZ	HZ/ Output	HZ	HZ/ Output	Output a Low
CMB_STATE	HZ	Input	←	←	←	←	←	←	←	←	←	←	←
DPC	HZ	HZ	HZ	HZ	Output a High	Output a High	Output a High	Output a High	Output a Low	Output a Low	Output a High	Output a High	Output a Low
SCL	HZ	Output	Output	Output	Input	←	←	←	←	←	←	←	←
SDA	HZ	I/O	I/O	I/O	Input	←	←	←	←	←	←	←	←

Remarks 1. HZ: High Impedance

2. IDE bus state for combo mode except for IDE bus release state indicates the condition which IDE bus is used by this device.

3. CMB_BSY is active at combo mode. And it becomes high impedance output at self-powered normal operation.

2.5 Handling Unused Pins for Mode 2

Handle unused pins as shown below.

Pin Name	Direction	Connection Method
GPIO(7:0)	I/O	Connect to ground
PIO(15:14)	I/O	Connect to ground
PIO5	I/O	Connect to ground
IRQ0	I	Connect to ground
TEST(3:0)	I	Connect to ground
SMC	I	Connect to ground
SPD	I	Connect to 3.3 V

When the data in serial ROM is used to initialize the IDE controller, handle unused pins as shown below.

Pin Name	Direction	Connection Method
DV(1:0)	I	Connect to ground
CLC	I	Connect to ground
PWR	I	Connect to ground
DCC	I	Switchable pull up or pull down is preferred

When this device is only one IDE controller in system, handle unused pins as shown below.

Pin Name	Direction	Connection Method
CMB_BSY	O	Open
CMB_STATE	I	Connect to ground

When the device needs not to control the power supply for IDE device, handle unused pins as shown below.

Pin Name	Direction	Connection Method
DPC	O	Open

CHAPTER 3 USB DESCRIPTOR INFORMATION

This chapter describes the default USB descriptors used in this device.

3.1 Device Descriptor

A device descriptor describes general information about a USB device. It includes information that applies globally to the device and the device's configuration.

Offset	Field	Size	Value	Description
0	bLength	byte	12H	Size of descriptor
1	bDescriptorType	byte	01H	Device descriptor Type
2	bcdUSB	word	0200H	USB specification version number (BCD)
4	bDeviceClass	byte	00H	Class Code
5	bDeviceSubClass	byte	00H	SubClass Code
6	bDeviceProtocol	byte	00H	Protocol Code
7	bMaxPacketSize0	byte	40H	Maximum packet size for this speed (64 byte)
8	idVender	word	0409H	NEC's vender ID
10	idProduct	word	006AH	μPD720130's product ID
12	bcdDevice	word	0000H	Device release number (BCD)
14	iManufacturer	byte	00H/01H	Index of string descriptor describing manufacturer
15	iProduct	byte	00H/02H	Index of string descriptor describing product
16	iSerialNumber	byte	00H/03H	Index of string descriptor describing device's serial number.
17	bNumConfigurations	byte	01H	Number of possible configuration

Remarks 1. The value of idVender, idProduct, and bcdDevice are loaded from serial ROM.

2. The value of iManufacturer, iProduct, and iSerialNumber are defined by data in serial ROM. If serial ROM does not have string descriptors, the iManufacturer, iProduct, or/and iSerialNumber are set to "00H".

3.2 String Descriptor

String descriptors describe Language ID, Manufacturer, Product and/or Serial Number. Serial ROM may have string data for Manufacturer, Product and Serial Number.

Language ID (string descriptor index 0)

Offset	Field	Size	Value	Description
0	bLength	byte	4H	Size of descriptor
1	bDescriptorType	byte	03H	String descriptor Type
2	WLANGID[0]	word	0409H	General (US English)

Standard string descriptor format for index 1-3

Offset	Field	Size	Value	Description
0	bLength	byte	XH	Size of descriptor
1	bDescriptorType	byte	03H	String descriptor Type
2	bString	N	XXXXH	UNICODE encoded string

3.2.1 Examples for string descriptor

This section describes the string descriptors for following samples.

Manufacturer : NEC
Product : uPD720130 Sample Board
Serial Number : 1.00

Manufacturer (string descriptor index 1)

Offset	Field	Size	Value	Description
0	bLength	byte	8H	Size of descriptor
1	bDescriptorType	byte	03H	String descriptor Type
2	bString	N	004E 0045 0043H	

Product (string descriptor index 2)

Offset	Field	Size	Value	Description
0	bLength	byte	2EH	Size of descriptor
1	bDescriptorType	byte	03H	String descriptor Type
2	bString	N	0075 0050 0044 0037 0032 0030 0031 0033 0030 0020 0053 0061 006D 0070 006C 0065 0020 0042 006F 0061 0072 0064H	

Serial Number (string descriptor index 3)

Offset	Field	Size	Value	Description
0	bLength	byte	0AH	Size of descriptor
1	bDescriptorType	byte	03H	String descriptor Type
2	bString	N	0031 002E 0030 0030H	

3.3 Device Qualifier Descriptor

A device qualifier descriptor describes general information about a high-speed capable device that would change if the device were operating at the other speed. For example, if the device is currently operating at full-speed, the device qualifier returns information about how it would operate at high-speed and vice-versa.

Offset	Field	Size	Value	Description
0	bLength	byte	0AH	Size of descriptor
1	bDescriptorType	byte	06H	Device qualifier descriptor type
2	bcdUSB	word	0200H	USB specification version number (BCD)
4	bDeviceClass	byte	00H	Class Code
5	bDeviceSubClass	byte	00H	SubClass Code
6	bDeviceProtocol	byte	00H	Protocol Code
7	bMaxPacketSize0	byte	40H	Maximum packet size for this speed (64 bytes)
8	bNumConfigurations	byte	01H	Number of this speed configuration
9	bReserved	byte	00H	Reserved for future use.

3.4 Configuration Descriptor

A configuration descriptor describes information about a specific device configuration. When the host requests the configuration descriptor, all related interface and endpoint descriptors are returned.

Offset	Field	Size	Value	Description
0	bLength	byte	09H	Size of descriptor
1	bDescriptorType	byte	02H	Configuration descriptor type
2	wTotalLength	word	0020H	Total length of data returned for this configuration.
4	bNumInterfaces	byte	01H	Number of interfaces supported by this configuration
5	bConfigurationValue	byte	01H	Value to use to select configuration
6	iConfiguration	byte	00H	Index of string descriptor describing configuration.
7	bmAttributes	byte	C0H/80H	Configuration characteristics
8	bMaxPower	byte	01H/FAH	Maximum power consumption of the USB device from the bus in this configuration when the device is fully operational. Expressed in 2 mA units

Remark The value of bmAttributes and bMaxPower are defined by the data in serial ROM. When this device set as bus powered, bmAttributes = 80H and bMaxPower = FAH. On the other hands, when this device set as self powered, bmAttributes = C0H and bMaxPower = 01H.

3.5 Other_Speed_Configuration Descriptor

An other_speed_configuration descriptor describes a configuration of a high-speed capable device if it were operating at its other possible speed. The structure of the other_speed_configuration is identical to a configuration descriptor. When the host requests the other_speed_configuration descriptor, all related interface and endpoint descriptors are returned.

Offset	Field	Size	Value	Description
0	bLength	byte	09H	Size of descriptor
1	bDescriptorType	byte	07H	Other_speed_configuration descriptor type
2	wTotalLength	word	0020H	Total length of data returned for this configuration.
4	bNumInterfaces	byte	01H	Number of interfaces supported by this speed configuration
5	bConfigurationValue	byte	01H	Value to use to select configuration
6	iConfiguration	byte	00H	Index of string descriptor describing configuration.
7	bmAttributes	byte	C0H/80H	Configuration characteristics
8	bMaxPower	byte	01H/FAH	Maximum power consumption of the USB device from the bus in this configuration when the device is fully operational.

Remark The value of bmAttributes and bMaxPower are defined by the data in serial ROM. When this device set as bus powered, bmAttributes = 80H and bMaxPower = FAH. On the other hands, when this device set as self powered, bmAttributes = C0H and bMaxPower = 01H.

3.6 Interface Descriptor

An interface descriptor describes a specific interface within a configuration. An interface descriptor is returned as part of the configuration information returned by a GET_DESCRIPTOR Configuration request.

Offset	Field	Size	Value	Description
0	bLength	byte	09H	Size of descriptor
1	bDescriptorType	byte	04H	Interface descriptor type
2	bInterfaceNumber	byte	00H	Number of interface
3	bAlternateSetting	byte	00H	Value used to select alternate setting for the interface identified in the prior field
4	bNumEndpoints	byte	02H	Number of endpoints used by this interface
5	bInterfaceClass	byte	08H/FFH	Class Code
6	bInterfaceSubClass	byte	05H/06H/FFH	SubClass Code
7	bInterfaceProtocol	byte	50H	Protocol Code
8	iInterface	byte	00H	Index of string descriptor describing interface

Remarks 1. The values of bInterfaceClass, bInterfaceSubClass, and bInterfaceProtocol are defined by connected IDE device type as shown in following table. It is possible to change these values by using serial ROM.

2. When the attached IDE device is broken, this device uses Class, SubClass, and Protocol values for none connected device.

Device Type	bInterfaceClass	bInterfaceSubClass	bInterfaceProtocol
None connected device	FFH	FFH	50H
ATA	08H	06H	50H
ATAPI	08H	05H	50H

3.7 Endpoint Descriptor

Each endpoint used for an interface has its own descriptor. This descriptor contains the information required by the host to determine the bandwidth requirements of each endpoint. An endpoint descriptor is always returned as part of the configuration information returned by a GET_DESCRIPTOR Configuration request.

3.7.1 Bulk in endpoint descriptor

Offset	Field	Size	Value	Description
0	bLength	byte	07H	Size of descriptor
1	bDescriptorType	byte	05H	Endpoint descriptor type
2	bEndpointAddress	byte	81H	In endpoint 1
3	bmAttributes	byte	02H	Endpoint's attributes (Bulk)
4	wMaxPacketSize	word	0040H/0200H	Maximum packet size
6	bInterval	byte	00H	Interval for polling endpoint for data transfers.

Remark The value of wMaxPacketSize is defined by the device operation mode. When this device is operating at full-speed mode, wMaxPacketSize is 40H (64 bytes). On the other hands, when this device is operating at high-speed mode, wMaxPacketSize is 200H (512 bytes).

3.7.2 Bulk out endpoint descriptor

Offset	Field	Size	Value	Description
0	bLength	byte	07H	Size of descriptor
1	bDescriptorType	byte	05H	Endpoint descriptor type
2	bEndpointAddress	byte	02H	Out endpoint 2
3	bmAttributes	byte	02H	Endpoint's attributes (Bulk)
4	wMaxPacketSize	word	0040H/0200H	Maximum packet size
6	bInterval	byte	00H	Interval for polling endpoint for data transfers.

Remark The value of wMaxPacketSize is defined by the device operation mode. When this device is operating at full-speed mode, wMaxPacketSize is 40H (64 bytes). On the other hands, when this device is operating at high-speed mode, wMaxPacketSize is 200H (512 bytes).

CHAPTER 4 REQUEST-DECODE TABLE

Request processing for control transfer is shown in the tables below.

4.1 USB Standard Requests

(1/2)

No	Field	bmRequest Type	bRequest	wValue		wIndex		wLength		Df[Note 1]	Ad[Note 2]	Cf[Note 3]
	Offset	0	1	3	2	5	4	7	6			
1	CLEAR_FEATURE Device (HW)[Note 4]	00H	01H	00H	01H	00H	00H	00H	00H	ACK NAK	ACK NAK	ACK NAK
2	CLEAR_FEATURE Endpoint 0 (HW)[Note 4]	02H	01H	00H	00H	00H	00H 80H	00H	00H	ACK NAK	ACK NAK	ACK NAK
3	CLEAR_FEATURE Endpoint 1 (HW)[Note 4]	02H	01H	00H	00H	00H	81H	00H	00H	STALL	STALL	ACK NAK
4	CLEAR_FEATURE Endpoint 2 (HW)[Note 4]	02H	01H	00H	00H	00H	02H	00H	00H	STALL	STALL	ACK NAK
5	GET_CONFIGURATION (HW)	80H	08H	00H	00H	00H	00H	00H	01H	ACK NAK	ACK NAK	ACK NAK
6	GET_DESCRIPTOR Device (FW)	80H	06H	01H	00H	00H	00H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
7	GET_DESCRIPTOR Device Qualifier (FW)	80H	06H	06H	00H	00H	00H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
8	GET_DESCRIPTOR Configuration (FW)	80H	06H	02H	00H	00H	00H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
9	GET_DESCRIPTOR Other Speed Configuration (FW)	80H	06H	07H	00H	00H	00H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
10	GET_DESCRIPTOR String(Index=00) (FW)	80H	06H	03H	00H	04H 00H	09H 00H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
11	GET_DESCRIPTOR[Note 6] String(Index=01) (FW)	80H	06H	03H	01H	04H	09H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
12	GET_DESCRIPTOR[Note 6] String(Index=02) (FW)	80H	06H	03H	02H	04H	09H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
13	GET_DESCRIPTOR[Note 6] String(Index=03) (FW)	80H	06H	03H	03H	04H	09H	XX	XX[Note 5]	ACK NAK	ACK NAK	ACK NAK
14	GET_INTERFACE (HW)	81H	0AH	00H	00H	00H	00H	00H	01H	STALL	STALL	ACK NAK
15	GET_STATUS Device (HW)	80H	00H	00H	00H	00H	00H	00H	02H	ACK NAK	ACK NAK	ACK NAK
16	GET_STATUS Interface (FW)	81H	00H	00H	00H	00H	00H	00H	02H	ACK NAK	ACK NAK	ACK NAK
17	GET_STATUS Endpoint 0 (HW)	82H	00H	00H	00H	00H	00H 80H	00H	02H	ACK NAK	ACK NAK	ACK NAK
18	GET_STATUS Endpoint 1 (HW)	82H	00H	00H	00H	00H	81H	00H	02H	STALL	STALL	ACK NAK
19	GET_STATUS Endpoint 2 (HW)	82H	00H	00H	00H	00H	02H	00H	02H	STALL	STALL	ACK NAK
20	SET_ADDRESS (HW)[Note 7]	00H	05H	00H	XX	00H	00H	00H	00H	ACK NAK	ACK NAK	ACK NAK
21	SET_CONFIGURATION (HW)	00H	09H	00H	00H 01H	00H	00H	00H	00H	ACK NAK	ACK NAK	ACK NAK

(2/2)

No	Field	bmRequest Type	bRequest	wValue		wIndex		wLength		Df[Note 1]	Ad[Note 2]	Cf[Note 3]
	Offset	0	1	3	2	5	4	7	6			
22	SET_FEATURE Device (HW) [Note 8]	00H	03H	00H	01H	00H	00H	00H	00H	ACK NAK	ACK NAK	ACK NAK
23	SET_FEATURE Endpoint 0 (HW)[Note 8]	02H	03H	00H	00H	00H	00H 80H	00H	00H	ACK NAK	ACK NAK	ACK NAK
24	SET_FEATURE Endpoint 1 (HW)[Note 8]	02H	03H	00H	00H	00H	81H	00H	00H	STALL	STALL	ACK NAK
25	SET_FEATURE Endpoint 2 (HW)[Note 8]	02H	03H	00H	00H	00H	02H	00H	00H	STALL	STALL	ACK NAK
26	SET_FEATURE TEST_MODE (TEST_J) (HW)	00H	03H	00H	02H	01H	00H	00H	00H	ACK NAK	ACK[Note 9] NAK	ACK[Note 9] NAK
27	SET_FEATURE TEST_MODE (TEST_K) (HW)	00H	03H	00H	02H	02H	00H	00H	00H	ACK NAK	ACK[Note 9] NAK	ACK[Note 9] NAK
28	SET_FEATURE TEST_MODE (TEST_SE0) (HW)	00H	03H	00H	02H	03H	00H	00H	00H	ACK NAK	ACK[Note 9] NAK	ACK[Note 9] NAK
29	SET_FEATURE TEST_MODE (TEST_PRBS) (HW)	00H	03H	00H	02H	04H	00H	00H	00H	ACK NAK	ACK[Note 9] NAK	ACK[Note 9] NAK
30	SET_FEATURETEST_MODE (TEST_FORCE) (HW)	00H	03H	00H	02H	05H	00H	00H	00H	ACK NAK	ACK[Note 9] NAK	ACK[Note 9] NAK
31	SET_INTERFACE (HW)	01H	0BH	00H	00H	00H	00H	00H	00H	STALL	STALL	ACK NAK
32	Other USB standard request	XX	XX	XX	XX	XX	XX	XX	XX	STALL	STALL	STALL

Notes 1. Response in Default state

2. Response in Addressed state

3. Response in Configured state

4. CLEAR_FEATURE Endpoint 0 request clears the endpoint 0's status (halt feature) when the token packet of the status stage has been correctly received. The other CLEAR_FEATURE requests clear the device status (remote wake up feature) or each endpoint's status except for endpoint 0 when the device receives ACK handshake from host in the status stage.

5. If the descriptor is longer than the *wLength* field, only the initial bytes of the descriptor are returned. If the descriptor is shorter than the *wLength* field, the device indicates the end of the control transfer by sending a short packet when further data is requested.

6. If a device does not support a requested string descriptor except for index 1, 2, 3, it responds with STALL handshake in the Data stage.

7. The device automatically responds by STALL handshake if the wValue value (address) is 128 or more.

8. SET_FEATURE sets the device status or each endpoint's status when the device receives ACK handshake from host in the status stage. If the halt feature of endpoint 0 is set, the device responds by STALL handshake in the Data stage of control transfers except for GET_STATUS Endpoint 0, SET_FEATURE Endpoint 0, and Mass storage class requests.

The device responds by STALL handshake for unsupported requests as Request Error. At this case, the halt feature of endpoint 0 is not set. The STALL handshake is cleared as soon as the next Setup token has been received.

9. For high-speed mode, the response for SET_FEATURE TEST_MODE request is defined in only Default state, There is no definition for the response in Address or Configured state. But the device handles this request as valid request even in Address or Configured state. On the other hand, The device automatically responds by STALL handshake even in the Default, Address, and Configured states in full-speed mode.

4.2 USB Mass Storage Class Requests

No	Field	bmRequest Type	bRequest	wValue		wIndex		wLength		Df[Note 1]	Ad[Note 2]	Cf[Note 3]
	Offset	0	1	3	2	5	4	7	6			
1	BULK-ONLY_MASS_ STORAGE_RESET (FW)	41H	FFH	XX Note 4	XX Note 4	XX Note 4	XX Note 4	XX Note 4	XX Note 4	ACK NAK	ACK NAK	ACK NAK
2	GET_MAX_LUN (FW)	A1H	FEH	XX Note 5	XX Note 5	XX Note 5	XX Note 5	XX Note 5	XX Note 5	ACK NAK	ACK NAK	ACK NAK

Notes 1. Response in Default state

2. Response in Addressed state

3. Response in Configured state

4. USB specification for Mass storage class specifies the wValue as 0000H, the wIndex as 0000H, and the wLength as 0000H. This device does not decode the wValue, wIndex, and wLength values because the device driver shall not issue invalid packet.

5. USB specification for Mass storage class specifies the wValue as 0000H, the wIndex as 0000H, and the wLength as 0001H. This device does not decode the wValue, wIndex, and wLength values because the device driver shall not issue invalid packet.

4.3 Supplement on USB Protocol

(1) When the sequence of control transfer does not comply with Universal Serial Bus Specifications 2.0,

a: If an IN or OUT token is received without a Setup stage or if an IN or OUT token is received after previous control transfer is completed.

ex. Setup → IN → OUT → IN, Setup → IN → OUT → OUT[Note]

Note This token is not the retry of previous token packet. This means that previous transaction is completed without error.

At this time, this device does not respond by any handshake or data transmission to these abnormal tokens.

b: This device does not respond by any handshake if the DATA PID in Setup stage is not DATA0.

c: If the received data in the Setup stage is not 8 bytes, it is assumed that the packet has been destroyed and the device does not respond by any handshake to the Setup token.

(2) Even if the host transmits data longer than 0 bytes in the Status stage, the device processes the Status stage correctly and responds by ACK handshake to the Status stage.

(3) When the wLength value of the Control Read transfer is 0x00, the device returns null byte packet as a No Data control transfer.

(4) If an IN token that is not a retry is received even when a short packet has been returned to the host by Control Read, the device responds by STALL handshake.

(5) If the data structure is an exact multiple of wMaxPacketSize for the pipe, the function will return a zero-length packet to indicate the end of the Data stage. If an IN token is received even when the zero-length packet has been correctly transmitted, the device responds by STALL handshake.

(6) When wLength ≠ 0 and the direction indicated by bmRequestType is different from the token packet for Data stage, the device responds by STALL handshake. When wLength = 0 (No Data Control) and a host issues Setup transaction followed by OUT token, the device responds by STALL handshake.

4.4 Processing of USB Requests

This section summarizes the response of this device for defined USB request.
The operation changes depending on the following states:

Default: State in which this device operates with the Default USB address.
Address: State after assignment of USB address
Configured: State after correctly receiving SET_CONFIGURATION wValue = 1

4.4.1 CLEAR_FEATURE()

If CLEAR_FEATURE() has been correctly processed, the halt feature of the endpoint status or the remote wake up feature of the device status is cleared. The cleared feature is specified by wIndex field of CLEAR_FEATURE() request. A CLEAR_FEATURE() request that references a feature that cannot be cleared, that does not exist, or that references an interface or endpoint that does not exist will cause the device to respond with STALL handshake. The device responds by STALL handshake if the wLength value is other than 0.

Default: When the recipient of this request is a device or endpoint 0 and a feature selector of this request is valid, the device processes this request. The references to interfaces or to endpoints other than endpoint zero shall cause the device to respond with STALL handshake in Status stage.
Address: When the recipient of this request is a device or endpoint 0 and a feature selector of this request is valid, the device processes this request. The references to interfaces or to endpoints other than endpoint zero shall cause the device to respond with STALL handshake in Status stage.
Configured: When the recipient of this request is a device or endpoint that exists and a feature selector of this request is valid, the device processes this request. The references to interfaces shall cause the device to respond with STALL handshake in Status stage.

4.4.2 GET_CONFIGURATION()

When GET_CONFIGURATION() has been correctly received, the current device configuration value is transmitted. If wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by STALL handshake in the Data stage.

Default: The value zero shall be returned when this request is received.
Address: The value zero shall be returned when this request is received.
Configured: The current device configuration value is returned when this request is received.

4.4.3 GET_DESCRIPTOR()

When GET_ DESCRIPTOR() has been correctly received, the expected descriptors are transmitted. The *wIndex* field specifies the Language ID for string descriptors or is reset to zero for other descriptors. If the descriptor is longer than the *wLength* field, only the initial bytes of the descriptor are returned. If the descriptor is shorter than the *wLength* field, the device indicates the end of the control transfer by sending a short packet when further data is requested. A short packet is defined as a packet shorter than the maximum payload size or a zero length data packet. The other_speed_configuration returns information in the same structure as a configuration descriptor, but for a configuration if the device were operating at the other speed. A request for a configuration descriptor returns the configuration descriptor, all interface descriptors, and endpoint descriptors for all of the interfaces in a single request. The first interface descriptor follows the configuration descriptor. The endpoint descriptors for the first interface follow the first interface descriptor. If a device does not support a requested descriptor, it responds with STALL handshake in the Data stage.

Default: The expected descriptors are returned when this request is received.
Address: The expected descriptors are returned when this request is received.
Configured: The expected descriptors are returned when this request is received.

4.4.4 GET_INTERFACE()

When GET_INTERFACE() has been correctly received, the value zero is transmitted. If wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by STALL handshake in the Data stage.

Default: STALL handshake response in Data stage when this request is received
Address: STALL handshake response in Data stage when this request is received
Configured: Value 0 is returned when this request is received.

4.4.5 GET_STATUS()

When GET_STATUS() has been correctly received, the endpoint status or the device status is transmitted. If wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by STALL handshake in the Data stage. When the recipient of this request is a interface, the device returns “00H” instead of STALL handshake.

Default: When the recipient of this request is a device or endpoint 0, the device returns the expected value. The references to endpoints other than endpoint zero shall cause the device to respond with STALL handshake in Data stage.
Address: When the recipient of this request is a device or endpoint 0, the device returns the expected value. The references to endpoints other than endpoint zero shall cause the device to respond with STALL handshake in Data stage.
Configured: When the recipient of this request is a device or endpoint that exists, the device returns the expected value.

4.4.6 SET_ADDRESS()

If SET_ADDRESS() has been correctly processed, the device is put into Address state and the *wValue* field specifies the device address to use for all subsequent accesses. The device does not change its device address until after the status stage of this request is completed successfully. If wIndex, and wLength are other than the values shown in the request-decode table or the specified device address is greater than 127, the device responds by STALL handshake in the Status stage.

Default: If the specified address is non-zero, the device enters the Address state and changes the USB address. Otherwise, the device remains in the Default state if the specified address is 0.

Address: The device enters the Default state if the specified address is 0. If the specified address is other than 0, the device remains in the Address state, but use the newly specified address.

Configured: The device enters unknown state. The device does not guarantee any further operation.

4.4.7 SET_CONFIGURATION()

If SET_CONFIGURATION() has been correctly processed, the device is put into Configured state. Even if the specified configuration value is the same as the current configuration value, the halt features of all endpoint status are cleared and the data toggle bit of all endpoints are initialized to DATA0 again after the request has been completed. If wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by STALL handshake in the Status stage.

Default: The device enters unknown state. The device does not guarantee any further operation.

Address: If the specified configuration value is 1, the device enters the Configured state. If the specified configuration value is 0, the device remains in the Address state.

Configured: If the specified configuration value is 0, the device returns to the Address state. If the specified configuration value is 1, the device remains in the Configured state.

4.4.8 SET_FEATURE() (Except for TEST_MODE)

If SET_FEATURE() (except for TEST_MODE) has been correctly processed, the halt feature of the endpoint status or the remote wake up feature of the device status is set. The set feature is specified by wIndex field of SET_FEATURE() request. A SET_FEATURE() request that references a feature that cannot be set, that does not exist, or that references an interface or endpoint that does not exist will cause the device to respond with STALL handshake. The device responds by STALL handshake if the wLength value is other than 0.

Default: When the recipient of this request is a device or endpoint 0 and a feature selector of this request is valid, the device processes this request. The references to interfaces or to endpoints other than endpoint zero shall cause the device to respond with STALL handshake in Status stage.

Address: When the recipient of this request is a device or endpoint 0 and a feature selector of this request is valid, the device processes this request. The references to interfaces or to endpoints other than endpoint zero shall cause the device to respond with STALL handshake in Status stage.

Configured: When the recipient of this request is a device or endpoint that exists and a feature selector of this request is valid, the device processes this request. The references to interfaces shall cause the device to respond with STALL handshake in Status stage.

4.4.9 SET_FEATURE() (TEST_MODE)

If SET_FEATURE() (TEST_MODE) has been correctly received in HS mode, USB transceiver will perform the test operation defined by TEST_MODE. Setting the TEST_MODE feature puts the device upstream facing port into test mode. The power to the device must be cycled to exit test mode of an upstream facing port of a device. If wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by STALL handshake in the Status stage. If SET_FEATURE() (TEST_MODE) is received in FS mode, the device responds by STALL handshake in all the Default, Address, and Configured states.

Default: The test mode defined by the wIndex value is executed in the Default state. The transition to test mode of an upstream facing port does not happen until after the Status stage of the request.

- 01H: TEST_J
- 02H: TEST_K
- 03H: TEST_SE0_NAK
- 04H: TEST_Packet
- 05H: TEST_Force_Enable

Address: The test mode defined by the wIndex value is executed in the Address state.

Configured: The test mode defined by the wIndex value is executed in the Configured state

4.4.10 SET_INTERFACE()

If SET_INTERFACE() has been correctly processed, the halt features of all endpoint status are cleared and the data toggle bit of all endpoints are initialized to DATA0 again after the request has been completed. If wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by STALL handshake in the Status stage.

Default: The device responds with STALL handshake in Status stage.

Address: The device responds with STALL handshake in Status stage.

Configured: 0-length packet transmitted in Status stage.

4.4.11 BULK-ONLY_MASS_STORAGE_RESET()

If BULK-ONLY_MASS_STORAGE_RESET() has been correctly processed, the halt features of all endpoint status are cleared and the data toggle bit of all endpoints are initialized to DATA0 again after the request has been completed. Even if wValue, wIndex, and wLength are any other values, the device responds by ACK handshake in the Status stage.

Default: 0-length packet transmitted in Status stage.

Address: 0-length packet transmitted in Status stage.

Configured: 0-length packet transmitted in Status stage.

4.4.12 GET_MAX_LUN()

If GET_MAX_LUN() has been correctly processed, the value 00h is transmitted. Even if wValue, wIndex, and wLength are other than the values shown in the request-decode table, the device responds by the value 00h in the Status stage.

Default: The value 00H transmitted in Status stage.

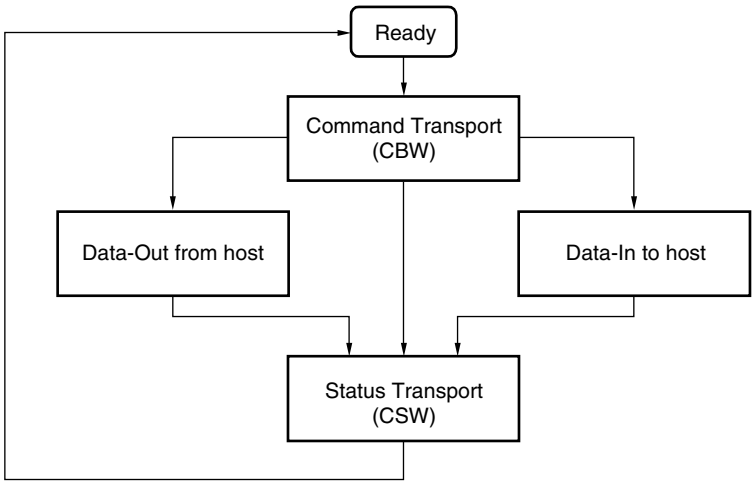
Address: The value 00H transmitted in Status stage.

Configured: The value 00H transmitted in Status stage.

4.5 Bulk-Only Transport Protocol

As shown in Figure 4-1, Bulk-Only Transport protocol consists of Command Transport, Data-In, Data-Out, and Status Transport. This section summarizes the protocol flow for Bulk-Only transport.

Figure 4-1. Bulk-Only Transport Protocol



4.5.1 Command transport

The host sends Command Block Wrapper (CBW) to device via Bulk-Out endpoint as the Command Transport. The CBW starts on the packet boundary and end as a short packet with exactly 31 (1FH) bytes transferred. The device indicates a successful transport of CBW by ACK handshake. If the host detects a STALL handshake of the Bulk-Out endpoint during Command Transport, the host shall respond with a Reset Recovery.

Table 4-1. Command Block Wrapper

Byte / bit	7	6	5	4	3	2	1	0
0-3	dCBWSignature = 43425355H (Little endian)							
4-7	dCBWTag							
8-11	dCBWDataTransferLength							
12	bmCBWFlags Bit 7 Direction 0: Data-Out from the host to the device. 1: Data-In from the device to the host. Bit 6:0 Reserved							
13	Reserved				bCBWLUN = 00H			
14	Reserved			bCBWCBLength				
15-30	CBWCB							

4.5.2 Data transport (Data-In or Data-Out)

All data transport shall begin on a packet boundary. The host shall attempt to transfer the exact number of bytes to or from the device as specified by the dCBWDataTransferLength and the Direction bit in CBW.

4.5.3 Status transport

The device sends Command Status Wrapper (CSW) to host via Bulk-In endpoint as the Status Transport. The CSW start on the packet boundary and end as a short packet with exactly 13 (DH) bytes transferred. The CSW indicates to the host the status of the execution of the command block from the corresponding CBW. The host shall perform a Reset Recovery when Phase Error status is returned in the CSW.

Table 4-2. Command Status Wrapper

Byte / bit	7	6	5	4	3	2	1	0
0-3	dCSWSignature = 53425355H (Little endian)							
4-7	DCSWTag							
8-11	DCSWDataResidue							
12	bCSWStatus							

Value	Description
00H	Command passed (“good status”)
01H	Command failed
02H	Phase Error
03H to FFH	Reserved

4.5.4 The thirteen cases

This section describes the thirteen possible cases of host expectations and device intent in the absence of overriding error conditions. Case (1), (6) and (12) represent the majority of host and device transactions. They indicate those conditions where the host and device agrees as to the direction and amount of data to be transferred.

Table 4-3. Host / Device Data Transfer Matrix

		Host		
		Hn	Hi	Ho
Device	Dn	(1) Hn = Dn	(4) Hi > Dn	(9) Ho > Dn
	Di	(2) Hn < Di	(5) Hi > Di	(10) Ho <> Di
			(6) Hi = Di	
			(7) Hi < Di	
	Do	(3) Hn < Do	(8) Hi <> Do	(11) Ho > Do
				(12) Ho = Do
				(13) Ho < Do

Remarks 1. Host Expectation

Hn : The host expects no data transfers.

Hi : The host expects to receive data from the device.

Ho : The host expects to transmit data to the device.

2. Device Intent

Dn : The device intends to transfer no data.

Di : The device intends to transmit data to the host.

Do : The device intends to receive data from the host.

Case (1) : If the device have no data to transmit or receive, then the device will set bCSWStatus to 00H or 01H and dCSWDataResidue to 0.

Case (2) : If the device have data to transmit, then the device will set bCSWStatus to 02H. At this case, the Endpoint 1 (Bulk-In) status is set to halt feature.

Case (3) : If the device need to receive data, then the device will set bCSWStatus to 02H. At this case, the Endpoint 1 (Bulk-In) status is set to halt feature.

Case (4) : If the device does not intend to transmit any data, then the Endpoint 1 (Bulk-In) endpoint status is set to halt feature.

Case (5) : If the device intends to transmit less data than dCBWDataTransferLength, then the device will transmit less data than dCBWDataTransferLength and may end the transfer with a short packet. And the device will set bCSWStatus to 00H or 01H and bCSWDataResidue to the difference between bCBWDataTransferLength and the actual amount of relevant data transmit.

Case (6) : If the device intends to transmit dCBWDataTransferLength, then the device will transmit dCBWDataTransferLength bytes of data. And the device will set bCSWStatus to 00H or 01H and dCSWDataResidue to 0.

Case (7) : If the device intends to transmit more data than dCBWDataTransferLength, then the device will transmit data up to dCBWDataTransferLength. And the device will set bCSWStatus to 02H. At this case, the Endpoint 1 (Bulk-In) status is set to halt feature.

Case (8) : If the device intends to receive data from the host, then the device will transmit 0-length packet to end transfer. And the device will set bCSWStatus to 02H. At this case, the Endpoint 1 (Bulk-In) status is set to halt feature. If the host indicates Data-In transport in CBW, but host issues PING/OUT packet to endpoint 2 of the device, the device will send NAK handshake continuously.

Case (9) : If the device does not intend to process any data, but the device will receive data. The device will end the transfer by STALL the Endpoint 2 (Bulk-Out). And the device will set bCSWStatus to 00H or 01H and bCSWDataResidue to the difference between bCBWDataTransferLength and the actual amount of data was processed by the device.

Case (10) : If the device intends to transmit data, but, the device will receive data. The device will end the transfer prematurely by STALL the Endpoint 2 (Bulk-Out). And the device will set bCSWStatus to 02H. At this case, the Endpoint 1 (Bulk-In) status is set to halt feature.

Case (11) : If the device intends to process less than the amount of data that indicated in dCBWDataTransferLength field, then the device will receive intended data. The device will accept a total of dCBWDataTransferLength. And the device will set bCSWStatus to 00H or 01H and bCSWDataResidue to the difference between bCBWDataTransferLength and the actual amount of data was processed by the device. Although the host sends less than dCBWDataTransferLength of data, If the host finishes Data transport and starts CSW, the device will send NAK handshake continuously.

Case (12) : If the device intends to process equal to the amount of data that indicated in dCBWDataTransferLength field, then the device will receive intended data. And the device will set bCSWStatus to 00H or 01H and bCSWDataResidue to 0.

Case (13) : If the device intends to process more data than dCBWDataTransferLength, then the device will receive data up to a total of dCBWDataTransferLength. The device will accept a total of dCBWDataTransferLength. And the device will set bCSWStatus to 02H. At this case, the Endpoint 1 (Bulk-In) status is set to halt feature.

CHAPTER 5 STALL OR NO HANDSHAKE

The error handling in this chip is defined as follows.

Transfer Type	Transaction	Packet	Error Type	Function Response	Processing
NA	NA	Token	PID Check error	No response	None
NA	NA	Token	Unsupported PID	No response	None
Control/Bulk	In/Out/Setup	Token	Unsupported Endpoint	No response	None
Control/Bulk	In/Out/Setup	Token	Mismatch the transfer direction for Endpoint	No response	None
Control/Bulk	In/Out/Setup	Token	CRC error	No response	None
Control/Bulk	In/Out/Setup	Token	Bit Stuffing error	No response	None
Control/Bulk	Out/Setup	Data	Timeout	No response	None
Control/Bulk	Out/Setup	Data	PID Check error	No response	None
Control/Bulk	Out/Setup	Data	Unsupported PID (other than data PID)	No response	None
Control/Bulk	Out/Setup	Data	CRC error	No response	Discards received data.
Control/Bulk	Out/Setup	Data	Bit Stuffing error	No response	Discards received data.
Control/Bulk	Out	Data	Data PID mismatch	ACK	Discards received data.
Control (Setup Stage)	Setup	Data	Overrun	No response	Discards received data.
Control (Data Stage)	Out	Data	Overrun	No response[Note 1]	Discards received data.
Control (Status Stage)	Out	Data	Overrun	ACK or no response[Note 2]	Discards received data.
Bulk	Out	Data	Overrun	No response[Note 1]	Sets halt feature in endpoint 1 or 2 status
Control/Bulk	In	Handshake	PID Check error	–	Holds transmitted data and retries[Note 3].
Control/Bulk	In	Handshake	Unsupported PID (other than ACK PID)	–	Holds transmitted data and retries[Note 3].
Control/Bulk	In	Handshake	Timeout	–	Holds transmitted data and retries[Note 3].

Notes 1. If the host retries the previous transfer, the device responds it by STALL handshake.

2. If the transfer data is less than the maximum packet size, the device responds by ACK handshake and discards received data. If the transfer data is greater than the maximum packet size, the device discards received data and does not respond by any handshake.

3. For Control transfer, the host that successfully received the data of the last IN(Data stage) for Control transfer will send ACK. Later, the host will issue an OUT token to start the Status stage of the transfer. If the device did not receive the ACK that ended the Data stage, the device will interpret the start of the Status stage as proof that the host successfully received the data.

Remark Response if two or more conditions overlap

• Response to OUT

Data Packet Error (Including Overrun)	halt feature	Data PID Mismatch	Data Reception Possible	Function Response
Yes	N/A	N/A	N/A	No response
No	Set	N/A	N/A	STALL
No	Not set	No	N/A	ACK
No	Not set	Yes	Yes	ACK[Note]
No	Not set	Yes	No	NAK

Note The device may use an NYET handshake instead of ACK handshake during high-speed operation

• Response to IN

Data Packet Error (Including Overrun)	halt feature	Data Reception Possible	Function Response
Yes	N/A	N/A	No response
No	Set	N/A	STALL
No	Not set	No	NAK
No	Not set	Yes	Issues data packet

CHAPTER 6 SERIAL ROM INFORMATION

This device loads configuration data such as Vendor ID, Product ID and some additional USB related information from serial ROM when the device is initialized. This chapter explains the data in serial ROM. Tool is released for serial ROM data configuration.

Detailed information of tools is provided in following application note. Read the application note when preparing serial ROM data for this device.

μPD720130 Application Note: S16447E

6.1 Serial ROM Format

Offset (H)	Data Size	Symbol	Description
+00	1 Word	idMark	Validation Mark of 55AAH
+02	1 Word	CheckSum	Check sum of serial ROM
+04	1 Word	Flags	Control for descriptor overwrite
+06	1 Byte	ExPinReset	PWR, CLC, DCC, DV[1:0] Reset bit map field
+07	1 Byte	ExPinSet	PWR, CLC, DCC, DV[1:0] Set bit map field
+08	1 Word	idVendor	idVendor field in Device descriptor
+0A	1 Word	idProduct	idProduct field in Device descriptor
+0C	1 Word	bcdDevice	bcdDevice field in Device descriptor
+0E	1 Word	Reserved	Reserved for future use.
+10	1 Byte	MaxPower Bus	bMaxPower field in Configuration descriptor for Bus powered mode
+11	1 Byte	MaxPower Self	bMaxPower field in Configuration descriptor for Self powered mode
+12	1 Byte	bInterfaceClass	bInterfaceClass field in Interface descriptor
+13	1 Byte	bInterfaceSubClass	bInterfaceSubClass field in Interface descriptor
+14	1 Byte	bInterfaceProtocol	bInterfaceProtocol field in Interface descriptor
+15	1 Byte	Reserved	Reserved for future use.
+16	1Word	TxModeReset	IDE transmission type such as Ultra DMA 66 Reset bit map field
+18	1Word	TxModeSet	IDE transmission type such as Ultra DMA 66 Set bit map field
+1A	6 Bytes	Reserved	Reserved for future use.
+20	32 Bytes	ManufactureString	String descriptor for Manufacturer
+40	32 Bytes	ProductString	String descriptor for Product
+60	32 Bytes	SerialString	String descriptor for Device serial number

6.1.1 Flags format

Bit	15	14	13	12	11	10	9	8
Name	0	0	0	0	0	0	0	0
Bit	7	6	5	4	3	2	1	0
Name	FWDL_ BUS	FWDL_ SELF	STR3_ AVAIL	STR2_ AVAIL	STR1_ AVAIL	IFOR_ AVAIL	CFOR_ AVAIL	EPOR_ AVAIL

Bit	Name	Description
15 - 8	Reserved	Reserved for future use.
7	FWDL_BUS	Set if additional firmware for bus powered application to be loaded. (For future release) 1: Firmware will be loaded from serial ROM (After offset 128 bytes) 0: Not used.
6	FWDL_SELF	Set if additional firmware for self powered application to be loaded. (For future release) 1: Firmware will be loaded from serial ROM (After offset 128 bytes) 0: Not used
5	STR3_AVAIL	Set if SerialString (String descriptor for Device serial number) is available. 1: Data in SerialString field is used as String descriptor for Device serial number. iSerialNumber in Device descriptor is set to “03H”. 0: No String descriptor for Device serial number. iSerialNumber in Device descriptor is set to “00H”.
4	STR2_AVAIL	Set if ProductString (String descriptor for Product) is available. 1: Data in ProductString field is used as String descriptor for Product. iProduct in Device descriptor is set to “02H”. 0: No String descriptor for Product. iProduct in Device descriptor is set to “00h”.
3	STR1_AVAIL	Set if ManufactureString (String descriptor for Manufacturer) is available. 1: Data in ManufactureString field is used as String descriptor for Manufacturer. iManufacturer in Device descriptor is set to “01H”. 0: No String descriptor for Manufacturer. iManufacturer in Device descriptor is set to “00H”.
2	IFOR_AVAIL	Set if bInterfaceClass, bInterfaceSubClass, and bInterfaceProtocol fields in serial ROM are available. 1: Data in bInterfaceClass, bInterfaceSubClass, and bInterfaceProtocol fields are used as parts of interface descriptor. 0: Original Interface descriptor is used to return for GET_DESCRIPTOR Configuration.
1	CFOR_AVAIL	Set if MaxPower Bus and MaxPower Self fields in serial ROM are available. 1: Data in MaxPower Bus and MaxPower Self fields are used as parts of configuration descriptor. 0: Original Configuration descriptor is used to return for GET_DESCRIPTOR Configuration.
0	EPOR_AVAIL	Set if ExPinReset and ExPinSet fields in serial ROM are available. 1: Data in ExPinReset and ExPinSet fields are used to initialize the IDE controller instead of external pin setting. 0: External pins setting are used to initialize the IDE controller.

6.1.2 ExPinReset format

Bit	7	6	5	4	3	2	1	0
Name	0	0	DCC Reset	DV1 Reset	DV0 Reset	SPD Reset	CLC Reset	PWR Reset

Bit	Name	Description
7 – 6	Reserved	Reserved for future use.
5	DCC Reset	DCC Reset bit is used to control ATA Direct Command Controller and, etc instead of DCC pin setting. 1: ATA Direct Command Controller is disabled. IDE controller communicates with ATA device by fastest PIO mode. For ATAPI device, IDE controller communicates by fastest PIO or Multi Word DMA. 0: DCC pin setting is enabled.
4	DV1 Reset	DV1 Reset bit is used to control IDE controller instead of DV1 pin setting. 1: See the description of pin functionality for connecting DV1 pin input to “low”. 0: DV1 pin setting is enabled.
3	DV0 Reset	DV0 Reset bit is used to control IDE controller instead of DV0 pin setting. 1: See the description of pin functionality for connecting DV0 pin input to “low”. 0: DV0 pin setting is enabled.
2	SPD Reset	NEC Reserved. Set to “low” is required.
1	CLC Reset	CLC Reset bit is used to control IDE controller instead of CLC pin setting. 1: See the description of pin functionality for connecting CLC pin input to “low”. 0: CLC pin setting is enabled.
0	PWR Reset	PWR Reset bit is used to control IDE controller instead of PWR pin setting. 1: The device is working at self powered mode. 0: PWR pin setting is enabled.

Remarks 1. ExPinSet and ExPinReset fields have higher priority than external pin setting. Once these fields are set, related external pin settings are ignored.

2. ExPinSet field have higher priority than ExPinReset field.

6.1.3 ExPinSet format

Bit	7	6	5	4	3	2	1	0
Name	0	0	DCC Set	DV1 Set	DV0 Set	SPD Set	CLC Set	PWR Set

Bit	Name	Description
7 – 6	Reserved	Reserved for future use.
5	DCC Set	DCC Set bit is used to control ATA Direct Command Controller instead of DCC pin setting. 1: ATA Direct Command Controller is enabled. IDE controller communicates with ATA device by fastest mode. For ATAPI device, IDE controller communicates by fastest PIO, Multi Word DMA, or Ultra DMA. 0: DCC pin setting is enabled.
4	DV1 Set	DV1 Set bit is used to control IDE controller instead of DV1 pin setting. 1: See the description of pin functionality for connecting DV1 pin input to “high”. 0: DV1 pin setting is enabled.
3	DV0 Set	DV0 Set bit is used to control IDE controller instead of DV0 pin setting. 1: See the description of pin functionality for connecting DV0 pin input to “high”. 0: DV0 pin setting is enabled.
2	SPD Set	NEC Reserved. Set to “high” is required.
1	CLC Set	CLC Set bit is used to control IDE controller instead of CLC pin setting. 1: See the description of pin functionality for connecting CLC pin input to “high”. 0: CLC pin setting is enabled.
0	PWR Set	PWR Set bit is used to control IDE controller instead of PWR pin setting. 1: The device is working at bus powered mode. 0: PWR pin setting is enabled.

Remarks 1. ExPinSet and ExPinReset fields have higher priority than external pin setting. Once these fields are set, related external pin settings are ignored.

2. ExPinSet field have higher priority than ExPinReset field.

6.1.4 IDE state controlled by ExPinSet or ExPinReset fields

DV1/DV0, CLC, PWR Setting

No.	Device Power	Internal Clock	ATA/ATAPI	PWR	CLC	DV1	DV0
0	Bus Powered	7.5 MHz	No device connected	1	1	1	1
1			ATA	1	1	1	0
2			ATAPI	1	1	0	1
3			Reserved	1	1	0	0
4		60 MHz	No device connected	1	0	1	1
5			ATA	1	0	1	0
6			ATAPI	1	0	0	1
7			Reserved	1	0	0	0
8	Self Powered	60 MHz	No device connected	0	1	1	1
9			Combo (ATA)	0	1	1	0
10			Combo (ATAPI)	0	1	0	1
11			Combo auto device detect	0	1	0	0
12			No device connected	0	0	1	1
13			ATA	0	0	1	0
14			ATAPI	0	0	0	1
15			Auto device detect	0	0	0	0

Remarks 1. Setting of no. 0, 3, 4, 7, 8, and 12 are not allowed.

2. For Bus powered setting, there are some critical considerations such as power consumption for the total system should be observed.

DV1/DV0, DCC Setting

Condition				DCC Pin Setting	DCC Setting in Serial ROM	Description
DV1	DV0	Mode	Target Device			
1	0	ATA	ATA	0	No setting	Ultra, Multi Word DMA are disabled.
				0	Reset	Ultra, Multi Word DMA are disabled.
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra, Multi Word DMA are disabled.
				1	Set	Ultra, Multi Word DMA are enabled.
0	1	ATAPI	ATAPI	0	No setting	Ultra DMA are disabled
				0	Reset	Ultra DMA are disabled
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra DMA are disabled
				1	Set	Ultra, Multi Word DMA are enabled.
0	0	Auto device detect	ATA	0	No setting	Ultra, Multi Word DMA are disabled.
				0	Reset	Ultra, Multi Word DMA are disabled.
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra, Multi Word DMA are disabled.
				1	Set	Ultra, Multi Word DMA are enabled.
			ATAPI	0	No setting	Ultra DMA are disabled
				0	Reset	Ultra DMA are disabled
				0	Set	Ultra, Multi Word DMA are enabled.
				1	No setting	Ultra, Multi Word DMA are enabled.
				1	Reset	Ultra DMA are disabled
				1	Set	Ultra, Multi Word DMA are enabled.

Remark PIO mode 0-4 are always enabled.

6.1.5 TxModeReset format

Bit	15	14	13	12	11	10	9	8
Name	0	0	0	Ultra DMA Mode 4 Reset	Ultra DMA Mode 3 Reset	Ultra DMA Mode 2 Reset	Ultra DMA Mode 1 Reset	Ultra DMA Mode 0 Reset
Bit	7	6	5	4	3	2	1	0
Name	Multi Word DMA Mode 2 Reset	Multi Word DMA Mode 1 Reset	Multi Word DMA Mode 0 Reset	PIO Mode 4 Reset	PIO Mode 3 Reset	PIO Mode 2 Reset	PIO Mode 1 Reset	PIO Mode 0 Reset

Bit	Name	Description
15 – 13	Reserved	Reserved for future use.
12	Ultra DMA Mode 4 Reset	1: Ultra DMA Mode 4 function is disabled even if IDE device supports this function. 0: Ultra DMA Mode 4 function is enabled if IDE device supports this function.
11	Ultra DMA Mode 3 Reset	1: Ultra DMA Mode 3 function is disabled even if IDE device supports this function. 0: Ultra DMA Mode 3 function is enabled if IDE device supports this function.
10	Ultra DMA Mode 2 Reset	1: Ultra DMA Mode 2 function is disabled even if IDE device supports this function. 0: Ultra DMA Mode 2 function is enabled if IDE device supports this function.
9	Ultra DMA Mode 1 Reset	1: Ultra DMA Mode 1 function is disabled even if IDE device supports this function. 0: Ultra DMA Mode 1 function is enabled if IDE device supports this function.
8	Ultra DMA Mode 0 Reset	1: Ultra DMA Mode 0 function is disabled even if IDE device supports this function. 0: Ultra DMA Mode 0 function is enabled if IDE device supports this function.
7	Multi Word DMA Mode 2 Reset	1: Multi Word DMA Mode 2 function is disabled even if IDE device supports this function. 0: Multi Word DMA Mode 2 function is enabled if IDE device supports this function.
6	Multi Word DMA Mode 1 Reset	1: Multi Word DMA Mode 1 function is disabled even if IDE device supports this function. 0: Multi Word DMA Mode 1 function is enabled if IDE device supports this function.
5	Multi Word DMA Mode 0 Reset	1: Multi Word DMA Mode 0 function is disabled even if IDE device supports this function. 0: Multi Word DMA Mode 0 function is enabled if IDE device supports this function.
4	PIO Mode 4 Reset	1: PIO Mode 4 function is disabled even if IDE device supports this function. 0: PIO Mode 4 function is enabled if IDE device supports this function.
3	PIO Mode 3 Reset	1: PIO Mode 3 function is disabled even if IDE device supports this function. 0: PIO Mode 3 function is enabled if IDE device supports this function.
2	PIO Mode 2 Reset	1: PIO Mode 2 function is disabled even if IDE device supports this function. 0: PIO Mode 2 function is enabled if IDE device supports this function.
1	PIO Mode 1 Reset	1: PIO Mode 1 function is disabled even if IDE device supports this function. 0: PIO Mode 1 function is enabled if IDE device supports this function.
0	PIO Mode 0 Reset	1: PIO Mode 0 function is disabled even if IDE device supports this function. 0: PIO Mode 0 function is enabled if IDE device supports this function.

Remarks 1. TxModeSet and TxModeReset fields have higher priority than the information from IDE device. If any of TxModeReset field are set, related transaction modes supported by IDE device are disabled.

2. TxModeSet field have higher priority than TxModeReset field.

6.1.6 TxModeSet format

Only for debug: Should be set all bits to 00H.

Bit	15	14	13	12	11	10	9	8
Name	0	0	0	Ultra DMA Mode 4 Set	Ultra DMA Mode 3 Set	Ultra DMA Mode 2 Set	Ultra DMA Mode 1 Set	Ultra DMA Mode 0 Set
Bit	7	6	5	4	3	2	1	0
Name	Multi Word DMA Mode 2 Set	Multi Word DMA Mode 1 Set	Multi Word DMA Mode 0 Set	PIO Mode 4 Set	PIO Mode 3 Set	PIO Mode 2 Set	PIO Mode 1 Set	PIO Mode 0 Set

Bit	Name	Description
15 – 13	Reserved	Reserved for future use.
12	Ultra DMA Mode 4 Set	1: Ultra DMA Mode 4 function is enabled even if IDE device does not support this function. 0: Ultra DMA Mode 4 function is enabled if IDE device supports this function.
11	Ultra DMA Mode 3 Set	1: Ultra DMA Mode 3 function is enabled even if IDE device does not support this function. 0: Ultra DMA Mode 3 function is enabled if IDE device supports this function.
10	Ultra DMA Mode 2 Set	1: Ultra DMA Mode 2 function is enabled even if IDE device does not support this function. 0: Ultra DMA Mode 2 function is enabled if IDE device supports this function.
9	Ultra DMA Mode 1 Set	1: Ultra DMA Mode 1 function is enabled even if IDE device does not support this function. 0: Ultra DMA Mode 1 function is enabled if IDE device supports this function.
8	Ultra DMA Mode 0 Set	1: Ultra DMA Mode 0 function is enabled even if IDE device does not support this function. 0: Ultra DMA Mode 0 function is enabled if IDE device supports this function.
7	Multi Word DMA Mode 2 Set	1: Multi Word DMA Mode 2 function is enabled even if IDE device does not support this function. 0: Multi Word DMA Mode 2 function is enabled if IDE device supports this function.
6	Multi Word DMA Mode 1 Set	1: Multi Word DMA Mode 1 function is enabled even if IDE device does not support this function. 0: Multi Word DMA Mode 1 function is enabled if IDE device supports this function.
5	Multi Word DMA Mode 0 Set	1: Multi Word DMA Mode 0 function is enabled even if IDE device does not support this function. 0: Multi Word DMA Mode 0 function is enabled if IDE device supports this function.
4	PIO Mode 4 Set	1: PIO Mode 4 function is enabled even if IDE device does not support this function. 0: PIO Mode 4 function is enabled if IDE device supports this function.
3	PIO Mode 3 Set	1: PIO Mode 3 function is enabled even if IDE device does not support this function. 0: PIO Mode 3 function is enabled if IDE device supports this function.
2	PIO Mode 2 Set	1: PIO Mode 2 function is enabled even if IDE device does not support this function. 0: PIO Mode 2 function is enabled if IDE device supports this function.
1	PIO Mode 1 Set	1: PIO Mode 1 function is enabled even if IDE device does not support this function. 0: PIO Mode 1 function is enabled if IDE device supports this function.
0	PIO Mode 0 Set	1: PIO Mode 0 function is enabled even if IDE device does not support this function. 0: PIO Mode 0 function is enabled if IDE device supports this function.

Remarks 1. TxModeSet and TxModeReset fields have higher priority than the information from IDE device. If there is any setting in TxModeSet field, related information from IDE device is ignored and related IDE transaction mode is enabled forcedly.

2. TxModeSet field is has higher priority than TxModeReset field.

3. The value on TxModeSet field is inconsistent with IDE device supported operational modes, proper operation of IDE bridge chip is not guaranteed. All register's bits should be set to "0" in normal use.

6.2 Setting for ExPinReset and ExPinSet Fields vs Different IDE Device Implementations

IDE Device Type	Operation Mode	ExPinReset	ExPinSet
ATA	Bus powered	0AH	35H
ATA	Self powered	0BH	34H
ATA	Combo self powered	09H	36H
ATAPI	Bus powered	2DH	12H
ATAPI	Self powered	13H	2CH
ATAPI	Combo self powered	31H	0EH

6.3 Serial ROM Information

The following table provides serial ROMs NEC Electronics evaluated.

(1) Equals or less than 2 Kbytes serial ROM (f_{SCL} = 100 kHz)

No.	Vendor	Product	Size
1	Atmel Corporation	AT24C01-10PI-2.7	128 bytes
2	Atmel Corporation	AT24C02-10PI-2.7	256 bytes
3	Atmel Corporation	AT24C04-10PI-2.7	512 bytes
4	Atmel Corporation	AT24C08-10PI-2.7	1 Kbytes
5	Atmel Corporation	AT24C16-10PI-2.7	2 Kbytes
6	STMicroelectronics	M24C01-WBN6	128 bytes
7	STMicroelectronics	M24C02-WBN6	256 bytes
8	STMicroelectronics	M24C04-WBN6	512 bytes
9	STMicroelectronics	M24C08-WBN6	1 Kbytes
10	STMicroelectronics	M24C16-WBN6	2 Kbytes

(2) Greater than 2 Kbytes serial ROM (f_{SCL} = 100 kHz)

No.	Vendor	Product	Size
1	Atmel Corporation	AT24C32-10PI-2.7	4 Kbytes
2	Atmel Corporation	AT24C64-10PI-2.7	8 Kbytes
3	STMicroelectronics	M24C32-WBN6	4 Kbytes
4	STMicroelectronics	M24C64-WBN6	8 Kbytes

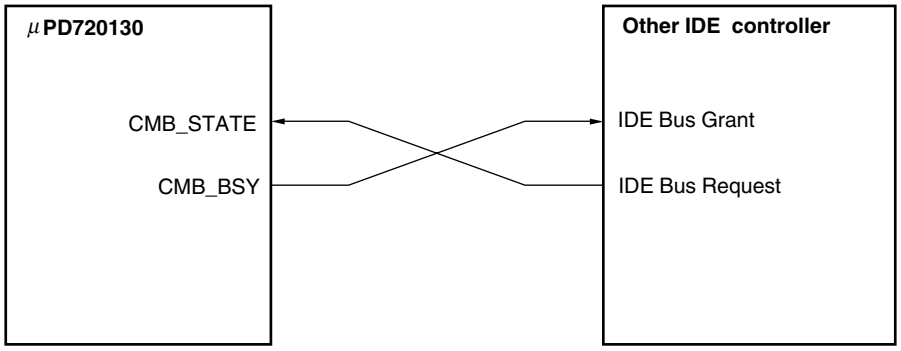
CHAPTER 7 COMBO MODE

This device can work in conjunction with another IDE controller in connecting to the same target IDE device in one system. To arbitrate IDE bus between two IDE controller chips, the device uses CMB_BSY and CMB_STATE. Combo mode is enabled when PWR = 0 and CLC = 1.

7.1 CMB_BSY and CMB_STATE Connection between Two IDE Controller Chips

CMB_BSY and CMB_STATE connect to other IDE controller chip as follows.

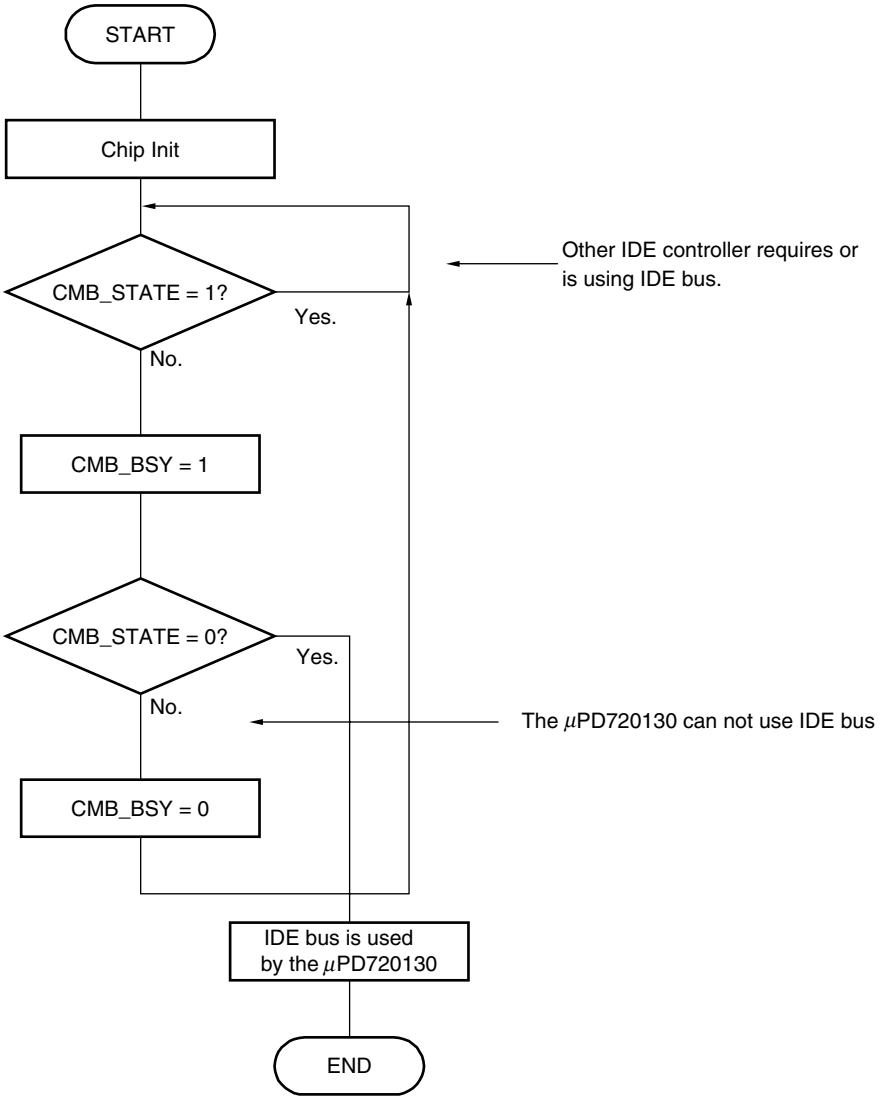
Figure 7-1. Connection for Combo Mode



7.2 IDE Bus Arbitration Sequence

The IDE bus arbitration is done in the following sequence. This device checks if other IDE controller request the ownership of the IDE bus. If other IDE controller request no ownership, this device will use IDE bus.

Figure 7-2. IDE Bus Arbitration

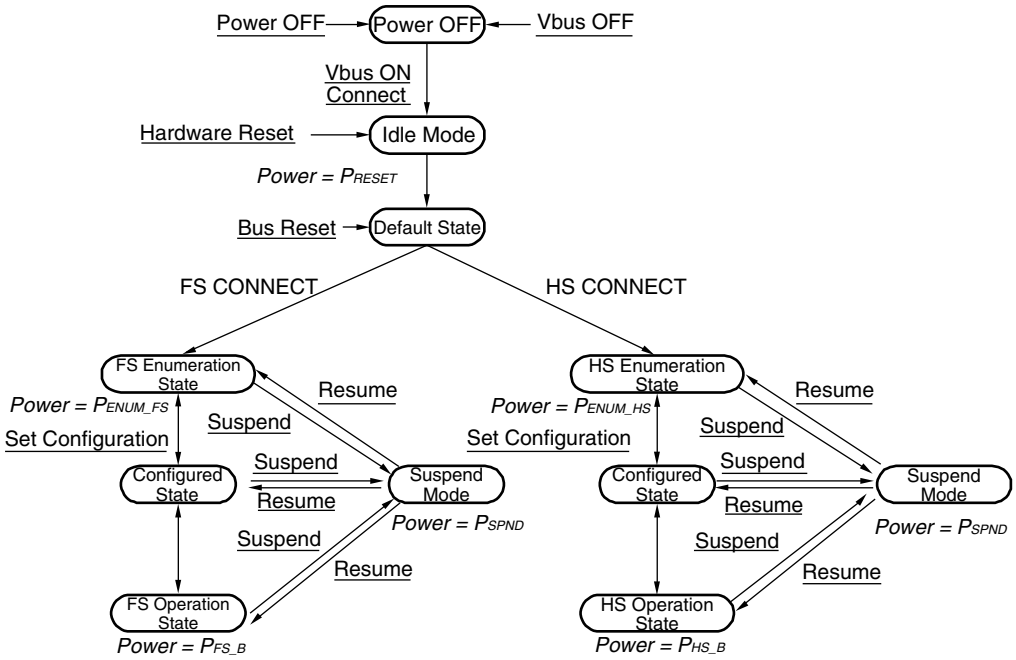


CHAPTER 8 POWER CONTROL INFORMATION

To implement bus-powered or high performance self-powered USB2.0 to IDE Bridge system, this device has two internal system clock modes. One is 7.5 MHz for bus-powered mode and the other is 60 MHz for self-powered mode. This device controls the power state according to events as follows. The underlined words represent events. The Italic words represent the power state.

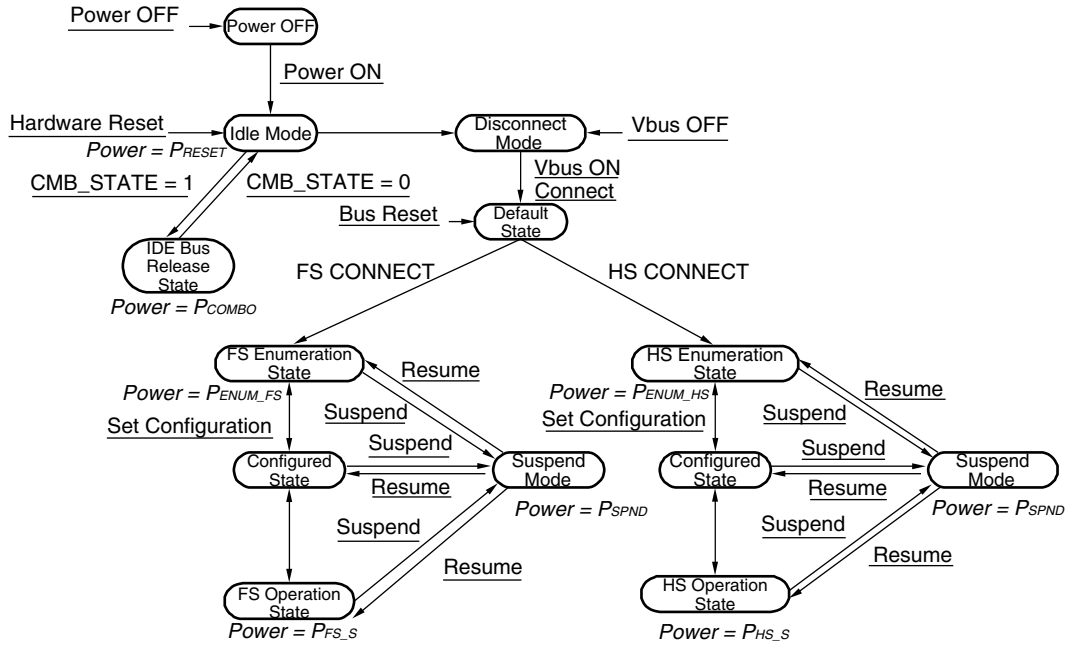
8.1 Bus-powered Mode

Figure 8-1. Bus-powered Mode



8.2 Self-powered Mode

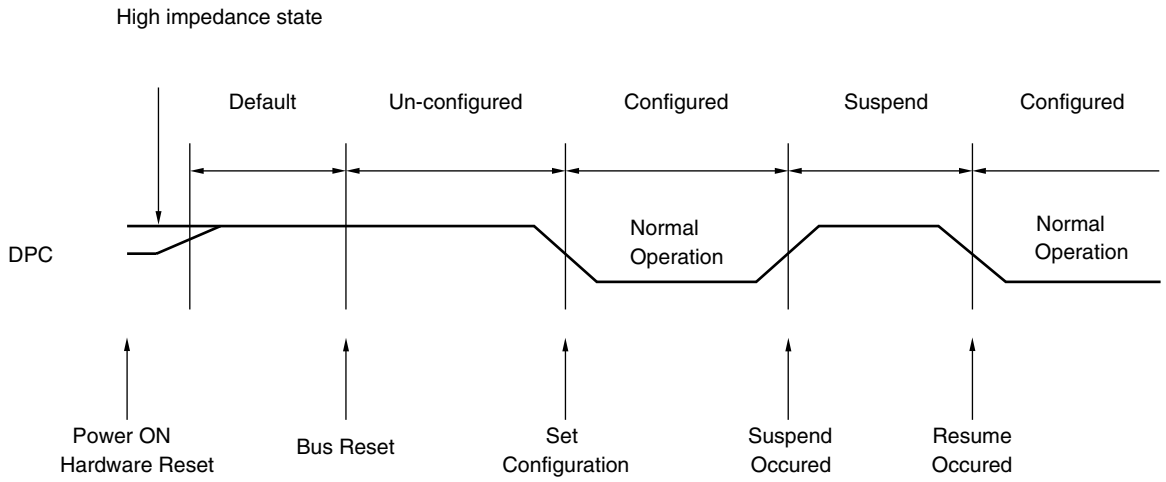
Figure 8-2. Self-powered Mode



8.3 DPC Pin to Control IDE Device's Power Circuit

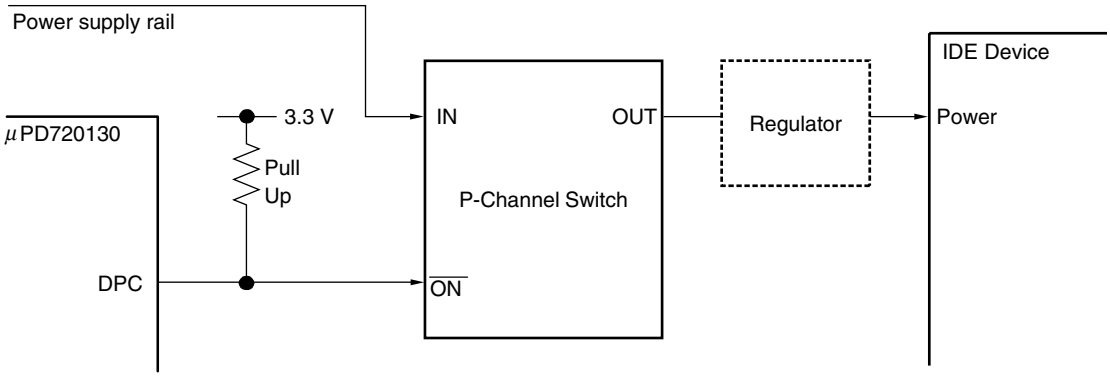
To implement bus-powered USB2.0 to IDE Bridge system, this device controls the power supplied to IDE device according to the power state. The device uses DPC pin to control IDE device's power circuit. DPC pin's output level relates to USB device states. DPC should be pull up to 3.3V because DPC output remained in high impedance state until the device is initialized

Figure 8-3. DPC Pin Signaling



Following reference circuit shuts off power supply to IDE device when the μPD720130 is in Default or un-configured state. Also, the power supply to IDE device is shut off during suspend state, too. Power consumption of total system under default, un-configured, and suspend state can be reduced by DPC pin.

Figure 8-4. Reference Power Circuit



CHAPTER 9 BOARD DESIGN GUIDELINE

USB 2.0 is a high-speed 480 Mbps path with a differential voltage swing of 400 mV. In order to design a board, conforming to USB Specification Revision 2.0, the following guidelines shall be observed.

In addition, refers to **High Speed USB Platform Design guidelines** released from USB I/F.

Note that the following guidelines are provided for better practices. Final condition of the board may vary due to other issues.

9.1 USB2.0 Signal Integrity Guidelines

(a) Limit the trace length of USB D+ and D- from USB2.0 chip to USB receptacles.

(b) Keep traces of USB bus D+ and D- in the same length. The difference between D+ and D- should be at least less than 0.5 mm.

(c) The distance between D+/D- to ground layer, trace width of D+/D-, and trace pitch between D+ and D-, dielectric material of the PCB shall be considered, in achieving 90 Ω differential characteristic impedance and 45 Ω common mode trace impedance for D+ and D-.

(d) Maintain parallelism between D+ and D- thru out the route from USB2.0 chip to receptacles.

(e) Prevents right-angle bended trace in minimizing trace length between USB2.0 chip to receptacles. If it becomes necessary to use two 45-degree turns or arc instead of a single 90-degree turn.

(f) Keep the signal as short as possible. Especially, keep the part of the signal highlighted by the solid line around Rs resister as shown in **Figure 9-1**.

(g) Do not route USB2.0 D+ and D- over the power/ground plane split.

(h) It is preferred to route USB2.0 D+ and D- on the same layer this device and USB connector resided. This avoids via on trace USB2.0 D+ and D- between USB2.0 chip to receptacles.

(i) Route USB2.0 D+ and D- using minimum vias and corners. This reduces signal reflections and impedance changes.

(j) Do not put copper pour close to USB2.0 D+ and D- signal since it may affect their impedance. But it is preferred to put copper pour along all edge of the board for FCC compliance.

(k) Maximize the distance between D+ and D- pair from other signals to avoid crosstalk.

(l) Make sure that the other signals do not cross the USB differential signal in the layer immediate above or below.

(m) The preferred layer stack is:

Signal layer 1
Ground
Power
Signal layer 2

USB2.0 D+/D- route on signal layer 1

Signal layer1
Power
Ground
Signal layer 2

USB2.0 D+/D- route on signal layer2

9.2 Analog V_{DD}

(a) Prepare Analog V_{DD} that is only used for analog circuit of USB2.0 devices. Separate analog V_{DD} from digital V_{DD}.
(b) AV_{DD25} pin of this device must be connected with analog V_{DD}.
(c) Reduce the noise on analog V_{DD} coming from digital signals or digital V_{DD}.
(d) Connect digital V_{DD} and analog V_{DD} via the inductor, ferrite bead, or the resistor as shown in **Figure 9-3**. The Bead is preferred. If inductors are used in filtering the analog power and ground of USB2.0 chip, they should be placed away from one other to avoid the resonance. If resistor is used to connect between digital V_{DD} and analog V_{DD}, less than 3 Ω resistor shall be used to prevent a large voltage drop between digital V_{DD} and analog V_{DD}.

9.3 Analog V_{SS}

(a) Preparing Analog V_{SS} filtered from digital V_{SS} that is only used for analog circuit of USB2.0 devices.
(b) 1% precision RREF resistor shall be used between AV_{SS} pin and RREF.
(c) Reduce the noise on analog V_{SS} coming from digital signals or digital V_{SS}.
(d) In case analog V_{SS} and digital V_{SS} are not separated, it is desirable to more RREF resister connecting AV_{SS} pin away from noise from digital V_{SS}.
(e) RREF resister is used to control current source, which is connected with AV_{SS}(R), as shown in **Figure 9-2**. The solid trace in **Figure 9-2** must be placed closed to USB2.0 chip in avoiding any noise.
(f) Connect digital V_{SS} and analog V_{SS} via the inductor, ferrite bead or the resistor as shown in **Figure 9-3**. If inductors are used in filtering to analog power and ground of USB2.0 chip, they should be placed away from one other to avoid the resonance. If resistor is used to connect between digital V_{SS} and analog V_{SS}, less than 3 Ω resistor shall be used to prevent a large voltage drop between digital V_{SS} and analog V_{SS}.

Remark The internal PLL may be unlocked by the noise on AV_{SS} / AV_{DD25} pins and renders the chip failing. And transaction errors on USB bus occurs.

9.4 Decoupling Capacitor

Decoupling capacitor can be used to smooth voltage fluctuation due to changes in current consumption, and as a filter that prevents noise from digital signals to the power supply and V_{SS} field. Choose the proper number and type of capacitors in considering the total board design.

(a) Mount enough decoupling capacitors between digital V_{DD} and V_{SS}. These should be located nearby USB2.0 devices. It may be effective to mount these capacitors on opposite side.
(b) Use surface-mount package with wide and squat mounting pads with vias jammed up next to the pads without traces. Vias should have big plate through holes.
(c) Mount at least one 10 μF capacitor and several pieces of 0.1 μF and 0.01 μF capacitor between analog V_{DD} and analog V_{SS}. These should be located closed to USB2.0 devices.
(d) Do not use electrolytic capacitors as decoupling capacitors, but use tantalum capacitors or ceramic capacitors, which have good performance under high frequency.

9.5 EMI Filter

EMI filter such as common mode choke may degrade USB signaling waveform. Design properly when it is used. Consult with EMI filter for USB 2.0 tested components.

9.6 ESD Protection

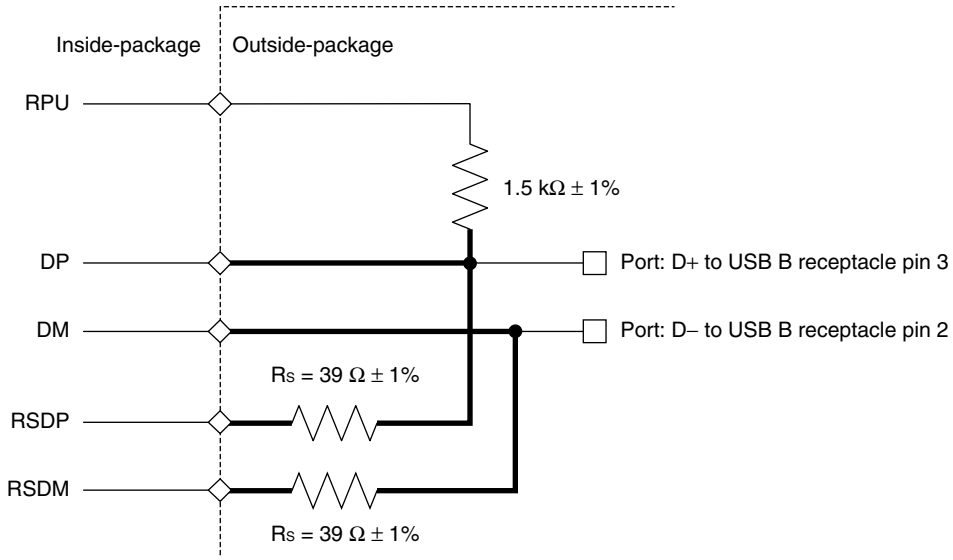
ESD suppressor may degrade USB signaling waveform. Design properly when it is used.

9.7 USB Cable and Receptacle

Use USB2.0 certified components such as USB receptacles on the PCB, and USB cables. No certification will be given if no certified component is used.

9.8 USB Circuit

Figure 9-1. USB Data Signaling



$R_S + R_{on}$ (Resistance for driver which is active) = 45 Ω ± 10%

Figure 9-2. USB Reference Resistor

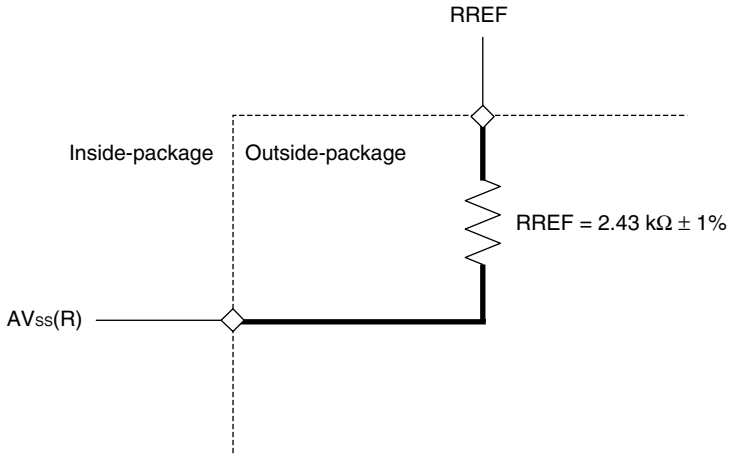
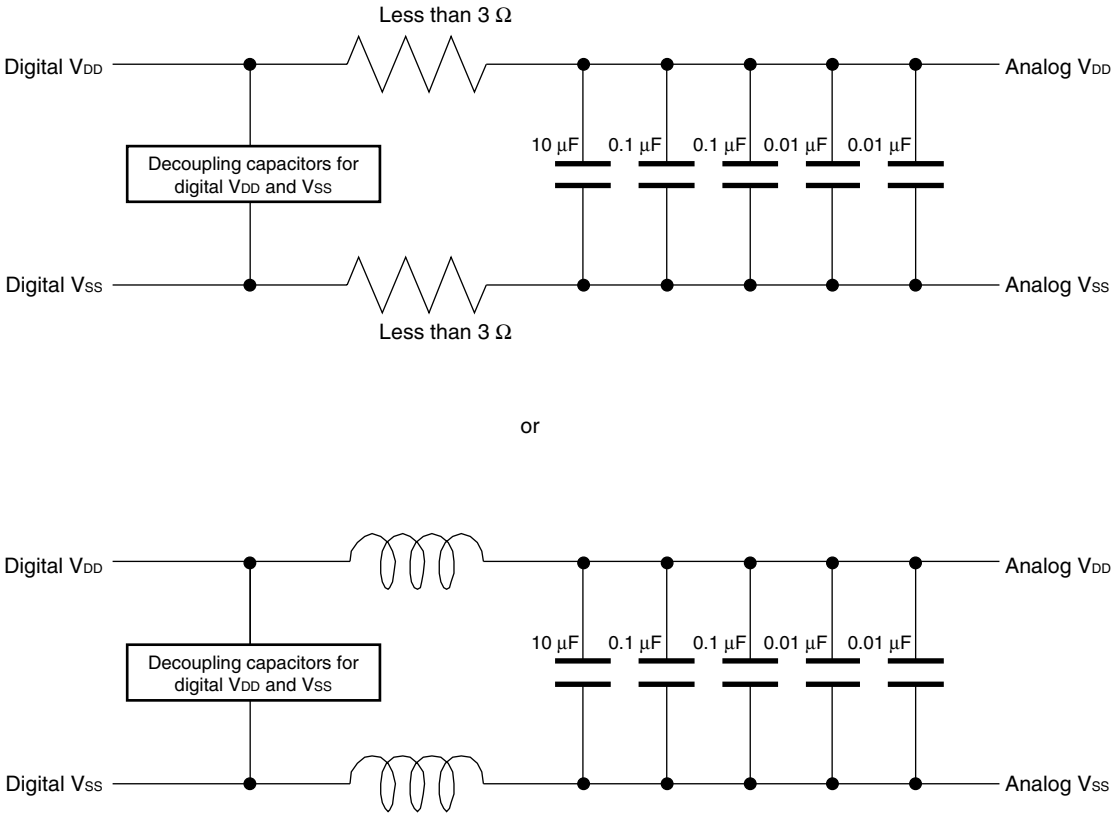


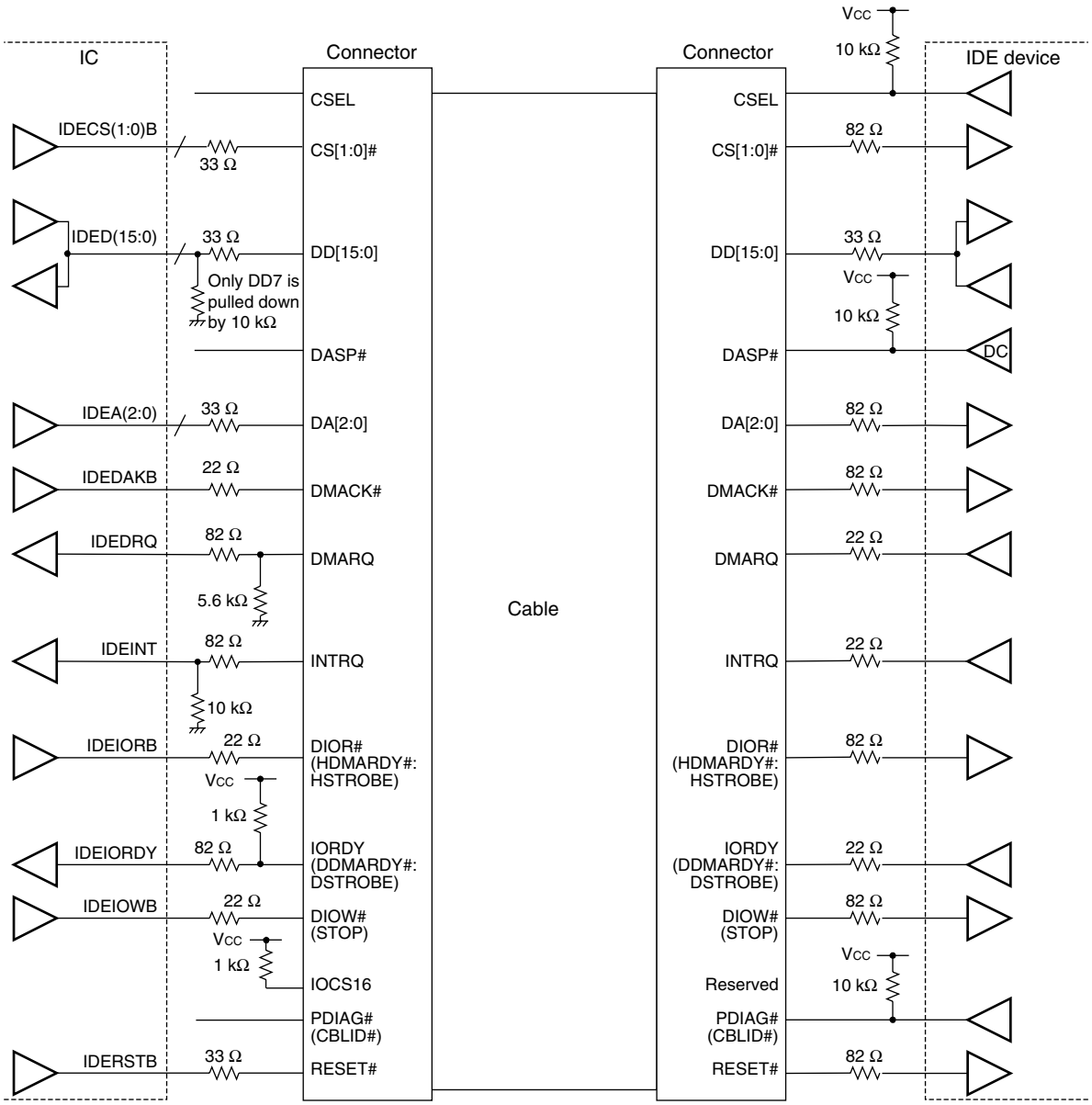
Figure 9-3. Decoupling Capacitor



Remark The value for inductor should be defined to prevent the resonance problem between board capacitance and inductance.

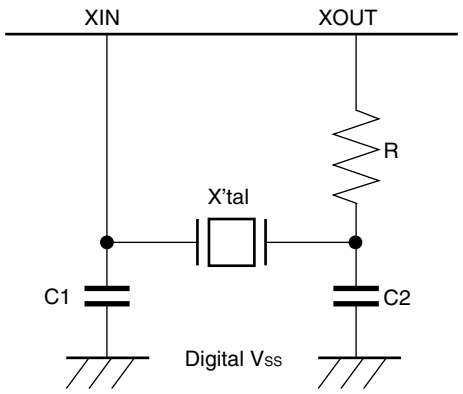
9.9 IDE Circuit

Figure 9-4. IDE Connection



9.10 Oscillator

Figure 9-5. Oscillator Circuit



NEC Electronics use AT-49 30 MHz on ET-0148 board. Following table shows the external parameters for AT-49 30 MHz.

Vendor	Name	R	C1	C2
KDS	AT-049 (30.000 MHz : ZB1090)	47 Ω	12 pF	12 pF

If AT-49 30 MHz is used on the board, contact to Daishinku Corp. (KDS) for getting the best external parameters depended on the board configuration.

KDS's home page: http://www.kdsj.co.jp

AT-49 catalogue No. : 1AI300002CA

NEC Electronics has evaluated NDK's X'tal. Following table shows the external parameters for each X'tal.

Vendor	Name	R	C1	C2
NDK	AT-41, AT-41CD2, NX3225DA, NX5032GA, NX8045GB (30.000 MHz)	47 Ω	10 pF	10 pF

If NDK's X'tal is used on the board, contact to NIHON DEMPA KOGYO CO.,LTD. (NDK) for getting the best external parameters depended on the board configuration.

NDK's home page : http://www.ndk.com

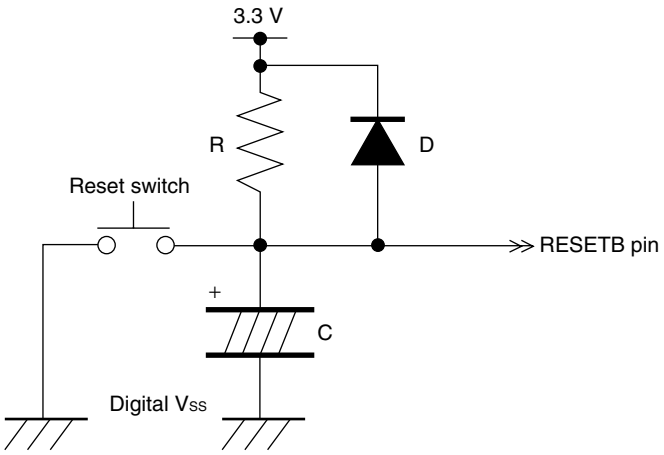
X'tal catalogue No. : 02092X

Caution When an oscillator circuit is used, observe the following guidelines.

- **Keep the signal length as short as possible.**
- **Do not cross the signal with the other signal lines.**
- **Do not route the signal near a signal line with high current flows.**
- **Always keep the V_{SS} point of the oscillator capacitor to the same potential as V_{SS} of the USB chip**
- **Do not ground the capacitor to a V_{SS} pattern in which a high current flows.**

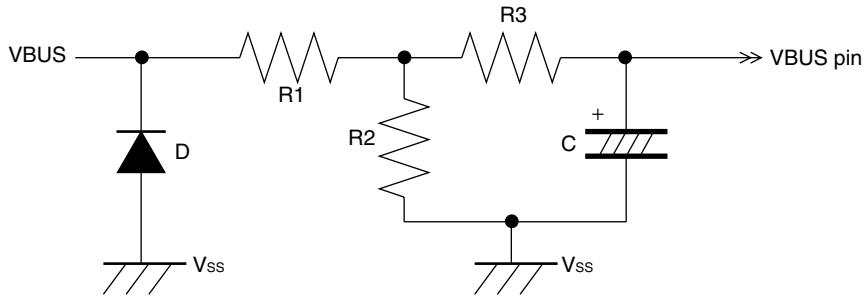
9.11 Reset Circuit

Figure 9-6. Reset Reference Circuit



9.12 VBUS Monitoring Circuit

Figure 9-7. VBUS Monitoring Circuit



Remarks 1. VBUS pin may be used to monitor for VBUS line even if V_{DD33}, V_{DD25}, and AV_{DD25} are shut off. System must ensure that the input voltage level for VBUS pin is less than 3.0 V in not exceeding the absolute maximum rating.

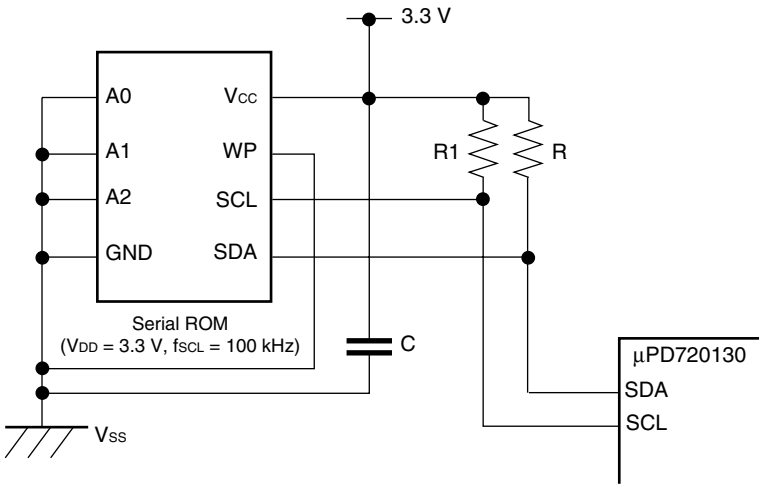
2. The unit of R1, R2, and R3 is kΩ order.

3. This circuit is not applicable for bus powered system.

9.13 Serial ROM Connection

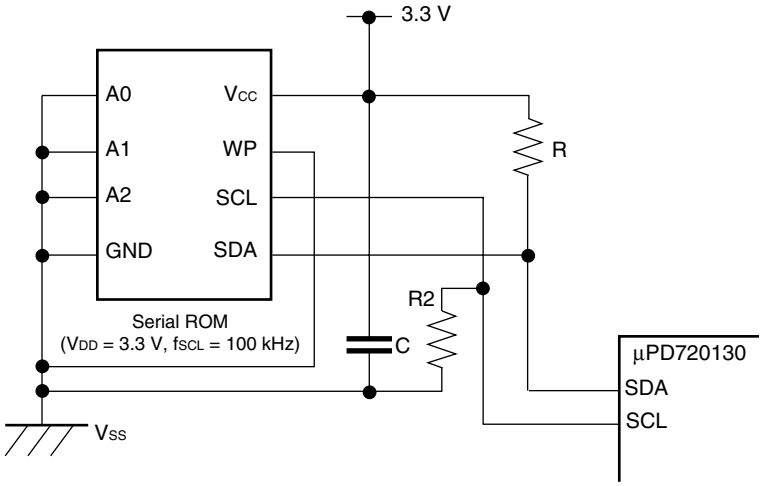
Figure 9-8. Serial ROM Connection

(a) Serial ROM Size ≤ 2 Kbytes



Remark If serial ROM size ≤ 2 Kbytes, SCL should be pulled up.

(b) Serial ROM Size > 2 Kbytes



Remark If serial ROM size > 2 Kbytes, SCL should be pulled down.

CHAPTER 10 ELECTRICAL SPECIFICATIONS

10.1 Buffer List

- 2.5 V Oscillator interface
  XIN, XOUT
- 3.3 V input buffer
  MD(1:0), TEST(3:0), SMC
- 3.3 V schmitt input buffer
  RESETB, IRQ0
- 3.3 V Input buffer with enable (OR type)
  DCC, DV(1:0), SPD, CLC, PWR, CMB_STATE
- 3.3 V I_{OL} = 6 mA 3-state Output buffer
  CMB_BSY, DPC
- 3.3 V I_{OL} = 3 mA bi-directional schmitt buffer with input enable (OR-type)
  GPIO(7:0), PIO5, SDA, SCL
- 3.3 V I_{OL} = 6 mA bi-directional buffer with input enable (OR-type)
  PIO(15:14)
- 5 V schmitt input buffer
  VBUS
- 5 V I_{OL} = 6 mA 3-state Output buffer
  IDECS(1:0)B, IDEA(2:0), IDEDAKB, IDEIORB, IDEIOWB, IDERSTB
- 5 V I_{OL} = 6 mA bi-directional buffer with input enable (OR-type)
  IDED(15:0), IDEINT, IDEIORDY, IDEDRQ
- USB interface
  DP, DM, RSDP, RSDM, RREF, RPU

Remark Above, “5 V” refers to a 3.3-V buffer with 5-V tolerant circuit. Therefore, it is possible to have a 5-V connection for an external bus, but the output level will be only up to 3.3 V, which is the V_{DD33} voltage.

10.2 Terms Used in Absolute Maximum Ratings

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD25}	Indicates voltage range within which damage or reduced reliability will not result when power is applied to a V_{DD} pin.
Input voltage	V_I	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an input pin.
Output voltage	V_O	Indicates voltage range within which damage or reduced reliability will not result when power is applied to an output pin.
Output current	I_O	Indicates absolute tolerance value for DC current to prevent damage or reduced reliability when a current flows out of or into an output pin.
Operating ambient temperature	T_A	Indicates the ambient temperature range for normal logic operations.
Storage temperature	T_{stg}	Indicates the element temperature range within which damage or reduced reliability will not result while no voltage or current are applied to the device.

10.3 Terms Used in Recommended Operating Conditions

Parameter	Symbol	Meaning
Power supply voltage	V_{DD33}, V_{DD25}	Indicates the voltage range for normal logic operations occur when V_{SS} = 0 V.
High-level input voltage	V_{IH}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the high level states for normal operation of the input buffer. * If a voltage that is equal to or greater than the “MIN.” value is applied, the input voltage is guaranteed as high level voltage.
Low-level input voltage	V_{IL}	Indicates the voltage, which is applied to the input pins of the device, is the voltage indicates that the low level states for normal operation of the input buffer. * If a voltage that is equal to or lesser than the “MAX.” value is applied, the input voltage is guaranteed as low level voltage.
Hysteresis voltage	V_H	Indicates the differential between the positive trigger voltage and the negative trigger voltage.
Input rise time	t_{ri}	Indicates allowable input rise time to input pins. Input rise time is transition time from $0.1 \times V_{DD}$ to $0.9 \times V_{DD}$.
Input fall time	t_{fi}	Indicates allowable input fall time to input pins. Input fall time is transition time from $0.9 \times V_{DD}$ to $0.1 \times V_{DD}$.

10.4 Terms Used in DC Characteristics

Parameter	Symbol	Meaning
Off-state output leakage current	I_{OZ}	Indicates the current that flows from the power supply pins when the rated power supply voltage is applied when a 3-state output has high impedance.
Output short circuit current	I_{OS}	Indicates the current that flows when the output pin is shorted (to GND pins) when output is at high-level.
Input leakage current	I_I	Indicates the current that flows when the input voltage is supplied to the input pin.
Low-level output current	I_{OL}	Indicates the current that flows to the output pins when the rated low-level output voltage is being applied.
High-level output current	I_{OH}	Indicates the current that flows from the output pins when the rated high-level output voltage is being applied.

10.5 Absolute Maximum Ratings

Parameter	Symbol	Condition	Rating	Unit
Power supply voltage	V_{DD33}	3.3 V power supply rail	–0.5 to +4.6	V
	V_{DD25}	2.5 V power supply rail	–0.5 to +3.6	V
Input voltage, 5 V buffer	V_I	3.0 V ≤ V_{DD33} ≤ 3.6 V V_I < V_{DD33} + 3.0 V	–0.5 to +6.6	V
Input voltage, 3.3 V buffer	V_I	3.0 V ≤ V_{DD33} ≤ 3.6 V V_I < V_{DD33} + 1.0 V	–0.5 to +4.6	V
Input voltage, 2.5 V buffer	V_I	2.3 V ≤ V_{DD25} ≤ 2.7 V V_I < V_{DD25} + 0.9 V	–0.5 to +3.6	V
Output voltage, 5 V buffer	V_O	3.0 V ≤ V_{DD33} ≤ 3.6 V V_O < V_{DD33} + 3.0 V	–0.5 to +6.6	V
Output voltage, 3.3 V buffer	V_O	3.0 V ≤ V_{DD33} ≤ 3.6 V V_O < V_{DD33} + 1.0 V	–0.5 to +4.6	V
Output voltage, 2.5 V buffer	V_O	2.3 V ≤ V_{DD25} ≤ 2.7 V V_O < V_{DD25} + 0.9 V	–0.5 to +3.6	V
Output current, 5 V buffer	I_O	I_{OL} = 6 mA	20	mA
Output current, 3.3 V buffer	I_O	I_{OL} = 6 mA	20	mA
		I_{OL} = 3 mA	10	mA
Operating ambient temperature	T_A		0 to +70	°C
Storage temperature	T_{stg}		–65 to +150	°C

Caution Product quality may degrade if the absolute maximum rating is exceeded even momentarily for any parameters. That is, the absolute maximum ratings are rated values at which the product is on the verge of suffering physical damage, and therefore the product must be used under conditions that ensure that the absolute maximum ratings are not exceeded.

The ratings and conditions indicated for DC characteristics and AC characteristics represent the quality assurance range during normal operation.

10.6 Two Power Supply Rails Limitation

This device has two power supply rails (2.5 V, 3.3 V). This device requires that V_{DD25} should be stabled before V_{DD33} is stabled. The system must ensure that the absolute maximum ratings for V_I/V_O are not exceeded. System reset signaling should be asserted with the specified time after both V_{DD25} and V_{DD33} are stabled.

10.7 Recommended Operating Range

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Operating voltage	V_{DD33}	3.3 V for V_{DD33} pins	3.0	3.3	3.6	V
	V_{DD25}	2.5 V for V_{DD25} pins	2.3	2.5	2.7	V
	V_{DD25}	2.5 V for AV_{DD25} pins	2.3	2.5	2.7	V
High-level input voltage	V_{IH}					
5.0 V high-level input voltage			2.0		5.5	V
3.3 V high-level input voltage			2.0		V_{DD33}	V
2.5 V high-level input voltage			1.7		V_{DD25}	V
Low-level input voltage	V_{IL}					
5.0 V low-level input voltage			0		0.8	V
3.3 V low-level input voltage			0		0.8	V
2.5 V low-level input voltage			0		0.7	V
Hysteresis voltage	V_H					
5 V hysteresis voltage			0.3		1.5	V
3.3 V hysteresis voltage			0.2		1.0	V
Input rise time	t_{ri}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms
Input fall time	t_{fi}					
Normal buffer			0		200	ns
Schmitt buffer			0		10	ms

10.8 DC Characteristics (V_{DD33} = 3.0 to 3.6 V, V_{DD25} = 2.3 to 2.7 V, T_A = 0 to +70°C)

10.8.1 DC characteristics of control pin block

Parameter	Symbol	Condition	Min.	Max.	Unit
Off-state output current	I_{OZ}	V_O = V_{DD33}, V_{DD25} or V_{SS}		±10	μA
Output short circuit current	I_{OS} Note			–250	mA
Low-level output current	I_{OL}				
5.0 V low-level output current		V_{OL} = 0.4 V	6.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	6.0		mA
3.3 V low-level output current		V_{OL} = 0.4 V	3.0		mA
High-level output current	I_{OH}				
5.0 V high-level output current		V_{OH} = 2.4 V	–2.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	–6.0		mA
3.3 V high-level output current		V_{OH} = 2.4 V	–3.0		mA
Input leakage current	I_I				
3.3 V buffer		V_I = V_{DD} or V_{SS}		±10	μA
5.0 V buffer		V_I = V_{DD} or V_{SS}		±10	μA

Note The output short circuit time is one second or less and is only for one pin on the LSI.

10.8.2 DC characteristics of USB interface

(1/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Serial Resistor between DP (DM) and RSDP (RSDM)	R_S		38.61	39.39	Ω
Output pin impedance	Z_{HSDRV}	Includes R_S resistor	40.5	49.5	Ω
Bus pull-up resistor on upstream facing port	R_{PU}	1.5 kΩ ±5% consists of resistance of transistor and pull-up resistor	1.485	1.515	Ω
Termination voltage for upstream facing port pull-up	V_{TERM}		3.0	3.6	V
Input Levels for full-speed:					
High-level input voltage (drive)	V_{IH}		2.0		V
High-level input voltage (floating)	V_{IHZ}		2.7	3.6	
Low-level input voltage	V_{IL}			0.8	V
Differential input sensitivity	V_{DI}	|(D+) – (D–)|	0.2		V
Differential common mode range	V_{CM}	Includes V_{DI} range	0.8	2.5	V
Output Levels for Full-speed:					
High-level output voltage	V_{OH}	R_L of 14.25 kΩ to V_{SS}	2.8	3.6	V
Low-level output voltage	V_{OL}	R_L of 1.425 kΩ to 3.6 V	0.0	0.3	V
SE1	V_{OSE1}		0.8		V
Output signal crossover point voltage	V_{CRS}		1.3	2.0	V

(2/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Input Levels for High-speed:					
High-speed squelch detection threshold (differential signal)	V_{HSSQ}		100	150	mV
High-speed disconnect detection threshold (differential signal)	V_{HSDSC}		525	625	mV
High-speed data signaling common mode voltage range	V_{HSCM}		–50	+500	mV
High-speed differential input signaling level	See **Figure 10-4**.				
Output Levels for High-speed:					
High-speed idle state	V_{HSOI}		–10.0	+10.0	mV
High-speed data signaling high	V_{HSOH}		360	440	mV
High-speed data signaling low	V_{HSOL}		–10.0	+10.0	mV
Chirp J level (different signal)	V_{CHIRPJ}		700	1100	mV
Chirp K level (different signal)	V_{CHIRPK}		–900	–500	mV

Figure 10-1. Differential Input Sensitivity Range for Full-speed

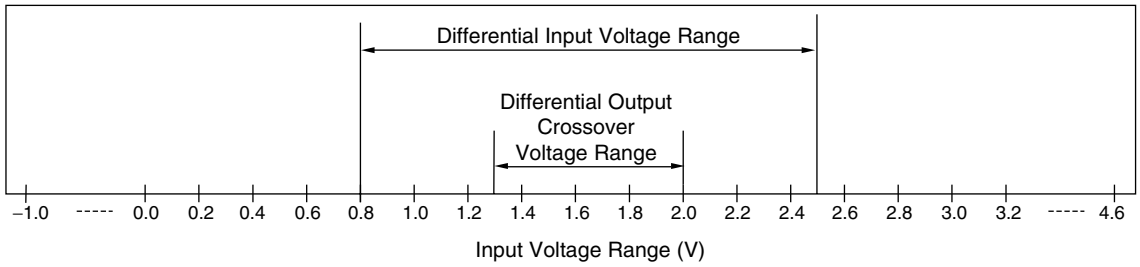


Figure 10-2. Full-speed Buffer V_{OH}/I_{OH} Characteristics for High-speed Capable Transceiver

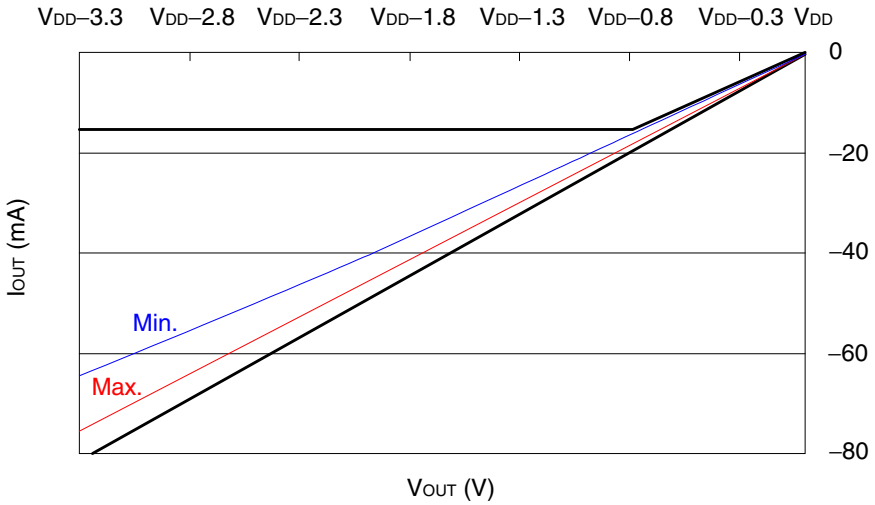


Figure 10-3. Full-speed Buffer V_{OL}/I_{OL} Characteristics for High-speed Capable Transceiver

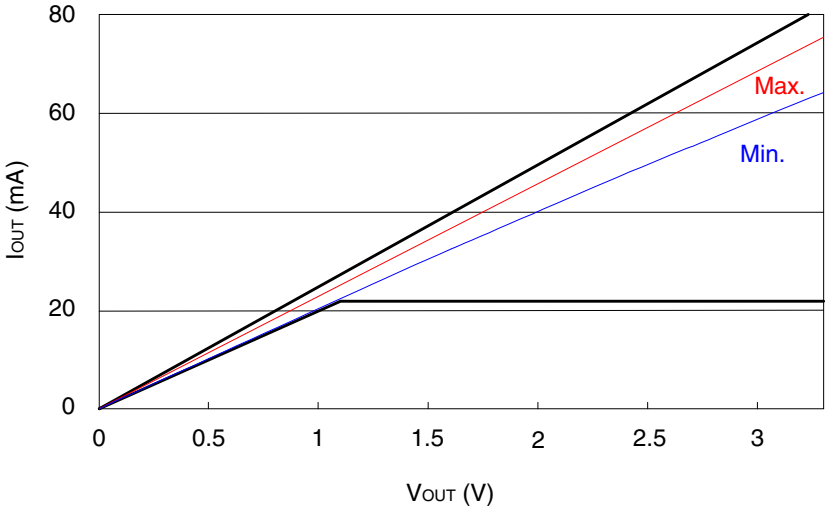


Figure 10-4. Receiver Sensitivity for Transceiver at DP/DM

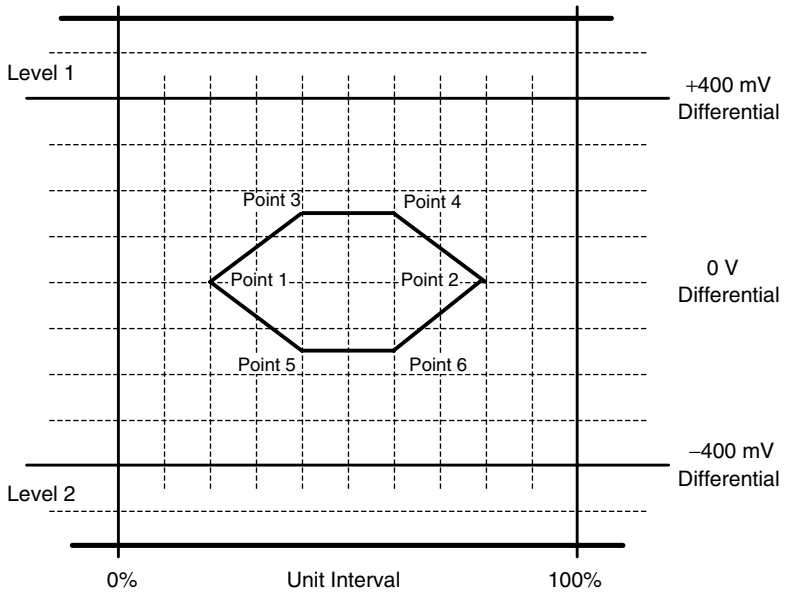
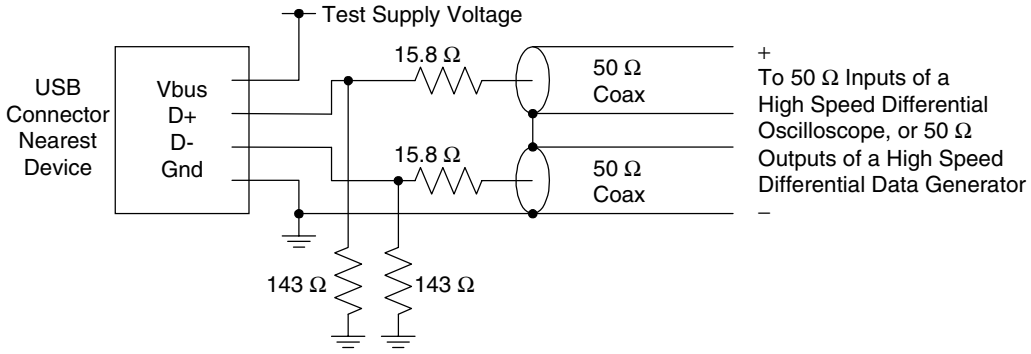


Figure 10-5. Receiver Measurement Fixtures



10.9 Pin Capacitance

Parameter	Symbol	Condition	Min.	Max.	Unit
Input capacitance	C_{IN}	V_{DD} = 0 V, T_A = 25°C	4	6	pF
Output capacitance	C_{OUT}	f_C = 1 MHz	4	6	pF
I/O capacitance	C_{IO}	Unmeasured pins returned to 0 V	4	6	pF

10.10 Power Consumption

(1) The power consumption when device works as bus-powered mode

Symbol	Condition	Max.			Unit
		V_{DD25}	V_{DD33}	AV_{DD25}	
$P_{ENUM-BUS}$	The Power consumption under UnConfigured stage.				
	High-speed operating	57	3	10	mA
	Full-speed operating	23	4	10	mA
P_{W-BUS}	The power consumption when device works.				
	High-speed operating	110	22	10	mA
	Full-speed operating	113	13	10	mA
$P_{W\_SPD-BUS}$	The power consumption Under suspend state	10	235	5	μA

(2) The power consumption when device works as self-powered mode

Symbol	Condition	Max.			Unit
		V_{DD25}	V_{DD33}	AV_{DD25}	
$P_{ENUM-SELF}$	The Power consumption under UnConfigured stage.				
	High-speed operating	85	5	10	mA
	Full-speed operating	60	5	10	mA
P_{W-SELF}	The power consumption when device works.				
	High-speed operating	120	25	10	mA
	Full-speed operating	113	13	10	mA
$P_{W\_SPD-SELF}$	The power consumption Under suspend state	50	5	5	mA
P_{W_UNP}	The power consumption under unplug state	87	3	10	mA
P_{W_COM}	The power consumption under combo mode. The device is releasing the IDE bus.	90	5	10	mA

10.11 AC Characteristics (V_{DD33} = 3.0 to 3.6 V, V_{DD25} = 2.3 to 2.7 V, T_A = 0 to +70°C)

10.11.1 System clock ratings

Parameter	Symbol	Condition	Min.	Typ.	Max.	Unit
Clock frequency	f_{CLK}	X'tal	–500 ppm	30	+500 ppm	MHz
		Oscillator block	–500 ppm	30	+500 ppm	MHz
Clock duty cycle	t_{DUTY}		45	50	55	%

Remarks 1. Recommended accuracy of clock frequency is ± 100 ppm.

2. Required accuracy of X'tal or Oscillator block is including initial frequency accuracy, the spread of X'tal capacitor loading, supply voltage, temperature, and aging, etc.

10.11.2 System reset signaling

Parameter	Symbol	Conditions	Min.	Max.	Unit
Reset active time	t_{rst}		2		μs

10.11.3 USB interface block

(1/2)

Parameter	Symbol	Conditions	Min.	Max.	Unit
Full-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{FR}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Fall time (90% - 10%)	t_{FF}	C_L = 50 pF, R_S = 36 Ω	4	20	ns
Differential rise and fall time matching	t_{FRFM}	(t_{FR}/t_{FF})	90	111.11	%
Full-speed data rate for device which are high-speed capable	$t_{FDRATHS}$	Average bit rate	11.9940	12.0060	Mbps
Frame interval	t_{FRAME}		0.9995	1.0005	ms
Consecutive frame interval jitter	t_{RFI}	No clock adjustment		42	ns
Source jitter total (including frequency tolerance):					
To next transition	t_{DJ1}		–3.5	+3.5	ns
For paired transitions	t_{DJ2}		–4.0	+4.0	ns
Source jitter for differential transition to SE0 transition	t_{FDEOP}		–2	+5	ns
Receiver Jitter:					
To next transition	t_{JR1}		–18.5	+18.5	ns
For paired transitions	t_{JR2}		–9	+9	ns
Source SE0 interval of EOP	t_{FEOPT}		160	175	ns
Receiver SE0 interval of EOP	t_{FEOPR}		82		ns
Width of SE0 interval during differential transition	t_{FST}			14	ns

(2/2)

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
High-speed Source Electrical Characteristics					
Rise time (10% - 90%)	t_{HSR}		500		ps
Fall time (90% - 10%)	t_{HSF}		500		ps
Driver waveform	See **Figure 10-6**.				
High-speed data rate	t_{HSDRAT}		479.760	480.240	Mbps
Microframe interval	t_{HSFRAM}		124.9375	125.0625	μs
Consecutive microframe interval difference	t_{HSRFI}			4 high-speed	Bit times
Data source jitter	See **Figure 10-6**.				
Receiver jitter tolerance	See **Figure 10-4**.				
Device Event Timings					
Time from internal power good to device pulling D+ beyond V_{IHZ} (min.) (signaling attached)	t_{SIGATT}			100	ms
Debounce interval provided by USB system software after attach	t_{ATTDB}			100	ms
Inter-packet delay for full-speed	t_{IPD}		2		Bit times
Inter-packet delay for device response w/detachable cable for full-speed	$t_{RSPIPD1}$			6.5	Bit times
High-speed detection start time from suspend	t_{SCA}		2.5		μs
Sample time for suspend vs reset	t_{CSR}		100	875	μs
Time to detect bus suspend state	t_{SPD}		3.000	3.125	ms
Power down under suspend	t_{SUS}			10	ms
Reversion time from suspend to high-speed	t_{RHS}			1.333	μs
Drive Chirp K width	t_{CKO}		1		ms
Finish Chirp K assertion	t_{FCA}			7	ms
Start sequencing Chirp K-J-K-J-K-J	t_{SSC}			100	μs
Finish sequencing Chirp K-J	t_{FSC}		-500	-100	μs
Detect sequencing Chirp K-J width	t_{CSI}		2.5		μs
Sample time for sequencing Chirp	t_{SCS}		1	2.5	ms
Reversion time to high-speed	t_{RHA}			500	μs
High-speed detection start time	t_{HDS}		2.5	3000	μs
Reset completed time	t_{DRS}		10		ms

10.11.4 IDE interface block

(1) PIO mode

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Mode 3	Mode 4	Unit
Cycle time (min.)	t_0	600	383	240	180	120	ns
Address setup time (min.)	t_1	70	50	30	30	25	ns
16 bits DIOR/DIOW pulse width (min.)	t_2	165	125	100	80	70	ns
8 bits DIOR/DIOW pulse width (min.)		290	290	290	80	70	ns
DIOR/DIOW recovery time (min.)	t_{2i}	–	–	–	70	25	ns
DIOW data setup time (min.)	t_3	60	45	30	30	20	ns
DIOW data hold time (min.)	t_4	30	20	15	10	10	ns
DIOR data setup time (min.)	t_5	50	35	20	20	20	ns
DIOR data hold time (min.)	t_6	5	5	5	5	5	ns
DIOR 3-state delay time (max.)	t_{6Z}	30	30	30	30	30	ns
Address hold time (min.)	t_9	20	15	10	10	10	ns
IORDY read data valid time (min.) Note	t_{RD}	0	0	0	0	0	ns
IORDY setup time (min.) Note	t_A	35	35	35	35	35	ns
IORDY pulse width (max.) Note	t_B	1250	1250	1250	1250	1250	ns
IORDY Inactive to Hi-Z time (max.) Note	t_C	5	5	5	5	5	ns

Note IORDY is an option in modes 0 to 2. IORDY is essential in modes 3 and 4.

(2) Multi word DMA mode

Parameter	Symbol	Mode 0	Mode 1	Mode 2	Unit
Cycle time (min.)	t_0	480	150	120	ns
DIOR/DIOW pulse width (min.)	t_D	215	80	70	ns
DIOR data access time (max.)	t_E	150	60	50	ns
DIOR data hold time (min.)	t_F	5	5	5	ns
DIOR data setup time (min.)	t_{Gr}	100	30	20	ns
DIOW data setup time (min.)	t_{Gw}	100	30	20	ns
DIOW data hold time (min.)	t_H	20	15	10	ns
DMACK setup time (min.)	t_I	0	0	0	ns
DMACK hold time (min.)	t_J	20	5	5	ns
DIOR negate pulse width (min.)	t_{Kr}	50	50	25	ns
DIOW negate pulse width (min.)	t_{Kw}	215	50	25	ns
DIOR-DMARQ delay time (max.)	t_{Lr}	120	40	35	ns
DIOW-DMARQ delay time (max.)	t_{Lw}	40	40	35	ns
DMACK 3-state delay time (max.)	t_Z	20	25	25	ns
CS setup time (min.)	t_M	50	30	25	ns
CS hold time (min.)	t_N	15	10	10	ns

(3) Ultra DMA mode

Parameter	Symbol	Mode 0		Mode 1		Mode 2		Mode 3		Mode 4		Unit
		Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	Min.	Max.	
Average cycle time for 2 cycles	t_{2CYC}	240	-	160	-	120	-	90	-	60	-	ns
Minimum cycle time for 2 cycles	t_{2CYC}	235	-	156	-	117	-	86	-	57	-	ns
Cycle time for 1 cycle	t_{CYC}	114	-	75	-	55	-	39	-	25	-	ns
Data setup time on receive side	t_{DS}	15	-	10	-	7	-	7	-	5	-	ns
Data hold time on receive side	t_{DH}	5	-	5	-	5	-	5	-	5	-	ns
Data setup time on transmit side	t_{DVS}	70	-	48	-	34	-	20	-	6	-	ns
Data hold time on transmit side	t_{DVH}	6	-	6	-	6	-	6	-	6	-	ns
First STROBE time	t_{FS}	0	230	0	200	0	170	0	130	0	120	ns
Interlock time with limitation	t_{LI}	0	150	0	150	0	150	0	100	0	100	ns
Minimum interlock time	t_{MLI}	20	-	20	-	20	-	20	-	20	-	ns
Interlock time without limitation	t_{UI}	0	-	0	-	0	-	0	-	0	-	ns
Output release time	t_{AZ}	-	10	-	10	-	10	-	10	-	10	ns
Output delay time	t_{ZAH}	20	-	20	-	20	-	20	-	20	-	ns
Output stabilization time (from release)	t_{ZAD}	0	-	0	-	0	-	0	-	0	-	ns
Envelope time	t_{ENV}	20	70	20	70	20	70	20	55	20	55	ns
STROBE DMARDY delay time	t_{SR}	-	50	-	30	-	20	-	NA	-	NA	ns
Last STROBE time	t_{RFS}	-	75	-	60	-	50	-	60	-	60	ns
Pause time	t_{RP}	160	-	125	-	100	-	100	-	100	-	ns
IORDY pull-up time	t_{IORYZ}	-	20	-	20	-	20	-	20	-	20	ns
IORDY wait time	t_{ZIORY}	0	-	0	-	0	-	0	-	0	-	ns
DMACK setup/hold time	t_{ACK}	20	-	20	-	20	-	20	-	20	-	ns
STROBE STOP time	t_{SS}	50	-	50	-	50	-	50	-	50	-	ns

10.11.5 Serial ROM interface block

Parameter	Symbol	Conditions	MIN.	MAX.	Unit
Clock frequency	t_{SCL}			100	kHz
Clock pulse with Low	t_{LOW}		4.7		μs
Clock pulse with High	t_{HIGH}		4.0		μs
Clock Low to data Valid	t_{AA}		100	4500	ns
Start hold time	$t_{HD.STA}$		4.0		μs
Start setup time	$t_{SU.STA}$		4.7		μs
Data in hold time	$t_{HD.DAT}$		0		ns
Data in setup time	$t_{SU.DAT}$		0.2		μs
Data out hold time	t_{DH}		50		ns
Stop setup time	$t_{SU.STO}$		4.7		μs
Time the bus must be free before a new transmission can start	t_{BUF}		10		μs
Write cycle time	t_{WR}		10		ms

Figure 10-6. Transmit Waveform for Transceiver at DP/DM

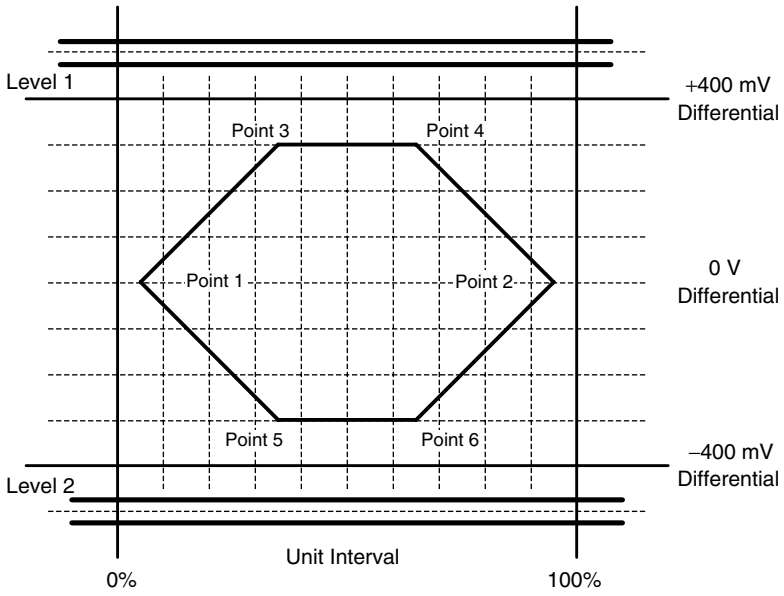
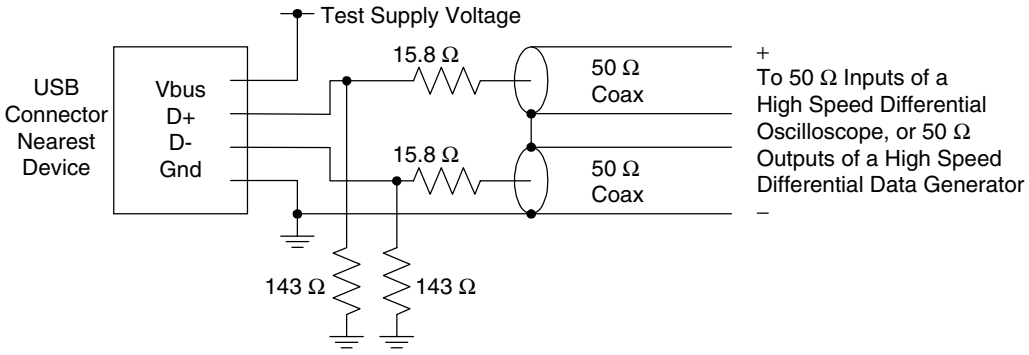


Figure 10-7. Transmitter Measurement Fixtures



10.12 Timing Diagram

Figure 10-8. System Reset Timing

Remark After RESET is negated, this chip read the serial ROM first. Do not reset while the serial ROM is read. The serial ROM is completed to read below time, after RESET is negated.

$5 + 0.1197 \times$ bytes (serial ROM size) $+ 0.5678$ (ms)

Example In the case of 512 bytes: 66.855 ms, in the case of 8 Kbytes: 986.15 ms

Figure 10-9. USB Power-on and Connection Events

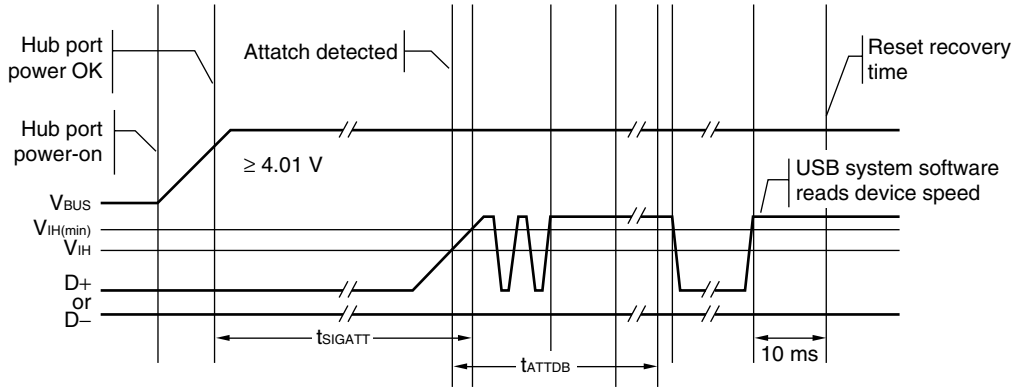


Figure 10-10. USB Differential Data Jitter for Full-speed

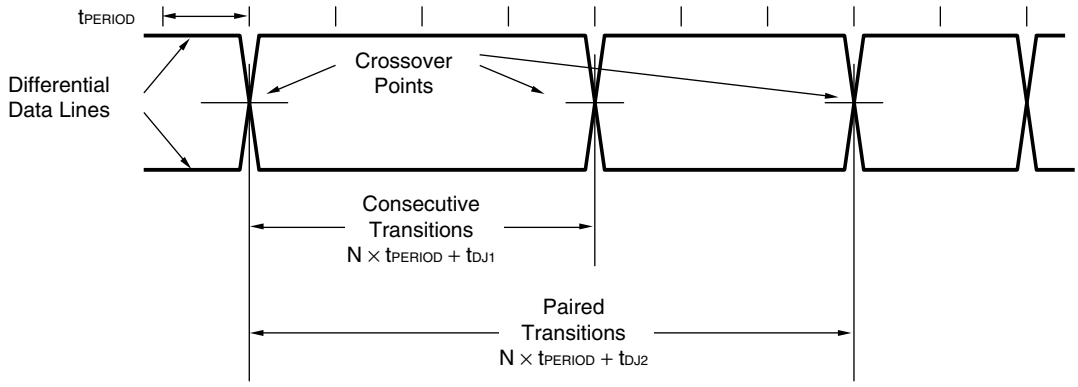


Figure 10-11. USB Differential-to-EOP Transition Skew and EOP Width for Full-speed

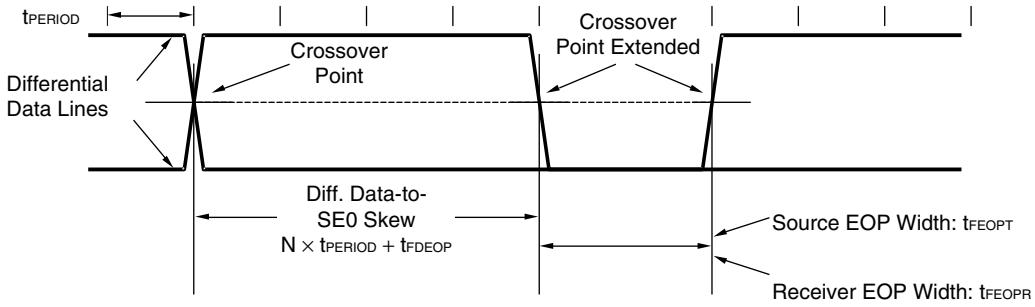


Figure 10-12. USB Receiver Jitter Tolerance for Full-speed

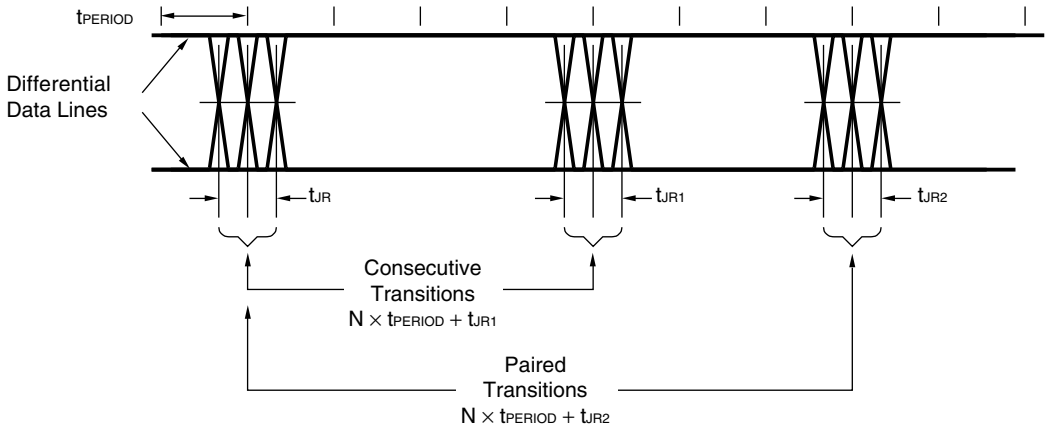


Figure 10-13. USB Connection Sequence on Full-speed System Bus

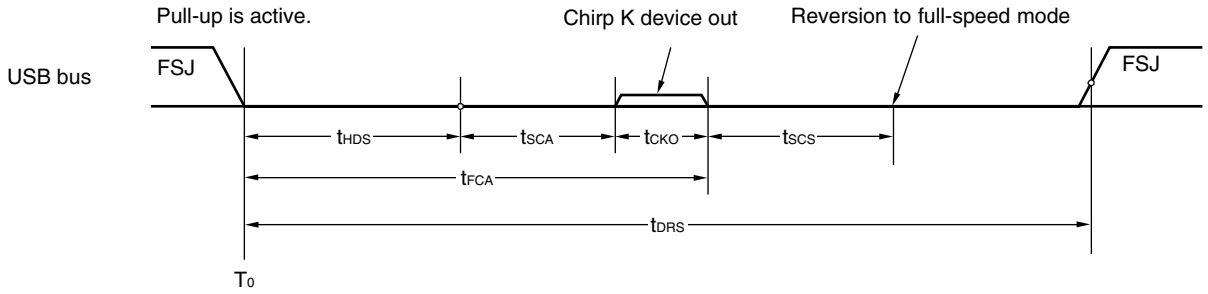


Figure 10-14. USB Connection Sequence on High-speed System Bus

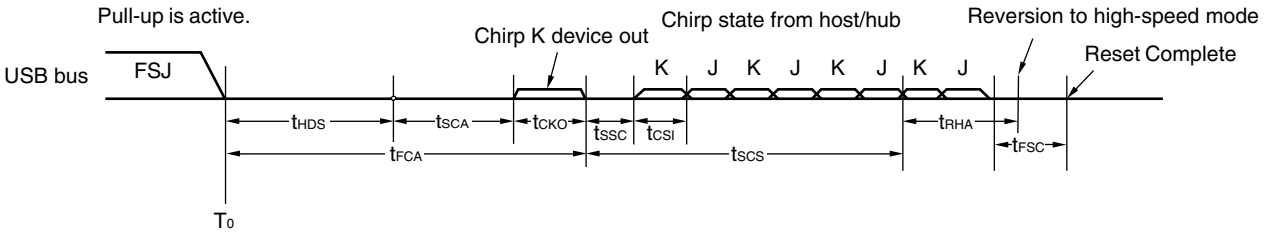


Figure 10-15. USB Reset Sequence from Suspend State on Full-speed System Bus

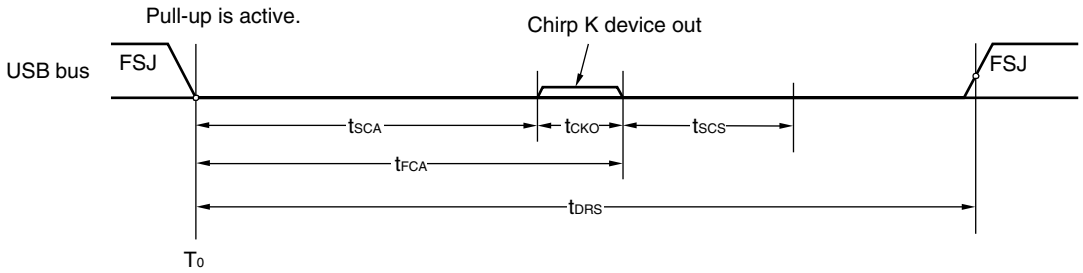


Figure 10-16. USB Reset Sequence from Suspend State on High-speed System Bus

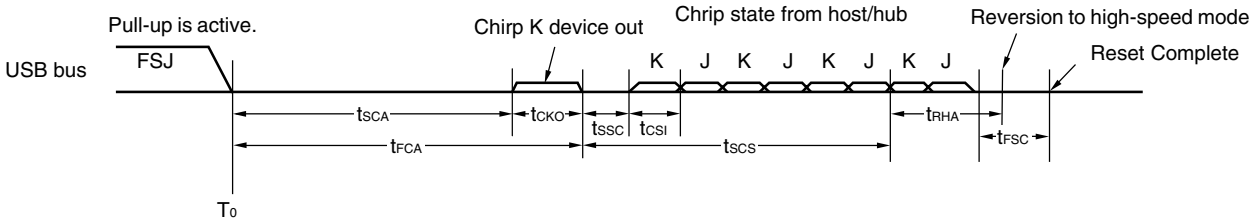


Figure 10-17. USB Suspend and Resume on Full-speed System Bus

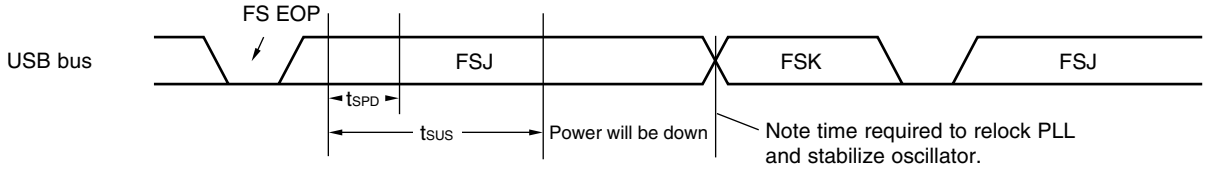


Figure 10-18. USB Suspend and Resume on High-speed System Bus

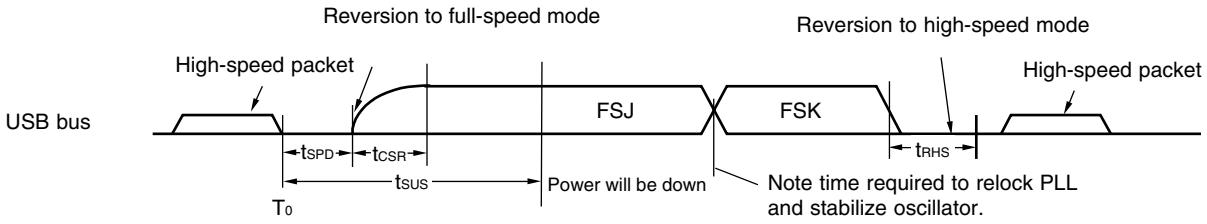


Figure 10-19. IDE PIO Mode Timing

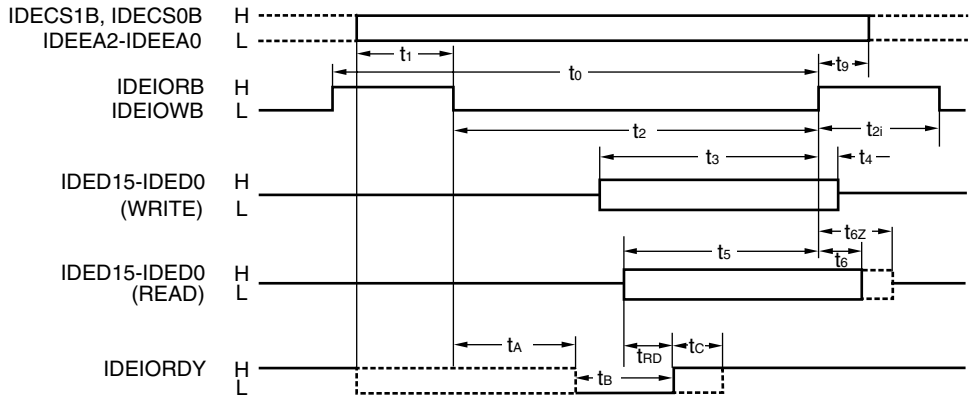


Figure 10-20. IDE Multi Word DMA Mode Timing

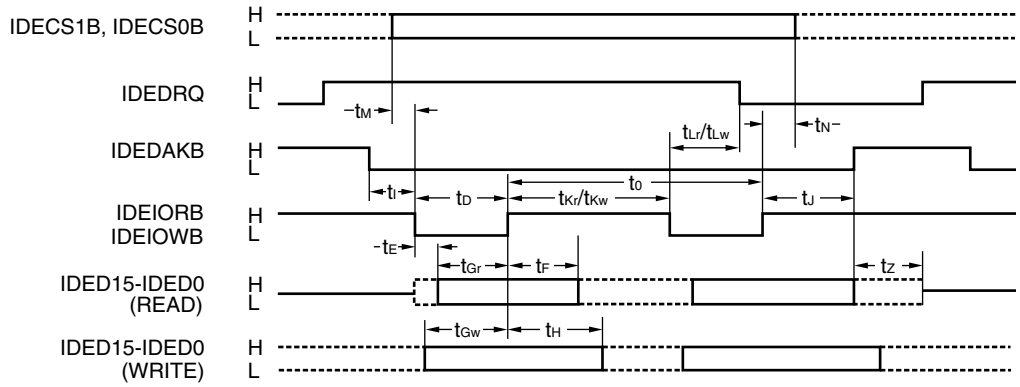


Figure 10-21. IDE Ultra DMA Mode Data-In Timing

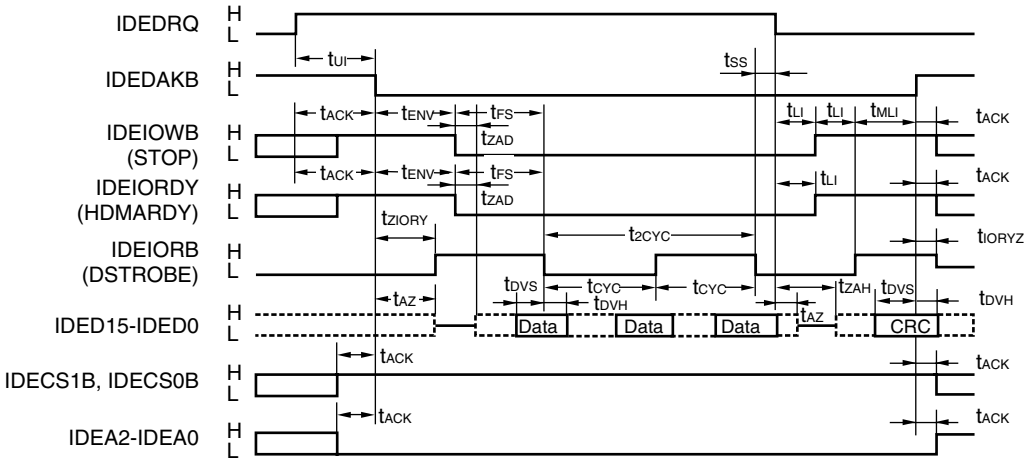


Figure 10-22. IDE Ultra DMA Mode Data-In Stop Timing

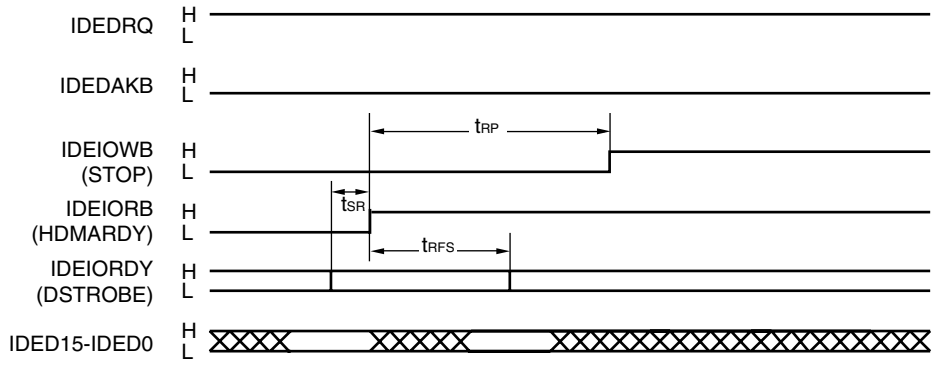


Figure 10-23. IDE Ultra DMA Mode Data-In End Timing

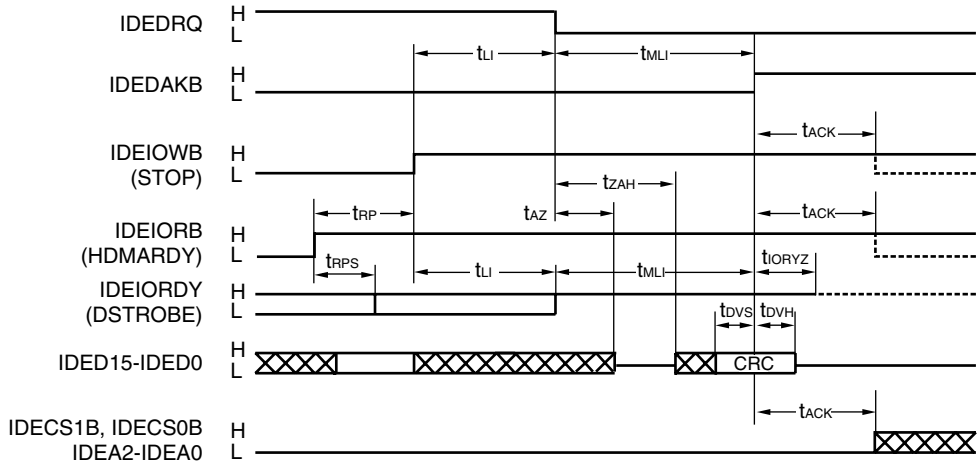


Figure 10-24. IDE Ultra DMA Mode Data-Out Timing

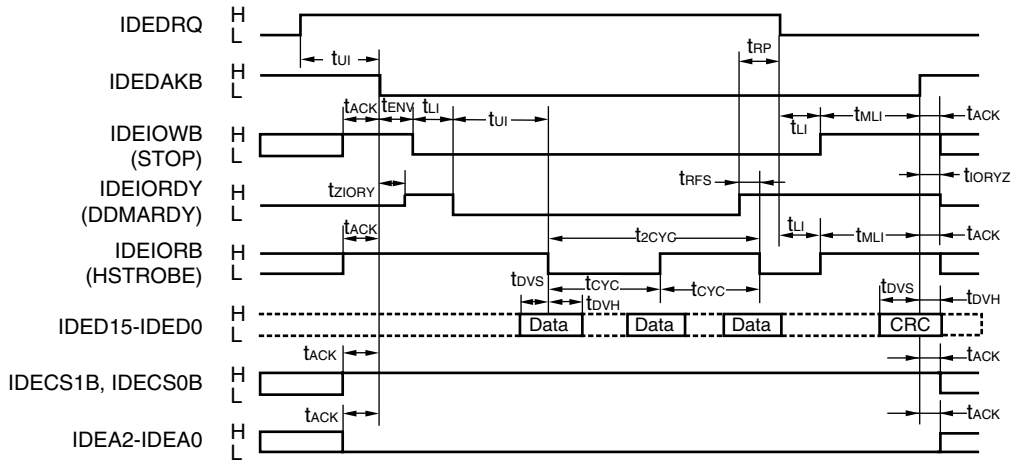


Figure 10-25. IDE Ultra DMA Mode Data-Out Stop Timing

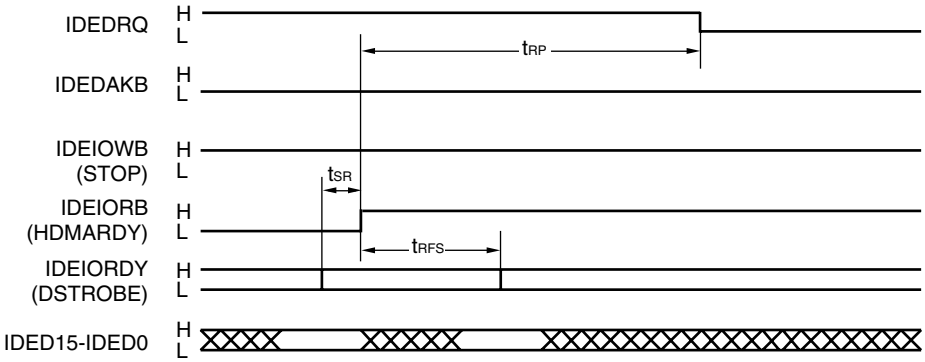


Figure 10-26. IDE Ultra DMA Mode Data-Out End Timing

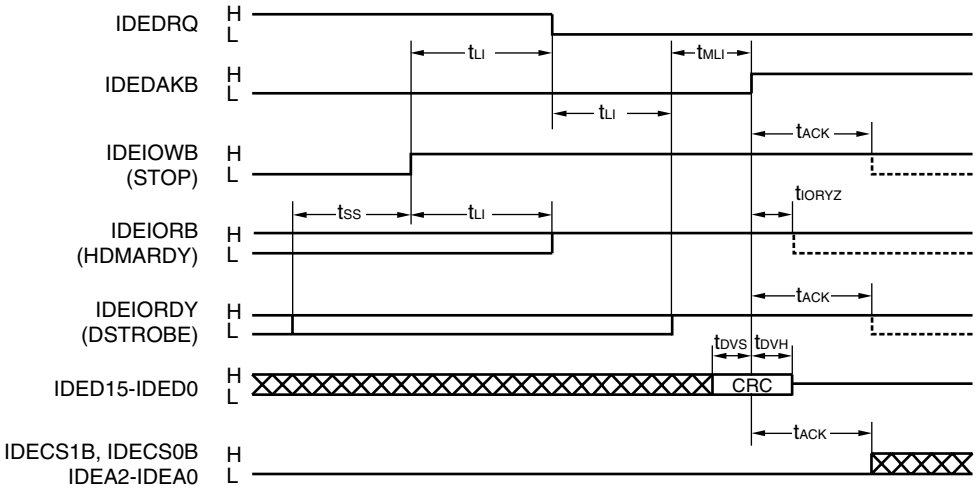


Figure 10-27. IDE Ultra DMA Mode Data Skew Timing

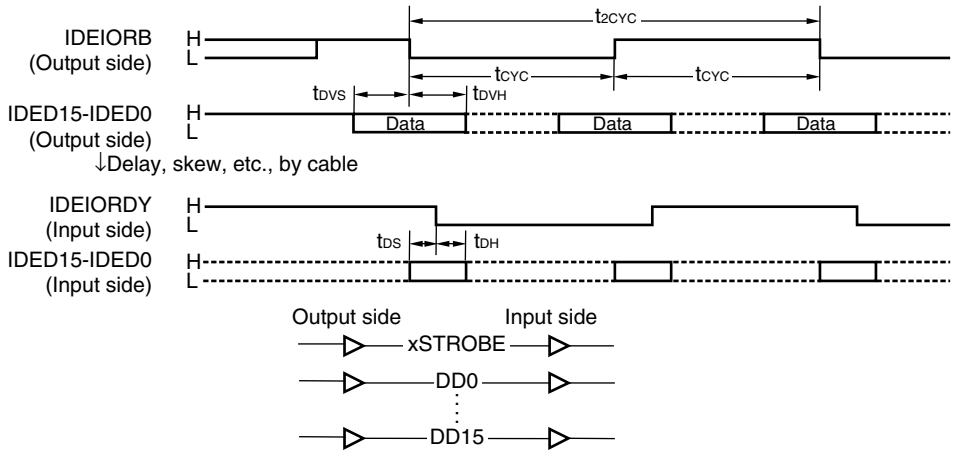


Figure 10-28. Serial ROM Access Timing

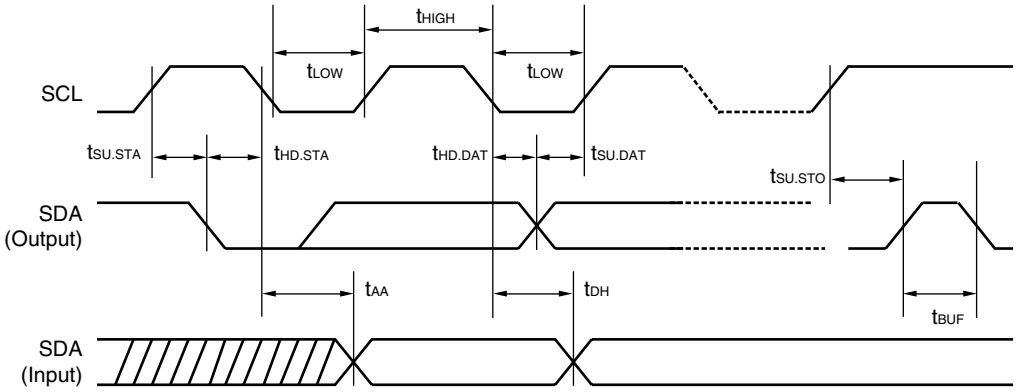


Figure 10-29. Serial ROM Write Cycle Timing