Description

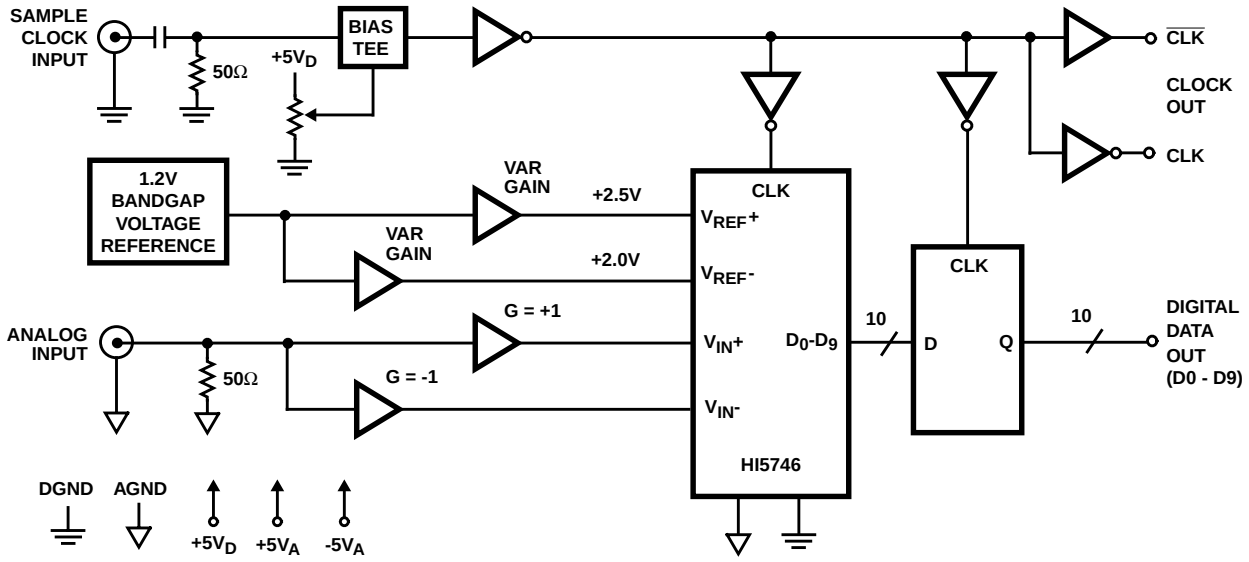
The HI5746EVAL1 evaluation board for the HI5746 can be used to evaluate the performance of the HI5746 10-bit 40MSPS analog-to-digital converter (ADC). As shown in the Evaluation Board Functional Block Diagram, this evaluation board includes sample clock driver circuitry, reference voltage generators and single-ended to differential analog input drive circuitry. Buffered digital data outputs are conveniently provided for easy interfacing to a ribbon connector or logic probes. The evaluation board is provided with some prototyping area for the addition of user designed custom interfaces or circuits.

HI5746 A/D Theory of Operation

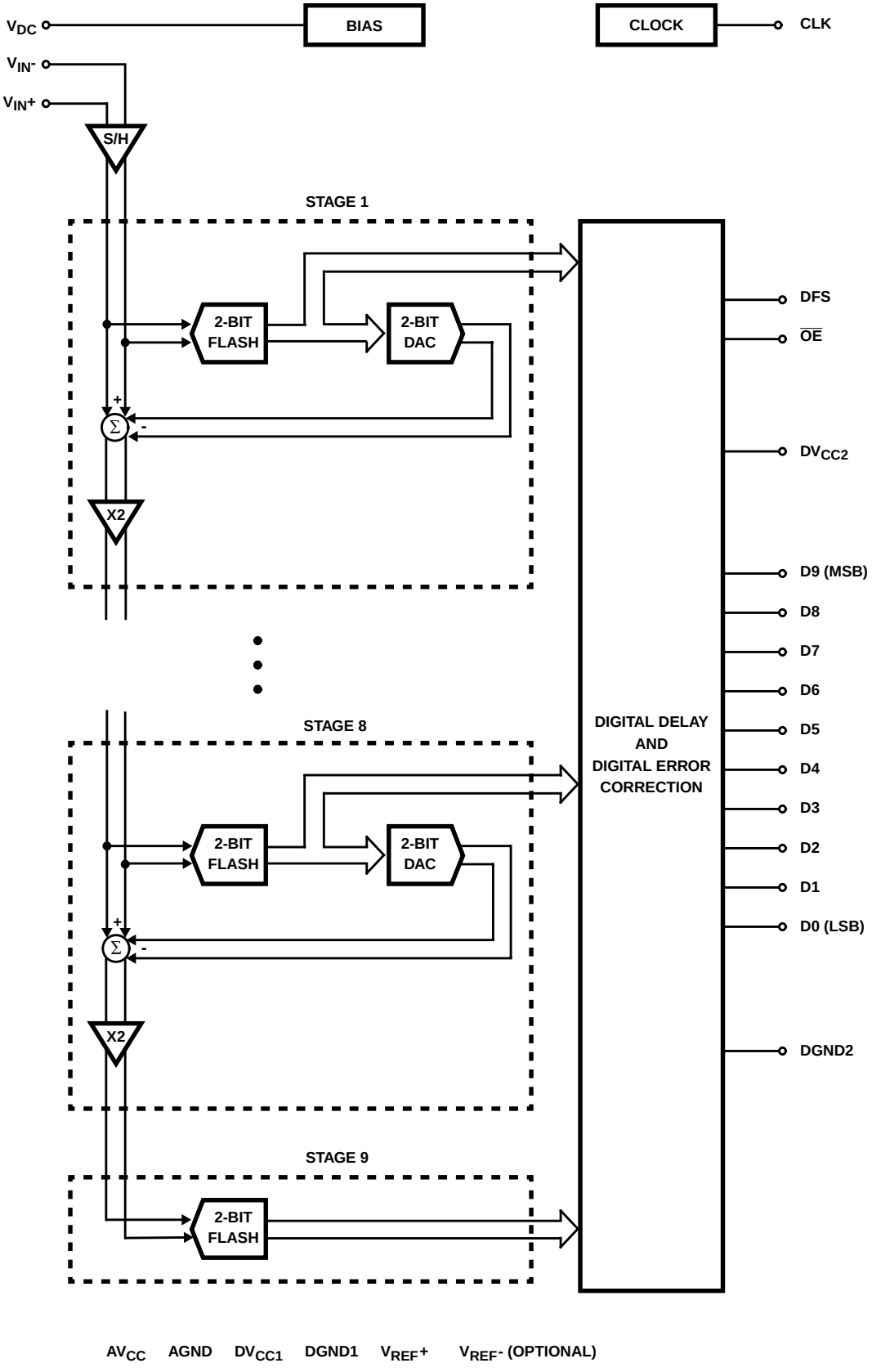
The HI5746 is a 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 1 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H). The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op-amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the V_{IN} pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

As illustrated in the HI5746 functional block diagram and the timing diagram in Figure 2, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

Evaluation Board Functional Block Diagram



HI5746 Functional Block Diagram



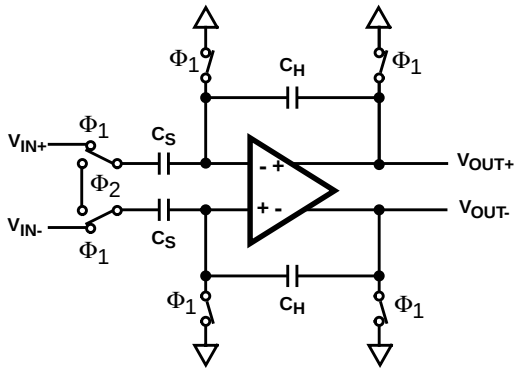
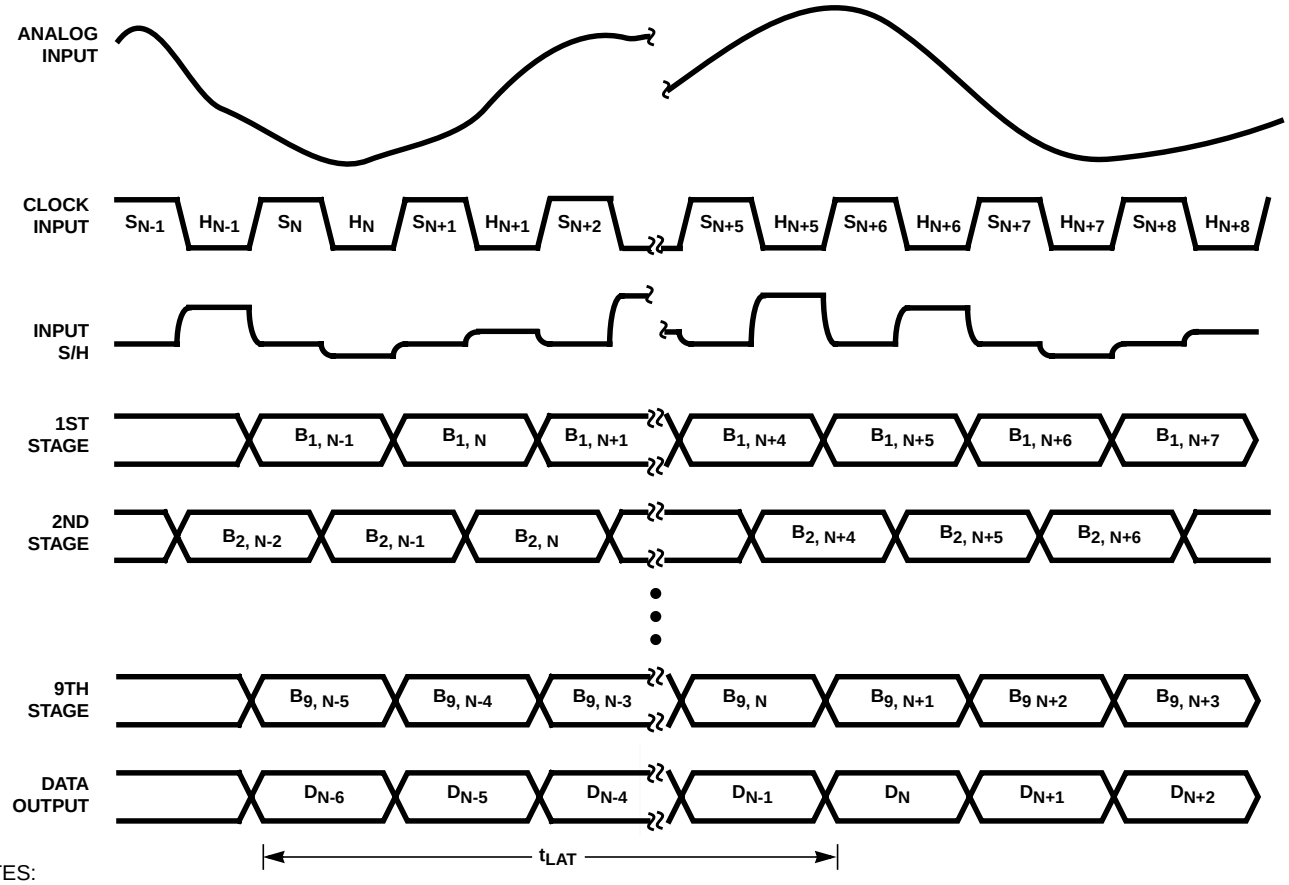


FIGURE 1. ANALOG INPUT SAMPLE-AND-HOLD

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus on the 7th cycle of the clock after the analog sample is taken. This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is synchronized to the external sampling clock by a double buffered latching technique. The output of the digital error correction circuit is available in two's complement or offset binary format depending on the state of the Data Format Select (DFS) control input (see HI5746 Data Sheet Table 1, A/D Code Table).



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. $B_{M, N}$: M-th stage digital output corresponding to N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 2. HI5746 INTERNAL CIRCUIT TIMING

Layout and Power Supplies

The HI5746EVAL1 evaluation board is a four layer board with a layout optimized for the best performance of the ADC. Included in the application note are electrical schematics of the evaluation board circuitry, a components layout, a components part list and views of the various board layers that make up the printed wiring board. The user should feel free to copy the layout in their application. Refer to the components layout and the evaluation board electrical schematics for the following discussions.

The HI5746 A/D converter has separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The evaluation board provides separate low impedance analog and digital ground planes. Since the analog and digital ground planes of the evaluation board are connected together at a single point where the power supplies enter the board, **DO NOT** tie the grounds together back at the power supplies.

The analog and digital supplies are also kept separate on the evaluation board and should be driven by clean linear regulated supplies. The power supplies can be hooked up with external wires to the holes marked +5VAIN, +5VA1IN, -5VAIN, +5VDIN, +5VD1IN and +5VD2IN. +5VDIN, +5VD1IN and +5VD2IN are digital supplies and should be returned to DGND. +5VAIN, +5VA1IN and -5VAIN are the analog supplies and should be returned to AGND. Table 1 lists the operational supply voltages for the evaluation board. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	NOMINAL VALUE	CURRENT (TYP)	FUNCTION(S) SUPPLIED
+5VAIN	5.0V ±5%	121mA	Analog Input and Reference Voltage Generator Op Amps, Bandgap Reference
+5VA1iN	5.0V ±5%	30mA	A/D AV_{CC}
-5VAIN	-5.0V ±5%	120mA	Analog Input and Reference Voltage Generator Op Amps, Bandgap Reference
+5VDIN	5.0V ±5%	5mA	Sample Clock Generator, D0-D9 D-FF
+5VD1IN	5.0V ±5%	13mA	A/D DV_{CC1}
+5VD2IN	5.0V ±5% / 3.0V ±10%	3mA	A/D DV_{CC2}

Reference Voltage Generator Circuit

The HI5746 is designed to accept two external reference voltage sources at the V_{REF} input pins. Typical operation of the converter requires V_{REF}+ to be set at +2.5V and V_{REF}- to be set at 2.0V. However, it should be noted that the input structure of the V_{REF}+ and V_{REF}- input pins consists of a resistive voltage divider with one resistor of the divider (nominally 500Ω) connected between V_{REF}+ and V_{REF}- and the other resistor of the divider (nominally 2000Ω) connected between V_{REF}- and analog ground. This allows the user the option of supplying only the +2.5V V_{REF}+ voltage reference with the +2.0V V_{REF}- being generated internally by the voltage division action of the input structure.

The HI5746 is tested with V_{REF}- equal to +2.0V and V_{REF}+ equal to +2.5V yielding a fully differential analog input voltage range of ±0.5V.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at **both** of the reference voltage input pins, V_{REF}+ and V_{REF}-.

The V_{REF}+ and V_{REF}- reference voltage generation circuitry on the evaluation board consists of a Intersil ICL8069 +1.2V bandgap voltage reference (D1) along with operational amplifiers (U3 and U4) both operating in a non-inverting variable gain configuration that is utilized to generate the reference voltages for the HI5746. The reference voltages, V_{REF}+ and V_{REF}-, are set at the factory to the proper voltage levels required by the HI5746. Variable resistor VR1 is used to adjust V_{REF}+ to +2.5V and variable resistor VR2 is used to adjust V_{REF}- to +2.0V.

Operation of the converter with a single +2.5V V_{REF}+ reference voltage can be demonstrated by simply removing R20 from the V_{REF}- generation circuit. This opens the path between the V_{REF}- operational amplifier (U4) output and the V_{REF}- input of the HI5746 while still providing decoupling at the converter V_{REF}- voltage reference input pin.

Sample Clock Driver

In order to ensure rated performance of the HI5746, the duty cycle of the sample clock should be held at 50%. It must also have low phase noise and operate at standard TTL logic levels.

It can be difficult to find a low phase noise generator that will provide a 40MHz squarewave at TTL logic levels. Consequently, the HI5746EVAL1 evaluation board is designed with a logic inverter (U7) acting as a voltage comparator to generate the sampling clock for the HI5746 when a sinewave (< ±1.5V) is applied to the CLK input of the evaluation board. The sample clock sinewave is AC coupled into the input of the inverter and a discrete bias tee is used to bias the sinewave around the trigger level of the inverter's input. A potentiometer (VR3) varies the DC bias voltage added to the sinewave input allowing the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC and to evaluate the effects of sample clock duty cycle on the performance of the converter. The trigger level for the sample clock input to the HI5746 converter is approximately 1.5V. Therefore, the duty cycle of the sampling clock should be measured around the 1.5V trigger level at the HI5746 sample clock input pin.

The sinewave to logic level comparator drives a series of additional inverters that provides isolation between the four sample clocks used on the evaluation board. One clock is used to drive the converter sample clock input pin, a second clock is used to drive the digital output data (D0-D9) D-type

flip-flop and the last two provide CLK and $\overline{CLK}$ at the data output connector, P2. The clock/data relationship at the P2 output connector is as follows. CLK has rising edges aligned with data transitions and $\overline{CLK}$ has rising edges mid-bit.

The data corresponding to a particular analog input sample will be available at the digital outputs of the HI5746 after the data latency (7 cycles) plus the HI5746 digital data output delay.

The sample clock and digital output data signals are buffered and made available through two connectors contained on the evaluation board. The line buffering allows for driving long leads or analyzer inputs. These drivers are not necessary for the digital output data if the load presented to the converter does not exceed the data sheet CMOS drive limits and a load capacitance of 10pF. P1 allows the evaluation board to be interfaced to the DSP evaluation boards available from Intersil and should be installed on the **far side (layer 4)** of the evaluation board for proper signal routing to the DSP evaluation boards. The digital output data and sample clock can also be accessed by clipping the test leads of a logic analyzer or data acquisition system onto the I/O pins of connector P2.

The A/D converters $\overline{OE}$ control input pin allows the digital output data bus of the converter to be switched to a three-state high impedance mode. This feature enables the testing and debugging of systems which are utilizing one or more converters. This three-state control signal is not intended for use as an enable/disable function on a common data bus and could result in possible bus contention issues. The A/D converters $\overline{OE}$ control input pin is controlled by the installation or removal of a shunt, JP1, contained on the evaluation board. Installation of JP1 forces the $\overline{OE}$ control input pin low for normal operation while removal of JP1 allows the digital output data bus of the converter to be switched to a three-state high impedance mode.

Analog Input

The fully differential analog input of the HI5746 A/D can be configured in various ways depending on the signal source and the required level of performance.

Differential Analog Input Configuration

For the AC coupled differential input (Figure 3) assume the difference between $V_{REF}+$, typically 2.5V, and $V_{REF}-$, typically 2.0V, is 0.5V. Fullscale is achieved when the V_{IN} and $-V_{IN}$ input signals are $0.5V_{P-P}$, with $-V_{IN}$ being 180 degrees out of phase with V_{IN}. The converter will be at positive fullscale when the $V_{IN}+$ input is at V_{DC} + 0.25V and the $V_{IN}-$ input is at V_{DC} - 0.25V ($V_{IN}+ - V_{IN}- = +0.5V$). Conversely, the converter will be at negative fullscale when the $V_{IN}+$ input is equal to V_{DC} - 0.25V and $V_{IN}-$ is at V_{DC} + 0.25V ($V_{IN}+ - V_{IN}- = -0.5V$).

Since the HI5746 is powered by a single +5V analog supply, the analog input is limited to be between ground and +5V. For the differential input connection this implies the analog input common mode voltage can range from 0.25V to 4.75V, see Figure 4. The performance of the ADC does not change significantly with the value of the analog input common mode voltage.

A DC voltage source, V_{DC}, equal to 3.2V (typical), is made available to the user to help simplify circuit design when using an AC coupled differential input. This low output impedance voltage source is not designed to be a reference but makes an excellent DC bias source and stays well within the analog input common mode voltage range over temperature.

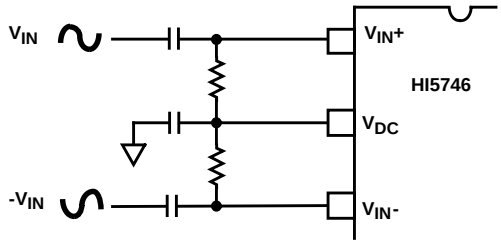


FIGURE 3. AC COUPLED DIFFERENTIAL INPUT

The HI5746EVAL1 evaluation board accepts a single-ended analog input and converts it to a differential signal for driving the $V_{IN}+$ and $V_{IN}-$ analog inputs of the converter. The single-ended to differential conversion is accomplished through the use of two operational amplifiers (U1 and U2). U1 is configured as a unity gain amplifier and U2 is configured as an inverting amplifier with a gain of minus one.

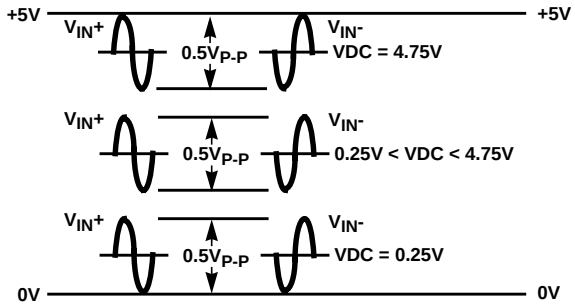


FIGURE 4. DIFFERENTIAL ANALOG INPUT COMMON MODE VOLTAGE RANGE

HI5746 Performance Characterization

Dynamic testing is used to evaluate the HI5746 performance. Among these tests are Signal-to-Noise and Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR) and InterModulation Distortion (IMD).

Figure 5 shows the test system used to perform dynamic testing on high-speed ADC's at Intersil. The clock (CLK) and analog input (AIN) signals are sourced from low phase noise HP8662A synthesized signal generators that are phase locked to each other to ensure coherence. The output of the signal generator driving the ADC analog input is bandpass filtered to improve the harmonic distortion of the analog input signal. The comparator on the evaluation board will convert the sine wave CLK input signal to a square wave to drive the

sample clock input of the HI5746. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has the required software to perform the Fast Fourier Transform (FFT) and do the data analysis.

Coherent testing is recommended in order to avoid the inaccuracies of windowing. The sampling frequency and analog input frequency have the following relationship: $f_I/f_S = M/N$, where f_I is the frequency of the input analog sinusoid, f_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and odd number (1, 3, 5, ...) the samples are assured of being nonrepetitive.

Refer to the HI5746 data sheet for a complete list of test definitions and the results that can be expected using the evaluation board with the test setup shown. Evaluating the part with a reconstruction DAC is only suggested when doing bandwidth or video testing.

Video Testing

Figure 6 shows how a test system can be configured to do video testing of the HI5746 with the DAC reconstruction board and the HI5746EVAL1 evaluation board. The appropriate test waveform is generated by a video source such as the TSG100 or TEK1001 from Tektronix and applied to the converter. The digitized video is converted back to analog by the reconstruction DAC for evaluation by a video analyzer, TEK VM700.

Since the HI5746 is a 10-bit A/D, install jumpers JP1 and JP2 on the DAC reconstruction board to tie the DAC two LSB's high. Install JP3 so that the video out of the reconstruction board will have negative going sync. JP5-9 on the DAC reconstruction board are utilized to establish the correct clock/data timing relationship into the DAC.

Set up the HI5746EVAL1 evaluation board for video testing by following the procedures outlined previously in the HI5746EVAL1 evaluation board application note on the video input configuration and single-ended DC coupled analog inputs. Input the video signal to the HI5746EVAL1 evaluation board through the SMA connector marked VIDEO. Note that all cables carrying video should be 75Ω.

Finally, mate the DAC reconstruction board P1 connector to the HI5746EVAL1 evaluation board P2 connector. Correct alignment between the two boards will have P1 pin 34 of the DAC reconstruction board plugged into P2 pin 25 of the HI5746EVAL1 evaluation board.

See Application Note AN9419 "Using the DAC Reconstruct Board" for additional applications information.

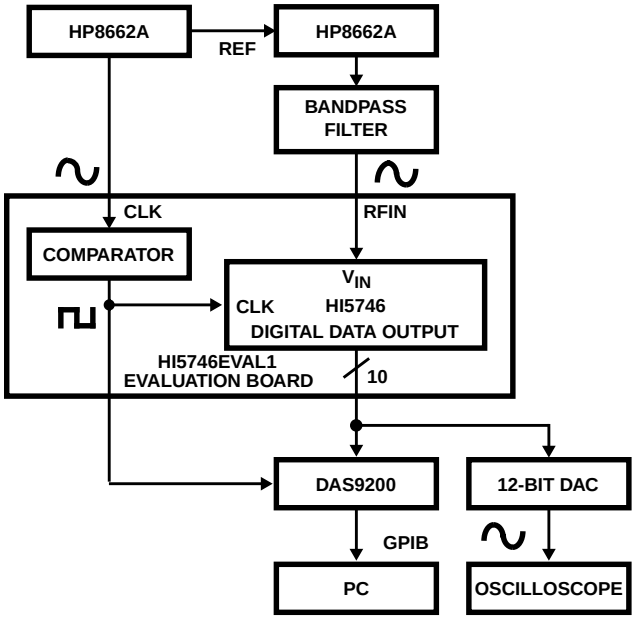


FIGURE 5. HIGH-SPEED A/D TEST SYSTEM

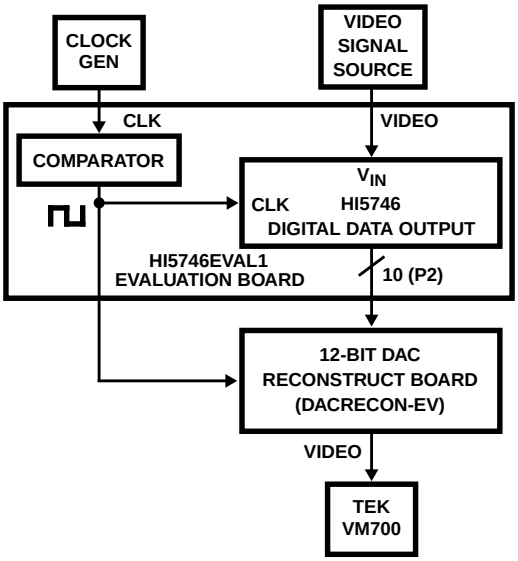


FIGURE 6. VIDEO TEST SETUP

Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	DV_{CC1}	Digital Supply (+5.0V)
2	DGND1	Digital Ground
3	DV_{CC1}	Digital Supply (+5.0V)
4	DGND1	Digital Ground
5	AV_{CC}	Analog Supply (+5.0V)
6	AGND	Analog Ground
7	$V_{REF}+$	+2.5V Positive Reference Voltage Input
8	$V_{REF}-$	+2.0V Negative Reference Voltage Input (Optional)
9	$V_{IN}+$	Positive Analog Input
10	$V_{IN}-$	Negative Analog Input
11	V_{DC}	DC Bias Voltage Output
12	AGND	Analog Ground
13	AV_{CC}	Analog Supply (+5.0V)
14	$\overline{OE}$	Digital Output Enable Control Input
15	DFS	Data Format Select Input
16	D9	Data Bit 9 Output (MSB)
17	D8	Data Bit 8 Output
18	D7	Data Bit 7 Output
19	D6	Data Bit 6 Output
20	D5	Data Bit 5 Output
21	DGND2	Digital Ground
22	CLK	Sample Clock Input
23	DV_{CC2}	Digital Output Supply (+3.0V or +5.0V)
24	D4	Data Bit 4 Output
25	D3	Data Bit 3 Output
26	D2	Data Bit 2 Output
27	D1	Data Bit 1 Output
28	D0	Data Bit 0 Output (LSB)

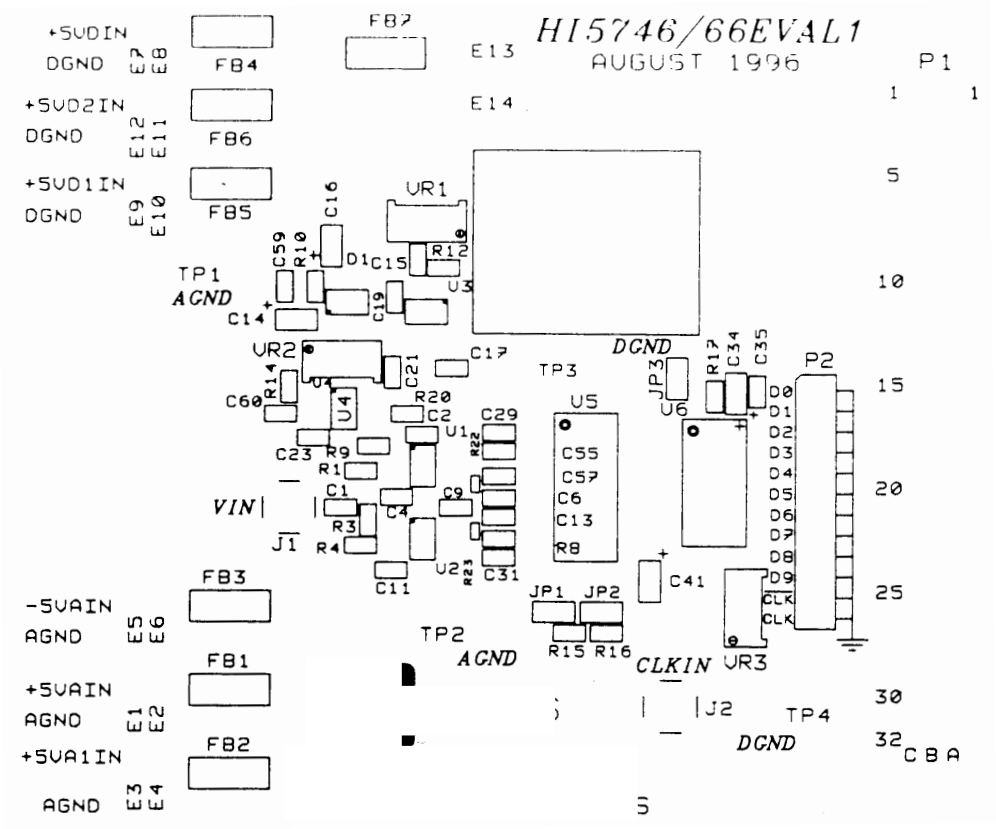


FIGURE 7. HI5746EVAL1 EVALUATION BOARD PARTS LAYOUT (NEAR SIDE)

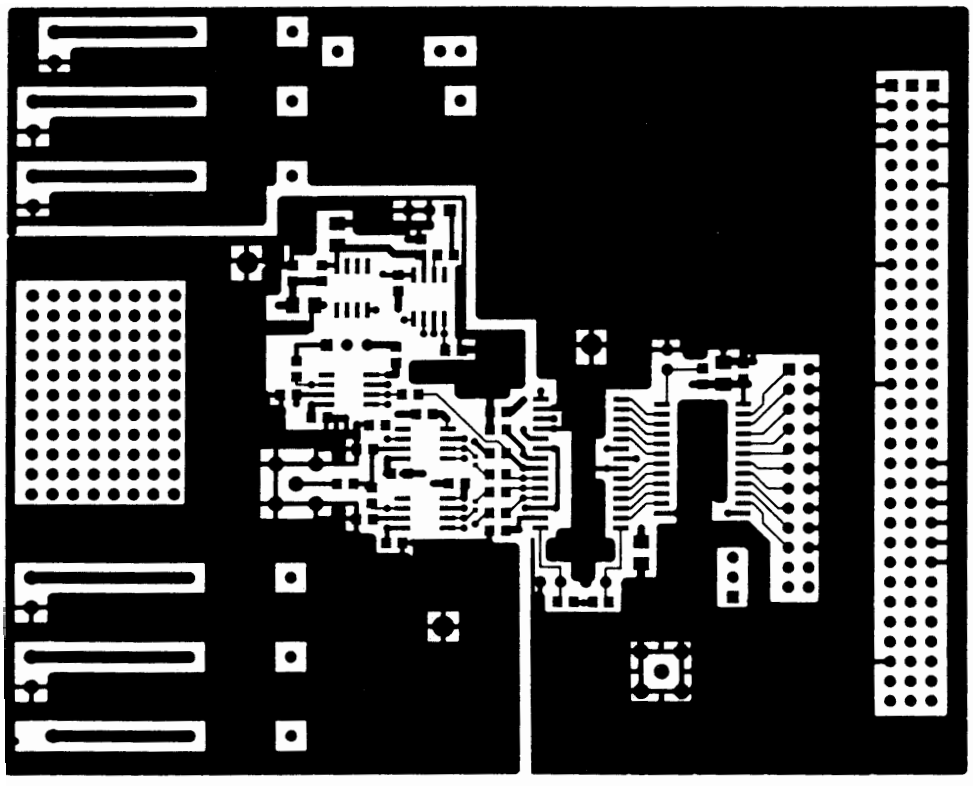


FIGURE 8. HI5746EVAL1 EVALUATION BOARD COMPONENT NEAR SIDE (LAYER 1)

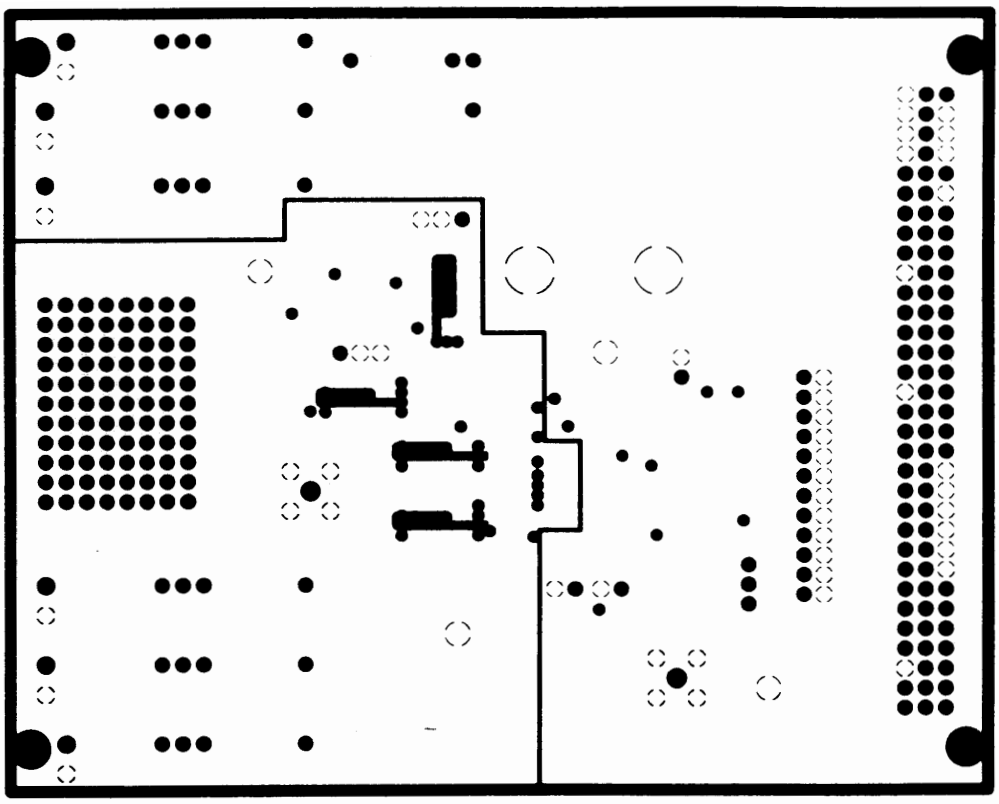


FIGURE 9. HI5746EVAL1 EVALUATION BOARD GROUND PLANE LAYER (LAYER 2)

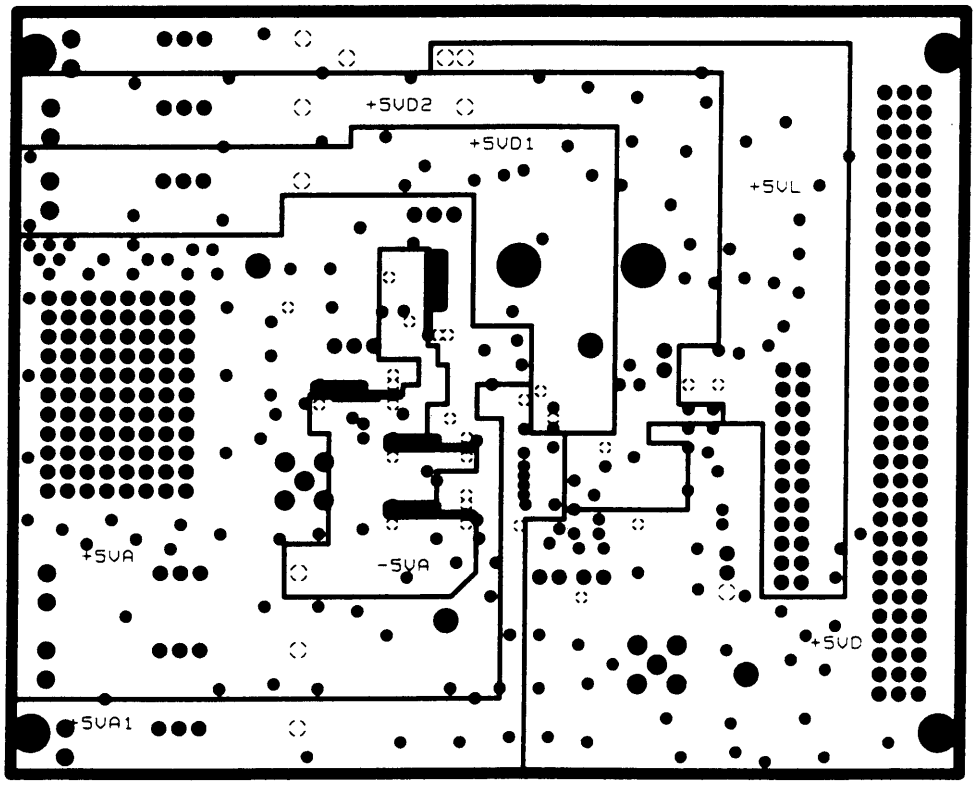


FIGURE 10. HI5746EVAL1 EVALUATION BOARD POWER PLANE LAYER (LAYER 3)

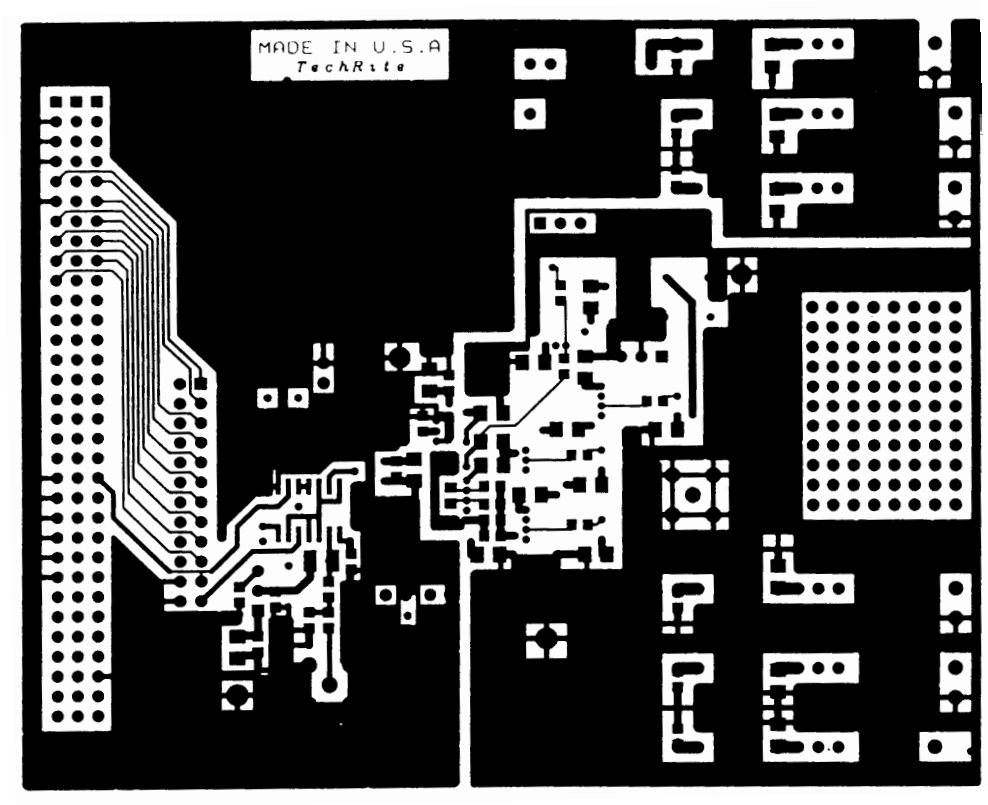


FIGURE 11. HI5746EVAL1 EVALUATION BOARD COMPONENT FAR SIDE (LAYER 4)

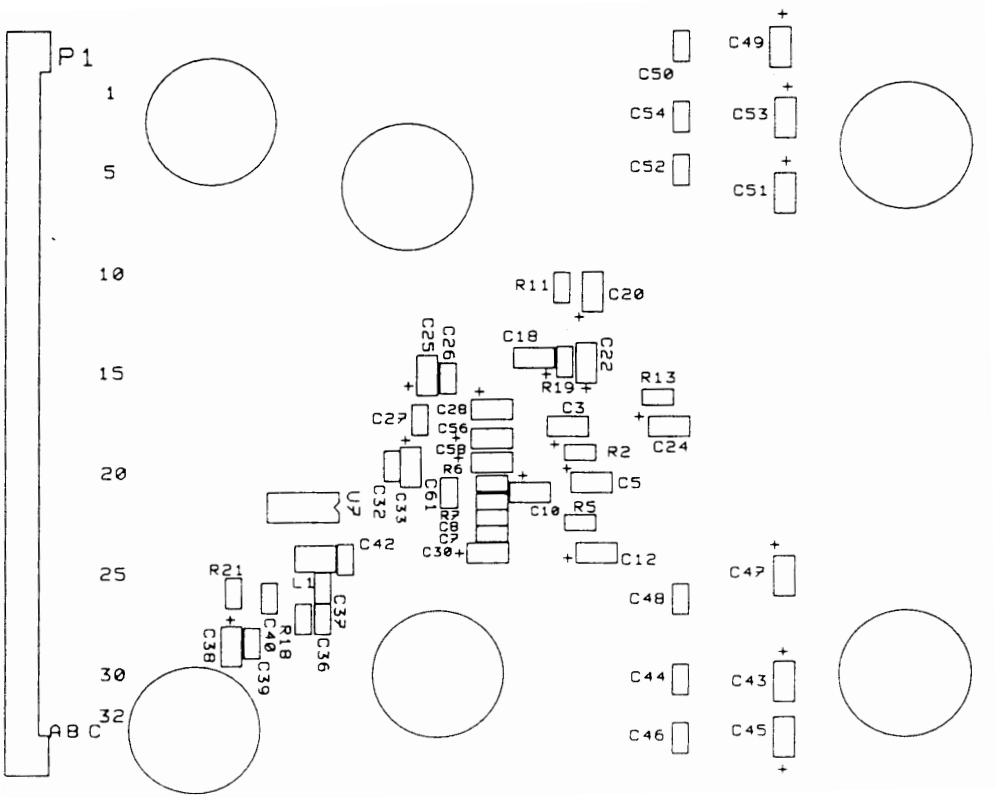
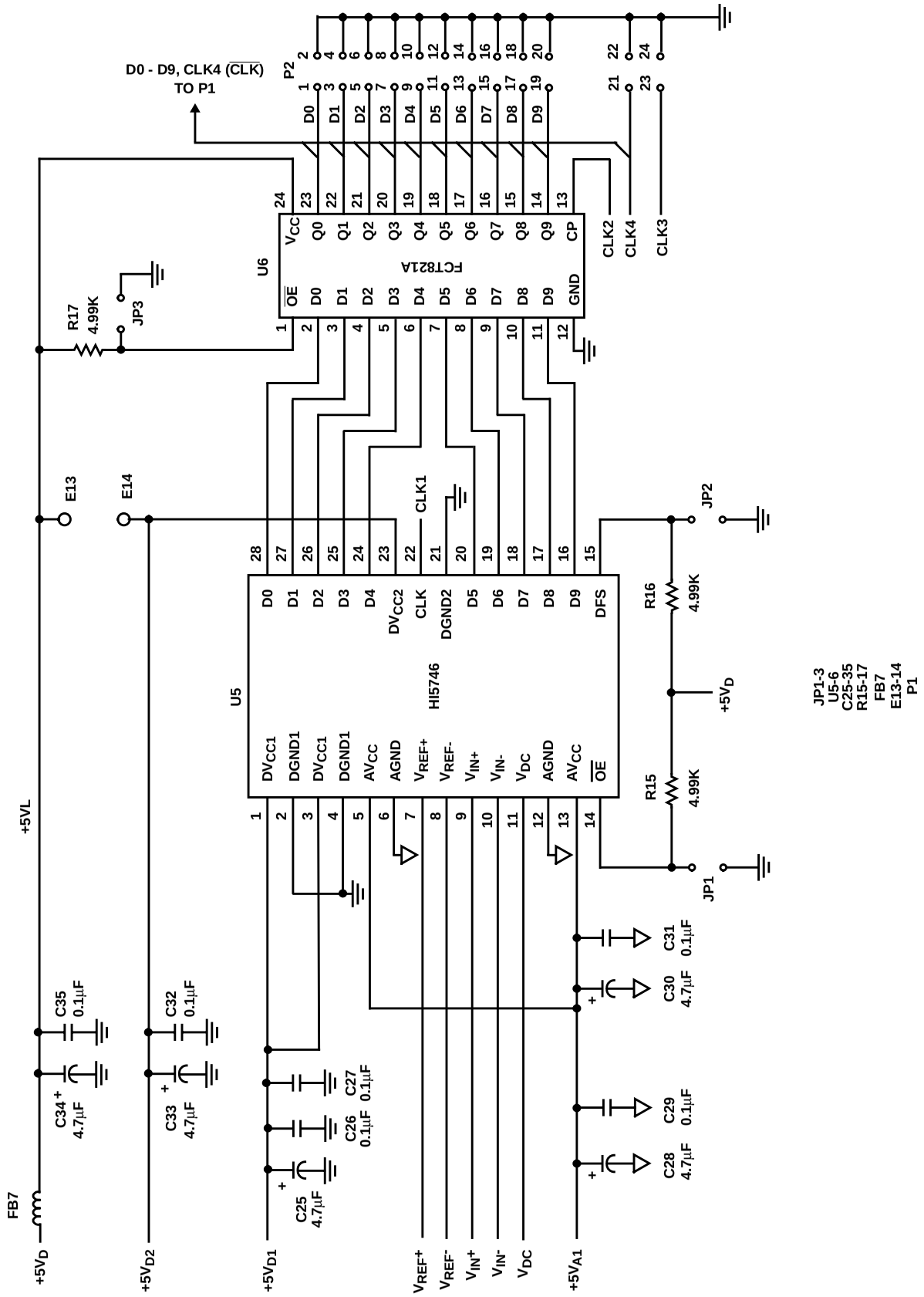
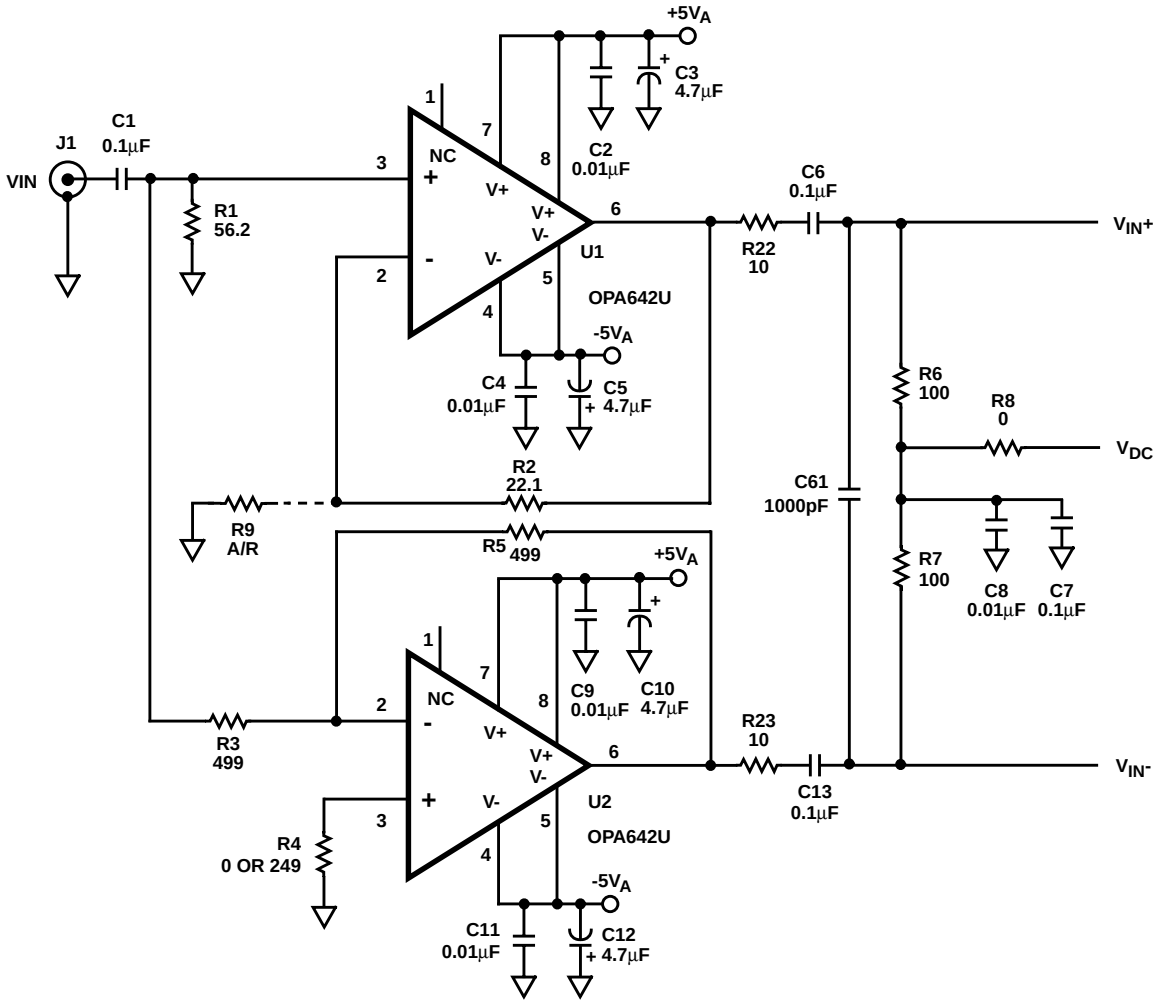


FIGURE 12. HI5746EVAL1 EVALUATION BOARD PARTS LAYOUT (FAR SIDE)

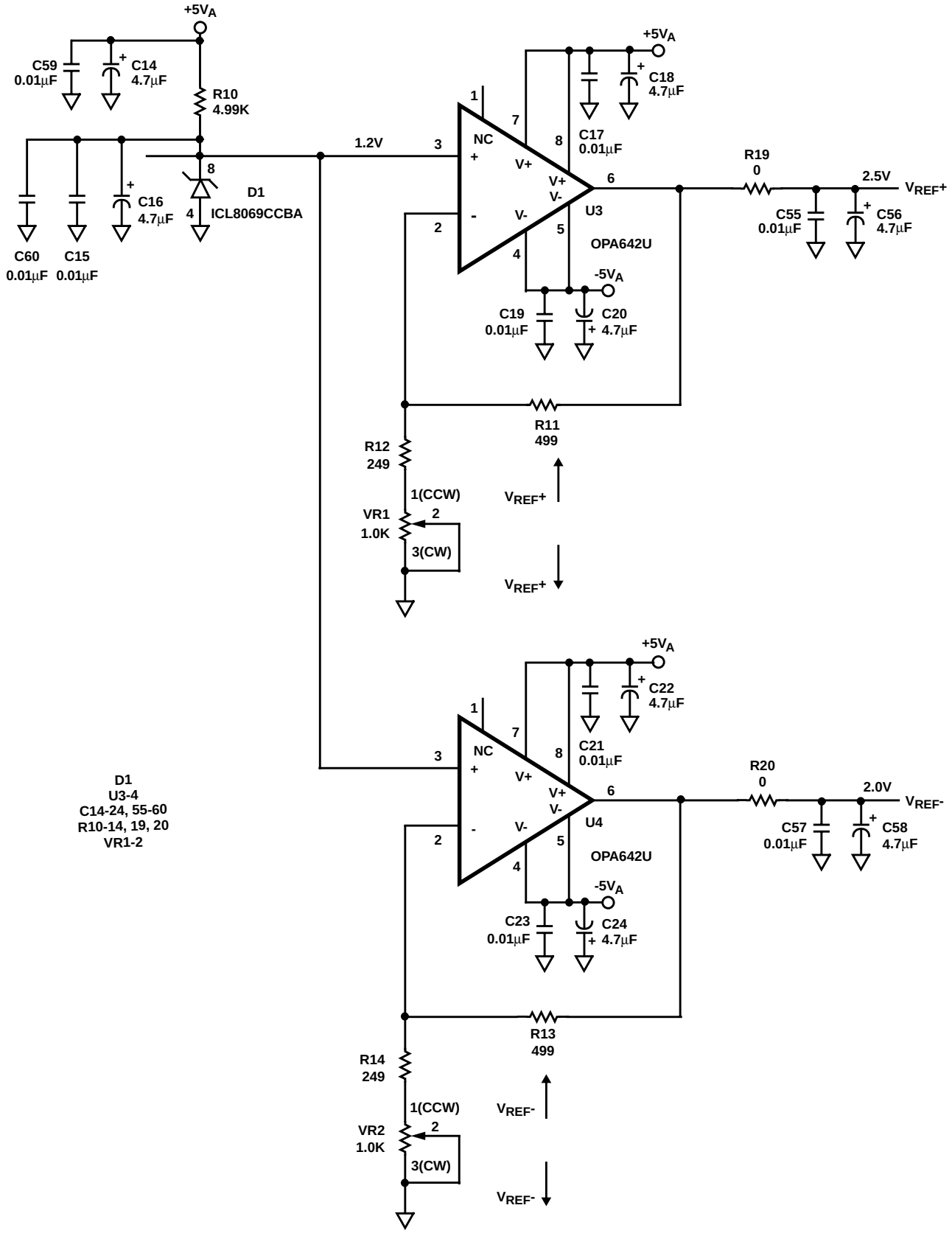
HI5746EVAL1 Evaluation Board Schematic Diagrams



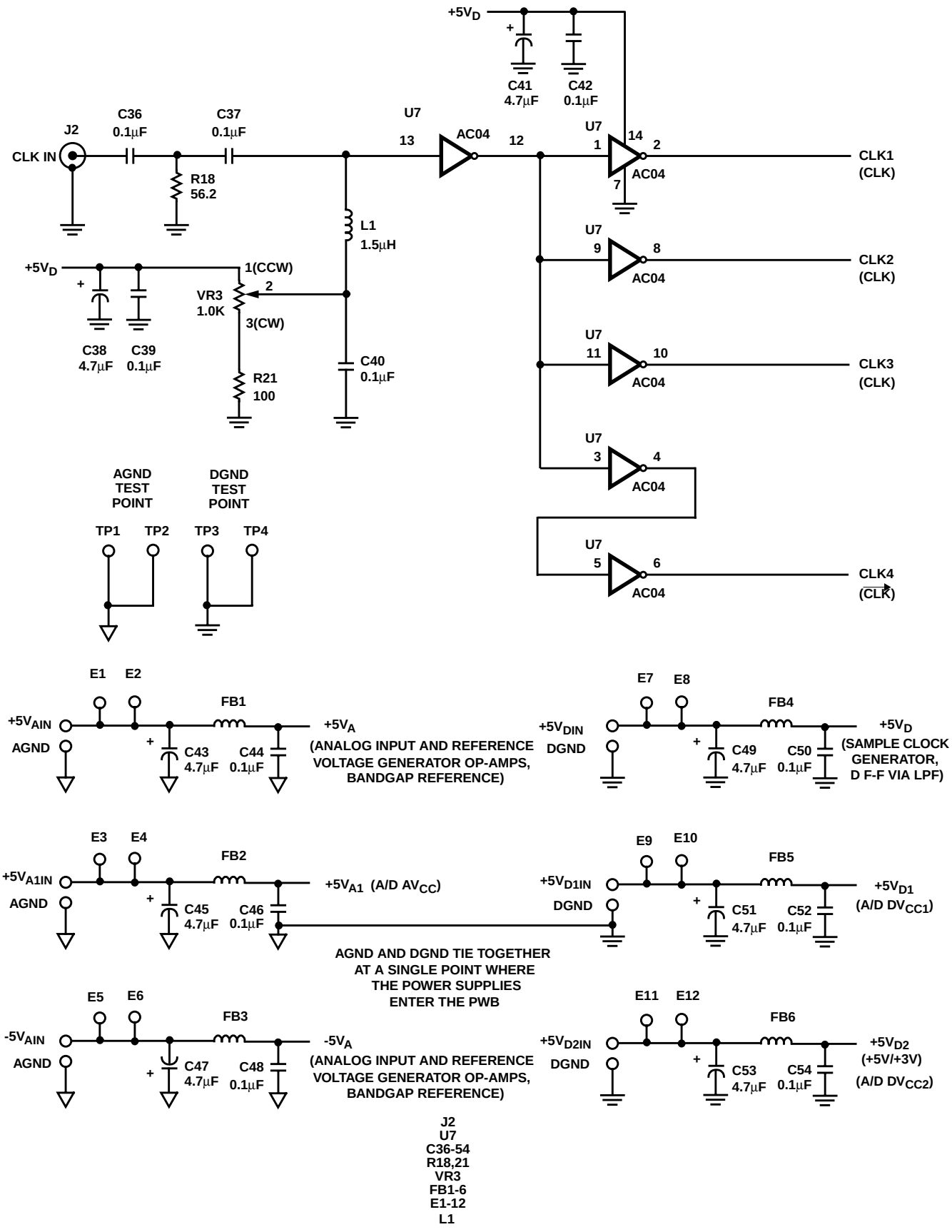
HI5746EVAL1 Evaluation Board Schematic Diagrams (Continued)



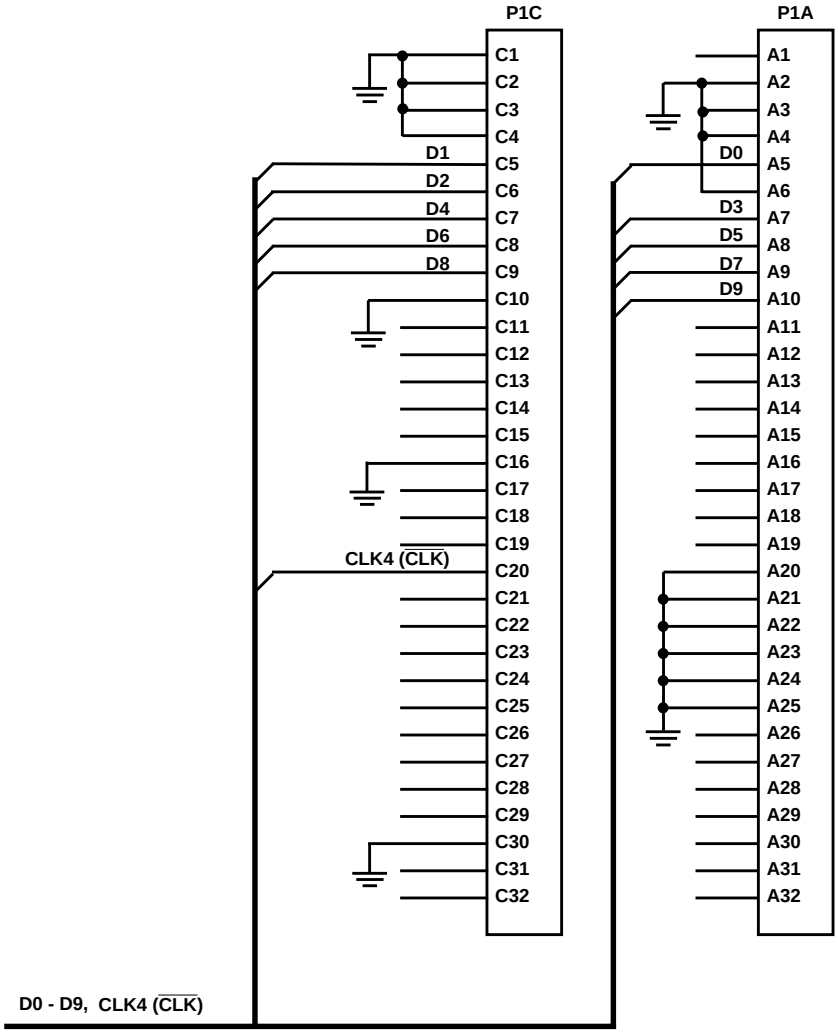
HI5746EVAL1 Evaluation Board Schematic Diagrams (Continued)



HI5746EVAL1 Evaluation Board Schematic Diagrams (Continued)



HI5746EVAL1 Evaluation Board Schematic Diagrams (Continued)



HI5746EVAL1 Evaluation Board Parts List

REFERENCE DESIGNATOR	QTY	DESCRIPTION
R1, 18	2	56.2Ω, 1/8W 805 CHIP, 1%
R9	1	A/RΩ, 1/8W 805 CHIP, 1%
R2	1	22.1Ω, 1/8W 805 CHIP, 1%
R3, 5, 11, 13	4	499Ω, 1/8W 805 CHIP, 1%
R4, 12, 14	3	249Ω, 1/8W 805 CHIP, 1%
R8, 19, 20	3	0.0Ω, 1/4W 805 CHIP, 1%
R6, 7, 21	3	100Ω, 1/8W 805 CHIP, 1%
R10, 15, 16, 17	4	4.99kΩ, 1/8W 805 CHIP, 1%
R22, 23	2	10Ω, 1/16W 402 CHIP, 1%
VR1, 2, 3	3	1kΩ TRIM POT
C3, 5, 10, 12, 14, 16, 18, 20, 22, 24, 25, 28, 30, 33, 34, 38, 41, 43, 45, 47, 49, 51, 53, 56, 58	25	4.7µF CHIP TANT CAP, 10WVDC, 20%, EIA CASE A
C1, 6, 7, 13, 26, 27, 29, 31, 32, 35, 36, 37, 39, 40, 42, 44, 46, 48, 50, 52, 54	21	0.1µF CER CAP, 50WVDC, 10%, 805 CASE, Y5V DIELECTRIC
C61	1	1000pF CER CAP, 50WVDC, 10%, 805 CASE, X7R DIELECTRIC
C2, 4, 8, 9, 11, 15, 17, 19, 21, 23, 55, 57, 59, 60	14	0.01µF CER CAP, 50WVDC, 10%, 805 CASE, X7R DIELECTRIC
FB1-7	7	10µH FERRITE BEAD
L1	1	1.5µH CHIP INDUCTOR, 1210 CASE
J1,2	2	SMA STRAIGHT JACK PCB MOUNT
-	4	RUBBER FEET
-		DUT CLAMP
JP1, 2, 3	3	1x2 HEADER
JPH1, 2, 3	3	1x2 HEADER JUMPER
P2	1	2x12 HEADER
P1	1	64-PIN EUROCARD RT ANGLE
AGND, DGND	4	TEST POINT
D1	1	INTERSIL ICL8069CCBA LOW VOLTAGE BANDGAP REFERENCE
U5	1	INTERSIL HI5746KCB 10-BIT 40MHz A/D CONVERTER
U1, 2, 3, 4	4	OP-AMP
U6	1	10-BIT D-TYPE FLIP-FLOP
U7	1	HEX INVERTER