Description

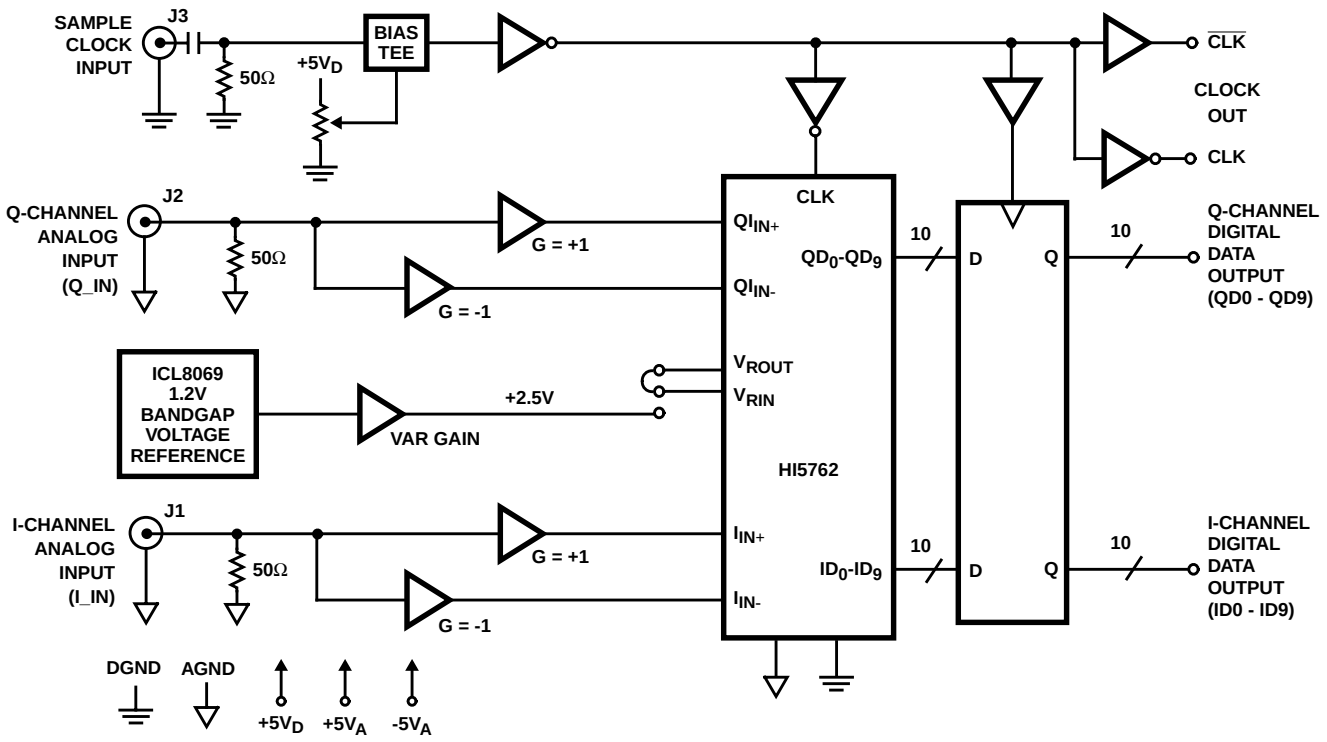
The HI5762EVAL2 evaluation board is made available to allow the circuit designer the ability to evaluate the performance of the Intersil HI5762 monolithic Dual 10-bit 60 MSPS analog-to-digital converter (ADC) with internal voltage reference. As shown in the Evaluation Board Functional Block Diagram, this evaluation board includes sample clock generation circuitry, a single-ended to differential analog input amplifier configuration for both the I and Q channel inputs, an external variable voltage reference and digital data output latches/buffers. The buffered digital data outputs are conveniently provided for easy interfacing to a ribbon connector or logic probes.

The sample clock generator circuit accepts the external sampling signal through an SMA type RF connector, J3. This input is AC-coupled and terminated in 50Ω allowing for connection to most laboratory signal generators. In addition, the duty cycle of the clock driving the A/D converter is made adjustable by way of a potentiometer so that the effects of sample clock duty cycle on the HI5762 may be observed.

The I and Q channel analog input signals are also connected through SMA type RF connectors, J1 and J2, and applied to single-ended to differential analog input amplifiers. These inputs are AC-coupled and terminated in 50Ω allowing for connection to most laboratory signal generators. Also, provisions for differential RC lowpass filters are incorporated on the output of the differential amplifiers to limit the broadband noise going into the HI5762 converter.

The I and Q channel digital data output latches/buffers consist of a pair of 74FCT2821 D-type flip-flops. The digital data output interface provides both phases of the sampling clock, CLK and $\overline{CLK}$, so that the digital data transitions are essentially time aligned with the rising edge of the $\overline{CLK}$ sampling clock or time aligned with the falling edge of the CLK sampling clock.

Evaluation Board Functional Block Diagram



Evaluation Board Layout and Power Supplies

The HI5762 evaluation board is a four layer board with a layout optimized for the best performance of the ADC. Included in the application note are electrical schematics of the evaluation board, a component parts list, a component placement layout drawing and reproductions of the various board layers used in the board stack-up. The user should feel free to copy the layout in their application. Refer to the component layout and the evaluation board electrical schematic for the following discussions.

The HI5762 monolithic A/D converter has been designed with separate analog and digital supply and ground pins to keep digital noise out of the analog signal path. The evaluation board provides separate low impedance analog and digital ground planes on layer 2. Since the analog and digital ground planes are connected together at a single point where the power supplies enter the board, **DO NOT** tie them together back at the power supplies.

The analog and digital power planes are also kept separate on the evaluation board and should be driven by clean linear regulated supplies. The external power supplies are hooked up with the twisted pair wires soldered to the plated through holes marked +5VAIN, +5VAIN1, -5VAIN, +5VDIN, +5VD1IN, +5VD2IN, AGND and DGND. The +5VDIN, +5VD1IN and +5VD2IN are digital supplies and are returned to DGND. The +5VAIN, +5VAIN1 and -5VAIN are the analog supplies and are returned to AGND. Table 1 lists the operational supply voltages, typical current consumption and the evaluation board circuit function being powered. Single supply operation of the converter is possible but the overall performance of the converter may degrade.

TABLE 1. HI5762EVAL2 EVALUATION BOARD POWER SUPPLIES

POWER SUPPLY	NOMINAL VALUE	CURRENT (TYP)	FUNCTION(S) SUPPLIED
+5VAIN	5.0V±5%	51mA	Analog Input Op Amps, Reference Voltage Op Amps, Bandgap Reference
+5VA1IN	5.0V±5%	73mA	A/D AV_{CC1} and AV_{CC2}
-5VAIN	-5.0V±5%	50mA	Analog Input Op Amps, Reference Voltage Op Amps
+5VDIN	5.0V±5%	15mA	Sample Clock Generator and D-FF's
+5VD1IN	5.0V±5%	61mA	A/D DV_{CC1} and DV_{CC2}
+5VD2IN	5.0V±5% or 3.0V±10%	4.5mA	A/D DV_{CC3}

Sample Clock Driver, Timing and I/O

In order to ensure rated performance of the HI5762, the duty cycle of the sample clock should be held at 50% ±5%. It must also have low phase noise and operate at standard TTL levels.

A CMOS inverter (U7) used as a voltage comparator is provided on the evaluation board to generate the sampling clock for the HI5762 when a sinewave (< $2V_{p-p}$) or squarewave clock is applied to the CLK input (J3) of the evaluation board. A potentiometer (VR2) is provided to allow the user to adjust the duty cycle of the sampling clock to obtain the best performance from the ADC and to allow the user to investigate the effects of expected duty cycle variations on the performance of the converter. The HI5762 clock input trigger level is approximately 1.5V. Therefore, the duty cycle of the sampling clock should be measured at this 1.5V trigger level. U7-2 provides a convenient point to monitor the sample clock duty cycle and make any required adjustments.

Figure 2 shows the sample clock and digital data timing relationship for the evaluation board. The data corresponding to a particular sample will be available at the digital data outputs of the HI5762 after the data latency time, t_{LAT}, of 6 sample clock cycles plus the HI5762 digital data output delay, t_{OD}. Table 2 lists the values that can be expected for the indicated timing delays. Refer to the HI5762 data sheet for additional timing information.

The sample clock and digital output data signals are made available through two connectors contained on the evaluation board. The line buffering provided by the data output latches allows for driving long leads or analyzer inputs. These data latches are not necessary for the digital output data if the load presented to the converter does not exceed the data sheet load limits of 100mA and 15pF. The P2 I/O connector allows the evaluation board to be interfaced to the DSP evaluation boards available from Intersil. Alternatively, the digital output data and sample clock can also be accessed by clipping the test leads of a logic analyzer or data acquisition system onto the I/O pins of connector header P1.

TABLE 2. TIMING SPECIFICATIONS

PARAMETER	DESCRIPTION	TYP
t_{OD}	HI5762 Digital Output Data Delay	50ns
t_{PD1}	U7 Prop Delay	9ns
t_{PD2}	U10/11 Prop Delay	4.5ns

HI5762 Performance Characterization

Dynamic testing is used to evaluate the performance of the HI5762 A/D converter. Among the tests performed are Signal-to-Noise and Distortion Ratio (SINAD), Signal-to-Noise Ratio (SNR), Total Harmonic Distortion (THD), Spurious Free Dynamic Range (SFDR) and Intermodulation Distortion (IMD).

Figure 1 shows the test system used to perform dynamic testing on high-speed ADCs at Intersil. The clock (CLK) and analog input (V_{IN}) signals are sourced from low phase noise HP8662A synthesized signal generators that are phase locked to each other to ensure coherence. The output of the signal generator driving the ADC analog input is bandpass filtered to improve the harmonic distortion of the analog input signal. The comparator on the evaluation board will convert the sine wave CLK input signal to a square wave at TTL logic levels to drive the sample clock input of the HI5762. The ADC data is captured by a logic analyzer and then transferred over the GPIB bus to the PC. The PC has the required software to perform the Fast Fourier Transform (FFT) and do the data analysis.

Coherent testing is recommended in order to avoid the inaccuracies of windowing. The sampling frequency and analog input frequency have the following relationship: $F_I/F_S = M/N$, where F_I is the frequency of the input analog sinusoid, F_S is the sampling frequency, N is the number of samples, and M is the number of cycles over which the samples are taken. By making M an integer and odd number (1, 3, 5, ...) the samples are assured of being nonrepetitive.

Refer to the HI5762 data sheet for a complete list of test definitions and the results that can be expected using the evaluation board with the test setup shown. Evaluating the part with a reconstruction DAC is only suggested when doing bandwidth or video testing.

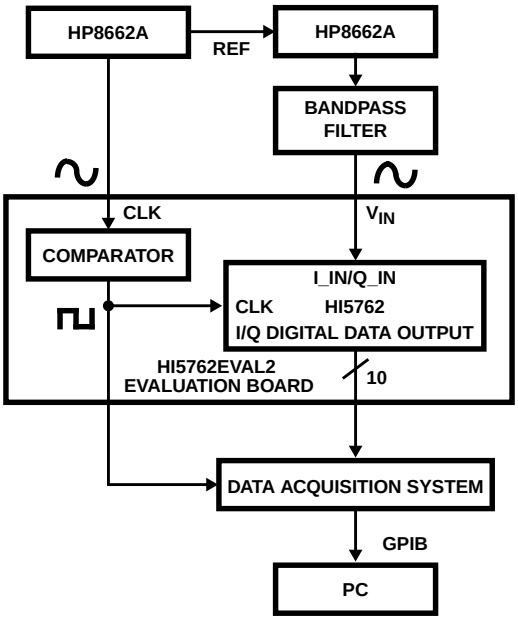


FIGURE 1. HIGH-SPEED A/D PERFORMANCE TEST SYSTEM

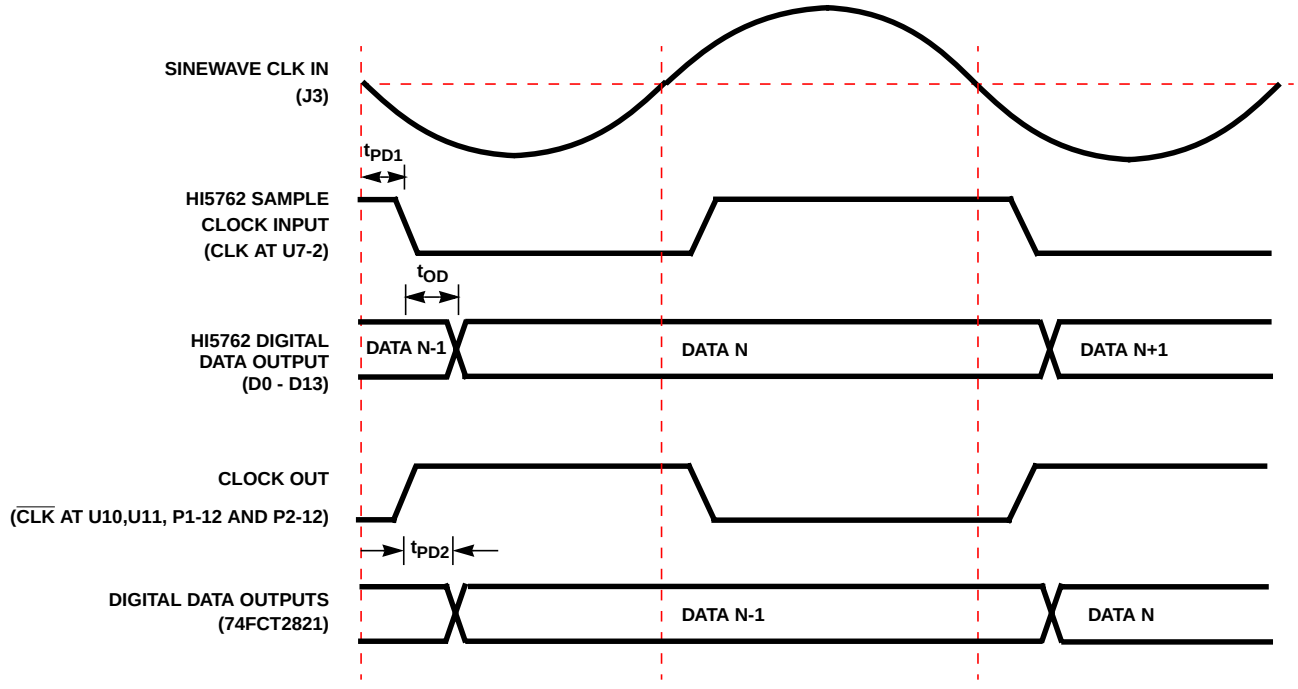


FIGURE 2. EVALUATION BOARD CLOCK AND DATA TIMING RELATIONSHIPS (TYPICAL)

HI5762EVAL2 Typical Performance (Input Amplitude at -0.5dBFS)

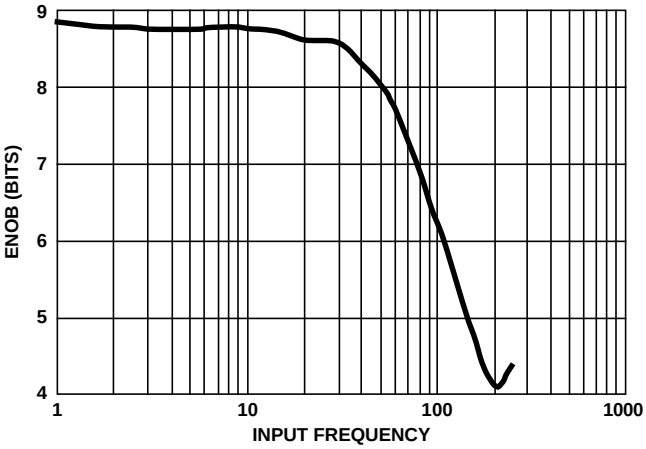


FIGURE 3. EFFECTIVE NUMBER OF BITS (ENOB) vs INPUT FREQUENCY

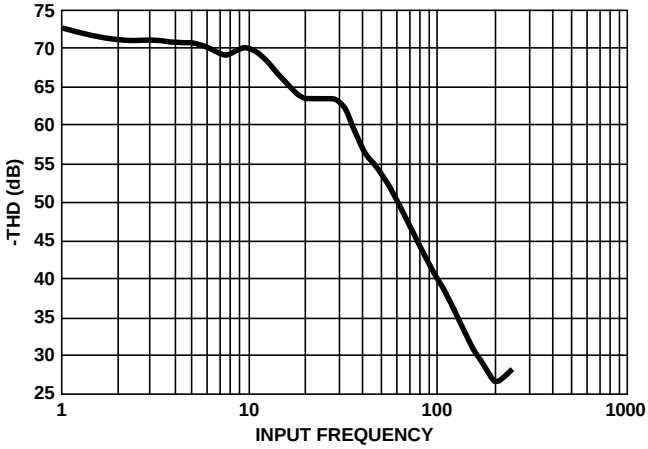


FIGURE 4. TOTAL HARMONIC DISTORTION (THD) vs INPUT FREQUENCY

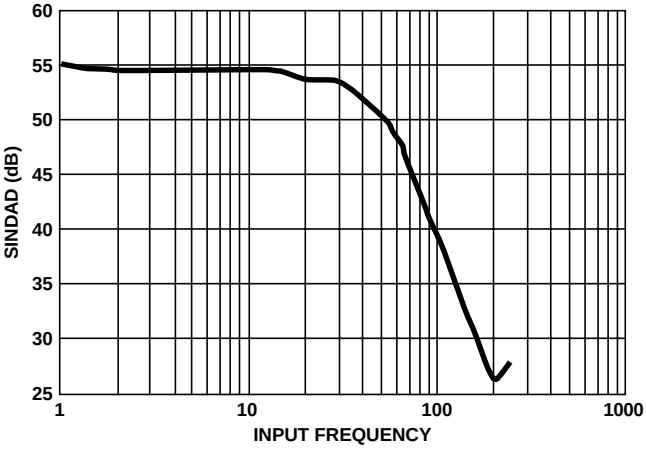


FIGURE 5. SINAD vs INPUT FREQUENCY

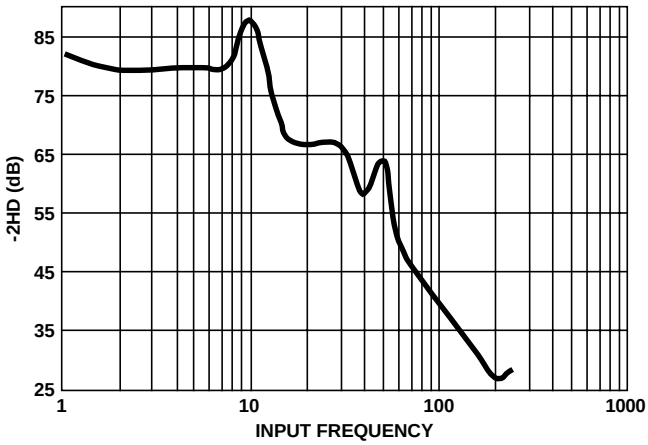


FIGURE 6. SECOND HARMONIC DISTORTION (2HD) vs INPUT FREQUENCY

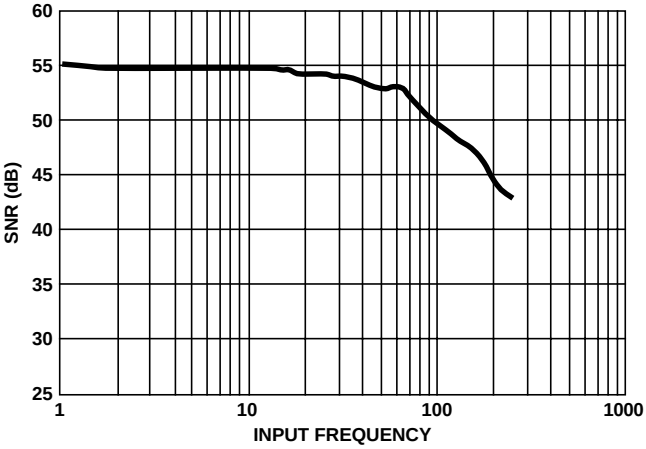


FIGURE 7. SNR vs INPUT FREQUENCY

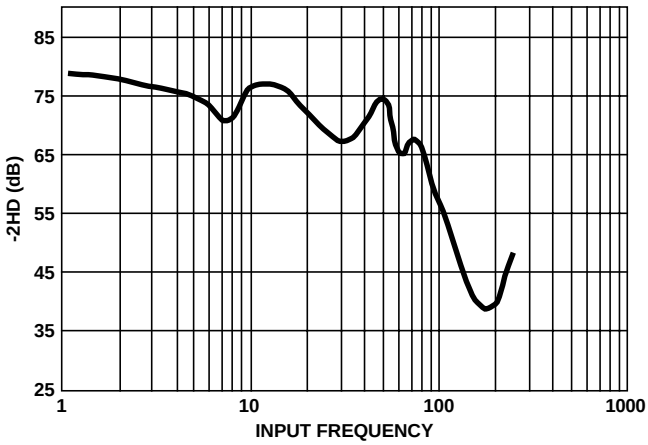


FIGURE 8. THIRD HARMONIC DISTORTION (3HD) vs INPUT FREQUENCY

Appendix A HI5762EVAL2 Board Layout

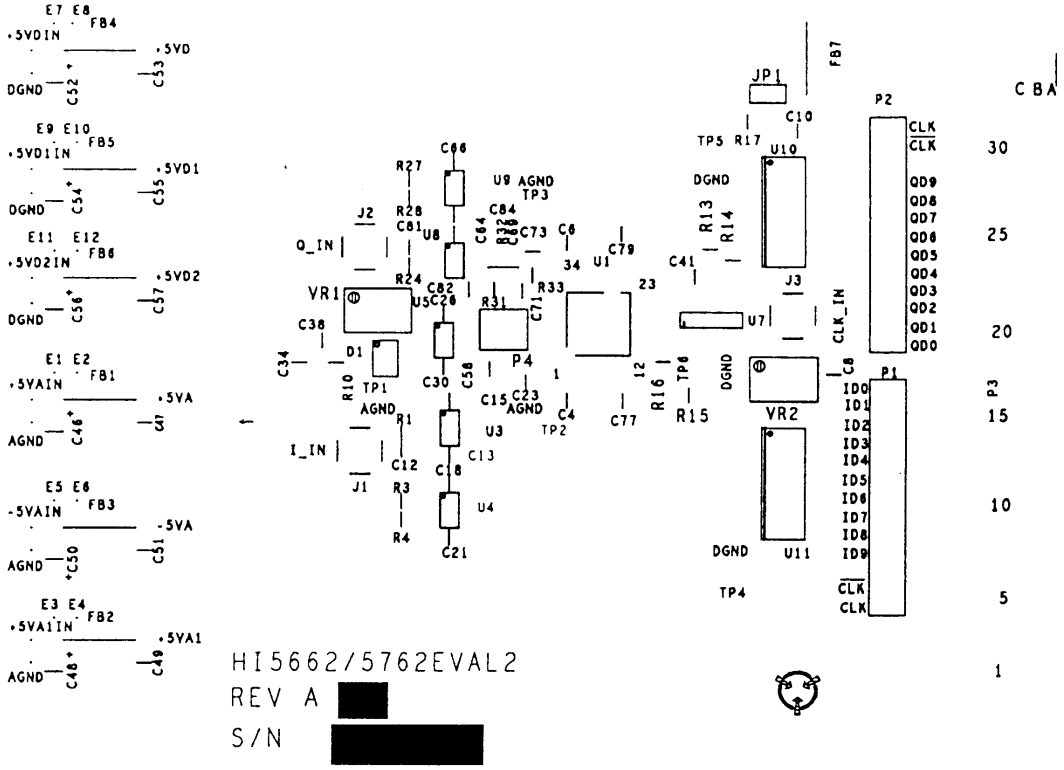


FIGURE 9. HI5762EVAL2 EVALUATION BOARD PARTS LAYOUT (NEAR SIDE)

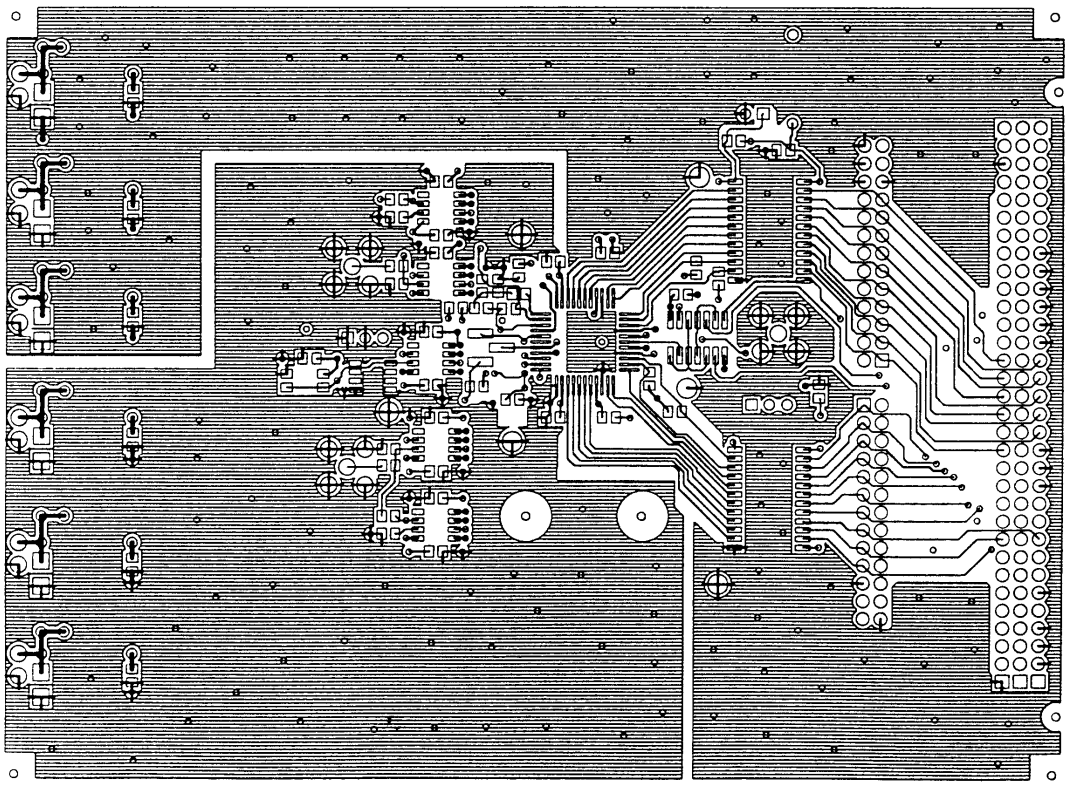


FIGURE 10. HI5762EVAL2 EVALUATION BOARD COMPONENT NEAR SIDE (LAYER 1)

Appendix A HI5762EVAL2 Board Layout (Continued)

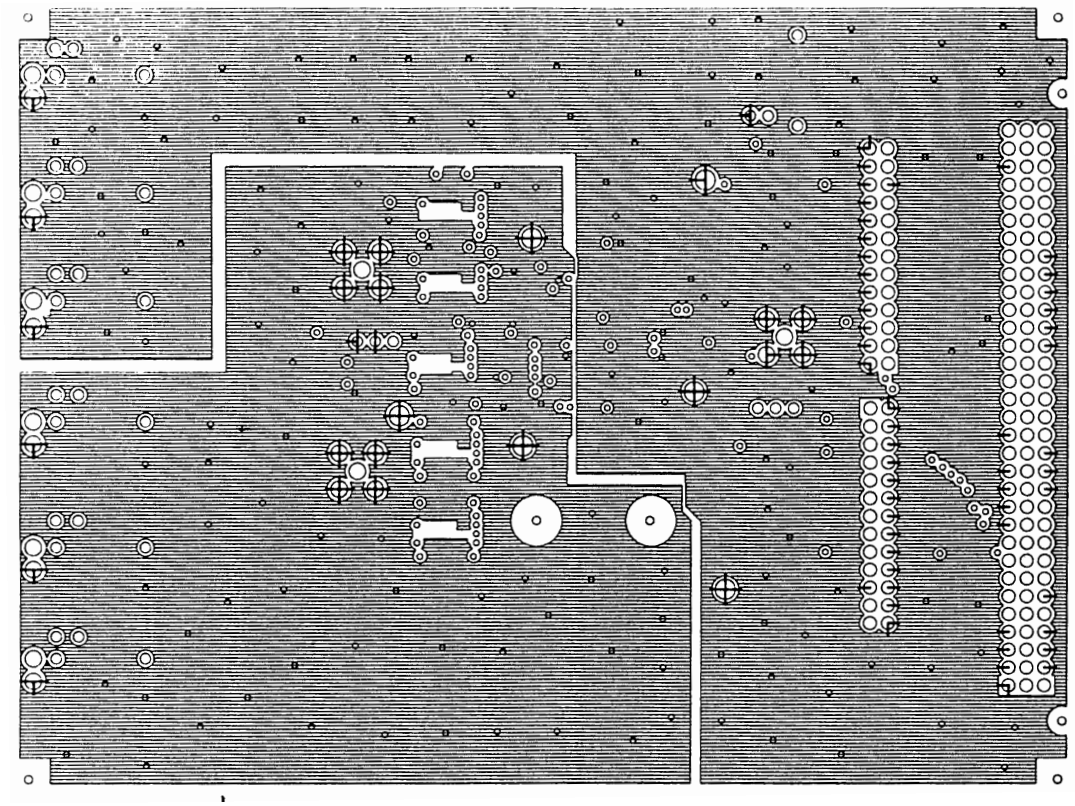


FIGURE 11. HI5762EVAL2 EVALUATION BOARD GROUND PLANE LAYER (LAYER 2)

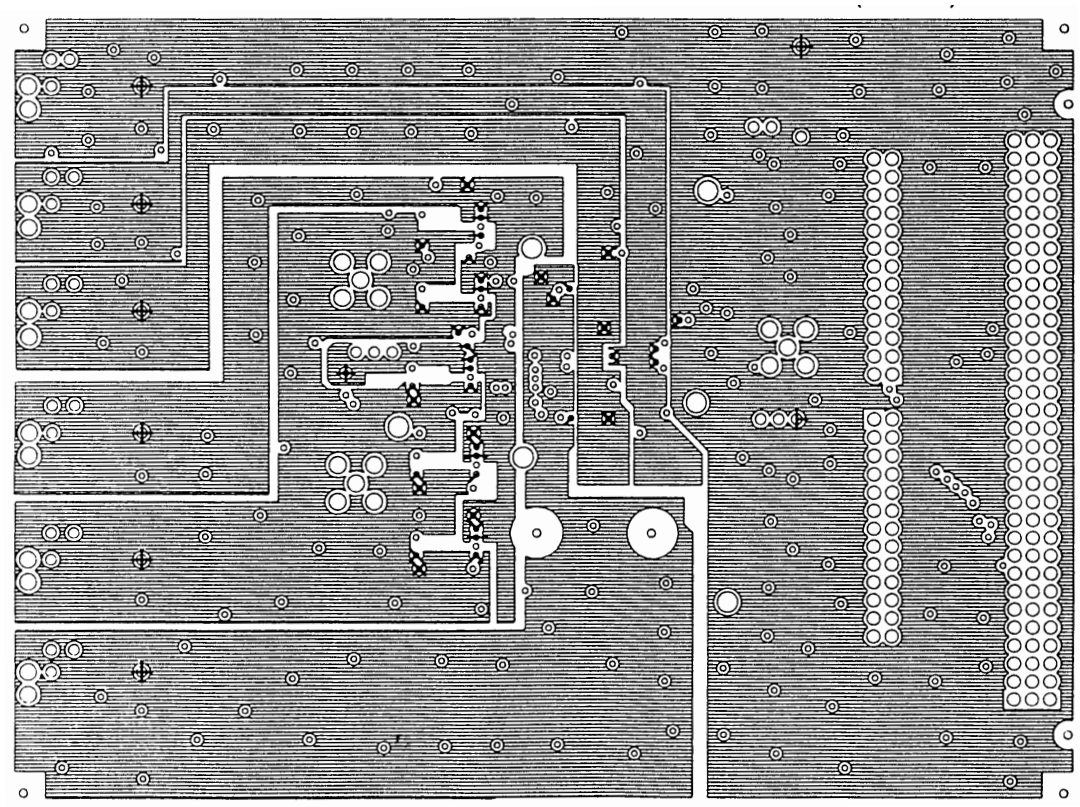


FIGURE 12. HI5762EVAL2 EVALUATION BOARD POWER PLANE LAYER (LAYER 3)

Appendix A HI5762EVAL2 Board Layout (Continued)

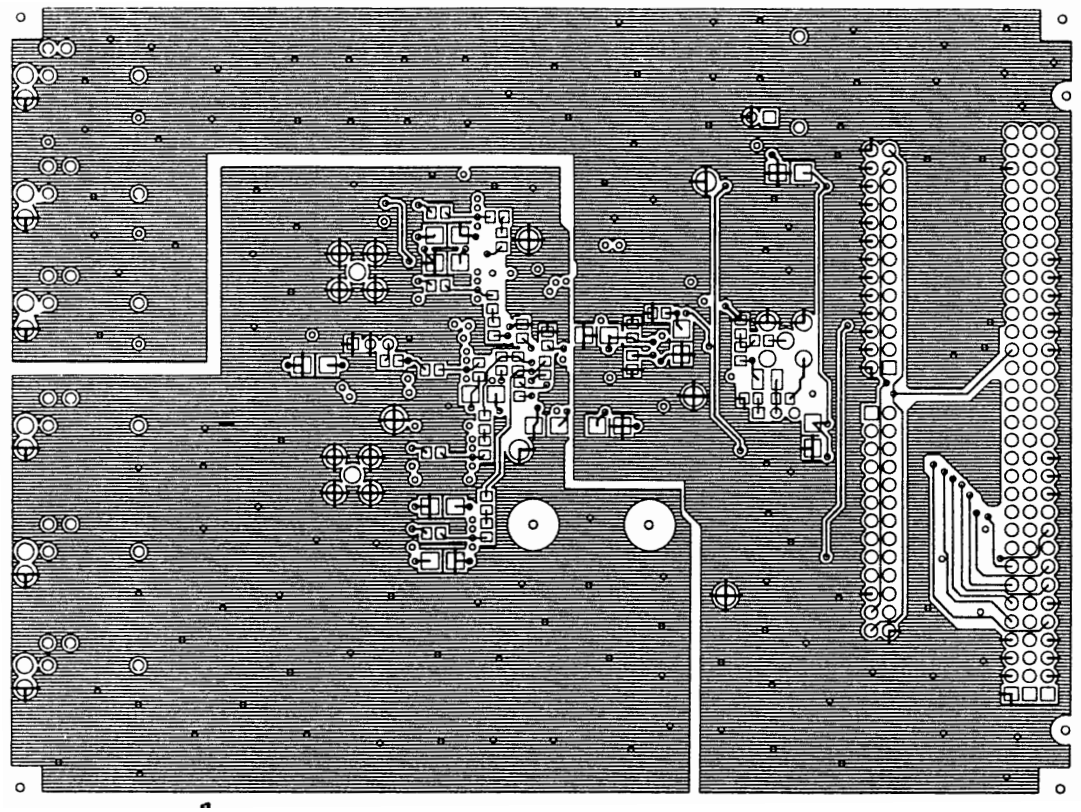


FIGURE 13. HI5762EVAL2 EVALUATION BOARD COMPONENT FAR SIDE (LAYER 4)

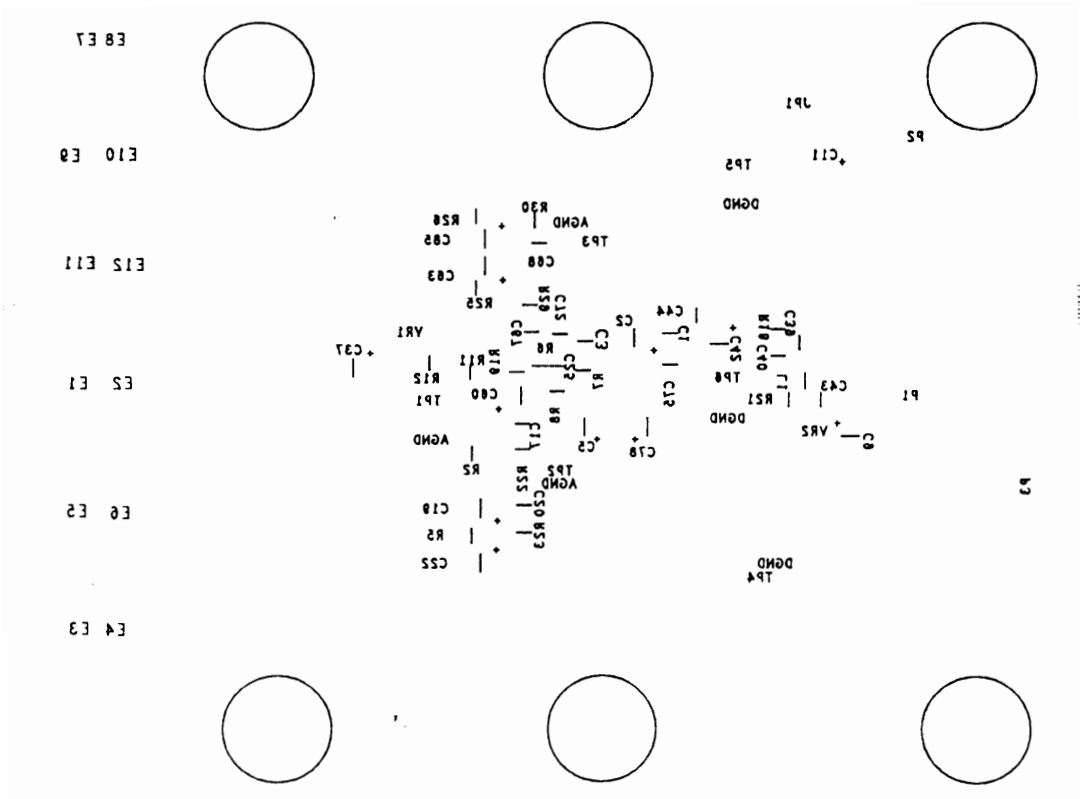


FIGURE 14. HI5762EVAL2 EVALUATION BOARD PARTS LAYOUT (FAR SIDE)

Appendix B HI5762EVAL2 Evaluation Board Schematic Diagrams

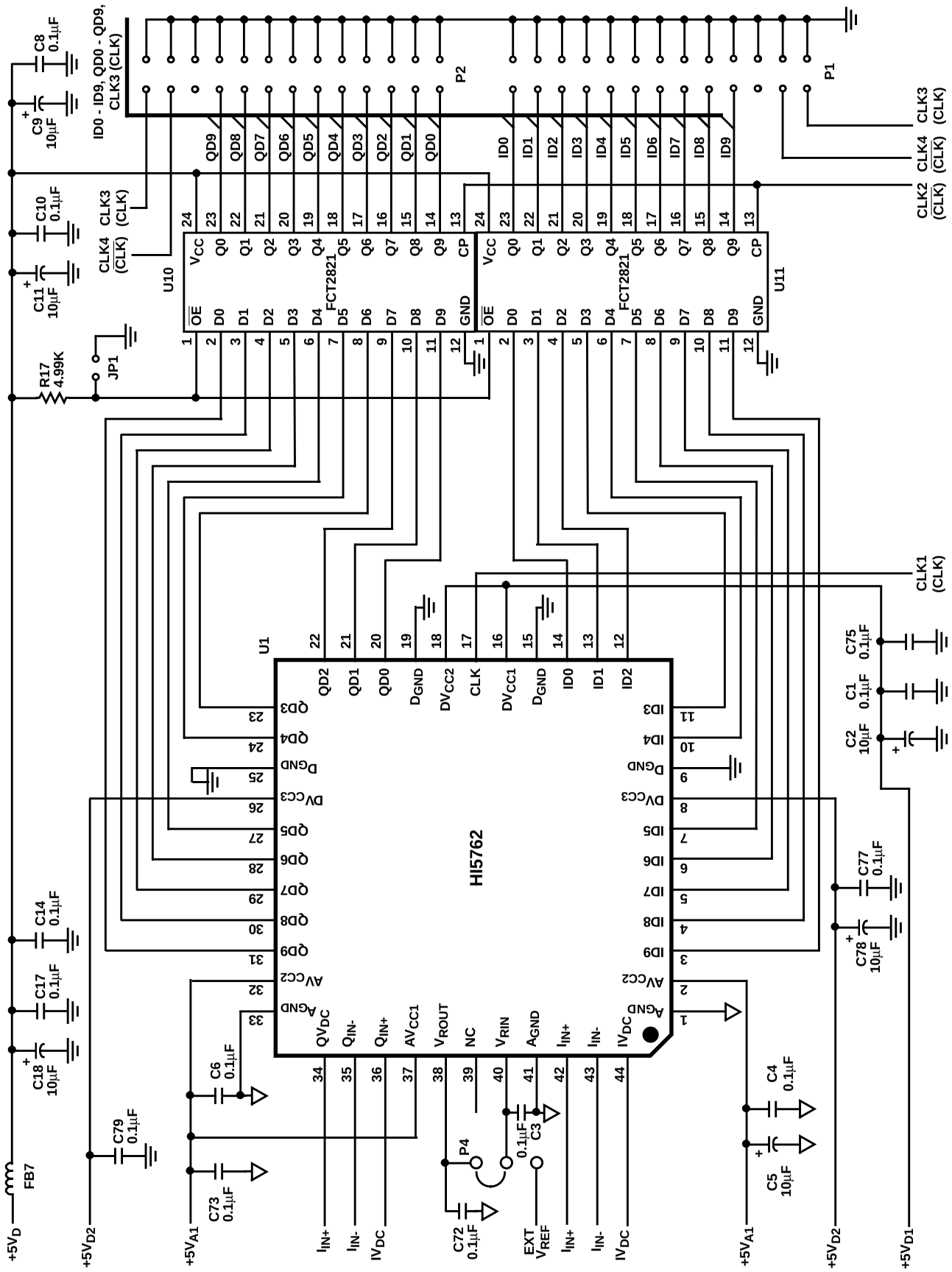


FIGURE 15. A/D CONVERTER AND DIGITAL DATA OUTPUT LATCHES/BUFFERS

Appendix B HI5762EVAL2 Evaluation Board Schematic Diagrams (Continued)

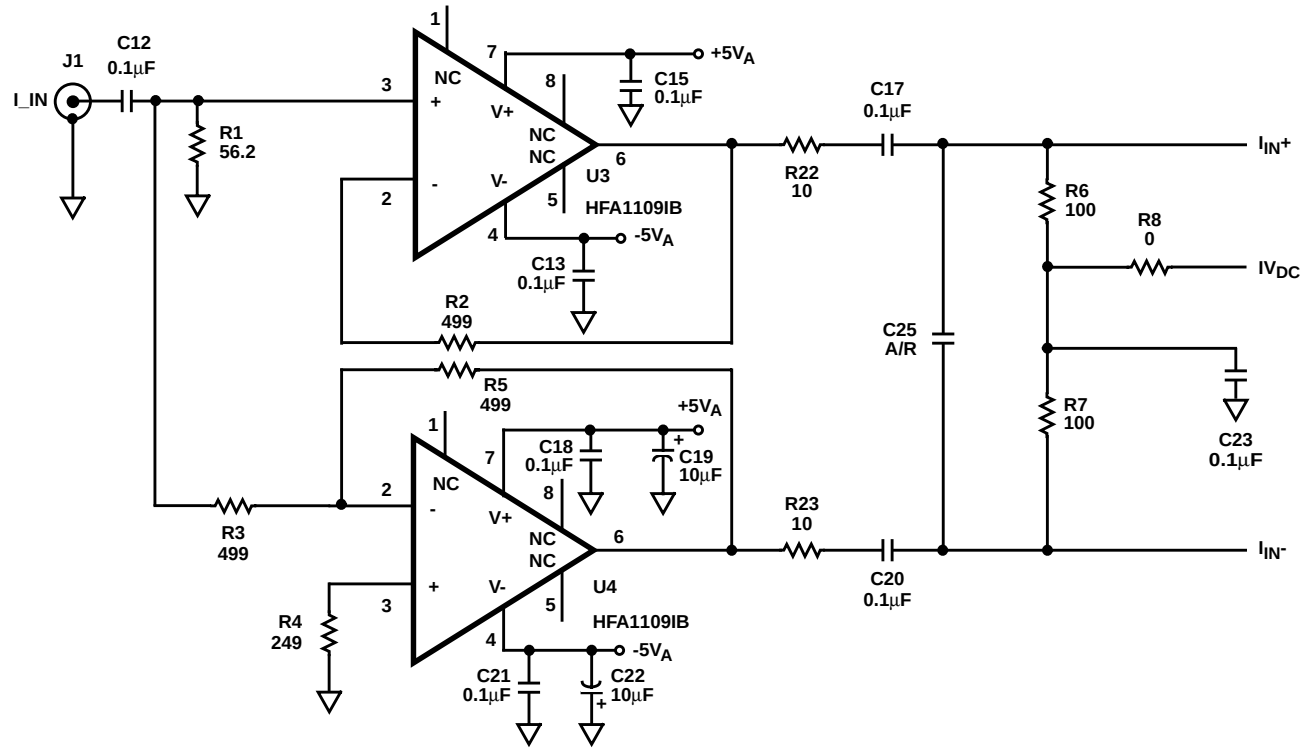


FIGURE 16. I CHANNEL ANALOG FRONT END

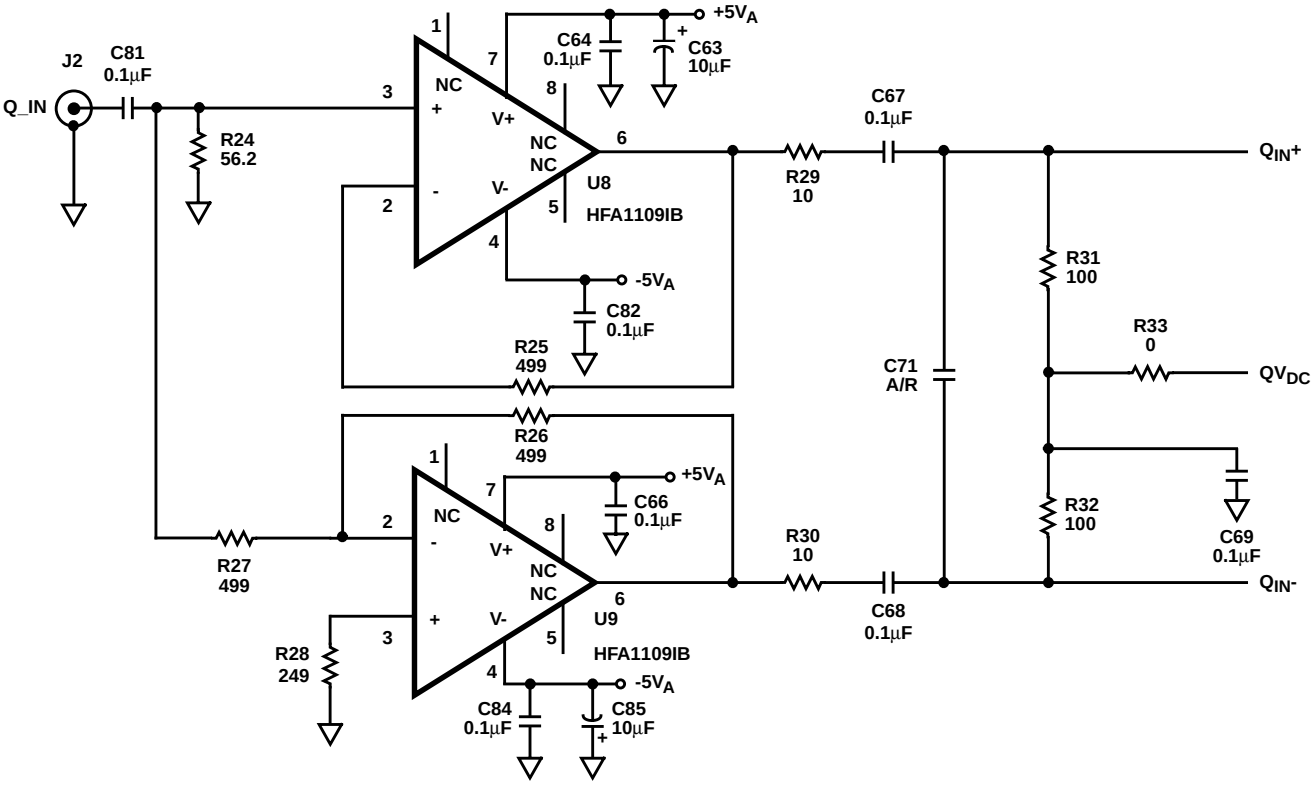


FIGURE 17. Q CHANNEL ANALOG FRONT END

Appendix B HI5762EVAL2 Evaluation Board Schematic Diagrams (Continued)

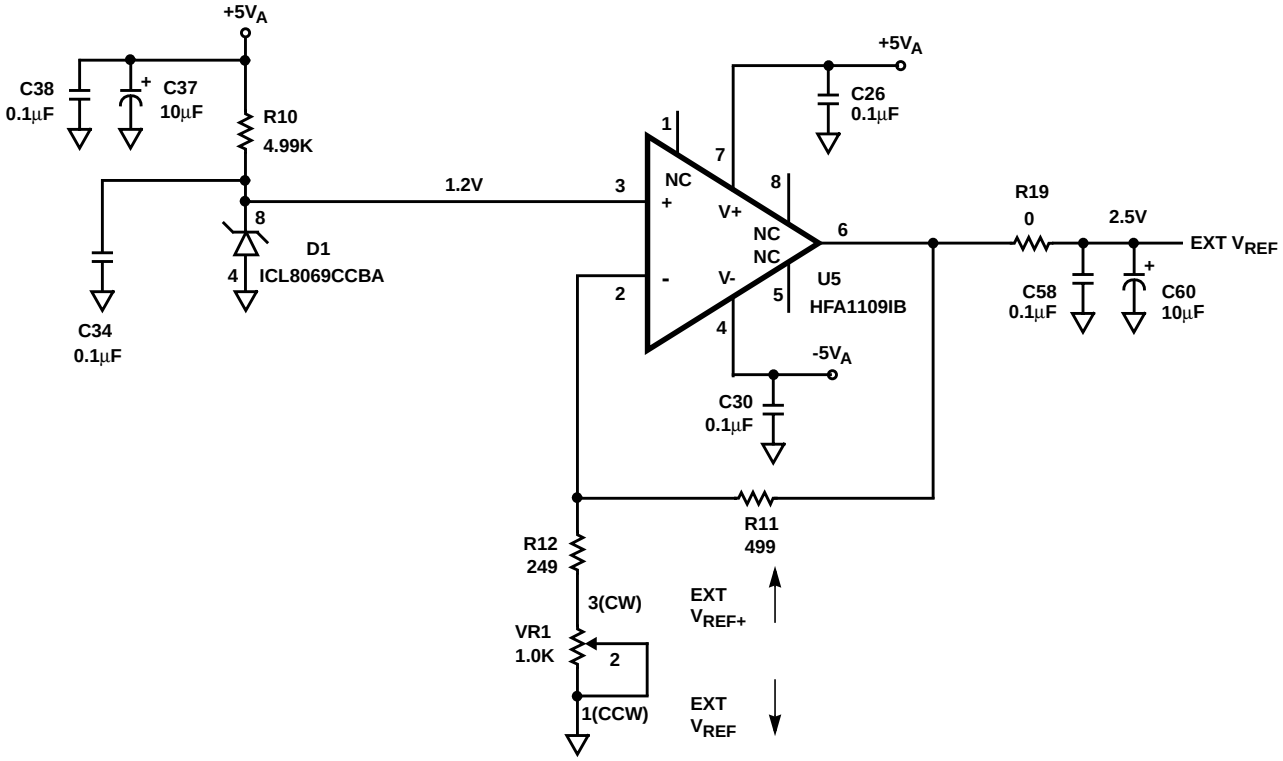


FIGURE 18. EXTERNAL REFERENCE VOLTAGE GENERATION CIRCUIT

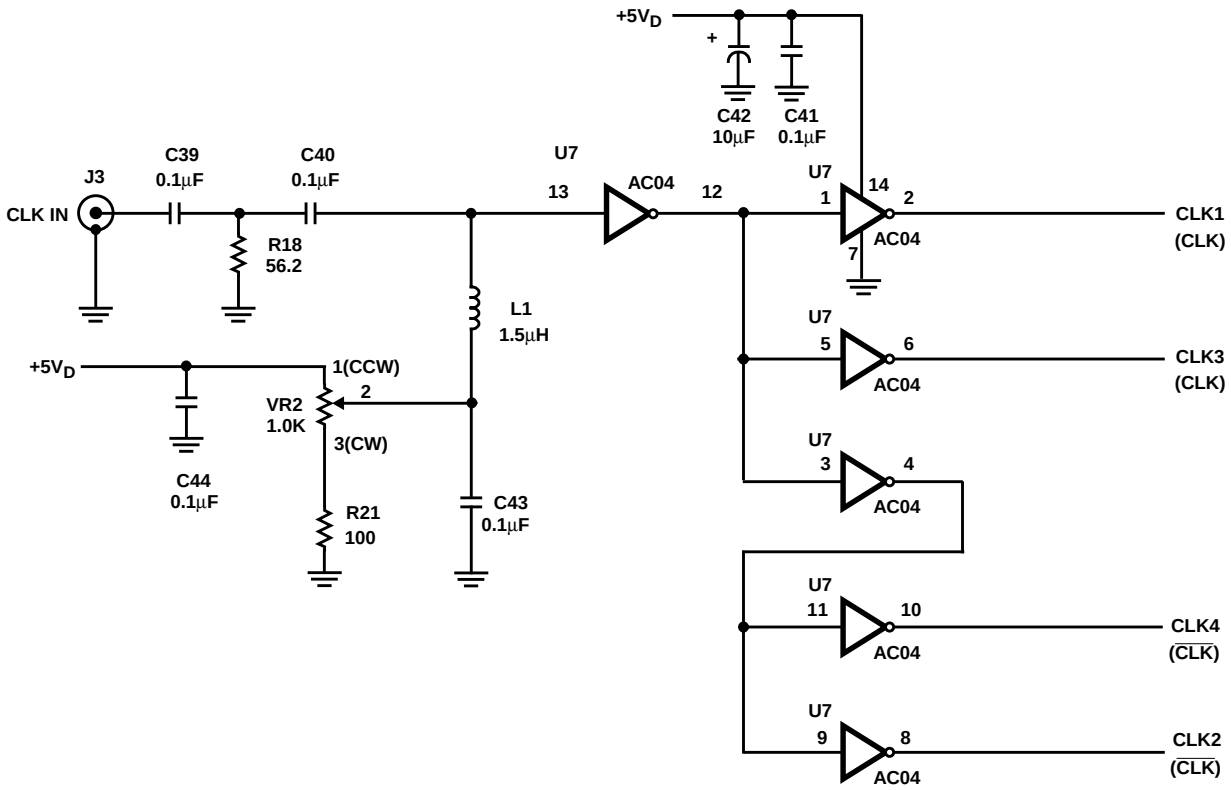


FIGURE 19. SAMPLE CLOCK DRIVER CIRCUIT

Appendix B HI5762EVAL2 Evaluation Board Schematic Diagrams (Continued)

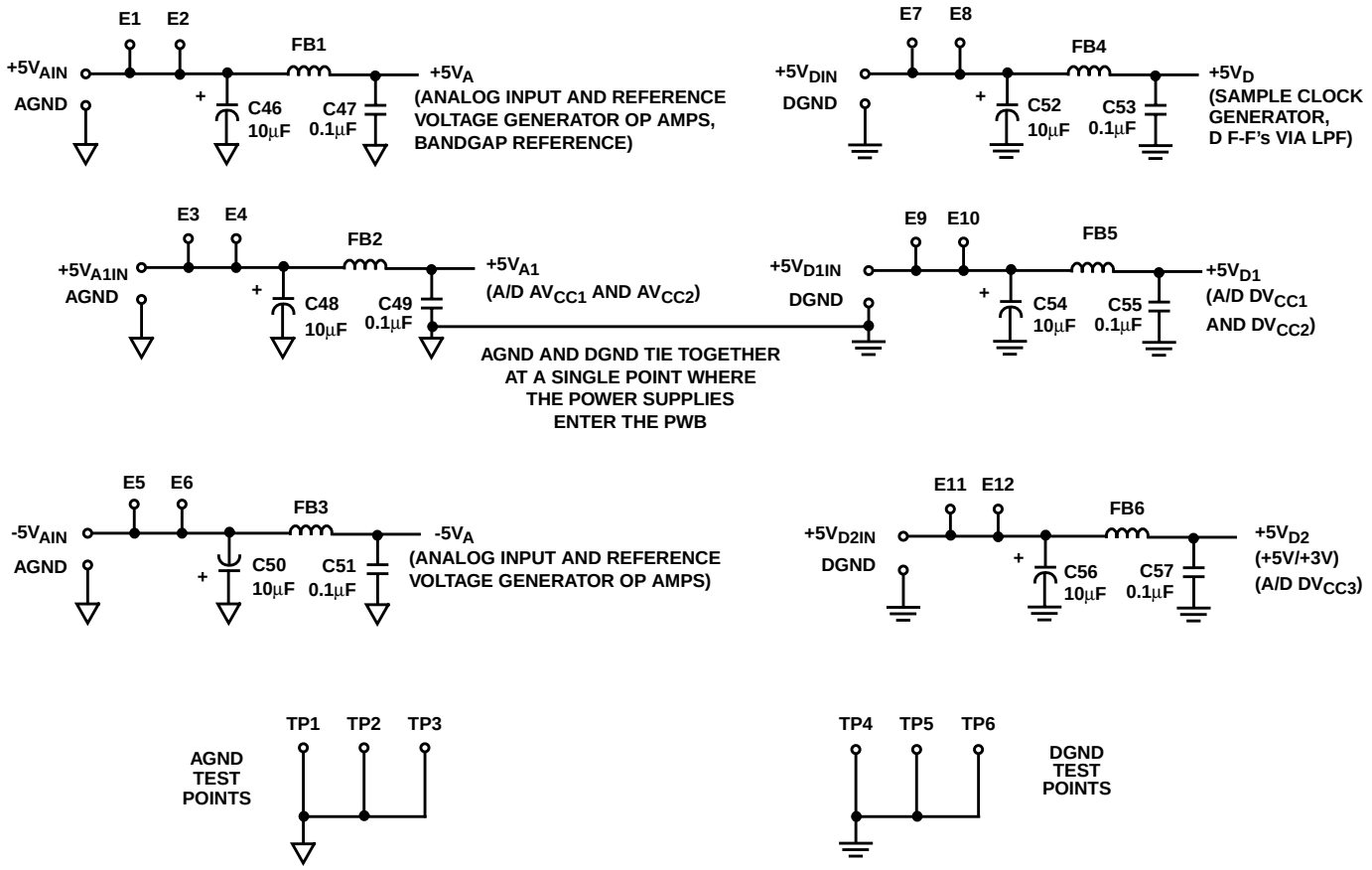


FIGURE 20. ANALOG AND DIGITAL POWER SUPPLIES

Appendix B HI5762EVAL2 Evaluation Board Schematic Diagrams (Continued)

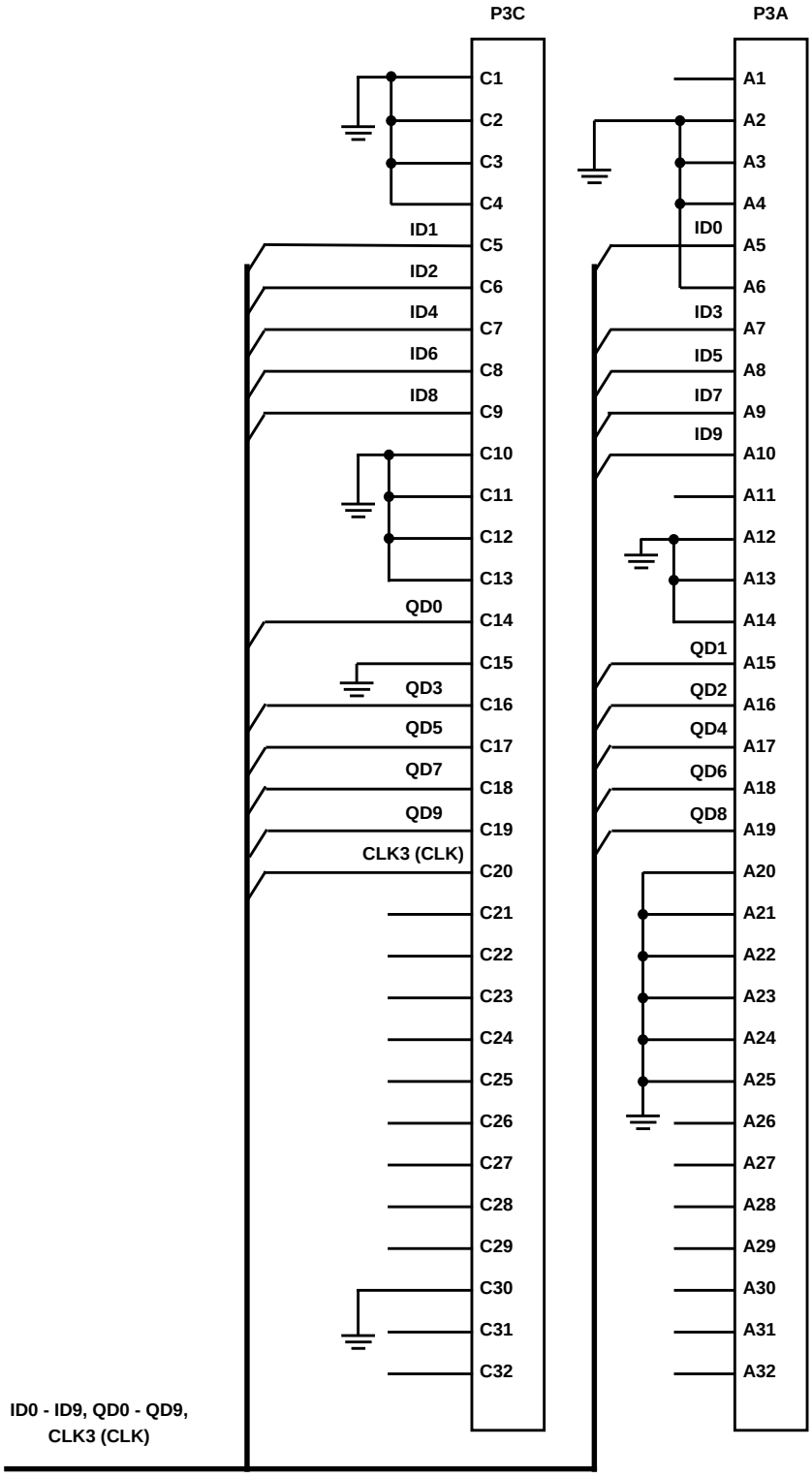


FIGURE 21. 96 PIN I/O CONNECTOR

Appendix C HI5762EVAL2 Evaluation Board Parts List

REFERENCE DESIGNATOR	QTY	DESCRIPTION
-	1	Printed Wiring Board
R2, 3, 5, 11, 25, 26, 27	7	499Ω, 1/10W 805 Chip, 1%
R1, 18, 24	3	56.2Ω, 1/10W 805 Chip, 1%
R22, 23, 29, 30	4	10Ω, 1/10W 805 Chip, 1%
R6, 7, 21, 31, 32	5	100Ω, 1/10W 805 Chip, 1%
R13, 14, 15, 16	4	22.1Ω, 1/10W 805 Chip, 1%
R8, 19, 33	3	0.0Ω, 1/4W 805 Chip, 5%
R10, 17	2	4.99kΩ, 1/10W 805 Chip, 1%
R4, 12, 28	3	249Ω, 1/10W 805 Chip, 1%
VR1, 2	2	1kΩ Trim Pot
C2, 5, 9, 11, 19, 22, 37, 42, 46, 48, 50,52, 54, 56, 60, 63, 78, 85	18	10µF Chip Tant Cap, 10WVDC, 20%, EIA Case B
C1, 3, 4, 6, 8, 10, 12, 13, 15, 17, 18, 20, 21, 23, 26, 30, 34, 38, 39, 40, 41, 43, 44, 47, 49, 51, 53, 55, 57, 58, 64, 66, 67, 68, 69, 72, 73, 75, 77, 79, 81, 82, 84	43	0.1µF Cer Cap, 50WVDC, 10%, 805 Case, Y5V Dielectric
C25, 71	2	A/R pF Cer Cap, 50WVDC, 10%, 805 Case
L1	1	1.5µH Chip Inductor, 1210 Case
FB1-7	7	10µH Ferrite Bead
J1, 2, 3	3	SMA Straight Jack PCB Mount
-	6	Protective Bumper
JP1	1	1x2 Header
JPH1	1	1x2 Header Jumper
P4	1	1x3 2mm Header
PH104	1	1x3 2mm Header Jumper
P1, 2	2	2x13 Heade
TP1, 2, 3, 4, 5, 6	6	Test Point
U1	1	Intersil HI5762IN Dual 10-Bi,t 60 MSPS A/D Converter with Internal Voltage Reference
U3, 4, 5, 8, 9	5	Intersil HFA1109IB 450MHz, Low Power, Current Feedback Video Operational Amplifier
U10, 11	2	Intersil CD74FCT2821BTM10-Bit Fast CMOS D-type Flip-flop
U7	1	Intersil CD74HC04M High Speed CMOS Logic Hex Inverter
D1	1	Intersil ICL8069CCBA Low Voltage Bandgap Reference
P3	1	64-Pin Eurocard RT Angle Receptacle

Appendix D HI5762 A/D Theory of Operation

The HI5762 is a dual 10-bit fully differential sampling pipeline A/D converter with digital error correction logic. Figure 22 depicts the circuit for the front end differential-in-differential-out sample-and-hold (S/H) amplifiers. The switches are controlled by an internal sampling clock which is a non-overlapping two phase signal, Φ_1 and Φ_2, derived from the master sampling clock. During the sampling phase, Φ_1, the input signal is applied to the sampling capacitors, C_S. At the same time the holding capacitors, C_H, are discharged to analog ground. At the falling edge of Φ_1 the input signal is sampled on the bottom plates of the sampling capacitors. In the next clock phase, Φ_2, the two bottom plates of the sampling capacitors are connected together and the holding capacitors are switched to the op amp output nodes. The charge then redistributes between C_S and C_H completing one sample-and-hold cycle. The front end sample-and-hold output is a fully-differential, sampled-data representation of the analog input. The circuit not only performs the sample-and-hold function but will also convert a single-ended input to a fully-differential output for the converter core. During the sampling phase, the I/QI_N pins see only the on-resistance of a switch and C_S. The relatively small values of these components result in a typical full power input bandwidth of 250MHz for the converter.

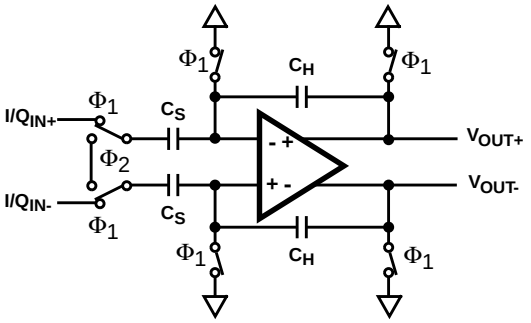


FIGURE 22. ANALOG INPUT SAMPLE-AND-HOLD

As illustrated in the functional block diagram and the timing diagram in Figures 23 and 24, eight identical pipeline subconverter stages, each containing a two-bit flash converter and a two-bit multiplying digital-to-analog converter, follow the S/H circuit with the ninth stage being a two bit flash converter. Each converter stage in the pipeline will be sampling in one phase and amplifying in the other clock phase. Each individual subconverter clock signal is offset by 180 degrees from the previous stage clock signal resulting in alternate stages in the pipeline performing the same operation.

The output of each of the eight identical two-bit subconverter stages is a two-bit digital word containing a supplementary bit to be used by the digital error correction logic. The output of each subconverter stage is input to a digital delay line which is controlled by the internal sampling clock. The function of the digital delay line is to time align the digital outputs of the eight identical two-bit subconverter stages with the corresponding output of the ninth stage flash converter before applying the eighteen bit result to the digital error correction logic. The digital error correction logic uses the supplementary bits to correct any error that may exist before generating the final ten bit digital data output of the converter.

Because of the pipeline nature of this converter, the digital data representing an analog input sample is output to the digital data bus following the 6th cycle of the clock after the analog sample is taken (see the timing diagram in Figure 24). This time delay is specified as the data latency. After the data latency time, the digital data representing each succeeding analog sample is output during the following clock cycle. The digital output data is provided in offset binary format.

Internal Reference Voltage Output, V_{REFOUT}

The HI5762 is equipped with an internal reference voltage generator, therefore, no external reference voltage is required. V_{ROUT} must be connected to V_{RIN} when using the internal reference voltage.

An internal band-gap reference voltage followed by an amplifier/buffer generates the precision +2.5V reference voltage used by the converter. A band-gap reference circuit is used to generate a precision +1.25V internal reference voltage. This voltage is then amplified by a wideband uncompensated operational amplifier connected in a gain-of-two configuration. An external, user-supplied, 0.1µF capacitor connected from the V_{ROUT} output pin to analog ground is used to set the dominant pole and to maintain the stability of the operational amplifier.

Reference Voltage Input, V_{REFIN}

The HI5762 is designed to accept a +2.5V reference voltage source at the V_{RIN} input pin. Typical operation of the converter requires V_{RIN} to be set at +2.5V. The HI5762 is tested with V_{RIN} connected to V_{ROUT} yielding a fully differential analog input voltage range of ±0.5V.

The user does have the option of supplying an external +2.5V reference voltage. As a result of the high input impedance presented at the V_{RIN} input pin, 1.25kΩ typically, the external reference voltage being used is only required to source 2mA of reference input current. In the situation where an external reference voltage will be used an external 0.1µF capacitor **must** be connected from the V_{ROUT} output pin to analog ground in order to maintain the stability of the internal operational amplifier.

In order to minimize overall converter noise it is recommended that adequate high frequency decoupling be provided at the reference voltage input pin, V_{RIN}.

Appendix D HI5762 A/D Theory of Operation (Continued)

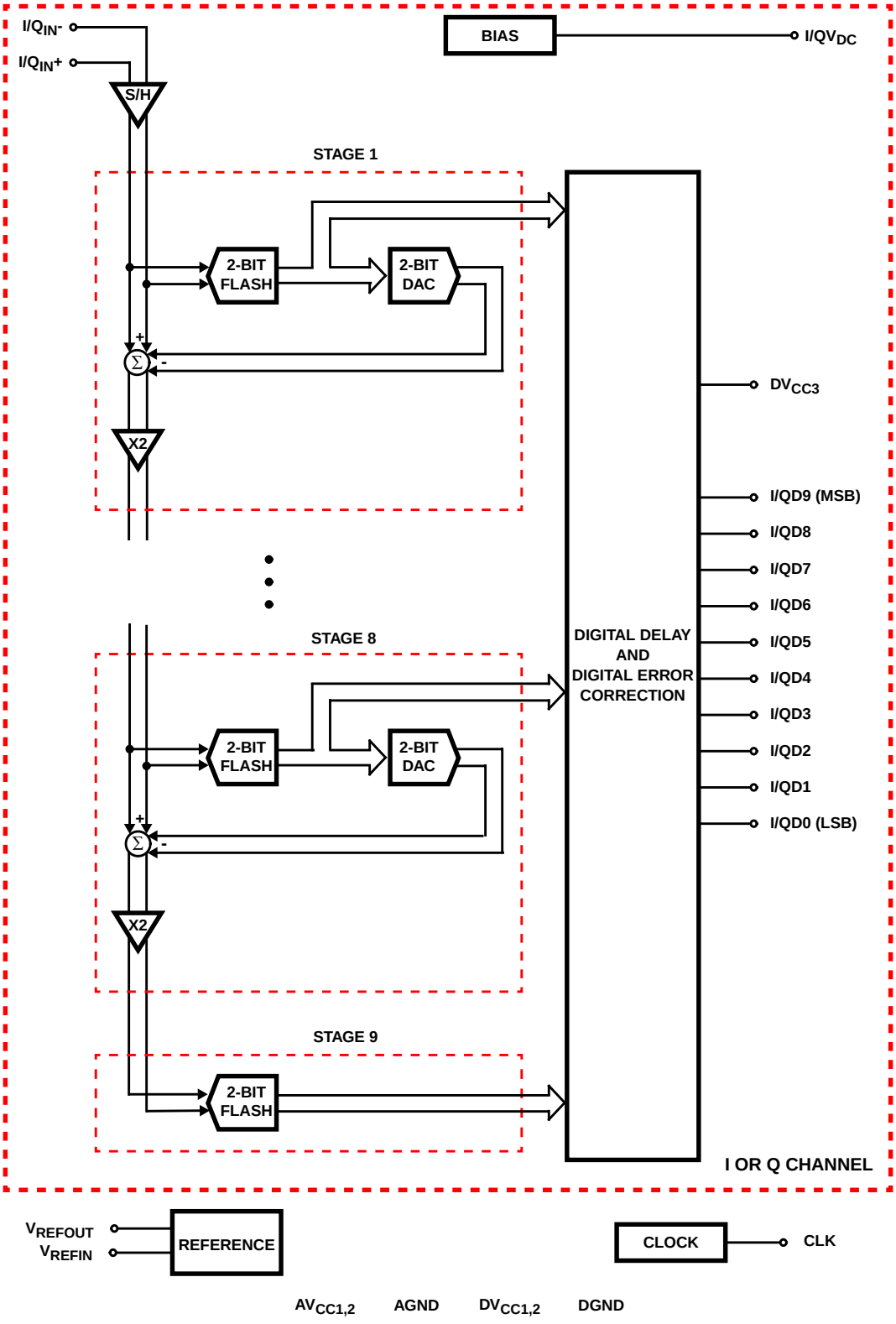
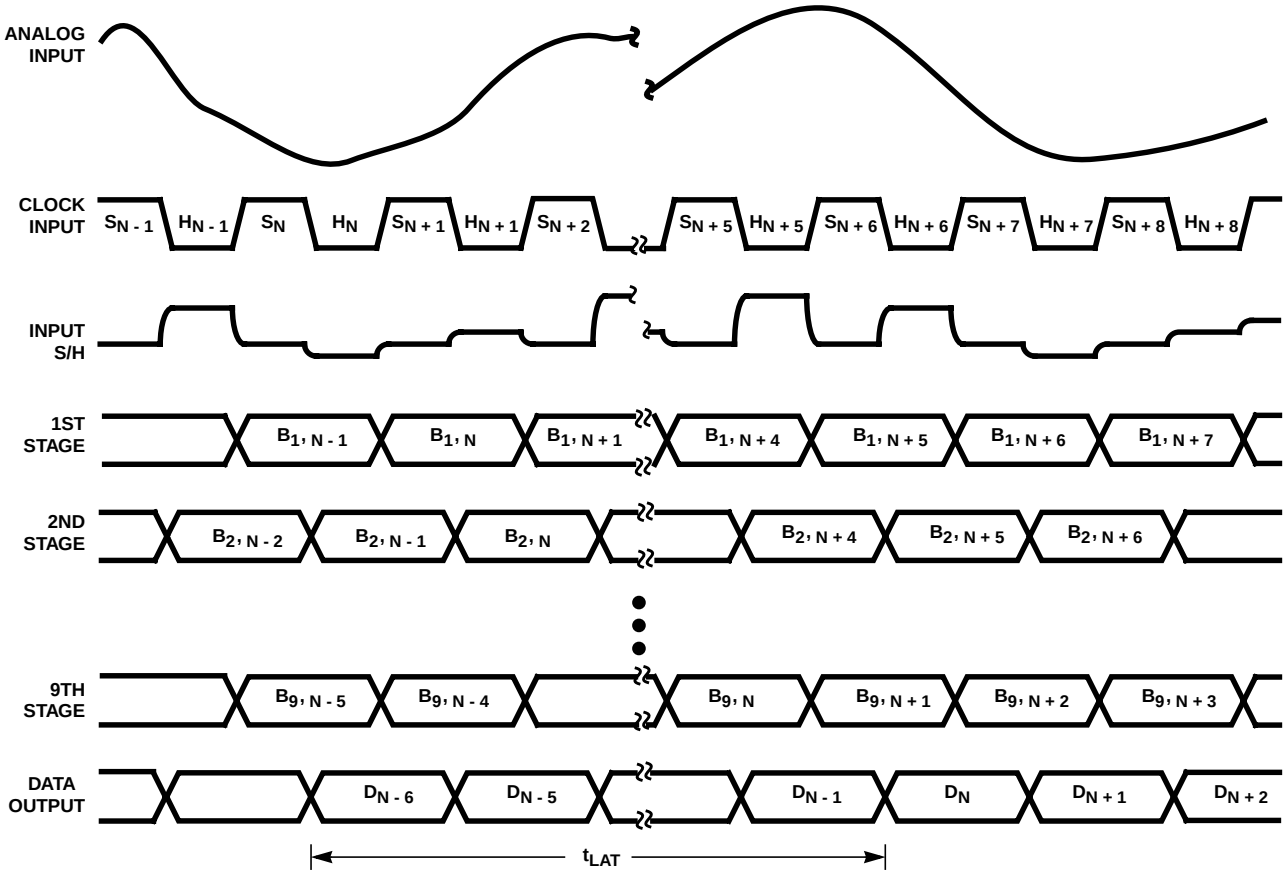


FIGURE 23. HI5762 FUNCTIONAL BLOCK DIAGRAM

Appendix D HI5762 A/D Theory of Operation (Continued)



NOTES:

1. S_N: N-th sampling period.
2. H_N: N-th holding period.
3. B_M, N: M-th stage digital output corresponding to the N-th sampled input.
4. D_N: Final data output corresponding to N-th sampled input.

FIGURE 24. HI5762 INTERNAL CIRCUIT TIMING

Appendix E HI5762 Pin Descriptions

PIN NO.	NAME	DESCRIPTION
1	A_{GND}	Analog Ground
2	AV_{CC2}	Analog Supply (+5.0V)
3	ID9	I-Channel, Data Bit 9 Output (MSB)
4	ID8	I-Channel, Data Bit 8 Output
5	ID7	I-Channel, Data Bit 7 Output
6	ID6	I-Channel Data Bit 6 Output
7	ID5	I-Channel, Data Bit 5 Output
8	DV_{CC3}	Digital Output Supply (+3.0V or +5.0V)
9	D_{GND}	Digital Ground
10	ID4	I-Channel, Data Bit 4 Output
11	ID3	I-Channel, Data Bit 3 Output
12	ID2	I-Channel, Data Bit 2 Output
13	ID1	I-Channel, Data Bit 1 Output
14	ID0	I-Channel, Data Bit 0 Output (LSB)
15	D_{GND}	Digital Ground
16	DV_{CC1}	Digital Supply (+5.0V)
17	CLK	Sample Clock Input
18	DV_{CC2}	Digital Supply (+5.0V)
19	D_{GND}	Digital Ground
20	QD0	Q-Channel, Data Bit 0 Output (LSB)
21	QD1	Q-Channel, Data Bit 1 Output
22	QD2	Q-Channel, Data Bit 2 Output

PIN NO.	NAME	DESCRIPTION
23	QD3	Q-Channel, Data Bit 3 Output
24	QD4	Q-Channel, Data Bit 4 Output
25	D_{GND}	Digital Ground
26	DV_{CC3}	Digital Output Supply (+3.0V or +5.0V)
27	QD5	Q-Channel, Data Bit 5 Output
28	QD6	Q-Channel, Data Bit 6 Output
29	QD7	Q-Channel, Data Bit 7 Output
30	QD8	Q-Channel, Data Bit 8 Output
31	QD9	Q-Channel, Data Bit 9 Output (MSB)
32	AV_{CC2}	Analog Supply (+5.0V)
33	A_{GND}	Analog Ground
34	QV_{DC}	Q-Channel DC Bias Voltage Output
35	Q_{IN-}	Q-Channel Negative Analog Input
36	Q_{IN+}	Q-Channel Positive Analog Input
37	AV_{CC1}	Analog Supply (+5.0V)
38	V_{ROUT}	+2.5V Reference Voltage Output
39	NC	No Connect
40	V_{RIN}	+2.5V Reference Voltage Input
41	A_{GND}	Analog Ground
42	I_{IN+}	I-Channel Positive Analog Input
43	I_{IN-}	I-Channel Negative Analog Input
44	IV_{DC}	I-Channel DC Bias Voltage Output