ISL6558EVAL2

Low-Profile, 5V/12V Input, 500kHz, and 90% Efficiency DC/DC Converter

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Introduction

The changing computer performance landscape has brought about the need for flexible power solutions. Peripheral performance continues to increase as higher speed bus interfaces are made available. Router designs continue to grow in complexity as on-board processors perform more functions within a limited board space while continuing to increase the speed of data transfer. This places higher power density requirements on the DC/DC converters which supply them.

Intersil's Endura™ multi-phase controllers (HIP63xx and ISL65xx) and synchronous-rectified buck MOSFET drivers (HIP66xx and ISL66xx) are suitable for the interleaved DC/DC buck converter implementation, as shown in Figure 1, and provide superior performance solutions with their space economical MLFP packages.

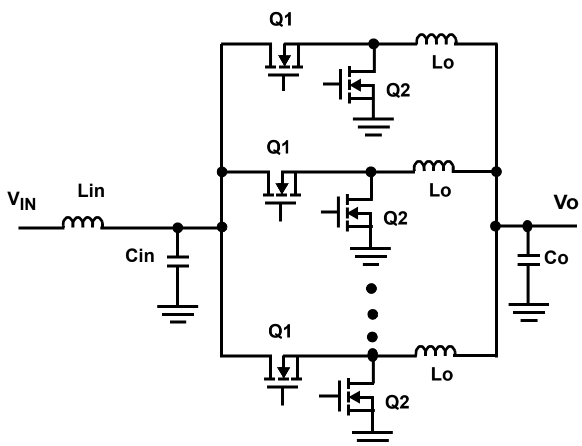


FIGURE 1. MULTI-PHASE INTERLEAVED BUCK CONVERTER

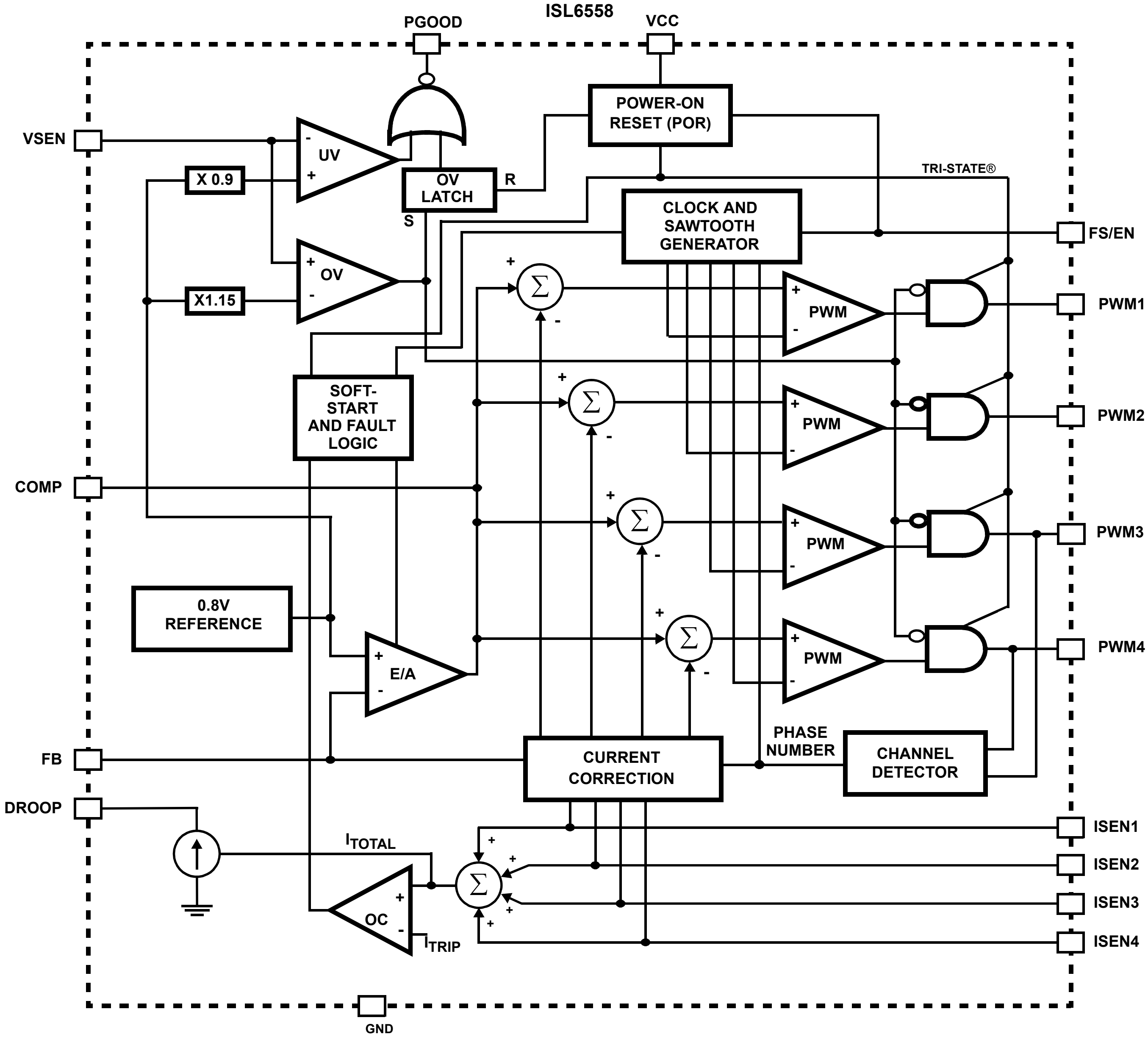
This application note first gives a brief introduction of Intersil's four-phase controller ISL6558 and synchronous-rectified driver ISL6609. A summary of the ISL6558 and ISL6609 based design follows. The experimental results for a low-profile 5V-to-1.35V@30A, 500kHz, and 90% efficiency converter in two-phase operation using the interleaved approach and with their space economical MLFP package ICs are discussed. The evaluation board can be pushed up to 80A in four-phase operation, or modified for 12V input applications by replacing the input capacitors with higher voltage rating capacitors. Term Definitions, Reference, Schematics, Bill of Materials, and Layout are included at the end of this application note.

Intersil's ISL6558 and ISL6609

The ISL6558 controller, coupled with ISL6609 single-channel driver ICs, forms the basic building blocks for applications which demand high current, rapid load transient response, and high efficiency performance at high switching frequency within a limited board area and height.

The ISL6558 regulates output voltage and balances load currents for two to four synchronous-rectified buck converter channels; its internal structure is shown in Figure 2. The internal 0.8V reference allows output voltage selection down to that level with a 1% system accuracy over temperature. The current-channel balance loop provides good thermal balance among all phases. Output voltage droop or active voltage positioning is optional. Overvoltage and overcurrent monitors and protection functions of the IC provide a safe environment for the microprocessor or other load. The controller is available in a 16-lead SOIC package and a 5x5mm^2 20-lead MLFP package with some space savings. For more detailed descriptions of the ISL6558 functionality, refer to the device datasheet [1].

The ISL6609 is a 5V driver IC capable of delivering up to 4A of gate current for rapidly switching both MOSFETs in a synchronous-rectified bridge; its internal structure is shown in Figure 2. It is especially designed for voltage regulators that require high efficiency performance at high switching frequency within a limited board space. The ISL6609 accepts a single logic input to control both upper and lower MOSFETs. Its Tri-State® feature, working together with Intersil's Multi-Phase PWM controllers, helps prevent a negative transient on the output voltage when the output is being shut down. This eliminates the Schottky diode that is used in some systems for protecting the microprocessor from reversed-output-voltage damage. Furthermore, adaptive shoot-through protection is implemented on both switching edges to provide optimal dead time and minimize conduction losses. Bootstrap circuitry permits greater enhancement of the upper MOSFET. The driver is available in a 8-lead SOIC package and a space economical 3x3mm^2 8-lead MLFP package. For a more detailed description of the ISL6609, refer to the device data sheet [2].



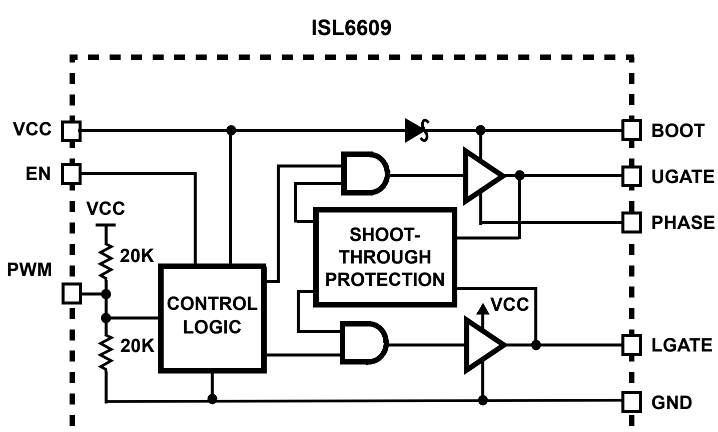


FIGURE 2. SIMPLIFIED ISL6558 AND ISL6609 INTERNAL STRUCTURE

Summary of Design

Table 1 summarizes the specifications of a power converter for mid-range router applications. The ISL6558 and ISL6609 based evaluation board has been designed to meet these criteria.

TABLE 1. ISL6558EVAL2 SPECIFICATIONS

PARAMETER	CONDITION	MIN	TYP	MAX
Input Voltage	VIN	4.5V	5V	5.5V
Output Regulation	0.1% R16 and R19	1.336	1.35	1.365
Transient Regulation	6.5A Step 200A/µs	Vo - 20mV		Vo + 20mV
Continuous Load	25°C with 200LFM		30A	
Transient Slew Rate			200A/µs	
Over Current	25°C with 200LFM		43A	
Minimum Airflow			0 LFM	
Channel Switching Frequency			500kHz	
Efficiency	25°C with 200LFM		89.7%	
	25°C with No Airflow		89.3%	
Undervoltage Rising Threshold			0.92Vo	
Undervoltage Falling Threshold			0.9Vo	
Overvoltage Threshold			1.15Vo	

Table 2 shows the calculation results of critical design parameters for the reference design, a two-phase interleaved DC/DC buck converter.

TABLE 2. CRITICAL DESIGN PARAMETERS

PARAMETER	CONDITIONS	VALUE	UNIT
DUTY CYCLE AND SWITCHING FREQUENCY			
D	V_{IN} = 5, Vo = 1.35	28.3	%
Fsw	RT = 51.1kΩ (measured)	500	kHz
INPUT INDUCTOR AND CAPACITORS			
Cin (min)	Io = 30A, N = 2, $\Delta V_{IN,CAP}$ = 20mV	180	µF
$I_{IN,RMS}$	V_{IN} = 5.5V, Io = 30A	7.63	A
Lin (min)	Cin = 180µFx3, dIin/dt = 0.1A/µs	300	nH
OUTPUT CAPACITORS			
Co(min)	f_c = Fsw/5 = 100kHz, f(Istep) = 20mV	517	µF
Io_{RMS}	Lo(Io) = 0.3µH, V_{IN} = 5.5V	1.34	A
ESR(max)	Istep = 6.5A, f(step) = 20mV	3.07	mΩ

TABLE 2. CRITICAL DESIGN PARAMETERS (Continued)

PARAMETER	CONDITIONS	VALUE	UNIT
OUTPUT INDUCTORS (ASSUMING EQUAL DISTRIBUTION AMONG OUTPUT INDUCTORS)			
$I_{Lo,PP}$	Lo(Io) = 0.3µH, V_{IN} = 5.5V	6.88	A
I_{PP}	Lo(Io) = 0.3µH, V_{IN} = 5.5V, N = 2	4.65	A
$I_{Lo,Peak}$	Lo(Io) = 0.3µH, V_{IN} = 5.5V	18.44	A
$I_{Lo,RMS}$	Lo(Io) = 0.3µH, V_{IN} = 5.5V	15.13	A
UPPER FETs			
$I_{Q1,RMS}$	Lo(Io) = 0.3µH, V_{IN} = 4.5V	8.48	A
LOWER FETs			
$I_{Q1,RMS}$	Lo(Io) = 0.3µH, V_{IN} = 5.5V	13.04	A

Table 3 summarizes a rough power dissipation analysis for the referenced design.

TABLE 3. FULL-LOAD POWER DISSIPATION BUDGET

ELEMENTS	POWER DISSIPATION AT 30A LOAD		
	4.5V	5.0V	5.5V
CALCULATION CONDITIONS			
Switching Frequency	500kHz		
Per-Channel Output Inductor	0.3µH at Full load		
Number of Active Channels	N = 2		
PER-CHANNEL LOSSES (xN)			
Upper FETs Conduction	0.395W	0.356W	0.323W
Upper FETs Switching	0.461W	0.516W	0.572W
Lower FETs Conduction	0.333W	0.328W	0.340W
Lower FETs Body-diode Conduction	0.233W	0.232W	0.231W
Output Inductor Copper	0.123W	0.123W	0.123W
Output Inductor Core (Estimated)	0.036W	0.0.036W	0.036W
Per-Channel Driver	0.305W	0.375W	0.454W
OTHERS (x1)			
Input Inductors Copper	0.055W	0.044W	0.037W
Input Inductors Core	Negligible		
Input Capacitors	0.273W	0.287W	0.291W
Output Capacitors	0.0035W	0.0048W	0.0061W
Controller	0.078W	0.078W	0.078W
PCB Copper	0.196W	0.184W	0.176W
Miscounted and Error	0.32W	0.28W	0.29W
TOTAL	**4.655W**	**4.688W**	**4.737W**

Experimental Results

The ISL6558EVAL2 evaluation board as configured is capable of 30A continuous load current and handling 200A/µs or higher speed load transients. The evaluation board meets the design specifications indicated in Table 1. Table 4 summarizes the equipment that was used for the performance evaluation.

TABLE 4. EQUIPMENT LIST

Equipment	EQUIPMENT DESCRIPTIONS
Boards Used	ISL6558EVAL2 Rev. A, #1 and #2
Power Supplies	1. Hewlett Packard 6653A, 35V, 15A. S/N: 3621A-03425
Oscilloscope	LeCroy LT364L. S/N: 01106
Multimeters	Fluke 8050A. S/N: 2466115 & 3200834
Load	1. Chroma 63103. S/N: 631030002967 2. Chroma 63103. S/N: 631030003051
Current Probe Amplifier	LeCroy AP015. SN: 3293
Fan	POPST-MOOREN TYP 4600X (4098547)

ISL6558EVAL2 OPERATION AND MODIFICATION TIPS

- Apply the input voltage (VIN) prior to the control voltage VCC5 (5V). This sequencing results in initializing the ISL6609 driver before the ISL6558 starts, and retains the soft-start interval. Vice versa, the ISL6558 could produce maximum duty cycle PWM drive signal, which results in an overcurrent or overvoltage trip due to lack of soft-start. The evaluation board is configured to power up from a single 5V supply, and it eliminates the problem discussed above.
- SW1 is used to engage or remove the load transient generator.
- Droop option is not selected in the reference design since the required load transient step is not greater than 50% of the full load. In another word, the droop only helps reduce the number of output capacitors and still retains the same transient performance when the load transient step is greater than 50% of full load.
- For 3-phase operation, add the current sense resistor R17 and place JP4 to ON position (away from TP8). The compensation gain (R11) should be scaled by 2/3 for system stability with a reasonable phase margin.
- For 4-phase operation, add the current sense resistors R2 & R17 and place JP4 &JP2 to ON position (away from TP8 and TP5). The compensation gain (R11) should be scaled by 1/2 for system stability with a reasonable phase margin.
- Use R25, R26, R28, and R29 to program the load transient speed. The higher values these resistors, the slower the transient.
- If there is sufficient airflow, use a single LPAK Hitachi HAT1264 for the upper FET and two SO-8 Siliconix Si4842DYs for the lower FETs in each channel; but it comes with the penalty of 1% lower efficiency, as shown in Table 5. Note that the current sense resistors (R2 and R17) need to be adjusted to get a proper over current setpoint.
- For 12V input operation, the jumper JP1 should be removed to prevent the controller and drivers from overvoltage damage. A 5V supply is required to power up the controller and the drivers; the diode D1 is to protect both the drivers and controller from reversed-bias damage. The 12V supply should be applied prior to the 5V; otherwise, the output voltage will lack soft-start and cause an over overcurrent or overvoltage at the output. Furthermore, the input capacitors should be replaced with higher voltage rating (16V or above) capacitors. In addition, the compensation gain (R11) should be scaled by 5/12 for system stability with a reasonable phase margin.
- Any change of the output filter will require the compensation network to change for an optimum transient response. If very lower ESR capacitors are used at the output, a type III compensation network is required to boost up the phase for a better transient performance.
- The feedback resistor (R19) can cause some delay in the soft-start interval, as discussed in the ISL6557A data sheet section SOFT-START [3]. It should not be a very high impedance resistor.

EFFICIENCY

The efficiency data, as plotted in Figure 3, are taken with a PAPST-MOTOREN TYP 4600X fan turned on 8” away from the input end of the evaluation board at room temperature (approximate 200LFM). This figure shows that the converter operates less efficiently at high line and low-to-medium load since the switching loss is the dominant portion of the total losses in that operating condition. As the load increases, the dominant conduction losses help cut down the difference.

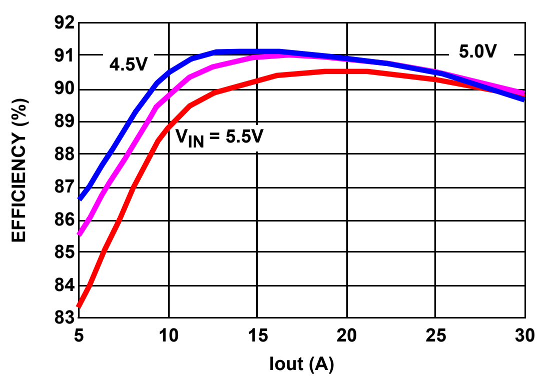


FIGURE 3. EFFICIENCY AT 500kHz AND 200LFM

Figure 4 shows the efficiency for various frequencies and airflow conditions.

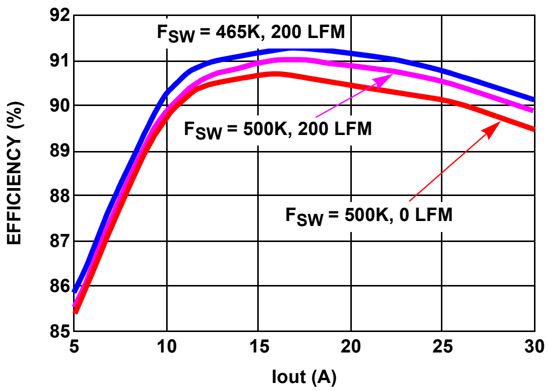


FIGURE 4. EFFICIENCY FOR VARIOUS FREQUENCY AND AIRFLOW AT V_{IN}=5V

Different combinations of upper and lower MOSFETs have been evaluated at Vin = 5V and Fsw = 500kHz with 200LFM airflow, as shown in Table 5. The last combination with one Hitachi HAT2164 upper FET and two Siliconix Si4842DY lower FETs provides high efficiency and good thermal performance with some space and cost reduction.

TABLE 5. EFFICIENCY WITH DIFF. UPPER & LOWER MOSFETs

#	UPPER FET	LOWER FET	EFFICIENCY
1	HAT2168 x2	HAT2164 x2	89.85%
2	HAT2168 x1	HAT2164 x2	87.94%
3	HAT2168 x2	Si4842DY x2	89.50%
4	HAT2164 x1	Si4842DY x2	88.90%

OUTPUT SOFT-START AND TURN-OFF

As the control voltage VCC5 reaches the POR rising threshold (4.38V nominal) of the ISL6558, the FS/EN pin is released from ground; the output begins a monotonic rise comprised of 2048 digital steps, as shown in Figure 4. At the end of the soft-start interval, the PGOOD signal transitions to indicate the output voltage is within specification.

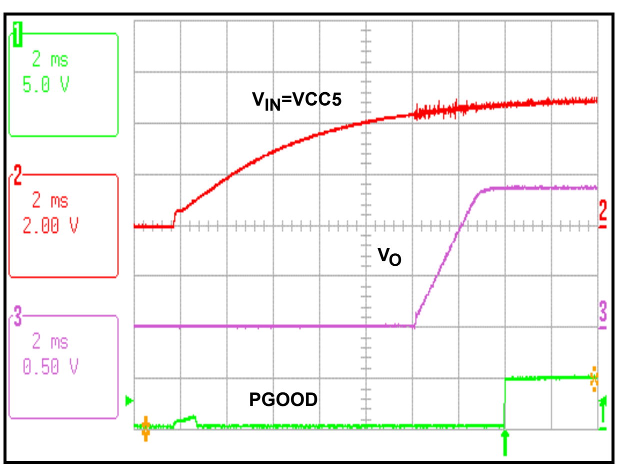


FIGURE 5. SOFT-START WAVEFORMS

As shown in Figure 6, the converter is disabled when the control voltage (VCC5) is pulled below the POR falling threshold (3.88V nominal) of the ISL6558. The PGOOD signal falls low indicating the output voltage is out of regulation. The ISL6609 enters Tri-State® and holds both upper and lower drive signals low. The L-C resonant tank is broken and cannot cause negative ringing at the output since the lower FETs are turned off, blocking any negative current.

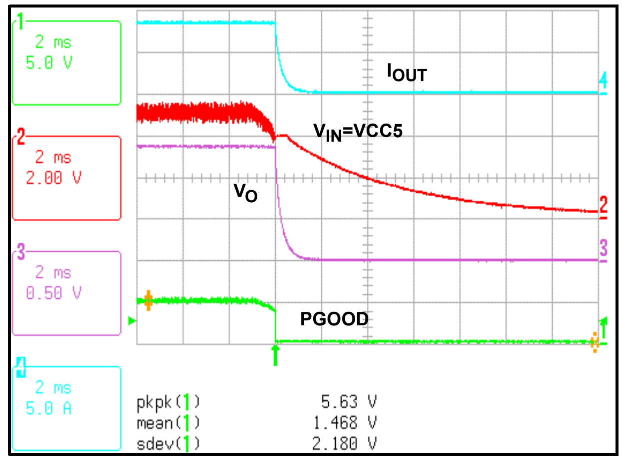


FIGURE 6. TURN-OFF WAVEFORMS

TRANSIENT RESPONSES

A transient load generator is populated on the board to evaluate the response of the converter at high-speed load transients. Current setting of the generator provides about 6.5A load step with 160A/μs on the rising edge and 210A/μs on the falling edge without output droop configuration.

The input current rises/falls at a speed limited by the input inductor and capacitors during step-up/step-down transients. Figure 7 shows a very low ramping up speed (0.02A/μs) of the input current at the load transient condition. This is due to a large effective input inductance seen by the converter. The effective input inductance is the sum of the on-board input inductance and the inductance of the long source leads of the bench power supply.

The transient performance at different operating conditions has been summarized in Table 6. Little difference is noted for various line and load conditions. Note that the ripple portion has been included.

TABLE 6. TRANSIENT RESPONSE (6.5A STEP)

INPUT VOLTAGE/LOAD CURRENT	STEP-UP/DOWN
4.5V/0A	21.9mV/21.9mV
4.5V/25A	21.9mV/21.9mV
5.0V/0A	21.9mV/23.1mV
5.0V/25A	22.5mV/21.9mV
5.5V/0A	21.9mV/21.2mV
5.5V/25A	23.8mV/24.4mV

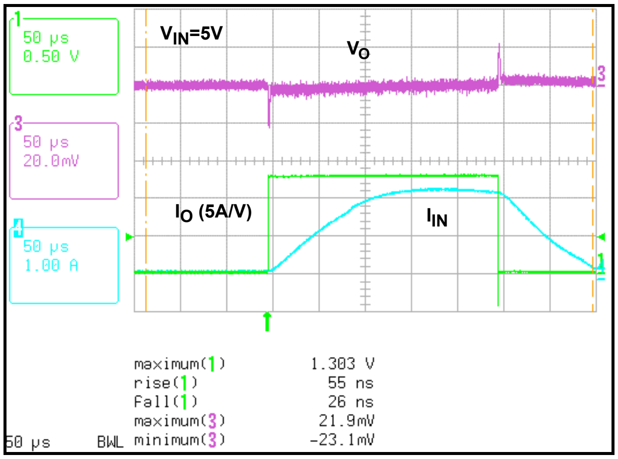


FIGURE 7. TRANSIENT RESPONSE AT NO LOAD (V_{IN} = 5.0V)

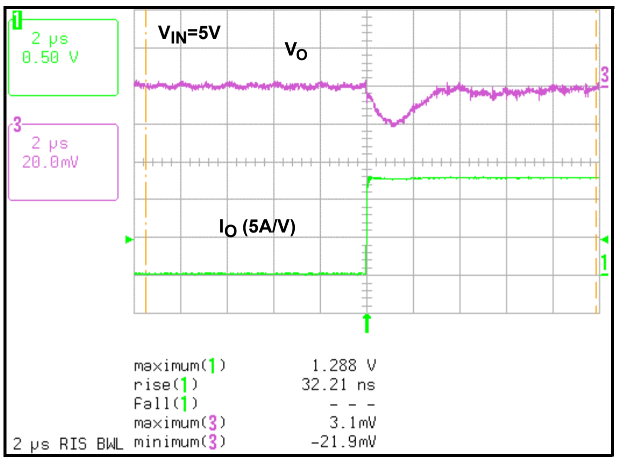


FIGURE 8. STEP-UP TRANSIENTS AT NO LOAD (V_{IN} = 5.0V)

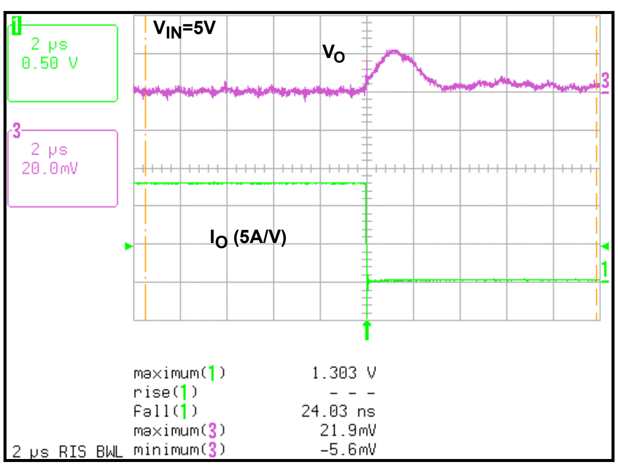


FIGURE 9. STEP-DOWN TRANSIENTS AT NO LOAD (V_{IN} = 5.0V)

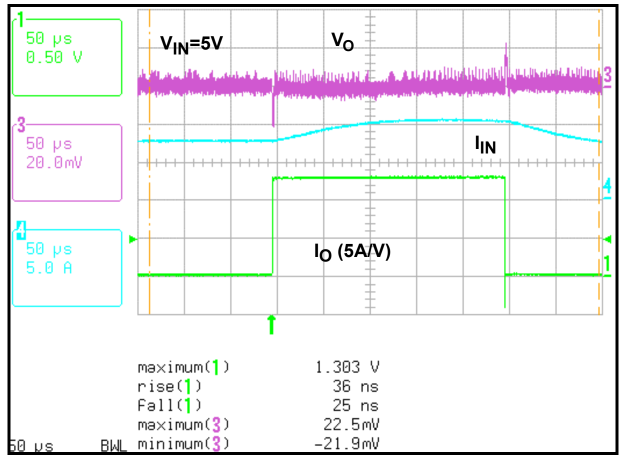


FIGURE 10. TRANSIENT RESPONSE AT 25A (V_{IN} = 5.0V)

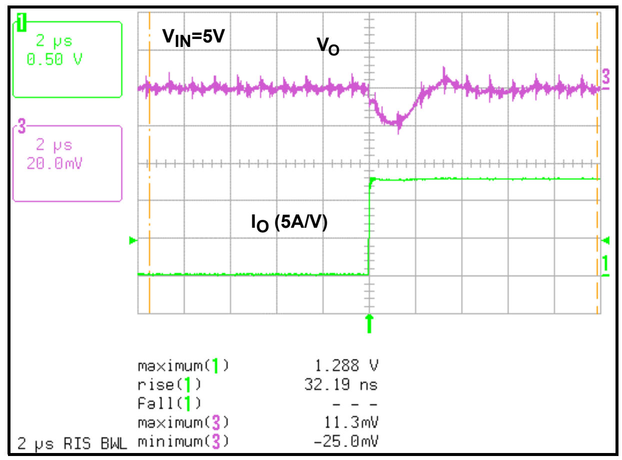


FIGURE 11. STEP-UP TRANSIENTS AT 25A (V_{IN} = 5.0V)

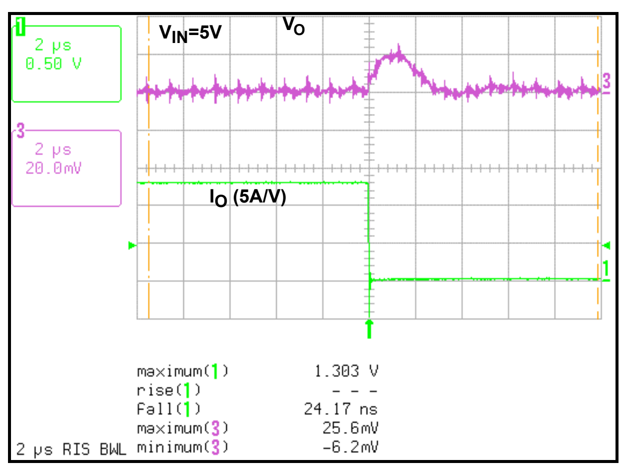


FIGURE 12. STEP-DOWN TRANSIENTS AT 25A (V_{IN} = 5.0V)

OVER CURRENT AND SHORT CIRCUIT

When the converter is momentarily shorted or overloaded, as shown in Figure 13, the converter enters hiccup mode with a narrow duty cycle and long switching period. PGOOD stays low during the overcurrent period; it indicates the output voltage is within regulation limits after the short is removed and the output completes a soft-start interval.

As shown in Figure 14, the converter can sustain a permanent short circuit remaining in hiccup mode with a frequency of 185Hz. The average load current and the average power dissipation in each power component are reduced significantly; thus, the converter can stay at a short without causing any permanent damage or thermal issues.

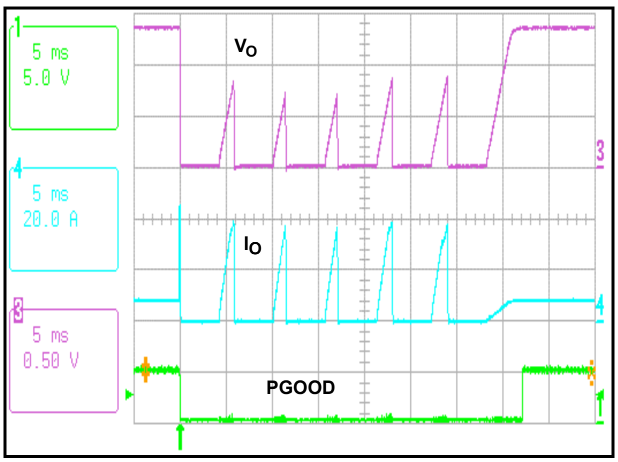


FIGURE 13. OVER-LOADED OUTPUT WAVEFORMS

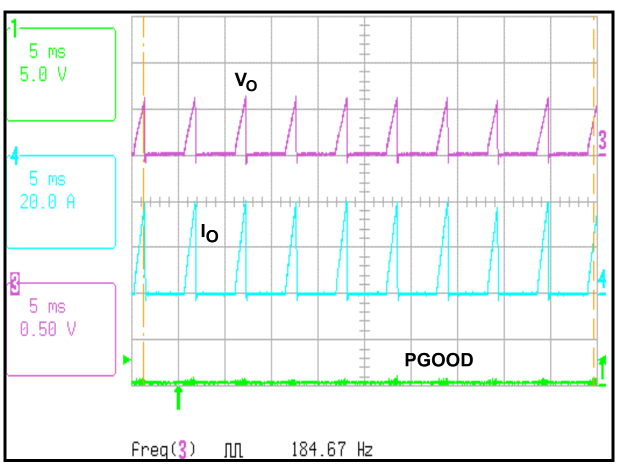


FIGURE 14. SHORT-CIRCUIT WAVEFORMS

OVERVOLTAGE SHUTDOWN

With the COMP pin momentarily tied to a 4V voltage source with respect to the ground, the error voltage jumps high and the duty cycle increases. Thus, the output voltage rises up immediately until it reaches the overvoltage threshold setting the OV latch and triggers the PWM outputs low. PGOOD is pulled low indicating output out of regulation, as shown in Figure 15.

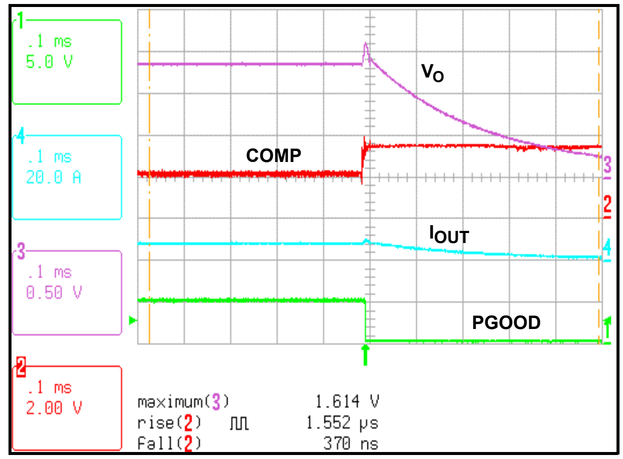


FIGURE 15. OVERVOLTAGE WAVEFORMS

Conclusion

The superior performance of Intersil's ISL6558 four-phase controller, coupled with Intersil's ISL6609 driver, has been demonstrated in the low-profile reference design of a 40W, 500kHz interleaved DC/DC buck converter. An ultra high efficiency of 90% at 1.35V output and 30A full load has been achieved.

The extensive experimental results give users a better understanding of the operation of the converter, the ISL6558 four-phase PWM controller, and the ISL6609 synchronous-rectified driver.

Term Definitions

Cin	Input Capacitance
Co	Output Capacitance
D	Ratio of ON Interval of Upper FET to Single-Channel Switching Period, Duty Cycle
$\Delta V_{IN,CAP}$	Allowable Input Voltage Ripple Contributed by the Input Capacitors
ESR	Overall ESR of Output Capacitors
f_c	System Closed-Loop Bandwidth
Fsw	Per-Channel Switching Frequency
I_{IN}	Input Current
$I_{IN,RMS}$	RMS Current thru Input Capacitors
I_{LO}	Current thru Each-Channel Inductor
$I_{Lo,PEAK}$	Peak Current thru Each-Channel Inductor
$I_{Lo,PP}$	Ripple Current thru Each-Channel Inductor
$I_{Lo,RMS}$	RMS Current thru Each-Channel Inductor
I_{PP}	Overall Ripdple Current thru Output Capacitors
Io	Output Load Current
$I_{Q1,RMS}$	RMS Current thru Upper FET, Q1
$I_{Q2,RMS}$	RMS Current thru Upper FET, Q2
Istep	Load Transient Step
Lin	Input Inductor
Lo	Inductance of Each-Channel Inductor
N	Number of Active Channels
Po	Output Power
η	Output Efficiency
V_{IN}	Input Voltage
Vo	Output Voltage

References

Intersil documents are available on the web at http://www.intersil.com.

[1] Intersil's ISL6558 Data Sheet.

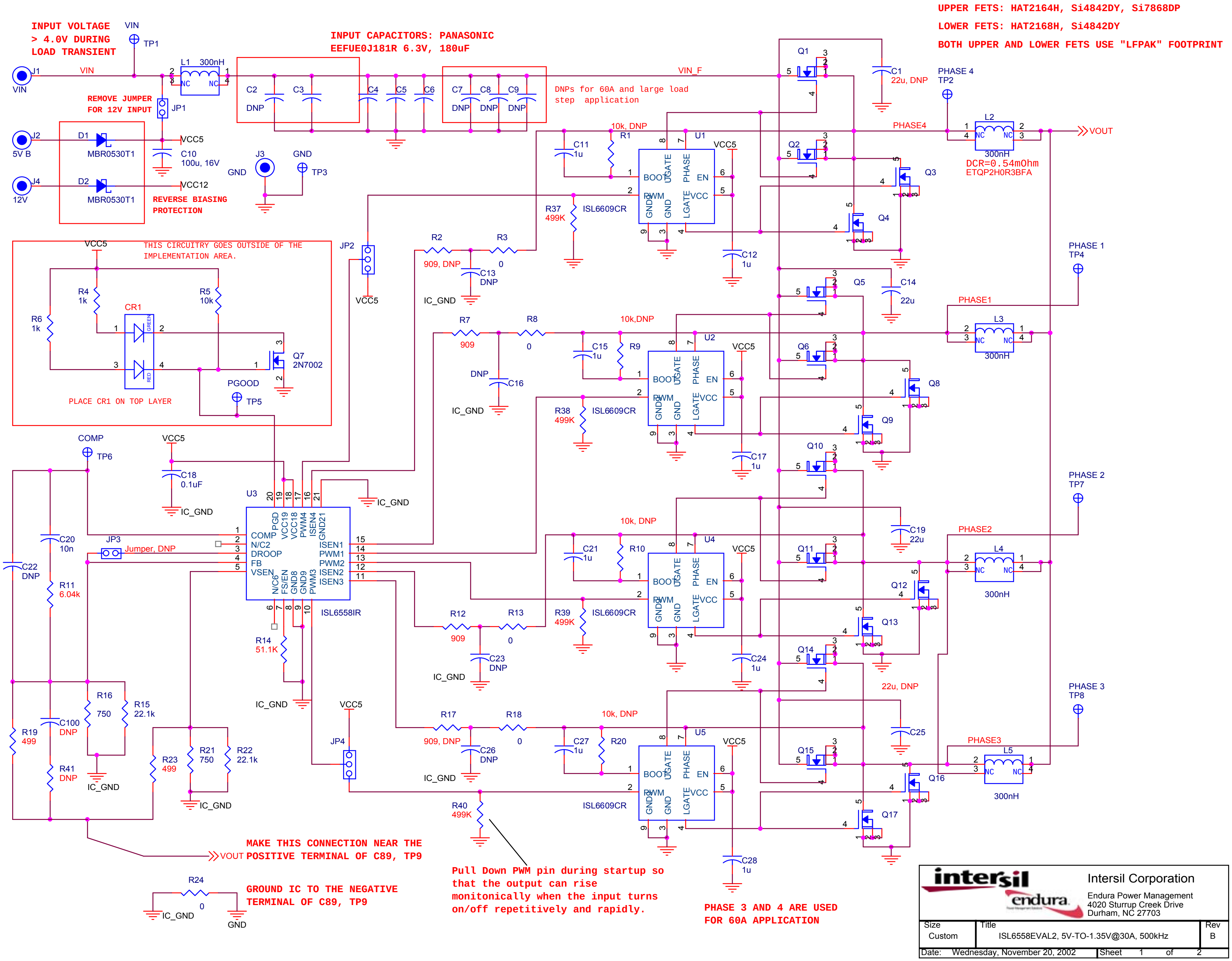
[2] Intersil's ISL6609 Data Sheet.

[3] Intersil's ISL6557A Data Sheet

Appendix

1. Schematics of Reference Design and Load Transient Generator.
2. Bill of Materials and Layout of Evaluation Board.

ISL6558EVAL2



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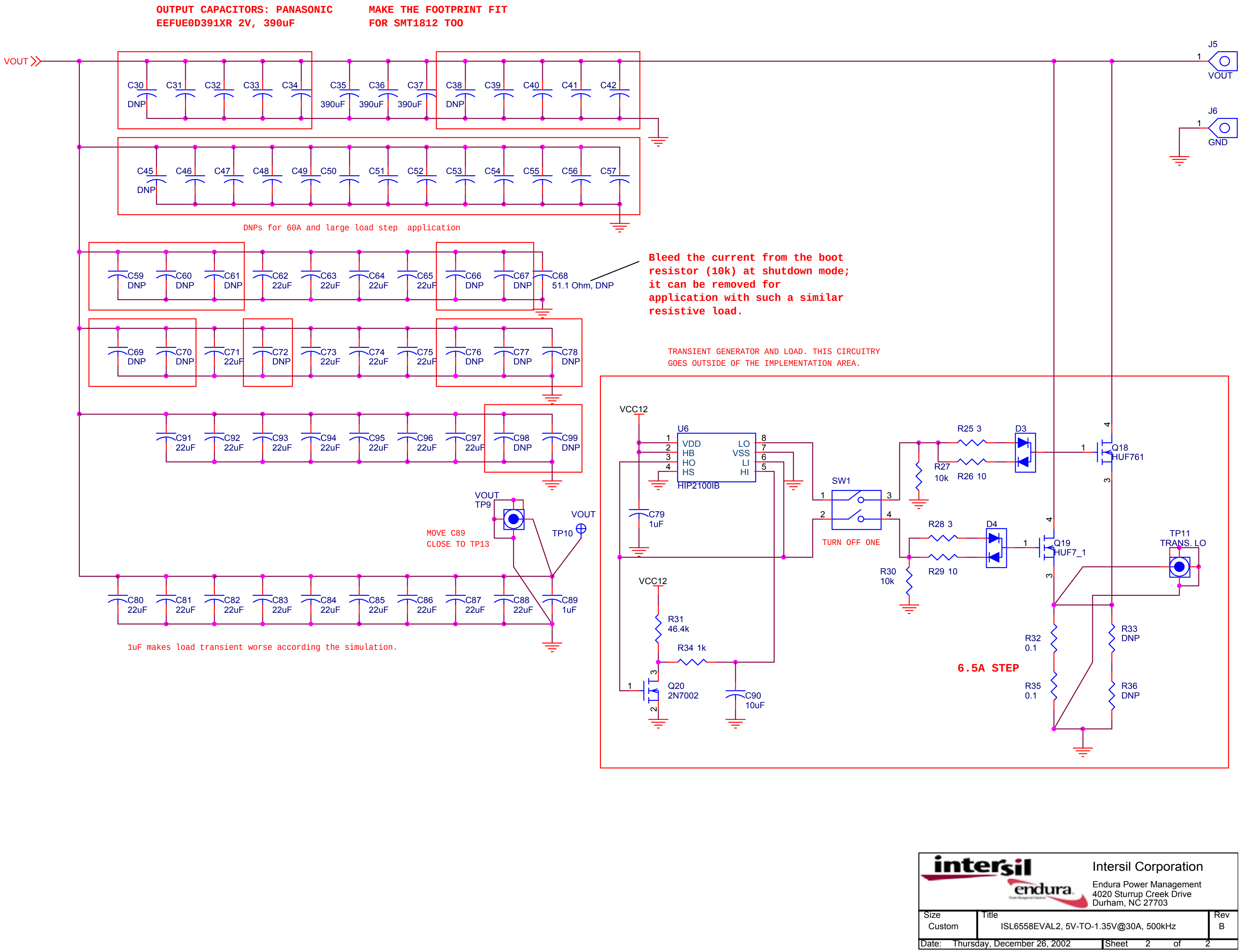

RENESAS

Bill of Materials

QUANTITY	REFERENCE	DESCRIPTION	PACKAGE	VENDOR	PART NO.
1	CR1	Dual LED		PANASONIC	LN2162C13-(TR)
0	C1, C25	22µF	SM/C_1206		DNP
0	C2, C3	680µF, 6.3V, AVX, TPS III, TPSV687M006R0035	CAP_7361	AVX	DNP
3	C4, C5, C6	180µF, 6.3V	CAP_TECAP	PANASONIC	EEFUE0J181XR
0	C7, C8, C9	180µF, 6.3V	CAP_TECAP	PANASONIC	DNP
1	C10	100µ, 16V	PTH	Panasonic	ECA1CHG101
10	C11, C12, C15, C17, C21, C24, C27, C28, C79, C89	1µ	SM/C_1206	Various	6.3V, X5R
0	C13, C16, C22, C23, C26	DNP	SM/C_0603		DNP
1	C18	0.1µF	SM/C_0805	Various	25V, X7R
1	C20	10n	SM/C_0603	Various	25V, X7R
3	C35, C36, C37	390µF, 2V, 10mΩ	CAP_TECAP	PANASONIC	EEFUE0D391XR
0	C30-C34, C38, C39, C40, C41, C42, C45-C57	DNP	CAP_TECAP		DNP
26	C14, C19, C62-C65, C71, C73-C75, C80-C88, C91-C97	22µF	SM/C_1206	Various	6.3V, X5R
0	C59-61, C66, C67-C70, C72, C76-C78, C98-C99	DNP	SM/C_1206		DNP
1	C90	10µF	SM/C_1206	Various	6.3V, X5R
2	D2, D1	MBR0530T1	SOD123	On Semiconductor	MBR0530T1
2	D3, D4	BAV99LT1	SOT23	Various	BAV99
2	JP3, JP1	2-pin Header	TP\2P	Berg	68000-236
2	JP2, JP4	3-pin Header	TP\3P	Berg	68000-236
3		Shunt for JP1, JP2 and JP4		Berg	71363-102
1	J1	VIN	BINDING/POST	Johnson Components	111-0702-001
1	J2	5V BIAS	BINDING/POST	Johnson Components	111-0702-001
1	J3	GND	BINDING/POST	Johnson Components	111-0703-001
1	J4	12V BIAS	BINDING/POST	Johnson Components	111-0707-001
1	J5	VOUT	BINDING/POST	Burndy	KPA8CTP
1	J6	GND	BINDING/POST	Burndy	KPA8CTP
4	L1, L2,L3,L4,L5	300nH	SMT	Panasonic	ETQP2H0R3BFA
8	Q1, Q2, Q5, Q6, Q10, Q11, Q14, Q15	9.4mΩ, 30V	LFPAK	HITACHI	HAT2168H
8	Q3, Q4, Q8, Q9, Q12, Q13, Q16, Q17	4.4mΩ, 30V	LFPAK	HITACHI	HAT2164H
2	Q20, Q7	2N7002	SOT23	On Semiconductor	2N7002LT1
2	Q18, Q19	HUF76129D3S	DPAK	Fairchild	HUF76129D3S
0	R1, R9, R10, R20	10k	SM/R_0805	Various	DNP
2	R7, R12	909	SM/R_0805	Various	1%
0	R2, R17	909	SM/R_0805	Various	DNP
5	R3, R8, R13, R18, R24	0	SM/R_0603	Various	1%

Bill of Materials (Continued)

QUANTITY	REFERENCE	DESCRIPTION	PACKAGE	VENDOR	PART NO.
2	R4, R6	1k	SM/R_0805	Various	1%
3	R5, R27, R30	10k	SM/R_0603	Various	1%
1	R11	6.04k	SM/R_0603	Various	1%
1	R14	51.1K	SM/R_0603	Various	1%
2	R22, R15	22.1k	SM/R_0603	Various	1%
1	**R16**	**750 (only 1% on board)**	SM/R_0603	Various	**0.1%**
1	**R19**	**499 (only 1% on board)**	SM/R_0603	Various	**0.1%**
1	R21	750	SM/R_0603	Various	1%
1	R23	499	SM/R_0603	Various	1%
2	R25, R28	3.01	SM/R_0603	Various	1%
2	R26, R29	10	SM/R_0603	Various	1%
1	R31	46.4k	SM/R_0603	Various	1%
2	R32, R35	0.1	SM/R_2512	Panasonic	1%
2	R33, R36	DNP	SM/R_2512	Various	DNP
1	R34	1k	SM/R_0603	Various	1%
1	SW1	DPST SWITCH		Grayhill	76SB02
1	TP1	VIN	TP	Keystone	5002
1	TP2	PHASE 4	TP	Keystone	5002
1	TP3	GND	TP	Keystone	5002
1	TP4	PHASE 1	TP	Keystone	5002
1	TP5	PGOOD	TP	Keystone	5002
1	TP6	COMP	TP	Keystone	5002
1	TP7	PHASE 2	TP	Keystone	5002
1	TP8	PHASE 3	TP	Keystone	5002
1	TP9	VOUT	PROBE-SOCKET	Tektronics	1314353-00
1	TP10	VOUT	TP	Keystone	5002
1	TP11	LOAD CURRENT	PROBE-SOCKET	Tektronics	1314353-00
4	U1, U2, U4, U5	ISL6609CR	MLFP8_3X3	Intersil	ISL6609CR
1	U3	ISL6558IR	MLFP20_5X5	Intersil	ISL6558IR
1	U6	HIP2100IB	SOIC8	Intersil	HIP2100
4	R37-R40	499k	SM/R_0603	Various	1%
0	C100, R41	DNP	SM/R_0603	Various	DNP

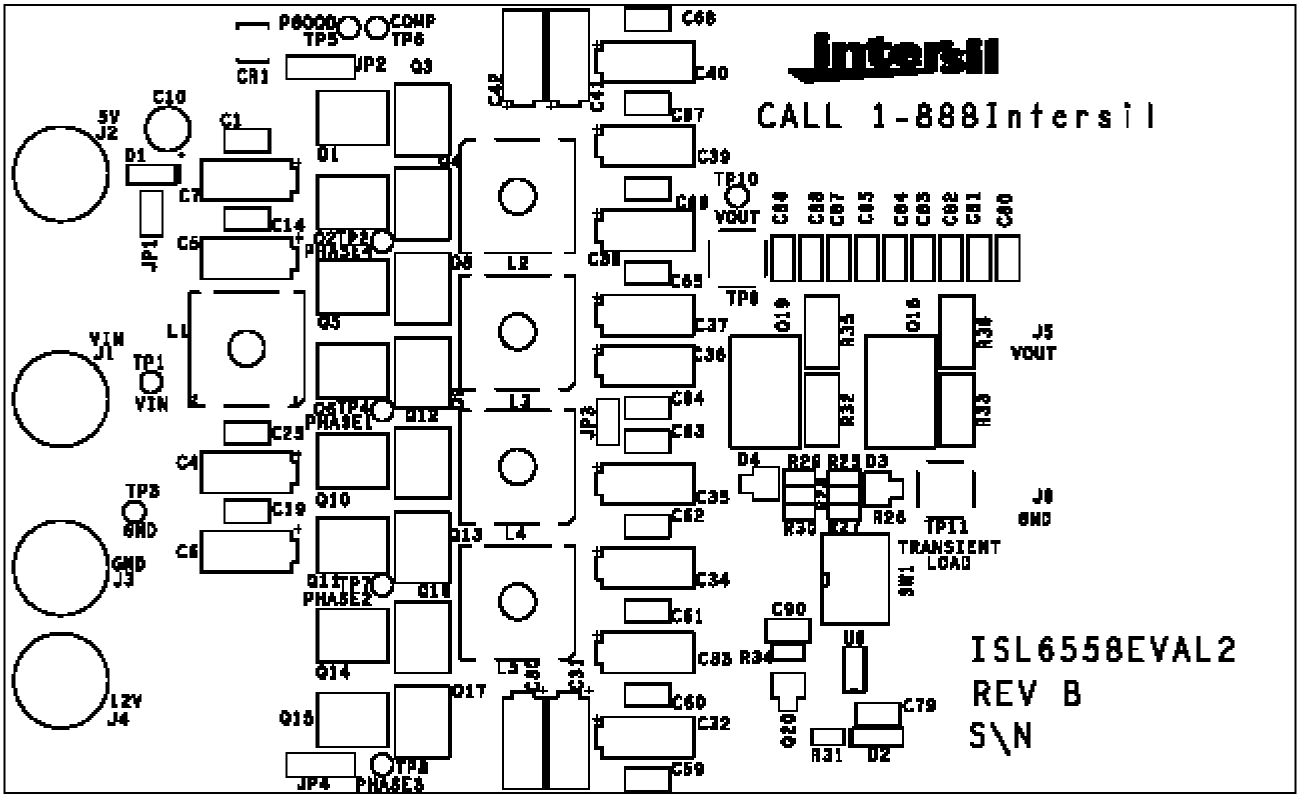

FIGURE 16. TOP LAYER SILK SCREEN

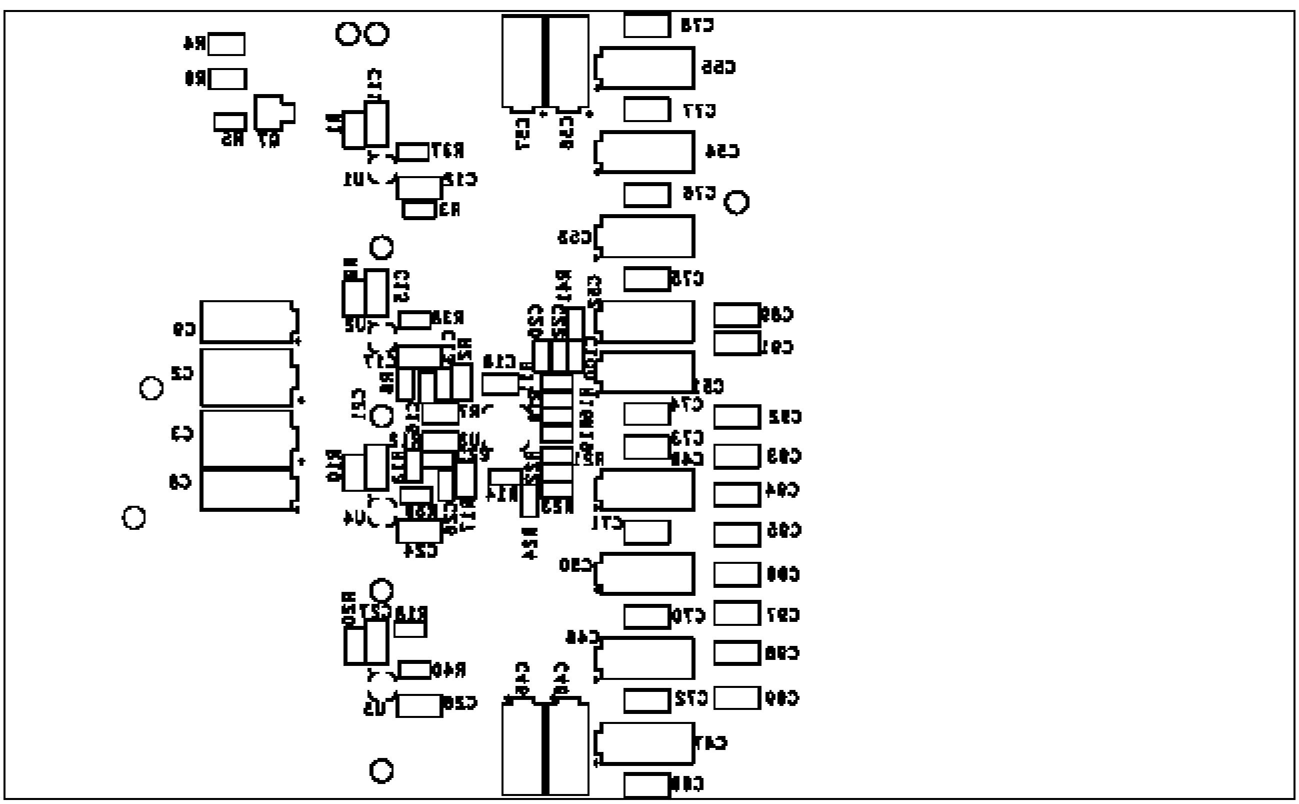

FIGURE 17. BOTTOM LAYER SILK SCREEN

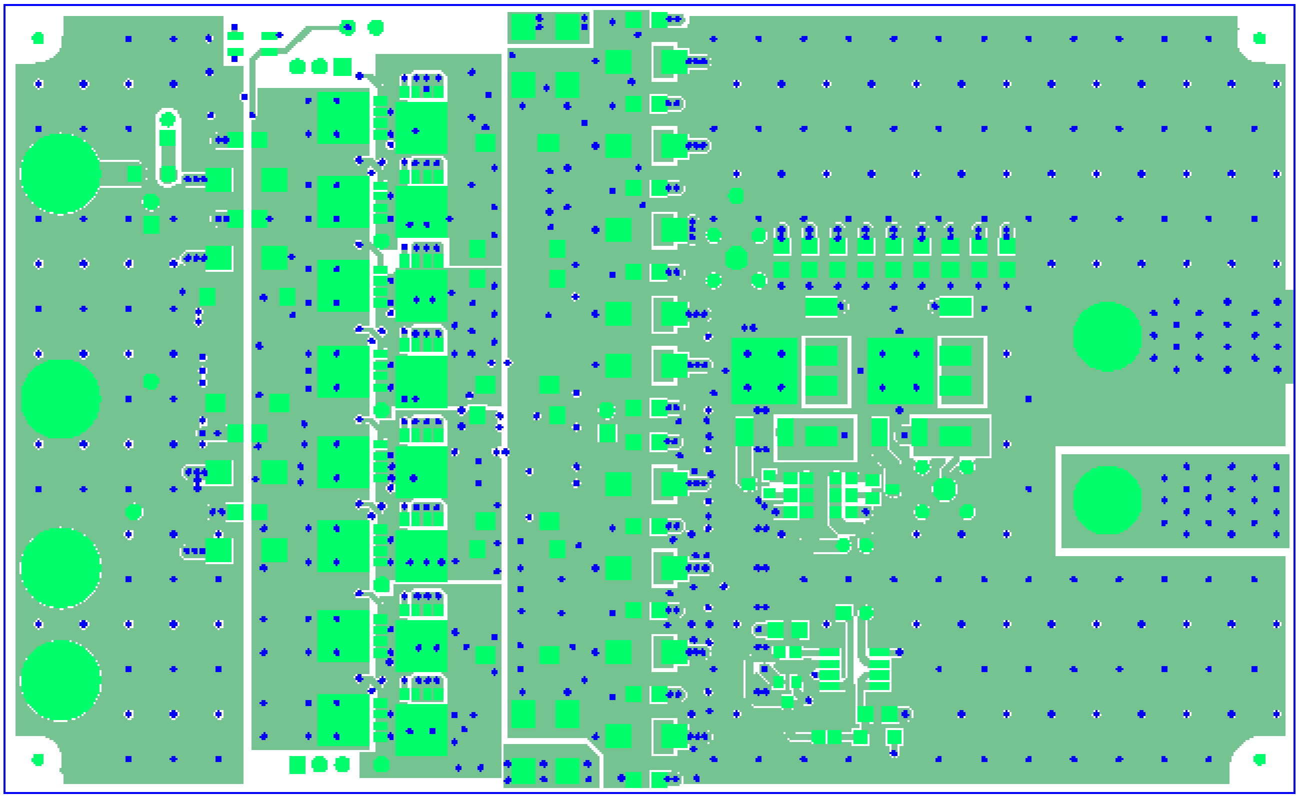

FIGURE 18. TOP LAYER COMPONENT SIDE

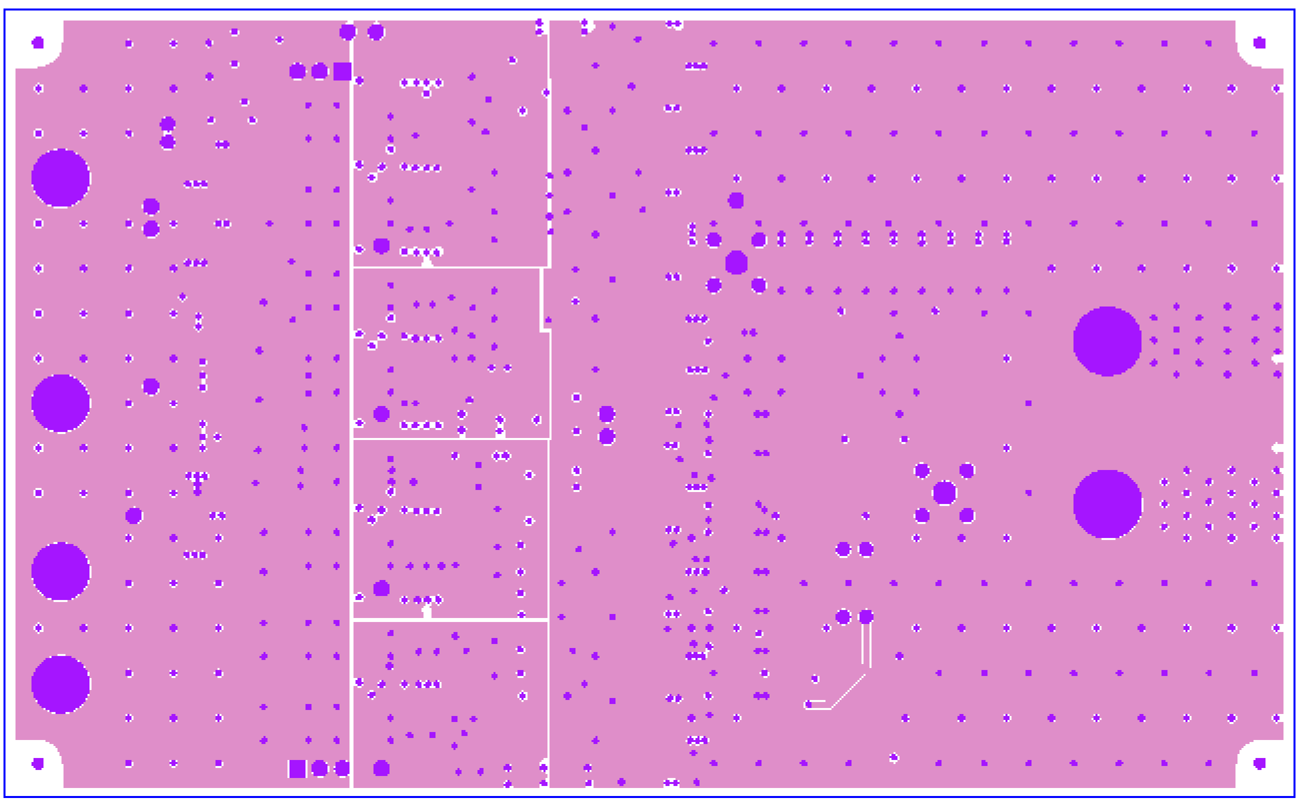

FIGURE 19. LAYER 2

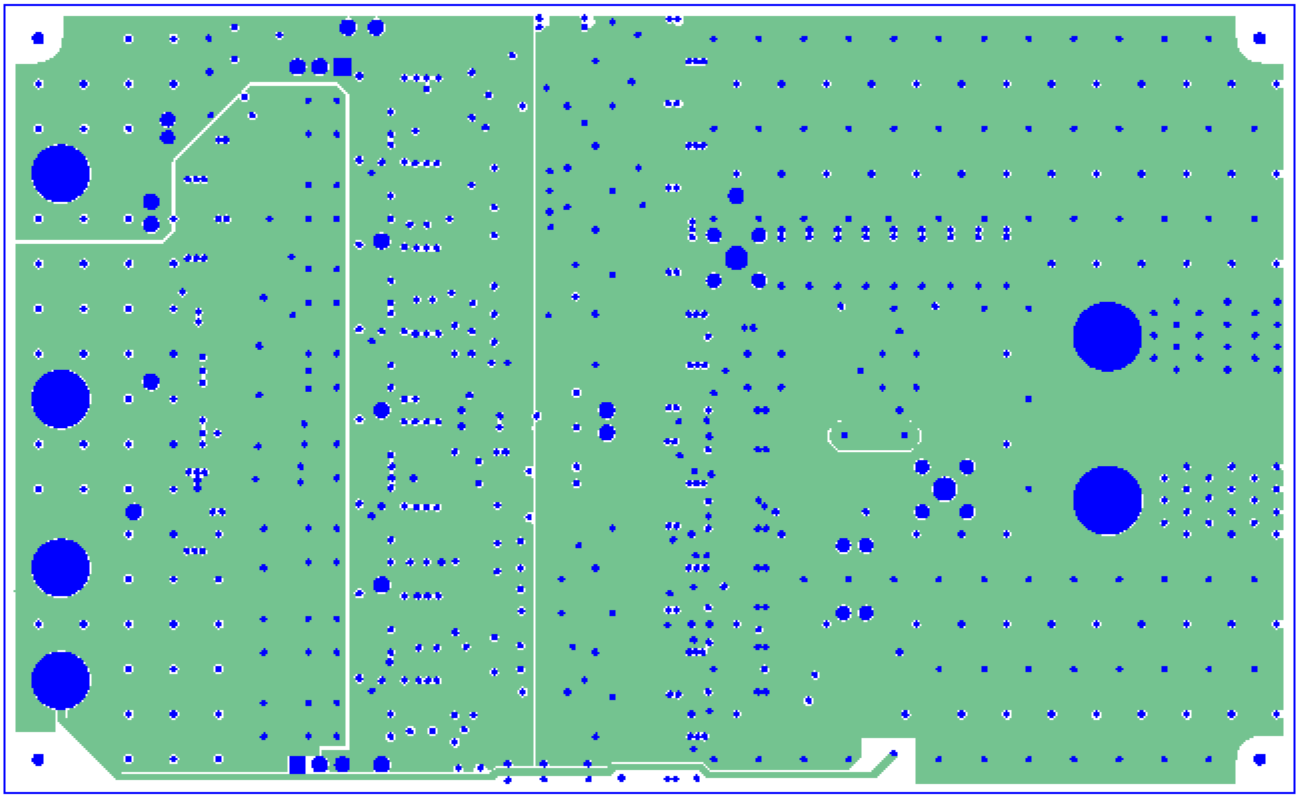

FIGURE 20. LAYER 3

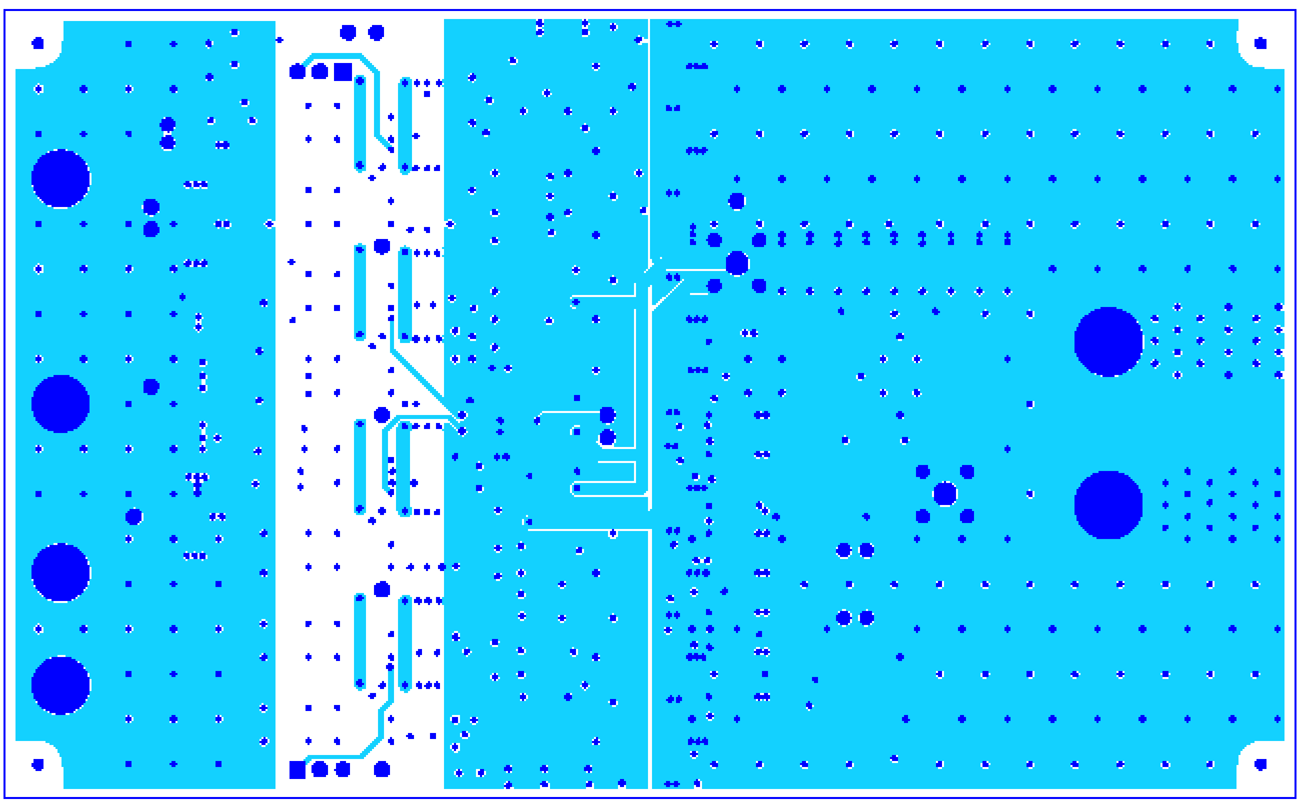

FIGURE 21. LAYER 4

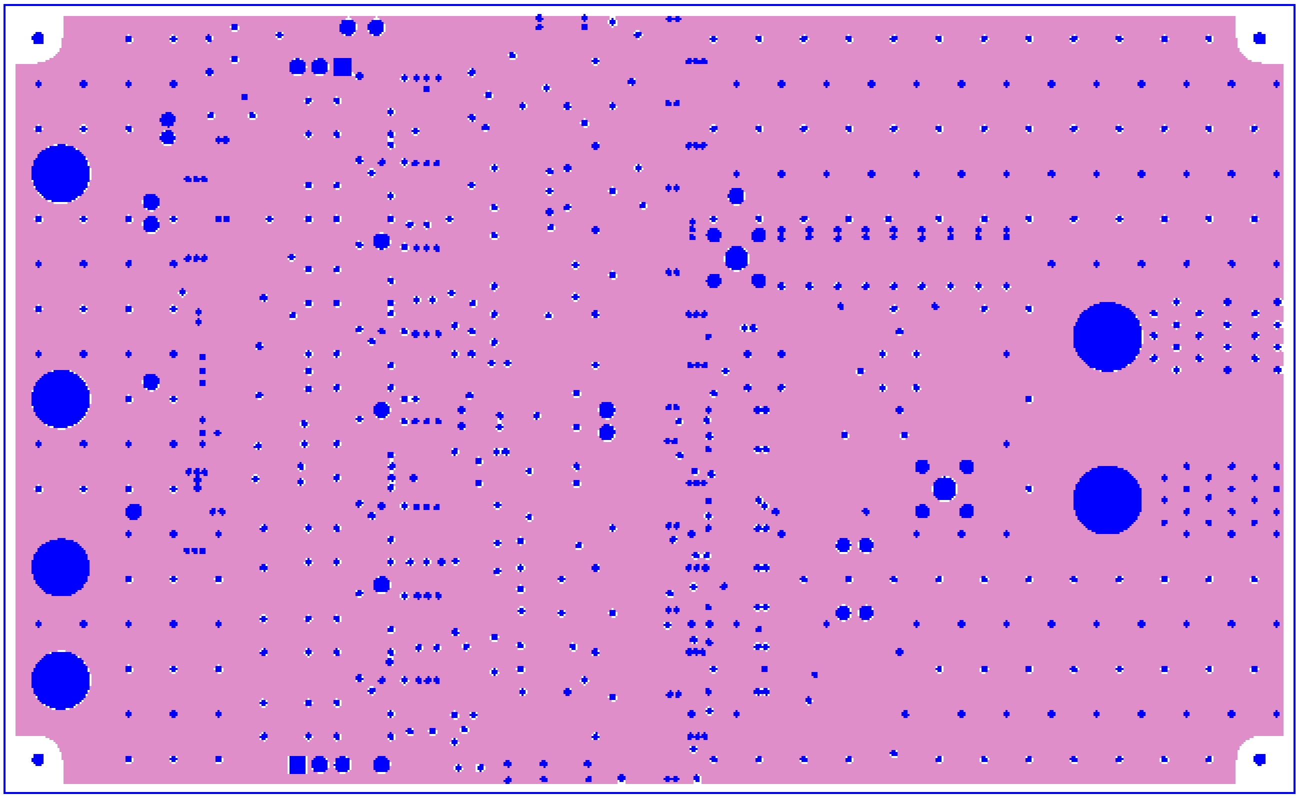

FIGURE 22. LAYER 5

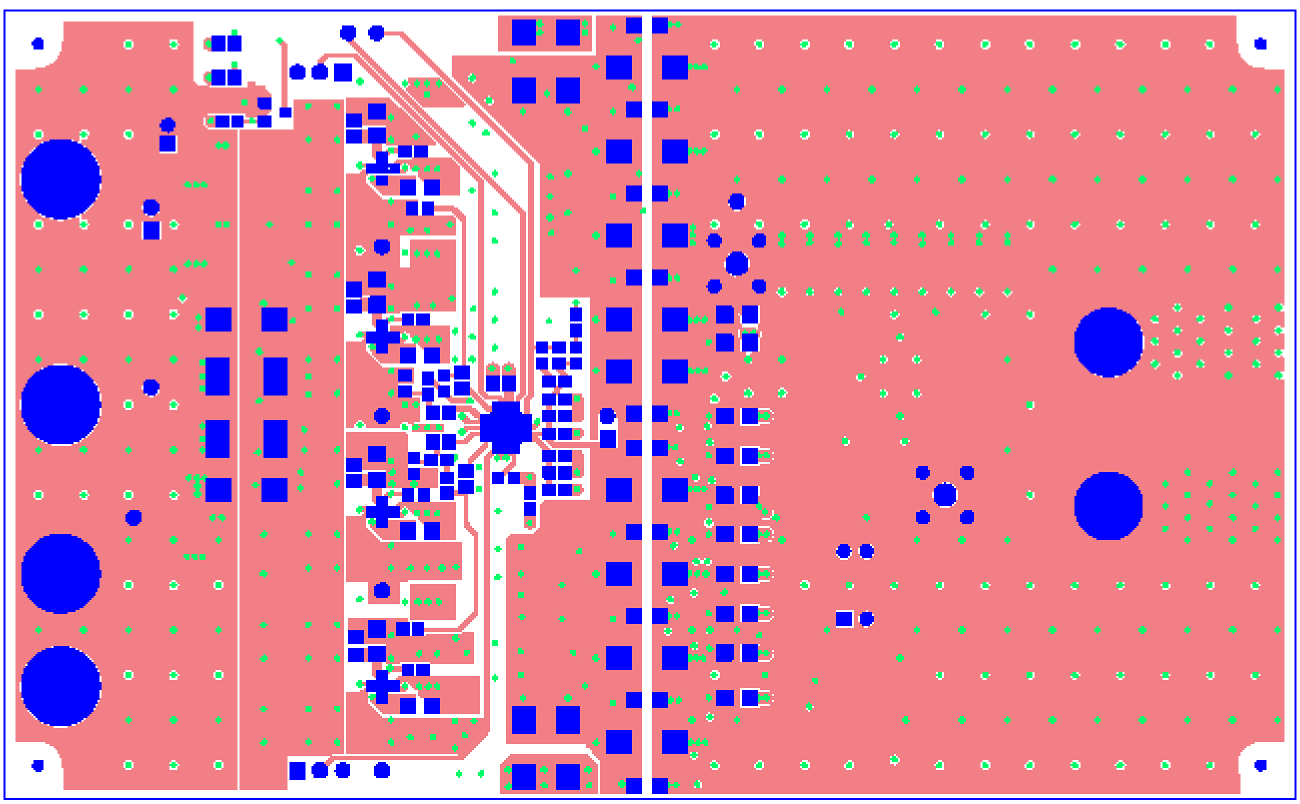

FIGURE 23. BOTTOM LAYER COMPONENT SIDE

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Refer to "http://www.renesas.com/" for the latest and detailed information.

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