# ISL6549LOW-EVAL1, ISL6549HI-EVAL1

A Widely-Applicable PWM and Linear Controller

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## Introduction

The PCI-Express is used in many PC's as the interface to the graphics card. Although the new format allows much higher data rate, one consequence is that 5V is no longer supplied to the interface. This has spawned a new generation of controller IC's that use 12V for bias, and can also use 12V (or any lower voltage) for the input to the regulators. The ISL6549 can control one PWM and one linear output for these conditions, but it can also be used in other systems with 12V available. These EVAL boards provide a simple way to configure a system, and test it out.

There are two current ranges that are presently supported: ISL6549LOW-EVAL1 for higher output voltages, but lower output currents and ISL6549HI-EVAL1 for lower output voltages, but higher output currents. The schematic provided is for the generic board, so the values listed may not match each board; use the appropriate BOM for the correct values, and also for which components are populated or not (DNP = Do Not Populate). Refer to the schematic, Bill Of Materials (BOM), and board layout (at the end of this document), as needed.

## Factory Configuration

The board should be preset from the factory in one of the following two configurations. The section "More Detailed Circuit Setup" has more information about the board, connections, and options for making changes.

**1. Low Power (ISL6549LOW-EVAL1):**

$V_{OUT1}$ = 5.0V @ 3A (with $V_{IN1}$ = $V_{CC12}$ = 12V, using JP1; 600kHz PWM $F_{SW}$)

$V_{OUT2}$ = 3.3V @ 1A (with $V_{IN2}$ = $V_{OUT1}$ = 5.0V, using JP2)

Note that $V_{OUT1}$ supplies 3A PLUS the 1A from $V_{OUT2}$, for a total of 4A. Both outputs should be able to run at their rated currents simultaneously, at room temperature ambient, with an appropriate 12V supply, rated at 3A. The output current capability of the linear regulator is determined mainly by the power dissipation of the pass FET.

**2. High Current (ISL6549HI-EVAL1):**

$V_{OUT1}$ = 1.2V @ 20A (with $V_{IN1}$ = $V_{CC12}$ = 12V, using JP1; 600kHz PWM $F_{SW}$)

$V_{OUT2}$ = 1.6V @ 1A (with $V_{IN2}$ = 3.3V; JP2 is **OPEN** (not used))

## Quick Start Evaluation

Figure 1 shows a picture of a blank board for reference, and details the available input and output connections. Each input ($V_{CC12}$, $V_{IN1}$, $V_{IN2}$) and its GND has binding posts. Each output has turrets for VOUT and GND, plus a scope probe socket, for low noise waveforms. JP1 and JP2 are jumpers, for those cases where voltages are shared. Most of the important IC signals on the board have a test pin for easy monitoring (or for making alternate connections). SW1 can be used to enable/disable the regulator. The CR1 LED lights when there is activity on the PHASE node.

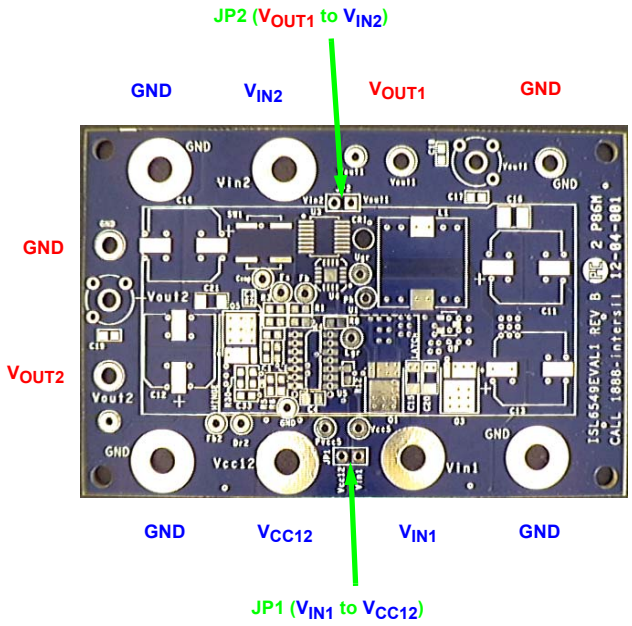


**FIGURE 1. ISL6549EVAL1 INPUT AND OUTPUT CONNECTIONS**

It is recommended that, should electronic or higher power loads not be available, light loads (40Ω or so) are connected to each output.

### Quick Start Setup (light load)

Switch SW1 should be pointing towards the bottom of the board; this should enable both outputs, and should allow the LED to light, when $V_{OUT1}$ is powered up.

Figure 2 shows the simple setup for the ISL6549LOW-EVAL1 board. To test the board as shipped, apply the 12V power input, and the CR1 LED should come up when $V_{OUT1}$ starts switching.

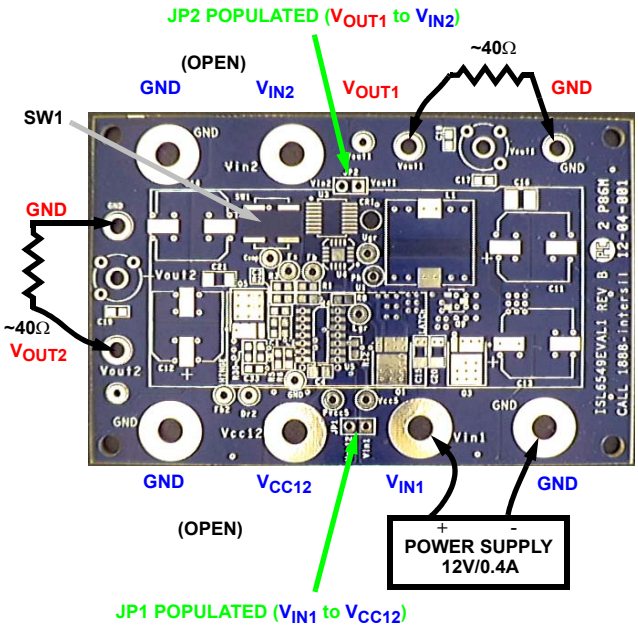


**FIGURE 2. TYPICAL ISL6549LOW-EVAL1 HOOK-UP**

The ISL6549HI-EVAL1 board requires a 2nd power supply for $V_{IN2}$, and removal of JP2, as shown in Figure 3. To test the board as shipped, apply the 12V power input, and 3.3V supply to $V_{IN2}$. The CR1 LED should come up when $V_{OUT1}$ starts switching.

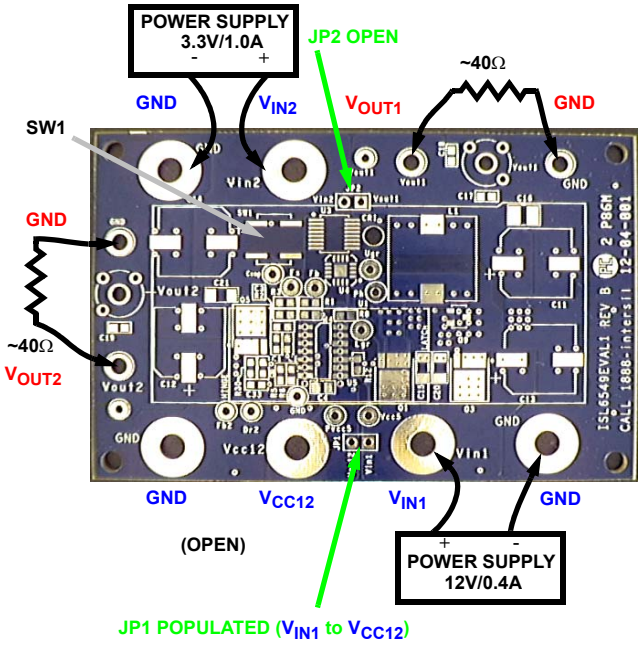


**FIGURE 3. TYPICAL ISL6549LOW-EVAL1 HOOK-UP**

In this setup, both outputs can be monitored with a voltmeter or oscilloscope. It is advisable to verify the board as is first. Once the basic functionality has been confirmed, more specific measurements, or changes to the board or setup can be attempted.

### *Input Power Supply Considerations*

This section discusses the circuit functions in more detail; section *Board Modifications* discusses changes that can be done. Make all changes and connections prior to application of power. For reference, orient the board with the "ISL6549EVAL1 REV B" label on the right, as shown in Figure 1 or 2.

The output load current needed determines the number and kind of FETs required for any given application. This evaluation board has numerous FET footprints that can be used (all are connected in parallel, so only use one configuration at a time). If the factory-supplied board doesn't meet the needs, substitute other FETs. The inductor is initially sized for the maximum current expected; substitutions can be made if desired.

The ISL6549 has two general purpose outputs, and the evaluation board allows for a lot of flexibility. It was designed for the PCI-Express (where 12V and 3.3V are available, but 5V is not), but can be used in many other applications as well. The ISL6549 requires a 12V input for $V_{CC12}$ bias; it creates its own internal 5.4V rail for bias and gate drivers. Either input ($V_{IN1}$ for the switcher, and $V_{IN2}$ for the linear) can use 12V, or any available voltage down to just above the 0.8V reference, including 3.3V, 5V (if available), or other regulator outputs.

The input voltages (and their GNDs) have binding posts for connections. For the most flexibility, this evaluation board has three sets (power and GND) of binding posts, one each for $V_{CC12}$, $V_{IN1}$ and $V_{IN2}$. All of the input and output GND posts are tied together (to the internal GND plane), but use the local one associated with each input or output for the best performance. In addition, two jumpers are available to tie common connections together.

If $V_{IN1}$ and $V_{CC12}$ share a common 12V supply, then JP1 should be shorted; if not, leave it open. If $V_{IN1}$ is not 12V, or if $V_{IN1}$ is not to be shared with $V_{CC12}$, then connect a separate 12V power supply (typically no more than ~100mA, depending on FETs and PWM switching frequency) to the $V_{CC12}$ post and its GND, and remove the JP1 shunt. The $V_{IN1}$ post is next to the upper FETs for a high current, low resistance path; do not use the $V_{CC12}$ post and JP1 instead of the $V_{IN1}$ post, when the input voltage is provided from the same supply.

$V_{IN2}$ is the input voltage for the linear regulator; connect its supply to the $V_{IN2}$ post (J2) on the top left side of the board. Make sure JP2 shunt is not populated, unless $V_{OUT1}$ is to be used as the $V_{IN2}$ supply. (Note: $V_{OUT1}$ must be a higher voltage than $V_{OUT2}$, in order to be used as $V_{IN2}$; $V_{OUT1}$ must also be able to supply the extra current).

For full-load testing, use input power supplies that can supply the current required for the desired maximum output load conditions; 5A rating is recommended for the high current board ($V_{IN1}$ = 12V = $V_{CC12}$). Since $V_{OUT2}$ is a linear

regulator, $V_{IN2}$ must be able to supply the full load current directly. An electronic load on the outputs is generally recommended for its ease of use evaluating different loads.

### Circuit Setup Options

Each output can be programmed with a resistor divider, to any voltage between its input voltage (12V maximum) and its internal reference voltage (0.8V). The input capacitors for both regulators are rated at 16V, for use with a 12V supply. The bulk output capacitors are rated at only 10V, and some of the ceramic output capacitors are only rated for 6.3V. See *Adjusting the Output Voltage* paragraph in the *Board Modifications* section for the details.

The frequency of the switching regulator can be set as low as 150kHz, and as high as 1MHz. The switching frequency plays into the output ripple current, and the selection of the output inductor and capacitors. A single resistor (R7) to GND programs the frequency; see datasheet for details.

The IC used on the evaluation board is the 14 Ld SOIC version. Dummy footprints for the 16 Ld QFN and 16 Ld QSOP packages are provided for size comparison. Smaller packages have tighter pin spacings, which may limit how tightly one can pack components around them, and still allow for proper trace routing. While the electrical performance of all three packages should be quite similar, the QFN should showcase best thermal performance in an application.

A switch (SW1) is connected from FS_DIS pin to GND, as a means to disable the controller IC when grounded. An LED (CR1) is lit whenever there is voltage on the phase node, offering a visual cue that the switching regulator is operating.

The compensation used for the switcher is type-2, but footprints are available for a type-3 network, as well. The compensation components have been chosen for the given inductor and capacitor values (and its ESR), and operating frequency. If any of these components or parameter changes, then the compensation may need to be adjusted accordingly, to maintain stable operation (see datasheet for details).

The linear regulator does not require external compensation for most conditions, but footprints are available for the those cases where it may be needed (generally, only when ceramic output capacitors are used). Other optional component footprints include series gate resistors, an RC snubber and a freewheeling diode on the switcher's phase node.

## Performance Waveforms

Figures 4 through 19 depict the evaluation board's performance during typical operational situations, as well as during fault conditions. Examples are usually shown for just one version of the board (low or high current); results on the other board should be similar, unless noted. Loading of the output can be most easily done via an electronic load; however, any other method will work as well.

### Power-up

Up to 3 power supplies ($V_{CC12}$, $V_{IN1}$, $V_{IN2}$) may be needed to power up the board, but some inputs can share a single supply, or the output of one regulator can be used as the input to the other.

Power-up can be performed in any order. In order to commence normal operation, however, the $V_{CC12}$ supply must be above the VCC12 pin's rising POR trip level, the internal 5.4V supply (on the VCC5 pin) must also be above its rising POR trip level, and FS must not be held low. Once all conditions are met, the IC will start a soft-start cycle, and ramp up both outputs. The soft-starting of the outputs takes ~6.8ms when running at 600kHz. Should VIN not be ready, or should there be an undervoltage condition detected on either output, the entire IC shuts off, and attempts to re-start following one soft-start period off. See *Fault Handling* for more information.

Figure 4 shows a typical power-up sequence, using the high current evaluation board. A 12V supply is used for both $V_{CC12}$ bias and $V_{IN1}$, while a separate 3.3V supply (not shown) ramps up with the 12V, and is used for $V_{IN2}$. As $V_{CC12}$ ramps up, the $V_{CC5}$ pin follows, until the internal regulator curbs its rise at around 5.4V. When $V_{CC12}$ exceeds its POR rising trip point (~9.5V), both outputs commence their soft-start ramps. Both outputs start and complete their soft-start ramps at the same time, and the waveforms should look the same, regardless of the load current.

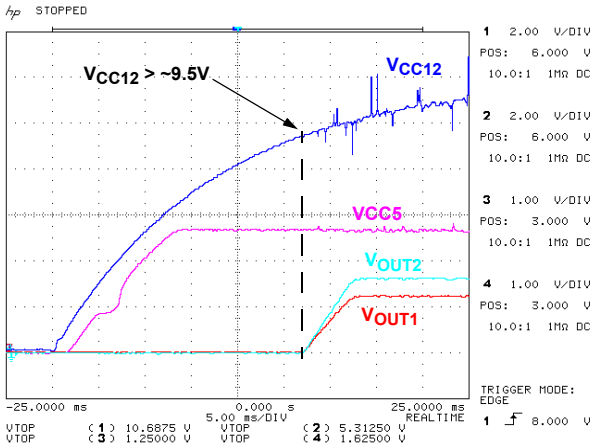


**FIGURE 4. TYPICAL POWER-UP WAVEFORMS**

### Soft-start Detail and Pre-charged Outputs

Figure 5 details a typical ISL6549EVAL1 output soft-start ramp in more detail. For this scope capture, the supply powering the board is turned on prior to time T0. At time T0, SW1 is enabling the circuit for operation and a soft-start sequence is initiated, after an initial delay of 64 switching cycles. The soft-start ramp is internally generated, using a digital approach, and it consists of 64 discrete steps, incremented every 64 switching cycles, to approximate a linear ramp. The output voltage is thusly stepped up gradually to its set value.

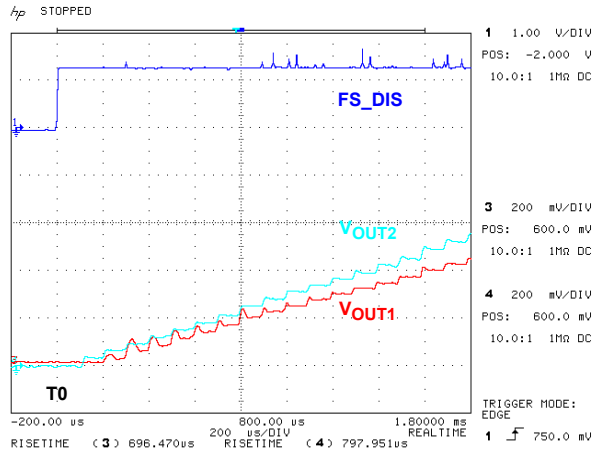


**FIGURE 5. ISL6549EVAL1 NORMAL START-UP DETAIL**

Special consideration is given to the PWM output's start-up into a pre-charged output. Under such circumstances, the ISL6549 keeps off both MOSFETs until the internal reference is ramped past the output voltage sensed at the FB pin. By using this approach, the output voltage ramp-up promptly commences at the pre-charge level, with little to no disturbance being inflicted, as detailed in Figure 6. The circuit is enabled, similar to Figure 5, at time T0 (FS_DIS signal not shown). $V_{OUT1}$ is precharged to ~4V; and as the internal ramp exceeds the magnitude of the output voltage at time T1, the MOSFETs drivers are enabled. The output voltage ramps up in a seamless fashion from the pre-existent level to the final level of 5.0V, reached at time T2. $V_{OUT2}$ is also shown, for timing reference.

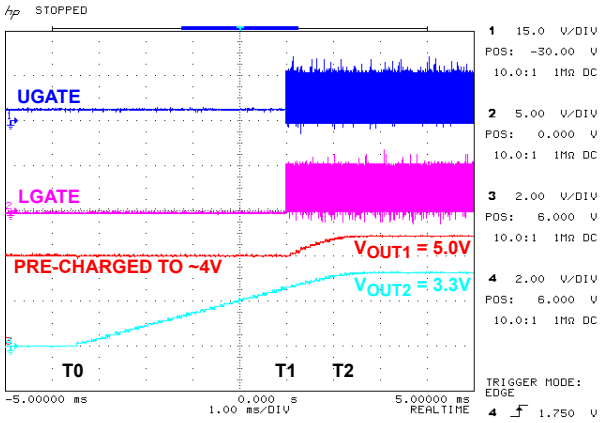


**FIGURE 6. ISL6549EVAL1 START-UP INTO A PARTIALLY CHARGED OUTPUT**

A second (and less likely) scenario is for the output to be pre-charged above the resistor-divider set point, as shown in Figure 7. In this situation, the ISL6549 keeps the MOSFETs off until the end of the SS ramp. Once the end of the soft-start ramp is reached (at time T2), the output drivers are enabled for operation, and the output is subjected to an abrupt correction down to the expected set-point level (5.0V here).

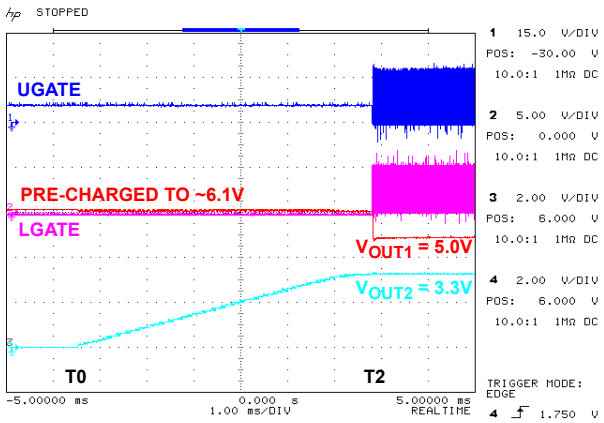


**FIGURE 7. ISL6549EVAL1 START-UP INTO AN OVER-CHARGED OUTPUT**

### *Fault Handling: Undervoltage Response*

The ISL6549 protects the output against undervoltage (UV) events. UV monitoring is disabled during the first 16 soft-start steps. Once enabled, if a UV event is detected on either output, the ISL6549 turns off both outputs, waits for a time period equaling one internal SS cycle, and then attempts an output soft-start. The behavior of the circuit in UV repeats until the fault condition is removed or the circuit is disabled. Review the appropriate datasheet sections for more details.

Figure 8 displays a pattern of typical circuit behavior when encountering an UV situation. In this example, $V_{IN1}$ is not powered, so $V_{OUT1}$ doesn't turn on, and should fail for UV.

A soft-start cycle begins at time T0; $V_{OUT2}$ ramps up 1/4 of the way (~ 0.825V out of the expected 3.3V output), at which time the UV comparators are enabled. Since $V_{IN1}$ is not present, $V_{OUT1}$ is not following the soft-start ramp up, and it trips the UV protection, shutting down both outputs. Following an internal wait period equal to one soft-start interval, from T1 to T0, the circuit initiates a new SS cycle, attempting to bring the outputs back within regulation limits. As the output voltage tries to increase, if it is held back by a short-circuit (or in this case, the lack of an input voltage), the UV protection is tripped again, at time T2, resulting in the repeat of the shut-down/wait/re-start cycle.

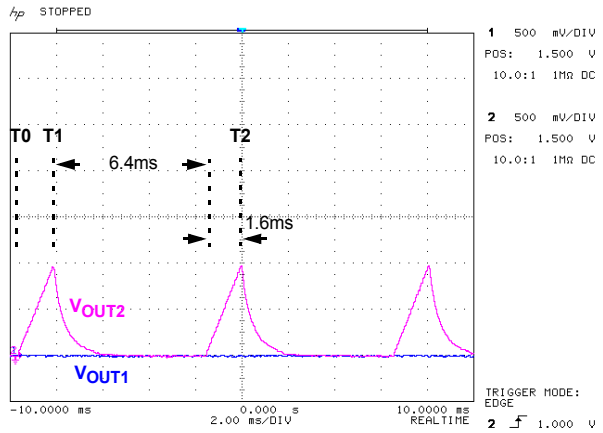


**FIGURE 8. ISL6549EVAL1 UNDER-VOLTAGE PROTECTION**

The example in Figure 8 shows a 1.6ms ramp up, and a 6.4ms off time, before the next ramp starts. Thus, the total period of 8ms is based on 1.25 soft-start cycles (one-quarter of the first ramp, and then one full time-out, at a clock period of around 1.6µs).

### *Switching Waveforms*

The following figures show the gate driver signals in the low current board, with a light output load (~600mA). The grounding of the scope probes is important in capturing waveforms representative of actual board signals. The following waveforms were not optimally captured, as they used the test pins and the nearest ground connection for the scope probe's ground connection, resulting in some extra ringing and overshoot being picked up due to the setup.

Figure 9 depicts one typical switching cycle. The switching frequency is measured at 622kHz, and the duty cycle is ~41%, matching the 5V/12V output to input ratio.

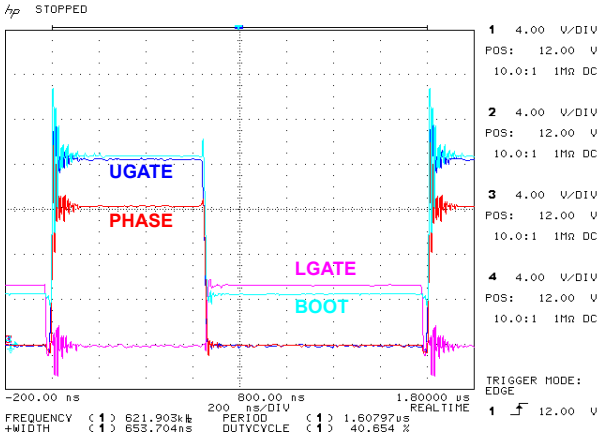


**FIGURE 9. ISL6549LOW-EVAL1 SWITCHING WAVEFORMS**

Switching detail coinciding with the rising edge of the PHASE node is pictured in Figure 10. The dead-time, defined here as from LGATE falling below 2V to UGATE-PHASE rising above 2V, is less than 20ns. Shorter deadtimes improve the switching efficiency.

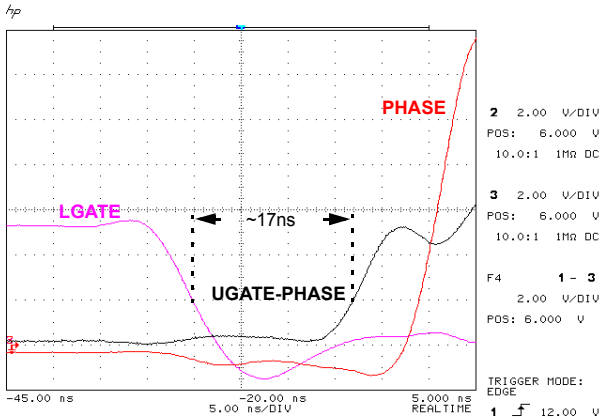


**FIGURE 10. ISL6549 RISING UGATE EDGE**

Similar detail, but this time captured at the falling PHASE edge is shown in Figure 11. Internal adaptable circuitry not only protects against shoot-through events, but also yields desirable dead times in the sub-20ns interval.

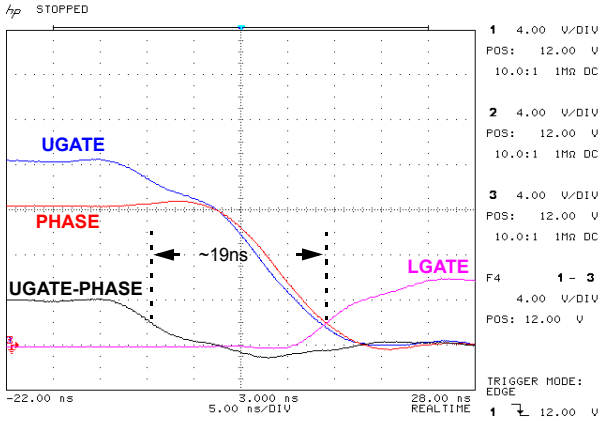


**FIGURE 11. ISL6549 FALLING UGATE EDGE**

### *Duty Cycle Jitter*

While jitter may look undesirable, small amounts don't significantly affect circuit performance. In certain applications, jitter is actually desired, as it has the beneficial effect of lowering the EMI emissions by spreading the energy across a broader spectrum of frequencies.

The duty cycle variation in a switching converter is a natural occurrence. Duty cycle is varied during soft-start to increase the output voltage, and both increased and decreased, as required to modulate the inductor current and keep the output at the set regulation point. During DC steady-state operating conditions, the duty cycle should ideally be a fixed value. However, normal perturbations in the output and input supplies, noise captured by the feedback loop, as well as the natural switching frequency ripple fed through the error amplifier, all can result in duty cycle variations. Figure 12 details the typical jitter of the

ISL6549LOW-EVAL1. The rising edge of UGATE is used for triggering.

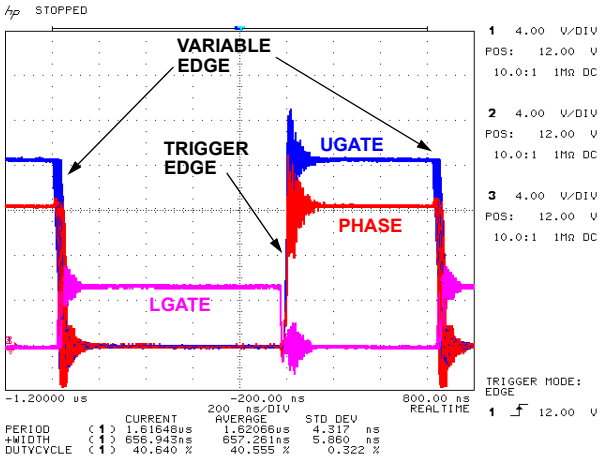


**FIGURE 12. ISL6549LOW-EVAL1 JITTER MEASUREMENT; STATISTICS AND INFINITE PERSISTENCE**

### *Output Ripple Voltage*

Figure 13 shows a typical output ripple voltage waveform for the ISL6549LOW-EVAL1 board. The ripple voltage is commensurate with the product of the inductor ripple current current (~1A) multiplied by the ESR (13mΩ) of the output capacitor used. Various tradeoffs are possible in order to adjust the resulting output voltage ripple. Increasing the value of the output inductor or the switching frequency leads to reductions in the inductor ripple. However, all other parameters being equal, such measures may have other less benefic effects, like larger inductor magnetic structures or increased switching losses.

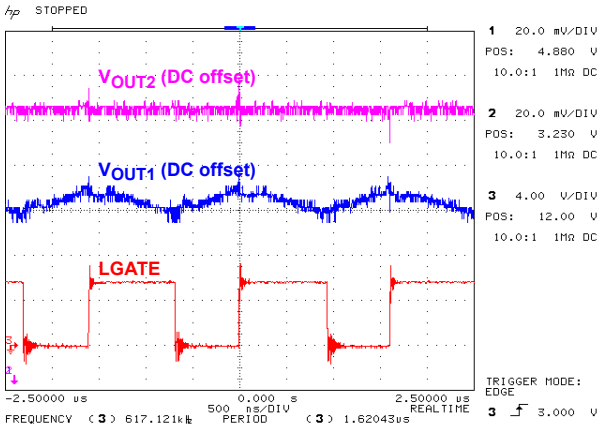


**FIGURE 13. ISL6549LOW-EVAL1 OUTPUT SWITCHING RIPPLE VOLTAGE**

### *Output Transient Response*

Figure 14 details the circuit's response to a load step transient on the switching output, $V_{OUT1}$, of the low current board. The current transient applied to $V_{OUT1}$ has a magnitude of 4A.

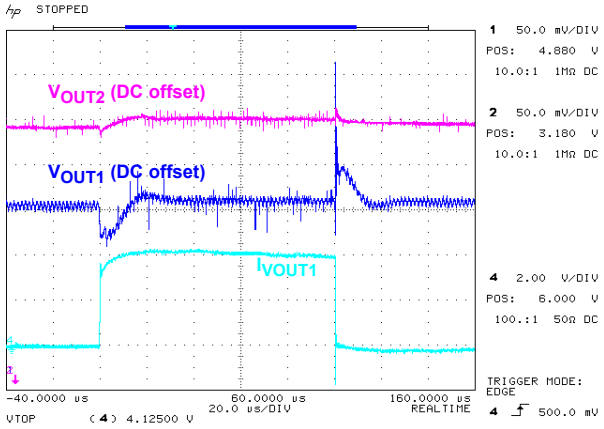


**FIGURE 14. ISL6549EVAL1 LOAD TRANSIENT RESPONSE**

Figure 15 shows the effect of a 1A load transient on the linear output, $V_{OUT2}$. As in Figure 14, some of the perturbation trickles into the cascaded regulator.

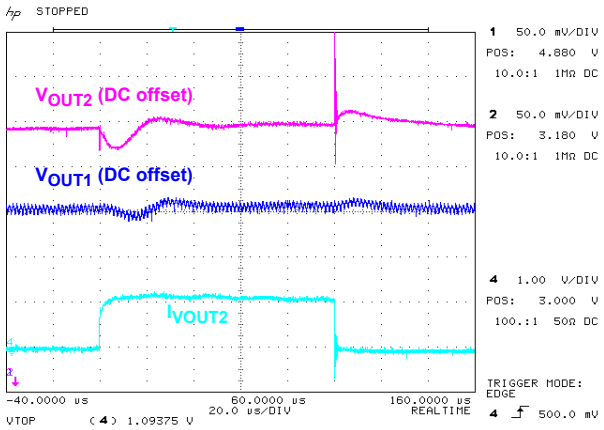


**FIGURE 15. ISL6549EVAL1 LOAD TRANSIENT RESPONSE**

### *PWM Conversion Efficiency*

Figure 16 highlights the ISL6549HI-EVAL1 board's conversion efficiency, including all bias power. The measurements were performed with the board operating at room temperature under natural convection and with $V_{IN1}$ = 5V. Three solid-line curves are shown, where measurements were performed with two MOSFETs for both upper and lower switch, at 3 different output voltages. Two dotted-line curves showcase efficiency with single MOSFETs for both switches, at two output voltages. Compared to the dual-MOSFET-per-switch curves, the single-MOSFET efficiencies are better at lower currents due to lower driving power losses and faster switching; however, single-MOSFET efficiencies drop off sooner than for the dual-MOSFETs at higher currents, as the

higher $r_{DS(ON)}$ of the single transistors lead to larger conduction losses as the output current increases. Due to the increased power dissipation, the single-MOSFET circuit is limited to a lower maximum output current level.

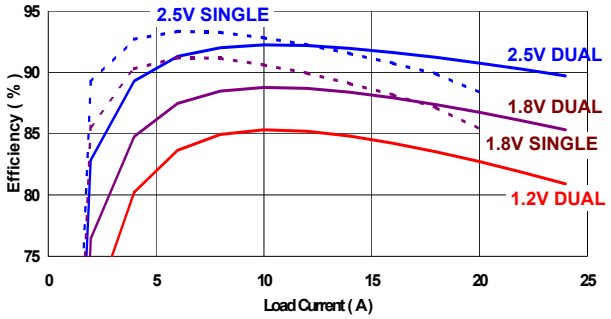


**FIGURE 16. ISL6549HI-EVAL1 MEASURED EFFICIENCY, WITH SEVERAL OUTPUT VOLTAGE AND FET COMBINATIONS, AT 600kHz.**

The range of curves displayed in Figure 17 were collected off the ISL6549LOW-EVAL1 board. The same MOSFET is used in each case, but the output voltage is varied.

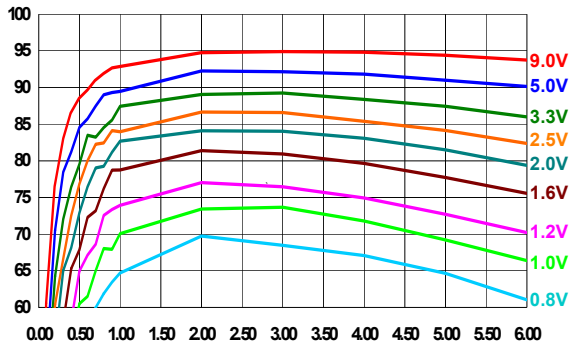


**FIGURE 17. ISL6549LOW-EVAL1 MEASURED EFFICIENCY, WITH $V_{IN1}$ = 12V, @575kHz, AT MULTIPLE OUTPUT VOLTAGES**

Figure 18 shows the variation in efficiency with switching frequency. Note that the board components were originally optimized for 600kHz, and were not adjusted for the other switching frequency settings. In general, lower frequencies result in less switching losses. However, lowering the frequency without adjusting the output inductor value results in increased ripple current which lowers the recorded efficiency; this very effect is clearly evident in the lower current range of the 200kHz measurement. capacitors. All the switching efficiency data was collected with the linear regulator output ($V_{OUT2}$) unloaded.

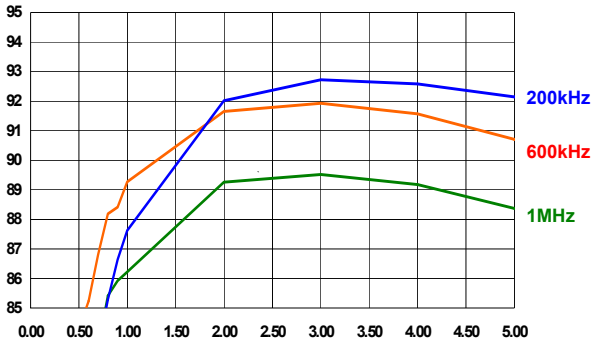


**FIGURE 18. ISL6549LOW-EVAL1 MEASURED EFFICIENCY, $V_{OUT1}$ = 5V, AT SEVERAL SWITCHING FREQUENCIES**

### *Boot Refresh*

In the event the PWM switching output reaches and sustains a 100% duty cycle for an extended period of time, there is a risk that the BOOT capacitor may discharge below an acceptable threshold. To prevent against this possibility, the ISL6549 will detect if UGATE has been at 100% duty cycle for 32 clock pulses, and force one full switching period LGATE pulse, to refresh the charge on the BOOT capacitor. The waveforms in Figure 19 show exactly this scenario. To force this special case, $V_{IN1}$ was set at 5V, just above the $V_{OUT1}$ setting of 4.9V. The measured forced LGATE pulse period is 1.6µs, resulting in an effective 96% maximum duty cycle.

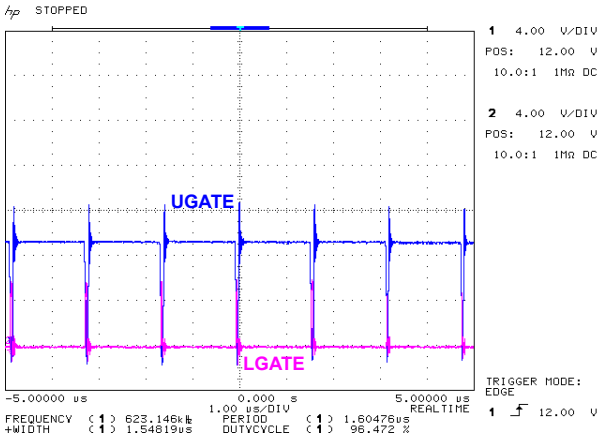


**FIGURE 19. ISL6549 BOOT REFRESH**

## Board Modifications

Any of the following changes should be made with the board powered down. Please refer to the ISL6549 datasheet as needed for more details.

### Power Supplies and Jumper Settings

The jumpers are for the user's convenience; they do not have to be used. There can be up to 3 power supplies ($V_{CC12}$, $V_{IN1}$, $V_{IN2}$); but some of them can be shared if desired. The output of either regulator can be used as the input to the other (assuming the voltages and currents are compatible). The input supplies can be ramped up in any sequence, but in order to avoid restart cycles, it is recommended that the $V_{CC12}$ supply be the last one to be brought up. If the order of the supplies cannot be changed, then another approach is to hold the FS_DIS pin low, via SW1, until all the input supplies are ready.

### Down-Converting From a Different Input Voltage

The ISL6549EVAL1 switcher design is primarily set up to use a 12V input supply as a bias and down-conversion source. If experimenting with a lower input voltage, be mindful of a few aspects (primarily for the switcher output):

- The minimum input voltage for down-conversion is dependent upon the output voltage setting and the power conversion efficiency of the PWM circuit at the given operating conditions. To have the circuit operate properly in a given set of operating conditions, the minimum voltage differential required between the input and the output of the PWM circuit increases with decreasing efficiency.
- The input-RMS current increases and reaches its peak as the duty cycle converges toward 50%.
- As the evaluation board (as shipped) was optimized for the specific operating parameters described in this app note; should these change, closely monitor the board temperatures and increase the output current only as allowed by the board thermal situation.
- A reduced input voltage will decrease the amount of loop gain the modulator contributes to the feedback loop; as a result, a more sluggish transient response can be expected.

For safety reasons, and to protect the board from inadvertent short-circuits, DO NOT TURN ON THE INPUT POWER UNTIL ALL OF THE INPUT AND OUTPUT CONNECTIONS HAVE BEEN MADE.

### Adjusting the Output Voltage

The output voltage can be adjusted via the external resistor-divider, according to the following equations. $V_{OUT1}$ is determined by R1 and R4 (See Figure 20); $V_{OUT2}$ is determined by R5 and R6 (See Figure 21). In order to avoid degradation of the input regulation DC setpoint, 1% resistors are recommended in the DC feedback path. Note that R1 is also part of the compensation network, so, for practical purposes, it is usually recommended to keep its value in the 1-5kΩ range.

$$R4 = \frac{R1 \cdot 0.8V}{VOUT1 - 0.8V}$$

$$R6 = \frac{R5 \cdot 0.8V}{VOUT2 - 0.8V}$$

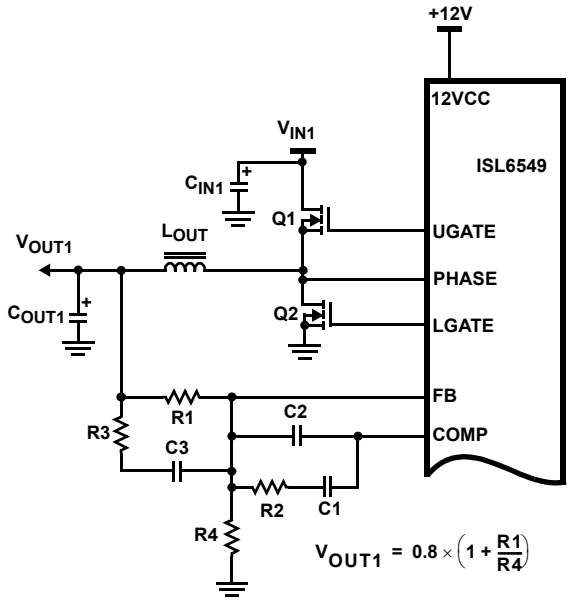


FIGURE 20. ADJUSTING $V_{OUT1}$

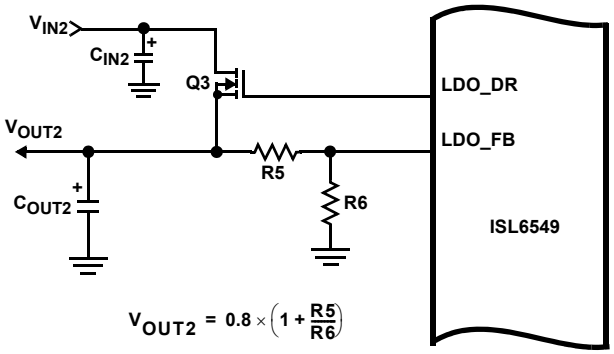


FIGURE 21. ADJUSTING $V_{OUT2}$

### Adjusting the Switching Frequency

The frequency of the switching regulator can be set as low as 150kHz, and up to 1MHz. The switching frequency helps determine the output ripple current, and the selection of the output inductor and capacitors. A single resistor (R7) to ground programs the frequency; see the datasheet for curves of frequency versus resistor values.

### Alternate FETs ($V_{OUT1}$ switcher)

There are four current ranges identified that this board can support, based on the MOSFETs used. The ranges are approximate, and depend upon the exact FET used, thermal

conditions (PCB area for heat-spreading, location of other heat sources, maximum ambient temperature, airflow, etc.), $V_{IN}$ and $V_{OUT}$ combinations, switching frequency, etc. The FET footprints are all connected in parallel, so only use one configuration at a time. The four ranges are as follows:

**High Power:** ~12A-20A. This configuration uses LFPAK or thermally-enhanced SO-8 packages, one/two upper FETs (Q1, Q3 on top of board); one/two lower MOSFETs (Q2, Q4 on bottom of board). The number of MOSFETs depends on the exact conditions, such as the current, and the duty cycle.

**Medium Power:** ~5A-12A. This configuration uses LFPAK or thermally-enhanced SO-8 packages, with one upper and one lower MOSFET. The same footprints as above are used; Q1 on top, and Q2 on the bottom of the board are preferred, as they are closer to the IC.

**Low Power:** ~1A-5A. This configuration uses a dual MOSFET (two devices in one thermally-enhanced SO-8 package) - use Q7 footprint on the bottom of the board.

**Very Low Power:** <1A. This configuration uses SOT-23 single MOSFETs for both upper and lower switches. Use Q8 for upper (bottom of board) and Q9 for lower (top of board).

### *Alternate FETs ($V_{OUT2}$)*

Separate from the above switcher ranges, the Linear output ($V_{OUT2}$) has two options:

**Low Power:** ~1W $P_D$. This configuration can use Q5, on top of the board, which can be an LFPAK or SO-8 FET. The power dissipation is limited primarily by the $\theta_{JA}$ of the package.

**Higher Power:** ~3W $P_D$. This configuration can use Q6, on the bottom of the board (TO-252). Monitor the FET temperature carefully as the load current is increased.

### *Alternate $C_{IN}$, $L_{OUT}$, or $C_{OUT}$*

These components can be changed for both regulators as desired. Capacitors might be changed for a different value or ESR, but make sure the voltage rating matches the output setting. The inductor can be changed for a different value, different DCR, or for a different maximum current; ensure the maximum load current (plus ripple current) is less than the saturation rating of the inductor under all conditions. Any change in any of the above components warrants a review of the suitability of the existing compensation component network.

### *Optional Component Footprints*

As some applications may benefit from one of these features, footprints are provided on the board for the following:

- a UGATE series resistor (R8; 0Ω) or an LGATE series resistor (R9; 0Ω). While the UGATE resistor is sometimes used to slow down the turn on/off of the upper MOSFET, the LGATE resistor is seldom to be employed.
- a schottky free-wheeling diode on the PHASE node (D1) can be used if the lower MOSFET has a fairly poor body diode, resulting in excessive negative ringing.
- an RC snubber on the PHASE node (R31, C32) helps absorb some of the energy in the PHASE node transitions and cut down on ringing. As the snubber works by dissipating energy, its employment results in decreased conversion efficiency
- the linear output should not require external compensation (R30, C30, C33), but these component footprints are provided in case either the output capacitor value or its ESR is too low, such as if only a ceramic capacitor is used. See the datasheet for more details.

### *Adjust Compensation*

Any significant change to the switcher circuit may require a re-calculation of the compensation network. Footprints are available for both type-2 and type-3. There are tools available for calculating compensation - inquire with your local Intersil contact for such assistance.

## *Board Layout*

The evaluation board is built on 1-ounce, 4-layer, printed circuit board (see the layout plots at the end of this document). The high-current board is designed to support a continuous output current level of up to 20A, while operating at room temperature, under natural convection cooling.

This board uses the recommended layout practices, within the constraints of also providing for input and output hardware, test points, and alternate FET footprints. The following list summarizes the most important ones, along with some references to the layout plots.

- The critical IC components (decoupling capacitors, compensation, FB resistor dividers, frequency resistor) are located next to the IC (or directly under it), with short traces to the IC pins. Pay special attention to the FB node of the compensation; it connects up to 5 components, with as short a trace as possible.
- The UGATE, LGATE and BOOT traces are wider than minimum and kept as short as reasonable, for low resistance.
- The IC section has a local “quiet” GND for these components (both on top and bottom layers) with vias to the GND plane (layer 2). This is meant to keep the GND for all of the quiet components close to the GND pin of the IC. The GND and PGND pins of the IC are both tied here. In addition, this GND is away from the FET switching GND, and out of the path of the FET GND current back to the $V_{IN1}$ GND post.

- The 12V to the VCC12 pin of the IC is somewhat isolated from the $V_{IN1}$ (if also 12V) through JP1; this keeps some of the switching noise of $V_{IN1}$ from the IC.
- The GND plane (layer 2) is one solid plane, except for openings for hardware and vias. There are additional GND straps on other layers as well.
- The various inputs and outputs use wide plane areas (on multiple layers in parallel) for low resistance and inductance. The $V_{IN}$ and PHASE planes also act as heatsinks for the drains of each FET (including the linear).
- The PHASE planes are the noisiest (high frequency and voltage), and do not overlap other planes (which could pick up the noise) except for the GND plane. The trace from the PHASE plane to the IC pin is carefully drawn (on bottom layer) to keep it away from sensitive signals; the BOOT capacitor is under the IC (bottom layer), between the BOOT and PHASE pins.
- There is very tight coupling between the FETs (Q1, Q3 on top layer; Q2 and Q4 on bottom layer) and the $V_{IN1}$ ceramic capacitors (C15, C20 on top layer). The bulk capacitor C13 is also nearby.
- On top layer, there is a separate low current trace from $V_{OUT1}$ (near the load) to the FB1 resistor divider (R1, R4); this places the point that is regulated as close to the load as practical. The $V_{OUT2}$ trace on top layer to the LDO_FB resistor divider (R5, R6) is not as isolated.

## Conclusion

The ISL6549EVAL1 evaluation board showcases a versatile, simple to implement, high-performance dual regulator, suitable for providing power management and control in a variety of 12V applications. The high-current PWM MOSFET drivers of the ISL6549 yield a highly efficient power conversion solution with a reduced number of external components in a compact footprint, while the linear controller offers the means to implement a second, lower current output.

## References

Data sheet: FN9168

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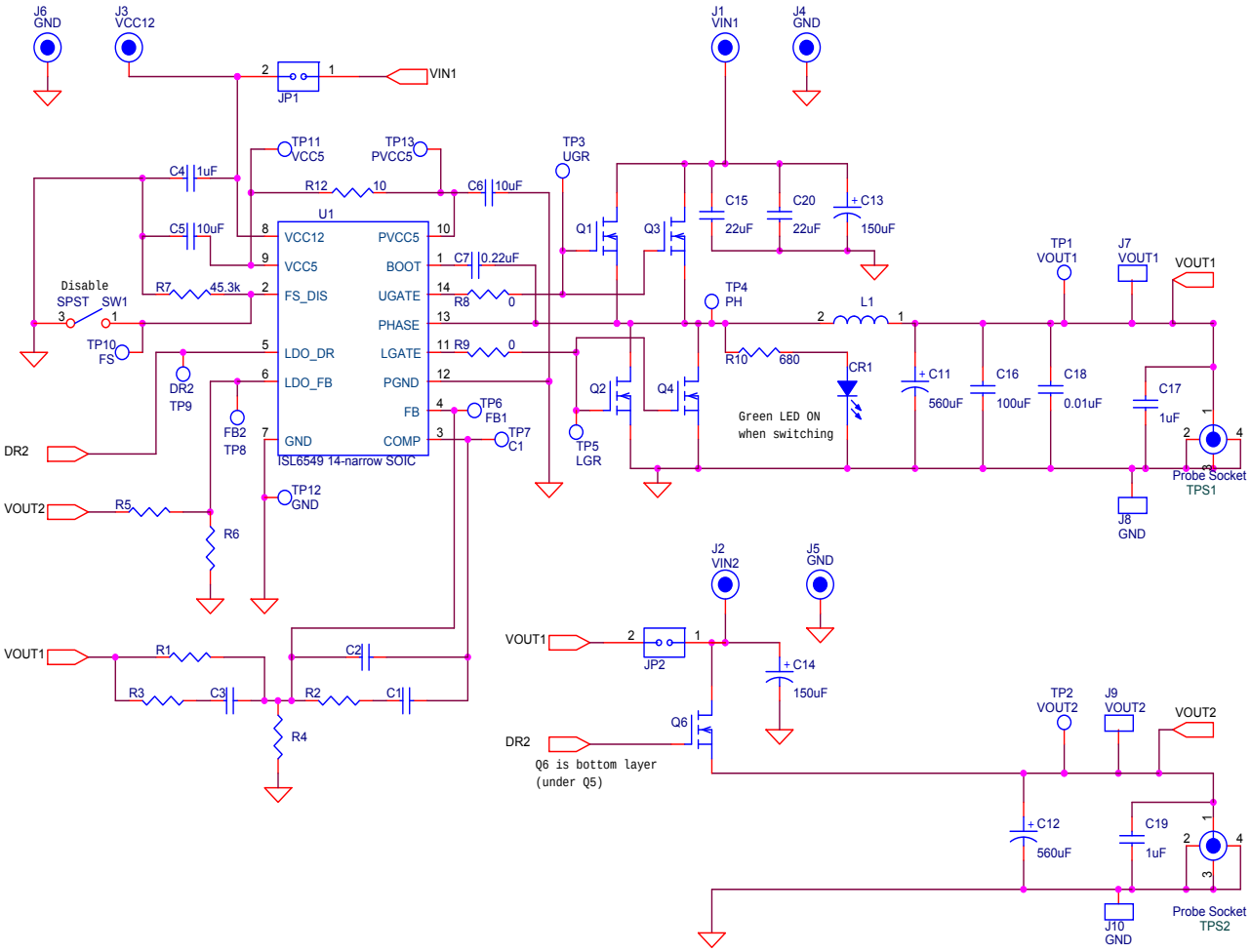
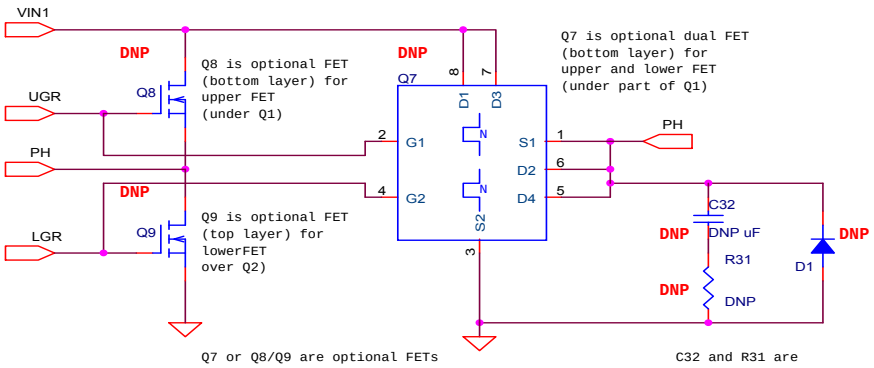
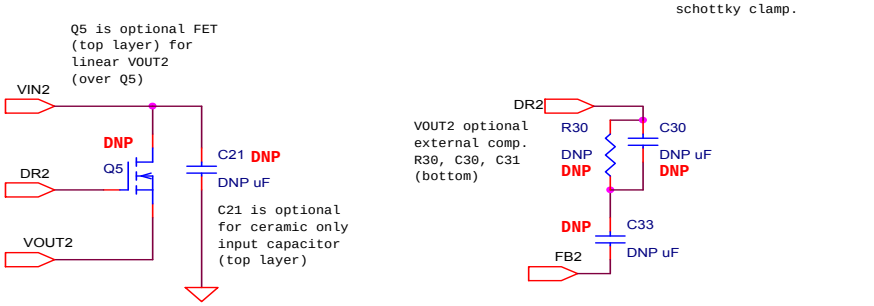
## *ISL6549EVAL1 Rev B Schematic*



## *ISL6549LOW-EVAL1 (Rev B) Bill of Materials*

### *Low (1A - 5A) Current; $V_{OUT1}$ = 5V@1A, $V_{OUT2}$ = 3.3V@1A*

| REFERENCE | PART NUMBER | DESCRIPTION | FOOTPRINT | MANUFACTURER | QUANTITY |
|---|---|---|---|---|---|
| C1 | | 33nF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C2 | | 0.022nF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C4 | | 1µF Capacitor, X7R, 16V | 0805 | | 1 |
| C5, 6 | | 10µF Capacitor, X7R, 6.3V | 0805 | | 2 |
| C7 | | 0.1µF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C11, 12 | 10SVP560M or similar | 560µF OS-CON Capacitor, 10V, ESR = 13mΩ | F12 | Sanyo | 2 |
| C13, 14 | 16SVP150M or similar | 150µF OS-CON Capacitor, 16V, ESR = 30mΩ | F8 | Sanyo | 2 |
| C15 | | 22µF Capacitor, X7R, 16V | 1206 | | 1 |
| C16 | | 100µF Capacitor, X7R, 6.3V | 1206 | | 1 |
| C17, 19 | | 1µF Capacitor, X7R, 6.3V | 0603 | | 2 |
| C18 | | 0.01µF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C3, 30, 32, 33 | | | 0603 | | DNP |
| C20, 21 | | | 1206 | | DNP |
| CR1 | CMD91-21VGC/TR10 | LED, green | | | 1 |
| D1 | | | SMA | | DNP |
| JP1, 2 | 68000-2336, 71363-102 | 2 pin header and shunt | | Berg | 2 |
| J1-3 | 111-0102-001 | Binding posts (red) | | Johnson | 3 |
| J4-6 | 111-0103-001 | Binding posts (black) | | Johnson | 3 |
| J7-10 | 1514-2 | Turrets | | | 3 |
| L1 | SD1201 (or similar) | Inductor, 4.7µH, 9.5mΩ, 8A | | Falco | 1 |
| Q6 | MTD3055VL or similar | 180mΩ max at 5.0V, 6A; | DPAK | ON | 1 |
| Q7 | IRF7313 or similar | 46mΩ max at 4.5V, 4.7A; | SOIC-8 | IR | 1 |
| Q1-5 | | | LFPAK | | DNP |
| Q8, 9 | | | SOT23 | | DNP |
| R1, 5 | | Resistor, 1.00kΩ, 1% | 0603 | | 2 |
| R2 | | Resistor, 14.7kΩ, 1% | 0603 | | 1 |
| R4 | | Resistor, 191Ω, 1% | 0603 | | 1 |
| R6 | | Resistor, 324Ω, 1% | 0603 | | 1 |
| R7 | | Resistor, 45.3kΩ, 1% | 0603 | | 1 |
| R8, 9 | | Resistor, 0Ω | 0603 | | 2 |
| R10 | | Resistor, 680Ω | 0603 | | 1 |
| R12 | | Resistor, 10Ω | 0603 | | 1 |
| R3, 30, 31 | | | 0603 | | DNP |
| SW1 | SPST GT12MSCKE | SPST Switch | | C&K | 1 |
| TPS1, 2 | 131-4353-00 | Probe socket | | Tektronix | 2 |
| TP1-13 | 5002 | Test pins | | | 13 |
| U1 | ISL6549 | PWM and Linear Controller | SOIC-14 | Intersil | 1 |
| U3 | | | QSOP-16 | | DNP |
| U4 | | | QFN (4x4) - 16 | | DNP |
| | | ISL6549EVAL1revB PCB board | | | 1 |
| | | Rubber feet | | | 4 |

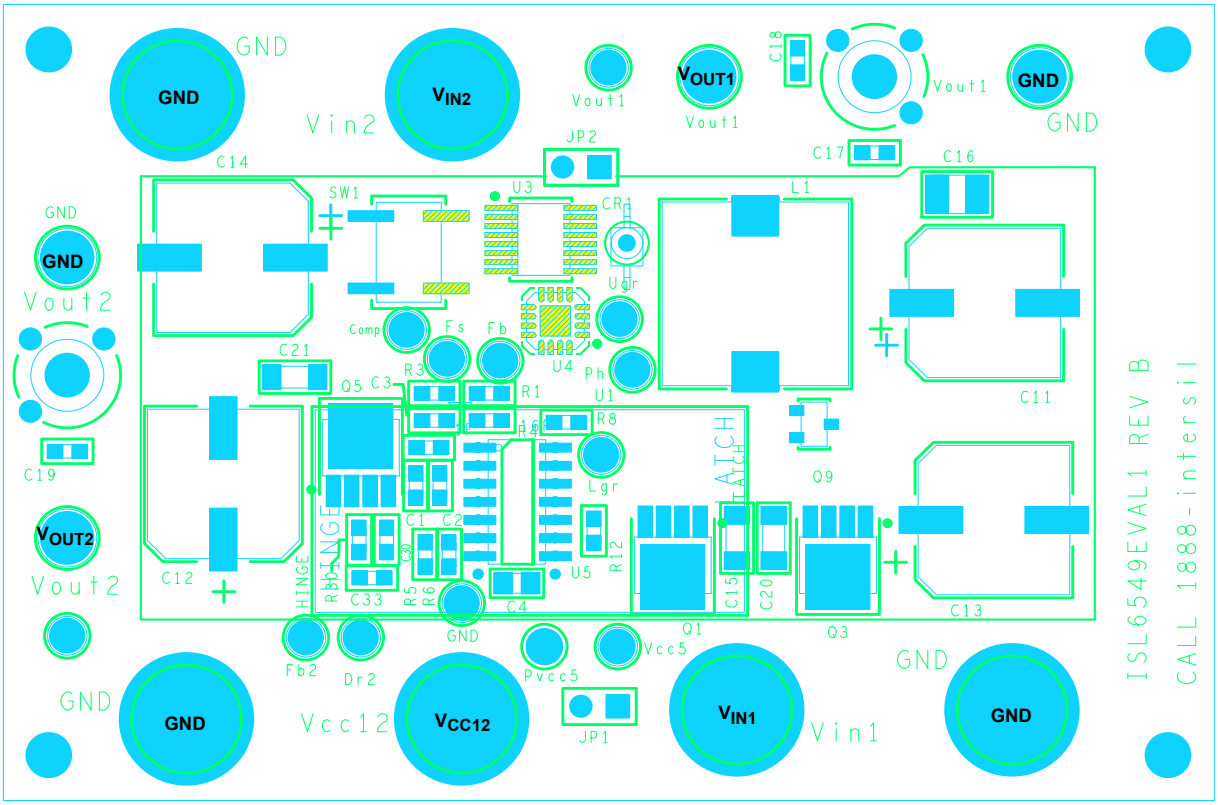
## *ISL6549HI-EVAL1 (Rev B) Bill of Materials*

***High (12A - 25A) Current; $V_{OUT1}$ = 1.2V @20A, $V_{OUT2}$ = 1.6V@1A***

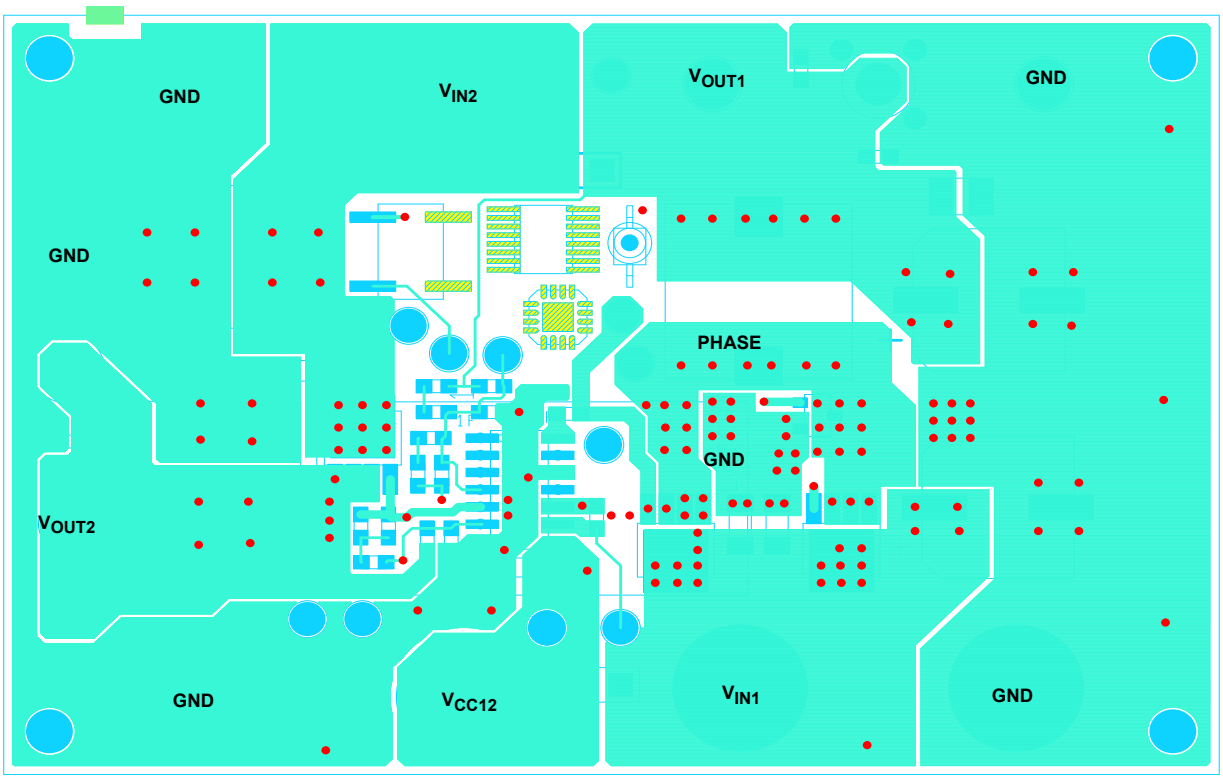
| REFERENCE | PART NUMBER | DESCRIPTION | FOOTPRINT | MANUFACTURER | QUANTITY |
|---|---|---|---|---|---|
| C1 | | 33nF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C2 | | 0.022nF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C4 | | 1µF Capacitor, X7R, 16V | 0805 | | 1 |
| C5, 6 | | 10µF Capacitor, X7R, 6.3V | 0805 | | 2 |
| C7 | | 0.22µF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C11, 12 | 10SVP560M or similar | 560µF OS-CON Capacitor, 10V, ESR = 13mΩ | F12 | Sanyo | 2 |
| C13, 14 | 16SVP150M or similar | 150µF OS-CON Capacitor, 16V, ESR = 30mΩ | F8 | Sanyo | 2 |
| C15, 20 | | 22µF Capacitor, X7R, 16V | 1206 | | 2 |
| C16 | | 100µF Capacitor, X7R, 6.3V | 1206 | | 1 |
| C17, 19 | | 1µF Capacitor, X7R, 6.3V | 0603 | | 2 |
| C18 | | 0.01µF Capacitor, X7R, 6.3V | 0603 | | 1 |
| C21 | | | 1206 | | DNP |
| C3, 30, 32, 33 | | | 0603 | | DNP |
| CR1 | CMD91-21VGC/TR10 | LED green CMD91-21VGC/TR10 | | | 1 |
| D1 | | | SMA | | DNP |
| JP1, 2 | 68000-2336, 71363-102 | 2 pin jumper and shunt | | Berg | 2 |
| J1-3 | 111-0102-001 | Binding posts (red) | | Johnson | 3 |
| J4-6 | 111-0103-001 | Binding posts (black) | | Johnson | 3 |
| J7-10 | 1514-2 | Turrets | | | 3 |
| L1 | IHLP-5050EZ-01 | Inductor, 1.5µH, 3.4  23A | | Vishay | 1 |
| Q1, 3 | HAT2168 | 13.5mΩ max at 4.5V, 15A, Qgd = 2.4 nC | LFPAK | Renesas | 2 |
| Q2, 4 | HAT2165H | 5.3mΩ max at 4.5V, 27.5A, Qgd = 7.1 nC | LFPAK | Renesas | 2 |
| Q6 | MTD3055VL or similar | 180mΩ max at 5.0V, 6A; | DPAK | ON | 1 |
| Q5 | | | LFPAK | | DNP |
| Q7 | | | SOIC-8 | | DNP |
| Q8, 9 | | | SOT23 | | DNP |
| R1, 5, 6 | | Resistor, 1.00kΩ, 1% | 0603 | | 3 |
| R2 | | Resistor, 14.7kΩ, 1% | 0603 | | 1 |
| R4 | | Resistor, 2.00kΩ, 1% | 0603 | | 1 |
| R7 | | Resistor, 45.3kΩ, 1% | 0603 | | 1 |
| R8, 9 | | Resistor, 0Ω | 0603 | | 2 |
| R10 | | Resistor, 680Ω, | 0603 | | 1 |
| R12 | | Resistor, 10Ω | 0603 | | 1 |
| R3, 30, 31 | | Resistor, TBDkΩ, 1% | 0603 | | DNP |
| SW1 | SPST GT12MSCKE | SPST Switch | | C&K | 1 |
| TPS1, S2 | 131-4353-00 | Probe socket | | Tektronix | 2 |
| TP1-13 | 5002 | Test pins | | | 13 |
| U1 | ISL6549 | ISL6549 | SOIC-14 | Intersil | 1 |
| U3 | | | QSOP-16 | | DNP |
| U4 | | | QFN (4x4) - 16 | | DNP |
| | | ISL6549EVAL1revB PCB board | | | 1 |
| | | Rubber feet | | | 4 |

## *ISL6549EVAL1 Layout*

**TOP SILK SCREEN**

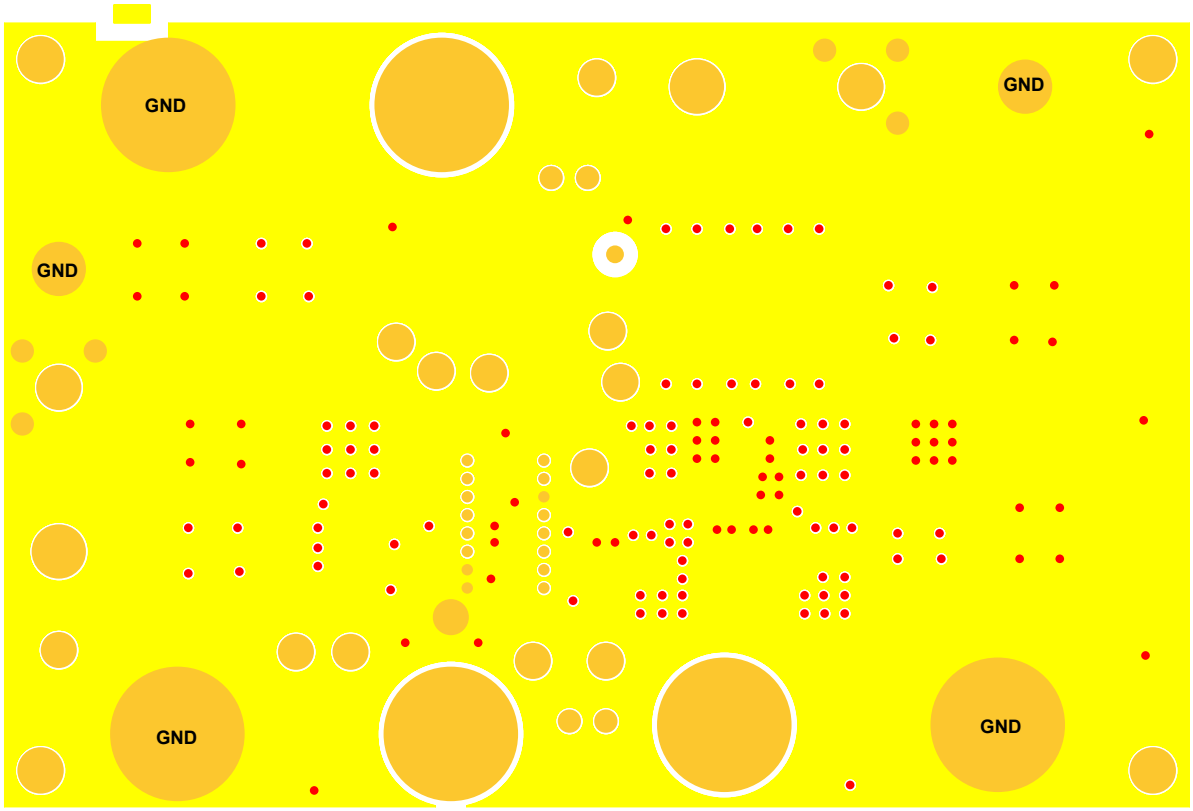



**TOP LAYER (1st)**

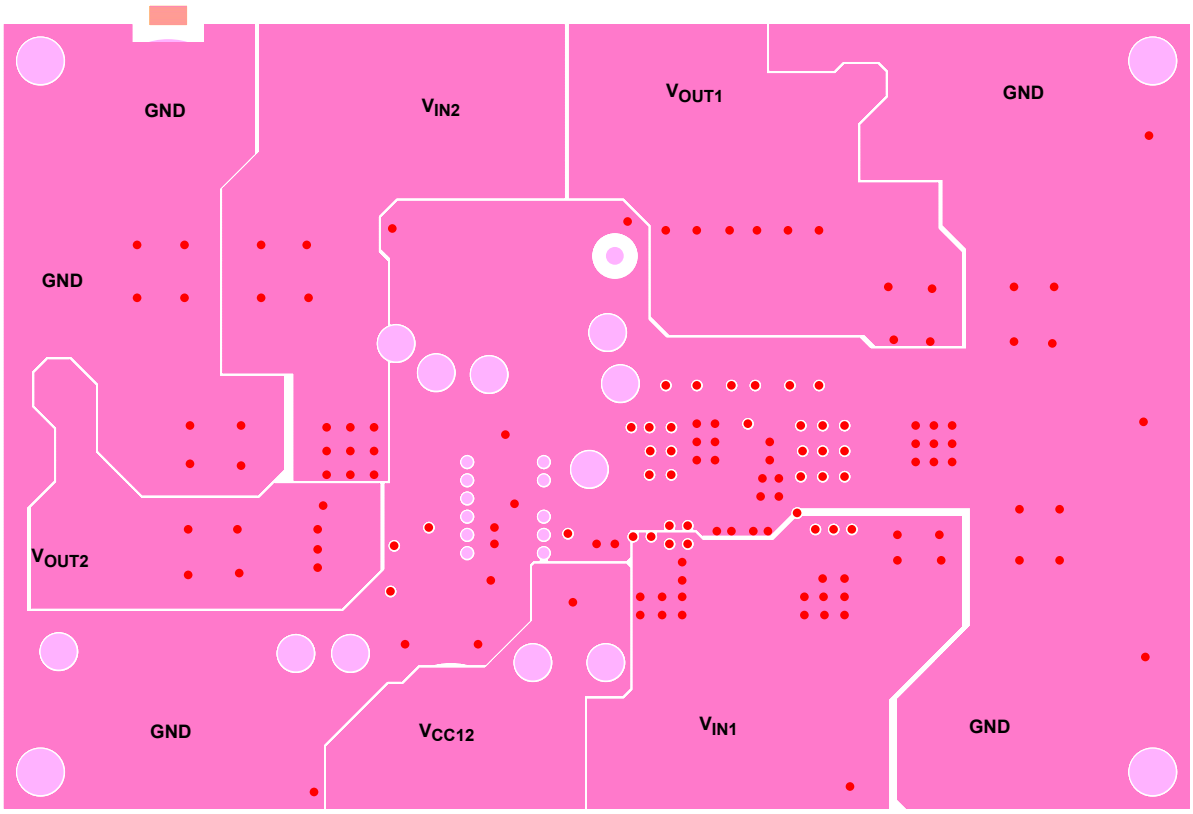


## *ISL6549EVAL1 Layout* (Continued)

GROUND LAYER (2nd)

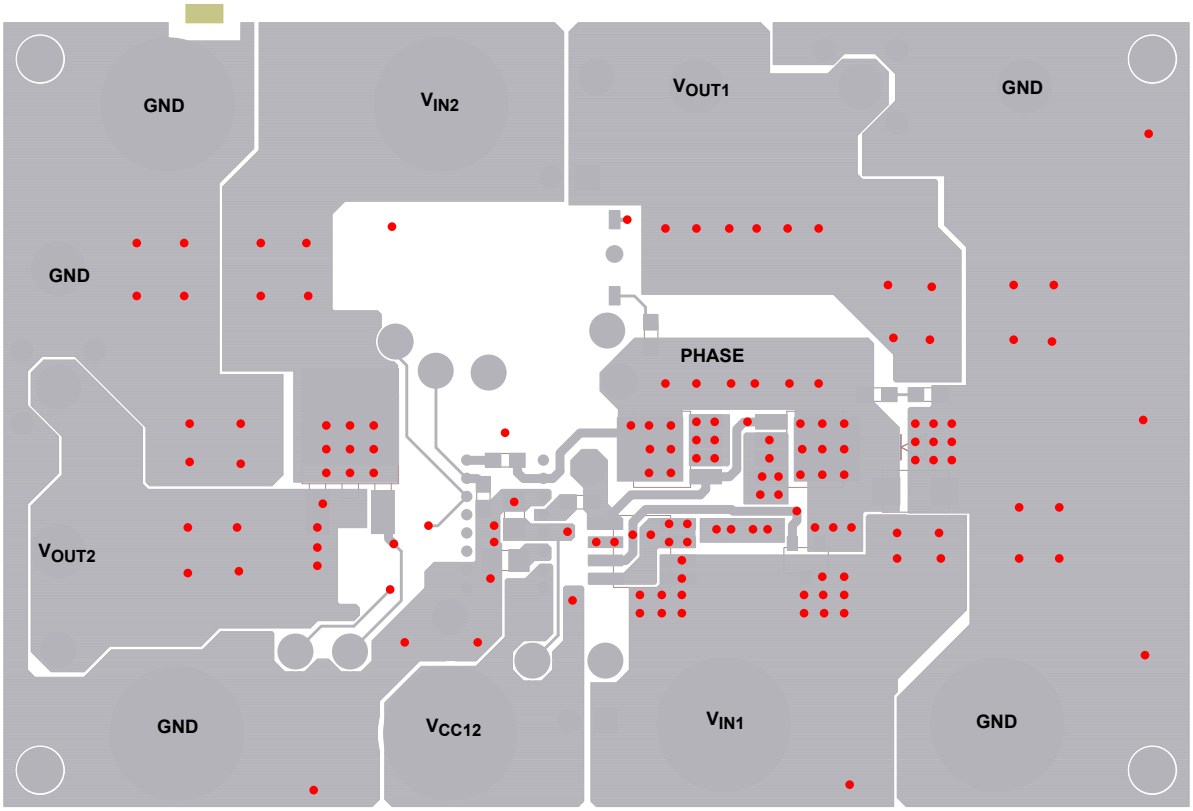



POWER LAYER (3rd)

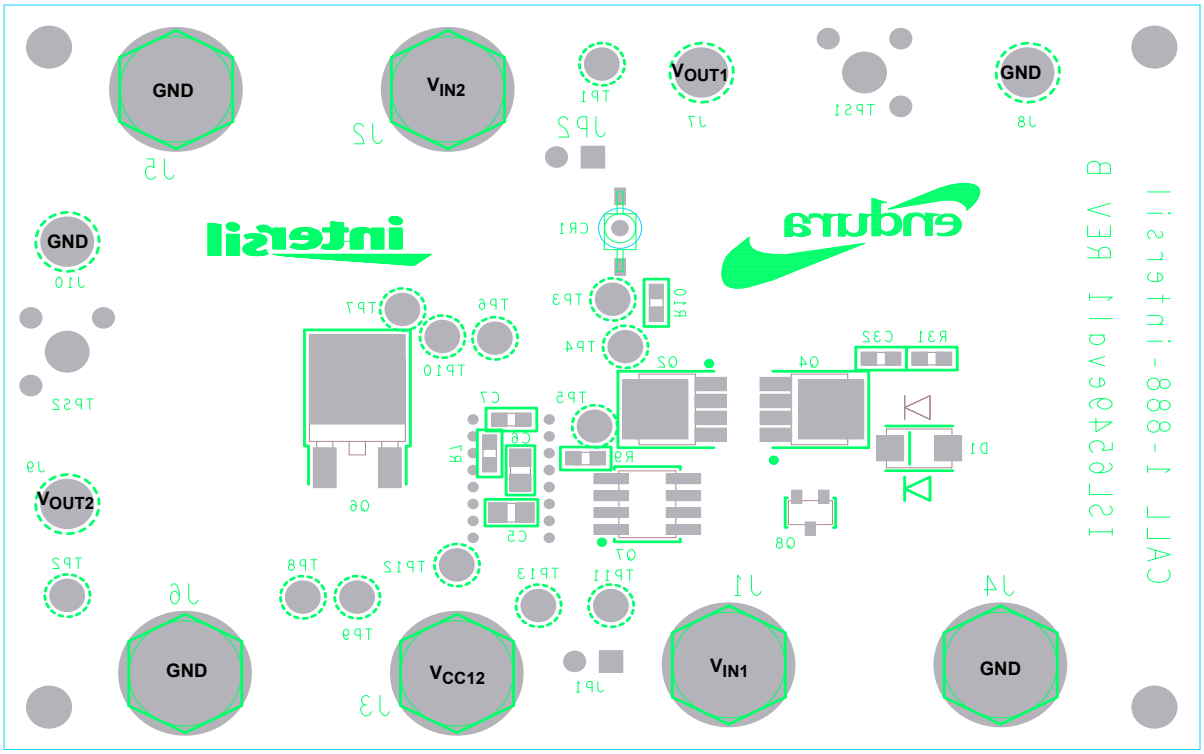


## *ISL6549EVAL1 Layout* (Continued)

**BOTTOM LAYER (4th)**




**BOTTOM SILK SCREEN**



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