ISL70002SEHEVAL2Z

Evaluation Board

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ISL70002SEHEVAL2Z

The ISL70002SEHEVAL2Z evaluation board is designed to evaluate the performance of the ISL70002SEH in a dual regulator current sharing configuration. The ISL70002SEH is a TID and SEE hardened 12A synchronous buck regulator IC with integrated MOSFETs intended for space applications. For more detailed information, please refer to the datasheet ISL70002SEH.

The ISL70002SEHEVAL2Z evaluation board accepts an input voltage of 3V to 5.5V and provides a regulated default output voltage of 1.0V configured to current share to provide 19A total output current, assuming ±27% worst-case current share accuracy. The output can be quickly adjusted to an alternate voltage using the onboard potentiometer. A PGOOD (power-good) signal goes high and lights a green LED to indicate that the output voltage is within a ±11% typical regulation window. A toggle switch (SW1) is provided to conveniently enable or disable the regulators.

The ISL70002SEHEVAL2Z evaluation board can be set to run from the nominal 500kHz or 1MHz internal oscillator of the master ISL70002SEH with the two devices synchronized 180° out-of-phase to reduce input RMS ripple current.

Specifications

This board has been configured for the following operating conditions:

- 96% peak efficiency at 3.3V V_{IN}, 2.5V V_{OUT}, 500kHz
- 19A max current

Key Features

- Dual regulator current sharing solution
- Dual-sided PCB

References

ISL70002SEH Datasheet

Ordering Information

PART NUMBER	DESCRIPTION
ISL70002SEHEVAL2Z	ISL70002SEH Dual Phase Current Share

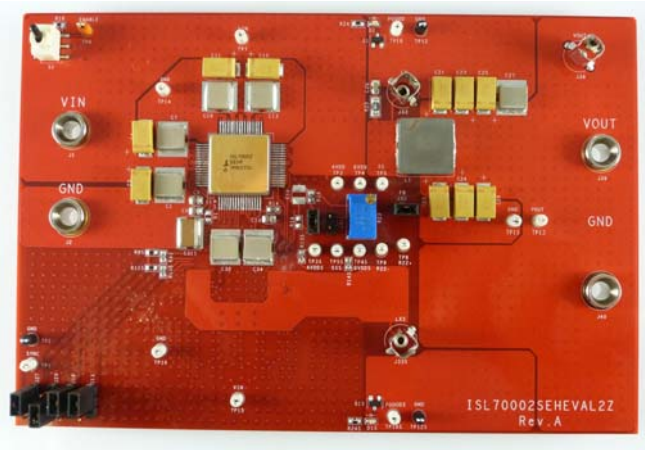


FIGURE 1. TOP VIEW

FIGURE 2. BOTTOM VIEW

What's Inside

The Evaluation Board Kit contains the following materials:

- ISL70002SEHEVAL2Z Evaluation Board
- ISL70002SEH Datasheet.
- ISL70002SEH Dual Phase Current Share Evaluation Board User Guide

Recommended Test Equipment

- 0 to 6V power supply with at least 35A current capability
- Electronic load capable of sinking current up to 21A
- Digital multimeters (DMMs)
- A 500MHz dual or quad trace oscilloscope
- Frequency response analyzer (0.01Hz to 10MHz)

Quick Start

1. Toggle S1 to the OFF position.
2. Turn on the power supply. Set the output voltage to 5V. Turn off the power supply.
3. Connect the positive lead of the power supply to VIN and the negative lead of the power supply to GND.
4. Ensure jumpers J30, J32, J27, J29, J13 and J18 are installed. This is the default shipping configuration.
5. Connect one DMM to monitor the input voltage from TP7 to TP14 and another DMM to monitor the output voltage from TP13 to TP11.
6. Connect oscilloscope to probe jacks LX and LXS to monitor the rectangular waveform on the LX pins of the master and slave ICs respectively.
7. Connect oscilloscope to probe jack VOUT to monitor the output voltage. Ripple voltage is customarily measured with 20MHz bandwidth limiting and AC coupling.
8. Turn on power supply and toggle S1 to the ON position.
9. Verify the output voltage is 1.0V ±3% and the frequency of the LXx waveform is 500kHz ±10%

Evaluating ISL70002SEHEVAL2Z Dual Phase Current Share Operation

Two ISL70002SEH devices are capable of operating as a single two-phase regulator with nearly twice the load current capacity. In this mode, a redundant current sharing bus balances the load current between the two devices and communicates any fault conditions. One ISL70002SEH is designated the master and the other the slave. The master ISHSL pin is connected to DGND and the slave ISHSL pin is connected to DVDD. The ISHEN pins on both master and slave are connected to DVDD. The SYNC, ISHA, ISHB, ISHC, ISHREFA, ISHREFB, ISHREFC, ISHCOM and FB pins are connected from the Master to the Slave and the REF pins are tied with a 10Ω resistor. Configured this way, the two-phase regulator nearly doubles the load current capacity, limited only by the current share match tolerance. See Figure 3 for an ISL70002SEH block diagram of the current sharing configuration.

In this master/slave configuration the two ISL70002SEH ICs operate ~180° out-of-phase to minimize the input ripple current, effectively operating as a single IC at twice the switching frequency. The master phase uses the falling edge of the SYNC clock to initiate the master switching cycle with the nonoverlap period before the rising edge of LX, while the slave phase internally inverts the SYNC input and uses the falling edge of the inverted copy to start its switching cycle. This is independent of whether the master phase is configured for an external clock (master M/S = DGND) or its internal clock (master M/S = DVDD). The master error amplifier and compensation controls the two phase regulator while the slave error amplifier is disabled. The "ISL70002SEHEVAL2Z Schematic" on page 9 shows the complete configuration connection used on this evaluation platform for the Master and Slave IC.

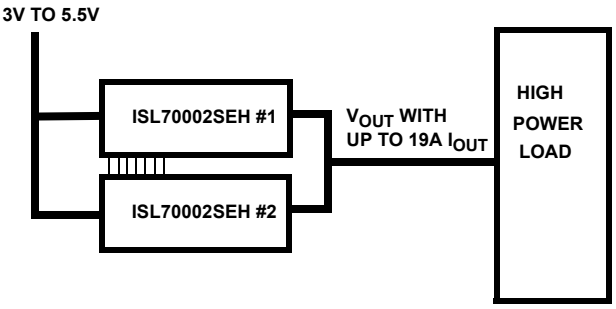


FIGURE 3. DUAL ISL70002SEH CURRENT SHARE BLOCK DIAGRAM

Figure 4 shows the turn on of the ISL70002SEHEVAL2Z into a 0.1Ω load, the load sharing for the ~10A total load is ~44% for the master device and ~56% for the slave device. Figure 5 shows a transient load from 0A to 14A with a current sharing ratio of 45% to 55% for the master to slave respectively at max current. Both of these current sharing ratios are within the share guidance provided as worst case.

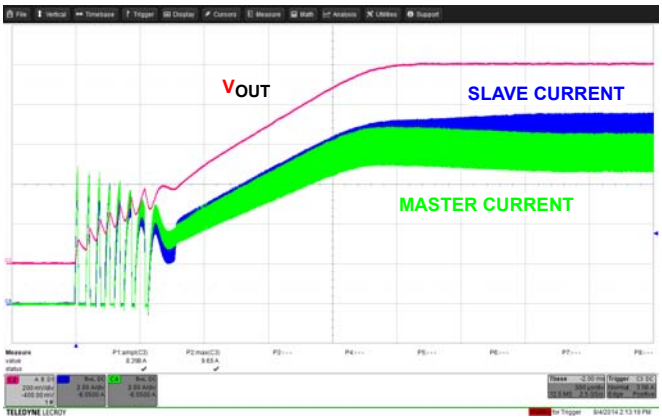


FIGURE 4. DUAL ISL70002SEH SHARING UPON TURN-ON INTO 0.055Ω LOAD, V_{IN} = 3.3V, V_{OUT} = 1.0V, 1MHz

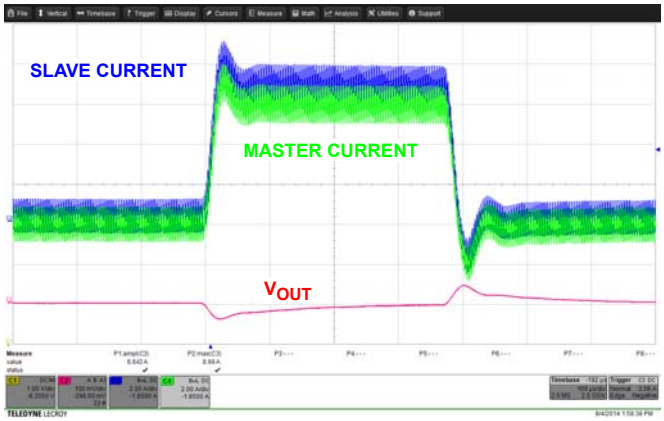


FIGURE 5. DUAL ISL70002SEH SHARING of 0 TO 14A LOAD CURRENT TRANSIENT STEP, V_{IN} = 3.3V, V_{OUT} = 1.0V, 1MHz

Loop Gain Measurements

Loop measurement is needed to analyze the robustness of the power converter design. The evaluation board comes equipped with a resistor (R_{22}) between the output voltage and the compensation network around the error amplifier, essentially breaking the loop and use test points TP9 and TP8 to inject the AC signal differentially across R_{22} (shorted by J32) and measure the loop response with the Frequency Response Analyzer. See Figures 26 and 27 for phase/gain plots. For more detailed information on loop measurement techniques refer to references [1] and [2].

Switching Frequency Selection

The ISL70002SEH can operate at a 500kHz or a 1MHz nominal switching frequency. Jumper connector J29 labeled 'FSEL' is used to set the switching frequency for both the master and slave devices. Use Table 1 to configure the evaluation board to the desired switching frequency.

TABLE 1. SETTINGS FOR CONNECTOR FSEL

PINS	CONDITION	SWITCHING FREQUENCY (kHz)
1, 2	SHORT to GND	500
2, 3	SHORT to VIN	1000

Evaluating Other Output Voltages

With a jumper installed on jumper J30, the ISL70002SEHEVAL2Z output voltage is preset to 1.0V. For quick evaluation of other output voltages, the ISL70002SEHEVAL2Z provides an on board potentiometer (R_{23}) on the feedback network, as shown in Figure 4.

To modify the output voltage through R_{23}, flip SW1 to the OFF position. Open J30 and short J31. Enable the ISL70002SEH and measure the output voltage with a DMM. Use a small flat head screw driver to turn the potentiometer until the desired output voltage is achieved.

Changing the Turn-On Voltage

The POR circuitry prevents the controller from attempting to soft-start before sufficient bias is present at the PVINx pins and is selectable on this evaluation board. The POR threshold is controlled by the PORSEL pin connection with J27. For a nominal 5V supply voltage, PORSEL should be connected to DVDD. For a nominal 3.3V supply voltage, PORSEL should be connected to DGND. For nominal supply voltages between 5V and 3.3V, PORSEL should be connected to DGND.

Slope Compensation

The SC0 (J18) and SC1 (J31) pins select four levels of current mode slope compensation. In current mode buck regulators, when the duty cycle approaches and exceeds 50%, the regulator will operate in subharmonic oscillation without slope compensation. Slope compensation is widely considered unnecessary if the duty cycle is held below 40% and provides better phase margin. Transient duty cycles must be taken into consideration when selecting the level of slope compensation. Table 2 describes the amount of effective current that is added to the output power stage signal that is used in the PWM modulator.

TABLE 2.

FSEL	SC1	SC0	SLOPE COMP (A/µs)
DGND	DGND	DGND	0.8
DGND	DGND	DVDD	1.6
DGND	DVDD	DGND	3.3
DGND	DVDD	DVDD	6.6
DVDD	DGND	DGND	1.7
DVDD	DGND	DVDD	3.4
DVDD	DVDD	DGND	6.7
DVDD	DVDD	DVDD	13.4

ISL70002SEHEVAL2Z Efficiency Testing

This dual current share application board is design with ISL70002SEH devices on both the top and bottom of the PCB. Because of this, the typical lab test methods of ambient air temperature control were unsuitable. In this instance we used calibrated temperature baths filled with electrically inert fluids to provide the ambient temperature the boards and ICs were exposed to. The immersion in a constantly swirling liquid controlled to within 0.1°C, makes it reasonable to assume that the ISL70002SEH case temperature is equal to the liquid's controlled temperature. The power efficiency curves (Figures 6 through 25) were all produced using this best case thermal test condition method. This testing presents the efficiency curves with a known case temperature making the Si junction temperature calculation simpler and more robust. Testing with typical ambient air temperature control methods will result in lower efficiency.

Schematic and BOM

A schematic and BOM of the ISL70002SEHEVAL2Z evaluation board are shown on page 9 and page 10, respectively. The schematic indicates the test points, which allow many nodes of the evaluation circuit to be monitored directly. The BOM shows components that are representative of the types needed for a design, but these components are not space qualified. Equivalent space qualified components would be required for flight applications.

Layout Guidelines

Layout is very important in high frequency switching converter design, particularly in a dual PWM IC configuration such as the ISL70002EVAL2Z. The resulting current transitions from one power device to another and causes voltage spikes across the interconnecting impedances and parasitic circuit elements. These voltage spikes can degrade efficiency, radiate noise into the circuit, and lead to device overvoltage stress. Careful component layout and printed circuit board design minimizes these voltage spikes. The following generic guidelines can be used:

1. Use an eight layer PCB with 2 ounce (70µm) copper or equivalent in thinner layers.
2. 2 layers should be dedicated for ground plane.
3. Top and bottom layers are used primarily for the ICs and signals, but can also be used to increase the VIN, VOUT and ground planes as required.
4. Connect all AGND, DGND and PGNDx pins directly to the ground plane. Connect all PVINx pins directly to the VIN portion of the power plane.
5. Locate ceramic bypass capacitors as close as possible to the PWM ICs. Prioritize the placement of the bypass capacitors on the pins of ICs in the order shown: PVINx, REF, AVDD, DVDD, SS, EN, PGOOD.
6. Locate the output voltage resistive divider as close as possible to the FB pin of the IC. The top leg of the divider should connect directly to the load and the bottom leg of the resistive divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.
7. Use a small island of copper to connect the LXx pins of the regulator to the inductor, to minimize the routing capacitance that degrades efficiency. Separate the island from ground and power planes as much as possible.
8. Keep all signal traces as short as possible.
9. A small series snubber (R25 and C20) connected from the LXx pins to the PGNDx pins may be used to dampen ringing on the LXx pins if desired.

Thermal Management for Ceramic Package

For optimum thermal performance, generally place a pattern of vias on the layer of the PCB directly underneath the IC and connect the vias to the plane which serves as a heatsink. In this specific case, since the evaluation platform was size optimized even with 2 ICs, the ICs are mounted on each side of the PCB and offset from each other to provide some PCB Cu area for each IC to dissipate heat into. In general, to ensure good thermal contact, thermal interface material such as a Sil-Pad or thermally conductive epoxy should be used to fill the gap between the vias and the bottom of the IC of the ceramic package. Additionally, the ISL70002SEH comes in both a thermally enhanced package with a heat spreading bottom which can be directly soldered to the PCB Cu pattern and a non thermally enhanced package which is the option installed on the ISL70002EVAL2Z.

Lead Strain Relief

The package leads protrude from the bottom of the package and the leads need forming to provide strain relief. On the ceramic bottom package R64.A, the Sil-pad or epoxy maybe be used to fill the gap left between the PCB board and the bottom of the package when lead forming is completed. On the heatsink option of the package R64.C, the lead forming should be made so that the bottom of the heatsink and the formed leads are flush.

General Heatsink Mounting Guidelines

The R64.C package option has a heatsink mounted on the underside of the package. The following JESD-51x series guidelines may be used to mount the package:

1. Place a thermal land on the PCB under the heatsink.
2. The land should be approximately the same size as to 1mm larger than the 10.16x10.16mm heatsink.
3. Place an array of thermal vias below the thermal land.
   - Via array size: ~9x9 = 81 thermal vias.
   - Via diameter: ~0.3mm drill diameter with plated copper on the inside of each via.
   - Via pitch: ~1.2mm.
   - Vias should drop to and contact as much metal area as feasible to provide the best thermal path.

Heatsink Electrical Potential

The heatsink is connected to pin 50 within the package; thus the PCB design and potential applied to pin 50 will therefore define the heatsink potential. In this evaluation board pin 50 and the heatsink are connected to ground.

Heatsink Mounting Materials

In the case of electrically conductive mounting methods (conductive epoxy, solder, etc) the thermal land, vias and connected plane(s) below must be the same potential as pin 50.

In the case of electrically nonconductive mounting methods (nonconductive epoxy), the heatsink and pin 50 could have different electrical potential than the thermal land, vias and connected plane(s) below.

References

[1] Venable Industries, Venable Technical Paper #1, "Testing Power Sources for Stability"

[2] Dr. Ray Ridley, "Loop Gain Measurement Injection Technique"

Typical Performance Curves

Efficiency data taken with (Best Case Thermal Condition) the ISL70002SEHEVAL2Z immersed in a calibrated temperature liquid bath to ensure notated ambient and package case temperatures on both IC component sides of this evaluation board. In typical lab air ambient test condition efficiency will be lower.

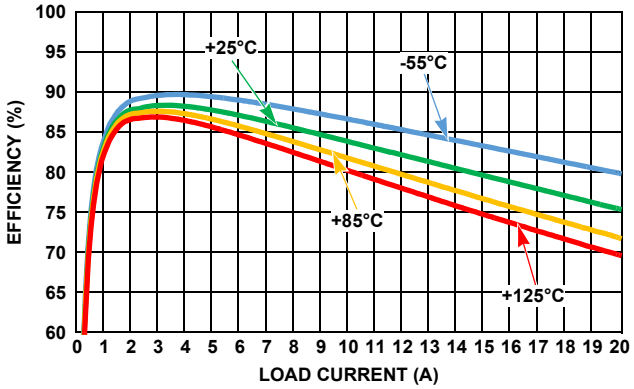


FIGURE 6. EFFICIENCY vs LOAD vs CASE TEMPERATURE
V_{IN} = 3.3V, V_{OUT} = 1.0V, f_{SW} = 500kHz

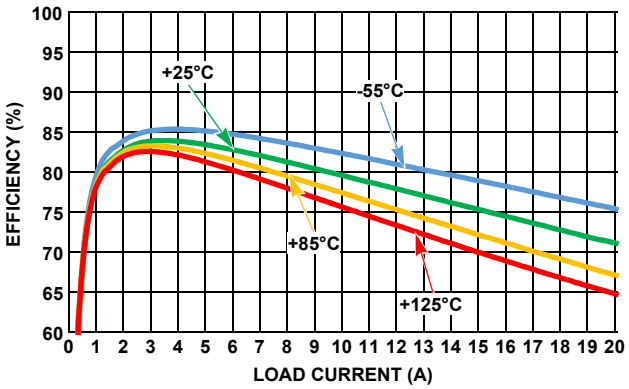


FIGURE 7. EFFICIENCY vs LOAD vs CASE TEMPERATURE
V_{IN} = 3.3V, V_{OUT} = 1.0V, f_{SW} = 1MHz

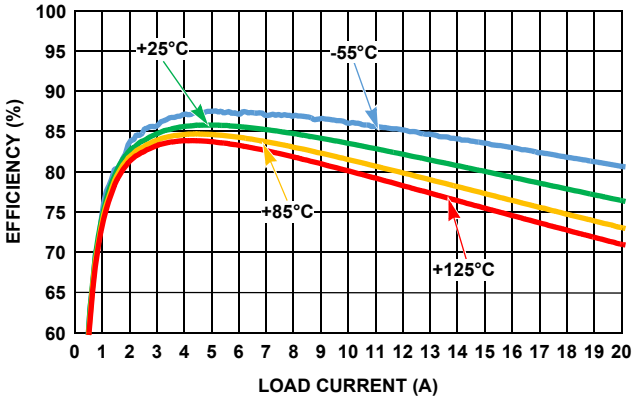


FIGURE 8. EFFICIENCY vs LOAD vs CASE TEMPERATURE
V_{IN} = 5V, V_{OUT} = 1.0V, f_{SW} = 500kHz

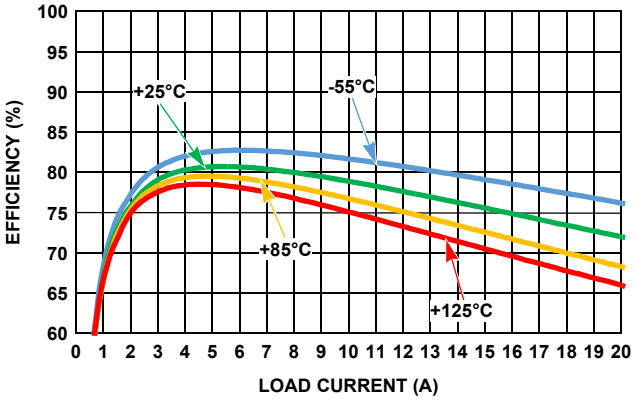


FIGURE 9. EFFICIENCY vs LOAD vs CASE TEMPERATURE
V_{IN} = 5V, V_{OUT} = 1.0V, f_{SW} = 1MHz

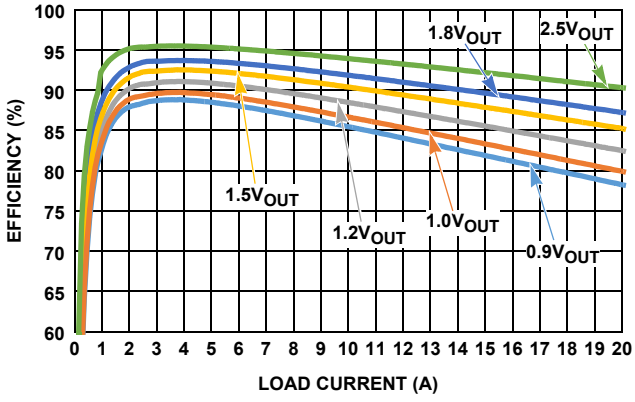


FIGURE 10. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 500kHz, -55°C CASE TEMPERATURE

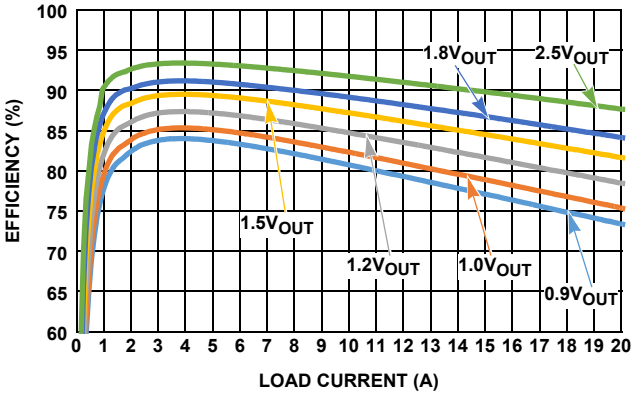


FIGURE 11. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 1MHz, -55°C CASE TEMPERATURE

Typical Performance Curves

Efficiency data taken with (Best Case Thermal Condition) the ISL70002SEHEVAL2Z immersed in a calibrated temperature liquid bath to ensure notated ambient and package case temperatures on both IC component sides of this evaluation board. In typical lab air ambient test condition efficiency will be lower. **(Continued)**

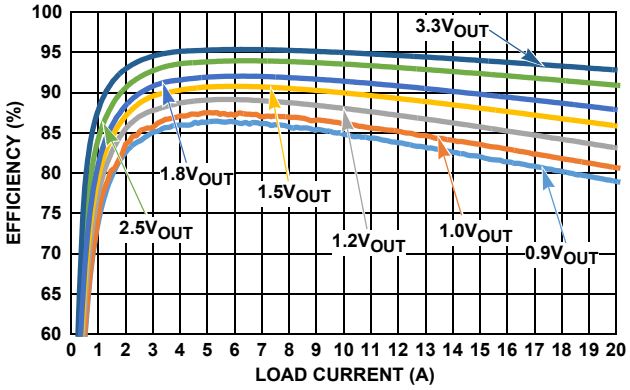


FIGURE 12. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 5V, f_{SW} = 500kHz, -55°C CASE TEMPERATURE

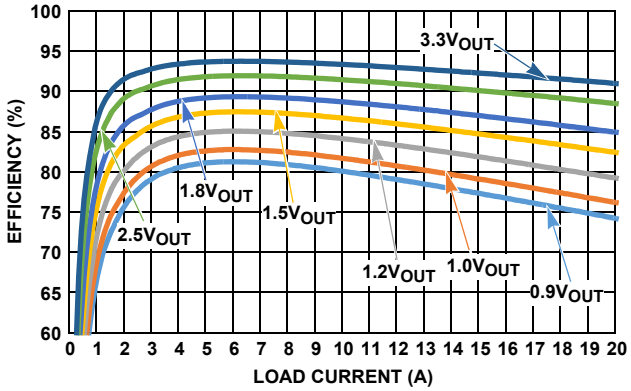


FIGURE 13. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 5V, f_{SW} = 1MHz, -55°C CASE TEMPERATURE

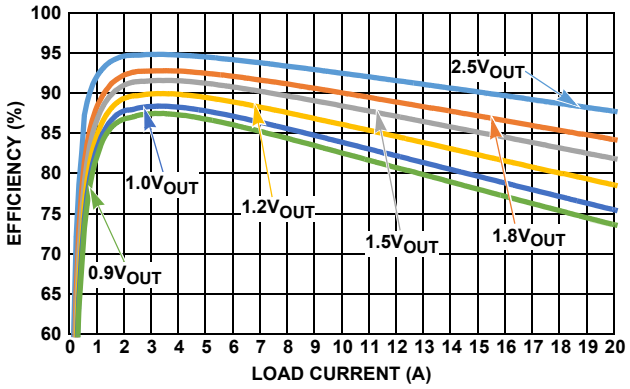


FIGURE 14. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 500kHz, +25°C CASE TEMPERATURE

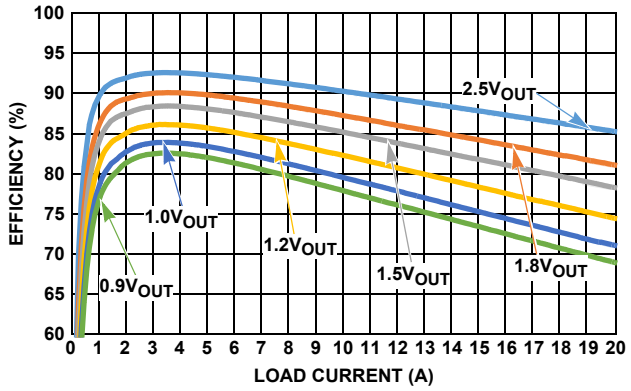


FIGURE 15. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 3.3V, f_{SW} = 1MHz, +25°C CASE TEMPERATURE

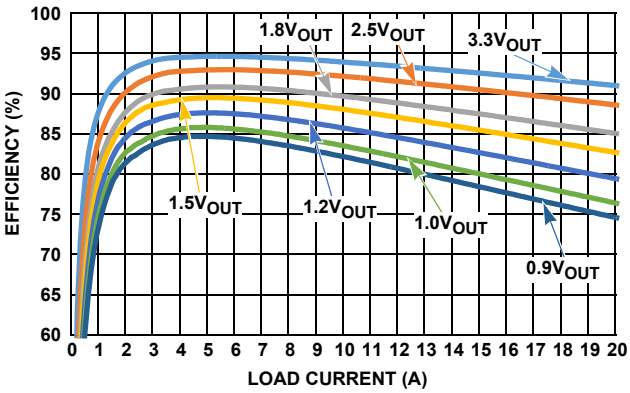


FIGURE 16. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 5V, f_{SW} = 500kHz, +25°C CASE TEMPERATURE

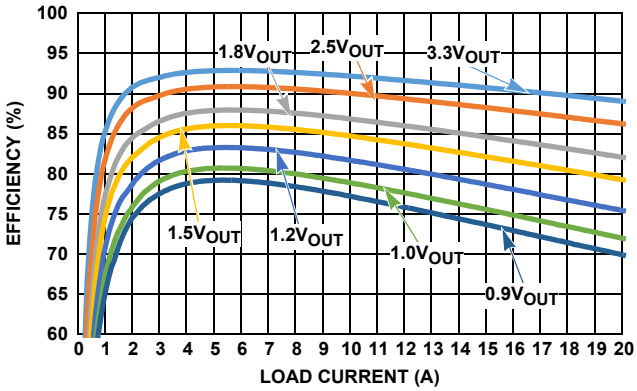


FIGURE 17. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE
V_{IN} = 5V, f_{SW} = 1MHz, +25°C CASE TEMPERATURE

Typical Performance Curves

Efficiency data taken with (Best Case Thermal Condition) the ISL70002SEHEVAL2Z immersed in a calibrated temperature liquid bath to ensure notated ambient and package case temperatures on both IC component sides of this evaluation board. In typical lab air ambient test condition efficiency will be lower. **(Continued)**

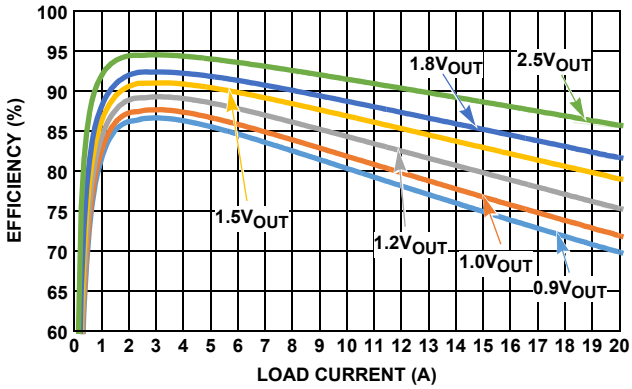


FIGURE 18. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 500kHz, +85°C CASE TEMPERATURE

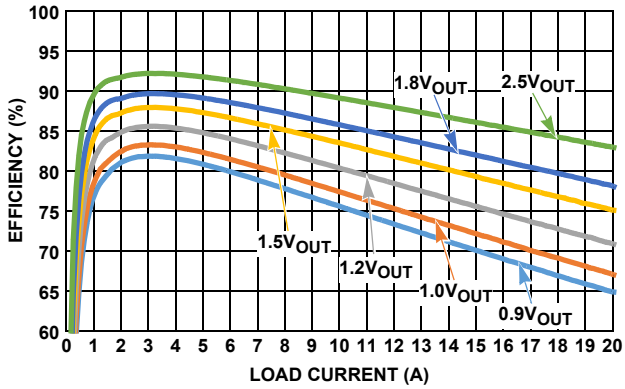


FIGURE 19. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 1MHz, +85°C CASE TEMPERATURE

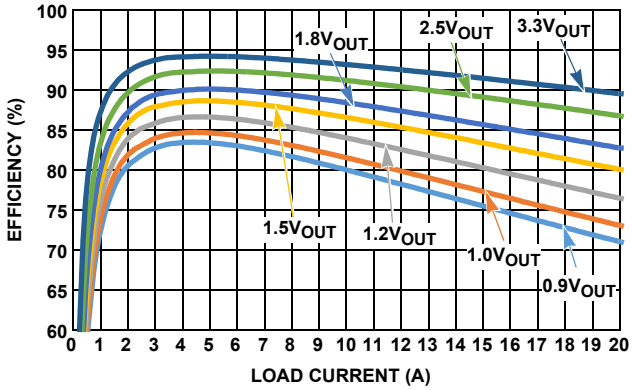


FIGURE 20. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 500kHz, +85°C CASE TEMPERATURE

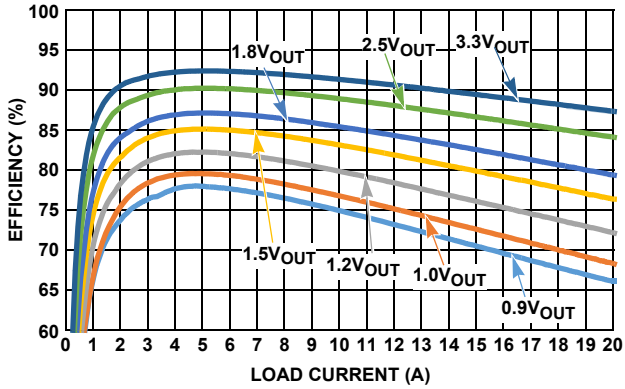


FIGURE 21. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 1MHz, +85°C CASE TEMPERATURE

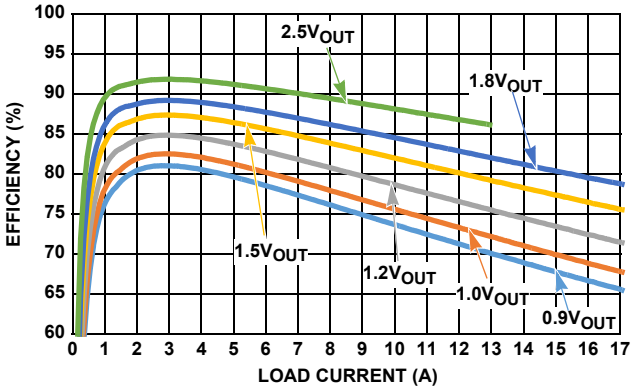


FIGURE 22. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 500kHz, +125°C CASE TEMPERATURE

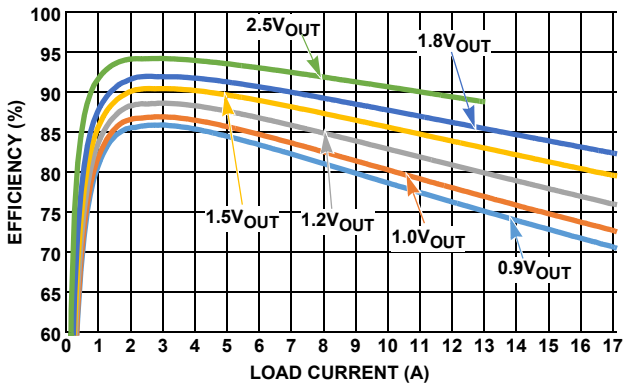


FIGURE 23. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 3.3V, f_{SW} = 1MHz, +125°C CASE TEMPERATURE

Typical Performance Curves

Efficiency data taken with (Best Case Thermal Condition) the ISL70002SEHEVAL2Z immersed in a calibrated temperature liquid bath to ensure notated ambient and package case temperatures on both IC component sides of this evaluation board. In typical lab air ambient test condition efficiency will be lower. **(Continued)**

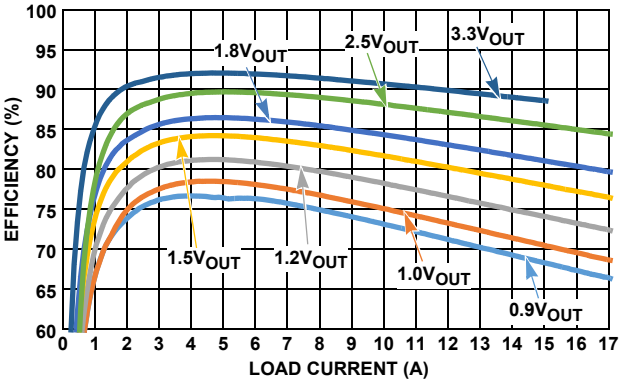


FIGURE 24. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW}= 500kHz, +125°C CASE TEMPERATURE

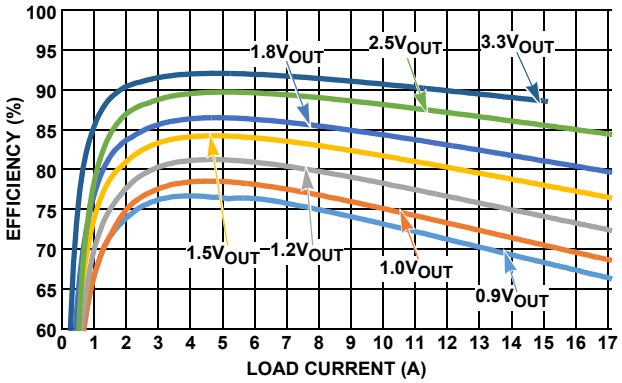


FIGURE 25. EFFICIENCY vs LOAD vs OUTPUT VOLTAGE V_{IN} = 5V, f_{SW} = 1MHz, +125°C CASE TEMPERATURE

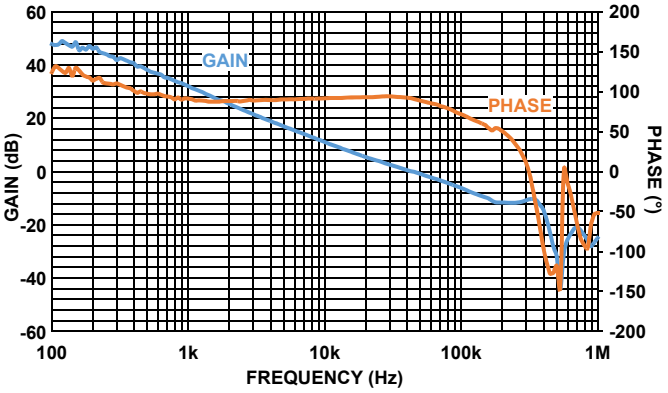


FIGURE 26. GAIN AND PHASE PLOTS, 9A LOAD, V_{IN} = 3.3V, V_{OUT} = 1.0V, f_{SW} = 500kHz, SCO = 0, SC1 = 0

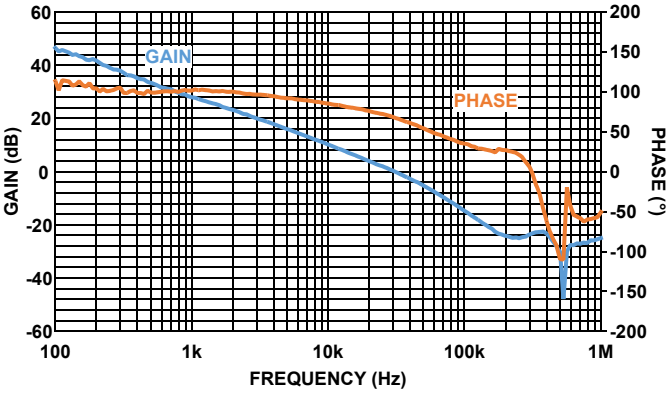


FIGURE 27. GAIN AND PHASE PLOTS, 9A LOAD, V_{IN} = 3.3V, V_{OUT} = 1.0V, f_{SW} = 500kHz, SCO = 1, SC1 = 1

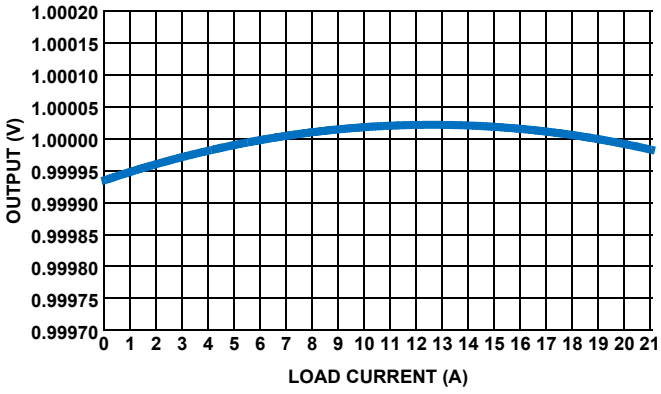


FIGURE 28. 0A - 21A V_{OUT} LOAD CURRENT REGULATION V_{IN} = 3.3V, V_{OUT} = 1.0V, f_{SW} = 500kHz

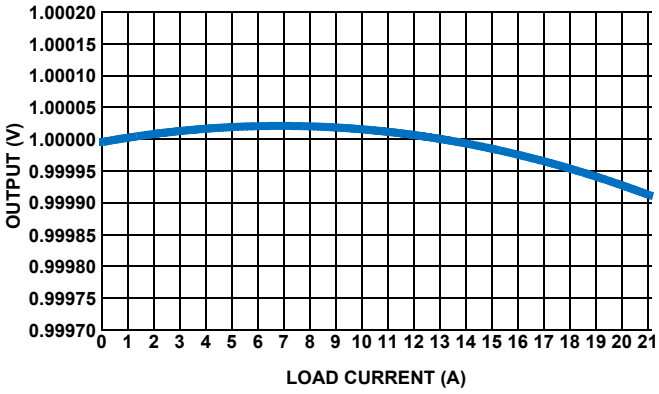
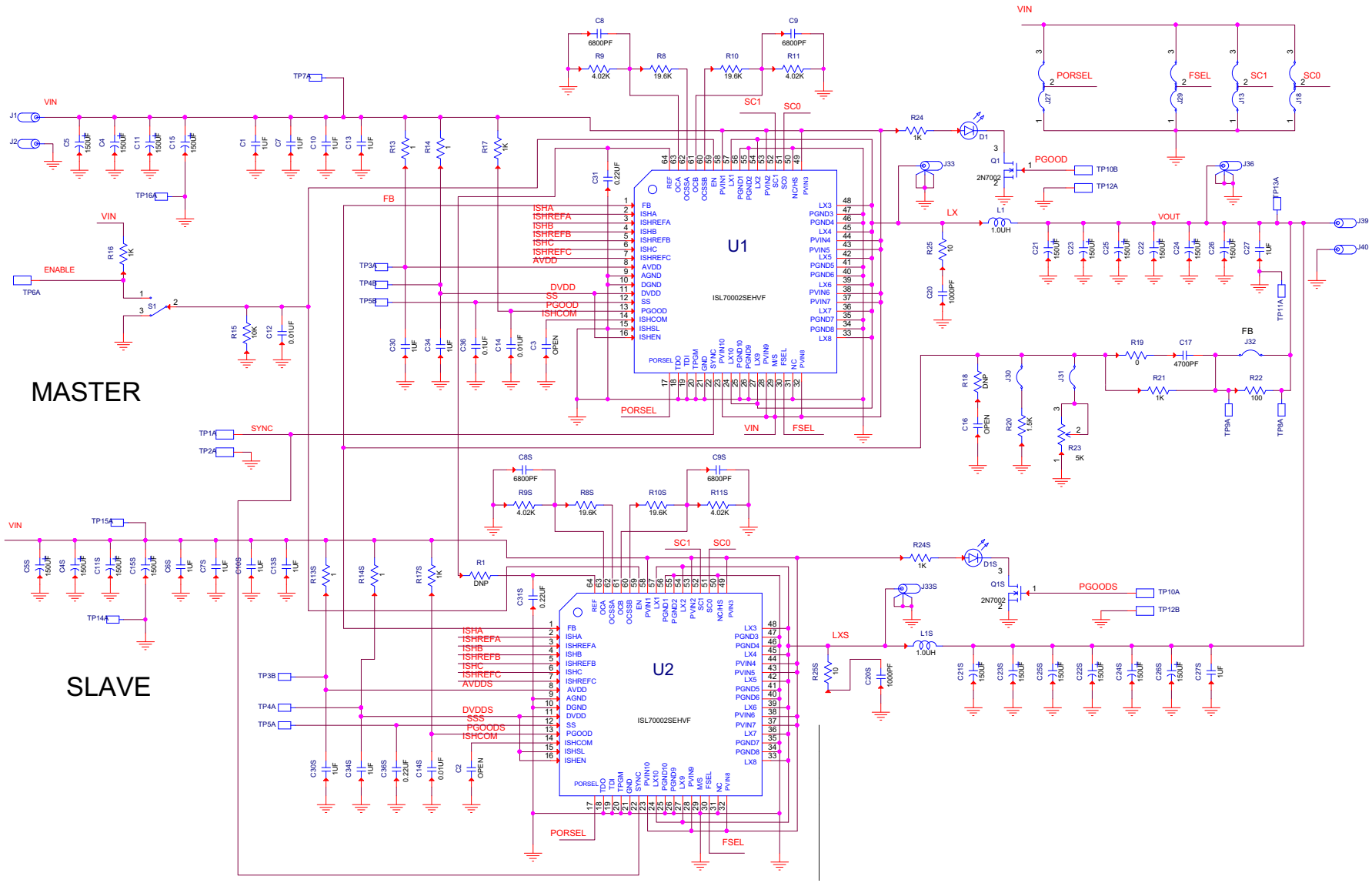


FIGURE 29. V_{OUT} LOAD CURRENT REGULATION V_{IN} = 5V, V_{OUT} = 1.0V, f_{SW} = 500kHz

ISL70002SEHEVAL2Z Schematic



Bill of Materials

REFERENCE DESIGNATOR	QTY	DESCRIPTION	PART NUMBER	MANUFACTURER
U1, U2	2	12A SYNCHRONOUS BUCK REGULATOR W/MOSFET	ISL70002SEHVF	INTERSIL
L1, L1S	2	LOW PROFILE HIGH CURRENT INDUCTOR (RoHS COMPLIANT)	IHLP-5050CE-ER-1R0-M-01	VISHAY
J33, J36, J33S	3	Scope Probe Test Point PCB Mount	131-4353-00	TEKTRONIX
Q1, Q1S	2	N-Channel EMF Effect Transistor	2N7002	FAIRCHILD
R23	1	TRIMMER POTENTIOMETER (RoHS COMPLIANT)	3299W-1-502-LF	BOURNS
TP2, TP12, TP12S	3	Miniature Black Test Point 0.100 Pad 0.040 Thole	5001	KEYSTONE
TP1, TP3-TP5, TP7-TP11, TP13-TP16, TP3S-TP5S, TP10S	17	Miniature White Test Point 0.100 Pad 0.040 Thole	5002	KEYSTONE
TP6	1	Miniature Orange Test Point 0.100 Pad 0.040 Thole	5003	KEYSTONE
J1, J2, J39, J40	4	SOLDER MOUNT BANANA PLUG	575-4	KEYSTONE
C20, C20S	2	Ceramic Chip Cap	C0805C102K2RAC	KEMET
C12, C14, C14S	3	Ceramic Chip Cap	C0805C103K2RAC	KEMET
C8, C9, C8S, C9S	4	Multilayer Cap	C0805C682K2RAC	KEMET
C36, C36S	2	Ceramic Chip Cap	C1210C104K2RAC	KEMET
C17	1	Multilayer Cap	C1812C472F2GAC	KEMET
C31, C31S	2	Ceramic Chip Cap	C1825C224K2RAC	KEMET
C1, C7, C10, C13, C27, C30, C34, C6S, C7S, C10S, C13S, C27S, C30S, C34S	14	Multilayer Cap	C2225C105K2RAC	KEMET
S1	1	SPDT On-None-On SMT Ultraminiture Toggle Switch (RoHS compliant)	GT11MSCBE-T	C&K
C2, C3	2	Multilayer Cap	H1045-OPEN	GENERIC
C16	1	Ceramic Chip Cap	H1082-OPEN	GENERIC
R18	1	Metal Film Chip Resistor (Do Not Populate)	H2505-DNP-DNP-1	GENERIC
R1	1	Metal Film Chip Resistor (Do Not Populate)	H2505-DNP-DNP-R1	GENERIC
R19	1	Thick Film Chip Resistor	H2511-00R00-1/16W1	GENERIC
R24, R24S	2	Thick Film Chip Resistor	H2511-01001-1/16W1	GENERIC
J13, J18, J27, J29	4	Three Pin Jumper	JUMPER-3-100	GENERIC
J30-J32	3	Two Pin Jumper	JUMPER2_100	GENERIC
D1, D1S	2	AlInGaP Green	LTST-C190KGKT	LITEON
R16	1	Metal Film Chip Resistor	MCR03EZPFX1001	ROHM
R17, R21, R17S	3	Thick Film Chip Resistor	S0603CA1001BEB	State of the Art
R20	1	25ppm Thin Film Chip Resistor	S0603CA1501BEZ	State of the Art
R8, R10, R8S, R10S	4	25ppm Thin Film Chip Resistor	S0603CA1962BEZ	State of the Art
R9, R11, R9S, R11S	4	25ppm Thin Film Chip Resistor	S0603CA4021BEZ	State of the Art
R22	1	100ppm Thick Film Chip Resistor	S0603CPZ1000F10	State of the Art
R15	1	100ppm Thick Film Chip Resistor	S0603CPZ1002F10	State of the Art
R13, R14, R13S, R14S	4	100ppm Thick Film Chip Resistor	S0603CPZ1R00F10	State of the Art
R25, R25S	2	100ppm Thick Film Chip Resistor	S1206CPZ10R0F10	State of the Art
C4, C5, C11, C15, C21-C26, C4S, C5S, C11S, C15S, C21S-C26S	20	High Capacitance Ultra-Low ESR Tantalum SMD Cap	T530D157M010AHE006	KEMET

ISL70002SEHEVAL2Z Layout

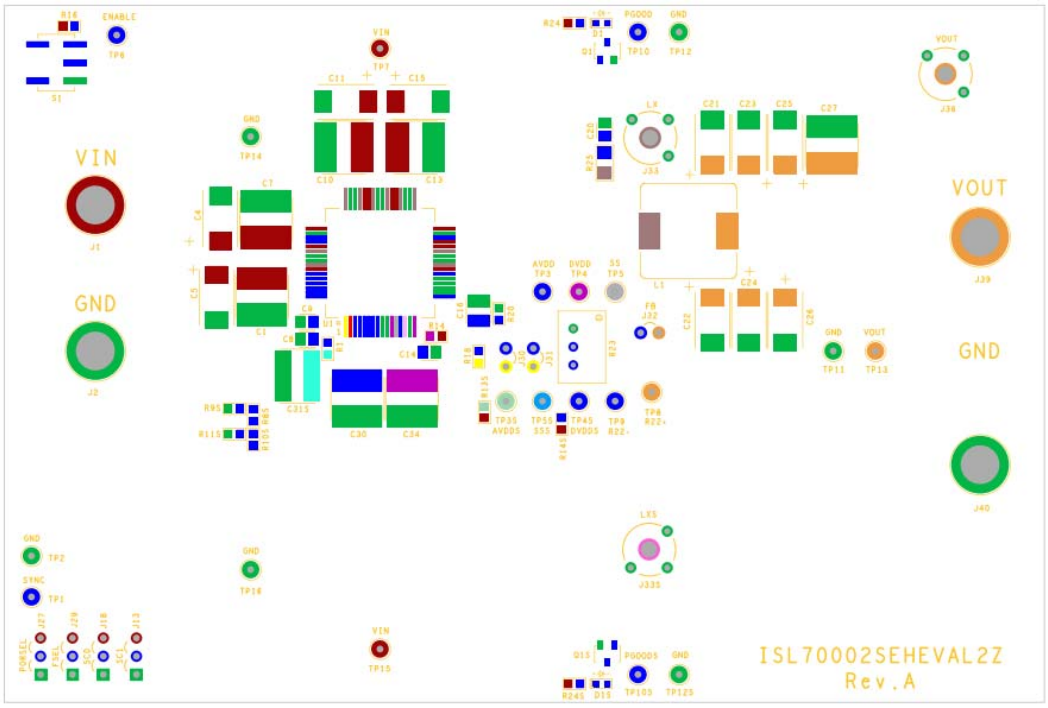


FIGURE 30. TOP SILK SCREEN

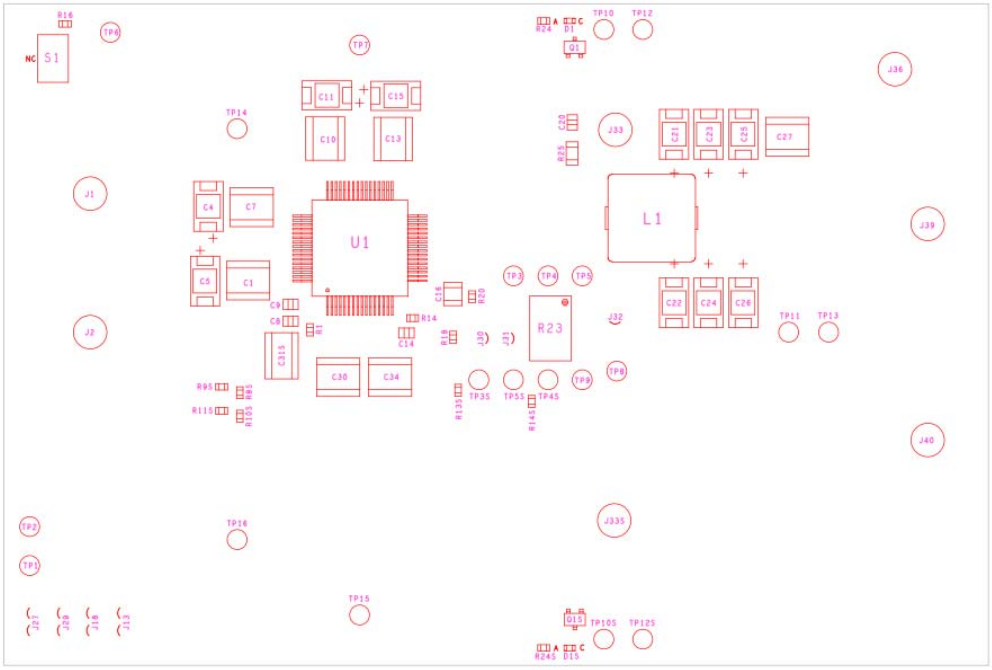


FIGURE 31. TOP LAYER COMPONENT PLACEMENT

ISL70002SEHEVAL2Z Layout (Continued)

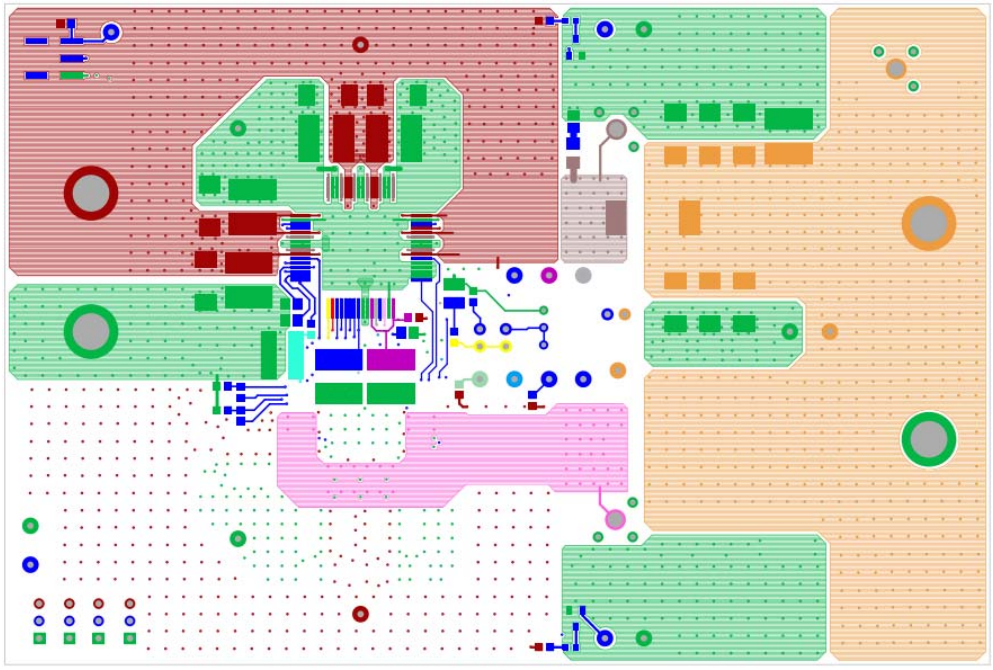


FIGURE 32. TOP COMPONENT LAYER

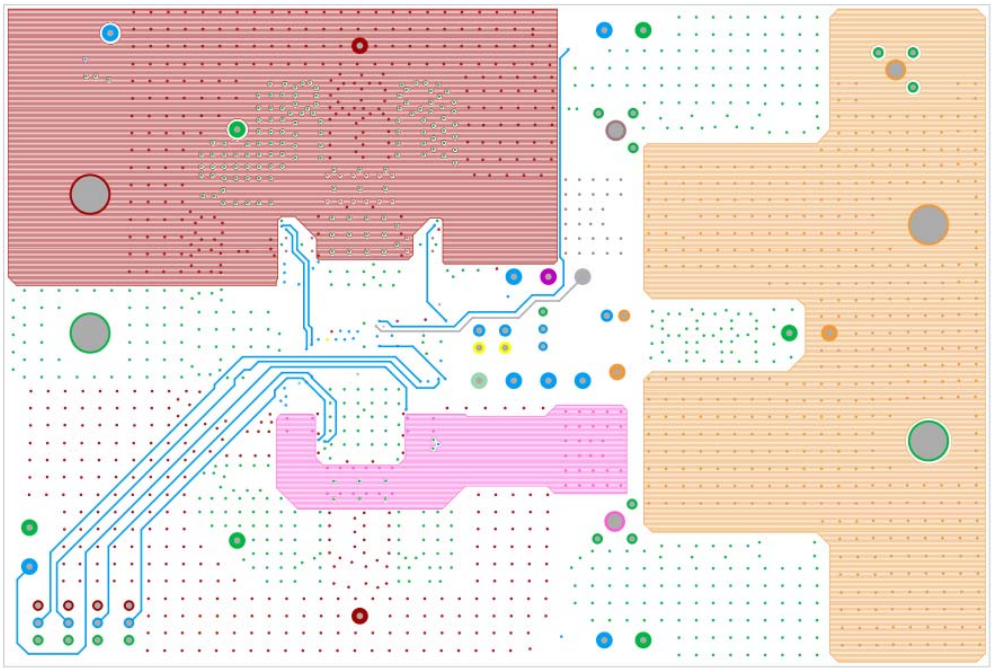


FIGURE 33. LAYER 2

ISL70002SEHEVAL2Z Layout (Continued)

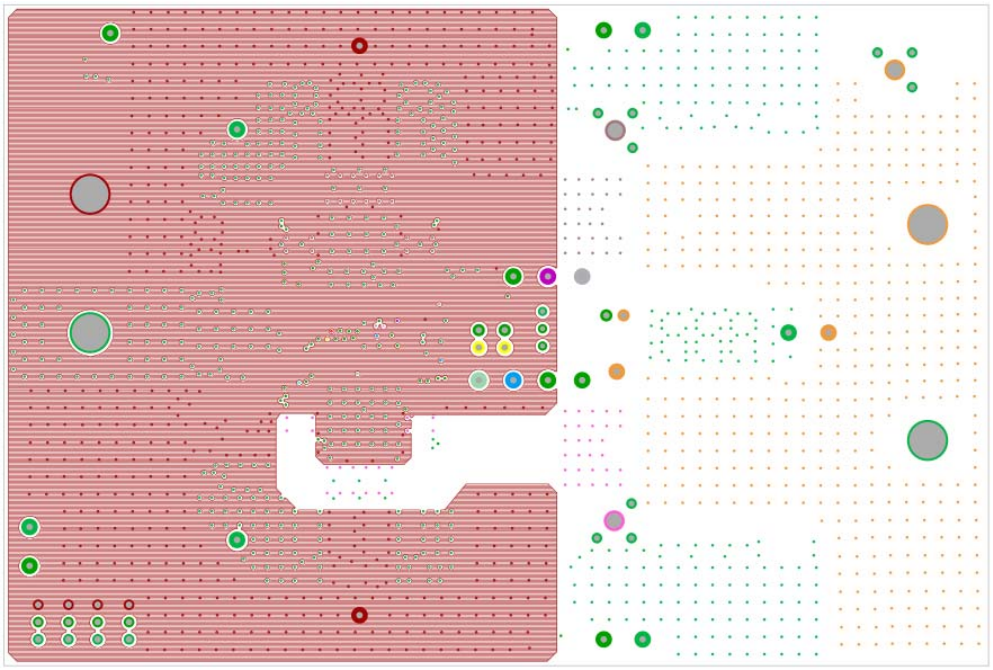


FIGURE 34. LAYER 3

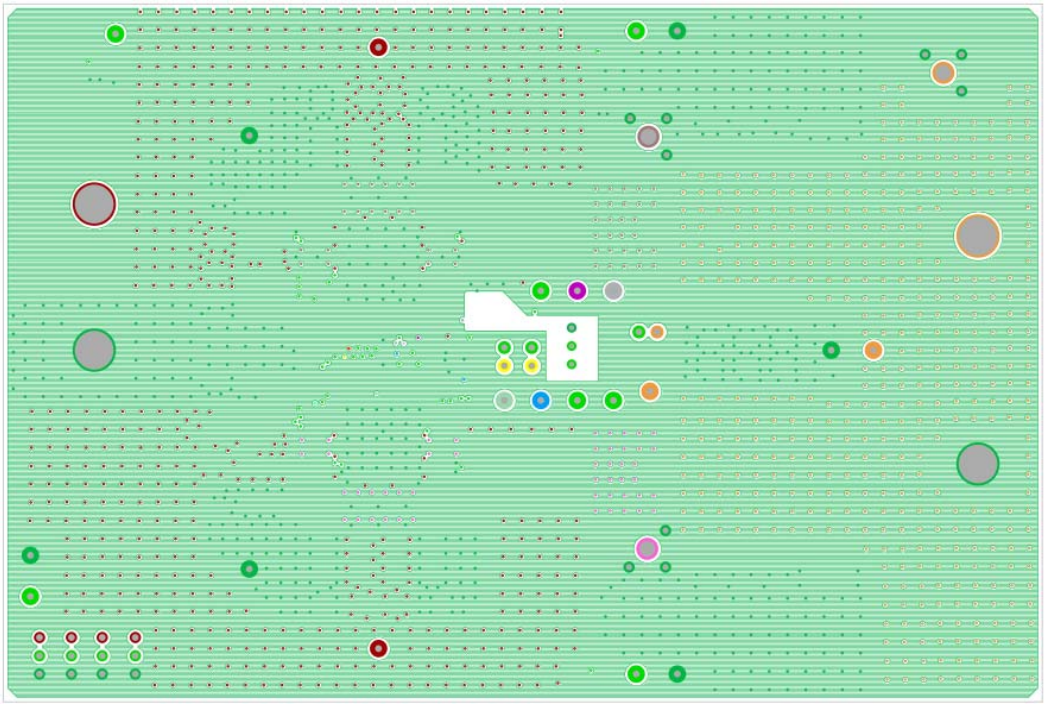


FIGURE 35. LAYER 4

ISL70002SEHEVAL2Z Layout (Continued)

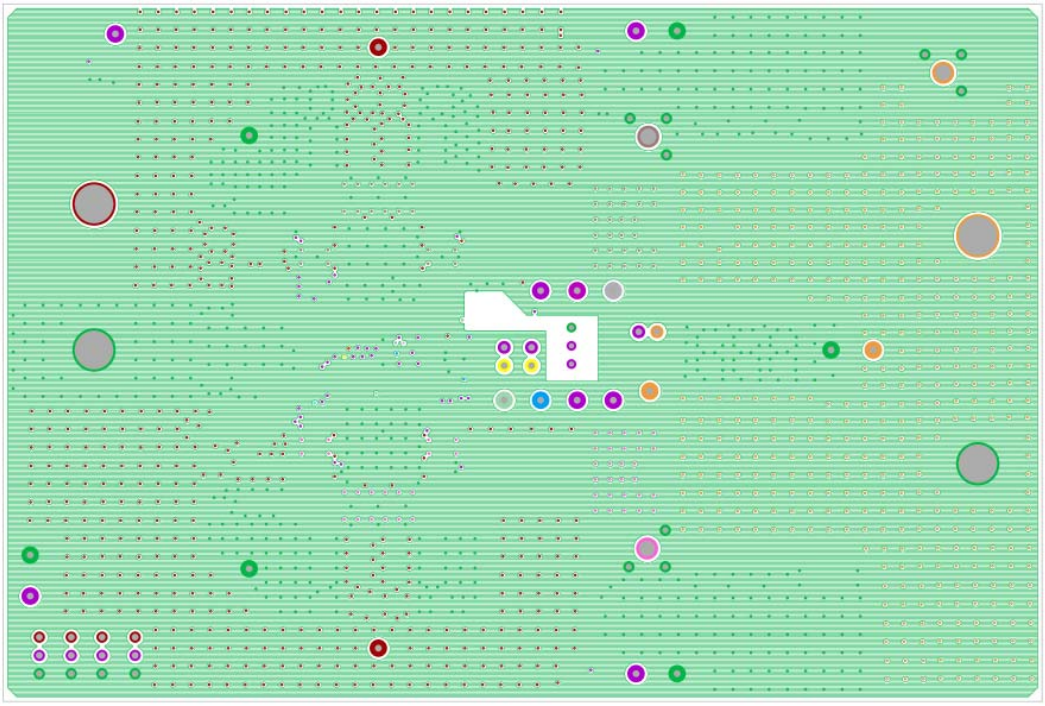


FIGURE 36. LAYER 5

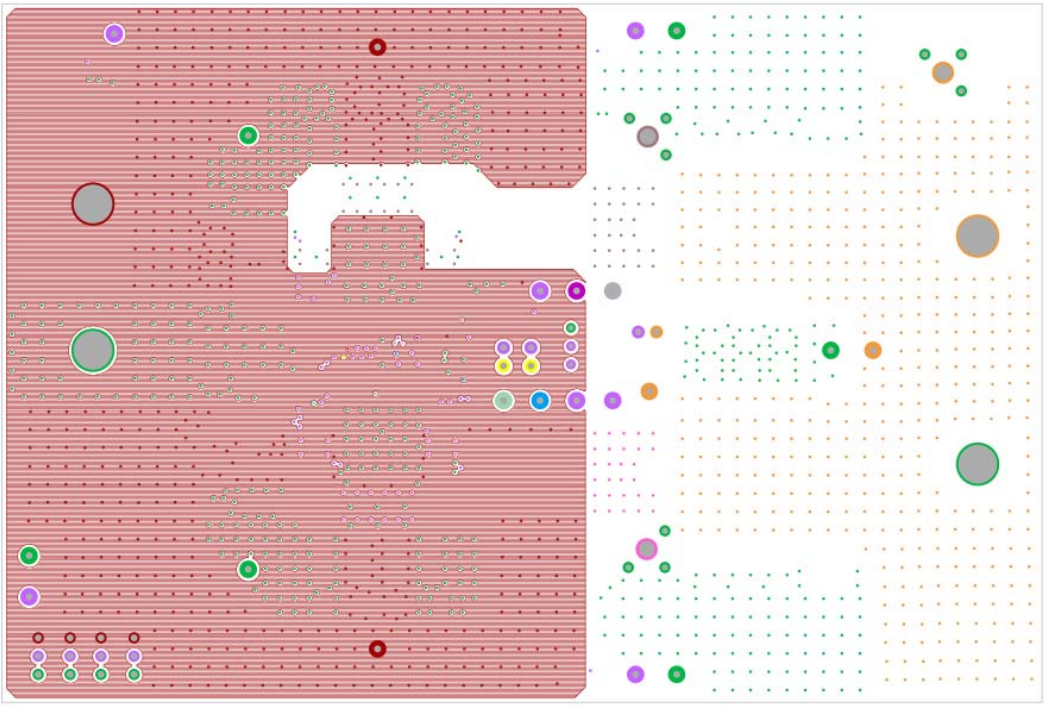


FIGURE 37. LAYER 6

ISL70002SEHEVAL2Z Layout (Continued)

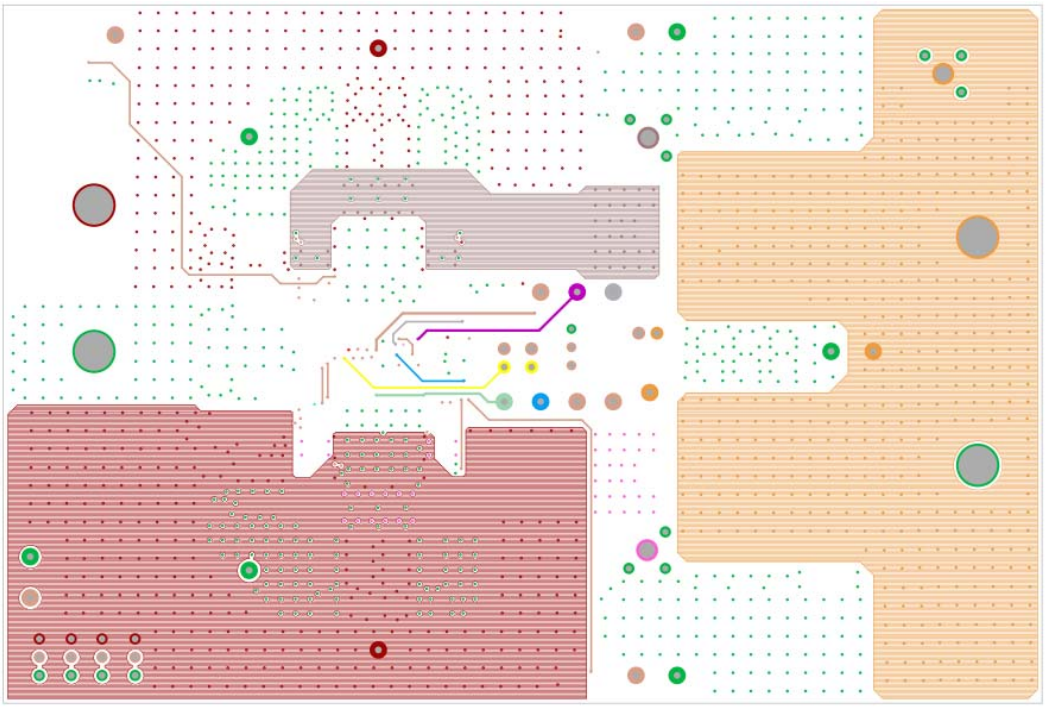


FIGURE 38. LAYER 7

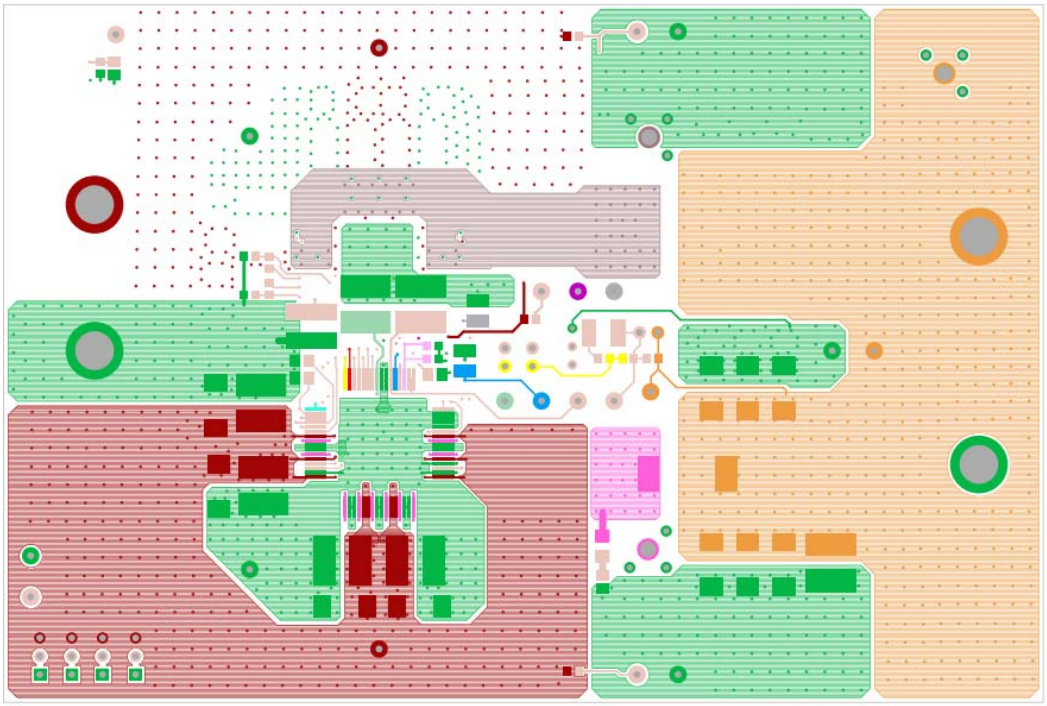


FIGURE 39. BOTTOM COMPONENT LAYER 8

ISL70002SEHEVAL2Z Layout (Continued)

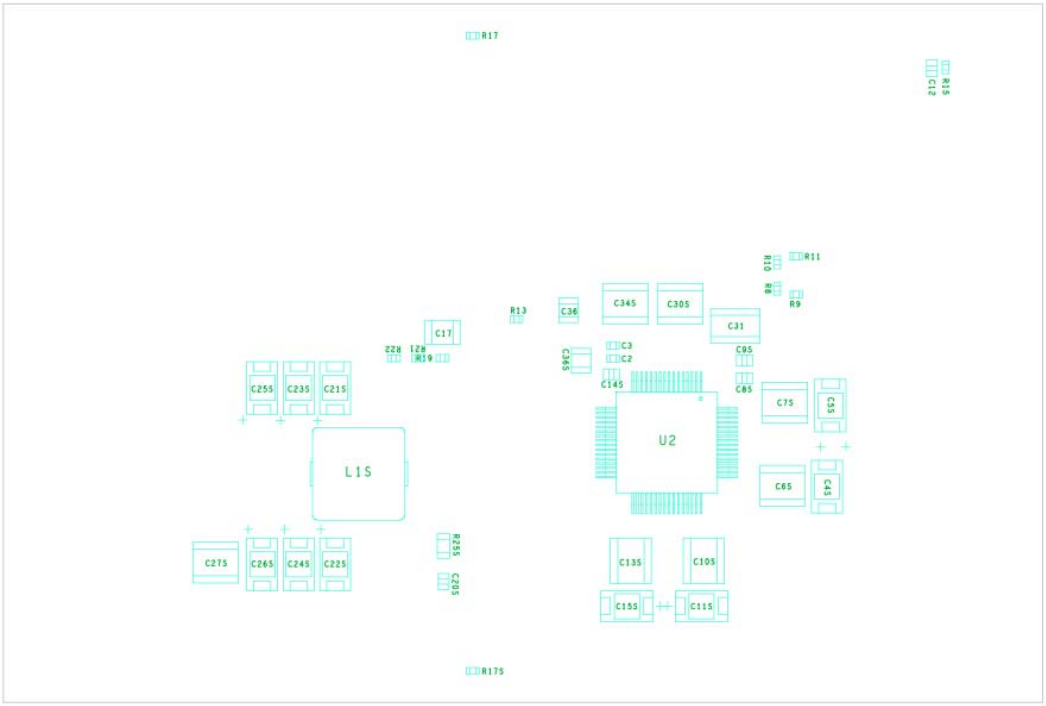


FIGURE 40. BOTTOM LAYER COMPONENT PLACEMENT

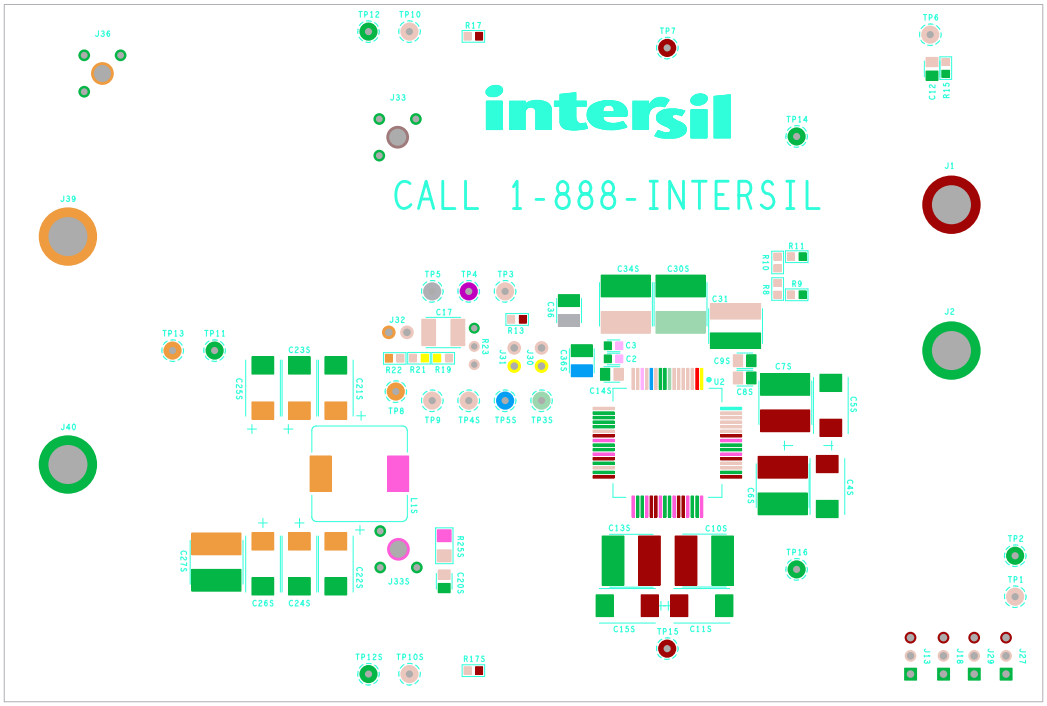


FIGURE 41. BOTTOM SILK SCREEN

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(Rev.4.0-1 November 2017)

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