ISL70219ASEHEV1Z

Evaluation Board

UG007
Rev.1.0
Jul 1, 2021

Introduction

The ISL70219ASEHEV1Z evaluation platform is designed to evaluate the ISL70219ASEH. The ISL70219ASEH contains two very high precision amplifiers featuring the perfect combination of low noise vs power consumption. Low offset voltage, low I_{BIAS} current and low temperature drift making them the ideal choice for applications requiring both high DC accuracy and AC performance. The combination of high precision, low noise, low power and small footprint provides the user with outstanding value and flexibility relative to similar competitive parts.

Applications for these amplifiers include precision active filters, medical and analytical instrumentation, precision power supply controls, and industrial controls.

The ordering number for this board is ISL70219ASEHEV1Z. Please go to ordering tab on the landing page for the ISL70219ASEH.

Related Literature

- ISL70219ASEH Datasheet
- ISL70219ASEH SMD 5962-14226
- ISL70219ASEH Radiation Test Report
- TR002: Single Event Effects (SEE) Testing of the ISL70219ASEH Dual Operational Amplifier

Key Features

- Wide V_{IN} range single supply or dual supply
  - ±2.25V to ±18V
  - +4.5V to +36V
- Singled-ended or differential input operation
- External VREF input
- Banana Jack connectors for power supply and VREF inputs
- BNC connectors for op amp input and output terminals
- Convenient PCB pads for op amp input/output impedance loading.

Specifications

- V+ range: +2.25V to 18V
- V- range: -2.25V to -18V
- Common mode input range: 2V within V+ and V- rails.

Ordering Information

PART NUMBER	DESCRIPTION
ISL70219ASEHEV1Z	Evaluation Board

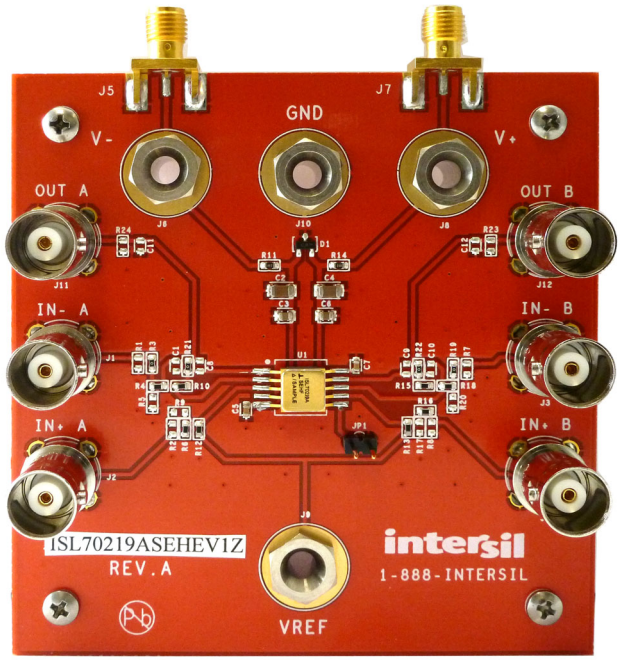

FIGURE 1. ISL70219ASEHEV1Z EVALUATION BOARD

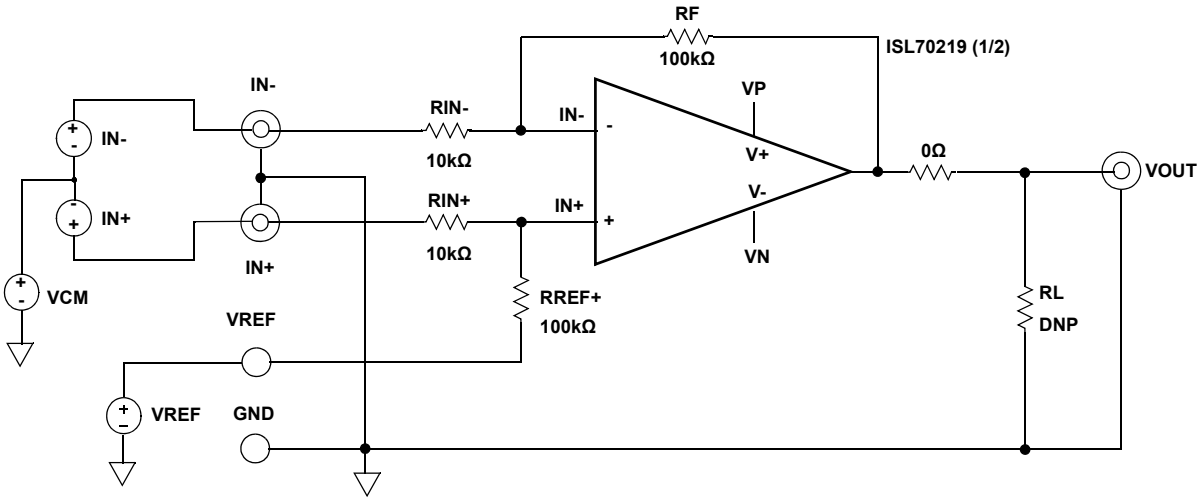

FIGURE 2. BASIC AMPLIFIER CONFIGURATION

Power Supplies

External power connections are made through the +V, -V, VREF and Ground connections on the evaluation board. For single supply operation, the -V and Ground pins are tied together to the power supply negative terminal. For split supplies, +V and -V terminals connect to their respective power supply terminals. Decoupling capacitors C_2, C_3, C_4 and C_6 connect to their respective supplies through R_{11} and R_{14} resistors. These resistors are 100Ω but can be changed by the user to provide additional power supply filtering, or to reduce the voltage rate of rise to less than ±1V/µs. Two additional capacitors, C5 and C_7, are connected close to the part to filter out high frequency noise. Anti-reverse diode D_1 protects the circuit in the momentary case of accidentally reversing the power supplies to the evaluation board. The VREF pin can be connected to ground to establish a ground referenced input for split supply operation, or can be externally set to any reference level for single supply operation.

Amplifier Configuration

A simplified schematic of the evaluation board is shown in Figure 2. The input stage with the components supplied is shown in Figure 4, with a closed loop gain of 10V/V. The differential amplifier gain is expressed in Equation 1:

$$V_{OUT} = (V_{IN+} - V_{IN-}) \bullet (R_F / R_{IN}) + V_{REF} \quad \text{(EQ. 1)}$$

For single-ended input with an inverting gain G = -10V/V, the IN+ input is grounded and the signal is supplied to the IN- input. The VREF can be connected to a reference voltage between the V+ and V- supply rails. For non-inverting operation with G = 11V/V, the IN- input is grounded and the signal is supplied to the IN+ input. The non-inverting gain is strongly dependent on any resistance from IN- to GND. For good gain accuracy, a 0Ω resistor should be installed on the empty R_5 pad. The VREF pin must be connected to ground to establish a ground referenced input for dual supply operation, or can be externally set to any reference level for single supply operation. The VREF should not be left floating.

PCB Layout Considerations

There a few layout constraints to consider when using the ISL70219ASEH, but this will generally apply to any generic operational amplifier. Analog circuits can conduct noise through paths that connect it to the “outside world”. These paths include the V+, V-, IN+, IN- and OUT terminals. It’s important to make sure these paths are kept away from known noise sources to ensure optimal performance of the part. If the ISL70219ASEH resides on the same boards as digital circuitry it is necessary to decouple the power pins on the analog as well as the digital circuitry. This is done on the evaluation board with C_2 through C_7, with the lower value capacitors, C_5 and C_7, placed near the V- and V+ pins respectively to minimize high frequency noise.

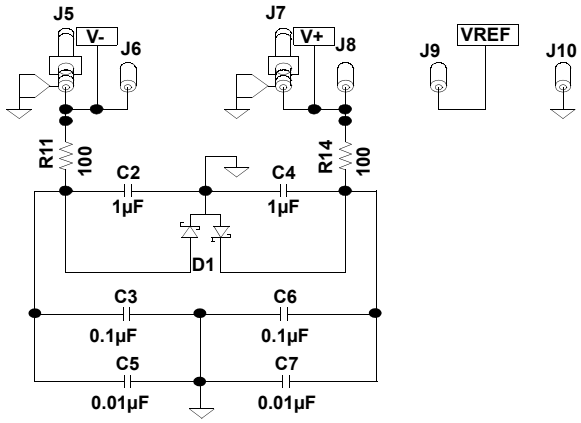

FIGURE 3. POWER SUPPLY CIRCUIT

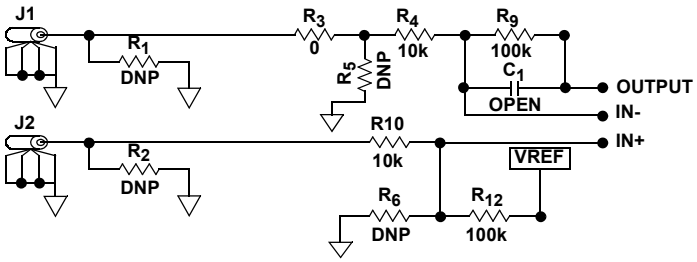

FIGURE 4. INPUT STAGE (1/2)

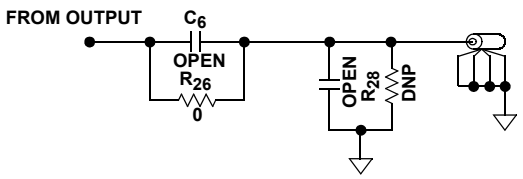

FIGURE 5. OUTPUT STAGE (1/2)

User-selectable Options

Component pads are included to enable a variety of user-selectable circuits to be added to the amplifier VREF, inputs, outputs, and the amplifier feedback loops.

A voltage divider (Figure 4, R_6 and R_{12}) can be added to establish a power supply-tracking common mode reference using the VREF input. The input stages (see Figure 4) have additional resistor and/or capacitor pads that may be used to add voltage divider networks or feedback networks for adding input attenuation, or to establish input DC offsets through the VREF pin. The output stages (see Figure 5) have additional resistor and capacitor placements for loading.

NOTE: Operational amplifiers are sensitive to output capacitance and may oscillate. In the event of oscillation, reduce output capacitance by using shorter cables, or add a resistor in series with the output.

Bill of Materials

DEVICE #	DESCRIPTION	COMMENTS
C2, C4	CAP, SMD, 1206, 1µF, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C3, C6	CAP, SMD, 0805, 0.1µF, 50V, 10%, X7R, ROHS	Power Supply Decoupling
C5, C7	CAP, SMD, 0603, 0.01µF, 25V, 10%, X7R, ROHS	Power Supply Decoupling
C1, C8, C9, C10, C11, C12	CAP, SMD, 0603, DNP-PLACE HOLDER, ROHS	User selectable capacitors - not populated
D1	DIODE-SCHOTTKY BARRIER, SMD, SOT-23, 3P, 40V, ROHS	Reverse Power Protection
U1	ISL70219ASEHF/PROTO, DUAL OP AMP, 10Ld. FLATPACK	
R1, R2, R5, R7, R8, R9, R17, R20, R23, R24	RESISTOR, SMD, 0603, 0.1%, MF, DNP PLACEHOLDER	User selectable resistors - not populated
R3, R19, R21, R22	RES, SMD, 0603, 0Ω, 1/10W,TF, ROHS	0Ω user selectable resistors
R11, R14	RES, SMD, 0603, 100Ω, 1/10W, 1%, TF, ROHS	
R4, R6, R16, R18	RES, SMD, 0603, 10kΩ, 1/10W, 1%, TF, ROHS	Gain resistors
R10, R12, R13, R15	RES, SMD, 0603, 100kΩ, 1/10W, 1%, TF, ROHS	Gain resistors

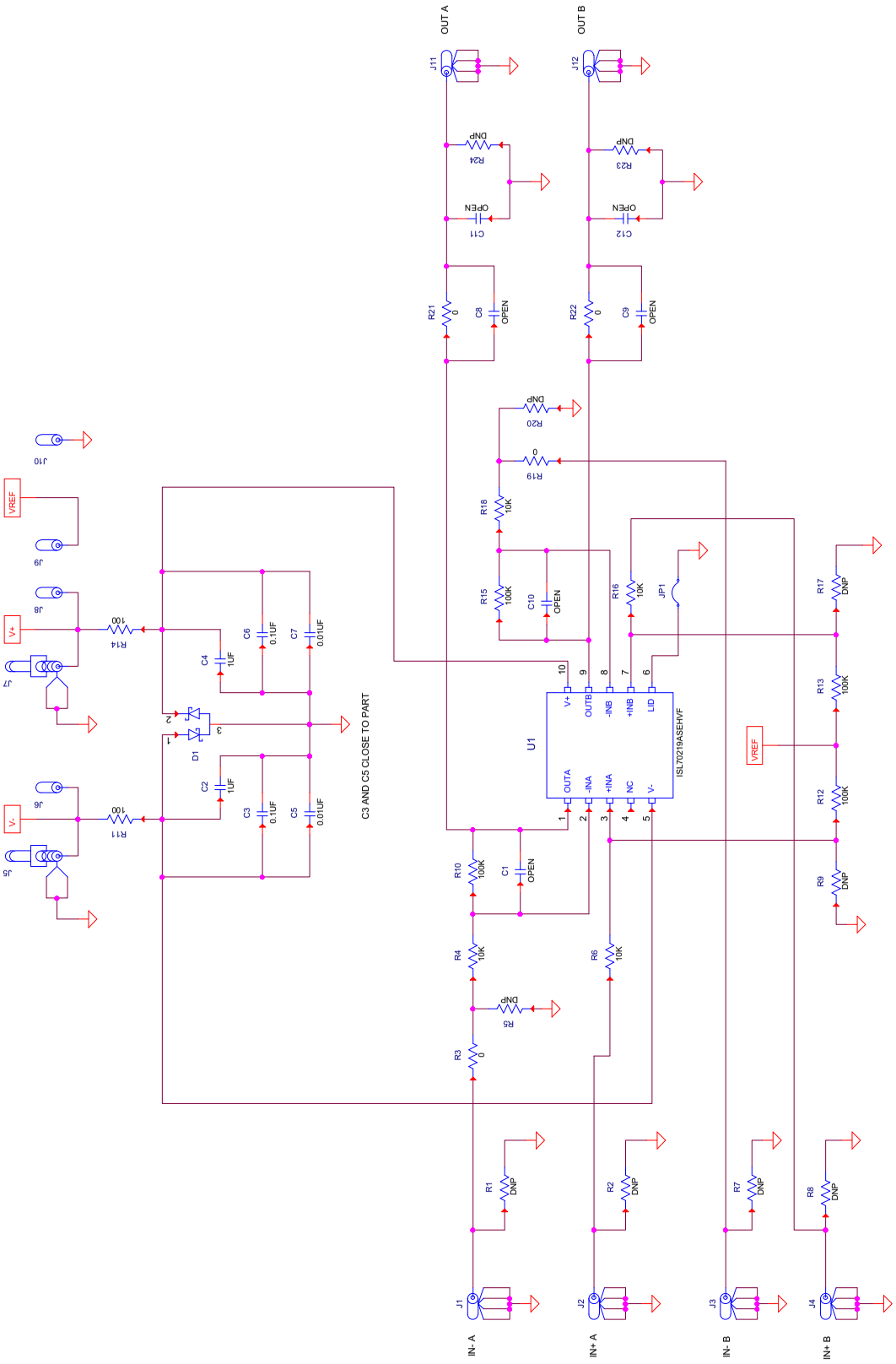

FIGURE 6. ISL70219ASEHEV1Z SCHEMATIC DIAGRAM

ISL70219ASEH Board Layout

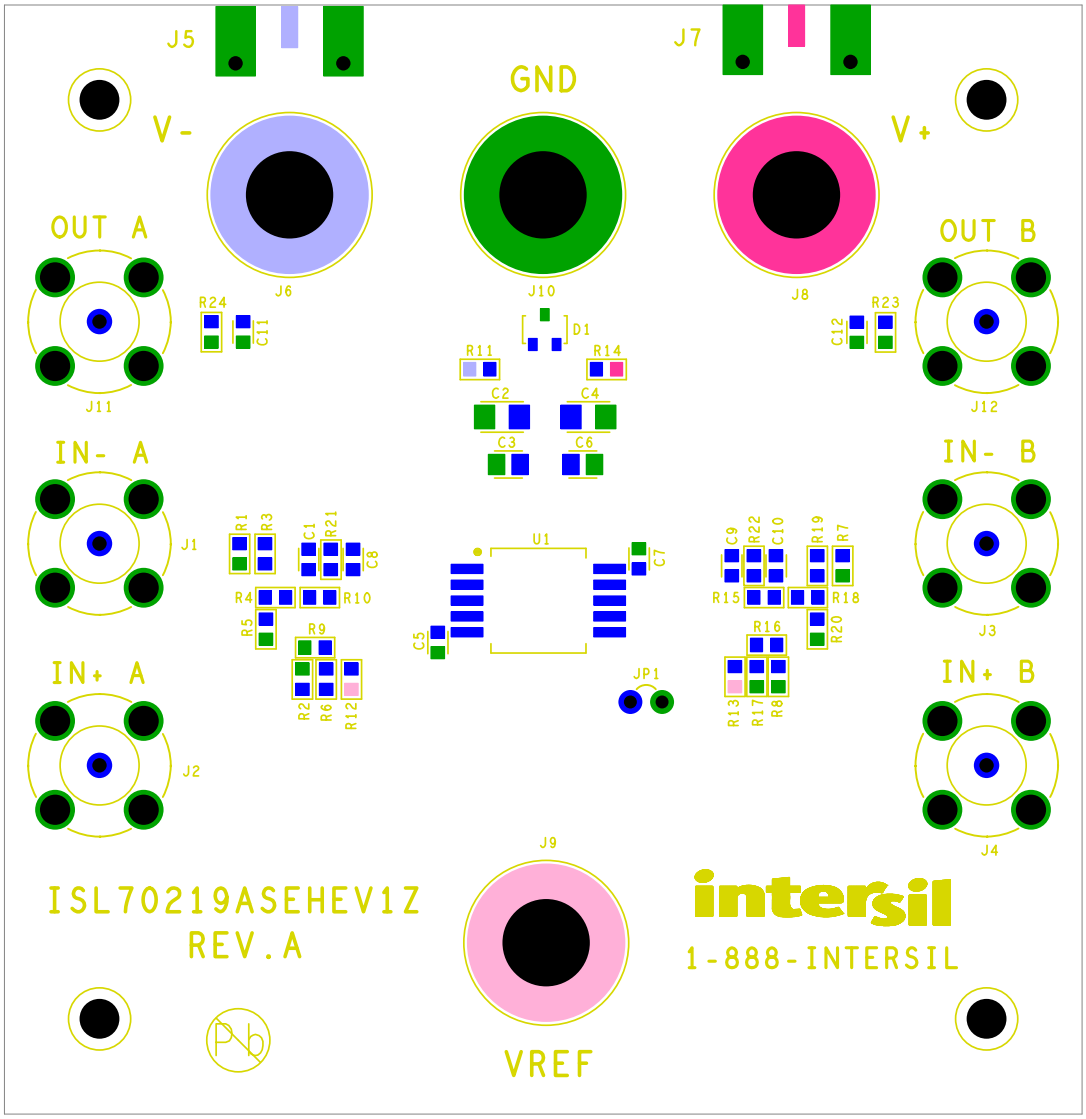

FIGURE 7. TOP VIEW

Typical Performance Curves

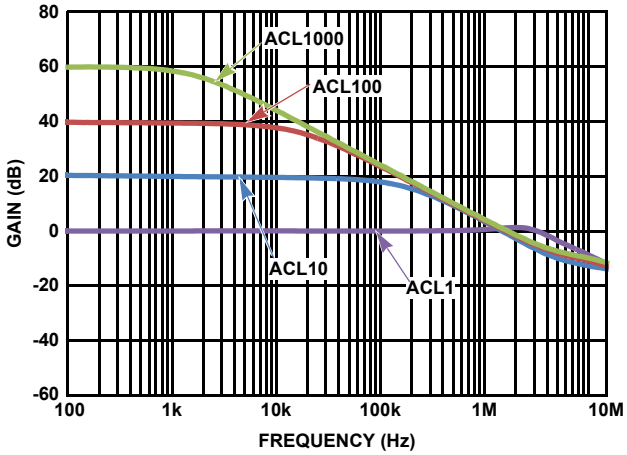

FIGURE 8. FREQUENCY RESPONSE vs ACL (±5.0V)

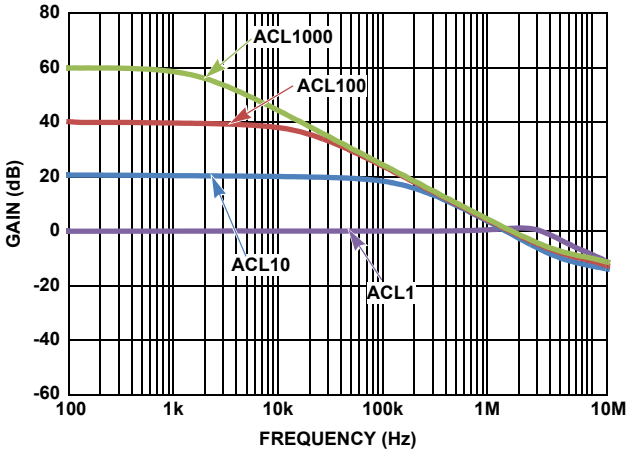

FIGURE 9. FREQUENCY RESPONSE vs ACL (±18.0V)

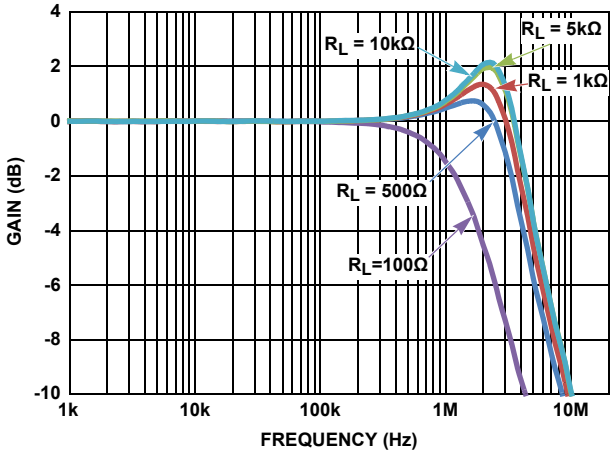

FIGURE 10. FREQUENCY RESPONSE vs R_L (±5.0V)

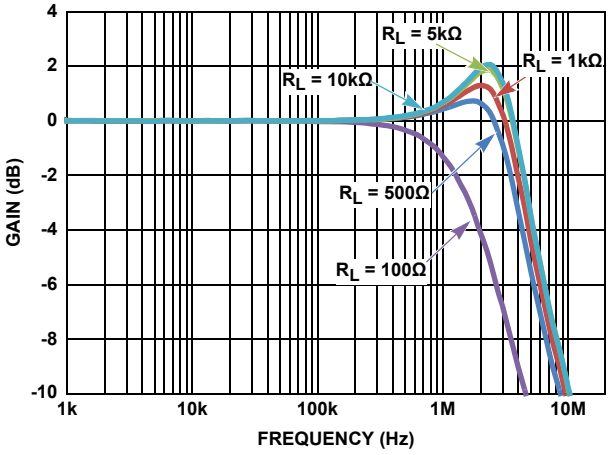

FIGURE 11. FREQUENCY RESPONSE vs R_L (±18.0V)

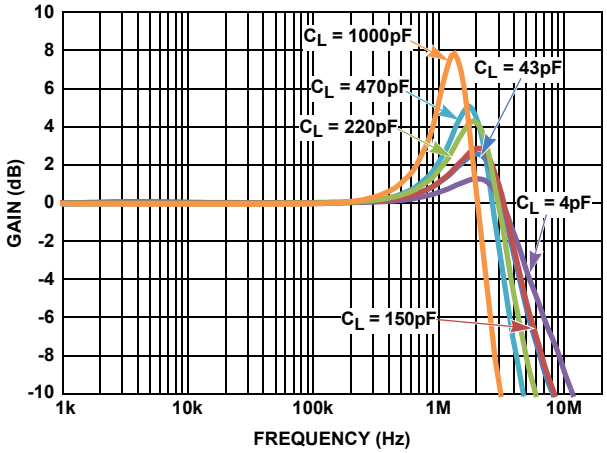

FIGURE 12. FREQUENCY RESPONSE vs C_L (±5.0V)

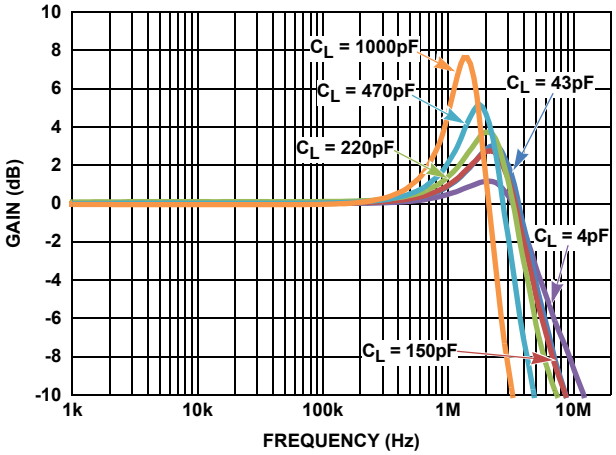

FIGURE 13. FREQUENCY RESPONSE vs C_L (±18.0V)

Typical Performance Curves (Continued)

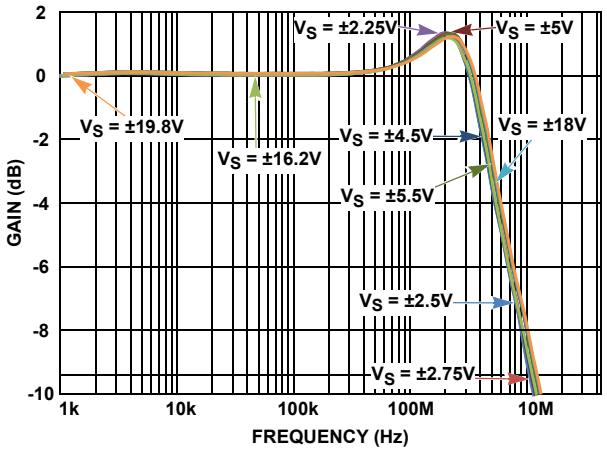

FIGURE 14. FREQUENCY RESPONSE vs SUPPLY VOLTAGE (+25°C)

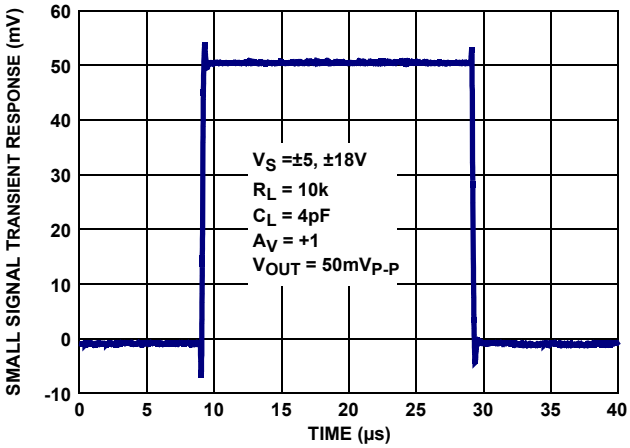

FIGURE 15. SMALL SIGNAL TRANSIENT RESPONSE (+25°C)

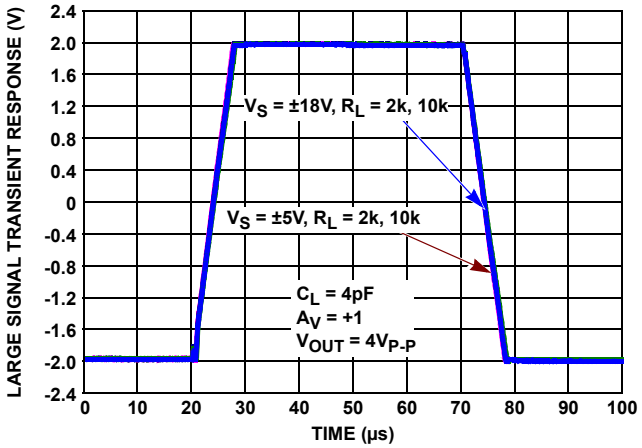

FIGURE 16. LARGE SIGNAL TRANSIENT RESPONSE (+25°C)

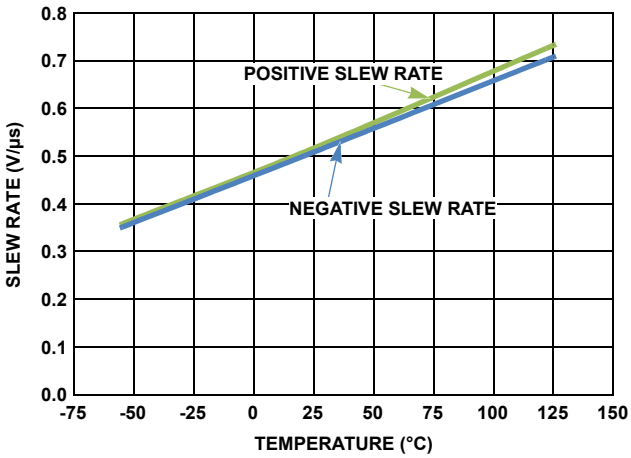

FIGURE 17. SLEW RATE vs TEMPERATURE V_S = ±5V

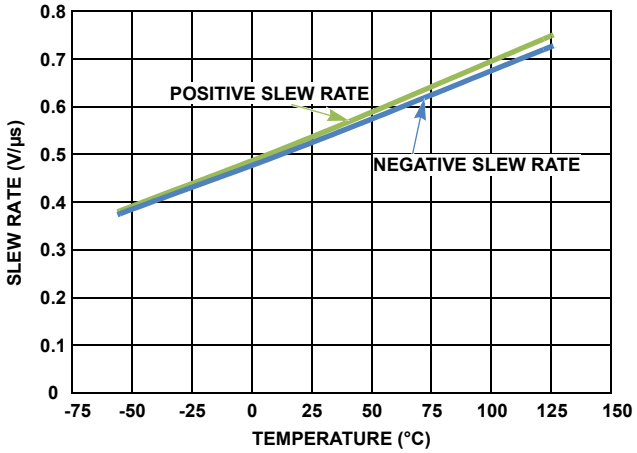

FIGURE 18. SLEW RATE vs TEMPERATURE V_S = ±18V

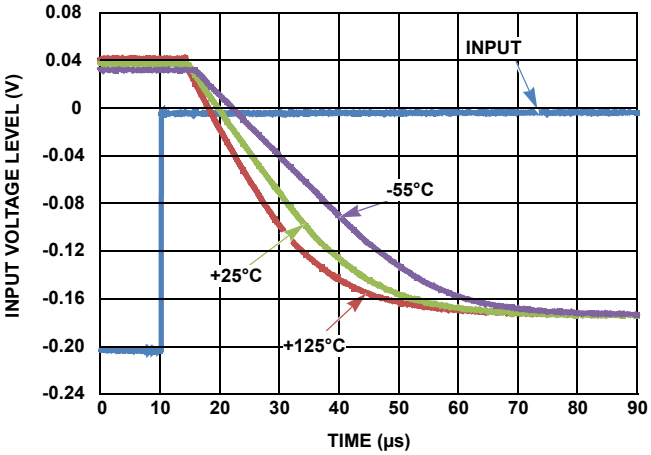

FIGURE 19. ±18V POSITIVE SATURATION RECOVERY TIME (+25°C)

Typical Performance Curves (Continued)

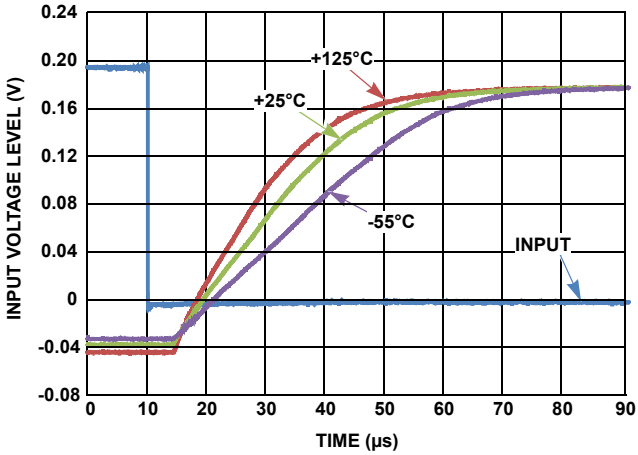

FIGURE 20. ±18V NEGATIVE SATURATION RECOVERY TIME (+25°C)

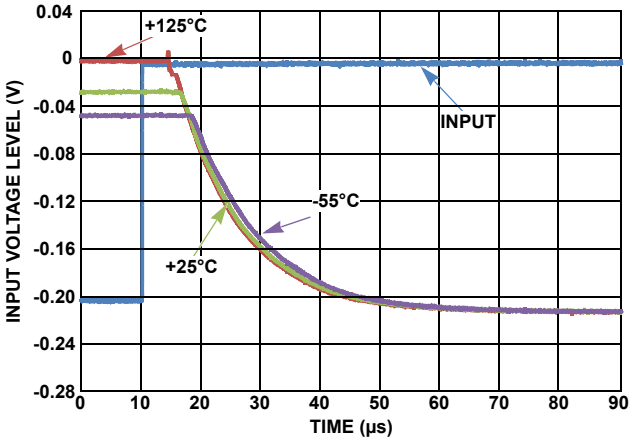

FIGURE 21. ±5V POSITIVE SATURATION RECOVERY TIME (+25°C)

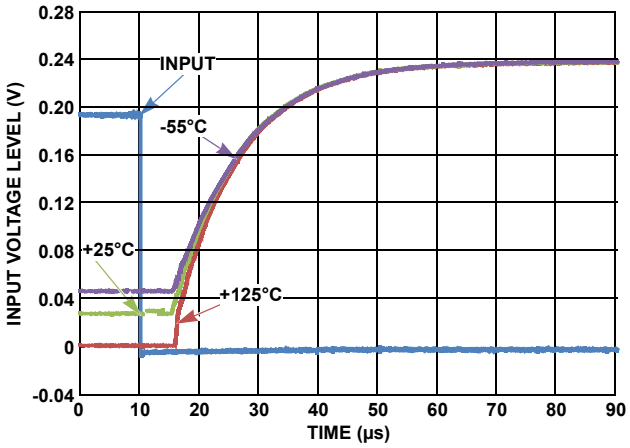

FIGURE 22. ±5V NEGATIVE SATURATION RECOVERY TIME (+25°C)

Revision History

REVISION	DATE	DESCRIPTION
1.0	Jul 1, 2021	Updated BOM, Figure 7, and minor text edits throughout document.
0.0	Oct 31, 2014	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/