ISL71148MNZEV1Z

The ISL71148MNZEV1Z board evaluates the operation of the Renesas ISL71148M radiation tolerant 8-channel high precision 14-bit, 900ksps/480ksps SAR ADC. The evaluation board is used with the RHADC-FMCEV1Z data capture board.

The ISL71148M device on the evaluation board supports the operation of the ISL71148M with AVCC set to 5V. DVCC can be set to 2.5V or 3.3V (default setting is 2.5V). The reference voltage to the ADC is set to 2.5V. The digital I/O voltage of the complex programmable logic device (CPLD) can also be set to 2.5V or 3.3V operational, but it matches the DVCC setting of the ISL71148M. By default, the supply voltage for the CPLD is also connected to the digital I/O voltage. The supply voltages to the analog input amplifier circuit are set to +7.5V/-4.5V. These voltages are all derived from the ±10V supply inputs to the board.

Specifications

- ±10V power supply inputs
- VITA 57.1 FPGA mezzanine card (FMC) connector for interoperability
- Supports -55°C to +125°C operation of the ISL71148M
- Supporting components operate across the temperature range of -40°C to +85°C
- Jumper selectable for +2.5V or +3.3V DVCC and digital I/O operation

Features

This evaluation board evaluates the common performance metrics of the ISL71148M listed in the datasheet. These parameters include:

- Signal-to-noise ratio (SNR)
- Signal-to-noise and distortion ratio (SINAD)
- Effective number of bits (ENOB)
- Total harmonic distortion (THD)
- Spurious free dynamic range (SFDR)
- Input voltage range (analog input)
- REF input voltage range (V_{REF} input)

Required Equipment

- ISL71148MNZEV1Z ADC evaluation board
- RHADC-FMCEV1Z data capture board
- Low phase noise analog signal source (such as the Rohde-Schwarz SMA100B)
- Low phase noise clock source (such as the clock synthesis on the Rohde-Schwarz SMA100B)
- ±10V DC power supply
- 5V, 3.6A switching power supply (such as the CUI ETSA050360UDC-P5P-SZ supplied with the RHADC-FMCEV1Z data capture board)
- USB 2.0 Cable and port on PC
- PC running Windows 10 or greater
- Renesas iRADAnalyzer software

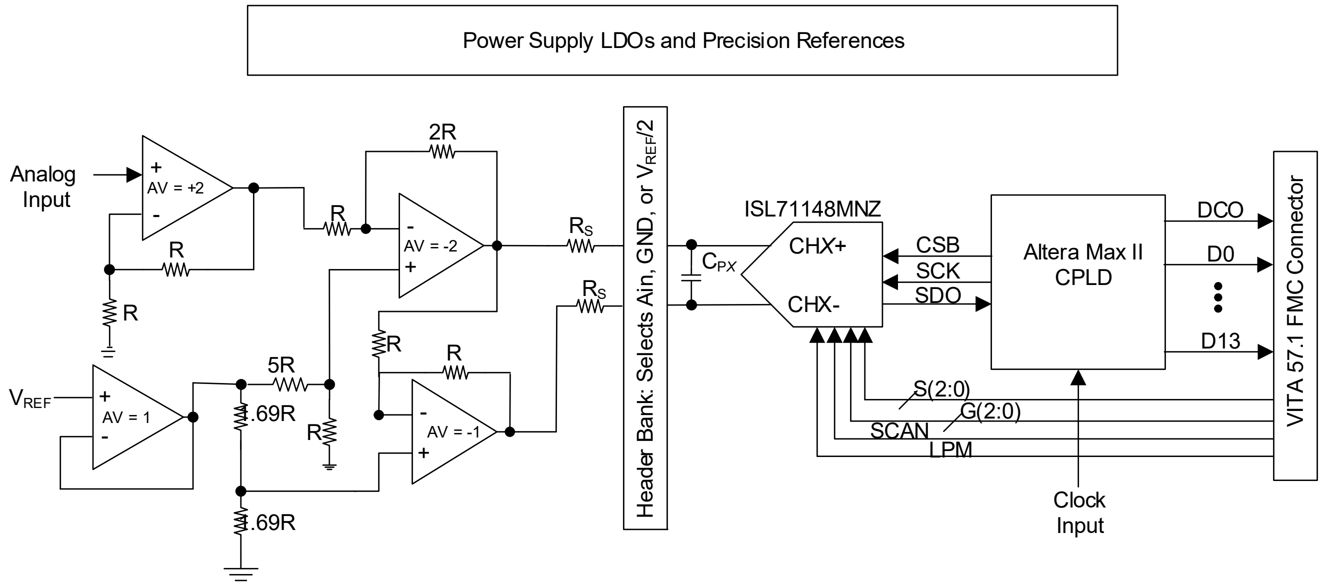

Figure 1. Block Diagram

Contents

1. Functional Description

The digitized data from the ADC is passed to the RHADC-FMCEV1Z using the VITA 57.1 FMC mezzanine connector. The iRADAnalyzer application software controls the capture of data and provides FFT performance data of the ADC. Figure 4 shows the GUI interface of the application software.

Figure 2 shows the location and position of the jumpers on the ISL71148MNZEV1Z board. The default horizontal jumper positions for channels 0 through 8 select the analog signal as the input. These channels can also be set to GND, VREF, or VREF/2 by placing the jumpers vertically at one of the pin columns (Figure 3).

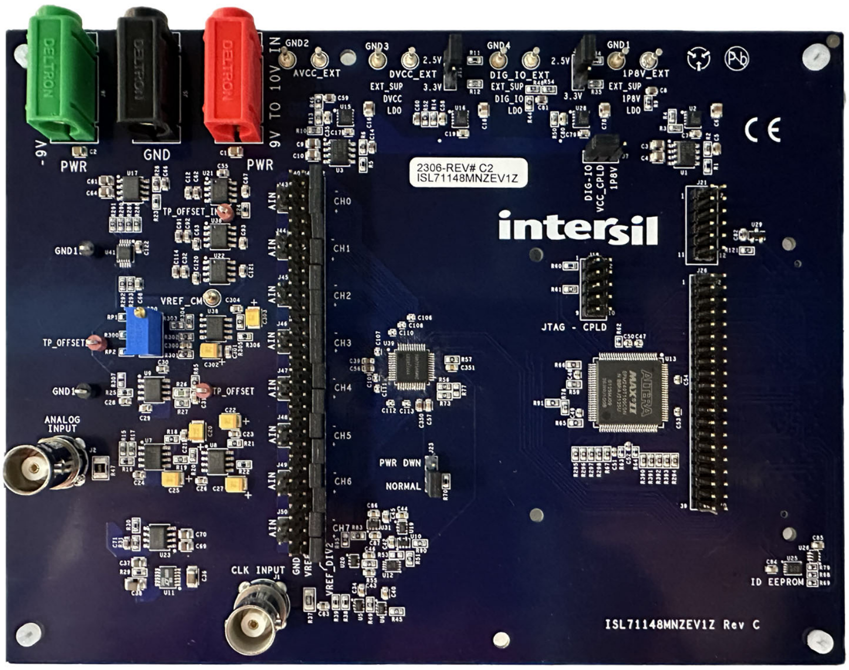

Figure 2. ISL71148MNZEV1Z Evaluation Board Jumper Location

Figure 1 provides a view of the ISL71148M evaluation board, and the RHADC-FMCEV1Z data capture board with the required external connections. Renesas power products ISL80410 and ISL80505 provide the voltages for the various supply domains, while the ISL21090 provides reference voltages for the ADC on the ISL71148M evaluation board. An analog potentiometer, 3296W-1-103LF, adjusts the negative input common mode to achieve its smallest voltage delta from the positive input common mode. A Renesas digital potentiometer, the ISL23315, divides down the voltage from one of the ISL21090 references to allow for proper common mode adjustment when operating the ISL71148M in single-ended by setting the negative channel input to $V_{REF}/2$ = 1.25V. An Altera MAX II CPLD captures the serial data from the ADC and parallelizes the data to present it at the 40-pin parallel connector and the VITA 57.1 FMC mezzanine connector.

Power for the system is provided by ±10V external power supplies on the three banana jack terminals, J4, J5, and J6. Connect the red banana jack (J4) to +10V, the black banana jack (J5) to ground, and the green banana jack (J6) to -10V.

Apply the analog input for the ADC to the BNC connector (J2). This input is terminated to ground using a 50Ω resistor. This input should be a clean, low-phase noise input source. A typical input frequency of 20.3kHz can be used with an amplitude of approximately $700mV_{P-P}$, setting the input level to the ADC at -1dBFS. Renesas recommends using a bandpass filter with sufficient stop-band attenuation to limit the harmonic distortion from the analog input source. A Q70 series bandpass filter in the 5294 case size with maximum-sized inductors and bandwidth of ≤30% from TTE is recommended. An alternative may also be used.

Apply the input clock to the BNC connector (J1). This clock is the master clock reference for the ISL71148M evaluation board. The sample rate of the ISL71148M is dependent on the input clock frequency and the mode of operation. For the maximum 900ksps sample rate operation of the ISL71148M ADC, an input clock rate of 100MHz is required, and the ADC must be operated with the PGA bypassed. While the ADC supports sample rates near DC (extremely sparse sampling over time), the evaluation board hardware minimum capture size is 32k samples; therefore, consider the acquisition time to collect this sample amount for low sample rates. Renesas recommends using a sample rate of at least 10ksps or higher because of the time required to acquire 32k samples. In addition, keep the input frequency appropriate to avoid severely undersampling the ADC (for example, set an input frequency <10x the sample rate).

The Altera Max II CPLD on the ISL71148M evaluation board takes the serial ADC data and parallelizes the data. The data output from the CPLD to the FMC connector is delivered to the Virtex 5 FPGA on the RHADC-FMCEV1Z data capture board. It is collected on the data capture board and passed using a USB to the PC to the iRADAnalyzer software application for processing.

The sample data and the channel/gain information bit data from the ISL71148M can be accessed directly from connectors J26 and J21, respectively, which allows access to observe and/or process the data externally. However, the ISL71148MNZEV1Z board must remain attached to the RHADC-FMCEV1Z data capture board to select the desired operating mode of the ISL71148M.

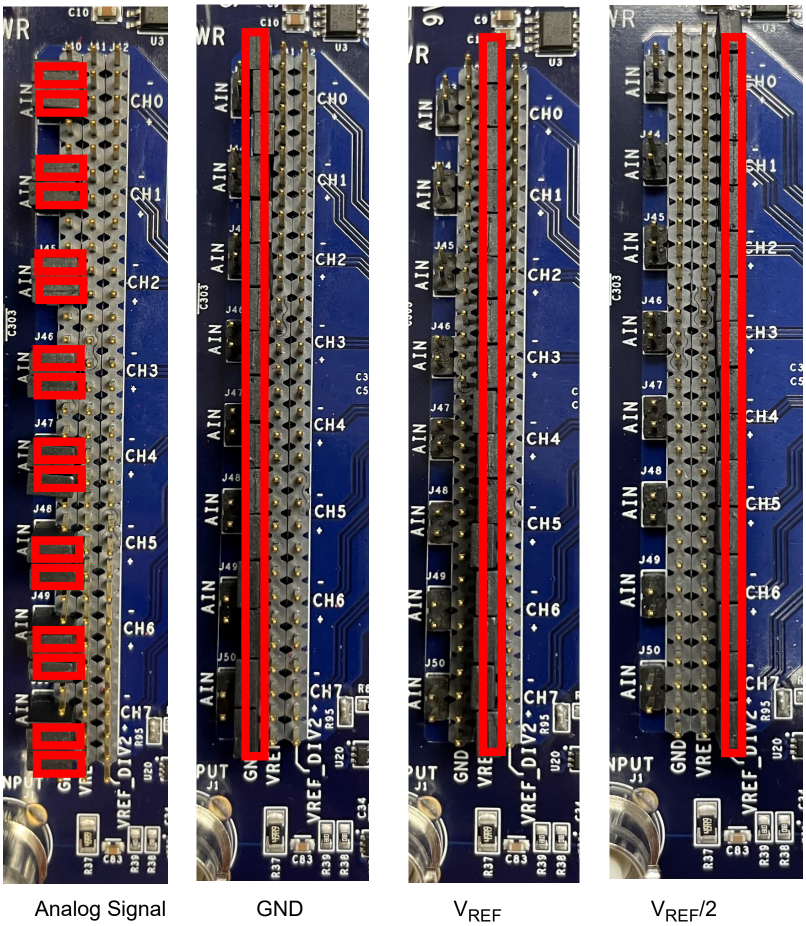

Figure 3. Jumper Position for Channel Input Selection

1.1 Operating Range

The ISL71148M device on the evaluation board supports operation from -55°C to +125°C. However, many of the components used on the evaluation board support a commercial temperature range of -40°C to +85°C. This evaluation board operates under ambient temperature conditions at 25°C. The ISL71148M device is heated or cooled across its operating temperature from -55°C to +125°C if an appropriate instrument (such as a Thermostream or similar) sets the device temperature.

1.2 Connecting the Evaluation and Data Capture Boards

Complete the following steps to connect the ISL71148MNZEV1Z and RHADC-FMCEV1Z boards properly.

1. Connect the supplied CUI 5V switching power supply to the RHADC-FMCEV1Z.
2. Connect a USB cable between the PC and the RHADC-FMCEV1Z. The board should be listed in the device manager on the PC as Renesas RHADC-FMCEV1Z under Universal Serial Bus Controllers (Figure 4).

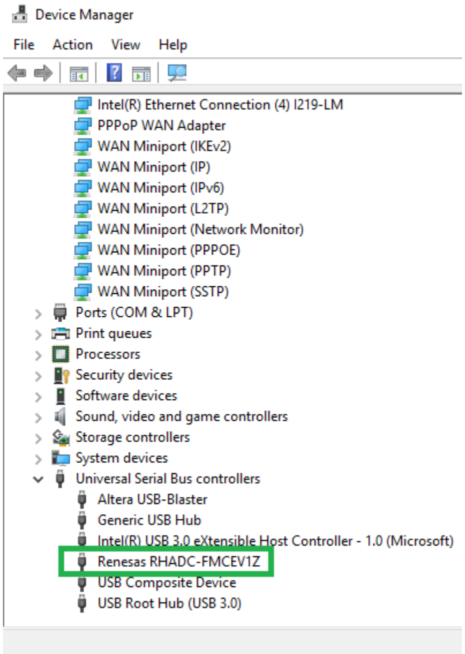

Figure 4. USB Device Driver in Device Manager

3. Connect the ISL71148M ADC evaluation board to the RHADC-FMCEV1Z data capture board. Four standoff guides on the RHADC-FMCEV1Z fit into alignment holes on the ISL71148M evaluation board that help to align the FMC connectors of the two boards. Carefully press the ISL71148M evaluation board into place on the RHADCFMCEV1Z board.
4. Ensure the jumpers are placed on the ADC evaluation board (Figure 2).
5. Supply ±10V and ground to the banana jacks on the ADC evaluation board.
6. Provide a clean, low-phase noise 100MHz input clock to the CLK INPUT connector (J1) on the ADC evaluation board. This placement provides the reference clock to the board, which sets the Convert Start Bar (CSB) signal to the ADC.
7. Provide a clean, low-phase noise 20.3kHz analog input tone to the ANALOG INPUT connector (J2) on the ADC evaluation board through a bandpass filter such as the Q70 series 30% bandwidth TTE bandpass filter.

8. Make all connections (Figure 5).

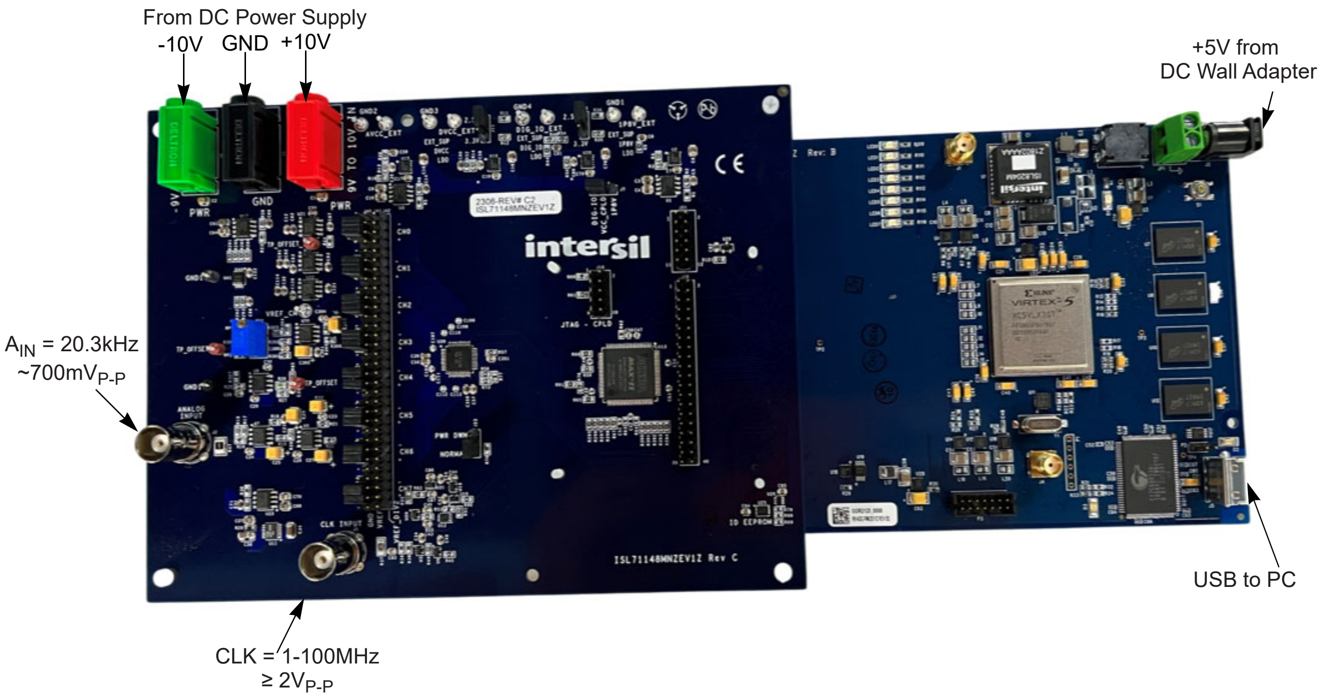

Figure 5. ISL71148MNZEV1Z/RHADC-FMCEV1Z Connection Diagram

1.2.1 iRADAnalyzer RHADC-FMCEV1Z Board Initialization

When the ISL71148MNZEV1Z board and the RHADC-FMCEV1Z board have been connected and set up correctly, open iRADAnalyzer on the PC by clicking **Start** > **Renesas iRADAnalyzer** > **iRADAnalyzer**. When the board is detected and configured by the iRADAnalyzer software application, it should indicate **Board Initialized** in the status window of the GUI (Figure 6).

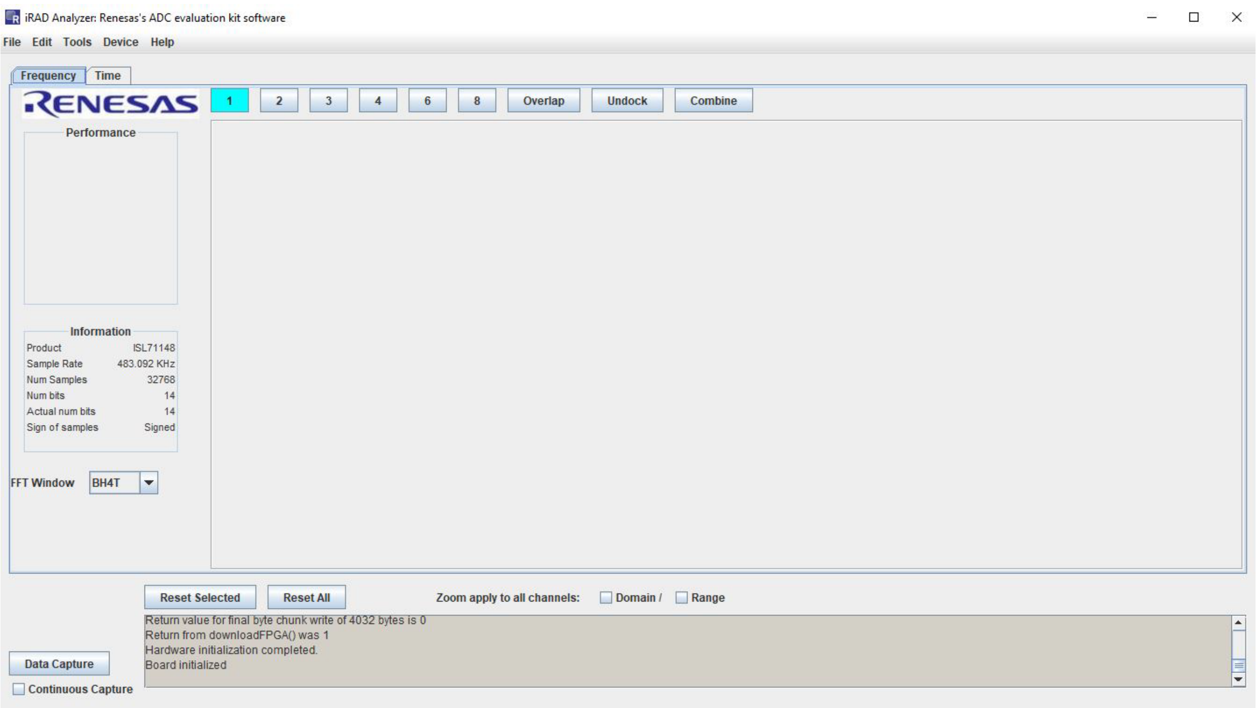

Figure 6. iRADAnalyzer Board Initialization

1.2.2 iRADAnalyzer Data Capture Settings

Verify the **Data Capture** settings under the **Edit** > **Data Capture** menu match the hardware configuration. The default input clock is set to 100MHz. If another frequency is required, enter it here, and the iRADAnalyzer automatically calculates the sample rate based on the ISL71148M device configuration. In this example, the ISL71148M has been configured with the PGA enabled to gain 2 in normal mode and no information bits are selected.

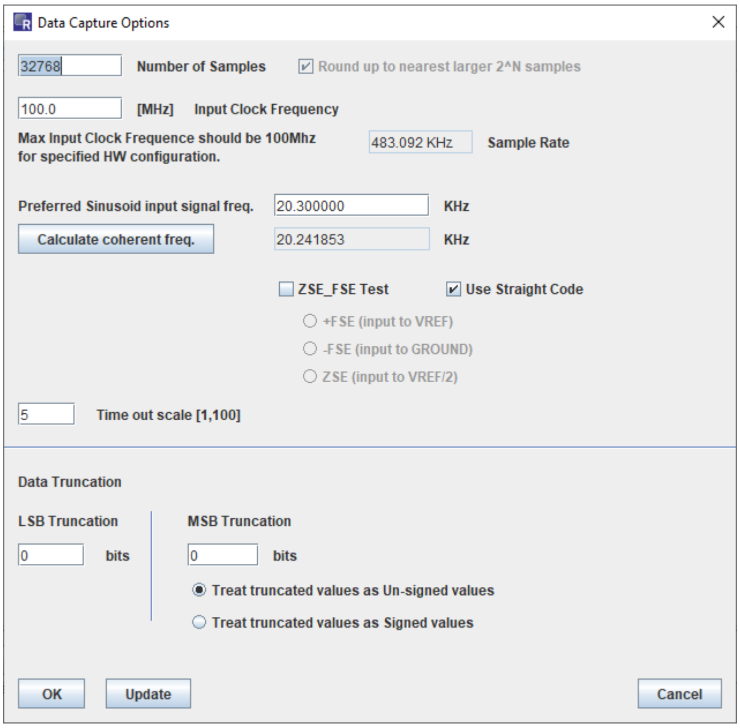

Figure 7. iRADAnalyzer Data Capture Settings

1.2.3 iRADAnalyzer Device Settings

The ISL71148M can be configured into different operation modes, configured from the **Settings** selections under the **Device** menu in iRADAnalyzer. The ISL71148M has an integrated Programmable Gain Amplifier (PGA) and an 8-channel multiplexer. The PGA may be bypassed if required and, when enabled, has available gain settings of 1, 2, 3, 4, 6, 8, 12, and 16. Up to eight channels can be selected for data capture. Each channel can have a different gain setting if required. However, iRADAnalyzer changes the gain setting using the gain select pins G[2:0] between data captures for each channel because there is one PGA inside the ISL71148M. The analog input common mode is set to $V_{REF}/2 = 1.25V$.

The ISL71148M can operate in normal mode or in low power mode to reduce power consumption. In either of these modes, the ISL71148M can provide channel and gain information (Info Bits) along with the sample data on the output SPI port. If operating with the PGA bypassed, the evaluation system provides only the channel information if Info Bits is selected and does not provide the gain information. The resolution defaults to 14 bits, which is the resolution of the ISL71148M.

For more information about the operating modes, see the *ISL71148M Datasheet*.

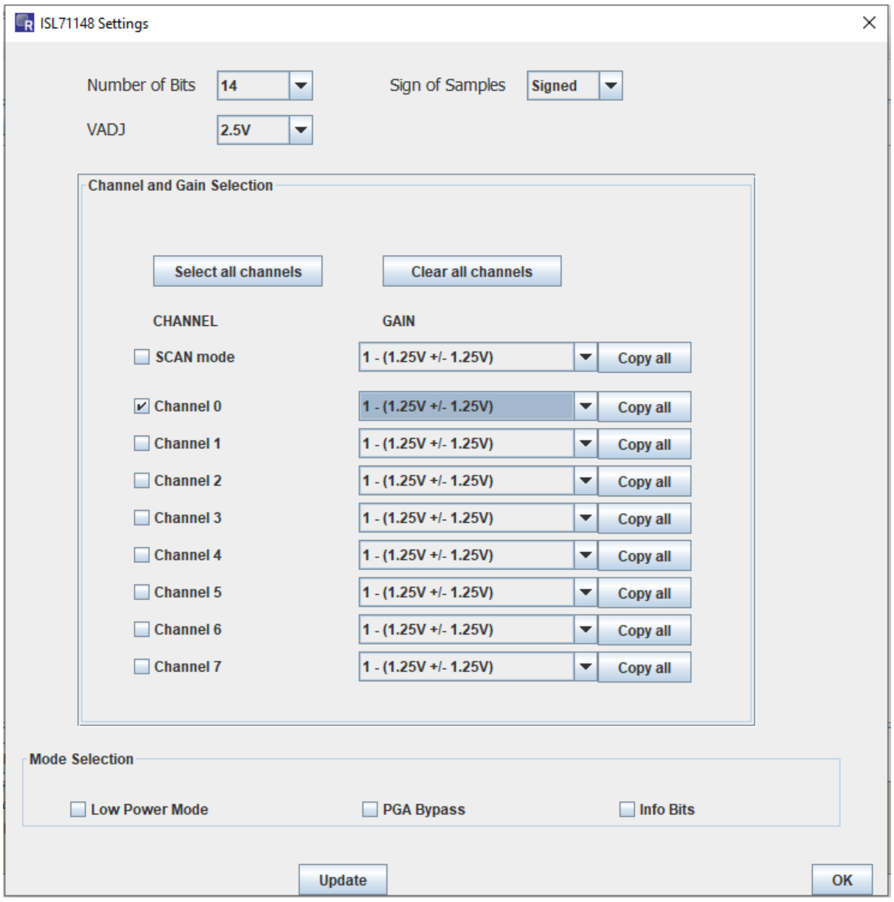

Figure 8. iRADAnalyzer Device Settings (Normal Mode, PGA Gain = 1, Signed)

Table 1 provides the information bits, sample period, and sample rate for all the various modes of the ISL71148M. The first three columns correspond to the three checkboxes under **Mode Selection** in the **Device Settings** menu (Figure 8). The sample period and rate shown are based on an input clock frequency 100MHz. If another input clock frequency is used, the sample period and rate change accordingly. To calculate the sample rate with a different input clock frequency, multiply the number in the sample period column by 100 and divide the input clock frequency by that result. For example, when operating in normal mode with PGA bypassed and no info bits, if an input clock frequency of 90MHz is used, the resulting sample rate is 90MHz/111 = 810.810ksps. While the ISL71148M has no lower limit on the sampling frequency, consider the sample collection time when using low sample rates because the minimum capture size is 32k samples.

Table 1. Operating Mode Information

Mode	PGA	Info Bits	Channel Bits	Gain Bits	Sample Period (µs)	Sample Rate (ksps)
Normal	Bypassed	No	No	No	1.11	900.901
Normal	Bypassed	Yes	Yes	No	1.17	854.701
Normal	Enabled	No	No	No	2.07	483.092
Normal	Enabled	Yes	Yes	Yes	2.19	456.621
Low Power	Bypassed	No	No	No	1.46	684.932
Low Power	Bypassed	Yes	Yes	No	1.52	657.895
Low Power	Enabled	No	No	No	2.42	413.223
Low Power	Enabled	Yes	Yes	Yes	2.54	393.701

1.2.4 iRADAnalyzer Data Capture - FFT

To begin the data capture from the ADC evaluation board, click on the **Data Capture** button in the iRADAnalyzer software application. The software captures the data and provides an FFT of the results (Figure 9).

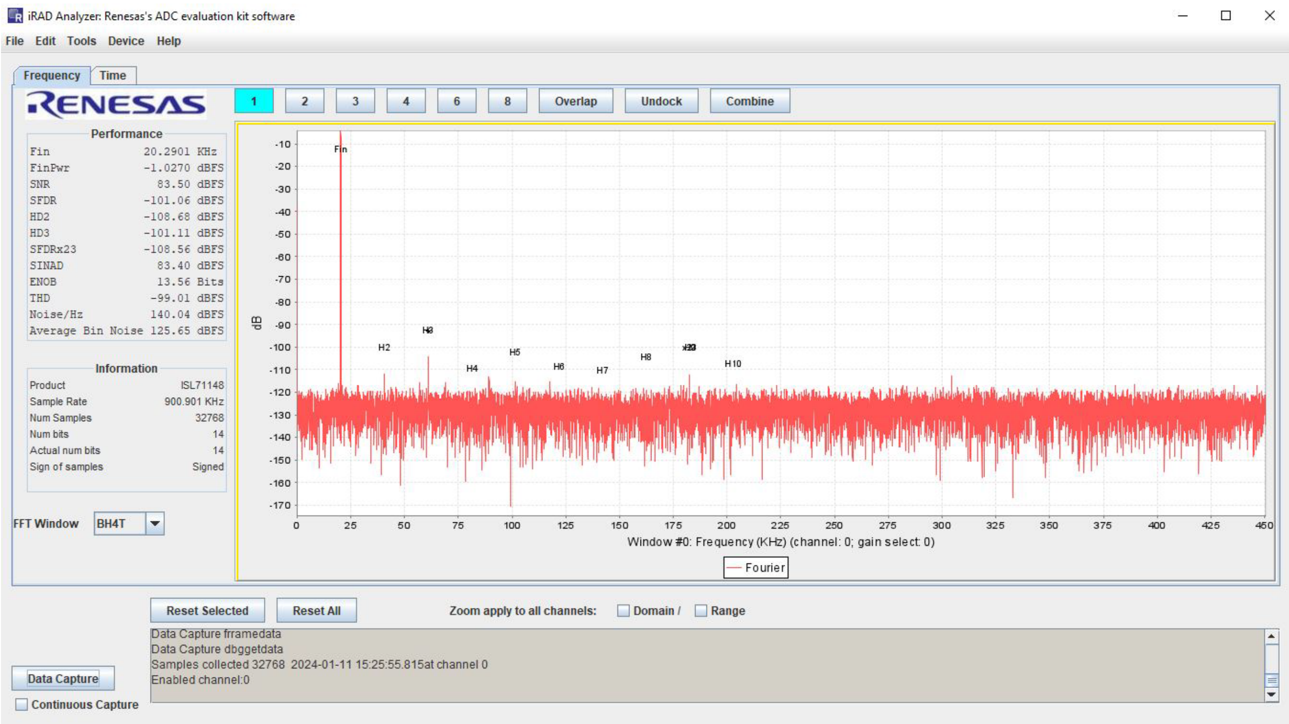

Figure 9. iRADAnalyzer FFT Plot

1.2.5 iRADAnalyzer Data Capture - Channel and Mode Selections

Up to eight channels can be displayed simultaneously on the ISL71148M in iRADAnalyzer. Select the channels from the **Settings** menu under the **Device** tab. The number of bits (default is 14), the VADJ voltage, the required channels, the required gains, the power mode, the PGA function, and the info bits can all be selected from this menu. The VADJ voltage can also be selected here and should match the jumper settings on the ISL71148MNZEV1Z evaluation board for the DVCC and DIG_IO supply domains (that is, if DVCC and DIG_IO are set to 2.5V the VADJ must match that voltage and also be set to 2.5V). The required channels and gains can also be set using the selections in this window. Any number of channels can be selected, and any gain value can be chosen. The **Select All Channels**, **Clear All Channels**, and **Copy All** shortcut buttons can be used to make channel selection easier. The checkboxes can be selected to determine if Low Power Mode, PGA Bypass, or Info Bits are enabled. To apply the selections, click **Update** and then **OK** to apply the settings and close the window.

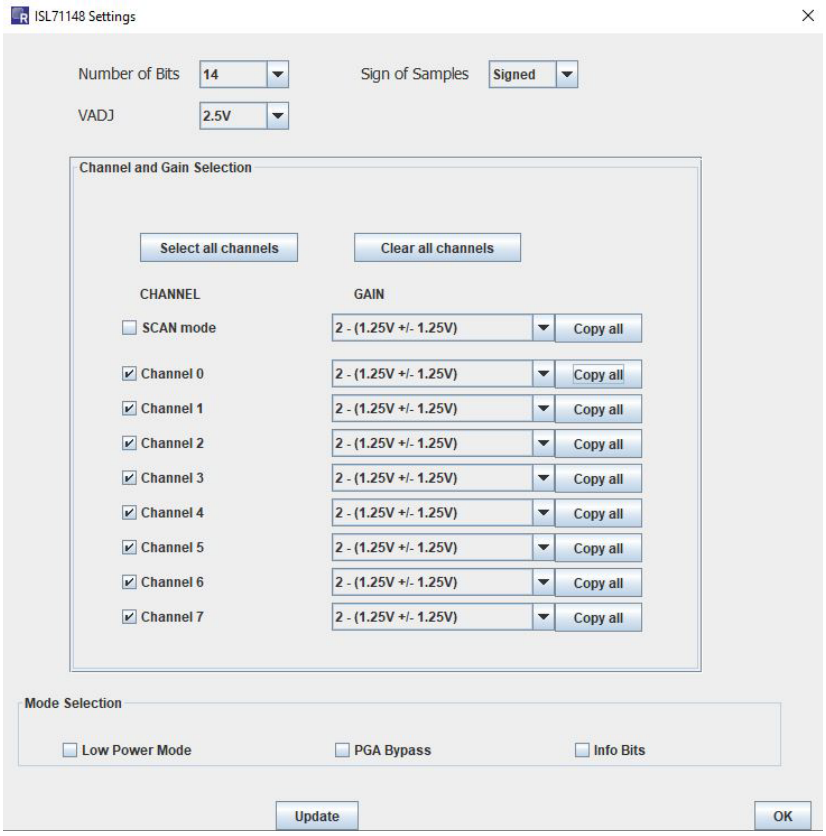

Figure 10. iRADAnalyzer Channel Selection Settings

The numbered boxes above the graph can be used to select 1, 2, 3, 4, 6, or 8 channels to display. When channels have been selected for measurement, the required channels for display must be chosen by clicking on one of these boxes. In this example, all eight channels are selected. A shortcut box can be used to select all eight channels to display.

Figure 11. iRADAnalyzer Channel Selection for Plotting

When the required channels for plotting are shown, a measurement can be performed. The active graph is highlighted in yellow. Figure 12 shows a display of eight channels with channel 0 highlighted. All eight channels are configured on the evaluation board to receive the same input signal. Each channel display can be zoomed if required by clicking and dragging to create a box in the required plot window for the zoomed-in area. To reset the selected plot, click **Reset Selected** to restore it to the full data plot. In addition, the **Reset All** button restores all the channels to the full data plot.

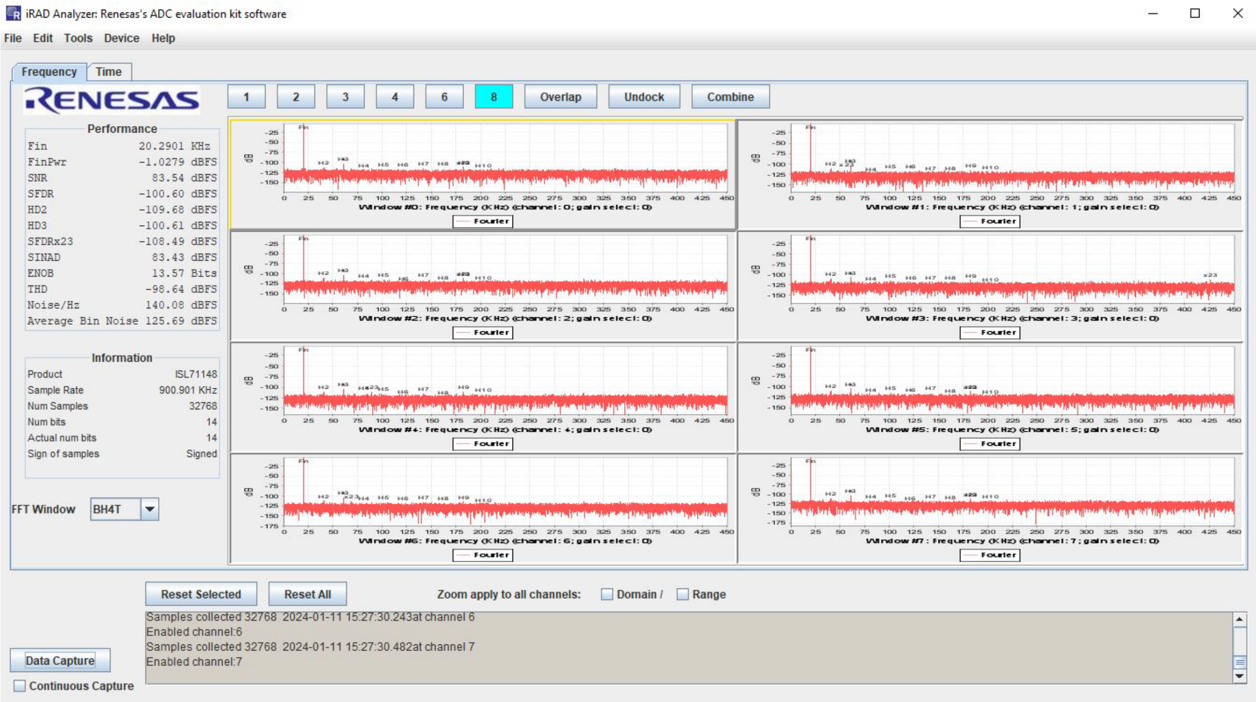

Figure 12. iRADAnalyzer FFT Plot of Eight Channels

In this example, all eight channels are selected for display. Similarly, SCAN mode can be enabled by clicking the checkbox, which places the ISL71148M into SCAN mode, where the ADC sequences through all eight channel inputs in order from Ch 0 to Ch 7 in a repeating manner. At each falling edge of CSB, the ISL71148M increments the channel. This results in a reduction of the sample rate of each channel by a factor of 8. The Info Bits checkbox must also be enabled if SCAN mode is enabled, allowing the iRADAnalyzer to read the information bits in the output data of the ISL71148M to synchronize data collection to the proper channel.

The data from the channels can be displayed in a few different ways using the buttons above the plots. The plots can overlap into a signal plot using the **Overlap** button. This option combines all selected channels into one plot, giving each channel a different color (Figure 13). This feature is enabled and disabled by clicking the **Overlap** button.

Figure 13. iRADAnalyzer Overlap of 8 Channels

The channel currently selected (indicated by the yellow highlight around the box) can be undocked for individual display, which is accomplished by clicking the **Undock** button. Any number of channels that have been measured can be undocked from the main display into a separate window. Each window is labeled with the channel number and gain selection. For example, the undocked window for Channel 2 is shown in Figure 14.

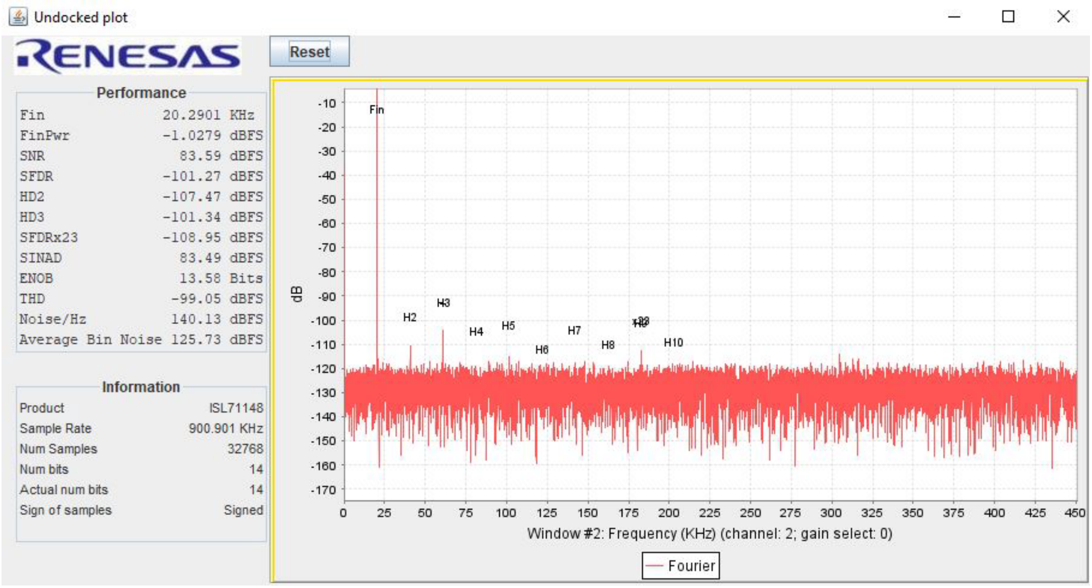

Figure 14. iRADAnalyzer Undocked Window for Channel 2

Individual plots can be combined into one plot by using the **Combine** button. To start combining plots, select the first required plot (a yellow border will appear around the plot); next, click the **Combine** button. Clicking the **Combine** button adds the selected plot to a separate plot window and allows the selection of an additional plot to combine from the main window (Figure 15). To add other channels, click to select the next plot (highlighted in yellow) and then click the **Add** button. It appears in the main window after clicking the **Combine** button.

Figure 15. iRADAnalyzer Main Window for Combining Multiple Plots

In this example, the data from Channel 1 and Channel 2 are combined into a separate plot window shown in Figure 16. When all required plots have been added, click the **Done** button in the main window. Similar to the main window, the plots selected to be combined can also be overlapped from within the combined window by clicking the **Overlap** button in the window.

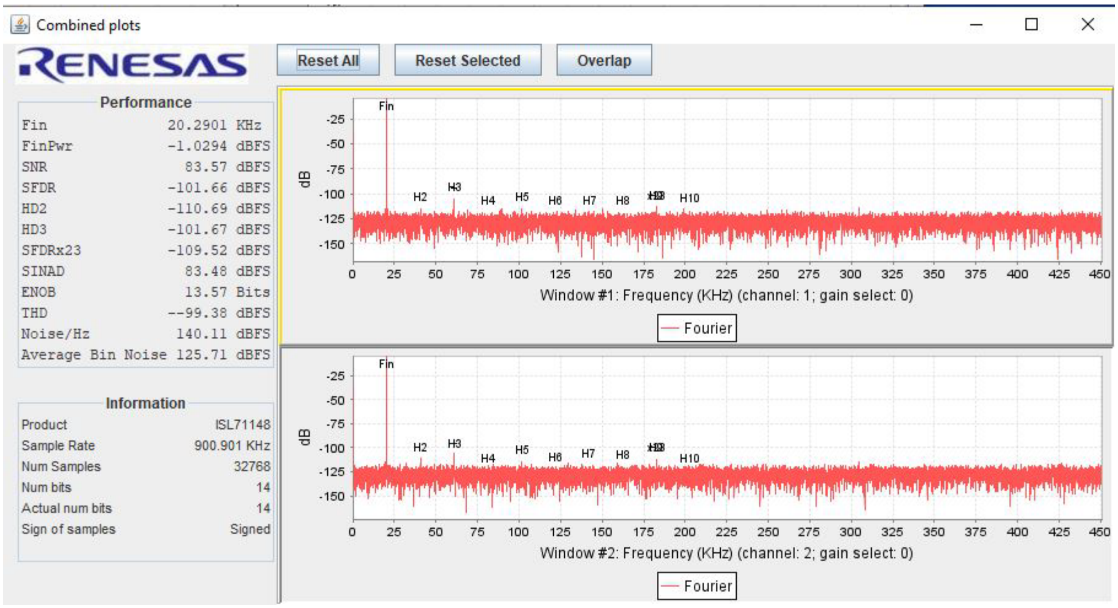

Figure 16. iRADAnalyzer Window with Combined Plots

1.2.6 iRADAnalyzer Data Capture - Time Domain

The time domain plot of the captured data can be viewed. To do so, click on the **Time** tab in the iRADAnalyzer GUI. This action plots the entire data capture in the time domain. Renesas recommends using the mouse to click and drag a zoom box in the time domain plot to see the waveform (Figure 17).

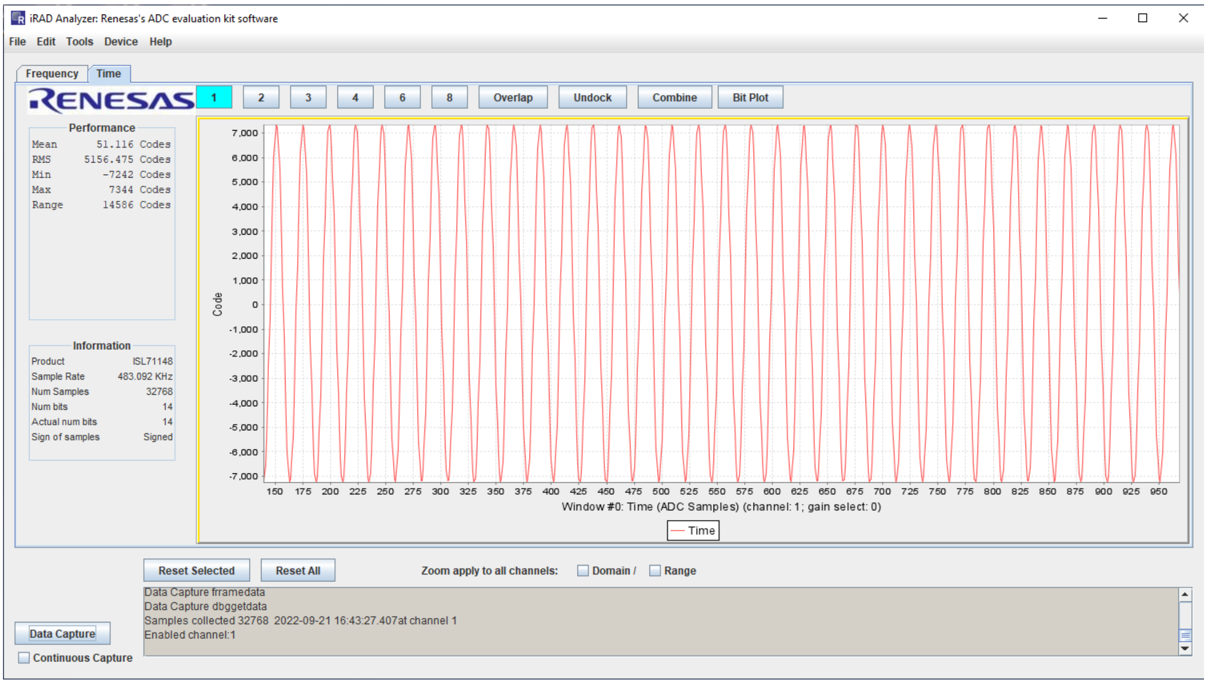

Figure 17. iRADAnalyzer Time Domain Plot

All plot features, overlap, undock, and combine, can be used when viewing the time domain plots in iRADAnalyzer and operate in the same manner as when viewing the frequency domain plots. The **Time domain** tab (Figure 18) offers an additional view called Bit Plot, which shows the individual bits plotted over time.

Figure 18. iRADAnalyzer 8-Channel Time Domain Plot

To activate the Bit Plot, select a channel to highlight it in yellow. It brings up a separate window (Figure 19). This plot can be zoomed and reset like the frequency and time domain plots. Renesas recommends zooming to make the bits more easily visible. The individual bits can be viewed in separate plots using the **Split** button if required. When the plots are split, a **Consolidate** button appears and can recombine the bits into the same plot again.

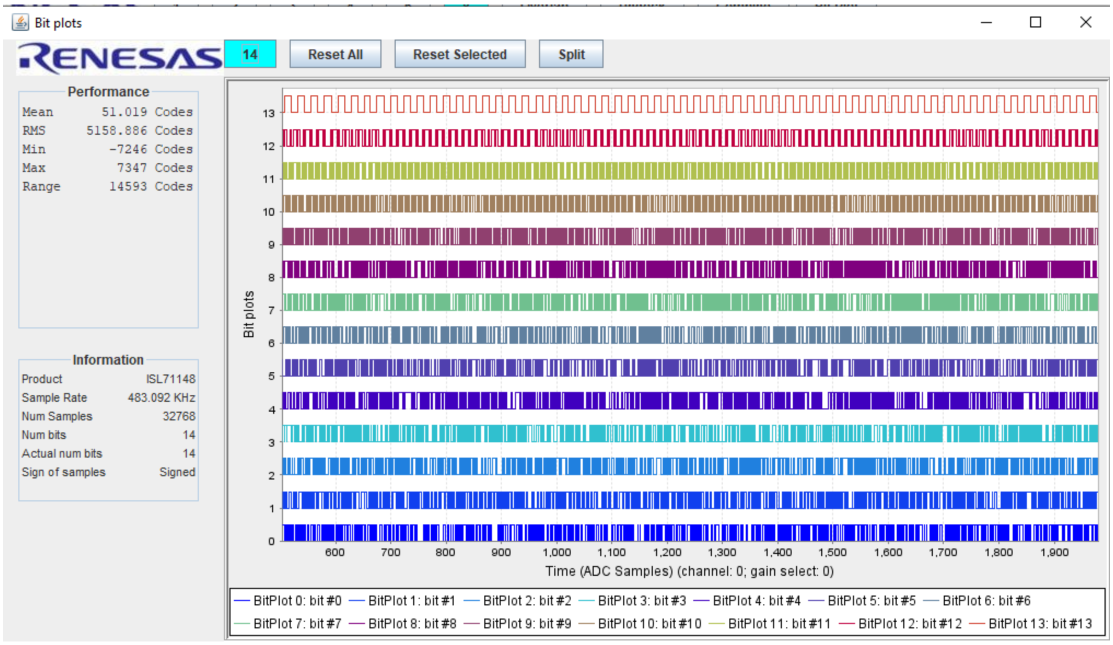

Figure 19. iRADAnalyzer Time Domain Bit Plot

1.2.7 iRADAnalyzer - Save Data Files

When the required data is collected, the iRADAnalyzer GUI can save the raw decimal data or the FFT data to a file. To save the raw decimal data to a file, select **File** > **Save Data File** > **Save Time Domain**. To save the FFT data to a file, select **File** > **Save Data File** > **Save Fourier Domain**. The menu options are shown in Figure 20.

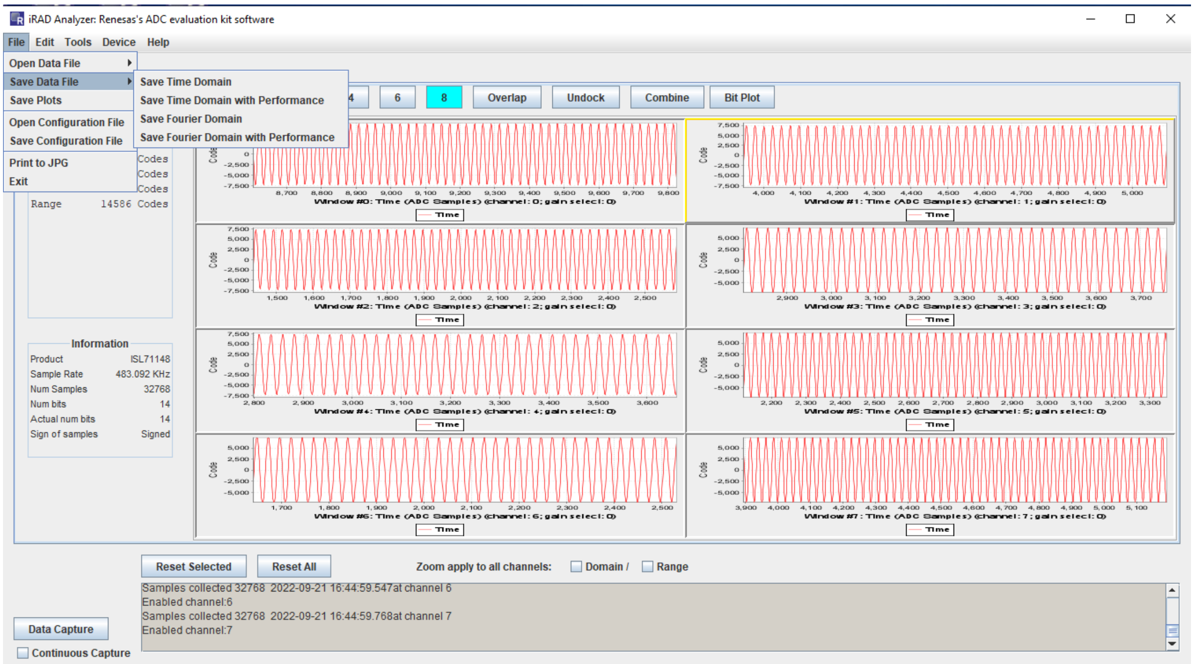

Figure 20. Using iRADAnalyzer to Save Data Files

2. Board Design

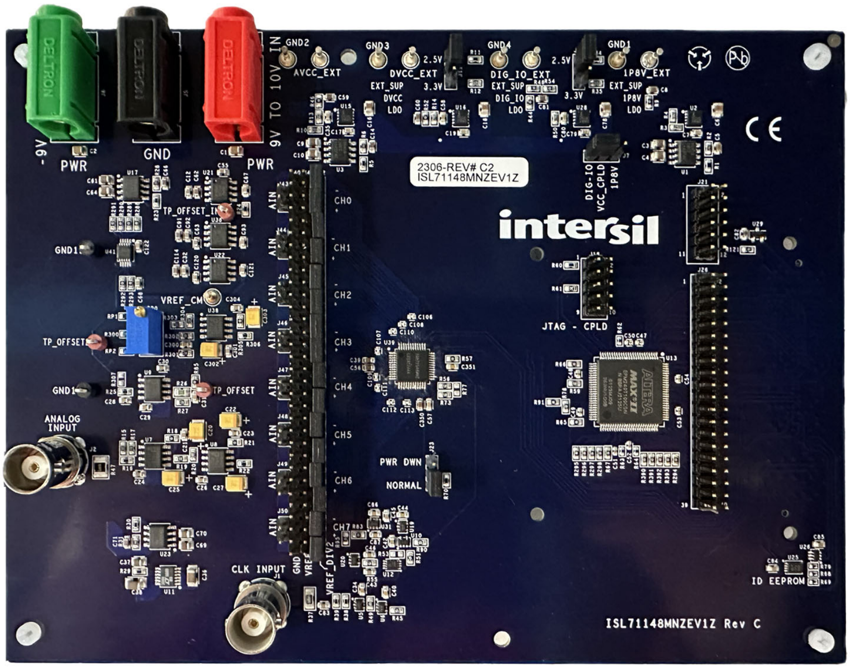

Figure 21. Evaluation Board (Top)

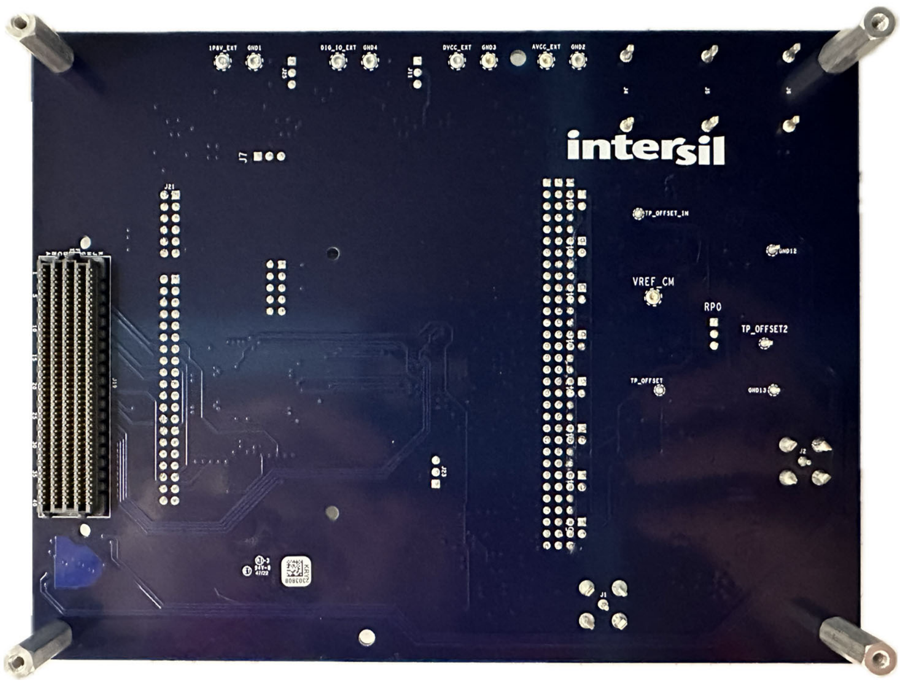

Figure 22. Evaluation Board (Bottom)

2.1 Layout Guidelines

For information about layout guidelines, see the *ISL71148M Datasheet*.

2.2 Board Schematics

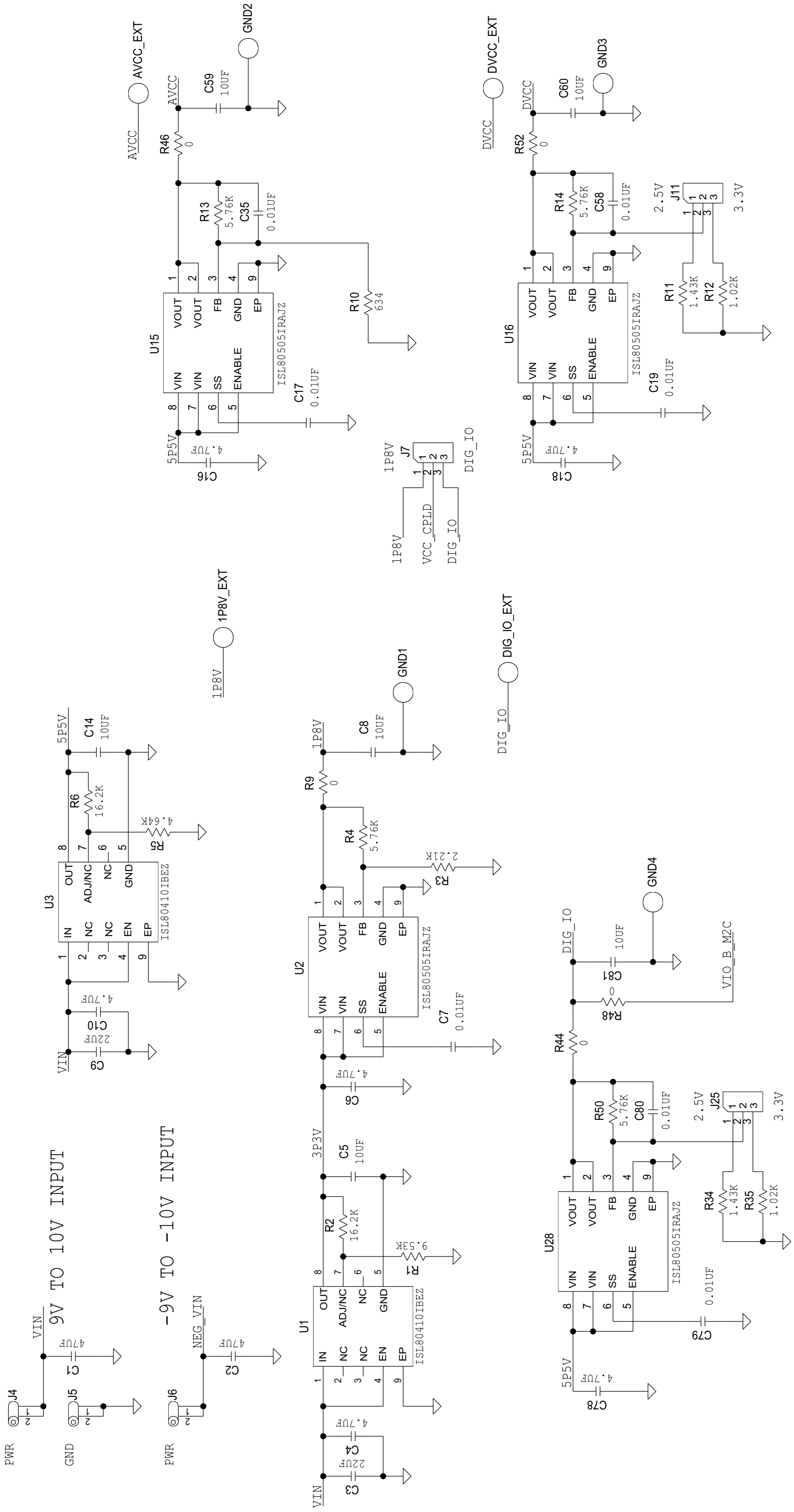

Figure 23. ISL71148M Board Schematic - DUT Power Supply Circuit

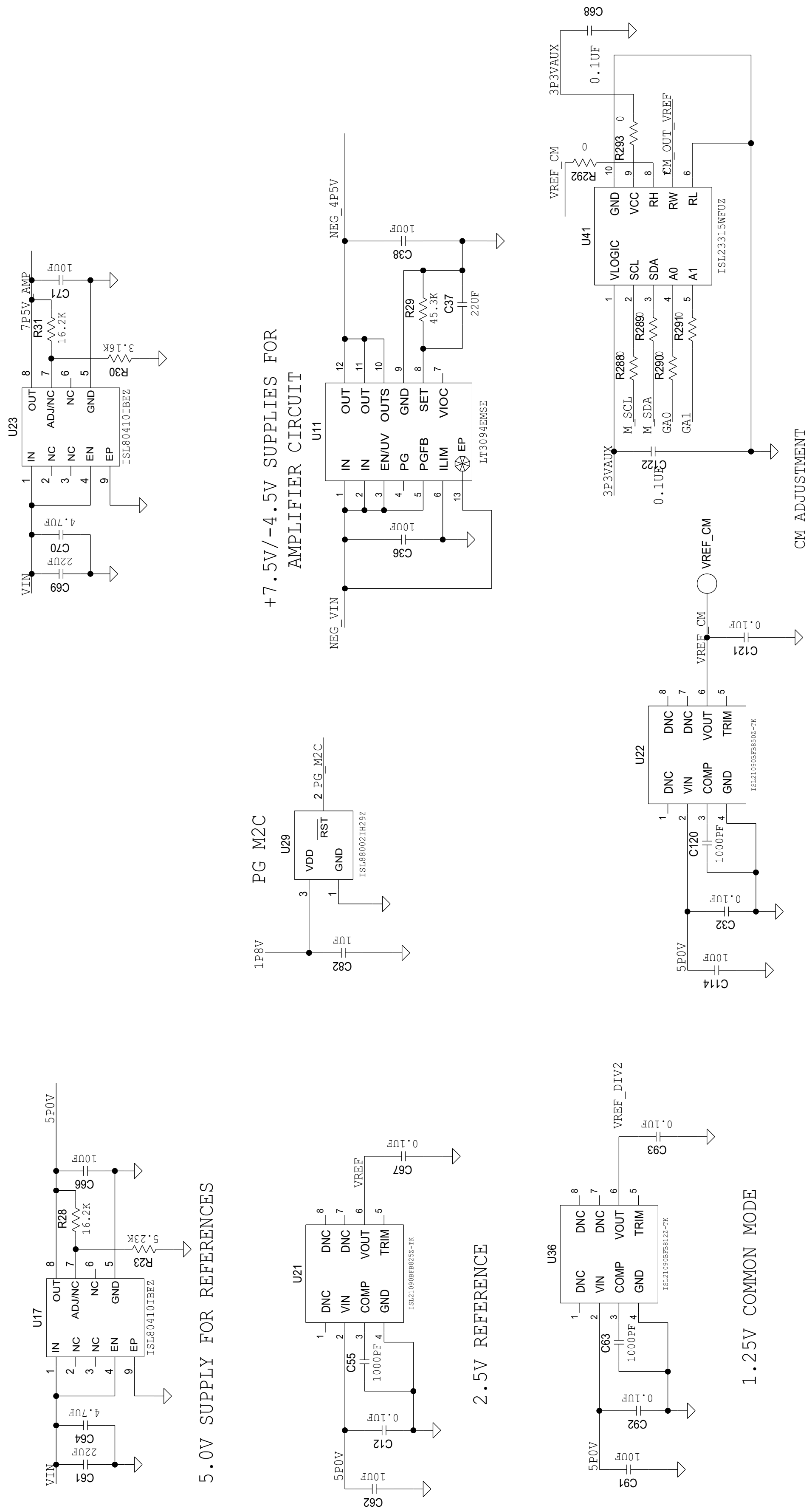

Figure 24. Amplifier Power Supply and VREF Circuits

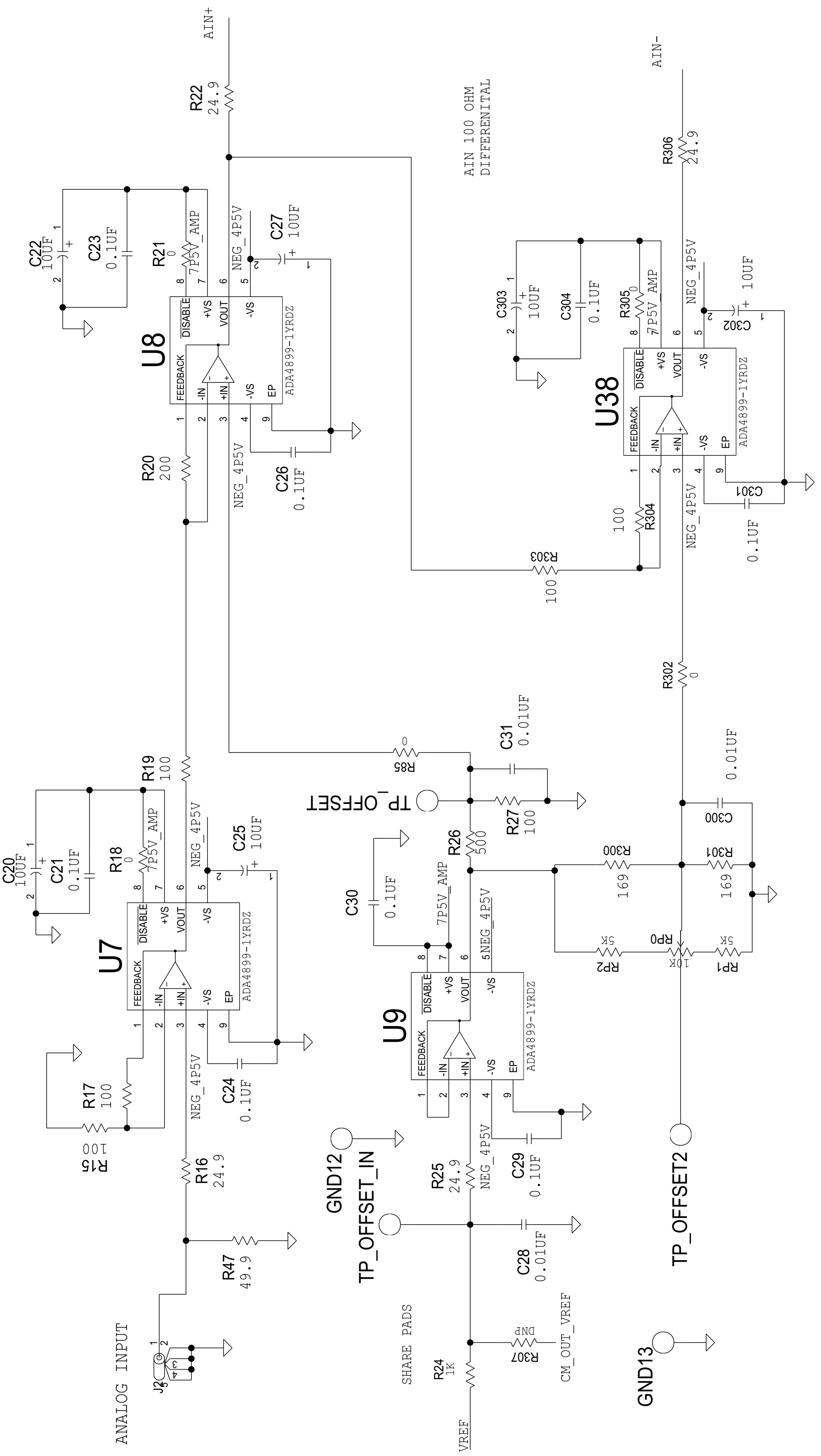

Figure 25. Analog Input Amplifier Circuit

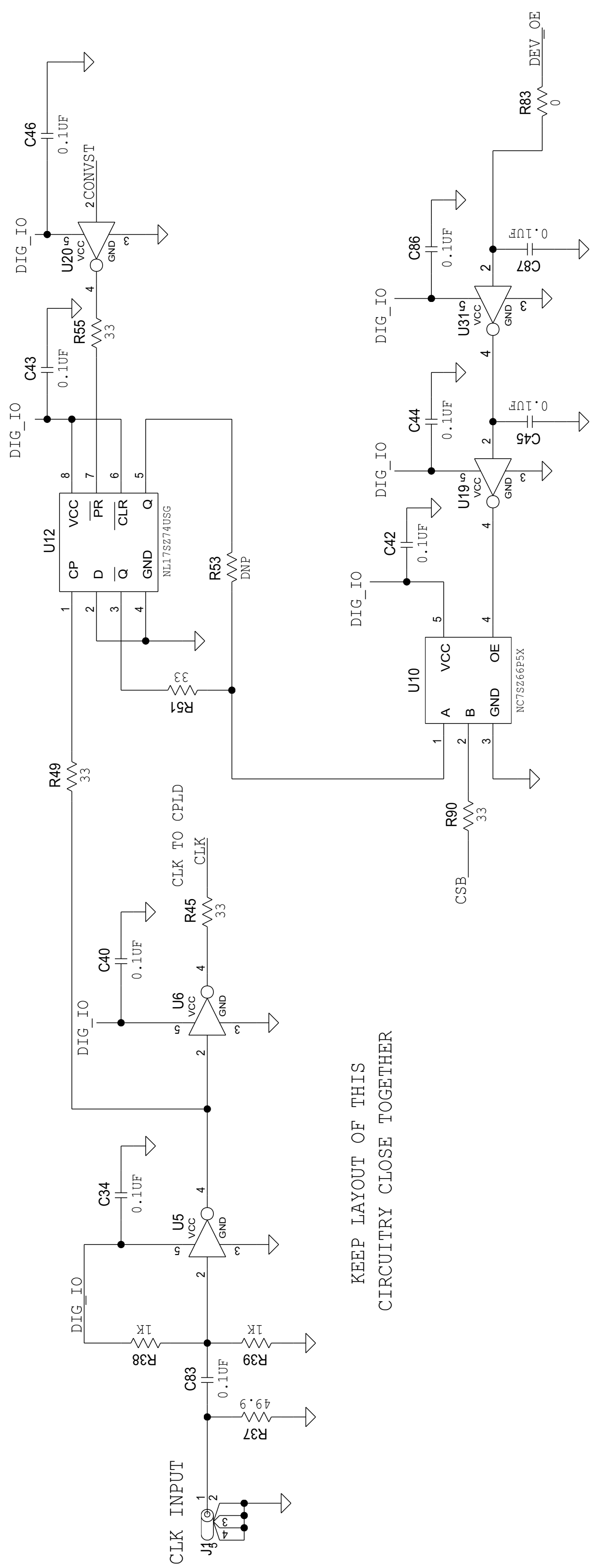

Figure 26. Passive Analog Input and Clock Circuits

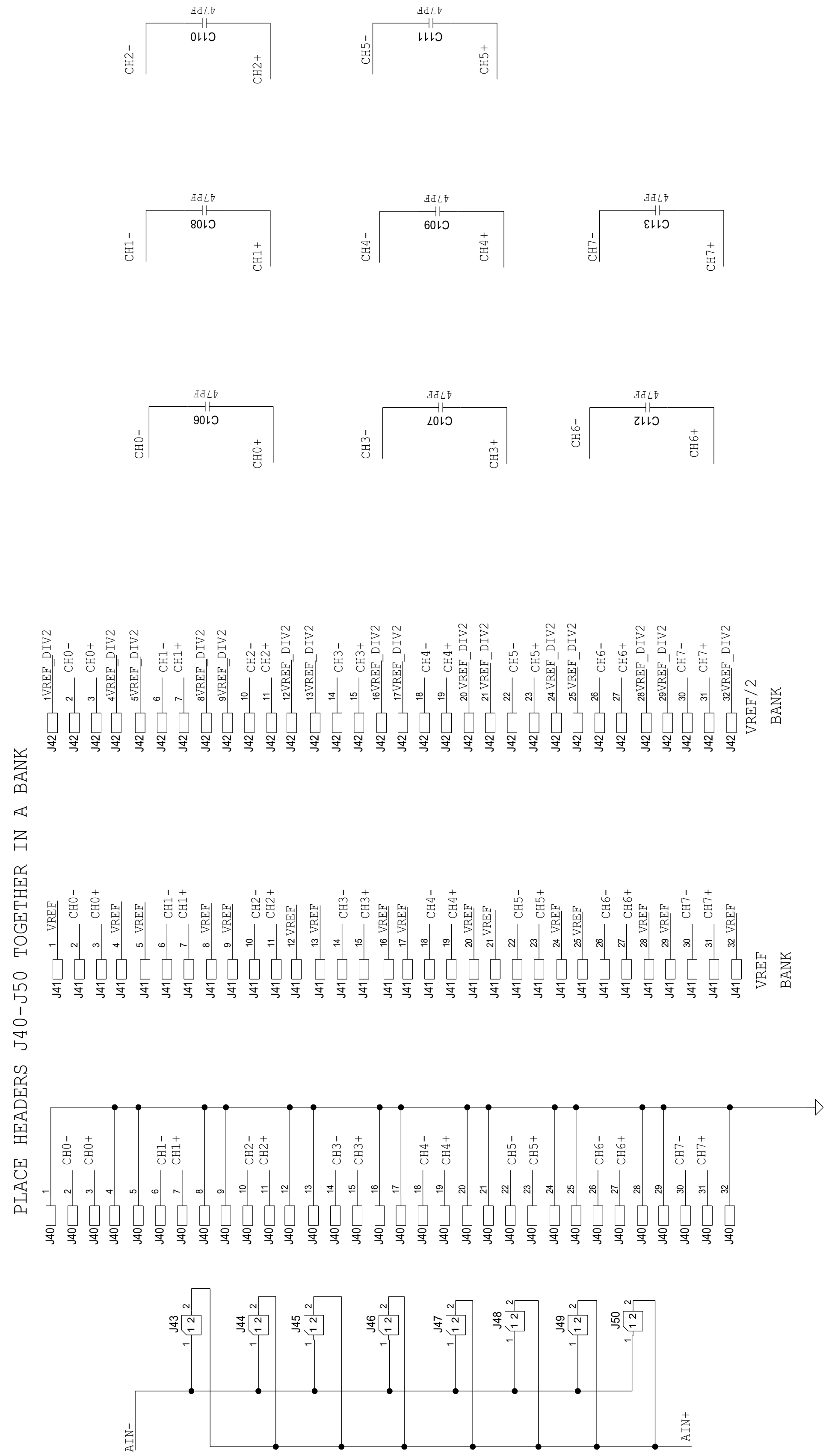

Figure 27. ADC Channel Input Circuitry

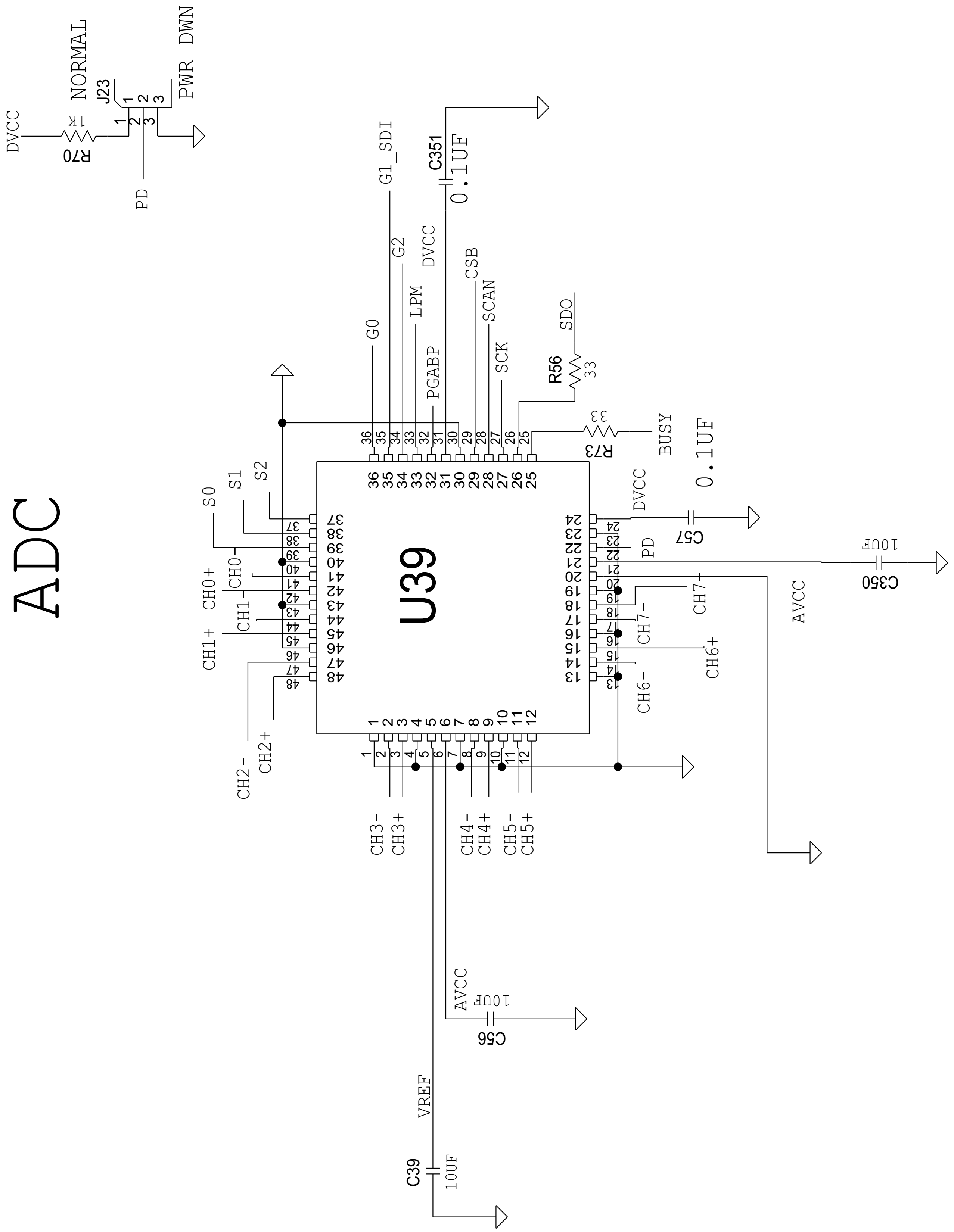

Figure 28. ADC Connections

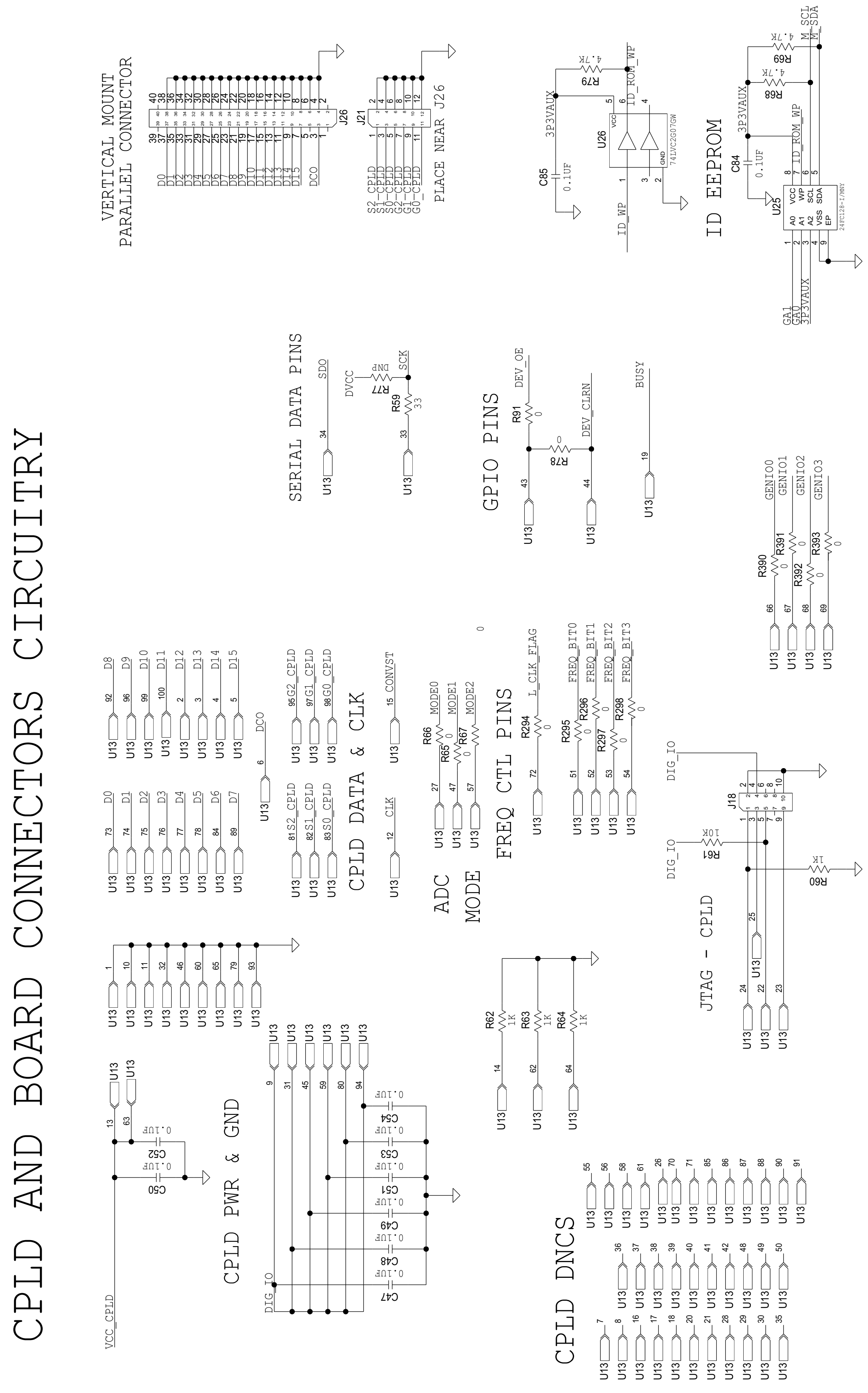

Figure 29. CPLD and Board Connector Circuits

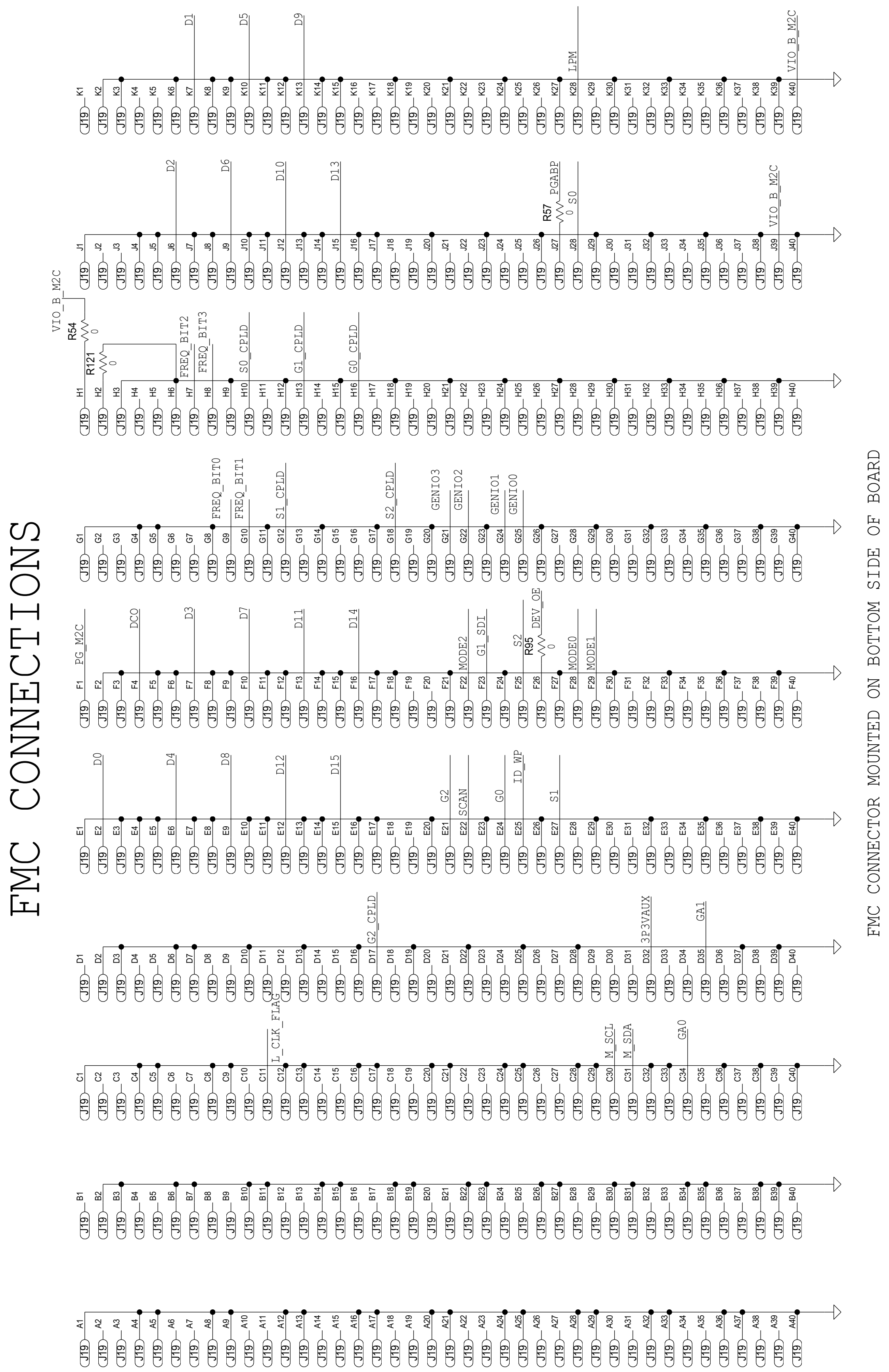

Figure 30. FMC Connector Circuit

2.3 Bill of Materials

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1		PCB, ISL71148MNZEV1Z, REVC, ROHS	Avanti	ISL71148MNZEV1ZREVAPCB
30	C12, C21, C23, C24, C26, C29, C30, C32, C34, C40, C42, C43, C44, C45, C46, C57, C67, C68, C83, C84, C85, C86, C87, C92, C93, C121, C122, C301, C304, C351	CAPACITOR, SMD, 0603, 0.10µF, 50V, 10%, X7R	TDK	C1608X7R1H104K
8	C4, C6, C10, C16, C18, C64, C70, C78	CAP-AEC-Q200, SMD, 0805, 4.7µF, 25V, 10%, X7R, ROHS	TDK	CGA4J1X7R1E475K125AC
8	C106, C107, C108, C109, C110, C111, C112, C113	CAP, SMD, 0402, 47pF, 50V, 10%, C0G/NP0, ROHS	AVX	04025A470KAT2A
14	C5, C8, C14, C39, C56, C59, C60, C62, C66, C71, C81, C91, C114, C350	CAP, SMD, 0603, 10µF, 16V, 20%, X5R, ROHS	Murata	GRM188R61C106MA73D
5	C3, C9, C37, C61, C69	CAP-AEC-Q200, SMD, 0805, 22µF, 25V, 20%, X5R, ROHS	Murata	GRT21BR61E226ME13L
8	C47-C54	CAP, SMD, 0402, 0.1µF, 16V, 10%, X7R, ROHS	Venkel	C0402X7R160-104KNE
3	C55, C63, C120	CAP, SMD, 0603, 1000pF, 50V, 10%, X7R, ROHS	AVX	06035C102KAT2A
10	C7, C17, C19, C28, C31, C35, C58, C79, C80, C300	CAP, SMD, 0603, 0.01µF, 50V, 10%, X7R, ROHS	AVX	06035C103KAT2A
2	C1, C2	CAP, SMD, 0805, 47µF, 10V, 20%, X5R, ROHS	TDK	C2012X5R1A476M125AC
6	C20, C22, C25, C27, C302, C303	CAP, TANT, SMD, B, 10µF, 16V, 10%, ROHS	Venkel	TA016TCR106KBR
1	C82	CAP, SMD, 0603, 1.0µF, 25V, 10%, X7R, ROHS	Taiyo Yuden	TMK107B7105KA-T
2	C36, C38	CAP, SMD, 1206, 10µF, 25V, 10%, X7R, ROHS	Taiyo Yuden	TMK316B7106KL-TD
9	1P8V_EXT, AVCC_EXT, DIG_IO_EXT, DVCC_EXT, GND1, GND2, GND3, GND4, VREF_CM	CONN-GEN, TURRET, SILVER, 0.082 LENGTH, 0.076 MOUNT HOLE	Cambion	160-2043-02-01-00
2	J1, J2	CONN-BNC, RECEPTACLE, TH, 4 POST, 50Ω, SILVERCONTACT, ROHS	Amphenol	31-5329-51RFX
3	TP_OFFSET, TP_OFFSET2, TP_OFFSET_IN	CONN-MINI TEST PT, VERTICAL, RED, ROHS	Keystone	5000
2	GND12, GND13	CONN-MINI TEST PT, VERTICAL, BLK, ROHS	Keystone	5001
1	J5	CONN-PLUG, BANA-INSUL-SDRLESS, BLACK, 4mm, RA	Deltron	571-0100

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	J6	CONN-PLUG, BANA-INSUL-SDRLESS, GREEN, 4mm, ROHS, RA	Deltron	571-0400
1	J4	CONN-PLUG, BANA-INSUL-SDRLESS, RED, 4mm, RA	Deltron	571-0500
1	J26	CONN-HEADER, 2×20, BRKAWY-2×36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
1	J18	CONN-HEADER, 2×5, BRKAWY-2×36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
1	J21	CONN-HEADER, 2×6, BRKAWY-2×36, 2.54mm, ROHS	BERG/FCI	67996-272HLF
4	J7, J11, J23, J25	CONN-HEADER, 1×3, BREAKAWY 1×36, 2.54mm, ROHS	BERG/FCI	68000-236HLF
3	J40, J41, J42	CONN-HEADER, 1×32, BRKAWY-1×36, 2.54mm, ROHS	FCI/BERG	68000-236HLF
8	J43.J44, J45, J46, J47, J48, J49, J50	CONN-HEADER, 1×2, RETENTIVE, 2.54mm, 0.230×0.120, ROHS	BERG/FCI	69190-202HLF
1	J19	CONN-SOCKET ARRAY, SMD, 400P, 0.05 PITCH, CUSTOM, ROHS	Samtec	ASP-134602-01
1	U39	IC-ADC, 8-CHANNEL DIFFERENTIAL W/PGA 48P, TQFP, ROHS	Renesas	ISL71148M30NZ
1	U25	IC-128KBIT, I2C SERIAL EEPROM, 1.7-5.5V, 8P, TDFN, ROHS	Microchip Technology	24FC128T-I/MNY
1	U26	IC-BUFFER/LINE DRIVER, NON-INVERT, OPEN DRAIN, 6P, TSSOP, ROHS	NXP Semiconductor	74LVC2G07GW,125
4	U7, U8, U9, U38	IC-OP AMP, HI SPEED, LOW NOISE, 8P, SOIC, ROHS	Analog Devices	ADA4899-1YRDZ
1	U13	IC-2.5V, 3.3V CPLD, 100P, TQFP, ROHS	Altera	EPM240T100C5N
1	U36	IC-PREC.VOLTAGE REFERENCE, 8P, SOIC, 1.25VOUT, ROHS	Renesas	ISL21090BFB812Z-TK
1	U21	IC-PREC.VOLTAGE REFERENCE, 8P, SOIC, 2.5VOUT, ROHS	Renesas	ISL21090BFB825Z-TK
1	U22	IC-5V PREC.VOLTAGE REFERENCE, 8P, SOIC, ROHS	Renesas	ISL21090BFB850Z
1	U41	IC-LOW VOLTAGE DCP, 10LD MSOP, ROHS	Renesas	ISL23315WFUZ
4	U1, U3, U17, U23	IC-40V, 150mA LDO REGULATOR, 8P, EPSOIC, ROHS	Renesas	ISL80410IBEZ

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
4	U2, U15, U16, U28	IC-Single 500mA, Adj V_{OUT} LDO, 3x3, 8ld, DFN, Pb-Free W/ANNEAL	Renesas	ISL80505IRAJZ
1	U29	IC-2.92V VOLTAGE SUPERVISOR, SMD, 3P, SOT-23, ROHS	Renesas	ISL88002IH29Z
1	U11	IC-500mA, -2.3V, ADJ. VOLTAGE REGULATOR, 12P, MSOP, ROHS	Linear Tech/Analog Devices	LT3094EMSE#PBF
1	U5	IC-INVERTER, SINGLE CIRCUIT/INPUT, SMD, 5P, SC70-5, ROHS	On Semiconductor	NC7S04P5X
4	U6, U19, U20, U31	IC-INVERTER, SINGLE CIRCUIT/INPUT, SMD, 5P, SC70-5, ROHS	On Semiconductor	NC7SVU04P5X
1	U10	IC-BUS SWITCH, SPST, SMD, 5P, SC70-5, ROHS	On Semiconductor	NC7SZ66P5X
1	U12	IC-FLIP FLOP, 1 ELEMENT D-TYPE, 8P, VFSOP, ROHS	On Semiconductor	NL17SZ74USG
1	RP0	POT-TRIM, TH, 3P, 10kΩ, 1/2W, 10%, 25TURN, TOPADJ, ROHS	Bourns	3296W-1-103LF
6	R15, R17, R19, R27, R303, R304, R53, R77, R95, R307, R491	RES-AEC-Q200, SMD, 0603, 100Ω, 1/10W, 0.1%, THINFILM, ROHS	Panasonic	ERA-3AEB101V
3	R62-R64	RES, SMD, 0402, 1K, 1/16W, 1%, TF, ROHS	Venkel	CR0402-16W-1001FT
3	R68, R69, R79	RES, SMD, 0402, 4.7K, 1/16W, 1%, TF, ROHS	Venkel	CR0402-16W-4701FT
8	R45, R49, R51, R55, R56, R59, R73, R90	RES, SMD, 0603, 33Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-33R0FT
35	R9, R18, R21, R44, R46, R48, R52, R54, R57, R65, R66, R67, R78, R83, R85, R91, R95, R121, R288-R298, R302, R305, R390, R391, R392, R393	RES, SMD, 0603, 0Ω, 1/10W, TF, ROHS	Venkel	CR0603-10W-000T
5	R24, R38, R39, R60, R70	RES, SMD, 0603, 1K, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1001V
1	R61	RES, SMD, 0603, 10K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-1002FT
2	R12, R35	RES, SMD, 0603, 1.02K, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-071K02L
2	R11, R34	RES, SMD, 0603, 1.43K, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1431V
4	R2, R6, R28, R31	RES, SMD, 0603, 16.2K, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF1622V
2	R300, R301	RES, SMD, 0603, 169Ω, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-07169RL

Qty	Reference Designator	Description	Manufacturer	Manufacturer Part
1	R20	RES, SMD, 0603, 200Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-2000FT
1	R3	RES, SMD, 0603, 2.21K, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-072K21L
2	R16, R25	RES, SMD, 0603, 24.9Ω, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF24R9V
2	R22, R306	RES, SMD, 0603, 49.9Ω, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-49R9FT
1	R30	RES, SMD, 0603, 3.16K, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF3161V
1	R29	RES, SMD, 0603, 45.3K, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-0745K3L
1	R5	RES, SMD, 0603, 4.64K, 1/10W, 1%, TF, ROHS	Yageo	9C06031A4641FKHFT
1	R23	RES, SMD, 0603, 5.23K, 1/10W, 1%, TF, ROHS	Panasonic	ERJ-3EKF5231V
4	R4, R13, R14, R50	RES, SMD, 0603, 5.76K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-5761FT
1	R10	RES, SMD, 0603, 634Ω, 1/10W, 1%, TF, ROHS	Yageo	RC0603FR-07634RL
1	R1	RES, SMD, 0603, 9.53K, 1/10W, 1%, TF, ROHS	Venkel	CR0603-10W-9531FT
1	R37	RES, SMD, 1206, 49.9Ω, 1/4W, 1%, TF, ROHS	Vishay/dale	CRCW120649R9FKEA
1	R47	RES, SMD, 1210, 49.9Ω, 1/4W, 1%, TF, ROHS	Venkel	CR1210-4W-49R9FT
1	R26	RES, SMD, 0805, 500Ω, 1/10W, 0.1%, 25ppm, THINFILM, ROHS	KOA	RN732ATTD5000B25
2	RP1, RP2	RES, SMD, 0603, 5K, 1/10W, 0.1%, THINFILM, ROHS	Yageo	RT0603BRE075KL
4	Four corners	SCREW, 4-40×1/4in, PHILLIPS, PANHEAD, STAINLESS, ROHS	Building Fasteners	PMSSS 440 0025 PH

2.4 Evaluation Board Layout

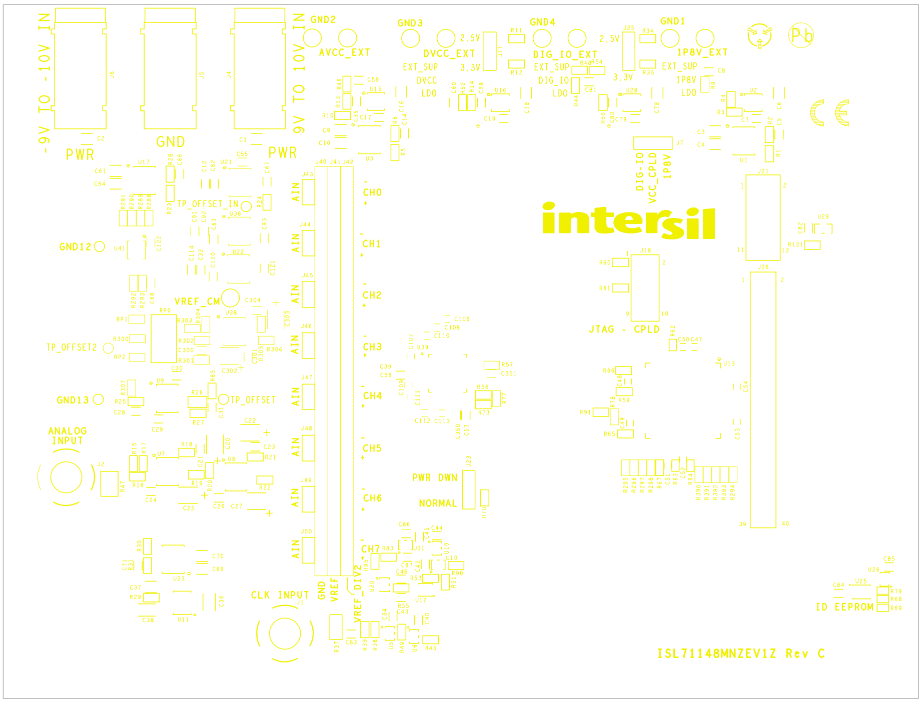

Figure 31. Top Silkscreen

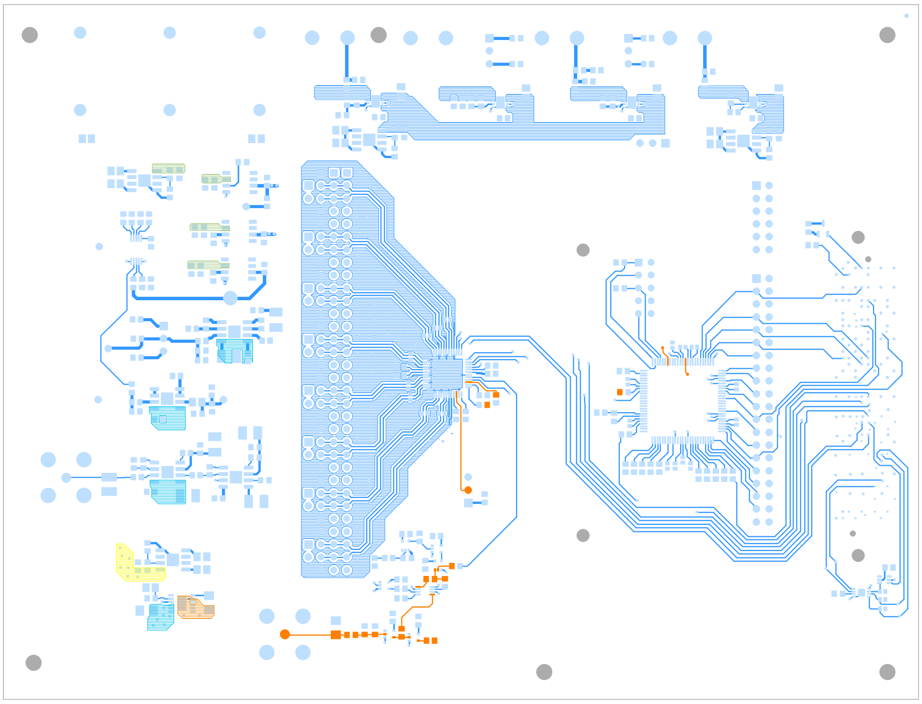

Figure 32. Top Layer

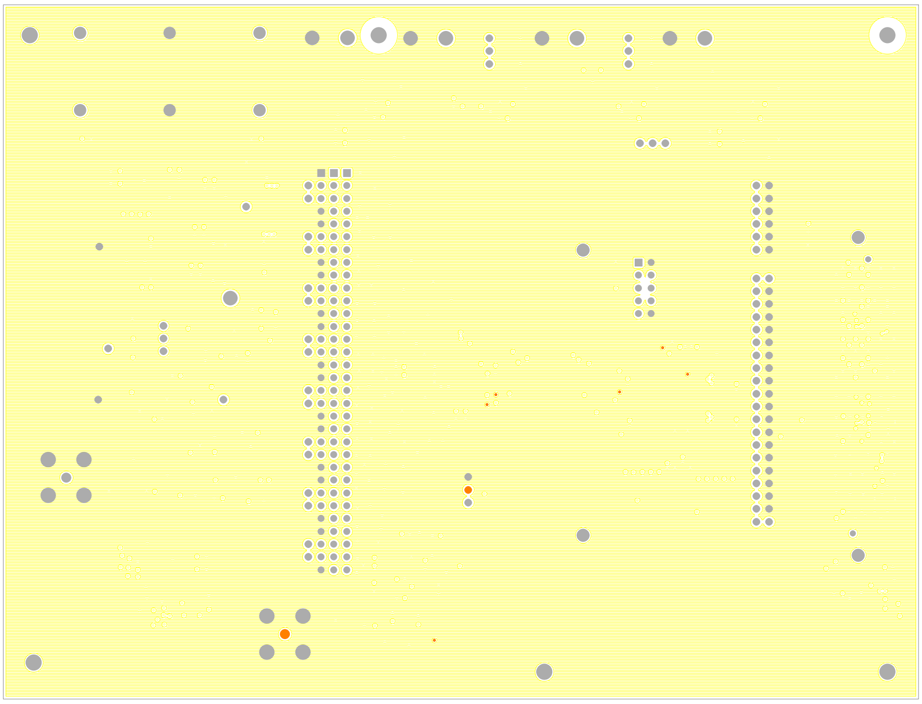

Figure 33. Layer 2

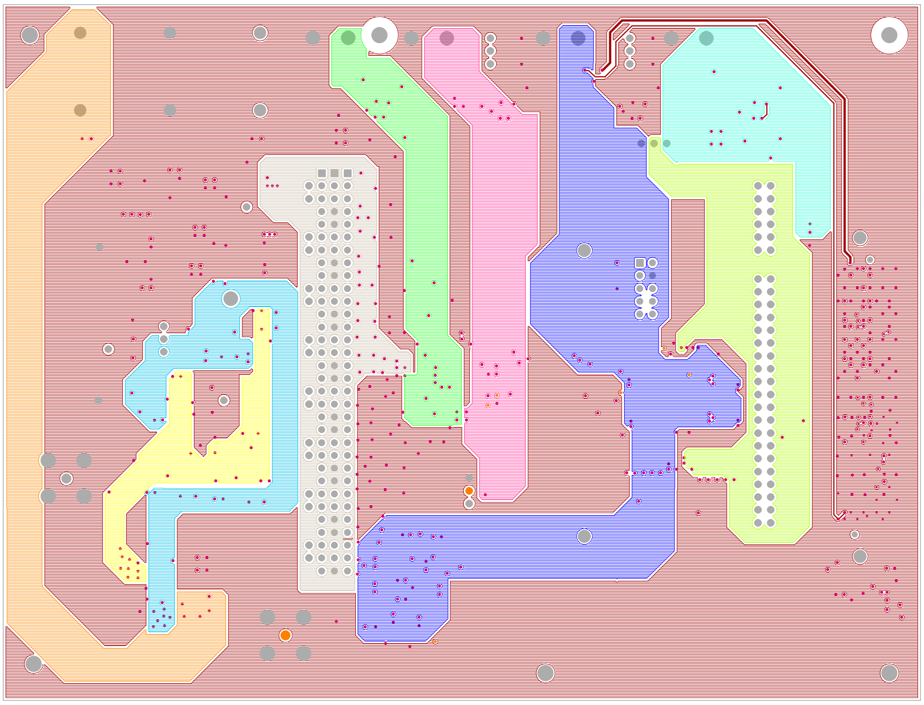

Figure 34. Layer 3

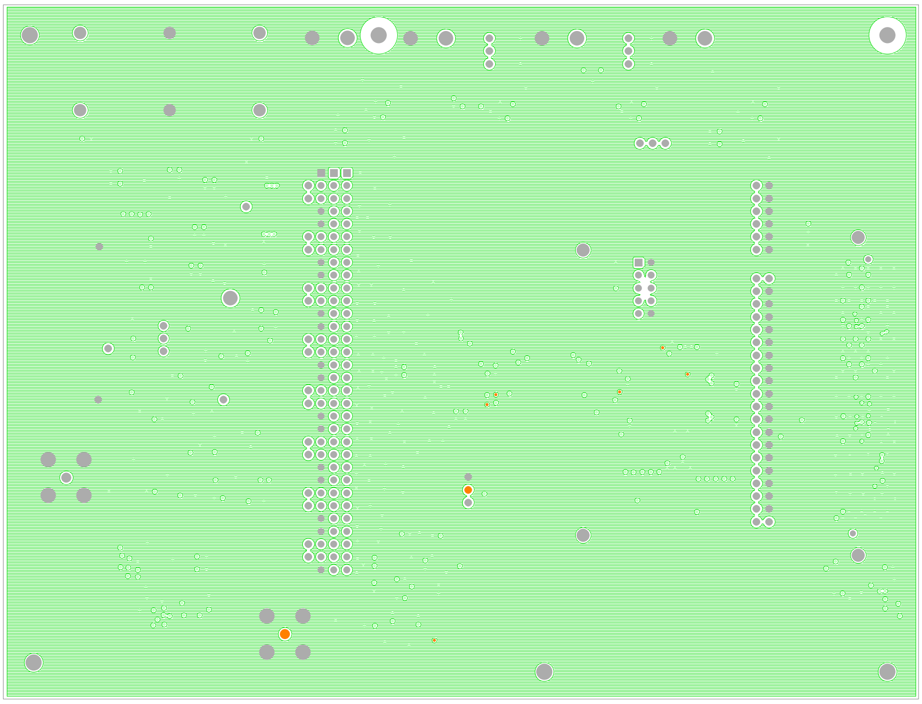

Figure 35. Layer 4

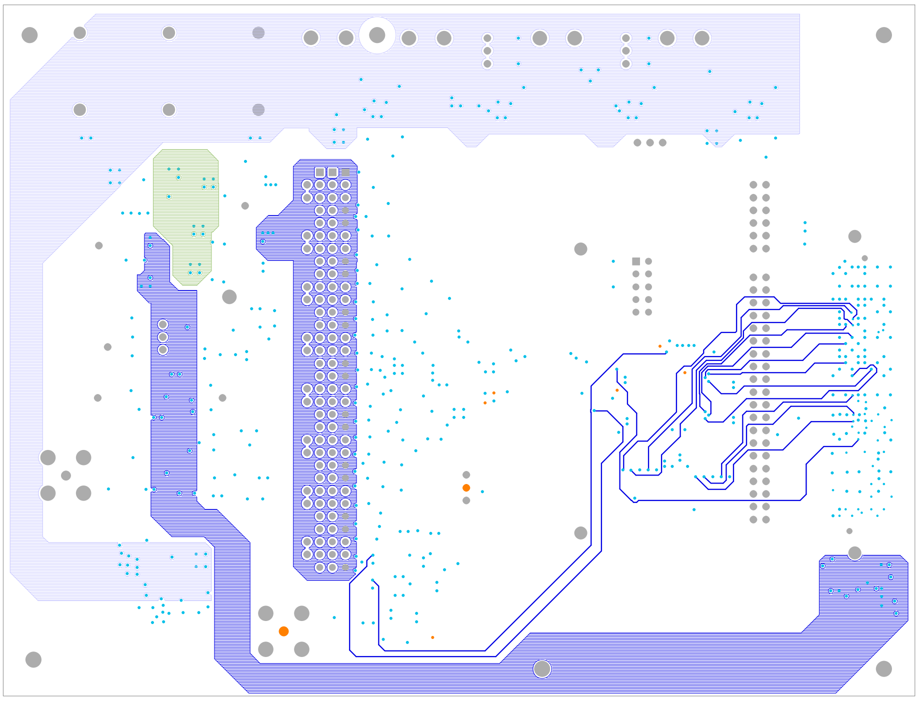

Figure 36. Layer 5

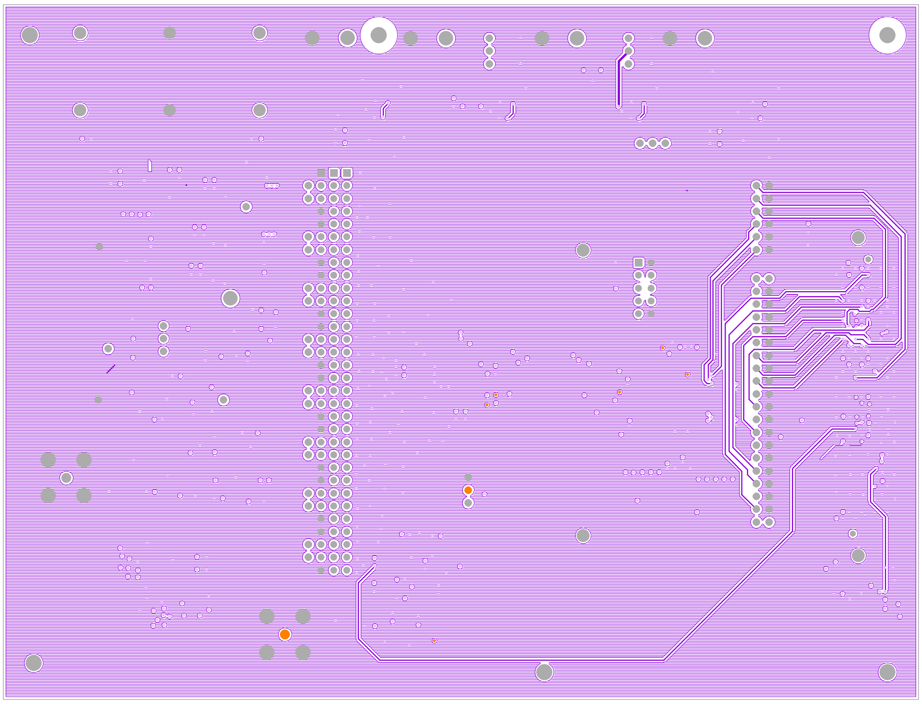

Figure 37. Layer 6

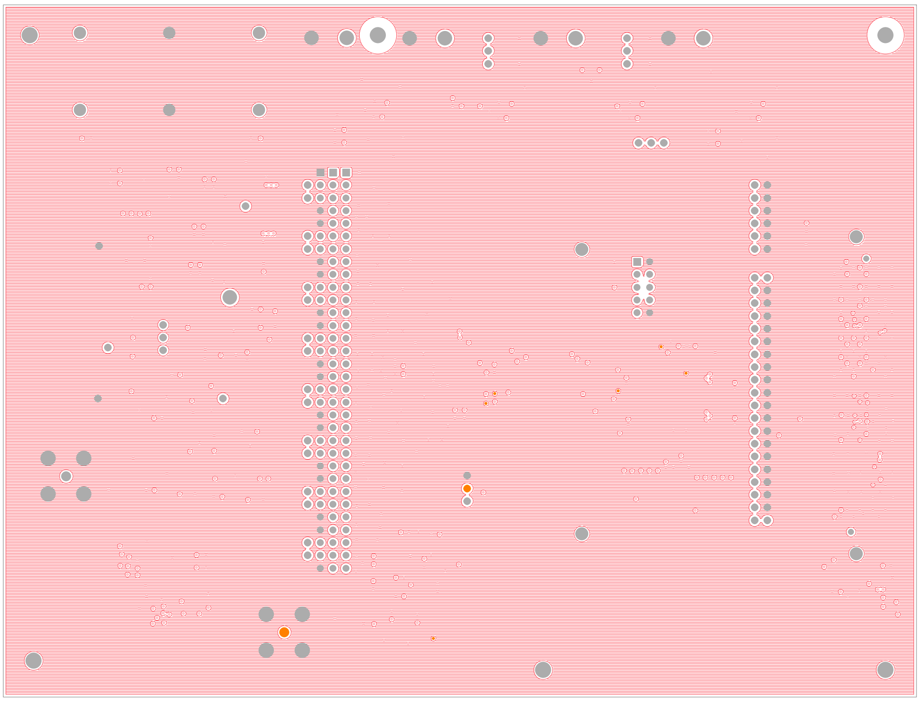

Figure 38. Layer 7

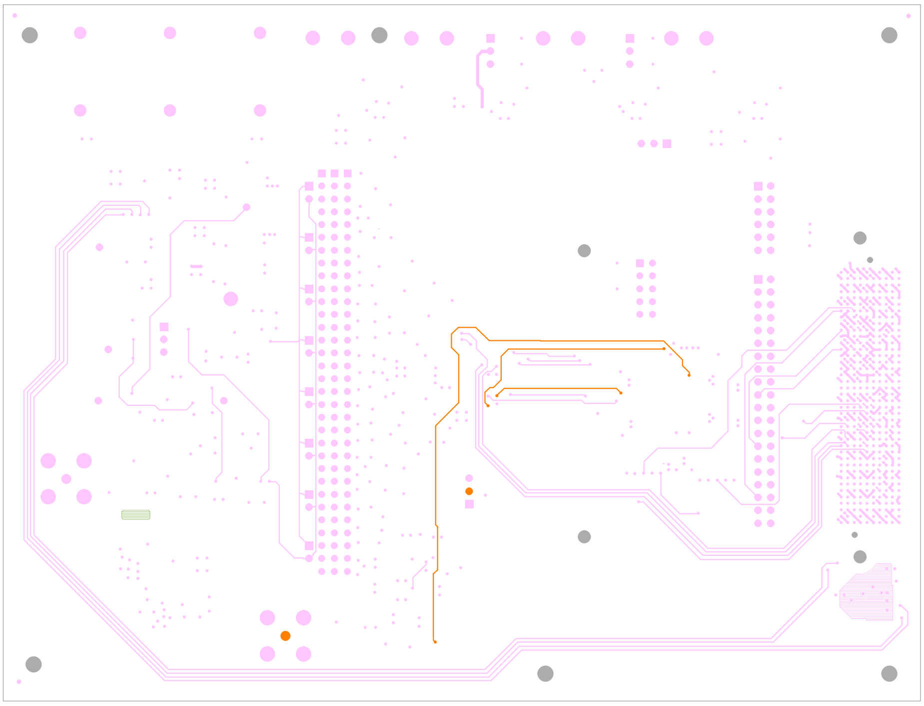

Figure 39. Bottom Layer

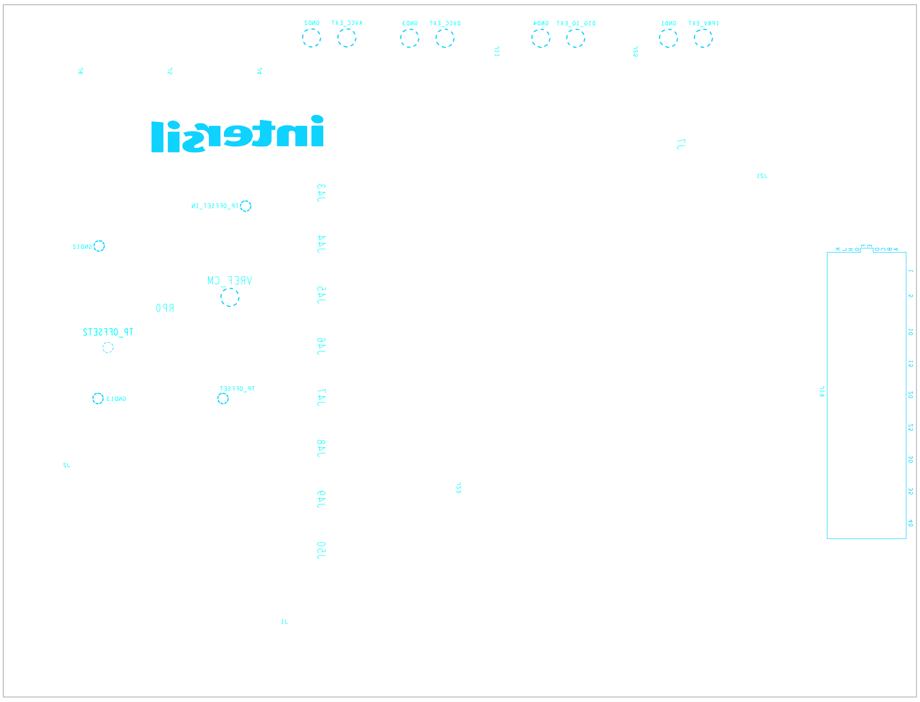

Figure 40. Bottom Silkscreen

3. Ordering Information

Part Number	Description
ISL71148MNZEV1Z	ISL71148M 14-Bit 900ksps SAR ADC evaluation board

4. Revision History

Revision	Date	Description
1.02	Jun 18, 2024	Added the Required Equipment section.
1.01	Feb 7, 2024	Updated the BOM.
1.00	Jan 18, 2024	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

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