ISL73006SLHDEMO2Z

The ISL73006SLHDEMO2Z demonstration board (Figure 3) features the ISL73006SLH buck regulator. This IC is a small footprint radiation hardened POL designed for critical low-power applications.

The ISL73006SLH is operational over 3V to 18V, integrating high-side and low-side power FETs and switches at a default 500kHz frequency. The ISL73006SLH uses constant-frequency peak current mode control architecture for fast loop transient response. The ISL73006SLH can use its internal compensation or an external Type II compensation to stabilize the loop as determined by specific design and performance requirements.

By integrating both P-channel and N-channel power devices and with the option of internal compensation, a minimum of external components are required, thereby reducing the BOM count and complexity of the design.

The ISL73006SLHDEMO2Z demonstration board and this accompanying manual provide a quick and easy method to evaluate the ISL73006SLH in the external compensation and slope configuration.

See the *ISL73006SLH datasheet* for information about the operation, function, and performance of the device.

Features

- Optimized for 12V to 3.3V conversion using the external slope and compensation configuration
- 1A output current

Specifications

The ISL73006SLHDEMO2Z demonstration board is set up with the external control loop compensation and slope configuration.

The board allows for other conditions to be evaluated with user modification of components and connections.

Table 1 shows the electrical ratings of the ISL73006SLHDEMO2Z demonstration board.

Table 1. Electrical Ratings

Parameter	Rating
PVIN Supply Voltage	6V - 18V
DC Output Voltage	3.3V
Operating Frequency	500kHz
Output Current	1A
Temperature	-55°C to +125°C

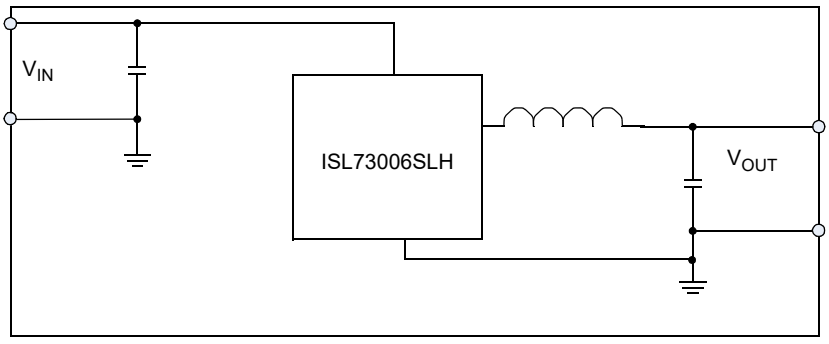

Figure 1. Block Diagram

Contents

1. Functional Description

The ISL73006SLHDEMO2Z demonstration board is configured by default for external control loop and slope and optimized for 12V to 3.3V conversion with a 1A maximum output current. It contains the ISL73006SLH voltage regulator IC. Figure 1 shows the ISL73006SLHDEMO2Z demonstration board block diagram. Figure 3 and Figure 4 show the ISL73006SLHDEMO2Z board images.

The ISL73006SLHDEMO2Z demonstration board provides access to the bias pins of the IC device and convenient pads for connecting test equipment. For more information, see the schematic (Figure 5), PCB layers (Figure 6 through Figure 11), and Bill of Materials. Figure 12 through Figure 17 show the performance data using the ISL73006SLHDEMO2Z and basic lab equipment.

1.1 Operational Characteristics

The ISL73006SLHDEMO2Z only requires a single voltage supply > 6V connected to the PVIN pad to operate, outputting 3.3V on the VOUT pad with a 1A output current capability. Configured for a nominal PVIN voltage of 12V, the input operating voltage at which the IC turns on is set by the resistor divider (R_1 and R_2) on the ENABLE pin. The operating ripple current was chosen to be approximately 1/3 of the 1A-rated, resulting in a 15µH inductor.

Note: Do not exceed 5V on the ENABLE pin.

1.2 Setup and Configuration

The following equipment is recommended for testing the board:

- 12V power supply
- 100MHz oscilloscope

Complete the following steps to configure and use the board:

1. Configure the board as shown in Figure 2.
2. Connect and turn on a 12V power supply to the PVIN pad.
3. Use the oscilloscope to look at VIN and VOUT waveforms and observe the behavior of the LX phase node located on pin 10 of the IC package. Proper probe grounding must be practiced when observing switching waveforms.
4. Output current loading can be externally added at the VOUT and GND pads for loaded output evaluations. A DVM(s) can monitor the input and output voltages and currents.

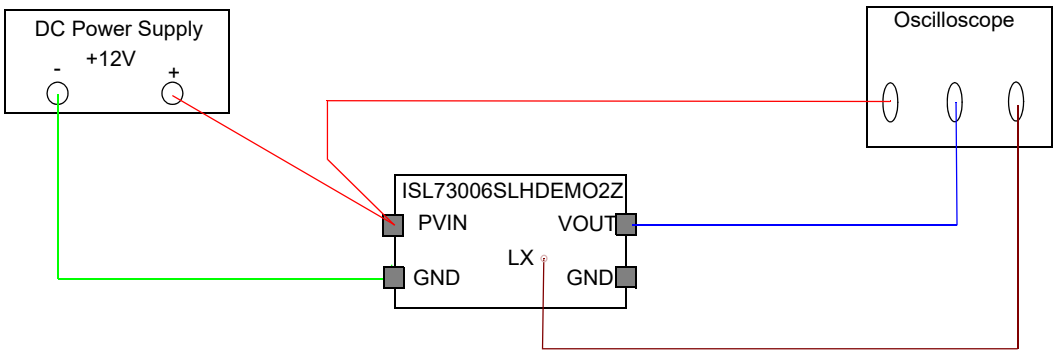

Figure 2. ISL73006SLH Basic Evaluation Test Setup Block Diagram

2. Board Design

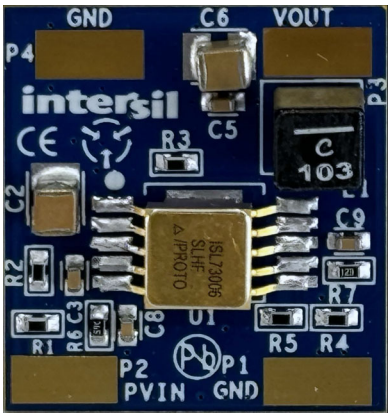

Figure 3. Evaluation Board (Top)

Figure 4. Evaluation Board (Bottom)

2.1 Basic Layout

The ISL73006SLH is located in the lower center of the board and is labeled U1. Connect the input power across the PVIN and GND jacks. The output voltage appears across the VOUT and GND jacks. C_{IN} is provided by C_1 and C_2. The output LC filter is comprised of the $L_{OUT,}$ L_1, and C_{OUT} is provided by C_6 and $C_{7.}$ The EN threshold to enable the IC when PVIN is ~6V and is set by R_1 and R_2. Consult the schematic in (Figure 5) for details.

2.2 Layout Guidelines

PCB design is critical to reducing parasitic inductances, with critical components being closely placed to the IC. The critical components are the loop compensation RC network and the low ESR ceramic input capacitors. Avoid placing traces or components under the LX shapes to avoid noise coupling from the switching node. Ensure that the SGND pin is not part of the PGND plane but is attached by a single point to reduce noise on the SGND pin.

2.3 Schematic Diagrams

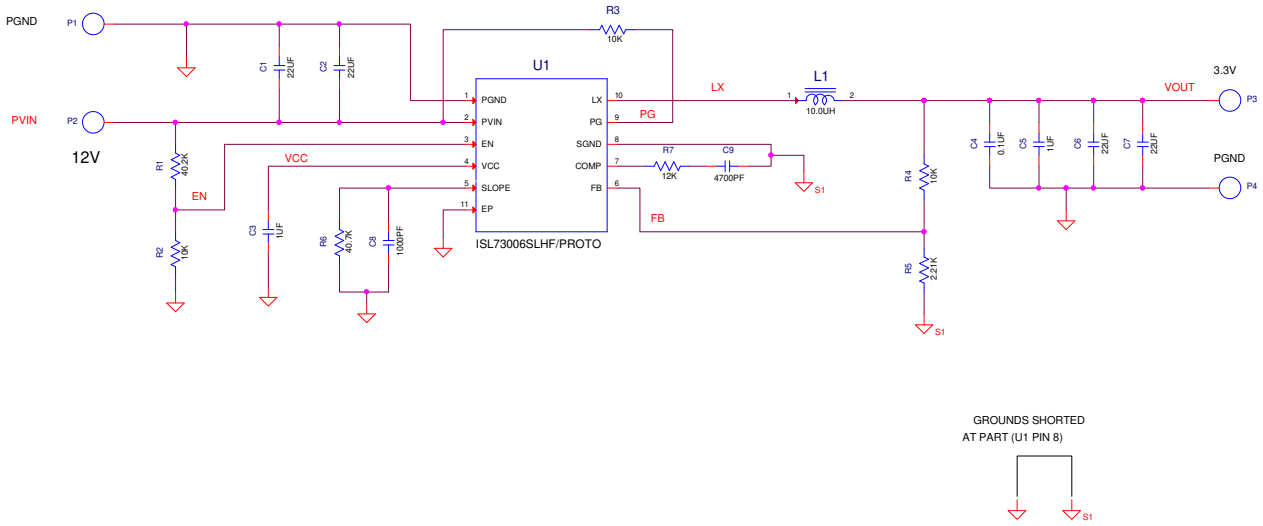

Figure 5. Schematic

2.4 Bill of Materials

Reference Designator	Description	Manufacturer	Manufacturer Part
U1	IC-RAD HARD 1A POL REGULATOR	Renesas Electronics	ISL73006SLHF/PROTO
L1	COIL-PWR INDUCT, SMD, 5.4x5.2mm, 15µH.20%, 3.7A, 76.6mΩ, ROHS	Coilcraft	XAL5050-153ME
C1, C2, C6, C7	22µF, Multilayer Cap	Various	Generic
C3, C5	1µF, Multilayer Cap	Various	Generic
C4	0.1µF, Multilayer Cap	Various	Generic
C8	1000pF, Multilayer Cap	Various	Generic
C9	4700pF, Multilayer Cap	Various	Generic
R1	40.2kΩ, Thick Film Chip Resistor	Various	Generic
R2, R3, R4	10kΩ, Thick Film Chip Resistor	Various	Generic
R5	2.21kΩ, Thick Film Chip Resistor	Various	Generic
R6	40.7kΩ, Thick Film Chip Resistor	Various	Generic
R7	12kΩ, Thick Film Chip Resistor	Various	Generic

2.5 Board Layout

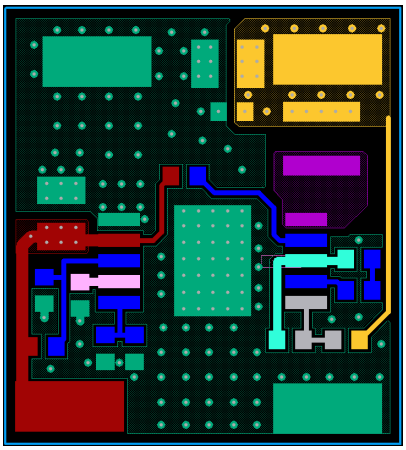

Figure 6. Top Layer

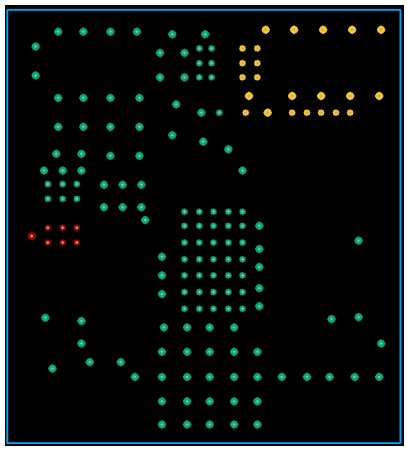

Figure 7. Layer 2

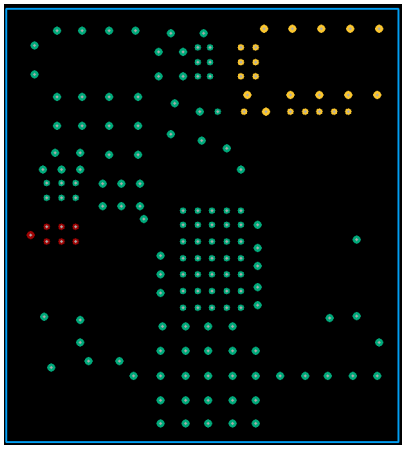

Figure 8. Layer 3

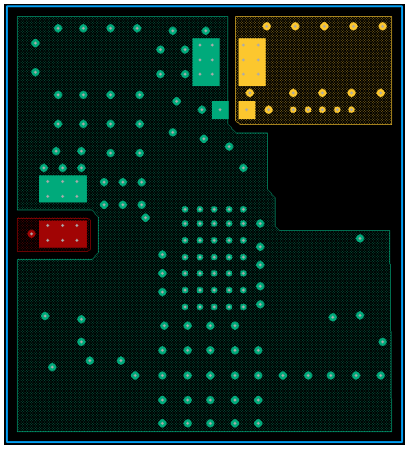

Figure 9. Bottom Layer

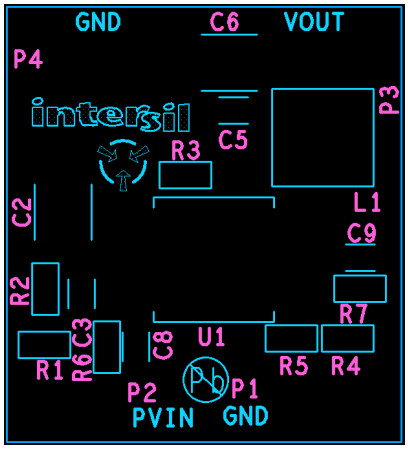

Figure 10. Top Silk Layer

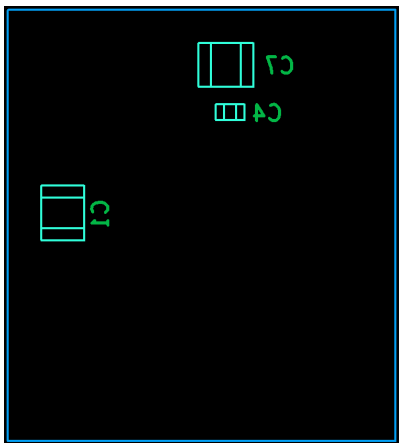

Figure 11. Bottom Assembly Layer

3. Typical Performance Graphs

Unless otherwise noted, PVIN = 12V; V_{OUT} = 3.3V, T_A = Room Ambient, circuit modifications necessary

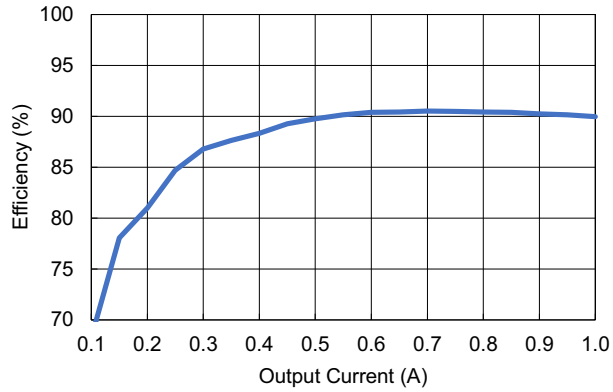

Figure 12. Efficiency vs Output Current

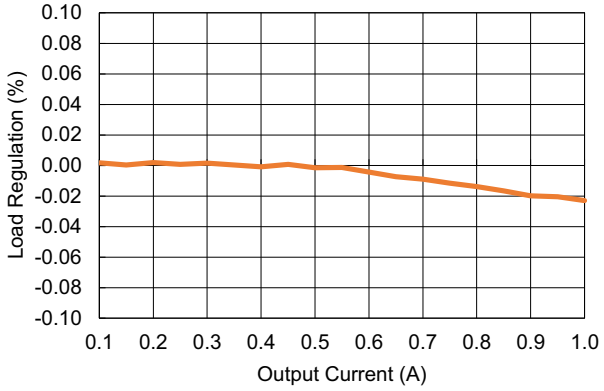

Figure 13. Load Regulation vs Output Current

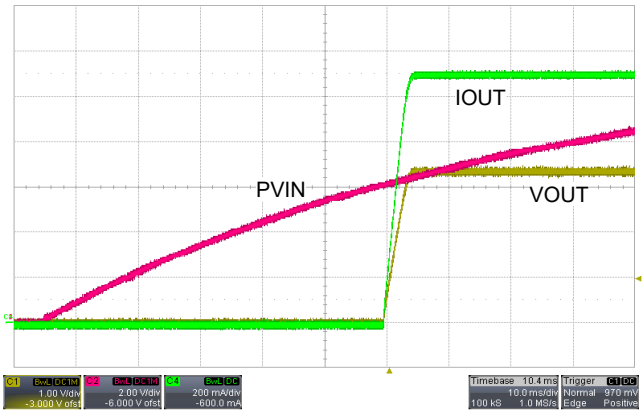

Figure 14. Turn-On by PVIN, 3Ω Load

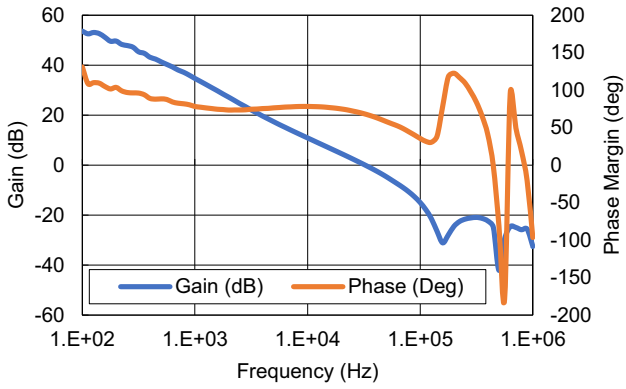

Figure 15. Gain/Phase Bode Plot, I_{OUT} = 0.65A

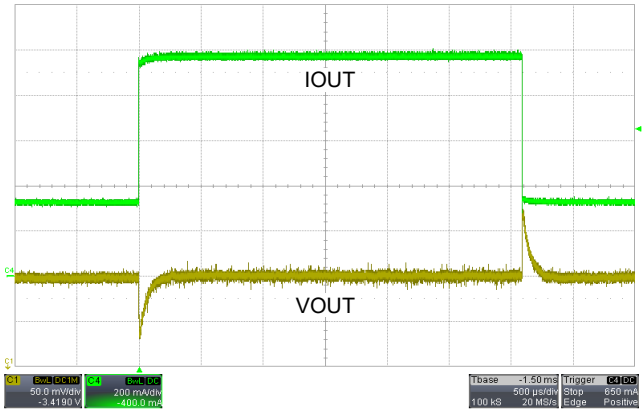

Figure 16. 0.65A Load Transient

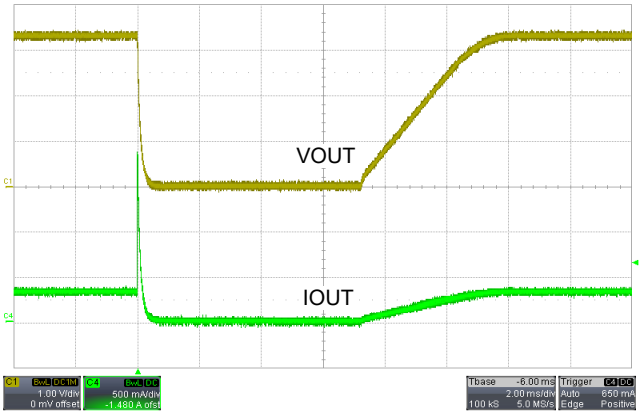

Figure 17. Positive Overcurrent Protection and Restart

4. Ordering Information

Part Number	Description
ISL73006SLHDEMO2Z	Radiation Hardened ISL73006SLH Buck Regulator Mini Demonstration Board configured with externally set loop and slope compensation, set up for wide VIN of 8V to 16V to 3.3VOUT

5. Revision History

Revision	Date	Description
1.00	Jan 9, 2024	Initial release

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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