

## ISL9107EVAL1Z, ISL9108EVAL1Z

Evaluation Board Application Manual

AN1399  
Rev 0.00  
July 29, 2008

### Description

The ISL9107EVAL1Z and ISL9108EVAL1Z provide the complete evaluation kit for the ISL9107 and ISL9108, which are 1.6MHz switching frequency, low quiescent current, high efficiency integrated step-down regulators. They are capable of delivering up to 1.5A output current with an output voltage range from 0.8V to  $\sim V_{IN}$ . The output voltage is set by two voltage divider resistors of  $R_2$  and  $R_3$  on the board. The default output voltage is set to be 1.6V on the evaluation board. In addition to ISL9108, ISL9107 offers a typical 215ms Power-Good (PG) timer when powered up. This timer output can be reset by RSI.

The complete ISL9107, ISL9108 regulator is located at the center of the board. On the left side of the board are the connectors for the input power source ( $V_{IN}$  and GND). The output connectors are located on the right side ( $V_O$  and GND). The other two test points are for the PG and RSI signals respectively (for ISL9107 only), as labelled on the board. The RSI input needs either be driven to a low or a high logic input (Please refer to the ISL9107, ISL9108 datasheet, FN6612, for more details regarding the RSI function). On the board, the open-drain PG signal is pulled up to the  $V_{IN}$  through a 100k $\Omega$  resistor ( $R_1$ ). Jumper JP1 allows the user to enable or disable the IC. Jumper JP2 is the mode selection input. **Do not leave the EN and the MODE signal floating.** The evaluation board also offers one oscilloscope probe tip connector connected to SW pin to minimize the switching noise during the evaluation. The evaluation board schematic, layout and bill-of-materials (BOM) can be found at the end of this application note.

### Ordering Information

- ISL9107EVAL1Z - Evaluation Board for ISL9107
- ISL9108EVAL1Z - Evaluation Board for ISL9108

### Features

- A Complete Evaluation Platform for ISL9107 and ISL9108
- Convenient Jumpers for Enable/Disable, Operation Mode Selection
- Integrated Synchronous Buck Regulator with High Efficiency
- 2.7V to 5.5V Supply Voltage
- 1.5A Output Current
- 17 $\mu$ A Quiescent Current in Skip (Low  $I_Q$ ) Mode

### Specifications

Table 1 below shows the recommended operating conditions for using ISL9107EVAL1Z, ISL9108EVAL1Z.

TABLE 1. RECOMMENDED OPERATING CONDITIONS

PARAMETER	MIN	TYP	MAX	UNIT
Input Voltage	2.7	-	5.5	V
Output Voltage (Note)	-	1.6	-	V
Maximum Output Current	1.5	-	-	A

NOTE: The output voltage can be set to other values by changing the  $R_2$ ,  $R_3$  values,  $V_{OUT} = 0.8V \cdot (1 + R_2/R_3)$ . Refer to ISL9107, ISL9108 datasheet for some recommended  $R_2$ ,  $R_3$  and  $C_3$  values for different output voltages.

### Recommended Equipment

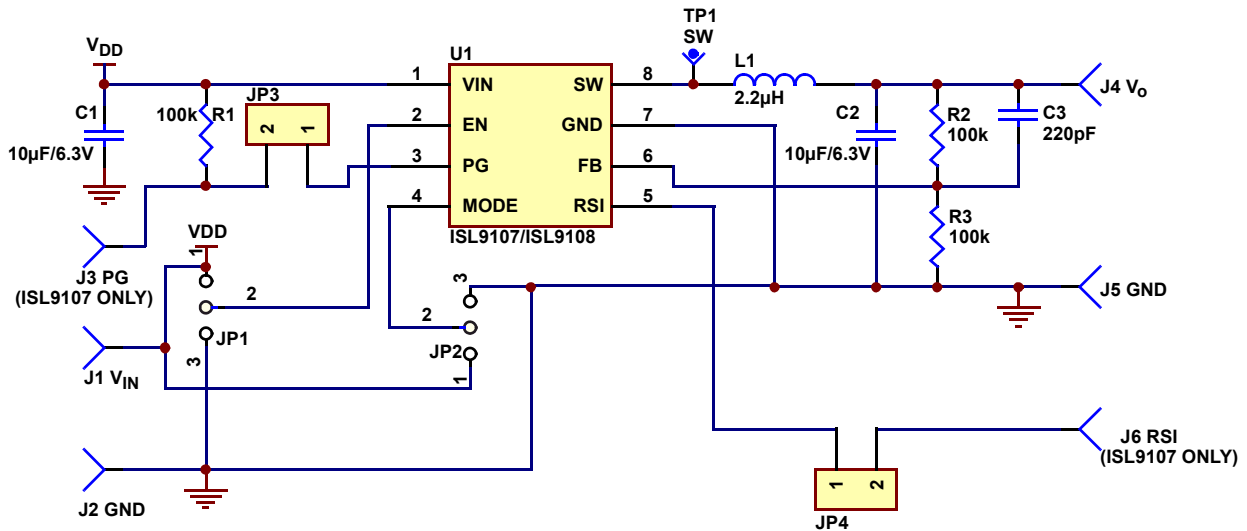
The following instruments are recommended for testing:

- DC Power Supply, 5V/3A
- Electronic loads capable of sinking current up to 4A
- Multimeters
- Function generator
- Oscilloscope

### Evaluation Board Setup

The following are recommended steps for setting up the ISL9107EVAL1Z and ISL9108EVAL1Z evaluation boards:

1. Connect Jumper JP1 at the position of "Enable" to enable the device. Connect JP1 at the position of "Disable" to disable the device.
2. Connect Jumper JP2 either at the position of "SKIP" or "PWM". With JP2 connected at the position of "SKIP", the device enters skip mode under light load condition; with JP2 connected at the position of "PWM", the device always operates under PWM mode regardless of the load condition.
3. For ISL9107EVAL1Z, connect the RSI input to either ground or  $V_{IN}$ . Please refer to the ISL9107, ISL9108 datasheet, FN6612, for more details regarding the function of RSI.
4. Connect DC power supply between  $V_{IN}$  and GND connectors on board. Make sure the power supply has enough supply current capability. The absolute maximum rating for  $V_{IN}$  pin is 6.5V and the recommended maximum input voltage applied on  $V_{IN}$  is up to 5.5V.
5. Connect the output to a load (resistor or electronic load).
6. Turn on the input power supply and start the evaluation.



J3, J6, JP3 AND JP4 ARE ONLY POPULATED FOR ISL9107EVAL1Z. FOR ISL9108EVAL1Z, THESE SHOULD BE UN-POPULATED ON THE BOARD.

FIGURE 1. ISL9107EVAL1Z, ISL9108EVAL1Z SCHEMATIC

**ISL9107EVAL1Z and ISL9108EVAL1Z Bill of Materials (BOM)**

ITEM	QTY	REFERENCE	PART DESCRIPTION	PCB FOOTPRINT	PART NUMBER	VENDOR
1	1	U1	ISL9107 for ISL9107EVAL1Z and ISL9108 for ISL9108EVAL1Z	8 Ld (2x3) DFN	ISL9107 or ISL9108	Intersil
2	1	C1	Capacitor, SMD, 10µF/6.3V, 10%, X5R	0805	GRM21BR60J106KE19L	Murata
3	1	C2	Capacitor, SMD, 10µF/6.3V, 10%, X5R	0805	GRM21BR60J106KE19L	Murata
4	1	C3	Capacitor, SMD, 220pF/50V, 10%, X7R	0603	GRM188R71H221KA01D	Murata
5	3	R1, R2, R3	Resistor, SMD, 100kΩ, 1%, 0.1W	0603	RC0603FR-07100KL	Yageo
6	1	L1	Inductor, 2.2µH	3.8x3.8	CDRH3D17/SNP-2R2	Sumida
7	6	VIN, VO, PG, RSI, GND (x2)	Turrent Terminal Pin. J3 (PG) and J6 (RSI) are only populated on ISL9107EVAL1Z.	-	3156-1-00-15-00-00-08-0	Mill-Max
8	1	TP1	Scope Probe Test Point	-	131503100	Tektronix
9	2	JP1, JP2	Connect Header, 1X3	-	68000-236-1X3	BERG/FCI
10	2	JP3, JP4	Connect Header, 1X2. Only populated for ISL9107EVAL1Z.	-	68000-236-1x2	BERG/FCI

**PCB Layout**

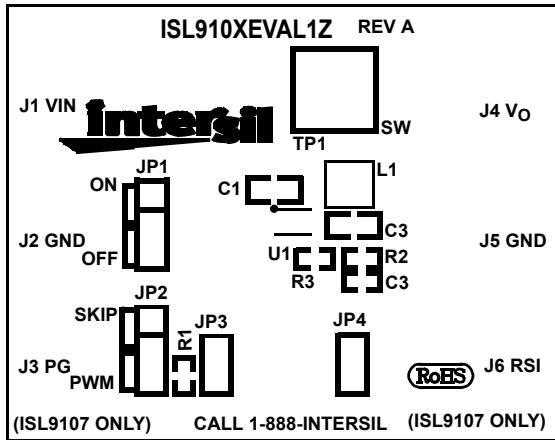


FIGURE 2. SILK LAYER

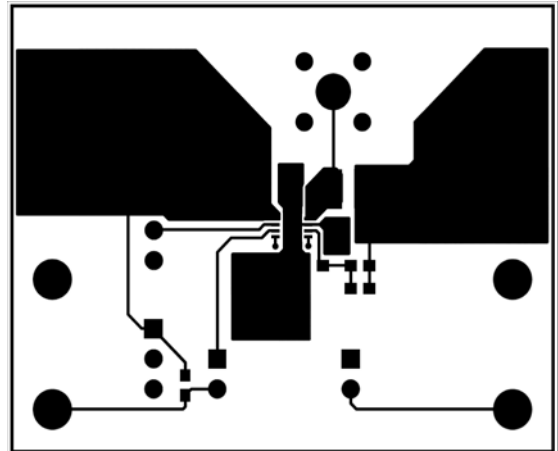


FIGURE 3. TOP LAYER

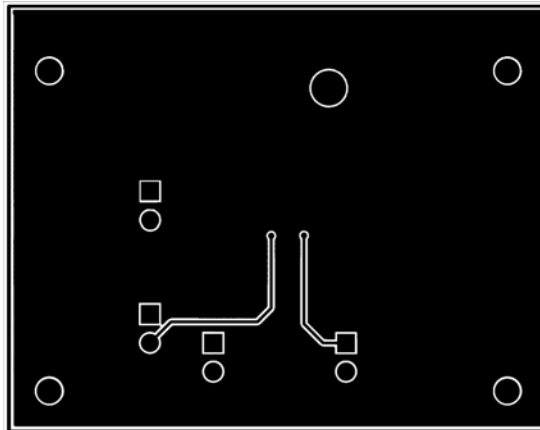


FIGURE 4. BOTTOM LAYER (Mirrored)

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(Rev.4.0-1 November 2017)



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