User's Manual

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RZ/N2L Group

Renesas Starter Kit+ for RZ/N2L

User's Manual

RZ/N Series for industrial Network
RZ Family
64-Bit & 32-Bit Arm®-Based High-End MPUs

Renesas Electronics
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General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Disclaimer

By using this Renesas Starter Kit (RSK+), the user accepts the following terms:

The RSK+ is not guaranteed to be error free, and the entire risk as to the results and performance of the RSK+ is assumed by the User. The RSK+ is provided by Renesas on an “as is” basis without warranty of any kind whether express or implied, including but not limited to the implied warranties of satisfactory quality, fitness for a particular purpose, title and non-infringement of intellectual property rights with regard to the RSK+. Renesas expressly disclaims all such warranties. Renesas or its affiliates shall in no event be liable for any loss of profit, loss of data, loss of contract, loss of business, damage to reputation or goodwill, any economic loss, any reprogramming or recall costs (whether the foregoing losses are direct or indirect) nor shall Renesas or its affiliates be liable for any other direct or indirect special, incidental or consequential damages arising out of or in relation to the use of this RSK+, even if Renesas or its affiliates have been advised of the possibility of such damages.

Precautions

The following precautions should be observed when operating any RSK+ product:

This Renesas Starter Kit is only intended for use in a laboratory environment under ambient temperature and humidity conditions. A safe separation distance should be used between this and any sensitive equipment. Its use outside the laboratory, classroom, study area or similar such area invalidates conformity with the protection requirements of the Electromagnetic Compatibility Directive and could lead to prosecution.

The product generates, uses, and can radiate radio frequency energy and may cause harmful interference to radio communications. However, there is no guarantee that interference will not occur in a particular installation. If this equipment causes harmful interference to radio or television reception, which can be determined by turning the equipment off or on, you are encouraged to try to correct the interference by one or more of the following measures;

ensure attached cables do not lie across the equipment
reorient the receiving antenna
increase the distance between the equipment and the receiver
connect the equipment into an outlet on a circuit different from that which the receiver is connected
power down the equipment when not in use
consult the dealer or an experienced radio/TV technician for help NOTE: It is recommended that wherever possible shielded interface cables are used.

The product is potentially susceptible to certain EMC phenomena. To mitigate against them it is recommended that the following measures be undertaken;

The user is advised that mobile phones should not be used within 10m of the product when in use.
The user is advised to take ESD precautions when handling the equipment.

The Renesas Starter Kit does not represent an ideal reference design for an end product and does not fulfil the regulatory standards for an end product.

How to Use This Manual

1. Purpose and Target Readers

This manual is designed to provide the user with an understanding of the CPU Board hardware functionality, and electrical characteristics. It is intended for users designing sample code on the CPU Board platform, using the many different incorporated peripheral devices.

The manual comprises of an overview of the capabilities of the RSK+ product but does not intend to be a guide to embedded programming or hardware design.

Particular attention should be paid to the precautionary notes when using the manual. These notes occur within the body of the text, at the end of each section, and in the Usage Notes section.

The revision history summarizes the locations of revisions and additions. It does not list all revisions. Refer to the text of the manual for details.

The following documents apply to the RSK+RZN2L. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

Document Type	Description	Document Title	Document No.
User's Manual	Describes the technical details of the RSK+ hardware.	Renesas Starter Kit + for RZ/N2L User's Manual	R20UT4984EG
Quick Start Guide	Provides simple instructions to setup the RSK+ and run the first sample.	Renesas Starter Kit + for RZ/N2L Quick Start Guide	R20UT4986EG
Hardware Manual	Provides technical details of the RZ/N2L microprocessor.	RZ/N2L Group Hardware Manual	R01UH0955EJ

2. List of Abbreviations and Acronyms

Abbreviation	Full Form
ADC	Analog-to-Digital Converter
bps	bits per second
CAN	Controller Area Network
CPU	Central Processing Unit
DIP	Dual In-line Package
DNF	Do Not Fit
EEPROM	Electronically Erasable Programmable Read Only Memory
ESC	EtherCAT Slave Controller
ESD	electrostatic discharge
EtherCAT	Ethernet for Control Automation Technology
GPT	General PWM Timer
I^2C (IIC)	Philips™ Inter-Integrated Circuit Connection Bus
J-Link®	SEGGER debug probe (Emulator)
J-Link® OB	SEGGER On-board debug probe (Emulator)
IRQ	Interrupt Request
LCD	Liquid Crystal Display
LED	Light Emitting Diode
MAC	Media Access Control
MCU	Micro controller Unit
MPU	Micro Processor Unit
MTU	Multi-Function Timer Pulse Unit
n/a (NA)	Not Applicable
n/c (NC)	Not Connected
NMI	Non-maskable Interrupt
PC	Personal Computer
PCB	Printed Circuit Board
POE	Port Output Enable
POEG	Port Output Enable for GPT
PWM	Pulse Width Modulation
RAM	Random Access Memory
RGMII	Reduced Gigabit Media-Independent Interface
RMII	Reduced Media-Independent Interface
ROM	Read Only Memory
RSK+	Renesas Starter Kit+
SCI	Serial Communications Interface
SHOST	Serial Host Interface
SPI	Serial Peripheral Interface
UART	Universal Asynchronous Receiver/Transmitter
USB	Universal Serial Bus

Table of Contents

1. Overview

1.1 Purpose

This RSK+ is an evaluation tool for Renesas microprocessors. This manual describes the technical details of the RSK+ hardware.

1.2 Features

This RSK+ provides an evaluation of the following features:

- Renesas microprocessor programming
- User code debugging
- User circuitry such as switches, LEDs and a potentiometer
- Sample applications

The RSK+ contains all the circuitry required for microprocessor operation.

1.3 Board specification

Board specification is shown in **Table 1-1** below.

Table 1-1: Board Specification

Item	Specification
Microprocessor	Part No: R9A07G084M04GBG
	Package: 225-pin FBGA
	On-Chip Memory: RAM 1.5MB
On-Board Memory	SDRAM: 256Mbit (Data width 16bit)
	NOR Flash: 256Mbit (Data width 16bit)
	Octa Flash: 512Mbit
	HyperRAM: 64Mbit
	QSPI Serial Flash: 512Mbit
	I^2C EEPROM: 32Kbit
Input Clock	RZ/N2L Main: 25MHz
	RL78/G1C Main: 12MHz
	Ethernet PHY (for RGMII): 25MHz
Power Supply	DC Power Jack: 5 V Input
	USB Type-C Connector: 5V Input
	Power Supply IC: 5V Input, 3.3V Output
	Power Supply IC: 5V Input, 1.8V Output
	Power Supply IC: 5V Input, 1.1V Output
	Power Supply IC: 5V Input, 1.0V Output (For Ethernet PHY)
	Power Supply IC: 5V Input, 2.5V Output (For Ethernet PHY)
Debug Interface	MIPI-10: 1.27mm pitch 10-pin header
	MIPI-20: 1.27mm pitch 20-pin header
	Mictor-38: 0.64mm pitch 38-pin header
	J-Link® OB: Micro-USB
DIP Switch	Mode Configuration: 8-pole x 1
	Signal Select: 10-pole x 2
	User: 4-pole x 1
Push Switch	Reset Switch x 1
	User Switch x 3
Potentiometer (for ADC)	Single-turn, 10kΩ
LED	3.3V Power Indicator: green x 1
	User: green x 1, yellow x 1, red x 2
	Ethernet Status: green x 3, yellow x 3
	Ether-CAT Status: green x 4, yellow green x 1, red x 3
	J-Link® OB Status: yellow x 1
Ethernet	Connector: RJ45 x 3
	PHY: Single Channel PHY x 3
CAN*2	Connector *1: 2.54mm pitch, 3-pin x 1
	CAN Driver x 1
USB	USB-Function: Mini-USB
	USB-Host: USB-Type A
RS485	Connector *1: 10-pin Connector
	RS485 Transceiver x 1
USB to Serial Converter Interface	Connector: Mini-USB
	Driver: RL78/G1C Microcontroller (Part No R5F10JBCAFP)
Pmod™	PMOD-2A, 6A: 12-pin Connector
	PMOD-3A: 12-pin Connector
mikroBUS™	2.54 mm pitch, 8-pin x 2 (J21, J22)
Grove®	2.00 mm pitch, 4-pin x 2 (J27, J28)
QWIIC®	1.00 mm pitch, 4-pin x 1 (J30)
Serial Host Interface	2.54mm pitch, 14-pin x 1 (CN4)
Pin Header	2.54 mm pitch, 20-pin x 2 (CN1, CN3)
Application Board Interface *1	2.54 mm pitch, 26-pin x 2 (JA1, JA2), 50-pin x 1 (JA3), 24-pin x 2 (JA5, JA6)

*1: This part is not mounted.
*2: The CAN on this board can transfer at up to 5Mbps.

2. Power Supply

2.1 Requirements

This board has a USB Type-C connector (CN5) and an optional centre positive supply connector using a 2.0mm barrel power jack (CN6). Supply power to the CPU board from either CN5 or CN6.
The main power supply connected to CN6 should supply a minimum of 15W to ensure full functionality.

This CPU board supports two external voltage input. Details of the external power supply connection are shown in **Table 2-1** below.

Table 2-1: Main Power Supply Requirements

Connector	Supply voltage
CN5	Type-C VBUS (5VDC)
CN6	Input 5VDC*

*: There are RSK+ products which require a 12V voltage input. Since this board requires a 5V voltage input, be careful not to connect the power supply of a high-voltage output accidentally. Moreover, the main power supply connected to CN6 should supply a minimum of 15W to ensure full functionality.

3. Board Layout

3.1 Component Layout

Figure 3-1 and **Figure 3-3** below shows the top component layout of the board.

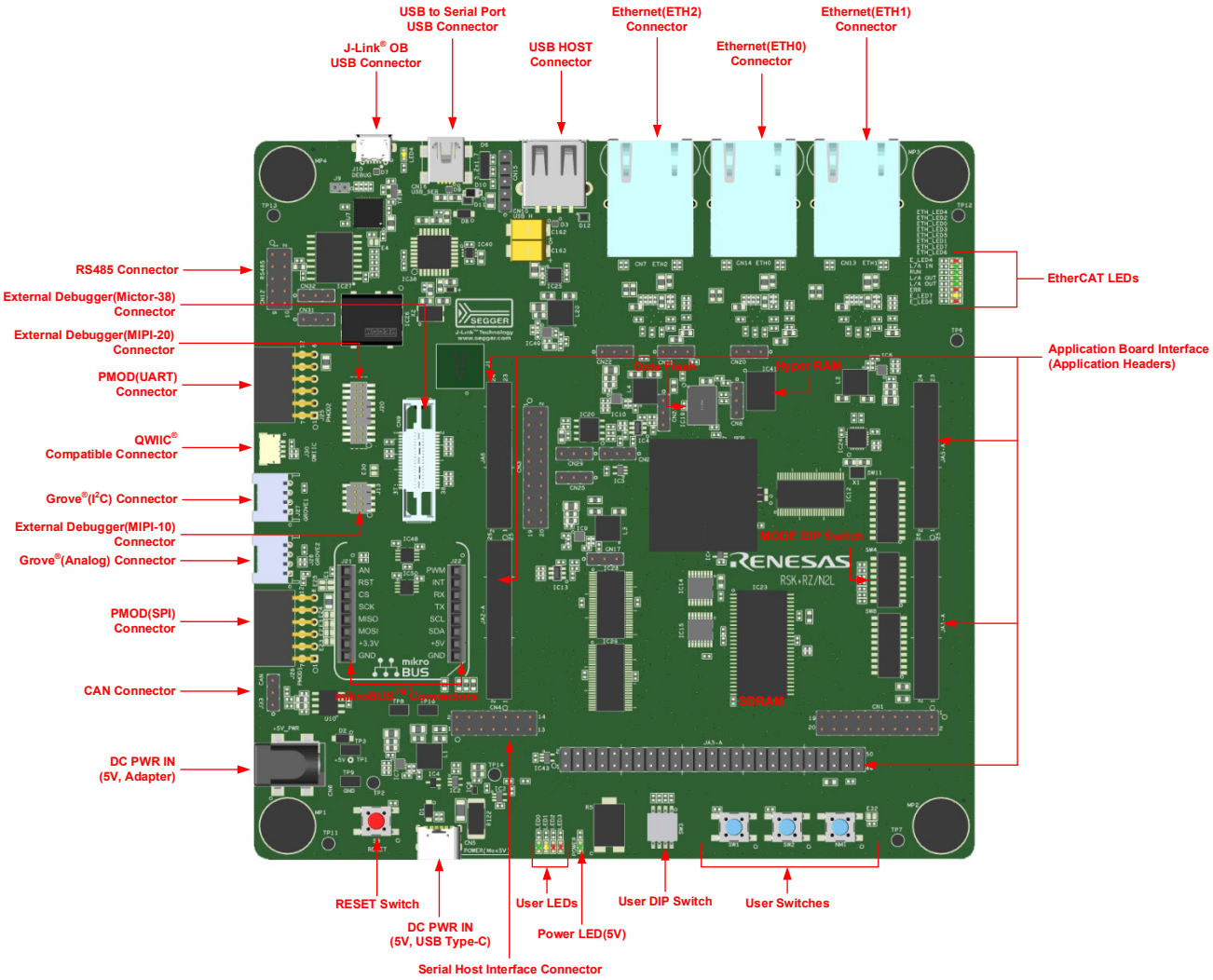

Figure 3-1: Board Layout (Top side)

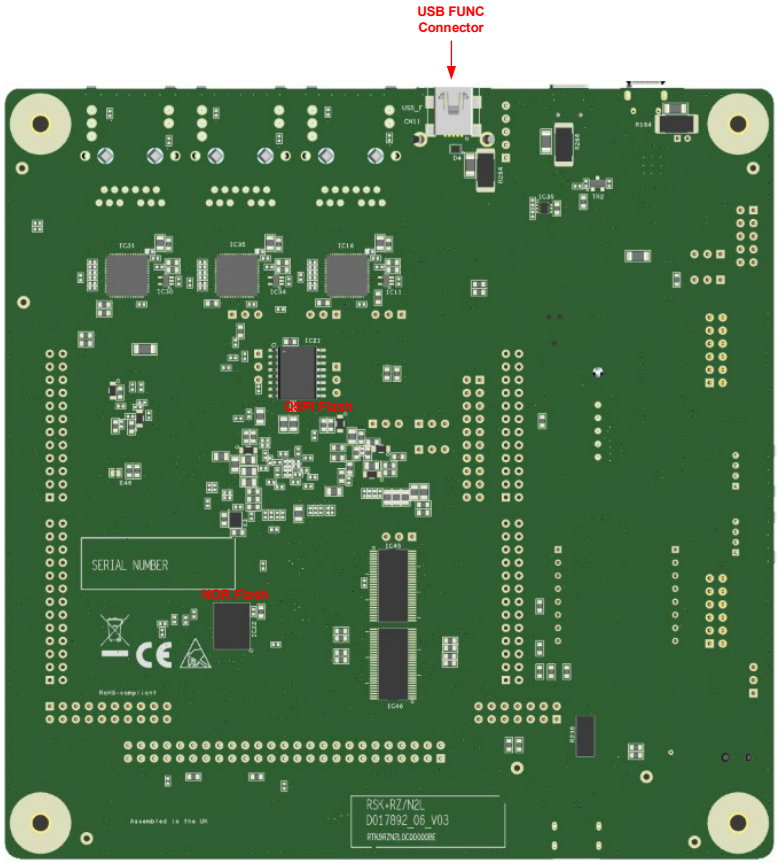

Figure 3-2: Board Layout (Bottom side)

3.2 Board Dimensions

Figure 3-3 below gives the board dimensions and connector positions. All the through-hole connectors are on a common 2.54mm pitch grid for easy interfacing.

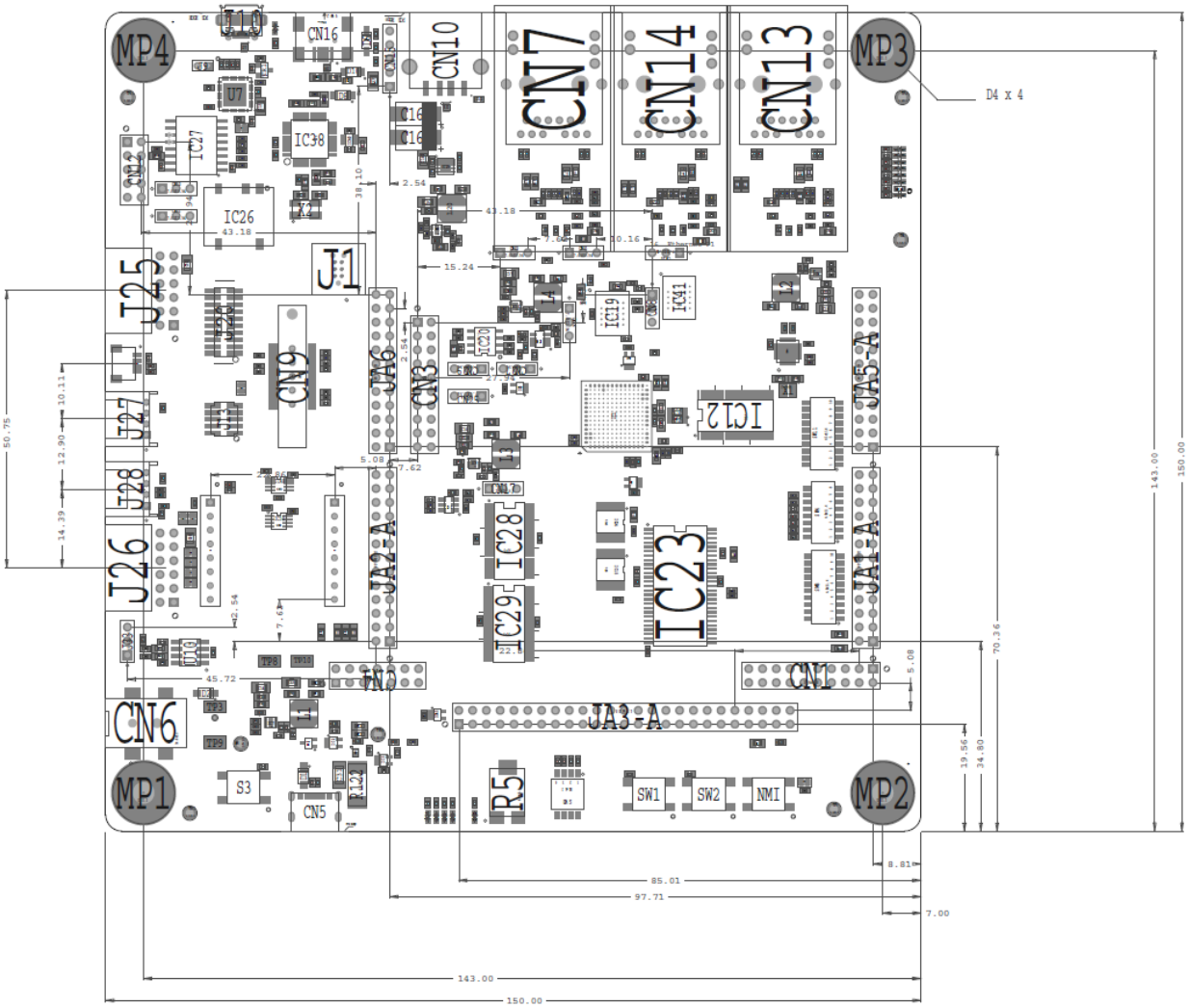

Figure 3-3: Board Dimensions (Unit: mm)

3.3 Component Placement

For placement details of individual components on the board, refer to section [10. Appendix].

4. Connectivity

4.1 Internal Board Connections

The diagram below shows the CPU board components and their connectivity to the MPU.

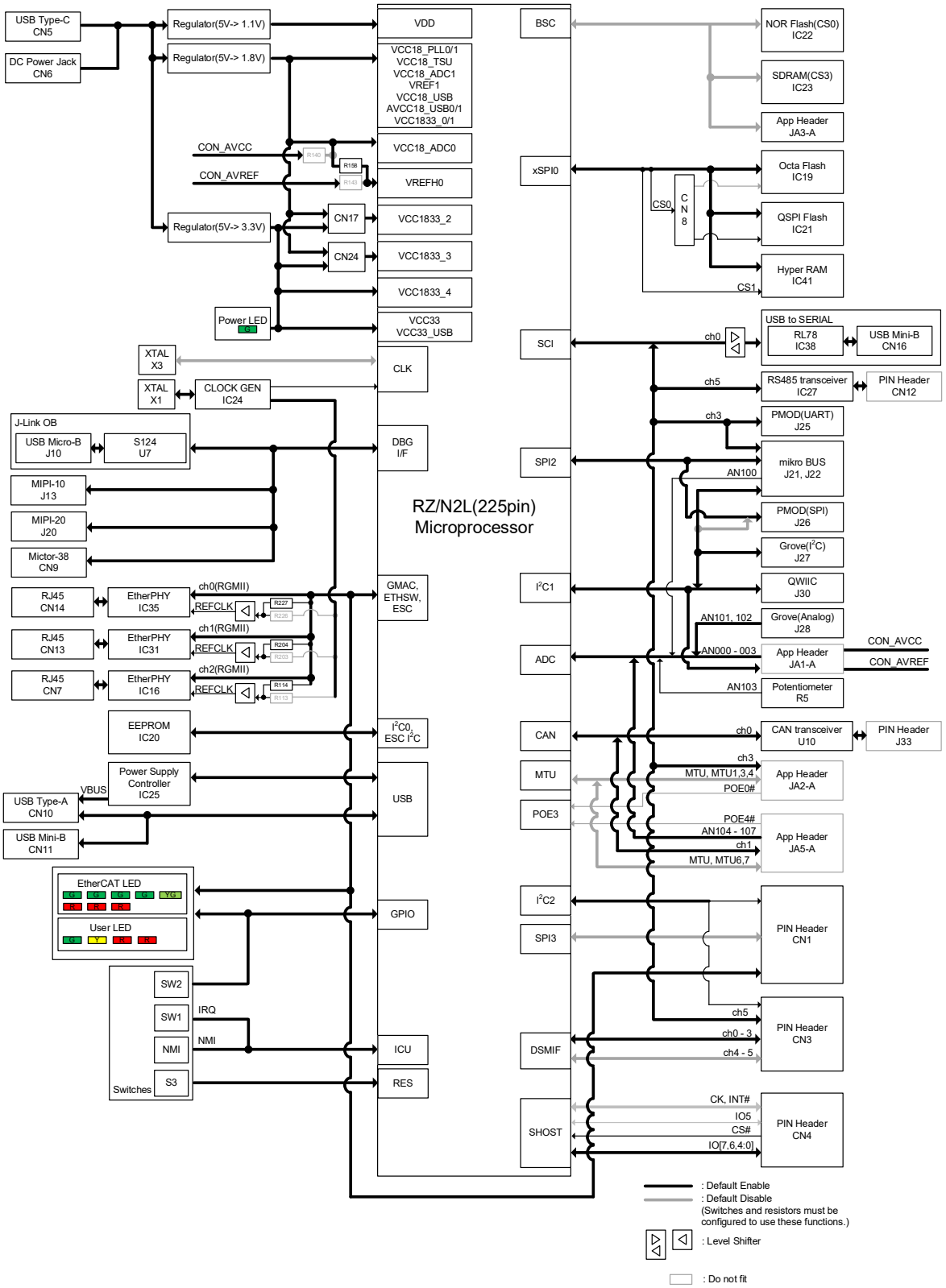

Figure 4-1: Internal Board Block Diagram

4.2 Emulator Connections

Figure 4-2 below shows the connection between the CPU board, emulator and the host PC, **Figure 4-3** below shows the connection between the CPU board, J-Link® OB and the host PC.

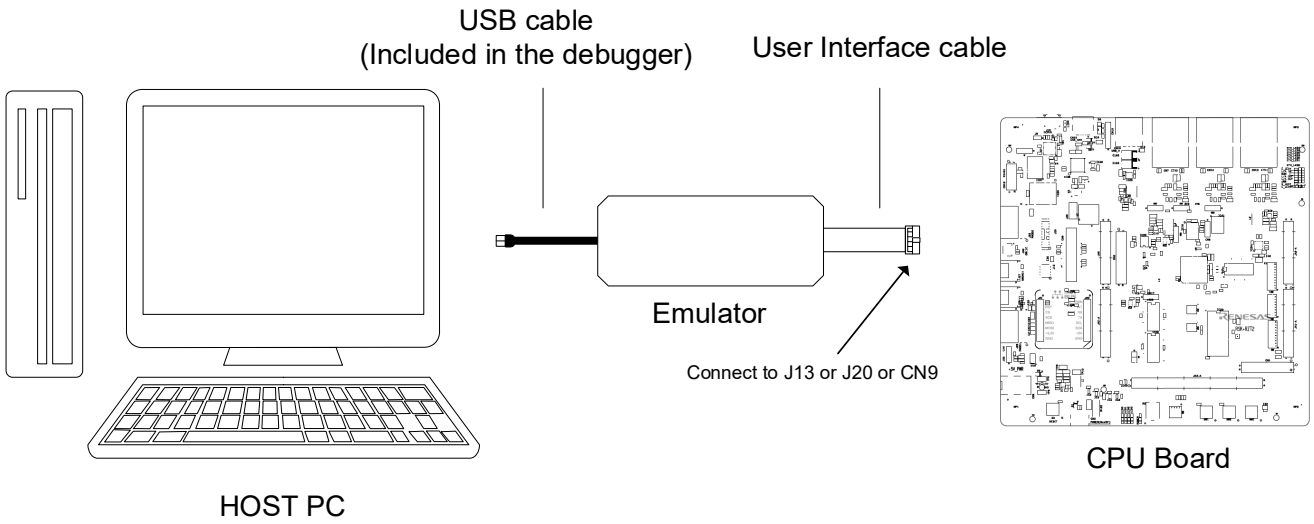

Figure 4-2: Emulator Connection Diagram (External Emulator)

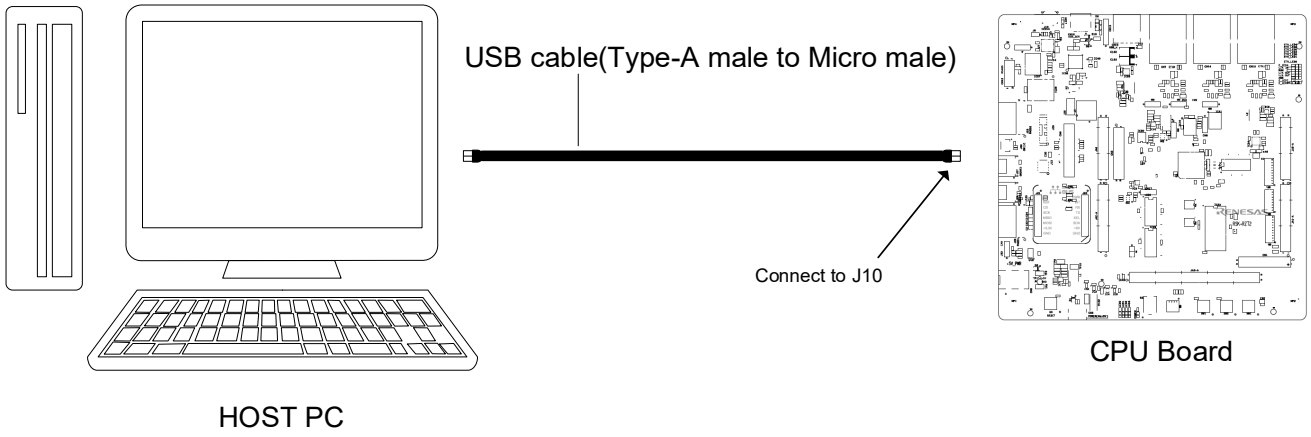

Figure 4-3: Emulator Connection Diagram (J-Link® OB)

5. User Circuitry

5.1 Reset Circuit

A reset control circuit is fitted to the CPU board to generate the required reset signal and is triggered from the RESET switch and the power-on-reset circuit. Refer to the RZ/N2L Group User's Manual: Hardware for details regarding the reset signal timing requirements, and the CPU board schematics for information regarding the reset circuitry in use on the board.

5.2 Clock Circuit

A clock circuit is fitted to the CPU board to generate the required clock signal to drive the MPU, and associated peripherals. Refer to the RZ/N2L Group Hardware Manual and the RL78/G1C hardware manual for details regarding the clock signal requirements, and the CPU board schematics for information regarding the clock circuitry in use on the CPU board. Details of the oscillators fitted to the board are listed in **Table 5-1** below.

Table 5-1: Crystal

Crystal	Function	Default Placement	Frequency	Device Package
X1	Main MPU crystal for RZ/N2L (via clock generator (IC24))	Fitted	25MHz	Encapsulated, SMT
X2	Main MCU crystal for RL78/G1C	Fitted	12MHz	Encapsulated, SMT
X3	Main MPU crystal for RZ/N2L (MPU direct)	Fitted	25MHz	Encapsulated, SMT

5.3 Switches

There are four push switches and four DIP switches located on the CPU board. The function of each switch and its connection is shown in **Table 5-2** and **Table 5-3**. For further information regarding switch connectivity, refer to the CPU board schematics.

Table 5-2: Push Switch Connections

Switch	Function	MPU	
		Port	Pin
S3	When pressed, the microprocessor is reset.	RES#	P6
SW1	Connects to IRQ7 for user controls.	P16_3	G12
SW2	Connects to IRQ12 for user controls.	P05_4	K1
NMI	Connects to an NMI input for user controls.	P16_2	H14

Table 5-3: DIP Switch Connections

Switch	Function	MPU	
		Port	Pin
SW3-1[*1]	Connects to P13_6 for user controls.	P13_6	M13
SW3-2[*1]	Connects to P13_5 for user controls.	P13_5	M12
SW3-3[*1]	Connects to P14_0 for user controls.	P14_0	L13
SW3-4	Connects to P13_7 for user controls.	P13_7	M11
SW4-1	Refer to section 6.3 for the setting contents.	P04_5	H3
SW4-2	Refer to section 6.3 for the setting contents.	P04_6	H5
SW4-3	Refer to section 6.3 for the setting contents.	P04_7	J1
SW4-4	Refer to section 6.3 for the setting contents.	P17_0	F12
SW4-5	Refer to section 6 for the setting contents.	-	-
SW4-6	Refer to section 6 for the setting contents.	-	-
SW4-7	Refer to section 6 for the setting contents.	-	-
SW4-8	Refer to section 6 for the setting contents.	-	-
SW8-1	Refer to section 6 for the setting contents.	P18_2	D14
SW8-2	Refer to section 6 for the setting contents.	P18_2	D14
SW8-3	Refer to section 6 for the setting contents.	P18_2	D14
SW8-4	Refer to section 6 for the setting contents.	P22_1	A6
SW8-5	Refer to section 6 for the setting contents.	P22_1	A6
SW8-6	Refer to section 6 for the setting contents.	P22_0	A7
SW8-7	Refer to section 6 for the setting contents.	P22_0	A7
SW8-8	Refer to section 6 for the setting contents.	P02_2	F3
SW8-9	Refer to section 6 for the setting contents.	P02_2	F3
SW8-10	Refer to section 6 for the setting contents.	P02_2	F3
SW11-1	Refer to section 6 for the setting contents.	P17_3	F14
SW11-2	Refer to section 6 for the setting contents.	P17_3	F14
SW11-3	Refer to section 6 for the setting contents.	P17_3	F14
SW11-4	Refer to section 6 for the setting contents.	P21_2	C8
SW11-5	Refer to section 6 for the setting contents.	P21_2	C8
SW11-6	Refer to section 6 for the setting contents.	P21_5	C7
SW11-7	Refer to section 6 for the setting contents.	P21_5	C7
SW11-8	Refer to section 6 for the setting contents.	P01_7	C1
SW11-9	Refer to section 6 for the setting contents.	P01_7	C1
SW11-10	Refer to section 6 for the setting contents.	P01_7	C1

[*1]: To use SW3, it is necessary to turn off the SW4.8 setting.

5.4 LEDs

There are 20 LEDs on the RSK+ board. The function of each LED, its colour, and its connections are shown in **Table 5-4**.

Table 5-4: LED Connections

LED	Colour	Function	MPU	
			Port	Pin
POWER	Green	Indicates the status of the 3.3V power rail.	-	-
LED0	Green	User operated LED.	P18_2	D14
LED1	Yellow	User operated LED.	P22_3	B6
LED2	Red	User operated LED.	P04_1	H2
LED3	Red	User operated LED.	P17_3	F14
LED4	Yellow	Indicates the status of the J-Link® OB.	-	-
ETH_LED0	Green	EtherCAT LED(LEDRUN)	P20_2	D8
ETH_LED1	Red	EtherCAT LED(LEDERR)	P20_3	D9
ETH_LED2	Green	EtherCAT LED(LINKACT0)	P20_1	B9
ETH_LED3	Green	EtherCAT LED(LINKACT1)	P20_4	A9
ETH_LED4	Red	EtherCAT LED	P03_0	G3
ETH_LED5	Green	EtherCAT LED(LINKACT2)	P22_1	A6
ETH_LED6	Red	EtherCAT LED	P04_4	H4
ETH_LED7	Yellow green	EtherCAT LED	P05_0	J5
ETHERNET Connector (ETH0)	Green	Ethernet LED(Link)	-	-
ETHERNET Connector (ETH0)	Yellow	Ethernet LED(Activity)	-	-
ETHERNET Connector (ETH1)	Green	Ethernet LED(Link)	-	-
ETHERNET Connector (ETH1)	Yellow	Ethernet LED(Activity)	-	-
ETHERNET Connector (ETH2)	Green	Ethernet LED(Link)	-	-
ETHERNET Connector (ETH2)	Yellow	Ethernet LED(Activity)	-	-

5.5 Potentiometer

A single-turn potentiometer is connected as a potential divider to analog input AN103, pin A13. The potentiometer can be used to create a voltage between VCC18_ADC1 and GROUND.
Refer to the Manufacturer's website for specification of the potentiometer (PIHER with part number N6L50T7S-103R).

The potentiometer offers an easy method of supplying a variable analog input to the microprocessor. It does not necessarily reflect the accuracy of the controller's ADC. Refer to the RZ/N2L Group User's Manual: Hardware for further details.

5.6 Pmod™

The RSK+ board is equipped with connectors for Digilent Pmod™ interface. Please connect the Pmod™ Peripheral module that is compatible with the PMOD connector.

The Digilent Pmod™ Compatible headers use an SPI interface, an I^2C interface and a UART interface. **Figure 5-1** below shows Digilent Pmod™ Compatible Header Pin Numbering. Connection information for the Digilent Pmod™ Compatible header is provided in **Table 5-5** and **Table 5-6** below.

Please note that the connector numbering adheres to the Digilent Pmod™ standard and is different from all other connectors on the RSK+ designs. Details can be found in the Digilent Pmod™ Interface Specification.

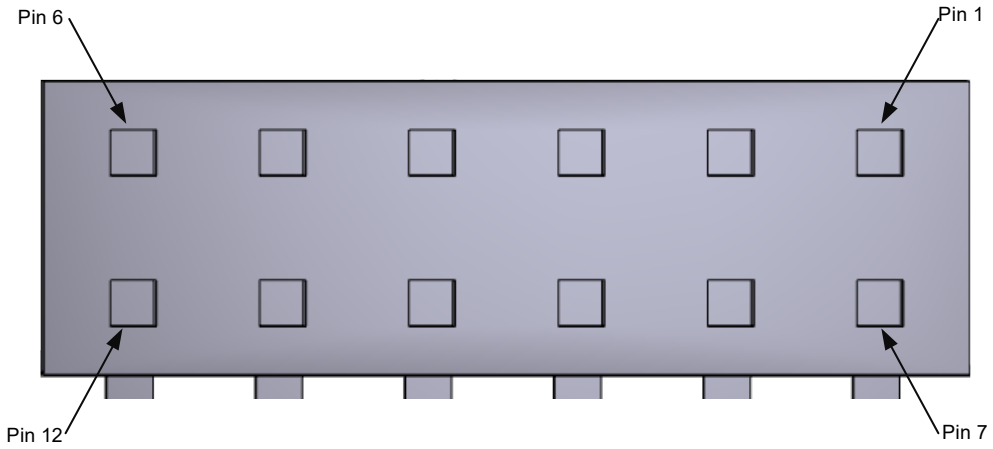

Figure 5-1: Digilent Pmod™ Compatible Header Pin Numbering

Table 5-5: Pmod™ Header (J25) Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MPU		Pin	Circuit Net Name	MPU	
		Port	Pin			Port	Pin
1	SCI_CTS	P17_4	F13	7	PMOD3A_INT	P03_5	G1
2	SCI_TXD	P18_0	E14	8	PMOD3A_RESET	P16_7	G14
3	SCI_RXD	P17_7	E15	9	PMOD3A_GPIO1_MDD	P17_0	F12
4	SCI_RTS_M1_UN	P18_1	D15	10	PMOD3A_GPIO2	P18_2	D14
5	GROUND	-	-	11	GROUND	-	-
6	3.3V	-	-	12	3.3V	-	-

Table 5-6: Pmod™ Header (J26) Connections

Digilent Pmod™ Compatible Header Connections							
Pin	Circuit Net Name	MPU		Pin	Circuit Net Name	MPU	
		Port	Pin			Port	Pin
1	CS	P21_1	B8	7	PMOD2A_INT	P03_6	G4
2	MOSI	P18_5	D13	8	PMOD2A_RESET	P04_0	H1
3*	P18_6_MISO SCL	P18_6 P05_2	C15 J4	9	PMOD2A_CS2_GPIO	P04_7	J1
4*	SCK SDA	P18_4 P05_3	E12 J3	10	PMOD2A_CS3_GPIO	P04_6	H5
5	GROUND	-	-	11	GROUND	-	-
6*	3.3V 5.0V	-	-	12	3.3V 5.0V	-	-

*: It is necessary to set the solder bridge jumper to change the function. Refer to section 6.2 for the required modifications.

5.7 Grove®

The RSK+ board is equipped with connectors for Grove® interface. Please connect the Grove® module that is compatible with connector.
The Grove® compatible headers use an I²C interface and an analog interface. **Figure 5-2** below shows Grove® Compatible Header Pin Numbering. Connection information for the Grove® Compatible header is provided in **Table 5-7** and **Table 5-8** below.

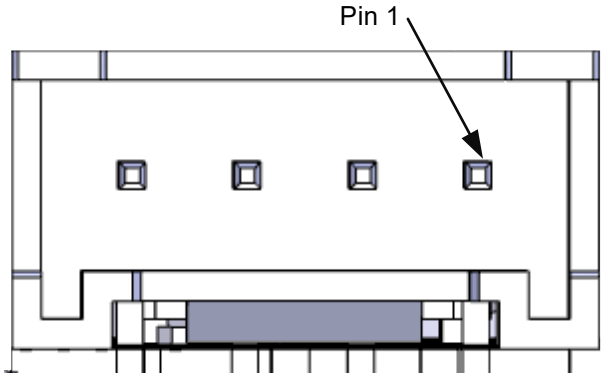

Figure 5-2: Grove® Compatible Header Pin Numbering

Table 5-7: Grove® Header (J27) Connections

Grove® Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	SCL	P05_2	J4
2	SDA	P05_3	J3
3	3.3V	-	-
4	GROUND	-	-

Table 5-8: Grove® Header (J28) Connections

Grove® Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	ADC_AN101	AN101	A14
2	ADC_AN102	AN102	B11
3	3.3V	-	-
4	GROUND	-	-

5.8 QWIIC®

The RSK+ board is equipped with connectors for QWIIC® interface. Please connect the QWIIC® products that is compatible with connector.
The QWIIC® compatible headers use an I²C interface. **Figure 5-3** below shows QWIIC® Compatible Header Pin Numbering. Connection information for the QWIIC® Compatible header is provided in **Table 5-9** below.

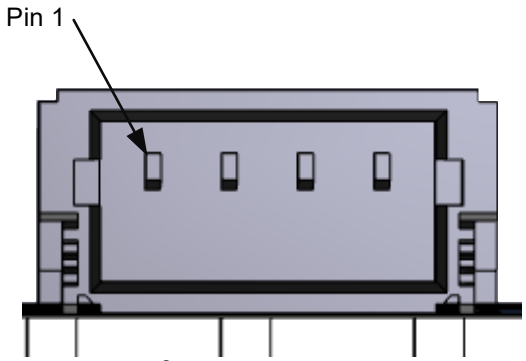

Figure 5-3: QWIIC® Compatible Header Pin Numbering

Table 5-9: QWIIC® Header (J30) Connections

QWIIC® Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	GROUND	-	-
2	3.3V	-	-
3	SDA	P05_3	J3
4	SCL	P05_2	J4

5.9 mikroBUS™

The RSK+ board is equipped with connectors for mikroBUS™ interface. Please connect the mikroBUS™ products that is compatible with connector.
The mikroBUS™ compatible headers use analog interface, SPI interface, UART interface, I2C interface, PWM and interrupt. Connection information for the mikroBUS™ Compatible header is provided in **Table 5-10 and Table 5-11** below.

Table 5-10: mikroBUS™ Header (J21) Connections

mikroBUS™ Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	ADC_AN100	AN100	B12
2	MB_RST#_M1_WN	P18_3	E13
3	CS	P21_1	B8
4	SCK	P18_4	E12
5	P18_6_MISO	P18_6	C15
6	MOSI	P18_5	D13
7	3.3V	-	-
8	GROUND	-	-

Table 5-11: mikroBUS™ Header (J22) Connections

mikroBUS™ Compatible Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	MIK_PWM_SCK	P17_6	G15
2	MIKROBUS_INT	P03_7	G5
3	SCI_RXD	P17_7	E15
4	SCI_TXD	P18_0	E14
5	SCL	P05_2	J4
6	SDA	P05_3	J3
7	5.0V	-	-
8	GROUND	-	-

5.10 USB Serial Port

A USB serial port is implemented in a Renesas low power microcontroller (RL78/G1C) and is connected to the RZ/N2L Serial Communications Interface (SCI) module. Connections between the USB to Serial converter and the microprocessor are listed in **Table 5-12** below.

Table 5-12: Serial Port Connections

Signal Name	Function	MPU	
		Port	Pin
UART_USB_TX	SCI0 Transmit Signal.	P16_5	H15
UART_USB_RX	SCI0 Receive Signal.	P16_6	G11

When the CPU board is first connected to a PC running Windows™ with the USB/Serial connection, the PC will look for a driver. Use the driver that is installed as standard on your PC.
If you do not have the driver, please download the driver installer from the following URL.
https://www.renesas.com/document/rsk-usb-serial-driver?language=en

5.11 Controller Area Network (CAN)

A CAN transceiver IC (U10) is fitted to the RSK+ board and connected to the CAN MPU peripheral. For further details regarding the CAN protocol and supported modes of operation, please refer to the RZ/N2L Group User's Manual: Hardware. Connection information for the CAN interface header is provided in **Table 5-13** below. The details of connecting to the connected device and MPU are shown in **Table 5-14** below.

Table 5-13: CAN Interface Header (J33) Connections

CAN Interface Header Connections	
Pin	**Circuit Net Name**
1	CAN_H
2	CAN_L
3	GROUND

Table 5-14: CAN Connections

CAN Signal	Function	MPU	
		Port	Pin
CAN_TX*1	CAN Data Transmission.	P02_2	F3
CAN_RX*1	CAN Data Reception.	P01_7	C1

*1: This connection is a not available in the default RSK+ configuration - refer to section 6 for the required modifications.

5.12 Ethernet

When running any Ethernet software, a unique MAC address should be used. A unique Renesas allocated MAC address is attached to the PCB as a sticker and should always be used with this device ensured to ensure full compatibility when using other Renesas hardware on a common Ethernet connection.

Three Ethernet PHY ICs are fitted to the CPU board and are connected to the MPU Ethernet peripherals. The RZ/N2L MPU supports half and full duplex, 10Mb/s and 100Mb/s and 1000Mb/s transmission and reception. Refer to section 5.4 Ethernet LEDs. The connections for the Ethernet controller are listed in **Table 5-15, Table 5-16, Table 5-17, Table 5-18, Table 5-19** below.
Note that Ethernet channel 2 cannot be used at the same time as the external bus.

Table 5-15: Ethernet Connections (ETH0)

Ethernet signal	Function	MPU	
		Port	Pin
ETH0_TXCLK	RGMII: Transmit clock output	P09_7	L7
ETH0_TXEN	RGMII: Transmit data enable / error	P10_0	N8
ETH0_TXD0	RGMII: Transmit data0	P09_6	M7
ETH0_TXD1	RGMII: Transmit data1	P09_5	N7
ETH0_TXD2	RGMII: Transmit data2	P09_4	M6
ETH0_TXD3	RGMII: Transmit data3	P09_3	R4
ETH0_RXCLK	RGMII: Receive clock input	P08_6	M5
ETH0_RXDV	RGMII: Receive data valid / Receive data error	P08_5	P3
ETH0_RXD0	RGMII: Receive data0	P10_1	M8
ETH0_RXD1	RGMII: Receive data1	P10_2	L8
ETH0_RXD2	RGMII: Receive data2	P10_3	L9
ETH0_RXD3	RGMII: Receive data3	P08_4	N4
ETH0_REFCLK	RGMII: Outputs 25MHz clock for EtherPHY0	P09_1	R3

Table 5-16: Ethernet Connections (ETH1)

Ethernet signal	Function	MPU	
		Port	Pin
ETH1_TXCLK	RGMII: Transmit clock output	P06_4	N1
ETH1_TXEN	RGMII: Transmit data enable / error	P06_5	N2
ETH1_TXD0	RGMII: Transmit data0	P06_3	K4
ETH1_TXD1	RGMII: Transmit data1	P06_2	M2
ETH1_TXD2	RGMII: Transmit data2	P05_7	M1
ETH1_TXD3	RGMII: Transmit data3	P06_0	L2
ETH1_RXCLK	RGMII: Receive clock input	P07_3	M4
ETH1_RXDV	RGMII: Receive data valid / Receive data error	P07_2	P2
ETH1_RXD0	RGMII: Receive data0	P06_6	L4
ETH1_RXD1	RGMII: Receive data1	P06_7	M3
ETH1_RXD2	RGMII: Receive data2	P07_0	P1
ETH1_RXD3	RGMII: Receive data3	P07_1	N3
ETH1_REFCLK	RGMII: Outputs 25MHz clock for EtherPHY1	P06_1	L3

Table 5-17: Ethernet Connections (ETH2)

Ethernet signal	Function	MPU	
		Port	Pin
ETH2_TXCLK	RGMII: Transmit clock output	P00_6	C3
ETH2_TXEN	RGMII: Transmit data enable / error	P00_2	A3
ETH2_TXD0	RGMII: Transmit data0	P01_5	B1
ETH2_TXD1	RGMII: Transmit data1	P01_4	E4
ETH2_TXD2	RGMII: Transmit data2	P01_3	C2
ETH2_TXD3	RGMII: Transmit data3	P01_2	B2
ETH2_RXCLK	RGMII: Receive clock input	P24_1	B5
ETH2_RXDV	RGMII: Receive data valid / Receive data error	P00_1	D5
ETH2_RXD0	RGMII: Receive data0	P23_7	D6
ETH2_RXD1	RGMII: Receive data1	P24_0	A5
ETH2_RXD2	RGMII: Receive data2	P24_2	C5
ETH2_RXD3	RGMII: Receive data3	P00_0	C4
ETH2_REFCLK	RGMII: Outputs 25MHz clock for EtherPHY2	P00_3	B3

Table 5-18: Ethernet Connections (ETH0/ETH1/ETH2)

Ethernet signal	Function	MPU	
		Port	Pin
ETH_MDIO	Management data I/O	P09_0	P4
ETH2_MDIO	Management data I/O	P01_0	A2
ETH_MDC	Management data clock	P08_7	N5
ETH2_MDC	Management data clock	P01_1	D3

Table 5-19: Default PHY setting

Default PHY setting items	Default PHY setting contents
PHY Address	ETH0 (IC35): = 0 ETH1 (IC31): = 1 ETH2 (IC16): = 2
MAC Interface	RGMII
Isolate	Disable
Speed	Depends auto negotiation
Duplex	Full-Duplex
Auto negotiation	Enable

5.13 Ethernet Switch (ETHSW)

The CPU board has an Ethernet Switch (ETHSW) and is connected to the ETHSW module of the microprocessor. The ETHSW connections to and from the MPU are shown in **Table 5-15, Table 5-16, Table 5-17, Table 5-18, Table 5-20** below. Note that ETHSW channel 2 cannot be used at the same time as the external bus.

Table 5-20: Ethernet Connections (ETHSW0/ETHSW1/ETHSW2)

Ethernet signal	Function	MPU	
		Port	Pin
ETHSW_LPI0	Port0 MAC status	P05_4	K1
ETHSW_LPI1	Port1 MAC status	P01_7	C1
ETHSW_LPI2	Port2 MAC status	P02_0	E3
ETHSW_PTPOUT0	Ethernet switch timer pulse	P13_6	M13
ETHSW_PTPOUT1	Ethernet switch timer pulse	P02_1	D1
ETHSW_PTPOUT2	Ethernet switch timer pulse	P13_2	L10
ETHSW_PTPOUT3	Ethernet switch timer pulse	P13_3	N12
ETHSW_TDMAOUT0	Ethernet switch TDMA timer	P02_2	F3
ETHSW_TDMAOUT1	Ethernet switch TDMA timer	P02_3	E1
ETHSW_TDMAOUT2	Ethernet switch TDMA timer	P20_3	D9
ETHSW_TDMAOUT3	Ethernet switch TDMA timer	P20_4	A9
ETH0_LINK	Ethernet switch PHY link status	P10_4	M9
ETH1_LINK	Ethernet switch PHY link status	P05_5	K2
ETH2_LINK	Ethernet switch PHY link status	P00_5	B4

5.14 EtherCAT Slave Controller (ESC)

To run the EtherCAT slave controller software, the EtherCAT ID number is required. Please use SW3 as necessary.

The CPU board has an EtherCAT slave controller (ESC) and is connected to the ESC module of the microprocessor. EtherCAT status LEDs are listed in section 5.4. The EtherCAT connections to and from the MPU are shown in **Table 5-15, Table 5-16, Table 5-17, Table 5-18, Table 5-21** below.
Note that ESC channel 2 cannot be used at the same time as the external bus.

Table 5-21: Ethernet Connections (ESC0/ESC1/ESC2)

Ethernet signal	Function	MPU	
		Port	Pin
ESC_LEDRUN	EtherCAT RUN LED signal output port	P20_2	D8
ESC_IRQ	EtherCAT IRQ signal output port	P17_0	F12
ESC_LEDERR	EtherCAT Error LED signal output port	P20_3	D9
ESC_LINKACT0	EtherCAT link / Activity LED signal output port	P20_1	B9
ESC_LINKACT1	EtherCAT link / Activity LED signal output port	P20_4	A9
ESC_LINKACT2	EtherCAT link / Activity LED signal output port	P22_1	A6
ESC_SYNC0	EtherCAT SYNC0 signal output port	P02_1	D1
ESC_SYNC1	EtherCAT SYNC1 signal output port	P02_1	D1
ESC_LATCH0	EtherCAT LATCH0 signal input port	P01_6	D2
ESC_LATCH1	EtherCAT LATCH1 signal input port	P01_6	D2
ESC_RESETOUT#	EtherCAT reset signal output port	P13_4	L12
EEPROM_SCL	EtherCAT EEPROM I^2C clock output port	P13_2	L10
EEPROM_SDA	EtherCAT EEPROM I^2C data signal I/O port	P13_3	N12
ETH0_LINK	EtherCAT PHY0 link status signal input port	P10_4	M9
ETH1_LINK	EtherCAT PHY1 link status signal input port	P05_5	K2
ETH2_LINK	EtherCAT PHY2 link status signal input port	P00_5	B4

5.15 Universal Serial Bus (USB)

This CPU board is fitted with a USB Host socket (type A, CN10) and a Function socket (type Mini B, CN11). USB module USB is connected to the Host and Function socket and can operate as either a Host or Function device. However, they cannot be used at the same time. The connection for the USB module is shown in **Table 5-22** below.

Table 5-22: USB Module Connections

USB Signal	Function	MPU	
		Port	Pin
USB_DP	D+ I/O pin of the USB on-chip transceiver	USB_DP	R13
USB_DM	D– I/O pin of the USB on-chip transceiver	USB_DM	P13
USB_VBUSIN	VBUS (5V) supply enable signal for external power supply chip	P07_4	R2
USB_VBUSEN	Outputs the VBUS power enable signal for USB.	P19_0	B15
USB_OVRCUR	External overcurrent detection signal B	P17_5	F15

5.16 External Bus

The RZ/N2L features an external data bus, which is connected to various devices on the CPU board. Details of the devices connected to the external data bus are listed in **Table 5-23** below. Further details of the devices connected to the external bus can be found in the board schematics.

Table 5-23: External Bus Address Space

Chip Select	Device Name	Device Description	Address Space
CS0	IC22	256Mbit NOR Flash	70000000h – 71FFFFFFh (32Mbyte)
CS2	IC23	256Mbit SDRAM	74000000h – 75FFFFFFh (32Mbyte)
CS3	IC23	256Mbit SDRAM	78000000h – 79FFFFFFh (32Mbyte)
	JA3-A	Application Header	78000000h – 7BFFFFFFh (64Mbyte)
CS5	JA3-A	Application Header	7C000000h – 7FFFFFFFh (64Mbyte)

5.17 Expanded Serial Peripheral Interface (xSPI)

The RZ/N2L features two Expanded Serial Peripheral Interface modules (xSPI). **Table 5-24** below details the connected devices, and their connections to the MPU.

Table 5-24: Expanded Serial Interface (xSPI) Address Space

Chip Select	Device Name	Device Description	Address Space
XSPI0_CS0*1	IC19	512Mbit Octa Flash	60000000h – 63FFFFFFh (64Mbyte)
XSPI0_CS0	IC21	512Mbit Serial Flash	60000000h – 63FFFFFFh (64Mbyte)
XSPI0_CS1	IC41	64Mbit Hyper RAM	64000000h – 647FFFFFh (8Mbyte)

*1: This connection is a not available in the default RSK+ configuration - refer to section 6 for the required modifications.

5.18 I²C Bus (Inter-IC Bus)

The RZ/N2L features three I²C (Inter-IC Bus) interface modules. Channel 0 of the IIC is connected to a 16Kbit EEPROM. Channel 0 of the IIC is also multiplexed with I²C for EtherCAT and can also be used as EEPROM for EtherCAT. Channel 1 of the IIC is connected to Pmod™ and Grove®, QWIIC®, mikroBUS™, Application Headers. **Table 5-25** below details the connected device, and their connection to the MPU.

Table 5-25: I²C BUS Port Connections

Signal Name	Function	MPU	
		Port	Pin
EEPROM_SCL (RIIC0)	CLOCK	P13_2	L10
EEPROM_SDA (RIIC0)	DATA	P13_3	N12
SCL (RIIC1)	CLOCK	P05_2	J4
SDA (RIIC1)	DATA	P05_3	J3

5.19 RS485 Interface

A RS485 transceiver IC is fitted to the RSK+ board and connected to the SCI MPU peripheral. Connection information for the RS485 Interface header is provided in **Table 5-26** below. The details of connecting to the connected device and MPU are shown in **Table 5-27** below.

Table 5-26: RS485 Interface Header (CN12) Connections

RS485 Interface Header Connections			
Pin	**Circuit Net Name**	**Pin**	**Circuit Net Name**
1	NC	2	NC
3	RS485_B	4	RS485_Y
5	RS485_Z	6	RS485_A
7	NC	8	NC
9	NC	10	NC

Table 5-27: SCI Port Connections

Signal Name	**Function**	**MPU**	
		Port	**Pin**
RS485_RX*1	SCI5 Transmit Signal	P21_2	C8
RS485_DE*1	SCI5 Driver Enable Signal	P22_0	A7
RS485_TX*1	SCI5 Transmit Signal	P21_3	A8

*1: This connection is a not available in the default RSK+ configuration - refer to section 6 for the required modifications.

5.20 Serial Host Interface

The RZ/N2L features a serial host interface to connect an external host CPU (SPI master) with up to eight input/output pins. These pins are connected to a pin header (CN4), and by connecting to the pin header and the external host CPU, the external host CPU can directly access the RZ/N2L's internal resources (mainly the system SRAM). Details of the pin headers are shown in **Table 5-28** below.

Table 5-28: Serial Host Interface Header (CN4) Connections

Serial Host Interface Header Connections			
Pin	**Circuit Net Name**	**MPU**	
		Port	**Pin**
1	GROUND	-	-
2	GROUND	-	-
3	HSPI_CK	P14_2	K12
4	HSPI_CS#	P16_0	G13
5	HSPI_IO0	P14_1	L14
6	HSPI_IO1	P14_3	M14
7	HSPI_IO2	P16_2	H14
8	HSPI_IO3	P16_3	G12
9	HSPI_IO4	P16_5	H15
10	HSPI_IO5	P16_6	G11
11	HSPI_IO6	P18_0	E14
12	HSPI_IO7	P18_1	D15
13	HSPI_INT#-B	P21_1	B8
14	3.3V	-	-

6. Configuration

6.1 Modifying the RSK+

This section lists the option links that are used to modify the way CPU board operates in order to access different configurations. Configurations are made by modifying link resistors or headers with movable jumpers or by configuration DIP switches.

A link resistor is a 0Ω surface mount resistor, which is used to short or isolate parts of a circuit. Option links are listed in the following sections, detailing their function when fitted or removed. **Bold, blue text** indicates the default configuration that the CPU board is supplied with. Refer to the component placement diagram (section 3) to locate the option links, jumpers and DIP switches.

When removing soldered components, always ensure that the CPU board is not exposed to a soldering iron for intervals greater than 5 seconds. This is to avoid damage to nearby components mounted on the board.

When modifying a link resistor, always check the related option links to ensure there is no possible signal contention or short circuits. Because many of the MPU's pins are multiplexed, some of the peripherals must be used exclusively. Refer to the RZ/N2L Group User's Manual: Hardware and CPU board schematics for further information.

6.2 Jumper Settings

Three types of jumpers are provided on the CPU board.
1. Solder bridge
2. Trace-cut
3. Traditional pin header jumpers

The following sections describe each type and their default configuration.

6.2.1 Solder Bridge

A **solder-bridge** jumper is provided with two isolated pads that may be joined together by one of three methods:
- Solder may be applied to both pads to develop a bulge on each and the bulges joined by touching a soldering iron across the two pads.
- A small wire may be placed across the two pads and soldered in place.
- A SMD resistor, size 0805, 0603, or 0402, may be placed across the two pads and soldered in place. A zero-ohm resistor shorts the pads together.

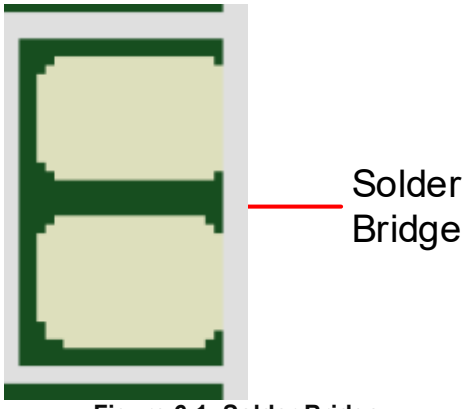

Figure 6-1: Solder Bridge

6.2.2 Trace Cut

A trace-cut jumper is provided with a narrow copper trace connecting its pads. The silk screen overlay printing around a trace-cut jumper is a solid box. To isolate the pads, cut the trace between pads adjacent to each pad, then remove the connecting copper foil either mechanically or with the assistance of heat. Once the etched copper trace is removed, the trace-cut jumper is turned into a solder-bridge jumper for any later changes.

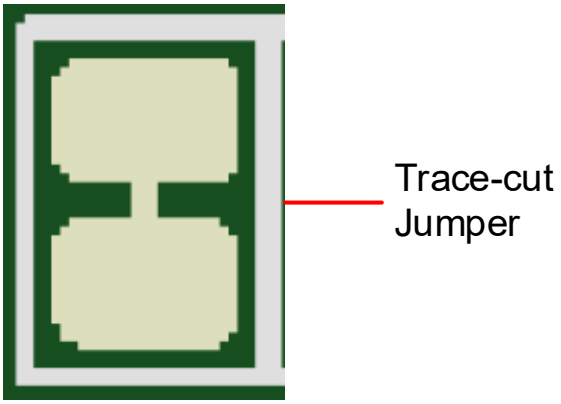

Figure 6-2: Trace Cut

6.2.3 Default Solder Bridge Jumper and Trace Cut Settings

The following table describes the default settings for solder bridge jumper and trace cut on the CPU board.

Table 6-1: Default Solder Bridge Jumper and Trace Cut Settings

Reference	Jumper Position	Explanation
E1	**Open**	**When using a Pmod™ module that requires a 3.3V supply. (J26)**
	Closed	When using a Pmod™ module that requires a 5V supply. Cannot be closed at the same time as E25.
E2	**Open**	**When the Pmod™ module of the I²C interface is not used. (J26)**
	Closed	When using the Pmod™ module of the I²C interface. (J26) Cannot be closed at the same time as E23.
E3	**Open**	**When the Pmod™ module of the I²C interface is not used. (J26)**
	Closed	When using the Pmod™ module of the I²C interface. (J26) Cannot be closed at the same time as E24.
E4	**Closed**	**When supplying 3.3V to the J-Link® OB circuit**
E23	Open	When the Pmod™ module of the SPI interface is not used. (J26)
	Closed	**When using the Pmod™ module of the SPI interface. (J26) Cannot be closed at the same time as E2**
E24	Open	When the Pmod™ module of the SPI interface is not used. (J26)
	Closed	**When using the Pmod™ module of the SPI interface. (J26) Cannot be closed at the same time as E3**
E25	Open	When using the Pmod™ module with a 5V power supply.
	Closed	**When using a Pmod™ module that requires a 3.3V supply. (J26) Cannot be closed at the same time as E1.**
E30	**Closed**	**When connecting to emulator.**
E32	**Closed**	**When using push switch of NMI.**
E46	**Open**	**When the external clock is not input from the application header (JA2-A).**
	Closed	When inputting the external clock from the application header (JA2-A).

6.2.4 Traditional Pin Header Jumpers

These jumpers are traditional small pitch jumpers that require an external shunt to open/close them. The following table describes the default settings for traditional small pitch jumpers on the CPU board.

Table 6-2: Default Traditional Small Pitch Jumper Settings

Reference	Jumper Position	Explanation
CN8	Short 1-2	When using Octa Flash
	Short 2-3	**When using QSPI Serial Flash**
CN17	Short 1-2	When using VCC1833_2 domain at 3.3V
	Short 2-3	**When using VCC1833_2 domain at 1.8V**
CN20	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes
CN21	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes
CN22	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes
CN24	Short 1-2	When using VCC1833_3 domain at 3.3V
	Short 2-3	**When using VCC1833_3 domain at 1.8V**
CN25	**Short 1-2**	**When using other than the SHOST interface**
	Short 2-3	When using the SHOST interface
CN27	**Short 1-2**	**When using the HyperRAM**
	Short 2-3	When using the SHOST interface
CN29	**Short 1-2**	**When using the USB Serial**
	Short 2-3	When using the SHOST interface
CN31	**Short 1-2**	**When using the RS485 transmission method in full duplex**
	Short 2-3	When using the RS485 transmission method in half duplex
CN32	**Short 1-2**	**When using the RS485 transmission method in full duplex**
	Short 2-3	When using the RS485 transmission method in half duplex
J9	**Open**	**When using the J-Link® OB**
	Short	When using the external emulator or not using the emulator

6.3 MPU Operating Modes

Table 6-3, Table 6-4, Table 6-5, Table 6-6 below details the option links associated with configuring the MPU Operating Modes.

Table 6-3: MPU Operating Modes Switch Settings (1)

SW4-1 (MD0)	SW4-2 (MD1)	SW4-3 (MD2)	Explanation
ON	**ON**	**ON**	**xSPI0 boot mode (x1 boot Serial flash)**
OFF	ON	ON	xSPI0 boot mode (x8 boot Serial flash) *1
ON	OFF	ON	16-bit bus boot mode (NOR flash)
OFF	OFF	ON	Serial host interface boot mode
ON	ON	OFF	Parallel host interface boot mode *1
OFF	ON	OFF	SCI (UART) boot mode
ON	OFF	OFF	USB boot mode
OFF	OFF	OFF	xSPI1 boot mode (x1 boot Serial flash) *1

*1: Not supported on this board.

Table 6-4: MPU Operating Modes Switch Settings (2)

SW4-4 (MDD)	Explanation
ON	**JTAG Authentication by Hash is disabled.**
OFF	JTAG Authentication by Hash mode

Table 6-5: MPU Operating Modes Switch Settings (3)

CN17 Pin 1-2	CN17 Pin 2-3	Explanation
OPEN	**SHORT**	**The operating voltage of VCC1833_2 is 1.8V*1**
SHORT	OPEN	The operating voltage of VCC1833_2 is 3.3V*2

*1: When using Ethernet (ETH2) in VCC1833_2.
*2: When using an external bus etc. in VCC1833_2.

Table 6-6: MPU Operating Modes Switch Settings (4)

CN24 Pin 1-2	CN24 Pin 2-3	Explanation
OPEN	**SHORT**	**The operating voltage of VCC1833_3 is 1.8V*1**
SHORT	OPEN	The operating voltage of VCC1833_3 is 3.3V*2

*1: When using xSPI0 in VCC1833_3.
*2: When using an external bus in VCC1833_3.

6.4 Emulator Configuration

6.4.1 External Emulator

Table 6-7, Table 6-8, Table 6-9 below details the function of the option links associated with External Emulator Configuration.

Table 6-7: External Emulator Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TMS	F5	P02_6	**TMS**	-	-	**J20.2**	-	-
						CN9.17	-	-
						J13.2	-	-
						U7.30	**R35**	-
TCK	F1	P02_7	**TCK**	-	-	**J20.4**	-	-
						CN9.15	-	-
						J13.4	-	-
						U7.40	**R23**	-
TDO	F4	P02_4	**TDO**	-	-	**J20.6**	-	-
						CN9.11	-	-
						J13.6	-	-
						U7.23	-	-
TDI	F2	P02_5	**TDI**	-	-	**J20.8**	-	-
						CN9.19	-	-
						J13.8	-	-
						U7.17	-	-
TRST#	E2	-	**POWER_RESET#**	-	-	**IC4.2**	-	-
						IC38.11	-	-
			TRST_OUT#	-	-	**J20.16**	-	-
						CN9.21	-	-
RESET#	P6	-	**POWER_RESET#**	-	-	**IC4.2**	-	-
						IC38.11	-	-
			RESET_SW#	-	-	**S3**	-	-
						U7.28	-	-
						J13.10	-	-
						J20.10	-	-
						CN9.9	-	-
TRACE_CLK_ BSC_D09	C6	P22_2	TRACE_CLK	IC28.16 (SW4-7 = ON) IC45.16 (SW4-6 = ON)	-	CN9.6	-	-
			BSC_D09	IC28.17 (SW4-7 = OFF)	-	IC22.F3	-	-
						IC23.44	-	-
						JA3-A.30	-	-
LED_RED2_ TRACE_CTL_ M1_POE	F14	P17_3	TRACE_CTL	IC45.47 (SW4-6 = ON)	-	CN9.36	-	-
			LED_RED2	**IC45.46 (SW4-6 = OFF) SW11-1 = ON**	**SW11-3 = OFF SW11-2 = OFF**	**LED3.A**	**R47**	-
			M1_POE	IC45.46 (SW4-6 = OFF) SW11-3 = ON	SW11-2 = OFF SW11-1 = OFF	JA2-A.24	-	-

Table 6-8: External Emulator Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D7_ BSC_D07	A7	P22_0	**TRACE_D7_ BSC_D07**	**-**	**-**	**CN3.8**	**-**	**-**
			TRACE_D7	IC28.11 (SW4-7 = ON) IC45.8 (SW4-6 = ON)	-	CN9.16	-	-
			M2_VN	IC28.11 (SW4-7 = ON) IC45.9 (SW4-6 = OFF) SW8-6 = ON	SW8-7 = OFF	JA5-A.22	-	-
			RS485_DE	IC28.11 (SW4-7 = ON) IC45.9 (SW4-6 = OFF) SW8-7 = ON	SW8-6 = OFF	IC27.5	-	-
			BSC_D07	IC28.12 (SW4-7 = OFF)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
TRACE_D6_ BSC_D06	B7	P21_7	**TRACE_D6_ BSC_D06**	**-**	**-**	**CN3.7**	**-**	**-**
			TRACE_D6	IC28.47 (SW4-7 = ON) IC45.50 (SW4-6 = ON)	-	CN9.18	-	-
			M2_WN	**IC28.47 (SW4-7 = ON) IC45.49 (SW4-6 = OFF)**	**-**	**JA5-A.24**	**-**	**-**
			BSC_D06	IC28.46 (SW4-7 = OFF)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-
TRACE_D5_ BSC_D05	D7	P21_6	TRACE_D5	IC28.8 (SW4-7 = ON) IC45.5 (SW4-6 = ON)	-	CN9.20	-	-
			M2_WP	**IC28.8 (SW4-7 = ON) IC45.6 (SW4-6 = OFF)**	**-**	**JA5-A.23**	**-**	**-**
			BSC_D05	IC28.9 (SW4-7 = OFF)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
P21_5_ TRACE_D4_ BSC_D04	C7	P21_5	TRACE_D4	IC28.50 (SW4-7 = ON) IC45.53 (SW4-6 = ON)	-	CN9.22	-	-
			M2_VP	IC28.50 (SW4-7 = ON) IC45.52 (SW4-6 = OFF) SW11-6 = ON	SW11-7 = OFF	JA5-A.21	-	-
			P21_5	IC28.50 (SW4-7 = ON) IC45.52 (SW4-6 = OFF) SW11-7 = ON	SW11-6 = OFF	CN1.5	-	-
			BSC_D04	IC28.49 (SW4-7 = OFF)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-

Table 6-9: External Emulator Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D3_ BSC_D03	E7	P21_4	**TRACE_D3_ BSC_D03**	**-**	**-**	**CN3.16**	**-**	**-**
			TRACE_D3	IC28.5 (SW4-7 = ON) IC45.2 (SW4-6 = ON)	-	CN9.24	-	-
			M2_UN	**IC28.5 (SW4-7 = ON) IC45.3 (SW4-6 = OFF)**	**-**	**JA5-A.20**	**-**	**-**
			BSC_D03	IC28.6 (SW4-7 = OFF)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
TRACE_D2_ BSC_D02	A8	P21_3	**TRACE_D2_ BSC_D02**	**-**	**-**	**CN3.15**	**-**	**-**
			TRACE_D2	IC28.53 (SW4-7 = ON) IC45.11 (SW4-6 = ON)	-	CN9.26	-	-
			RS485_TX	**IC28.53 (SW4-7 = ON) IC45.12 (SW4-6 = OFF)**	**-**	**IC27.6**	**-**	**-**
			BSC_D02	IC28.52 (SW4-7 = OFF)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-
TRACE_D1_ BSC_D01	C8	P21_2	**TRACE_D1_ BSC_D01**	**-**	**-**	**CN3.18**	**-**	**-**
			TRACE_D1	IC28.2 (SW4-7 = ON) IC45.56 (SW4-6 = ON)	-	CN9.28	-	-
			M2_UP	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-4 = ON	SW11-5 = OFF	JA5-A.19	-	-
			RS485_RX	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-5 = ON	SW11-4 = OFF	IC27.3	-	-
			BSC_D01	IC28.3 (SW4-7 = OFF)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
CS_ TRACE_D0_ BSC_D00_ HSPI_INT#-B	B8	P21_1	**CS_TRACE_ D0_BSC_D00**	**CN25 (short 1-2)**	**-**	**CN3.17**	**-**	**-**
			TRACE_D0	CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.42 (SW4-6 = ON)	-	CN9.38	-	-
			CS	**CN25 (Short 1-2) IC28.56 (SW4-7 = ON) IC45.41 (SW4-6 = OFF)**	**-**	**J26.1**	**-**	**-**
						J21.3	**-**	**-**
			BSC_D00	CN25 (short 1-2) IC28.55 (SW4-7 = OFF)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			HSPI_INT#-B	CN25 (short 2-3)	-	CN4.13	-	-

Table 6-10 and **Table 6-11** below details the function of the switches associated with the External Emulator.

Table 6-10: External Emulator Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-11: External Emulator Configuration Switch Settings (2)

SW4-6	Explanation
ON	Enables the trace signal.
OFF	**Enables signals other than the trace signal. (Motor, RS485, etc)**

Table 6-12 below details the function of jumpers associated with the External Emulator.

Table 6-12: External Emulator Configuration Jumper Settings

Reference	Jumper Position	Explanation
J9	Short	Enable the External Emulator.
	Open	**Enable the J-Link® OB.**
CN25	**Short 1-2**	**Enable other signals. (Trace, SPI, External Bus)**
	Short 2-3	Enable the SHOST signal.

6.4.2 J-Link® OB

Table 6-13 below details the function of the option links associated with J-Link® OB Configuration.

Table 6-13: J-Link® OB Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TMS	F5	P02_6	**TMS**	-	-	**J20.2**	-	-
						CN9.17	-	-
						J13.2	-	-
						U7.30	**R35**	-
TCK	F1	P02_7	**TCK**	-	-	**J20.4**	-	-
						CN9.15	-	-
						J13.4	-	-
						U7.40	**R23**	-
TDO	F4	P02_4	**TDO**	-	-	**J20.6**	-	-
						CN9.11	-	-
						J13.6	-	-
						U7.23	-	-
TDI	F2	P02_5	**TDI**	-	-	**J20.8**	-	-
						CN9.19	-	-
						J13.8	-	-
						U7.17	-	-
TRST#	E2	-	**POWER_RESET#**	-	-	**IC4.2**	-	-
						IC38.11	-	-
			TRST_OUT#	-	-	**J20.16**	-	-
						CN9.21	-	-
RESET#	P6	-	**POWER_RESET#**	-	-	**J20.10**	-	-
						CN9.9	-	-
			RESET_SW#	-	-	**S3**	-	-
						U7.28	-	-
						J13.10	-	-
						J20.10	-	-
						CN9.9	-	-

Table 6-14 below details the function of jumpers associated with the J-Link® OB.

Table 6-14: J-Link® OB Configuration Jumper Settings

Reference	Jumper Position	Explanation
J9	Short	Enable the External Emulator.
	Open	**Enable the J-Link® OB.**

6.5 Power Supply Configuration

Table 6-15 below details the function of the option links associated with Power Supply Configuration.

Table 6-15: Power Supply Configuration Option Links

Reference	Explanation	Fit	DNF
5.0V	**Connect 5V Power rail to 5.0V.**	**-**	**-**
CON_5V	**Connect 5V Power rail to CON_5V.**	**R133**	**-**
3.3V	**Connect 3.3V Power rail to 3.3V.**	**-**	**-**
CON_3V3	**Connect 3.3V Power rail to CON_3V3.**	**R134**	**-**
+3V3JLOB	**Connect 3.3V Power rail to +3V3JLOB.**	**E4**	**-**
1.8V	**Connect 1.8V Power rail to 1.8V.**	**-**	**-**
VCC11_RZCORE	**Connect 1.1V Power rail to VCC11_RZCORE .**	**-**	**-**
ETH_VDD10	**Connect 1.0V Power rail to ETH_VDD10.**	**-**	**-**
ETH_VDD25	**Connect 2.5V Power rail to ETH_VDD25.**	**-**	**-**
VCC1833_0	**Connect 1.8V Power rail to VCC1833_0.**	**-**	**-**
VCC1833_1	**Connect 1.8V Power rail to VCC1833_1.**	**-**	**-**
VCC1833_2	Connect 3.3V Power rail to VCC1833_2.	CN17 (Short 1-2)	-
	Connect 1.8V Power rail to VCC1833_2.	**CN17 (Short 2-3)**	**-**
VCC1833_3	Connect 3.3V Power rail to VCC1833_3.	CN24 (Short 1-2)	-
	Connect 1.8V Power rail to VCC1833_3.	**CN24 (Short 2-3)**	**-**
VCC1833_4	**Connect 3.3V Power rail to VCC1833_4.**	**-**	**-**
VCC18_PLL0	**Connect 1.8V Power rail to VCC18_PLL0.**	**-**	**-**
VCC18_PLL1	**Connect 1.8V Power rail to VCC18_PLL1.**	**-**	**-**
VCC18_TSU	**Connect 1.8V Power rail to VCC18_TSU.**	**-**	**-**
VCC18_ADC0	**Connect 1.8V Power rail to VCC18_ADC0.**	**R158**	**-**
VCC18_ADC1	**Connect 1.8V Power rail to VCC18_ADC1.**	**R159**	**-**

Table 6-16 below details the function of jumpers associated with the Power Supply.

Table 6-16: Power Supply Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using Ethernet)**
CN24	Short 1-2	Connect 3.3V Power rail to VCC1833_3. (When using external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_3. (When using XSPI)**

6.6 Clock Configuration

Table 6-17 below details the function of the option links associated with Clock Configuration.

Table 6-17: Clock Configuration Option Links

Reference	Explanation	Solder, FIT	De-solder, DNF
XIN, XOUT	Connect 25MHz crystal (X3) to RZ/N2L.	R242, R244	R286
EXTCLKIN	**Connect 25MHz crystal (X1) via a clock generator (IC24) to RZ/N2L.**	**R160, R245**	**E46, R246**
	Connect JA2-A.2 to X1.	E46	R245, R246

6.7 Analog Power & ADC Configuration

Table 6-18 below details the function of the option links associated with Analog Power & ADC Configuration.

Table 6-18: Analog Power & ADC Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ADC_AN000	B13	-	**ADC_AN000**	-	-	**JA1-A.9**	-	-
ADC_AN001	C12	-	**ADC_AN001**	-	-	**JA1-A.10**	-	-
ADC_AN002	B14	-	**ADC_AN002**	-	-	**JA1-A.11**	-	-
ADC_AN003	C13	-	**ADC_AN003**	-	-	**JA1-A.12**	-	-
ADC_AN100	B12	-	**ADC_AN100**	**R197**	-	**J21.1**	-	-
ADC_AN101	A14	-	**ADC_AN101**	**R200**	-	**J28.1**	-	-
ADC_AN102	B11	-	**ADC_AN102**	**R201**	-	**J28.2**	-	-
ADC_AN103	A13	-	**ADC_AN103**	-	-	**R5**	-	-
ADC_AN104	A12	-	**ADC_AN104**	-	-	**JA5-A.1**	-	-
ADC_AN105	B10	-	**ADC_AN105**	-	-	**JA5-A.2**	-	-
ADC_AN106	A11	-	**ADC_AN106**	-	-	**JA5-A.3**	-	-
ADC_AN107	C9	-	**ADC_AN107**	-	-	**JA5-A.4**	-	-
VCC18_ADC0	E11	-	**VCC18_ADC0**	**L11**	**R140**	-	-	-
		-	CON_AVCC	R140	-	-	-	-
VCC18_ADC1	E9	-	**VCC18_ADC1**	**L12**	-	-	-	-
VREFH0	C11	-	**VCC18_ADC0**	**L11, R158**	**R143, R140**	-	-	-
			CON_AVREF	R143	R158, R140	-	-	-
			CON_AVCC	R140, R158	R143	-		
VREFH1	C10	-	**VCC18_ADC1**	**L12, R159**	-	-	-	-

6.8 External BUS & NOR Flash Configuration

Table 6-19 to **Table 6-25** below details the function of the option links associated with External BUS & NOR Flash Configuration.

Table 6-19: External BUS & NOR Flash Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
XSPI0_IO3_ BSC_A25	K15	P15_2	**XSPI0_IO3**	**IC12.8 (Short 2-3 of CN24)**	-	**IC19.D4**	-	-
						IC21.1	-	-
						IC41.D4	-	-
			BSC_A25	IC12.9 (Short 1-2 of CN24)		IC22.F8	-	-
XSPI0_IO2_ BSC_A24	K14	P15_1	**XSPI0_IO2**	**IC12.50 (Short 2-3 of CN24)**	-	**IC19.C4**	-	-
						IC21.9	-	-
						IC41.C4	-	-
			BSC_A24	IC12.49 (Short 1-2 of CN24)	-	IC22.B5	-	-
XSPI0_IO1_ BSC_A23	L11	P15_0	**XSPI0_IO1**	**IC12.5 (Short 2-3 of CN24)**	-	**IC19.D2**	-	-
						IC21.8	-	-
						IC41.D2	-	-
			BSC_A23	IC12.6 (Short 1-2 of CN24)	-	IC22.D8	-	-
XSPI0_IO0_ BSC_A22	M15	P14_7	**XSPI0_IO0**	**IC12.53 (Short 2-3 of CN24)**	-	**IC19.D3**	-	-
						IC21.15	-	-
						IC41.D3	-	-
			BSC_A22	IC12.52 (Short 1-2 of CN24)	-	IC22.C8	-	-
						JA3-A.43	-	-
XSPI0_CKP_ BSC_A21	K13	P14_6	**XSPI0_CKP**	**IC12.2 (Short 2-3 of CN24)**	-	**IC19.B2**	-	-
						IC21.16	-	-
						IC41.B2	-	-
			BSC_A21	IC12.3 (Short 1-2 of CN24)	-	IC22.C5	-	-
						JA3-A.42	-	-
P01_6_BSC_A20	D2	P01_6	**P01_6**	**IC28.33 (SW4-7 = ON)**	-	**CN1.1**	-	-
						JA2-A.23	-	-
			BSC_A20	IC28.32 (SW4-7 = OFF)	-	IC22.B6	-	-
						JA3-A.41	-	-
P01_7_ CAN_RX_ ADTRG_ BSC_A19	C1	P01_7	CAN_RX	IC28.22 (SW4-7 = ON), SW11-8=ON	SW11-10=OFF, SW11-9=OFF	U10.4	-	-
			ADTRG	IC28.22 (SW4-7 = ON), SW11-9=ON	SW11-10=OFF, SW11-8=OFF	JA1-A.8	-	-
			P01_7	IC28.22 (SW4-7 = ON), SW11-10=ON	SW11-9=OFF, SW11-8=OFF	CN1.2	-	-
			BSC_A19	IC28.23 (SW4-7 = OFF)	-	IC22.C3	-	-
						JA3-A.40	-	-
P02_0_ CAN1_TX_ BSC_A18	E3	P02_0	**P02_0_ CAN1_TX**	**IC28.36 (SW4-7 = ON)**	-	**CN1.3**	-	-
						JA5-A.5	-	-
			BSC_A18	IC28.35 (SW4-7 = OFF)	-	IC22.D3	-	-
						JA3-A.39	-	-
BSC_A17	D1	P02_1	**BSC_A17**	-	-	**IC22.E8**	-	-
						CN1.12		
						JA3-A.38	-	-

Table 6-20: BUS & External NOR Flash Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P02_2_ CAN_TX_ IRQ4_ BSC_A16	F3	P02_2	CAN_TX	IC29.25 (SW4-7 = ON), SW8-8 = ON	SW8-10 = OFF, SW8-9 = OFF	U10.1	-	-
			IRQ4	IC29.25 (SW4-7 = ON), SW8-9 = ON	SW8-10 = OFF, SW8-8 = OFF	JA5-A.9	-	-
			P02_2	IC29.25 (SW4-7 = ON), SW8-10 = ON	SW8-9 = OFF, SW8-8 = OFF	CN1.4	-	-
			BSC_A16	IC29.26 (SW4-7 = OFF)	-	IC22.B8	-	-
						JA3-A.37	-	-
P02_3_ CAN1_RX_ BSC_A15	E1	P02_3	**P02_3_ CAN1_RX**	**IC29.33 (SW4-7 = ON)**	-	**CN1.6**	-	-
						JA5-A.6	-	-
			BSC_A15	IC29.32 (SW4-7 = OFF)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-
LED4_BSC_A14	G3	P03_0	**LED4**	**IC29.22 (SW4-7 = ON)**	-	**ETH_LED4.A**	**R12**	-
			BSC_A14	IC29.23 (SW4-7 = OFF)	-	IC22.C7	-	-
						IC23.20	-	-
						JA3-A.15	-	-
ETH2_RXDV_ BSC_A13	D5	P00_1	**ETH2_RXDV**	**IC46.42 (Short 2-3 of CN17)**	-	**IC16.30**	**R107**	-
			BSC_A13	IC46.41 (Short 1-2 of CN17)	-	IC22.B7	-	-
						IC23.36	-	-
						JA3-A.14	-	-
PMOD3A_INT_ BSC_A12	G1	P03_5	**PMOD3A_INT_ BSC_A12**	**-**	-	**CN3.13**	-	-
			PMOD3A_INT	**IC29.19 (SW4-7 = ON)**	-	**J25.7**	-	-
			BSC_A12	IC29.20 (SW4-7 = OFF)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
PMOD2A_INT_ BSC_A11	G4	P03_6	**PMOD2A_INT_ BSC_A11**	**-**	-	**CN3.14**	-	-
			PMOD2A_INT	**IC29.39 (SW4-7 = ON)**	-	**J26.7**	-	-
			BSC_A11	IC29.38 (SW4-7 = OFF)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
MIKROBUS_INT_ BSC_A10	G5	P03_7	**MIKROBUS_ INT**	**IC29.16 (SW4-7 = ON)**	-	**J22.2**	-	-
			BSC_A10	IC29.17 (SW4-7 = OFF)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
PMOD2A_ RESET_BSC_A09	H1	P04_0	**PMOD2A_ RESET**	**IC29.42 (SW4-7 = ON)**	-	**J26.8**	-	-
			BSC_A09	IC29.41 (SW4-7 = OFF)	-	IC22.A6	-	-
						IC23.33	-	-
						JA3-A.10	-	-
LED6_BSC_A08	H4	P04_4	**LED6**	**IC29.11 (SW4-7 = ON)**	-	**ETH_LED6.A**	**R14**	-
			BSC_A08	IC29.12 (SW4-7 = OFF)	-	IC22.A2	-	-
						IC23.32	-	-
						JA3-A.9	-	-

Table 6-21: External BUS & NOR Flash Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
BSC_A07_MD0	H3	P04_5	**BSC_A07_MD0**	**-**	**-**	**IC14.4**	**-**	**-**
			BSC_A07	IC29.46 (SW4-7 = OFF)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-
PMOD2A_CS3_ GPIO_BSC_A06_ MD1	H5	P04_6	**PMOD2A_ CS3_GPIO_ BSC_A06_MD1**	**-**	**-**	**IC14.7**	**-**	**-**
			PMOD2A_ CS3_GPIO	**IC29.8 (SW4-7 = ON)**	**-**	**J26.10**	**-**	**-**
			BSC_A06	IC29.9 (SW4-7 = OFF)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-
PMOD2A_CS2_ GPIO_BSC_A05_ MD2	J1	P04_7	**PMOD2A_ CS2_GPIO_ BSC_A05_MD2**	**-**	**-**	**IC14.9**	**-**	**-**
			PMOD2A_ CS2_GPIO	**IC29.50 (SW4-7 = ON)**	**-**	**J26.9**	**-**	**-**
			BSC_A05	IC29.49 (SW4-7 = OFF)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
LED7_BSC_A04	J5	P05_0	**LED7**	**IC29.5 (SW4-7 = ON)**	**-**	**ETH_LED7.A**	**R15**	**-**
			BSC_A04	IC29.6 (SW4-7 = OFF)	-	IC22.B1	-	-
						IC23.26	-	-
						JA3-A.5	-	-
P05_1_BSC_A03	J2	P05_1	BSC_A03	IC29.52 (SW4-7 = OFF)	-	IC22.C1	-	-
						IC23.25	-	-
						JA3-A.4	-	-
SCL_BSC_A02	J4	P05_2	**SCL**	**IC29.2 (SW4-7 = ON)**	**-**	**J22.5**	**-**	**-**
						J27.1	**-**	**E2**
						J30.4	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	E2	E23
			BSC_A02	IC29.3 (SW4-7 = OFF)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
SDA_BSC_A01	J3	P05_3	**SDA**	**IC29.56 (SW4-7 = ON)**	**-**	**J22.6**	**-**	**-**
						J27.2	**-**	**E3**
						J30.3	**-**	**-**
						CN1.18	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	E3	E24
			BSC_A01	IC29.55 (SW4-7 = OFF)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
ETH2_RXD3_ BSC_D15	C4	P00_0	**ETH2_RXD3**	**IC46.36 (Short 2-3 of CN17)**	**-**	**IC16.25**	**R111**	**-**
			BSC_D15	IC46.35 (Short 1-2 of CN17)	-	IC22.F7	-	-
						IC23.53	-	-
						JA3-A.36	-	-
ETH2_RXD2_ BSC_D14_MDAT5	C5	P24_2	**ETH2_RXD2**	**IC46.19 (Short 2-3 of CN17)**	**-**	**IC16.26**	**R110**	**-**
			BSC_D14	IC46.20 (Short 1-2 of CN17), R274	R275	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			MDAT5	IC46.20 (Short 1-2 of CN17), R275	R274	CN3.4	-	-

Table 6-22: External BUS & NOR Flash Configuration Option Links (4)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_RXCLK_ BSC_D13_MCLK5	B5	P24_1	**ETH2_RXCLK**	**IC46.33 (Short 2-3 of CN17)**	**-**	**IC16.32**	**R106**	**-**
			BSC_D13	IC46.32 (Short 1-2 of CN17), R268	R270	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			MCLK5	IC46.32 (Short 1-2 of CN17), R270	R268	CN3.3	-	-
ETH2_RXD1_ BSC_D12_MDAT4	A5	P24_0	**ETH2_RXD1**	**IC46.39 (Short 2-3 of CN17)**	**-**	**IC16.27**	**R109**	**-**
			BSC_D12	IC46.38 (Short 1-2 of CN17), R276	R277	IC22.G6	-	-
						IC23.48	-	-
						JA3-A.33	-	-
			MDAT4	IC46.38 (Short 1-2 of CN17), R277	R276	CN3.6	-	-
ETH2_RXD0_ BSC_D11_MCLK4	D6	P23_7	**ETH2_RXD0**	**IC46.16 (Short 2-3 of CN17)**	**-**	**IC16.29**	**R108**	**-**
			BSC_D11	IC46.17 (Short 1-2 of CN17), R272	R273	IC22.H4	-	-
						IC23.47	-	-
						JA3-A.32	-	-
			MCLK4	IC46.17 (Short 1-2 of CN17), R273	R272	CN3.5	-	-
LED_ORANGE_ BSC_D10	B6	P22_3	**LED_ORANGE**	**IC28.39 (SW4-7 = ON)**	**-**	**LED1.A**	**R44**	**-**
			BSC_D10	IC28.38 (SW4-7 = OFF)	-	IC22.G3	-	-
						IC23.45	-	-
						JA3-A.31	-	-
TRACE_CLK_ BSC_D09	C6	P22_2	TRACE_CLK	IC28.16 (SW4-7 = ON), IC45.16 (SW4-6 = ON)	-	CN9.6	-	-
			BSC_D09	IC28.17 (SW4-7 = OFF)	-	IC22.F3	-	-
						IC23.44	-	-
						JA3-A.30	-	-
LED5_BSC_D08	A6	P22_1	**LED5**	**IC28.42 (SW4-7 = ON), SW8-4 = ON**	**SW8-5 = OFF**	**ETH_LED5.A**	**R13**	**-**
			M2_POE	IC28.42 (SW4-7 = ON), SW8-5 = ON	SW8-4 = OFF	JA5-A.16	-	-
			BSC_D08	IC28.41 (SW4-7 = OFF)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-

Table 6-23: External BUS & NOR Flash Configuration Option Links (5)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D7_ BSC_D07	A7	P22_0	**TRACE_D7_ BSC_D07**	**-**	**-**	**CN3.8**	**-**	**-**
			TRACE_D7	IC28.11 (SW4-7 = ON), IC45.8 (SW4-6 = ON)	-	CN9.16	-	-
			M2_VN	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-6 = ON	SW8-7 = OFF	JA5-A.22	-	-
			RS485_DE	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-7 = ON	SW8-6 = OFF	IC27.5	-	-
			BSC_D07	IC28.12 (SW4-7 = OFF)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
TRACE_D6_ BSC_D06	B7	P21_7	**TRACE_D6_ BSC_D06**	**-**	**-**	**CN3.7**	**-**	**-**
			TRACE_D6	IC28.47 (SW4-7 = ON), IC45.50 (SW4-6 = ON)	-	CN9.18	-	-
			M2_WN	**IC28.47 (SW4-7 = ON), IC45.49 (SW4-6 = OFF)**	**-**	**JA5-A.24**	**-**	**-**
			BSC_D06	IC28.46 (SW4-7 = OFF)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-
TRACE_D5_ BSC_D05	D7	P21_6	TRACE_D5	IC28.8 (SW4-7 = ON), IC45.5 (SW4-6 = ON)	-	CN9.20	-	-
			M2_WP	**IC28.8 (SW4-7 = ON), IC45.6 (SW4-6 = OFF)**	**-**	**JA5-A.23**	**-**	**-**
			BSC_D05	IC28.9 (SW4-7 = OFF)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
P21_5_ TRACE_D4_ BSC_D04	C7	P21_5	TRACE_D4	IC28.50 (SW4-7 = ON), IC45.53 (SW4-6 = ON)	-	CN9.22	-	-
			M2_VP	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-6 = ON	SW11-7 = OFF	JA5-A.21	-	-
			P21_5	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-7 = ON	SW11-6 = OFF	CN1.5	-	-
			BSC_D04	IC28.49 (SW4-7 = OFF)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-

Table 6-24: External BUS & NOR Flash Configuration Option Links (6)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D3_ BSC_D03	E7	P21_4	**TRACE_D3_ BSC_D03**	**-**	**-**	**CN3.16**	**-**	**-**
			TRACE_D3	IC28.5 (SW4-7 = ON), IC45.2 (SW4-6 = ON)	-	CN9.24	-	-
			M2_UN	**IC28.5 (SW4-7 = ON), IC45.3 (SW4-6 = OFF)**	**-**	**JA5-A.20**	**-**	**-**
			BSC_D03	IC28.6 (SW4-7 = OFF)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
TRACE_D2_ BSC_D02	A8	P21_3	**TRACE_D2_ BSC_D02**	**-**	**-**	**CN3.15**	**-**	**-**
			TRACE_D2	IC28.53 (SW4-7 = ON), IC45.11 (SW4-6 = ON)	-	CN9.26	-	-
			RS485_TX	**IC28.53 (SW4-7 = ON), IC45.12 (SW4-6 = OFF)**	**-**	**IC27.6**	**-**	**-**
			BSC_D02	IC28.52 (SW4-7 = OFF)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-
TRACE_D1_ BSC_D01	C8	P21_2	**TRACE_D1_ BSC_D01**	**-**	**-**	**CN3.18**	**-**	**-**
			TRACE_D1	IC28.2 (SW4-7 = ON), IC45.56 (SW4-6 = ON)	-	CN9.28	-	-
			M2_UP	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-4 = ON	SW11-5 = OFF	JA5-A.19	-	-
			RS485_RX	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-5 = ON	SW11-4 = OFF	IC27.3	-	-
			BSC_D01	IC28.3 (SW4-7 = OFF)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
CS_ TRACE_D0_ BSC_D00_ HSPI_INT#-B	B8	P21_1	**CS_TRACE_ D0_BSC_D00**	**CN25 (short 1-2)**	**-**	**CN3.17**	**-**	**-**
			TRACE_D0	CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.42 (SW4-6 = ON)	-	CN9.38	-	-
			CS	**CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.41 (SW4-6 = OFF)**	**-**	**J26.1**	**-**	**-**
						J21.3	**-**	**-**
			BSC_D00	CN25 (short 1-2) IC28.55 (SW4-7 = OFF)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			HSPI_INT#-B	CN25 (short 2-3)	-	CN4.13	-	-

Table 6-25: External BUS & NOR Flash Configuration Option Links (7)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_LINK_ BSC_CS0#	B4	P00_5	**ETH2_LINK**	**IC46.22 (Short 2-3 of CN17)**	**-**	**IC16.59**	**-**	**-**
			BSC_CS0#	IC46.23 (Short 1-2 of CN17)	-	IC22.F1	-	-
ETH2_TXEN_ BSC_RD#	A3	P00_2	**ETH2_TXEN**	**R83, IC46.56 (Short 2-3 of CN17)**	**-**	**IC16.33**	**-**	**-**
			BSC_RD#	R83, IC46.55 (Short 1-2 of CN17)	-	IC22.F2	-	-
						JA3-A.25	-	-
ETH2_TXD0_ BSC_DQMLL	B1	P01_5	**ETH2_TXD0**	**R89, IC46.5 (Short 2-3 of CN17)**	**-**	**IC16.38**	**-**	**-**
			BSC_DQMLL_ WE0#	R89, IC46.6 (Short 1-2 of CN17)	-	IC22.A5	-	-
						IC23.15	-	-
						JA5-A.48	-	-

Table 6-26 below details the function of the switches associated with the NOR Flash.

Table 6-26: External BUS & NOR Flash Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-27 below details the function of jumpers associated with the NOR Flash.

Table 6-27: External BUS & NOR Flash Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)*1
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)*2**
CN24	Short 1-2	Connect 3.3V Power rail to VCC1833_3. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_3. (When using the XSPI0)**

*1: When using on the external bus (SDRAM and NOR Flash), use the Ethernet switch (CN20-CN22) setting at 2-3.
*2: BUS (SDRAM and NOR Flash) and Ethernet / Switch / ESC channel 2 cannot be used at the same time.

6.9 External BUS & SDRAM Configuration

Table 6-28 to **Table 6-33** below details the function of the option links associated with External BUS & SDRAM Configuration.

Table 6-28: External BUS & SDRAM Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P02_3_ CAN1_RX_ BSC_A15	E1	P02_3	**P02_3_ CAN1_RX**	**IC29.33 (SW4-7 = ON)**	-	**CN1.6**	-	-
						JA5-A.6	-	-
			BSC_A15	IC29.32 (SW4-7 = OFF)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-
LED4_BSC_A14	G3	P03_0	**LED4**	**IC29.22 (SW4-7 = ON)**	-	**ETH_LED4.A**	**R12**	-
			BSC_A14	IC29.23 (SW4-7 = OFF)	-	IC22.C7	-	-
						IC23.20	-	-
						JA3-A.15	-	-
ETH2_RXDV_ BSC_A13	D5	P00_1	**ETH2_RXDV**	**IC46.42 (Short 2-3 of CN17)**	-	**IC16.30**	**R107**	-
			BSC_A13	IC46.41 (Short 1-2 of CN17)	-	IC22.B7	-	-
						IC23.36	-	-
						JA3-A.14	-	-
PMOD3A_INT_ BSC_A12	G1	P03_5	**PMOD3A_INT_ BSC_A12**	-	-	**CN3.13**		
			PMOD3A_INT	**IC29.19 (SW4-7 = ON)**	-	**J25.7**	-	-
			BSC_A12	IC29.20 (SW4-7 = OFF)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
PMOD2A_INT_ BSC_A11	G4	P03_6	**PMOD2A_ INT_BSC_A11**	-	-	**CN3.14**	-	-
			PMOD2A_INT	**IC29.39 (SW4-7 = ON)**	-	**J26.7**	-	-
			BSC_A11	IC29.38 (SW4-7 = OFF)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
MIKROBUS_INT_ BSC_A10	G5	P03_7	**MIKROBUS_ INT**	**IC29.16 (SW4-7 = ON)**	-	**J22.2**	-	-
			BSC_A10	IC29.17 (SW4-7 = OFF)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
PMOD2A_ RESET_BSC_A09	H1	P04_0	**PMOD2A_ RESET**	**IC29.42 (SW4-7 = ON)**	-	**J26.8**	-	-
			BSC_A09	IC29.41 (SW4-7 = OFF)	-	IC22.A6	-	-
						IC23.33	-	-
						JA3-A.10	-	-
LED6_BSC_A08	H4	P04_4	**LED6**	**IC29.11 (SW4-7 = ON)**	-	**ETH_LED6.A**	**R14**	-
			BSC_A08	IC29.12 (SW4-7 = OFF)	-	IC22.A2	-	-
						IC23.32	-	-
						JA3-A.9	-	-
BSC_A07_MD0	H3	P04_5	**BSC_A07_MD0**	-	-	**IC14.4**	-	-
			BSC_A07	IC29.46 (SW4-7 = OFF)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-

Table 6-29: External BUS & SDRAM Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD2A_CS3_ GPIO_BSC_A06_ MD1	H5	P04_6	**PMOD2A_ CS3_GPIO_ BSC_A06_MD1**	**-**	**-**	**IC14.7**	**-**	**-**
			PMOD2A_ CS3_GPIO	**IC29.8 (SW4-7 = ON)**	**-**	**J26.10**	**-**	**-**
			BSC_A06	IC29.9 (SW4-7 = OFF)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-
PMOD2A_CS2_ GPIO_BSC_A05_ MD2	J1	P04_7	**PMOD2A_ CS2_GPIO_ BSC_A05_MD2**	**-**	**-**	**IC14.9**	**-**	**-**
			PMOD2A_ CS2_GPIO	**IC29.50 (SW4-7 = ON)**	**-**	**J26.9**	**-**	**-**
			BSC_A05	IC29.49 (SW4-7 = OFF)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
LED7_BSC_A04	J5	P05_0	**LED7**	**IC29.5 (SW4-7 = ON)**	**-**	**ETH_LED7.A**	**R15**	**-**
			BSC_A04	IC29.6 (SW4-7 = OFF)	-	IC22.B1	-	-
						IC23.26	-	-
						JA3-A.5	-	-
P05_1_BSC_A03	J2	P05_1	BSC_A03	IC29.52 (SW4-7 = OFF)	-	IC22.C1	-	-
						IC23.25	-	-
						JA3-A.4	-	-
SCL_BSC_A02	J4	P05_2	**SCL**	**IC29.2 (SW4-7 = ON)**	**-**	**J22.5**	**-**	**-**
						J27.1	**-**	**E2**
						J30.4	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	E2	E23
			BSC_A02	IC29.3 (SW4-7 = OFF)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
SDA_BSC_A01	J3	P05_3	**SDA**	**IC29.56 (SW4-7 = ON)**	**-**	**J22.6**	**-**	**-**
						J27.2	**-**	**E3**
						J30.3	**-**	**-**
						CN1.18	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	E3	E24
			BSC_A01	IC29.55 (SW4-7 = OFF)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
ETH2_RXD3_ BSC_D15	C4	P00_0	**ETH2_RXD3**	**IC46.36 (Short 2-3 of CN17)**	**-**	**IC16.25**	**R111**	**-**
			BSC_D15	IC46.35 (Short 1-2 of CN17)	-	IC22.F7	-	-
						IC23.53	-	-
						JA3-A.36	-	-
ETH2_RXD2_ BSC_D14_MDAT5	C5	P24_2	**ETH2_RXD2**	**IC46.19 (Short 2-3 of CN17)**	**-**	**IC16.26**	**R110**	**-**
			BSC_D14	IC46.20 (Short 1-2 of CN17), R274	R275	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			MDAT5	IC46.20 (Short 1-2 of CN17), R275	R274	CN3.4	-	-

Table 6-30: External BUS & SDRAM Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_RXCLK_ BSC_D13_MCLK5	B5	P24_1	**ETH2_RXCLK**	**IC46.33 (Short 2-3 of CN17)**	**-**	**IC16.32**	**R106**	**-**
			BSC_D13	IC46.32 (Short 1-2 of CN17), R268	R270	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			MCLK5	IC46.32 (Short 1-2 of CN17), R270	R268	CN3.3	-	-
ETH2_RXD1_ BSC_D12_MDAT4	A5	P24_0	**ETH2_RXD1**	**IC46.39 (Short 2-3 of CN17)**	**-**	**IC16.27**	**R109**	**-**
			BSC_D12	IC46.38 (Short 1-2 of CN17), R276	R277	IC22.G6	-	-
						IC23.48	-	-
						JA3-A.33	-	-
			MDAT4	IC46.38 (Short 1-2 of CN17), R277	R276	CN3.6	-	-
ETH2_RXD0_ BSC_D11_MCLK4	D6	P23_7	**ETH2_RXD0**	**IC46.16 (Short 2-3 of CN17)**	**-**	**IC16.29**	**R108**	**-**
			BSC_D11	IC46.17 (Short 1-2 of CN17), R272	R273	IC22.H4	-	-
						IC23.47	-	-
						JA3-A.32	-	-
			MCLK4	IC46.17 (Short 1-2 of CN17), R273	R272	CN3.5	-	-
LED_ORANGE_ BSC_D10	B6	P22_3	**LED_ORANGE**	**IC28.39 (SW4-7 = ON)**	**-**	**LED1.A**	**R44**	**-**
			BSC_D10	IC28.38 (SW4-7 = OFF)	-	IC22.G3	-	-
						IC23.45	-	-
						JA3-A.31	-	-
TRACE_CLK_ BSC_D09	C6	P22_2	TRACE_CLK	IC28.16 (SW4-7 = ON), IC45.16 (SW4-6 = ON)	-	CN9.6	-	-
			BSC_D09	IC28.17 (SW4-7 = OFF)	-	IC22.F3	-	-
						IC23.44	-	-
						JA3-A.30	-	-
LED5_BSC_D08	A6	P22_1	**LED5**	**IC28.42 (SW4-7 = ON), SW8-4 = ON**	**SW8-5 = OFF**	**ETH_LED5.A**	**R13**	**-**
			M2_POE	IC28.42 (SW4-7 = ON), SW8-5 = ON	SW8-4 = OFF	JA5-A.16	-	-
			BSC_D08	IC28.41 (SW4-7 = OFF)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-

Table 6-31: External BUS & SDRAM Configuration Option Links (4)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D7_ BSC_D07	A7	P22_0	**TRACE_D7_ BSC_D07**	**-**	**-**	**CN3.8**	**-**	**-**
			TRACE_D7	IC28.11 (SW4-7 = ON), IC45.8 (SW4-6 = ON)	-	CN9.16	-	-
			M2_VN	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-6 = ON	SW8-7 = OFF	JA5-A.22	-	-
			RS485_DE	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-7 = ON	SW8-6 = OFF	IC27.5	-	-
			BSC_D07	IC28.12 (SW4-7 = OFF)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
TRACE_D6_ BSC_D06	B7	P21_7	**TRACE_D6_ BSC_D06**	**-**	**-**	**CN3.7**	**-**	**-**
			TRACE_D6	IC28.47 (SW4-7 = ON), IC45.50 (SW4-6 = ON)	-	CN9.18	-	-
			M2_WN	**IC28.47 (SW4-7 = ON), IC45.49 (SW4-6 = OFF)**	**-**	**JA5-A.24**	**-**	**-**
			BSC_D06	IC28.46 (SW4-7 = OFF)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-
TRACE_D5_ BSC_D05	D7	P21_6	TRACE_D5	IC28.8 (SW4-7 = ON), IC45.5 (SW4-6 = ON)	-	CN9.20	-	-
			M2_WP	**IC28.8 (SW4-7 = ON), IC45.6 (SW4-6 = OFF)**	**-**	**JA5-A.23**	**-**	**-**
			BSC_D05	IC28.9 (SW4-7 = OFF)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
P21_5_ TRACE_D4_ BSC_D04	C7	P21_5	TRACE_D4	IC28.50 (SW4-7 = ON), IC45.53 (SW4-6 = ON)	-	CN9.22	-	-
			M2_VP	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-6 = ON	SW11-7 = OFF	JA5-A.21	-	-
			P21_5	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-7 = ON	SW11-6 = OFF	CN1.5	-	-
			BSC_D04	IC28.49 (SW4-7 = OFF)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-

Table 6-32: External BUS & SDRAM Configuration Option Links (5)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D3_ BSC_D03	E7	P21_4	**TRACE_D3_ BSC_D03**	**-**	**-**	**CN3.16**	**-**	**-**
			TRACE_D3	IC28.5 (SW4-7 = ON), IC45.2 (SW4-6 = ON)	-	CN9.24	-	-
			M2_UN	**IC28.5 (SW4-7 = ON), IC45.3 (SW4-6 = OFF)**	**-**	**JA5-A.20**	**-**	**-**
			BSC_D03	IC28.6 (SW4-7 = OFF)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
TRACE_D2_ BSC_D02	A8	P21_3	**TRACE_D2_ BSC_D02**	**-**	**-**	**CN3.15**	**-**	**-**
			TRACE_D2	IC28.53 (SW4-7 = ON), IC45.11 (SW4-6 = ON)	-	CN9.26	-	-
			RS485_TX	**IC28.53 (SW4-7 = ON), IC45.12 (SW4-6 = OFF)**	**-**	**IC27.6**	**-**	**-**
			BSC_D02	IC28.52 (SW4-7 = OFF)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-
TRACE_D1_ BSC_D01	C8	P21_2	**TRACE_D1_ BSC_D01**	**-**	**-**	**CN3.18**	**-**	**-**
			TRACE_D1	IC28.2 (SW4-7 = ON), IC45.56 (SW4-6 = ON)	-	CN9.28	-	-
			M2_UP	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-4 = ON	SW11-5 = OFF	JA5-A.19	-	-
			RS485_RX	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-5 = ON	SW11-4 = OFF	IC27.3	-	-
			BSC_D01	IC28.3 (SW4-7 = OFF)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
CS_ TRACE_D0_ BSC_D00_ HSPI_INT#-B	B8	P21_1	**CS_TRACE_ D0_BSC_D00**	**CN25 (short 1-2)**	**-**	**CN3.17**	**-**	**-**
			TRACE_D0	CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.42 (SW4-6 = ON)	-	CN9.38	-	-
			CS	**CN25 (Short 1-2) IC28.56 (SW4-7 = ON) IC45.41 (SW4-6 = OFF)**	**-**	**J26.1**	**-**	**-**
						J21.3	**-**	**-**
			BSC_D00	CN25 (short 1-2) IC28.55 (SW4-7 = OFF)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			HSPI_INT#-B	CN25 (short 2-3)	-	CN4.13	-	-

Table 6-33: External BUS & SDRAM Configuration Option Links (6)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
XSPI0_CKN_ BSC_CS3#	J12	P14_5	**XSPI0_CKN**	**IC12.56 (Short 2-3 of CN24)**	**-**	**IC41.B1**	**-**	**-**
			BSC_CS2#_ CS3#	IC12.55 (Short 1-2 of CN24)	-	IC46.46	R343, R342	-
						IC23.19	R343	-
						JA3-A.28	R343	-
M1_VP_ BSC_RAS#	D4	P00_7	**M1_VP**	**IC28.19 (SW4-7 = ON)**	**-**	**JA2-A.15**	**-**	**-**
			BSC_RAS#	IC28.20 (SW4-7 = OFF)	-	IC23.18	-	-
						JA3-A.50	-	-
ETH2_MDIO_ M1_VN_ BSC_CAS#	A2	P01_0	ETH2_MDIO	IC46.2 (Short 2-3 of CN17), CN21 (short 2-3)	-	IC16.50	-	-
			BSC_CAS#_ M1_VN	IC46.3 (Short 1-2 of CN17)	-	IC23.17	-	-
						JA2-A.16	-	-
						JA3-A.49	-	-
ETH2_REFCLK_ BSC_WR#	B3	P00_3	**ETH2_ REFCLK_25**	**R84, IC46.53 (Short 2-3 of CN17) R114**	**R113**	**IC16.63**	**R339**	**R338**
			ETH2_REFCLK	R84, IC46.53 (Short 2-3 of CN17)	R113, R114	IC16.37	R338	R339
			BSC_WR#	R84, IC46.52 (Short 1-2 of CN17)	-	IC23.16	-	-
						JA3-A.26	-	-
ETH2_TXD1_ BSC_DQMLU	E4	P01_4	**ETH2_TXD1**	**R88, IC46.50 (Short 2-3 of CN17)**	**-**	**IC16.40**	**-**	**-**
			BSC_DQMLU	R88, IC46.49 (Short 1-2 of CN17)	-	IC23.39	-	-
						JA3-A.47	-	-
ETH2_TXD0_ BSC_DQMLL	B1	P01_5	**ETH2_TXD0**	**R89, IC46.5 (Short 2-3of CN17)**	**-**	**IC16.38**	**-**	**-**
			BSC_DQMLL_ WE0#	R89, IC46.6 (Short 1-2 of CN17)	-	IC22.A5	-	-
						IC23.15	-	-
						JA3-A.48	-	-
ETH2_MDC_ BSC_CKE	D3	P01_1	ETH2_MDC	IC46.11 (Short 2-3 of CN17), CN20 (short 2-3)	-	IC16.48	-	-
			BSC_CKE	IC46.12 (Short 1-2 of CN17)	-	IC23.37	-	-
						JA3-A.46	-	-
LED_RED1_ BSC_CKIO	H2	P04_1	**LED_RED1**	**IC29.36 (SW4-7 = ON)**	**-**	**LED2.A**	**R46**	**-**
			BSC_CKIO	IC29.35 (SW4-7 = OFF)	-	IC23.38	-	-
						JA3-A.44	-	-
ETH2_TXD3_MPU _BSC_CS2#	B2	P01_2	**ETH2_TXD3**	**R86, IC46.47 (Short 2-3 of CN17)**	**-**	**IC16.42**	**-**	**-**
			BSC_CS2#_ CS3#	R86, IC46.46 (Short 1-2 of CN17)	-	IC12.55	R342, R343	-
						IC23.19	R342	-
						JA3-A.28	R342	-

Table 6-34 below details the function of the switches associated with the SDRAM.

Table 6-34: External BUS & SDRAM Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-35 below details the function of jumpers associated with the SDRAM.

Table 6-35: External SDRAM Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short Pin 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)*1
	Short Pin 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)*2**
CN24	Short Pin 1-2	Connect 3.3V Power rail to VCC1833_3. (When using the external bus)*3
	Short Pin 2-3	**Connect 1.8V Power rail to VCC1833_3. (When using the XSPI0)**

*1: When using the external bus (SDRAM, NOR Flash), set the Ethernet switch (CN20-CN22) to 2-3.
*2: BUS (SDRAM and NOR Flash) and Ethernet / Switch / ESC channel 2 cannot be used at the same time.
*3: When using CS2# with the CS signal of SDRAM, it is not necessary to set CN24 to 1-2.

6.10 CAN Configuration

Table 6-36 below details the function of the option links associated with CAN Configuration.

Table 6-36: CAN Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P01_7_ CAN_RX_ ADTRG_ BSC_A19	C1	P01_7	CAN_RX	IC28.22 (SW4-7 = ON), SW11-8=ON	SW11-10=OFF, SW11-9=OFF	U10.4	-	-
			ADTRG	IC28.22 (SW4-7 = ON), SW11-9=ON	SW11-10=OFF, SW11-8=OFF	JA1-A.8	-	-
			P01_7	IC28.22 (SW4-7 = ON), SW11-10=ON	SW11-9=OFF, SW11-8=OFF	CN1.2	-	-
			BSC_A19	IC28.23 (SW4-7 = OFF)	-	IC22.C3	-	-
						JA3-A.40	-	-
P02_2_ CAN_TX_ IRQ4_ BSC_A16	F3	P02_2	CAN_TX	IC29.25 (SW4-7 = ON), SW8-8 = ON	SW8-10 = OFF, SW8-9 = OFF	U10.1	-	-
			IRQ4	IC29.25 (SW4-7 = ON), SW8-9 = ON	SW8-10 = OFF, SW8-8 = OFF	JA5-A.9	-	-
			P02_2	IC29.25 (SW4-7 = ON), SW8-10 = ON	SW8-9 = OFF, SW8-8 = OFF	CN1.4	-	-
			BSC_A16	IC29.26 (SW4-7 = OFF)	-	IC22.B8	-	-
						JA3-A.37	-	-
P02_3_ CAN1_RX_ BSC_A15	E1	P02_3	**P02_3_ CAN1_RX**	**IC29.33 (SW4-7 = ON)**	-	**CN1.6**	-	-
						JA5-A.6	-	-
			BSC_A15	IC29.32 (SW4-7 = OFF)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-
P02_0_ CAN1_TX_ BSC_A18	E3	P02_0	**P02_0_ CAN1_TX**	**IC28.36 (SW4-7 = ON)**	-	**CN1.3**	-	-
						JA5-A.5	-	-
			BSC_A18	IC28.35 (SW4-7 = OFF)	-	IC22.D3	-	-
						JA3-A.39	-	-

Table 6-37 to **Table 6-39** below details the function of the switches associated with the CAN.

Table 6-37: CAN Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I^2C, etc.)**
OFF	Enables the external bus signal.

Table 6-38: CAN Configuration Switch Settings (2)

SW8-10	SW8-9	SW8-8	Explanation
ON	OFF	OFF	Enable the "P02_2" signal.
OFF	ON	OFF	Enable the "IRQ4" signal.
OFF	OFF	ON	Enable the "CAN_TX" signal.

Table 6-39: CAN Configuration Switch Settings (3)

SW11-10	SW11-9	SW11-8	Explanation
ON	OFF	OFF	Enable the "P01_7" signal.
OFF	ON	OFF	Enable the "ADTRG" signal.
OFF	OFF	ON	Enable the "CAN_RX" signal.

6.11 Ethernet Configuration

Table 6-40 to **Table 6-43** below details the function of the option links associated with Ethernet Configuration.

Table 6-40: Ethernet Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH0_TXCLK	L7	P09_7	**ETH0_TXCLK**	**R99**	**-**	**IC35.37**	**R329**	**R328**
ETH0_TXEN	N8	P10_0	**ETH0_TXEN**	**R100**	**-**	**IC35.33**	**-**	**-**
ETH0_TXD0	M7	P09_6	**ETH0_TXD0**	**R98**	**-**	**IC35.38**	**-**	**-**
ETH0_TXD1	N7	P09_5	**ETH0_TXD1**	**R97**	**-**	**IC35.40**	**-**	**-**
ETH0_TXD2	M6	R09_4	**ETH0_TXD2**	**R96**	**-**	**IC35.41**	**-**	**-**
ETH0_TXD3	R4	P09_3	**ETH0_TXD3**	**R95**	**-**	**IC35.42**	**-**	**-**
ETH0_RXCLK	M5	P08_6	**ETH0_RXCLK**	**-**	**-**	**IC35.32**	**R38**	**-**
ETH0_RXDV	P3	P08_5	**ETH0_RXDV**	**-**	**-**	**IC35.30**	**R280**	**-**
ETH0_RXD0	M8	P10_1	**ETH0_RXD0**	**-**	**-**	**IC35.29**	**R281**	**-**
ETH0_RXD1	L8	P10_2	**ETH0_RXD1**	**-**	**-**	**IC35.27**	**R282**	**-**
ETH0_RXD2	L9	P10_3	**ETH0_RXD2**	**-**	**-**	**IC35.26**	**R283**	**-**
ETH0_RXD3	N4	P08_4	**ETH0_RXD3**	**-**	**-**	**IC35.25**	**R284**	**-**
ETH0_REFCLK (RGMII)	R3	P09_1	**ETH0_REFCLK_25**	**R94, R277**	**R226**	**IC35.63**	**R243, R329**	**R328**
ETH0_REFCLK_G *1	-	-		R161, R226	R227			
ETH_MDIO	P4	P09_0	**ETH_MDIO**	**-**	**-**	**IC35.50**	**-**	**-**
						IC31.50	**-**	**-**
				CN21(short 1-2)	**-**	**IC16.50**	**-**	**-**
ETH_MDC	N5	P08_7	**ETH_MDC**	**-**	**-**	**IC35.48**	**-**	**-**
						IC31.48	**-**	**-**
				CN20(short 1-2)	**-**	**IC16.48**	**-**	**-**

*1: In the default RSK+ configuration, ETH0_REFCLK_G signal is not connected to the XTAL1 pin of the Ethernet controller IC (IC35). If you want to connect the external clock (X1) on the RSK+ to the Ethernet controller IC, configure as shown in Table 6-40 above.

Table 6-41: Ethernet Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH1_TXCLK	N1	P06_4	**ETH1_TXCLK**	**R92**	**-**	**IC31.37**	**R334**	**R333**
ETH1_TXEN	N2	P06_5	**ETH1_TXEN**	**R93**	**-**	**IC31.33**	**-**	**-**
ETH1_TXD0	K4	P06_3	**ETH1_TXD0**	**R91**	**-**	**IC31.38**	**-**	**-**
ETH1_TXD1	M2	P06_2	**ETH1_TXD1**	**R90**	**-**	**IC31.40**	**-**	**-**
ETH1_TXD2	M1	P05_7	**ETH1_TXD2**	**R2**	**-**	**IC31.41**	**-**	**-**
ETH1_TXD3	L2	P06_0	**ETH1_TXD3**	**R3**	**-**	**IC31.42**	**-**	**-**
ETH1_RXCLK	M4	P07_3	**ETH1_RXCLK**	**-**	**-**	**IC31.32**	**R206**	**-**
ETH1_RXDV	P2	P07_2	**ETH1_RXDV**	**-**	**-**	**IC31.30**	**R207**	**-**
ETH1_RXD0	L4	P06_6	**ETH1_RXD0**	**-**	**-**	**IC31.29**	**R208**	**-**
ETH1_RXD1	M3	P06_7	**ETH1_RXD1**	**-**	**-**	**IC31.27**	**R209**	**-**
ETH1_RXD2	P1	P07_0	**ETH1_RXD2**	**-**	**-**	**IC31.26**	**R210**	**-**
ETH1_RXD3	N3	P07_1	**ETH1_RXD3**	**-**	**-**	**IC31.25**	**R211**	**-**
ETH1_REFCLK (RGMII)	L3	P06_1	**ETH1_REFCLK_25**	**R4, R204**	**R203**	**IC31.63**	**R220, R334**	**R333**
ETH1_REFCLK_G *1	-	-		R162, R203	R204			
ETH_MDIO	P4	P09_0	**ETH_MDIO**	**-**	**-**	**IC35.50**	**-**	**-**
						IC31.50	**-**	**-**
				CN21(short 1-2)	**-**	**IC16.50**	**-**	**-**
ETH_MDC	N5	P08_7	**ETH_MDC**	**-**	**-**	**IC35.48**	**-**	**-**
						IC31.48	**-**	**-**
				CN20(short 1-2)	**-**	**IC16.48**	**-**	**-**

*1: In the default RSK+ configuration, ETH1_REFCLK_G signal is not connected to the XTAL1 pin of the Ethernet controller IC (IC31). If you want to connect the external clock (X1) on the RSK+ to the Ethernet controller IC, configure as shown in Table 6-41 above.

Table 6-42: Ethernet Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_TXCLK_ M1_UP_ BSC_CS5#	C3	P00_6	**ETH2_TXCLK**	**R85, IC46.25 (Short 2-3 of CN17)**	-	**IC16.37**	**R339**	**R338**
			M1_UP_ BSC_CS5#	R85, IC46.26 (Short 1-2 of CN17)	-	JA2-A.13	-	-
						JA3-A.27	-	-
ETH2_TXEN_ BSC_RD#	A3	P00_2	**ETH2_TXEN**	**R83, IC46.56 (Short 2-3 of CN17)**	-	**IC16.33**	-	-
			BSC_RD#	R83, IC46.55 (Short 1-2 of CN17)	-	IC22.F2	-	-
						JA3-A.25	-	-
ETH2_TXD0_ BSC_DQMLL	B1	P01_5	**ETH2_TXD0**	**R89, IC46.5 (Short 2-3of CN17)**	-	**IC16.38**	-	-
			BSC_DQMLL_ WE0#	R89, IC46.6 (Short 1-2 of CN17)	-	IC22.A5	-	-
						IC23.15	-	-
						JA3-A.48	-	-
ETH2_TXD1_ BSC_DQMLU	E4	P01_4	**ETH2_TXD1**	**R88, IC46.50 (Short 2-3 of CN17)**	-	**IC16.40**	-	-
			BSC_DQMLU	R88, IC46.49 (Short 1-2 of CN17)	-	IC23.39	-	-
						JA3-A.47	-	-
ETH2_TXD2_MPU	C2	P01_3	**ETH2_TXD2**	**R87 IC46.8 (Short 2-3 of CN17)**	-	**IC16.41**	-	-
ETH2_TXD3_MPU _BSC_CS2#	B2	P01_2	**ETH2_TXD3**	**R86, IC46.47 (Short 2-3 of CN17)**	-	**IC16.42**	-	-
			BSC_CS2#_ CS3#	R86, IC46.46 (Short 1-2 of CN17)	-	IC12.55	R342, R343	-
						IC23.19	R342	-
						JA3-A.28	R342	-
ETH2_RXCLK_ BSC_D13_MCLK5	B5	P24_1	**ETH2_RXCLK**	**IC46.33 (Short 2-3 of CN17)**	-	**IC16.32**	**R106**	-
			BSC_D13	IC46.32 (Short 1-2 of CN17), R268	R270	IC22.F6	-	-
						IC23.50	-	-
						JA3-A.34	-	-
			MCLK5	IC46.32 (Short 1-2 of CN17), R270	R268	CN3.3	-	-
ETH2_RXDV_ BSC_A13	D5	P00_1	**ETH2_RXDV**	**IC46.42 (Short 2-3 of CN17)**	-	**IC16.30**	**R107**	-
			BSC_A13	IC46.41 (Short 1-2 of CN17)	-	IC22.B7	-	-
						IC23.36	-	-
						JA3-A.14	-	-
ETH2_RXD0_ BSC_D11_MCLK4	D6	P23_7	**ETH2_RXD0**	**IC46.16 (Short 2-3 of CN17)**	-	**IC16.29**	**R108**	-
			BSC_D11	IC46.17 (Short 1-2 of CN17), R272	R273	IC22.H4	-	-
						IC23.47	-	-
						JA3-A.32	-	-
			MCLK4	IC46.17 (Short 1-2 of CN17), R273	R272	CN3.5	-	-

Table 6-43: Ethernet Configuration Option Links (4)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_RXD1_ BSC_D12_MDAT4	A5	P24_0	**ETH2_RXD1**	**IC46.39 (Short 2-3 of CN17)**	**-**	**IC16.27**	**R109**	**-**
			BSC_D12	IC46.38 (Short 1-2 of CN17), R276	R277	IC22.G6	-	-
						IC23.48	-	-
						JA3-A.33	-	-
			MDAT4	IC46.38 (Short 1-2 of CN17), R277	R276	CN3.6	-	-
ETH2_RXD2_ BSC_D14_MDAT5	C5	P24_2	**ETH2_RXD2**	**IC46.19 (Short 2-3 of CN17)**	**-**	**IC16.26**	**R110**	**-**
			BSC_D14	IC46.20 (Short 1-2 of CN17), R274	R275	IC22.H7	-	-
						IC23.51	-	-
						JA3-A.35	-	-
			MDAT5	IC46.20 (Short 1-2 of CN17), R275	R274	CN3.4	-	-
ETH2_RXD3_ BSC_D15	C4	P00_0	**ETH2_RXD3**	**IC46.36 (Short 2-3 of CN17)**	**-**	**IC16.25**	**R111**	**-**
			BSC_D15	IC46.35 (Short 1-2 of CN17)	-	IC22.F7	-	-
						IC23.53	-	-
						JA3-A.36	-	-
ETH2_REFCLK_ BSC_WR#	B3	P00_3	**ETH2_ REFCLK_25 (RGMII)**	**R84, IC46.53 (Short 2-3 of CN17) R114**	**R113**	**IC16.63**	**R265, R339**	**R338**
			BSC_WR#	R84, IC46.52 (Short 1-2 of CN17)	-	IC23.16	-	-
						JA3-A.26	-	-
ETH2_REFCLK_G *1	-	-	ETH2_ REFCLK_25	R113, R163	R114	IC16.63	R262	-
ETH_MDIO	P4	P09_0	**ETH_MDIO**	**-**	**-**	**IC35.50**	**-**	**-**
						IC31.50	**-**	**-**
				CN21(short 1-2)	**-**	**IC16.50**	**-**	**-**
ETH_MDC	N5	P08_7	**ETH_MDC**	**-**	**-**	**IC35.48**	**-**	**-**
						IC31.48	**-**	**-**
				CN20(short 1-2)	**-**	**IC16.48**	**-**	**-**
ETH2_MDIO_ M1_VN_ BSC_CAS#	A2	P01_0	ETH2_MDIO	IC46.2 (Short 2-3 of CN17), CN21 (short 2-3)	-	IC16.50	-	-
			BSC_CAS#_ M1_VN	IC46.3 (Short 1-2 of CN17)	-	IC23.17	-	-
						JA2-A.16	-	-
						JA3-A.49	-	-
ETH2_MDC_ BSC_CKE	D3	P01_1	ETH2_MDC	IC46.11 (Short 2-3 of CN17), CN20 (short 2-3)	-	IC16.48	-	-
			BSC_CKE	IC46.12 (Short 1-2 of CN17)	-	IC23.37	-	-
						JA3-A.46	-	-

*1: In the default RSK+ configuration, ETH2_REFCLK_G signal is not connected to the XTAL1 pin of the Ethernet controller IC (IC16). If you want to connect the external clock (X1) on the RSK+ to the Ethernet controller IC, configure as shown in Table 6-43 above.

Table 6-44 below details the function of jumpers associated with the Ethernet.

Table 6-44: Ethernet Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)*1**
CN20, CN21, CN22*2	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes

*1: BUS (SDRAM and NOR Flash) and Ethernet / Switch / ESC channel 2 cannot be used at the same time.
*2: When using VCC1833_2 at 3.3 V, use a jumper setting of 2-3.

6.12 Ethernet Switch Configuration

Table 6-40 to **Table 6-43** and **Table 6-45** and **Table 6-46** below details the function of the option links associated with Ethernet Switch (ETHSW) Configuration.

Table 6-45: ETHSW Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SW2_ BSC_A00_18	K1	P05_4	**SW2_BSC_A00_ 18**	-	-	**SW2**	-	-
			BSC_A00_33 (ETHSW_LPI0)	-	-	**JA3-A.1**	-	-
P01_7_ CAN_RX_ ADTRG_ BSC_A19	C1	P01_7	CAN_RX	IC28.22 (SW4-7 = ON), SW11-8=ON	SW11-10=OFF, SW11-9=OFF	U10.4	-	-
			ADTRG	IC28.22 (SW4-7 = ON), SW11-9=ON	SW11-10=OFF, SW11-8=OFF	JA1-A.8	-	-
			P01_7 (ETHSW_LPI1)	IC28.22 (SW4-7 = ON), SW11-10=ON	SW11-9=OFF, SW11-8=OFF	CN1.2	-	-
			BSC_A19	IC28.23 (SW4-7 = OFF)	-	IC22.C3	-	-
						JA3-A.40	-	-
P02_0_ CAN1_TX_ BSC_A18	E3	P02_0	**P02_0_ CAN1_TX (ETHSW_LPI2)**	**IC28.36 (SW4-7 = ON)**	-	**CN1.3**	-	-
						JA5-A.5	-	-
			BSC_A18	IC28.35 (SW4-7 = OFF)	-	IC22.D3	-	-
						JA3-A.39	-	-
DIP_SW1_18_ M1_TRDCLK	M13	P13_6	**DIP_SW1_18_ M1_TRDCLK (ETHSW_ PTPOUT0)**	**SW4-8 = OFF**	-	**SW3.1**	-	-
				-	-	**CN1.11**	-	-
				IC50(SW4-8 = ON)	-	JA2-A.26	-	-
BSC_A17	D1	P02_1	**BSC_A17 (ETHSW_ PTPOUT1)**	-	-	**IC22.E8**	-	-
						JA3-A.38	-	-
						IC15.4	-	-
EEPROM_SCL	L10	P13_2	**EEPROM_SCL (ETHSW_ PTPOUT2)**	-	-	**IC20.6**	-	-
EEPROM_SDA	N12	P13_3	**EEPROM_SDA (ETHSW_ PTPOUT3)**	-	-	**IC20.5**	-	-
P02_2_ CAN_TX_ IRQ4_ BSC_A16	F3	P02_2	CAN_TX	IC29.25 (SW4-7 = ON), SW8-8 = ON	SW8-10 = OFF, SW8-9 = OFF	U10.1	-	-
			IRQ4	IC29.25 (SW4-7 = ON), SW8-9 = ON	SW8-10 = OFF, SW8-8 = OFF	JA5-A.9	-	-
			P02_2 (ETHSW_ TDMAOUT0)	IC29.25 (SW4-7 = ON), SW8-10 = ON	SW8-9 = OFF, SW8-8 = OFF	CN1.4	-	-
			BSC_A16	IC29.26 (SW4-7 = OFF)	-	IC22.B8	-	-
						JA3-A.37	-	-
P02_3_ CAN1_RX_ BSC_A15	E1	P02_3	**P02_3_ CAN1_RX (ETHSW_ TDMAOUT1)**	**IC29.33 (SW4-7 = ON)**	-	**CN1.6**	-	-
						JA5-A.6	-	-
			BSC_A15	IC29.32 (SW4-7 = OFF)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-

Table 6-46: ETHSW Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH_LED1_MDV2	D9	P20_3	**ETH_LED1_ MDV2 (ETHSW_ TDMAOUT2)**	-	-	**CN1.17**	-	-
				-	-	**ETH_LED1.A**	**R7**	-
ETH_LED3_MDV3	A9	P20_4	**ETH_LED3_ MDV3 (ETHSW_ TDMAOUT3)**	-	-	**CN1.18**	-	-
				-	-	**ETH_LED3.A**	**R11**	-
ETH0_LINK	M9	P10_4	**ETH0_LINK (ETHSW_ PHYLINK0)**	-	-	**IC35.59**	-	-
ETH1_LINK	K2	P05_5	**ETH1_LINK (ETHSW_ PHYLINK1)**	-	-	**IC31.59**	-	-
ETH2_LINK_ BSC_CS0#	B4	P00_5	**ETH2_LINK (ETHSW_ PHYLINK2)**	**IC46.22 (Short 2-3 of CN17)**	-	**IC16.59**	-	-
			BSC_CS0#	IC46.23 (Short 1-2 of CN17)	-	IC22.F1	-	-

Table 6-47 and **Table 6-48** below details the function of the switches associated with the ETHSW.

Table 6-47: ETHSW Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-48: ETHSW Configuration Switch Settings (2)

SW8-10	SW8-9	SW8-8	Explanation
ON	OFF	OFF	Enable the "P02_2" signal.
OFF	ON	OFF	Enable the "IRQ4" signal.
OFF	OFF	ON	Enable the "CAN_TX" signal.

Table 6-49 below details the function of jumpers associated with the ETHSW.

Table 6-49: ETHSW Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)*1**
CN20, CN21, CN22*2	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes

*1: BUS (SDRAM and NOR Flash) and Ethernet / Switch / ESC channel 2 cannot be used at the same time.
*2: When using VCC1833_2 at 3.3 V, use a jumper setting of 2-3.

6.13 EtherCAT Slave Controller Configuration

Table 6-40 to **Table 6-43** and **Table 6-50** below details the function of the option links associated with EtherCAT Slave Controller (ESC) Configuration.

Table 6-50: ESC Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH_LED0_MDV1	D8	P20_2	**ETH_LED0_ MDV1 (ESC_LEDRUN)**	-	-	**ETH_LED0.A**	**R6**	-
PMOD3A_GPIO1_ MDD	F12	P17_0	**PMOD3A_GPIO1 _MDD (ESC_IRQ)**	-	-	**J25.9**	-	-
						IC14.12	-	-
ETH_LED1_MDV2	D9	P20_3	**ETH_LED1_ MDV2 (ESC_LEDERR)**	-	-	**CN1.17**	-	-
						ETH_LED1.A	**R7**	-
ETH_LED2_MDV0	B9	P20_1	**ETH_LED2_ MDV0 (ESC_ LINKACT0)**	-	-	**ETH_LED2.A**	**R8**	-
ETH_LED3_MDV3	A9	P20_4	**ETH_LED3_ MDV3 (ESC_ LINKACT1)**	-	-	**CN1.18**	-	-
						ETH_LED3.A	**R11**	-
LED5_BSC_D08	A6	P22_1	**LED5**	**IC28.42 (SW4-7 = ON), SW8-4 = ON**	**SW8-5 = OFF**	**ETH_LED5.A**	**R13**	-
			M2_POE (ESC_LINKACT1)	IC28.42 (SW4-7 = ON), SW8-5 = ON	SW8-4 = OFF	JA5-A.16	-	-
			BSC_D08	IC28.41 (SW4-7 = OFF)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
BSC_A17	D1	P02_1	**BSC_A17 (ESC_SYNC0, ESC_SYNC1)**	-	-	**IC22.E8**	-	-
						JA3-A.38	-	-
						IC15.4	-	-
P01_6_BSC_A20	D2	P01_6	**P01_6 (ESC_LATCH0, ESC_LATCH1)**	**IC28.33 (SW4-7 = ON)**	-	**CN1.1**	-	-
						JA2-A.23	-	-
			BSC_A20	IC28.32 (SW4-7 = OFF)	-	IC22.B6	-	-
						JA3-A.41	-	-
ESC_RESETOUT#	L12	P13_4	**ESC_ RESETOUT#**	-	-	**IC35.53**	-	-
				-	-	**IC31.53**	-	-
				CN22(short 1-2)	-	**IC16.53**	-	-
EEPROM_SCL	L10	P13_2	**EEPROM_SCL (ESC_I2CCLK)**	-	-	**IC20.6**	-	-
EEPROM_SDA	N12	P13_3	**EEPROM_SDA (ESC_I2CDATA)**	-	-	**IC20.5**	-	-
ETH0_LINK	M9	P10_4	**ETH0_LINK (ESC_ PHYLINK0)**	-	-	**IC35.59**	-	-
ETH1_LINK	K2	P05_5	**ETH1_LINK (ESC_ PHYLINK1)**	-	-	**IC31.59**	-	-
ETH2_LINK_ BSC_CS0#	B4	P00_5	**ETH2_LINK (ESC_ PHYLINK2)**	**IC46.22 (Short 2-3 of CN17)**	-	**IC16.59**	-	-
			BSC_CS0#	IC46.23 (Short 1-2 of CN17)	-	IC22.F1	-	-

Table 6-51 and **Table 6-52** below details the function of the switches associated with the ESC.

Table 6-51: ESC Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-52: ESC Configuration Switch Settings (2)

SW8-5	SW8-4	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	**ON**	**Enable the "LED5" signal.**

Table 6-53 below details the function of jumpers associated with the ESC.

Table 6-53: ESC Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)*1**
CN20, CN21, CN22*2	**Short 1-2**	**When using 3 ports in the same PHY mode**
	Short 2-3	When ports 0 and 1 use the same PHY mode and port 2 uses different PHY modes

*1: BUS (SDRAM and NOR Flash) and Ethernet / Switch / ESC channel 2 cannot be used at the same time.
*2: When using VCC1833_2 at 3.3 V, use a jumper setting of 2-3.

6.14 LED Configuration

Table 6-54 and **Table 6-55** below details the function of the option links associated with LED Configuration.

Table 6-54: LED Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD3A_GPIO2_ LED_GRN_ M1_WP	D14	P18_2	PMOD3A_GPIO2	SW8-1 = ON	SW8-3 = OFF, SW8-2 = OFF	J25.10	-	-
			LED_GREEN	**SW8-2 = ON**	**SW8-3 = OFF, SW8-1 = OFF**	**LED0.A**	**R43**	**-**
			M1_WP	SW8-3 = ON	SW8-2 = OFF, SW8-1 = OFF	JA2-A.17	-	-
LED_ORANGE_ BSC_D10	B6	P22_3	**LED_ORANGE**	**IC28.39 (SW4-7 = ON)**	**-**	**LED1.A**	**R44**	**-**
			BSC_D10	IC28.38 (SW4-7 = OFF)	-	IC22.G3	-	-
						IC23.45	-	-
						JA3-A.31	-	-
LED_RED1_ BSC_CKIO	H2	P04_1	**LED_RED1**	**IC29.36 (SW4-7 = ON)**	**-**	**LED2.A**	**R46**	**-**
			BSC_CKIO	IC29.35 (SW4-7 = OFF)	-	IC23.38	-	-
						JA3-A.44	-	-
LED_RED2_ TRACE_CTL_ M1_POE	F14	P17_3	TRACE_CTL	IC45.47 (SW4-6 = ON)	-	CN9.36	-	-
			LED_RED2	**IC45.46 (SW4-6 = OFF) SW11-1 = ON**	**SW11-3 = OFF SW11-2 = OFF**	**LED3.A**	**R47**	**-**
			M1_POE	IC45.46 (SW4-6 = OFF) SW11-3 = ON	SW11-2 = OFF SW11-1 = OFF	JA2-A.24	-	-
ETH_LED0_MDV1	D8	P20_2	**ETH_LED0_ MDV1**	**-**	**-**	**ETH_LED0.A**	**R6**	**-**
ETH_LED1_MDV2	D9	P20_3	**ETH_LED1_ MDV2**	**-**	**-**	**CN1.17**	**-**	**-**
						ETH_LED1.A	**R7**	**-**
ETH_LED2_MDV0	B9	P20_1	**ETH_LED2_ MDV0**	**-**	**-**	**ETH_LED2.A**	**R8**	**-**
ETH_LED3_MDV3	A9	P20_4	**ETH_LED3_ MDV3**	**-**	**-**	**CN1.18**	**-**	**-**
						ETH_LED3.A	**R11**	**-**
LED4_BSC_A14	G3	P03_0	**LED4**	**IC29.22 (SW4-7 = ON)**	**-**	**ETH_LED4.A**	**R12**	**-**
			BSC_A14	IC29.23 (SW4-7 = OFF)	-	IC22.C7	-	-
						IC23.20	-	-
						JA3-A.15	-	-
LED5_BSC_D08	A6	P22_1	**LED5**	**IC28.42 (SW4-7 = ON), SW8-4 = ON**	**SW8-5 = OFF**	**ETH_LED5.A**	**R13**	**-**
			M2_POE	IC28.42 (SW4-7 = ON), SW8-5 = ON	SW8-4 = OFF	JA5-A.16	-	-
			BSC_D08	IC28.41 (SW4-7 = OFF)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-

Table 6-55: LED Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
LED6_BSC_A08	H4	P04_4	**LED6**	**IC29.11 (SW4-7 = ON)**	**-**	**ETH_LED6.A**	**R14**	**-**
			BSC_A08	IC29.12 (SW4-7 = OFF)	-	IC22.A2	-	-
						IC23.32	-	-
						JA3-A.9	-	-
LED7_BSC_A04	J5	P05_0	**LED7**	**IC29.5 (SW4-7 = ON)**	**-**	**ETH_LED7.A**	**R15**	**-**
			BSC_A04	IC29.6 (SW4-7 = OFF)	-	IC22.B1	-	-
						IC23.26	-	-
						JA3-A.5	-	-

Table 6-56 to **Table 6-59** below details the function of the switches associated with the LED.

Table 6-56: LED Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-57: LED Configuration Switch Settings (2)

SW8-5	SW8-4	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	**ON**	**Enable the "LED5" signal.**

Table 6-58: LED Configuration Switch Settings (3)

SW8-3	SW8-2	SW8-1	Explanation
ON	OFF	OFF	Enable the "M1_WP" signal.
OFF	**ON**	**OFF**	**Enable the "LED_GREEN" signal.**
OFF	OFF	ON	Enable the " PMOD3A_GPIO2" signal.

Table 6-59: LED Configuration Switch Settings (4)

SW11-3	SW11-2	SW11-1	Explanation
ON	OFF	OFF	Enable the "M1_POE" signal.
OFF	**OFF**	**ON**	**Enable the " LED_RED2" signal.**

6.15 I²C & EEPROM Configuration

Table 6-60 below detail the function of the option links associated with I²C & EEPROM Configuration.

Table 6-60: I²C & EEPROM Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
EEPROM_SCL	L10	P13_2	**EEPROM_SCL**	**-**	**-**	**IC20.6**	**-**	**-**
EEPROM_SDA	N12	P13_3	**EEPROM_SDA**	**-**	**-**	**IC20.5**	**-**	**-**

6.16 IRQ & Switch Configuration

Table 6-61 to **Table 6-63** below details the function of the option links associated with IRQ & Switch Configuration.

Table 6-61: IRQ & Switch Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P02_3_ CAN1_RX_ BSC_A15	E1	P02_3	**P02_3_ CAN1_RX (IRQ15)**	**IC29.33 (SW4-7 = ON)**	-	**CN1.6**	-	-
						JA5-A.6	-	-
			BSC_A15	IC29.32 (SW4-7 = OFF)	-	IC22.D7	-	-
						IC23.21	-	-
						JA3-A.16	-	-
P02_2_ CAN_TX_ IRQ4_ BSC_A16	F3	P02_2	CAN_TX	IC29.25 (SW4-7 = ON), SW8-8 = ON	SW8-10 = OFF, SW8-9 = OFF	U10.1	-	-
			IRQ4 (IRQ14)	IC29.25 (SW4-7 = ON), SW8-9 = ON	SW8-10 = OFF, SW8-8 = OFF	JA5-A.9	-	-
			P02_2	IC29.25 (SW4-7 = ON), SW8-10 = ON	SW8-9 = OFF, SW8-8 = OFF	CN1.4	-	-
			BSC_A16	IC29.26 (SW4-7 = OFF)	-	IC22.B8	-	-
						JA3-A.37	-	-
ETH2_INT#_ BSC_WAIT#	A4	P00_4	**ETH2_INT#_ BSC_WAIT# (IRQ13)**	-	-	**IC16.51**	**R341**	**R340**
						JA3-A.45	R340	R341
ETH1_INT#	K3	P05_6	**ETH1_INT# (IRQ12)**	-	-	**IC31.51**	-	-
SW2_ BSC_A00_18	K1	P05_4	**SW2_ BSC_A00_18 (IRQ12)**	-	-	**SW2**	-	-
			BSC_A00_33	-	-	**JA3-A.1**	-	-
ETH0_LINK	M9	P10_4	**ETH0_LINK (IRQ11)**	-	-	**IC35.59**	-	-
SCI_RTS_ M1_UN_ HSPI_IO7	D15	P18_1	**SCI_RTS_ M1_UN (IRQ10)**	**R314**	-	**J25.4**	-	-
						JA2-A.14	-	-
			HSPI_IO7	**R315**	-	**CN4.12**	-	-
MIKROBUS_INT_ BSC_A10	G5	P03_7	**MIKROBUS_INT (IRQ9)**	**IC29.16 (SW4-7 = ON)**	-	**J22.2**	-	-
			BSC_A10	IC29.17 (SW4-7 = OFF)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
PMOD2A_INT_ BSC_A11	G4	P03_6	**PMOD2A_ INT_BSC_A11**	-	-	**CN3.14**	-	-
			PMOD2A_INT (IRQ8)	**IC29.39 (SW4-7 = ON)**	-	**J26.7**	-	-
			BSC_A11	IC29.38 (SW4-7 = OFF)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
SW1_HSPI_IO3	G12	P16_3	**SW1(IRQ7)**	**R318**	-	**SW1**	-	-
			HSPI_IO3	**R319**	-	**CN4.8**	-	-
HSPI0_ECS#_ HSPI_CK	K12	P14_2	**XSPI0_ECS# (IRQ6)**	**R309**	-	**IC19.A5**	-	-
			HSPI_CK	**R310**	-	**CN4.3**	-	-

Table 6-62: IRQ & Switch Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD3A_INT_ BSC_A12	G1	P03_5	**PMOD3A_INT_ BSC_A12**	**-**	**-**	**CN3.13**	**-**	**-**
			PMOD3A_INT (IRQ5)	**IC29.19 (SW4-7 = ON)**	**-**	**J25.7**	**-**	**-**
			BSC_A12	IC29.20 (SW4-7 = OFF)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
P02_0_ CAN1_TX_ BSC_A18	E3	P02_0	**P02_0_ CAN1_TX (IRQ4)**	**IC28.36 (SW4-7 = ON)**	**-**	**CN1.3**	**-**	**-**
						JA5-A.5	**-**	**-**
			BSC_A18	IC28.35 (SW4-7 = OFF)	-	IC22.D3	-	-
						JA3-A.39	-	-
ETH2_TXD1_ BSC_DQMLU	E4	P01_4	**ETH2_TXD1**	**R88, IC46.50 (Short 2-3 of CN17)**	**-**	**IC16.40**	**-**	**-**
			BSC_DQMLU (IRQ3)	R88, IC46.49 (Short 1-2 of CN17)	-	IC23.39	-	-
						JA3-A.47	-	-
ETH0_INT#	N6	P09_2	**ETH0_INT# (IRQ0)**	**-**	**-**	**IC35.51**	**-**	**-**
NMI_18_ HSPI_IO2	H14	P16_2	**NMI_18**	**R316**	**-**	**NMI**	**E32**	**-**
			HSPI_IO2	**R317**	**-**	**CN4.7**	**-**	**-**
RESET#	P6	-	**DBG_RESET#**	**-**	**-**	**J20.10**	**-**	**-**
						CN9.9	**-**	**-**
			RESET#	**-**	**-**	**JA2-A.1**	**-**	**-**
			RESET_SW#	**IC2, IC3, IC4**	**-**	**S3**	**-**	**-**
DIP_SW1_18_ M1_TRDCLK	M13	P13_6	**DIP_SW1_18_ M1_TRDCLK**	**SW4-8 = OFF**	**-**	**SW3.1**	**-**	**-**
				-	**-**	**CN1.11**	**-**	**-**
				IC50(SW4-8 = ON)	-	JA2-A.26	-	-
DIP_SW2_18_ M1_TRCCLK	M12	P13_5	**DIP_SW2_18_ M1_TRCCLK**	**SW4-8 = OFF**	**-**	**SW3.2**	**-**	**-**
				-	**-**	**CN1.15**	**-**	**-**
				IC48(SW4-8 = ON)	-	JA2-A.25	-	-
DIP_SW3_18_ M2_TRDCLK	L13	P14_0	**DIP_SW3_18_ M2_TRDCLK**	**SW4-8 = OFF**	**-**	**SW3.3**	**-**	**-**
			M2_TRDCLK_3 3	IC50(SW4-8 = ON)	-	JA5-A.18	-	-
DIP_SW4_18_ M2_TRCCLK	M11	P13_7	**DIP_SW4_18_ M2_TRCCLK**	**SW4-8 = OFF**	**-**	**SW3.4**	**-**	**-**
			M2_TRCCLK_3 3	IC48(SW4-8 = ON)	-	JA5-A.17	-	-
BSC_A07_MD0	H3	P04_5	**BSC_A07_MD0**	**-**	**-**	**IC14.4 (SW4.1)**	**-**	**-**
			BSC_A07	IC29.46 (SW4-7 = OFF)	-	IC22.B2	-	-
						IC23.31	-	-
						JA3-A.8	-	-
PMOD2A_CS3_ GPIO_BSC_A06_ MD1	H5	P04_6	**PMOD2A_ CS3_GPIO_ BSC_A06_MD1**	**-**	**-**	**IC14.7 (SW4.2)**	**-**	**-**
			PMOD2A_ CS3_GPIO	**IC29.8 (SW4-7 = ON)**	**-**	**J26.10**	**-**	**-**
			BSC_A06	IC29.9 (SW4-7 = OFF)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-

Table 6-63: IRQ & Switch Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
PMOD2A_CS2_GPIO_BSC_A05_MD2	J1	P04_7	**PMOD2A_CS2_GPIO_BSC_A05_MD2**	**-**	**-**	**IC14.9 (SW4.3)**	**-**	**-**
			PMOD2A_CS2_GPIO	**IC29.50 (SW4-7 = ON)**	**-**	**J26.9**	**-**	**-**
			BSC_A05	IC29.49 (SW4-7 = OFF)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
PMOD3A_GPIO1_MDD	F12	P17_0	**PMOD3A_GPIO1_MDD**	**-**	**-**	**J25.9**	**-**	**-**
						IC14.12 (SW4.4)	**-**	**-**
BSC_A17_MDW	D1	P02_1	**BSC_A17_MDW**	**-**	**-**	**IC22.E8**	**-**	**-**
						JA3-A.38	**-**	**-**
						SW4.12	**-**	**-**
TRACE_OPTION_SEL (SW4.6)	-	-	**TRACE_OPTION_SEL**	**-**	**-**	**IC45.29**	**-**	**-**
						IC45.30	**-**	**-**
BSC_OPTION_SW (SW4.7)	-	-	**BSC_OPTION_SEL**	**-**	**-**	**IC28.29**	**-**	**-**
						IC28.30	**-**	**-**
						IC29.29	**-**	**-**
						IC29.30	**-**	**-**
DIP_SW3_EN (SW4.8)	-	-	**DIP_SW3_EN**	**-**	**-**	**IC48.5**	**-**	**-**
						IC50.5	**-**	**-**

Table 6-64 and **Table 6-66** below details the function of the switches associated with the IRQ & Switch.

Table 6-64: IRQ & Switch Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I^2C, etc.)**
OFF	Enables the external bus signal.

Table 6-65: IRQ & Switch Configuration Switch Settings (2)

SW4-8	Explanation
ON	Enables the signal of the connector (JA2-A).
OFF	**Enable SW3.**

Table 6-66: IRQ & Switch Configuration Switch Settings (3)

SW8-10	SW8-9	SW8-8	Explanation
ON	OFF	OFF	Enable the "ENCIF03" signal.
OFF	ON	OFF	Enable the "IRQ4" signal.
OFF	OFF	ON	Enable the "CAN_RX" signal.

Table 6-67 below details the function of jumpers associated with the IRQ & Switch.

Table 6-67: IRQ & Switch Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)**

6.17 MTU & POE & Timer Configuration

Table 6-68 to **Table 6-70** below details the function of the option links associated with MTU & POE & Timer Configuration.

Table 6-68: MTU & POE & Timer Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_TXCLK_ M1_UP_ BSC_CS5#	C3	P00_6	**ETH2_TXCLK**	**R85, IC46.25 (Short 2-3 of CN17)**	**-**	**IC16.37**	**R339**	**R338**
			M1_UP_ BSC_CS5#	R85, IC46.26 (Short 1-2 of CN17)	-	JA2-A.13	-	-
						JA3-A.27	-	-
SCI_RTS_ M1_UN_ HSPI_IO7	D15	P18_1	**SCI_RTS_ M1_UN**	**R314**	**-**	**J25.4**	**-**	**-**
						JA2-A.14	**-**	**-**
			HSPI_IO7	**R315**	**-**	**CN4.12**	**-**	**-**
M1_VP_ BSC_RAS#	D4	P00_7	**M1_VP**	**IC28.19 (SW4-7 = ON)**	**-**	**JA2-A.15**	**-**	**-**
			BSC_RAS#	IC28.20 (SW4-7 = OFF)	-	IC23.18	-	-
						JA3-A.50	-	-
ETH2_MDIO_ M1_VN_ BSC_CAS#	A2	P01_0	ETH2_MDIO	IC46.2 (Short 2-3 of CN17), CN21 (short 2-3)	-	IC16.50	-	-
			BSC_CAS#_ M1_VN	IC46.3 (Short 1-2 of CN17)	-	IC23.17	-	-
						JA2-A.16	-	-
						JA3-A.49	-	-
PMOD3A_GPIO2_ LED_GRN_ M1_WP	D14	P18_2	PMOD3A_ GPIO2	SW8-1 = ON	SW8-3 = OFF, SW8-2 = OFF	J25.10	-	-
			LED_GREEN	**SW8-2 = ON**	**SW8-3 = OFF, SW8-1 = OFF**	**LED0.A**	**R43**	**-**
			M1_WP	SW8-3 = ON	SW8-2 = OFF, SW8-1 = OFF	JA2-A.17	-	-
MB_RST#_ M1_WN	E13	P18_3	**MB_RST#_ M1_WN**	**-**	**-**	**J21.2**	**-**	**-**
						JA2-A.18	**-**	**-**
P01_6_BSC_A20	D2	P01_6	**P01_6**	**IC28.33 (SW4-7 = ON)**	**-**	**CN1.1**	**-**	**-**
						JA2-A.23	**-**	**-**
			BSC_A20	IC28.32 (SW4-7 = OFF)	-	IC22.B6	-	-
						JA3-A.41	-	-
LED_RED2_ TRACE_CTL_ M1_POE	F14	P17_3	TRACE_CTL	IC45.47 (SW4-6 = ON)	-	CN9.36	-	-
			LED_RED2	**IC45.46 (SW4-6 = OFF) SW11-1 = ON**	**SW11-3 = OFF SW11-2 = OFF**	**LED3.A**	**R47**	**-**
			M1_POE	IC45.46 (SW4-6 = OFF) SW11-3 = ON	SW11-2 = OFF SW11-1 = OFF	JA2-A.24	-	-
DIP_SW2_18_ M1_TRCCLK	M12	P13_5	**DIP_SW2_18_ M1_TRCCLK**	**SW4-8 = OFF**	**-**	**SW3.2**	**-**	**-**
				-	**-**	**CN1.15**	**-**	**-**
				IC48(SW4-8 = ON)	-	JA2-A.25	-	-
DIP_SW1_18_ M1_TRDCLK	M13	P13_6	**DIP_SW1_18_ M1_TRDCLK**	**SW4-8 = OFF**	**-**	**SW3.1**	**-**	**-**
				-	**-**	**CN1.11**	**-**	**-**
				IC50(SW4-8 = ON)	-	JA2-A.26	-	-

Table 6-69: MTU & POE & Timer Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P02_2_ CAN_TX_ IRQ4_ BSC_A16	F3	P02_2	CAN_TX	IC29.25 (SW4-7 = ON), SW8-8 = ON	SW8-10 = OFF, SW8-9 = OFF	U10.1	-	-
			IRQ4	IC29.25 (SW4-7 = ON), SW8-9 = ON	SW8-10 = OFF, SW8-8 = OFF	JA5-A.9	-	-
			P02_2	IC29.25 (SW4-7 = ON), SW8-10 = ON	SW8-9 = OFF, SW8-8 = OFF	CN1.4	-	-
			BSC_A16	IC29.26 (SW4-7 = OFF)	-	IC22.B8	-	-
						JA3-A.37	-	-
LED5_BSC_D08	A6	P22_1	**LED5**	**IC28.42 (SW4-7 = ON), SW8-4 = ON**	**SW8-5 = OFF**	**ETH_LED5.A**	**R13**	**-**
			M2_POE	IC28.42 (SW4-7 = ON), SW8-5 = ON	SW8-4 = OFF	JA5-A.16	-	-
			BSC_D08	IC28.41 (SW4-7 = OFF)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
DIP_SW4_18_ M2_TRCCLK	M11	P13_7	**DIP_SW4_18_ M2_TRCCLK**	**SW4-8 = OFF**	**-**	**SW3.4**	**-**	**-**
			M2_TRCCLK_33	IC48(SW4-8 = ON)	-	JA5-A.17	-	-
DIP_SW3_18_ M2_TRDCLK	L13	P14_0	**DIP_SW3_18_ M2_TRDCLK**	**SW4-8 = OFF**	**-**	**SW3.3**	**-**	**-**
			M2_TRDCLK_33	IC50(SW4-8 = ON)	-	JA5-A.18	-	-
TRACE_D1_ BSC_D01	C8	P21_2	**TRACE_D1_ BSC_D01**	**-**	**-**	**CN3.18**	**-**	**-**
			TRACE_D1	IC28.2 (SW4-7 = ON), IC45.56 (SW4-6 = ON)	-	CN9.28	-	-
			M2_UP	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-4 = ON	SW11-5 = OFF	JA5-A.19	-	-
			RS485_RX	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-5 = ON	SW11-4 = OFF	IC27.3	-	-
			BSC_D01	IC28.3 (SW4-7 = OFF)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
TRACE_D3_ BSC_D03	E7	P21_4	**TRACE_D3_ BSC_D03**	**-**	**-**	**CN3.16**	**-**	**-**
			TRACE_D3	IC28.5 (SW4-7 = ON), IC45.2 (SW4-6 = ON)	-	CN9.24	-	-
			M2_UN	**IC28.5 (SW4-7 = ON), IC45.3 (SW4-6 = OFF)**	**-**	**JA5-A.20**	**-**	**-**
			BSC_D03	IC28.6 (SW4-7 = OFF)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-

Table 6-70: MTU & POE & Timer Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
P21_5_ TRACE_D4_ BSC_D04	C7	P21_5	TRACE_D4	IC28.50 (SW4-7 = ON), IC45.53 (SW4-6 = ON)	-	CN9.22	-	-
			M2_VP	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-6 = ON	SW11-7 = OFF	JA5-A.21	-	-
			P21_5	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-7 = ON	SW11-6 = OFF	CN1.5	-	-
			BSC_D04	IC28.49 (SW4-7 = OFF)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-
TRACE_D7_ BSC_D07	A7	P22_0	**TRACE_D7_ BSC_D07**	**-**	**-**	**CN3.8**	**-**	**-**
			TRACE_D7	IC28.11 (SW4-7 = ON), IC45.8 (SW4-6 = ON)	-	CN9.16	-	-
			M2_VN	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-6 = ON	SW8-7 = OFF	JA5-A.22	-	-
			RS485_DE	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-7 = ON	SW8-6 = OFF	IC27.5	-	-
			BSC_D07	IC28.12 (SW4-7 = OFF)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
TRACE_D5_ BSC_D05	D7	P21_6	TRACE_D5	IC28.8 (SW4-7 = ON), IC45.5 (SW4-6 = ON)	-	CN9.20	-	-
			M2_WP	**IC28.8 (SW4-7 = ON), IC45.6 (SW4-6 = OFF)**	**-**	**JA5-A.23**	**-**	**-**
			BSC_D05	IC28.9 (SW4-7 = OFF)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
TRACE_D6_ BSC_D06	B7	P21_7	**TRACE_D6_ BSC_D06**	**-**	**-**	**CN3.7**	**-**	**-**
			TRACE_D6	IC28.47 (SW4-7 = ON), IC45.50 (SW4-6 = ON)	-	CN9.18	-	-
			M2_WN	**IC28.47 (SW4-7 = ON), IC45.49 (SW4-6 = OFF)**	**-**	**JA5-A.24**	**-**	**-**
			BSC_D06	IC28.46 (SW4-7 = OFF)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-

Table 6-71 to **Table 6-78** below details the function of the switches associated with the MTU & POE & Timer.

Table 6-71: MTU & POE & Timer Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-72: MTU & POE & Timer Configuration Switch Settings (2)

SW8-10	SW8-9	SW8-8	Explanation
ON	OFF	OFF	Enable the "P02_2" signal.
OFF	ON	OFF	Enable the "IRQ4" signal.
OFF	OFF	ON	Enable the "CAN_TX" signal.

Table 6-73: MTU & POE & Timer Configuration Switch Settings (3)

SW8-7	SW8-6	Explanation
ON	OFF	Enable the "RS485_DE" signal.
OFF	ON	Enable the "M2_VN" signal.

Table 6-74: MTU & POE & Timer Configuration Switch Settings (4)

SW8-5	SW8-4	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	ON	Enable the "LED5" signal.

Table 6-75: MTU & POE & Timer Configuration Switch Settings (5)

SW8-3	SW8-2	SW8-1	Explanation
ON	OFF	OFF	Enable the "M1_WP" signal.
OFF	**ON**	**OFF**	**Enable the "LED_GREEN" signal.**
OFF	OFF	ON	Enable the " PMOD3A_GPIO2" signal.

Table 6-76: MTU & POE & Timer Configuration Switch Settings (6)

SW11-7	SW11-6	Explanation
ON	OFF	Enable the "P21_5" signal.
OFF	ON	Enable the "M2_VP" signal.

Table 6-77: MTU & POE & Timer Configuration Switch Settings (7)

SW11-5	SW11-4	Explanation
ON	OFF	Enable the "RS485_RX" signal.
OFF	ON	Enable the "M2_UP" signal.

Table 6-78: MTU & POE & Timer Configuration Switch Settings (8)

SW11-3	SW11-2	SW11-1	Explanation
ON	OFF	OFF	Enable the "M1_POE" signal.
OFF	**OFF**	**ON**	**Enable the " LED_RED2" signal.**

Table 6-79 below details the function of jumpers associated with the MTU & POE & Timer.

Table 6-79: MTU & POE & Timer Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)**

6.18 GPT & POEG & Timer Configuration

Table 6-80 to **Table 6-82** below details the function of the option links associated with GPT & POEG & Timer Configuration.

Table 6-80: GPT & POEG & Timer Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ETH2_TXCLK_ M1_UP_ BSC_CS5#	C3	P00_6	**ETH2_TXCLK**	**R85, IC46.25 (Short 2-3 of CN17)**	**-**	**IC16.37**	**R339**	**R338**
			M1_UP_ BSC_CS5#	R85, IC46.26 (Short 1-2 of CN17)	-	JA2-A.13	-	-
						JA3-A.27	-	-
SCI_RTS_ M1_UN_ HSPI_IO7	D15	P18_1	**SCI_RTS_ M1_UN**	**R314**	**-**	**J25.4**	**-**	**-**
						JA2-A.14	**-**	**-**
			HSPI_IO7	**R315**	**-**	**CN4.12**	**-**	**-**
M1_VP_ BSC_RAS#	D4	P00_7	**M1_VP**	**IC28.19 (SW4-7 = ON)**	**-**	**JA2-A.15**	**-**	**-**
			BSC_RAS#	IC28.20 (SW4-7 = OFF)	-	IC23.18	-	-
						JA3-A.50	-	-
ETH2_MDIO_ M1_VN_ BSC_CAS#	A2	P01_0	ETH2_MDIO	IC46.2 (Short 2-3 of CN17), CN21 (short 2-3)	-	IC16.50	-	-
			BSC_CAS#_ M1_VN	IC46.3 (Short 1-2 of CN17)	-	IC23.17	-	-
						JA2-A.16	-	-
						JA3-A.49	-	-
PMOD3A_GPIO2_ LED_GRN_ M1_WP	D14	P18_2	PMOD3A_ GPIO2	SW8-1 = ON	SW8-3 = OFF, SW8-2 = OFF	J25.10	-	-
			LED_GREEN	**SW8-2 = ON**	**SW8-3 = OFF, SW8-1 = OFF**	**LED0.A**	**R43**	**-**
			M1_WP	SW8-3 = ON	SW8-2 = OFF, SW8-1 = OFF	JA2-A.17	-	-
MB_RST#_ M1_WN	E13	P18_3	**MB_RST#_ M1_WN**	**-**	**-**	**J21.2**	**-**	**-**
						JA2-A.18	**-**	**-**
P01_6_BSC_A20	D2	P01_6	**P01_6**	**IC28.33 (SW4-7 = ON)**	**-**	**CN1.1**	**-**	**-**
						JA2-A.23	**-**	**-**
			BSC_A20	IC28.32 (SW4-7 = OFF)	-	IC22.B6	-	-
						JA3-A.41	-	-
LED_RED2_ TRACE_CTL_ M1_POE	F14	P17_3	TRACE_CTL	IC45.47 (SW4-6 = ON)	-	CN9.36	-	-
			LED_RED2	**IC45.46 (SW4-6 = OFF) SW11-1 = ON**	**SW11-3 = OFF SW11-2 = OFF**	**LED3.A**	**R47**	**-**
			M1_POE	IC45.46 (SW4-6 = OFF) SW11-3 = ON	SW11-2 = OFF SW11-1 = OFF	JA2-A.24	-	-
P02_2_ CAN_TX_ IRQ4_ BSC_A16	F3	P02_2	CAN_TX	IC29.25 (SW4-7 = ON), SW8-8 = ON	SW8-10 = OFF, SW8-9 = OFF	U10.1	-	-
			IRQ4	IC29.25 (SW4-7 = ON), SW8-9 = ON	SW8-10 = OFF, SW8-8 = OFF	JA5-A.9	-	-
			P02_2	IC29.25 (SW4-7 = ON), SW8-10 = ON	SW8-9 = OFF, SW8-8 = OFF	CN1.4	-	-
			BSC_A16	IC29.26 (SW4-7 = OFF)	-	IC22.B8	-	-
						JA3-A.37	-	-

Table 6-81: GPT & POEG & Timer Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
LED5_BSC_D08	A6	P22_1	**LED5**	**IC28.42 (SW4-7 = ON), SW8-4 = ON**	**SW8-5 = OFF**	**ETH_LED5.A**	**R13**	**-**
			M2_POE	IC28.42 (SW4-7 = ON), SW8-5 = ON	SW8-4 = OFF	JA5-A.16	-	-
			BSC_D08	IC28.41 (SW4-7 = OFF)	-	IC22.H2	-	-
						IC23.42	-	-
						JA3-A.29	-	-
TRACE_D1_ BSC_D01	C8	P21_2	**TRACE_D1_ BSC_D01**	**-**	**-**	**CN3.18**	**-**	**-**
			TRACE_D1	IC28.2 (SW4-7 = ON), IC45.56 (SW4-6 = ON)	-	CN9.28	-	-
			M2_UP	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-4 = ON	SW11-5 = OFF	JA5-A.19	-	-
			RS485_RX	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-5 = ON	SW11-4 = OFF	IC27.3	-	-
			BSC_D01	IC28.3 (SW4-7 = OFF)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
TRACE_D3_ BSC_D03	E7	P21_4	**TRACE_D3_ BSC_D03**	**-**	**-**	**CN3.16**	**-**	**-**
			TRACE_D3	IC28.5 (SW4-7 = ON), IC45.2 (SW4-6 = ON)	-	CN9.24	-	-
			M2_UN	**IC28.5 (SW4-7 = ON), IC45.3 (SW4-6 = OFF)**	**-**	**JA5-A.20**	**-**	**-**
			BSC_D03	IC28.6 (SW4-7 = OFF)	-	IC22.F4	-	-
						IC23.7	-	-
						JA3-A.20	-	-
P21_5_ TRACE_D4_ BSC_D04	C7	P21_5	TRACE_D4	IC28.50 (SW4-7 = ON), IC45.53 (SW4-6 = ON)	-	CN9.22	-	-
			M2_VP	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-6 = ON	SW11-7 = OFF	JA5-A.21	-	-
			P21_5	IC28.50 (SW4-7 = ON), IC45.52 (SW4-6 = OFF), SW11-7 = ON	SW11-6 = OFF	CN1.5	-	-
			BSC_D04	IC28.49 (SW4-7 = OFF)	-	IC22.F5	-	-
						IC23.8	-	-
						JA3-A.21	-	-

Table 6-82: GPT & POEG & Timer Configuration Option Links (3)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D7_ BSC_D07	A7	P22_0	**TRACE_D7_ BSC_D07**	**-**	**-**	**CN3.8**	**-**	**-**
			TRACE_D7	IC28.11 (SW4-7 = ON), IC45.8 (SW4-6 = ON)	-	CN9.16	-	-
			M2_VN	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-6 = ON	SW8-7 = OFF	JA5-A.22	-	-
			RS485_DE	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-7 = ON	SW8-6 = OFF	IC27.5	-	-
			BSC_D07	IC28.12 (SW4-7 = OFF)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
TRACE_D5_ BSC_D05	D7	P21_6	TRACE_D5	IC28.8 (SW4-7 = ON), IC45.5 (SW4-6 = ON)	-	CN9.20	-	-
			M2_WP	**IC28.8 (SW4-7 = ON), IC45.6 (SW4-6 = OFF)**	**-**	**JA5-A.23**	**-**	**-**
			BSC_D05	IC28.9 (SW4-7 = OFF)	-	IC22.H6	-	-
						IC23.10	-	-
						JA3-A.22	-	-
TRACE_D6_ BSC_D06	B7	P21_7	**TRACE_D6_ BSC_D06**	**-**	**-**	**CN3.7**	**-**	**-**
			TRACE_D6	IC28.47 (SW4-7 = ON), IC45.50 (SW4-6 = ON)	-	CN9.18	-	-
			M2_WN	**IC28.47 (SW4-7 = ON), IC45.49 (SW4-6 = OFF)**	**-**	**JA5-A.24**	**-**	**-**
			BSC_D06	IC28.46 (SW4-7 = OFF)	-	IC22.E6	-	-
						IC23.11	-	-
						JA3-A.23	-	-

Table 6-83 to **Table 6-90** below details the function of the switches associated with the GPT & POEG & Timer.

Table 6-83: GPT & POEG & Timer Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-84: GPT & POEG & Timer Configuration Switch Settings (2)

SW8-10	SW8-9	SW8-8	Explanation
ON	OFF	OFF	Enable the "P02_2" signal.
OFF	ON	OFF	Enable the "IRQ4" signal.
OFF	OFF	ON	Enable the "CAN_TX" signal.

Table 6-85: GPT & POEG & Timer Configuration Switch Settings (3)

SW8-7	SW8-6	Explanation
ON	OFF	Enable the "RS485_DE" signal.
OFF	ON	Enable the "M2_VN" signal.

Table 6-86: GPT & POEG & Timer Configuration Switch Settings (4)

SW8-5	SW8-4	Explanation
ON	OFF	Enable the "M2_POE" signal.
OFF	ON	Enable the "LED5" signal.

Table 6-87: GPT & POEG & Timer Configuration Switch Settings (5)

SW8-3	SW8-2	SW8-1	Explanation
ON	OFF	OFF	Enable the "M1_WP" signal.
OFF	**ON**	**OFF**	**Enable the "LED_GREEN" signal.**
OFF	OFF	ON	Enable the " PMOD3A_GPIO2" signal.

Table 6-88: GPT & POEG & Timer Configuration Switch Settings (6)

SW11-7	SW11-6	Explanation
ON	OFF	Enable the "P21_5" signal.
OFF	ON	Enable the "M2_VP" signal.

Table 6-89: GPT & POEG & Timer Configuration Switch Settings (7)

SW11-5	SW11-4	Explanation
ON	OFF	Enable the "RS485_RX" signal.
OFF	ON	Enable the "M2_UP" signal.

Table 6-90: GPT & POEG & Timer Configuration Switch Settings (8)

SW11-3	SW11-2	SW11-1	Explanation
ON	OFF	OFF	Enable the "M1_POE" signal.
OFF	**OFF**	**ON**	**Enable the " LED_RED2" signal.**

Table 6-91 below details the function of jumpers associated with the GPT & POEG & Timer.

Table 6-91: GPT & POEG & Timer Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN17	Short 1-2	Connect 3.3V Power rail to VCC1833_2. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_2. (When using the Ethernet)**

6.19 PMOD (UART) Configuration

Table 6-92 below details the function of the option links associated with PMOD (UART) Configuration.

Table 6-92: PMOD (UART) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SCI_CTS	F13	P17_4	**SCI_CTS**	**-**	**-**	**J25.1**	**-**	**-**
SCI_TXD_ HSPI_IO6	E14	P18_0	**SCI_TXD**	**R312**	**-**	**J22.4**	**-**	**-**
						J25.2	**-**	**-**
						JA2-A.6	**-**	**-**
			HSPI_IO6	**R313**	**-**	**CN4.11**	**-**	**-**
SCI_RXD	E15	P17_7	**SCI_RXD**	**-**	**-**	**J22.3**	**-**	**-**
						J25.3	**-**	**-**
						JA2-A.8	**-**	**-**
SCI_RTS_ M1_UN_ HSPI_IO7	D15	P18_1	**SCI_RTS_ M1_UN**	**R314**	**-**	**J25.4**	**-**	**-**
						JA2-A.14	**-**	**-**
			HSPI_IO7	**R315**	**-**	**CN4.12**	**-**	**-**
PMOD3A_INT_ BSC_A12	G1	P03_5	**PMOD3A_INT_ BSC_A12**	**-**	**-**	**CN3.13**	**-**	**-**
			PMOD3A_INT	**IC29.19 (SW4-7 = ON)**	**-**	**J25.7**	**-**	**-**
			BSC_A12	IC29.20 (SW4-7 = OFF)	-	IC22.A7	-	-
						IC23.35	-	-
						JA3-A.13	-	-
PMOD3A_RESET	G14	P16_7	**PMOD3A_RESE T**	**-**	**-**	**J25.8**	**-**	**-**
PMOD3A_GPIO1_ MDD	F12	P17_0	**PMOD3A_GPIO1 _MDD**	**-**	**-**	**J25.9**	**-**	**-**
						IC14.12	**-**	**-**
PMOD3A_GPIO2_ LED_GRN_ M1_WP	D14	P18_2	PMOD3A_ GPIO2	SW8-1 = ON	SW8-3 = OFF, SW8-2 = OFF	J25.10	-	-
			LED_GREEN	**SW8-2 = ON**	**SW8-3 = OFF, SW8-1 = OFF**	**LED0.A**	**R43**	**-**
			M1_WP	SW8-3 = ON	SW8-2 = OFF, SW8-1 = OFF	JA2-A.17	-	-

Table 6-93 and **Table 6-94** below details the function of the switches associated with the PMOD (UART).

Table 6-93: PMOD (UART) Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I^2C, etc.)**
OFF	Enables the external bus signal.

Table 6-94: PMOD (UART) Configuration Switch Settings (2)

SW8-3	SW8-2	SW8-1	Explanation
ON	OFF	OFF	Enable the "M1_WP" signal.
OFF	**ON**	**OFF**	**Enable the "LED_GREEN" signal.**
OFF	OFF	ON	Enable the " PMOD3A_GPIO2" signal.

6.20 PMOD (SPI) Configuration

Table 6-95 below details the function of the option links associated with PMOD (SPI) Configuration.

Table 6-95: PMOD (SPI) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
CS_ TRACE_D0_ BSC_D00_ HSPI_INT#-B	B8	P21_1	**CS_TRACE_ D0_BSC_D00**	**CN25 (short 1-2)**	**-**	**CN3.17**	**-**	**-**
			TRACE_D0	CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.42 (SW4-6 = ON)	-	CN9.38	-	-
			CS	**CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.41 (SW4-6 = OFF)**	**-**	**J26.1**	**-**	**-**
						J21.3	**-**	**-**
			BSC_D00	CN25 (short 1-2) IC28.55 (SW4-7 = OFF)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			HSPI_INT#-B	CN25 (short 2-3)	-	CN4.13	-	-
MOSI	D13	P18_5	**MOSI**	**-**	**-**	**J21.6**	**-**	**-**
						J26.2	**-**	**-**
P18_6_MISO	C15	P18_6	**P18_6_MISO**	**-**	**-**	**J21.5**	**-**	**-**
						J26.3	**E23**	**E2**
						J27.1	E2	E23
						CN1.7	-	-
SCK	E12	P18_4	**SCK**	**-**	**-**	**J21.4**	**-**	**-**
						J26.4	**E24**	**E3**
						J27.2	E3	E24
PMOD2A_INT_ BSC_A11	G4	P03_6	**PMOD2A_INT_ BSC_A11**	**-**	**-**	**CN3.14**	**-**	**-**
			PMOD2A_INT	**IC29.39 (SW4-7 = ON)**	**-**	**J26.7**	**-**	**-**
			BSC_A11	IC29.38 (SW4-7 = OFF)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
PMOD2A_ RESET_BSC_A09	H1	P04_0	**PMOD2A_ RESET**	**IC29.42 (SW4-7 = ON)**	**-**	**J26.8**	**-**	**-**
			BSC_A09	IC29.41 (SW4-7 = OFF)	-	IC22.A6	-	-
						IC23.33	-	-
						JA3-A.10	-	-
PMOD2A_CS2_ GPIO_BSC_A05_ MD2	J1	P04_7	**PMOD2A_ CS2_GPIO_ BSC_A05_MD2**	**-**	**-**	**IC14.9**	**-**	**-**
			PMOD2A_ CS2_GPIO	**IC29.50 (SW4-7 = ON)**	**-**	**J26.9**	**-**	**-**
			BSC_A05	IC29.49 (SW4-7 = OFF)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
PMOD2A_CS3_ GPIO_BSC_A06_ MD1	H5	P04_6	**PMOD2A_ CS3_GPIO_ BSC_A06_MD1**	**-**	**-**	**IC14.7**	**-**	**-**
			PMOD2A_ CS3_GPIO	**IC29.8 (SW4-7 = ON)**	**-**	**J26.10**	**-**	**-**
			BSC_A06	IC29.9 (SW4-7 = OFF)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-

Table 6-96 below details the function of the switches associated with the PMOD (SPI).

Table 6-96: PMOD (SPI) Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-109 below details the function of jumpers associated with the PMOD (SPI).

Table 6-97: PMOD (SPI) Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN25	**Short 1-2**	**Enable other signals. (Trace, SPI, External Bus)**
	Short 2-3	Enables the interrupt signal for the SHOST interface.

6.21 PMOD (I²C) Configuration

Table 6-98 below details the function of the option links associated with PMOD (I²C) Configuration.

Table 6-98: PMOD (I²C) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SCL_BSC_A02	J4	P05_2	**SCL**	**IC29.2 (SW4-7 = ON)**	-	**J22.5**	-	-
						J27.1	-	**E2**
						J30.4	-	-
						JA1-A.26	-	-
						J26.3	E2	E23
			BSC_A02	IC29.3 (SW4-7 = OFF)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
SDA_BSC_A01	J3	P05_3	**SDA**	**IC29.56 (SW4-7 = ON)**	-	**J22.6**	-	-
						J27.2	-	**E3**
						J30.3	-	-
						CN1.18	-	-
						JA1-A.25	-	-
						J26.4	E3	E24
			BSC_A01	IC29.55 (SW4-7 = OFF)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-
PMOD2A_INT_ BSC_A11	G4	P03_6	**PMOD2A_INT_ BSC_A11**	-	-	**CN3.14**	-	-
			PMOD2A_INT	**IC29.39 (SW4-7 = ON)**	-	**J26.7**	-	-
			BSC_A11	IC29.38 (SW4-7 = OFF)	-	IC22.D6	-	-
						IC23.22	-	-
						JA3-A.12	-	-
PMOD2A_ RESET_BSC_A09	H1	P04_0	**PMOD2A_ RESET**	**IC29.42 (SW4-7 = ON)**	-	**J26.8**	-	-
			BSC_A09	IC29.41 (SW4-7 = OFF)	-	IC22.A6	-	-
						IC23.33	-	-
						JA3-A.10	-	-
PMOD2A_CS2_ GPIO_BSC_A05_ MD2	J1	P04_7	**PMOD2A_ CS2_GPIO_ BSC_A05_MD2**	-	-	**IC14.9**	-	-
			PMOD2A_ CS2_GPIO	**IC29.50 (SW4-7 = ON)**	-	**J26.9**	-	-
			BSC_A05	IC29.49 (SW4-7 = OFF)	-	IC22.D2	-	-
						IC23.29	-	-
						JA3-A.6	-	-
PMOD2A_CS3_ GPIO_BSC_A06_ MD1	H5	P04_6	**PMOD2A_ CS3_GPIO_ BSC_A06_MD1**	-	-	**IC14.7**	-	-
			PMOD2A_ CS3_GPIO	**IC29.8 (SW4-7 = ON)**	-	**J26.10**	-	-
			BSC_A06	IC29.9 (SW4-7 = OFF)	-	IC22.C2	-	-
						IC23.30	-	-
						JA3-A.7	-	-

Table 6-99 below details the function of the switches associated with the PMOD (I²C).

Table 6-99: PMOD (I²C) Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

6.22 Grove® (I²C) Configuration

Table 6-100 below details the function of the option links associated with Grove® (I²C) Configuration.

Table 6-100: Grove® (I²C) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SCL_BSC_A02	J4	P05_2	**SCL**	**IC29.2 (SW4-7 = ON)**	-	**J22.5**	-	-
						J27.1	-	**E2**
						J30.4	-	-
						JA1-A.26	-	-
						J26.3	E2	E23
			BSC_A02	IC29.3 (SW4-7 = OFF)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
SDA_BSC_A01	J3	P05_3	**SDA**	**IC29.56 (SW4-7 = ON)**	-	**J22.6**	-	-
						J27.2	-	**E3**
						J30.3	-	-
						CN1.18	-	-
						JA1-A.25	-	-
						J26.4	E3	E24
			BSC_A01	IC29.55 (SW4-7 = OFF)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-

Table 6-101 below details the function of the switches associated with the Grove® (I²C).

Table 6-101: Grove® (I²C) Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

6.23 Grove® (Analog) Configuration

Table 6-102 below details the function of the option links associated with Grove® (Analog) Configuration.

Table 6-102: Grove® (Analog) Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ADC_AN101	A14	-	**ADC_AN101**	-	-	**J28.1**	**R200**	-
ADC_AN102	B11	-	**ADC_AN102**	-	-	**J28.2**	**R201**	-

6.24 QWIIC® Configuration

Table 6-103 below details the function of the option links associated with QWIIC® Configuration.

Table 6-103: QWIIC® Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SCL_BSC_A02	J4	P05_2	**SCL**	**IC29.2 (SW4-7 = ON)**	**-**	**J22.5**	**-**	**-**
						J27.1	**-**	**E2**
						J30.4	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	E2	E23
			BSC_A02	IC29.3 (SW4-7 = OFF)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
SDA_BSC_A01	J3	P05_3	**SDA**	**IC29.56 (SW4-7 = ON)**	**-**	**J22.6**	**-**	**-**
						J27.2	**-**	**E3**
						J30.3	**-**	**-**
						CN1.18	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	E3	E24
			BSC_A01	IC29.55 (SW4-7 = OFF)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-

Table 6-104 below details the function of the switches associated with the QWIIC®.

Table 6-104: QWIIC® Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I^2C, etc.)**
OFF	Enables the external bus signal.

6.25 mikroBUS™ Configuration

Table 6-105 and **Table 6-106** below details the function of the option links associated with mikroBUS™ Configuration.

Table 6-105: mikroBUS™ Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
ADC_AN100	B12	-	**ADC_AN100**	**-**	**-**	**J21.1**	**R197**	**-**
MB_RST#_ M1_WN	E13	P18_3	**MB_RST#_ M1_WN**	**-**	**-**	**J21.2**	**-**	**-**
						JA2-A.18	**-**	**-**
CS_ TRACE_D0_ BSC_D00_ HSPI_INT#-B	B8	P21_1	**CS_TRACE_ D0_BSC_D00**	**CN25 (short 1-2)**	**-**	**CN3.17**	**-**	**-**
			TRACE_D0	CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.42 (SW4-6 = ON)	-	CN9.38	-	-
			CS	**CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.41 (SW4-6 = OFF)**	**-**	**J26.1**	**-**	**-**
						J21.3	**-**	**-**
			BSC_D00	CN25 (short 1-2) IC28.55 (SW4-7 = OFF)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			HSPI_INT#-B	CN25 (short 2-3)	-	CN4.13	-	-
SCK	E12	P18_4	**SCK**	**-**	**-**	**J21.4**	**-**	**-**
						J26.4	**E24**	**E3**
						J27.2	E3	E24
P18_6_MISO	C15	P18_6	**P18_6_MISO**	**-**	**-**	**J21.5**	**-**	**-**
						J26.3	**E23**	**E2**
						J27.1	E2	E23
						CN1.7	-	-
MOSI	D13	P18_5	**MOSI**	**-**	**-**	**J21.6**	**-**	**-**
						J26.2	**-**	**-**
MIK_PWM_SCK	G15	P17_6	**MIK_PWM_SCK**	**-**	**-**	**J22.1**	**-**	**-**
						JA2-A.10	**-**	**-**
MIKROBUS_INT_ BSC_A10	G5	P03_7	**MIKROBUS_ INT**	**IC29.16 (SW4-7 = ON)**	**-**	**J22.2**	**-**	**-**
			BSC_A10	IC29.17 (SW4-7 = OFF)	-	IC22.C6	-	-
						IC23.34	-	-
						JA3-A.11	-	-
SCI_RXD	E15	P17_7	**SCI_RXD**	**-**	**-**	**J22.3**	**-**	**-**
						J25.3	**-**	**-**
						JA2-A.8	**-**	**-**
SCI_TXD_ HSPI_IO6	E14	P18_0	**SCI_TXD**	**R312**	**-**	**J22.4**	**-**	**-**
						J25.2	**-**	**-**
						JA2-A.6	**-**	**-**
			HSPI_IO6	**R313**	**-**	**CN4.11**	**-**	**-**

Table 6-106: mikroBUS™ Configuration Option Links (2)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
SCL_BSC_A02	J4	P05_2	**SCL**	**IC29.2 (SW4-7 = ON)**	**-**	**J22.5**	**-**	**-**
						J27.1	**-**	**E2**
						J30.4	**-**	**-**
						JA1-A.26	**-**	**-**
						J26.3	E2	E23
			BSC_A02	IC29.3 (SW4-7 = OFF)	-	IC22.D1	-	-
						IC23.24	-	-
						JA3-A.3	-	-
SDA_BSC_A01	J3	P05_3	**SDA**	**IC29.56 (SW4-7 = ON)**	**-**	**J22.6**	**-**	**-**
						J27.2	**-**	**E3**
						J30.3	**-**	**-**
						CN1.18	**-**	**-**
						JA1-A.25	**-**	**-**
						J26.4	E3	E24
			BSC_A01	IC29.55 (SW4-7 = OFF)	-	IC22.E1	-	-
						IC23.23	-	-
						JA3-A.2	-	-

Table 6-107 below details the function of the switches associated with the mikroBUS™.

Table 6-107: mikroBUS™ Configuration Switch Settings

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I^2C, etc.)**
OFF	Enables the external bus signal.

6.26 xSPI & QSPI & Octa Flash Configuration

Table 6-108 below details the function of the option links associated with xSPI & QSPI & Octa Flash Configuration.

Table 6-108: xSPI & QSPI & Octa Flash Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
XSPI0_CKP_ BSC_A21	K13	P14_6	**XSPI0_CKP**	**IC12.2 (Short 2-3 of CN24)**	-	**IC19.B2**	-	-
						IC21.16	-	-
						IC41.B2	-	-
			BSC_A21	IC12.3 (Short 1-2 of CN24)	-	IC22.C5	-	-
						JA3-A.42	-	-
OQFLASH_CS0	J15	P15_7	OSPI_CS	CN8 (short 1-2)	-	IC19.C2	-	-
			QSPI_CS	**CN8 (Short 2-3)**	-	**IC21.7**	-	-
XSPI0_RESET0	H11	P16_1	**XSPI0_ RESET0**	-	-	**IC19.A4**	-	-
						IC21.3	-	-
						IC41.A4	-	-
XSPI0_DS_MPU	J13	P14_4	**XSPI0_DS**	**IC12.39 (Short 2-3 of CN24)**	-	**IC19.C3**	-	-
						IC41.C3	-	-
HSPI0_ECS#_ HSPI_CK	K12	P14_2	**XSPI0_ECS#**	**R309**	-	**IC19.A5**	-	-
			HSPI_CK	**R310**	-	**CN4.3**	-	-
XSPI0_IO7_MPU	H12	P15_6	**XSPI0_IO7**	**IC12.16 (Short 2-3 of CN24)**	-	**IC19.E1**	-	-
						IC41.E1	-	-
XSPI0_IO6_MPU	J14	P15_5	**XSPI0_IO6**	**IC12.42 (Short 2-3 of CN24)**	-	**IC19.E2**	-	-
						IC41.E2	-	-
XSPI0_IO5_MPU	H13	P15_4	**XSPI0_IO5**	**IC12.11 (Short 2-3 of CN24)**	-	**IC19.E3**	-	-
						IC41.E3	-	-
XSPI0_IO4_MPU	K11	P15_3	**XSPI0_IO4**	**IC12.47 (Short 2-3 of CN24)**	-	**IC19.D5**	-	-
						IC41.D5	-	-
XSPI0_IO3_ BSC_A25	K15	P15_2	**XSPI0_IO3**	**IC12.8 (Short 2-3 of CN24)**	-	**IC19.D4**	-	-
						IC21.1	-	-
						IC41.D4	-	-
			BSC_A25	IC12.9 (Short 1-2 of CN24)		IC22.F8	-	-
XSPI0_IO2_ BSC_A24	K14	P15_1	**XSPI0_IO2**	**IC12.50 (Short 2-3 of CN24)**	-	**IC19.C4**	-	-
						IC21.9	-	-
						IC41.C4	-	-
			BSC_A24	IC12.49 (Short 1-2 of CN24)	-	IC22.B5	-	-
XSPI0_IO1_ BSC_A23	L11	P15_0	**XSPI0_IO1**	**IC12.5 (Short 2-3 of CN24)**	-	**IC19.D2**	-	-
						IC21.8	-	-
						IC41.D2	-	-
			BSC_A23	IC12.6 (Short 1-2 of CN24)	-	IC22.D8	-	-
XSPI0_IO0_ BSC_A22	M15	P14_7	**XSPI0_IO0**	**IC12.53 (Short 2-3 of CN24)**	-	**IC19.D3**	-	-
						IC21.15	-	-
						IC41.D3	-	-
			BSC_A22	IC12.52 (Short 1-2 of CN24)	-	IC22.C8	-	-
						JA3-A.43	-	-

Table 6-109 below details the function of jumpers associated with the xSPI & QSPI & Octa Flash.

Table 6-109: xSPI & QSPI & Octa Flash Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN8	Short 1-2	Enable Octa Flash (IC19).
	Short 2-3	**Enable QSPI (IC21).**
CN24	Short 1-2	Connect 3.3V Power rail to VCC1833_3. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_3. (When using the XSPI0)*1**

*1: BUS (SDRAM and NOR Flash) and XSPI0 cannot be used at the same time.

6.27 xSPI & HyperRAM Configuration

Table 6-110 below details the function of the option links associated with xSPI & HyperRAM Configuration.

Table 6-110: xSPI & HyperRAM Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
XSPI0_CKP_ BSC_A21	K13	P14_6	**XSPI0_CKP**	**IC12.2 (Short 2-3 of CN24)**	-	**IC19.B2**	-	-
						IC21.16	-	-
						IC41.B2	-	-
			BSC_A21	IC12.3 (Short 1-2 of CN24)	-	IC22.C5	-	-
						JA3-A.42	-	-
XSPI0_CKN_ BSC_CS3#	J12	P14_5	**XSPI0_CKN**	**IC12.56 (Short 2-3 of CN24)**	-	**IC41.B1**	-	-
			BSC_CS2#_ CS3#	IC12.55 (Short 1-2 of CN24)	-	IC46.46	R343, R342	-
						IC23.19	R343	-
						JA3-A.28	R343	-
ORAM_CS0_ HSPI_CS#	G13	P16_0	**OSPI_CS0**	**CN27 (short 1-2)**	-	**IC41.A3**	-	-
			HSPI_CS#	**CN27 (short 2-3)**	-	**CN4.4**	-	-
XSPI0_RESET0	H11	P16_1	**XSPI0_ RESET0**	-	-	**IC19.A4**	-	-
						IC21.3	-	-
						IC41.A4	-	-
XSPI0_DS_MPU	J13	P14_4	**XSPI0_DS**	**IC12.39 (Short 2-3 of CN24)**	-	**IC19.C3**	-	-
						IC41.C3	-	-
XSPI0_IO7_MPU	H12	P15_6	**XSPI0_IO7**	**IC12.16 (Short 2-3 of CN24)**	-	**IC19.E1**	-	-
						IC41.E1	-	-
XSPI0_IO6_MPU	J14	P15_5	**XSPI0_IO6**	**IC12.42 (Short 2-3 of CN24)**	-	**IC19.E2**	-	-
						IC41.E2	-	-
XSPI0_IO5_MPU	H13	P15_4	**XSPI0_IO5**	**IC12.11 (Short 2-3 of CN24)**	-	**IC19.E3**	-	-
						IC41.E3	-	-
XSPI0_IO4_MPU	K11	P15_3	**XSPI0_IO4**	**IC12.47 (Short 2-3 of CN24)**	-	**IC19.D5**	-	-
						IC41.D5	-	-
XSPI0_IO3_ BSC_A25	K15	P15_2	**XSPI0_IO3**	**IC12.8 (Short 2-3 of CN24)**	-	**IC19.D4**	-	-
						IC21.1	-	-
						IC41.D4	-	-
			BSC_A25	IC12.9 (Short 1-2 of CN24)		IC22.F8	-	-
XSPI0_IO2_ BSC_A24	K14	P15_1	**XSPI0_IO2**	**IC12.50 (Short 2-3 of CN24)**	-	**IC19.C4**	-	-
						IC21.9	-	-
						IC41.C4	-	-
			BSC_A24	IC12.49 (Short 1-2 of CN24)	-	IC22.B5	-	-
XSPI0_IO1_ BSC_A23	L11	P15_0	**XSPI0_IO1**	**IC12.5 (Short 2-3 of CN24)**	-	**IC19.D2**	-	-
						IC21.8	-	-
						IC41.D2	-	-
			BSC_A23	IC12.6 (Short 1-2 of CN24)	-	IC22.D8	-	-
XSPI0_IO0_ BSC_A22	M15	P14_7	**XSPI0_IO0**	**IC12.53 (Short 2-3 of CN24)**	-	**IC19.D3**	-	-
						IC21.15	-	-
						IC41.D3	-	-
			BSC_A22	IC12.52 (Short 1-2 of CN24)	-	IC22.C8	-	-
						JA3-A.43	-	-

Table 6-111 below details the function of jumpers associated with the xSPI & HyperRAM.

Table 6-111: xSPI & HyperRAM Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN24	Short 1-2	Connect 3.3V Power rail to VCC1833_3. (When using the external bus)
	Short 2-3	**Connect 1.8V Power rail to VCC1833_3. (When using the XSPI0)*1**
CN27	**Short 1-2**	**Enable the HyperRAM (IC41) signal.**
	Short 2-3	Enable the SHOST signal.

*1: BUS (SDRAM and NOR Flash) and XSPI0 cannot be used at the same time.

6.28 Serial & USB to Serial Configuration

Table 6-112 below details the function of the option links associated with Serial & USB to Serial Configuration.

Table 6-112: Serial & USB to Serial Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
UART_USB_TX_ HSPI_IO4	H15	P16_5	**UART_USB_TX**	**R320**	**-**	**IC38.15**	**-**	**-**
			HSPI_IO4	**R321**	**-**	**CN4.9**	**-**	**-**
UART_USB_RX_ HSPI_IO5	G11	P16_6	**UART_USB_RX**	**CN29 (short 1-2)**	**-**	**IC38.16**	**-**	**-**
			HSPI_IO5	**CN29 (short 2-3)**	**-**	**CN4.10**	**-**	**-**

Table 6-113 below details the function of jumpers associated with Serial & USB to Serial.

Table 6-113: Serial & USB to Serial Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN29	**Short 1-2**	**Enable the USB serial signal.**
	Short 2-3	Enable the SHOST signal.

6.29 Serial & RS485 Configuration

Table 6-114 and **Table 6-115** below details the function of the option links associated with Serial & RS485 Configuration.

Table 6-114: Serial & RS485 Configuration Option Links (1)

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
TRACE_D1_ BSC_D01	C8	P21_2	**TRACE_D1_ BSC_D01**	-	-	**CN3.18**	-	-
			TRACE_D1	IC28.2 (SW4-7 = ON), IC45.56 (SW4-6 = ON)	-	CN9.28	-	-
			M2_UP	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-4 = ON	SW11-5 = OFF	JA5-A.19	-	-
			RS485_RX	IC28.2 (SW4-7 = ON) IC45.55 (SW4-6 = OFF) SW11-5 = ON	SW11-4 = OFF	IC27.3	-	-
			BSC_D01	IC28.3 (SW4-7 = OFF)	-	IC22.E3	-	-
						IC23.4	-	-
						JA3-A.18	-	-
TRACE_D7_ BSC_D07	A7	P22_0	**TRACE_D7_ BSC_D07**	-	-	**CN3.8**	-	-
			TRACE_D7	IC28.11 (SW4-7 = ON), IC45.8 (SW4-6 = ON)	-	CN9.16	-	-
			M2_VN	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-6 = ON	SW8-7 = OFF	JA5-A.22	-	-
			RS485_DE	IC28.11 (SW4-7 = ON), IC45.9 (SW4-6 = OFF), SW8-7 = ON	SW8-6 = OFF	IC27.5	-	-
			BSC_D07	IC28.12 (SW4-7 = OFF)	-	IC22.G7	-	-
						IC23.13	-	-
						JA3-A.24	-	-
TRACE_D2_ BSC_D02	A8	P21_3	**TRACE_D2_ BSC_D02**	-	-	**CN3.15**	-	-
			TRACE_D2	IC28.53 (SW4-7 = ON), IC45.11 (SW4-6 = ON)	-	CN9.26	-	-
			RS485_TX	**IC28.53 (SW4-7 = ON), IC45.12 (SW4-6 = OFF)**	-	**IC27.6**	-	-
			BSC_D02	IC28.52 (SW4-7 = OFF)	-	IC22.H3	-	-
						IC23.5	-	-
						JA3-A.19	-	-

Table 6-115: Serial & RS485 Configuration Option Links (2)

Reference	Setting	Explanation
R193	**Fit**	**Enable termination resistor R194 (130Ω) for RS485 receive signal** *1
	DNF	Disable termination resistor R194 (130Ω) for RS485 receive signal *1

*1: Configure according to the usage of this board and connection destination.

Table 6-116 to **Table 6-119** below details the function of the switches associated with the Serial & RS485.

Table 6-116: Serial & RS485 Configuration Switch Settings (1)

SW4-7	Explanation
ON	**Enables signals other than the external bus. (CAN, Emulator, I²C, etc.)**
OFF	Enables the external bus signal.

Table 6-117: Serial & RS485 Configuration Switch Settings (2)

SW4-6	Explanation
ON	Enable the trace signal.
OFF	**Enables signals other the trace.**

Table 6-118: Serial & RS485 Configuration Switch Settings (3)

SW8-7	SW8-6	Explanation
ON	OFF	Enable the "RS485_DE" signal.
OFF	ON	Enable the "M2_VN" signal.

Table 6-119: Serial & RS485 Configuration Switch Settings (4)

SW11-5	SW11-4	Explanation
ON	OFF	Enable the "RS485_RX" signal.
OFF	ON	Enable the "M2_UP" signal.

6.30 USB Configuration

Table 6-120 below details the function of the option links associated with the USB Configuration.

Table 6-120: USB Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
USB_DP	R13	-	USB_DP	-	-	CN10.3	-	-
						CN11.3	-	-
USB_DM	P13	-	USB_DM	-	-	CN10.2	-	-
						CN11.2	-	-
USB_VBUSEN_ MDV4	B15	P19_0	USB_VBUSEN_ MDV4	-	-	IC25.3	-	-
						IC15.4	-	-
USB_OVRCUR	F15	P17_5	USB_OVRCUR	-	-	IC25.8	-	-
USB_VBUSIN	R2	P07_4	USB_VBUSIN	-	-	CN11.1	R181	-

6.31 Serial Host Interface Configuration

Table 6-121 below details the function of the option links associated with the Serial Host Interface Configuration.

Table 6-121: Serial Host Interface Configuration Option Links

Signal name	MPU		MPU Peripheral Selection			Destination Selection		
	Pin	Port	Signal	Fit	DNF	Interface /Function	Fit	DNF
HSPI0_ECS#_ HSPI_CK	K12	P14_2	**XSPI0_ECS#**	**R309**	-	**IC19.A5**	-	-
			HSPI_CK	**R310**	-	**CN4.3**	-	-
ORAM_CS0_ HSPI_CS#	G13	P16_0	**OSPI_CS0**	**CN27 (short 1-2)**	-	**IC41.A3**	-	-
			HSPI_CS#	**CN27 (short 2-3)**	-	**CN4.4**	-	-
HSPI_IO0	L14	P14_1	**HSPI_IO0**	-	-	**CN4.5**	-	-
HSPI_IO1_A	M14	P14_3	**HSPI_IO1**	**R311**	-	**CN4.6**	-	-
NMI_18_ HSPI_IO2	H14	P16_2	**NMI_18**	**R316**	-	**NMI**	**E32**	-
			HSPI_IO2	**R317**	-	**CN4.7**	-	-
SW1_HSPI_IO3	G12	P16_3	**SW1**	**R318**	-	**SW1**	-	-
			HSPI_IO3	**R319**	-	**CN4.8**	-	-
UART_USB_TX_ HSPI_IO4	H15	P16_5	**UART_USB_TX**	**R320**	-	**IC38.15**	-	-
			HSPI_IO4	**R321**	-	**CN4.9**	-	-
UART_USB_RX_ HSPI_IO5	G11	P16_6	**UART_USB_RX**	**CN29 (short 1-2)**	-	**IC38.16**	-	-
			HSPI_IO5	**CN29 (short 2-3)**	-	**CN4.10**	-	-
SCI_TXD_ HSPI_IO6	E14	P18_0	**SCI_TXD**	**R312**	-	**J22.4**	-	-
						J25.2	-	-
						JA2-A.6	-	-
			HSPI_IO6	**R313**	-	**CN4.11**	-	-
SCI_RTS_ M1_UN_ HSPI_IO7	D15	P18_1	**SCI_RTS_ M1_UN**	**R314**	-	**J25.4**	-	-
						JA2-A.14	-	-
			HSPI_IO7	**R315**	-	**CN4.12**	-	-
CS_ TRACE_D0_ BSC_D00_ HSPI_INT#-B	B8	P21_1	**CS_TRACE_ D0_BSC_D00**	**CN25 (short 1-2)**	-	**CN3.17**	-	-
			TRACE_D0	CN25 (short 1-2) IC28.56 (SW4-7 = ON) IC45.42 (SW4-6 = ON)	-	CN9.38	-	-
			CS	**CN25 (Short 1-2) IC28.56 (SW4-7 = ON) IC45.41 (SW4-6 = OFF)**	-	**J26.1**	-	-
						J21.3	-	-
			BSC_D00	CN25 (short 1-2) IC28.55 (SW4-7 = OFF)	-	IC22.G2	-	-
						IC23.2	-	-
						JA3-A.17	-	-
			HSPI_INT#-B	CN25 (short 2-3)	-	CN4.13	-	-

Table 6-122 below details the function of jumpers associated with the Serial Host Interface.

Table 6-122: Serial Host Interface Configuration Jumper Settings

Reference	Jumper Position	Explanation
CN25	**Short 1-2**	**Enable other signals. (Trace, SPI, External Bus)**
	Short 2-3	Enable the SHOST signal.
CN27	**Short 1-2**	**Enable the HyperRAM (IC41) signal.**
	Short 2-3	Enable the SHOST signal.
CN29	**Short 1-2**	**Enable the USB serial signal.**
	Short 2-3	Enable the SHOST signal.

7. Headers

7.1 Application Headers

This RSK+ board is fitted with application headers, which can be used to connect compatible Renesas application devices or as easy access to MPU pins. Please check the option link when using it.

Table 7-1 below lists the connections of the application header, JA1-A.

Table 7-1: Application Header JA1-A Connections

Application Header JA1-A					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	5V CON_5V	-	2	0V GROUND	-
3	3V3 CON_3V3	-	4	0V GROUND	-
5	AVCC CON_AVCC	E11	6	AVSS CON_AVSS	-
7	AVREF CON_AVREF	C11	8	ADTRG ADTRG	C1
9	ADC0 ADC_AN000	B13	10	ADC1 ADC_AN001	C12
11	ADC2 ADC_AN002	B14	12	ADC3 ADC_AN003	C13
13	DAC0 NC	NC	14	DAC1 NC	NC
15	IO_0 NC	NC	16	IO_1 NC	NC
17	IO_2 NC	NC	18	IO_3 NC	NC
19	IO_4 NC	NC	20	IO_5 NC	NC
21	IO_6 NC	NC	22	IO_7 NC	NC
23	IRQd / IRQAEC / M2_HSIN0 NC	NC	24	IIC_EX NC	NC
25	IIC_SDA SDA	J3	26	IIC_SCL SCL	J4

Table 7-2 below lists the connections of the application header, JA2-A.

Table 7-2: Application Header JA2-A Connections

Application Header JA2-A					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	RESET RESET#	P6	2	EXTAL CON_EXTAL	R6
3	NMI NC	NC	4	Vss1 GROUND	-
5	WDT_OVF NC	NC	6	SCIaTX SCI_TXD	E14
7	IRQa / WKUP / M1_HSIN0 NC	NC	8	SCIaRX SCI_RXD	E15
9	IRQb / M1_HSIN1 NC	NC	10	SCIaCK MIK_PWM_SCK	G15
11	M1_UD NC	NC	12	CTSaRTSa NC	NC
13	M1_UP M1_UP_BSC_CS5#	C3	14	M1_UN SCI_RTS_M1_UN	D15
15	M1_VP M1_VP	D4	16	M1_VN BSC_CAS#_M1_VN	A2
17	M1_WP M1_WP	D14	18	M1_WN MB_RST#_M1_WN	E13
19	TimerOut0 NC	NC	20	TimerOut1 NC	NC
21	TimerIn0 NC	NC	22	TimerIn1 NC	NC
23	IRQc / M1_EncZ / M1_HSIN2 P01_6	D2	24	M1_POE M1_POE	F14
25	M1_TRCCLK M1_TRCCLK_33	M12	26	M1_TRDCLK M1_TRDCLK_33	M13

Table 7-3 below lists the connections of the BUS application header, JA3-A.

Table 7-3: Application Header JA3-A Connections

Application Header JA3-A (Bus)					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	A0 BSC_A00_33	K1	2	A1 BSC_A01	J3
3	A2 BSC_A02	J4	4	A3 BSC_A03	J2
5	A4 BSC_A04	J5	6	A5 BSC_A05	J1
7	A6 BSC_A06	H5	8	A7 BSC_A07	H3
9	A8 BSC_A08	H4	10	A9 BSC_A09	H1
11	A10 BSC_A10	G5	12	A11 BSC_A11	G4
13	A12 BSC_A12	G1	14	A13 BSC_A13	D5
15	A14 BSC_A14	G3	16	A15 BSC_A15	E1
17	D0 BSC_D00	B8	18	D1 BSC_D01	C8
19	D2 BSC_D02	A8	20	D3 BSC_D03	E7
21	D4 BSC_D04	C7	22	D5 BSC_D05	D7
23	D6 BSC_D06	B7	24	D7 BSC_D07	A7
25	RDn BSC_RD#	A3	26	WR / SDWE BSC_WR#	B3
27	CSa M1_UP_BSC_CS5#	C3	28	CSb *1 BSC_CS2#_CS3#	J12
29	D8 BSC_D08	A6	30	D9 BSC_D09	C6
31	D10 BSC_D10	B6	32	D11 BSC_D11	D6
33	D12 BSC_D12	A5	34	D13 BSC_D13	B5
35	D14 BSC_D14	C5	36	D15 BSC_D15	C4
37	A16 BSC_A16	F3	38	A17 BSC_A17	D1
39	A18 BSC_A18	E3	40	A19 BSC_A19	C1
41	A20 BSC_A20	D2	42	A21 BSC_A21	K13
43	A22 BSC_A22	M15	44	SDCLK BSC_CKIO	H2
45	CSc / Wait ETH2_INT#_BSC_WAIT#	A4	46	ALE / SDCKE BSC_CKE	D3
47	HWRn / DQMH BSC_DQMLU	E4	48	LWRn / DQML BSC_DQMLL_WE0#	B1
49	CAS BSC_CAS#_M1_VN	A2	50	RAS BSC_RAS#	D4

*1: The chip select signal assigned on this board can also be used as a SDRAM chip select.

Table 7-4 below lists the connections of the application header, JA5-A.

Table 7-4: Application Header JA5-A Connections

Application Header JA5-A					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	ADC4 ADC_AN104	A12	2	ADC5 ADC_AN105	B10
3	ADC6 ADC_AN106	A11	4	ADC7 ADC_AN107	C9
5	CAN1TX P02_0_CAN1_TX	E3	6	CAN1RX P02_3_CAN1_RX	E1
7	CAN2TX NC	NC	8	CAN2RX NC	NC
9	IRQe / M2_EncZ / M2HSIN1 IRQ4	F3	10	IRQf / M2_HSIN2 NC	NC
11	M2_UD NC	NC	12	M2_Uin NC	NC
13	M2_Vin NC	NC	14	M2_Win NC	NC
15	M2_Toggle NC	NC	16	M2_POE M2_POE	A6
17	M2_TRCCLK M2_TRCCLK_33	M11	18	M2_TRDCLK M2_TRDCLK_33	L13
19	M2_UP M2_UP	C8	20	M2_Un M2_UN	E7
21	M2_VP M2_VP	C7	22	M2_Vn M2_VN	A7
23	M2_WP M2_WP	D7	24	M2_Wn M2_WN	B7

Table 7-5 below lists the connections of the application header, JA6.

Table 7-5: Application Header JA6 Connections

Application Header JA6					
Pin	**Header Name** **Circuit Net Name**	**MPU Pin**	**Pin**	**Header Name** **Circuit Net Name**	**MPU Pin**
1	DREQ NC	NC	2	DACK NC	NC
3	TEND NC	NC	4	STBYn NC	NC
5	RS232TX NC	NC	6	RS232RX NC	NC
7	SCIbRX NC	NC	8	SCIbTX NC	NC
9	SCIcTX NC	NC	10	SCIbCK NC	NC
11	SCIcCK NC	NC	12	SCIcRX NC	NC
13	M1_Toggle M1_TOG	K2	14	M1_Uin NC	NC
15	M1_Vin NC	NC	16	M1_Win NC	NC
17	EXT_USB_VBUS NC	NC	18	Reserved NC	NC
19	EXT_USB_BATT NC	NC	20	Reserved NC	NC
21	EXT_USB_CHG NC	NC	22	Reserved NC	NC
23	Unregulated_VCC NC	-	24	Vss GROUND	-

7.2 Pin Headers

This RSK+ board is equipped with a header that connects specific MPU pins separately from the application headers. Please check the option link when using it.

Table 7-6 below lists the connections of the Pin header, CN1.

Table 7-6: Pin Header CN1 Connections

Pin Header CN1					
Pin	**Circuit Net Name**	**MPU Pin**	**Pin**	**Circuit Net Name**	**MPU Pin**
1	P01_6	D2	2	P01_7	C1
3	P02_0_CAN1_TX	E3	4	P02_2	F3
5	P21_5	C7	6	P02_3_CAN1_RX	E1
7	P18_6_MISO	C15	8	NC	-
9	GROUND	-	10	GROUND	-
11	DIP_SW1_18_M1_TRDCLK (P13_6)	M13	12	BSC_A17 (P02_1)	D1
13	EEPROM_SCL (P13_2)	L10	14	EEPROM_SDA (P13_3)	N12
15	DIP_SW2_18_M1_TRCCLK	M12	16	BSC_A00_33	K1
17	ETH_LED1_MDV2	D9	18	ETH_LED3_MDV3	A9
19	3.3V	-	20	5.0V	-

Table 7-7 below lists the connections of the Pin header, CN3.

Table 7-7: Pin Header CN3 Connections

Pin Header CN3					
Pin	**Circuit Net Name**	**MPU Pin**	**Pin**	**Circuit Net Name**	**MPU Pin**
1	5.0V	-	2	3.3V	-
3	MCLK5 (P24_1)	B5	4	MDAT5 (P24_2)	C5
5	MCLK4 (P23_7)	D6	6	MDAT4 (P24_0)	A5
7	TRACE_D6_BSC_D06 (P21_7/MCLK3)	B7	8	TRACE_D7_BSC_D07 (P22_0/MDAT3)	A7
9	GROUND	-	10	GROUND	-
11	5.0V	-	12	3.3V	-
13	PMOD3A_INT_BSC_A12 (P03_5/MCLK2)	G1	14	PMOD2A_INT_BSC_A11 (P03_6/MDAT2)	G4
15	TRACE_D2_BSC_D02 (P21_3/MCLK1))	A8	16	TRACE_D3_BSC_D03 (P21_4/MDAT1)	E7
17	CS_TRACE_D0_BSC_D00 (P21_1/MCLK0))	B8	18	TRACE_D1_BSC_D01 (P21_2/MDAT0)	C8
19	GROUND	-	20	GROUND	-

8. Code Development

8.1 Overview

There are several ways to debug the code for this device:
Connect CPU Board to PC through SEGGER development tool J-Link® OB that is mounted on CPU Board.
Connect CPU Board to PC through each emulator.
Refer to the manufacturer's website for more details about each emulator.

8.2 Mode Support

The MPU supports various boot modes configured with RSK+ board. Details of the modifications required can be found in section 6.3. All other MPU operating modes are configured within the MPU's registers, which are listed in the RZ/N2L Group User's Manual: Hardware.

Only ever change the MPU operating mode whilst the RSK+ is turned off; otherwise the MPU may become damaged as a result.

8.3 Address Space

For the MPU address space details, refer to the 'Address Space' section of RZ/N2L Group User's Manual: Hardware.

9. Precautions For Use

9.1 About voltage conversion using level shifter

Level shifters are used to connect signals between different voltage power domain in this board, but must be take care with the following signals.

- A0
  A level shifter is inserted to adjust the amplitude of the "A0" signal at the JA3-A connector to 3.3V when VCC1833_1=1.8V, but we don't guarantee the operation of the "A0" signal, including the AC timing.
  When using the JA3-A connector, please understand the above, and if customer use "P05_4" as "A0" on customer's board, please supply 3.3V to VCC1833_1 according to the electrical characteristics* of the device.
- MTCLKA, MTCLKB, MTCLKC, MTCLKD
  A level shifter is inserted to adjust the amplitude of each signal at the JA2-A and JA5-A connectors to 3.3V when VCC1833_3 = 1.8V, but we don‘t guarantee the operation of each signal including AC timing.
  When using JA2-A, JA5-A connectors, please understand the above, and if customer use "P13_5, P13_6, P13_7 and P14_0" as MTCLKA, MTCLKB, MTCLKC and MTCLKD on customer’s board, Please supply 3.3V to VCC1833_3 according to the electrical characteristics* of the device.

* : Please refer below.
RZ/N2L Group User’s Manual: Hardware (R01UH0955EJ)
48. Electrical Characteristics, Table 48.14 IO setting (DRCTLm register setting) condition (1 of 2)

10. Additional Information

Design and Manufacturing Information

The design and manufacturing information for this board “Renesas Starter Kit+ for RZ/N2L Design Package” is available from https://www.renesas.com/rskrzn2l.

- File Name：rskplus-rzn2l-v1-designpackage.zip
- Contents

Table 10-1: Renesas Starter Kit+ for RZ/N2L Design Package Contents

File Type	Content	File/Folder Name
File (txt)	Readme	Readme for schematic.txt
File (PDF)	Schematics	rskplus-rzn2l-v1-schematic.pdf
File (PDF)	Mechanical Drawing	rskplus-rzn2l-v1-mechdwg.pdf
File (PDF)	3D Drawing	rskplus-rzn2l-v1-3d.pdf
File (csv)	BOM	rskplus-rzn2l-v1-BOM.csv
Folder	Manufacturing Files	rskplus-rzn2l-Manufacturing Files
Folder	Design Files	rskplus-rzn2l-Design Files - Cadence

Technical Support

For information about the RZ/N2L Group microprocessors refer to the RZ/N2L Group Hardware Manual.

General information on Renesas microprocessors can be found on the Renesas website at:
https://www.renesas.com/

Trademarks

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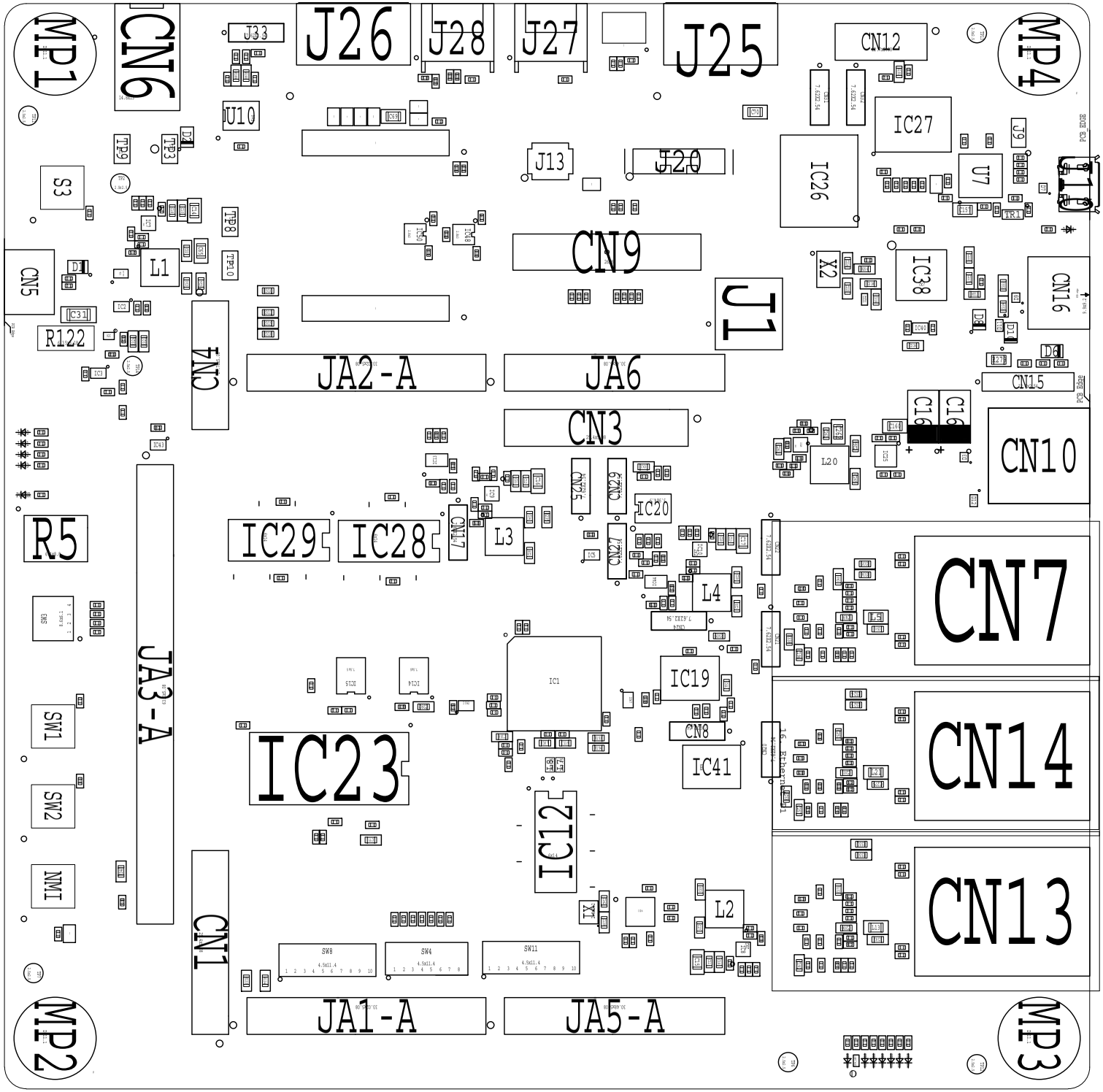
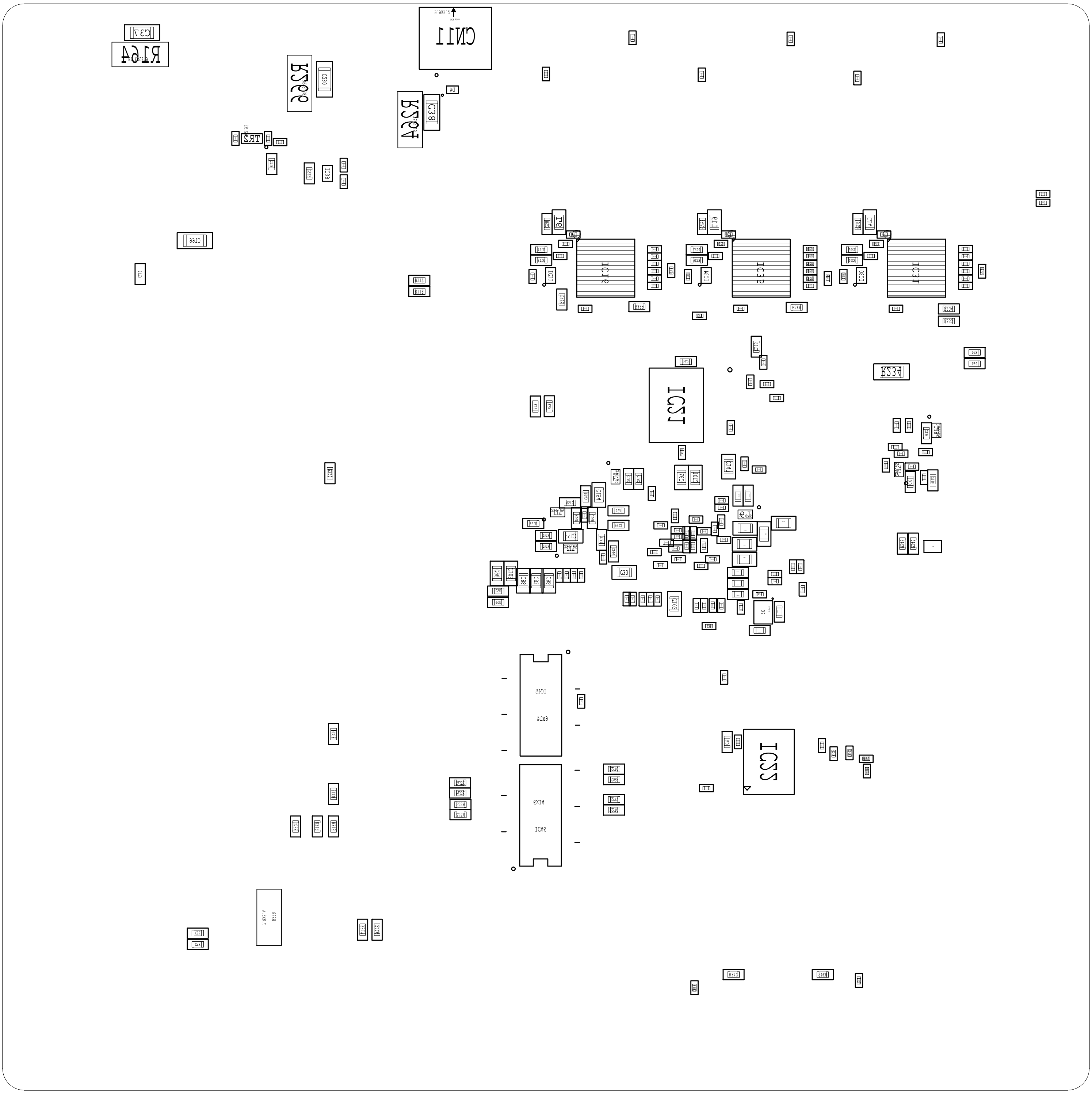
11. Appendix

Details on the placement of individual components on the board are shown on the next page.


MP1
MP4
MP2
MP3
CN6
J26
J28
J27
J25
CN12
U33
U10
IC27
IC26
U7
J9
J13
J20
S3
CN9
J1
CN5
L1
X2
IC38
CN16
R122
CN4
JA2-A
JA6
CN15
CN3
CN10
IC29
IC28
CN17
L3
IC20
L4
R5
CN7
JA3-A
IC19
CN8
IC41
IC23
IC12
CN14
SW1
SW2
NMI
CN1
L2
CN13
JA1-A
JA5-A



CN11
R164
C37
R256
R254
C38
TR2
IC16
IC35
IC31
IC33
R234

REVISION HISTORY	RZ/N2L Group Renesas Starter Kit+ for RZ/N2L User's Manual

Rev.	Date	Description	
		Page	Summary
1.00	Apr 20, 2022	-	First Edition issued
1.01	Sep 20, 2022	15 17 40	Change Default Enable of CLK in Figure 4-1 Change X1 to Fitted in Table 5-1 Change default configuration in Table 6-17
1.02	Dec 22, 2022	10 24, 25 46, 52 57, 58, 60 61 73, 77, 92 93	Correct I2C EEPROM description in Table 1-1 Removed RMII related description in Table 5-15, Table 5-16, Table 5-17 Correct SW4-6 setting of P22_0 in Table 6-23, Table 6-31 Removed RMII related description in Table 6-40, Table 6-41, Table 6-43. Removed Table 6-45, along with this, the table number in Chapter 6 has been shifted by one. Correct SW4-6 setting of P22_0 in Table 6-70, Table 6-82, Table 6-114 Add Table 6-115 as description of R193. Along with this, correct title of Table 6-114, and the table number in Chapter 6 has been shifted by one.
1.03	Apr 24, 2023	5 103	Deleted descriptions related to Schematics from the "How to use this manual" table. Added Design and Manufacturing Information to 10 Additional Information
1.04	Nov 17, 2023	103	Added 9 Precautions For Use, and subsequent chapter numbers has been shifted by one.
1.05	Oct 25, 2024	34	Correct MPU operation mode setting in Table 6-3

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