

RTKA210610DE0000BU

User's Manual: Evaluation Board

Industrial Analog and Power

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RTKA210610DE0000BU

Evaluation Board

Overview

The RTKA210610DE0000BU evaluation board (shown in [Figure 1](#)) features the [RAA210610](#). Capable of delivering up to 15A of continuous current, the RAA210610 is a single-channel, synchronous step-down power supply that is optimized for high power density applications without the need for airflow or heatsink.

The RTKA210610DE0000BU evaluation board is a 1.8inx3in 4-layer FR4 board with 2oz. copper on all layers. Operating from a single 7V to 54V wide input power rail, the RTKA210610DE0000BU evaluation board offers adjustable output voltages down to 0.6V and efficiencies of up to 97.6%. It is based on a valley current mode PWM control scheme with V_{IN} feed forward, which provides a fast transient response and excellent loop stability. The RTKA210610DE0000BU evaluation board is designed to program switching frequencies up to 2MHz, with the additional option of synchronizing to an external clock through the SYNC pin. A selectable Pulse Skipping Mode (PSM) with Diode Emulation Mode (DEM) is easily enabled to improve light-load efficiency for battery-related applications. The evaluation board also features output voltage tracking that is implemented through the SS/TRK pin.

By default, the board is set to a 5V output voltage with a 300kHz switching frequency.

Key Features

- Wide input voltage range from 7V to 54V
- Adjustable output voltage from 0.6V to 12V with $\pm 1.5\%$ accuracy over line, load, and temperature
- Up to 97.6% conversion efficiency
- High light-load efficiency with pulse-skipping DEM operation
- Programmable soft-start with output voltage tracking
- Prebias output start-up
- External frequency synchronization up to 1MHz
- Dedicated enable pin and PGOOD indicator
- UVLO, programmable overcurrent, overvoltage, and over-temperature
- Thermally enhanced 19mmx13mmx5.3mm HDA package

Specifications

The evaluation board is configured and optimized for the following operating conditions:

- $V_{IN} = 7V$ to 54V
- $V_{OUT} = 5V$
- $I_{OUT-MAX} = 15A$
- $f_{SW} = 300kHz$
- Set to PWM/CCM mode by default

Ordering Information

Part Number	Description
RTKA210610DE0000BU	RAA210610 single 15A power module evaluation board

Related Literature

For a full list of related documents, visit our website:

- [RAA210610](#) device page

Recommended Testing Equipment

- 0V to 54V power supply with at least 12A source current capability
- Electronic loads capable of sinking current up to 15A
- Digital Multimeters (DMMs)
- Oscilloscope with higher than 100MHz bandwidth

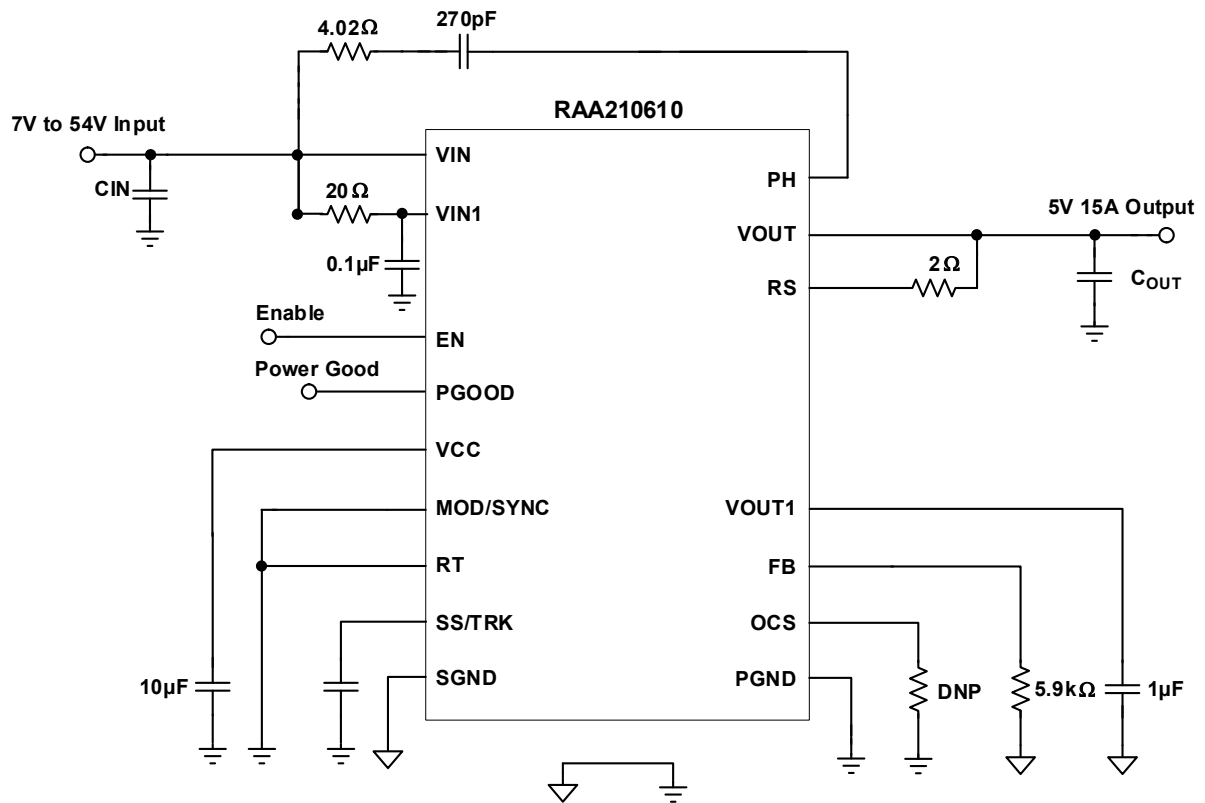


Figure 1. RTKA210610DE0000BU Block Diagram

1. Functional Description

The RTKA210610DE0000BU provides the peripheral circuitry to evaluate the feature set of the RAA210610. The evaluation board includes several connectors, test points, and jumpers that simplify the validation of the module. The converter is enabled and disabled by moving the jumper across the EN pin as shown in [Figure 2 on page 5](#). Connecting a jumper across the MOD/SYNC pin and VCC (as shown in [Figure 2](#)) enables the PSM/DEM mode of operation, which can lead to higher efficiencies at light loads. Resistors R_4 and R_5 are used to evaluate the tracking functionality. Selecting features like external frequency synchronization is performed by connecting the signal generator (square pulse waveform clock signal) to the MOD/SYNC pin. The output voltage (0.6V - 12V) and the switching frequency (300kHz to 2MHz) are programmed by changing the resistors as shown in [Figure 3 on page 5](#).

1.1 Quick Test Guide

1. Disable the module by moving the jumper across the EN pin as shown in [Figure 2 on page 5](#).
2. Use the appropriate cables to connect the DC input power supply to banana sockets J1 and J4 and the electronic load to sockets J3 and J2. Ensure that the polarity for the power leads is correct and the input voltage is within the operating range (7V - 54V) of the module. Use test points TP1 (VIN) and TP2 (PGND) for accurately measuring the input voltage.
3. Turn on the input power supply.
4. To enable the module, you can either move the jumper on J6 for EN pin to enable the module or remove the jumper completely.
5. To enable the PWM/CCM operation mode, you can move the jumper on J5 to PWM. To enable the PSM/DEM operation mode, you can move the jumper on J5 to DEM. To enable external frequency synchronization, remove the jumper on J5 and connect the external clock to TP8 (MOD/SYNC). PWM/CCM operation mode is selected by default.
6. Probe test points TP3 (VOUT) and TP4 (PGND) to observe the output voltage. The output voltage should read 5V.
7. Adjust the input voltage, V_{IN} , within the specified range and observe the output voltage. The output voltage variation should be within $\pm 1.5\%$.
8. Adjust the load current to within the specified range (0 - 15A) and observe the output voltage. The output voltage variation should be within $\pm 1.5\%$.
9. To change V_{OUT} , disconnect the evaluation board from the setup and populate a standard 0603 resistor at the R_2 placeholder location on the bottom layer. The Output Voltage Resistor Settings table in the [RAA210610](#) datasheet can be used as a reference for programming different output voltages. See the RAA210610 Design Guide Matrix table in the [RAA210610](#) datasheet for correct input and output capacitors, switching frequency, and output voltage combinations.
10. The switching frequency is modified by populating a standard 0603 resistor at the R_{11} placeholder location on the bottom layer. See Equation 2 in the [RAA210610](#) datasheet for selecting the correct value of R_{11} within the admissible operating range (300kHz - 2MHz).

1.2 Thermal Considerations and Current Derating

The board layout is very critical so that the module can operate safely and deliver the maximum allowable power. For the board to operate properly at high ambient temperature environments and carry full load current, the board layout needs to be carefully designed to maximize thermal performance. To achieve this, use enough trace width, copper weight, and proper connectors.

The RTKA210610DE0000BU evaluation board is capable of operating at 15A full load current at room temperature without the need for additional cooling systems. However, if the board is to operate at elevated ambient temperatures, the available output current may need to be derated. See the derated current curves in the [RAA210610](#) datasheet to determine the maximum output current that the evaluation board can supply.

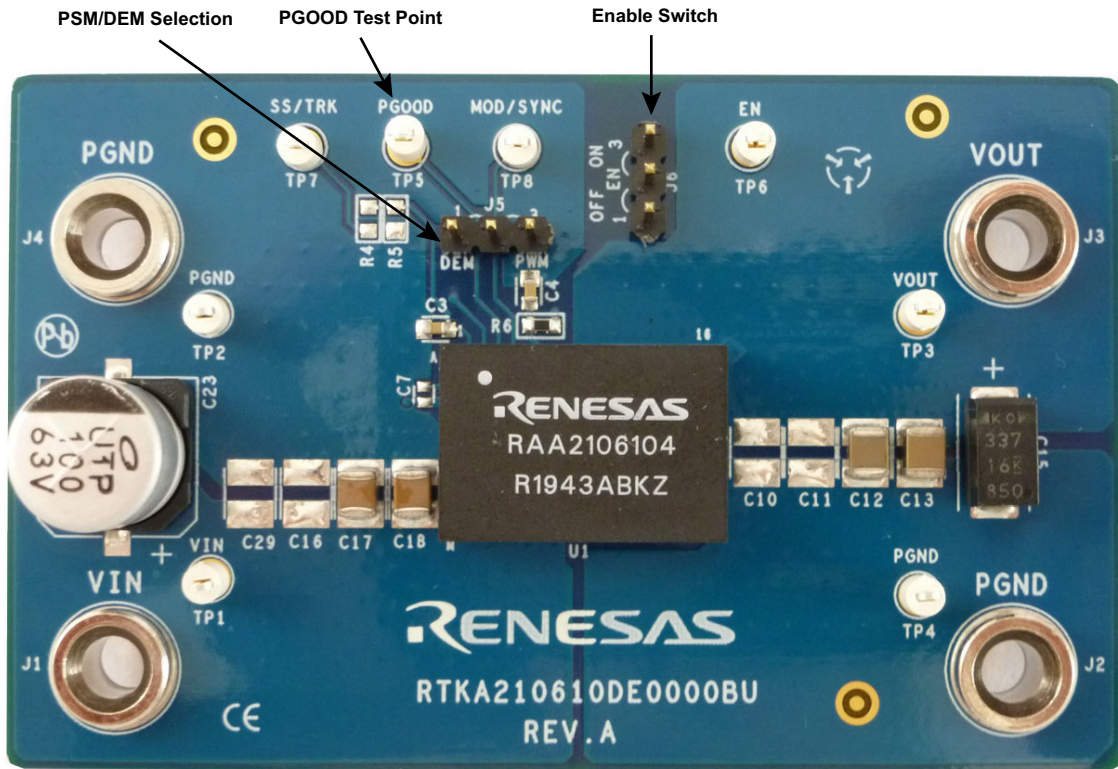


Figure 2. Top of Board

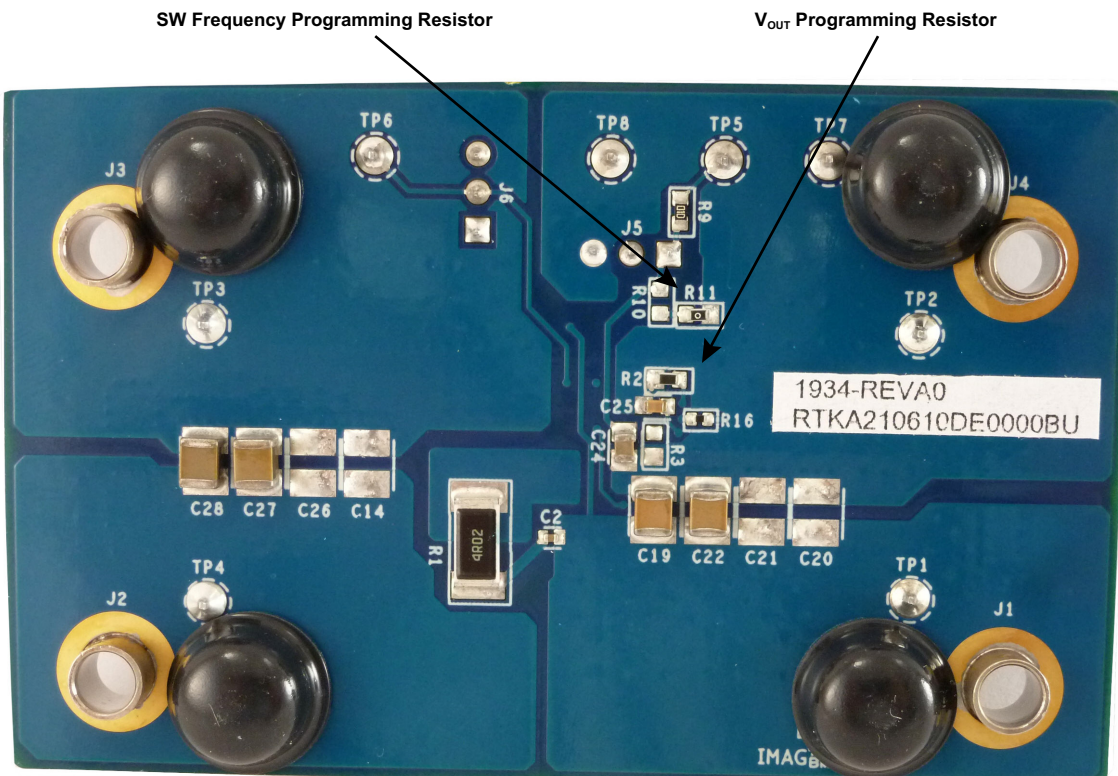


Figure 3. Bottom of Board

2. PCB Layout Guidelines

The RTKA210610DE0000BU evaluation board is a 1.8inx3in four-layer FR-4 board with 2oz. copper on all the layers. The board can be used as a single 15A reference design. See [Figures 8](#) through [13](#) for board layout information.

The RTKA210610DE0000BU board layout is optimized for electrical performance, low loss, and good thermal performance. Similar performance is obtained for designs involving RAA210610 while adhering to the following layout design tips:

2.1 Layout Considerations

- Place the input capacitors and high frequency decoupling ceramic capacitors between VIN and PGND, as close to the module as possible. The loop formed by the input capacitor, VIN pad, and PGND must be as small as possible to minimize the high-frequency noise. Place the output capacitors close to the load. Use short, wide copper planes to connect the output capacitors to the load to avoid any parasitic inductances and resistances. A layout example is shown in [Figures 4](#) and [5](#) on [page 7](#).
- Use large copper planes to minimize conduction loss and thermal stress for VIN, VOUT, and PGND. Use enough vias to connect the power planes in different layers.
- Use full ground planes in the internal layers (underneath the module) with shared SGND and PGND to simplify the layout design. Renesas recommends using slots (as shown in [Figure 6 on page 7](#)) to ensure that the switching current avoids the SGND pad of the module. Use as much GND plane as possible for the layer directly above the bottom layer (containing components such as input caps and output caps). Use the top and bottom layers to route the EN, VCC, and PGOOD signals.
- For a switching frequency of 300kHz and a 54V input, connect a 4.02Ω 0805 resistor and a 270pF 100V X7R 0603 capacitor in series from PH to VIN. Derate the resistor size for switching frequencies higher than 300kHz. Calculate the power dissipated in resistor R5 (P_{cal}) by using the formula $C \times V^2 \times f$, where:
 - $C = 270\text{pF}$
 - $V = \text{input voltage}$
 - $f = \text{frequency of operation}$
 For derating purposes, the nominal power handling capability of the resistor package size should be at least $P_{cal}/0.65$. The 65% derating is derived from the resistor operation at +100°C ambient temperature. Use a standard thick film chip resistor datasheet to find the correct resistor package size for different switching frequencies and input voltage.
- Make sure that UG1 and UG2 (D6 and K4) are connected externally through a PCB trace. Make a similar connection for the two EN pins (A6 and A8). See the pin configuration and descriptions in the [RAA210610](#) datasheet.
- Use a remote sensing trace to connect to the VOUT+ load to achieve a tight output voltage regulation. Route the remote sense trace underneath the GND layer and avoid routing the sense lines near noisy planes such as the PHASE node. Place a 2Ω resistor close to the RS pin to damp the noise on the traces.
- To avoid ground bouncing issues, place the VIN return and the VOUT return diagonally opposite to each other. This ensures that the switching noise generated by the power-train has minimal effect on the controller operation.
- Do not unnecessarily oversize the copper islands for the PHASE node. Because the phase nodes are subjected to very high dv/dt voltages, the parasitic capacitor formed between these islands and the surrounding circuitry tends to couple the switching noise. Ensure that none of the sensitive signal traces are routed close to the PHASE node plane.
- Place the VCC bypass capacitor underneath the VCC pin and connect its ground to the PGND pad. Connect the low side feedback resistor and the decoupling cap for VOUT1 to the SGND pad.

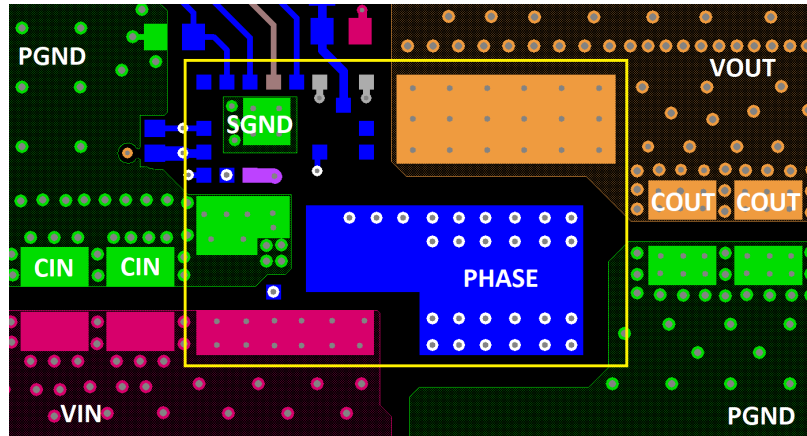


Figure 4. Layout Example - Top Layer

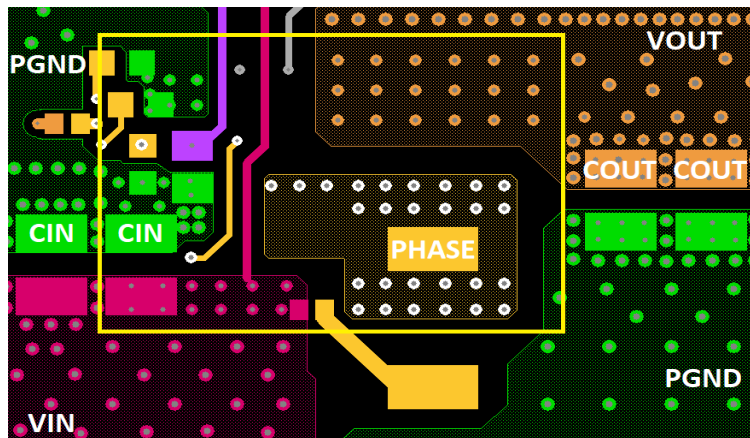


Figure 5. Layout Example - Bottom Layer

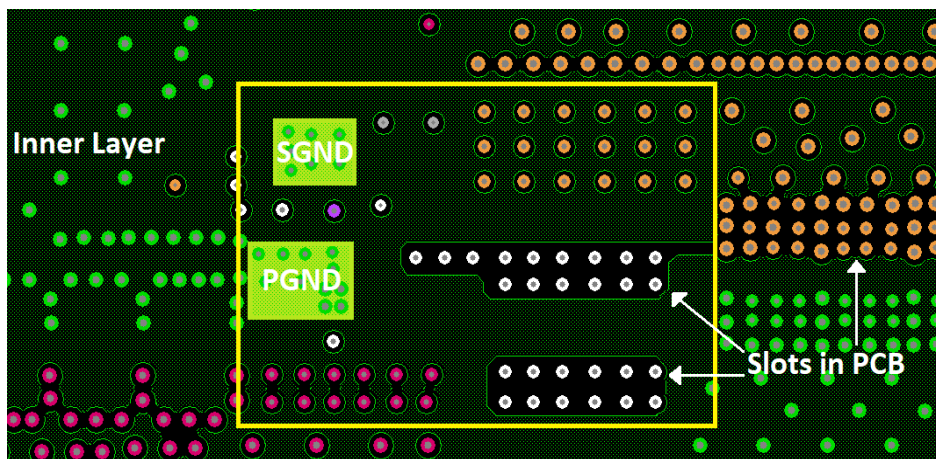


Figure 6. Layout Example - SGND is Connected to PGND Through Internal Layer

2.2 RTKA210610DE0000BU Schematic

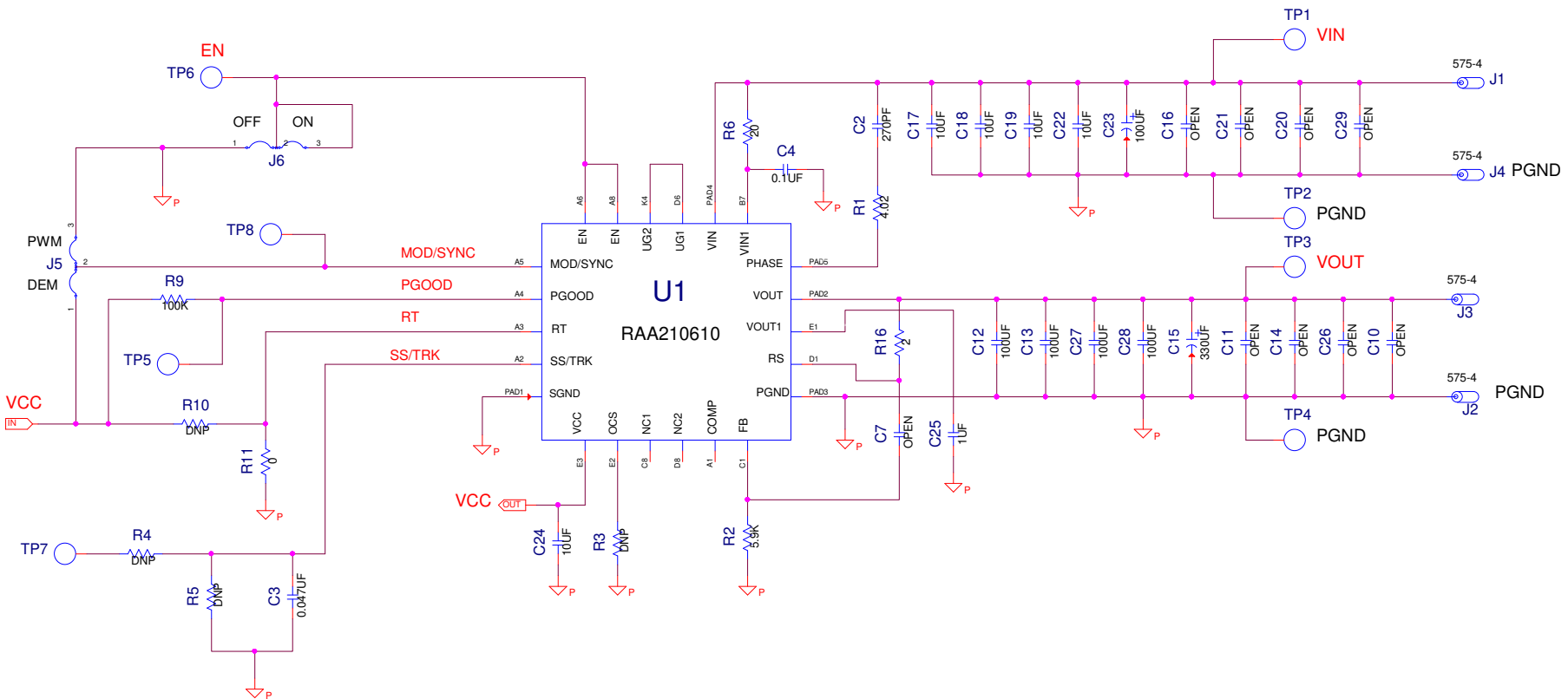


Figure 7. Schematic

2.3 Bill of Materials

Reference Designators	Qty	Value	Tol.	Voltage	Power	Package Type	Manufacturer	Part Number	Description
C15	1	330 μ F	\pm 20%	16V		2917	KEMET	T521X337M016ATE025	POSCAP
C12, C13, C27, C28	4	100 μ F	\pm 20%	16V		1210	Taiyo Yuden	EMK325ABJ107MM-P	Ceramic Capacitor
C10, C11, C14, C26	4	OPEN	\pm 20%	16V		1210			Ceramic Capacitor
C17, C18, C19, C22	4	10 μ F	\pm 10 %	100V		1210	Murata	GRM32EC72A106KE05L	Ceramic Capacitor
C16, C20, C21	3	OPEN	\pm 10 %	100V		1210			Ceramic Capacitor
C23	1	100 μ F	\pm 20%	63V		Radial, Can - SMD	Nichicon	UUX1J101MNL1GS	Aluminum Electrolytic Capacitor
C3	1	0.047 μ F	\pm 5%	25V		0603	AVX	06033C473KAT2A	Ceramic Capacitor
C4	1	0.1 μ F	\pm 10%	100V		0603	Samsung	CL10B104KC8NNNC	Ceramic Capacitor
C25	1	1.0 μ F	\pm 10%	25V		0603	Murata	GCM188R71E105KA64D	Ceramic Capacitor
C7	1	OPEN	\pm 10%	25V		0402			Ceramic Capacitor
C2	1	270pF	\pm 5%	100V		0603	Kemet	C0402C271J1GAC7867	Ceramic Capacitor
C24	1	10 μ F	\pm 10%	16V		0805	Samsung	CL21B106KOQNNNE	Ceramic Capacitor
J1-J4	4					CONN-JACK	Keystone	575-4	Solder Mount Banana Jack
TP1-TP8	8					CONN-MINI TEST POINT	Keystone	5002	Miniature PC Test Point
J5, J6	2					CONN-HEADER	BERG/FCI	68000-236HLF	Three Pin Jumper
U1	1					19X13 HDA	Renesas	RAA210610	54V 15A Step-Down Power Module
R1	1	4.02 Ω	\pm 1%		1W	2512	Stackpole	RMCF2512FT4R02	Thick film Chip Resistor
R2	1	5.9k Ω	\pm 1%		1/10W	0603	Panasonic	ERJ-3EKF5901V	Thick Film Chip Resistor
R3-R5, R10	4	DNP	\pm 1%		1/10W	0603			Thick Film Chip Resistor
R6	1	20 Ω	\pm 1%		1/10W	0603	Panasonic	ERJ-3EKF20R0V	Thick Film Chip Resistor
R11	1	0 Ω			1/10W	0603	Venkel	CR0603-10W-000T	Thick Film Chip Resistor
R9	1	100k Ω	\pm 1%		1/10W	0603	Venkel	CR0603-10W-1003FT	Thick Film Chip Resistor
R16	1	2 Ω	\pm 1%		1/16W	0402	Venkel	CR0402-16W-02R0FT	Thick Film Chip Resistor

2.4 RTKA210610DE0000BU PCB Layout

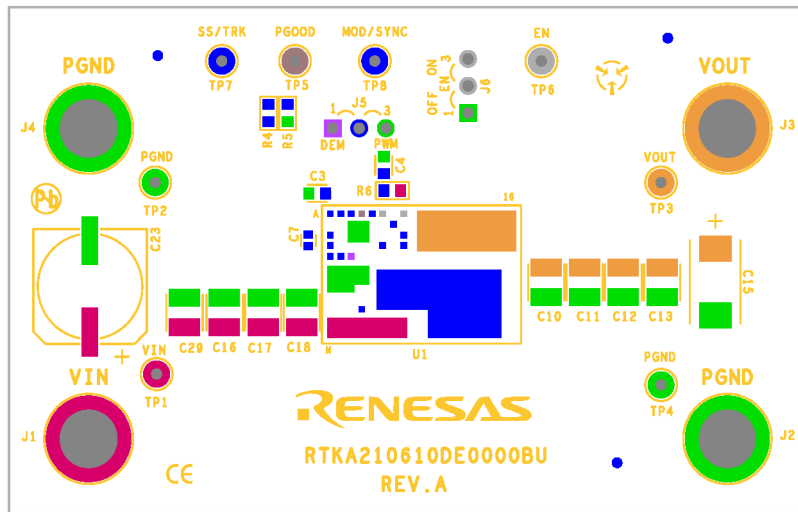


Figure 8. Silkscreen Top

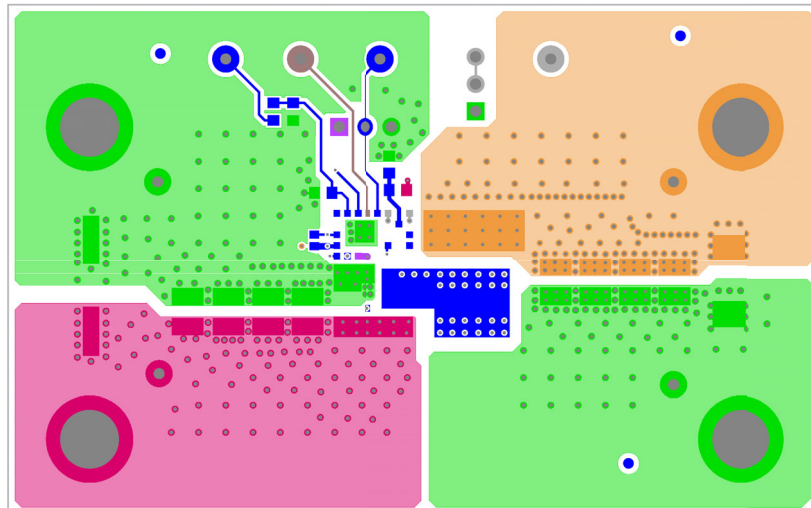


Figure 9. Top Layer Component Side

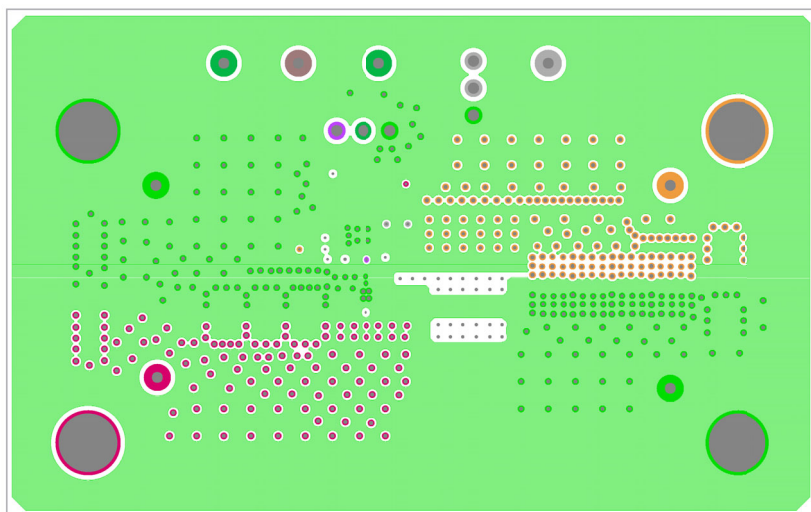


Figure 10. Inner Layer 2

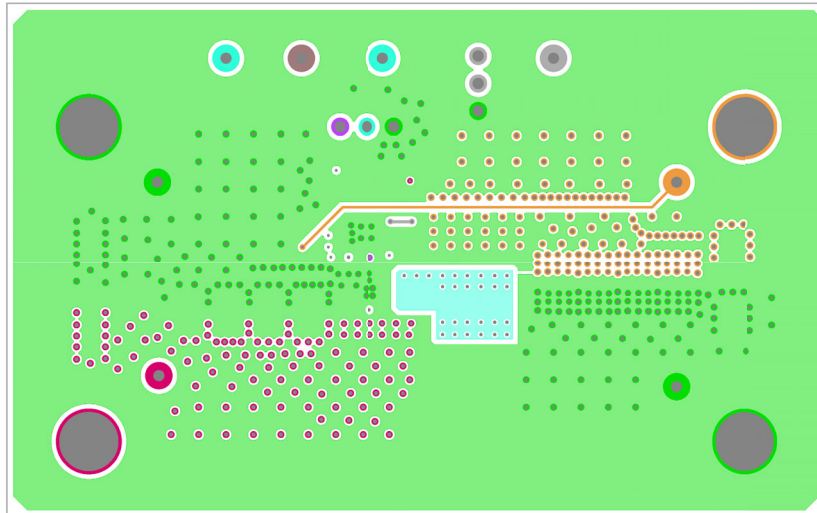


Figure 11. Inner Layer 3

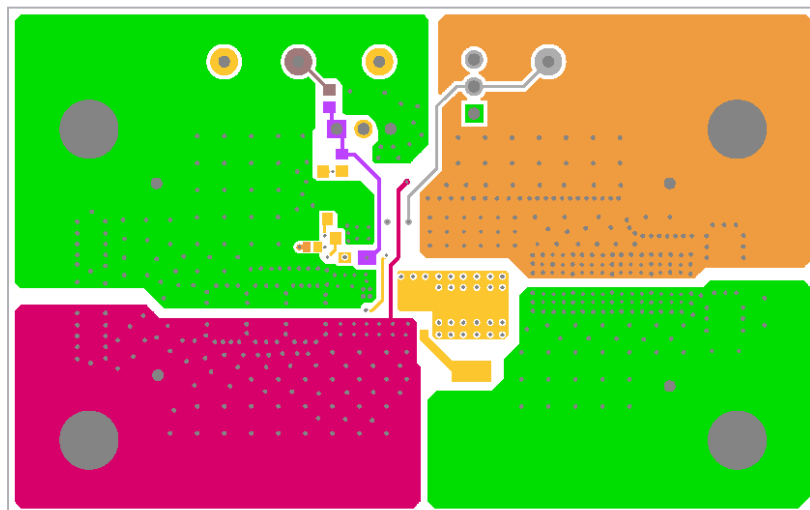


Figure 12. Bottom Layer Solder Side

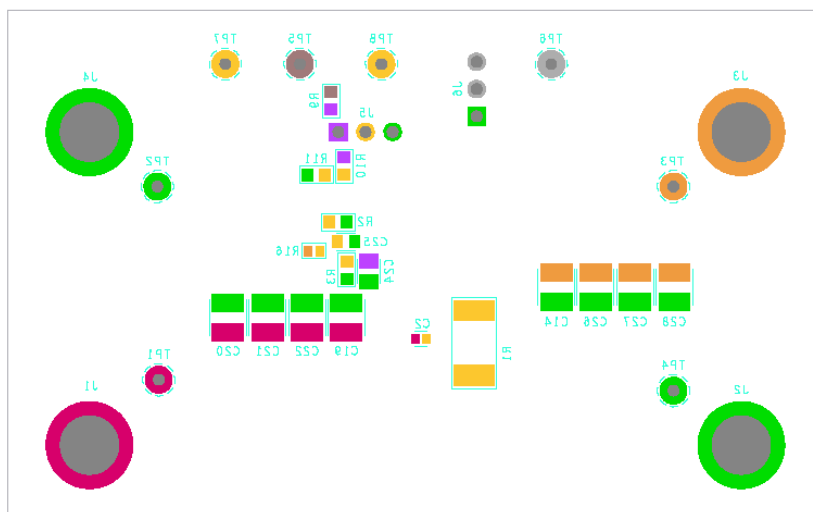


Figure 13. Silkscreen Bottom

3. Typical Evaluation Board Performance Curves and Data

The following data was acquired using the RTKA210610DE0000BU evaluation board at +25°C ambient and free air 0LFM.

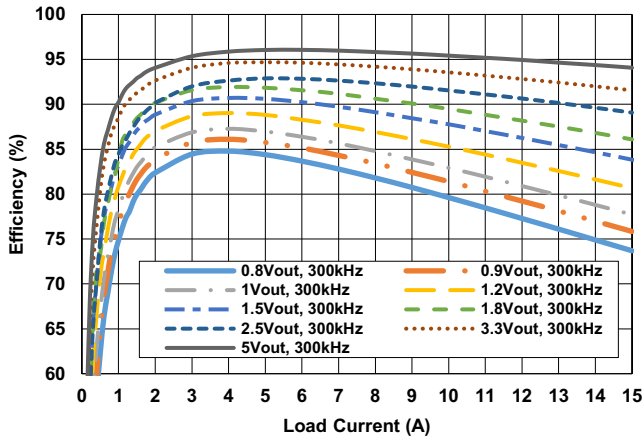


Figure 14. Efficiency vs Load Current at $V_{IN} = 12V$, PWM/CCM Mode

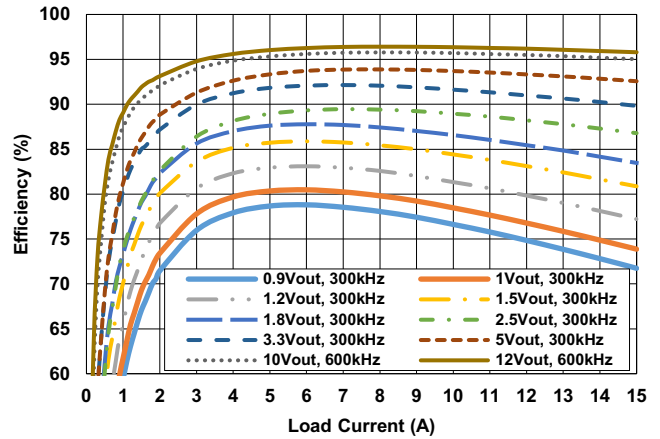


Figure 15. Efficiency vs Load Current at $V_{IN} = 24V$, PWM/CCM Mode

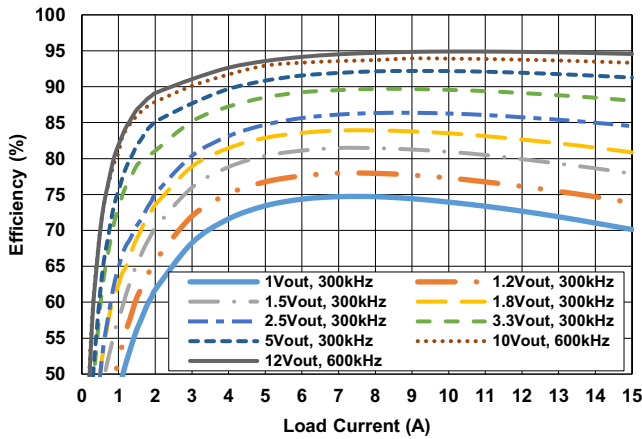


Figure 16. Efficiency vs Load Current at $V_{IN} = 36V$, PWM/CCM Mode

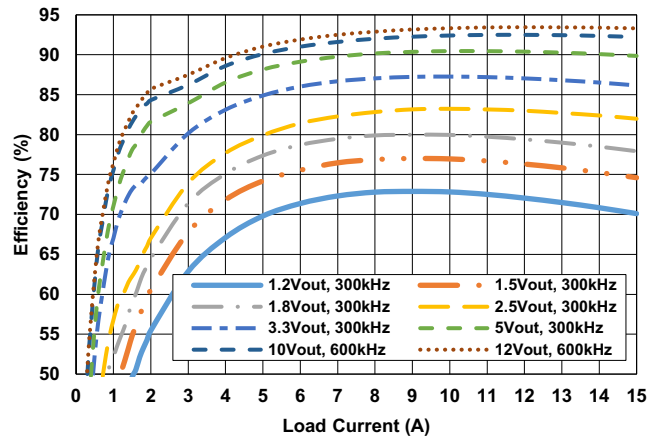


Figure 17. Efficiency vs Load Current at $V_{IN} = 48V$, PWM/CCM Mode

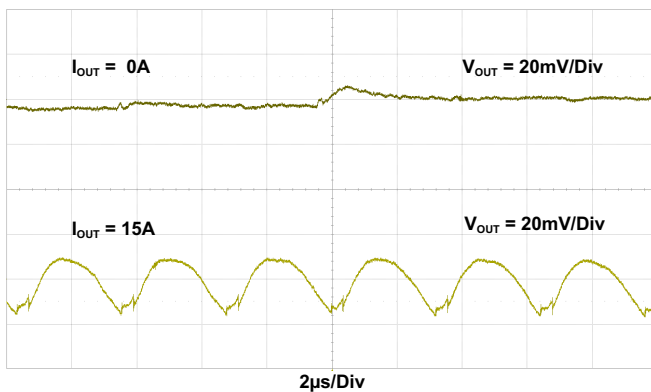


Figure 18. Output Ripple, $V_{IN} = 48V$, $V_{OUT} = 5V$, PSM/DEM Mode, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

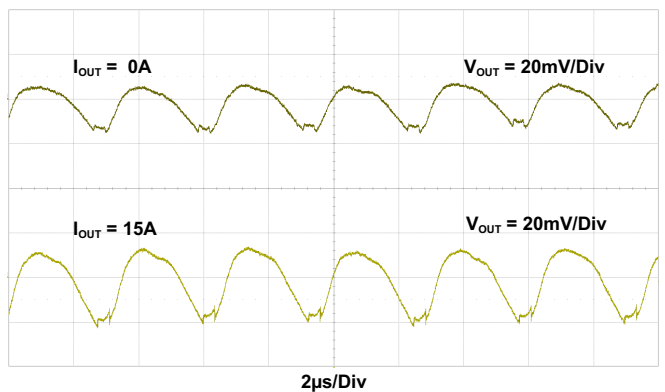


Figure 19. Output Ripple, $V_{IN} = 48V$, $V_{OUT} = 5V$, $f_{SW} = 300kHz$, PWM/CCM Mode, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

Operating condition: $V_{IN} = 48V$, $f_{SW} = 300kHz$, PWM/CCM Mode, unless otherwise noted.

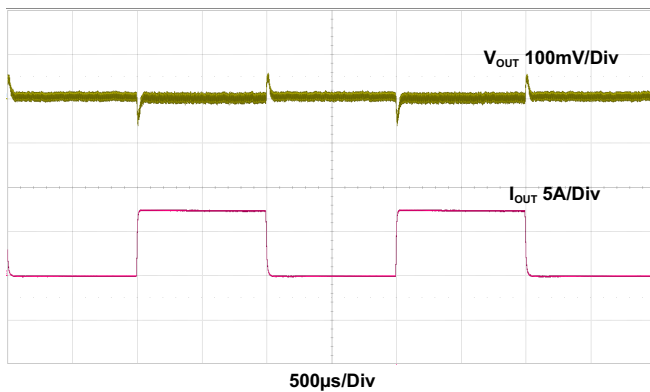


Figure 20. Transient Response, $V_{OUT} = 5V$, $I_{OUT} = 0A$ to $7.5A$, $2.5A/\mu s$ Step Load, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

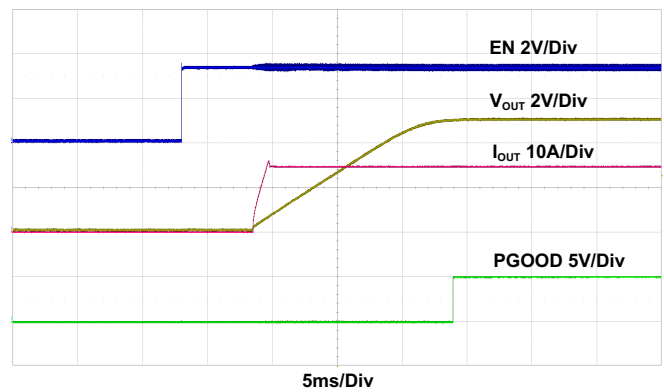


Figure 21. Start-Up Waveform, $V_{OUT} = 5V$, $I_{OUT} = 15A$, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

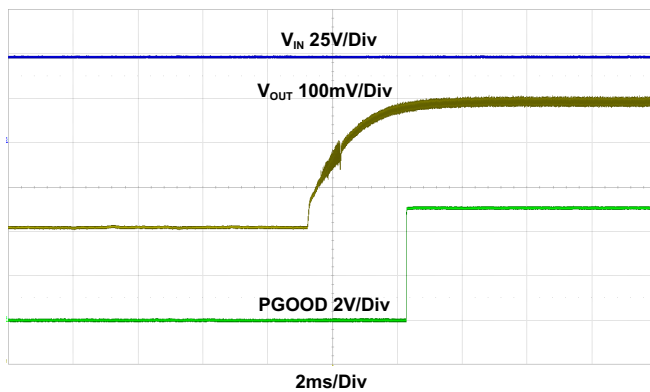


Figure 22. Prebiased Power-Up Waveform, Prebiased Voltage = $4.7V$, $V_{OUT} = 5V$, $I_{OUT} = \text{No Load}$, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

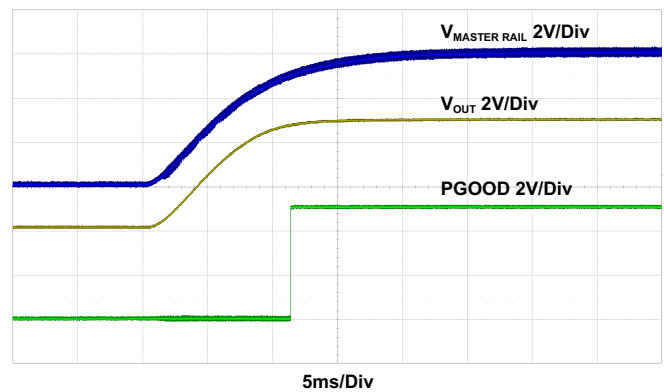


Figure 23. Tracking Operation Waveform, $V_{OUT} = 5V$, $V_{MASTER RAIL} = 6V$, $I_{OUT} = 15A$, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

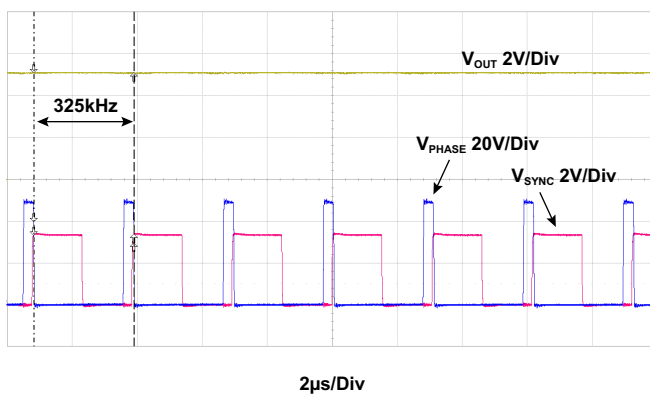


Figure 24. External Frequency Synchronization Waveform, $V_{OUT} = 5V$, $f_{SYNC} = 325kHz$, $I_{OUT} = 0A$, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

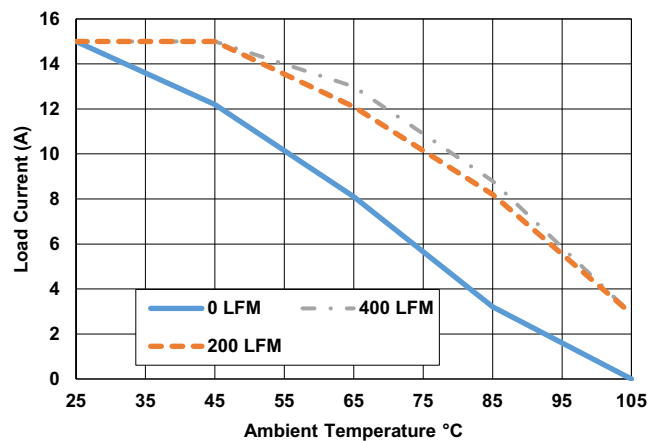


Figure 25. Derating Curve, $V_{OUT} = 5V$, $C_{OUT} = 4 \times 100\mu F$ Ceramic + $1 \times 330\mu F$ POSCAP

4. Revision History

Rev.	Date	Description
1.01	Mar.10.20	Updated Figure 1.
1.00	Jan.16.20	Initial release

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