SLG47115V Evaluation Board Quick Start

This user manual provides basic guidelines for developers to get familiar with the Evaluation Board for SLG47115V. It consists of the functional description of the board.

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1. Terms and Definitions

ADB	Advanced Development Board
EVB	Evaluation Board
PDB	Pro Development Board
TP	Test Point

2. References

[1] SLG47115, Datasheet, Renesas Electronics.

[2] NXP «I2C-bus specification and user manual». User manual. UM10204–Rev.6, 4 April 2014. https://www.nxp.com/docs/en/user-guide/UM10204.pdf

3. Introduction

SLG47115V Evaluation Board (EVB) (see Figure 1) allows to get acquainted with SLG47115's functionality, especially the H-Bridge/Half-Bridge functions, and allows the User to test the power part of the chip.

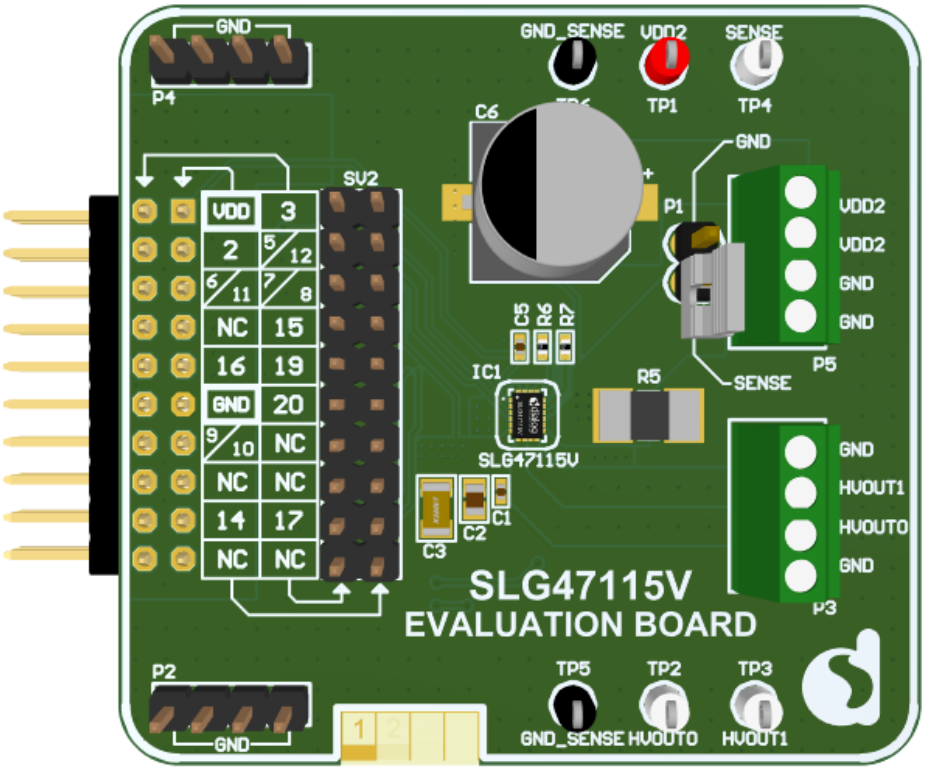


Figure 1. SLG47115V EVB General View

You can emulate/program the SLG47115 chip with the Advanced Development Board (ADB) or Pro Development Board (PDB). Insert EVB expansion connector SV1 into the ADB or PDB socket. In the case with PDB connect EVB expansion connector SV1 into the socket connector. The first pin locates at the right connector side. See Figure 2.

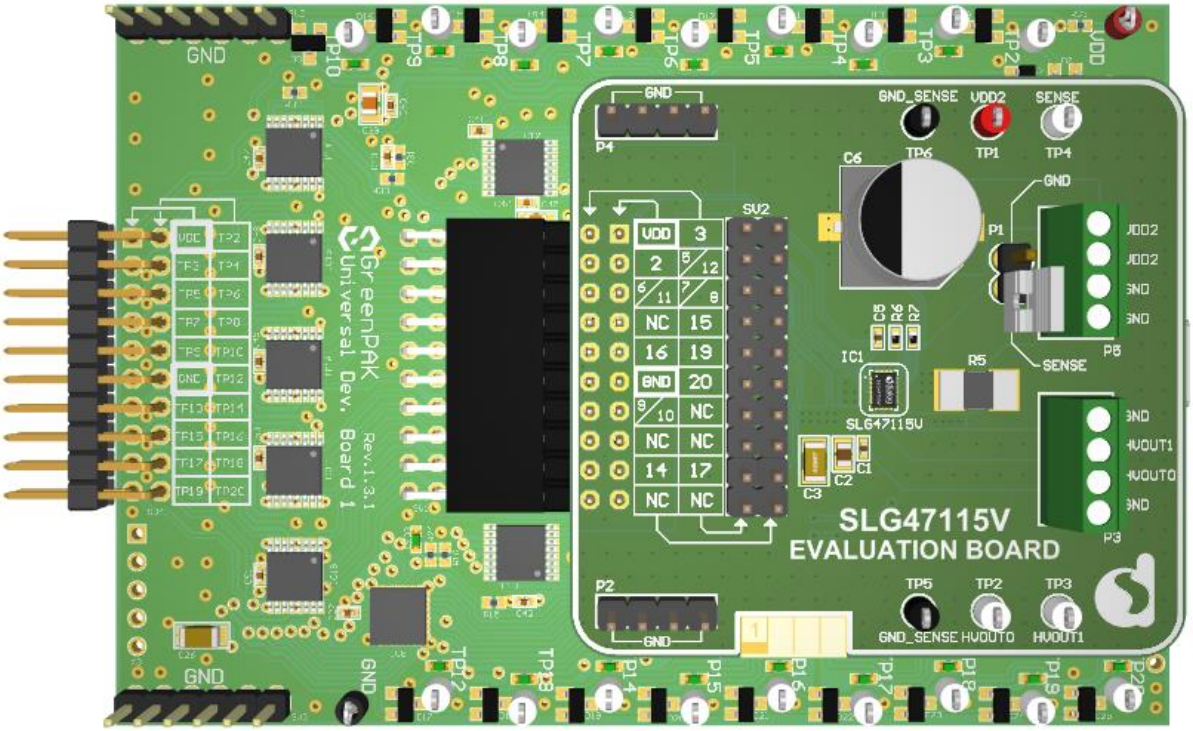


Figure 2. SLG47115V EVB Connected into ADB

4. Functional Description

4.1 Expansion Connectors and Test Points

4.1.1. Expansion Connectors SV1 and SV2

There are two male headers SV1 and SV2 placed on the board.

The SV1 male header is used only to connect SLG47115V Evaluation Board to the GreenPAK Advanced Development Platform or the GreenPAK Pro Development Platform. Therefore, SV1 has a connection with Chip Low Voltage IO Pins only. High Voltage Pins 6, 7, 8, 9, 10, and 11 are not connected to SV1 by default.

Only in case V_{DD} = V_{DD2}, it is possible to connect High Voltage Pins 6, 7, 8, 9, 10, and 11 to SV1 by installing resistors R2-R4 on the board.

The SV2 male header has a connection with all the chip pins and can be used in the debugging process. This allows monitoring the chip functionality by connecting measuring devices (oscilloscope, voltmeter, logic analyzer) to SV2.

Male headers SV1 and SV2 functions can be found in Table 1.

Table 1. Male Headers SV1 and SV2 Functions

Header	Marked on Board	IC Pin	Function	Notes
SV1.1 SV2.1	V_{DD}	Pin 1	V_{DD}	
SV1.2 SV2.2	3	Pin 3	GPI	
SV1.3 SV2.3	2	Pin 2	GPIO0	
SV1.4 SV2.4	5, 12	Pin 5, 12	SENSE	Connected to SV1 through 200R resistor R1
SV1.5 SV2.5	6, 11	Pin 6, 11	HV_{DD}	Not Connected to SV1. Connection option through resistor R2
SV1.6 SV2.6	7, 8	Pin 7, 8	HV_GPO0	Not Connected to SV1. Connection option through resistor R3
SV1.7 SV2.7	NC			
SV1.8 SV2.8	15	Pin 15	GPIO2	
SV1.9 SV2.9	16	Pin 16	GPIO3	
SV1.10 SV2.10	19	Pin 19	GPIO5	
SV1.11 SV2.11	GND	Pin 18	GND	GND connected through PTC protection to SV1
SV1.12 SV2.12	20	Pin 20	GPIO6	

Header	Marked on Board	IC Pin	Function	Notes
SV1.13 SV2.13	9, 10	Pin 9, 10	HV_GPO1	Not Connected to SV1. Connection option through resistor R4
SV1.14 SV2.14	NC			
SV1.15 SV2.15	NC			
SV1.16 SV2.16	NC			
SV1.17 SV2.17	14	Pin 14	GPIO1	
SV1.18 SV2.18	17	Pin 17	GPIO4	
SV1.19 SV2.19	NC			
SV1.20 SV2.20	NC			

4.1.2. Power Supply and Power Selection Connector (P5)

V_{DD2} is supplied from an external power supply through the connector P5.

For P5 connector pin functions refer to Table 2.

Table 2. P5 Connector Functions

Header	Marked on Board	IC Pin	Function	Notes
P5.1	V_{DD2}	Pin 6, 11	V_{DD2}	
P5.2	V_{DD2}	Pin 6, 11	V_{DD2}	
P5.3	GND			
P5.4	GND			

Using test point TP1 (V_{DD2}) the User can control the voltage on V_{DD2} rail.

Capacitor C6 is used to decouple noise on the V_{DD2} power line. It is optional and is not board mounted by default. It is possible to install it by the User independently, for example, when testing a high-power motor close to the chip maximum capabilities.

4.1.3. High-voltage Output Connector (P3)

The connector P3 is used for connecting the electric motor or another high-power load powered by V_{DD2}. For P3 connector pin functions see Table 3.

Table 3. P3 Connector Functions

Header	Marked on board	IC Pin	Function	Notes
P3.1	GND	Pin 4, 13	GND	Test point TP5, TP6
P3.2	HVOUT1	Pin 9, 10	HV_GPO 1	Test point TP3 (HVOUT1) mounted on board
P3.3	HVOUT0	Pin 7, 8	HV_GPO 0	Test point TP2 (HVOUT0) mounted on board
P3.4	GND	Pin 4, 13	GND	Test point TP5, TP6

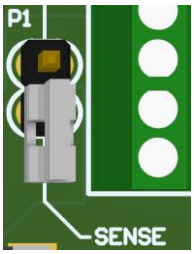
Test points TP2 (HVOUT0), TP3 (HVOUT1) make possible controlling the output signals.

4.1.4. Current Measurement Shunt P1

Resistor R5 is connected to the input SENSE (Pin 5, 12) of the Current Sense Comparator macrocells, which allow controlling the load current of each H-Bridge. This function can be switch on/off with the help of Jumper P1.

Jumper P1 functions can be found in Table 4.

Table 4. Jumper P1 Functions

Jumper	Marked on Board	IC Pin	Function	Notes
P1		Pin 5, 12	Connect SENSE to GND	OPEN – Current Sense Comparator0 current control function is turned on CLOSED – Current Sense Comparator0 current control function is turned off

It is possible to control voltage on resistor R5 by connecting measuring devices (voltmeter, oscilloscope) to the test point TP4 (SENSE), installed on the board.

Also, there are two test points TP5, TP6 (GND_SENSE) installed on the board. They are connected to Pin 4 (GND) and Pin 13 (GND) and can be used for measurements **only**.

4.1.5. I²C Pull-Up Resistors

If the board is not connected to the GreenPAK Advanced Development Platform or the GreenPAK Pro Development Platform and used separately, for example, with a programmed chip for debugging in the final production, two pull-up resistors, R6 and R7 for SDA and SCL, should be installed on the board. Their resistance should be calculated according to the procedure described in Reference [2] (Section 2 References).

4.1.6. Protection Digital GND from Power GND

PTC1 is used for protecting digital GND from power GND (HV_GND). The maximum current that can flow from power GND through PTC1 to digital GND pin is limited to 50 mA.

5. Board Design

5.1 Board Dimensions

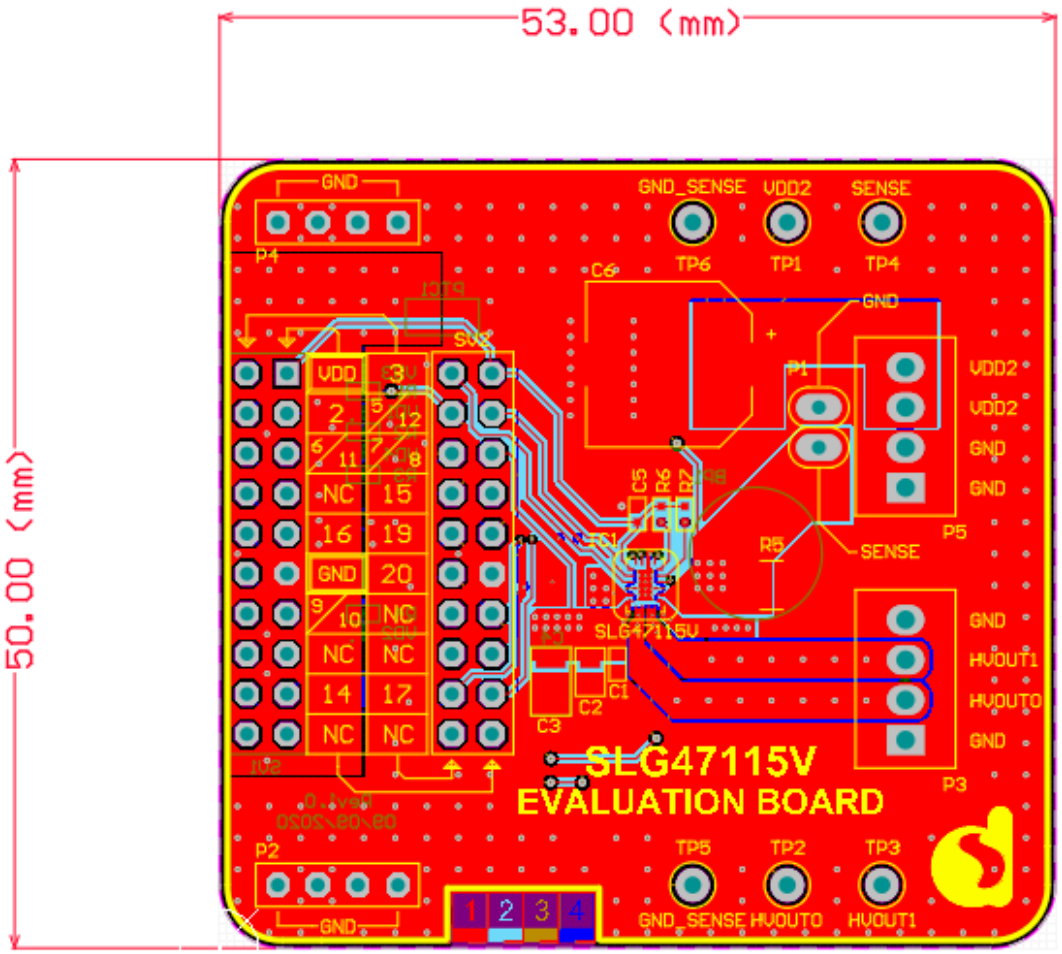


Figure 3. SLG47115V Evaluation Board Dimensions

5.2 Top View

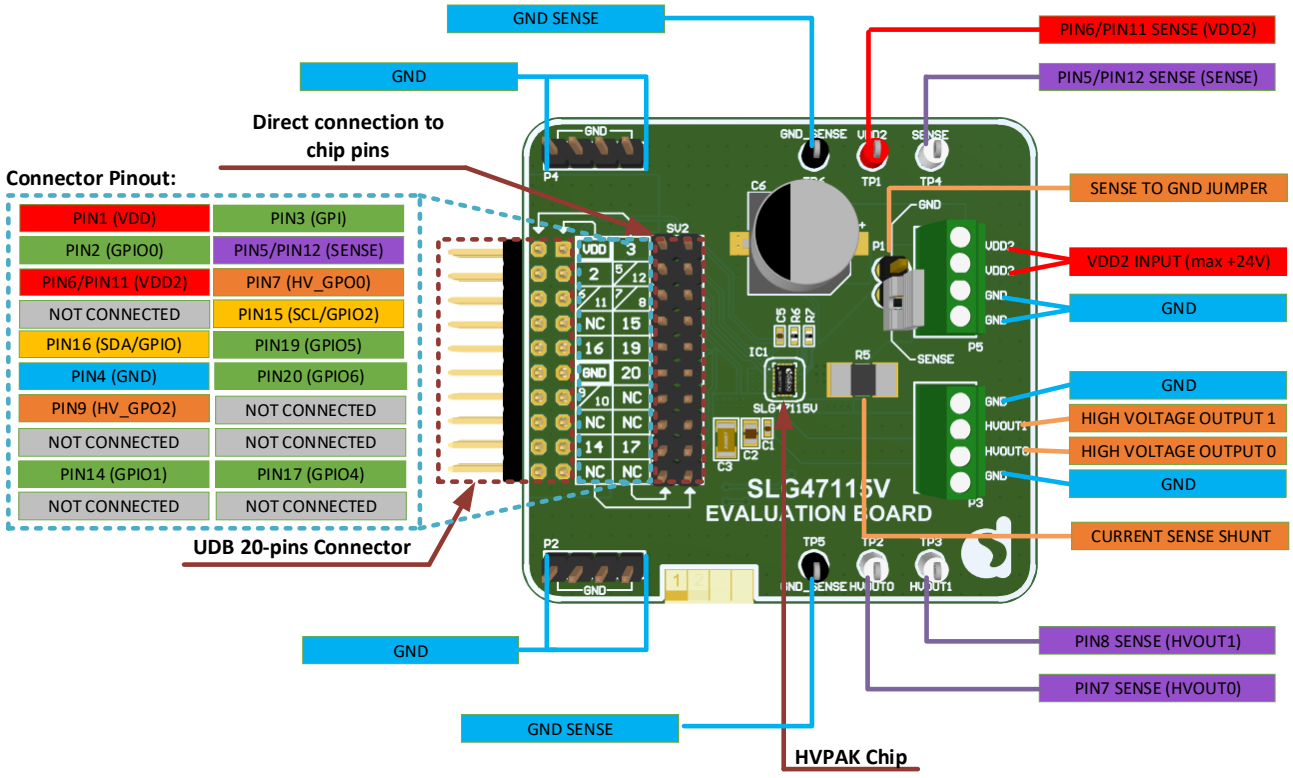


Figure 4. SLG47115V Evaluation Board, Top View

5.3 Board Schematic

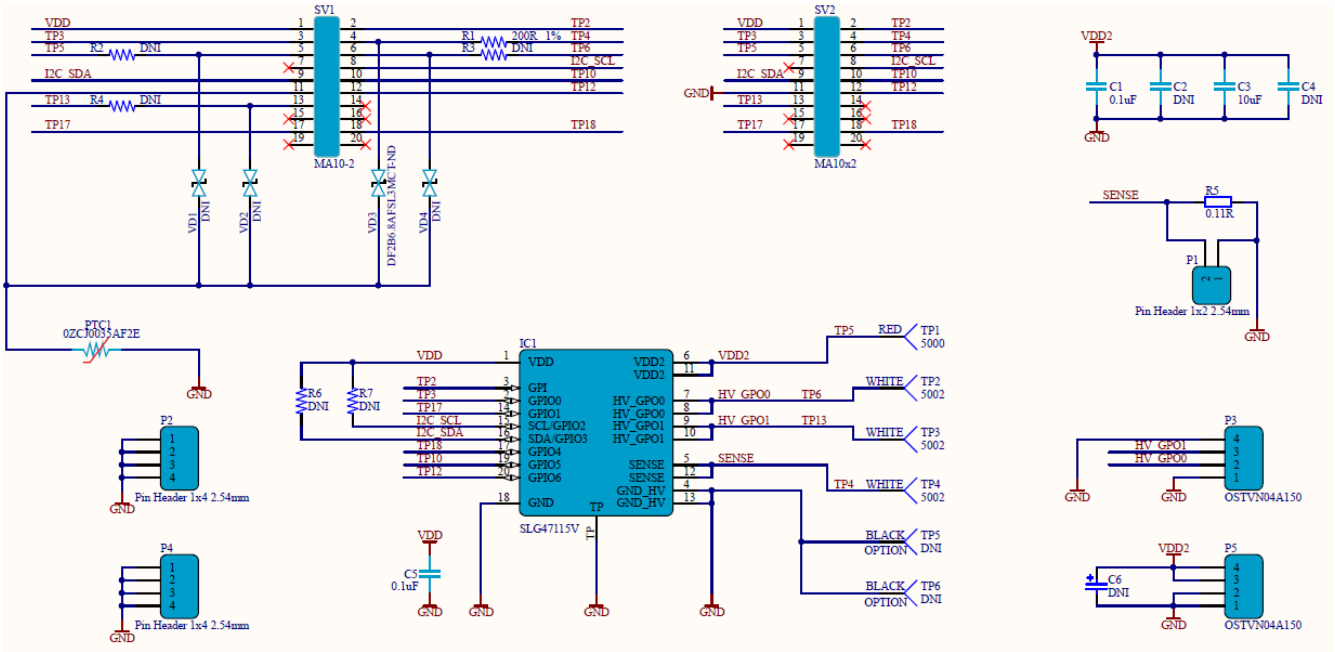


Figure 5. SLG47115V Evaluation Board Schematic

5.4 BOM

#	Designator	Description	Manufacturer Part Number	Footprint	Quantity
1	BP1	BUMPER CYLIN 0.312" DIA BLK	70006431426		1
2	C1, C5	CAP CER 0.1UF 50V X7R 0402	C1005X7R1H104K050BB	C0402	2
3	C2, C4	DNI		C0805, C1206	2
4	C3	CAP CER 10UF 50V X5R 1206	CL31A106KBHNNNE	C1206	1
5	C6	DNI		Size code: G	1
6	IC1	PROGRAMMABLE MIXED-SIGNAL MATRIX WITH H-BRIDGE FUNCTIONS	SLG47105V	STQFN-20-2.0X3.0	1
7	JP1	CONN JUMPER SHORTING 2.54mm GOLD	NPC02SXON-RC		1
8	P1	CONN HEADER VERT 2POS 2.54mm	5-146268-1	1x2 2.54mm	1
9	P2, P4	CONN HEADER VERT 4POS 2.54mm	61300411121	1x4 2.54mm	2
10	P3, P5	TERM BLK 4P SIDE ENT 2.54mm PCB	OSTVN04A150	1x4 2.54mm	2
11	PTC1	PTC RESET FUSE 30V 350MA 1206	0ZCJ0035AF2E	PTC1206	1
12	R1	RES 200 OHM 1% 1/16W 0402	CRCW0402200RFKED	R0402	1
13	R2, R3, R4	DNI		R0402	3
14	R5	RES 0.11 OHM 1% 1/2W 2010	WSL2010R1100FEA	R2512	1
15	R6, R7	DNI		R0402	2
16	SV1	CONN HEADER VERT 10POS 2.54mm	68021-220HLF	1x10 2.54mm	1
17	SV2	CONN HEADER VERT 10POS 2.54mm	67996-420HLF	1x10 2.54mm	1
18	TP1	PC TEST POINT MINIATURE RED	5000	Hole Diameter(1.02mm)	1
19	TP2, TP3, TP4	PC TEST POINT MINIATURE WHITE	5002	Hole Diameter(1.02mm)	3
20	TP5, TP6	DNI		Hole Diameter(1.02mm)	2
21	VD1, VD2, VD4	DNI	DF2B6.8AFS, L3M	SOD-923	3
22	VD3	TVS DIODE 5V 7V FSC		SOD-923	1

6. Conclusions

Evaluation Board has been designed as a high-power debugging platform for SLG47115V. It is a convenient tool that allows the customer to get acquainted with SLG47115's functionality, especially the H-Bridge functions.

7. Ordering Information

Part Number	Description
SLG47115V-EVB	Evaluation Board for SLG47115V. Developed for testing designs with all features and high current loads.

8. Revision History

Revision	Date	Description
1.01	Aug 14, 2024	Fixed typos Updated section References
1.00	May 5, 2022	Initial release

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