

User Manual

DA7283 Daughterboard 359-09-X

UM-HA-006

Abstract

This board can be used standalone or attached to a motherboard for evaluation.

Contents

Abstract	1
Contents	2
Figures	2
Tables	2
1 Terms and Definitions	3
2 References	3
3 Introduction	3
4 359-09-X PCB Layout and Connections	4
5 Board Setup for Device	6
5.1 Standalone Operation	6
5.2 Motherboard Setup	6
6 359-09-X Schematic	7
7 359-09-X Layout	8
Revision History	14

Figures

Figure 1: 359-09-X PCB	4
Figure 2: Standalone Operation	6
Figure 3: Motherboard Operation	6
Figure 4: 359-09-X Schematic	7
Figure 5: 359-09-X Composite View	8
Figure 6: 359-09-X Top Layer Silkscreen	9
Figure 7: 359-09-X Top Layer Routing	10
Figure 8: 359-09-X Inner Layer 2	11
Figure 9: 359-09-X Inner Layer 3	12
Figure 10: 359-09-X Bottom Layer Routing	13

Tables

Table 1: Jumper Connections and Descriptions	5
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1 Terms and Definitions

NOTE: "X" can denote different version of boards such as A and B variants

359-05-x	DA728x Motherboard, containing LRA as well as the digital and analogue accelerometer circuitry
359-06-x	DA7280 Daughterboard
359-07-x	DA7281 Daughterboard
359-08-x	DA7282 Daughterboard
359-09-x	DA7283 Daughterboard
DA7280	Dialog Semiconductor's haptic driver integrated circuit
DA7281	DA7280 variant with I2C address select
DA7282	DA7280 variant with ultra-low power shutdown
DA7283	DA7280 variant without I2C control and with ultra-low power shutdown
DUT	Device under test
ERM	Eccentric Rotating Mass
GUI	Graphical User Interface
I ² C	Inter-Integrated Circuit Communication Standard
LRA	Linear Resonant Actuator
PCB	Printed Circuit Board
PWM	Pulse Width Modulation
BEMF	Back Electro-Motive Force
GPI	General purpose input
PCB	Printed circuit board
DCDC	Direct current to direct current convertor
IRQ	Interrupt request

2 References

- [1] DA7280, Datasheet, Dialog Semiconductor.
- [2] DA7281, Datasheet, Dialog Semiconductor.
- [3] DA7282, Datasheet, Dialog Semiconductor.
- [4] DA7283, Datasheet, Dialog Semiconductor.
- [5] UM-HA-003, DA7280 Daughterboard User Manual, User Manual, Dialog Semiconductor.
- [6] UM-HA-004, DA7281 Daughterboard User Manual, User Manual, Dialog Semiconductor.
- [7] UM-HA-005, DA7282 Daughterboard User Manual, User Manual, Dialog Semiconductor.
- [8] UM-HA-006, DA7283 Daughterboard User Manual, User Manual, Dialog Semiconductor.
- [9] DA728x GUI software
- [10] UM-HA-001, DA728x Motherboard 359-05-A User Manual, User Manual, Dialog Semiconductor.
- [11] UM-HA-002, DA728x Generating LRA configuration script

3 Introduction

This document describes the use and connections of 359-09-X DA7283 daughterboard to allow evaluation of the DA7283 device. A layout is shown in [Figure 1](#) and details of all jumper connections are listed in [Table 1](#).

4 359-09-X PCB Layout and Connections

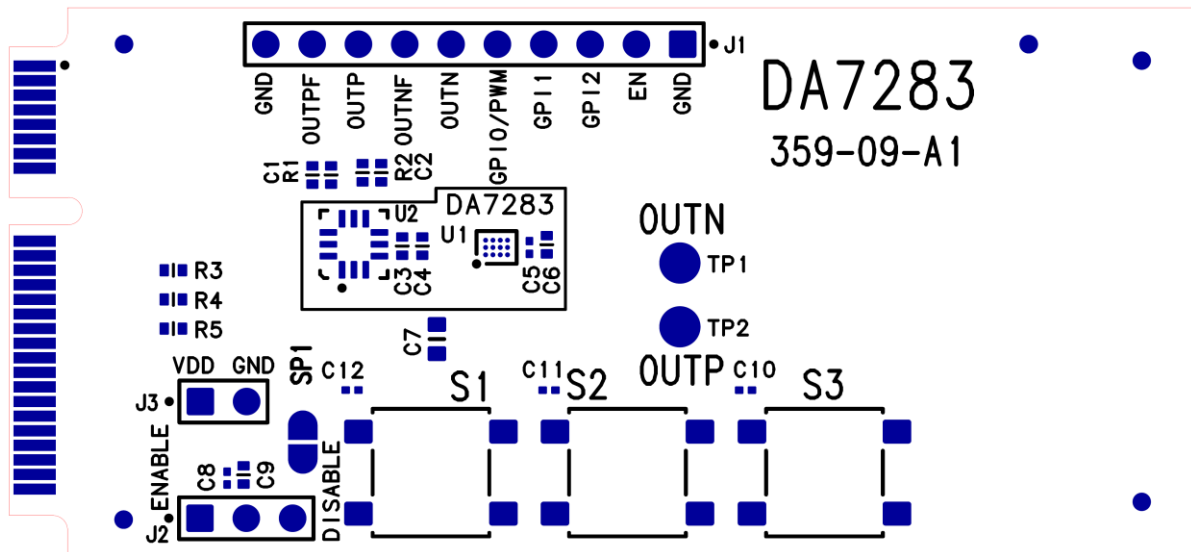


Figure 1: 359-09-X PCB

Table 1: Jumper Connections and Descriptions

Jumper/ Test Point	Pin/Connecti on	Description
J1	GND	Ground connection
	EN	Supply range = 1.35 V to 5.5 V, 1.8 V typical (VDDIO recommended supply) Set to 0 V for ultra-low power standby
	GPI2	GPI sequence trigger 2, low triggered buzz effect, 1 Vrms (medium strength) drive level, second low trigger needed to stop buzz or 60 second timeout
	GPI1	GPI sequence trigger 1, low triggered buzz effect, 1.8 Vrms (maximum strength) drive level, second low trigger needed to stop buzz or 60 second timeout
	GPI0	GPI sequence trigger 0, low triggered click effect, 1.8 Vrms drive level 25 ms drive, 10 ms brake, 20 ms silence
	OUTN	Negative output for LRA connection - TP1 can also be used
	OUTNF	Filtered version of negative output Bandwidth limited to 3.38 kHz for output waveform analysis via an oscilloscope
	OUTP	Positive output for LRA connection - TP2 can also be used
	OUTPF	Filtered version of positive output Bandwidth limited to 3.38 kHz for output waveform analysis via an oscilloscope
	GND	Ground connection
J2	SHORT 1 to 2 (default)	Connects VDDIO to EN line of DA7283
	SHORT 2 to 3	Grounds EN line of DA7283 to enter ultra-low power mode
J3	VDD	VDD supply line to device Supply range = 2.8 V to 5.5 V input
	GND	Ground connection
TP1	TP1	Test point for OUTN, use for LRA connection when using standalone
TP2	TP2	Test point for OUTP, user for LRA connection when using standalone
SP1	Short (default)	Connects ground connection to enable on-board push switches. Remove short if switches need to be disabled, for example when using DA728x motherboard which has on board touch pads.

5 Board Setup for Device

5.1 Standalone Operation

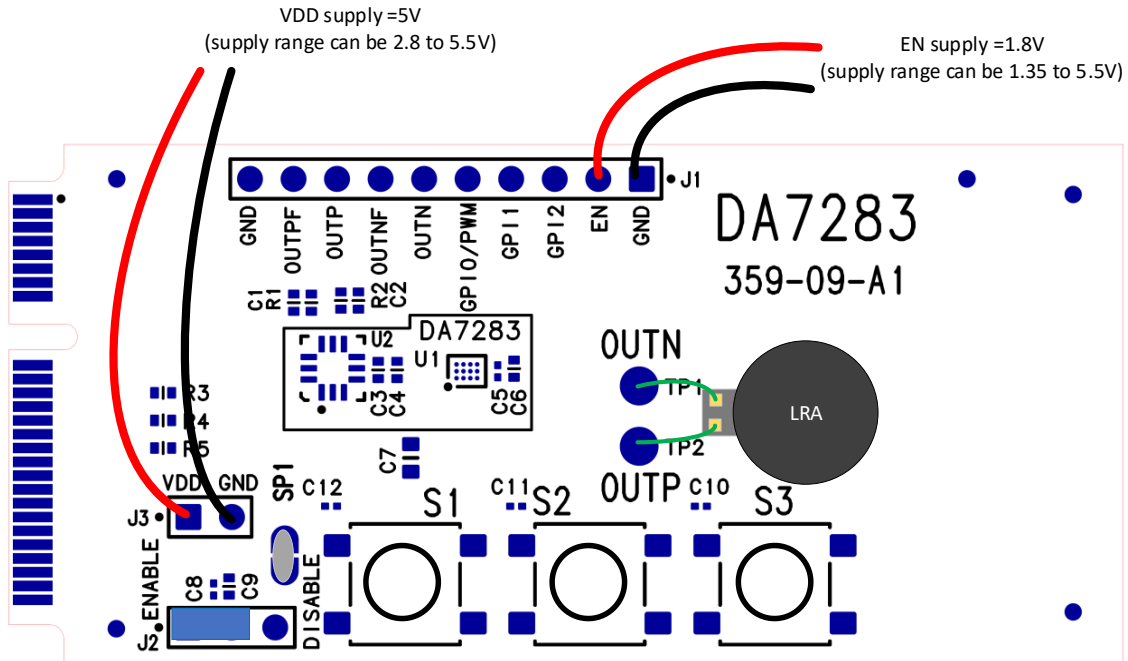


Figure 2: Standalone Operation

5.2 Motherboard Setup

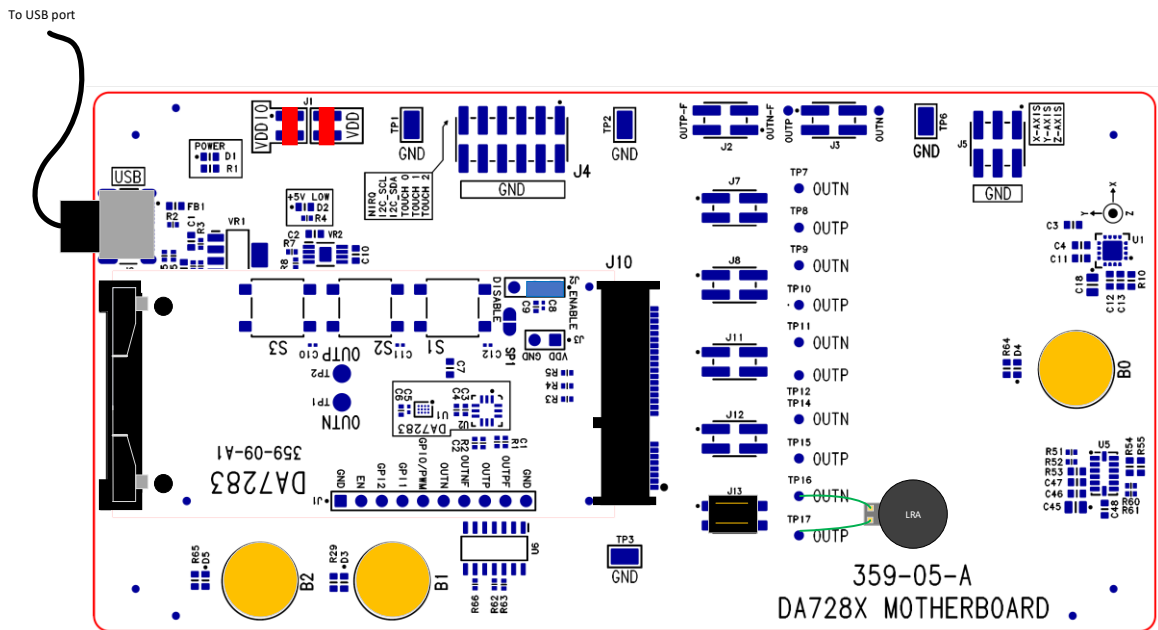


Figure 3: Motherboard Operation

6 359-09-X Schematic

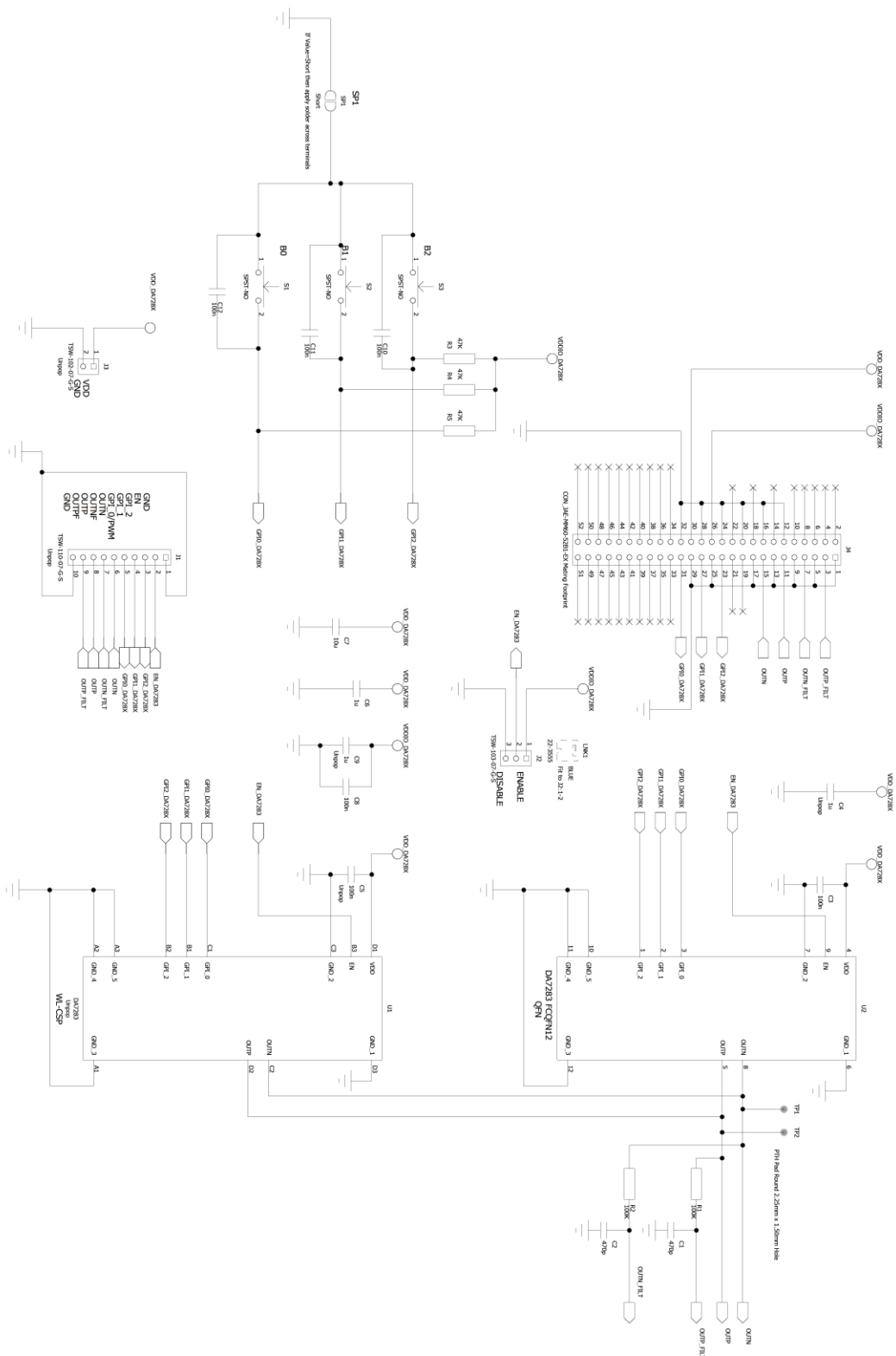


Figure 4: 359-09-X Schematic

7 359-09-X Layout

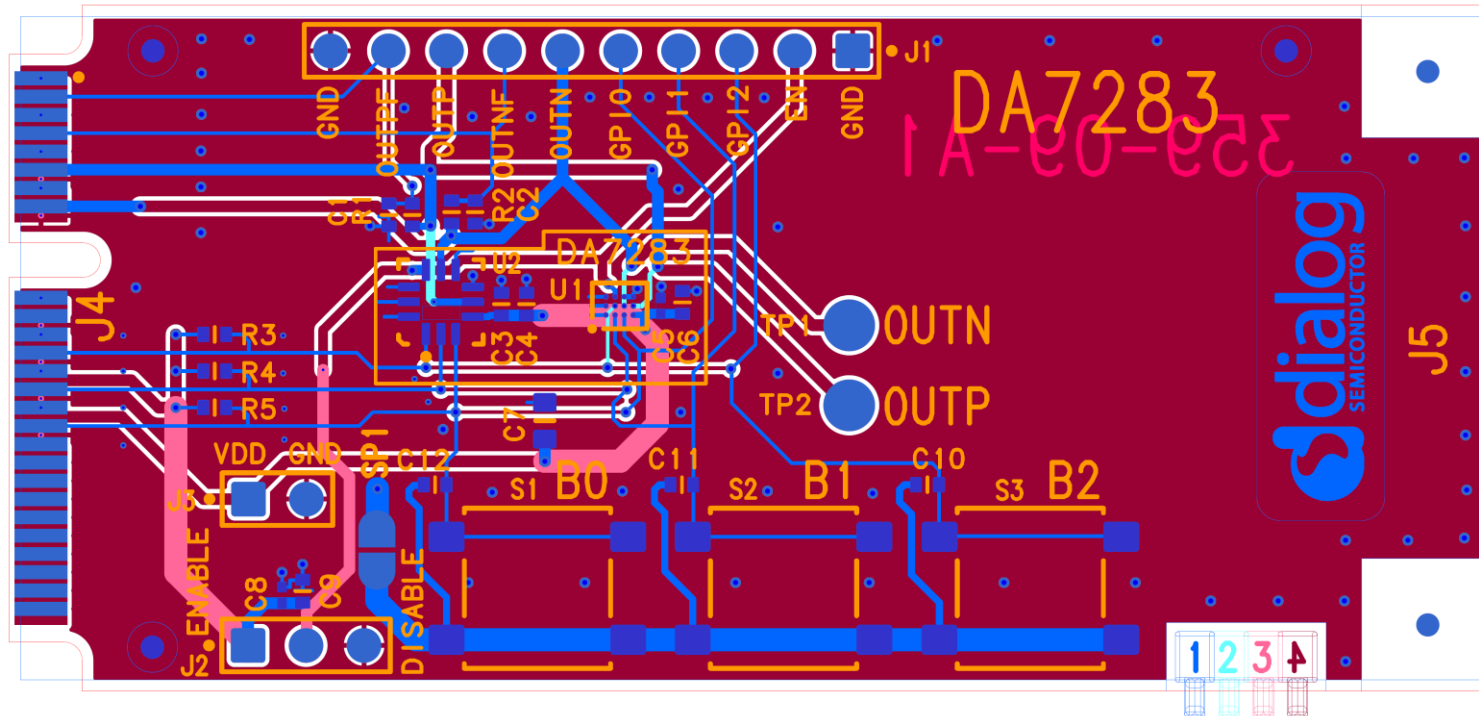


Figure 5: 359-09-X Composite View

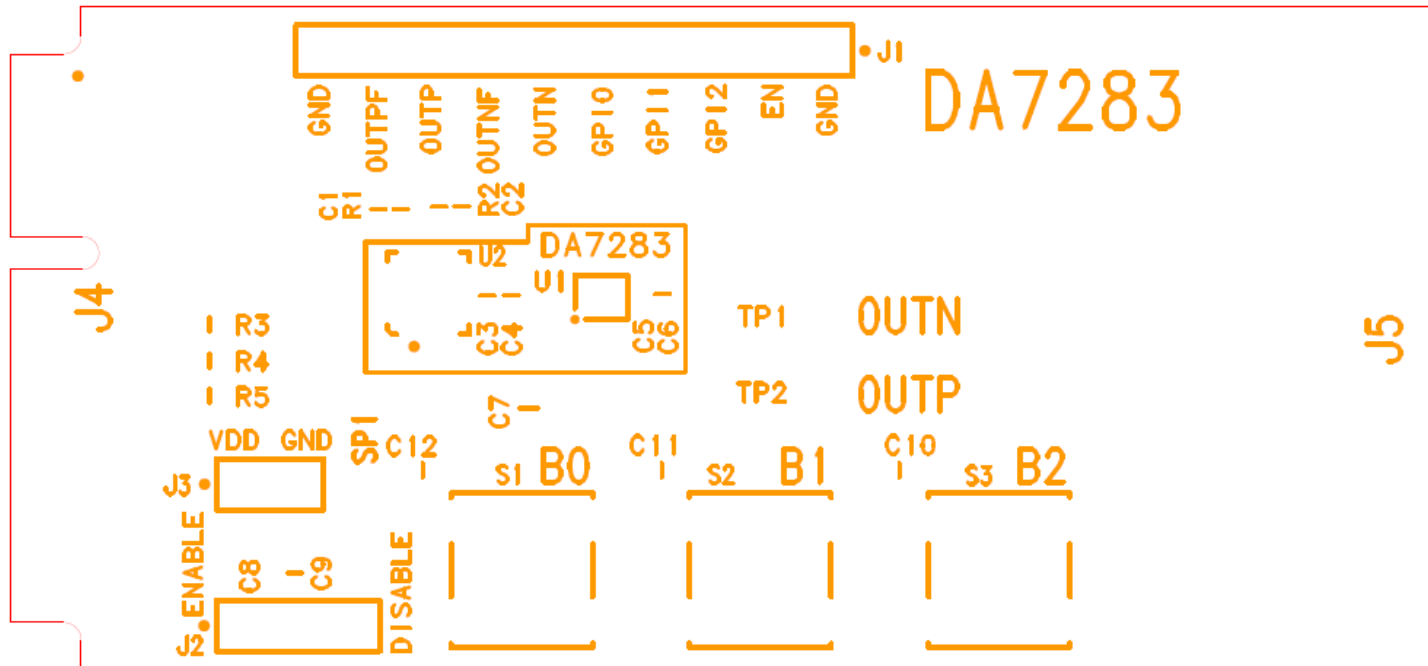


Figure 6: 359-09-X Top Layer Silkscreen

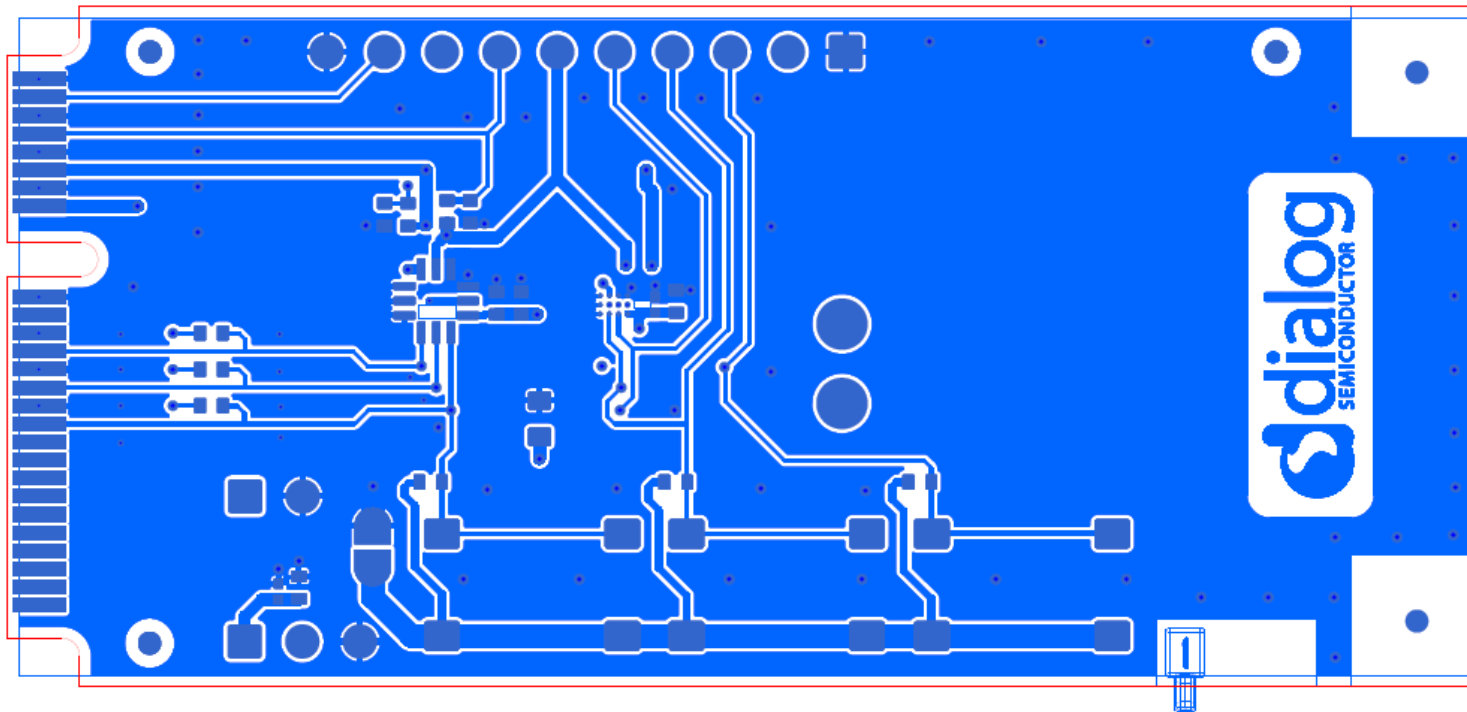


Figure 7: 359-09-X Top Layer Routing

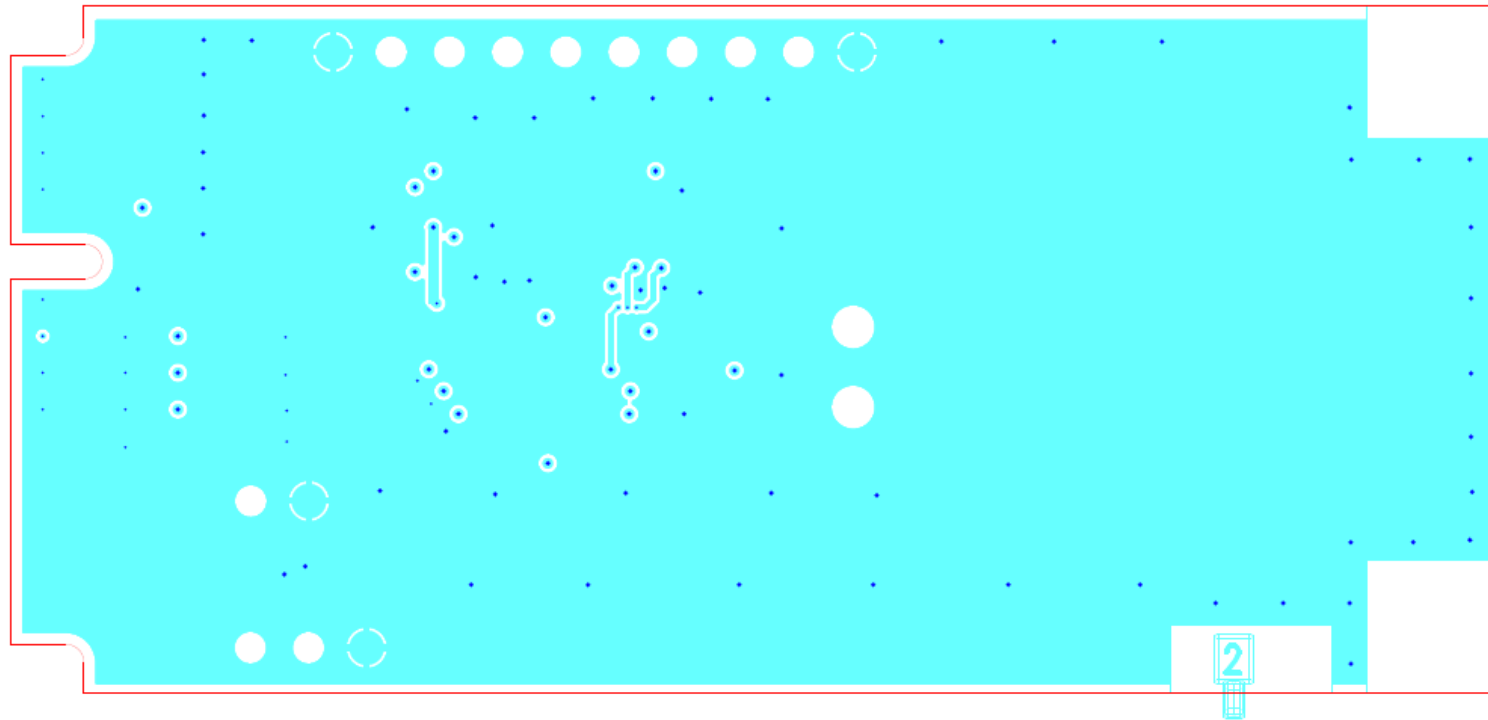


Figure 8: 359-09-X Inner Layer 2

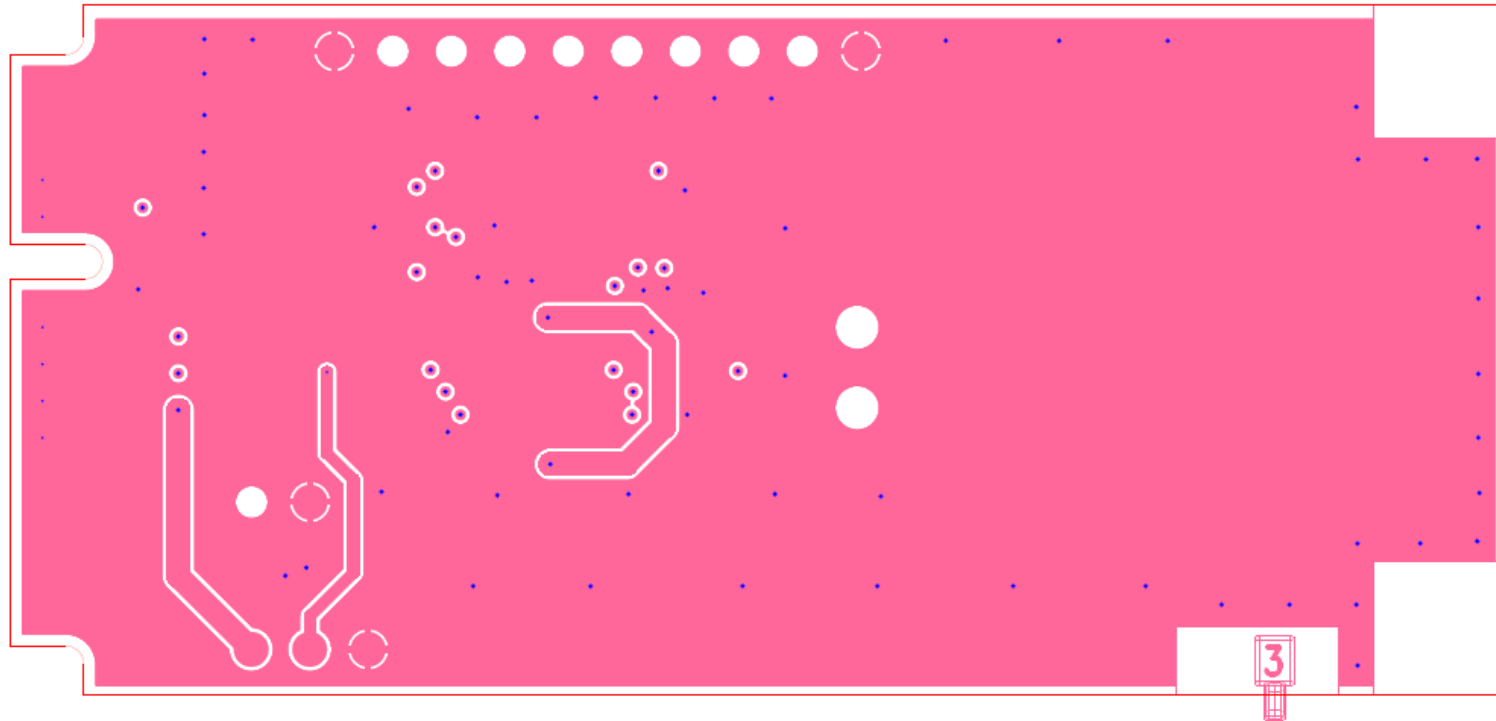


Figure 9: 359-09-X Inner Layer 3

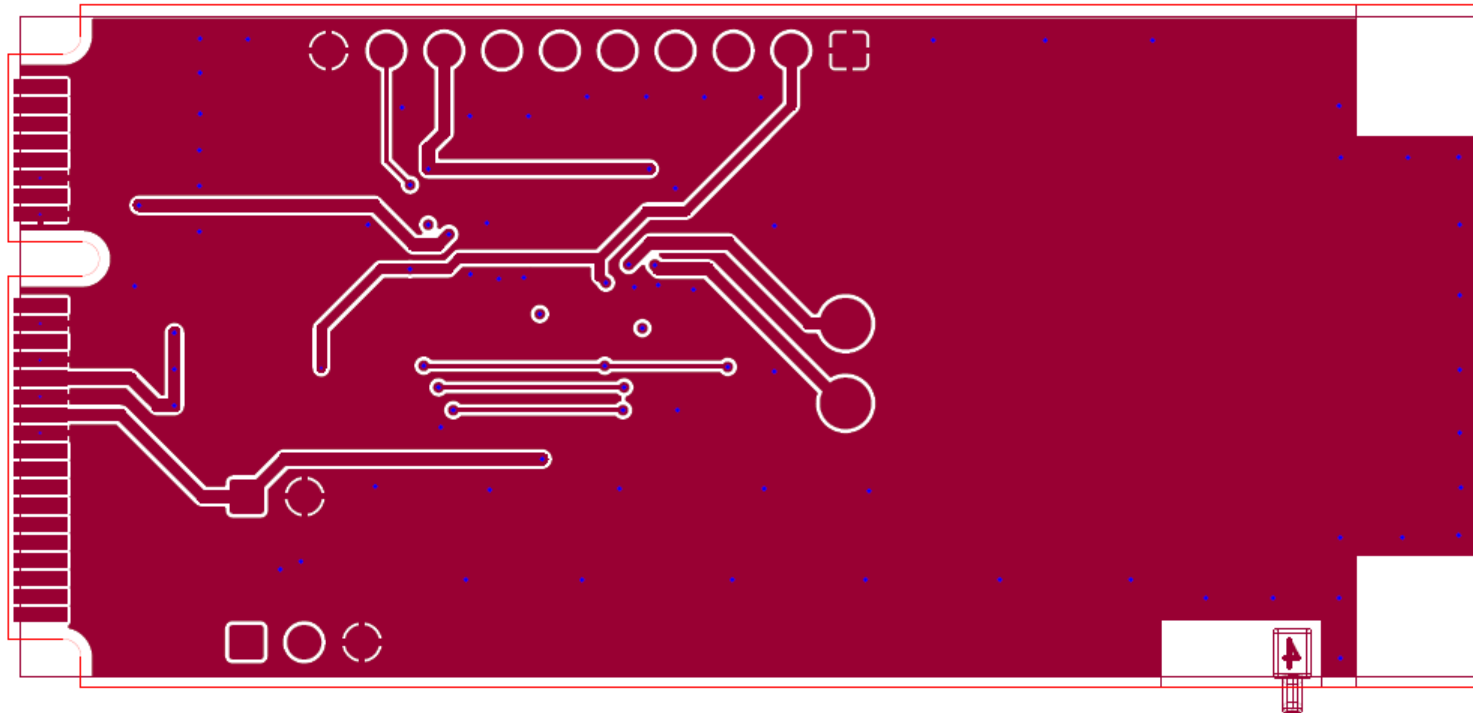


Figure 10: 359-09-X Bottom Layer Routing

Revision History

Revision	Date	Description
1.1	08-Jun-2022	Rebranded to Renesas.
1.0	15-Apr-2020	Initial version

Status Definitions

Status	Definition
DRAFT	The content of this document is under review and subject to formal approval, which may result in modifications or additions.
APPROVED or unmarked	The content of this document has been approved for publication.

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(Rev.1.0 Mar 2020)

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