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April 1st, 2010
Renesas Electronics Corporation

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High-Speed CMOS Logic IC HD74HC Series

Outline

1. Features of High-Speed CMOS Logic

Renesas's HS-CMOS logics–the HD74HC series–and the HCT series based on the EIA/JEDEC specification. Their specification are shown in the Maximum Ratings and the Electrical Characteristics Tables. The HS-CMOS has the characteristics of both standard CMOS logic series and LS-TTL series.

The features of this logic are:

- High-Speed equivalent to the LS-TTL's
- Capable of driving 10LS-TTL loads
  (Capable of driving 15LS-TTL loads in bus drivers)
- Maximum input current of ± 1 µA at 6 V power supply
- Wide supply voltage range: HC series 2 to 6 V
  HCT series 4.5 to 5.5 V
- Wide noise margin
- V_{CC} assurance of Electrical Characteristics at 2.0, 4.5 and 6.0 V
- Low Static Power Consumption 1/2 of EIA/JEDEC

2. Type Name of High-Speed CMOS Logic

The JEDEC has divided the HS-CMOS's into two types: HC and HCT. The HC type has the CMOS logic level for inputs and outputs with buffers. The HCT type has the TTL logic level for inputs and the outputs have buffers.

The industry-standarized maximum ratings and recommended operating range are shown below. Limits for the static characteristics are shown below (right): Table 1 is in the industry-standard and Table 2 is the Renesas specifications.

The Renesas specification is used throughout this document. Additional specifications are shown in the individual data sheets. Switching characteristics are specified under the following conditions:

- Input pulse voltage: + V_{CC}
- Load capacitance: 50 pF
- Input pulse rise/fall time: 6 ns

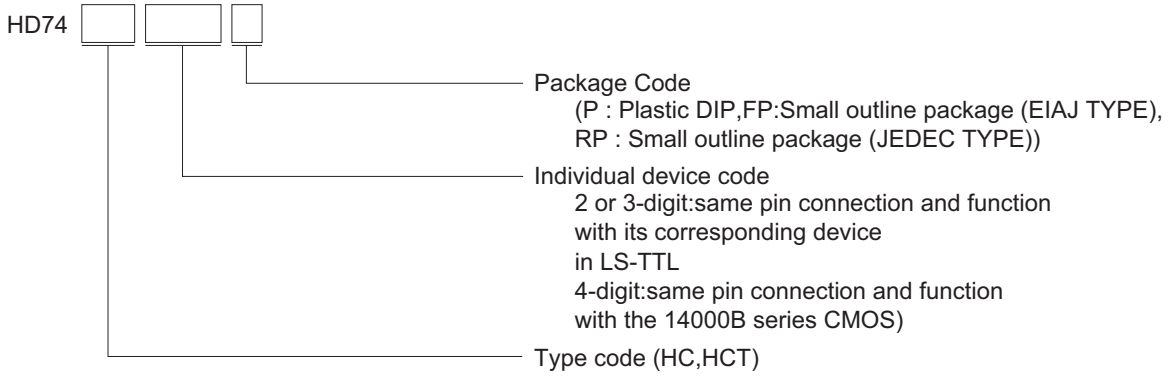
Switching times measured from 50% point of input voltage to 50% point of output voltage

- Three different supply voltages: 2.0, 4.5 and 6.0 V

3. Input Levels of Each Series Type (V_{CC} = 5 V)

Type	Input level		Remarks
	V_{IH}	V_{IL}	
HC series	3.5 V	1.5 V	—
HCT series	2.0 V	0.8 V	TTL logic level for inputs

3.1 Type Name of HS-CMOS Logic



4. Absolute Maximum Ratings (Voltages Referenced to GND)

Item	Symbol	Rating	Unit
Supply voltage	V_{CC}	–0.5 to +7	V
I/O voltage	V_{IN}, V_{OUT}	–0.5 to V_{CC} +0.5	V
I/O diode current	I_{IK}, I_{OK}	±20	mA
Output current	I_O	±25	mA
V_{CC}, GND current	I_{CC}, I_{GND}	±50	mA
Power dissipation	P_T	500	mW
Storage temperature Range	Tstg	–65 to +150	°C

Additional specification values are shown on the individual data sheets.

5. Recommended Operating Range

5.1 HD74HC

Item	Symbol	Rating	Unit	Condition
Supply voltage	V_{CC}	2 to 6	V	
I/O voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

5.2 HD74HCT

Item	Symbol	Rating	Unit	Condition
Supply voltage	V_{CC}	4.5 to 5.5	V	
I/O voltage	V_{IN}, V_{OUT}	0 to V_{CC}	V	
Operating temperature	Ta	–40 to +85	°C	
Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

5.3 HD74HC14, HC132

Item	Symbol	Rating	Unit	Condition
Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V

5.4 HD74HC123A, HC221, HC423A

Item	Symbol	Rating	Unit	Condition
A, B Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V
CLR Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

5.5 HD74HC4538

Item	Symbol	Rating	Unit	Condition
A, B Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V
CD Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

5.6 HD74HC540, HC541

Item	Symbol	Rating	Unit	Condition
A Input rise/fall time	tr, tf	0 to unlimited	ns	V_{CC} = 2.0 V
		0 to unlimited		V_{CC} = 4.5 V
		0 to unlimited		V_{CC} = 6.0 V
G Input rise/fall time	tr, tf	0 to 1000	ns	V_{CC} = 2.0 V
		0 to 500		V_{CC} = 4.5 V
		0 to 400		V_{CC} = 6.0 V

Table 1 EIA/JEDEC Format for High-Speed CMOS Specifications

Parameters			Symbol	V_{CC}(V)	Limits +25°C min	Limits +25°C max	Limits –40 to +85°C min	Limits –40 to +85°C max	Unit	Test Conditions	
Input voltage		HC Series	V_{IH}	2.0	1.5	—	1.5	—	V		
				4.5	3.15	—	3.15	—			
				6.0	4.2	—	4.2	—			
		HCT Series		4.5 to 5.5	2.0	—	2.0	—			
		HC Series	V_{IL}	2.0	—	0.3	—	0.3	V		
				4.5	—	0.9	—	0.9			
				6.0	—	1.2	—	1.2			
		HCT Series		4.5 to 5.5	—	0.8	—	0.8			
Output voltage	HC Series	Standard type	V_{OH}	2.0	1.9	—	1.9	—	V	Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	4.4	—	4.4	—			
				6.0	5.9	—	5.9	—			
				4.5	3.98	—	3.84	—			Iout = –4.0 mA
				6.0	5.48	—	5.34	—			Iout = –5.2 mA
		Bus driver type		2.0	1.9	—	1.9	—		Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	4.4	—	4.4	—			
				6.0	5.9	—	5.9	—			
				4.5	3.98	—	3.84	—			Iout = –6.0 mA
				6.0	5.48	—	5.34	—			Iout = –7.8 mA
	HCT Series	Standard type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	3.98	—	3.84	—			Iout = –4.0 mA
		Bus driver type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL}	Iout = –20 µA
				4.5	3.98	—	3.84	—			Iout = –6.0 mA
	HC Series	Standard type Bus driver type	V_{OL}	2.0	—	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.1	—	0.1			
				6.0	—	0.1	—	0.1			
				4.5	—	0.26	—	0.33			Iout = 4.0 mA
				6.0	—	0.26	—	0.33			Iout = 5.2 mA
				2.0	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.1	—	0.1			
				6.0	—	0.1	—	0.1			
Output voltage	HC Series	Bus driver type		4.5	—	0.26	—	0.33	V	Vin = V_{IH} or V_{IL}	Iout = 6.0 mA
				6.0	—	0.26	—	0.33			Iout = 7.8 mA
	HCT Series	Standard type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.26	—	0.33			Iout = 4.0 mA
		Bus driver type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	Iout = 20 µA
				4.5	—	0.26	—	0.33			Iout = 6.0 mA
Input leakage current		HC Series	I_I	6.0	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
		HCT Series		5.5	—	±0.1	—	±1.0			
Analog switch off-state current		HC Series	$I_{S(off)}$	6.0	—	±0.1	—	±1.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.1	—	±1.0		$\|V_S\|$ = V_{CC} or V_{CC} – V_{EE}	
3-state output off-state current		HC Series	I_{OZ}	6.0	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.5	—	±5.0		Vout = V_{CC} or GND	

Parameters			Symbol	V_{CC}(V)	Limits +25°C min	Limits +25°C max	Limits –40 to +85°C min	Limits –40 to +85°C max	Unit	Test Conditions
Quiescent supply current	HC Series	SSI	I_{CC}	6.0	—	2.0	—	20	µA	Vin = V_{CC} or GND Iout = 0 µA
		FF		6.0	—	4.0	—	40		
		MSI		6.0	—	8.0	—	80		
	HCT Series	SSI		5.5	—	2.0	—	20		
		FF		5.5	—	4.0	—	40		
		MSI		5.5	—	8.0	—	80		

Table 2 Renesas High-Speed CMOS Series Specifications

Parameters			Symbol	V_{CC}(V)	Limits +25°C min	Limits +25°C max	Limits –40 to +85°C min	Limits –40 to +85°C max	Unit	Test Conditions	
Input voltage		HC Series	V_{IH}	2.0	1.5	—	1.5	—	V		
				4.5	3.15	—	3.15	—			
				6.0	4.2	—	4.2	—			
		HCT Series		4.5 to 5.5	2.0	—	2.0	—			
		HC Series	V_{IL}	2.0	—	0.5	—	0.5	V		
				4.5	—	1.35	—	1.35			
				6.0	—	1.8	—	1.8			
		HCT Series		4.5 to 5.5	—	0.8	—	0.8			
Output voltage	HC Series	Standard type	V_{OH}	2.0	1.9	—	1.9	—	V	Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
				4.5	4.4	—	4.4	—			
				6.0	5.9	—	5.9	—			
				4.5	4.18	—	4.13	—			I_{OH} = –4.0 mA
				6.0	5.68	—	5.63	—			I_{OH} = –5.2 mA
		Bus driver type		2.0	1.9	—	1.9	—		Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
				4.5	4.4	—	4.4	—			
				6.0	5.9	—	5.9	—			
				4.5	4.18	—	4.13	—			I_{OH} = –6.0 mA
				6.0	5.68	—	5.63	—			I_{OH} = –7.8 mA
	HCT Series	Standard type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
				4.5	4.18	—	4.13	—			I_{OH} = –4.0 mA
		Bus driver type		4.5	4.4	—	4.4	—		Vin = V_{IH} or V_{IL}	I_{OH} = –20 µA
				4.5	4.18	—	4.13	—			I_{OH} = –6.0 mA
	HC Series	Standard type	V_{OL}	2.0	—	0.1	—	0.1	V	Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
				4.5	—	0.1	—	0.1			
				6.0	—	0.1	—	0.1			
				4.5	—	0.26	—	0.33	V	Vin = V_{IH} or V_{IL}	I_{OL} = 4.0 mA
				6.0	—	0.26	—	0.33			I_{OL} = 5.2 mA
		Bus driver type		2.0	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
				4.5	—	0.1	—	0.1			
				6.0	—	0.1	—	0.1			

Parameters			Symbol	V_{CC}(V)	Limits				Unit	Test Conditions	
					+25°C		−40 to +85°C				
					min	max	min	max			
Output voltage	HC Series	Bus driver type	V_{OL}	4.5	—	0.26	—	0.33	V	Vin = V_{IH} or V_{IL}	I_{OL} = 6.0 mA
				6.0	—	0.26	—	0.33			I_{OL} = 7.8 mA
	HCT Series	Standard type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
				4.5	—	0.26	—	0.33			I_{OL} = 4.0 mA
		Bus driver type		4.5	—	0.1	—	0.1		Vin = V_{IH} or V_{IL}	I_{OL} = 20 µA
				4.5	—	0.26	—	0.33			I_{OL} = 6.0 mA
Input leakage current		HC Series	I_I	6.0	—	±0.1	—	±1.0	µA	Vin = V_{CC} or GND	
		HCT Series		5.5	—	±0.1	—	±1.0			
Analog Switch		HC Series	$I_{S(off)}$	6.0	—	±0.1	—	±1.0	µA	Vin = V_{IH} or V_{IL}	
Off-state Current		HCT Series		5.5	—	±0.1	—	±1.0		$\|V_S\|$ = V_{CC} or V_{CC} – V_{EE}	
3-state output Off-state Current		HC Series	I_{OZ}	6.0	—	±0.5	—	±5.0	µA	Vin = V_{IH} or V_{IL}	
		HCT Series		5.5	—	±0.5	—	±5.0		Vout = V_{CC} or GND	
Quiescent Supply Current	HC Series	SSI	I_{CC}	6.0	—	1.0	—	10	µA	Vin = V_{CC} or GND Iout = 0 µA	
		FF		6.0	—	2.0	—	20			
		MSI		6.0	—	4.0	—	40			
	HCT Series	SSI		5.5	—	1.0	—	10			
		FF		5.5	—	2.0	—	20			
		MSI		5.5	—	4.0	—	40			

6. Symbols and Terms Defined for HD74HC Series

6.1 Explanation of Symbols Used in Electrical Characteristics and Recommended Operating Conditions

6.1.1 DC characteristics

Symbol	Term	Description
V_{IH}	"H" level input voltage	"H" level input voltage to ensure that a logic element operates under some constraint.
V_{IL}	"L" level input voltage	"L" level input voltage to ensure that a logic element operates under some constraint.
V_{OL}	"L" level output voltage	Output voltage in effect when, under the input condition for bringing the output Low, the rated output current is allowed to flow to the output terminal.
V_{OH}	"H" level output voltage	Output voltage in effect when, under the input condition for bringing the output High, the rated output current is allowed to flow to the output terminal.
V_T^+	Forward input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to go up from a voltage level lower than the forward input threshold voltage V_T^-.
V_T^-	Reverse input threshold voltage	Input voltage in effect when the operation of a logic element varies as the input is allowed to go up from a voltage level lower than the reverse input threshold voltage V_T^+.
V_H	Hysteresis voltage	Difference between forward input threshold voltage V_T^+ and reverse threshold voltage V_T^-.
I_{OH}	"H" level output current	Output current that flows out when, under the condition for bringing the output High, the rated output voltage V_{OUT} is applied to the output terminal.
I_{OL}	"L" level output current	Output current that flows out when, under the condition for bringing the output High, the rated output voltage V_{OUT} is applied to the output terminal.
I_{IN}	Input leakage current	Input current that flows in when the rated maximum input voltage is applied to the input terminal.
I_{IH}	"H" level input current	Input current that flows in when the rated "H" level voltage is applied to the input.
I_{IL}	"L" level input current	Input current that flows out when the rated "L" level voltage is applied to the input.
I_{OZ}	Off-state output current (high impedance)	Current that flows to the 3-state output of an element under the input condition for bringing the output to High impedance.
Is(off)	Analog switch off-state current	Current that flows to the analog switch of an element under the input condition for bringing the switch to off-state.
I_{CC}	Quiescent supply current	Current that flows to the supply terminal (V_{CC}) under the rated input condition.

6.1.2 AC characteristics

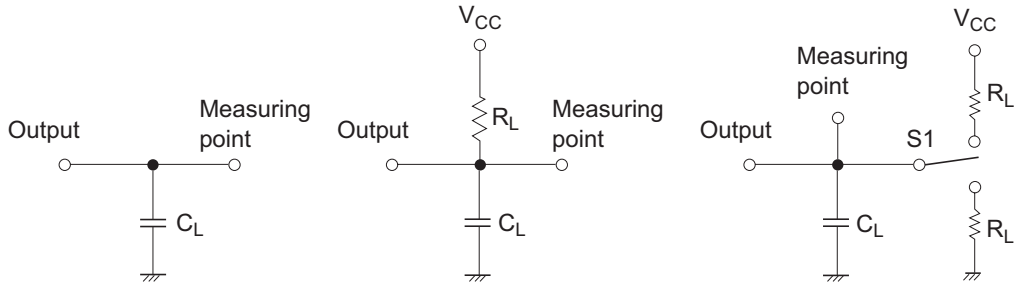
Symbol	Term	Description
f_{max}	Maximum clock frequency	Maximum clock frequency that maintains the stable changes in output logic level in the rated sequence under the I/O condition allowing clock pulses to change the output state.
t_{TLH}	Rise (transient) time	Rated time from “L” level to “H” level of a waveform during the defined transient period changing from “L” level to “H” level.
t_{THL}	Fall (transient) time	Rated time from “H” level to “L” level of a waveform during the defined transient period changing from “H” level to “L” level.
t_{PLH}	Output rise propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from “L” level to “H” level.
t_{PHL}	Output fall propagation delay time	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the output changing from “H” level to “L” level.
t_{HZ}	3-state output disable time (“H” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from “H” level to the high impedance state.
t_{LZ}	3-state output disable time (“L” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from “L” level to the high impedance state
t_{ZH}	3-state output enable time (“H” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high impedance state to “H” level.
t_{ZL}	3-state output enable time (“L” level)	Delay time between the rated voltage levels of an I/O voltage waveform under a defined load condition, with the 3-state output changing from the high impedance state to “L” level.
t_w	Pulse width	Duration of time between the rated levels from a leading edge to a trailing edge of a pulse waveform.
t_h	Hold time	Time in which to hold date at the specified input terminal after a change at another related input terminal (e.g., clock input).
t_{su}	Setup time	Time in which to set up and keep data at the specified input terminal before a change at another related input terminal (e.g., clock input).
t_{rm}	Removal time	Time period between the time when data at the specified input terminal is released and the time when another related input terminal (e.g., clock input) can be changed.
C_{in}	Input capacitance	Capacitance between GND terminal and an input terminal to which 0 V is applied.

6.2 Explanation of Symbols Used in Function Table

Symbol	Description
H	High level (in steady state; noted "H" or “H” level in sentences)
L	Low level (in steady state; noted "L" or “L” level in sentences)
⎍	Transition from L level to H level
⎎	Transition from H level to L level
X	Either H or L
Z	3-state output off (high impedance)
a·····h	Input level of steady state for each of inputs A-H
Q0	Q level immediately before the indicated input condition is established
Q0	Complement of Q
Qn	Q level immediately before the latest active change (⎍ or ⎎) occurs
⎍⎎	Single H level pulse
⎎⎍	Single L level pulse
TOGGLE	Each output is changed to the complement of the preceding state by an active input change (⎍ or ⎎)

6.2.1 Measuring Method of AC Characteristics

Loading Circuit



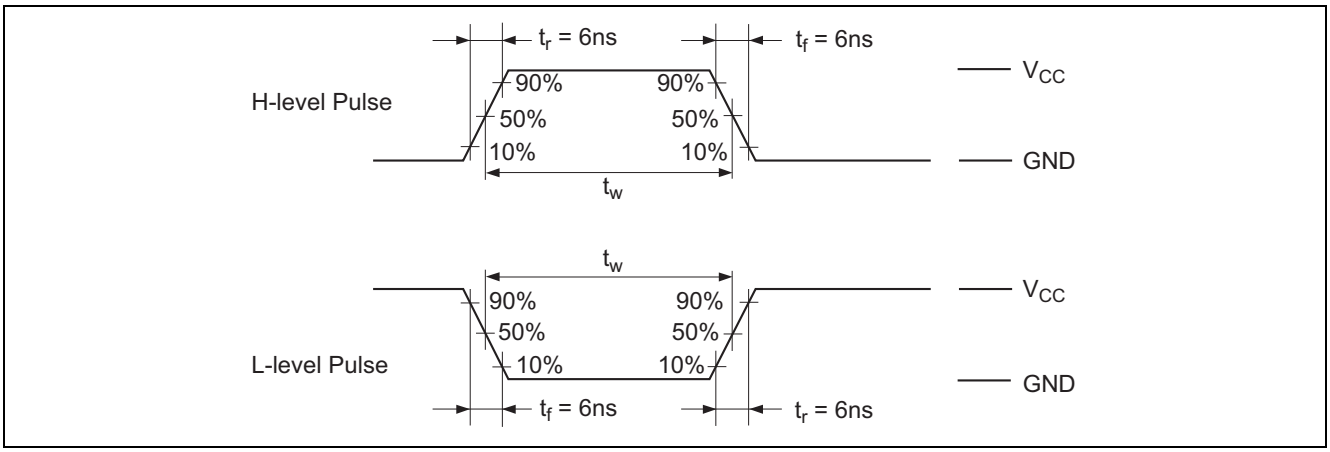
(a) CMOS output (b) Open drain output (c) 3-state output

Notes: 1. C_L includes the floating capacitance of probe and jig.
2. R_L = 1 kΩ (except for a particular specification)

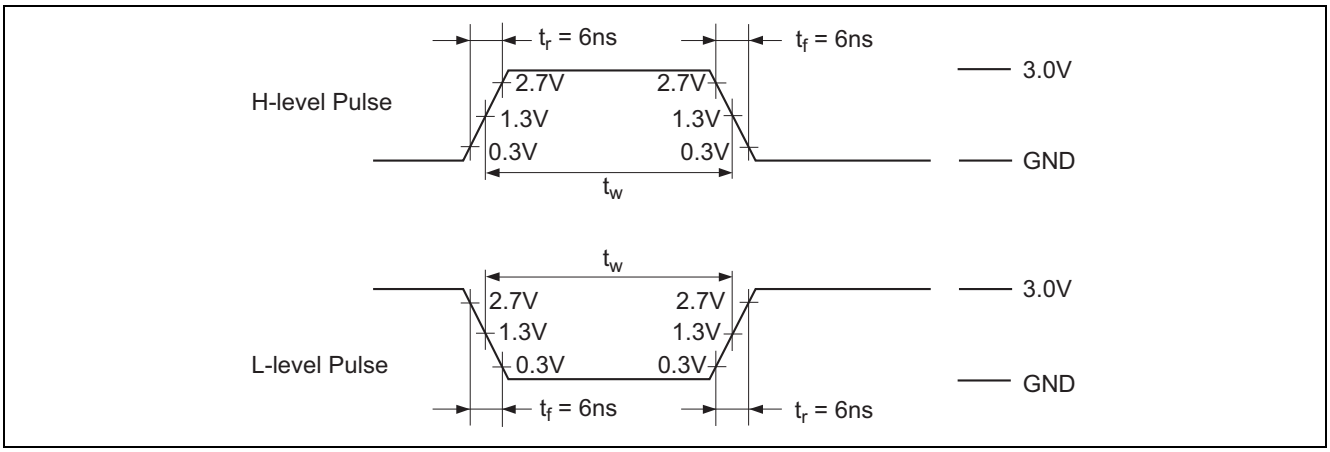
7. Waveforms (Mutual relationship of waveforms)

7.1 Pulse Width (T_W)

7.1.1 74HC Series

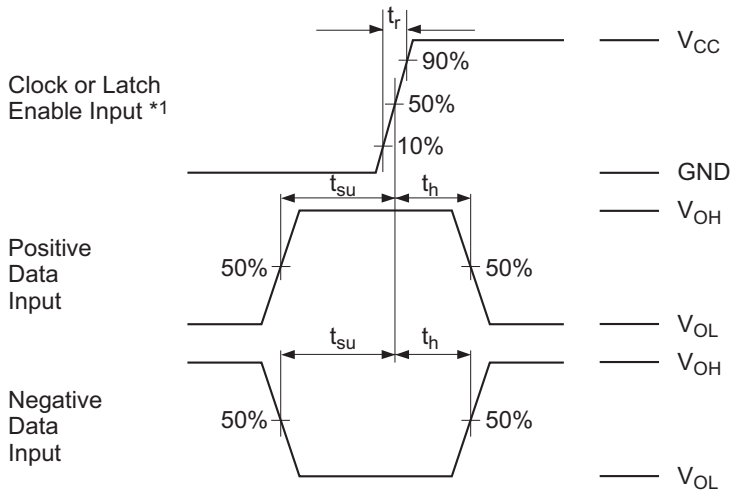


7.1.2 74HCT Series

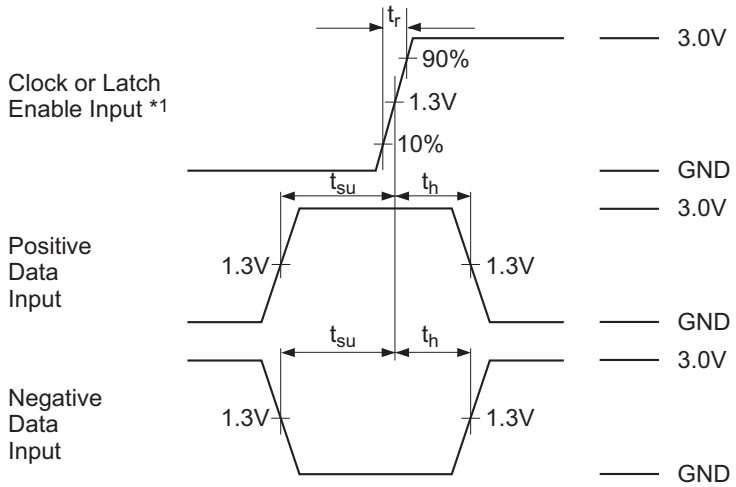


7.2 Setup Time and Hold Time

7.2.1 74HC Series



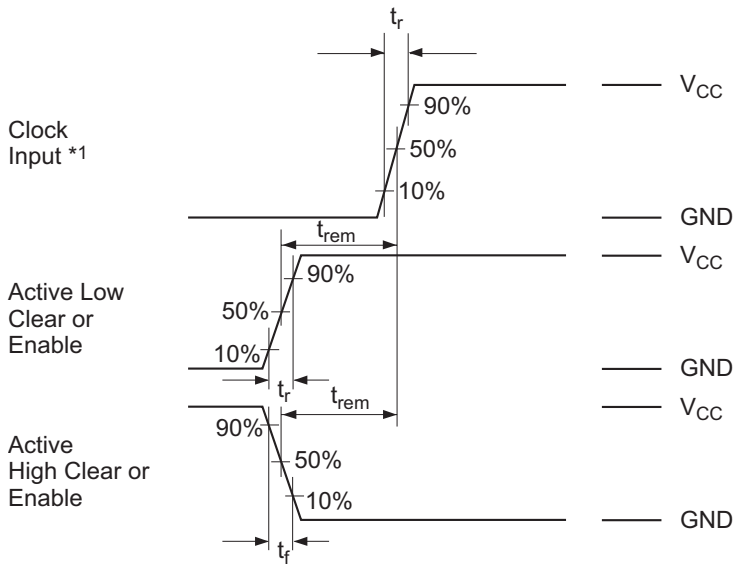
7.2.2 74HCT Series



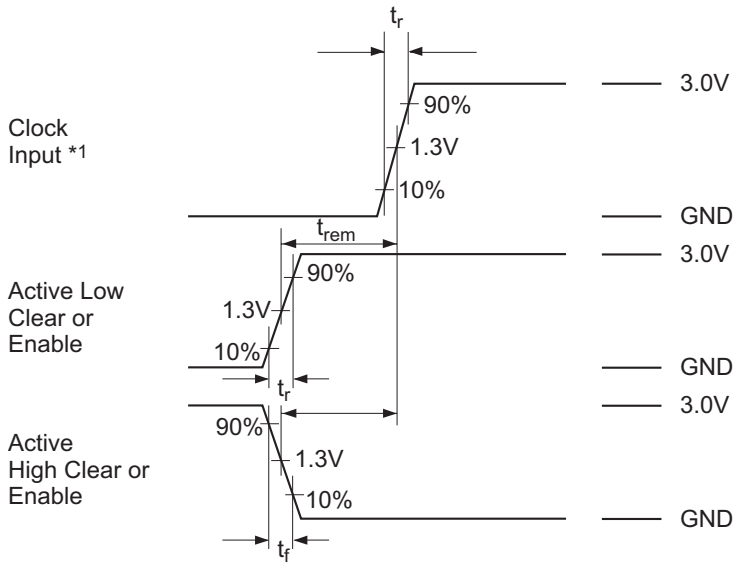
Note: Waveform for negative edge sensitive circuits will be inverted.

7.3 Removal Time

7.3.1 74HC Series



7.3.2 74HCT Series

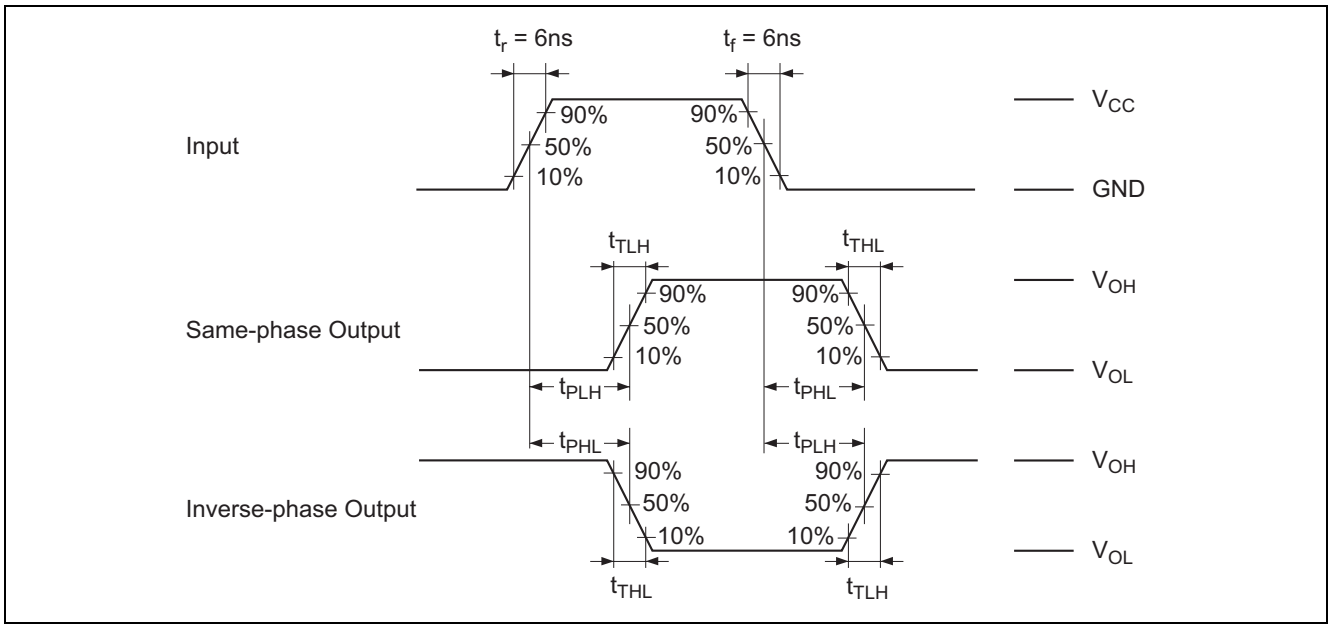


Note: Waveform for negative edge sensitive circuits will be inverted.

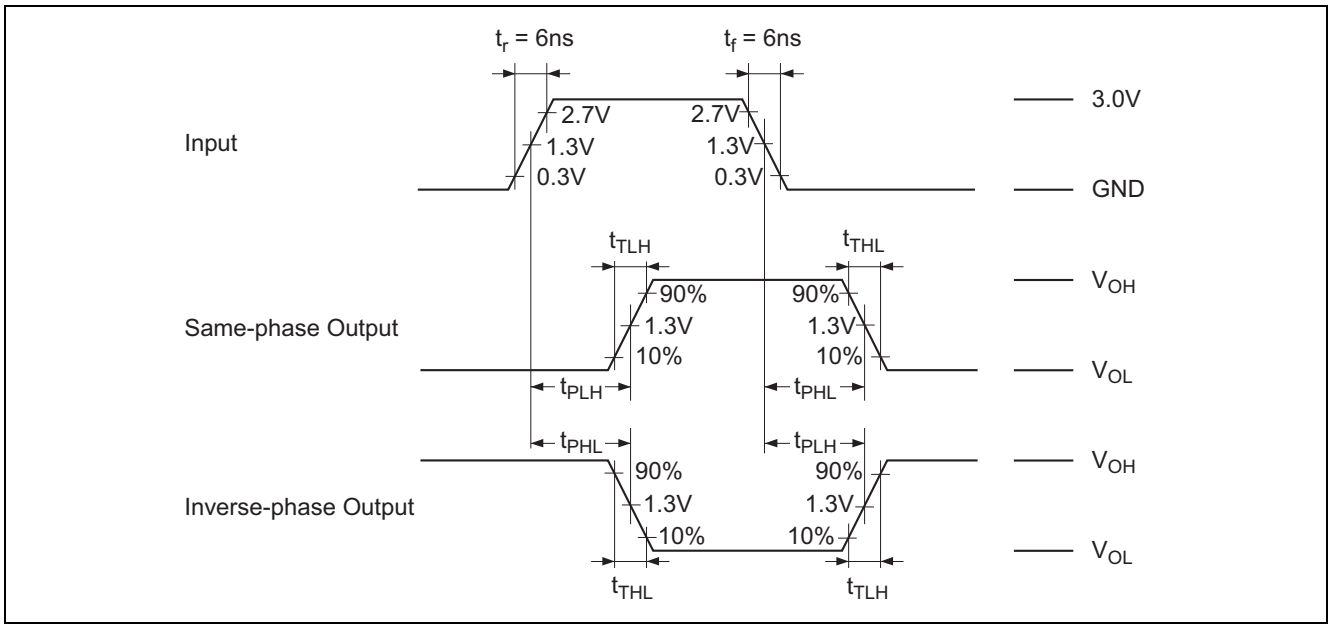
8. Waveforms (Mutual relationship of waveforms)

8.1 Propagation Delay Time, Output Rise Time and Output Fall time

8.1.1 74HC Series



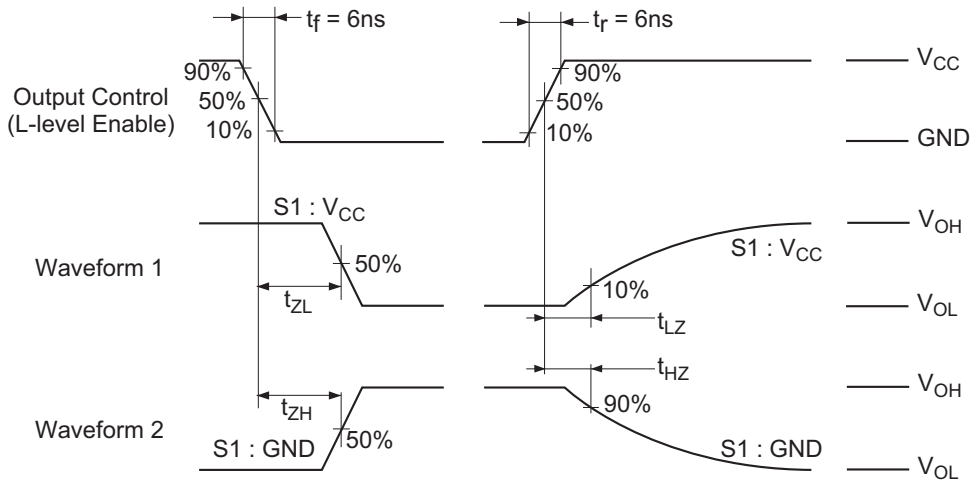
8.1.2 74 HCT Series



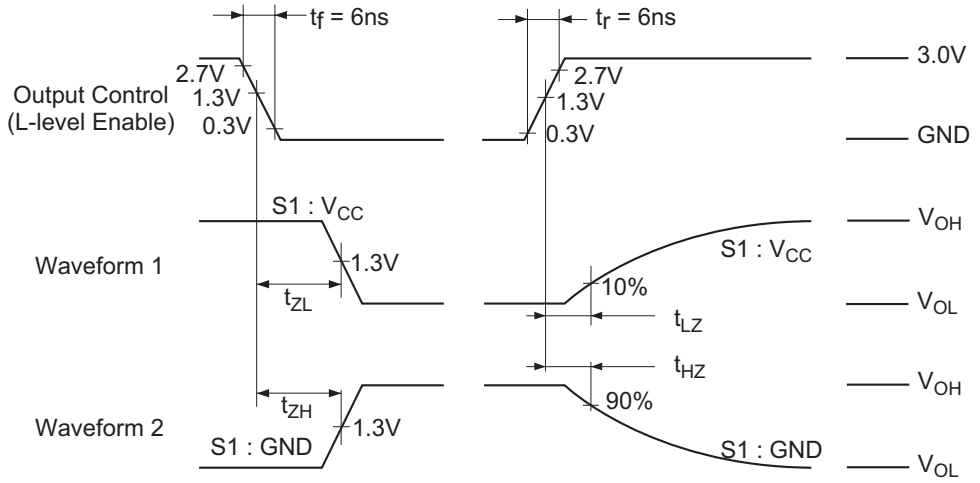
9. Waveforms (Mutual relationship of waveforms)

9.1 Three-state Output, Enable Time and Disable Time

9.1.1 74HC Series



9.1.2 74HCT Series



Notes: 1. Waveform 1 is an output under the internal condition like “L” except for the output disabled by the output control.
2. Waveform 2 is an output under the internal condition like “H” except for the output disabled by the output control.

Revision Record

Rev.	Date	Description	
		Page	Summary
1.00	Jul.09.04	—	First edition issued

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