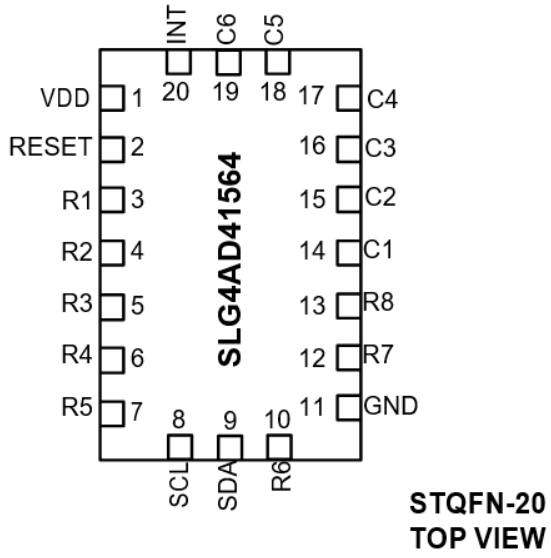
SLG4AD41564
Vertical Marketing - Keypad Scanner

General Description
Silego SLG4AD41564 is a low power and small form device. The SoC is housed in a 2mm x 3mm STQFN package which is optimal for using with small devices.

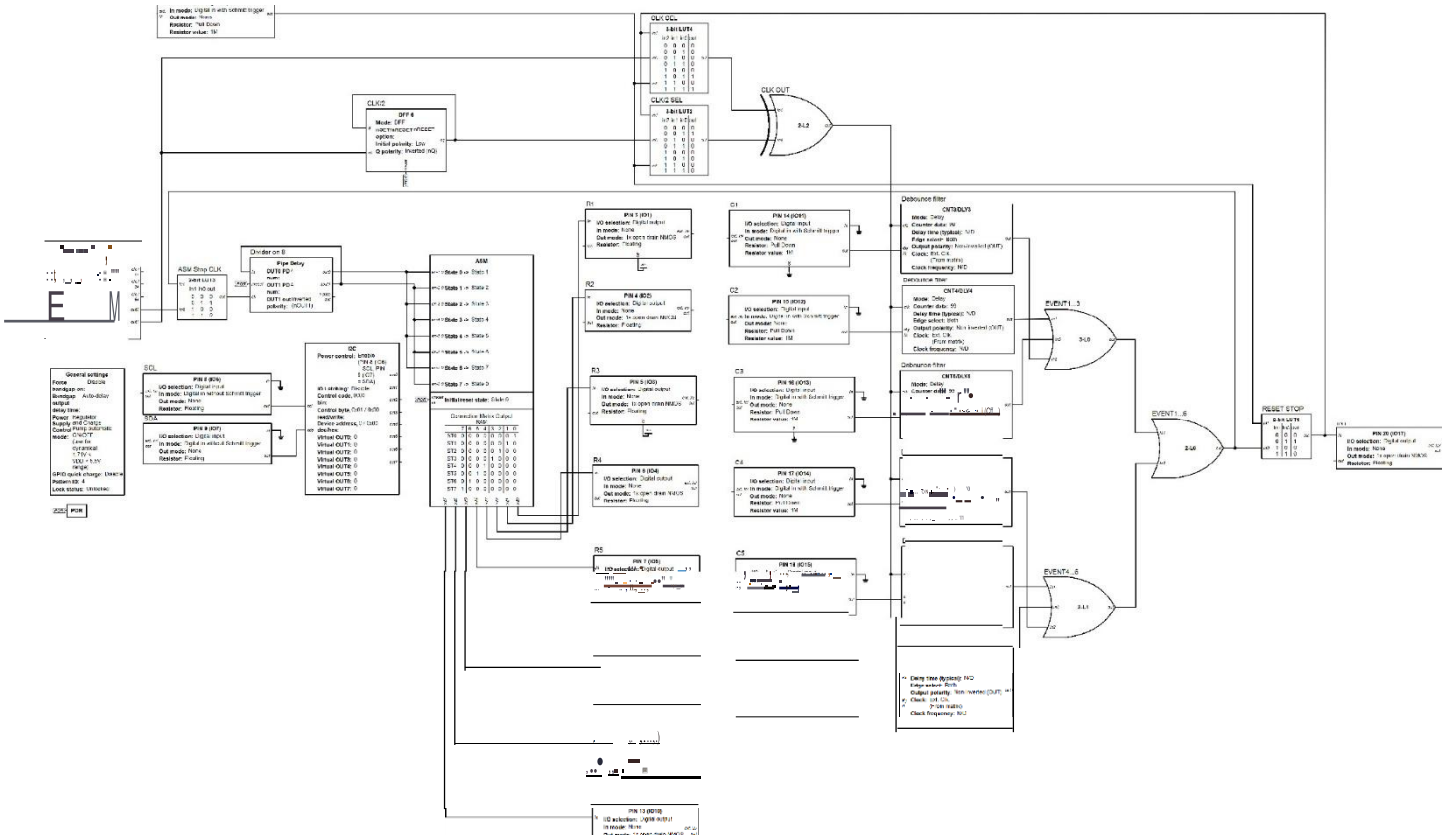
Features
- Low Power Consumption
- Pb-Free / RoHS Compliant
- Halogen-Free
- STQFN-20 Package

Output Summary
- 9 Outputs — Open Drain NMOS 1X

Pin Configuration



Block Diagram



Pin Configuration

Pin #	Pin Name	Type	Pin Description
1	VDD	PWR	Supply Voltage
2	RESET	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
3	R1	Digital Output	Open Drain NMOS 1X
4	R2	Digital Output	Open Drain NMOS 1X
5	R3	Digital Output	Open Drain NMOS 1X
6	R4	Digital Output	Open Drain NMOS 1X
7	R5	Digital Output	Open Drain NMOS 1X
8	SCL	Digital Input	Digital Input without Schmitt trigger
9	SDA	Digital Input	Digital Input without Schmitt trigger
10	R6	Digital Output	Open Drain NMOS 1X
11	GND	GND	Ground
12	R7	Digital Output	Open Drain NMOS 1X
13	R8	Digital Output	Open Drain NMOS 1X
14	C1	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
15	C2	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
16	C3	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
17	C4	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
18	C5	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
19	C6	Digital Input	Digital Input with Schmitt trigger with internal pull down 1M
20	INT	Digital Output	Open Drain NMOS 1X

Ordering Information

Part Number	Package Type
SLG4AD41564V	V=STQFN-20
SLG4AD41564VTR	VTR=STQFN-20 – Tape and Reel (3k units)

Absolute Maximum Conditions

Parameter	Min.	Max.	Unit
V_{HIGH} to GND	-0.3	7	V
Voltage at input pins	-0.3	7	V
Current at input pin	-1.0	1.0	mA
Storage temperature range	-65	125	°C
Junction temperature	--	150	°C
ESD Protection (Human Body Model)	2000	--	V
ESD Protection (Charged Device Model)	1300	--	V
Moisture Sensitivity Level	1		

Electrical Characteristics

(@ 25°C, unless otherwise stated)

Symbol	Parameter	Condition/Note	Min.	Typ.	Max.	Unit
V_{DD}	Supply Voltage		1.8	3.3	5	V
T_A	Operating Temperature		-40	25	85	°C
I_Q	Quiescent Current	Static inputs and outputs Scan mode work	--	8.2	--	µA
I_A	Active Current	Static outputs Scan work stop	--	12.5	--	µA
V_O	Maximal Voltage Applied toany PIN in High-Impedance State		--	--	VDD	V
I_O	Maximal Average or DCCurrent (note 1)	Per Each Chip Side (PIN2-PIN10, PIN12-PIN20)	--	--	90	mA
V_{IH}	HIGH-Level Input Voltage	Logic Input, at VDD=1.8V	1.06	--	VDD	V
		Logic Input with Schmitt Trigger, at VDD=1.8V	1.28	--	VDD	
		Logic Input, at VDD=3.3V	1.81	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=3.3V	2.14	--	VDD	
		Logic Input, at VDD=5.0V	2.68	--	VDD	
		Logic Input with Schmitt Trigger, at VDD=5.0V	3.34	--	VDD	
V_{IL}	LOW-Level Input Voltage	Logic Input, at VDD=1.8V	0	--	0.76	V
		Logic Input with Schmitt Trigger, at VDD=1.8V	0	--	0.49	
		Logic Input, at VDD=3.3V	0	--	1.31	
		Logic Input with Schmitt Trigger, at VDD=3.3V	0	--	0.97	
		Logic Input, at VDD=5.0V	0	--	1.96	
		Logic Input with Schmitt Trigger, at VDD=5.0V	0	--	1.41	
V_{HYS}	Schmitt Trigger Hysteresis Voltage	Logic Input with Schmitt Trigger at VDD=1.8V	0.10	0.41	0.66	V

		Logic Input with Schmitt Trigger at VDD=3.3V	0.29	0.62	0.94	
		Logic Input with Schmitt Trigger at VDD=5.0V	0.44	0.90	1.38	
IIH	HIGH-Level Input Current	Logic Input PINs; VIN = VDD	-1.0	--	1.0	µA
IIL	LOW-Level Input Current	Logic Input PINs; VIN = 0V	-1.0	--	1.0	µA
VOL	LOW-Level Output Voltage	Open Drain, IOL = 100uA, 1X Driver, at VDD=1.8 V	--	0.006	0.009	V
		Open Drain, IOL = 3mA, 1X Driver, at VDD=3.3 V	--	0.08	0.15	
		Open Drain, IOL = 5mA, 1X Driver, at VDD=5.0 V	--	0.12	0.16	
IOL	LOW-Level Output Current	Open Drain, VOL = 0.15V, 1X Driver, at VDD=1.8 V	1.38	2.53		mA
		Open Drain, VOL = 0.4V, 1X Driver, at VDD=3.3 V	7.31	12.37		
		Open Drain, VOL = 0.4V, 1X Driver, at VDD=5.0 V	10.82	17.38		
RPULL_DOW N	Internal Pull Down Resistance	Pull down on PINs 2, 14, 15, 16, 17, 18, 19	862	1097	1371	kΩ
TDLY0	Delay0 Time	At temperature 25°C	--	8.09	--	ms
		At temperature -40°C +85°C (note 1)	--	8.11	--	
TDLY1	Delay1 Time	At temperature 25°C	--	8.09	--	ms
		At temperature -40°C +85°C (note 1)	--	8.11	--	
TDLY3	Delay3 Time	At temperature 25°C	--	8.09	--	ms
		At temperature -40°C +85°C (note 1)	--	8.11	--	
TDLY4	Delay4 Time	At temperature 25°C	--	8.09	--	ms
		At temperature -40°C +85°C (note 1)	--	8.11	--	
TDLY5	Delay5 Time	At temperature 25°C	--	8.09	--	ms
		At temperature -40°C +85°C (note 1)	--	8.11	--	
TDLY6	Delay6 Time	At temperature 25°C	--	8.09	--	ms
		At temperature -40°C +85°C (note 1)	--	8.11	--	
TSU	Start up Time	From VDD rising past PONTHR	0.526	1.4	5.148	ms
PONTHR	Power On Threshold	VDD Level Required to Start Up the Chip	0.950	1.462	1.708	V

POFFTHR	Power Off Threshold	VDD Level Required to Switch Off the Chip	0.935	1.103	1.281	V
FSCL	Clock Frequency, SCL		--	--	400	kHz
tLOW	Clock Pulse Width Low		800	--	--	ns
tHIGH	Clock Pulse Width High		200	--	--	ns
tI	Input Filter Spike Suppression (SCL, SDA)		--	--	168	ns
tAA	Clock Low to Data Out Valid		--	--	900	ns
tBUF	Bus Free Time between Stop and Start		1300	--	--	ns
tHD_STA	Start Hold Time		448	--	--	ns
tSU_STA	Start Set-up Time		5.8	--	--	ns
tHD_DAT	Data Hold Time		0	--	--	ns
tSU_DAT	Data Set-up Time		89	--	--	ns
tR	Inputs Rise Time		--	--	300	ns
tF	Inputs Fall Time		--	--	300	ns
t_{SU_STD}	Stop Set-up Time		9.1	--	--	ns
t_{DH}	Data Out Hold Time		444	--	--	ns
$t_{st\_out\_delay}$	State Machine Output Delay Time		67	--	275	ns
t_{st_out}	State Machine Output Transition Time		--	--	165	ns
t_{st_pulse}	State Machine Input Pulse Acceptance Time		9.2	--	--	ns
t_{st_comp}	State Machine Input Compete Time		--	--	29	ns

1. Guaranteed by Design.

Chip address

HEX	BIN	DEC
0x00	0000000	0

Description

1. I2C Basic Command Structure

Each command to the I2C Serial Communications block begins with a Control Byte. The bits inside this Control Byte are shown in Figure 1. After the Start bit, the first four bits are a control code, which can be set by the user in reg<xx:yy>.

The Block Address is the next three bits (A10, A9, A8), which will define the most significant bits in the addressing of thedata to be read (“1”) or written (“0”) by the command. This Control Byte will be followed by an Acknowledge bit (ACK).

With the exception of the Current Address Read command, all commands will have the Control Byte followed by the Word Address. The Word Address, in conjunction with the three address bits in the Control Byte, will define the specificdata byte to be read or written in the command. Figure 1 shows this basic command structure.

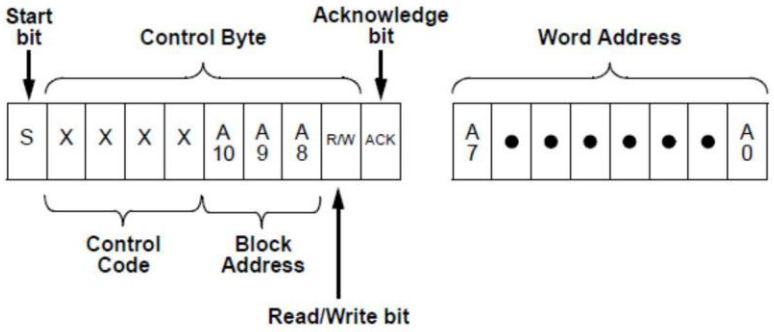


Figure1. I2C Basic Command Structure

2.I2C Serial General Timing

Shown in Figure 2 is the general timing characteristics for the I2C Serial Communications block.

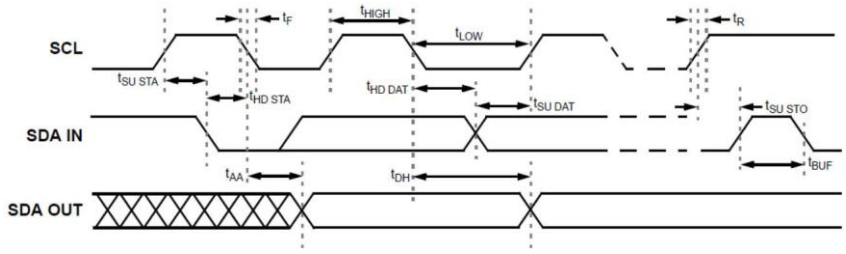


Figure2. I2C Serial General Timing

3.I2C Serial Communications: Read and Write Commands

Following the Start condition from the master, the Control Code [4 bits], the block address [3 bits] and the R/W bit (set to“0”), is placed onto the bus by the Bus Master. After the I2C Serial Communications block has provided an Acknowledgebit (ACK) the next byte transmitted by the master is the Word Address. The Block Address is the next three bits, and is the higher order addressing bits (A10, A9, A8), which when added to the Word Address will together set the internal address pointer in the SLG46537 to the correct data byte to be written. After the SLG46537 sends another Acknowledgebit, the Bus Master will transmit the data byte to be written into the addressed memory location. The SLG46537 again provides an Acknowledge bit and then the Bus Master generates a Stop condition. The internal write cycle for the data will take place at the time that the SLG46537 generates the Acknowledge bit.

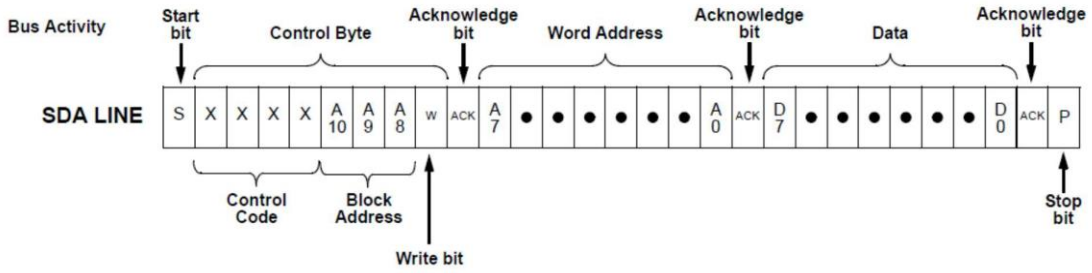


Figure3. I2C Write Command

The Random Read command starts with a Control Byte (with R/W bit set to “0”, indicating a write command) and Word Address to set the internal byte address, followed by a Start bit, and then the Control Byte for the read (exactly the sameas the Byte Write command). The Start bit in the middle of the command will halt the decoding of a Write command, but will set the internal address counter in preparation for the second half of the command. After the Start bit, the Bus Master issues a second control byte with the R/W bit set to “1”, after which the SLG46537 issues an Acknowledge bit, followed by the requested eight data bits.

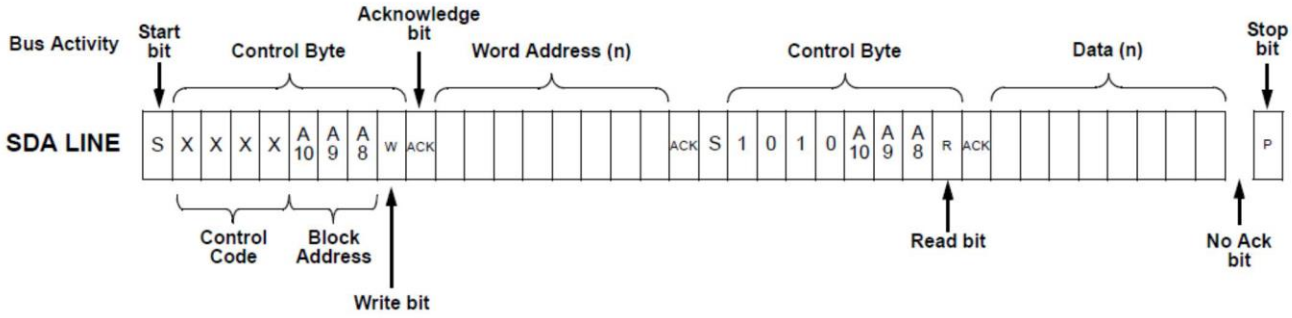


Figure4. I2C Random Read Command

4.Data row keypad scanner

Address Byte	Register Bit	Block	Function
0xF5	reg<1960>	RAM_0 Output for ASM-state	R1 value
	reg<1961>	RAM_1 Output for ASM-state	R2 value
	reg<1962>	RAM_2 Output for ASM-state	R3 value
	reg<1963>	RAM_3 Output for ASM-state	R4 value
	reg<1964>	RAM_4 Output for ASM-state	R5 value
	reg<1965>	RAM_5 Output for ASM-state	R6 value
	reg<1966>	RAM_6 Output for ASM-state	R7 value
	reg<1967>	RAM_7 Output for ASM-state	R8 value

5.Data column keypad scanner

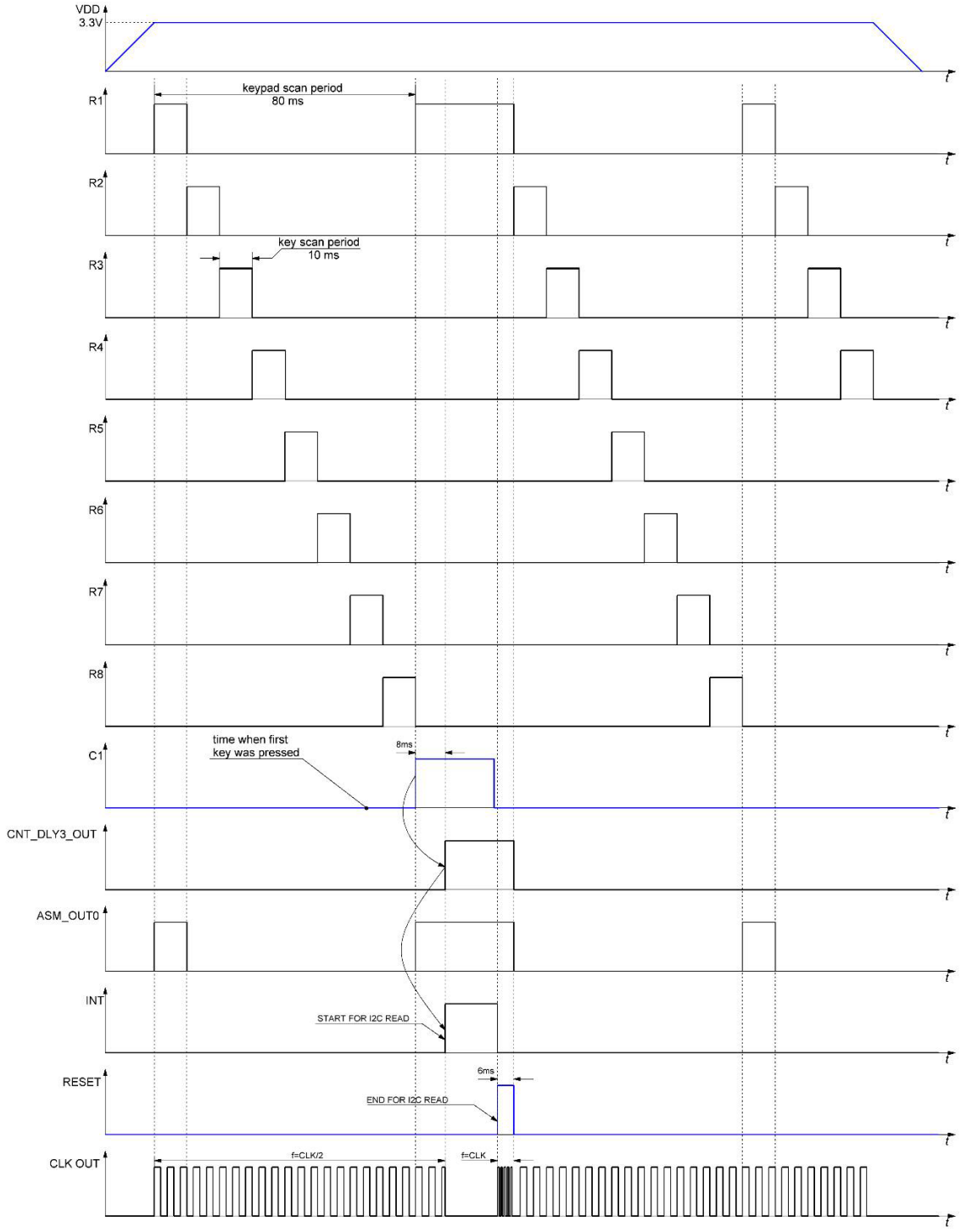
Address Byte	Register Bit	Block	Function
0xF2	reg<1936>	--	Not used
	reg<1937>	--	Not used
	reg<1938>	CNT_DLY3 Output	C1 value
	reg<1939>	CNT_DLY4 Output	C2 value
	reg<1940>	CNT_DLY5 Output	C3 value
	reg<1941>	CNT_DLY6 Output	C4 value
	reg<1942>	CNT_DLY0 Output	C5 value
	reg<1943>	CNT_DLY1 Output	C6 value

Truth Tables

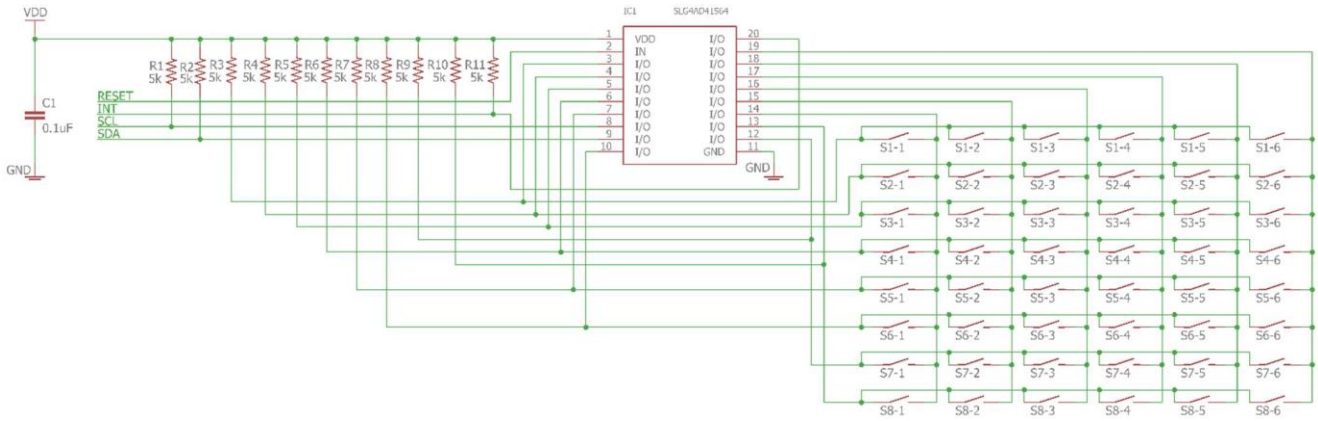
Table1

Keypad Code Number														
	R1	R2	R3	R4	R5	R6	R7	R8	C1	C2	C3	C4	R5	R6
Key1	**H**	L	L	L	L	L	L	L	**H**	L	L	L	L	L
Key2	**H**	L	L	L	L	L	L	L	L	**H**	L	L	L	L
Key3	**H**	L	L	L	L	L	L	L	L	L	**H**	L	L	L
Key4	**H**	L	L	L	L	L	L	L	L	L	L	**H**	L	L
Key5	**H**	L	L	L	L	L	L	L	L	L	L	L	**H**	L
Key6	**H**	L	L	L	L	L	L	L	L	L	L	L	L	**H**
Key7	L	**H**	L	L	L	L	L	L	**H**	L	L	L	L	L
Key8	L	**H**	L	L	L	L	L	L	L	**H**	L	L	L	L
Key9	L	**H**	L	L	L	L	L	L	L	L	**H**	L	L	L
Key10	L	**H**	L	L	L	L	L	L	L	L	L	**H**	L	L
Key11	L	**H**	L	L	L	L	L	L	L	L	L	L	**H**	L
Key12	L	**H**	L	L	L	L	L	L	L	L	L	L	L	**H**
Key13	L	L	**H**	L	L	L	L	L	**H**	L	L	L	L	L
Key14	L	L	**H**	L	L	L	L	L	L	**H**	L	L	L	L
Key15	L	L	**H**	L	L	L	L	L	L	L	**H**	L	L	L
Key16	L	L	**H**	L	L	L	L	L	L	L	L	**H**	L	L
Key17	L	L	**H**	L	L	L	L	L	L	L	L	L	**H**	L
Key18	L	L	**H**	L	L	L	L	L	L	L	L	L	L	**H**
Key19	L	L	L	**H**	L	L	L	L	**H**	L	L	L	L	L
Key20	L	L	L	**H**	L	L	L	L	L	**H**	L	L	L	L
Key21	L	L	L	**H**	L	L	L	L	L	L	**H**	L	L	L
Key22	L	L	L	**H**	L	L	L	L	L	L	L	**H**	L	L
Key23	L	L	L	**H**	L	L	L	L	L	L	L	L	**H**	L
Key24	L	L	L	**H**	L	L	L	L	L	L	L	L	L	**H**
Key25	L	L	L	L	**H**	L	L	L	**H**	L	L	L	L	L
Key26	L	L	L	L	**H**	L	L	L	L	**H**	L	L	L	L
Key27	L	L	L	L	**H**	L	L	L	L	L	**H**	L	L	L
Key28	L	L	L	L	**H**	L	L	L	L	L	L	**H**	L	L
Key29	L	L	L	L	**H**	L	L	L	L	L	L	L	**H**	L
Key30	L	L	L	L	**H**	L	L	L	L	L	L	L	L	**H**
Key31	L	L	L	L	L	**H**	L	L	**H**	L	L	L	L	L
Key32	L	L	L	L	L	**H**	L	L	L	**H**	L	L	L	L
Key33	L	L	L	L	L	**H**	L	L	L	L	**H**	L	L	L
Key34	L	L	L	L	L	**H**	L	L	L	L	L	**H**	L	L
Key35	L	L	L	L	L	**H**	L	L	L	L	L	L	**H**	L
Key36	L	L	L	L	L	**H**	L	L	L	L	L	L	L	**H**
Key37	L	L	L	L	L	L	**H**	L	**H**	L	L	L	L	L
Key38	L	L	L	L	L	L	**H**	L	L	**H**	L	L	L	L
Key39	L	L	L	L	L	L	**H**	L	L	L	**H**	L	L	L
Key40	L	L	L	L	L	L	**H**	L	L	L	L	**H**	L	L
Key41	L	L	L	L	L	L	**H**	L	L	L	L	L	**H**	L
Key42	L	L	L	L	L	L	**H**	L	L	L	L	L	L	**H**
Key43	L	L	L	L	L	L	L	**H**	**H**	L	L	L	L	L
Key44	L	L	L	L	L	L	L	**H**	L	**H**	L	L	L	L
Key45	L	L	L	L	L	L	L	**H**	L	L	**H**	L	L	L
Key46	L	L	L	L	L	L	L	**H**	L	L	L	**H**	L	L
Key47	L	L	L	L	L	L	L	**H**	L	L	L	L	**H**	L
Key48	L	L	L	L	L	L	L	**H**	L	L	L	L	L	**H**

Timing Diagram



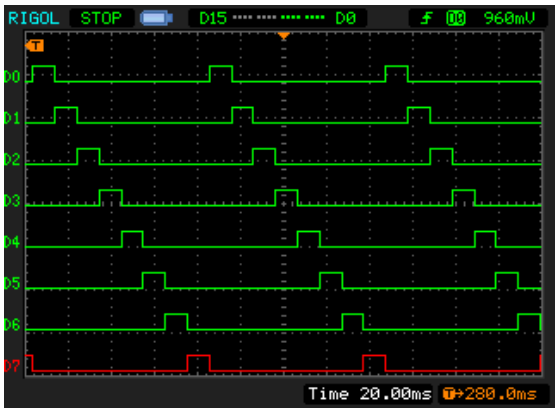
Typical Application Circuit



Functionality Waveforms

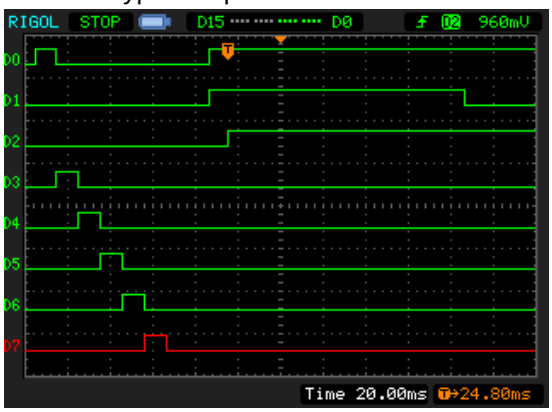
D0 – PIN#3 (R1) with external 5kΩ pull up resistor
D1 – PIN#4 (R2) with external 5kΩ pull up resistor
D2 – PIN#5 (R3) with external 5kΩ pull up resistor
D3 – PIN#6 (R4) with external 5kΩ pull up resistor
D4 – PIN#7 (R5) with external 5kΩ pull up resistor
D5 – PIN#10 (R6) with external 5kΩ pull up resistor
D6 – PIN#12 (R7) with external 5kΩ pull up resistor
D7 – PIN#13 (R8) with external 5kΩ pull up resistor

1. Keypad scan mode

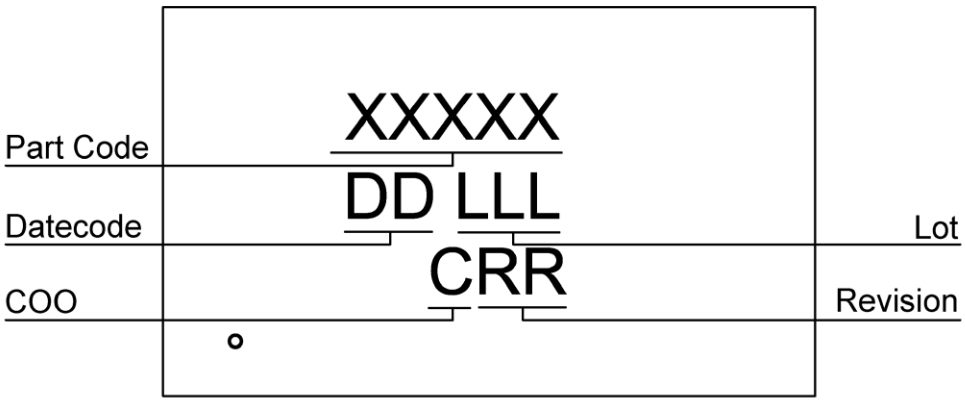


D0 – PIN#3 (R1) with external 5kΩ pull up resistor
D1 – PIN#14 (C1)
D2 – PIN#20 (INT) with external 5kΩ pull up resistor
D3 – PIN#4 (R2) with external 5kΩ pull up resistor
D4 – PIN#5 (R3) with external 5kΩ pull up resistor
D5 – PIN#6 (R4) with external 5kΩ pull up resistor
D6 – PIN#7 (R5) with external 5kΩ pull up resistor
D7 – PIN#10 (R6) with external 5kΩ pull up resistor

2. Keypad stop mode



Package Top Marking



XXXXX – Part ID Field: identifies the specific device configuration
DD – Date Code Field: Coded date of manufacture
LLL – Lot Code: Designates Lot #
C – Assembly Site/COO: Specifies Assembly Site/Country of Origin
RR – Revision Code: Device Revision

Datasheet Revision	Programming Code Number	Locked Status	Part Code	Revision	Date
0.14	004	U	41564	AA	02/22/2017

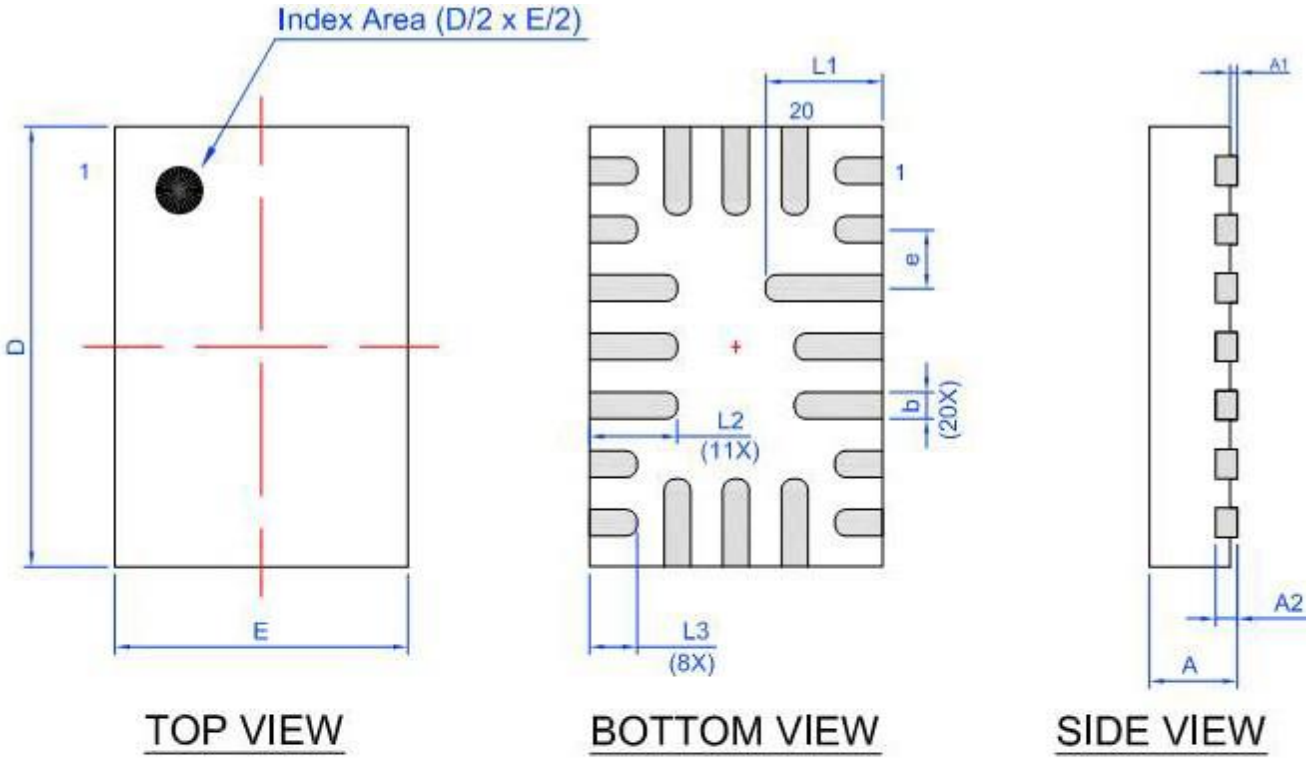
Lock coverage for this part is indicated by √, from one of the following options:

√	**Unlocked**
	Locked for read, bits <1535:0>
	Locked for write, bits <1535:0>
	Locked for read and write, bits <1535:0>

The IC security bit is locked/set for code security for production unless otherwise specified. Revision number is not changed for bit locking.

Package Drawing and Dimensions

20 Lead STQFN Package
JEDEC MO-220, Variation WECE



Unit: mm

Symbol	Min	Nom.	Max	Symbol	Min	Nom.	Max
A	0.50	0.55	0.60	D	2.95	3.00	3.05
A1	0.005	-	0.050	E	1.95	2.00	2.05
A2	0.10	0.15	0.20	L1	0.75	0.80	0.85
b	0.13	0.18	0.23	L2	0.55	0.60	0.65
e	0.40 BSC			L3	0.275	0.325	0.375

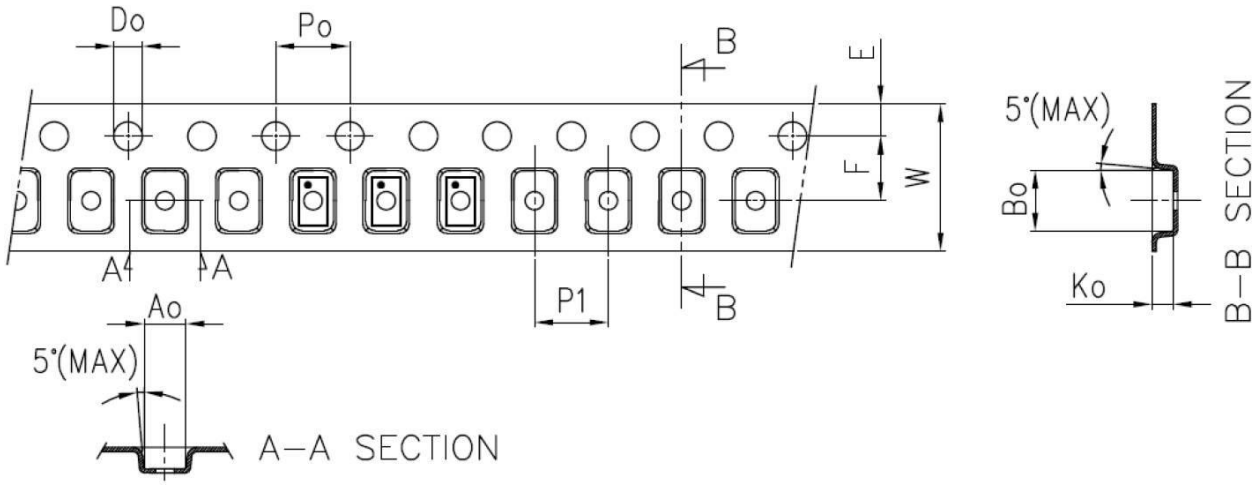
Tape and Reel Specification

Package Type	# of Pins	Nominal Package Size (mm)	Max Units		Reel & Hub Size (mm)	Trailer A		Leader B		Pocket (mm)	
			per reel	per box		Pockets	Length (mm)	Pockets	Length (mm)	Width	Pitch
STQFN 20L 2x3mm 0.4P Green	20	2x3x0.55	3000	3000	178/60	100	400	100	400	8	4

Carrier Tape Drawing and Dimensions

Package Type	Pocket BTM Length (mm)	Pocket BTM Width (mm)	Pocket Depth (mm)	Index Hole Pitch (mm)	Pocket Pitch (mm)	Index Hole Diameter (mm)	Index Hole to Tape Edge (mm)	Index Hole to Pocket Center (mm)	Tape Width (mm)
	A0	B0	K0	P0	P1	D0	E	F	W
STQFN 20L 2x3mm 0.4P Green	2.2	3.15	0.76	4	4	1.5	1.75	3.5	8

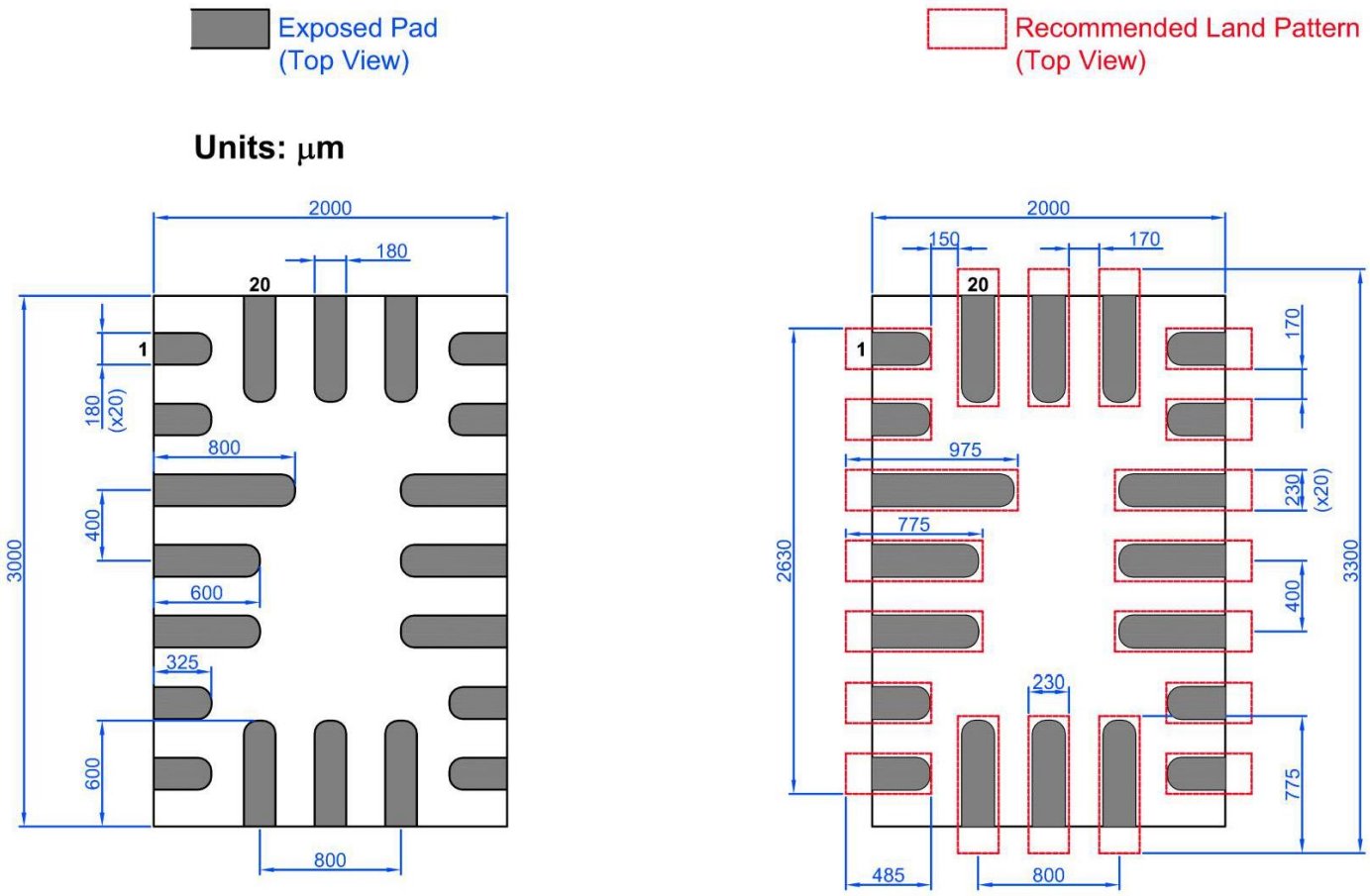
Refer to EIA-481 Specifications



Recommended Reflow Soldering Profile

Please see IPC/JEDEC J-STD-020: latest revision for reflow profile based on package volume of 3.3 mm^3 (nominal).More information can be found at www.jedec.org.

Recommended Land Pattern



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