

ISL62771

Disabling the North Bridge Regulator

TB497  
Rev 0.00  
February 19, 2014

The ISL62771 is a feature rich power supply controller targeted for AMD SVI2 compliant processors that is capable of controlling two independent rails. One of the rails, referred to as the Core regulator, can be configured as either a two-phase regulator or a single-phase regulator. The second rail is a single phase regulator and is referred to as the North Bridge regulator.

Many applications require a single AMD SVI2 compliant power supply that utilizes only one or two phases. The ISL62771 can support these requirements but it lacks an option for disabling the North Bridge regulator so that only the Core regulator is

running. This technical brief describes the method that can be used to effectively disable the North Bridge regulator so that the ISL62771 is controlling a single output.

Figure 1 shows how to configure the ISL62771 with the North Bridge regulator disabled and the Core regulator configured as a two-phase system.

Figure 2 shows how to configure the ISL62771 with the North Bridge regulator disabled and the Core regulator configured as a single-phase system.

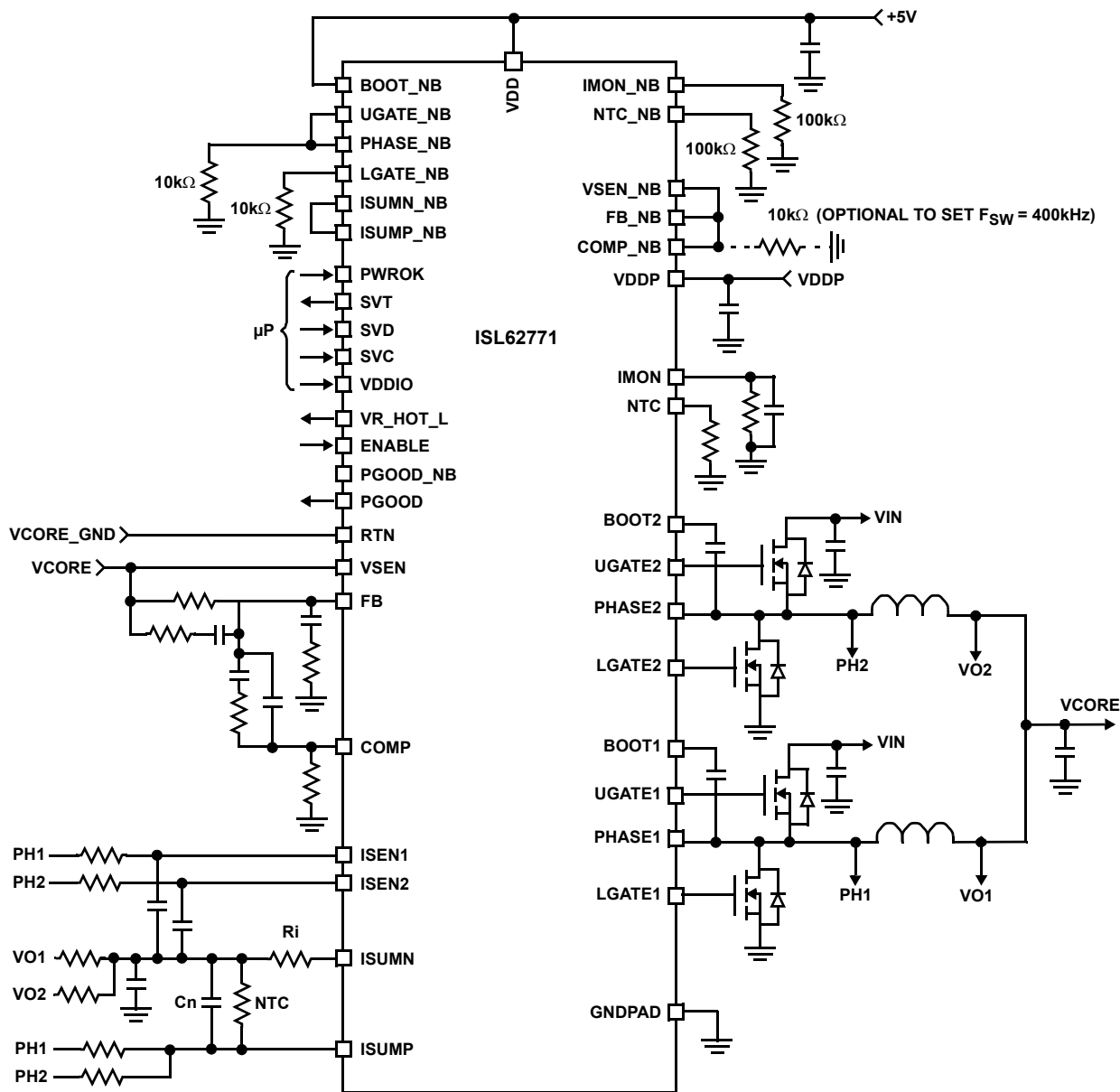


FIGURE 1. TWO-PHASE CORE REGULATOR WITH NORTH BRIDGE DISABLED

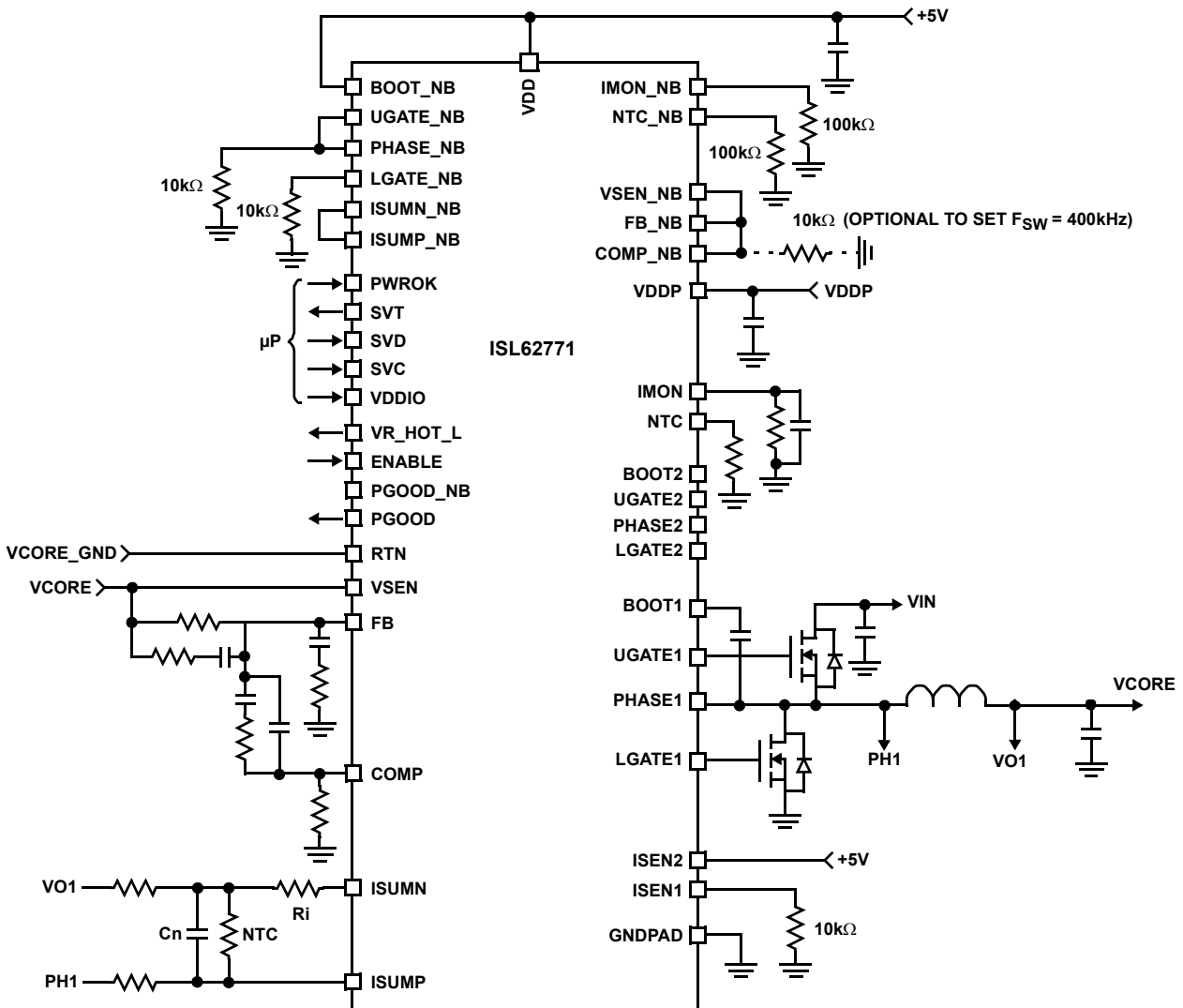


FIGURE 2. SINGLE-PHASE CORE REGULATOR WITH NORTH BRIDGE DISABLED

The Core regulator is configured as either a one- or two-phase system per the instructions given in the ISL62771 datasheet. Whether the Core regulator is configured as a one- or two-phase system, the North Bridge regulator is disabled in the same manner:

1. Short the following pins together: COMP\_NB (pin 36), FB\_NB (pin 37), and VSEN\_NB (pin 38).
2. Short the following pins together: ISUMN\_NB (pin 39) and ISUMP\_NB (pin 40).
3. Tie pin IMON\_NB (pin 2) to ground through a 100k $\Omega$  resistor.
4. Tie pin NTC\_NB (pin 1) to ground through a 100k $\Omega$  resistor.
5. Tie pin BOOT\_NB (pin 31) to pin VDD (pin 25).
6. Tie pin PHASE\_NB (pin 33) to pin UGATE\_NB (pin 32).
7. Tie pin LGATE\_NB (pin 34) to ground through a 10k $\Omega$  resistor.
8. Tie pin UGATE\_NB (pin 32) to ground through a 10k $\Omega$  resistor.
9. Pin PGOOD\_NB (pin 35) can be left floating.

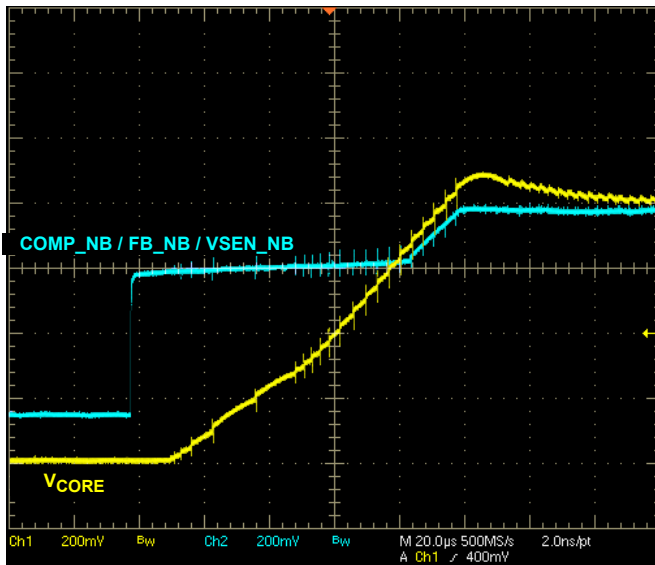
These instructions will yield a system with a switching frequency of 300kHz. In order to obtain a 400kHz switching frequency, the COMP\_NB pin should be tied to ground through a 10k $\Omega$  resistor.

Programming an offset on the Core regulator is accomplished through the prescribed method in the ISL62771 datasheet.

### Behavior of the ISL62771

With the ISL62771 configured as described in this technical brief, the internal circuitry for the North Bridge regulator is not powered down nor is it disabled. All feedback, control, protection, and gate driver circuits are active. Due to this, there is a minor bias current draw for this active circuitry.

The shorting of the COMP\_NB and FB\_NB pins places a unity gain on the North Bridge amplifier. This will force the North Bridge DAC voltage on both of these pins after soft-start. Shorting the VSEN\_NB pin to COMP\_NB and FB\_NB insures that there will be no over or undervoltage events that could shut the regulators down.



**FIGURE 3. STARTUP WITH NORTH BRIDGE DISABLED**

Figure 3 shows how the VSEN\_NB, COMP\_NB, and FB\_NB pins will act during startup. Following startup, these pins will remain at whatever the MetalVID voltage is, unless an SVID command is sent to change the North Bridge DAC value.

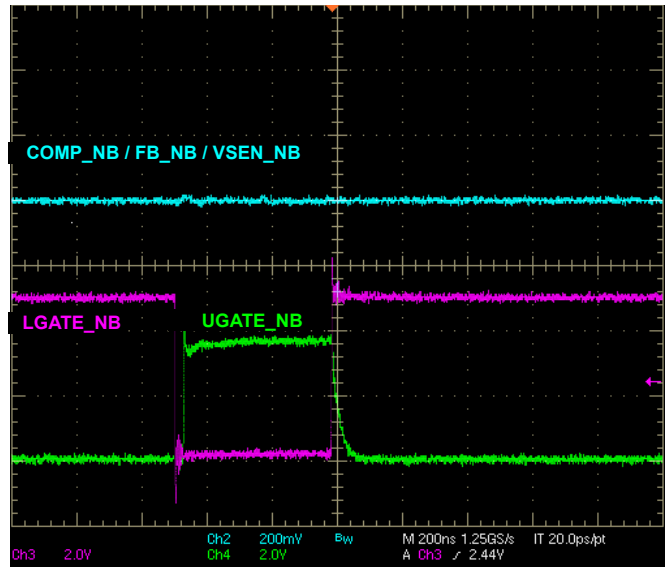
If an SVI command is sent to the ISL62771 that commands the North Bridge DAC to a particular VID level, the COMP\_NB, FB\_NB, and VSEN\_NB pins will ramp to that new VID level, tracking the DAC as it ramps. If an SVI command is never sent to the North Bridge regulator, then the COMP\_NB, FB\_NB, and VSEN\_NB voltages will remain at the MetalVID voltage that was prescribed by the initial SVC and SVD voltages at startup.

Shorting the ISUMP\_NB and ISUMN\_NB pins together will force the current sensing amplifiers to measure a zero load current. As such, there can be no shutdowns due to a sensed overcurrent by the North Bridge circuitry.

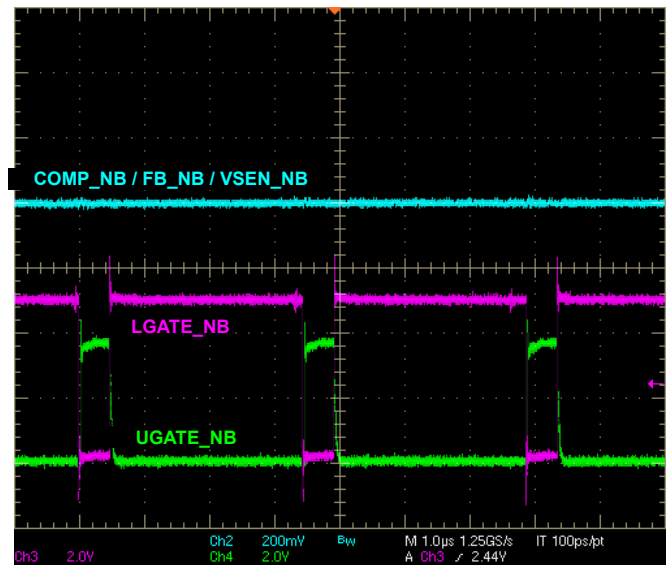
Both the IMON\_NB and NTC\_NB pins are tied to ground through a 100kΩ resistor. These resistors will insure that there will be no overcurrent or thermal shutdown initiated by the North Bridge control circuitry.

The gate drivers for the North Bridge regulator remain active in this configuration. For this reason, the BOOT\_NB pin is tied to VDD so that the upper gate driver retains a bias. The 10kΩ resistors on the UGATE\_NB and LGATE\_NB pins allow for a minimal amount of current to flow through the drivers when turned on. The PHASE\_NB pin is tied to the UGATE\_NB pin to simulate the switching of the PHASE node.

Figure 4 shows what the upper and lower gate signals will look like for the North Bridge regulator in this configuration. Figure 5 shows a number of switching cycles. If an SVI command is sent to the North Bridge regulator and the DAC is changed, the duty cycle of the gate signals will likely change. If the North Bridge DAC is commanded to a low enough voltage, the COMP\_NB signal can fall below the oscillator and switching could halt entirely.



**FIGURE 4. NORTH BRIDGE GATE SIGNALS**



**FIGURE 5. NORTH BRIDGE GATE SIGNALS SHOWING DUTY CYCLE**

**References**

For Intersil documents available on the web, see [www.intersil.com](http://www.intersil.com)

[1] [ISL62771](#) Datasheet

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(Rev.4.0-1 November 2017)



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