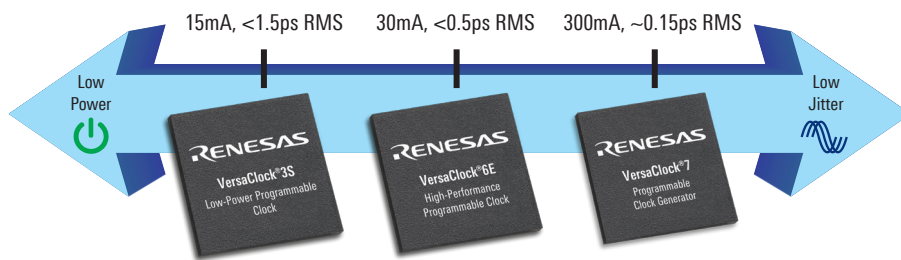# VERSACLOCK® FAMILY OVERVIEW

Renesas' VersaClock® family offers an industry leading portfolio of more than 20 programmable clock generators that provide industry leading versatility for consumer, data communications, telecommunications, and networking applications.

VersaClock devices enable a wide range of applications with a unique combination of low power, flexibility and high performance. These attributes make them ideal candidates for simplifying system design by replacing multiple discrete timing components and reducing bill of materials (BOM).

The VersaClock product family supports operating voltages from 1.8 to 3.3 V, differential (LVPECL/ HCSL/LVDS/LPHCSL) and LVCMOS output types, up to 3 PLLs and multiple fractional dividers to accurately generate virtually any frequency. Products satisfy system requirements from oscillator replacement to PCIe® Gen1 to Gen6 and to communications applications, while consuming very little power.

Ease of use

- Online configuration tool
- Delivery of custom programmed samples from the factory in as little as two weeks
- Software utilities to configure, program, and monitor sophisticated timing devices
- Lab On the Cloud (LOtC) to evaluate phase noise performance on the cloud
- Complete development tool kit with samples

Flexibility

- Programmable through I2C/SPI/SMB
- Configurable output types
- One-time programmable (OTP) memory

Applications

- Computing
  - AI accelerator cards
  - Server and Storage
  - Switches/Routers
  - PCIe Gen 1 to 6
  - Embedded systems
  - USB 3.0/Thunderbolt/RapidIO™
- Consumer
  - Smart devices
  - Set-top boxes
- Communications
  - Broadcast video
  - Gigabit ethernet
- Industrial
- Medical
- Automotive

Key Specifications	VersaClock 3S	VersaClock 6E	VersaClock 7
Core Power (mA)	15	30	300
RMS Phase Jitter (ps) (12k to 20M)	1.5	0.5	0.15
Output Frequency Range (Mhz)	1 to 500	0.001 to 350	0.001 to 650
Architecture	2 Fractional PLL 1 Integer Low Power PLL DCO	1 PLL with 4 Fractional Output Dividers	3 Fractional Output Divider 4 Integer Divider APLL DPLL
Package Size	3 x 3 mm 20-QFN 4 x 4 mm 24-QFN	4 x 4 mm 24-LGA 4 x 4 mm 24-QFN 5 x 5 mm 40-QFN 6 x 6 mm 48-QFN	5 x 5 mm 40-QFN 6 x 6 mm 48-QFN 5 x 5 mm 40-LGA 6 x 6 mm 48-LGA
VDD	1.8 | 2.5 | 3.3V Supported by different product options	1.8 | 2.5 | 3.3V	1.8 | 2.5 | 3.3V
Software Tool	Timing Commander	Timing Commander	RICBox

VERSACLOCK® FAMILY OVERVIEW

VersaClock Family Selector Guide

VersaClock 7 Family

Clock Generator

Part Number	# of Outputs	Internal Crystal	VDD Core VDD IO	Output Frequency	Output Types	Package
RC21008A	8 Universal Pairs*	No	1.8V to 3.3V	0.001 – 650MHz	LPHCSL LVCMOS LVDS AC-LVPECL	5 x 5 mm QFN
RC21008AQ	8 Universal Pairs*	Yes				5 x 5 mm LGA
RC21012A	12 Universal Pairs*	No				6 x 6 mm QFN

Jitter Attenuator

Part Number	# of Outputs	Internal Crystal	VDD Core VDD IO	Output Frequency	Output Types	Package
RC31008A	8 Universal Pairs*	No	1.8V to 3.3V	0.001 – 650MHz	LPHCSL LVCMOS LVDS AC-LVPECL	5 x 5 mm QFN
RC31008AQ	8 Universal Pairs*	Yes				5 x 5 mm LGA
RC31012A	12 Universal Pairs*	No				6 x 6 mm QFN

VersaClock 3S Family

Part Number	# of Outputs†	Internal Crystal	VDD Core	VDD IO	Output Frequency	Output Types	Package
5P35021**	2 Universal Pairs* 1 LVCMOS	No	3.3V	1.8, 2.5, 3.3V (LVCMOS) 2.5, 3V (LVPECL, LVDS, LPHCSL)	LVCMOS: 1 to 160 MHz Differential: 1 to 500 MHz	LVCMOS LVPECL LVDS LPHCSL	3 x 3 mm 20-QFN
5P35023**	2 Universal Pairs* 3 LVCMOS	No					4 x 4 mm 24-QFN 4 x 4 mm 24-WFQFN** (Wettable Flank)
5L35021	2 LPHCSL Pairs 1 LVCMOS	No	1.8V	1.8V	1 to 125 MHz	LVCMOS LPHCSL	3 x 3 mm 20-QFN
5L35023	2 LPHCSL Pairs 3 LVCMOS	No					4 x 4 mm 24-QFN
5X35023	2 Universal Pairs* 3 LVCMOS	Yes	3.3	1.8, 2.5, 3.3V (LVCMOS) 2.5, 3.3 (LVPECL, LVDS, LPHCSL)	LVCMOS: 1 to 160 MHz Differential: 1 to 500 MHz	LVCMOS, LVPECL LVDS, LPHCSL	4 x 4 mm 24-QFN

VersaClock 6E Family

Part Number	# of Outputs†	Internal Crystal	VDD Core VDD IO	Output Types Frequency	Output Types	Package
5P49V60**	4 Universal Pairs*	No	1.8 to 3.3V	LVCMOS: 0.001 to 200 Mhz Differential: 0.001 to 350 Mhz	LVCMOS LVPECL LVDS HCSL	4 x 4 mm 24-WFQFN (Wettable Flank)
5P49V6965						4 x 4 mm 24-QFN
5P49V6967	3 Universal Pairs* 4 LPHCSL Pairs	No				
5P49V6968	3 Universal Pairs* 8 LPHCSL Pairs	No			LVCMOS LVPECL LVDS HCSL LPHCSL	5 x 5 mm 40-QFN
						6 x 6 mm 48-QFN
5P49V6975	4 Universal Pairs*	Yes	1.8 to 3.3V	LVCMOS: 0.001 to 200 MHz Differential: 0.001 to 350 MHz	LVCMOS, LVPECL LVDS, HCSL	4 x 4 mm 24-LGA

*Configurable to differential or LVCMOS   **AEC-Q100 qualified   †All devices have one reference output

To request samples, download documentation or learn more visit: **renesas.com/versaclock**